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EMI MODELING AND REDUCTION FOR POWER ELECTRONICS SYSTEM WITH SIC DEVICES IN ELECTRIC VEHICLE (EV) AND MORE ELECTRIC AIRCRAFT (MEA) APPLICATIONS

By

Boyi Zhang

May 2021

Chair: Shuo Wang
Major: Electrical and Computer Engineering

Wide bandgap power semiconductor devices have been increasingly desirable due to low switching loss and high power density. However, their faster switching speed and abilities to operate at higher frequency brought new challenges, especially for high-power applications. Combined with the parasitic inductance in the package, large current and voltage oscillations during switching transient will increase switching loss, electromagnetic interference (EMI), and high voltage stress on power semiconductor devices. At the same time, fast switching speed will induce undesirable spikes in the driver loop. The induced voltage spikes could falsely turn on the power devices and lead to dangerous shoot-through scenarios. In addition, with high speed and high operation frequency, the radiated EMI noise in the WBG power device applications are more severe compared to the one with Si power devices. The radiated EMI noise could cause the power electronics system to fail EMI standards. In this dissertation, the electromagnetic interference issues in power electronics systems with WBG power devices are discussed. This research aims to model and reduce the EMI issues in the
power electronics system from three aspects: power module packages, power electronics drivers, and power electronics systems with cables. This dissertation proposed a parasitic inductance model that accurately predicts the total parasitic inductance in the power module. The normally neglected mutual inductance between paralleled devices is modeled with the proposed model. Based on the proposed model, an evaluation process that combines the analytical circuit model and finite element analysis (FEA) software is proposed that could help optimize the power module package. With the proposed technique, optimized layout structures are proposed that could reduce the voltage overshoot, EMI, and dynamic current unbalance without increase any fabrication difficulty. Other than package improvement, a Miller capacitance cancellation technique is proposed to address the crosstalk and Miller platform issues in bridge-leg configuration. Finally, a three-phase motor drive system with SiC inverter power module is modeled. The radiated emission source is modeled.
CHAPTER 1
INTRODUCTION

1.1 Application Background

With the development of electricity application, power electronics has become a key factor of power conversion, from low power applications like phone chargers to high power applications like grid-tied converters. Power electronics act as bridges between different voltage and current levels. Among the numerous uses of power electronics, electric vehicles (EV) and aviation are a booming industry and possess lots of research opportunities.

![Figure 1-1 Power electronics in an electric vehicle [1]](image)

As shown in Figure 1-1, power electronics play a vital role in EV’s whole system. Power converters like buck converter change the high DC voltage from the battery array to different low voltage levels for various onboard electronic loads. Bi-directional converters transfer power from the battery to the electric motor. At the same time, when electric energy is transferred from motion energy, like during brakes, the bidirectional converter will also generate current to charge the batteries. The inverter between the battery array and the electric motor could generate AC current from the high DC voltage and drive the electric motor to provide torque and controls the speed.
The above-mentioned power electronics converters and inverters are usually packaged in the form of power modules like Figure 1-2. Power semiconductor devices are enclosed inside the module; silicone gel is usually applied inside for insulation and heat dissipation.

Figure 1-2. Power modules used in electric vehicles a) CREE 1200 V / 50 A all SiC half-bridge module b) SiC half-bridge power module by RHOM, c) half-bridge inverter from Mitsubishi, d) three-phase inverter from Mitsubishi

With the development of power electronics, high efficiency and high power density have always been the goal, as shown in Figure 1-3. To realize the goal, new power semiconductor devices have been developed with the ability to switch at a fast speed. In this way, switching loss could be reduced. Within the same efficiency requirement, the power electronics system with small switching loss could operate in a higher frequency. The volume and weight of passive components used in the system, such as inductors and capacitors, will be reduced. The passive components in the
power electronics system could take up more than 50% of the total volume. With the volume of the passive components reduced, the power density of the whole system will increase.

![Figure 1-3. Future and trend of power electronics](image)

With the pursuing of high power density and faster speed, the power semiconductor devices are being pushed to the limit of Si material. At the same time, Wide Bandgap semiconductor materials, including SiC and GaN, have presented multiple advantages over Si materials. As shown in Table I-I, WBG materials present a higher critical electric field compared to Si, which enables higher breakdown voltage in the same size. In addition, the higher thermal conductivity of SiC improves high power operation performance. These material properties that used to impair the increase of power density due to limitations of Si have been greatly improved by WBG material.

Because of the higher critical field of Wide Bandgap material, as shown in Table I-I, under the same power rating, WBG power switches usually have a smaller die size
than their Si counterparts. As a result, the input junction capacitors of WBG power devices are usually smaller than Si devices, which enables faster switching speed.

1.2 Popular WBG Power Devices and Their Characteristics

The core of power electronics is switching devices. The switching devices are made with semiconductor materials. As shown in Table 1-1 [2][3], WBG materials have multiple superior properties to Si. As a result, the power semiconductor devices made from WBG materials are becoming more and more popular. WBG materials present a higher critical electric field, higher saturation drift velocity, higher electron mobility (GaN), and higher thermal conductivity (SiC) than Si material. The limits of these properties, which have been the barriers to higher power density design for Si materials, have been greatly elevated by WBG materials.

Table 1-1. Comparison of material properties

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Si</th>
<th>SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap $E_g$ (eV)</td>
<td>1.12</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Critical Field $E_{crit}$ (MV/cm)</td>
<td>0.3</td>
<td>3.5</td>
<td>3.3</td>
</tr>
<tr>
<td>Electron Mobility $\mu_n$ (cm$^2$/V·s)</td>
<td>1500</td>
<td>650</td>
<td>990-2000</td>
</tr>
<tr>
<td>Permittivity $\varepsilon_r$</td>
<td>11.8</td>
<td>9.7</td>
<td>9</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm°C)</td>
<td>1.5</td>
<td>4.9</td>
<td>1.3</td>
</tr>
<tr>
<td>Saturation Drift Velocity (cm/s $\cdot 10^7$)</td>
<td>1</td>
<td>2.7</td>
<td>2.7</td>
</tr>
</tbody>
</table>

With the commercialization of WBG power devices [2], it has been proven in many applications that WBG devices can achieve higher efficiency, higher power
density, and higher temperature withstand ability [6] – [11] than Si devices. However, the high \(dv/dt\) and \(di/dt\) during switching transient, the voltage and current’s high frequency (HF) ringing caused by parasitic inductance, as well as high operating frequency raise the concern of electromagnetic interference (EMI). Meanwhile, the high switching speed and the unique structures of WBG devices also cause power converter reliability issues. As an inevitable design consideration, EMI issues must be addressed properly. Otherwise, the benefits of WBG power devices will be compromised. In this Section, the popular WBG devices, including WBG diodes, MOSFETs, and HEMTs are discussed.

![Figure 1-4. Structures of power diodes. (a) PiN junction diode and (b) Schottky barrier diode](image)

The structures of power diodes are shown in Figure 1-4. Figure 1-4 (a) shows the structure of a PiN junction diode. The large concentration of free carriers in the drift region of the PN junction diode provides a low on-state voltage drop. However, to switch
the diode from an on-state to voltage blocking state, these free carriers must be removed. A large reverse current will occur before the PN junction diode can block voltage, which is known as the reverse recovery current [8]. The reverse recovery current during the diode’s hard switching process causes switching power loss as well as EMI [10]. Si Schottky barrier diode (SBD) was designed to eliminate the reverse recovery currents.

Schottky barrier diodes, as shown in Figure. 1-4 (b), applies a Schottky metal layer at the anode. Using SBDs could potentially eliminate the reverse recovery current. However, a thick, lightly doped drift region must be used to block reverse voltage. Consequently, the drift region will cause a resistive forward voltage drop. To keep the on-resistance low, the drift region of the Si Schottky diode should be very thin. As a result, the breakdown voltage becomes a limitation of Si Schottky diodes.

On the other hand, SiC material presents a huge advantage in this case. As in Table I-I, due to its high critical field, SiC SBD could have a thinner drift region than Si SBDs under the same breakdown voltages. This leads to smaller resistance and lower forward voltage. Under the same breakdown voltage requirement, the drift region for the diodes made of SiC material has nearly 2000 times smaller on-resistance than that for the diodes made of Si material. Meanwhile, for the same on-resistance, the SiC SBDs have a much higher breakdown voltage than Si SBDs, so they are suitable for high power applications. As a result, the SiC SBDs have become a promising replacement for Si PN diodes. It is shown that the SiC SBD has the lowest EMI. However, as stated
in [10], the benefit of EMI reduction by replacing Si diode with SiC SBD is limited. This is because the EMI performance of the whole system is not only determined by diodes but also other semiconductor switches and parasitic parameters.

![Power Switches Diagram](image)

Figure 1-5. Structures of power switches. (a) Power MOSFET and (b) Junction capacitance in a power switch and (c) Power HEMT

The most popular power switches made with WBG materials are SiC MOSFETs [9] and GaN HEMTs [2]. The structures of SiC MOSFET and GaN HEMT are shown in Figure. 1-5. The drift region of WBG power switches is usually narrower than that of their Si counterparts with the same power ratings. With an acceptable on-resistance, the switching device made with WBG material has a much smaller die size than Si devices.
under the same breakdown voltage requirement. With a smaller die size, the junction capacitance of WBG devices, as shown in Figure. 1-5 (b), is smaller than Si devices.

Cgs, Cgd, and Cds of commercial SiC MOSFET and GaN HEMT are compared with those of Si MOSFET at the same power ratings (1200 V / 20A, 600 V / 60 A) and packages in TABLE 1-2.

Table 1-2. Comparison of the parasitic capacitance of Si IGBT, SiC MOSFET, and GaN HEMT

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Power Rating</th>
<th>Input Capacitance</th>
<th>Output Capacitance</th>
<th>Reverse Transfer Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC MOSFET (SCT20N120)</td>
<td>1200 V / 20A</td>
<td>650 pF</td>
<td>65 pF</td>
<td>14 pF</td>
</tr>
<tr>
<td>Si MOSFET (IXFX 20N120)</td>
<td>1200 V / 20A</td>
<td>7400 pF</td>
<td>550 pF</td>
<td>100 pF</td>
</tr>
<tr>
<td>GaN HEMT (IGLD60R070D1)</td>
<td>600 V / 60A</td>
<td>380 pF</td>
<td>72 pF</td>
<td>0.3 pF</td>
</tr>
<tr>
<td>Si MOSFET (SiHG70N60AEF)</td>
<td>600 V / 60A</td>
<td>5348 pF</td>
<td>238 pF</td>
<td>7 pF</td>
</tr>
</tbody>
</table>

During switching transient, the junction capacitances along with the gate resistors contribute to the time constant, which determines the switching speed of the device.

With smaller junction capacitances, WBG devices are able to switch at a higher speed.
than Si MOSFETs. As shown in Figure. 1-6, the turn-on and turn-off time of GaN HEMT are much shorter than Si MOSFET.

Because of the reduced on-resistance and increased switching speed, the switching and conduction power loss of WBG devices can be reduced. As a result, WBG devices can operate at a higher frequency than Si devices.

![Figure 1-6 Switching waveforms comparison between GaN HEMT and Si MOSFET during (a) turn on and (b) turn off](image)

Another major advantage of WBG materials is that WBG devices have the potential to operate under much higher temperatures [21]. The maximum allowed temperature of SiC and GaN can be as high as 600 °C. In comparison, the maximum allowed temperature of Si is around 150 to 300 °C. However, the devices made from a WBG material normally have lower maximum allowed temperature limits than the material itself due to the limitation of packaging techniques. The typical maximum allowed temperature of SiC MOSFET, and GaN HEMT is 150 °C to 175 °C. But it should
be noted that power devices made from WBG materials have the potential to endure higher temperatures.

In general, WBG devices have four advantages over their Si counterparts: 1) smaller reverse recovery current and reverse recovery time, 2) faster switching speed, and 3) higher operating frequency. These three factors are good for high-efficiency and high-density design. However, from an EMI perspective, these characteristics will have a negative impact on system reliability and radiated EMI.

1.3 Research Motives and Objectives

The EMI issues in power electronics systems with WBG power devices are caused by different reasons.

Firstly, combined with the parasitic parameters inside the package, the fast switching speed will cause voltage overshoot and oscillation during device switching off transient, as shown in Figure 1-7.

![Figure 1-7](image-url)

Figure 1-7 Measured drain to source voltage during the device turn-off transient. (a) SiC half bridge module switching at 600 V/100 A and (b) GaN half bridge module switching at 400V/100 A
As shown in Figure 1-7, when the power device is turning-off, the voltage between the drain and the source of the power device increases. The current flowing through the power device decreases. During this transient, the magnetic energy stored in the parasitic inductance in the power module causes the voltage to rise higher than the DC voltage, which is also known as the overshoot voltage. After that, this energy transfers between the parasitic inductance and the junction capacitance of the power devices. An oscillating voltage can be observed between the drain and source of the power device. The high voltage overshoot and oscillation will cause additional voltage stress on the power device. At the same time, the long oscillation time will increase switching loss. The high-frequency ringing will increase EMI. The voltage overshoot and oscillation are caused by the parasitic inductance inside the power module package. Therefore, to reduce the EMI caused by the voltage ringing, the parasitic inductance inside the package should be accurately modeled first and then reduced.

Secondly, the fast switching speed of power semiconductor devices will cause the interaction between the main power loop and the drive loop. The fast switching speed generates high $di/dt$ in the power loop and high $dv/dt$ at the switching node. The drive loops of power devices, on the other hand, have relatively low power.
For example, the 1200 V / 30 A SiC MOSFETs are driven with 15 V / 0.5 A driver. The high di/dt and high dv/dt could couple to the drive loop through the inductive and capacitive coupling, also known as the crosstalk effect. Because of the high power of the power loop, even a small portion of coupling could induce a large voltage in the drive loop, which could lead to a device falsely turned on. As shown in Figure 1-8, when top switch S1 is being turned on, bottom switch S2 is kept off. During switching
transient, because of the high switching speed, the voltage will be induced in the drive loop of S2. When the gate to source voltage is higher than the threshold, the bottom switch S2 will be turned on, shoot-through will happen. Shoot through of the power devices is very dangerous because a large current will shoot between the terminals of the DC source. As shown in Figure 1-8 (b), the power devices can be destroyed by the shoot-through current. In practice, the false turn-on should be avoided by all means.

![Figure 1-9 Illustrations of Miller effect. (a) Miller plateau and (b) sustained oscillation caused by false triggering](image)

The coupling between the power loop and the drive loop causes the gate voltage to be clamped at a constant value for a period of time during switching transient, as shown in Figure 1-9. This period of time is also known as the Miller plateau [2]. The Miller plateau determines the switching speed of the device.

The third issue is electromagnetic interference brought by the fast switching speed and high operating frequency, as shown in Figure 1-10.

If the switching waveform is regarded as a trapezoidal waveform, the spectrum can be calculated and plotted as Figure 1-10. It is obvious that with the increasing
switching speed and frequency, the magnitude of the noise spectrum is higher. At the same time, the high-frequency oscillation caused by large parasitic inductance will lead to spikes in the high-frequency region. As a result, for power modules featuring high-speed power semiconductor devices, both conductive EMI and radiated EMI are major concerns. If EMI is higher than standards, a larger filter must be designed, which will increase the system volume.

Figure 1-10 Comparison for different switching speed and operation frequency. (a) Time domain comparison, (b) spectrum comparison.
The power electronics systems need to pass EMI standards before production. Based on the application, different EMI standards are used. For example, CISPR 25 for electric vehicle applications, DO-160 for aviation applications, MIL-STD-461G for military applications. A typical EMI testing setup is shown in Figure 1-11 (a). The radiated EMI measurement setup is shown in Figure 1-11 (b). In this dissertation, the...
radiated emission (RE) is focused on because the conductive emission (CE) has been discussed thoroughly in previous studies.

In this dissertation, the objective is to model and reduce the EMI in power electronics systems with WBG power devices. The EMI caused by parasitic package parameters, device junction capacitance as well as the attached cables are investigated. Techniques that could reduce the EMI are proposed. The objective of this dissertation is to reduce the EMI in the power electronics systems with WBG power devices while taking into design considerations such as power loss, feasibility, and cost. In this way, the full potential of WBG power devices can be realized.
CHAPTER 2
PARASITIC INDUCTANCE MODELING AND REDUCTION FOR WIRE-BONDED HALF-BRIDGE SiC MULTICHIP POWER MODULES

2.1 Introduction of Chapter 2

Among WBG power devices, SiC MOSFETs have characteristics such as high breakdown voltage, high operating temperature, and low switching power loss, so they are widely used to replace Si IGBTs in high power applications such as electric vehicles and the aviation industry. Due to the limited current capability of a single SiC MOSFET chip [31][32], the paralleled multichip structure is typically adopted in SiC MOSFET packages. The wire-bonded direct bond copper (DBC) packing technology is the most popular in multichip power modules. However, the bond wires and 2D layout have large parasitic inductance resulting in severe voltage overshoots and oscillations at high di/dt switching. This leads to high switching power loss, high voltage stress, and electromagnetic interference (EMI) issues [30][59][60].

The parasitic inductance in power modules has been modeled in many papers. In [35], the current commutation loop (CCL) is used to model parasitic inductance, and the switching cell concept is used in the reduction of the CCL loop area and the parasitic inductance. The loop inductance model was also used in [37] to develop a multiloop design technique in multilayer PCB prototypes. However, the mutual inductance between paralleled current path segments is not included in the model. The parasitic inductance is extracted via finite element analysis (FEA) software in [38][53] for the simulations of the voltages and currents outside the module. [38] shows that the
simulated overshoot is 14% smaller than the measured. A measurement-based parasitic inductance extraction technique is proposed in [54] for multichip power modules. The parasitic inductance of each parallel path segment was measured using an impedance analyzer. However, the mutual inductance between parallel path segments is still not modeled. A detailed parasitic inductance model that includes mutual inductance was developed in [37] for the planar bus bar of an IGBT H bridge. The relationship between current paths and parasitic inductance was firstly illustrated in a bus bar, but the mutual inductance between the parallel current path segments inside multichip power modules has not been thoroughly investigated.

The reduction of parasitic inductance is mostly realized by reducing the CCL area. Some general design guidelines were summarized in [35]. [36] adopted the switching cell concept in [35] to reduce the parasitic inductance. Bond wires and the planar hybrid structure were proposed in [48]. PCB and DBC hybrid structures were proposed in [45] and [49] – [51]. Mutual inductance between the partial inductance of the same power loop is analyzed in [45] and [49] – [51]. A twisted loop structure is designed to reduce loop inductance. However, the mutual inductance between parallel power loops is not considered. The mutual inductance between the driving loop and the power loop is investigated in [45]. It is discovered in [46] that interleaving half-bridge (HB) units can reduce parasitic inductance, but the resulting structure requires a complicated bus bar design with DC capacitors on each unit. The mutual inductance between loops was discussed in [37] for multilayer PCB trace loop design but not for 2D
power module design. [34] [48] [40] - [44] showed that planar and 3D structures could reduce parasitic inductance by eliminating bond wires, but they significantly increase the fabrication difficulty. The DBC with a wire-bonded structure is still the most economical and suitable package technology for SiC multichip power modules at this time.

![Commercial SiC multichip power module layout](image)

Figure 2-1 Commercial SiC multichip power module layout: (a) top view with the case and terminals hidden, (b) schematic with parasitic inductance.

Different from the above techniques, the mutual inductance among the parallel current path segments will be investigated in this paper. A parasitic inductance model is developed to predict voltage overshoots and oscillations during switching transients. A wire-bonded package layout is proposed to reduce parasitic inductance based on the developed model.
2.1 Develop the Parasitic Inductance Model

A commercial HB SiC multichip power module layout is shown in Figure.2-1 (a). The module has a maximum power rating of 1200 V / 300 A. There are two cells in parallel. In each cell, both top and bottom switches have three parallel SiC MOSFET and three antiparallel SiC Schottky diode chips. There are equivalently six HBs in parallel. The gate drivers are connected to high gates (HG) and high source (HS), and low gates (LG), and low source (LS) pins. The schematic is in Figure.2-1 (b). In Figure. 2-1 (a), the output terminal branches are not in CCL, so its parasitic inductance will not be analyzed.

In Figure. 2-1 (a), each paralleled HB consists of three current path segments labeled with red, black, and green. Figure. 2-2 shows the side view. For clarity, gate drive loops and gate resistors are hidden. Different materials are labeled with different colors. Because the copper plane that connects to the negative terminal (N) overlaps the copper plane that connects to the output terminal OUT, a different color (brown) is used for the overlap. As shown in Figures. 2-1 and 2-2, the 1st path segment (red arrow) with inductance Ld is from positive terminal (P) to the DBC copper plane and to the drains of top switches and the cathodes of top diodes. The 2nd path segment (black arrow) with inductance LO is from the bond wires to the DBC copper plane, to the output terminal OUT, the drains of low switches, and the cathodes of low diodes. Finally, the 3rd path segment (green arrow) with inductance LS is from the bond wires to the DBC copper plane and to terminal N. A partial and mutual inductance modeling
technique is used in this paper to model the total parasitic inductance. The inductance is calculated based on the self-inductance of each path segment and the mutual inductance between each pair. As in Figure 2-1 (a), the current paths for each paralleled HB are different.

![Diagram](image)

Figure 2-2 Illustration of the three conduction path segments of the current commutation loop inside the power module with a side view.

To investigate the mutual inductance between paralleled path segments, a model is developed in Figure 2-3. Points P, A, and B have voltage potentials $V_0$, $V_1$, and $V_2$ on a copper plane. The mutual inductance between current path segments $\overrightarrow{PA}$ and $\overrightarrow{PB}$ can be calculated as:

$$M_{12} = \iiint \mu_0 H_1 H_2 \cos \theta \, dV \quad (2-1)$$

Where $H_1$ and $H_2$ are the magnetic field generated by $I_1$ and $I_2$ respectively and the position angle between $\overrightarrow{PA}$ and $\overrightarrow{PB}$ is $\theta$.

In a traditional multichip power module in Figure 2-1 (a), the paralleled chips are very close to each other, and the parallel current segments share the same conductors such as copper planes and some bond wires. As a result, the angles between any two are very small, leading to large mutual inductance.
Figure 2-3 Current paths on a copper plane with one input and two outputs: (a) current paths and (b) simulated current vectors.

Figure 2-4 Self and mutual inductance of paralleled HB $i$ and $j$.

In the inductance model in Figure 2-4, $L_{di}$, $L_{oi}$, and $L_{si}$ are the self-inductance of the three path segments of the HB $i$ in Figure 2-2, respectively. The mutual inductance
\( M_{(d,o,s)i(d,o,s)j} \) between any two path segments of HB \( i \) and \( j \) are also shown in Figure 2-4.

Because the drains of switches are bonded on a low impedance DBC copper plane connected to OUT, there is no inductance between the drains. The induced voltages across different inductances during switching transients are different because the parasitic self and mutual inductances of each path segment are different. Each HB includes a top and a bottom branch. The voltage difference between parallel branches leads to inter-branch current in Figure 2-4, resulting in an unbalanced dynamic current:

if the currents flowing through the top and bottom switches of the \( i^{th} \) and \( j^{th} \) HBs are represented with \( i_{di}, i_{si}, \) and \( i_{dj}, i_{sj}, \) because of the inter-branch current, they are not equal. In Figure 2-4, the parasitic inductance can be represented with self and mutual inductance matrices \( L_i \) and \( M_{ij}: \)

\[
L_i = \begin{bmatrix}
L_{di} & M_{dloi} & M_{disi} \\
M_{olidi} & L_{oi} & M_{sloi} \\
M_{sidi} & M_{oisi} & L_{si}
\end{bmatrix}
\]

\[
M_{ij} = \begin{bmatrix}
M_{didj} & M_{dloj} & M_{disj} \\
M_{olidj} & M_{oloj} & M_{oisj} \\
M_{sijdj} & M_{sloj} & M_{sisj}
\end{bmatrix}
\]

\( L_i \) consists of the self-inductance of each path segment and the mutual inductance between any two path segments within HB \( i \). \( M_{ij} \) consists of all the mutual inductance between any two path segments on HB \( i \) and HB \( j \). During the transient, the voltage drops on the parasitic inductance of the \( i^{th} \) HB is:

\[
\begin{bmatrix}
V_{di} \\
V_{oi} \\
V_{si}
\end{bmatrix} = L_i \cdot \frac{d}{dt} \begin{bmatrix}
i_{di} \\
i_{si}
\end{bmatrix} + M_{f1} \cdot \frac{d}{dt} \begin{bmatrix}
i_{d1} \\
i_{s1}
\end{bmatrix} + \ldots + M_{ij} \cdot \frac{d}{dt} \begin{bmatrix}
i_{dj} \\
i_{sj}
\end{bmatrix}
\]

(2-4)
The transient responses of the power module can be discussed based on the inductance model in the analysis below.

2.2.1 Turn-off Transient Analysis

The turn-off transient of the top switches is firstly analyzed. Figure 5 (a) shows the turn-off transient of the ith HB in four stages. $L_{wire}$ is the inductance of the conductors between the DC source and the DC-link capacitors. ESL and ESR are the equivalent series inductance and resistance of the DC capacitors CDC, respectively. $L_{lead}$ is the parasitic inductance of the interconnections such as lead wires, PCB traces and the external bus bar between the DC capacitors and the module terminals. The physical structure which results in $L_{lead}$ is shown later in Figure 8. The inductive couplings between $L_{lead}$ and the CCL segments inside the module is very small so they can be ignored.
Figure 2-5 (a) The turn-off transient waveforms of the top switch and the equivalent circuits during: (b) stage 1, (c) stage 2 and 3 (d) stage 4.

**Stage 1:** before top switches are turned off \((< t_0)\).

In Figure 2-5 (b), the load current \(I_L\) is the sum of the current \(i_{di}\) in all branches.

The currents are given by:

\[
\sum_{i} i_{di} = I_L \tag{2-5}
\]

\[
i_{s1} = i_{s2} = \ldots = i_{sj} = 0 \tag{2-6}
\]

In multichip power modules, the current in each branch is nearly equal to \(I_L/j\) at the steady-state and \(I_L\) is constant due to the large load inductance.

**Stage 2:** before Miller plateau \((t_0 - t_1)\).

The gate voltage \(V_{gsi}\) of top switches decreases after the driving signal switches from high \(V_H\) to low \(V_L\). The drain to source voltage \(V_{dsi}\) of the top switches is still low.

The MOSFET operates in the Ohmic region. The drain current is given by:

\[
i_{chi} = i_{di} = K_m (V_{gsi} - V_{thi})V_{dsi} \tag{2-7}
\]
Where $i_{ch1}$ and $V_{th1}$ are the channel current and top switch threshold voltage in the ith HB; $K_m$ is transconductance in A/V2. $i_{di}$ is controlled by $V_{gs1}$, not affected by the parasitic inductance.

**Stage 3:** voltage rising stage ($t_1 - t_2$).

At $t_1$, the drain to source voltage of the top switches rises, and the gate voltage reaches the Miller plateau. The MOSFETs operate in the saturation region. $g_m$ is transconductance in A/V.

\[
\begin{align*}
    i_{ch1} &= g_m(V_{gs1} - V_{th1}) \quad (2-8) \\
    i_{di} &= i_{ch1} + C_{ossi1} \frac{dv_{dsi}}{dt} \quad (2-9) \\
    C_{ossi1} &= C_{gdi1} + C_{dsi1} \quad (2-10) \\
    i_{gi} &= C_{gdi1} \cdot \left( \frac{dv_{gs1}}{dt} - \frac{dv_{dsi}}{dt} \right) + C_{gs1} \frac{dv_{gs1}}{dt} \quad (2-11) \\
    i_{si} &= -C_{ossi2} \frac{dv_{dsi}}{dt} \quad (2-12) \\
    C_{ossi2} &= C_{gdi2} + C_{dsi2} \quad (2-13)
\end{align*}
\]

At Miller plateau, $dV_{gs1}/dt \approx 0$, from (2-11):

\[
\frac{dv_{dsi}}{dt} = -\frac{i_{gi}}{C_{gdi}} \quad (2-14)
\]

The gate current $i_{gi}$ and Miller voltage $V_{Miller}$ are given by:

\[
\begin{align*}
    i_{gi} &= \frac{V_L - V_{gs1}}{R_{gi}} \quad (2-15) \\
    V_{Miller} &= V_{gs1} = \frac{i_L}{g_m} + V_{thi} \quad (2-16)
\end{align*}
\]

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Where $R_{gi}$ is the gate resistance of the top switch of the $i^{th}$ HB. From (2-8) (2-9) (2-12) (2-14) and (2-15), during the Miller plateau period, $\frac{dV_{dsi}}{dt}$, $i_{di}$, and $i_{si}$ are constant [30]. The drain current of the $i^{th}$ HB is given by:

$$i_{di} = I_{const} = \frac{I_L}{j} + i_{si}$$

(2-17)

The $i_{si}$ is negative during this stage, as shown in (2-12). Therefore, the drain current is a constant value smaller than $\frac{I_L}{j}$, as shown in Figure. 2-5 (a). Because the parasitic inductance is much smaller than the load inductor, it has little impact on the device current.

**Stage 4:** ringing stage ($> t_2$)

In Figure. 2-5 (d), the ringing stage starts when the bottom diodes start to conduct currents ($i_{si}<0$), which bypass the bottom switches. The magnitude of the ringing depends on the initial current in parasitic inductance and the initial voltage of the output capacitance.

In Figure. 2-6 (a), $R_{di}$ and $R_{si}$ are total the resistance of the path segments and the diode which $i_{di}$ and $i_{si}$ flowing through. The impedance of the DC link capacitor is in parallel with the power module. In practice, the DC link capacitors, including high frequency (HF) film and ceramic capacitors with small ESL and ESR, are directly mounted on the power module’s P and N terminals. The DC link capacitors can thus provide a small impedance to HF currents and decouple the power module from the DC
source, so the frequency domain circuit without $L_{\text{wire}}$ and $V_{\text{DC}}$ in Figure 2-6 (b) will be analyzed later.

![Equivalent circuits during the ringing stage: (a) time domain and (b) frequency domain.](image)

In Figure 2-6 (b), the initial currents in the parasitic inductances and initial voltages on output capacitances are represented with equivalent voltage sources $V_{1i}$ and $V_{2i}$ for top and bottom branches, respectively.

By solving (2-9), (2-12), (2-14), and (2-17), the initial currents at $t_2$ in the parasitic inductance are:

$$i_{dl}(t_2) = \frac{i_L}{j} + i_{sl}(t_2) \quad (2-18)$$

$$i_{sl}(t_2) = C_{\text{oss}2l} \cdot \frac{V_L - V_{\text{Müller}}}{R_{gl}c_{gd1}} \quad (2-19)$$

The initial voltages on the output capacitance of the top switch can be calculated from Figure 2-6 (a) with KVL:
\[ V_{cl}(t_2) = V_{DC} - [i_{dl}(t_2)R_{dl} + i_{si}(t_2)R_{si} + i_c(t_2)ESR + V_{ESL} + V_{di} + V_{oi} + V_{si}] \] (2-20)

Where,

\[ i_c(t_2) = \sum_{i=1}^{j} i_{di}(t_2) = \sum_{i=1}^{j} i_{si}(t_2) \] (2-21)

\[
\begin{bmatrix}
V_{dl} \\
V_{oi} \\
V_{si}
\end{bmatrix}_{t_2} = L_i \cdot \frac{d}{dt} \begin{bmatrix}
i_{di}(t_2) \\
i_{d1}(t_2) \\
i_{si}(t_2)
\end{bmatrix} + M_{i1} \cdot \frac{d}{dt} \begin{bmatrix}
i_{d1}(t_2) \\
i_{d1}(t_2) \\
i_{s1}(t_2)
\end{bmatrix} + \cdots + M_{ij} \frac{d}{dt} \begin{bmatrix}
i_{di}(t_2) \\
i_{d1}(t_2) \\
i_{si}(t_2)
\end{bmatrix} / dt + \cdots \] (2-22)

\[ V_{ESL}(t_2) = ESL \cdot \frac{di_c(t_2)}{dt} \] (2-23)

With the initial conditions, \( V_{1i} \) and \( V_{2i} \) are calculated from (2-24) and (2-25). ESL only contributes to the initial voltage of the output capacitance, as given by (2-20).

\[ V_{1i} = \left( L_i \cdot \begin{bmatrix}
i_{di}(t_2) \\
i_{di}(t_2) \\
i_{si}(t_2)
\end{bmatrix} \right)^T + \left( M_{i1} \cdot \begin{bmatrix}
i_{d1}(t_2) \\
i_{d1}(t_2) \\
i_{s1}(t_2)
\end{bmatrix} \right)^T + \cdots + \left( M_{ij} \cdot \begin{bmatrix}
i_{di}(t_2) \\
i_{d1}(t_2) \\
i_{si}(t_2)
\end{bmatrix} \right)^T \cdot \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix} + \frac{V_{ci}(t_2)}{s} \] (24)

\[ V_{2i} = \left( L_i \cdot \begin{bmatrix}
i_{di}(t_2) \\
i_{di}(t_2) \\
i_{si}(t_2)
\end{bmatrix} \right)^T + \left( M_{i1} \cdot \begin{bmatrix}
i_{d1}(t_2) \\
i_{d1}(t_2) \\
i_{s1}(t_2)
\end{bmatrix} \right)^T + \cdots + \left( M_{ij} \cdot \begin{bmatrix}
i_{di}(t_2) \\
i_{d1}(t_2) \\
i_{si}(t_2)
\end{bmatrix} \right)^T \cdot \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} \] (25)

Based on Figure. 2-6 (b), the drain-to-source voltages of the top switches are given by (2-26).

\[
\begin{bmatrix}
V_{d1}(s) \\
\vdots \\
V_{dj}(s)
\end{bmatrix}_{t_2} = \begin{bmatrix}
V_{11} + V_{21} \\
\vdots \\
V_{1j} + V_{2j}
\end{bmatrix} - \begin{bmatrix}
V_{d1}(s) + V_{o1}(s) + V_{s1}(s) \\
\vdots \\
V_{dj}(s) + V_{oj}(s) + V_{sj}(s)
\end{bmatrix} - \begin{bmatrix}
I_{d1}(s)R_{d1} \\
\vdots \\
I_{dj}(s)R_{dj}
\end{bmatrix} - \begin{bmatrix}
I_{s1}(s)R_{s1} \\
\vdots \\
I_{sj}(s)R_{sj}
\end{bmatrix} - \begin{bmatrix}
I_c(s) \cdot (s \cdot ESL + ESR) \\
\vdots \\
I_c(s) \cdot (s \cdot ESL + ESR)
\end{bmatrix} \] (2-26)

Where,
\[
\begin{bmatrix}
I_{d1}(s) \\
\vdots \\
I_{dj}(s)
\end{bmatrix} = s
\begin{bmatrix}
C_{oss1} \cdot V_{ds1}(s) \\
\vdots \\
C_{ossj} \cdot V_{dsj}(s)
\end{bmatrix}
\]

\[
\begin{bmatrix}
V_{al}(s) \\
V_{ol}(s) \\
V_{sl}(s)
\end{bmatrix} = L_i \cdot s
\begin{bmatrix}
I_{di}(s) \\
I_{di}(s) \\
I_{si}(s)
\end{bmatrix}
+ M_{i1} \cdot s
\begin{bmatrix}
I_{d1}(s) \\
I_{d1}(s) \\
I_{s1}(s)
\end{bmatrix}
+ \ldots
M_{ij} \cdot s
\begin{bmatrix}
I_{dj}(s) \\
I_{dj}(s) \\
I_{sj}(s)
\end{bmatrix}
\]  

(2-28)

Because of the unbalanced inductance in each parallel HBs, the initial conditions of each HBs are different. The DM current \( I_{DMij} \) flowing between the \( i^{th} \) HB and the \( j^{th} \) HB due to different initial voltages can be calculated as:

\[
I_{DMij}(s) = \frac{V_{2j} - V_{2i}}{s(L_{si} + L_{sj} - 2M_{sisj}) + R_{si} + R_{sj}} + \frac{V_{1i} - V_{1j}}{sL_{dij} + s^2M_{dij} + \frac{1}{sC_{dij}} + R_{dij}}
\]

(2-29)

Where \( L_{dij}, M_{dij}, C_{dij} \) and \( R_{dij} \) represent the sum of the impedance of the current segments where \( I_{di} \) and \( I_{dj} \) flow. \( L_{dij} = L_{di} + L_{oi} + L_{dj} + L_{oj} \), \( M_{dij} = M_{dlo} + M_{djo} - M_{dist} - M_{dist} - M_{dist} - M_{dist} - M_{dist} \cdot C_{dij} = \frac{C_{ossi}C_{ossj}}{C_{ossi} + C_{ossj}} \). \( R_{dij} = R_{di} + R_{dj} \).

For the \( i^{th} \) HB:

\[
I_{si}(s) = I_{di}(s) - I_{DMij}(s)
\]

(2-30)

Because there are \( 3 \times j \) unknown parameters in (2-26) and \( 3 \times j \) equations from (2-26) to (2-30), the voltage and current of each switch can be solved.

2.2.2 Turn-on Transient Analysis

The analysis of turn-on transient is similar to that of the turn-off transient. Figure. 2-7 (a) shows the turn-on transient of the top switch in the \( i^{th} \) HB.
Figure 2-7 Top switch turn-on transient: (a) time-domain waveforms, (b) time-domain equivalent circuit and (c) frequency-domain equivalent circuit

**Stage 1:** before top switches are turned on ($t_3$).

The circuit is the same as Figure. 5 (b). The load current flows through the antiparallel diodes of the bottom switches.

$$\sum_{i=1}^{j} i_{si} = -i_L \quad (2-31)$$

$$i_{d1} = i_{d2} = \ldots = i_{dj} = 0 \quad (2-32)$$

**Stage 2:** current rising stage ($t_3 - t_4$).

During the current rising stage, the circuit is the same as Figure.2-5 (c). The MOSFETs are operating in the saturation region. The channel current is governed by (2-8). The drain to source voltage of the top switches drops due to the power loop parasitic inductance.

$$V_{dsi}(t_3) = V_{DC} - [i_{di}(t_3)R_{di} + i_{si}(t_3)R_{si} + i_{c}(t_3)ESR + V_{ESL}(t_3) + V_{di} + V_{oi} + V_{si}] \quad (2-33)$$
Where,

\[ V_{ESL}(t_3) = ESL \cdot \frac{d(\sum_{i=1}^{L} i_{sl}(t_3))}{dt} \]  \hspace{1cm} (2-34)

\[ V_{di}, V_{oi}, V_{si} \] are governed by (2-4). The voltage drops caused by the parasitic inductance in this stage have little impact on \( i_{di} \).

**Stage 3:** voltage decreasing stage \((t_4 - t_5)\).

After \( i_{di} \) reaches \( I_L/j \), the top MOSFET enters Miller plateau. \( V_{dsi} \) decreases. The decreasing rate is governed by (2-14).

**Stage 4:** current ringing stage \((> t_4)\).

After the MOSFET is on, the channel resistance is \( R_{on} \). \( V_{dsi} \) is very small due to the small \( R_{on} \) of SiC MOSFET. Figure 2-7 (b) shows the time-domain equivalent circuit.

The drain current overshoot during top switch turn-on transient is caused by the initial conditions and reverse recovery charge of the antiparallel diodes of the bottom switches. In the all-SiC power modules, the reverse recovery current is very small [28]. The magnitude of current oscillation largely depends on the initial conditions. Figure 2-7 (c) shows the equivalent frequency-domain circuit. Similarly, the initial voltage on the output capacitance of the bottom switch in the \( f^{th} \) HB is:

\[
V_{cl2}(t_4) = V_{DC} - [i_{di}(t_4)(R_{di} + R_{on}) + i_{si}(t_4)R_{si} + i_{C}(t_4)ESR + V_{ESL}(t_4) + V_{di} + V_{oi} + V_{si}] 
\]  \hspace{1cm} (2-35)

Where,
The voltage and current can be solved by:

\[
\begin{bmatrix}
V_{dl}
\end{bmatrix}
= L \cdot d \begin{bmatrix}
i_{dl}(t_4)
i_{sl}(t_4)
\end{bmatrix}/dt + M_{t1} \cdot d \begin{bmatrix}
i_{d1}(t_4)
i_{s1}(t_4)
\end{bmatrix}/dt + \ldots M_{lj} \cdot d \begin{bmatrix}
i_{dl}(t_4)
i_{sl}(t_4)
\end{bmatrix}/dt
\]  

(2-36)

The equivalent voltage sources are calculated by:

\[
V_{1l} = \left( \left( L \cdot \begin{bmatrix}
i_{dl}(t_4)
i_{sl}(t_4)
\end{bmatrix} \right)^T + \left( M_{t1} \cdot \begin{bmatrix}
i_{d1}(t_4)
i_{s1}(t_4)
\end{bmatrix} \right)^T + \ldots \left( M_{lj} \cdot \begin{bmatrix}
i_{dl}(t_4)
i_{sl}(t_4)
\end{bmatrix} \right)^T \right) \cdot \begin{bmatrix}1
\end{bmatrix} + \frac{v_{a2}(t_4)}{s}
\]

(2-37)

\[
V_{2l} = \left( \left( L \cdot \begin{bmatrix}
i_{dl}(t_4)
i_{sl}(4)
\end{bmatrix} \right)^T + \left( M_{t1} \cdot \begin{bmatrix}
i_{d1}(t_4)
i_{s1}(4)
\end{bmatrix} \right)^T + \ldots \left( M_{lj} \cdot \begin{bmatrix}
i_{dl}(t_4)
i_{sl}(4)
\end{bmatrix} \right)^T \right) \cdot \begin{bmatrix}0
\end{bmatrix} + \frac{v_{a2}(t_4)}{s}
\]

(2-38)

\[
V_{ESL}(t_4) = ESL \cdot \frac{dt_c(t_4)}{dt}
\]

(2-39)

\[
i_c(t_4) = \sum_{i=1}^{j} i_{dl}(t_4) = \sum_{i=1}^{j} i_{sl}(t_4)
\]

(2-40)

The voltage and current can be solved by:

\[
\begin{bmatrix}
V_{ds12}(s)
\vdots
V_{dsj2}(s)
\end{bmatrix} = \begin{bmatrix}
V_{11} + V_{21}
\vdots
V_{1j} + V_{2j}
\end{bmatrix} - \begin{bmatrix}
V_{d1}(s) + V_{o1}(s) + V_{s1}(s)
\vdots
V_{dj}(s) + V_{oj}(s) + V_{sj}(s)
\end{bmatrix} - \begin{bmatrix}
l_{d1}(s) \cdot (R_{d1} + R_{o1})
\vdots
l_{dj}(s) \cdot (R_{dj} + R_{oj})
\end{bmatrix}
\]

(2-41)

\[
\begin{bmatrix}
I_{s1}(s) \cdot R_{s1}
\vdots
I_{sj}(s) \cdot R_{sj}
\end{bmatrix} - \begin{bmatrix}
l_c(s) \cdot (s \cdot ESL + ESR)
\vdots
l_c(s) \cdot (s \cdot ESL + ESR)
\end{bmatrix}
\]

Where,

\[
\begin{bmatrix}
l_{s1}(s)
\vdots
l_{sj}(s)
\end{bmatrix} = s \begin{bmatrix}
C_{oss21} \cdot V_{ds12}(s)
\vdots
C_{oss2j} \cdot V_{dsj2}(s)
\end{bmatrix}
\]

(2-42)

\[
\begin{bmatrix}
V_{dl}(s)
V_{ol}(s)
V_{sl}(s)
\end{bmatrix} = L \cdot s \begin{bmatrix}
l_{dl}(s)
I_{dl}(s)
I_{sl}(s)
\end{bmatrix} + M_{t1} \cdot s \begin{bmatrix}
l_{d1}(s)
I_{d1}(s)
I_{s1}(s)
\end{bmatrix} + \ldots M_{lj} \cdot s \begin{bmatrix}
l_{dl}(s)
I_{dl}(s)
I_{sl}(s)
\end{bmatrix}
\]

(2-43)
\[ I_{DMij}(s) = \frac{v_{2j}-v_{2i}}{s(L_{si}+L_{sj}-2M_{sisj})+Rs_{ij}+\frac{1}{sC_{sij}}} + \frac{v_{1i}-v_{1j}}{sL_{sij}+s^2(2M_{sij})+R_{dij}+R_{onj}+R_{onj}} \] (2-44)

\[ I_{di}(s) = I_{DMij}(s) + I_{si}(s) \] (2-45)

Where \( R_{sij} = R_{si} + R_{sj} \) and \( C_{sij} = \frac{C_{ossij}C_{ossj}}{C_{ossi}+C_{ossj}} \).

2.2.3 Discussion and Model Verification

Although the math model from (2-26) – (2-30) or (2-41) – (2-45) are very difficult to analytically solved, based on the model, the following important analysis and optimization can be conducted: 1) the proposed parasitic inductance model discloses that the switching transient of the power devices is not merely determined by the self-inductance matrices, the ESL of the DC link capacitors and the mutual inductance within one HB as used in existing literatures, but rather by an inductance matrices which includes both self and mutual inductances of parallel branches; 2) the developed model discloses that the magnitudes of voltage and current ringing depend on the self-inductance of each HB branch, the mutual inductance between the HB branches and the ESL of the DC link capacitor because they determine the initial voltage sources; large self-inductance and positive mutual inductance lead to large initial voltage sources (note: \( di/dt < 0 \) in (2-22)); 3) based on (2-24) and (2-25), the SiC module layout can be optimized with negative mutual inductance to cancel the 1\(^{st}\) term of the initial voltage equations, so the proposed layout technique generates negative mutual inductance to reduce initial values to reduce overshoot and ring magnitude; while most other papers focuses on reducing self-inductance within one HB; 4) based on the developed model,
the overshoot and ring magnitude can be reduced by reducing both self and mutual
inductance; 5) The proposed model gives more accurate voltage overshoot and ringing
predictions because the mutual inductance is included as evidenced in Figure. 2-8.

Figure 2-8 Switching waveforms comparison: (a) turn-off transient, (b) turn-on transient,
and (c) simulated turn-on and turn-off transient waveforms based on the
model without mutual inductance.
In this Chapter, the parasitic inductance is extracted with Ansys Q3D in Figure 2-9 (b). The maximum mutual inductance between Llead and the CCL segments inside the module is 1.05 nH, much smaller than the self-inductance (around 20 nH) of each segment of the HB in (46) – (48). Therefore, it can be ignored. The assumption in Section II-B is thus valid.

![Figure 2-9 The SiC power module with the external bus bar: (a) prototype and (b) 3D simulation model.](image)

To show the influence of mutual inductance, the inductance matrices of the left two HBs in Figure 2-2 are shown in (2-46) – (2-48),

\[
L_1 = \begin{bmatrix}
20.73 & -1.22 & -6.12 \\
-1.22 & 21.61 & -4.17 \\
-6.12 & -4.17 & 19.59
\end{bmatrix} \text{ nH} \tag{2-46}
\]

\[
L_2 = \begin{bmatrix}
20.3 & -1.01 & -6.05 \\
-1.01 & 21.58 & -4.19 \\
-6.05 & -4.19 & 19.1
\end{bmatrix} \text{ nH} \tag{2-47}
\]
\[ M_{12} = \begin{bmatrix} 17.74 & -0.93 & -6.1 \\ -1.02 & 9.49 & -4.14 \\ -6.07 & -4.97 & 17.61 \end{bmatrix} \text{nH} \]  

(2-48)

(2-46) and (2-47) are the self-inductance matrices of HB 1 and 2, as defined in (2-2). (2-48) is the mutual inductance matrix, as defined in (2-3). The effects of P and N bus-bar terminals have been included in both self and mutual inductance matrices as all half-bridges share P and N bus-bar terminals. As mentioned, due to the small position angle between two HBs, the mutual inductances are large and positive.

In power modules with a phase leg configuration, the voltage and current oscillations can cause crosstalk. The crosstalk is caused by the capacitive and inductive couplings between the device gate loop and the power loop [28]. The switching of one switch can induce spurious gate voltage on the complementary switch. The capacitive coupling is through the device gate to drain capacitance. When the drain to source voltage changes, a current will be induced across the gate to drain capacitance, causing gate voltage variation. The inductive coupling is through the mutual inductance between the gate loop and the power loop. The current in the power loop induces a voltage in the device’s gate loop. Both voltage and current oscillation contribute to the crosstalk. Serious crosstalk can lead to false turn-ons and negative gate voltage breakdown.

To validate the developed model, the self and mutual inductance matrices are extracted with Ansys Q3D. SiC MOSFETs and Schottky diodes are characterized using the Ansys Simploter device characterization tool. Both static and dynamic characteristics are curve fitted based on the device datasheets. The ESL and ESR of
the DC link capacitors are measured with Keysight E4990A. The drain-to-source voltage of the top SiC MOSFETs on the 1st HB is measured and simulated.

The measured and the simulated turn-on and turn-off switching waveforms match very well in Figures.2-8 (a) (b). On the other hand, the simulation results without the mutual inductance between two HBs in Figures. 2-8 (c) cannot match the measured. The measured turn-off overshoot voltage in Figure. 2-8 (a) is about 120 V, during the turn-off overshoot voltage in Figure. 2-8 (c) is about 70 V. With the proposed model, the transient analysis is much more accurate than the traditional model. The comparison also proves the significance of mutual inductance.

### 2.3 Layout Improvement

Based on the transient analysis in Section II, the magnitude of voltage and current ringing is determined by both the self and mutual inductance matrices. Therefore, the oscillations could be reduced through power module layout optimization. The layout optimization should not only focus on the reduction of the self-inductance but also the mutual inductance. In the self-inductance matrix Li, the self-inductance should be as small as possible, and the mutual inductance should be negative; the mutual inductance in Mij between parallel HBs should be negative or small. Three techniques are used to achieve this. First, both the loop length and area of each HB should be as small as possible. Second, the position angle of corresponding current path segments in parallel HBs should be 180° to achieve negative mutual inductance. Third, the P-N HB
loops should not be overlapped to reduce mutual inductance. In this paper, the DBC layout and the internal bus bar structure are improved.

![Original layout for HB 1 and 2](image1)

![Original internal bus bar structure](image2)

![Equivalent circuit of HB 1 and 2](image3)

Figure 2-10 The original module has large self and mutual inductances between two parallel HBs.

The layout of the two parallel HBs, internal bus bar structure and the equivalent circuit of HB 1 and 2, along with the current path segments and their associated parasitic inductances in the original and the proposed modules, are shown in Figures 2-10 and 2-11 respectively. In the original layout in Figure 11, the top and bottom switches are located in the top and bottom regions of the module; consequently, the current path loop area and the total self-inductance from the P terminal to the N terminal are large for each HB. At the same time, the current path segments share the same path on the internal bus bar. The mutual inductances between current path segments,
such as $L_{d1}$ and $L_{d2}$ are therefore positive and large due to the very small position angle.

Figure 2-11 The proposed module has a small self and mutual inductances between two parallel HBs.

In the proposed layout in Figure 11, the top and bottom switches are very close, so the P-to-N loop is small, and the inductance of every single HB is reduced.

Meanwhile, the corresponding current path segments in two parallel HBs are separated and positioned at a 180° angle on the layout. The current path segments on the internal bus bar are also separated and interleaved. So, the mutual inductance between them is small.

An HB multichip power module with the same power rating as the original commercial module is designed in Figure 2-12. The separated positive and negative terminals are connected with the bus bar in the middle of the module. The distances
between parallel chips and between parallel branches are determined by the heat
dissipation angle [5] and power clearance distance IEC 60664-1. The minimum distance
is determined by the larger distance of the two to avoid heat overlaps or power
breakdown. Drivers are connected by the kelvin connection. The terminal bars that
connect the module to the DC source and AC output are soldered on DBC copper, as in
Figure. 2-10 (b). The terminal locations and layout are the same as the original.

![Figure 2-12](image)

(a) proposed layout design with terminals hidden and (b) proposed module
design with terminals.

The parasitic inductance matrices of the top two HBs in Figure. 2-12 are shown
as (2-49) – (2-51) in comparison to (2-46) – (2-48).

\[
L_{1,p} = \begin{bmatrix}
13.25 & 0.01 & -7.16 \\
0.01 & 1.60 & -0.22 \\
-7.16 & -0.22 & 13.98
\end{bmatrix} \text{ nH} \quad (2-49)
\]

\[
L_{2,p} = \begin{bmatrix}
13.57 & -0.05 & -5.74 \\
-0.05 & 1.64 & -0.17 \\
-5.47 & -0.17 & 10.63
\end{bmatrix} \text{ nH} \quad (2-50)
\]
Figure 2-13 Comparison of the simulated drain-to-source voltage of the top switch of the top HB during turn-off transition between original and proposed layouts.

Compared to (2-46) – (2-48), both self and mutual inductance are reduced. In (2-51), the mutual inductance $M_{12.p}$ are greatly reduced compared with those in (2-48). They are still positive because they include the inductance of the shared P and N bus bar terminals. The comparison of the simulated drain-to-source voltage ringing of the MOSFET in the first HB (from the left) in a double pulse tester is shown in Figure.2-13. Due to the reduced parasitic inductance, the overshoot and oscillation are both significantly reduced.

The turn-off voltage overshoot and oscillation depend on the parasitic inductance not only inside but also outside the module. A parametric study was conducted on the proposed inductance model with Llead increases from 0 nH to 30 nH. The simulated peak voltage overshoot in Figure. 2-14 shows that for the module under investigation if

$$M_{12.p} = \begin{bmatrix} 3.41 & -0.22 & -4.17 \\ -0.02 & 0.01 & -0.2 \\ -3.75 & -0.01 & 2.02 \end{bmatrix} \text{nH} \quad (2-51)$$
Llead is above 15 nH, the benefits of the minimized-inductance inside the module would be limited. Therefore, it is critical to minimize Llead to fully take advantage of the proposed module layout. In this paper, paralleled DC link capacitors are used to minimize ESL, and they are directly mounted to the terminals of the module. As a result, the measured total inductance Llead+ESL is only 4.8 nH. Because of this, the module layout and internal bus bar optimization lead to a greatly reduced parasitic inductance.

![Figure 2-14](image)

**Figure 2-14** Simulated peak overshoot voltage comparison between the original module and the proposed module with different Llead.

### 2.4 Experimental Verification

An HB multichip SiC power module with the proposed layout was fabricated using wire bonds with a DBC process. The proposed module consists of 12 SiC MOSFETs (CPM2-1200-0025B) and 12 SiC Schottky diodes (CPW51200Z050B), the same as the commercial module. The fabricated prototype is shown in Figure.2-15. The self and mutual inductance of the original and proposed layouts are firstly extracted with
S-parameter measurement. The transient response of the two modules is tested with a double pulse tester.

Figure 2-15 The prototype of the proposed HB multichip power module.

A. Two-port S-parameters Measurement

Figure 2-16 shows the extraction of self and mutual inductance of two inductors using S-parameters [24]. The inductance can be derived from the measured S-parameters in (2-52)-(2-56).

![Diagram of two-port S-parameters measurement](image)

Figure 2-16 Extraction of the inductance of two inductors with S-parameters.

For a pair of conductors with a common ground connection inside the power module, as in Figure 2-17, port 1 and port 2 are connected to the DBC plane where the drains of the parallel MOSFETs $S_1$ and $S_3$ are positioned. The reference ground plane
of the two ports is connected to the P terminal. Calibration was first conducted to the measurement interface, so the parasitics of the extra interconnections were excluded from the measurement results. The measured S-parameter matrix with PLANAR-808/1 network analyzer was converted to Z parameters based on (2-52) to (2-56). Self-inductance $L_{d1}$, $L_{d2}$ and the mutual inductance $M_{d1d2}$ are derived from (2-56).

Figure 2-17 using two-port S-parameters to extract inductance with common ground connection: (a) ports and ground connections and (b) equivalent circuit.

Figure 2-18 Two-port S-parameters measurement with different ground connections: (a) ports and ground connections and (b) equivalent circuit.
\[
Z_{11} = Z_0 \frac{(1-S_{21})/(1-S_{11}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \quad (2-52)
\]

\[
Z_{12} = Z_0 \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \quad (2-53)
\]

\[
Z_{21} = Z_0 \frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \quad (2-54)
\]

\[
Z_{22} = Z_0 \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \quad (2-55)
\]

\[
\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = j\omega \begin{bmatrix} L_{11} & M_{12} \\ M_{21} & L_{22} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (2-56)
\]

Figure 2-19 Extracted impedance: (a) \(L_{d1}\), (b) \(L_{d2}\) and (c) \(M_{d1d2}\).
Figure 2-20 Comparison of the measured self and mutual inductance of the two modules: (a) self-inductance and (b) mutual inductance.

If the conductors do not share the ground, one of the terminals of each conductor is locally connected to the reference ground of the two ports, as in Figure. 2-18. Port 1 is connected to the DBC plane where the drain of the MOSFET $S_1$ is positioned. Port 2 is connected to the source of the MOSFET $S_1$. The reference ground plane of the two ports is connected to the P terminal, and the drain of $S_2$. This extracts the self-inductance $L_{d1}$, $L_{o1}$ and the mutual inductance $M_{d1o1}$. The extracted impedance curves are shown in Figure. 2-19. The extracted inductances for both the original and the proposed layouts are compared with the simulated in (2-46) - (2-48) and (2-49) - (2-51) in TABLE 2-1 and TABLE 2-2. The simulated and the extracted match well. The comparison of self and mutual inductance is shown in Figure. 2-20. Both self and mutual inductance are reduced.
Table 2-1. The inductance of the original layout (nH)

<table>
<thead>
<tr>
<th></th>
<th>Simulated</th>
<th>Measured</th>
<th>Simulated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{d1}$</td>
<td>20.73</td>
<td>20.69</td>
<td>-4.19</td>
<td>-4.91</td>
</tr>
<tr>
<td>$L_{d2}$</td>
<td>20.30</td>
<td>19.89</td>
<td>17.74</td>
<td>16.7</td>
</tr>
<tr>
<td>$L_{o1}$</td>
<td>21.61</td>
<td>23.21</td>
<td>-0.93</td>
<td>-1.50</td>
</tr>
<tr>
<td>$L_{o2}$</td>
<td>21.58</td>
<td>23.17</td>
<td>-6.10</td>
<td>-6.41</td>
</tr>
<tr>
<td>$L_{s1}$</td>
<td>19.59</td>
<td>19.63</td>
<td>-1.02</td>
<td>-1.80</td>
</tr>
<tr>
<td>$L_{s2}$</td>
<td>19.10</td>
<td>19.22</td>
<td>9.49</td>
<td>10.03</td>
</tr>
<tr>
<td>$M_{d1o1}$</td>
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<td>-2.34</td>
<td>-4.14</td>
<td>-4.75</td>
</tr>
<tr>
<td>$M_{d1s1}$</td>
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<td>-6.32</td>
<td>-6.07</td>
<td>-6.61</td>
</tr>
<tr>
<td>$M_{o1s1}$</td>
<td>-4.17</td>
<td>-4.97</td>
<td>-4.97</td>
<td>-5.52</td>
</tr>
<tr>
<td>$M_{d2o2}$</td>
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<td>-2.09</td>
<td>17.61</td>
<td>17.77</td>
</tr>
<tr>
<td>$M_{d2s2}$</td>
<td>-6.05</td>
<td>-6.33</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

B. Double Pulse Testing

The setup of a double pulse testing is shown in Figure. 2-21. The top switches are driven with a double pulse signal while the gate voltage of the bottom switches is kept at -4 V. The gate resistors used in the experiments are 15 Ω. The DC link capacitors include a 1 mF electrolytic capacitor (Cornell Dubilier 947D), a 20 µF film capacitor (B32758G8306K000), and three 220nF ceramic capacitors.
(2220Y1K20224KXTWS3) in parallel. The total ESL is 4.8 nH. The load inductor is a 2 mH air-core inductor.

| Table 2-2. The inductance of the proposed layout |
|-----------------|--------------|--------------|--------------|--------------|
| (nH)            | Simulated    | Measured     | Simulated    | Measured     |
| $L_{d1}$        | 13.25        | 13.52        | $M_{d2s2}$   | -0.03        | -0.31        |
| $L_{d2}$        | 13.57        | 13.8         | $M_{d1d2}$   | 3.41         | 2.99         |
| $L_{o1}$        | 1.60         | 2.06         | $M_{d1o2}$   | -0.22        | -0.52        |
| $L_{o2}$        | 1.64         | 1.82         | $M_{d1s2}$   | -4.17        | -3.87        |
| $L_{s1}$        | 13.98        | 14.35        | $M_{o1d2}$   | -0.02        | -0.43        |
| $L_{s2}$        | 14.22        | 14.59        | $M_{o1o2}$   | 0.01         | 0.20         |
| $M_{d1o1}$      | 0.01         | 0.47         | $M_{o1s2}$   | -0.01        | 0.20         |
| $M_{d1s1}$      | -7.16        | -6.50        | $M_{s1d2}$   | -3.75        | -3.29        |
| $M_{o1s1}$      | -0.22        | -0.52        | $M_{s1o2}$   | -0.20        | -0.20        |
| $M_{d2o2}$      | -0.05        | -0.08        | $M_{s1s2}$   | 2.02         | 1.84         |
| $M_{d2s2}$      | -7.47        | -6.12        |              |              |              |
Figure 2-21 Double pulse test setup

Figure 2-22 Drain-to-source voltage measurement and circuit.

The voltage probes are inserted into the insulating gel inside the power module to measure the device voltage. Figure 2-22 (a) shows the probe positions. The die voltage instead of terminal voltage can be measured, as shown in Figure 2-22(b).
Figure 2-23 Comparison of the measured turn-off transient voltage waveforms between the original and the proposed layouts under a 600 V / 120 A test.

Figure 2-24 Comparison of the measured gate voltage waveforms of the bottom switch when the top switch (a) turns on and (b) turns off.
The measured switching waveforms of the proposed and original layouts during the turn-off transition are shown in Figure. 2-23. The modules were tested at a 600 V/120 A. The original layout has a peak overshoot of 120 V compared with 50 V of the proposed layout. The waveforms in Figure. 2-23 also matches the simulation results in Figure.2-13. It is expected that the HF EMI caused by the voltage oscillation can be significantly reduced. The experimental results validate the effect of parasitic inductance reduction.

The gate voltages of the bottom switches of the two modules are measured in the experiment. Figure. 2-24 shows the measured gate voltage of the bottom switches during the top switch’s switching transients. In the original module, the peak positive induced gate voltage is 7.2 V, which is higher than the threshold voltage (3V). The devices are falsely turn-on. The lowest negative induced voltage of the original layout is -7.8 V, which is close to the negative gate breakdown voltage of the SiC MOSFETs (-10V). The off-state voltage of the driver cannot move to a negative value to avoid the false turn-on without risking device negative gate breakdown. In the proposed layout, because of the reduced parasitic inductance, the voltage and current oscillations are reduced. So, the induced gate voltage is reduced. The highest induced gate voltage is 4.8 V, and the lowest induced gate voltage is -5 V. Setting the off-state voltage to -4V can avoid the false turn-on. This greatly improves the reliability of the module [28].
2.5 Thermal Simulation

To validate the proposed layout has no thermal issues. A thermal simulation was carried out in Ansys Icepak for both modules with an identical heatsink. The two modules are first simulated in Ansys Simplorer under 600V/120A at 70 kHz. Based on the simulated drain to source voltage $V_{ds}$ and drain current $I_d$ in Figure 2-25, the voltage and current ringing in the proposed module are smaller. As a result, the switching power loss of the proposed layout is 56 W vs. 67 W of the original layout. The SiC MOSFET conduction power loss is 2.4W, and diode conduction power loss is 16W for both cases. In the Ansys Icepak simulation, finite element analysis is conducted on the 3D models of the two modules. Three mesh levels were assigned to the models. The maximum cubical mesh size for the DBC dies, and bus bars is $1 \text{ mm} \times 1 \text{ mm} \times 0.2 \text{ mm}$. The maximum mesh size for the region enclosing the module is $2 \text{ mm} \times 2 \text{ mm} \times 1 \text{ mm}$. The region outside the module is 5 times larger than the module dimensions in xyz directions. It is in an open region with 5 m/s air flow. The maximum mesh size of the air is $10 \text{ mm} \times 10 \text{ mm} \times 8 \text{ mm}$. The boundary of the region is opening. Gravity is set to be 9.8 m/s$^2$.

![Graph showing voltage and current over time](image)
Figure 2-25 Simulated switching waveforms during turn-on and turn-off transient for switching loss calculation: (a) Original layout (b) proposed layout.

Figure 2-26 Simulated temperatures of (a) original layout and (b) proposed layout.

The simulated results are shown in Figure 2-26. The highest junction temperature of the proposed layout is 120 °C vs. 130 °C of the original layout. It is concluded that because of the reduced switching power loss, the thermal performance of the proposed module is better than the original module.

2.6 Near Field Discussion

Other than direct EMI and driver coupling, the fast switching speed and voltage oscillation could magnetically be coupled to other circuits near the power module.
Because of the high power rating of the power loop, the current is much larger than most of the peripheral circuits. Even a small amount of coupling could cause the victim circuits, such as digital filters, ICs, or controller chips, to fail.

Figure 2-27 shows the magnetic coupling mechanism between the power module and the victim circuit. The mutual inductance $M$ is the near magnetic field generated by the current in the power loop.

Figure 2-27 Near magnetic field emission from power modules

The magnetic flux is generated by current loops in the power module. It is the root cause of the parasitic inductance. As a result, if the total parasitic inductance is reduced, it can be predicted that the near magnetic field emission would be reduced.

In the case of SiC power modules, as shown in Figure 2-28, the current loops formed by the bus bars dominate the magnetic field source because their size area is much larger than the loop in the package.
Figure 2-28 Current loops in the original layout structure.

Figure 2-29 Near magnetic field vector for the SiC MPM. (a) Overview and (b) top view.
To simulate the near magnetic field outside the power module, current excitations are added with the waveforms in Figure 2-25. The magnetic field vectors are shown in Figure 2-29. Figure 2-29 shows the near magnetic field vectors for the SiC power module with the original layout. The magnetic field vector clearly shows that the current loops formed by the bus bar are the main source of emission. At the same time, it can be observed that the peripheral of the power module is more severely influenced by the near magnetic field emission than the top.

The current loops in the proposed layout are shown in Figure 2-30. Compared with the current loops in the original layout in Figure 2-28, the current loops in the proposed layout are interleaved. The magnetic flux generated by each current loop can partially cancel each other.

![Current loops in the proposed layout structure.](image)

Because of the interleaved structure, the near magnetic field emission of the proposed layout is expected to be smaller than the original layout. The simulation is
shown in Figure. 2-31.

Figure 2-31 Near magnetic field vector comparison. (a) The original layout and (b) proposed layout

Figure. 2-31 shows the spatial magnetic field distribution outside the power module. It can be observed that the near magnetic field emission of the proposed layout is smaller than the original one. Both magnitude and area of the near magnetic field is smaller with the proposed layout.

Figure. 2-32 shows the magnetic field strength along the two lines outside the power module. From Figure. 2-32, the magnetic field strength of the proposed layout is smaller than the original layout along both lines.
Different from the conventional parasitic inductance model, the parasitic mutual inductance between parallel current path segments is included in the parasitic inductance model of SiC multichip power modules in this paper. It is found that the mutual inductance plays an important role in the switching transient voltage ringing, which can be reduced with negative mutual inductance. The negative mutual inductance can be realized with a $180^\circ$ position angle between parallel current path segments. A technique was proposed to extract parasitic inductance, and the extracted parasitic inductances match the simulated well. A layout was proposed to reduce the parasitic inductance inside the package without increasing fabrication difficulty. Double-pulse testing and thermal simulations were conducted to validate the proposed technique can reduce parasitic voltage ringing, crosstalk effect, power loss, and thermal stress. In addition, the near magnetic field emission is discussed for the two power module layout.
structures. Because of the mutual inductance cancellation technique, the near magnetic field generated by the proposed power module is much smaller compared to the original power module.
CHAPTER 3
PACKAGE OPTIMIZATION FOR POWER MODULES WITH GAN HEMTS TOWARDS
LOW EMI AND HIGH RELIABILITY

3.1 Introduction of Chapter 3

Other than SiC MOSFETs, another popular power device made with WBG material is the GaN HEMT. Different from SiC MOSFETs, GaN HEMTs have a wide range of power ratings [58]. Both high power and low power GaN have faster switching speed and higher operation frequency compared with their Si counterparts with similar power ratings [59]. Because of the smaller junction capacitance, high power GaN HEMTs have higher switching speeds even compared to SiC MOSFETs. In addition, GaN HEMTs have a unique reverse conduction characteristic [59]. This means GaN HEMT could conduct current in both ways. Even when the current is flows from source to drain, the channel resistance of GaN HEMTs is still very small. This is a desirable feature because, in power modules made with GaN HEMTs, there is no need for anti-parallel diodes. With the absence of anti-parallel diodes, the cost and volume of the power module are reduced, which leads to a higher power density.

Figure 3-1 shows the package structure of a half-bridge power module made with GaN HEMTs. In this half-bridge power module, two pairs of GaN HEMTs are used. Two as the high switch and two as the low switch. Figure 3-1 (b) shows the package with bus bars and pins hidden. For each switch, two paralleled GaN HEMTs are used. As shown in Figure 3-1 (c), the structure of the GaN HEMT die is different from SiC MOSFETS.
Because of the horizontal structure, drain, source, and gate pads are all on the top of the die.

![Package Structure Diagram](image)

Figure 3-1 The package structure of a power module made with GaN HEMTs. (a) Power module package, (b) power module package with bus bars and pins hidden. (c) GaN HEMT structure and (d) schematic with parasitic inductance

Similar to the SiC power modules, power modules with GaN HEMTs also applied a wire-bonded DBC package technology. The parasitic inductance in the package of
GaN HEMT power modules is also large. As shown in Figure. 3-1 (d), parasitic inductance inside the power loop could cause voltage overshoot and oscillation, just like in the SiC power modules.

Figure 3-2 Evaluation and optimization flowchart for the power module package

Since a detailed parasitic inductance model has already been proposed in Chapter II, in this Chapter, the model is used directly. The derivation process is excluded. The investigation of the power module with GaN HEMT went through an evaluation process, as shown in Figure. 3-2. The 3D model is firstly built for the power module. The parasitic inductance is then extracted with the Q3D software based on the model proposed in Chapter II. The parasitic inductance model is then imported into a circuit simulator, where the switching waveforms are recorded. At this stage, the model is verified by comparing the simulated switching waveforms to the measured ones. After the accuracy of the model is verified, the switching waveforms are imported to field
simulators such as HFSS and IcePak for EM field and thermal evaluation. The evaluation could provide feedback so that the power module package layout can be optimized.

Different from SiC MOSFETs, GaN HEMTs can switch at an even higher speed. Therefore, power modules with GaN HEMTs are more sensitive to the parasitic inductance than SiC power modules. Other than the voltage overshoot and oscillation, the dynamic current unbalance caused by the high switching speed also causes EMI issues. In addition, the dynamic current unbalance causes devices to overheat. GaN HEMTs have smaller thermal conductivity compared to SiC MOSFETs. As a result, GaN HEMTs require stricter thermal consideration.

Therefore, the objectives of the package optimization are:

a) Dynamic current balancing
b) Small parasitic inductance
c) Good thermal performance

3.2 Dynamic Current Unbalance Issue in Power Modules with GaN HEMTs

After the evaluation process, it was found that the dynamic current unbalance issue is very serious in this power module. As shown in Figure. 3-3, during the switching transient, the current that flows through the two paralleled branches are very different. The dynamic current unbalances among the paralleled branches cause the device to overheat, damaging the power module reliability, and generate differential mode EMI noises. As a result, it is very important to suppress the dynamic current unbalance.
In previous studies, it is believed that the dynamic current unbalances in the power module are caused by parasitic parameter mismatches [61]. The mismatch could be caused by the power loop and drive loop. In [61], it is believed that the drive loop unbalance a large impact on the dynamic current. Therefore, the driver loops of paralleled devices should be designed to be balanced as much as possible. Avoiding shared paths is also a good practice. In [62]-[64], the impact of power loop parasitic parameters is discussed. In [63], an almost completely symmetrical layout is proposed to balance the dynamic current. In practice, a perfectly symmetrical layout is impossible. As a result, in [65] [66], additional components such as DM chokes are implemented. However, these techniques inevitably increase the cost.

Figure 3-3 Illustration of dynamic current in the power module with GaN HEMT. (a) Current waveform during SW1 and SW3 turn-on transient. (b) Equivalent circuit
Based on the previous research, the self parasitic inductance of the power loop and drive loop is firstly extracted. The extracted parasitic inductance is shown in TABLE 3-1.

<table>
<thead>
<tr>
<th>Table 3-1 Parasitic inductance in the paralleled branches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>----------------------------------------------------------</td>
</tr>
<tr>
<td>Power loop inductance (nH)</td>
</tr>
<tr>
<td>Drive loop inductance (nH)</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

In TABLE III-I, the difference between the self-inductance in the power loop of branch 1 and branch 2 is 7%. The difference between the drive loop is 1.4 %. Based on the previous research, this very small difference will not cause a large dynamic current to unbalance. However, as shown in Figure. 3-3 (a), the dynamic current unbalance is larger and obvious. As a result, the dynamic model proposed in previous research cannot fully explain the dynamic current in the power modules with GaN HEMTs. There are other reasons that cause the dynamic current to unbalance.

3.2.1. Dynamic Current Analysis During Device Switching Transient

The dynamic current during device switching transient is caused by the energy stored in the parasitic inductance. As shown in Figure.3-4, during SW1 and SW3 turn-on transient, the current that flows through branch 1 and branch 2 are given by:

\[ i_{d1} = g_{m1} (V_{gs1} - V_{th1}) \]  

(3-1)
\[ i_{d2} = g_{m3}(V_{gs3} - V_{th3}) \]  \hspace{1cm} (3-2)

Where \( g_{m1} \) and \( g_{m2} \) are the transconductance of SW1 and SW3, respectively. \( V_{gs1} \) and \( V_{gs3} \) are the gate to source voltage of SW1 and SW3, respectively. \( V_{th1} \) and \( V_{th3} \) are the threshold voltage of SW1 and SW3, respectively.

\[
V_{gs1} = V_{g1} - i_{g1}R_{g1} - L_{g1}\frac{di_{g1}}{dt} \hspace{1cm} (3-3)
\]

Where \( V_{g1} \) is the voltage given by the driver. \( i_{g1} \) is the gate current during the driving. \( R_{g1} \) and \( L_{g1} \) are the drive loop resistance and inductance, respectively.

During the switching transient, the difference between the current is given by:

\[
i_{DM} = i_{d1} - i_{d2} \hspace{1cm} (3-4)
\]
$i_{DM}$ represents the dynamic current unbalance. It is defined as the differential
current, as shown in Figure.3-4. Normally, the driver voltage and current are identical for
each switch. The variation is not brought by the package. In the simulation, this part of
variation can be avoided. In addition, the gate resistors of all four switches have the
same value. As a result, the drive loop variation is solely caused by the parasitic
inductance.

From (3-1) - (3-3), the drive loop mismatch, namely $L_{g1} \neq L_{g3}$ causes the drain
current to be different. Device mismatches, namely $g_{m1} \neq g_{m3}$ or $V_{th1} \neq V_{th3}$ can also
be caused by the dynamic current unbalance. However, after the device is turned on,
the drive loop quickly loses control of the drain current. The current in the two branches
is governed by the parasitic parameters in the power loops.

During the switching transient, the power loop equations are given by:

$$
\begin{bmatrix}
V_{d1} \\
V_{s1}
\end{bmatrix} = 
\begin{bmatrix}
L_{d1} & M_{d1s1} \\
M_{d1s1} & L_{s1}
\end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_{d1} \\
i_{d1}
\end{bmatrix} + 
\begin{bmatrix}
M_{d1d3} & M_{d1s3} \\
M_{d3s1} & M_{s1s3}
\end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_{d2} \\
i_{d2}
\end{bmatrix} \tag{3-5}
$$

$$
\begin{bmatrix}
V_{d3} \\
V_{s3}
\end{bmatrix} = 
\begin{bmatrix}
M_{d13} & M_{s1d3} \\
M_{d1s3} & M_{s1s3}
\end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_{d1} \\
i_{d1}
\end{bmatrix} + 
\begin{bmatrix}
L_{d3} & M_{d3s3} \\
M_{d3s3} & L_{s3}
\end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_{d2} \\
i_{d2}
\end{bmatrix} \tag{3-6}
$$

When the voltage drops are different on parasitic inductance, a differential
voltage $\Delta V = V_{d1} + V_{s1} - V_{d3} - V_{s3}$ causes differential current. The differential current
can be calculated in the frequency domain:

$$
i_{DM} = \frac{\Delta V}{j \omega (L_{d1} + L_{d3} + L_{s1} + L_{s3} + 2M_{d1s1} + 2M_{d3s3} - 2M_{d1d3} - 2M_{d1s3} - 2M_{d3s3} - 2M_{s1s3} - 2M_{d1s3} - 2M_{s1d3})} \tag{3-7}
$$

Where $\Delta V$ is the differential voltage. The differential voltage is caused by the
parasitic parameter mismatch between drive loops and power loops, as well as between
the devices. In previous studies, most of the efforts are to reduce this differential voltage with a symmetrical design. However, from (3-7), the differential voltage is not the only reason that causes the dynamic current to unbalance. The impedance in the power loop also has a large impact. In this Chapter, the impedance on the denominator of (3-7) is defined as the differential (DM) impedance. In most previous research, because of the absence of mutual inductance, the DM impedance seems just like the power loop inductance. However, they are different because the mutual inductance has opposite polarities.

3.2.2. Dynamic Current Case Study

From (3-7), the dynamic current is not only caused by the differential voltage but also the DM impedance. To show the impact of DM impedance, a simple case is discussed. As shown in Figure 3-5, a paralleled half-bridge is under discussion. Only two power loop inductance is present. The self-inductance of the two inductances has a 5% variation. At the same time, the mutual inductance is represented by the coupling coefficient, which is given by:

$$K = \frac{M_{d1d3}}{\sqrt{L_{d1}L_{d3}}} \quad (3-7)$$

The larger the coupling coefficient is, the more closely coupled these two inductances are. With the same 5% variation, the differential voltage $\Delta V$ is kept constant. At the same time, the coupling coefficient changes from -0.5 to 0.9,
representing from negative coupling to positive coupling. The differential current $i_{DM}$ is simulated and compared. As shown in Figure. 3-6.

![Simplified circuit for the case study](image)

**Figure 3-5 A simplified circuit for the case study**

![Differential current graph](image)

**Figure 3-6 The differential current under different coupling coefficient**

As shown in Figure. 3-6, under the same differential voltage, the differential current varies largely with different coupling coefficients. When the two inductances are
positively coupled, the DM current is large. When the two inductances are not closely coupling or negatively coupled, the DM current is small. The result agreed with (3-7).

When the two inductances are positively coupled, the DM impedance of the circuit is very small. Namely, the denominator in (3-7) dominates the outcome. Even with a very small differential voltage, the DM current could be very large.

3.2.3. Dynamic Current in Power Modules With GaN HEMTs

In the case of power modules with GaN HEMTs, the differential voltage \( \Delta V \) is large because of the fast switching speed. From (3-5) and (3-6), when \( \frac{dI_d}{dt} \) is high, the differential voltage is high. A small amount of parasitic parameter mismatch could lead to a high differential voltage. At the same time, as shown in Figure.3-1, the paralleled switches are located close to each other. As a result, the mutual inductance between the paralleled branches is positive and large. The DM impedance of the power module is very small. Which leads to a large differential dynamic current.

Since it is impractical to completely eliminate the differential voltage, it is important to increase the DM impedance in the power module to suppress the DM current. However, simply increasing the DM impedance is not enough. If the power loop inductance is large, the issues brought by the voltage overshoot and oscillation will cause additional EMI concerns.

To achieve a high DM impedance and small power loop inductance. The parasitic inductances inside the power module package are divided into two parts: Cm
impedance and DM impedance. As shown in Figure 3-7 and Figure 3-8, the CM impedance represents the power loop inductance for each branch and the mutual inductance between each pair. The DM impedance represents the path impedance where the DM current flows.

Figure 3-7 (a) Power current in the circuit and (b) CM impedance paths

Figure 3-8 (a) Differential current in the circuit and (b) DM impedance paths
The difference between the CM impedance and DM impedance is the polarity of the mutual inductance. To increase DM impedance while reduce the CM impedance, the mutual inductance should be small and negative.

### 3.3 Package Optimization for Power Module with GaN HEMTs

To reduce the mutual inductance between paralleled branches, the technique proposed in Chapter II can be applied. As shown in Figure 3-9, an interleaved package layout is proposed for the power module with GaN HEMTs. The positions and the bus bar remain the same.

![Figure 3-9 Power module comparison between the original package and the proposed package. (a) The original layout and (b) proposed layout.](image)

Figure 3-10 shows the detailed layout with bus bars and pins hidden. The top switches and bottom switches are placed close together. At the same time, the segments that carry the opposite current direction is put close together. In this way, the mutual inductance is minimized. It is worth noticing that one of the considerations during the design process is to keep the cost low. As a result, the overall shape and bus bar
position of the power module is not changed so that the power module can be easily manufactured on the original platform.

![Figure 3-10 Layout comparison between the original package and the proposed package. (a) The original layout and (b) proposed layout.](image)

Figure 3-10 shows the layout comparison between the original package and the proposed package. (a) The original layout and (b) proposed layout.

Figure 3-11 and Figure 3-12 show the CM and DM impedance path in the original and proposed layout. For the CM impedance paths, the proposed layout adopted an interleaved structure. The magnetic field generated by the power loop of the paralleled branch can partially cancel each other. As a result, the total power loop inductance would be smaller in the proposed layout.

![Figure 3-11 CM impedance comparison. (a) The original layout and (b) proposed layout](image)
Figure 3-12 DM impedance comparison. (a) The original layout and (b) proposed layout

From Figure 3-12, the DM impedance path in the original layout is very short. The DM impedance in the original layout is large. In the proposed layout, the DM current path is long. Therefore, the DM impedance in the proposed layout is much larger than the original one.

The extracted DM impedance is shown in Figure 3-13. From the extracted inductance, the DM impedance of the proposed layout is effectively increased.

Figure 3-13 Extracted DM impedance comparison
3.4 Simulation Verification for The Proposed Layout

To verify the proposed, the same evaluation process shown in Figure 3-2 is carried out. The proposed power module went through the process. The current in each paralleled branch is shown in Figure 3-14.

![Figure 3-14 Current comparison. (a) The original layout and (b) proposed layout](image)

As shown in Figure 3-14, the dynamic in the paralleled branch is very balanced in the proposed power module. Compared with the original layout, there is hardly any DM current in the proposed layout.

To verify the benefits of the increased DM impedance, a 10% power loop impedance variation is deliberately added to the proposed layout. The DM current is calculated based on the current waveform and shown in Figure 3-15.

From Figure 3-15, even with 10% variation, the proposed layout has superior performance in terms of dynamic current balancing. Because of the increase DM current, the proposed layout has a certain level of immunity to mismatches caused by the parasitic parameters in the package, as well as device parameter variations. This is
a desirable feature considering there will always be some imperfections during the design and fabrication. With the increased DM impedance in the proposed layout, the dynamic current can be balanced without increasing any cost or additional components.

Figure 3-15 Differential current comparison

To verify that the power loop inductance is not increased in the proposed layout, a double pulse tester circuit is applied. During the turn-off transient, the drain to source voltage of SW1 is recorded and shown in Figure 3-16.

Figure 3-16 Turn-off voltage comparison
Form Figure 3-16. The turn-off voltage of the proposed layout is smaller compared to the original layout. However, the advantage is not obvious. This is because there are only two paralleled branches in this power module. The benefit of mutual inductance cancellation is more obvious with a higher number of paralleled branches. In addition, the bus bar structure in this power module is not changed, not like the case in Chapter II. Therefore, the total voltage overshoot reduction is not obvious.

![Figure 3-17](image1)

(a) (b)

Figure 3-17 Thermal performance comparison. (a) The original layout and (b) proposed layout.

Figure 3-17 shows the thermal performance comparison between the original and proposed layout. Under the same power loss, the proposed layout has a similar junction temperature to the original layout. Considering the footprint of the power module is the same for both layouts, the result verified that the proposed layout would not have thermal concerns.
3.5 Conclusion of Chapter 3

In this Chapter, the package of the power modules with high power GaN HEMTs is optimized. The dynamic current unbalance issues are discussed in detail. Different from the previous research, the impact of differential impedance is identified in this Chapter. The dynamic current unbalances in this power module is caused by the low DM impedance. A package layout with increased DM impedance is proposed to suppress the dynamic current unbalance and reduce the total power loop inductance at the same time. The analysis and the proposed layout are verified with simulation.
CHAPTER 4
A MILLER EFFECT SUPPRESSION TECHNIQUE FOR SiC MOSFETS IN A PHASE-LEG CONFIGURATION

4.1 Introduction of Chapter 4

For the SiC MOSFETs in a phase-leg configuration, there are two types of Miller effect: The coupling between the power loop and drive loop [69], and the coupling between the top and the bottom switches. The coupling between the power loop and the drive loop causes the gate voltage to be clamped at a constant value for a period of time during switching transient. This is also known as the Miller plateau [68]. The length of the Miller plateau determines the switching speed of the device.

The coupling between the top and bottom switches is the interaction between the two switches in a phase-leg configuration at high dv/dt switching [69]. Positive and negative voltage spikes are induced at the gates of the devices; this is also known as the crosstalk effect. The positive voltage spike causes potential false triggering, which leads to hazardous shoot-through failure. The negative gate voltage spike could cause a gate-oxide breakdown [70]. In industrial applications, both false triggering and negative voltage over-range must be avoided by all means. It is worth noticing that the common source inductance (CSI) [69] also contributes to the crosstalk effect. Reducing the value of CSI by Kelvin connection or package optimization usually mitigates the crosstalk caused by CSI. In contrast, the Miller capacitance is an intrinsic property of the power device. Reducing the crosstalk caused by the Miller capacitance is a major
challenge. Therefore, this paper focuses on the issues brought by the Miller capacitance.

In previous researches, many have proposed techniques to suppress the crosstalk effect in the bridge-leg configuration. These techniques mainly fall into three categories.

1. Reducing the switching speed. Increasing the gate resistor value or adding an additional gate capacitor can effectively mitigate the crosstalk effect [71] [72]. However, by doing this, the switching speed of the power device would be sacrificed.

2. Control the gate loop impedance. The magnitude of the induced gate voltage depends on the impedance of the drive loop. As a result, providing a low-impedance path between the gate and source of the victim device mitigates the crosstalk. Methods to provide low gate impedance during crosstalk are proposed in [73] – [75]. In [76], a high gate impedance technique is proposed to damp the gate voltage oscillation while

---

**Figure 4-1 Safe operation margin for gate driver**

1. Reducing the switching speed. Increasing the gate resistor value or adding an additional gate capacitor can effectively mitigate the crosstalk effect [71] [72]. However, by doing this, the switching speed of the power device would be sacrificed.

2. Control the gate loop impedance. The magnitude of the induced gate voltage depends on the impedance of the drive loop. As a result, providing a low-impedance path between the gate and source of the victim device mitigates the crosstalk. Methods to provide low gate impedance during crosstalk are proposed in [73] – [75]. In [76], a high gate impedance technique is proposed to damp the gate voltage oscillation while

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the Miller capacitance is pre-charge and pre-discharge to avoid crosstalk. Controlling the gate impedance usually requires complicate circuit design and control logic.

3. Applying Multi-level driver voltage [77] – [81]. Multi-level gate voltage techniques do not suppress the induced gate voltage spikes. Instead, different levels of off-state gate voltage are added to prevent false triggering and negative voltage over-range after the crosstalk has occurred. In cases with SiC MOSFETs, both positive and negative induced gate voltage spikes are high due to high switching speed. As shown in Figure. 4-1, the safe operation region of the gate voltage is much narrower compared to the Si IGBTs. The off-state gate voltage must be controlled precisely to avoid false triggering and negative breakdown at the same time. The design of a multi-level gate driver becomes costly and challenging.

Some research attempts to reduce the Miller plateau. Closed-loop techniques were proposed in [82] – [85]. These closed-loop techniques compare the sampled voltage and/or current waveforms to the desired waveforms, then change the gate voltage accordingly. The closed-loop techniques require many additional analog and/or digital circuits design. The crosstalk effect is not considered in these closed-loop driver designs. In some cases, applying a closed-loop driver increases the chances of false-triggering [18] and requires additional circuits [85].

In this Chapter, a Miller current cancellation technique is proposed. Different from previous works, the Miller capacitance can be equivalently canceled by injecting a cancellation current. The proposed technique takes the non-linearity of the Miller
capacitance into consideration. The circuit requires no driving signal or control strategies. It can be applied to most commercial drivers or integrated inside the power module package. The rest of the paper will be organized as follows: The root cause of the Miller effect is analyzed in Section II. Based on the analysis, the Miller current cancellation technique is proposed in Section III. Section IV discusses the design considerations. Simulation and experimental verifications are presented in Section V. Section VI concludes the paper.

4.2 Review of the Miller Effect During the Switching Transient of SiC MOSFETs

There are four switching states for the switches in a phase-leg circuit: top switch turn-on trainset, top switch turn-off trainset, bottom switch turn-on transient, bottom switch turn-off transient. During the switching transients of one switch, the other switch is off. Because the detailed switching transient has been presented in many papers \[68][88][90], this paper only focuses on the role of the Miller capacitance.

As shown in Figure. 4-2, during the switching transient, both drain to source voltage and gate voltage of the top and bottom switches are changing. The interactions are caused by the junction capacitance of the SiC MOSFET.

M1 is off, (d) M2 turn-off transient, M1 is off

The four switching transients of the devices in a phase-leg configuration are presented in Figure.4-2. The gate driver signals of each device, as well as the load current direction, indicate the switching states. The current flows through the junction
The capacitance of the M2 is shown in Figure 4.2. Because the top switch and bottom switch are symmetrical, the transient analysis of M1 is the same as M2.

Figure 4.2 Switching transients of devices in a phase-leg configuration. (a) M1 turn-on transient, M2 is off, (b) M1 turn-off transient, M2 is off, (c) M2 turn-on transient during M1 turn-on transient, as shown in Figure 4.2(a). The drain to source voltage of the bottom switch M2 rises drastically. Because of the presence of \( \frac{dV_{ds2}}{dt} \), a current is induced, flowing through the Miller capacitance of M2. This current is referred to as the Miller current. The drain to gate voltage of M2 is given by:

\[
V_{dg2} = V_{ds2} - V_{gs2}
\]  

(4-1)
In high power applications, the gate voltage of M2 is much smaller than the drain to source voltage, hence $V_{dg2} \approx V_{ds2}$. The derivation of the drain to gate voltage can be expressed as:

$$\frac{dV_{dg2}}{dt} = \frac{dV_{ds2}}{dt} \quad (4-2)$$

The Miller current can be expressed as:

$$I_{Miller} = C_{gd2} \cdot \frac{dV_{ds2}}{dt} \quad (4-3)$$

The Miller current flows through the gate resistor $R_{g2}$ and gate to source capacitance $C_{gs2}$,

$$\frac{V_{gs2}}{R_{g2}} + C_{gs2} \frac{dV_{gs2}}{dt} = i_{Miller} \quad (4-4)$$

$V_{gs2}$ can be solved by with (4-3) and (4-4):

$$V_{gs2} = R_{g2} C_{gd2} \frac{dV_{ds2}}{dt} \left(1 - e^{-\frac{1}{R_{g2}C_{iss2}}} \right) - e^{-\frac{1}{R_{g2}C_{iss2}}} \int R_{g2} C_{gd2} \frac{d^2V_{ds2}}{dt^2} - e^{-\frac{1}{R_{g2}C_{iss2}}} dt + V_{L} \quad (4-5)$$

Where $C_{iss2} = C_{gs2} + C_{gd2}$.

In (4), the first term represents the peak induced gate voltage magnitude and the time delay caused by $R_{g2}$ and $C_{iss2}$. The second term represents the gate voltage ringing, caused by $V_{ds2}$ parasitic oscillation [69]. The third term is the off-state driver voltage. In most studies, the $V_{ds2}$ is analyzed as a trapezoidal waveform. In that case, $\frac{d^2V_{ds2}}{dt^2} = 0$ (4-5) reduces to:

100
\[ V_{gs2} = R_{g2}C_{gd2} \frac{dV_{ds2}}{dt} \left( 1 - e^{-\frac{1}{R_{g2}C_{iss2}t}} \right) + V_L \]  

Equation (4-6) has a similar expression in previous research [74] [75]. (4-6) gives a quick estimation of the peak induced gate voltage. Because \( \frac{dV_{ds2}}{dt} \) in this state is positive, the induced gate voltage is higher than the off-state driver voltage \( V_L \). In SiC MOSFET applications, the \( V_{ds2} \) oscillation can no longer be neglected. Therefore, (4-5) gives a more accurate \( V_{gs2} \) expression.

Similarly, during M1 turn-off transient, as shown in Figure 1 (b). The drain to source voltage of M2 drops drastically. In this state the \( V_{gs2} \) has the same expression as (4-6) except \( \frac{dV_{ds2}}{dt} \) is negative, causing the induced gate voltage to be lower than \( V_L \).

During the M2 turn-on transient, as shown in Figure 4-2 (c). The driver voltage is at \( V_H \). The gate current is given by:

\[ i_g = \frac{V_H-V_{gs2}}{R_{g2}} = C_{gd2} \left( \frac{dV_{gs2}}{dt} - \frac{dV_{ds2}}{dt} \right) + C_{gs2} \frac{dV_{gs2}}{dt} \]  

\[ (4-7) \]

The drain to source voltage of M2 decreases during the Miller plateau, when \( V_{gs2} \) is nearly constant [68]. As a result, \( \frac{dV_{gs2}}{dt} \approx 0 \). (6) can be simplified as:

\[ \frac{V_H-V_{gs2}}{R_{g2}} = -C_{gd2} \frac{dV_{ds2}}{dt} \]  

\[ (4-8) \]

The turn-on switching speed is given by:

\[ \left. \frac{dV_{ds2}}{dt} \right|_{on} = - \frac{V_H-V_{gs2}}{C_{gd2}R_{g2}} \]  

\[ (4-9) \]
Similarly, during the M2 turn-off transient, as shown in Figure.4-2 (d). The drain to source voltage of M2 increases during the Miller plateau. The turn-off voltage slope of M2 is given by:

\[
\frac{dV_{ds2}}{dt}|_{off} = \frac{V_{gs2} - V_L}{C_{gd2}R_{g2}} \tag{4-10}
\]

\(V_{gs2}\) in (4-9) and (4-10) is the Miller plateau voltage. It is determined by the load current [90].

From (4-2) to (4-10), the root cause of the crosstalk and the Miller plateau is the Miller capacitance \(C_{gd2}\). If \(C_{gs2} = 0\), both the Miller plateau and the crosstalk would be eliminated.

### 4.3 The Miller Current Cancellation Technique and Working Principle

As shown in Figure. 4-3, the proposed Miller current cancellation technique (MCCT) comprises three parts: the voltage-sampling circuit (VSC), the voltage-inverting circuit (VIC), and the injection capacitor (\(C_{inj}\)).

The input voltage of the VSC is the drain to source voltage of the SiC MOSFET. As shown in Figure. 4-4, the VSC consists of a voltage-dividing impedance network and a low power MOSFET Q1. Impedance \(Z_{i(i=1 \text{ to } 4)} = \frac{R_i}{sC_iR_i+1}\) consists of a resistor and a capacitor in parallel. This impedance network provides the same sampling ratio in a wide frequency range. \(Z_5 = \frac{1}{sC_{dsq2}}\) represents the impedance of the drain to source junction capacitance of Q1. The gate to drain and gate to source junction capacitance of Q1 are included in \(Z_2\) and \(Z_3\). The VSC operates in two stages and provides two
different gains under different input voltage. The reason for this is to compensate for the non-linearity of the Miller capacitance under different drain to source voltage level.

Figure 4-3 Illustration of the Miller current cancellation technique applied to a SiC MOSFET with a commercial driver

When the input voltage $V_{ds}$ is lower than $V_{div}$, the gate to source voltage lower power MOSFET Q1 $V_{Z3}$ is below its threshold voltage $V_{thQ1}$. Therefore, Q1 is off, as shown in Figure 4-4 (a). The dynamic gain of VSC in stage 1 is defined as:

$$G_{s1} = \frac{dV_{VS}/dt}{dV_{ds}/dt} = \frac{Z_{Q1} + Z_4}{Z_{VD} + Z_{Q1}}$$

(4-11)

Where,

$$Z_{Q1} = \frac{Z_3(Z_2 + Z_3)}{Z_2 + Z_3 + Z_5}$$

(4-12)

$$Z_{VD} = Z_1 + Z_4$$

(4-13)

The dividing voltage $V_{div}$ is given by:
\[ V_{div} = V_{thQ1} \frac{(Z_{Q1} + Z_{VD})(Z_2 + Z_3)}{Z_{Q1}Z_3} \] (4-14)

When \( V_{ds} \) is higher than \( V_{div} \), Q1 is on, as shown in Figure 4-4 (b). The small channel resistance of Q1 bypasses \( C_2 \) and \( C_3 \). Once turned on, Q1 always operates in the saturation region. The channel current of Q1 is given by:

\[ i_{Q1} = g_{mQ1} \cdot (V_{Z3} - V_{thQ1}) \] (4-15)

Where \( g_{mQ1} \) is the transconductance of Q1. The drain to source voltage of Q1 is given by:

\[ V_{Q1} = \frac{V_{ds} + g_{mQ1}Z_{VD}V_{thQ1}}{1 + \frac{Z_{VD}}{Z_{Q1}} + \frac{g_{mQ1}Z_{VD}}{Z_2 + Z_3}} \] (4-16)

Figure 4-4 Voltage sampling circuit operation stages. (a) stage 1 and (b) stage 2

In practice, \( Z_{VD} \) has large value (\( > 10^7 \) \( \Omega \)) at low frequencies to reduce the power loss of the VSC. The value of \( 1 + \frac{Z_{VD}}{Z_{Q1}} \) is determined by the ratio of the impedance \( Z_{VD} \)
and \( Z_{Q1} \), which is < 100. The \( V_{ds} \) of the SiC MOSFET is limited by the maximum power ratings. Therefore, the following assumptions can be made:

\[
\frac{g_{mQ1}Z_{3}Z_{VD}}{Z_{2}+Z_{3}} \gg 1 + \frac{Z_{VD}}{Z_{Q1}} \quad (4-17)
\]

\[
g_{mQ1}Z_{VD}V_{thQ1} \gg V_{ds} \quad (4-18)
\]

Based on (4-17) and (4-18), the \( V_{Q1} \) in (4-16) can be simplified as:

\[
V_{Q1} = V_{thQ1} \frac{Z_{2}+Z_{3}}{Z_{3}} \quad (4-19)
\]

The second stage output voltage of VSC is given by:

\[
V_{VS2} = \frac{Z_{4}}{Z_{VD}}(V_{ds} - V_{Q1}) + V_{Q1} \quad (4-20)
\]

Since \( V_{Q1} \) is a constant value in (4-19). The dynamic gain of VSC in stage 2 is given by:

\[
G_{s2} = \frac{dV_{VS2}/dt}{dV_{ds}/dt} = \frac{Z_{4}}{Z_{VD}} \quad (4-21)
\]

Based on (4-11) and (4-21), by adjusting the impedance \( Z_{1} \) to \( Z_{4} \), the VSC could give two gains under different \( V_{ds} \). \( G_{s1} \) is a large gain when the input voltage is low and \( G_{s2} \) is a small gain when the input voltage is high.

The function of VIC is to invert the voltage signal sensed by VSC. As shown in Figure. 4-5, the VIC consists of two resistors, a low power MOSFET Q2, and a diode \( D_f \). The VIC connects to a DC power supply \( V_{cc} \). This power supply can be the same power supply used by the driver or an independent power supply. The diode \( D_f \) is used to avoid interference from the succeeding circuits. \( R_{inj} \) is the injection resistor. \( R_s \) is the feedback resistor.
When the sensed voltage $V_{VS}$ is higher than the threshold voltage of Q2 $V_{thQ2}$, Q2 turns on. Assuming Q2 operates in the saturation region, the channel current $i_{dQ2}$ is given by:

$$i_d = g_{mQ2}(V_{gsQ2} - V_{thQ2})$$  (4-22)

$$V_{gsQ2} = V_{VS} - R_s i_d$$  (4-23)

Solving (4-22) and (4-23) simultaneously,

$$i_d = \frac{g_{mQ2}(V_{VS} - V_{th})}{1 + g_{mQ2}R_s}$$  (4-24)

The output voltage of the VIC is given by:

$$V_{IV} = V_{cc} - i_d R_{inj}$$  (4-25)

Substitute (4-24) to (4-25),

$$V_{IV} = V_{cc} - \frac{g_{mQ2}R_{inj}(V_{VS} - V_{th})}{1 + g_{mQ2}R_s}$$  (4-26)

The derivation of (4-26) over time is:
\[
\frac{dV_{IV}}{dt} = -\frac{g_{mQ2R_{inj}}}{1+g_{mQ2R_s}} \frac{dV_{VS}}{dt}
\]  
(4-27)

Substitute (4-11) and (4-21) to (4-27), the total gain of the two sub-circuit can be calculated:

\[
G_{MCCT} = \frac{dV_{IV}}{dV_{ds}} = \begin{cases} 
-\frac{Z_{Q1}+Z_4}{Z_{VD}+Z_{Q1}} \cdot \frac{g_{mQ2R_{inj}}}{1+g_{mQ2R_s}}, & V_{ds} < V_{div} \\
-\frac{Z_4}{Z_{VD}} \cdot \frac{g_{mQ2R_{inj}}}{1+g_{mQ2R_s}}, & V_{ds} \geq V_{div}
\end{cases}
\]  
(4-28)

When \(V_{ds}\) of the MOSFET with the MCCT changes drastically, the cancellation current will be injected to the gate of the SiC MOSFET through the injection capacitor \(C_{inj}\), as shown in Figure 4-6. The injected current is given by:

\[
I_{inj} = C_{inj} \left( \frac{dV_{IV}}{dt} - \frac{dV_{gs}}{dt} \right) \approx C_{inj} \frac{dV_{IV}}{dt} = C_{inj} G_{MCCT} \frac{dV_{ds}}{dt}
\]  
(4-29)

During the turn-on of the complementary switch, the drain to source voltage rises. The gate voltage is induced by the Miller current. At the same time, \(i_{inj}\) is injected.

The total current flows through \(R_g\) and \(C_{gs}\) is given by:

\[
\frac{V_{gs}-V_L}{R_g} + C_{gs} \frac{dV_{gs}}{dt} = i_{Miller} + i_{inj}
\]  
(4-30)

Substitute (4-2) and (4-29) to (4-30),

\[
\frac{V_{gs}}{R_g} + C_{iss1} \frac{dV_{gs}}{dt} = \left( C_{gd} + C_{inj} G_{MCCT} \right) \frac{dV_{ds}}{dt}
\]  
(4-31)

Where \(C_{iss1} = C_{gs} + C_{inj} + C_{gd}\).

\(V_{gs}\) can be calculated by:

\[
V_{gs} = R_g \left( C_{gd} + C_{inj} G_{MCCT} \right) \frac{dV_{ds}}{dt} \left( 1 - e^{-\frac{1}{R_g C_{iss1} t}} \right)
\]
\[ e^{-\frac{1}{R_g C_{iss}} t} \int R_g \left( C_{gd} C_{inj} G_{MCCCT} \right) \frac{d^2 V_{ds}}{dt^2} e^{\frac{1}{R_g C_{iss}} t} \, dt + V_L \]  

(4-32)

Compare (4-5) and (4-32), when the following condition is met:

\[ C_{inj} = -\frac{C_{gd}}{G_{MCCCT}} \]  

(4-33)

The first two terms in (4-32) become zero. The Miller capacitance is equivalently canceled. \( V_{gs} \) can be solved as \( V_{gs} = V_L \). The induced positive gate voltage has been canceled.

Similarly, during the turn-off transient of the complimentary switch, the negative induced gate voltage is also canceled when (4-33) is met.

During the turn-on transient of the MOSFET, the driver voltage \( V_{dr} = V_H \). The gate current satisfies:

\[ i_g = \frac{V_H - V_{gs}}{R_g} = -(i_{Miller} + i_{inj}) \]  

(4-34)

The switching speed of the MOSFET is solved by substituting (4-2) and (4-29) to (4-34),

\[ \frac{dV_{ds}}{dt} \bigg|_{on} = -\frac{V_H - V_{gs}}{(C_{gd} + C_{inj} G_{MCCCT})R_g} \]  

(4-35)

Similarly, during the device turn-off transient, the driver voltage \( V_{dr} = V_L \), the switching speed is given by:

\[ \frac{dV_{ds}}{dt} \bigg|_{off} = \frac{V_{gs} - V_L}{(C_{gd} + C_{inj} G_{MCCCT})R_g} \]  

(4-36)
From (4-35) and (4-36), when (4-33) is met, Miller plateau could be equivalently canceled. The switching speed would increase.

Based on the discussion in this Section, the proposed MCCT has the potential to cancel the Miller capacitance. As a result, the crosstalk and Miller plateau could be canceled.

Figure 4-6 Miller current of the MOSFET with the MCCT implemented.

4.4 Design Considerations for the Proposed Miller Capacitance Cancellation Technique

The proposed MCCT needs to be designed properly to fully realize the Miller capacitance cancellation. This Section discusses the design considerations for MCCT, including the compensation of the non-linearity of the Miller capacitance, the high-frequency performance of the VSC, and the operation region of VIC.
4.4.1. Compensate the Non-Linearity of the Miller Capacitance

It is well known that the value of Miller capacitance changes drastically with the drain to source voltage \( V_{ds} \). As shown in Figure. 4-7 (a), the value of \( C_{gd} \) decreases quickly with \( V_{DS} \). The relationship between \( C_{gd} \) and \( V_{DS} \) is given by [21]:

\[
C_{gd}(V_{ds}) = \frac{c_0}{\sqrt{1+V_{ds}/V_0}}
\]  

(4-37)

Where \( c_0 \) and \( V_0 \) are dimension-related constants, they can be acquired from datasheets. The value of Miller capacitance vs. drain to source voltage is calculated with (36) for a SiC MOSFET (SCT3060AR), where \( c_0 = 700 \, pF, \, V_0 = 1.05 \, V \). As shown in Figure. 4-7 (a), the calculation matches the datasheet very well.

![Miller capacitance value from datasheet](image1)

![Calculation](image2)

Figure 4-7 The non-linearity of Miller capacitance of a SiC MOSFET SCT3060AR. (a) Comparison of the datasheet and calculation (b) Charge-equivalence with two constant capacitance value.
Because of the non-linearity of $C_{gd}$, $G_{MCCT}$ need to change with $V_{ds}$ as well to satisfy (4-33) with a constant $C_{inj}$. In this paper, this is achieved by a charge equivalence technique.

During the switching transient, the Miller current is essentially the total charge transferred through Miller over time [87]. Two constant capacitance values, $C_{cst1}$ and $C_{cst2}$ are used as equivalence to the Miller capacitance under different $V_{ds}$, as shown in Figure. 4-7 (b). The two gains of VSC is given by:

$$\frac{G_1}{G_2} = \frac{C_{cst1}}{C_{cst2}}$$  \hspace{1cm} (4-38)

The total charge of two constant capacitors should be the same as the charge of the Miller capacitance with $V_{ds}$ increases from 0 V to $V_{DC}$. As a result, the values of the two equivalent constant capacitors are given by:

$$\int_0^{V_{div}} C_{cst1} dV_{ds} = \int_0^{V_{div}} C_{gd}(v_{ds}) dV_{ds}$$  \hspace{1cm} (4-39)

$$\int_{V_{div}}^{V_{DC}} C_{cst2} dV_{ds} = \int_{V_{div}}^{V_{DC}} C_{gd}(v_{ds}) dV_{ds}$$  \hspace{1cm} (4-40)

During switching transients, (4-33) is satisfied perfectly when $V_{ds}$ is at $V_{c1}$ and $V_{c2}$, as shown in Figure. 4-7 (b). When $V_{ds}$ changes from 0 V to $V_{DC}$ the remaining Miller effect depends on the charge difference between the equivalent capacitors, namely $C_{cst1}$ and $C_{cst2}$, and the Miller capacitance. To minimize the remaining Miller effect, the charge difference must be minimized. Figure.4-7 (b) shows the charge difference $Q_1$ to $Q_4$ when $V_{ds}$ changes from 0 V to $V_{DC}$. $Q_1$ to $Q_4$ are given by:

$$Q_1 = \int_0^{V_{c1}} C_{gd}(v_{ds}) dV_{ds} - \int_0^{V_{c1}} C_{cst1}(v_{ds}) dV_{ds}$$  \hspace{1cm} (4-41)
\[ Q_2 = \int_{V_{c1}}^{V_{div}} c_{\text{st1}}(v_{ds}) dv_{ds} - \int_{V_{c1}}^{V_{div}} c_{gd}(v_{ds}) dv_{ds} \]  
\[ (4-42) \]

\[ Q_3 = \int_{V_{div}}^{V_{c2}} c_{gd}(v_{ds}) dv_{ds} - \int_{V_{div}}^{V_{c2}} c_{\text{st2}}(v_{ds}) dv_{ds} \]  
\[ (4-43) \]

\[ Q_4 = \int_{V_{c2}}^{V_{DC}} c_{\text{st2}}(v_{ds}) dv_{ds} - \int_{V_{c2}}^{V_{DC}} c_{gd}(v_{ds}) dv_{ds} \]  
\[ (4-44) \]

Figure 4-8 Charge difference comparison with \( V_{\text{div}} \) increases.

From (4-39) and (4-40), \( C_{\text{st1}} \) and \( C_{\text{st2}} \) are given by:

\[ C_{\text{st1}} = \frac{2C_0V_0}{V_{\text{div}}} \left( \sqrt{1 + \frac{V_{\text{div}}}{V_0}} - 1 \right) \]  
\[ (4-45) \]

\[ C_{\text{st2}} = \frac{2C_0V_0}{V_{\text{DC}} - V_{\text{div}}} \left( \sqrt{1 + \frac{V_{\text{DC}}}{V_0}} - \sqrt{1 + \frac{V_{\text{div}}}{V_0}} \right) \]  
\[ (4-46) \]

Solving (4-41) - (4-44) simultaneously,

\[ Q_1 = Q_2 = 2C_0V_0 \cdot \left( \sqrt{1 + \frac{V_{\text{div}}}{V_0}} - 1 \right) - C_{\text{st1}} \cdot V_{c1} \]  
\[ (4-47) \]

\[ Q_3 = Q_4 = 2C_0V_0 \cdot \left( \sqrt{1 + \frac{V_{c2}}{V_0}} - \sqrt{1 + \frac{V_{\text{div}}}{V_0}} \right) - C_{\text{st2}} \cdot (V_{c2} - V_{\text{div}}) \]  
\[ (4-48) \]

Where,
\[ V_{c1} = (V_0 \left( \frac{C_0}{C_{cst1}} \right)^2 - 1 ) \]  \hfill (4-49)

\[ V_{c2} = (V_0 \left( \frac{C_0}{C_{cst2}} \right)^2 - 1 ) \]  \hfill (4-50)

From (4-47) to (4-50), \( Q_1 \) and \( Q_3 \) are functions of \( V_{div} \). To minimize the charge differences, the values of \( Q_1 \) and \( Q_3 \) should have a minimum value at \( V_{div} \). With \( V_{div} \) increases from 0V to \( V_{DC} \), \( Q_1 \) increases and \( Q_3 \) decreases. The minimum value can be achieved when \( Q_1 = Q_3 \), as shown in Figure. 4-8.

The impedance network value can be thusly calculated:

\[ \frac{Z_{Q1}+Z_3}{Z_4} = \frac{C_{cst1}}{C_{cst2}} \]  \hfill (4-51)

The capacitance of the injection capacitor is calculated by:

\[ C_{inj} = -\frac{C_{cst1}}{g_{mQ1} g_{mQ2} R_{inj}} \left( \frac{1+g_{mQ2} R_s}{g_{s1}} \right) \]  \hfill (4-52)

The value of the injection capacitor is the same when calculated with \( C_{cst2} \) and \( g_{s2} \) because of (4-40). In this way, the Miller capacitance could be minimized.

**4.4.2. Improve High-Frequency Performance of The MCCT**

As discussed in Section 4.3, the high voltage gain of the VSC is separated with low voltage gain as long as (4-17) and (4-18) are true. However, at high frequencies, (4-17) may not be true because \( Z_{VD} \) decrease with frequency. There is a high-frequency limit for the VSC. To discuss this high-frequency limit, define the left part of (4-17) as \( Z_{hf} \):

\[ Z_{hf} = \frac{g_{mQ1} Z_3 Z_{VD}}{Z_2+Z_3} \]  \hfill (4-52)
At low frequencies, $Z_{hf}$ has very large value because $Z_{VD}$ has a large value. (3-12) is true. At high frequencies, the impedance $Z_1$ to $Z_4$ in VSC are mainly capacitive. (4-53) can be expressed as:

$$Z_{hf} = \frac{1}{s} \cdot G_{hf}$$  \hspace{1cm} (4-53)

Where $G_{hf} = \frac{g_{mQ1}C_2}{C_1(C_2 + C_3)}$. Based on (4-53), $Z_{hf}$ decreases with a -20dB/dec slope with frequency. When $Z_{hf}$ becomes comparable with $\frac{Z_{VD}}{Z_{Q1}}$, (4-17) is no longer true. In such a situation, the VSC loses the ability to provide a low gain at input high voltage, while the gain of the VIC does not change. Consequently, the high-frequency components of the sampled signal would be injected into the gate loop with a large gain ($>G_{s2}$). If the high-frequency components of the sampled signal, which is the SiC MOSFET drain to source voltage, is large, the injected high-frequency signals will over-compensate the Miller current, causing additional interference.
Figure 4-9 Example of over-compensation during top switch turn-on transient. (a) Without MCCT (b) MOSEFT connects to the MCCT with $G_{hf} < G_{hf-crit}$. (c) MOSEFT connects to the MCCT with $G_{hf} > G_{hf-crit}$.

To avoid the over-compensation, $Z_{hf}$ should be large in the frequency range of the SiC MOSFET voltage spectrum. The spectrum of SiC MOSFET switching waveform decreases with frequency [23]. After the cross frequency $\frac{1}{t_{sw}}$, the magnitude of the spectrum decreases at -40 dB/dec, where $t_{sw}$ is the switching time of the SiC MOSFET. The magnitude of the components higher than $\frac{10}{t_{sw}}$ is very small. To improve high-frequency performance, $Z_{hf}$ should be at least larger than $\frac{Z_{VP}}{Z_{Q1}}$ at all frequencies below $\frac{10}{t_{sw}}$. The $G_{hf-crit}$ is thusly defined as:

$$G_{hf-crit} = 2\pi \cdot \frac{Z_{VP}}{Z_{Q1}} \cdot \frac{10}{t_{sw}}$$  \hspace{1cm} (4-54)

An example is given in Figure 4-9. The induced positive gate voltage due to the turn-on transition of the other switch in a phase-leg configuration is shown in Figure 4-9 (a). The phase-leg circuit is tested under a low power condition (100 V/3A) for safety.
reasons. Figure. 4-9 (b) shows a case where the MCCT is applied to the MOSFET with a $G_{hf} < G_{hf-crit}$. The over-compensation can be clearly observed. The gate voltage is higher than the case without the MCCT due to additional high-frequency signals.

Another case where the same MCCT is applied to the same MOSFET but with a $G_{hf} > G_{hf-crit}$ is shown in Figure. 4-9 (c). Because the $Z_{hf}$ maintain high value at high frequencies. There are no additional high-frequency signals injected to the gate. The parameters of VSC shall be selected so that $G_{hf} > G_{hf-crit}$.

4.4.3. Design Considerations for the VIC

Before Q2 is on, the channel current of Q2 is zero. $C_{gsQ2}$ is charged by $V_{VS}$. A delay time $t_{dQ2}$ is determined by the time constant $\tau_{Q2} = R_s C_{gsQ2}$. The delay time can be reduced by use small value of $R_s$. After Q2 is on, to achieve the function of VIC, Q2 must operate in the saturation region. Namely,

$$V_{dsQ2} > V_{gsQ2} - V_{thQ2}. \quad (4-55)$$

Where $V_{dsQ2}$, $V_{gsQ2}$ and $V_{thQ2}$ are the drain to source voltage, gate to source voltage and threshold voltage of Q2, respectively. The drain to source voltage is:

$$V_{dsQ2} = V_{cc} - i_d(R_{inj} + R_s) \quad (4-56)$$

Substitute (4-23) (4-24) and (4-55) to (4-56), the saturation condition can be calculated as:

$$V_{VSMax} - V_{th} < \frac{V_{cc}(1+g_mR_s)}{g_m(R_{inj}+R_s)+1} \quad (4-57)$$

Where $V_{VSMax}$ is the maximum output voltage of VSC.
\[ V_{VSMax} = V_{dsMax} \cdot G_s^2 + V_{Q1} \]  

(4-58)

Where \( V_{dsMax} \) is the maximum VSC input voltage. \( V_{Q1} \) is given in (4-19). The value of \( R_{inj} \) and \( R_s \) should be selected to satisfy (4-57). At the same time, \( R_s \) should be kept minimum to reduce the delay time before Q2 is turned on.

**Table 4-1. Parameter value of the MCCT**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value/name</th>
</tr>
</thead>
<tbody>
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<td>( C_1 )</td>
<td>VSC capacitor 1</td>
<td>5.1 pF</td>
</tr>
<tr>
<td>( C_2 )</td>
<td>VSC capacitor 2</td>
<td>150 pF</td>
</tr>
<tr>
<td>( C_3 )</td>
<td>VSC capacitor 3</td>
<td>300 pF</td>
</tr>
<tr>
<td>( C_4 )</td>
<td>VSC capacitor 4</td>
<td>1.6 nF</td>
</tr>
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<td>( R_{inj} )</td>
<td>Injection resistor</td>
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<tr>
<td>( R_s )</td>
<td>Source resistor</td>
<td>7.5 ( \Omega )</td>
</tr>
<tr>
<td>( C_{inj} )</td>
<td>Injection capacitor</td>
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<td>( Q2 )</td>
<td>VIC MOSFET</td>
<td>IRLMS1503</td>
</tr>
<tr>
<td>M1, M2</td>
<td>SiC MOSFETs</td>
<td>SCT3060AR</td>
</tr>
<tr>
<td>D1, D2</td>
<td>SiC anti-parallel diodes</td>
<td>IDH20G120C5</td>
</tr>
<tr>
<td>Drivers</td>
<td>Commercial drivers</td>
<td>2SC0108T2Dx</td>
</tr>
</tbody>
</table>
4.5 Simulation and Experiment Results

An MCCT circuit is designed and applied to the SiC MOSFETs in a phase-leg configuration to verify the effectiveness of the proposed circuit. The selected parameters are listed in TABLE 4-1.

4.5.1. Simulation Verification

The simulation is conducted in Ansys Simplorer. The phase-leg circuit consists of two SiC MOSFETs and two SiC Schottky diodes. The power devices are generated with the device characterization tool of the software. Four switching transients are simulated. When being driven, the gate driver voltage is 15 V for the turn-on process and 0 V for the turn-off process. When being off, the gate driver voltage is 0 V.

The four switching states discussed in Section II are firstly simulated under a 500 V/ 20 A condition. The gate resistors are 10 Ω. During the top switch turn-on and turn off transient, the gate voltage of the bottom switch is shown in Figure. 4-10. Figure. 4-11 show that both the positive and negative induced gate voltage are large without the MCCT. With the MCCT added, both positive and negative spikes are effectively suppressed. The magnitude of the positive spike is reduced by more than 85 %, and the magnitude of the negative spike is reduced by more than 90 %. During the bottom switch turn-on and turn-off transient, the drain to source voltage is shown in Figure. 4-11. Because of the reduced Miller platform, the turn-on and turn-off speed are increased in the case with the MCCT. The simulation results verify the analysis in Section 4.3.
4.5.2. Experimental Verification

A double pulse test circuit is built for the measurement. The phase-leg circuit is fabricated with PCB. Two kinds of prototypes are made, one without the MCCT circuit, the other with the proposed MCCT connected to the gates of the SiC MOSFETs. The layout of the main power circuit is the same for the two prototypes.

![Simulated gate voltage waveforms of bottom switch](image1)

(a) Simulated gate voltage waveforms of bottom switch during (a) Top switch turn-on and (b) top switch turn-off

![Simulated drain to source voltage waveforms](image2)

(a) Simulated drain to source voltage waveforms of bottom switch during (a) Turn-on and (b) Turn-off
The switches in the prototypes are SiC MOSFETs and SiC Schottky diodes. A commercial driver (2SC0108T2Dx) is connected to the gate pin and the Kelvin source pin. The turn-on gate voltage is 15 V, the turn-off gate voltage is –8 V. SiC MOSFETs could endure the shoot-through current caused by false triggering in a short time. In the meantime, the gate breakdown caused by the negative gate voltage over-range is non-reversible. As a result, when the device kept off the gate and source terminals are connected with only the gate resistor. The DC decoupling capacitor 20 μF. The load inductor is 2.5 mH.

The prototype and experiment set up is shown in Figure. 4-12. The MCCT circuit is on the bottom side of the board. The DC power source that supplies the power loop is Chroma 62024P-600-8. The DC power supply for the driver and MCCT is RIGOL DP832. A wideband (350 MHz) oscilloscope RIGOL MSO4034 is used to measure the voltage.
Figure 4-12 The bridge-leg circuit under test

Figure 4-13 Measured gate voltage waveform of bottom switch during top switch turn-on transient. (a) Without the MCCT and (b) with the MCCT
Figure 4-14 Measured gate voltage waveform of bottom switch during top switch turn-off transient. (a) Without the MCCT and (b) with the MCCT
Without MCCT

\( V_{ds2} \) (200 V/div)

M1 off
M2 turn-on transient

7.2 V/ns

With MCCT

\( V_{ds2} \) (200 V/div)

M1 off
M2 turn-on transient

10 V/ns
Figure 4-15 Measured gate voltage waveform. (a) Bottom switch during top switch turn-on transient. (b) Bottom switch during top switch turn-off transient.

The SiC MOSFETs used in the prototype have a TO-247 package. It has kelvin gate connections to minimize the influence of common source inductance. The voltage probes connect directly to the package terminals. The low voltage probe used in the experiment is RIGOL PVP21250. The probe tips are connected to the gate and Kelvin source of the MOSFET package. As a result, the error brought by the parasitic inductance of the probe is neglectable. Because the drain to source voltage of the SiC MOSFET is much larger than the gate voltage, an isolated high voltage probe is used to measure the drain and source voltage. Only one of the probes is connected to the circuit during measurement each time to avoid the interference brought by the probe
impedance [22]. In this way, both gate to source and drain to source voltage can be accurately measured.

The prototypes are firstly tested with 500 V DC voltage and 20 A load current. Gate resistors used for turn-on and turn-off are 10 Ω for both top and bottom switches. The gate voltage waveforms of the bottom switch during top switch switching transients are presented in Figure. 4-13 and Figure. 4-14. The comparison in Figure. 4-15 shows that the positive induced gate voltage spikes are effectively reduced with MCCT. Even with 0 V off state driver voltage, the gate voltage is still below the threshold voltage. Figure. 4-14 shows that the negative induced gate voltage is also reduced with the MCCT. Small negative induced gate voltage increases the reliability of SiC MOSFET by avoiding the gate oxide breakdown. As shown in Figure. 4-15 and Figure. 4-16, the drain to source voltage during switching transient is compared. It is shown in Figure. 4-15 and Figure. 4-16 that both turn-on and turn-off speed of the MOSFET with the MCCT are increased. The test results in Figure. 4-13 to Figure. 4-16 present a good agreement with the analysis.

The phase-leg circuit could operate under different DC bus voltage. The induced gate voltage under different DC bus voltage is different. The variation is due to the non-linearity of the Miller capacitance. Figure. 4-16 illustrates the absolute peak values of positive and negative induced gate voltage under different DC bus voltage. The load current in these tests are 20 A. Figure. 4-16 shows that, with the non-linearity of the
Miller capacitance compensated, the proposed MCCT could suppress the induced gate voltage under different DC voltage levels.

![Figure 4-16](image)

**Figure 4-16** Maximum absolute values of the induced gate voltage vs. DC bus voltage  
(a) Positive induced gate voltage  (b) Negative induced gate voltage

To calculate the switching energy, the drain to source voltage and drain current data are exported from the oscilloscope. The voltage and current waveforms are plotted in Figure. 4-17 and Figure. 4-18. Figure. 4-17 shows that the turn-on speed of the case with the MCCT is 20 % faster than the case without the MCCT. Figure. 4-18 shows that the turn-on speed of the case with the MCCT is 50 % faster than the case without the MCCT. The switching energy is calculated by multiplying the $V_{ds}$ and $i_d$. As shown in Figure. 4-19, both turn-on and turn-off switching energy is reduced with the proposed MCCT. The turn-on switching energy is reduced by 17 %, and turn-off switching energy is reduced by 60%. The total switching energy is reduced by 45% with the proposed MCCT. With the reduced switching energy, the SiC MOSFET with the proposed MCCT could operate at high frequency.
The test results in Figure 4-17 to Figure 4-19 present a good agreement with the analysis.

Figure 4-17 Measured drain to source voltage and drain current waveforms of the bottom switch during bottom switch turn-on transient. (a) Without the MCCT and (b) with the MCCT

Figure 4-18 Measured drain to source voltage and drain current waveforms of the bottom switch during bottom switch turn-off transient. (a) Without the MCCT and (b) with the MCCT
Figure 4-19. Comparison of the Turn-on and turn-off switching energy for the case with and without the proposed MCCT.

4.6 Conclusion of Chapter 4

This paper proposed a Miller effect suppression for the SiC MOSFETs in a phase-leg configuration. A Miller current cancellation technique (MCCT) is developed to cancel the Miller current directly. The proposed MCCT equivalently cancels the Miller capacitance. The crosstalk between the top and the bottom switch is suppressed, and the switching speed of the device is increased. Compared to the existing technologies, the proposed technique has three advantages:

1. The proposed technique addresses the Miller capacitance directly. The Miller effect during all four switching-state of a phase-leg configuration can be effectively reduced.

2. The proposed technique can compensate for the non-linearity of Miller capacitance.

3. The circuit requires no driving signal or control strategies. It can be applied to most commercial drivers or integrated inside the power module package.
CHAPTER 5
RADIATED ELECTROMAGNETIC INTERFERENCE MODELING FOR THREE PHASE MOTOR DRIVE SYSTEMS WITH SiC POWER MODULE

5.1 Introduction of Chapter 5

As discussed in previous chapters, SiC MOSFETs have characteristics such as high breakdown voltage, high operating temperature, and low switching power loss, so they are widely used to replace Si IGBTs in high power applications such as electric vehicles and the aviation industry. However, the fast switching speed and the high switching frequency of the SiC power module generate high frequency (HF) EMI noises [91]. The radiated EMI has become the primary factor in preventing the development of power electronics systems with SiC power modules.

In this Chapter, the radiated EMI of a three-phase motor drive system for EV and aircraft applications are analyzed in detail. The modeling of the system is based on three aspects: the noise generated by the gate drivers, the noise source generated by the SiC inverter module, and the noise propagation paths.

In the existing research, it was believed that the noise generated by the driver has little impact on the radiated emission. In [100], the drivers are put in a conductive shield and operated with no inverter connections. The RE (radiated emission) is measured, and it was found that the noise is close to the ambient noise level. However, in the test conditions in [100], the drivers are not connected to the system cables, which are the unintentional antennas that could cause the RE [94]. In a power electronics system, the attached cables are inevitable parts, as shown in Figure 5-1. Besides, in
many EMI standards, the length of the input and output cables is defined in the test. Simply leave the cables out cannot represent the actual EMI performance of the system. In the paper, it is discovered that the switching noise of the driver would couple to the input and output cables and generated considerable RE.

When the power inverter module turns on, the SiC MOSFETs start to switch. The SiC MOSFETs have fast speed, high switching frequency, and severe parasitic oscillations. As a result, the EMI noises generated by SiC power modules are higher in magnitude and are at higher frequencies compared to Si power modules. In previous studies, some research has investigated the radiation mechanisms [92] by modeling the common-mode current or focus on the far-field region [93]. In most EMI standards, radiated EMI is measured with an antenna in an anechoic chamber. The radiated EMI is determined by both the noise source and the unintentional antenna formed by the input and output cables. The noise source and the unintentional antennas were analyzed in [94] and [95]. However, the characteristics of SiC MOSFETs and their impact on the noise source have not been thoroughly discussed. In most studies, the hard-switching waveforms are regards as asymmetrical trapezoidal waveforms [96]. The switching speed is calculated with an equivalent capacitance. At high frequencies where the radiated EMI is concerned, the trapezoidal wave assumption is no longer valid. The small difference in the time-domain waveform could cause a big difference in the HF spectrum. In [97], the possibility of EMI reduction with waveform shaping is discussed.
However, the hard-switching waveforms used as baselines are still under the trapezoidal waveform assumption.

In most EMI/EMC standards, such as MIL-STD-461G [106] and DO-160 [107], the measurement set up for different equipment under test (EUT) is the same. The input cable length, antenna distance, and height of EUT from the ground are the same for all kinds of EUT. Therefore, the EMI noise source of a specific EUT determines its radiated EMI. To investigate the radiated EMI, the accurate modeling of the noise source is crucial. Specifically, in MIL-STD-461G, the limit of the near field RE is also defined. The near field electric field is rarely tested and analyzed in the power electronics system. In this paper, the near electric field is analyzed in detail.

Different from existing literature, this paper proposed an analytical modeling technique that could accurately predict both near-field and far-field radiated EMI. The model considers the impact of the driver, the non-linearity of the junction capacitance of SiC devices, the parasitic inductance inside the module package, the DC voltage, and the load current as well as the cable dimensions.

5.2 EMI Source Generated by the Gate Drivers

As shown in Figure. 5-1, the testing setup of a three-phase motor drive system with SiC power modules consists of three parts: the power module and the driver board, the input and output cables, and the load. The drivers deliver the digital control signal from the DSP to the gate of the SiC MOSFETs. The DSP is a low-power digital chip, while the SiC MOSFETs are high-power devices. It is important to separate the low
power and high power signals. As a result, the drivers of the SiC MOSFETs usually consist of isolated power converters, such as flyback converters [101]. The switching behavior of the flyback converter also generates high-frequency EMI noises [102].

Figure 5-1. Three-phase motor drive system with SiC power module

![Three-phase motor drive system with SiC power module](image)

Figure 5-2. Isolated driver circuit

As shown in Figure 5-2, the secondary ground of the driver is connected to the source terminals of the top and bottom switches in the power module. The noise
produced by the isolated driver is coupled to the input and output cables through this connection. As shown in Figure 5-3, the equivalent noise source of the flyback converter is connected to the input and output cables. The CM noise travels in the input and output cables and generates radiated EMI noise.

Figure 5-3 Driver noise sources and their coupling path

The noise source of the drivers is between the primary and secondary ground of the isolated DCDC converter [103]. Depending on the power supply, the primary ground of the driver could be connected to the DC bus of the system. However, in the case of high-power applications, the DC bus has a very high voltage. An auxiliary power supply is usually used. The negative rail of the auxiliary DC supply is grounded. In this paper, the auxiliary DC power supply is put in the shield box.

In the beginning, only the driver power supply is on, and the drivers are working. The inverter module is not working. The RE is measured with the test set up described in Section 5-5.
Figure 5-4 Measure RE with only the drivers working.

As shown in Figure. 5-4, the near electric field generated by the drivers is high. Even when the inverter power module is not working, the measured RE has already higher than the limit of MIL-STD-461G standard. When the input and output cables disconnected, as shown in Figure. 5-4, the RE significantly reduced. It proves that it is the input and output cables that generate the RE. The noise generated by the driver should be evaluated with the input and output cables connected.

5.3 EMI Source Modeling Based on Switching Transient Analysis of SiC MOSFETs

The noise sources in this system are identified in previous studies [94] – [96] as the pulsating voltage of the output terminals of the power module. The pulsating voltage of the output terminals generates common-mode current travels through the input and output cables, which are unintentional antennas and radiate electric field. To accurately
predict the radiated EMI, it is crucial to model the switching waveforms accurately. The high-frequency characteristics of the EMI noise source are determined by the rising and dropping slope in the time domain waveforms. Therefore, in this paper, the switching transient is analyzed.

The turn-on process of the MOSFET is shown in Figure 5-2 (a). Before the driver voltage reaches the threshold voltage of the device, the drain current and the drain to source voltage stay constant. During the current rising state, the gate to source voltage, drain current, and the drain to source voltage are given by:

\[
\frac{V_H - V_{gs}}{R_g} = C_{iss} \frac{dV_{gs}}{dt} - C_{gd} \frac{dV_{ds}}{dt}
\]

\[
V_{ds} = V_{DC} - L_{ccl} \frac{di_d}{dt}
\]

\[
i_d = g_m (V_{gs} - V_{th})
\]

Where,

\[
C_{iss} = C_{gs} + C_{gd}
\]

\[
L_{ccl} = L_d + L_s
\]

Solving (5-1) – (5-5), the voltage drop during \((t_1 - t_2)\) is given by:

\[
V_{ds} = V_{DC} - L_{ccl}(g_m(V_H - V_{th}) e^{-\frac{t - t_0}{\tau_a}} \cdot \left(\frac{\tau_b}{\tau_a} + \frac{1}{\tau_b}\right) \cdot \sin\left(\frac{t - t_0}{\tau_b}\right))
\]

Where \(\tau_a = \frac{2 \tau_1}{\tau_2}, \tau_b = \frac{2 \tau_1}{\sqrt{4 \tau_1 - \tau_2}}, \tau_1 = L_{ccl} C_{gd} R_g g_m, \tau_2 = R_g C_{iss}\). The parameters in (5-6) are determined by the parasitic inductance inside the package, junction.
capacitance of the power devices, the transconductance of the power devices, and the gate resistors.

From (5-6), the voltage of the MOSFET starts to drop before the Miller plateau. The voltage drop during \((t_1 - t_2)\) is caused by the parasitic inductance. Because the voltage on the parasitic inductance can change instantly, the voltage dropping slope during this period is considerably large. Depending on the value of parasitic inductance, the voltage drop could dominant the whole turn-on process [98].

![Diagram](a) (b)

Figure 5-5 Turn-on transients of the bottom SiC MOSFET in one phase-leg of the power module (a) turn-on transient waveforms and (b) circuit representation
Figure 5-6 Turn-off transients of the bottom SiC MOSFET in one phase-leg of the power module (a) turn-off transient waveforms and (b) circuit representation

During \((t_2 - t_3)\), there are two scenarios. The first scenario is that after the voltage drop before \(t_2\), the MOSFET operates in the linear region. The gate voltage has already lost control of the channel current. In this scenario, the voltage drop process is completed.

In the second scenario, the MOSFET still operates in the saturation region after \(t_2\). In this case, the voltage decreasing speed is controlled by the Miller plateau \([99]\), which is given by:

\[
\frac{dV_{ds}}{dt} = -\frac{V_H - V_M}{R_g C_{gd}}
\]  

(5-7)

Where

\[
V_M = \frac{I_{ch}}{g_m} + V_{th}
\]  

(5-8)

137
$I_{ch}$ is the channel current of the MOSFET. $V_M$ is the Miller plateau gate voltage. $V_{th}$ is the threshold voltage. $g_m$ is the transconductance.

From (5-7), the turn-off voltage slope depends on the Miller capacitance $C_{gd}$. The Miller capacitance is a highly non-linear capacitance, the value of which changes drastically with $V_{ds}$. The relationship between the Miller capacitance and the drain to source voltage is given by:

$$C_{gd} = \frac{c_0}{\sqrt{1+V_{ds}/V_0}} \quad (5-9)$$

Where $c_0$ is the capacitance when $V_{ds}$ is 0, $V_0$ is a dimension-related constant. Both values can be obtained from the datasheet. Substitute (5-6) to (5-5), the $V_{ds}$ during the Miller plateau can be solved as:

$$V_{ds} = V_0 \left( \frac{V_M-V_H}{2R_gV_0c_0} \cdot t + \sqrt{1 + \frac{V_{DC}}{V_0}} \right)^2 - 1 \quad (5-10)$$

From (5-6) - (5-10), two voltage slopes are identified during turn-on transient. The switching speed is determined by the gate resistance, junction capacitance parasitic inductance, and the load current. The HF noise spectrum of the voltage waveform depends on all of the slopes.

The turn-off process is shown in Figure. 5-3 (a). During the turn-off process, the voltage starts to change after the gate voltage reaches the Miller plateau. In the meantime, the current is clamped at $I_{const}$. As a result, the voltage during $(t_5 - t_6)$ is controlled by the Miller plateau. The voltage slope during turn-off transient is given by:
\[ V_{ds} = V_0 \left( \left( \frac{V_M}{2R_g V_0 C_0} \cdot t + 1 \right)^2 - 1 \right) \]  \hspace{1cm} (5-11)

Figure 5-7 Comparison between the switching waveform under the trapezoidal assumption and the proposed analytical waveform. (a) Turn-off transient and (b) turn-on transient

The parasitic oscillation after \( t_6 \) has been thoroughly discussed in [96]. This paper will not repeat the process. From (5-6), the impact of junction capacitance and parasitic inductance is clearly shown. For SiC MOSFETs, \( C_{iss} \) and \( C_{gd} \) are much smaller than Si IGBTs under similar power ratings. The \( di_a/dt \) of SiC MOSFETs is higher than Si IGBTs. As a result, the voltage drop caused by the parasitic inductance during the turn-on process is more prominent. The driver no longer controls the turn-on voltage slope. From (5-10) and (5-11), the voltage slopes during the Miller plateau is a squared function of time. The switching speed increases with the DC voltage. The switching speed does not only depend on the load current and gate resistors, as commonly assumed.
The comparison between the calculated switching waveforms with the traditional modeling technique and the proposed technique is shown in Figure 5-4. Both waveforms are calculated based on the same datasheet.

As shown in Figure 5-4, the proposed technique could model the switching slope with more detail. The different switching slopes can be clearly observed.

5.4 Near Electric Field Modeling Based on EMI Noise Propagation Mechanism

The analysis in Section 5.2 focused on the EMI noise sources. In this Section, the noise propagation path is discussed. The mechanisms of RE are modeled. The noise generated by the drivers and power module propagates through the input and output cables. In existing research, it is believed that the radiation EMI is caused by the common-mode current in the cables. The radiation model considers the input and output cables as transmission line antennas. The accuracy of the RE model depends on accurate modeling of the common-mode current. However, in the case of the near electric field, the conductive common mode current is not the only radiation source. In the MIL-STD-461G standard, the near electric field is measured 0.9 m away from the EUT. In the frequency range of 150 kHz – 30 MHz, the wavelength is much longer than the distance. The measured E field is the sum of radiated E field and reactive E field [103].

Figure 5-8 shows the equivalent circuit model of the common-mode noise. The noise source of the inverter module is between the output terminal and the bus bars. The bus bars are connected to the input cables. It is well known that the radiated EMI is
caused by the common-mode noise instead of differential mode noise [103]. The input and output cables are modeled as transmission lines. $Z_{LISN}$ is the LISN grounding impedance. In this case, it is 50 ohms. $Z_{gL}$ is the load ground impedance. $Z_{BH}$ is the impedance between the bus bars and the heatsink. $Z_{MH}$ is the impedance between the power model output and the heatsink. $Z_{gH}$ is the grounding impedance of the heatsink. $V_{cm}$ is the common mode noise source, it is the spectrum of the switching waveform derived in Section 5.3.

In Figure 5-8 (b), $Z_i$ and $Z_o$ are the input and output impedance seen from the power module, respectively. They can be calculated with:
Where $Z_{s0}$ and $Z_{L0}$ are the characteristic impedance of the input and output transmission lines, respectively. $l_{in}$ and $l_{out}$ are the length of the input and output cables, respectively. (5-12) and (5-13) are derived from the terminated lossless transmission line model [104].

$Z_{BH}$, $Z_{MH}$ and $Z_{gH}$ have a Y connection. Figure 5-8 (b) can be transformed to the equivalent circuit as shown in Figure 5-9 by conducting the Y to delta transformation.

![Common mode equivalent circuit after Y to delta transformation](image)

In Figure. 5-9, $Z_{d1} = \frac{Z_{BH}Z_{MH}+Z_{BH}Z_{gH}Z_{MH}}{Z_{MH}}, Z_{d2} = \frac{Z_{BH}Z_{MH}+Z_{BH}Z_{gH}+Z_{gH}Z_{MH}}{Z_{BH}}, Z_{d3} = \frac{Z_{BH}Z_{MH}+Z_{BH}Z_{gH}+Z_{gH}Z_{MH}}{Z_{gH}}$. Based on Figure. 5-9, the voltage on the unintentional antenna formed by the input and output cables can be calculated:

$$V_i = -V_{cm} \cdot \frac{Z_{AC}}{Z_{AC}+Z_{DC}} \quad (5-14)$$
\[ V_o = V_{cm} \cdot \frac{Z_{DC}}{Z_{AC} + Z_{DC}} \]  

(5-15)

Where,

\[ Z_{DC} = \frac{Z_1 Z_{d1}}{Z_l + Z_{d1}} \]  

(5-16)

\[ Z_{AC} = \frac{Z_o Z_{d2}}{Z_o + Z_{d2}} \]  

(5-17)

From (5-12) – (5-17), the voltage on the unintentional antennas is determined by the CM noise source and the grounding impedance of input, heatsink, and the load.

Based on Ampere's law with Maxwell's addition, the total current of the cable is the sum of the conductive current and the displacement current. In most antenna and radiation EMI modeling research, only the conductive current is considered. However, because the near electric field is measured with a rod antenna close to the EUT and attached cables, the displacement current can directly be coupled to the receiving antenna. As shown in Figure. 5-10 (a), for RE measurement, the antenna is located very close to the EUT. In MIL-STD-461G, the antennas are placed 1 m away from the EUT. For frequencies under 30 MHz, the distance is smaller than the quarter of the wavelength. At the same time, As shown in Figure.5-8 (a), the length of the input and output cables is relatively long. The distance between the receiving antenna and the power electronics system is both electrically and spatially short. The far-field assumptions made in the antenna modeling are no longer true. As a result, the accurate way to modeling the near electric field would be to consider the electric field generated by both conductive current and the displacement current.
As shown in Figure 5-9, the voltage on the input and output antenna can be calculated based on the cable and load impedance. After the voltage at the terminal is calculated, the E field of the cable can be calculated. In this way, the problem can be simplified. The E field can be calculated based on the simple geometric structure shown in Figure 5-11 (a). The output cable equivalent circuit is shown. The E field of each cable can be calculated. Because in the test, the chamber table and floor are covered
with conductive materials. In this case, copper planes. The E field will be reflected by the ground. The total E field should consider the image of each source. As shown in Figure 5-11, (b), the total E field at the observation point P is the vector summation of the E field generated by each cable as well as their images.

Figure 5-11 System simplification. (a) Output cable equivalent circuit (b) System with input and output antennas as well as their images.
As shown in Figure. 5-11 (a), the output cable is a terminated transmission line. The line extends in the z-direction. The voltage and current distribution along the line can be calculated:

\[ V_o(z) = V_o^* e^{-j\beta z} + \Gamma e^{j\beta z} \quad (5-18) \]

\[ I_o(z) = \frac{V_o^*}{Z_{L0} + Z_{gl}} (e^{-j\beta z} + \Gamma e^{j\beta z}) \quad (5-19) \]

Where,

\[ \Gamma = \frac{Z_{gl} - Z_{L0}}{Z_{gl} + Z_{L0}} \quad (5-20) \]

\( \Gamma \) is the reflection coefficient.

The displacement current flows through the distributed capacitance between the cable and the ground. Because the voltage of the cable is changing, the displacement current flows from the cable to the ground. A simulation is conducted in HFSS, with a voltage excitation added to the output cable, the E field vectors are observed. As shown in Figure. 5-12 (a), the E field of the cable can be observed to be flowing towards the ground.

Based on (5-18), the voltage on the cable changes with length. Therefore, to calculate the E field, a short segment of the cable is considered. The segment length is assumed to be very small that the voltage of the segment does not change with length. As shown in Figure. 5-12 (b), the E field of the segment is equivalented by a point charge \( Q_0 \) and its image \(-Q_0\). The charge is given by:

\[ Q_0 = C_0 V_0(z) \quad (5-21) \]
Figure 5-12 E field generated by the displacement current. (a) E field vector from simulation (b) E field of a cable segment.

Where $C_0$ is the capacitance of this transmission line segment. $V_0(z)$ is the voltage on this cable segment. Based on the transmission line theory [104], the characteristic capacitance of the transmission line above the ground plane is given by:

$$C_0 = \frac{2\pi \varepsilon_0}{\ln(2h/r_0)}$$  \hspace{1cm} (5-22)
Where \( h \) is the height between the cable and the ground plane, \( r_0 \) is the cable radius. \( \varepsilon_0 \) is the permittivity of the free space. Based on the coordinate system shown in Figure 5-13, the E field can be calculated.

![Diagram of E field calculation for a cable that extends in the z-direction](image)

Figure 5-13 E field calculation for a cable that extends in the z-direction

\[
E_+ = \frac{Q_0 r_1}{2\pi \varepsilon_0 r_1^2} \tag{5-23}
\]

\[
E_- = -\frac{Q_0 r_2}{2\pi \varepsilon_0 r_2^2} \tag{5-24}
\]

Where \( E_+ \) and \( E_- \) are the E field generated by the cable segment and its image, respectively. The total E field is the summation of \( E_+ \) and \( E_- \). Consider \( E_+ \) first, solving (5-18) - (5-23) simultaneously, the E field is given by:

\[
E_R = \int V_0 \frac{e^{j\beta z} + r_0 e^{j\beta z}}{(1 + \gamma) \cdot \ln \left( \frac{2R}{r_0} \right)} \cdot \frac{R}{(Z^2 + R^2)^{\frac{3}{2}}} \, dz \tag{5-25}
\]

\[
E_R = \int V_0 \frac{e^{-j\beta z} + r_0 e^{-j\beta z}}{(1 + \gamma) \cdot \ln \left( \frac{2R}{r_0} \right)} \cdot \frac{Z}{(Z^2 + R^2)^{\frac{3}{2}}} \, dz \tag{5-26}
\]

\[
E_{total+} = \sqrt{E_R^2 + E_Z^2} \tag{5-27}
\]
$E_R$ and $E_Z$ are the E field in R direction and Z direction, respectively. The total E field should be the vector summation, as shown in Figure. 5-11 (b).

The E field generated by the current has been solved in [103] and [105]. In this paper, the derivation process will not be repeated.

5.5 Parameter Extraction

From (5-6) – (5-11), the accuracy of the proposed source model highly depends on the accuracy of the parasitic inductance and parasitic capacitance. At the same time, the near electric field model depends on the load and transmission line impedance. In this paper, the parasitic parameters are extracted with FEA software.

As shown in Figure. 5-14, the 3D model of the SiC power module used in the motor drive system is built and simulated. The parasitic parameters are extracted with Ansys Q3D with the same methods used in [95]. The parasitic inductance matrix is imported into Ansys Simpler for circuit simulation.

In the simulation, the power module and the drivers are enclosed in a metal box, just like the setup in the experiment. The setup is shown in Figure. 5-6. The parasitic capacitance between the power module and the heatsink is also extracted.

The LISN, load, and cable impedance is measured with an impedance analyzer for frequency up to 50 MHz.
Figure 5-14 (a) Three-phase SiC power module used in the experiment (b) 3D model for parameter extraction (c) circuit representation

5.4 Experimental Verification

The simulation and experiments are firstly done with a single-phase circuit with a double pulse tester circuit. The power module is tested under 300 V/8 A condition and 600 V/8 A condition. The time-domain waveform is calculated with the extracted parameters and compared with the measured waveforms.
Under the 300V/8A testing condition, the proposed waveform is compared with measured waveforms. As shown in Figure 5-16, the analytical model matches the measured waveform very well under different testing conditions.

The system is then tested under the 600V/8A condition. With the traditional model, the change in DC voltage cannot be correctly modeled. With the proposed model, on the other hand, the switching waveform can be modeled correctly with the same sets of equations. As shown in Figure 5-17, the analytical results match the measurement very well.

![Diagram](image)

Figure 5-15 (a) Power module and heatsink in exploded view (b) Power module and heatsink in the metal box
The motor drive system is then tested under 300 V and 600 V DC voltage conditions with a switching frequency of 160 kHz SWPM driving. The voltage spectrum comparisons between the proposed model, the traditional model, and the measured waveform are shown in Figure 5-18 and Figure 5-19. From Figure 5-18 and Figure 5-19, the switching waveform comparison between the proposed analytical measurement result under a 300 V/8A testing condition. (a) Turn-off transient and (b) turn-on transient.

Figure 5-16 Switching waveform comparison between the proposed analytical measurement result under a 300 V/8A testing condition. (a) Turn-off transient and (b) turn-on transient.
the proposed model can catch the measured waveform up to 1 GHz. The trapezoidal waveform can match the measured waveform up to 10 MHz. With the noise source accurately modeled, the radiated EMI can be predicted based on the proposed model.

Figure 5-17 Switching waveform comparison between the proposed analytical measurement result under a 600 V/8A testing condition. (a) Turn-off transient and (b) turn-on transient
The radiated EMI is measured in an anechoic chamber, as shown in Figure 5-20. The power module, driver circuit, and heatsink are enclosed in a metal box. For frequency under 30 MHz, the E field is measured with a rod antenna. For frequencies above 30 MHz, the E field is measured with a biconical antenna. The setup is defined in the MIL-STD-461G requirement. The distance between the antenna and the power
module is 1 m. The near electric field in the frequency range 150 kHz to 30 MHz is measured.

The E field at the center of the rod antenna is calculated with (5-25) - (5-27). The noise sources are the calculated spectrum as shown in Figure.5-18 and Figure. 5-19. The motor drive system is tested with RL load. Three-phase resistors and inductors with Y connection are used as the load. A 120 Hz modulation frequency sine wave is generated by the inverter. The output phase current is shown in Figure. 5-20.

![Phase current under RL load](image)

Figure 5-20 Phase current under RL load

The calculated near electric field is compared with the measured electric field in Figure. 5-21. The calculated results match the measurement very well. At frequencies close to 30 MHz, the parasitic resonance of the load and LISN impedance have an impact on the voltage distribution. The accuracy of the proposed model depends on the accuracy of the high-frequency impedance model. In this calculation, a simple ESL EPC high-frequency model is used for the load, which results in a certain level of a mismatch at high frequencies.
Figure. 5-22 shows the calculated RE when only the conductive current is considered. As shown in Figure. 5-22, the near electric field generated by the conductive current is very small. The prediction based on the conductive current has a huge difference when compared with measurement, especially for low-frequency RE. This is because SiC MOSFETs have a high switching frequency. The noise source generated by the SiC power module has high voltage spectral components at the frequency range of 150 kHz to 30 MHz. The displacement current generated by this pulsating voltage is the main source of near electric field emission. As a result, the near field RE prediction should be based on the pulsating voltage (displacement current) analysis instead of the conductive current analysis. The two would result in opposite conclusions.

Figure 5-21 Comparison between the measured RE and the calculated RE.
For example, when the cable is grounded with a small impedance, the conductive current is high because of the small loop impedance. However, the displacement current will increase because the voltage across the cable is very small. On the other hand, when the cable termination is opened, the conductive current will be very small, assuming the line is shorter than the quarter wavelength. But the voltage will be large. A simple verification is shown in Figure. 5-23.

![Graph showing calculated and measured E fields](image_url)

**Figure 5-22** Calculated E where only the conductive current is considered.

Figure. 5-23 shows the measure RE when only the driver is working. Case 1 is when the LISN is grounded with a 50-ohm impedance, case 2 is LISN open circuit. From Figure. 5-23, when the LISN is opened, the conductive current is very small. However, the measured RE is much higher than case 1. This proves that the near field RE is mainly caused by the displacement current of the cables.
The far-field RE in this thesis is modeled with HFSS simulation. The far-field antenna model is studied extensively in other papers. The measurement in this paper is to verify the benefit of the proposed noise source model. As discussed in Section 5.3, the proposed noise source model has good accuracy at high frequencies.

![Graph comparing measured RE with LISN opened and terminated with 50 Ohm resistor.](image)

Figure 5-23 Comparison of the measured RE with LISN opened and terminated with 50 Ohm resistor.

The noise source modeled with the traditional model and proposed modeling technique is transformed into a spectrum by FFT. The gain of the unintentional antenna formed by the input and output cables is obtained in Ansys HFSS simulation. By multiplying the antenna gain and the noise source spectrum, the E field can be calculated.

The measured radiated and calculated E field is shown in Figure. 5-25 and Figure. 5-26. The RE is measured with a biconical antenna for frequencies higher than 100 MHz. As shown in Figure.5-25 and Figure 5-26, the proposed model can accurately
predict the radiated EMI. The error is less than 5 dB. The noise source modeled with the traditional technique, on the other hand, has more than 20 dB difference compared to the measured radiated EMI noise. Since the antenna gain is the same in both calculations, the underestimated radiation EMI in the traditional model is caused by the inaccurate noise source modeling.

Figure 5-24 Radiated EMI measured set up
Figure 5-25 Comparison between the E field calculated by the proposed model and measurement result. (a) 100MHz – 400MHz and (b) 400MHz – 1GHz
Figure 5-26 Comparison between the E field calculated by the traditional model and measurement result. (a) 100MHz – 400MHz and (b) 400MHz – 1GHz

5.5 Conclusion of Chapter 5

In this paper, an analytical modeling technique is proposed that could accurately predict the radiated EMI for a motor drive system with SiC power modules. The model firstly focused on the noise sources. The source generated by the inverter gate drivers and the coupling path is studied first. After that, the noise source generated by the inverter switching is analyzed. The proposed technique could accurately predict the time domain voltage switching waveform. From the time domain waveform, the spectrum of the radiated EMI noise source is calculated with FFT. The mechanisms of the near electric field emission are investigated in detail. It is revealed that the main contributor of the near field RE is the displacement current generated by the pulsating voltage. The analysis is verified with the experiment. The proposed modeling technique has the following advantages: 1) The RE contribution of the gate drivers is first identified. 2) The
non-linearity of the junction capacitance is considered. 3) The impact of parasitic inductance on the radiated EMI noise source is identified. 4) The main contributor to the near field is identified. Based on the proposed analytical model, the near field RE can be accurately modeled. Besides, the noise reduction methods can be developed based on the model since the radiation mechanisms are analyzed in detail.
CHAPTER 6
CONCLUSIONS

The electromagnetic interference issues are very important considerations in power electronics systems. With the emerging of wide bandgap power devices, the EMI becomes an even more serious concern. The EMI issues in the power electronics systems with wide bandgap power devices have different forms. Different from much other research where only the EMI standards are concerned, in this dissertation, the root causes of EMI are investigated in detail. The EMI within the power module package, the EMI that concerns the driver, the EMI that concerns the peripheral electronics circuits as well as the EMI that concerns the system are all investigated.

This dissertation focuses on the EMI issues brought by the nature of wide bandgap power devices. The root causes of EMI at different levels are identified and modeled. Reduction techniques that can reduce the EMI while maintaining a low cost and high efficiency. The main objective of this dissertation is to improve the EMI performance of the power modules with WBG power devices without having to sacrifice the advantage of WBG power devices. This dissertation starts from theoretical analysis and builds an analytical model for each EMI-related issue and proposed solutions based on the analysis. The contributions of this dissertation are summarized below:

1) On the package level. The parasitic inductance that causes the voltage overshoot and oscillation is modeled. In particular, the mutual inductance that is usually neglected in other research has been studied in detail.
2) A complete evaluation process is built in this paper based on the parasitic inductance model. By integrating the analytical model and FEA software, the evaluation process can provide accurate and detailed evaluation for power modules.

3) A mutual inductance cancellation technique is proposed for the multichip power modules. The technique can reduce the total power loop inductance without increasing fabrication difficulty. The proposed layout could reduce the related EMI issues, including voltage overshoot and oscillation, crosstalk, and near field emission.

4) A Miller capacitance cancellation technique is proposed. The MCCT technique can equivalently cancel the Miller capacitance. Consequently, the crosstalk effect in the bridge leg configuration circuit is eliminated. The Miller platform during the switching transient is reduced. The switching speed of the power devices can be further increased to reduce switching loss.

5) The radiated EMI is investigated for three-phase motor drive systems with SiC MOSFETs. The radiated emission source is modeled in the time domain. The impact of the non-linearity junction capacitance and the power loop inductance on the radiated EMI is firstly discussed in detail. The main contributor to the near electric field is identified. The model could accurately predict the radiated EMI at a frequency range from 150 kHz to 1GHz.
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BIOGRAPHICAL SKETCH

Boyi Zhang was born in Beijing, China. He received the B.S degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2015, and the M.S. degree in electrical and computer engineering from the University of Florida, Gainesville, FL, USA, in 2017. He has been working as a research assistant in the power electronics and electrical power research lab, the University of Florida since 2017. He finished his work in spring 2021. He received his Ph.D. from the University of Florida in 2021. His research interests include electromagnetic interference, wide bandgap power device packaging, and magnetic components.