To my family
ACKNOWLEDGMENTS

First of all, I would like to appreciate my advisor and supervisory committee chair, Dr. Fan Ren. Thanks for his broad and profound knowledge, patience and encouragement through my Ph.D. study. The completion of this work would not have been possible without the guidance from Dr. Fan Ren. He has always been there to provide technical and personal support whenever I had problems. He has treated me like his kid, and provided an excellent academic atmosphere for me to perform my research. His education and dedication in the past three years have been priceless and will benefit my future life.

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<td>2DEG</td>
<td>2-Dimensional Electron Gas</td>
</tr>
<tr>
<td>AES</td>
<td>Auger Electron Spectroscopy</td>
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<tr>
<td>ALD</td>
<td>Atomic Layer Deposition</td>
</tr>
<tr>
<td>AlGaN</td>
<td>Aluminum Gallium Nitride</td>
</tr>
<tr>
<td>AlN</td>
<td>Aluminum Nitride</td>
</tr>
<tr>
<td>BOE</td>
<td>Buffer Oxide Etchant</td>
</tr>
<tr>
<td>BSD</td>
<td>Back Scattering Electron Detector</td>
</tr>
<tr>
<td>CI</td>
<td>Contact Inclusion</td>
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<td>C-V</td>
<td>Capacitance-Voltage</td>
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<tr>
<td>DLTS</td>
<td>Deep-Level Transient Spectroscopy</td>
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<tr>
<td>DRIE</td>
<td>Deep Reactive Ion Etching</td>
</tr>
<tr>
<td>$E_c$</td>
<td>Conduction Band Edge</td>
</tr>
<tr>
<td>EDX</td>
<td>Energy Dispersive X-Ray Spectroscopy</td>
</tr>
<tr>
<td>$E_v$</td>
<td>Valence Band Edge</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
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<tr>
<td>FLOODS</td>
<td>FLorida Object Oriented Device Simulator</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
</tr>
<tr>
<td>HJ</td>
<td>HeteroJunction</td>
</tr>
<tr>
<td>ICP</td>
<td>Inductively Coupled Plasma</td>
</tr>
<tr>
<td>InAlN</td>
<td>Indium Aluminum Nitride</td>
</tr>
<tr>
<td>IR</td>
<td>Infrared</td>
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<tr>
<td>I-V</td>
<td>Current-Voltage</td>
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<tr>
<td>L&lt;sub&gt;DG&lt;/sub&gt;</td>
<td>Drain to Gate Distance</td>
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<tr>
<td>L&lt;sub&gt;DS&lt;/sub&gt;</td>
<td>Drain to Source Distance</td>
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<tr>
<td>L&lt;sub&gt;GS&lt;/sub&gt;</td>
<td>Gate to Source Distance</td>
</tr>
<tr>
<td>LOR</td>
<td>Lift-Off Resist</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
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<tr>
<td>MISHEMT</td>
<td>Metal Insulator Semiconductor High Electron Mobility Transistor</td>
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<tr>
<td>MOCVD</td>
<td>Metal Organic Chemical Vapor Deposition</td>
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<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
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Ni  Nitrogen Interstitial
NSS  Surface States Density
ODEPR  Optically Detected Electron Paramagnetic Resonance
OM  Optical Microscope
PAC  Photoactive Compound
PEALD  Plasma-Enhanced Atomic Layer Deposition
PECVD  Plasma-Enhanced Chemical Vapor Deposition
PMGI  Poly(methyl glutarimide)
PMMA  Poly(methyl methacrylate)
PPC  Persistent Photocapacitance
PR  Photo Resist
Rc  Contact Resistance
RI  Refractive Index
Rs  Sheet Resistance
RT  Transfer Resistance
SBH  Schottky Barrier Height
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<td>SD</td>
<td>Secondary Electron Detector</td>
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<tr>
<td>SEM</td>
<td>Scanning Electron Microscopy</td>
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<tr>
<td>SiC</td>
<td>Silicon Carbide</td>
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<td>SRIM</td>
<td>Stopping and Range of Ions In Matter</td>
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<td>SS</td>
<td>Subthreshold Swing</td>
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<tr>
<td>TCAD</td>
<td>Technology Computer Aided Design</td>
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<td>TEM</td>
<td>Transmission electron microscopy</td>
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<tr>
<td>TLM</td>
<td>Transmission line measurement</td>
</tr>
<tr>
<td>TMA</td>
<td>Trimethyl Aluminum</td>
</tr>
<tr>
<td>UD</td>
<td>Under Development</td>
</tr>
<tr>
<td>UV</td>
<td>Ultra Violet</td>
</tr>
<tr>
<td>$V_{Ga}$</td>
<td>Gallium Vacancy</td>
</tr>
<tr>
<td>$V_H$</td>
<td>Hall voltage</td>
</tr>
<tr>
<td>$V_N$</td>
<td>Nitrogen Vacancy</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>Threshold voltage</td>
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<tr>
<td>XPS</td>
<td>X-Ray Photoelectron Spectroscopy</td>
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Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

FABRICATION AND CHARACTERIZATION OF GAN-BASED HIGH ELECTRON MOBILITY TRANSISTORS

By

Ya-Hsi Hwang

May 2015

Chair: Fan Ren
Major: Chemical Engineering

Aluminum nitride (AlN) was employed as a gate insulator and a passivation layer. By introducing AlN as the gate insulator, the gate modulation can be extended from 2 V to 4 V, for a Schottky gate HEMT. Moreover, the subthreshold leakage current was suppressed to 1.13 nA/mm and thus the on/off ratio was increased to 3.3E8. Besides reducing the leakage current, the effectiveness of passivation was observed. The $I_{DS}$ only showed a 7% dispersion at 100kHz. In addition, off-state drain breakdown voltage ($V_{BR}$) over 2000 V and specific on resistance of 10.9 m$\Omega$-cm$^2$ at drain to gate distance of 37.5 $\mu$m were achieved.

The effects of proton, gamma and electron irradiation on AlGaN / GaN HEMT DC performance were investigated. For proton irradiation, the mechanism of $V_{BR}$ improvement was investigated through backside proton irradiation. The result indicating the increase of $V_{BR}$ was from the reduction of peak electric field on the gate edges due to the extra charges created by irradiated defects. For gamma irradiation, AlGaN/GaN HEMTs were irradiated at doses of 50, 300, 450, or 700 Gy at a fixed energy of 10MeV. After irradiation, $I_{DS}$ proportionally increased with the dose due to the increase of mobility and reached a maximum of 10% with a dose of 700
For electron irradiation, the capacitance-voltage curve shifted positively after irradiation due to the increase of deep acceptor traps in the barrier/interface region. In AlGaN/GaN/Si transistors, the increases of deep barrier/interface traps with activation energy of 0.3, 0.55, 0.8 eV were observed. These increases correlated with the current dispersion at gate lag measurement.

Novel structure with a backside metal via under the active area of the HEMT was also proposed. It is found out by simulations that the thermal resistance decreased 17% by removing the thermal resistive nucleation layer and filling the via with Cu. Besides, the maximum junction temperature could be decreased from 146°C to 120°C at a power density of 5 W/mm. Furthermore, $V_{BR}$ could be improved by 10% upon connecting the via with the front-side gate. By biasing the backside gate at -25 V, $V_{BR}$ could be improved by 40%.
CHAPTER 1
INTRODUCTION

1.1 Background

1.1.1 Introduction to High Electron Mobility Transistors

Transistor, a three-terminal device which can be used as a switch or an amplifier, is viewed as the most important invention in the 20th century. It is composed of a semiconductor material and at least three electrodes, which are source (S), drain (D) and gate (G) to connect to the external circuit. Source and drain electrodes are Ohmic contacts which conduct current. Gate is either a Schottky contact or a metal-insulator-semiconductor contact which controls the conductivity of the channel. The drain-source current ($I_{DS}$) can be modulated by varying the change of gate voltage ($V_G$), and thus amplify the signal changing at gate electrode. The most common semiconductor material is silicon. Although Si technology is relatively cheap and matured, it can’t meet the requirements of high power electronics such as high breakdown voltage. III-V composite materials such as AlGaN / GaN or InAlN / GaN heterojunctions start to get more attention because of their superior material properties such as thermal stability, chemical stability, high electron mobility, high breakdown electric field, high saturated drift velocity, and high radiation tolerance. Thus, GaN based HEMTs are extremely suitable for high power and high frequency applications such as space, satellite or military technologies. Table 1-1 shows the summary of material properties of Si and AlGaN / GaN heterojunction.

The formation of AlGaN / GaN high electron mobility transistors (HEMTs) is by employing AlGaN as barrier layer on GaN as buffer layer. The energy band gap of $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ and GaN are 4.05 eV and 3.4 eV, respectively. The band gap difference between AlGaN and GaN allows the 2 dimensional electron gas (2DEG) channel to be formed at the AlGaN/GaN interface. Because of the piezoelectric polarization and spontaneous polarization, the 2DEG
electron sheet density could be up to $10^{13}$ cm$^{-2}$ even without doping. Figure 1-1 shows the schematic view of the 2DEG and the energy band gap diagram of Al$_{0.25}$Ga$_{0.75}$N and GaN heterojunction. In other words, unlike traditional Si FETs, the carriers in 2DEG channel will not be scattered by the impurity because no impurity in 2DEG channel is needed to generate carriers. This characteristic guarantees the high electron mobility (~1400 cm$^2$/Vs) as compared to other semiconductor material such as Si (~400 cm$^2$/Vs).

The performance of HEMT can be further improved by optimizing the material structure. Increase the Al mole fraction in the AlGaN layer will lead to higher carrier concentration, but mobility will drop due to alloy disorder scattering. Besides, AlGaN barrier layer with a higher Al content is accompanied with enhanced lattice mismatch effects, which degrade the crystalline quality of barrier layer leading to a lower carrier mobility.$^{11}$ Therefore, the improvement of output power density by increasing the Al content is limited. Instead of increasing the Al content to enhance the carrier concentration, Shen et al. inserted a 1-nm-AlN layer between AlGaN and GaN layer and achieved an increase in carrier mobility by 25% and 10% increase in carrier concentration.$^{2}$ Besides increasing Al content in AlGaN / GaN based HEMT, In$_{0.18}$Al$_{0.82}$N can be adopted as an alternative barrier layer as well. In InAlN / GaN system, the polarization charge is completely determined by spontaneous polarization since the structure is free from strain so the piezoelectric polarization is nearly zero.$^{1}$ Kuzmik has predicted the 2DEG density to be around $2.7 \times 10^{13}$ cm$^{-2}$ when In$_{18}$Al$_{0.82}$N is nearly lattice matched to GaN. The higher 2DEG density of InAlN / GaN system is due to the large spontaneous polarization difference and the large conduction band discontinuity.$^{22}$

1.1.2 Substrate

Due to the lack of availability of thick GaN substrate, HEMTs are usually grown on substrates such sapphire, SiC or Si. Sapphire is the most common one but its poor thermal
conductivity hinders the electrical performance and the reliability especially for high power application. Devices fabricated on GaN grown on SiC usually exhibit the best performance because of the least lattice mismatch between GaN and SiC. However, SiC is a lot more expensive than that of Si or sapphire substrate. Due to the readiness of Si technology, HEMT grown on Si have attracted more attentions recently. HEMTs grown on 8 inch Si (111) substrate have been demonstrated by Arulkumaran et al. recently. To grow GaN on Si, AlN nucleation was generally grown on Si substrate first and AlGaN grading transition layer was grown subsequently to release the lattice mismatch. Table 1-2 summarizes the material properties of Si, GaN, and sapphire.

1.1.3 Review of HEMTs Performance

The first AlGaN/GaN high electron mobility transistor (HEMT) was demonstrated by Khan et al. in 1993. The current density was just 50 mA/mm and the transconductance was 28 mS/mm. After that, many studies have been devoted to improve the quality of the epitaxy layers, process techniques or even propose new structures. Till now, the record current density for AlGaN/GaN HEMT is 2.9 A/mm fabricated by Cao et al. Additionally, a current-gain cutoff frequency (fT) of 225 GHz with a gate length (Lg) of 55 nm and a power-gain cutoff frequency (fmax) of 300 GHz with a gate length of 60 nm have been demonstrated in AlGaN/GaN HEMTs. Source-drain breakdown voltage of 2200 V was obtained at LD = 20 µm.

1.1.4 Issues

1.1.4.1 Self-heating effect

Despite good performance of GaN based device, the long-term stability and reliability remain major concerns especially at higher power densities. During device operation, the power is generated at device active area and causes local Joule self-heating. This phenomenon usually becomes even worse due to the poor thermal conductivity of sapphire (~30 W/mK). Although
Si substrate has better thermal conductivity (~149 W / mK) as compared to sapphire, there is a huge thermal resistance layer of AlN nucleation layer between the Si substrate and GaN. This nucleation layer is very defective and thermally resistive with a thermal resistance of $7 \times 10^{-8}$ m$^2$K / W.\textsuperscript{11} Figure 1-2 shows the typical drain I-Vs and transfer characteristics of AlGaN / GaN HEMT degraded with self-heating effect; negative drain output resistance. Not only does the output current reduce because of self-heating effect, the carrier mobility drop because of phonon scattering.\textsuperscript{8} Kuzmik et al. reported the channel temperature of HEMTs on sapphire substrate will reach ~320°C at an output power of 6 W/mm.\textsuperscript{12} Chang et al. simulated the thermal behavior based on Schrödinger’s equation and plotted the relationship between electron mobility and temperature, as shown in Figure 1-3.\textsuperscript{14} Several methods including simulation and experimental methods have been used to estimate the junction temperature of AlGaN / GaN interface including finite element method,\textsuperscript{15} DC characterization,\textsuperscript{16} IR microscope,\textsuperscript{15} scanning thermal microscopy and Micro-Raman spectrum.\textsuperscript{17} Simms et al. utilized Micro-Raman to measure the channel temperature along source and drain contact.\textsuperscript{18} Kuzmik et al. reported the channel temperature of AlGaN/GaN on Si substrate was around 75°C at a power density of 5 W / mm by electrical method while it was 250°C on sapphire substrate.\textsuperscript{16} Singhal et al. studied the thermal performance by Infrared (IR) microscopy on AlGaN / GaN grown on Si substrate. It was found out the channel temperature was around 200°C at a power density of 22.5 W / mm.\textsuperscript{19} Although there are several studies about the thermal performance of AlGaN / GaN on different substrates, there are few effective solutions to reduce the junction temperature yet.

1.1.4.2 Breakdown voltage

Based on the GaN breakdown field, the off-state drain breakdown voltage of an AlGaN/GaN HEMT with a drain to source distance ($L_{DS}$) of 10 µm should be 1.01 MV / cm$\times$10
\[ \mu m \times 10^4 \text{ cm} / 1\mu m = 1010 \text{ V} \]. Till now, the reported breakdown voltage of \( L_{DS} = 10 \mu m \) is 500 V, which is still below the limit of GaN.\(^{11,21}\) However, breakdown voltage of 600 V or higher for applications in switching mode power supplies and inverter systems is needed.\(^{20,22-23}\) By increasing the drain to source distance, the breakdown voltage could be increased but the device on-resistance would also be sacrificed. As a result, methods to improve the breakdown voltage, other than just increasing the drain to source distance have to be developed.

The reason that the breakdown voltage is lower than theoretical value is the existence of local peak of electric field at the corner of gate close to drain electrode. One way to solve this issue is to implement a field plate (FP), which is a metal plate placed on top of an insulator protruded from gate\(^{12}\) or source\(^{24}\) electrode. The length of the field plate (\( L_{FP} \)) is an important parameter which influences the extent of breakdown voltage improvement.\(^{12}\) Lu et al. reported electric field distribution along gate to drain by a 2-dimensional simulation. The device structure and electric field distribution along gate to drain is shown in Figure 1-4. The breakdown voltage was improved from 55 V to 150 V after implementing a 1 \( \mu m \) length source field plate at drain to source distance equals to 3.9 \( \mu m \). Ando et al. reported an improvement of breakdown voltage from 50 V to 150 V after employing 1 \( \mu m \) wide gate field plate.\(^{12}\) Besides, the breakdown voltage improvement reached a maximum at \( L_{FP} = 1 \mu m \) but decreased after that.

Another important factor which influences the breakdown voltage is the material quality of GaN. Residual impurities, presumably oxygen and silicon,\(^{25}\) in a unintentionally n-doped GaN buffer have been identified as a main source of buffer leakage.\(^{26}\) These residual donors could be compensated by deep acceptor states such as Fe or C.\(^{27,28}\) Carbon doped (C-doped) or iron doped (Fe-doped) GaN buffer layer provides traps that closed to the mid band-gap. These traps can help to grab charges and made the buffer layer more resistive. By growing thicker buffer layer, the
dislocation defects could be reduced and thus improved the breakdown voltage. Selvaraj et al. grew 1.25 to 7 µm GaN buffer layer by Metal Organic Chemical Vapor Deposition (MOCVD) and measured the dislocation densities and breakdown voltage. By increasing the buffer layer thickness, screw dislocation density decreased while the breakdown voltage increased from 100 V to 400 V. Yu et al. reported breakdown voltage of 500 V with a gate to drain distance of 3 µm and 2.7 µm thick GaN buffer layer on a 4-inch Si substrate.

1.1.4.3 Current dispersion

Alternating (AC) drain current of AlGaN/GaN HEMT is usually less than the direct current (DC) for high frequency application. This phenomenon, commonly defined as the current collapse, is caused by the formation of a virtual gate between gate to drain electrode because of the existence of surface states. When \( V_{DS} \) is biased at a higher voltage, hot electrons can be trapped by the surface states and formed the virtual gate. These charged traps form an additional depletion region between gate and drain electrode. Under high frequency operations, those trapped charges cannot respond to the AC signal. To eliminate the current dispersion, passivation layer such as SiN or Al\(_2\)O\(_3\) was utilized to passivate the surface states. Liu et al. reduced current dispersion at frequency of 5 MHz using PECVD grown SiN / ALD deposited Al\(_2\)O\(_3\) composite material. Besides, Romero et al. reported the passivation effect could be improved by in situ lower-power N\(_2\) plasma pretreatment prior to SiN deposition.

1.2 Dissertation Outline

This dissertation covers three main topics; the fabrication of AlN based metal-insulator-semiconductor high electron mobility transistors (HEMTs), the irradiation effects on GaN-based HEMTs and the novel structure to improve self-heating effect and increase off-state drain breakdown voltage.
Background knowledge on the III-V compound semiconductor transistors, especially, the properties and current status of gallium nitride (GaN) based high electron mobility transistors, as well as the reliability issues hindering the further development of GaN HEMTs technology are presented in Chapter 1.

The methodology including fabrication process, material and device characterization that are used in this thesis is reviewed in Chapter 2.

The next several chapters cover research studies on the topics of fabrication of HEMTs and characterization and solution to the reliability issues of GaN HEMTs outlined in Chapter 1. Chapter 3 presents the DC performance and high-frequency performance of the fabricated AlN-MISHEMT. Chapter 4 examines the breakdown voltage of the fabricated AlN-MISHEMT. The degradation of buffer oxide etchant (BOE) to Ohmic contacts is discussed in Chapter 5 in order to understand the mechanism of BOE to device performance and optimize our process flows. Chapter 6 examines the mechanism of the breakdown voltage improvement after proton irradiation through back-side proton irradiation. Chapter 7 discusses the effect of low-dose gamma irradiation on DC performance and high-frequency response. Chapter 8 reviews the effect of defects generated after electron irradiation on the device performance of AlGaN and InAlN based heterojunctions. Chapter 9 reports the thermal response of proposed-AlGaN / GaN HEMTs with a back-side Cu via under the device active area. Chapter 10 discusses the DC performance and reliability improvement of the proposed AlGaN / GaN HEMTs structures. Chapter 11 provides a summary and conclusion for all the topics discussed in this dissertation.
Table 1-1. Summary of material properties of Si and AlGaN/GaN heterojunction.

<table>
<thead>
<tr>
<th>Material</th>
<th>Si</th>
<th>AlGaN / GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band gap (eV)</td>
<td>1.1</td>
<td>3.49</td>
</tr>
<tr>
<td>Electron mobility (cm$^2$/V-s)</td>
<td>400</td>
<td>1400</td>
</tr>
<tr>
<td>Saturated electron velocity ($\times 10^7$ cm/s)</td>
<td>1</td>
<td>2.7</td>
</tr>
<tr>
<td>Critical breakdown voltage (MV/cm)</td>
<td>0.3</td>
<td>1.3</td>
</tr>
</tbody>
</table>
Figure 1-1. A) Origin of 2DEG B) Energy band gap diagram of AlGaN and GaN heterojunction.\textsuperscript{50}
Table 1-2. Summary of material properties of Si, sapphire and SiC.

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Sapphire</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal conductivity (W / m-K)</td>
<td>149</td>
<td>30</td>
<td>300</td>
</tr>
<tr>
<td>Lattice mismatch (%)</td>
<td>17</td>
<td>3.5</td>
<td>14</td>
</tr>
<tr>
<td>Substrate cost (US $ / piece)</td>
<td>~4</td>
<td>~100</td>
<td>~200</td>
</tr>
<tr>
<td>Integration capability</td>
<td>High</td>
<td>Low</td>
<td>Moderate</td>
</tr>
</tbody>
</table>
Figure 1-2. Drain I-V and transfer characteristics of AlGaN / GaN HEMTs on sapphire and on silicon.⁸
Figure 1-3. Calculated electron mobility as a function of temperature.\textsuperscript{14}
Figure 1-4. 2D simulations of the electrostatic field distributions between source and drain contacts for HEMT with and without source field plate.24
CHAPTER 2
METHODOLOGY REVIEW

2.1 SEMICONDUCTOR FABRICATION PROCESSES

2.1.1 Isolation

Isolation is the process to reduce the leakage current between devices through GaN buffer layer. Isolation could be either achieved by mesa etching or ion implantation. Poor isolation might induce issues such as high leakage current and low breakdown voltage. A good isolation requires the leakage current across a 5 µm gap to be in around $10^{-9}$ A scale.

Mesa etching technique involves defining regions surrounding the active devices with a mask layer, and subsequently etching away the exposed area to form isolated islands or “mesa”. For AlGaN / GaN HEMTs, mesa etching is generally performed by removing AlGaN layer and some of the underneath GaN buffer layer. Mesa etching needs to be well calibrated, serious undercut might create leakage path and fail the isolation. The schematic view of mesa etching is shown in Figure 2-1 A.

Another common method of isolation is ion implantation. The isolation is achieved by implanting high energy ions such as H, He, N, O, Zn to the device. By a Monte-Carlo based simulation software, Stopping and Range of Ions in Matter (SRIM), vacancy concentrations created by the implantation and the stopping range of the vacancies could be estimated. As a result, by varying ion energy or dose, specific stopping range or vacancies could be achieved. Multiple implantations were used to achieve uniform vacancies distribution in the device. The schematic view of mesa etching is shown in Figure 2-1 B. The major concern of implantation isolation is the thermal stability. Lo. et al. reported that the isolation effect will be removed after annealing at temperature above 600ºC.
2.1.2 Photolithography

Photolithography is one of the most critical processes in semiconductor fabrication. It is a process which allows patterns to be transferred to the device accurately. The process requires photoresist, mask, exposure tool, and developer solution. The photolithography process could be further divided into spin coating, exposure and resist developing.

Photoresist (PR) is usually composed of a base resin, photo active compound (PAC), and organic solvent. The resin could be poly-(methyl methacrylate) (PMMA), poly-(methyl glutarimide) (PMGI), novolac resin, or epoxy. Based on the solubility of PR after exposure, the PR could be further divided into positive PR or negative PR. For positive PR, the dissolution rate in development solution increased after exposure. For negative PR, the dissolution rate in development solution decreased after exposure. By putting a mask, which has opaque and transparent patterns, on top of the photoresist, the pattern on the mask can be transferred to the photoresist. Figure 2-2 shows the difference of positive and negative photoresist.

The first step of the photolithography process is spin coating. The liquid PR is usually dispensed at the center of the wafer and spread out by the spinner. The range of the thickness of a PR can achieve is mainly determined by its viscosity but it can be further adjusted by the parameters of spin coating. The main rotation speed and time can be used to adjust the thickness of the PR within its specific thickness range. Other factors such as the acceleration speed, the exhaust of the spinner, and the pretreatment of the wafer can affect the uniformity of the thickness. Prebake, which is also called soft bake, is a thermal treatment to vaporize some of the organic solvent in the resist after spin coating. It affects the profile of the pattern, the adhesion of the PR to the substrate, and the solubility after exposure. The prebake temperature also affects the thickness of the PR.

The second step of the photolithography process is exposure. The exposure is usually
performed under the wavelength ranging from 193 to 465 nm. The common exposure tools are in the form of contact aligner, stepper or scanner. Only contact aligner is discussed here because it is the tool used in this thesis. By setting the power of the mercury lamp and exposure time, PR is exposed with a specific wavelength ultra-violet (UV) light. If the UV power or exposure time is not enough, the resist might result in underdevelopment (UD). If the light intensity or exposure time is too high or too long, respectively, the feature size on the resist might be bigger than the size on the mask. To keep mask clean is also very important. If there were particles on the sample or mask, the contact between mask and wafer would have a gap to induce light diffraction and affect resist profile and pattern resolution.

2.1.3 Lift off

Lift off is a technology that can pattern a target material on the surface of the substrate. The gate, Ohmic metal, and final metal pattern were all fabricated through the standard lift off process in this thesis. Standard photolithography is patterned first and metal contacts are deposited on top of patterned PR. After metal deposition, the samples are soaked in solvent such as acetone to lift off the unwanted area of PR together with the metal on top of it. The thickness of metal is preferred to be thinner than 1/3 of the thickness of PR to assist lift-off process. Lift-off process is not generally employed in the silicon process due to the following issues. First, the PR pattern is very critical in lift-off process. An overhang structure of the top surface layer of PR as illustrated in Figure 2-3 A is preferable. However, it is very difficult to fabricate an overhang structure by a simple photolithography process. As a result, toluene soaking or lift-off resist (LOR) is generally employed to assist the lift-off process. If the side wall of the PR is tapered, the deposited metal on the side wall is relatively thick. The continuous metal would be easily lifted off with no pattern been generated. Another disadvantage for the tapered angel side wall is the generation of the ear structure, which is a very tall metal at the edge of the pattern. The ear
structure might induce bad contact in the following photolithography processes. Figure 2-3 B shows the effect of side wall profile to lift-off process. Last, the removed metal might be re-deposited on to the surface. It is very difficult to remove these particles after the wafer has been dried.

2.1.4 Electron beam evaporation

One of the most common metal deposition methods is e-beam evaporation. The schematic view of an evaporation system is shown in Figure 2-4. The system is usually consisted of a metal target, a crucible, a shutter and a vacuum system. The source metal, which usually sits in a thermal stable carrier called crucible, is heated above its melting point by electron beam bombardment. The chamber is usually connected to either diffusion pump or cryo pump to achieve ultra-high vacuum. The samples are located on a dome-shaped sample holder directly on top of the target. Because the deposition chamber is under an ultra-high vacuum (~10⁻⁸ torr), the evaporated atoms can travel at line trajectories all the way to the samples. Electron beam evaporation is a very useful process for pure metal deposition, but it is difficult for alloy deposition.

2.1.5 Rapid thermal annealing

Rapid thermal annealing (RTA) is usually used to decrease the resistance of metal alloys contact to semiconductor such as Ohmic contacts or remove the defects generated after irradiation or etching process during the device fabrication. The system usually includes a heating lamp or laser which allows a short time temperature ramping, gas purging line, and thermal couple to monitor the temperature. For Ohmic contacts annealing, the annealing temperature and ramping rate are very critical to achieve low resistance metal contact on semiconductor. Besides, to ensure low-resistance of the Ohmic contacts, the oxygen
concentration inside the RTA system needs to be monitored. The low oxygen concentration is achieved by constantly purging N\textsubscript{2} in the system.

2.1.6 Plasma-enhanced chemical vapor deposition

Plasma-enhanced chemical vapor deposition (PECVD) is the most common process for low-temperature passivation layer deposition such as SiO\textsubscript{2} or SiN. The plasma enhanced mode can reduce the thermal budget a lot by introducing plasma energy. In this dissertation, PECVD is chosen to prevent high temperature deposition to avoid degradations such as loss of isolation and metal diffusion in the gate electrode. For SiN deposition, silane, NH\textsubscript{3} and N\textsubscript{2} are introduced simultaneously first and plasma is ignited subsequently. The reactions are as follows:

\[
\text{SiH}_4 + \text{NH}_3 \overset{300^\circ C}{\longrightarrow} \text{SiNH} + 3\text{H}_2
\]

\[
2\text{SiH}_4 + \text{N}_2 \overset{300^\circ C}{\longrightarrow} 2\text{SiNH} + 3\text{H}_2
\]

A RF voltage is biased on the top electrode, while the bottom electrode is grounded. The RF voltage causes a plasma discharge between the electrodes. Wafers are placed on the bottom electrode, which is heated between 100 to 400\textdegree C. There are several parameters needed to be adjusted to optimize the film properties including refractive index (RI), density and etching resistivity. The composition of silane, NH\textsubscript{3}, and N\textsubscript{2} is a critical parameter because it affects the film properties such as etch rate in buffered oxide etchant and refractive index. The deposition rate generally increased with increasing temperature and RF power. The advantage of PECVD is also its disadvantage. Because of the low-temperature deposition, low tensile stress (~2×10\textsuperscript{9} dyne/cm\textsuperscript{2}) film can be prepared. However, the SiN film deposited by PECVD usually contains 20-25% hydrogen.
2.1.7 Atomic layer deposition

Atomic layer deposition (ALD) is a thin film deposition that is based on the sequential gas phase chemical processes on a solid surface. Figure 2-5 shows the schematic view of the plasma-enhanced ALD (PEALD) process. For the plasma enhanced AlN deposition mode, trimethylaluminum (TMA) and N₂/H₂ are used as precursors for Al and nitrogen, respectively. In one cycle of the deposition, TMA is first flowed into the system and attached to sample surface with Ar gas constantly purging the excessive TMA. As a result, there is just one atomic TMA layer uniformly adsorbed on the wafer surface. Following the TMA deposition, N₂ and H₂ gases are introduced into the deposition chamber and the plasma is ignited. The nitrogen will react with Al and break the Al-C bond. AlN is thus formed after this cycle. The thickness of the AlN for each deposition cycle is around 1 Å. Because the deposition is self-limiting and a monolayer-by-monolayer process, it can achieve a very conformal deposition even on wafers with high aspect-ratio patterns. The temperature of ALD process is usually relatively low because the metal-organic precursors might decompose at high temperature. For example, the temperature for ALD process using TMA as a precursor is usually below 300°C. This eliminates the potential thermal degradation to the device such as Ohmic metal degradation.

2.1.8 Bosch etching

Bosch process is a dry etching process which features in high aspect ratio Si etching. It is named after a German company Robert Bosch GmbH which patented the idea. This process uses a two-step process which alternates between deposition and etching. The deposited layer is usually a chemical inert passivation layer such as the dielectric deposited by CF₄. This passivation layer can provide protection to the side wall for the following etching process. The result is an anisotropic etch that can have a vertical sidewall regardless of the orientation of the silicon crystal. Although a noticeable rippling of the surface can be found on the sidewalls, the
Bosch process is currently the most popular process for deep silicon etching. It provides a very consistent etching with a near 90 degree sidewall.

2.2 Material Characterization

2.2.1 Hall measurement

Hall measurement is a method to estimate the carrier type, carrier concentration and carrier mobility. The system includes a magnetic field, current supply and a voltage monitor. Figure 2-6 shows the schematic view of a Hall measurement system setup. As shown in Figure 2-6, the current is applied in x direction and the magnetic field is applied in z direction.\(^{46}\)

Because of Lorentz force, the majority carrier in the semiconductor will be swept to +y direction. Thus, by determining the sign and the value of the voltage drop between +y and –y direction, the carrier type and carrier concentration can be calculated. The equation to calculate carrier concentration is as shown in Equation 2-1. If the sheet resistance of the semiconductor is known, the mobility can be estimated from Equation 2-2 as well.

\[
{n_S} = \frac{IB}{q|V_H|} \quad \text{Eq. 2-1}
\]

where \(n_S\) is sheet density of carrier concentration

- \(I\) is the current applied
- \(B\) is the magnetic field applied
- \(q\) is elementary charge
- \(V_H\) is the Hall voltage measured

\[
\mu = \frac{V_H}{R_SIB} = \frac{1}{qn_SR_S} \quad \text{Eq. 2-2}
\]

where \(V_H\) is the Hall voltage

- \(I\) is current applied
- \(B\) is magnetic field applied
Rs is the sheet resistance of the semiconductor

2.2.2 Transmission electron microscopy

Transmission electron microscopy (TEM) is a method which uses high energy focused electron beam to examine a very thin (below ~100 nm) structure. The electron beam passes through the thin sample and interacts with the specimen and forms the image. To get high resolution image, the TEM system is usually operated under pressure range at $10^{-7}$ to $10^{-9}$ Pa. The resolution of TEM is around 1-2 Å and can provide information such as crystallographic phase, crystallographic orientation.47

2.2.3 Scanning electron microscopy and energy dispersive X-ray spectroscopy

Scanning electron microscopy (SEM) is a method which uses high energy focused electron beam to examine the surface topography of the sample. Under the incident of focused electron beam, secondary electrons or back scattering electrons emit from the excited atoms. By analyzing the intensities of backscattering electrons or secondary electrons, the atomic numbers and the topography of the analyzed surface can be determined, respectively.

There are generally two types of detectors for SEM system. One of the detectors is called backscattering electron detector (BSD) which collects the back scattering electron. The BSD is usually located on top of the sample. The probability of backside electron generated is in proportional to the atomic mass of the element. In other words, the numbers of backside electron been collected are in proportional to the atomic mass. As a result, by the contrast of the image, the relative atomic mass distribution can be estimated. The other detector is secondary electron detector (SD). The energy of secondary electrons is generally lower than 50 eV. As a result, the electrons that are collected by the SD originate within a few nanometers from the sample surface. Besides, the brightness of the signal depends on the number of secondary electrons reaching the detector. As a result, the number of secondary electrons reaching the SD is very sensitive to the
topography. The image generated from SD thus provides a well-defined, 3-dimensional appearance. Use secondary detector, the resolution of SEM image can be down to 1 nm.

In SEM system, there is usually embedded an energy dispersive X-ray spectroscopy (EDX, EDS, or XEDS). It is a technique generally used in semi-quantitative elemental analysis. The analysis is performed by analyzing the X-ray intensity and energy generated from the interaction of incident electron beam and sample. Each element has its own specific spectrum based on its atomic number and chemical state. EDX can provide elemental analysis on areas as small as nanometers in diameter and thickness with micrometer scale. With the assistance of SEM, it can provide an elemental and spatial analysis on the sample which is especially good for defect analysis.

2.2.4 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a surface-sensitive qualitative and quantitative spectroscopic technique that obtains the elemental composition, chemical state and electronic state of the elements that exist within a material. Different from EDX, X-ray is used instead of focused electron beam to excite the atoms. The detector analyzes the electron excited from the top 10 nm of the sample surface. X-ray incident knocks the 1s electron, so electrons at other higher energy states such as 2s or 2p state jump from excited states to ground state. During this process, specific energy will be released. Because of this, each element except hydrogen and helium thus produces a characteristic set of XPS peaks at characteristic binding energy. The characteristic spectrum thus identifies each element in different electron states. The number of electrons is directly related to the amount of elements in the sample. Generally speaking, the resolution of the atomic concentration is around 1000 ppm.
2.2.5 Auger electron spectroscopy

Auger Electron Spectroscopy (AES) is a surface sensitive spectroscopic technique used for elemental analysis of surfaces. It offers high sensitivity of all elements except of H and He. AES can be further divided into three steps which are atomic ionization, electron relaxation and analysis of the emitted auger electrons. The atomic ionization is the process of incident electron to remove the core 1s electron. After the removal of core electron, the electrons at higher energy states jump to fill the cavity of the 1s vacancy. To compensate for the energy change from this transition, an Auger electron or an X-ray is emitted. By analyzing the energy of the emitted Auger electron, the characteristics spectrum is generated. For light elements, the probability is greatest for emission of an Auger electron, which accounts for the light-element sensitivity for AES. Similar to XPS, the chemical state of the atoms can also be determined from energy shifts and peak shapes. Because of the energy of Auger electron is relatively low, only the Auger electrons from top 1nm surface will have sufficient energy to escape the surface and reach the detector as shown in Figure 2-7. Utilizing this fact with the ion milling process, elemental depth profile can be generated.

2.2.6 Ellipsometer

Ellipsometer is a way to measure thin film thickness and refractive index (RI) by an optical method. The thickness range for measurement is around 1 nanometer to few hundred nanometers. The technique uses plane polarized monochromatic light source with wavelength ranging 200 to 1050 nm to illuminate the thin film/substrate at an angle. Based on the angle and intensity of the reflective light measured by the detector, the RI and thickness can be back calculated. Multi-stack of thin films can also be measured if the model is constructed appropriately.
2.2.7 Four point probe measurement

Four point probe measurement is a technique to measure the material sheet resistance. The schematic view of four point probe measurement is illustrated in Figure 2-8. The outer two probes are connected a current supply to supply current \( I \) while the inner two probes connect to a high impedance voltage meter to monitor the voltage drop \( V \). Each probe has the same spacing which is around 1mm. Depends on the sample geometries, edge effect, and probe spacing \( s \), correction factor \( F \) needs to be considered. The correction factor will be usually provided by the tool vendor. The sheet resistance, \( \rho \), can be calculated by \( \rho = \frac{2\pi s F V}{I} \).

2.3 Device Characterization

2.3.1 DC performance

DC performance is one of the most important characteristics of a field effect transistor. It is generally composed of drain I-V, gate I-V and transfer characteristics. The DC performance is obtained by connecting a FET to a three-channel DC parameter analyzer. Source is grounded and drain, gate is connected to channel which supplies voltage and monitors current simultaneously. Drain I-V is a plot shows modulation of gate voltage \( V_G \) to the relationship of drain source current \( I_{DS} \) versus drain source voltage \( V_{DS} \). Figure 2-9 shows a typical drain I-V characteristic of an AlGaN/GaN FET. From drain I-V characteristics, several parameters can be obtained, such as drain saturation current, drain to source resistance, and the mobility. Saturated drain source current \( I_{DSS} \), which is the maximum \( I_{DS} \) of a FET, can be obtained. The drain current is usually normalized to gate width, leading to a unit of mA/mm. From the low-field drain I-V curves, the resistance of drain to source and the mobility can be obtained. The resistance of drain to source \( R_{DS} \) is the reciprocal of the slope of the low field drain I-V curve.
If the resistance of drain contact \( R_D \), source contact \( R_S \), and threshold voltage \( V_{TH} \) is known, the mobility can be estimated by Equation 2-3.53

\[
\frac{V_{DS}}{I_{DS}} = R_S + R_D + \frac{Ld}{\mu W \varepsilon (V_G - V_{TH})}
\]

where \( V_{DS} \) is drain source voltage

\( I_{DS} \) is the drain source current

\( R_S \) is the resistance between gate to source

\( R_D \) is the resistance between drain to gate

\( L \) is the gate length

\( d \) is the thickness of AlGaN layer

\( \mu \) is the mobility

\( W \) is the gate width

\( \varepsilon \) is the permittivity of AlGaN layer

\( V_G \) is the gate voltage

\( V_{TH} \) is the threshold voltage

Gate I-V is the relationship of gate current to gate voltage \( (V_G) \). To measure gate I-V, gate electrode is swept from deep depletion region to forward turn-on voltage while drain electrode is floated. From gate I-V, the reverse leakage current, Schottky barrier height (SBH) can be obtained. When the \( V_G \) is biased at deep depletion, the gate current is called the leakage current. By plotting the log \( (I_G) \) with \( V_G \), the SBH can be obtained by Equation 2-4.

\[
SBH = \frac{kT}{q} \ln \left( \frac{A^* T^2}{I_0} \right)
\]

Where \( k \) is Boltzmann constant \( 1.38 \times 10^{-23} \text{[J/K]} \)

\( T \) is absolute temperature \([\text{K}]\)

\( q \) is elementary charge \( 1.6 \times 10^{-19} \text{[q]} \)

\( A \) is gate area
A* is Richard constant which is 31 AlGaN and 26 for GaN, respectively

$I_0$ is ten to the power of y-intercept of regression line on forward gate I-V part

Another important performance is transfer characteristics. To measure transfer characteristics, the drain voltage is biased at fixed voltage at device saturation region and gate voltage is swept from off region to on region with both drain current and gate current being monitored. From transfer characteristics, transconductance ($G_m$), subthreshold swing ($SS$), and threshold voltage ($V_{TH}$) can be obtained. Transconductance, which represents the amplification of a FET, is defined as the derivative of $I_{DS}$ to $V_G$ at fixed $V_{DS}$. As shown in Figure 2-10 A, the $G_m$ peaks at around $V_G=1.2$ V. To obtain $SS$, semilog curve of $I_{DS}$ versus $V_G$ is required. In the subthreshold curve as shown in Figure 2-10 B, the slope is the subthreshold slope. The reciprocal of subthreshold slope is subthreshold swing, which shows the effectiveness of the gate control. The unit of $SS$ is mV/dec, and $SS$ represents the voltage required to change one decade of the drain current. As shown in Figure 2-11, by taking square root of the $I_{DS}$ and linear regression at forward turn on region, the threshold voltage can be obtained.

2.3.2 Transmission line method

Transmission line method (TLM) is a set of test key used to estimate the contact and sheet resistance of a FET. The common TLM test key is designed as shown in Figure 2-12. Rectangular metal pads were deposited and separated in different gaps. The resistance across different gaps are measured by an hp parameter analyzer. By plotting the resistance versus gap spacing, the sheet resistance ($R_{sh}$), transfer resistance ($R_T$) and transfer length ($L_T$) can be extracted from the linear regression of the curve. Utilizing this technique, the source resistance ($R_S$) and drain resistance of a FET can be calculated from Equation 2-5.

$$R_S = R_{Sh} \times \frac{L}{W} + \frac{R_T}{Z}$$

Eq. 2-5
where $R_s$ is source resistance

- $R_{sh}$ is sheet resistance of semiconductor
- $L$ is gate length
- $W$ is the distance between gate to source
- $Z$ is the length of Ohmic contact

### 2.3.3 Gate lag measurement

The gate lag measurement is a technique that can evaluate the drain current dispersion and characterize the defects in the semiconductor. The system setup includes a pulse generator, power supply, resistor and an oscilloscope. Gate is connected to a pulse generator, and source is connected to ground. A DC power supply is connected to the resistor which is connected in series with the drain electrode. By reading the voltage drop across the resistor by the oscilloscope, the current can be calculated. Figure 2-13 shows the setup of gate lag measurement. When the device is pulsed from off to on at high frequency, the trapped charges can’t respond due to large time constant of the defects. As a result, the drain current measured in AC mode is lower than that measured in DC, which is known as current dispersion. Usually the drain current dispersion from AC to DC is more severe when the drain voltage or the frequency is higher. The amount of current dispersion from DC to AC current can represent the amounts of the defects.\(^{56}\)

### 2.3.4 Off-state drain breakdown voltage

Off-state drain breakdown voltage is a very important characteristic to evaluate the performance of FET in high power application. The off-state drain breakdown voltage is usually performed at a fixed $V_G$ which sets the device be operated at deep depletion state with $V_{DS}$ gradually increases. When the $I_{DS}$ or $I_G$ suddenly increases dramatically, the voltage is recorded as off-state drain breakdown voltage ($V_{BR}$).
2.3.5 Deep level transient spectrum

Deep level transient spectrum (DLTS) is a useful technique to characterize and identify the defects. DLTS establishes fundamental defect parameters and measures their concentration in the material. Some of the parameters are considered as defect "finger prints" used for their identifications and analysis. It utilizes the fact that the RF capacitance of the sample depends on the charge state of deep levels in the space charge region. The device capacitance is monitored with time with the gate constantly being pulsed. \( T_1 \) and \( T_2 \) is chosen to estimate the recovery of capacitance after the pulse. The rate window \( (e) \), which is the reciprocal of time constant, can then be calculated by Eq. 6. By plotting the rate window versus temperature, the activation energy can be obtained by Equation 2-6 as well.57

\[
e = \frac{\ln\left(\frac{T_2}{T_1}\right)}{T_2 - T_1} = \frac{1}{\tau_e} = \frac{N_{c,v} C_{n,p}}{g} \exp\left(-\frac{E_t}{kT}\right)
\]

where \( e \) is the rate window

\( \tau_e \) is the time constant

\( N_{c,v} \) is effective density of states in the conduction band or the valence band

\( C_{n,p} \) is capturing coefficient

\( g \) is the degeneracy factor for the level, usually assumed to be 1

\( kT \) is the thermal energy

\( E_t \) is the activation energy

2.3.6 Admittance spectrum

Admittance spectrum is another method to obtain the thermal activation energy of the defect. It mainly measures the change of admittance in the semiconductor when the carriers are captured or emitted from the defects. In admittance spectrum measurement, the diode is treated as an equivalent circuit which has a capacitor and resistor in series. When the angular frequency is \( \omega \), the capacitance and admittance are as shown in Equation 2-7.
\[ C_p = \frac{C}{1 + (\omega\tau)^2}, \quad G_p = \frac{\omega\tau C}{1 + (\omega\tau)^2} \] \hspace{1cm} \text{Eq. 2-7}

where \( C_p \) is the measured capacitance

\( C \) is the real capacitance

\( \omega \) is the angular frequency

\( G_p \) is the measured conductance

\( \tau \) is the time constant which equals to \( R \times C \)

When \( \omega\tau \) equal to 1, the \( G_p / \omega \) reaches a maximum and there exists an inflection point in the capacitance versus temperature plot. Substitute \( \omega, T \) where local maximum \( G_p / \omega \) happens into Equation 2-8, the thermal activation energy can be obtained.\(^{58}\)

\[ \omega = \gamma T^2 \exp\left(-\frac{E_A}{kT}\right) \] \hspace{1cm} \text{Eq. 2-8}

where \( \gamma \) is the coefficient which is independent of temperature

\( E_A \) is activation energy

\( T \) is temperature

\( k \) is Boltzmann constant

2.3.7 Capacitance-voltage measurement

Capacitance-voltage measurement is a very powerful technique which can gives users information about doping type, carrier concentration, and interface state densities. The C-V curve is usually obtained with a C-V meter, which applies a DC bias voltage and a small sinusoidal signal (1 kHz-10 MHz) to the capacitor and measures the capacitive current with an AC ammeter.

When the Schottky contact on AlGaN/GaN HEMT is biased at 0 V, the depletion region barely touches 2DEG. As a result, the capacitance measured is mainly contributed by AlGaN
barrier layer. Utilizing this fact, the thickness of AlGaN layer can be calculated within 10% accuracy by Equation 2-9.

\[
W = \frac{e\varepsilon_0 A}{c} \hspace{1cm} \text{Eq. 2-9}
\]

With the bias being more negative, the depletion region penetrates through 2DEG. In the point when the depletion region completely penetrates through the 2DEG, the capacitance drops dramatically. At deep depletion, the capacitance measured can be viewed as two parallel capacitors connected in series. Figure 2-14 shows the typical C-V curve of AlGaN / GaN HEMT.\(^{70}\)

Besides the barrier layer, the carrier concentration distribution can also be generated by C-V measurement. At each capacitance and voltage, the space charge region, \(W\), can be generated by Eq. 9 and the carrier concentration can be generated by Equation 2-10. Carrier concentration distribution can thus be obtained.

\[
N = \frac{C^3}{q\varepsilon_0 A^2 (dC/dV)} \hspace{1cm} \text{Eq. 2-10}
\]

Last, the existence of traps can also be characterized by the capacitance-voltage curve. Typically, the defects can be categorized into four types including mobile charges \((Q_m)\), fixed charges at the surface \((Q_f)\), or fixed charges distributed in oxide layer \((Q_o)\), and interface charges \((Q_i)\). For an ideal C-V curve, the stretching at the transition region is almost zero. However, the C-V curve might be parallel shifted because of \(Q_m\), \(Q_f\) or \(Q_o\) and the transition region might be stretched because of \(Q_i\). In Figure 2-15, the non-ideal CV curve is shown. Figure 2-15 B curve is the typical C-V curve resulted from the existence of \(Q_m\), \(Q_f\) or \(Q_o\). As shown in Figure 2-15, both shifting and stretching happens on C curve. The mechanism of shifting is the same as B curve while the stretching is due to \(Q_i\). By reading the voltage shift, the interface densities can be estimated. Figure 2-16 shows the typical location of mobile charges...
(Q_m), fixed charges at the surface (Q_f), fixed charges distributed in oxide layer (Q_o), interface traps (Q_it) in a MOS diode.

### 2.4 Finite element method

Finite element method (FEM) is a numerical method to solve differential equations. It uses variation method and small elements, meshes, to approach the solution numerically. If the meshes are small enough, the change of the parameters inside this mesh can be viewed as linear. The process of solving is an iterative process until the error function is minimized. With proper boundary condition and mesh size, the solution can be fairly accurate.
Figure 2-1. Schematic view of isolation by A) mesa etching and B) ion implantation.
Figure 2-2. Schematic view of photolithography process of A) positive or B) negative photoresist.\textsuperscript{13}
Figure 2-3. Effect of photoresist profile A) ideal overhang structure and B) tapered angle profile to lift-off performance.
Figure 2-4. Schematic view of an evaporation system.\textsuperscript{39}
Figure 2-5. Schematic view of ALD process.
Figure 2-6. Schematic view of Hall measurement system setup.\textsuperscript{46}
Figure 2-7. Generation of Auger electrons, backscattered electrons by the incident electron.\textsuperscript{50}
Figure 2-8. Schematic view of four point probe measurement.\textsuperscript{52}
Figure 2-9. Typical drain I-V characteristics of a field effect transistor.
Figure 2-10. Transfer characteristics of A) transconductance characteristics and B) threshold voltage determination.\textsuperscript{54}
Figure 2-11. Threshold voltage determined by the saturation extrapolation technique.\textsuperscript{55}
Figure 2-12. The configuration of TLM test key and data analysis.\textsuperscript{54}

Figure 2-13. The system setup for gate pulse measurement.
Figure 2-14. High-frequency C-V curve for a Schottky diode on a HEMT.\textsuperscript{70}
Figure 2-15. Effect of a fixed oxide charge and interface traps on the C-V characteristics of MOS diode.⁴⁰
Figure 2-16. Location of the charges associated with a MOS diode.\textsuperscript{40}
CHAPTER 3
GAN METAL-INSULATOR-SEMICONDUCTOR HEMTS WITH PLASMA ENHANCED
ATOMIC LAYER DEPOSITED ALN AS GATE DIELECTRIC AND PASSIVATION

3.1 Introduction to Metal Oxide Semiconductor High Electron Mobility Transistors

AlGaN/GaN high electron mobility transistor (HEMT) performance has made remarkable
progress in recent years, showing great promise for applications such as military radar and
satellite-based communications systems.\textsuperscript{1,2} Conventional Schottky metal gate HEMTs are
expected to offer the highest frequency performance, however, issues such as current collapse,
high gate leakage and questionable long-term reliability have limited the potential for high power
applications. To resolve the gate leakage problem, SiO\textsubscript{2},\textsuperscript{23} Si\textsubscript{3}N\textsubscript{4},\textsuperscript{59,60} Al\textsubscript{2}O\textsubscript{3},\textsuperscript{61-67} Sc\textsubscript{2}O\textsubscript{3},\textsuperscript{68} 
HfO\textsubscript{2},\textsuperscript{69,70} La\textsubscript{2}O\textsubscript{3},\textsuperscript{72} and TaO\textsubscript{x}N\textsubscript{y}\textsuperscript{73} based metal-oxide-semiconductor (MOS) or metal-insulator-
semiconductor (MIS) HEMTs have been employed. These gate dielectrics may also be used for
device passivation to alleviate the issue of current collapse.\textsuperscript{69} However, inserting a gate dielectric
has typically resulted in suppression of transconductance, $g_m$, and a negative threshold voltage
shift.\textsuperscript{66,74} Use of dielectrics with high permittivity could help solve these problems, because a
larger dielectric constant translates to more efficient gate modulation and thus a smaller decrease
in $g_m$ and threshold voltage shift.\textsuperscript{69-73}

AlN with a band gap of 6.2 eV and a relatively high permittivity of $\sim$8.9 is another
candidate for the gate dielectric on nitride-based HEMTs. AlN deposited by a molecular beam
epitaxy system (MBE) was used to replace an AlGaN for an AlN / GaN-based HEMT to achieve
higher sheet carrier concentration due to a larger conduction band difference between AlN and
GaN.\textsuperscript{66,72-73} Selvaraj et al. used metal organic chemical vapor deposition (MOCVD) to grow an
AlGaN / GaN HEMT structure capped with a 2-nm-AlN layer as the gate insulator and the
passivation layer.\textsuperscript{74} The HEMTs showed a very low gate leakage current of $5 \times 10^{-5}$ mA / mm;
however, the DC performance suffered from a relatively high contact resistance of 5 Ω-mm due to the incorporation of the AlN cap layer.

Atomic layer deposition (ALD) is a surface controlled layer-by-layer deposition process. Each atomic layer formed in sequence is the result of saturated surface controlled chemical reactions. Films deposited by ALD have been demonstrated to have low defect density, high uniformity and precisely controlled thickness at the nanometer scale. ALD deposited AlN has also been used as a passivation layer for AlGaN/GaN HEMTs, which significantly reduced current collapse. To date, there is no report of ALD deposited AlN as a gate insulator for AlGaN / GaN HEMTs.

In this study we report the DC and power performance of AlGaN/GaN MIS-HEMTs employing ALD AlN as the gate dielectric and surface passivation layer. X-ray photoelectron spectroscopy (XPS) and Auger electron spectroscopy (AES) were used to analyze the AlN films. DC performance and gate pulse measurements were conducted to investigate the effectiveness of AlN as the gate insulator and passivation layer.

3.2 Experimental

3.2.1 Material Growth

HEMT structures were grown on 3 inch c-plane Al2O3 substrates using a metal organic chemical vapor deposition system, starting with a thin AlGaN nucleation layer followed with a 2 μm low-defect, carbon-doped GaN buffer layer, a 23 nm undoped GaN layer, a 21.2 nm undoped AlGaN layer with a 25.6% Al mole fraction and capped with a 2.5 nm undoped GaN layer. Hall measurements on the as-grown structures showed sheet carrier densities of $1.2 \times 10^{13}$ cm$^{-2}$ and the corresponding electron mobility of 1050 cm$^2$/V-s.

3.2.2 HEMTs Fabrication

Device fabrication began with Ohmic contact deposition with a standard lift-off e-beam
evaporated Ti / Al / Ni / Au based metallization, and the samples were subsequently annealed at 850°C for 30 s under N\textsubscript{2} ambient. A typical transfer resistance of 0.4 Ω-mm was obtained using the transmission line method (TLM). Multiple energy and dose nitrogen implantation was used for the device isolation, and photoresist AZ1045 was used as the mask to define the active region of the devices. Isolation currents were less than 10 nA at 40 V of bias voltage across two 100 μm × 100 μm square Ohmic contact pads separated by a 5 μm implanted gap.\textsuperscript{75} Prior to AlN based gate insulator deposition, the sample was treated with UV ozone for 3 minutes and followed by 30\% NH\textsubscript{4}OH for 1 min.to remove the surface contaminations and improve the adhesion. 10 nm AlN was deposited in a Cambridge Nano Fiji 200 remote RF-plasma enhanced atomic layer deposition (ALD) system at 300°C.\textsuperscript{30,44} Trimethyl aluminum (TMA) was used as Al precursors and N\textsubscript{2} / H\textsubscript{2} was used as N precursors. Ar was used as carrier/purging gas. For plasma enhance ALD, N\textsubscript{2} / H\textsubscript{2} flowed into the chamber first and then 300 W of RF power was used to ignite the plasma and kept on for 40 s. The growth rate of AlN film was 0.73 Å / cycle. The exposure time for TMA was set at 0.06 seconds and the growth temperature was kept at 300°C. After ALD AlN, 1 μm × 200 μm gates were achieved via standard lift-off e-beam deposited Pt / Ti / Au metallization. Ti / Au based metallization was utilized for the interconnect metals. The source to gate distance was 1 μm.

3.2.3 Device Characterization

The AlN surface and bulk film analyses were carried out with an X-ray photoelectron spectroscopy (XPS) utilizing a Perkin Elmer 5100 system and by Auger electron spectroscopy utilizing a Perkin Elmer 660 system. A J.A. Woolam EC110 ellipsometer was used to measure the refractive index (RI) and the thicknesses of the AlN films. The DC characteristics of the AlN-MISHEMTs were measured with a Tektronix curve tracer 370A and an HP 4156 parameter
For gate lag measurement, the VDS was kept at 5 V. The gate pulse was created by Agilent 81104A pulse generated with 10% duty cycle and frequency of 100 kHz.

3.3 Results and Discussion

Figure 3-1 shows the optical microscope picture of AlN deposited on Ohmic metal. As shown in Figure 3-1, the AlN peeled off from the edge of the Ohmic metal. The peeling might be due to the stress induced poor adhesion from the AlGaN surface to AlN film. UV ozone treatment was performed to remove the possible carbon contamination to clean the surface. However, as shown in Figure 3-1B, there is no noticeable improvement after ozone treatment. NH₄OH treatment was known to remove surface oxidation such as Al- and Ga- oxide.⁴¹,⁴² As a result, the sample was treated with NH₄OH prior to AlN deposition. As shown in Figure 3-1C, there is no peeling at the Ohmic edge after O₃ UV and NH₄OH treatment.

The refractive index (RI) of a 40 nm AlN film grown on a Si substrate was 1.92 at a wavelength of 632.8 nm, which was slightly lower than the reported value, 2.1.³⁰,⁴⁴ The atomic concentration on the AlN surface layer was oxygen measured with XPS, as shown in Figure 3-2A. To further investigate the content of the AlN film, high resolution scans of the Al 2p peak and N 1s peak were used as illustrated in Figure 3-2B and Figure 3-2C. The Al 2p photoelectron peak at 73 eV was attributed to Al-N bonds. The N 1s photoelectron peak was deconvoluted into 2 subpeaks with binding energies of ~396.07 eV and ~397.9 eV, respectively. The peak at 396.07 eV was attributed to Al-N bonds while the 398 eV peak was attributed to Al-O-N bonds.⁴⁴ Based on the XPS surface analysis, Al₂O₃ was definitely present on the surface of the ALD AlN film. The theoretical RI of AlN and Al₂O₃ were 2.1 and 1.72, respectively. However, the measured RI of the ALD AlN was 1.92. The lowering of the RI indicated the existing of oxygen in the AlN film. Auger electron spectroscopy of AlN film depth profiling was also performed to determine the oxygen throughout the ALD AlN film, as shown in Figure 3-3. The oxygen signal
disappeared at 1-2 nm depth from the top of AlN surface. This Al$_2$O$_3$ layer was formed because of the exposure of AlN to the ambient. Leskelä et al. also reported a similar result that a 5-10 nm thick Al$_2$O$_3$ layer formed after the AlN film was exposed to air.\textsuperscript{75} Figure 3-4 shows the drain I-V and transfer characteristics of the ALD-AlN / AlGaN / GaN MISHEMTs. As illustrated in Figure 3-4 A, the drain current could be modulated to + 4 V of the gate voltage with a sharp channel pinch-off at -3 V of the gate voltage, and the maximum saturation drain current was around 600 mA / mm. The drain current of conventional metal gate HEMTs can typically only be modulated up to around +2 V of gate voltage. In other words, by introducing AlN, the gate voltage modulation was extended around 2 V. This degree of extension was limited by the breakdown field of gate insulator. The breakdown field of unannealed ALD-AlN was reported around 1.7-2.2 MV/cm,\textsuperscript{44,76} thus 10 nm of ALD-AlN should provide an additional 2 V of gate voltage to the typical Schottky barrier height. The breakdown field of the crystalline AlN have been reported as much higher values around 10-12.8 MV / cm.\textsuperscript{78,79} As a result, it is possible to change the process sequence by depositing the ALD-AlN right after the Ohmic metal deposition and annealing both the Ohmic contacts and ALD-AlN at the same time to improve the ALD-AlN crystallinity and breakdown strength. A maximum extrinsic transconductance of 127 mS / mm was obtained; this was comparable to 133 mS / mm for the Schottky gate based HEMT. The reduction in transconductance was due to the increased gate-channel distance from inserting the dielectric layer under the gate contact.\textsuperscript{61,73} There was a negative threshold voltage shift of 0.23 V observed for ALD-AlN MISHEMT as compared to that of the Schottky gate HEMT. Figure 3-4 B also shows the sub-threshold drain leakage current, which strongly depended on the reverse bias gate leakage current. The ALD-AlN MISHEMT, with a 10 nm ALD AlN gate, exhibited a very low sub-threshold drain leakage current of $1.13 \times 10^{-9}$ (A / mm) at $V_G = -3.5$ V and resulted in a large
drain current on-off ratio of $3.3 \times 10^8$. Below the threshold voltage, the drain current increased exponentially with the gate voltage. The slope of this exponential increase on a logarithmic scale was defined as the drain current sub-threshold slope, which has been used to quantify trap densities in the gate modulated region of metal insulator semiconductor field effect transistors.\textsuperscript{79,80} The drain current sub-threshold slope was also dominated by the reverse bias gate leakage current.\textsuperscript{79,80} A drain current sub-threshold slope of 76 mV/decade was obtained, indicating that a good quality AlN / AlGaN interface was achieved.

To investigate the effectiveness of ALD AlN for surface passivation in these structures, we employed gate lag measurements. Figure 3-5 shows the drain current response of an ALD AlN / AlGaN / GaN MISHEMT to a pulsed gate voltage as well as measured in DC mode. In this figure, $V_G$ was pulsed from -5 V to different gate voltages ranging from -2.2 to 0 V at different frequencies with a 10% duty cycle. There was less than a 7% reduction in drain current measured in DC mode compared to the pulsed measurements. By sharp contrast, the unpassivated HEMTs exhibited a 50% decrease in drain current. This is clear evidence that the ALD-AlN effectively mitigated the surface states to avoid current collapse.
Figure 3-1. Optical microscope picture of A) reference B) treated with UV ozone C) treated with UV ozone and NH$_4$OH.
Figure 3-2. XPS analysis of AlN thin film deposited by plasma enhanced mode ALD. A) Surface survey of the as deposited 10 nm AlN by PEALD. B) High resolution scan of Al 2p spectrum. C) High resolution scan of N 1s spectrum.
Figure 3-3. Depth profile of 10 nm AlN thin film deposited by plasma enhanced mode ALD.
Figure 3-4. A) Drain current versus drain bias for different gate bias voltages. B) Transconductance characteristics measured with the MIS-HEMT in saturation.
Figure 3-5. Gate lag measured on the AlN MISHEMT
3.4 Summary

In conclusion, an ALD AlN film was employed as the gate insulator in nitride HEMTs to suppress the gate leakage current and to increase the gate voltage modulation range as well as the passivation layer to reduce drain collapse. GaN MISHEMTs with an AlN gate insulator thickness of 10 nm and 1 μm gate length were fabricated, which exhibited a drain current on-off ratio of $3.3 \times 10^8$, a maximum transconductance of 127 mS / mm and a saturation current of 600 mA / mm at $V_G = +4$ V. The drain current reduction was less than 7% reduction when AlN passivation was introduced. These results indicated that ALD-AlN can be used to improve the performance of AlGaN / GAN HEMTs for high power applications.
CHAPTER 4
HIGH BREAKDOWN VOLTAGE IN ALN/GAN MISHEMTS

4.1 Overview of High Breakdown Voltage HEMTs

There is a strong interest in GaN-based switching devices with breakdown voltages of 600 V or higher for applications in switching mode power supplies and inverter systems where the higher figure of merits obtained relative to Si could reduce power losses.\textsuperscript{22,23} The realization of efficient GaN power devices with high breakdown could lead to smaller, more efficient power supplies. The on-state resistance of GaN can be more than an order of magnitude less than Si, and combined with the higher breakdown voltage this should lead to smaller, simpler cooling systems that result in significant energy savings. These characteristics have made GaN devices potential candidates in power conditioning in large industrial motors, pulsed power for avionics and electric ships, in solid-state drivers for heavy electric motors and in advanced power management and control electronics. There are now commercially available 600 V class GaN power devices, but even higher values are desirable.

The lower on-resistances of AlGaN / GaN heterostructure devices such as high electron mobility transistors (HEMTs) relative to Si transistors are due to the high carrier mobility and larger sheet carrier concentration in the two-dimensional electron gas (2DEG) channels. High breakdown voltage AlGaN / GaN devices have been demonstrated and have shown on-resistances below those achieved in Si. A typical breakdown voltage for HEMTs with a common layer thickness of 2 µm is roughly 800 V. Increasing this voltage requires methods such as acceptor doping of the buffer layer, increasing the active layer thickness, use of a recessed gate or increasing the band gap of the buffer layers through use of AlGaN. Another approach to increasing gate breakdown voltage is to use a metal-insulator semiconductor HEMT (MISHEMT) structure rather than the conventional Schottky gate.\textsuperscript{81-97} While Schottky metal gate
HEMTs offer the highest frequency performance, issues such as current collapse, high gate leakage, and reliability problems related to the stability of the metal gate have limited the potential for high power applications. Many different dielectric layers have been demonstrated for GaN-based metal-oxide-semiconductors (MOS) or MISHEMTs, including SiO₂, Si₃N₄, Al₂O₃, Sc₂O₃, HfO₂, La₂O₃, and TaOₓNy. Use of a gate dielectric with high permittivity produces more efficient gate modulation and thus a smaller decrease in transconductance and threshold voltage shifts. Arulkumaran et al. has employed AlN (band gap 6.2 eV and permittivity of ~8.9) to demonstrate GaN MISHEMTs. Finally, the use of field plates over dielectric passivation layers can increase the device breakdown voltage. The use of two field plates, combined with a gate-drain distance of 24 µm, produced a breakdown voltage of 900 V. This compares to a value of 250 V for devices without field plates.

In this chapter, we report on the breakdown performance of AlGaN / GaN MISHEMTs employing ALD AlN as the gate insulator and surface passivation layer, as a function of gate-to-drain distance without the need for field plates.

4.2 Experimental

4.2.1 Material Growth

HEMT structures were grown on 3 in c-plane Al₂O₃ substrates using a metal organic chemical vapor deposition system, starting with a thin AlGaN nucleation layer followed with a 2 µm low-defect carbon-doped GaN buffer layer, a 23 nm undoped GaN layer, a 21.2 nm undoped AlGaN layer with a 25.6% Al mole fraction and capped with a 2.5 nm undoped GaN layer. Hall measurements on the as-grown structures showed sheet carrier densities of 1.2 × 10¹³ cm⁻² and the corresponding electron mobility of 1050 cm² / V s.
HEMTs Fabrication

Device fabrication began with Ohmic contact deposition with a standard lift-off e-beam evaporated Ti / Al / Ni / Au based metallization, and the samples were subsequently annealed at 850°C for 30 s under N₂ ambient. Typical transfer resistance and sheet resistance of 0.4 Ω-mm and 500 Ω/□ were obtained using the transmission line method (TLM). Multiple energy and dose nitrogen implantation were used for the device isolation, and photoresist AZ1045 was used as the mask to define the active region of the devices. Isolation currents were less than 10 nA at 40 V of bias voltage across two 100 × 100 μm² Ohmic contact pads separated by a 5 μm implanted gap. Prior to the AlN gate insulator deposition, device was treated with UV ozone for three minutes and subsequently treated with 30% NH₄OH for 1 min to remove surface contamination. It is imperative that the nitride surface be as clean as possible to achieve a high quality interface with the gate dielectric. The AlN was deposited in a Cambridge Nano Fiji 200 remote RF-plasma enhanced ALD system at 300°C. The growth rate of AlN film was 0.73 Å/cycle. Trimethyl aluminum (TMA) and N₂ / H₂ plasma were used as the precursors for Al and N, respectively, while Ar was used as the carrier / purging gas. For plasma enhance ALD, N₂ / H₂ flowed into the chamber first and then 300 W of RF power was used to ignite the plasma and kept on for 40 s. The exposure time for TMA was set at 0.06 s and the growth temperature was kept at 300°C. The AlN had a refractive index of 1.92 and no detectable oxygen was measured in the film by Auger Electron Spectroscopy. The breakdown field of the AlN was of the order of 2 MV/cm. After 10 nm ALD AlN deposition, 1 μm × 200 μm gates were achieved via standard lift-off e-beam deposited Pt / Ti / Au metallization and Ti / Au based metallization was utilized for the interconnect metals. The source-drain distance was varied from 5–40 μm, while the gate-source distance was kept at 1.5 μm.
4.2.3 Device Characterization

The DC characteristics of the AlN-MISHEMTs were measured with a Tektronix curve tracer 370A and an HP 4156 parameter analyzer.

4.3 Results and Discussion

Figure 4-1 shows drain current versus source-drain voltage characteristics and off-state drain breakdown voltage as a function of drain bias for different gate bias voltages for devices with drain-source distances of either 10 µm or 40 µm. The AlN layer not only served as the passivation layer but also as a gate insulator. The gate was able to be modulated up to +2 V and both devices showed a pinch-off around -3 V of the gate voltage. Under pulsed conditions, the drain current was typically ~7% less than under DC conditions, showing the effectiveness of the AlN as a surface passivation layer as a gate dielectric. The suppression of DC-to-RF dispersion or so-called current collapse is a key issue for the GaN-based devices and the fact that the AlN can perform as both gate dielectric and surface passivation layer is advantageous. Off-state drain breakdown voltage was measured at a gate voltage of -6 V. The off-state drain breakdown voltage increased from 500 to 2000 V, when the drain to source distance of the devices increased from 10 to 40 µm. With a larger gate-drain distance, parasitic resistance and knee voltage would increase. Owing to the low sheet resistance of AlGaN / GaN MISHEMT, 500 Ω / □, the HEMT on-resistance only increased from 1.3 to 10.9 mΩ / cm² for the devices with the drain-source distance increasing from 10 to 40 µm. The knee voltage increased from 4.8 to 9.5 V for the device with the larger gate-drain distance. Usually the devices with a larger knee voltage suffer with a low output radiofrequency (RF) power efficiency. A higher drain off-state breakdown voltage allows device to be operated a larger voltage range. Since the drain off-state breakdown voltage of the 40 µm devices improved significantly from 500 to 2000 V, the impact of the knee voltage could be neglected.
Figure 4-2 shows transfer characteristics, drain and gate for MISHEMTs with drain-source distance of 10 μm or 40 μm measured at drain voltage of +5 and +10 V, respectively. The peak transconductances were 119 and 90 mS / mm for MISHEMTs with drain-source distance of 10 μm and 40 μm, respectively. The reduction of the peak transconductance was due to the increase of gate-channel distance by inserting the dielectric layer under the gate contact. Although the MISHEMT peak transconductance was lower as compared to the peak transconductance of Schottky gate based HEMT, a much broader transconductance curve was achieved with MISHEMTs which resulted from a higher gate turn-on voltage. Both peak transconductance and saturation drain current were lower for the device with 40 μm drain-source distance owing to larger parasitic resistance. Figure 4-3 shows the saturation drain current as a function of the drain to source distance. The saturation drain current is inversely linear-proportional to the drain to source distance and the slope of the fitting line depends on the sheet resistance of the HEMT structure. As a result of 10 nm AlN gate insulator, these MISHEMTs exhibited a very low gate current in the range of $1.2 \times 10^{-9}$ A/mm at $V_G = -3.5$ V and $V_D = +5$ or +10 V for MISHEMTs with drain-source distance of 10 μm and 40 μm, respectively. Since the sub-threshold drain leakage current is dominated by the gate leakage current, the lower gate leakage current of the AlN based MISHEMTs achieved a large drain current on-off ratio of $3 \times 10^8$. Lower sub-threshold drain leakage not only increases the power added efficiency, linearity, and noise figure of the power amplifiers, it also significantly improves the drain current on-off ratio of the HEMT.

Figure 4-4 A shows off-state drain-source characteristics as a function of gate voltage for individual devices with different drain-source distance, while Figure 4-4 B shows the off-state drain breakdown voltage as a function of gate drain distance ($L_{GD}$) at a fixed gate voltage of -6
V. The latter reached a value of 2000 V at a source-drain distance of 40 µm without the use of field plates. This shows that the combination of a MIS gate and increasing the source-drain distance is capable of producing high breakdown voltage devices with relatively low on-state resistances. The off-state drain breakdown voltage was linearly proportional to the gate-drain distance and the off-state drain breakdown strength derived from Figure 4-4 B was 0.5 MV/cm.

Figure 4-5 shows specific on-state resistance, $R_{on}$, as a function of breakdown voltage.\textsuperscript{11,79,100-106} The theoretical limit line of GaN was calculated using the equation $R_{on} = 4V_{BR}^2 / (\varepsilon \mu E_c^3)$, where $\varepsilon$ is the dielectric constant, $\mu$ is the electron mobility and $E_c$ is the electrical strength of GaN.\textsuperscript{107} The specific on resistance of these devices was calculated based on the total resistance extracted from the low field I–V characteristics in Figure 4-1 and the active area between the source and drain contacts including a 1-µm transfer length from the contact pads. The specific on-state resistances were 1.3, 3.7, 6.6 and 10.9 mΩ-cm\textsuperscript{2} for devices with gate-drain distances of 7.5, 17.5, 27.5 and 37.5 µm respectively. The increase of specific on-resistance for the larger gate-drain devices was resulted from the parasitic resistance of the HEMT structure. The sheet resistance of the AlGaN / GaN used in this work and typical InAlN / GaN based HEMT structure are 500 and 200 Ω / □. By employing InAlN/GaN HEMT structure, the specific on-resistance can be reduced more than 60%. 

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Figure 4-1. Drain current as a function of drain bias for different gate bias voltages for devices with drain-source distance of (A) 10 µm or (B) 40 µm.
Figure 4-2. Transfer characteristics, drain and gate current for devices with drain-source distance of A) 10 µm or B) 40 µm measured with the MISHEMTs in saturation.
Figure 4-3. Saturation drain-source current as a function of drain source distance ($L_{DS}$).
Figure 4-4. A) Off-state drain-source characteristics as a function of gate voltage for individual devices and B) off-state drain breakdown voltage as a function of $L_{GD}$ at $V_G = -6$ V.
Figure 4-5. Specific on-state resistance as a function of breakdown voltage.
4.4 Summary

While use of field plates is an effective method to increase HEMT breakdown voltage, there are penalties in terms of increased process complexity and degradation of high frequency performance because of the additional gate capacitance and thus limitations in terms of power switching above the 1 GHz range. Use of a gate dielectric to produce a MISHEMT structure and then increasing the gate-drain spacing avoids the additional processing complexity of field plate formation and can produce high breakdown voltages. The fact that the gate dielectric can also act as a surface passivation layer is critical because while unpassivated devices show large breakdown due to the reduced field resulting from negatively charged surface traps, the current dispersion is large. The ability of AlN to increase gate breakdown voltage and also passivate these surface traps is an attractive approach. Breakdown voltages up to 2000 V were achieved with use of gate-to-drain spacing of 37.5 µm.
CHAPTER 5
DEGRADATION MECHANISMS OF Ti / Al / Ni / Au-BASED OHMIC CONTACTS ON AlGaN / GaN HEMTs

5.1 Introduction to Ti / Al / Ni / Au Based Ohmic Contacts

The performance of AlGaN / GaN high electron mobility transistors (HEMT) has made remarkable progress in recent years, showing great promise for applications such as military radar and satellite-based communications systems. Due to the large energy band gap of GaN (3.26 eV) and high breakdown field, these devices are well-suited to high power applications. However, due to this large band gap, it is difficult to create a low resistance Ohmic metal on nitride HEMTs. The typical Ohmic contact used is a Ti / Al / Ni / Au metal stack annealed at 800-850°C in N₂ ambient. By changing the annealing temperature or time, a contact resistance of 3.22 × 10⁻⁷ Ω / cm² was achieved for Ti / Al / Ni / Au metal stacks to AlGaN / GaN HEMT. This data is reported for measurement right after annealing and without exposure to chemicals that are part of subsequent processing steps. During the fabrication process, these contacts might be exposed to a number of chemicals, including Buffered Oxide Etchant (BOE) which is an acidic buffered solution. As a result, it is important to know the performance change of Ohmic metal and possible degradation mechanisms after such BOE exposure.

Buffered oxide etchant is a typical etchant to remove the native oxide or passivation layers such as silicon oxide or silicon nitride. It is a mixture of HF and NH₄F, which gives a stable etching performance by acting as a buffering agent to maintain pH. Based on their standard electrode potentials, most of the metals including Ti, Al, Ni are anodic and will react with acid solution to form hydrogen gas. The etching rate of HF for sputtered Ti was reported to be faster than 10 kÅ / min. For another common contact metal, Al, the etching rate in 5:1 BOE solutions was reported to be 11 nm/min. The etching rate of 5:1 BOE solution for Ni and Au is almost zero. During the opening of the passivation layer on HEMTs, the Ohmic metal is
exposed to the BOE solution and it is inevitable it will react with HF. As a result, care must be taken to open the passivation window but not damage the Ohmic metal.

There is no study on changes in Ohmic metal performance of Ti / Al / Ni / Au contacts on nitride HEMTs after BOE treatment. Therefore, it is important to study this performance change after BOE treatment. In this work, we monitored the resistance change of Ti / Al / Ni / Au Ohmic metal when exposed to BOE by four point probe measurements and the transmission line method (TLM). After treatment, energy dispersive X-ray spectroscopy (EDX), Auger analysis was used to quantitatively determine the composition change. Possible mechanisms are discussed to explain the performance changes after BOE treatment.

5.2 Experimental

HEMT structures were grown on Si substrates using a metal organic chemical vapor deposition (MOCVD) system, starting with a thin AlN nucleation layer followed with a 2 μm low-defect carbon-doped GaN buffer layer, a 23 nm undoped GaN layer, a 21.2 nm undoped AlGaN layer with a 18% Al mole fraction and capped with a 2.5 nm undoped GaN layer. Ohmic contact was deposited with a standard lift-off e-beam evaporated Ti / Al / Ni / Au (45 nm / 125 nm / 45 nm / 100 nm) based metallization, and the samples were subsequently annealed at 850°C for 1 min under N₂ ambient. After annealing at 850°C for 1 min under a N₂ ambient, the sheet resistance of the Ohmic metal from four point probe measurements was around 2 Ω/□.

The Ti / Al / Ni / Au Ohmic metal was treated in BOE for 3 min, with the sheet resistance being monitored every 15 sec by four point probe measurements. Scanning electron microscope (SEM) with either backscattering electron detector or secondary electron detector was used to examine the surface morphology change before and after BOE treatment. EDX was used to quantify the composition change before and after BOE treatment. Lastly, Auger depth profiling was used to analyze the composition within the metal film.
5.3 Results and Discussion

Figure 5-1 shows the sheet resistance (Rs) of alloyed Ti / Al / Ni / Au Ohmic metallization as a function of BOE treatment time. The metal sheet resistance gradually increased from 2.7 to 3.7 Ω after 180 sec of BOE treatment. The BOE solution was composed of a 6:1 volume ratio of 40% NH₄F in water to 49% HF in water. Au should be inert in BOE. However, since the standard reduction potentials of Ti, Al and Ni are all negative, oxidation and dissolution processes are favorable for these three metals. The reaction of these three metals with BOE might lift Au metal and result in the increase of metal sheet resistance after treatment in BOE.

Broad area EDX scan was used to estimate the composition change of alloyed Ohmic metallization after BOE treatment, as shown in Figure 5-2, and the composition of each element was averaged for individual content across an area of 30 µm by 30 µm. Unexpectedly, Au decreased by around 7% and Ga increased by 4%. The content of Ti decreased by 0.1% and the contents for the rest of elements, Al, Ni and N, increased by 0.2, 1.3 and 0.6%, respectively. For EDX, the X-rays are generated in a region about 2 µm in depth of the sample. The thickness of the Ti / Al / Ni / Au Ohmic metallization was around 0.3 µm, and thus the EDX signals of Ga and N should be dominated by the bulk GaN even with some Ga or N out-diffusing through the alloyed Ohmic metallization. Thus, it is reasonable to assume that the Ga and N contents did not change significantly. The percent increases of Ga and N content after BOE treatment were due to the decrease of the Au content. By comparing the increases of percent content of Al, it was less than the percent increase of Ga or N. Therefore, besides Ti and Au, the content of Al also decreased after BOE treatment. However the increase of Ti / Al / Ni / Au Ohmic metallization sheet resistance should be mainly caused by the decrease of Au content in the BOE treated sample.
Figure 5-3 shows optical microscope (OM) pictures of alloyed Ohmic metallization before and after BOE treatment, and pictures for the same samples taken with SEM using a secondary electron detector as well as a backscattering electron detector. There were no clear differences for the pictures taken with the optical microscope between Figure 5-3 A the reference and Figure 5-3 B BOE treated sample, and both pictures exhibited very rough surface morphology across the entire alloyed Ohmic metallization. However, the SEM pictures using the secondary electron detector clearly exhibited 3 distinct regions on the alloyed Ohmic metallization. There were islands bulging up and surrounded by a ring, and there was a flat surface between these islands. The SEM pictures also revealed a couple of distinct differences between Figure 5-3 C the reference and Figure 5-3 D BOE treated samples. First, the surface of the islands was etched and became rougher after BOE treatment. Besides etching the surface of islands, those rings surrounding the islands also got etched and became narrower. The height of islands was reduced from around 300 nm to 200-250 nm after BOE treatment, as measured with an Alpha-Step profiler. Further, SEM pictures taken with backscattering electron detector also exhibited 3 distinct regions on the alloyed Ohmic metallization; dark color black islands surrounded by a brighter ring, and islands connected with a gray color area, as shown in Figure 5-3 E and Figure 5-3 F. The signal intensities detected by the backscattering electron detector are proportional to the atomic numbers; the brighter areas are dominated by heavier elements, such as Au in our system, and the darker areas should comprise lighter elements, such as Al. Thus, those darker color islands ranging from 3 to 5 µm must have Al, Ni and Ti bounded by a ~ 1 µm wide ring containing Au. The gray color region, defined as the field region, could have both a heavier element, Au, as well as lighter elements, Al, Ti and Ni. It was reported that Ni-Al intermetallic phases react to form bumps and are bounded by Au-Al intermetallic phases.86
Based on these results, some of the Al and Ga were etched off by BOE. Au in the ring area could be removed by the etching of Al underneath this layer.

Figure 5-4 illustrates the EDX mapping of Au, Ga, Al, Ti, and Ni for reference and BOE treated samples. Al and Ni are mainly located in those islands, and Au and Ga mostly contained in the ring and field areas, respectively. Ti, on the other hand, is uniformly dispensed in the ring and field areas and scattered in the islands. After BOE treatment, the contrast between Au-based rings and the island areas became less obvious, which were consistent with the results obtained by SEM. The intensities of the Ga signal in the ring areas also decreased after BOE treatment. The Al signal generally decreased for the entire areas, which was in line with Auger surface scan result shown in Figure 5-5. For the as-alloyed sample, Titanium (Ti), Aluminum (Al), carbon (C) and oxygen (O) were present on the surface for all three regions. After BOE treatment, Al was removed and Ga was detected in the island areas.

To investigate the depth-dependent composition of alloyed Ti / Al / Ni / Au Ohmic metallization in island, ring and field regions between islands, Auger depth profiling analyses were performed. Figure 5-6 A shows the Auger depth profiling of the island area on the untreated sample. The surface region consisted of C, O, Ti and Al, followed with a 40 nm Ti layer and a layer of 200 nm Ni-Al alloy. Ga clearly diffused throughout the Ni-Al alloy and Ti layer. It has previously been reported that a Ni-Al intermixing layer in these types of contacts was formed after annealing to minimize the interfacial energy. After BOE treatment, the surface Al was removed, as shown in Figure 5-6 B. There was no clear effect of BOE treatment on both Ti and Ni-Al alloy layer. However, there was a Ti peak appearing at the Ni-Al alloy and GaN interface for the reference sample, which was not observed for the untreated sample. Zhou et al. reported that TiN-based contact inclusion (CIs) form at the GaN surface. The diameter and density of
CIs were around 100 nm and $2 \times 10^{-7}$ / cm$^2$, respectively. The Auger beam spot size used in this study was around 35 nm. Thus, it is possible that the CI region might be missed during the Auger depth profiling for the untreated sample.

Figure 5-7 A shows Auger depth profile of the ring area for the untreated sample. There was a surface layer containing C, O, Ti and Al, followed with a Ti layer mixed with Au-Al alloy layer, a thicker Au-Al layer, and an interface layer between Au-Al-Ti alloy layer and GaN. After BOE-treatment, not only was the surface Al was removed, but also some Ti and Au-Al alloyed layers were etched off, as shown in Figure 5-7 B. This is consistent with EDX data which Au decreased around 7%. Although Au is quite stable with acid solution, the etching of surface Al and Al in Au-Al alloy layers might take away Au. The removal of Au on these surface layers increased the Ohmic metallization sheet resistance.

Figure 5-8 shows the Auger depth profiles of the field region of an untreated sample and BOE treated sample. There was a similar surface layer as the one on island and ring areas, containing C, O, Ti and Al, followed with a Ti layer mixed with Au-Al alloy layer, a Ti layer on the top of GaN. After treatment, the surface Al was etched off. There were no changes on the other layers.
Figure 5-1. Sheet resistance of alloyed Ti / Al / Ni / Au-based Ohmic metallization as a function of BOE treatment time measured with the four point probe technique.
Figure 5-2. Percentages of metal elements in alloyed Ti / Al / Ni / Au metallization prior to and after BOE treatment, measured by energy-dispersive x-ray spectroscopy (EDX).
Figure 5-3. OM picture A) before and B) after treatment; SEM pictures from SD C) before and D) after treatment; SEM pictures from BSD E) before and F) after treatment.
Figure 5-4. EDX elemental mappings of alloyed Ti / Al / Ni / Au metallization prior to and after 180 sec of BOE treatment.
Figure 5-5. Auger surface scan analyses of island, ring and field regions for A) untreated sample and B) BOE treated sample.
Figure 5-6. Auger depth profile of the island area on A) untreated sample and B) BOE treated sample.
Figure 5-7. Auger depth profile of the ring area on A) untreated sample and B) BOE treated sample.
Figure 5-8. Auger depth profile of the field area on A) untreated sample and B) BOE treated sample.
5.4 Summary

The degradation of Ohmic metallization dipped in BOE was studied. The sheet resistance increased significantly after treatment in BOE for 3 minutes. Moreover, after annealing, there were island-like structures surrounded by Au-Al alloy rings and a field area between the islands. The BOE etching occurred mainly at the island and ring areas instead of the field area between the islands. The increase of sheet resistance was due to the etching of surface Al and Ti and the loss of Au in the island and ring areas.
CHAPTER 6
EFFECT OF BACKSIDE PROTON IRRADIATION ON ALGAN / GAN HEMT ON OFF-STATE DRAIN BREAKDOWN VOLTAGE

6.1 Introduction to Proton Irradiation

AlGaN/GaN devices successfully proved that they could outperform conventional silicon-based devices in high power, high frequency and high temperature applications (ex. high temperature gas sensors, base station in wireless communication, weather forecasting system, space communication system etc.). Since the lattice constants of wurtzite GaN is $a = 3.19\,\text{Å} \; c = 5.19\,\text{Å}$, which is much smaller than conventional Silicon (5.43 Å) and GaAs (5.65 Å), III-nitrides can demonstrate exceptional tolerance under high energy proton radiations. Typically, proton irradiated AlGaN/GaN high electron mobility transistors (HEMTs) exhibited degradation of Schottky barrier height, gate leakage, saturation drain current and extrinsic transconductance ($g_m$), whose magnitude depends on the proton energy and dose. However, it was recently reported that the off-state drain breakdown voltage and the critical voltage during the off-state drain-voltage step-stress improved in the proton irradiated HEMTs. The defects created by the high energy proton irradiation were evenly distributed throughout the entire HEMT structure. Since the proton irradiation created defects in the GaN buffer layer or in the 2DEG, these effects could not be separated and, it was very difficult to identify the cause of drain breakdown voltage and step-stress critical voltage improvement through the proton irradiation.

In this work, protons were irradiated from the backside of the HEMT active area through via holes etched through the Si substrate. Proton energies of 275 and 330 keV with the doses of $4 \times 10^{12} \,\text{cm}^{-2}$ to $5 \times 10^{12} \,\text{cm}^{-2}$, respectively, were used to place the defects created by proton irradiation at different positions within the HEMT structure. Drain current and off-state drain breakdown voltage were measured before and after proton irradiations to examine the impact of
proton irradiation on device dc performance. The Florida Object Oriented Device and Process Simulator (FLOODs) Technology Computer Aided Design (TCAD) finite-element solver was employed to simulate the electrical field around the gate edge under the influence of proton irradiation induced defects placed at specific locations inside the AlGaN / GaN HEMT structure.

6.2 Experimental

6.2.1 Material Growth

The AlGaN / GaN HEMT structure was grown by metal organic chemical vapor deposition (MOCVD) on Si wafers with conventional precursors in a cold-wall, rotating-disc reactor designed from flow dynamic simulations. The epitaxial layer structure included an AlGaN transition layer,$^{15}$ and an ~ 800 nm thick GaN buffer layer capped with a 16 nm unintentionally-doped Al$_{0.26}$Ga$_{0.74}$N barrier layer.

6.2.2 HEMTs Fabrication

HEMT fabrication began with Ti / Al / Ni / Au Ohmic metallization and rapid thermal annealing in flowing N$_2$ at approximately 825°C. Device isolation was achieved with multiple-energy and multiple-dose of N$^+$ ion implantations. Plasma enhanced chemical vapor deposited (PECVD) 70 nm silicon nitride was used for device passivation. Schottky gate were defined on the SiN$_x$ layer by patterning the gate and selectively removing the SiN$_x$ passivation layer. After SiN$_x$ etching, wider gate patterns were redefined with another photolithography step and Ni / Au-based gate metallization was deposited as the gate metallization. The wafers were then passivated with another 400-nm layer of PECVD SiN$_x$ at 300°C. There was an additional metal deposition for the HEMT with the source field plate. The field plate was connected to the source terminal and extended by 1 μm out over the gate to the gate-to-drain region. Rectangular via holes, which covered the entire device active area, were fabricated from the back side of the sample (the Si substrate side), by etching through the Si substrate and stopping on the AlGaN
transition layer with a standard Bosch process using a Surface Technology Systems (STS) deep reactive ion etching (DRIE) system. Figure 6-1 shows the TEM cross section view of the device used in this study.
Figure 6-1. Cross-sectional TEM image of AlGaN/GaN HEMT structure.
6.2.3 **Device Irradiation Simulation and Experiment**

Proton irradiations were performed with proton energy at 275 and 330 keV and proton doses of $4 \times 10^{12}$ cm$^{-2}$ and $5 \times 10^{12}$ cm$^{-2}$, respectively, to achieve the same peak vacancy concentration from the back side of the samples. The implanted samples were intentionally tilted $7^\circ$ away from the normal direction of the proton beam to prevent the channeling effect. The Stopping and Range of Ions in Matter (SRIM) simulator was used to estimate the penetration depth of the protons into the AlGaN / GaN HEMT structure and the distributions of the Ga and N vacancies generated through proton irradiations.

6.2.4 **Electrical Simulation**

The FLOODS TCAD finite-element solver was employed to simulate the electric field around the gate edge under the influence of proton irradiation induced defects placed at specific locations inside the AlGaN / GaN HEMT structure. To model irradiation-induced changes, the Ga and N vacancy concentrations, $Trap$, estimated with the SRIM simulation were included in the Poisson equation as shown in Equation 6-1.

$$\nabla^2 \psi = -\frac{q}{\varepsilon} [p - n + Doping + Trap] \quad \text{Eq. 6-1}$$

where $\psi$ is electrostatic potential, $n$ is the density of electrons, $p$ is the hole density, $Doping$ is the ionized pre-irradiation acceptor or donor densities, $Trap$ is the ionized post-irradiation trap concentration, $q$ is charge, and $\varepsilon$ is permittivity. The continuity equations for electrons and holes were simultaneously solved with the Poisson equation.

6.2.5 **Device Characterization**

Device DC performance was measured with an Agilent 4156C parameter analyzer, and the off-state drain breakdown voltage measurements was conducted with a Glassman high voltage power supply.
6.3 Results and Discussion

Figure 6-2 shows the schematic view of the vacancy distribution among the device after irradiation at 275 and 330 keV. As shown in Figure 6-2, the tails of the vacancy distribution profiles dropped very sharply. Utilizing this feature, by irradiating the device from the backside of the wafer, the defects could be placed at specific region, i.e. transition layer, buffer layer or 2DEG layer. As a result, 275 keV and 330 keV were chosen to put the defects at buffer layer and 2DEG layer respectively. The purpose of selecting doses at $5 \times 10^{12}$ cm$^{-2}$ or $4 \times 10^{12}$ cm$^{-2}$ was to create a similar peak vacancy density as the vacancies created with the conventional MeV implantation from the front side of the sample.

Figure 6-3 shows the drain I-V characteristics before and after irradiation with 330 keV protons from the backside of the samples. The drain voltage was swept from 0 V to 3 V, and the corresponding drain current was measured at different gate voltage ranging from 0 to -2 V with a step of -0.5 V. As illustrated in Figure 6-3, the drain current suffered a 13% reduction for the HEMTs irradiated with 330 keV protons, demonstrating that the proton irradiation induced defects placed in the 2DEG region and AlGaN barrier layer degraded the drain current. On the contrary, no drain current degradation was observed for the HEMTs irradiated with 275 keV protons from the backside of the sample. This indicates that the proton irradiation induced defects placed in the GaN buffer do not affect the drain current. Figure 6-3 also shows the off-state drain breakdown voltage of the un-irradiated and 330 keV proton irradiated HEMTs. These proton irradiated HEMTs exhibited an improvement of off-state drain breakdown voltage, similar to the previously reported MeV proton irradiated HEMTs. There was no such improvement of the off-state drain breakdown voltage observed for the HEMTs irradiated with 275 keV protons. Thus, the defects placed in the GaN buffer layer by 275 keV irradiation only decreased the residual conductivity of the un-intentional doped GaN buffer. On the contrary, the
vacancies placed in the 2DEG channel and AlGaN barrier with 330 keV proton irradiations not only removed carriers and decreased the drain current but also could form a virtual gate resulting from the charged vacancies. Such a virtual gate could change the electric field distribution around the gate edges. By reducing the maximum electric field under the drain side of the gate edge, the off-state drain breakdown would be improved.

Figure 6-4 shows the simulated electric field distributions around the gate edge for the proton irradiated and the pre-irradiated HEMTs. By introducing a virtual gate in the GaN buffer layer assuming 4% of the vacancies created by the proton irradiation with a dose of $4 \times 10^{12} \text{ cm}^{-2}$ become negatively-charged traps, the simulated peak electric field at the gate edges only lessened around 1% for the post-irradiated HEMT as compared to the pre-irradiated HEMT. Therefore, it seemed unlikely that the increase of off-state drain breakdown voltage could be attributed to the electric field reduction at the gate edges by charged defects in the GaN buffer. By sharp contrast, by introducing the same amount of negative trap charges introduced by the irradiation at the AlGaN / GaN interface, the simulated electric field at the gate edges was reduced 50%. Thus the improvements of the off-state drain breakdown voltage for 330 keV proton irradiations are consistent with the simulated results.
Figure 6-2. Schematic of backside proton implantation through via hole and proton irradiation-induced vacancy distributions as a function of proton penetration depth.
Figure 6-3. Drain I-V characteristics of the HEMT before and after irradiated with a proton energy of 330 keV and a dose of $5 \times 10^{12} \text{ cm}^{-2}$. 
Figure 6-4. Electric field distributions around the gate edge for the proton irradiated and the pre-irradiated HEMTs.
6.4 Summary

In summary, we studied the effect of proton irradiations on DC performance and off-state drain breakdown voltage of AlGaN / GaN HEMTs grown on Si substrates. Proton irradiations were performed from the backside of the samples through via holes fabricated on the Si substrate. There was no degradation observed for the proton irradiated AlGaN / GaN HEMTs in which the defects created by the proton irradiations were intentionally placed in the GaN buffer. On the contrary, the irradiated HEMTs with the defects placed in the 2DEG channel region and AlGaN barrier using higher energy protons showed degradation of drain current and extrinsic transconductance. FLOODS TCAD finite-element simulations were performed to confirm the hypothesis of a virtual gate formed around the 2DEG region to reduce the peak electric field around the gate edges and increase the off-state drain breakdown voltage.
CHAPTER 7
EFFECT OF LOW DOSE GAMMA IRRADIATION ON DC PERFORMANCE OF ALGaN / GaN HIGH ELECTRON MOBILITY TRANSISTORS

7.1 Introduction to Gamma Irradiation

AlGaN / GaN high electron mobility transistors (HEMTs) have received increasing attention because of their great promise for applications such as military radar and satellite-based communications systems.\textsuperscript{1,22} Due to their potential use in extreme radiation environments, it is important to characterize the hardness of the AlGaN / GaN heterostructure under these environments. There are many studies reporting the performance under proton,\textsuperscript{112} neutron,\textsuperscript{113} and electron irradiation\textsuperscript{120} for AlGaN / GaN HEMTs. However, comparable studies for γ-irradiation are limited. The effect of γ-irradiation on these devices is both qualitatively and quantitatively different from other forms of radiation, e.g. some studies report drain saturation current increases \textsuperscript{121,122} while others report decreases after γ-irradiation.\textsuperscript{123-125} In addition, the mechanism for the current changes is not well understood. Detailed studies are needed to characterize the performance of HEMTs after γ-irradiation.

The bulk of experiments with AlGaN / GaN HEMTs\textsuperscript{121-124} and GaN\textsuperscript{126} diodes have been carried out using \textsuperscript{60}Co γ-irradiation of various energies and doses. Compton electrons induced from γ-radiation create electron-hole pairs, thus changing occupancy of traps. Unlike proton irradiation,\textsuperscript{112} some studies claim that these defects can improve device performance such as increasing drain saturation current.\textsuperscript{121,122} These defects are believed to be nitrogen vacancies that have electrical activation energies about 216 meV from the conduction band. Nitrogen vacancies act as donors and increase the effective channel doping and thus increase $I_{DS}$.\textsuperscript{121} These types of defects have been reported after low-energy proton, electron, and γ-irradiation.\textsuperscript{122,127-129} It was also reported that low dose γ-irradiations partially relaxed the AlGaN/GaN hetero-structure...
elastic strains and enhanced the electron mobility by around 7-8%. This improvement of the electron mobility could also increase the drain current.

In contrast to these results, Schwartz et al. showed that the drain current was reduced by about 60% after γ-irradiation at around 700 Gy. These defects in that case must reduce the carrier concentration in the irradiated devices, and there was more degradation with increasing γ-irradiation dose. The defects produced by γ-irradiation may be structure sensitive which would be one reason for the discrepancies between different reports. Also, dose clearly plays a role in the performance of the devices after irradiation. Vintusevich et al. found out that at 10^5 rad, the Ids increased but started to deteriorate after higher doses of 10^6 rad.

In this study, we report on the effect of low dose γ-irradiations on DC characteristics of AlGaN / GaN HEMTs. Drain and gate I-V characteristics, sheet resistance, sub-threshold drain and gate current as well as gate lag measurements were conducted for the HEMTs prior to and after γ-irradiations.

7.2 Experimental

7.2.1 Material Growth

AlGaN / GaN HEMTs layer structures were grown on c-plane Al₂O₃ substrates by molecular beam epitaxy. The layer structure consisted of a thin AlGaN nucleation layer followed with a 2 μm thick undoped GaN buffer topped by a 25 nm thick unintentionally doped AlGaN layer. The mobility was determined to be 1080 cm²/V-s with a sheet carrier concentration of ~1x10^{13} cm⁻² by Hall measurements conducted at room temperature.

7.2.2 Device Fabrication

Device fabrication started with mesa isolation. Mesa isolation was achieved by using an inductively coupled plasma system with Ar / Cl₂-based discharges. The Ohmic contacts were formed by lifting-off e-beam evaporated Ti / Al / Ni / Au (200 Å / 1000 Å / 400 Å / Au 800 Å).
The contacts were annealed at 850°C for 45 s under a flowing N₂ ambient in Heatpulse 610T system. Standard lift-off of e-beam deposited Ni / Au was used for gate metallization. 1000 Å plasma enhanced chemical vapor deposited SiNₓ was used for device passivation and the crossover between the gate finger and gate contact pad. The final step was the deposition of e-beam evaporated Ti / Pt / Au (300 Å / 200 Å / 2000 Å) metallization for interconnection contacts. Figure 7-1 shows a micrographic image of the circular AlGaN / GaN. The diameter of the circular gate finger was 100 µm and the gate dimension was 1.5 µm × 314 µm. The gate to source and gate to drain distance were kept at 2 and 4 µm, respectively. Transmission line method (TLM) testers were also fabricated along with the HEMTs for monitoring sheet resistance change upon the γ-irradiations.
Figure 7-1. Device configuration of the circular HEMTs.
7.2.3 Gamma Irradiation and Device Characterization

Devices were exposed to $^{60}$Co $\gamma$-rays with different doses of 50, 300, 450, or 700 Gy. Irradiations were performed at temperatures <50°C. During irradiation, the samples were held in nitrogen ambient and the electrodes of the HEMTs were floated. The device DC performance was characterized using an Agilent 4156 parameter analyzer.

7.3 Results and Discussion

Figure 7-2 illustrates the drain I-Vs of a typical circular HEMT before and after 450 Gy of $\gamma$-irradiation as well as drain current increase percentage as a function of $\gamma$-irradiation dose, respectively. In Figure 7-2 A, the drain I-V curves were modulated by sweeping the gate voltage from 0 to -3 V with a step of -1 V. The drain saturation current increased from 293 to 339 mA/mm after 450 Gy of $\gamma$-irradiation. As shown in Figure 7-2 B, the saturation drain current increased around 10% after $\gamma$-irradiations with the doses used in this experiment. As mentioned in the introduction, several groups have reported drain current increases after low doses of $\gamma$-irradiation. However, different mechanisms for such drain current increases were proposed. Aktas et al. reported around 10% increase of drain current at $V_G = 0$ V and 6 V of drain voltage after 300 or 600 Mrad $\gamma$-irradiation, and there was no change of sheet resistance or mobility observed after the irradiation. They suggested that donor type defects generated by $\gamma$-irradiation contributed electrons to the channel under the gate. The density of these defects are small enough not to effect the linear band bending induced by the polarization charge, thus there is no effect on the conduction channel under the silicon passivated layer to vary the sheet resistance. Bertlhet et al. studied the effect of 4 krad $\gamma$-irradiation on drain current, Schottky gate characteristics, sheet resistance measured with TLM testers, and light sensitivity of the drain current under white light illumination. They advocated that the low dose $\gamma$-radiation produced a decrease of the electrical traps and resulted in an increase of drain current, with a lower drain I-
V on-resistance. The HEMT also became less sensitive to the white light due to the decrease of the traps. There was no change for the Schottky gate characteristics or the sheet resistance of the TLM testers after irradiation. Besides the commonly observed drain current enhancement after a low dose $\gamma$-radiation, Kurakin et al. reported a decrease of sheet resistance resulting from an increase of electron mobility through the relaxation of the elastic strain in the HEMT heterostructures.\textsuperscript{130} Magneto-transport spectroscopy exhibited a significant decrease in short-range carrier scattering, which was also consistent with the increase of mobility measured by Hall measurements. X-ray diffraction spectra revealed a shift of the peak corresponding to the (0004) plane of the AlGaN layer to a lower angle indicating a strain relaxation in the AlGaN layer after irradiation. They also employed surface curvature measurements to confirm the relaxation of the elastic strain in the HEMT hetero-structures.

In our study, the impacts of $\gamma$-radiation on HEMT performance were generally different from previously reported results. As illustrated in Table 7-1, drain current, electron mobility, on-state resistance, source and drain resistance as well as sheet resistance were all affected by the $\gamma$-radiation. The electron mobility was assessed using the drain I-Vs at different gate voltages in the low field region, the on-state resistances were determined by dividing the device total resistance of the saturated drain I-V in the low field region with the active area of the device. The source and drain resistances were estimated with sheet resistance, TLM transfer resistance and device layout configuration. Unlike the work from Berthlet et al., in our case, the channel resistance reduction and drain current increase were responsible for the reduction of the on-resistance.\textsuperscript{121} In contrast to the work from Kurakin et al., the sheet resistance reduction in our case can be attributed to the mobility increase in the channel.\textsuperscript{130} In our study, the on-state resistance or device total resistance reduction resulted from the decreases of source, drain and
channel resistances, as shown in Figure 7-3. In other words, the drain current increase and on-resistance reduction in this study could be due to the combined effects of strain relaxation induced electron mobility enhancement and additional carriers under the gate provided by γ-radiation generated donor type defects.

Besides the resistances and electron mobility, the effects of the γ-radiation on the drain current sub-threshold characteristics were also investigated, as shown in Figure 7-4. The drain current was measured as a function of the gate voltage for the reference and 450 Gy γ-irradiated samples at a fixed drain voltage of 5 V, and the gate current was simultaneously recorded during the drain current measurement. The sub-threshold leakage current, sub-threshold slope and on/off drain current ratio are essential to the power added efficiency, linearity, noise figure and reliability of power amplifiers. The current sub-threshold characteristics were insensitive to the low dose γ-radiation. The typical drain current on-off ratio and the sub-threshold slope for the reference HEMTs were in the range of 105 and 95 mV / dec, respectively and there was no difference observed between the reference and γ-radiated HEMTs.

Figure 7-4 B shows the gate I-V characteristics of typical AlGaN / GaN HEMTs before and after γ-irradiation with doses of 450 Gy. The gate I-Vs were measured by sweeping the gate voltage from +1 to -10 V, grounding the source electrode and floating the drain electrode. The ideality factor was not sensitive to the γ-irradiation and barely changed for samples irradiated with other doses as well. The Schottky barrier heights were 0.72 and 0.73 V for the reference and γ-irradiated HEMT, respectively. The differences of the Schottky barrier height were within the measurement errors. There was a very slight increase of the reverse biased gate leakage currents.

Gate pulse measurements were also performed, in which the drain was fixed at +5 V and the gate was simultaneously pulsed from -5 V to the values shown on the x-axis at 10 kHz with
10% duty cycle. As illustrated in Figure 7-5 A, there was no dispersion between DC and pulsed data observed for the reference sample. HEMTs exhibited around 5% drain current dispersions after γ-irradiations regardless of the doses due to more defects being generated close to the surface in the access region between the gate and drain, where a virtual gate was formed resulting from the injection of hot electrons into the surface between the gate and drain electrodes.
Figure 7-2. A) Drain I-V of a circular AlGaN/GaN HEMT before and after γ-irradiation at a dose of 450 Gy. B) Drain current increase as a function of γ-irradiation dose.
Table 7-1. Summary of drain current at $V_G = 0$ V, on-state resistance, device total resistance, sheet resistance and mobility prior and after exposure to $\gamma$-irradiation.

<table>
<thead>
<tr>
<th>Dose (Gy)</th>
<th>Ref.</th>
<th>50</th>
<th>300</th>
<th>450</th>
<th>700</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\triangle I_{DS}$ (%)</td>
<td>(300)</td>
<td>10.24</td>
<td>7.85</td>
<td>9.82</td>
<td>11.44</td>
</tr>
<tr>
<td>% Total resistance ($\Omega$) decrease</td>
<td>(38)</td>
<td>4.82</td>
<td>7.48</td>
<td>14.99</td>
<td>14.37</td>
</tr>
<tr>
<td>% On-state resistance ($\Omega / \text{cm}^2$) decrease</td>
<td>$(1.1 \times 10^6)$</td>
<td>-</td>
<td>1.17</td>
<td>0.85</td>
<td>2.29</td>
</tr>
<tr>
<td>% Sheet Resistance ($\Omega / \square$) decrease</td>
<td>(510)</td>
<td>-</td>
<td>0.2</td>
<td>0.8</td>
<td>3.6</td>
</tr>
<tr>
<td>% Mobility ($V / \text{cm}^2$-s) increase</td>
<td>(1200)</td>
<td>18.48</td>
<td>17.43</td>
<td>35.71</td>
<td>34.53</td>
</tr>
</tbody>
</table>
Figure 7-3. Source resistance, drain resistance, channel resistance and total resistance of a circular AlGaN / GaN HEMT as a function of γ-irradiation dose.
Figure 7-4. A) Sub-threshold drain and gate current of HEMT before and after γ-irradiation with a dose of 450 Gy. B) Gate I-V before and after γ-irradiation with a dose of 450 Gy.
Figure 7-5. Gate lag measurements of circular AlGaN / GaN HEMTs before and after γ-irradiation with different doses.
7.4 Summary

The effect of relatively low dose $\gamma$-irradiation doses of 50, 300, 450 or 700 Gy on circular AlGaN / GaN HEMTs has been studied with dc and pulse measurements. The increases in drain currents and the reduction of on-state resistance for the $\gamma$-irradiated samples could be due to the combined effects of strain relaxation induced electron mobility enhancement and additional carriers generated under the gate via $\gamma$-radiation generated donor type defects. The sub-threshold drain and gate current were insensitive to the $\gamma$-irradiation. The Schottky barrier height and ideality factor of the HEMTs were not influenced by the lose dose $\gamma$-radiation either. There was a minimal drain current dispersion observed for the $\gamma$-radiated HEMTs due to more defects generated between gate and drain, where an virtual gate was formed resulting from the injection of hot electrons into the surface between gate and drain electrodes.
CHAPTER 8
EFFECT OF ELECTRON IRRADIATION ON ALGAN / GAN AND INALN / GAN HETEROJUNCTIONS

8.1 Introduction to Electron Irradiation

AlGaN / GaN high electron mobility transistors (HEMTs) based on AlGaN / GaN heterojunctions (HJs) have applications in radar and communications systems.\textsuperscript{133} They must sustain their characteristics when subjected to irradiation in space and military applications, and nuclear safety. For space applications, the most important types of particles are protons with energies up to hundreds of MeV, electrons with energies up to 10 MeV, as well as $\alpha$-particles, $\gamma$-rays, and heavy particles with very high energies.\textsuperscript{134} Early experiments performed on single layers of GaN and on AlGaN / GaN HEMTs showed that, in general, the radiation tolerance of GaN and GaN-based devices to all types of radiation is much higher than for their AlGaAs / GaAs counterparts.\textsuperscript{135-137} For single layers of n-GaN, the main defects introduced were the nitrogen vacancy $V_N$ related donors with levels near $E_C-0.06$ eV, the nitrogen interstitials related acceptors $Ni$ with levels near $E_C-1$ eV, and relatively shallow electron traps with levels near $E_C-(0.15-0.18)$ eV and $E_C-0.2$ eV.\textsuperscript{136,138} The latter defects were variously attributed to complexes involving gallium vacancy-nitrogen interstitials $V_{Ga-N_i}$\textsuperscript{139} or nitrogen vacancies-nitrogen interstitials $V_N-N_i$.\textsuperscript{138,140} Among the defects on the gallium sublattice deep Ga vacancy acceptors $V_{Ga}$ with the triply negatively charged state level predicted to be near $E_V+1$ eV and Ga interstitials donors $Ga_i$ with levels close to $E_C-0.9$ eV.\textsuperscript{141}

The bulk of experiments with AlGaN / GaN HJs and HEMTs have been carried out using protons of various energies.\textsuperscript{142-147} The main effects observed were a decrease of 2DEG mobility and the decrease of the negative threshold voltage of transistor structures $V_{TH}$. For reactor neutron irradiation\textsuperscript{113} and for 10MeV electron irradiation of MBE grown AlGaN / GaN HJs,\textsuperscript{148} similar effects were observed. A higher radiation tolerance of AlN/GaN HJs compared to AlGaN
/GaN HJs subjected to electron irradiation was attributed to lower energy deposited into lattice defects formation in the thinner AlN barriers.\textsuperscript{53}

There has been much less research on the effects of electron irradiation of GaN. Look \textit{et al.} showed that electron irradiation with energies 0.7-1 MeV introduced new donors with ionization energy of~ 0.06 eV and introduction rates of 1 cm\textsuperscript{-1}.\textsuperscript{149-151} The net electron concentration was not affected while the electron mobility decreased with dose. Acceptor centers were introduced at a rate similar to the rate of the 0.06 eV donors. Deep centers in as-grown, electron-irradiated n-GaN on sapphire using 1 MeV electrons were ascribed to N vacancy related centers (the 0.06 eV donors) and a deeper center with a thermal activation energy of 0.85 eV. Electron irradiated n-GaN showed the presence of deep electron traps with activation energies of 0.9 eV that could be attributed to N\textsubscript{i} acceptors. In undoped n-GaN samples irradiated with 10 MeV electrons, deep acceptor traps with activation energy ~1 eV were attributed to N\textsubscript{i} 2.5 MeV electron irradiation at 4.2K of GaN produced a strong defect photoluminescence band near 0.95 eV, for which optically detected electron paramagnetic resonance spectra could be obtained. The transition was attributed to Ga vacancies, V\textsubscript{Ga}, with a level near E\textsubscript{v}+1 eV and the optically detected electron paramagnetic resonance (ODEPR) process was interpreted as interaction with two different Ga\textsubscript{i} interstitial centers with levels close to E\textsubscript{v}+2.6 eV. The quenching of the electron resonance signal for annealing to room temperature was then attributed to moving of the Ga\textsubscript{i} defect away from V\textsubscript{Ga}.

In terms of the effects of electron irradiation on GaN devices, McClory \textit{et al.} reported the effects of 0.45 MeV electron radiation on the gate and drain currents of Al\textsubscript{0.27}Ga\textsubscript{0.73}N / GaN High Electron Mobility Transistors (HEMTs).\textsuperscript{152} Following irradiation, the gate and drain currents increased at low temperatures and reached a saturation level. Following a subsequent
room temperature anneal, the gate and drain currents returned to pre-irradiation levels. These results were explained by the buildup of positive charge in the AlGaN layer at low temperature and traps formed in the AlGaN layer. The positive charge increased the carrier concentration in the two dimensional electron gas (2DEG) and hence the drain current.

Studies of AlGaN / AlN / GaN, AlGaN / GaN, and InAlN / GaN HJs after fast reactor neutron irradiation showed an increase in the density of deep negatively charged traps in the barrier or at the interface with GaN. These deep centers have thermal activation energy of 0.6-0.8 eV, optical ionization energy of 1.5-1.7 eV and a high barrier for capture of electrons, resulting in persistent changes in the charged state of the traps after illumination at low temperature. They are present in high areal concentration of >10^{12} cm^{-2} in all types of HJs and HEMTs. They account for deviation to more positive voltages of room temperature $V_{TH}$ values in AlGaN / AlN / GaN HJs as compared to the results of modeling based solely on the strength of the piezoelectric and spontaneous polarization field. The filling of these centers by electrons due to tunneling from the Schottky metal at high reverse voltage is responsible for the shift of low temperature $V_{TH}$ after cooling at high reverse voltage as compared to cooling at 0 V, whilst persistent $V_{TH}$ decreases after illumination are also caused by these centers.

In this paper we perform similar analysis for the effects of 10 MeV electrons irradiation on electrical properties of MOCVD grown HJs. We compare results for AlGaN / GaN, AlGaN / AlN / GaN, InAlN / GaN HJs on sapphire substrates with those for AlGaN / GaN HJs and HEMTs on Si substrates and show that, as with neutron irradiation, the presence of deep acceptor centers can explain the results of electron irradiation in GaN-based HJs and HEMTs. Since the radiation effects in GaN-based heterojunctions grown on Si have not been studied in any detail, the main thrust in these experiments was on the behavior of AlGaN / GaN / Si HJs and HEMTs.
8.2 Experimental

8.2.1 HEMTs Fabrication

HEMT device fabrication involved Ohmic contact deposition with standard lift-off e-beam evaporated Ti / Al / Ni / Au annealed at 800°C for 30 s under N₂ ambient. Multiple energy and dose nitrogen implantations were used for device isolation and AZ1045 resist used as the mask to define the active region of the devices. Isolation currents were <10 nA at 40 V bias across two 100 µm × 100 µm Ohmic pads separated by a 5 µm implanted gap. 1 µm gates were defined by lift-off of an e-beam evaporated metal stack of Pt / Ti / Au (total gate length of the multi-finger gate was 8000 µm). Ti / Au metallization was used for the interconnect metals for source, gate, and drain electrodes. The transistors were passivated with 400 nm of plasma enhanced chemical vapor deposited SiNx at 300°C, followed by opening of contact windows using plasma etching.

8.2.2 Device Characterization

Static current-voltage (I-V) characteristics were measured for the HEMTs before and after the electron irradiation, including transconductance (g_m) and sub-threshold characteristics at various doses using an Agilent 4156C.

Gate pulse measurements were employed to evaluate traps created during electron irradiation. In this technique, the drain current (I_DS) response to a pulsed gate-source voltage (V_GS) was measured. The V_GS was pulsed from -5 V at frequencies of 100 Hz and 10 kHz with 10% duty cycle, while drain voltage was kept constant at +5 V. The reduction of the drain current in the pulsed mode as compared to the drain current in the dc mode was due to the presence of traps located in the access region between gate and drain contact. In addition, gate-source C-V and I-V characteristics of transistors were measured at different temperatures for cooling in the dark at various gate voltages and after illumination at low temperature, as for the
large area Schottky diodes on HJs. These measurements were complemented by deep level transient spectroscopy (DLTS) and admittance spectra measurements. The measurements conditions for DLTS was biased at -1.5 V, forward bias pulse of 1 V, time windows 1 ms / 10 ms. The 2DEG concentration and mobility at room temperature before and after electron irradiation was measured by Hall / van der Pauw using evaporated In contacts in the standard geometry. For HJs, capacitance-voltage (C-V), current-voltage (I-V) and admittance spectra were measured on Ni Schottky diodes with area 5\times10^{-3} \text{ cm}^2. Low temperature C-V characteristics were observed after cooling down in the dark at various reverse biases and after illumination with high power GaN-based light emitting diodes (LEDs) with wavelength 365 - 660 nm.\textsuperscript{156,158}

### 8.3 Results and Discussion

The results of Hall / van der Pauw measurements performed on the four studied types of HJs before irradiation are presented in Table 8-1. The trends in these results are expected. The 2DEG concentration in AlGaN / GaN / sapphire structure is the lowest and increases when a thin AlN interlayer is introduced due to increased strain. The main effect is the increased 2DEG mobility in the AlGaN / AlN / GaN HJ caused by suppression of scattering on ionized donors and on composition fluctuations in AlGaN by the undoped AlN insert. For the AlGaN / GaN / Si structure, the 2DEG concentration and mobility are not too different from the structure on sapphire indicating a good quality GaN buffer on Si and AlGaN/GaN interface, although the lower threshold voltage $V_{TH}$ as determined from C-V characteristics indicates a higher strain level in the structure. For the InAlN / GaN HJ the 2DEG concentration is high due to the high spontaneous polarization field while the 2DEG mobility is relatively low, which points to a comparatively high defect density characteristic currently for such heterojunctions.
After electron irradiation the 2DEG concentration is only slightly affected and the main
effect is the gradual decrease of the 2DEG mobility in all HJs, as illustrated by Figure 8-1. The
rate of mobility decrease is comparable for AlGaN / AlN / GaN / sapphire, AlGaN / GaN /
sapphire, and AlGaN / GaN / Si HJs suggesting that the radiation tolerance of the structures on
sapphire is not significantly lower than for those on sapphire. The onset of mobility degradation
is near a fluence of $5 \times 10^{15}$ cm$^{-2}$, close to that reported for AlGaN / GaN / sapphire HJs grown
by MBE.$^{157}$ However, the rate at which the 2DEG mobility of MOCVD grown AlGaN / GaN
HJs decreases for further higher doses is much lower than previously reported for the MBE
grown structures.

For InAlN / GaN HJs the degradation of 2DEG mobility with electron fluence proceeds
much faster than for other HJs. For the highest electron fluence of $3.3 \times 10^{16}$ cm$^{-2}$, no 2DEG
conductance could be observed. This is in line with the results reported for neutron irradiated
HJs.$^{155}$ For AlGaN / AlN / GaN HJs with Al mole fractions in the AlGaN barrier of 40% and
50%, the rate of 2DEG mobility decrease was also much higher than for the barriers with 20%
and 30% Al. The conclusion, as in the case of neutron irradiation,$^{155}$ is that the lower the
crystalline quality of the barrier layer and the higher the expected level of contamination, the
lower is the radiation tolerance of the heterojunctions.

Based on previous neutron irradiation data, changes in the threshold voltage of transistors
and in 2DEG mobility might depend on the density of deep acceptor traps in the barrier or at the
barrier interface with GaN. Such deep acceptors are present in high density in all studied HJs.$^{155-}
156$ The deep acceptors densities in the AlGaN / AlN / GaN / sapphire, AlGaN / GaN / sapphire,
AlGaN / GaN / Si, and InAlN / GaN / sapphire are, respectively, $1.7 \times 10^{12}$ cm$^{-2}$, $1.5 \times 10^{12}$ cm$^{-2}$,
(1-1.4) × 10^{12} \text{ cm}^2, and 3.4 × 10^{12} \text{ cm}^2. These concentrations increase with electron irradiation, as will be seen below.

Figure 8-2 compares the room temperature C-V characteristics of the AlGaN / GaN / Si HJ before and after irradiation with the fluence of $1.3 × 10^{16} \text{ cm}^{-2}$ of 10 MeV electrons. The threshold voltage $V_{TH}$ (determined as the voltage at which the 2DEG electrons are driven away from the triangular quantum well near the interface and the space charge region boundary moves into the GaN buffer) decreases by 0.2 V after irradiation and the capacitance in accumulation decreases. This is similar to neutron irradiated HEMT structures\textsuperscript{155} and can be attributed to increased concentration of deep acceptors in the barrier. The increase in concentration to account for such shift would be $7 × 10^{11} \text{ cm}^{-2}$. The decreased capacitance after irradiation could be due to increased non-uniformity of $N_{ss}$ causing local total or partial pinching off of the 2DEG thus reducing the effective 2DEG area. These local variations can also change the effective 2DEG Hall mobility if the Fermi level at the surface is pinned.\textsuperscript{155} The reason is the switching from uniform two-dimensional conductivity to percolation type conductivity because of the fluctuations of local band bending caused by high density of deep acceptors.

The concentration of $N_{ss}$ before and after irradiation can be estimated from the difference in $V_{TH}$ values obtained from low temperature C-V characteristics measured after cooling down in the dark and after subsequent illumination. Figure 8-3 compares these C-V characteristics before and after irradiation. The curve, marked as “cooled at 0 V”, was taken after cooling in the dark without bias. The curve, marked “cooled at -2 V”, was taken after cooling at -2 V in the dark. The curve, marked as “PPC”, corresponds to measurements after cooling down in the dark at -2 V and illumination with 365-nm-wavelength LED; it shows the PPC increase after illumination and was used for calculating the density of deep traps in the barrier / interface. Before irradiation
the calculated Nss value is $1.4 \times 10^{12}$ cm$^{-2}$, after irradiation it is $2.1 \times 10^{12}$ cm$^{-2}$ and the difference fits the room temperature data. Further irradiation to $3.3 \times 10^{16}$ cm$^{-2}$ increased the Nss value to $3.1 \times 10^{12}$ cm$^{-2}$, i.e. the Nss change is approximately linear with fluence, with an introduction rate of about $5 \times 10^{-5}$.

Standard DLTS measurements on large area Schottky diodes on HJs are unreliable because of the shift of the threshold voltage with temperature during the measurements and the effects of the series resistance of the structure. Such measurements are possible for HEMT structures with the total Schottky gate contact area suitable for capacitance transient detection, as for the structures used in this study.$^{157}$ Figure 8-4 presents spectra measured for quiescent bias -1.5 V corresponding to partial depletion of the 2DEG region. The space charge region boundary in stationary conditions is near the AlGaN / GaN interface while the 1 V filling pulse can also fill the traps in the barrier.$^{155}$ The interface trap spectra in the AlGaN / GaN / Si HEMTs varied from sample to sample. In the case of the HEMT structure in Figure 8-4, the interface spectrum before irradiation showed only a prominent peak near 0.8 eV. After irradiation with $1.3 \times 10^{16}$ cm$^{-2}$ 10 MeV electrons we observed an increased concentration of 0.17 eV, 0.3 eV, 0.45 eV, 0.55 eV, and 0.8 eV interfacial traps.

Admittance spectra for the AlGaN / GaN / Si HJ before and after irradiation with $1.3 \times 10^{16}$ cm$^{-2}$ electrons are compared in Figure 8-5. The data are shown for only one frequency of 2 kHz and an applied bias of -1.5 V below the threshold voltage, so that only the traps near the interface or in the barrier could be detected. A strong increase in the magnitude of the signals from traps with activation energy 0.3 eV and 0.55 eV occurs after irradiation, in agreement with DLTS results for transistors. Similar results were observed for admittance spectra measured on transistors. Thus, both DLTS and admittance spectra measurements indicate that electron
irradiation increases the concentration of interface/barrier traps with activation energy 0.3 eV and 0.55 eV, with the density of “interfacial” traps with activation energy 0.17 eV, 0.45 eV, and 0.8 eV also increased. Among these traps the 0.8 eV centers seem to be the ones related the threshold voltage shift after irradiation since only they are observed in high density before irradiation. Among these barrier / interface traps the traps with activation energy 0.55 eV have been detected previously in AlGaN / GaN HEMTs and their concentration observed to increase after high voltage stress experiments. The gate lag measurements before and after irradiation with $1.3 \times 10^{16}$ cm$^{-2}$ 10 MeV electrons fluence are presented in Figure 8-6. After irradiation the pulsed signal compared to DC signal decreased by about 2 times pointing to a much more prominent contribution of deep traps. From DLTS and admittance spectra results it seems reasonable to associate this decrease with the increased density of barrier/interface traps with activation energy 0.3 eV, 0.45 eV, 0.55 eV, and 0.8 eV introduced by irradiation.

For other types of HJs, the shift of C-V characteristics increasing with electron fluence was observed and is compatible with increased concentration of deep traps in the barrier/interface. At that, the AlGaN / GaN / sapphire and AlGaN / AlN / GaN / sapphire HJs show an introduction rate of deep acceptors similar to the one observed for AlGaN / GaN / Si HJs, whereas, for InAlN / GaN HJs, the introduction rate was about 5 times higher.
Table 8-1. Initial characteristics of 2DEG in studied HJs before irradiation: 2DEG concentration $N$ (2DEG) (cm$^{-2}$) and 2DEG mobility $\mu$ (2DEG) (cm$^2$/Vs), also shown are threshold voltages $V_{TH}$ (V) as deduced from room temperature C-V characteristics

<table>
<thead>
<tr>
<th>HJ type</th>
<th>N(2DEG) (cm$^{-2}$)</th>
<th>$\mu$(2DEG), (cm$^2$/Vs)</th>
<th>$V_{TH}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlGaN / AlN / GaN / sapphire</td>
<td>$1.2 \times 10^{13}$</td>
<td>1490</td>
<td>-4</td>
</tr>
<tr>
<td>AlGaN / GaN / sapphire</td>
<td>$9 \times 10^{12}$</td>
<td>1250</td>
<td>-3</td>
</tr>
<tr>
<td>AlGaN / GaN / Si</td>
<td>$1.1 \times 10^{13}$</td>
<td>1150</td>
<td>-2</td>
</tr>
<tr>
<td>InAlN / GaN / sapphire</td>
<td>$1.9 \times 10^{13}$</td>
<td>1210</td>
<td>-3.5</td>
</tr>
</tbody>
</table>
Figure 8-1. Mobility as a function of electron fluence for type 1 AlGaN / AlN / GaN / sapphire, type 2 AlGaN / GaN / sapphire, type 3 AlGaN / GaN / Si, and type 4 InAlN / GaN / sapphire HJ.
Figure 8-2. C-V characteristics measured on the AlGaN / GaN / Si HJ before irradiation (square line) and after electron irradiation with the fluence of $1.3 \times 10^{16}$ cm$^{-2}$ (circle line).
Figure 8-3. 85K C-V characteristics measured on the AlGaN / GaN / Si HJ A) before irradiation and B) after irradiation.
Figure 8-4. DLTS spectra measured on the AlGaN / GaN / Si HEMT before irradiation (dashed curve) and after irradiation with $1.3 \times 10^{16} \text{ cm}^{-2}$ 10 MeV electrons (solid curve).
Figure 8-5. The temperature dependence of capacitance and AC conductance (G). Black curves refer to pre-irradiation, red curves refer to after irradiation.
Figure 8-6. A) Gate lag measured on the AlGaN / GaN / Si HEMT before irradiation B) gate lag measured on the AlGaN / GaN / Si HEMT after irradiation.
8.4 Summary

The main effect of electron irradiation of AlGaN / AlN / GaN, AlGaN / GaN, and InAlN / GaN heterojunctions grown by MOCVD on sapphire and of AlGaN / GaN HJs grown by MOCVD on Si (111) is the decrease of 2DEG mobility of heterojunctions with consequent increase of the sheet resistivity, while the 2DEG concentration was effected only slightly. The decrease in threshold voltage of AlGaN / GaN / Si HJs and HEMTs can be explained by an increase of the density of deep acceptor traps. DLTS and admittance measurements on AlGaN / GaN / Si HEMTs and admittance spectra measurements on AlGaN / GaN / Si HJs show that the traps involved have activation energies of 0.3 eV, 0.45 eV, 0.55 eV, and 0.8 eV. The radiation tolerance of AlGaN / GaN on Si HEMTs is similar to that of more established AlGaN / GaN and AlGaN / AlN / GaN structures on sapphire, while the radiation tolerance of InAlN / GaN structures are considerably lower.
CHAPTER 9
A NOVEL APPROACH TO IMPROVE HEAT DISSIPATION OF ALGAN/GAN HEMTS
WITH A CU FILLED VIA UNDER DEVICE ACTIVE AREA

9.1 Introduction to Thermal Performance of HEMTs

AlGaN / GaN high electron mobility transistors (HEMTs) have received increasing
attention for high power and high frequency applications such as military radar and satellite-
based communications systems,\textsuperscript{1,22} due to their superior mobility (~1400 cm\textsuperscript{2} / V-s) and larger
energy band gap as compared to Si-based power transistors. Due to the lack of readily available,
large-area GaN bulk materials, GaN epi-layers are usually grown on sapphire, Si or SiC
substrates. Among these substrates used for GaN epi-layers, sapphire is the most common one
and is mainly used for GaN-based light emitting diode growth. However, the thermal
conductivity of GaN is very poor, impacting the electronic device performance and reliability
especially for high power applications.\textsuperscript{120,121} SiC substrates are an excellent choice for epitaxial
growth owing to their high thermal conductivity and smaller lattice mismatch to GaN, but they
are very expensive.\textsuperscript{4} Si is another common substrate because of the low cost, availability of
larger area wafers, relatively high thermal conductivity and mature Si-based processing
techniques. Recently, HEMT structures grown on 8-inch Si substrates have been demonstrated
and makes Si substrates a prime candidate for commercialized GaN mass production
applications.\textsuperscript{4,123} However, the large lattice mismatch between Si and GaN makes the nucleation
interface layer become defective and requires a thicker transition to grow good quality GaN epi-
layers. Therefore it is important to study the thermal response of HEMT/Si structures operated at
high power density and to determine how effectively they dissipate the heat within the HEMT to
enhance both device performance and improve the reliability.
Although Si has a relatively high thermal conductivity as compared to sapphire, it is known that the nucleation interfacial defective layer between GaN and Si creates another non-negligible heat resistance. This thermally resistive nucleation layer contains high densities of dislocations and impurities, which degrade device performance due to the self-heating effect induced by this defective interfacial layer.\textsuperscript{12} Micro-Raman spectroscopy was used to measure the thermal resistance of these defective nucleation layers and showed values ranging from 33 to 70 m\textsuperscript{2}-K / GW,\textsuperscript{12,17} which is 3.3 to 9 times the thermal resistance contributed by 2 µm of GaN epilayer. In order to improve the heat dissipation, this highly thermally resistive nucleation layer needs to be removed. Through-wafer, source-ground via holes are widely used for monolithic microwave integrated circuits to provide low inductance grounding, increase packing density and offer an additional heat sink. Russo \textit{et al.} simulated the thermal behavior of AlGaN / GaN HEMTs grown on SiC with different transition layer thicknesses, both with and without Au-filled, source-grounded via holes.\textsuperscript{125} The thermal resistance of the HEMT with Au-filled via holes decreased by 3.7 to 6.3\% depending on the thickness of the defective nucleation layer as compared to the HEMT without the source-grounded via hole.\textsuperscript{124}

In this work, a novel device configuration is proposed, which employs an additional through Si substrate via hole directly under the device active. The highest temperature region of the HEMT is located at the device active area directly under the gate fingers. By forming such via holes, the thermally-resistive nucleation layer under the gate area is exposed and can be removed by etching. After removing this thermally resistive AlN nucleation layer, the via hole can be back-filled with plated copper to enhance the heat dissipation. Three-dimensional finite element simulations were performed to examine the effect of this additional through Si substrate via hole directly under the device active area on the junction temperature of AlGaN / GaN
HEMTs fabricated on Si substrates. The effects of HEMT power density, nucleation layer, the width of the via-hole and thickness of copper on the maximum junction temperature were also investigated.

9.2 Simulation Approach

Figure 9-1 A and B shows the 3-D mesh of the simulated AlGaN / GaN HEMT and 3-D frame structure with through-wafer via hole to the source contact pad and through Si substrate via hole under the active area of the HEMT, respectively. Simulation results were generated with $4 \times 10^6$ tetrahedra and $8 \times 10^6$ grid points, and the mesh density was adjusted depending on the magnitude of temperature gradient. The HEMT structure used in the modeling consists a 25 nm AlGaN barrier layer, a 0.8 $\mu$m GaN buffer layer, a 1.4 $\mu$m AlGaN transition layer and 28 nm AlN nucleation layer on 100 $\mu$m thickness Si substrate. The dimensions of the Ohmic contacts were 30 $\mu$m $\times$ 100 $\mu$m, and the source to drain distance was 4 $\mu$m. The gate length and width were 0.45 and 100 $\mu$m, respectively. A square through wafer via hole of 50 $\mu$m $\times$ 50 $\mu$m was placed under the source contact pad. A rectangular through Si substrate via hole of 6 $\mu$m (1 $\mu$m of Ohmic contact transfer length on each side of source and drain contact plus the space between source and drain contacts of 4 $\mu$m) $\times$ 110 $\mu$m was configured beneath the HEMT active area. Both via holes were filled with copper. The thermal resistances for each layer used in the HEMT structure are listed in Table 9-1.

The model used for the thermal simulation is based on the steady state energy balance of the 3-D unit chip using rectangular coordinates (x-, y- and z-axes).

$$k \left( \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right) = P_D$$
where $k$ is the thermal conductivity in units $\text{W} / \text{m-K}$, $T$ is the temperature and $P_0$ is the heat source density in $\text{W} / \text{m}^3$. A boundary condition was set with a temperature of 300K at the bottom of the Si substrate.
Figure 9-1. A) 3-D mesh structure of the AlGaN / GaN HEMT used in the simulation. B) 3-D frame structure with a via under source contact and via under the active area.
Table 9-1. Material thermal conductivity.

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal conductivity (W / m-K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu</td>
<td>401</td>
</tr>
<tr>
<td>Si</td>
<td>149</td>
</tr>
<tr>
<td>AlN defective layer</td>
<td>0.538</td>
</tr>
<tr>
<td>AlGaN</td>
<td>25 @ 300K</td>
</tr>
<tr>
<td>GaN</td>
<td>130 @ 300K</td>
</tr>
<tr>
<td>Ohmic metal</td>
<td>200</td>
</tr>
<tr>
<td>Metal contact</td>
<td>381</td>
</tr>
<tr>
<td>Gate metal</td>
<td>381</td>
</tr>
<tr>
<td>SiN</td>
<td>30</td>
</tr>
</tbody>
</table>
9.3 Results and Discussion

Figure 9-2 A illustrates the cross-sectional temperature contours for the reference HEMT with a conventional through-wafer source-contact via hole. Figure 9-2 B shows the HEMT with an additional via hole, in which the Si substrate is etch off, formed directly under the active area filled with copper simulated at a power density of 5 W/mm. For the reference HEMT, the simulated maximum junction temperature was 146°C, while the maximum junction temperature of the HEMT with additional Cu-filled Si-substrate via hole under the device active area was 120°C. The reduction of the maximum junction temperature for the HEMT with additional Cu-filled Si-substrate via hole under the device active area was achieved by removing the highly defective and thermally resistive nucleation layer under the device active area, as well as filling the through Si-substrate via hole with thermally conductive copper. To evaluate the effectiveness of thermal dissipation, absolute thermal resistance, $R$, is typically used, which is defined as

$$ R = \frac{\Delta T}{W} $$

where $\Delta T$ is $T_J - T_S$, $T_J$ is the maximum junction temperature, $T_S$ is the temperature of the heat sink and $W$ is the total power dissipated by the device in Watts. To study the effects of the defective nucleation layer and copper filled through Si-substrate via hole on the absolute thermal resistance and maximum junction temperature, the temperature distributions of the devices with and without the removal of defective AlN nucleation layer as well as the devices with through Si-substrate via hole filled with Cu were simulated. The maximum junction temperature and absolute thermal resistance for different conditions is presented in Table 9-2 and the nucleation layer exhibited the lowest thermal conductivity among all the layers. In other words, the total thermal resistance could be reduced 18% if the nucleation layer was etched off. On the other sides, the difference of the absolute thermal resistance between the device with and without the
copper filled through-Si substrate via hole under the active area of the device was around 10 K/W. Thus the combination of the removal of the nucleation layer and the implementation of the copper filled via hole provided a reduction of 18% of the total thermal resistance of the device.

Figure 9-3 shows vertical temperature distributions in the region of epitaxial layers directly under the gate finger for the reference HEMT with a through-wafer source-contact via hole and the HEMT with both a through-wafer source-contact via hole and an additional through Si-substrate via hole under the active area filled with copper. The dimensions of the top AlGaN layer and 2DEG channel are too thin and the temperature changes across these regions are also too small to be observed in Figure 9-3. For the reference sample, the temperature drops across the GaN buffer layer, AlGaN transition layer and AlN nucleation layer were 9, 64 and 6°C, respectively. The thermal conductivity of the ~800 nm GaN buffer layer is 130 W/K-m, which is around 6 times larger than the thermal conductivity of the 1.4 μm AlGaN transition layer, 25 W/K-m. Thus, the temperature drop in the AlGaN transition layer is around 6 times larger than the one simulated in the GaN buffer layer. Although the thickness of the very defective AlN nucleation is only 28 nm, there is an obvious 6°C temperature drop due to its very high thermal resistivity, as shown in Figure 9-3. In the case where the defective AlN nucleation layer under the active layer of the HEMT with the through Si via hole was removed and the via hole was filled up with plated copper, not only was the junction temperature much lower than the reference HEMT, but also the temperature at the bottom of the AlGaN transition layer was around 10°C lower than that of the reference HEMT. This indicates the effectiveness of heat removal from the copper filled via hole.

Figure 9-4 shows 2 dimensional temperature contours on the plane of two dimensional electron gas (2DEG) channel for the reference HEMT with a through-wafer source-contact via
hole and the HEMT with both a through-wafer source-contact via hole and an additional Si-substrate via hole under the active area filled with copper, respectively, simulated at a power density of 5 W/mm. The gradient of the temperature distribution was much larger, and the temperature dropped to less than 35°C for the region 30 µm away from the gate area. Since the through-wafer source-contact via hole was placed 50 µm away from the gate finger, it could not effectively assist in the heat dissipation. By contrast, when the through-Si via hole was placed directly under the active area with a distance of 2.2 µm between the gate finger and via hole, the heat generated in the 2DEG channel could be effectively dissipated from under the active area.

As shown in Figure 9-5, the maximum junction temperature is directly proportional to the power consumption of the HEMT. For the reference HEMT, the maximum junction temperature increased around 28°C per watt of power consumption. On the other hand, the maximum junction temperature only increased 23°C per watt of power consumption for the HEMTs with a 6 µm × 100 µm through Si via hole filled with plated copper under the active area. The effect of the plated copper thickness inside the via hole on the maximum junction temperature was also investigated, as illustrated in Figure 9-5. The heat transfer mechanism inside the via hole without filling any metal is dominated by free convection, which is a couple of orders less efficient than that of heat conduction. As a result, the via holes have to be filled with plated metal to achieve better step coverage. However, as shown in Figure 9-5, with 1 µm thick copper around the via hole, the maximum junction temperature changing rate can be reduced to 25°C per watt of heat dissipation. When the copper thickness increased to 2 µm, the maximum junction temperature increase rate was 23.8°C per watt of power consumption, which is very close to the rate of 23°C per watt of heat consumption for the via hole completely filled with plated copper.
The effect of the dimensions of the through Si substrate via holes on the maximum junction temperature was also studied. The simulation results presented so far for the HEMT with a through Si substrate via hole were based on the via hole covering the regions of 4 µm between source and drain contacts as well as 1 µm of the transfer length on each side the Ohmic metal electrode. The majority of the heat generation of the HEMT is in these two regions. Thus the maximum junction temperature increases dramatically when the opening of the through Si substrate via hole is symmetrically decreased around the gate finger, as shown in the area designated in Figure 9-6 as region I. The maximum junction temperature increases from 120°C for the HEMT with a 6 µm wide through Si substrate via hole to 146°C for the HEMT without the through Si substrate via hole. Region II of Figure 9-6 shows the impact of expanding the width of the through Si substrate via hole under the source Ohmic metal contact on the maximum junction temperature. The maximum junction temperature continuously decreases as the width of the via hole increases due to larger areas of thermal resistive layer being removed and replaced with a less resistive copper layer. Since this through Si substrate via hole is electrically connected to the conventional source via hole, this via hole can be treated as a backside source field plate. Thus this via hole can not only reduce the maximum junction temperature but also reduce the maximum electric field around the gate edges to increase the drain breakdown voltage. The gate-source capacitance for HEMTs with the through Si substrate via hole in the region II of Figure 9-6 should be the same as the HEMT with 6µm wide through Si substrate via hole. The maximum junction temperature can be further reduced by extending the width of the through Si substrate via hole to under the drain Ohmic contact, as shown in region III of Figure 9-6, but the gate-source and source-drain feed-back capacitance will significantly increase and degrade the RF performance of the HEMTs.
Figure 9-2. A) Cross-sectional temperature contours of the reference HEMT. B) Cross-sectional temperature contours of the proposed HEMT structure.
Table 9-2. Absolute thermal resistance of HEMT with different configurations.

<table>
<thead>
<tr>
<th>Type of HEMT</th>
<th>Reference HEMT</th>
<th>HEMT I</th>
<th>Proposed HEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source via</td>
<td>Cu filled</td>
<td>Cu filled</td>
<td>Cu filled</td>
</tr>
<tr>
<td>Si via</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Removal of AlN defective layer</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Maximum junction temperature at 5 W / mm (°C)</td>
<td>152</td>
<td>146</td>
<td>120</td>
</tr>
<tr>
<td>Absolute heat resistance [K / W]</td>
<td>304</td>
<td>292</td>
<td>240</td>
</tr>
<tr>
<td>Percentage change compared to reference HEMT (%)</td>
<td>---</td>
<td>-3.45</td>
<td>-17.24</td>
</tr>
</tbody>
</table>
Figure 9-3. Vertical temperature distributions directly under the gate finger for the reference HEMT and the proposed HEMT structure with copper filled via.
Figure 9-4. A) 2-dimensional temperature contours at 2DEG plane of the reference HEMT. B) 2-dimensional temperature contours at 2DEG plane of the proposed HEMT.
Figure 9-5. Maximum junction temperature as a function of power density for the reference, the proposed HEMT, and the proposed HEMT with 1 µm or 2 µm filled copper.
Figure 9-6. Effect of the through Si substrate via hole location on the maximal junction temperature.
9.4 Summary

In summary, a new approach of implementing an additional through Si-substrate via-hole under the active area of HEMT is proposed to reduce the maximal junction temperature. For AlGaN / GaN structures grown on Si substrates, the AlN nucleation layer on the Si substrate is a very defective and thermally resistive layer, which causes inefficient heat dissipation. The proposed through Si-substrate via hole provides access to this AlN nucleation layer. Based on the simulation result, the maximum junction temperature can be significantly decreased by removing this thermally resistive layer and plating Cu or Au to fill the via holes. At a 5 W / mm condition, the maximum junction temperature of the reference HEMT was 146°C, while the maximum junction temperature decreased to 120°C for the HEMT with an additional through Si-substrate via-hole under the active area of HEMT. Besides reducing the maximal junction temperature, since this through Si-substrate via-hole is electrically connected to the conventional source via hole, it acts as a backside source field plate. This via hole can also reduce the maximum electric field around the gate edges and increase the drain breakdown voltage. If this through Si-substrate via-hole is separately connected to the front gate pad, it can behave as a back gate to improve front gate modulation.
CHAPTER 10
A NOVEL STRUCTURE TO IMPROVE BREAKDOWN VOLTAGE BY BACKSIDE GATE ON ALGAN/GAN HEMTS

10.1 Introduction to Multiple Gate Device and Field Plate

AlGaN / GaN high electron mobility transistor (HEMT) performance has gained more attention in recent years because of the high breakdown voltage.\textsuperscript{159,160} Based on the material property, the breakdown field of GaN could go up to 1.01 MV / cm.\textsuperscript{107} However, breakdown voltage was around 1300 V at \( L_{GD} = 20 \) µm.\textsuperscript{10} Not only the breakdown voltage is lower than theoretical value, but also subthreshold swing (SS) is higher than theoretical value (~60 mV / dec).\textsuperscript{79} The intrinsic defects serve as a tunneling center and increase the leakage current at off-state. As a result, the breakdown voltage decreased and SS increased because of the increased leakage current. Thus, it is important to find a way to suppress the leakage current and thus improve the breakdown voltage and subthreshold swing.

To suppress gate leakage current, one way is to implement additional gates on the transistors. There are several forms of multigate devices. One example is double-gate SOI MOSFETS, which could be used to suppress short-channel effect.\textsuperscript{161,162} The other example is FinFET, which is also known as tri-gate transistor, utilizes three gates to suppress the gate leakage.\textsuperscript{163} The body is wrapped around by the gate, which provides a better electrical control over the channel to reduce gate leakage current and prevent short channel effect. There are even transistors which have four gates such as gate-all-around (GAA) FET\textsuperscript{164} and \( G^4 \)-FET.\textsuperscript{165} The additional gate could provide robustness to the device; either induced more current or suppressed leakage current depends on the operation mode. So far, this four gate technology has not been implemented in HEMT technology yet.
The source or gate field plate (FP) can be used to redistribute the electric field to decrease peak electric field around the gate edges and reduce hot electrons. Thus, drain breakdown voltage was enhanced and drain current collapse was lessened.\textsuperscript{21,24,108,166-170} Zhang \textit{et al.} extended the gate on top of SiN and get breakdown voltage of 570 V at $L_{GD} = 13 \ \mu m$.\textsuperscript{171} Hikita \textit{et al.} opened a via through the epitaxy layer to Si on the front side of the device to connect the front side source to back side grounding electrode and achieve low on-state resistance (1.9 m\ohm\cdot\text{cm}^2) and breakdown voltage as 350 V.\textsuperscript{172} Lu \textit{et al.} also demonstrated the effect of source field plate which improve the breakdown voltage from 55 V to 155 V.\textsuperscript{24}

\textbf{10.2 Experimental}

\textbf{10.2.1 HEMTs Fabrication}

HEMT structures were grown on Si substrates using a metal organic chemical vapor deposition (MOCVD) system, starting with a thin AlN nucleation layer followed with a 1.4 \ \mu m AlGaN graded transition layer, a 0.8 \ \mu m low-defect carbon-doped GaN buffer layer, 50 nm undoped GaN layer and a 16 nm undoped AlGaN barrier layer with 26% Al mole fraction.

\textbf{10.2.2 Front Side Device Fabrication}

Front side device fabrication started with Ohmic contact formation. Ti / Al / Ni / Au Ohmic metallization was deposited using electron beam evaporator and the metal contacts were subsequently annealed in a rapid thermal annealing system at 825ºC. Inter-device isolation was accomplished by the use of multiple energy N+ implantations to create damages throughout the top 400 nm of the HEMT structure. After implantation, the devices were passivated with 70-nm-thick SiNx in a plasma enhanced chemical vapor deposition (PECVD) system. Schottky gate definition was achieved by patterning the gate and contact windows to the Ohmic contact pads were also opened at the same time. After SiNx etching, wider patterns for Schottky gates and contact windows to the Ohmic contacts were re-patterned with another photolithography step. Ni
Au-based gate metallization was deposited on the gate and Ohmic contact pads simultaneously. The devices were then passivated with another 400-nm layer of PECVD SiNx. The contact windows to Ohmic contact and gate pads were opened by dry etching. There was an additional metal deposition for source field plate. The field plate was connected to the source terminal and extended by 1 µm over the gate electrode to the gate-to-drain region. The source to gate distance and channel length of the HEMTs was kept constant at 1 and 4.7 µm, respectively.

10.2.3 Backside Device Fabrication

After finishing the front side device fabrication, wafers were mounted on another Si substrate for back processing. Prior to drilling via holes, the wafers were polished and thinned to 150 µm. Photoresist AZ9260 were used to pattern via holes on the backside of the wafer aligning to alignment marks fabricated on the front side of the wafer with a backside aligner. High aspect-ratio via holes were fabricated by employing BOSCH process to etch through the Si substrate. The dimensions of via holes are 25 µm × 60 µm × 150 µm. BCl₃/Cl₂/Ar based plasma was subsequently employed to etch off AlN nucleation and 1.4 µm graded AlGaN transient layers in an inductively coupled plasma system. After via hole etching, Ti/Au was sputtered to cover the entire backside of the wafer to form back-side contacts. A schematic of the HEMT with both front and back gate contact is illustrated in Figure 10-1.

10.3 Results and Discussion

Figure 10-2 A and B show drain IV characteristics of AlGaN/GaN HEMTs by either biasing front gate or back gate. Front gate modulated the two dimensional gas (2DEG) channel well exhibiting a saturation current and a pinch-off gate voltage of 574 mA/mm and -1.5 V, respectively. The back gate was formed on the bottom of carbon-doped GaN buffer layer, which is 0.8 µm away from the 2DEG channel, thus the modulation of 2DEG channel was not effectively. The back-gate modulated around 120 mA of the drain current by applying gate
voltages ranging from 0 to -25 V, but could not able to pinch-off the 2DEG channel. However, these problems can be overcome by etching a part of the GaN buffer layer and placing back gate closer to the 2DEG channel.

Figure 10-3 A and B show the drain IV and transfer characteristics of AlGaN / GaN HEMTs by biasing both front and back gate together as compared to the ones with the front gate only. Since the back gate was not effective as the front gate for modulating 2DEG channel, the applied voltages for the back-gate was set 10 times of voltages applied to the front gate. As shown in Figure 10-3, the drain saturation current increased from 512 mA / mm to 547 mA / mm. The increase might be due to the better 2DEG confinement by the additional backside gate. Besides, because of the additional gate, the Gm peak increased from 267 mS / mm to 322 mS / mm. In other words, the HEMTs biased with both gate biasing exhibited a higher peak extrinsic transconductance resulted from a better 2DEG channel modulation by depleting the 2DEG channel on both sides at the same time.

To examine the modulation of back-side gate, the drain current was measured by changing the back-side gate voltage while kept $V_G$ constant. Figure 10-4 A shows the transfer characteristics of device with and without applying $V_{BG}$. As shown in Figure 10-4 A, gate leakage current decreased from $3.9 \times 10^5$ to $1.2 \times 10^6$ mA / mm, subthreshold swing improved from 204 to 137 mV / dec while $I_{DS}$ slightly decreased after applying $V_{BG}$ at -10 V. In other words, on / off ratio increased after applying $V_{BG}$ due to reduction of $I_G$. Also, from Figure 10-4 A, the subthreshold swing (SS) became steeper after applying $V_{BG}$, which meant SS improved. Besides, the threshold voltage ($V_{TH}$) shift positively with increasing backside voltage. Table 10-1 shows the $V_{TH}$ change with different backside voltage. The $V_{TH}$ could shift positively from -1.38 V to -1.09 V. In other words, $V_{TH}$ could also be adjusted based by applying $V_{BG}$. Figure
10-4 B illustrates the increase of on/off ratio and improvement of subthreshold swing with $V_{BG}$. On/off ratio improved about one order after applying $V_{BG}$ as -40 V and subthreshold swing improved from 204 mV / dec to 137 mV / dec. The on/off ratio was improved by the reduction of $I_G$. In our study, double gate was implemented in D-mode device. However, it could also be used in E-mode device. By implementing other gates, it would give better control of the device, i.e. better depletion or inversion. Akarvardar et al. utilized four gates in the silicon-on-insulator device. It was reported that subthreshold swing, mobility, transconductance, high transconductance to current ratio and early voltage were improved with the specific gate bias.

To further examine the effect of backside voltage, front-side gate I-V was also monitored with backside gate voltage at different voltages. From Figure 10-5 A, it shows the gate leakage current can be suppressed from $3.8 \times 10^{-4}$ mA / mm to $2.3 \times 10^{-4}$ mA / mm by applying the additional backside gate voltage at -25 V. When the back-side gate was biased at negative voltage, it provided another depletion at the backside of the device. This depletion region makes the buffer layer more resistive, leading to a smaller leakage current. Because of the suppressed leakage current, the breakdown voltage is expected to improve. As shown in Figure 10-5 B, the breakdown voltage was improved dramatically after first applying $V_{BG}$ at -5 V but reached saturation at $V_{BG} = -25$ V. The depletion depth might touch the channel at $V_{BG} = -25$ V already so it no longer provided noticeable improvement. In summary, the breakdown voltage can be improved by 40% with $V_{BG} = -25$ V because of the suppression of leakage current.

10.4 Summary

In summary, using the back-side gate technology, the device DC performance and breakdown voltage can be improved. The drain saturation current can be improved from 512 to 537 mA / mm. The on/off ratio can improve by one order and the subthreshold swing can be improved from 204 to 137 mV / dec. Most important of all, because of the suppression of
leakage current, the breakdown voltage can be improved by 40% when the backside voltage was biased at -25 V. This technique could not only implement to D-mode device but E-mode device, making the device more robust and perform better in analog application.
Figure 10-1. Schematic view of the proposed structure with a backside via.
Figure 10-2. Drain I-V modulated by A) front-side gate or B) backside gate.
Figure 10-3. A) Drain I-V modulated by both front-side and backside gate. B) Transfer characteristics modulated by both front-side and backside gate.
Figure 10-4. A) Transfer characteristics of ref sample and sample with backside voltage at -10 V. B) On/off ratio and subthreshold swing change versus different backside gate voltage.
Table 10-1. Threshold voltage change with backside gate voltage

<table>
<thead>
<tr>
<th>BG (V)</th>
<th>0</th>
<th>-5</th>
<th>-10</th>
<th>-20</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TH}$ (V)</td>
<td>-1.38</td>
<td>-1.27</td>
<td>-1.23</td>
<td>-1.09</td>
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<tr>
<td>$V_{TH}$ change (%)</td>
<td>7.97</td>
<td>10.87</td>
<td>21.01</td>
<td></td>
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Figure 10-5. A) Gate I-V with backside gate biased at different voltages. B) Breakdown voltage change at different backside gate voltages.
CHAPTER 11
CONCLUSIONS

AlN used as gate insulator and passivation for the high electron mobility transistors deposited by plasma-enhanced atomic layer deposition was characterized by X-ray photoelectron microscopy (XPS) and Auger electron spectroscopy. The refractive index of deposited AlN was 1.9, which was lower than the crystalline AlN due to the top 2 nm AlN oxidized during the device fabrication. DC performance of AlN based MISHEMT was also reported. The modulation of gate voltage could be increased to 4 V from 2 V for the same epitaxy structure with Schottky gate. The drain saturation current ($I_{DS}$) was 600 mA / mm and the transconductance was 127 mS / mm. Because of the introduction of AlN, the gate leakage current could be suppressed to $1.13 \times 10^{-9}$ (A / mm). Due to the reduction of gate leakage current, the drain current on/off ratio was increased to $3.3 \times 10^{8}$. In addition, the drain current dispersion at 100 kHz was only 7%, showing the effective passivation of this AlN passivation layer. The enhancement of the drain breakdown voltage of AlN MISHEMTs was also investigated. The drain breakdown voltages of 500 and 2000 V were achieved for MISHEMT with a drain-source distance of 10 $\mu$m and 40 $\mu$m, respectively.

The mechanism of Ti-Al-Ni-Au based Ohmic contacts degradation upon exposure of buffer oxide etchant (BOE) solution was studied. The main effect of BOE on Ohmic contacts degradation was the increase of metal sheet resistance from 2.7 to 3.7 $\Omega$ / after 180 sec of BOE exposure. Scanning electron microscopy (SEM), energy dispersive X-ray spectrum (EDX) and Auger electron microscopy were used to characterize the change before and after BOE treatment. Ohmic contacts were composed of 3 to 5 $\mu$m-wide Ni-Al based islands surrounded by 1 $\mu$m-wide Au-Al based ring. After BOE treatment, the height of islands reduced from 300 nm to 200-250 nm and the Au based ring became narrower. The contents of Ni, Al and Au decreased
after BOE treatment confirmed with EDX and Auger electron microscopy. The reductions of Ni and Al were due to the etching reaction between BOE to metals. The reduction of Au might be resulted from Au removal by etching off Al underneath Au layer.

The mechanism of breakdown voltage improvement of AlGaN / GaN HEMTs after proton irradiation was investigated. The devices were irradiated at 275 keV or 330 keV from the back-side of the device. The defects generated after proton irradiation at 275 keV or 330 keV were in GaN buffer layer or AlGaN barrier layer of the HEMT structure, respectively. By putting $2 \times 10^{18}$ numbers / cm$^3$ vacancies in the AlGaN barrier layer, the drain saturation current decreased from 300 mA / mm to 250 mA / mm. However, the drain breakdown voltage increased from 55 V to 150 V. Simulation was perform to identify the degradation mechanism; electric field at the gate edge near the drain electrode decreased around 50% by placing defects in the AlGaN barrier layer, which would account for the increase of drain breakdown voltage.

The effect of low-dose gamma irradiation on DC performance of AlGaN / GaN HEMTs was examined. After gamma irradiation, the $I_{DS}$ increased and the resistance between drain and source contacts decreased. The increase of $I_{DS}$ was in positive correlation with doses and reached 11% at dose of 700 Gy. The resistance decrease between drain and source contacts after 700 Gy was around 14%. The increase of the $I_{DS}$ and reduction of source-drain resistance were mainly due to the increase of the 2DEG electron mobility. The gate I-V characteristics didn’t change much after irradiation.

The effect of electron irradiation on device performance of AlGaN / AlN / GaN, AlGaN / GaN, and InAlN / GaN HJs were studied. After electron irradiation on AlGaN / GaN / Si HJs, the threshold voltage shifted positively because of the increase of the density of deep acceptor traps. Besides, the surface states increased linearly with dose of electron irradiation, with an
introduction rate of about $5 \times 10^{5}$. Deep level transient spectrum (DLTS) and admittance measurements on AlGaN / GaN / Si HEMTs and admittance spectra measurements on AlGaN / GaN / Si HJs revealed the trap activation energies of 0.3 eV, 0.45 eV, 0.55 eV, and 0.8 eV. The drain current dispersion in gate pulsed measurement increased after electron irradiation, which was in agreement with the DLTS and admittance spectrum.

Thermal performance of the HEMT structure with an additional Cu via underneath the active area was investigated. The maximum junction temperature could be reduced for 26°C from 146 to 120°C at a power density of 5 W / mm. The absolute thermal resistance of the device decreased from 292 K / W to 240 K / W due to the removal of thermal resistive nucleation layer and the introduction of Cu via.

The effect of backside via structure to DC performance and off-state drain breakdown voltage was studied. The drain saturation current can be improved from 512 to 547 mA / mm when $V_{BG}$ and $V_G$ was biased simultaneously. At this condition, the transconductance can be improved from 267 mS / mm to 322 mS / mm. Besides, the subthreshold swing can be improved from 204 to 137 mV / dec when the backside voltage was biased at -10 V. Because of the suppression of leakage current, the on / off ratio can be improved from $3.9 \times 10^5$ to $1.2 \times 10^6$. Last, because of the suppression of leakage current, the breakdown voltage can be improved by 40% when the backside voltage was biased at -25 V.
LIST OF REFERENCES


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