AN INSTRUMENTATION-GRADE DIFFERENTIAL CAPACITIVE MEMS SHEAR STRESS SENSOR SYSTEM FOR WIND TUNNEL APPLICATIONS

By

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To my mother
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AN INSTRUMENTATION-GRADE DIFFERENTIAL CAPACITIVE MEMS SHEAR STRESS SENSOR SYSTEM FOR WIND TUNNEL APPLICATIONS

By

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December 2012

Committee Chair: Mark Sheplak
Major: Electrical and Computer Engineering

This dissertation describes the development of a differential capacitive microelectromechanical systems (MEMS) shear stress sensor, the associated packaging, and the interface electronics required for operation as an instrumentation-grade sensing system. The sensor is a floating element possessing a differential comb drive designed to meet the spatial and temporal requirements for use as a measurement tool for turbulent boundary layers. The capacitive sensing interface circuitry is an analog synchronous modulation/demodulation system that enables the system to make time-resolved measurements of both mean and dynamic wall shear stress events. The packaging of the sensor creates a hydraulically smooth surface for moderate Reynolds numbers with a small footprint to enable array design and non-intrusive installation. The calibration of the sensor is extended to include a new method in estimating the frequency response function of shear stress sensors and a new test bed to quantify the impact of varying humidity and temperature in the ambient environment.

The sensor system is demonstrated in three wind tunnel facilities against a variety of comparative measurement techniques and in many flow conditions. The final system
exhibits a sensitivity of 6.5 mV/Pa, a bandwidth of 4.7 kHz, and is the first MEMS-based shear stress system to successfully demonstrate both mean and dynamic measurements in multiple wind tunnel facilities.
Quantification of skin friction drag is an area of research with immediate impact on consumer markets as well as emerging technologies. In consumer applications the quantification and study of skin friction drag can assist in the design of more fuel-efficient automobiles and airplanes. In a multi-billion dollar industry [1], reduction in fuel consumption would have enormous economic impact. In scientific research, the field of flow control would benefit greatly from the ability to make a time-resolved, directional measurement of wall shear stress in order to detect and perhaps predict separation. As a feedback mechanism, the sensor would enhance the ability of a controller to suppress and prevent separation [2]. Beyond separation, the ability to make direct time-resolved measurements of mean and dynamic wall shear stress will help elucidate complex flow fields, where traditional fluid measurement techniques used to estimate wall shear stress fail.

The goal of this dissertation is to create an instrumentation-grade sensor system for the quantification of shear forces at the fluid-solid boundary. This includes design and fabrication of a shear stress sensor, design and implementation of interface circuitry, packaging of the sensor and interface circuitry, and characterization including calibration and proof of concept deployment into several wind tunnels.

1.1 Research Objectives

Given the need for time-resolved measurements of wall shear stress, this dissertation outlines the development and characterization of a differential capacitive MEMS shear stress sensor system, including sensor packaging, and the development of appropriate instrumentation. The aim of this work is a full sensor characterization,
including characterization of environmental and cross axis sensitivities to provide a system capable of benchmark measurements in flow facilities at the University of Florida and NASA Langley Research Center.

1.1.1 Research Contributions

The contributions from this dissertation are as follows.

- Packaging, development of interface electronics, and characterization of sensor system smooth to within 70 μm
- Sensor system optimization, including prediction and reduction of cross axis sensitivity
- Transition of a shear stress sensor system to a government wind tunnel facility

1.1.2 Dissertation Organization

This dissertation is comprised of seven chapters. First the concept of a boundary layer is briefly discussed, along with a review of the traditional measurement techniques and an introduction to the MEMS capacitive shear stress sensor. The second chapter discusses the sensor modeling, and the third the electronics that are required in order to interface with the sensor. The fourth uses models and constraints developed in chapters two and three to perform a formal optimization of the mechanical sensor design. The fifth chapter discusses the fabrication and packaging of the sensor system. The sixth discusses the test beds at the University of Florida and NASA Langley Research Center that serve to characterize the sensor, and presents results of the system in its entirety. The seventh chapter outlines some conclusions and recommends some concepts to extend this work.

The remainder of this chapter introduces the concept of wall shear stress, discusses the physical phenomena that determine the length and time scales of interest
for different flow conditions that drive the design of the sensor, and provides a general outline of the remainder of this dissertation.

1.2 Boundary Layers and Wall Shear Stress

In order to measure shear stress the foundations of the physics that produce it must be understood. Flow at a contact interface is characterized by two conditions; normal velocity at the interface and tangential velocity at the interface. Given a fluid-solid interface in a continuum flow, the normal velocity component must be zero by definition [3]. At the fluid/solid boundary viscosity forces the local fluid velocity to match the wall velocity, resulting in a “no-slip” boundary condition, seen in Figure 1-1.

\[
\begin{align*}
  u(y) &= U_x \\
  u(y) &= 0 \\
  y &= x \\
  \delta &= \text{thickness of boundary layer}
\end{align*}
\]

Figure 1-1. A schematic of the velocity profile for a flow over a solid surface.

For a Newtonian fluid, the wall shear stress is expressed as
\[ \tau_{\text{wall}} = \mu \frac{du}{dy}_{y=0}, \quad (1-1) \]

where \( \mu \) is the dynamic viscosity, \( u \) is the streamwise velocity of the fluid, and \( y \) is normal to the wall [4].

The region between the wall and the freestream, where viscous forces dominate, is known as the boundary layer. The boundary layer is characterized by several metrics. The simplest description is boundary layer height, \( \delta_{99\%} \), and is defined as the height from the boundary where the local fluid velocity reaches 99% of the free stream velocity. While this metric is important, particularly when discussing measurement techniques, greater physical insight is gained by examining the displacement thickness, \( \delta^* \), and the momentum thickness, \( \theta \). The displacement thickness is a measure of how viscous effects displace inviscid flow from the boundary and is defined for incompressible flow by the integral

\[ \delta^* = \int_0^\delta \left( 1 - \frac{u(y)}{U_\infty} \right) dy. \quad (1-2) \]

Similarly, momentum thickness represents the momentum lost to interactions with the wall and is defined as

\[ \theta = \int_0^\delta \frac{u(y)}{U_\infty} \left( 1 - \frac{u(y)}{U_\infty} \right) dy. \quad (1-3) \]

In the case of flow over a flat plate with zero pressure gradient, these metrics can relate a mean velocity profile to the coefficient of friction, and thus wall shear stress [3], as

\[ C_f = \frac{\tau_{\text{wall}}}{\frac{1}{2} \rho U_\infty^2} = 2 \frac{d\theta}{dx}. \quad (1-4) \]
There are two wall-bounded shear flows used as a basis in this work; laminar boundary layers and turbulent boundary layers. Laminar boundary layers are characterized by smooth flow, molecular transport, and zero frequency content while turbulent boundary layers are characterized by a highly unsteady, multi-scale mixing via turbulent eddies [4]. The magnitude, spatial size, and frequency content of the shear stresses in these two flows will ultimately set the requirements for sensor design.

1.2.1 Laminar Boundary Layers

Laminar flow is characterized by smooth streamlines and is generally observed at low Reynolds numbers. Reynolds number is a dimensionless number representing the ratio of inertial forces to viscous forces and is given by

\[ \text{Re}_x = \frac{\rho U_\infty x}{\mu}, \quad (1-5) \]

where \( \rho \) is the density of the fluid, \( U_\infty \) is the freestream velocity of the fluid, and \( x \) a characteristic dimension.

Table 1-1. Parameters of Blasius’ exact solution for a laminar boundary layer (adapted from [5]).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Blasius Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \frac{\theta}{x} \sqrt{\text{Re}_x} )</td>
<td>0.664</td>
</tr>
<tr>
<td>( \frac{\delta^*}{x} \sqrt{\text{Re}_x} )</td>
<td>1.721</td>
</tr>
<tr>
<td>( \frac{\delta_{99%}}{x} \sqrt{\text{Re}_x} )</td>
<td>5.0</td>
</tr>
<tr>
<td>( C_f \sqrt{\text{Re}_x} )</td>
<td>0.664</td>
</tr>
<tr>
<td>( C_D \sqrt{\text{Re}_x} )</td>
<td>1.328</td>
</tr>
</tbody>
</table>

In the case of laminar boundary layers this dimension is the distance from the leading edge of the wall. There are several similarity solutions that reduce the system
of partial differential equations used to describe a laminar boundary layer to an ordinary
differential equation. For incompressible laminar flow with a zero pressure gradient
over a flat plate, the Blasius solution describes the velocity profile of the boundary layer
[5]. The parameters for this solution are shown in Table 1-1. By definition there is no
frequency content in a laminar boundary layer.

1.2.2 Turbulent Boundary Layers

At high Reynolds number flows, small disturbances in the surface or flow
conditions result in the transition to turbulent flow [6]. Turbulence is a dynamic process
that is described in statistical terms. Although turbulent boundary layer flows do not
possess a closed form analytical solution, empirical relations exist to estimate mean
wall shear stress and the relative frequency content as functions of Reynolds number.
In general the mean shear stress in a turbulent flow is higher than in a laminar flow due
to Reynolds stresses and turbulent mixing. Figures 1-2 and 1-3 below show an
example of a fully developed two-dimensional turbulent boundary layer acquired with a
traversing hot-wire probe in the 20”x28” Shear Flow Control tunnel at the NASA LaRC
facility where $U_\infty = 25 \text{ m/s}$.

A turbulent boundary layer is traditionally decomposed into four major sections;
the viscous sublayer, the buffer layer, the logarithmic region (inertial sublayer), and the
wake, shown in Figure 1-3. These regions are defined by non-dimensionalizing the
parameters into viscous wall units,

$$y^+ = \frac{u_*}{\nu} y,$$

(1-6)

where $u_*$ is the friction velocity given by
\[ u_* = U_\infty \sqrt{C'_t / 2} = \sqrt{\frac{\tau_w}{\rho}} \] (1-7)

and dimensionless velocity,

\[ u' = \frac{u}{u_*} \] (1-8)

Figure 1-2. An example of the velocity profile of a turbulent boundary layer normalized by freestream velocity, where \( U_\infty = 25 \text{ m/s} \), acquired using a traversing hotwire probe at NASA LaRC.

The regions of a turbulent boundary layer are clearly seen in Figure 1-3. The black line indicates the region in where \( u^* = y^* \). It spans from \( y^* = 0 \) to approximately \( y^* = 5 \) defining the viscous sublayer. The red line indicates the region where
where $\kappa = 0.41$ and $B = 5$ via experiment. The data follows this curve defining the log layer from $y^+ = 45$ to $\frac{y}{\delta} = 0.2$. The region in between these two areas is the buffer region and the region beyond the log layer is the wake. Spalding’s Law [7] provides a composite formula accounting for all regions except for the wake

$$y^+ = u^+ + e^{\kappa B}\left[e^{\kappa u^+} - 1 - \kappa u^+ - \frac{(\kappa u^+)^2}{2} - \frac{(\kappa u^+)^3}{6} - \ldots\right].$$  (1-10)

Figure 1-3. The velocity profile in Figure 1-2 converted into wall units using Spalding’s law to determine the friction velocity for non-dimensionalization.

Given these canonical flows the requirements to make a quantitative shear stress measurement and the current measurement techniques are discussed in Section 1.3.
1.3 Shear Stress Measurement Requirements

The basic considerations in shear stress sensor design are; the measurement methods, the physical sensor structure, and the transduction properties. In this section the constraints on physical sensor size and the influence of transduction mechanism are discussed. The measurement methods are discussed in Section 1.4 along with a review of current measurement methods.

1.3.1 Physical Sensor Structure

The physical structure of the sensor must be able to provide accurate spatial resolution, be forgiving to alignment errors, and be hydraulically smooth. The spatial and temporal requirements for the measurement of a turbulent boundary layer are best described by the empirical study from Hutchins et al. [8]. In this study, the effects of probe size on the measurement of velocities in a turbulent boundary layer are parametrically studied. While this is not a direct analog to the measurement of wall shear stress, it is the best estimation of the size and frequency of the structures that induce a wall shear stress.

If a sensing element is too physically large, the smaller structures in the flow will be spatially averaged. Insight is provided by non-dimensionalizing the length of the sensing element, $L$, and the temporal response of the sensor, $t$, using viscous units

\[
L^* = \frac{Lu^*}{v} \tag{1-11}
\]

and

\[
t^* = \frac{tu^{*2}}{v} \tag{1-12}
\]
As long as the sensor’s area meets the requirements for measurement accuracy and is smaller than the characteristic eddy size for bandwidth of the turbulence then the turbulence statistics should be reasonable. According to Hutchins et al. reliable statistics are produced when the non-dimensional length is less than or equal to 20,
\[
L^+ \leq 20, \quad (1-13)
\]
and the non-dimensional timescale is less than or equal to 3,
\[
t^+ \leq 3. \quad (1-14)
\]
Given a known shear stress, and thus a known \(\mu^-\), the maximum sensor length and timescale, and therefore frequency, are given by
\[
L_{\text{max}} \leq 20 \frac{\mu^-}{u^-}, \quad (1-15)
\]
\[
t_{\text{max}} \leq 3 \frac{\mu^-}{u^-}, \quad (1-16)
\]
and
\[
f_{\text{max}} \geq \frac{u^-}{3 \nu}. \quad (1-17)
\]

Along with sensor size restrictions for adequate bandwidth and resolution, sensor height into the flow and surface gaps must be limited so the sensor will not act as an additional source of turbulence. A sensor height of less than five viscous wall units \((y^+ = 5)\) is considered hydraulically smooth and be considered unobtrusive to the flow. Viscous dissipation within \(y^+ = 5\) is dominant and thus any perturbation resultant from the sensor is suppressed [9].

35
1.3.2 Transducer Properties

A transducer converts a signal from one energy domain to another, in this case it will transfer energy from the mechanical domain to the electrical domain by measuring a physical quantity in the flow field and converting it into an electrical signal [10]. There are a variety of mechanisms to achieve this conversion.

The output of an ideal sensor would only be sensitive to an input wall shear force. The transducer should be able to provide both mean and fluctuating information with a frequency range suitable for capturing the dynamics of the flow. In order to measure wall shear forces the transducer must be open to the flow environment. This lack of hermetic packaging means that any other force or change in the environment will act directly on the sensor in addition to the desired shear force. Any pressure input or changes in ambient conditions, such as temperature, humidity, or gas composition should not be fed through to the output signal. No transduction mechanism is truly ideal and a sensor that is open to the environment can react to a multitude of inputs but through careful design the sensitivity to these inputs are reduced. Rejection of cross-axis inputs is achieved through manipulation of the transducer mechanics or through signal conditioning. Understanding how cross axis sensitivities effect the measurement of shear stress requires knowledge of existing measurement techniques.

1.4 Existing Shear Stress Measurement Techniques

This second provides a brief overview of existing shear stress measurement techniques. The primary focus of this work is to leverage existing technology developed at the University of Florida, discussed in Section 1.5, so the breadth of this review is limited. There are a large number of existing methods used to either qualitatively or quantitatively measure wall shear stress. Despite the large number of tools available,
the ability to perform a time-resolved quantitative mean and dynamic shear stress measurement is still unavailable [11].

Shear stress measurement techniques have historically been divided into two general categories, indirect measurement and direct measurement. Indirect measurement techniques measure a physical quantity other than shear stress and then relate the behavior of that physical quantity back to wall shear stress. Direct measurement measures the shear force at the wall. Within each of these categories there are methods that can measure mean shear stress alone and methods that can measure time-resolved mean and dynamic shear stress. The indirect methods that rely on relationships between other quantities and shear stress are discussed in Section 1.4.1. The direct methods that do not rely on correlations or relationships are discussed in Section 1.4.2. Ultimately, the direct microscale sensors have the greatest promise for use as a quantitative time-resolved measurement of wall shear stress.

1.4.1 Indirect Shear Stress Sensors

Indirect measurement techniques rely on underlying correlations between a measured parameter and shear stress to estimate mean or dynamic shear stress values. Comprehensive reviews have been made by Haritonidis [12], Winter [13], Naughton and Sheplak[11], Sheplak et al. [14], Chandrasekharan et al. [15], and Schetz[16].

Methods that are not capable of dynamic measurement include those that are based on surface obstacles or velocity profiles. Surface obstacle measurements, such as Preston tubes, Stanton tubes, razor blades, or fences relate a measured pressure to wall shear stress by empirical correlations. Additionally, the probe for these methods must be contained within the viscous sublayer of the boundary layer. This limits either
the flow conditions to include a thick boundary layer or the probes to be very small [12]. Velocity profile based measurements, such as a velocity profile acquired using a traversing Pitot probe [13], particle image velocimetry (PIV), or low speed laser Doppler velocimetry (LDV) [17], are also limited to mean measurement but as the determination of wall shear stress is based on an empirical fit, such as in Spalding’s law [7], over the whole profile the probe size and proximity to the surface are not as critical. The lack of resolution in near wall data affects the uncertainty of the estimated value of mean shear stress, but an estimate is still available.

Indirect time-resolved measurement methods include heat transfer based devices and high speed optical methods. Heat transfer based devices, like hot-wire anemometers [18], hot film sensors [11], or more recently carbon nanotube based heat transfer devices [19], relate the exchange of heat and mass flux from the device to the flow to velocity through an in-situ calibration. While these devices possess high sensitivity and small size, the tedious and constantly changing calibration prevent them from being a reliable quantitative measurement technique. High-speed optical methods are limited by the near-wall seeding and are not capable of measurement over geometries with separation as seeing cannot access those areas [17].

Micropillars are short compliant structures that extrude into the viscous sublayer. As flow moves across the pillars they displace proportional to the input velocity profile. The displacement of the pillar is imaged, like seed particles in PIV, or sensed using an electromechanical transduction scheme. Additionally, the pillars must be compliant enough to make a measurement while still being small enough to remain in the viscous sublayer [20–22]. Micropillars are categorized generally as indirect as the state of the
flow must be assumed in order to determine the relationship between wall shear stress and pillar displacement. A pillar immersed in the viscous sublayer of a turbulent boundary layer is shown in Figure 1-4. For non-linear velocity gradients the pillar displacement will be dependent on the pressure gradient, so there is no universal calibration for a micropillar and the result given by a micropillar relies on an assumption of the state of the flow.

![Figure 1-4](image.png)

Figure 1-4. A schematic view of a single micropillar where the pillar displacement is indicated by a hashed outline. Image adapted from B. Nottebrock, “Measuring the Two-Dimensional, Two-Directional Temporal Wall-Shear Stress Distribution with the Micro-Pillar Shear-Stress Sensor MPS 3,” (page 3 Figure 1(c)) 48th AIAA Aerospace Sciences Meeting, no. January, 2010.

In all cases as the final determination of wall shear stress is based on empirical relationships. These empirical relationships rely on the flow having a fully developed two-dimensional turbulent boundary layer. Characterization of three-dimensional or separated flows is not possible with these methods.

1.4.2 Direct Shear Stress Sensors

Direct measurement sensors measure shear force on the wall directly without relying on assumptions about the larger flow field. These direct methods will again be
decomposed into methods capable of making time-resolved measurements and those that are not.

Direct mean measurement is achieved using liquid crystal or oil film techniques. In a liquid crystal application the surface is coated with a liquid crystal display that displaces under shear stress. When illuminated the liquid crystal display will appear to have a gradient related to the input shear stress. Oil film techniques are similar as an oil is applied to the surface and is displaced with an input shear stress [11]. Both of these techniques require large optical access and require significant post processing in order to achieve quantitative results. The benefit of this technique is that it is a field measurement and is able to make measurements in a three-dimensional flow.

Figure 1-5. A generalized floating element sensor with the displacement under an input shear stress shown in dashed outlines.
Floating element shear stress sensors are direct methods that both have the capability of making mean and dynamic shear stress measurements. Microscale floating element sensors show the greatest promise in being able to make mean and time-resolved measurements of wall shear stress. A generalized floating element is shown in Figure 1-5. The floating element and tethers are released and are free to move. As flow moves across the sensor the floating element displaces, as shown in the hashed outlines. The tethers act as restoring springs to move the floating element back to a nominal location when the flow input is removed. As discussed by Winter [13] favorable scaling, monolithic fabrication, and minimal cross axis sensitivity indicate that MEMS is an enabling technology for shear stress measurement. The success of the floating element measurement technique is the ability to detect the motion of the floating element.

An example of a microscale floating element shear stress sensor is an optical shutter sensor developed by Padmanabhan, et al. in 1996 [23]. The floating element was suspended over two photodiodes. An incoherent light source is placed opposite the sensor and the floating element acted as an optical shutter. The output of the two photodiodes is read as a differential photocurrent. The structure of the photodiode based floating element sensor is shown in Figure 1-6. While demonstrating a 320 mV/Pa sensitivity and was calibrated in both ac and dc shear stress bench top experiments, it had several drawbacks which prevented extension into wind tunnel testing. The largest source of error was the requirement of an external light source. The placement of this light source relative to the sensor was a large source of error and in a wind tunnel environment vibrations and thermal gradients are expected. The
mechanical motion of the light source and sensor relative to each other prevent this from being a robust measurement technique.

Figure 1-6. A cross-section of the photodiode floating element sensor fabricated by Padmanabhan, et al. Figure adapted from A. Padmanabhan, H. Goldberg, K. D. Breuer, and M. A. Schmidt, “A Wafer-Bonded Floating-Element Shear Stress Microsensor with Optical Position Sensing by Photodiodes,” (page 308, Figure 2) Journal of Microelectromechanical Systems, vol. 5, no. 4, pp. 307–315, 1996.

Since the 1980s many attempts have been made to realize a MEMS floating element sensor for quantifying wall shear stress using various transduction schemes [23–29]. The focus of this work is capacitive transducers.

1.5 Summary of Existing Floating Element Capacitive Shear Stress Sensors

Capacitive sensors are comprised of two electrodes, one attached to the floating element and one to the fixed substrate. The first micromachined direct shear stress sensor was a capacitive transduction based sensor developed by Schmidt, et al. [24] in 1988. A schematic of this device is shown in Figure 1-7. The sensor relied on a change in overlap between an electrode in the floating element and two electrodes beneath a gap below the floating element. As the floating element was made from polyimide the sensor suffered from drift as the in plane stress of polyimide changes with
cycling temperature and humidity. In addition to the embedded electrodes two p-MOS transistors were embedded in the substrate of the sensor. This set a precedent for integrated electronics. However, due to a polyimide layer in the fabrication process, the device suffered significant drift due to moisture accumulation.

Figure 1-7. A cross-section of the capacitive shear stress sensor with integrated electronics fabricated adapted from M. A. Schmidt, R. T. Howe, S.D.Senturia, and J. H. Haritonidis, “Design and Calibration of a Micromachined Floating-Element Shear-Stress Sensor,” (page 753, Figure 4) *IEEE Transactions on Electron Devices*, vol. 35, no. 6, pp. 750–757, 1988.

Comb drive based capacitive shear stress sensors have been developed by researchers at Case Western [30], [31]. In Hyman et al. [31] work the sensor output was overwhelmed by parasitics and undetectable. Pan et al. hoped to improve upon this by using a structure similar to an accelerometer and by implementing force feedback with on board circuitry to avoid the parasitics seen in the first-generation sensor. A schematic of the floating element with force-feedback electrodes is shown in Figure 1-8. The force feedback was found to be insufficient at high shear inputs so the dynamic range of the sensor was lower than predicted [30].
A cantilever based shear stress sensor was developed by Zhe et al. [32] where the lateral movement of a proof mass was detected using capacitive transduction. The beam suspending the floating element was designed with a high aspect ratio in order to reject out of plane motion of the proof mass. The interface electronics consisted of a commercially available MS3110 Capacitive Readout IC. The MS3110 utilizes a charge amplifier and on chip trimming capacitors to detect aF of capacitance change. The charge amplifier is limited to a 1.5 pF minimum feedback capacitance and the bandwidth of the hip is limited to a maximum of 8 kHz. The minimum detectable signal was measured to be 0.04 Pa, but the sensor was only demonstrated in mean flow. The proof mass floating element shear stress sensor, along with the sense and actuate electrodes, is shown in Figure 1-9.
Taking note of the shortcomings of these previous efforts Chandrasekharan et al. [29] designed and calibrated a monolithically fabricated floating element sensor with minimal parasitic contributions [33]. The sensor possessed a normalized sensitivity of 0.766 mV / V / Pa for ac shear stress, but was not able to achieve a reliable dc calibration due to a strong cross-axis sensitivity to humidity and insufficient interface circuitry.

Sells expanded on the design in Chandrasekharan et al. and implemented a wireless detection scheme. The capacitive sensor was used in a single ended fashion as one half of a passive resonant circuit. Due to an additional Teflon-like coating the
humidity sensitivity appeared to be mitigated and Sells was able to attain a static calibration [34]. Again, a lack of instrumentation prevented dynamic measurement and static measurements were only achieved using large bench top spectrum analyzers.

![Diagram of capacitive shear stress sensor](image)

Figure 1-10. A schematic of the capacitive shear stress sensor designed by Chandrasekharan, et al. with an inset view of the asymmetric capacitor gaps. Figure adapted from V. Chandrasekharan, J. Sells, J. Meloy, D. P. Arnold, and M. Sheplak, “A Microscale Differential Capacitive Direct Wall-Shear-Stress Sensor,” (page 623, Figure 1) *Journal Of Microelectromechanical Systems*, vol. 20, no. 3, pp. 622–635, 2011.

### 1.6 Summary

In this chapter the state of shear stress measurement is described and the technical challenges of making a time-resolved direct measurement using a MEMS based system are outlined. To date the most successful attempts at time-resolved direct measurement are floating-element based MEMS sensors, outlined in Table 1-2, however, no existing MEMS shear stress sensor system has been demonstrated in a wind tunnel facility. This work will expand upon the most successful attempts at shear stress measurement, the capacitive sensors by Chandrasekharan [29] and Sells [35], improving on the sensor packaging, supporting system, and calibration in order to make mean and dynamic shear stress measurements in multiple wind tunnel facilities. In addition, the sensor modeling is expanded and an additional fabrication process is
outlined and the technical challenges of improving the overall smoothness of the sensor are described.

Table 1-2. Existing MEMS based floating element methods

<table>
<thead>
<tr>
<th>Sensor System</th>
<th>Element Size [mm]</th>
<th>Shear Stress Range [Pa]</th>
<th>Sensitivity [mV/Pa]</th>
<th>Calibration Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sells [35]</td>
<td>1</td>
<td>4e-3 – 3.9</td>
<td>2729 ppm/Pa</td>
<td>dc</td>
</tr>
<tr>
<td>Chandrasekharan [29]</td>
<td>2</td>
<td>14.9e-6 – 1.9</td>
<td>7.66</td>
<td>ac</td>
</tr>
<tr>
<td>Zhe [32]</td>
<td>3.2</td>
<td>0.04 - .16</td>
<td>337</td>
<td>dc</td>
</tr>
<tr>
<td>Padmanabhan [23]</td>
<td>0.5</td>
<td>1.4e-3 – 10</td>
<td>320</td>
<td>ac(dc)</td>
</tr>
<tr>
<td>Schmidt [24]</td>
<td>0.5</td>
<td>0.01 – 13</td>
<td>0.47</td>
<td>dc</td>
</tr>
</tbody>
</table>
CHAPTER 2
SENSOR MODELING

A capacitive shear stress sensor is an electromechanical transducer used to make
time-resolved mean and dynamic measurements of wall shear stress. The quasi-static
electrical and mechanical behavior along with the coupled dynamic behavior must be
understood before the sensor is fabricated. This work will expand upon models that
describe the in plane response of the floating element structure to include an additional
description of the out of plane response of the sensor. The performance of the sensor is
predicted using quasi-static models, ultimately resulting in a lumped element
representation of the sensor dynamics that are used for optimization.

This chapter is divided into three sections; the quasi-static mechanical model, the
electrostatic model, and the resulting multi-domain lumped element model for the
dynamic response due to an input shear force and the resulting lumped element model
for the dynamic response due to an input pressure force.

2.1 Quasi-Static Mechanical Model

The sensor consists of a perforated rectangular floating element suspended over a
cavity by four tethers, as shown in Figure 2-1. As flow moves across the sensor, the
floating element will move in plane, changing the distance between the comb fingers.
This change in distance is detected electrically by capacitive transduction that is
discussed in Section 2.2. When the flow stops, the tethers, serve as restoring springs,
move the floating element back to its nominal position. Ideally the displacement of the
floating element, and thus the change in distance between the sets of comb fingers, is
linear.
Figure 2-1. A schematic of sensor geometry, not to scale, indicating the design variables of the floating element width, \( W_e \), and length, \( L_e \), the hole diameters, \( d_h \), the finger width, \( W_f \), length, \( L_f \), and overlap, \( L_o \), and the gaps between the fingers \( g_{01} \) and \( g_{02} \).

In order to predict the range of input forces where the displacement is linear Euler-Bernoulli beam theory is used to analyze the behavior of the sensor for both small and large deflections. The non-linear behavior is characterized by an energy model that accounts for in-plane strain in the tethers [36]. By assuming that the tether length is much larger than its width and thickness, that the silicon that is used to produce the floating element is isotropic and linearly elastic, and that the floating element and fingers move as a rigid mass the structure is represented by a clamped-clamped beam. The beam has a length \( 2L_f \), width \( W_f \), and a distributed force, \( Q \), where

\[
Q = \tau_w W_f. \tag{2-1}
\]

The floating element is represented as a point load including the forces of the floating element where the element length and width are \( L_e \) and \( W_e \), respectively, and the force
on the N fingers, that have width \( W_i \) and length \( L_i \). This point load, \( P \), applied to the center of the beam is

\[
P = \frac{\tau_w W_i L_i}{2} + \frac{\tau_w N W_i L_i}{2}.
\]

This simplified structure of the mechanical model with applied forces is shown below in Figure 2-2.

![Figure 2-2](image)

Figure 2-2. A schematic simplifying the floating element sensor to a clamped-clamped beam under an input shear force.

For the case of in-plane deflection, the moment of inertia is about the x-axis is

\[
I_{xw} = \frac{T_i W_i^2}{12}.
\]

The deflection of the beam is,

\[
w(x) = -\frac{\tau_w}{E I_{xw}} \left( \frac{3(L_e W_0 L_i + N W_i L_i L_i) + 8 W_i L_i^2 x^2}{48} - \frac{(L_e W_0 + N W_i L_i + 4 W_i L_i) x^3 + W_i x^4}{24} \right),
\]

that is reduced by substituting in for the moment of inertia,
\[
w(x) = -\frac{\tau_w}{4E_tW_t^2} \left[ \frac{(3L_eW_eL_t + NW_tL_t) + 8W_tL_t^2}{(-2L_eW_e + 2NW_tL_t + 8W_tL_t)x^2 + 2W_tx^4} \right],
\]

where \( E \) is the Young’s modulus of elasticity for the [110] direction of silicon [10]. The deflection at \( x = L_t \) represents the displacement of the floating element, \( \delta \), and is

\[
\delta = -w(L_t) = \frac{\tau_w}{4E_t} \left( W_eL_e + NW_tL_t + 2W_tL_t \right) \left( \frac{L_t}{W_t} \right)^3.
\]

Given the mechanical displacement of the floating element as a function of input shear force the potential or kinetic energy of the system under a physical force is described. As the sensor converts energy from the mechanical domain to the electrical domain its performance in the electrical domain must also be characterized before a full model is developed.

### 2.2 Electrostatic Model

The mechanical motion of the floating element is transferred into a voltage signal by capacitive transduction. When a bias is applied across the sensor floating element and substrate, charge accumulates on the comb fingers. These comb form a parallel plate capacitor and the change in the capacitance will be a function of the change in distance between the comb fingers and is measured electrically. Capacitance is defined as

\[
C = \frac{Q}{V},
\]

where \( Q \) is the charge on the plates and \( V \) is the potential difference between the two plates. By examining the electric field between the plates the capacitance between these plates is
\[ C = \frac{\varepsilon A}{g}, \quad (2-8) \]

where \( \varepsilon \) is the permittivity of the material separating the plates, \( A \) is the area of the plates that overlap, and \( g \) is the gap between them. Due to the 1:5 aspect ratio of the tether structures the field is assumed to be contained in the gap between the two fingers and fringing fields are assumed to be negligible therefore the parallel plate assumption is applied. The validity of this assumption has been discussed in prior work by both Sells [34] and Chandrasekharan [37]. In those studies the capacitance due to fringing fields is approximately 10% of the total capacitance of the finger or tether structure. The total change of the fringing capacitance is approximately 13% of the total capacitance change. The parallel plate assumption greatly simplifies the electrostatic modeling of the transducer while only serving to underestimate overall performance slightly.

As a plate is charged, the source of that charge is expending energy to distribute that charge and is stored in the form of electrostatic potential co-energy, \( W_e \). The electrostatic potential energy is defined as [38]

\[ W_e = \frac{1}{2} CV^2. \quad (2-9) \]

This energy is related to the force acting on the plates due to the attraction or repulsion of the charges on the plates by [38]

\[ F_e = -\nabla W_e. \quad (2-10) \]

For the one-dimensional case of parallel plates this simplifies to

\[ F_e = \frac{Q^2}{2Cg} = \frac{V^2C}{2g}. \quad (2-11) \]
It is important to note that for a change in voltage or a change in gap the force acting on the plates will change.

Now considering the sensor structure, there are three sources of capacitance on the sensor structure; the comb fingers, $C_1$, the tethers, $C_2$, and the floating element, $C_3$. Each of this is indicated below on Figure 2-3, the contributions to $C_1$ outlined with dashes, $C_2$ with dots, and $C_3$ with dashes and dots.

As the floating element moves the gap of each capacitor is changed as a function of input shear as

$$C(\tau_w) = \frac{\epsilon A}{g_0 - \delta(\tau_w)}, \quad (2-12)$$

where $\delta(\tau_w)$ is in the direction indicated by the flow direction.
Capacitor \( C_1 \) is between the moving comb fingers on the floating element and the fixed comb fingers on the substrate. In total three electrodes, indicated as \( E_1 \), \( E_2 \), and \( E_3 \) in Figure 2-3, are involved and four capacitors are formed. Looking at a close up of the finger structure in Figure 2-4 the formation of two of the capacitors is seen.

![Figure 2-4](image-url)

Figure 2-4. The physical structure of capacitor \( C_1 \) showing the asymmetric gaps between comb fingers.

This means for each set of comb fingers two capacitances are formed creating:

\[
C_{1a} = \frac{\varepsilon A}{g_{01}} = \frac{(N-1) \varepsilon T_L}{2 g_{01}} \tag{2-13}
\]

and

\[
C_{1b} = \frac{\varepsilon A}{g_{02}} = \frac{(N-1) \varepsilon T_L}{2 g_{02}} \tag{2-14}
\]

where \( T_L \) is the thickness of the device layer and \( L_o \) is the overlapping distance of the fingers, shown in Figure 2-4. As there is a symmetric structure between electrodes \( E_2 \) and \( E_3 \) the total impedance due to the comb fingers is represented as a capacitive half-bridge seen in Figure 2-5. The arrows represent the trend of the capacitance under a flow in the direction indicated in Figure 2-1.
As $g_{02}$ is designed to be much larger than $g_{01}$, the effects of $C_{tb}$ should be much smaller than $C_{ta}$ in order to concentrate the electric field across $g_{01}$, resulting in a larger nominal capacitance and fewer parasitics.

![Electrical equivalent circuit for $C_1$.](image)

Figure 2-5. The electrical equivalent circuit for $C_1$.

Capacitor $C_2$ is between the moving floating element and the fixed substrate. In total three electrodes, indicated as $E_1$, $E_2$, and $E_3$ in Figure 2-3, are involved and two capacitors are formed.

Capacitor $C_3$ is formed between the moving tether and the fixed substrate. All three electrodes are involved and in total eight capacitors are formed. Looking at a close up of the corner of the element structure in Figure 2-6 the formation of three of the capacitors is shown.

![Physical structures of the floating element capacitance, $C_2$, and the tether capacitance, $C_3$.](image)

Figure 2-6. Physical structures of the floating element capacitance, $C_2$, and the tether capacitance, $C_3$. 
Due to the symmetry of the structure two capacitances are formed; one on each side of
the floating element. This floating element capacitance, $C_2$, is

$$C_2 = \frac{\varepsilon T L_{teff}}{g_{01}}.$$  \hspace{1cm} (2-15)

Four sets of $C_3$ capacitors are formed by the interaction of the tethers with the
substrate. This tether capacitance, $C_3$, is composed of two parallel capacitances

$$C_{3a} = \frac{\varepsilon T L_{teff}}{g_{01}}$$  \hspace{1cm} (2-16)

and

$$C_{3b} = \frac{\varepsilon T L_{teff}}{g_{02}},$$

where $L_{teff}$ is the length of the tether that is approximated as a parallel plate capacitor
when the tether is displaced and is approximated as

$$L_{teff} = \frac{L_1}{2}.$$  \hspace{1cm} (2-18)

Figure 2-7. The half-bridge circuit representation of all variable capacitances on the
sensor structure.

Combining all of these capacitances together, including the direction of change
when under the influence of an applied force indicated in Figure 2-1, produces the
equivalent circuit in Figure 2-7. This is simplified to a smaller structure by grouping terms dependent on each of the gaps resulting in Figure 2-8 where

\[
C_{10} = C_{20} = \frac{(N-1) \epsilon T_L}{2 g_{01}} + \frac{(N-1) \epsilon T_L}{2 g_{02}} + \frac{\epsilon T_{L_{eff}}}{g_{01}} + \frac{3 \epsilon T_{L_{eff}}}{g_{02}}.
\] (2-19)

![Diagram of Figure 2-8](image)

Figure 2-8. The simplified half-bridge representation of the complete floating element structure.

When the floating element is displaced, the capacitances \( C_{10} \) and \( C_{20} \) are no longer be equal. The capacitance associated with the left side of Figure 2-1, \( C_{10} \), becomes

\[
C_{10}(\tau_w) = \frac{(N-1)}{2} \frac{\epsilon T_L}{g_{01} - \delta(\tau_w)} + \frac{(N-1)}{2} \frac{\epsilon T_L}{g_{02} + \delta(\tau_w)} + \frac{\epsilon T_{L_{eff}}}{g_{01} - \delta(\tau_w)} + \frac{3 \epsilon T_{L_{eff}}}{g_{02} + \delta(\tau_w)}
\] (2-20)

or

\[
C_{10}(\tau_w) = \frac{\epsilon T_L}{g_{01} - \delta(\tau_w)} \left( \frac{(N-1)}{2} L_o + L_e + 3L_{eff} \right) + \frac{\epsilon T_{L_{eff}}}{g_{02} + \delta(\tau_w)} \left( \frac{(N-1)}{2} L_o + L_{eff} \right).
\] (2-21)

The capacitance associated with the right side of Figure 2-2, \( C_{20} \), becomes

\[
C_{20}(\tau_w) = \frac{(N-1)}{2} \frac{\epsilon T_L}{g_{01} + \delta(\tau_w)} + \frac{(N-1)}{2} \frac{\epsilon T_L}{g_{02} - \delta(\tau_w)} + \frac{\epsilon T_{L_{eff}}}{g_{01} + \delta(\tau_w)} + \frac{3 \epsilon T_{L_{eff}}}{g_{02} - \delta(\tau_w)}
\] (2-22)
or
\[ C_{20}(\tau_w) = \frac{\varepsilon T_t}{g_{01} + \delta(\tau_w)} \left( \frac{(N-1)}{2} L_o + L_e + 3L_{\text{teff}} \right) + \frac{\varepsilon T_t}{g_{02} - \delta(\tau_w)} \left( \frac{(N-1)}{2} L_o + L_{\text{teff}} \right) \]  
\hfill (2-23)

assuming that the direction of \( \delta(\tau_w) \) is positive in the direction shown in Figure 2-1.

Assuming that a voltage \( V_b \) is applied to \( E_1 \) and a voltage \(-V_b\) is applied to \( E_3 \) the voltage at \( E_2 \) via superposition is

\[ V_{E_2} = \frac{1}{j\omega C_{20}} - \frac{1}{j\omega C_{10}} = \frac{C_{10} - C_{20}}{C_{10} + C_{20}} V_b. \]  
\hfill (2-24)

Substituting in for \( C_{10} \) and \( C_{20} \) produces

\[ V_{E_2} = \frac{1}{j\omega C_{20}} - \frac{1}{j\omega C_{10}} = \frac{C_{10} - C_{20}}{C_{10} + C_{20}} V_b. \]  
\hfill (2-25)

Reducing and assuming the displacement is much smaller than the primary gap this becomes

\[ V_{E_2} = \frac{\delta}{g_{01}} \left( \frac{(N-1)}{2} L_o + L_e + 3L_{\text{teff}} \right) \left( g_{01}^2 + \frac{1}{2} g_{02}^2 \right) \]  
\hfill (2-26)

The second term in the product is
and is associated with attenuation due to the secondary gap. Just as the primary gap creates a sensing capacitance, the gap caused by the proximity of the next set of comb fingers will create an additional parallel electric field. As the relative motion of this secondary gap is opposite that of the primary gap it will be an undesired parasitic to the measurement.

Now that the mechanical response of the sensor to an input shear force and the corresponding change in impedance due to a change in sensor position have been described, a dynamic model coupling the two domains is developed in order to predict sensor performance.

Under an input pressure force ideally the voltage change at electrode $E_2$ is zero, however process variation and the resulting mismatch between the two differential capacitors will allow for generation of an attenuated pressure signal.

### 2.2 Dynamic Modeling

The technique of lumped element modeling (LEM) is used in order to bridge the domains and provide a computationally simple model to predict the dynamic behavior of the system [10]. In order for LEM to be a valid approximation, the wavelength of the physical quantity being measured must be much larger than the size of the sensor, allowing for decoupling of the spatial and temporal effects being measured. In this

\[
H_{\text{gap}} = \left\{ \begin{array}{l}
1 - \frac{(N-1)L_o + L_e + 3L_{\text{teff}}}{2} \left( \frac{g_{01}}{g_{02}} \right)^2 \\
1 + \frac{(N-1)L_o + L_e + 3L_{\text{teff}}}{2} \left( \frac{g_{01}}{g_{02}} \right)
\end{array} \right. \quad (2-27)
\]
case, it means that the spatial variations in shear stress must be larger than the floating element. While this approach is used for many domains, this work will focus on the transfer of energy between the mechanical and electrical domains.

A lumped element model is comprised of elements that can either store or dissipate energy. These “lumped” elements is represented by passive circuit elements; a resistor representing the dissipation of energy, a capacitor representing the storage of potential energy, and an inductor representing the storage of kinetic energy. In the electrical domain these three elements would make up a second order system. In the mechanical domain these three elements could represent a spring-mass-damper system. The sources in both systems are represented by conjugate power variables. In the electrical domain a voltage source would produce a current that moves through the RLC circuit. In the mechanical domain a force produces a velocity. Generally these are referred to as “effort” and “flow” variables respectively. By examining the frequency response of both systems using traditional techniques the analogy is obvious.

The floating element structure is approximated as a mass spring damper system, where the mass is made up of the floating element and the distributed masses of the fingers and tethers, the tethers act as restoring springs, and the damper is a combination of fluidic damping of the air around the floating structure and internal friction of the tethers. In order to predict the electrical response to movement in the system the mechanical and electrical domains are coupled together using a transformer.

A lumped element model is used to predict the dynamic system performance to both in plane and out of plane forces up to just beyond the first resonance of the
structure. The following sections will construct both models given the floating element structure.

2.2.1 **Lumped Element Model for a Shear Input**

Given an input shear stress the floating element will translate in plane. As the floating element displaces the tethers act as restoring springs and the floating element as a mass, storing kinetic and potential energy respectively. By lumping around the point of maximum displacement a lumped mass and lumped compliance is extracted given the sensor geometry.

In order to “lump” an element, the kinetic or potential energy or co-energy of the system must be evaluated. To determine the lumped compliance the potential energy and co-energy of the system are evaluated. The displacement, \( q \), associated with effort, \( e \), is examined resulting in the potential energy

\[
W_{PE} = \int_0^q edq
\]

and co-energy

\[
W_{PE}^* = \int_0^e qde.
\]

The lumped compliance represented the storage of potential energy in the system. As this is a linear time-invariant system the potential energy and co-energy are equal. The potential energy of the system is

\[
W_{PE} = \int dW_{PE} = \int_0^{q_0} edq = \frac{1}{2} \frac{w^2(L_1)}{C_{ME}}.
\]

Using Equation 2.28 the lumped compliance, through the derivation shown in Appendix A, is
To determine the lumped mass, the kinetic energy and co-energy of the system are evaluated. The momentum, \( p \), associated with flow, \( f \), is examined resulting in the kinetic energy

\[
W_{KE} = \int_0^p fdp
\]  

(2-32)

and co-energy

\[
W_{KE}^* = \int_0^f pdf .
\]  

(2-33)

The lumped mass represents the kinetic energy of the system. For a linear time-invariant system the energy and co-energy are equal. The total kinetic energy of the system is

\[
W_{KE} = \int dW_{KE}^* = \int_0^f pdf = \frac{1}{2} M_{ME} f_0^2 .
\]  

(2-34)

Using Equation 2.34, the lumped mass is fully derived in Appendix A is

\[
M_{ME} = \rho T_l \left( \frac{L_t}{W_f} \right)^3 \frac{1}{4ET_f} \left( \frac{L_t}{W_f} \right)^3 \frac{1}{4ET_f} \left( \frac{L_t}{W_f} \right)^3 \left( 1 + \frac{NW_l}{W_e L_e} + 2 \left( \frac{W_l}{W_e L_e} \right)^2 \right)^2 \right.
\]

\[
1 + \frac{2(NW_l + 2W_l)}{W_e L_e} + \frac{4NW_l W_l}{W_e L_e} + \frac{(NW_l + 65 (W_l)^2)}{(W_e L_e)^2} .
\]  

(2-31)
The mechanical natural frequency of the sensor is predicted by assuming a second order system as
\[ f_n = \frac{1}{2\pi} \sqrt{\frac{1}{C_{ME} M_{ME}}} \]  
(2-36)

Assuming that the system is under-damped, the natural frequency approximates the resonant frequency.

Relating these mechanical parameters to an output electrical signal is done using a two-port transformer, as described in Appendix A. The parameter that determines how the two domains couple together is represented by the turns ratio of the transformer and is represented as

\[ \phi' = \frac{V_b}{g_{d1} H_{gap}} C_{ME} \]  
(2-37)

These lumped parameters are represented as a generalized circuit using impedance and inerance analysis. Lumped compliance can also be viewed as

\[ q = Ce = \int f dt, \]  
(2-38)

where \( C \) is compliance, \( q \) is displacement, \( e \) is effort, and \( f \) is flow. Lumped mass is viewed as

\[ p = Lf = \int edt, \]  
(2-39)

where \( L \) is mass and \( p \) is momentum. Combining all of these parameters together into a single circuit model produces Figure 2-7.

As a constant charge-biasing scheme has been chosen for the transducer, the voltage across the sensor capacitance can change. When considering a two-port
model of the reciprocal transduction scheme, the changing voltage indicates a “free” impedance, meaning there is not a fixed potential across the sensor. In order to capture the changing sensor voltage while coupling to the mechanical system, the impedances are transformed into the free impedances indicated with the prime superscript. The complete details of this are available in Appendix A.

Figure 2-9. Circuit representation of the LEM for a shear force input where the mechanical domain is on the left, the electrical domain is on the right, and the electromechanical coupling is represented by lossless transformers.

Using circuit analysis techniques the expected voltage at the sensor output is

$$V_o = H_{gap} \left( \frac{2C_0}{2C_0 + C_p(1 - \kappa^2)} \right) V_b C_{ME} f_e,$$

(2-40)

where $f_e$ is the force acting on the floating element.

The method used to predict sensitivity and dynamics for response to an in-plane force is extended to out of plane forces as well.
2.2.2 Lumped Element Model for a Pressure Input

Given a dynamic pressure force, the floating element will act as a diaphragm and will move in plane. The loading of the beam will be the same as derived in 2.2.1 except that the beam is now moving in the y direction and the moment of inertia of the beam changes to

\[ I_p = \frac{W_t T_t^3}{12}, \] (2-41)

with a resulting transverse displacement of

\[ w(x) = -p \frac{1}{4E W_t T_t^3} \left[ (3(L_e W_e L_l + NW_t L_l L_t) + 8W_t L_t^2) x^2 \right] \]
\[-(2L_e W_e + 2NW_t L_l + 8W_t L_l) x^3 + 2W_t x^4 \]. (2-42)

The lumped mass and compliance of the floating element structure are expressed as

\[ M_{ME pressure} = \rho T_t L_l W_e \left[ 1 + \frac{192}{35} \left( \frac{W_l L_l}{W_e L_e} \right) + 3 \left( \frac{NW_l L_l}{W_e L_e} \right) \right] + \frac{384}{35} \left( \frac{W_l L_l}{W_e L_e} \right) \]
\[+ \frac{1072}{105} \left( \frac{W_l L_l}{W_e L_e} \right)^2 + 3 \left( \frac{NW_l L_l}{W_e L_e} \right)^2 \]
\[+ \frac{1072}{105} \left( \frac{W_l L_l}{W_e L_e} \right)^2 \left( \frac{NW_l L_l}{W_e L_e} \right) \]
\[+ 3 \left( \frac{NW_l L_l}{W_e L_e} \right)^2 \left( \frac{W_l L_l}{W_e L_e} \right) + \frac{2048}{315} \left( \frac{W_l L_l}{W_e L_e} \right)^3 \]
\[+ \frac{NW_l L_l}{W_e L_e} \left( 1 + \frac{NW_l L_l}{W_e L_e} + 2 \frac{W_l L_l}{W_e L_e} \right)^2 \] (2-43)

and

\[ C_{ME pressure} = \frac{60W_e^2 L_e^2 L_l^2}{4E W_t T_t^3 \left( (4W_e + W_e L_e + NW_t L_l) \right)} \left[ 15(L_e W_e + NW_t L_l) + 88W_t L_l \right] \]. (2-44)

The full derivation of these elements is present in Appendix B.

Unlike the shear stress case, the acoustic properties of the cavity will now contribute to the mechanics of the system. As the floating element moves the air in the
cavity will act as a spring. The squeeze film damping and viscous losses of the fluid moving under, around, and through the perforations in the floating will act as a resistive element. Following the procedure used to develop a perforated diaphragm capacitive microphone that uses models developed by Skvor [39] and Homentcovschi and Miles [40] to predict the resistance due to viscous losses as,

\[ R_{\text{viscous}} = \frac{72 \mu_{\text{air}} T n_h}{(L_e W_e)^2 A_r^2}, \]  

where \( n_h \) is the number of holes in the element, \( A_r \) is the ratio of the area of the holes to the area of the floating element, and \( \mu_{\text{air}} \) is the viscosity of air. The resistance due to squeeze film damping is predicted by Skvor as

\[ R_{\text{squeeze film}} = \frac{12 \mu}{\pi n_h g_0} B(A_r), \]  

where \( g_0 \) is the height of the back cavity and

\[ B(A_r) = \frac{1}{4} \ln \left( \frac{1}{A_r} \right) - \frac{3}{8} + \frac{1}{2} A_r - \frac{1}{8} A_r^2. \]  

The total acoustic resistance is the sum of these two resistive elements

\[ R_{AC} = R_{\text{viscous}} + R_{\text{squeeze film}}. \]  

The lumped approximation for cavity compliance is [41]

\[ C_{AC} = \frac{V}{\rho_0 c_0^2}, \]  

where \( V \) is the volume of the cavity.

As the motion of the element has changed the way that motion creates a change in capacitance has changed. While the change in capacitance due to an input shear force was due to a change in the gap between electrodes an input pressure will cause a
change in the overlapping area of two electrodes, that will change the coupling coefficient and the conclusion of the electrostatics discussion.

The coupling coefficient is found using the two-port model derived in Appendix B as

\[
\phi' = \frac{T}{Z_{MO}} = -\frac{V_b}{T_1}C_{ME\text{pressure}}.
\]

(2-50)

The full model is shown below in Figure 2-10.

Figure 2-10. Circuit representation of the LEM for a pressure input where the mechanical domain is on the left, the electrical domain is on the right, and the electromechanical coupling is shown by lossless transformers.

The prediction of the output voltage is difficult because ideally pressure is ideally a common mode signal to both sides of the bridge. In the ideal equation for output voltage, the tether thickness term drops out. In reality, process variation creates a mismatch between the two capacitors and the common mode rejection is imperfect. The output voltage is
Assuming that $C'_{10} = C'_{20}$, this term would be zero meaning there is no output due to a pressure input. Assuming a mismatch, $M$, such that $C'_{10} = MC'_{20}$ and a pressure force acting on the sensor, $f_p$, the output becomes

$$V_o = \frac{C'_{10} - C'_{20}}{C'_{10} + C'_{20}} \frac{V_b}{T_i} \delta(t_w).$$

(2-51)

This mismatch, $M$, is estimated using the fabrication in Chandrsekharan, et al. [29] as $0.91$ where the capacitance values $C_{10}$ and $C_{20}$ were measured as $14.8$ pF and $16.3$ pF respectively [37], which resulted in a $64$ dB overall rejection to an input pressure.

### 2.3 Summary

In this chapter the models used to predict the static and dynamic response of the sensor to an input shear stress sensor are outlined and additional models for the dynamic response to pressure are developed. Using these models sensor mechanical performance given shear and pressure inputs is predicted. Before overall sensitivity is determined the interface between the sensor and the electronics must be examined in order to determine what impact the electronics have on sensor performance.
CHAPTER 3
INSTRUMENTATION DESIGN FOR CAPACITIVE TRANSDUCERS

In order to predict the system response, the characteristics of the interface circuitry and the corresponding effects on sensor performance must be derived. This chapter will first outline the need for an interface circuit, then the building blocks for circuit modeling, and finally discuss two common interface circuits. Larger circuit topologies will then be discussed in the context of prior work using them as an interface with capacitive sensors. Finally the chosen system will be described in detail.

3.1 Impact of Interface Circuitry on Transducer Performance

In order for a transducer to be used in any kind of system, it must ultimately interface with a data acquisition system or a component that will attempt to read the output signal, whether that is a voltage or current, of the transducer. For the capacitive shear stress sensor this will be an output voltage present at the middle node of the differential capacitor, $V_o$, as shown in Figure 2-8. Ideally, the interface will not alter the signal in any way.

There are two primary considerations when analyzing how an interface circuit will influence the measurement; additional noise sources that can change the overall signal to noise ratio of the system, and parasitic impedances that can act as a source of signal attenuation. Higher order effects, such as the dynamic response of the circuit, will also impact design but are less generalized and are left to the discussion of specific interface topologies in Section 3.4. Section 3.2 discusses amplifiers, the most common building block for interface circuitry, and the sources of attenuation including parasitic impedances of common interface circuits and other sources of signal attenuation within
amplifiers. Section 3.3 discusses the major noise sources in an interface circuit and how they contribute to the output of a sensor system.

3.2 Amplifiers

An operational amplifier is a basic active component that is configured to provide gain in a system or simply provide an impedance buffer. There are five ideal operational amplifier assumptions that must be examined for validity before building an amplifier; (1) the input impedance is infinite, (2) the output impedance is zero, (3) rejection of common mode signals is infinite, (4) open-loop gain is infinite, and (5) the bandwidth of the amplifier is infinite.

The input impedance of the operational amplifier is particularly important when interfacing with any kind of transducer as this impedance will be in parallel with any device attached to the amplifier. An ideal operational amplifier is shown in Figure 3-1 with impedances at the inputs to account for non-ideal op amp input properties.

![Figure 3-1. The model of an operational amplifier showing input referred noise current and voltage noise sources and finite input impedances.](image-url)
In Figure 3-1 the common mode input impedances are shown as $R_{icm}$ and $C_i$, and the differential input impedance as $R_{idm}$. The voltage supply to the amplifier is shown as $V_{cc}$ for the positive supply voltage and $V_{ee}$ as the negative supply voltage. The magnitudes of these impedances are given in the electrical specifications portion of an operational amplifier datasheet and are largely dependent on the technology used to manufacture the amplifier and the amplifier topology [42].

The output impedance assumption is important when considering the load that the amplifier will be driving [43]. Assuming moderate cable lengths and small scale installations, the assumption of zero output impedance should not be an issue for this the capacitive sensor application.

Common-mode signal rejection is most easily described by a fully differential transducer. Taking the example of a fully active Wheatstone bridge any signal that affects all of the elements of the bridge equally will not propagate to the output of the sensor [44]. Amplifiers are capable of this same rejection from signals that are either common to both the inverting and non-inverting amplifier inputs or to the power supply inputs. The ability of an amplifier to reject a common mode signal is dependent on the architecture of the amplifier and the tolerance of the process used to fabricate the amplifier. Given that the capacitive transducer is not fully differential, meaning that only one amplifier input will be utilized, only the power supply rejection will be of interest and should be considered when the final system noise model is constructed.

The open-loop gain of an operational amplifier is determined by its architecture. Finite open-loop gain impacts frequency performance when the operational amplifiers are configured into high gain amplifiers or when amplifiers are operated at high
frequencies by attenuating at higher frequencies. At low frequencies, keeping in mind that an amplifier cannot produce an output voltage that exceeds the voltage level that it is biased with, the output of the amplifier is limited based on the sensitivity of the transducer that it is being interfaced with. In most instances, the closed-loop gain required to keep the sensor output within the rails of the amplifier is low enough so the open-loop gain is considered comparably infinite [44].

![Frequency response of the open-loop gain of an operational amplifier.](image)

Figure 3-2. Frequency response of the open-loop gain of an operational amplifier.

The final assumption considers the amplifier bandwidth. Most operational amplifiers rely on an internal compensation circuit to stabilize the internal feedback loop [45]. The capacitance required in this stabilization circuit is usually chosen such that it creates a dominant pole in the amplifier, generating a low pass response. The open-loop gain is expressed as a general single-pole system.

\[
A(\omega) = \frac{A_0}{1 + \frac{j\omega}{\omega_c}}
\]  

(3-1)
where $A_0$ is the open-loop gain and $\omega_c$ is the 3dB frequency. The open-loop gain of such a single pole system rolls off at -20dB/decade. The frequency where the response reaches 0dB is defined as the unity gain bandwidth, $\omega_b$. These frequencies are labeled in Figure 3-2.

The roll-off in open-loop gain with increasing frequency will eventually cause the assumption that the open-loop gain is much larger than the closed-loop gain to fail. This will attenuate the amplifier output. This effect is normally described as the gain-bandwidth product (GBWP).

### 3.3 Basic Noise Models and Non-Idealities

This section will present the noise models and other non-ideal characteristics of passive components, how they combine, and finally the noise characteristics of operational amplifiers.

#### 3.3.1 General Noise Characterization

Generally, noise is defined as any unwanted disturbance in a signal and the characterization and minimization of noise is critical to the success of any system. Electronic noise is expressed in terms of a power spectral density and is a function of frequency. To characterize the propagation of noise through a system individual noise sources are modeled as voltage or current sources [46]. There are many categories of noise, however in this work the dominant noise sources are thermal noise and low-frequency noise.

Thermal noise is characterized by flat spectral density content across the frequencies of interest. It is caused by random thermal carrier excitation. In a bulk material the electrons vibrate in Brownian motion. While the net current through the
bulk material due to this random motion is zero the random charge fluctuations create a
time varying voltage across the material. The total available noise power of a conductor
is represented as

\[ N_i = kT \Delta f, \]  

(3-2)

where \( k \) is Boltzmann’s constant, \( T \) is the temperature in Kelvin, and \( \Delta f \) is the
bandwidth that the noise is measured over. One of the goals of this work is to perform a
dc measurement, the behavior of both of these theoretical noise types at zero frequency
is also important.

Low-frequency noise, also called \( 1/f \), or flicker, is a noise characterized by large
low-frequency content that decreases in power proportionally to an increase in
frequency. It is present in almost all electronic systems, including transistors, diodes,
and some resistors. Flicker noise is largely a property of the surface of the material that
a device is made from due to the random recombination and generation of carriers due
to bulk or surface charges, such as those present at the interface between silicon and
silicon dioxide. Low frequency noise should be infinite by definition at dc. While the
level of noise is constantly decreasing as frequency increases, the total noise power
contained within each frequency decade is constant. This restriction on total power per
decade combined with the time scales of actual equipment usage constrains the noise
power from going to infinity at dc.

In all cases, a specific device will have some combination of thermal and \( 1/f \)
noise, resulting in a shaped noise spectrum. Given multiple uncorrelated noise sources
in a linear system, the source spectra will add in power, resulting in an overall noise
spectrum for the system. Every passive and active component contains multiple noise
sources. The representations for commonly used components follow in Sections 3.3.2 and 3.3.3.

3.3.2 Noise in Passive Components

There are two types of passive components used in this system, resistors and capacitors. This section will discuss the noise characteristics of both independently and then their combined effect on the noise spectrum.

Resistors are made using many different technologies. In this work they will be generalized into two kinds of resistors, metal-film and polysilicon (poly) [46]. In CMOS integration, resistances are realized using polysilicon strips of a given sheet resistance. By manipulating the geometry of the poly the resistance is changed, however low resistances require very thick or wide films with higher doping concentrations. Metal-film resistors are implemented with metal strips of varying geometry. Given the sheet resistances of metals, lower resistances are easier to achieve using metal-film technology. While both technologies result in theoretical thermal noise levels, the low frequency performance varies greatly depending on the fabrication technology. Poly resistors generally have higher $1/f$ noise [46]. Theoretically metal film resistors should have no $1/f$ noise, but in practice some low frequency noise is observed due to non-idealities in packaging. The available noise power, shown in 3.3.1, is the total available power that is sourced by a noisy resistor to a noiseless load resistor. For maximum power transfer the load resistance is equivalent to the source resistance and thus the power spectral density of noise in a resistor is given by

$$S_n = 4kTR \left[ \frac{V_{\text{rms}}^2}{\sqrt{\text{Hz}}} \right],$$

(3-3)
where $T$ is the absolute temperature of the resistor, $R$ is the resistance value, and $k$ is Boltzmann’s constant. This is represented as a voltage source or equivalent current source given by

$$v_n = \sqrt{4kTR\Delta f} \ [V_{rms}]$$ \hspace{1cm} (3-4)$$

and

$$i_n = \sqrt{\frac{4kT\Delta f}{R}} \ [A_{rms}] \hspace{1cm} (3-5)$$

A noisy resistor is decomposed into the equivalent noise voltage source and a noiseless resistor, or into a noiseless resistor and a Norton equivalent current source, as shown in Figure 3-3 [46], per the fluctuation-dissipation theorem.

An ideal air-gap parallel plate capacitor has no mechanism for noise generation, as there are no carriers to vibrate and no direct charge transfer. Many capacitors are made with a ceramic insulator, so that the dielectric properties are manipulated to achieve a larger range of capacitance values. These ceramic materials have a finite resistance that can result in a parallel resistance, that is then subject to noise induced by a resistor.

![Figure 3-3](image.png)

Figure 3-3. A noisy resistor and the equivalent Thevenin and Norton equivalents showing the noise as an independent voltage or current source.

The noise characteristic across the parallel combination of a resistor, $R$, and capacitor, $C$, known as $kT/C$ noise, is a shaped spectrum dependent on the values of $T$, $R$, and $C$. 

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R and C. Given a parallel RC circuit, shown in Figure 3-4, the thermal noise of the resistor is low pass filtered.

![Parallel RC Circuit](image)

Figure 3-4. The circuit model for analysis of the effect of a parallel capacitance on the thermal noise of a resistor.

As the RC product changes, the shape of the noise at the output will change as

\[ v_{nRC} = \sqrt{4kTR} \frac{1}{1 + j\omega RC} . \]  

(3-6)

To illustrate this shaping, assume an initial RC product of 0.1, the effect varying the value of R from 1 to 9 is shown in Figure 3-5 versus normalized frequency. As the RC product increases the corner of the low pass filter moves lower in frequency, resulting in higher noise at low frequencies but lower noise values as frequency increases. While varying the resistance changes the shape of the noise, it does not change the root mean square value. The total noise power is given by

\[ v_{nRC}^2 = \int_0^\infty v_n^2 \left( \frac{1}{1 + j\omega RC} \right) df . \]  

(3-7)

Using change of variables, letting \( f = \frac{1}{2\pi RC} \tan \theta \) results in

\[ v_{nRC}^2 = \int_0^{\pi/2} v_n^2 \frac{1}{2\pi RC} \sec^2 \theta \frac{1}{1 + \tan^2 \theta} d\theta . \]  

(3-8)

Substituting in for \( v_n \) gives
This is interesting in that the total output root mean squared noise is not dependent on
the thermal noise source being shunted, but rather solely the parallel capacitance. This
will become important as more complex circuit systems are constructed using RC
combinations.

\[ v_{nRC}^2 = \int_0^{\pi/2} \frac{4kTR}{2\pi RC} d\theta = \frac{kT}{C}. \] (3-9)

Figure 3-5. The spectral density of the thermal noise of a resistor shaped by a parallel
capacitance plotted against normalized frequency to demonstrate the spectral
shaping of the RC product.

3.3.3 Amplifier Noise

The most common method in instrumentation design to create an amplifier is to
use external feedback with an operational amplifier to perform a specific function. As an
operational amplifier is constructed using multiple transistors and passive components,
it is more useful to combine all of the individual noise sources to the input of the
amplifier. Operational amplifier noise is characterized by two sources, a voltage noise source at the input of the amplifier and a current source in parallel with the inputs. This model is shown in Figure 3-6 [47]. The voltage supply to the amplifier is shown as $V_{cc}$ for the positive supply voltage and $V_{ee}$ as the negative supply voltage, while $v_n$ and $i_n$ represent the input referred voltage and current noise sources respectively.

![Operational Amplifier Noise Model](image)

Figure 3-6. The operational amplifier noise model, showing the overall noise of the amplifier as an input referred voltage and current source.

Usually the amplifier manufacturer will produce a plot describing the low frequency noise characteristics of the amplifier.

### 3.3.4 Other Non-Idealities

One of the most basic constraints on amplifier performance is the output swing. An amplifier cannot physically produce a voltage larger than what it is supplied from its power inputs, and in many cases is restricted to some incremental value below these power inputs depending on the operational amplifier architecture. The resulting output is said to be "clipped". Clipping is visualized in Figures 3-7.
3.4 Interface Circuits

In this section two basic interface circuits are discussed. The noise characteristics and transfer functions are explained and the applications that they are well suited for use in are outlined.

3.4.1 Unity Gain Voltage Buffer

The simplest non-inverting operational amplifier implementation is the unity gain voltage follower, shown in Figure 3-8. Simple circuit analysis shows that $V_{out} = V_{in}$, meaning that if this circuit is interfaced with a transducer the output voltage of the transducer would be translated, but the impedance of the transducer would be decoupled from anything attached to the output node.
Figure 3-8. The circuit schematic of a unity gain operational amplifier.

To interface the capacitive transducer with a voltage amplifier, a constant charge-biasing scheme is used. In this case, two signals of opposite phase are placed on either end of the capacitive half-bridge, as shown in Figure 3-9. Interfacing the capacitive transducer with the small signal noise and parasitic model of the voltage buffer provides meaningful insight into its behavior and the metrics that should be examined when choosing the amplifier.

Through analysis shown in detail in Appendix C the output when considering parasitics is

\[
V_{\text{out}} = V_{\text{bias}} \frac{j \omega R_b (C_1 - C_2)}{j \omega R_b (C_1 + C_2 + C_p + C_I) + 1}. \tag{3-10}
\]

This shows the output voltage has a high pass characteristic based on device capacitance and bias resistance. Past the system cut-on, \( \omega R_b (C_1 + C_2 + C_p + C_I) \gg 1 \), the output voltage reduces to

\[
V_{\text{out}} = V_{\text{bias}} \frac{C_1 - C_2}{C_1 + C_2 + C_p + C_I}. \tag{3-11}
\]
Next, considering that $C_1$ and $C_2$ are described as $C_1 = C_0 - \Delta C$ and $C_2 = C_0 + \Delta C$

Equation 3.10 is further reduced to

$$V_{out} = V_{bias} \frac{(C_0 - \Delta C) - (C_0 + \Delta C)}{C_0 - \Delta C + C_0 + \Delta C + C_p + C_i}$$

(3-12)

or

$$V_{out} = V_{bias} \frac{2\Delta C}{2C_0 + C_p + C_i}.$$  

(3-13)

In this simplification the frequency term drops out, however it is important to note that as the impedance of a capacitor is infinite at dc. This means that when sensing a mean capacitance change when a dc bias is applied the output voltage will be undefined.

The noise performance of the voltage buffer is also important in determining its usefulness in interfacing with capacitive transducers. In Appendix D the output referred noise characteristic is derived in detail. From the schematic shown in Figure 3-10 the total output referred noise is
\[
V_{\text{out}}^2 = V_n^2 + (i_n Z_{\text{in}})^2 + 4kTR_b \left( \frac{Z_{\text{in}}}{R_b} \right)^2,
\]  

(3-14)

where
\[
Z_{\text{in}} = \frac{R_b}{j \omega R_b (C_i + C_p + C_1 + C_2) + 1}
\]  

(3-15)

as indicated in Figure 3-12.

For simplicity, consider operation and performance above the system cut-on, where \( \omega R_b (C_i + C_2 + C_p + C_i) \gg 1 \). The output referred noise from Equation 3.13 then reduces to
\[
V_{\text{out}}^2 = V_n^2 + \left( i_n \frac{1}{j \omega (C_i + C_p + C_1 + C_2)} \right)^2 + \frac{4kTR_b}{(j \omega R_b (C_i + C_p + C_1 + C_2))^2}.
\]  

(3-16)

It is important to note that two of the three noise contributions are shaped by frequency. First, the current noise of the amplifier is scaled by the impedance of the capacitive elements. Second, thermal noise of the bias resistor is shaped by the impedance of the capacitive elements.

Figure 3-10. The small-signal model of the sensor and a unity gain amplifier including noise sources.
The relative order of magnitudes of the three noise sources will allow for further simplification in this expression. As reported in Chandrasekharan [29], measured values for the device capacitance, including parasitics associated with the device, are on the order of 15 pF. A nominal value for an off the shelf amplifier with a low capacitance input is around 1 pF. This produces a total capacitance of around 16 pF. In order to quantify all of the noise sources, the bias resistance must be determined.

As shown in Figure 3-11, the device capacitance and bias resistance form a high pass filter network. This creates a cut on frequency and eliminates the possibility of measuring an input voltage with at low frequencies or dc. As the value of the bias resistance increases, it will approach the input impedance of the amplifier and inhibit the proper functioning of the input stage of the amplifier. The selection of the bias resistance becomes a balancing act between voltage noise, amplifier input impedance, and desired frequency of operation. As the frequency of operation of the sensor is increased, the bias resistance value can decrease and the overall performance of the circuit will improve.

### 3.4.2 Charge Amplifier

The second simple interface circuit topology is the charge amplifier, shown in Figure 3-11. Again, this circuit serves as a means to decouple the transducer from the output node while maintaining signal integrity and is commonly used in low signal application such as accelerometer interface circuitry. This differs fundamentally from the voltage amplifier as a gain is introduced by changing the feedback impedance.

Using superposition, similar to the derivation shown in Appendix C, the output voltage of this system assuming $C_1 = C_0 - \Delta C$ and $C_2 = C_0 + \Delta C$ is
\[ V_{\text{out}} = 2V_{\text{bias}}j\omega\Delta C \frac{R_{\text{fb}}}{j\omega C_{\text{fb}}R_{\text{fb}} + 1}. \] (3-17)

Assuming that the system is operating beyond the high-pass cut-on set by the feedback impedance the output is simplified to

\[ V_{\text{out}} = V_{\text{bias}}2\frac{\Delta C}{C_{\text{fb}}}. \] (3-18)

Figure 3-11. The circuit schematic of a charge amplifier interfaced with the sensor, including parasitic capacitances.

The important thing to notice is that the output is independent of any parasitic contributions. This relaxes packaging requirements as the interface electronics no longer have to be co-located with the sensor. Again, as in the case of the voltage buffer in this simplification the frequency term drops out, however as the impedance of a capacitor at dc is infinite this simplification is invalid at dc. The dc operation of the circuit is defined by the bias and feedback resistances and the amplifier. This means that without a frequency component the output voltage will be undefined.

The noise characteristics of a charge amplifier are examined using Figure 3-12.
Figure 3-12. The schematic of the sensor interfaced with a charge amplifier including small signal noise sources.

Again using superposition, following the analysis in Appendix D for the voltage amplifier case, the output-referred noise is.

\[
V_{out}^2 = V_n^2 \left(1 + \frac{Z_{fb}}{Z_{in}}\right)^2 + \left(i_n^2 + \left(\frac{\sqrt{4kTR_{fb}}}{R_{fb}}\right)^2 + \left(\frac{\sqrt{4kTR_b}}{R_b}\right)^2\right)Z_{fb}^2,
\]

(3-19)

where

\[
Z_{in} = \frac{R_b}{j\omega(C_p + C_{in} + C_2 + C_i)R_b + 1}
\]

(3-20)
as shown in Figure 3-14 and

\[
Z_{fb} = \frac{R_{fb}}{1 + j\omega C_{fb} R_{fb}}.
\]

(3-21)

The feedback impedance while providing a source of gain also serves as a low pass filter for the interface circuit. If the transducer output has frequency content above the filter cutoff it will be attenuated, making charge amplifiers more suited for low frequency applications.
Given these basic interface building blocks the overall circuit topology is chosen. Using the noise and impedance characteristics developed in this section, the overall performance is predicted.

3.4.3 Comparison of Voltage and Charge Amplifiers

Given the models developed in 3.4.1 and 3.4.2 the performance of voltage amplifiers and charge amplifiers are compared in this section so that the chosen interface topology has the largest possible signal to noise ratio (SNR). For this study two amplifiers will be chosen as representative examples of op-amps. The first is the AD8022 from Analog Devices and is an example of a low voltage noise, low input capacitance amplifier [48]. The second is the OPA129 from Texas Instruments and is an example of a low current noise, low input capacitance amplifier [49]. The parameters for each are shown in Table 3.1.

Table 3-1. Op-Amp parameters for parametric study of interface amplifier topologies.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Input Capacitance</th>
<th>Input Referred Current Noise</th>
<th>Input Referred Voltage Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD8022</td>
<td>0.8 pF</td>
<td>1 pA / \sqrt{Hz}</td>
<td>2.3 nV / \sqrt{Hz}</td>
</tr>
<tr>
<td>OPA129</td>
<td>1 pF</td>
<td>0.1 fA / \sqrt{Hz}</td>
<td>15 nV / \sqrt{Hz}</td>
</tr>
</tbody>
</table>

The comparison is made for several nominal capacitances (0.1 pF, 1 pF, and 10 pF) and bandwidths of interest (10 kHz, 100 kHz, and 1 MHz) in order to determine scaling trends in overall SNR. In all cases the assumed bias voltage is 8 Vac and the change in capacitance is 1 fF. The charge amplifier is configured such that there is no gain in order to compare the performance directly to the voltage amplifier. If gain is programmed into the charge amplifier, the signal to noise ratio will be effected only if the bias resistance is the dominant noise contribution. As the feedback capacitance
decreases, the resistances will have to increase in order to maintain the same cut-on frequency and thus the noise floor will change. The bias resistance is assumed to be equivalent between the two topologies. The results are categorized by nominal device capacitance, where the amplifier and bandwidth are swept for each device. The metrics that are examined are the total noise and the signal to noise ratio.

### 3.4.3.1 Comparison with smallest device capacitance

For a device with a nominal capacitance of 0.1 pF the bias resistances in order to hit the bandwidths of interest are 1.6 GΩ, 0.16 GΩ, and 16 MΩ, respectively. Realistically, these impedances are too large to be implemented with the AD8022 as they are on the order of the input resistance. The OPA129 would still be able to function with input resistances on this order, so only it is considered for this nominal capacitance. As the lowest bias resistance is associated with the 1 MHz bandwidth, it is used to examine the magnitudes of the voltage noise, current noise, and resistor noise in a given configuration.

The total noise and the considered contributions are shown in Figure 3-13 for the total noise of a charge amplifier and voltage amplifier. The total noise for the different configurations and all bandwidths are shown in Figure 3-14. From this figure it is clear that in all configurations the OPA129 in the voltage amplifier configuration has the lowest noise floor. While at this point in the analysis the obvious choice is the voltage amplifier configuration the impact of parasitic capacitance on signal attenuation has not yet been considered.
Figure 3-13. The noise contributions and total noise for interfacing with a 0.1 pF capacitor with a signal of interest at 1 MHz using an OPA129 configured as a A) a voltage amplifier and B) a charge amplifier.
Figure 3-14. The noise spectra of the OPA129 configured as a voltage amplifier and current amplifier for multiple bias resistances to interface with a transducer with a nominal capacitance of 0.1pF.

The metric that these effects are evaluated is the overall signal to noise ratio of the system. The signal to noise ratio is determined by the power of the output signal when the total capacitance change is 1 fF and the power of the noise. The results of this analysis are shown in Figure 3-15. While the voltage amplifier has the lower noise floor, the small nominal capacitance is completely overwhelmed by the parasitic input capacitance of the amplifier and so the overall signal to noise ratio is very small. The charge amplifier configuration, while having higher noise, has much higher signal and thus has a much better overall performance. For small nominal capacitances the overall signal to noise ratio is improved by using a charge amplifier. When the nominal device capacitance changes the trends in signal to noise ratio also change.
Figure 3-15. The comparison of the signal to noise ratio of multiple configurations.

3.4.3.2 Comparison with intermediate device capacitance

For a device with a nominal capacitance of 1 pF the bias resistances in order to hit the bandwidths of interest are 0.16 GΩ, 16 MΩ, and 1.6 MΩ, respectively. At the lower bias resistances the AD8022 is now functional. For this case both the AD8022 and OPA129 are considered. First, the AD8022 is examined.

The AD8022 is chosen as a representative amplifier for low input capacitance and low voltage noise. As in Section 3.4.3.1, the noise contributions and resultant total spectrum is shown for the AD8022 configured as a charge and voltage amplifier in Figure 3-16. As this amplifier has relatively high current noise, the current noise becomes the dominant term in the overall noise equation. Examining all of the output referred noise plots again it appears that the voltage amplifier configuration has lower overall noise, as the current noise of the amplifier is shaped by an overall lower
impedance than in the charge amplifier configuration. The compiled noise spectra are shown in Figure 3-17.

As the OPA129 is chosen as a representative of a low current noise amplifier the noise spectra are shaped by the bias resistance rather than this current noise, as shown in Figure 3-20. Also, the overall noise spectra for varying bandwidths also appear to have trending as seen in 3.4.3.1, as seen in Figure 3-18, where the voltage amplifiers have overall lower noise floors and all spectra are shaped with respect to the magnitude of the bias resistance.

The view of system performance through noise floor is again only part of the total picture. The signal to noise ratio is the final evaluation of overall system performance. The signal to noise ratios for all configurations are shown for the AD8022 and OPA129 in Figure 3-19. In the case of the AD8022 the overall signal to noise ratio is roughly equivalent in all implementations. For the OPA129, however, the signal to noise ratio demonstrates that the charge amplifier is the more appropriate implementation at high frequencies.

It is important to note, however, than the AD8022 implementations have overall higher signal to noise ratios but the signal to noise ratio is also greatly frequency dependent. This is due to the heavy shaping of the dominant current noise and the difference in fundamental noise level between the OPA129 and AD8022 that is a result of the dominant noise mechanisms in both cases. This is seen in Figure 3-20, where the signal to noise ratio for all implementations is plotted against frequency.
Figure 3-16. The noise spectra of an AD8022 for a nominal capacitance of 1pF at 1 MHz A) configured as a charge amplifier and B) configured as a voltage amplifier.
Figure 3-17. The noise spectra of the AD8022 configured as a voltage amplifier and current amplifier for multiple bias resistances to interface with a transducer with a nominal capacitance of 1pF.

Figure 3-18. The noise spectra of the OPA129 configured as a voltage amplifier and current amplifier for multiple bias resistances to interface with a transducer with a nominal capacitance of 1pF.
Figure 3-19. The noise spectra of an OPA129 for a nominal capacitance of 1pF at 1 MHz configured as A) a charge amplifier and B) a voltage amplifier.
Figure 3-20. The signal to noise ratio for all configurations when interfanced with a device of 1 pF nominal capacitance using A) an AD8022 and B) an OPA 129.
3.4.3.3  **Comparison with largest device capacitance**

For a device with a nominal capacitance of 10 pF, the bias resistances in order to hit the bandwidths of interest are 16 MΩ, 1.6 MΩ, and 160 kΩ, respectively. At the lower bias resistances the AD8022 is now functional. For this case both the AD8022 and OPA129 are considered. First, the AD8022 is examined. The noise spectra for the AD8022 configured as a charge amplifier and voltage amplifier are shown in Figure 3-21. As seen in 3.4.3.2 the dominant noise source is the amplifier current noise and the overall noise shape and level tracks the bias resistance. The corner of the noise, however, is being pushed to higher frequencies making the overall noise level higher. The output referred noise for all configurations is shown in Figure 3-23.

Next, the OPA129 is again considered. The noise spectra for the OPA129 configured as a charge amplifier and voltage amplifier are shown in Figure 3-22. It is interesting to note that at this lower bias resistance the shaping of the resistor noise is greatly decreased and the overall level of the resistor noise is now approaching the amplifier voltage noise. The total noise spectra is a combination of these two effects, but is reduce overall in magnitude compared to the implementations in Sections 3.4.3.1 and 3.4.3.2. The output referred noise for all configurations is shown in Figure 3-24.

Again, the signal to noise ratio is the ultimate determining factor for choosing an interface topology. The signal to noise ratio for the AD8022 implementations and the OPA129 implementations are shown in Figure 3-25.
Figure 3-21. The noise spectra of an AD8022 interfaced with a nominal capacitance of 10pF at 1 MHz configured as A) charge amplifier and B) a voltage amplifier.
Figure 3-22. The noise spectra of an OPA129 interfaced with a nominal capacitance of 10pF at 1 MHz configured as A) charge amplifier and B) a voltage amplifier.
Figure 3-23. The noise spectra of the AD8022 configured as a voltage amplifier and current amplifier for multiple bias resistances to interface with a transducer with a nominal capacitance of 10pF.

Figure 3-24. The noise spectra of the OPA129 configured as a voltage amplifier and current amplifier for multiple bias resistances to interface with a transducer with a nominal capacitance of 10pF.
Figure 3-25. The signal to noise ratio for multiple implementations of interface circuitry constructed to interface with a transducer with a nominal capacitance of 10pF with A) the AD8022 and B) the OPA129.
While it appears that charge amplifiers again are the correct choice, the lowest bias resistance implementation of the voltage amplifier gains ground to again be comparable to a charge amplifier. This demonstrates the fundamental tipping point of the tradeoff between parasitic insensitivity and lowered noise floor. The same trade-offs are seen in Figure 3-26, showing the signal to noise ratio for the OPA129.

### 3.4.3.4 Conclusions and practical considerations

From Sections 3.4.3.1 through 3.4.3.3 there are demonstrated instances where both topologies are required. For cases where the nominal sensor capacitance is much lower than the parasitic input impedance of an amplifier a charge amplifier is the appropriate interface. If the nominal sensor capacitance is on the order of or greater than the parasitic input impedance of an amplifier, then the choice of interface topology is highly dependent on the amplifier current noise and the frequency of interest. There are also practical implications that can drive the choice of interface topology.

The passive components required to implement either of these topologies and the physical implementation of the circuit greatly impact the overall performance. If implemented in a printed circuit board stray capacitance in layout and the tolerance of the external passive capacitors and resistors must be considered. For simplicity in implementation and given prior efforts resulting in a nominal capacitance varying between 1.5 pF and 16.8 pF, a voltage amplifier implemented with an AD8022 and a bias frequency of 1 MHz is the appropriate interface.

### 3.5 Open-loop Interface Circuitry Topologies

There are two distinct categories of interface circuitry, continuous-time, also referred to as analog, and discrete-time. Discrete-time systems are characterized by
the presence of one or more clock signals that are used to discretize the signal being processed by the interface circuit before it reaches a traditional data acquisition system. Realistically, all signals are discrete-time at some point, as any measurement system includes a digital analysis component, but a continuous-time system refers to the signal conditioning before digitization during data acquisition.

3.5.1 Continuous-Time Implementation

There are two approaches to continuous-time implementation of capacitive interface circuitry, direct interface and synchronous modulation and demodulation (synch MOD/DMOD). Direct interface, as the name implies, is a simple “read-out” of the sensor output, while synch MOD/DMOD involves at least one stage of frequency translation. This section will discuss the tradeoffs of both approaches.

Direct interface is achieved by interfacing the capacitive transducer with either a voltage follower or charge amplifier, as shown in 3.2.1 and 3.2.2 respectively. The choice between a voltage amplifier and charge amplifier is reliant on the nominal capacitance of the system and whether that nominal capacitance will be overwhelmed by the inherent parasitic capacitances. Additionally, the noise characteristics must be considered given the signal level at the output of the transducer and the required system signal to noise ratio.

The largest drawback of a direct interface system is the system output given a mean capacitance shift. As discussed in 3.2.1 and 3.2.2 the output of a capacitive half-bridge is undefined if there is no frequency content, and therefore does not function at dc. If the bias signal provided to the bridge is a dc voltage, then any fluctuating input will be directly transduced. Assuming a voltage buffer configuration is used, due to the
bias resistor, a mean displacement will have a transient output voltage that will decay with the time constant formed by the bias resistance and device capacitance,

\[ V_{\text{out}} = V_{\text{dc bias}} \frac{2\Delta C e^{-t/Rpc}}{2C_0 + C_p + C_i}. \]  
(3-22)

The solution to this is to apply an ac bias to the bridge making the output signal

\[ V_{\text{out}} = V_{\text{ac bias}} \frac{2\Delta C}{2C_0 + C_p + C_i}, \]  
(3-23)

where \( V_{\text{bias}} \) is a sinusoidal signal. This produces an amplitude modulated (AM) signal at the output, where the bias frequency is what is traditionally referred to as the carrier frequency. This process of translating to a higher frequency is referred to as “up-conversion”.

This technique is referred to as synchronous modulation/demodulation (synch MOD/DMOD) and will be fully outlined in Section 3.7. While the up-converted sensor output is adequate, some applications, such as feedback for flow control, require the base-band sensor information. This requires a down-conversion stage that will translate the information back to the frequencies of the flow dynamics. This approach has been used previously in the development of microphones for infrasound, accelerometers, and other low frequency acoustic applications [50–53].

3.5.2 Discrete-Time Implementation

Integrated circuits are implemented to measure capacitance using digital techniques without using feedback switched capacitor [54–56]. Due to the noise characteristics of MOS switches continuous time sensing, particularly of small capacitance values, has better overall system noise characteristics [57]. These noise sources is mitigated by correlated double sampling, or chopper stabilization [58], [59].
3.6 Closed-loop Interface Circuitry Topologies

In a closed-loop system the output is fed back to the input and acts as a restoring force on the capacitive transducer to move it back into its nominal position for a given displacement. The restoring voltage required to maintain the equilibrium position is a function of the input shear stress. The application of the restoring force and the system read-out must be multiplexed in time in order to prevent the force feedback from affecting the measurement. The result implementing a closed-loop is increased linearity and possible manipulation of sensor mechanics.

3.6.1 Continuous-Time Implementation

In continuous-time a closed-loop system is implemented by a baseband feedback signal. The separation of the feedback signal and the sensor output is achieved in frequency in order to prevent signal contamination. These are most commonly implemented in capacitive accelerometer interface circuits or capacitive microphone interfaces to improve device linearity and increase bandwidth [60–62].

3.6.2 Discrete-Time Implementation

The most common discrete-time closed-loop system is the sigma delta (ΣΔ), also sometimes referred to as delta sigma, system. Widely available in analog to digital conversion schemes [63], the benefit of a ΣΔ system is the low frequency noise performance. Through oversampling and decimation, the low frequency noise of the system is up converted away from the baseband. This has become standard in data acquisition systems as it improves dynamic range at low frequencies.

Systems using a ΣΔ topology require careful timing to ensure proper operation and control of trace lengths as they require high sampling rates in order to achieve adequate oversampling, particularly for higher bandwidth applications. As they have largely been
implemented as application specific integrated circuits (ASICs), $\Sigma\Delta$ systems have been
extended to post-CMOS MEMS applications due to ease of integration [64], [65]. The
design and implementation of a $\Sigma\Delta$ system for interface with a capacitive transducer
was approached by Kadirvel [66] in a discrete component based implementation. The
overwhelming parasitics and power supply noise, issues that could be mitigated in an
ASIC application, were two of the items Kadirvel found to require improvement. While a
system level optimization, including an ASIC $\Sigma\Delta$ interface, would be an interesting
contribution, it is outside of the scope of this dissertation.

3.7 Synchronous Modulation/Demodulation

With favorable design tolerances allowing for discrete implementation without
compromising circuit performance a synch MOD/DMOD system, such as those
implemented in low frequency microphone and accelerometer applications [50], [51],
[53], [67], will be constructed. There are two basic synch MOD/DMOD approaches; a
mixer based system and an envelope detector.

3.7.1 Mixer Based Implementation

Mixers are non-linear devices that enable frequency translation through the
effective multiplication of two sinusoids [68]. For example, if the sensor is biased with a
signal $f(t) = A \sin(\omega_1 t)$ and the sensor output is $g(t) = B \sin(\omega_2 t)$ where $\omega_2 = \omega_1 - \omega_r$ and $\omega_r$ represents the frequency that the sensor is physically excited. The mixer will
multiply $f(t)$ and $g(t)$ resulting in.

$$f(t)g(t) = AB\cos(\omega_1 t)\cos(\omega_2 t).$$ (3-24)

Recalling the trigonometric identity

$$\cos(X)\cos(Y) = \frac{1}{2}[\cos(X+Y)+\cos(X-Y)]$$ (3-25)
Equation 4.20 is expanded to

\[ f(t)g(t) = \frac{AB}{2} [\cos(\omega_1 t + \omega_2 t) + \cos(\omega_1 t - \omega_2 t)]. \]  

(3-26)

Substituting in the definition of \( \omega_2 \), the baseband information is extracted from higher order effects using analog filtering as the frequency separation between the two signals is twice the original carrier as seen in.

\[ f(t)g(t) = \frac{AB}{2} [\cos(\omega_1 t + \omega_1 t - \omega_1 t) + \cos(\omega_1 t - \omega_1 t + \omega_1 t)] \]

\[ = \frac{AB}{2} [\cos(2\omega_1 t - \omega_1 t) + \cos(\omega_1 t)]. \]  

(3-27)

As mixing is inherently non-linear, higher order harmonics will also be generated, however with careful frequency planning they can fall outside of the signal bandwidth and be removed using analog filters. In the first-generation of this sensor [37], a mixer based approach was attempted using the AD835 4-Quadrant Multiplier, however an apparent dc drift was noticed during experimentation. Analog Devices, the manufacturer of the AD835, has since moved away from mixers derived from the Gilbert Cell mixer architecture, because the Gilbert Cell contains inherent phase and amplitude errors that propagate to the output of the mixer, manifesting as dc errors [69].

For applications where dc information is not required, where the signals are inherently phase locked, or where multiple frequency translations are required a mixer is an elegant solution.

### 3.7.2 Envelope Detector Implementation

An alternate approach to demodulation is the envelope detector [70]. An envelope detector is made up of two main blocks; a rectification block and a filtering block. The
frequency translation that occurs during multiplication in the mixer case is achieved through rectification. Considering an amplitude-modulated signal

\[ x_{Am}(t) = [A+m(t)]\cos(\omega_c t) , \]  

(3-28)

where \( A \) represents a dc shear response combined with any inherent dc offset of the sensor due to mismatches in the bridge, \( m(t) = B\cos(\omega t) \) is the ac wall shear stress response, and \( \omega_c \) is the carrier frequency. The time series of this signal is shown in Figure 3-26 where the modulated signal is in blue and the signal that is to be recovered is in red.

![Figure 3-26. An amplitude modulated signal with 100% modulation depth and the corresponding output of a passive rectification scheme.](image)

Envelope detection is not without design constraints. At the simplest level, rectification is thought of as taking the absolute value of the modulated signal. As the amplitude of the signal being modulated approaches that of the carrier, signal errors in
the rectified signal may result. This is quantified by the modulation index, also referred to as modulation depth [71],

\[
\text{depth} = \frac{\max(m(t))}{A}.
\]  

(3-29)

Figure 3-27. An amplitude modulated signal with 150% modulation depth and the corresponding output of a passive rectification scheme.

As modulation depth increases beyond 100%, rectification will fail to capture the phase inversion, and amplitude and dc errors will occur. Figure 3-26 shows a signal with 100% modulation depth and the resulting rectification output both in blue, superimposed with the original message signal in red. At this limit the message is preserved. Considering a purely oscillating input to a perfectly matched capacitive half-bridge the modulation depth would be infinite. Realistically there are imperfections in the capacitive half-bridge that result in a static dc offset. This results in defined, albeit high, modulation depths. Figure 3-27 demonstrates that at a modulation depth of 150% the
modulated signal with the original message superimposed in red. In order to preserve the phase inversion, the rectification mechanism must also be phase locked to the signal. This means that an active rectification scheme must be implemented. Active rectification is the multiplication of an amplitude-modulated wave, \( x_{AM}(t) \), with a phase locked square wave, \( w(t) \). The resulting multiplication is

\[
x_{AM}(t) \cdot w(t) = \left[ A + m(t) \right] \cos(\omega_c t) \cdot \left( \frac{1}{2} + \cos(\omega_c t) + \frac{1}{3} \cos(3\omega_c t) + \frac{1}{5} \cos(5\omega_c t) + \ldots \right). \tag{3-30}
\]

Implementing the trigonometric identity given in 3.21, Equation 3.27 becomes

\[
x_{AM}(t) \cdot w(t) = \left[ A + m(t) \right] + \left( \frac{5}{6} \cos(2\omega_c t) + \frac{8}{15} \cos(4\omega_c t) + \frac{1}{5} \cos(6\omega_c t) + \ldots \right). \tag{3-31}
\]

![Figure 3-28. An amplitude modulated signal with modulation depth of 150% and the corresponding output of active rectification with no phase error.](image-url)
The result is similar to the result given by the mixing case in that the baseband signal is separated out from the rest of the modulation by at least $2\omega_c$. If the example of 150% modulation depth from Figure 3-28 is rectified using an active rectification scheme the result is shown in Figure 3-29, where the modulated signal is again shown in blue, the message in red, and the rectification signal in black.

As a phase mismatch is introduced between the rectification signal and the modulated signal the rectified signal will appear "less rectified" meaning more harmonics are being generated and fed through. The worst case occurs when the rectification signal and modulated signal are 90 degrees out of phase with one another. At this point the signal does not appear to be rectified at all. This is shown mathematically this makes sense from Equation 3.26 by substituting in a phase shift

$$x_{AM}(t) \cdot w(t) = [A + m(t)] \sin(\omega_c t) \cdot \left( \frac{1}{2} + \cos(\omega_c t) + \frac{1}{3} \cos(3\omega_c t) \right) + \frac{1}{5} \cos(5\omega_c t) + ... \right).$$

(3-32)

Instead of the multiplication of two cosine functions, the result is the multiplication of a sine and cosine. Using the trigonometric identity

$$\sin X \cos Y = \frac{1}{2} \left[ \sin(X - Y) + \sin(X + Y) \right]$$

(3-33)

Equation 3.29 reduces to

$$x_{AM}(t) \cdot w(t) = [A + m(t)] + \left( \sin(2\omega_c t) + \frac{1}{3} \sin(\omega_c t) \cos(3\omega_c t) \right) + \frac{1}{5} \sin(\omega_c t) \cos(5\omega_c t) + ... \right).$$

(3-34)

The message signal is still recoverable, however the filtering requirements will be more stringent due to larger harmonic content and the time series is much less intuitive as
seen in Figure 3-29. Intermediate phase mismatches result in a decreased sensitivity as it results in an attenuating dc offset.

![Graph of modulated and rectified signals](image)

Figure 3-29. An amplitude modulated signal with modulation depth of 150% and the corresponding output of active rectification with a 90 degree phase error.

### 3.8 Generalized Interface Circuit

Given the tradeoffs discussed in this chapter, the system shown in Figure 3-30 has been designed and implemented. At the points along the signal path the color coding used in Section 3.5 has been preserved, so a blue shape means that is a modulated signal, a red shape means that is the message of interest. The signal has been shown at multiple points along the circuit for further illustration.
The voltage follower will be co-located with the sensor die in order to reduce the parasitics associated with cabling going to and from the die and to condition the sensor impedance down to mitigate electromagnetic interference. The rest of the circuitry is located an arbitrary distance from the sensor in order to reduce restrictions on its size. An active rectifier was chosen due to its robust response to phase errors.

This chosen topology isolates the majority of the circuitry from interfacing directly with the sensor. The only point where the sensor is loaded by the circuit is at the node between the common electrode of the sensor and the input to the voltage follower. As described in Section 3.2.1 the voltage follower will have finite input impedance that is modeled as a parallel resistance and capacitance. In this case, the parallel input capacitance will act as an attenuation factor to the sensor, as derived in Appendix C. Combining these effects with Equation 2.3.2 derived in Section 2.3.1 the expected output voltage given an input shear force becomes

$$V_o = V_b H_{gap} \left( \frac{C_{10} - C_{20}}{C_{10} + C_{20} + (C_p + C_t)(1 - \kappa^2)} \right) \delta(\tau_w) \frac{g_{b1}}{g_{b1}},$$

(3-35)
where $C_{10}$ and $C_{20}$ are the nominal device capacitances, $C_p$ are the device parasitics, $C_i$ is the input capacitance of the amplifier, $V_b$ is the bias voltage applied to the sensor, $H_{gap}$ is the attenuation due to the secondary gap between comb fingers, $\kappa$ is the coupling coefficient, $g_{01}$ is the dimension of the primary gap, and $\delta(\tau_w)$ is the deflection of the floating element due to an input shear stress.

The circuit is broken up into three main blocks; modulation, demodulation, and demodulation control. The specifics of each block are discussed in Sections 3.8.1, 3.8.2, and 3.8.3.

3.8.1 Modulation

The modulation block creates two out of phase sinusoids for biasing the sensor and provides the basis of the demodulation control signal. The details associated with the demodulation control are discussed in Section 3.8.3.

![Diagram](image)

Figure 3-31. A generalized schematic of the bias generation for modulation indicating the original sinusoid at the input and resulting in two out of phase sinusoids at each sensor bias node.

In order to evaluate the system performance the intended functionality of the block and the noise considerations of the block must be evaluated. The primary function of creating two out of phase sinusoids is achieved by two blocks; one for inversion and one for buffering. This nominally creates a $180^\circ$ phase shift between the two bias signals applied to the sensor such that Sensor Bias 1 = $A \sin(\omega t)$ and
Sensor Bias 2 = -Asin(ωt), as shown in Figure 3-31. Applying these biases to the
generalized sensor impedance bridge, seen in Figure 3-33, the output voltage of the
sensor is

\[ V_{out} = \frac{C_2 A \sin(\omega t) - C_1 A \sin(\omega t)}{C_1 + C_2}. \]  

(3-36)

Assuming that \( C_1 = C_0 - \Delta C \) and \( C_2 = C_0 + \Delta C \), this becomes

\[ V_{out} = \frac{\Delta C}{C_0} A \sin(\omega t). \]  

(3-37)

As the inverter and buffer may have slight phase offsets, the impact of phase error must be considered. To account for phase errors in bias generation the second bias becomes Sensor Bias 2 = -Asin(ωt + φ). The resulting sensor output is

\[ V_{out} = \frac{(C_0 + \Delta C) A \sin(\omega t) - (C_0 - \Delta C) A \sin(\omega t + \phi)}{2C_0}. \]  

(3-38)

Simplifying and assuming that \( \phi \) is very small Equation 3.37 becomes

\[ V_{out} = \frac{\Delta C}{C_0} A \sin(\omega t) + \frac{\phi A}{2} \cos(\omega t), \]  

(3-39)

showing that while the sensitivity of the device is not affected a dc offset is generated.

Figure 3-32. The circuit representation of the sensor for an analysis of the errors associated with the modulation block.
The addition of a variable resistor in the inverting amplifier driving Sensor Bias 2 allows for some compensation for dc signals generated by non-ideal sensor impedances. Consider \( C_1 = C_0 - \Delta C \) and \( C_2 = 1.5C_0 + \Delta C \) in Figure 3-32. Equation 3.36 becomes

\[
V_{\text{out}} = \frac{0.5C_0 + 2\Delta C}{2.5C_0} A \sin(\omega t) = \frac{0.5}{2.5} A \sin(\omega t) + \frac{2\Delta C}{2.5C_0} A \sin(\omega t). \tag{3-40}
\]

This shows a dc offset term generated by the impedance mismatch along with a slight attenuation in device sensitivity. If the bias is changed such that

\[
\text{Sensor Bias 2} = -\beta \sin(\omega t) \quad \text{and} \quad \beta = 1.5
\]

equation 3.39 is now

\[
V_{\text{out}} = \frac{(1.5C_0 + \Delta C)A \sin(\omega t) - (C_0 - \Delta C)\beta A \sin(\omega t)}{(1.5C_0 + \Delta C) + (C_0 - \Delta C)} \tag{3-41}
\]

or

\[
V_{\text{out}} = \frac{[(1.5C_0 + \Delta C) - (1.5C_0 - 1.5\Delta C)]A \sin(\omega t)}{(1.5C_0 + \Delta C) + (C_0 - \Delta C)} = \frac{2.5\Delta C}{2.5C_0} A \sin(\omega t). \tag{3-42}
\]

Comparing this result to Equation 3.36, where the capacitances are balanced, the nominal sensitivity is produced without additional dc offset. The danger of having this adjustability available to the end user of the instrument is that changing this gain beyond this nominal point results in a change in device sensitivity. Ideally this gain value will be selected during calibration and then set for the lifetime of the sensor system.

As the circuit topology fits the needs of the system, the implementation of this topology will decide the ultimate system performance, specifically the noise contributions of this design.

There are three noise sources in the modulation portion of the circuit; noise associated with the bias sinusoid, noise associated with the buffering block, and noise
associated with the inverting block. The noise associated with the bias sinusoid is negligible as it is a common mode signal to the output of the capacitive bridge. The noise of the inverting and buffering blocks is uncorrelated and will combine at the output of the sensor. The noise due to circuitry at the output of the sensor is

\[ v_{\text{MOD}}^2 = v_{\text{MOD buffer}}^2 + \beta v_{\text{MOD inverter}}^2. \]  

(3-43)

### 3.8.2 Demodulation

For the purposes of this work, the demodulation block contains the signal path from the output of the sensor to the read out of the base band signal. This includes signal conditioning pre-demodulation and the demodulation itself.

![Block Diagram of the Demodulation Portion of the Synch MOD/DMOD System](image)

Figure 3-33. A block diagram of the demodulation portion of the Synch MOD/DMOD system, with sub-sections indicated in dashed boxes.

The chosen demodulation technique is envelope detection that is realized using an active rectifier [72]. For simplicity, the demodulation block as a whole is split into separate sections: signal conditioning before rectification, rectification, and signal conditioning after rectification. Then the noise model of each section is outlined and combined for a total noise model of the demodulation block. A high-level block diagram
of the demodulation circuitry is shown in Figure 3-33 with indications of the separation between the operational sections.

### 3.8.2.1 Signal conditioning before rectification

As the sensor is a high impedance device immediate impedance buffering is critical to prevent electromagnetic interference and signal attenuation. A unity gain amplifier, discussed in 3.4.1, is implemented and co-located with the sensor die. The rest of the demodulation block is then located on a PCB away from the testing area. The incoming signal is ac coupled onto the board and then band pass filtered with the pass band centered at the carrier frequency. The unity gain amplifier and band pass filter make up the signal conditioning before rectification block. The band pass filter is realized using a low pass filter and high pass filter in series. The details of the filters result from the selection of bias frequency, however generally the low pass filter needs to be of sufficiently high order to filter out the second harmonic of the bias frequency and the high pass filter is of lower order as it is meant to filter out dc offsets or noise associated with electromagnetic interference from speakers, fan drivers, or other wind tunnel related sources. A generalized block diagram of this block is shown in Figure 3-34. In this case the low pass filter portion of the band pass filter is shown as the first. The high pass filter portion could also come first. The implications of this choice will be explained in Sections 3.8.4 and 3.8.5.

There are three sources of noise associated with this block; the noise from the unity gain amplifier, the noise from the low pass filter, and the noise from the high pass filter. There is also the opportunity to add gain to the system at each of the filter blocks, that are represented as $G_1$ and $G_2$. The implementation of the filter stages will set the
noise contributions, for simplicity they will be assumed to be voltage noise dominated and are represented by \( v_{n_{LPF}} \) and \( v_{n_{HPF}} \) for the low pass and high pass portions, respectively. The noise at the input to the rectification is

\[
v^2_{nDMOD1} = G_2^2 \left( G_1^2 \left( v^2_{nMOD} + v^2_{buffer} + v^2_{n_{LPF}} \right) + v^2_{n_{HPF}} \right). \tag{3-44}
\]

From this it is seen that the initial gain stage of the demodulation, \( G_1 \), has the greatest impact on the overall signal to noise ratio of this stage as it is further amplified by the second gain stage, and changes the magnitude of the noise contributed by the modulation section, the buffer, and the first filter stage.

Figure 3-34. The block diagram of the signal conditioning before rectification block demonstrating the construction of a band-pass filter through the series combination of a low-pass filter and a high-pass filter.

**3.8.2.2 Rectification**

Rectification is achieved by switching between two out of phase versions of the filtered sensor output. The switching is synchronized to one of the bias signals. The implementation of this synchronization is discussed in 3.8.2.3 that preserves the phase of the original flow information. Two out of phase versions of the source signal are generated using inverter and buffer blocks, like those used in Section 3.8.1, as shown in Figure 3-35. The rectification is of the signal is performed by an analog double-pole-single-throw switch. This switch-based demodulation is explained in Section 3.7.2.
This frequency translation works in two ways; it demodulates the high frequency sensor data back down to the baseband and additionally is up-converts the low frequency noise of the system to the modulation frequency. Up until this point the low frequency noise contributions have been neglected in the analysis of noise due to this effect. The noise of the inverter block, buffer block, and switch will be subject to this but all stages from the output of the switch on will have low frequency noise contributions. The noise associated with the inverter block is higher than the noise of the buffer block, as they use the same base amplifier, so for simplicity the noise of the inverting channel will be considered as the noise added by the buffer and inverter blocks. The noise at the output of the switch is

\[ v_{nDMOD2}^2 = v_{nDMOD1}^2 + v_{inverter}^2 + v_{switch}^2 \]  

(3-45)

where \( v_{inverter}^2 \) is the voltage noise of the inverter block and \( v_{switch}^2 \) is the voltage noise of the switch. Ideally the control signal is completely decoupled from the switch signal path, so any noise on the demodulation control signal is not considered in the final noise formulation. This assumption will be re-evaluated when the real switch is selected as part of Sections 3.9 and 3.10. The derivation of the control signal is described in Section 3.8.2.3.

Figure 3-35. The block diagram of the rectification block including a phase inversion stage and a DPST switch.
While the noise of the switch is fairly straightforward, it is not the sole driver for switch selection. The dominant non-ideality in a switch is the non-zero switching time, meaning the period between the triggering of the switch and the switch being fully conducting or non-conducting. There are two metrics associated with this effect; the time it takes for the switch to turn on, \( t_{on} \), and the time it takes for the switch to turn off, \( t_{off} \). Each of these are defined as the delay between the logic input reaching 50\% of the maximum logic voltage and the output voltage of the switch reaching 90\% of the maximum output voltage on that switch [73]. This timing is demonstrated in Figure 3-36.

![Figure 3-36. An illustration of switch timing showing the various time-scales used as metrics for switch selection.](image)

These timing considerations impact switch choice more profoundly than the noise of the switch. In the active envelope detector the switch will change states at two times the bias frequency. If the combined switch transition times approach the total time the switch needs to be on, then the rectified signal is attenuated by the switch.
In general, this switching time is dependent on the size of the transistor used to implement the switch and the load on the output of the switch. The larger the transistor used as the switch path, the larger the capacitance associated with the transistor, and the longer this transition period is. At the same time, the resistance of the switch is inversely proportional to transistor size. With these competing requirements there are trade-offs between bias frequency selection and the noise contribution of the switch. Ultimately, order of magnitude of the switch noise is not a dominant source of noise in the system.

### 3.8.2.3 Demodulation control

The demodulation control block provides a transistor-transistor logic (TTL) signal to the switch that rectifies the incoming sensor signal. This TTL signal is derived from one of the sensor bias signals in order to simplify the synchronization between modulation and demodulation. This signal derivation is broken into three blocks; a buffer, a regulator to step down the voltage, and an inverter. This is shown in Figure 3-37. The first buffering stage is to decouple the bias signal from the conversion to a TTL level signal, preventing feedback into the sensor bias. The regulator stage then steps the bias signal down by clipping it into a TTL square wave. Finally, the square wave is buffered by a logic inverter to drive the rectification switch.

![Figure 3-37. A block diagram representation of the demodulation control circuitry.](image)

Following rectification, the signal passes through one additional circuit section in order to reclaim the baseband flow information.
3.8.2.4 Signal conditioning after rectification

After rectification, the signal is low pass filtered to complete the demodulation. The order of this filter is dependent on the difference between the sensor bandwidth and choice of bias frequency. The noise characteristics of this portion of the circuit are dependent solely on the component chosen to implement the low pass filter. The noise at the output of this stage is

\[
\nu_{nDMOD3}^2 = \nu_{nDMOD2}^2 + \nu_{LPF}^2
\]

where \( \nu_{LPF} \) is the voltage noise associated with the low pass filter implementation. This concludes the noise added by the direct signal path and now the total noise model is completed.

3.8 Generalized Noise Model

The final noise model of the generalized system is broken into two components, the noise from the modulation and the noise from the demodulation. These are expressed as

\[
\nu_{nMOD}^2 = \nu_{nMODbuffer}^2 + \beta\nu_{nMODinverter}^2
\]

and

\[
\nu_{nDMOD}^2 = G_2^2 \left( G_1^2 \left( \nu_{nMODth}^2 + \nu_{buffer}^2 + \nu_{nLPF}^2 \right) + \nu_{n_eff}^2 \right) + \nu_{inverter}^2 + \nu_{switch}^2 + \nu_{LPF}^2
\]

respectively. As the sensor is differential, noise sources that are common to both bias signals are rejected. The remaining noise is fed through into the demodulation and is represented as \( \nu_{nDMOD}^2 \). There is no differentiation in the demodulation stages, so the power of each noise source feeds through to the output. Assuming that each stage has a noise contribution of equal order the dominant sources are those that are multiplied by the most gain, being the noise of the buffer amplifier that follows the sensor and the
noise of the first filter stage. Though this filter is identified as the low-pass filter stage in this equation, recall that the order of the low-pass and high-pass stages that make up the band-pass filter is not important and they may be switched in order to minimize total noise based on the final parts chosen for implementation.

The synch MOD/DMOD system was realized in two stages. Initially the synch MOD/DMOD system is constructed alone as a proof of concept. Bench-top power supplies and function generators are used for the various required bias voltages. Finally the synch MOD/DMOD system is realized with the majority of these external sources built in so only a single power supply is required for system support. The proof of concept construction and final system are described in Sections 3.9 and 3.10, respectively.

3.9 First-Generation Synch MOD/DMOD

Initially, the system is constructed on a single printed circuit board (PCB) requiring a dual voltage bench top power supply and bench-top function generator to run. The bias frequency is set at 100 kHz, that is more than a decade above the sensor resonance of 5 kHz but still low enough to be monitored on spectrum analyzers and oscilloscopes available in the laboratory. The circuitry is again broken into multiple subsections; modulation, demodulation, rectification, and rectification control. Each subsection is described in detail before a final parts list and conclusions are presented.

3.9.1 Modulation

The sensor bias circuit consists of an external sinusoidal generator, two phase shift circuits, a buffer, and an inverter, configured as shown in Figure 3-38. The buffer and inverter portions of the circuit provide the 180° phase shift between the two bias
signals. Realistically the phase between the buffer and inverter blocks will not be exactly $180^\circ$. The phase adjust circuitry was used to compensate for this small offset, however unmatched cabling and impedance mismatches in the sensor generated during fabrication will also contribute in the same manner. The phase adjust circuitry is only used to give the best-case signal at the Synch MOD/DMOD circuit board output.

In order to characterize the noise performance of the modulation block, a noise model for each component is derived and then cascaded. The equivalent noise circuit and output referred noise for a buffer is explained in 3.4.1. This section provides equivalent noise circuits and analysis for the phase adjust and inverter components and provide an expression for the noise of the entire block.

Figure 3-38. A schematic of the modulation portion of the Synch MOD/DMOD system showing the phase adjustability and gain control to eliminate offset in the sensor output.

Following the analysis outlined in 3.4.1, the noise circuit of an inverting amplifier is shown in Figure 3-39. The resulting output referred noise is
\[ v_{out}^2 = \left(1 + \frac{R_2 + R_{adj}}{R_1}\right)v_n^2 + \left(\frac{i_n^2}{R_2} + \frac{4kT}{R_{adj}}\right)(R_2 + R_{adj}). \quad (3-49) \]

The analysis of the phase adjust block is complicated by the differential topology of the circuit. Instead of lumping the amplifier voltage and current noise sources the differential inputs must each have their own associated noise network. In this case, \( v_{n1} \) and \( i_{n1} \) are associated with the inverting input to the amplifier while \( v_{n2} \) and \( i_{n2} \) are associated with the non-inverting input. They are related to the generalized noise model [46] as

\[ v_n = \sqrt{v_{n1}^2 + v_{n2}^2} \quad (3-50) \]

and

\[ i_n = i_{n1} = i_{n2}. \quad (3-51) \]

![Figure 3-39. Equivalent noise circuit of an inverting amplifier including the input referred noise of the amplifier as well as thermal noise sources associated with resistances.](image)

The full noise circuit, including this differential noise source approach, is shown in Figure 3-40. The output referred noise in this configuration is

\[ v_{out}^2 = \left(1 + \frac{R_2}{R_1}\right)^2 \left(v_{n2}^2 + v_p^2 + i_{n2}^2 Z_p^2 + v_{n1}^2\right) + \left(\frac{R_2}{R_1}\right)^2 v_{R1}^2 + v_{R2}^2 + i_{n1}^2 R_2^2 \quad (3-52) \]

where
\[ Z_p = \frac{R_3}{C_{adj}} \] (3-53)

and

\[ \sigma^2_p = \frac{kT}{C_{adj}} \] (3-54)

The noise added by the function generator is not considered in this model as it is not a designed portion of the Synch MOD/DMOD system. Additionally, as it is a source to two paths that are then differenced, it is considered a common mode source. The final output due to noise at the function generator is a function of the gain stage of the modulation circuit and the sensor imbalance. Assuming a perfectly matched sensor the output noise due to function generator non-idealities is zero.

Figure 3-40. Equivalent noise circuit of a phase adjust block where the amplifier noise is represented by differential input current and voltage sources.

The total noise model of the modulation block is the summation of uncorrelated noise sources due to each component of the modulation block. The full circuit, with labeled components, is shown in Figure 3-41. The voltage \( V_{c1} \) is the cascade of a phase adjust block with a voltage inverter with gain and is expressed as
\[ v_{c1}^2 = \left( 1 + \frac{R_{15}}{R_{14}} \right)^2 \left( v_{nA1}^2 + \frac{kT}{C_{adj1}} + i_{nA1}^2 \left( \frac{R_{13}}{j\omega C_{adj1} R_{13} + 1} \right) \right)^2 \left( \frac{R_{18} + R_{adj}}{R_{22}} \right) \]
\[ + \left( 1 + \frac{R_{15}}{R_{14}} \right)^2 4kTR_{14} + 4kTR_{15} + i_{nA1}^2 R_{15}^2 \]
\[ + \left( 1 + \frac{R_{18} + R_{adj}}{R_{22}} \right) v_{nA2}^2 + \left( i_{nA2}^2 + \frac{4kT}{R_{18}} + \frac{4kT}{R_{adj}} \right)(R_{18} + R_{adj}). \]

(3-55)

The voltage \( V_{c2} \) is the cascade of a voltage buffer with a phase adjust block and is

\[ v_{c2}^2 = v_{nA3}^2 + \left( 1 + \frac{R_{19}}{R_{21}} \right)^2 \left( v_{nA4}^2 + v_p^2 + i_{nA4}^2 Z_p^2 \right) + \left( \frac{R_{19}}{R_{21}} \right)^2 v_{R21}^2 + v_{R19}^2 + i_{nA4}^2 R_{19}^2 \]

(3-56)

where

\[ Z_p = \frac{R_{20}}{C_{adj2}} \]

(3-57)

and

\[ v_p = \frac{kT}{C_{adj2}}. \]

(3-58)

These two noise models will the propagated through to the sensor output to give

\[ v_{mod}^2 = \left( 1 + \frac{R_{15}}{R_{14}} \right)^2 \left( v_{nA1}^2 + \frac{kT}{C_{adj1}} + i_{nA1}^2 \left( \frac{R_{13}}{j\omega C_{adj1} R_{13} + 1} \right) \right)^2 \left( \frac{R_{18} + R_{adj}}{R_{22}} \right) \]
\[ + \left( 1 + \frac{R_{15}}{R_{14}} \right)^2 4kTR_{14} + 4kTR_{15} + i_{nA1}^2 R_{15}^2 \]
\[ + \left( 1 + \frac{R_{18} + R_{adj}}{R_{22}} \right) v_{nA2}^2 + \left( i_{nA2}^2 + \frac{4kT}{R_{18}} + \frac{4kT}{R_{adj}} \right)(R_{18} + R_{adj}) \]
\[ + v_{nA3}^2 + \left( 1 + \frac{R_{19}}{R_{21}} \right)^2 \left( v_{nA4}^2 + v_p^2 + i_{nA4}^2 Z_p^2 \right) + \left( \frac{R_{19}}{R_{21}} \right)^2 v_{R21}^2 + v_{R19}^2 + i_{nA4}^2 R_{19}^2. \]

(3-59)
Figure 3-41. Modulation circuit with labeled components for use in noise analysis.

For the purposes of this chapter inherent transducer noise is neglected. This equivalent noise model for the output of the sensor is used as an input noise signal for the demodulation sections.

3.9.2 Demodulation

Again, the demodulation block is broken down into several smaller blocks; signal conditioning before rectification, rectification, rectification control, and signal conditioning after rectification. Each section is described individually in the following sections.

3.9.2.1 Signal conditioning before rectification

For this proof of concept implementation, the demodulation block is constructed as outlined in Section 3.8, meaning that before modulation the band-pass filter is constructed by cascading a low-pass filter with a high-pass filter. The band pass filter is
realized by using two different analog filters, a single-pole high pass filter and a fourth-order low pass Chebyshev filter. The justification for the imbalance of the two halves of the filter lies in the predicted harmonic content of the system. The bandwidth of the high-pass filter slightly exceeds the sensor bandwidth to ensure that the entirety of the sensor output signal is within the flat band region of the filter. A detailed block diagram of this block is shown in Figure 3-42.

Below the carrier frequency spurious frequencies are generated primarily by electromagnetic interference, whether that be 60Hz line noise, a mechanical fan in a wind tunnel, or any other power based low frequency source. As the carrier is ideally in the hundreds of kilohertz or higher the frequency separation is significant, relaxing the requirements on the filter order of this stage. The low pass portion of the band pass filter has significantly more stringent requirements.

Figure 3-42. Detailed drawing of the signal conditioning path before rectification in the demodulation block.

Any nonlinearities in the modulation frequency or higher order mixing products will appear above the carrier frequency, starting at the second multiple of the carrier
frequency. The higher order low pass filter ensures that regardless of the harmonic content of the oscillator chosen as a modulation signal, the harmonics will be sufficiently rejected before demodulation. The chosen component, the LT1563 by Linear Technologies, was selected as due to its configurability and low noise floor. It also allows for the addition of gain by a single resistor selection. Adding gain immediately after the signal is read in will increase the overall signal to noise ratio of the system by making the noise to this point dominant over the other noise sources in the demodulation signal path. This concept is seen by examining the noise characteristics of this demodulation block section.

In this case, there are three sections that make up this block; a unity gain amplifier, a low pass filter, and a high pass filter. These are shown in Figure 3-43 along with component labels.

Figure 3-43. The demodulation before rectification block with components labeled for noise analysis.

The noise contributions of a unity gain amplifier are fully described in Section 3.4.1. The noise contribution due to the unity gain amplifier is repeated here for
simplicity. The input parasitics of the amplifier are considered though they are not shown in 3-27. The noise at the output of the unity gain amplifier block is

$$v_1^2 = v_{mod}^2 + v_{nA5}^2 + \left(\frac{1}{i_{nA5}j\omega(C_1 + C_p + C_1 + C_2)}\right)^2 + \frac{4kTR_b}{(j\omega R_b(C_1 + C_p + C_1 + C_2))^2}. \quad (3-60)$$

The noise of the low pass filter block is largely dependent on the filter implementation. As described in Section 3.8.2.1 the chosen component is an LT1563 by Linear Technologies. It has a specified voltage gain, $G$, and input voltage noise, $v_{in}$, given by the manufacturer datasheet. Considering the addition of the noise in the system from previous sources and the filter gain the noise at node $v_2$ is

$$v_2^2 = G^2 \cdot \left[ (v_{in})^2 + v_1^2 \right]. \quad (3-61)$$

The final portion of this section is the single pole high pass filter. The noise of this filter has four components; the thermal noise of the feedback resistance, the thermal noise of the resistance at the inverting input to the amplifier, the amplifier voltage noise, and the amplifier current noise. The total noise added by the high pass filter block is

$$v_{HPF}^2 = i_{nA6}^2 R_{30}^2 + v_{R_{30}}^2 + (v_{R_{29}}^2 + v_{nA6}^2) \cdot \frac{j\omega R_{30} C_{21}}{1 + j\omega R_{29} C_{21}}. \quad (3-62)$$

The total noise up to this point in the system is

$$v_3^2 = G^2v_{mod}^2 + G^2v_{in}^2 + G^2v_{nA5}^2 + G^2 \left(\frac{1}{i_{nA5}j\omega(C_1 + C_p + C_1 + C_2)}\right)^2 + \frac{G^24kTR_b}{(j\omega R_b(C_1 + C_p + C_1 + C_2))^2} + i_{nA6}^2 R_{30}^2 + v_{R_{30}}^2 + (v_{R_{29}}^2 + v_{nA6}^2) \cdot \frac{j\omega R_{30} C_{21}}{1 + j\omega R_{29} C_{21}}. \quad (3-63)$$
3.9.2.2 Rectification

Signal rectification is achieved by using a single pole double throw (SPDT) solid-state switch that alternates between the filtered signal and an inverted version of the filtered signal. The details of the switch control will be discussed in Section 3.8.2.3, for the purposes of this section assume that the switch control is a 50% duty cycle square wave that is phase locked to Sensor Bias 1. A schematic of this section of the demodulation block is shown in Figure 3-44.

![Figure 3-44](image)

Figure 3-44. A detailed drawing of the rectification portion of the demodulation block.

Following the initial signal conditioning section the signal is fed into a unity gain buffer, creating the signal that will be passed through the rectifier during the positive portion of the demodulation control signal. The initial signal conditioning section also feeds into an inverter followed by a unity gain buffer, creating the signal that will be passed through the rectifier during the negative portion of the demodulation control signal. The resulting output is a rectified version of the input signal where the rectification direction, whether the signal is rectified in the positive direction or negative
direction, depends on the phase relationship between the input signal and the demodulation control.

In this case, the signal is split into two pathways with different noise characteristics. The worst case for noise is the inverting signal path so that will be considered the sole signal path for the purposes of analysis for simplicity. This means that noise contributions due to A7, shown in Figure 3-45, will be neglected, assuming it is implemented using the same components as A9. The total noise from this rectification portion is subdivided into three noise sources; noise due to the inverting amplifier implemented with A8, the noise due to the buffer amplifier A9, and noise associated with the switch.

![Diagram of signal conditioning and rectification](image)

Figure 3-45. The rectification portion of the demodulation circuit with the components labeled for noise analysis.

The noise associated with the inverting amplifier is a combination of the inherent noise of the op amp, A8, and the thermal noise of the two resistors. The noise at the output of the inverting amplifier is
The noise contributions of the buffer amplifier, A9, have already been outlined making the noise at the input to the rectifying switch

\[ v_5^2 = v_4^2 + v_{nA9}^2. \]  (3-65)

The noise associated with the switch is significantly more complicated as it requires knowledge of both the way the switch is implemented and the effect of switching on noise characteristics. The switch is implemented using CMOS for maximum isolation of the drive signal from the sensor signal path. In order to achieve switching of both negative and positive voltages a CMOS switch, also called a transmission gate, is used [72]. Transmission gates are typically used in sample and hold circuits or switched capacitor filters and are implemented by parallel nMOS and pMOS transistors as shown in Figure 3-46.

![Figure 3-46. The circuit schematic of a transmission gate showing the parallel nMOS and pMOS transistors.](image)

The noise of a MOSFET is made up of two components, a \(1/f\) low frequency noise component and a thermal noise floor. This is expressed as an input referred noise for the FETs use as an amplifier component and

\[ \frac{v_i^2}{\Delta f} = 4kT \frac{2}{3} \frac{1}{g_m} + \frac{K_i}{WLC_{ox}} f, \]  (3-66)
where $g_m$ is the FET transconductance, $K_f$ is a property of the gate oxide, $W$ and $L$ describe the physical gate size, and $C_{ox}$ is the oxide capacitance [74]. In this case the flat band noise of the switch is the contributing term, so the noise at the output of the switch is

$$n^2 = n_s^2 + 4kT \frac{2}{3g_m}.$$  

(3-67)

Any noise contributions present in the drive signal are significantly attenuated due to the MOS implementation of the switch, however they are described for completeness.

### 3.9.2.3 Rectification control

A detailed diagram of the rectification control circuitry is shown in Figure 3-47. Functionally, Sensor Bias 1 is pulled from the modulation block and fed through a unity gain buffer, creating an isolated version of this sinusoid to generate the TTL control signal. This buffered signal then passes through a phase adjustment circuit allowing for user control of the rectification. The phase-shifted sinusoid is the input into a comparator, creating a 10V/-10V square wave. The comparator output is then tied to a Zener regulator that regulates these voltages down to 0V and 5V. Functionally, when the sinusoid is negative, the combination of comparator and Zener regulator outputs 0V, when it is positive it outputs 5V. This ideally creates a 50% duty cycle square wave. Finally, the square wave is fed through a standard logic inverter. The logic inverter provides an additional level of noise rejection, as the input to the inverter acts as a switch control, where the switch selects between the 5V rail and the ground of the system rather than using the derived signal directly trigger the demodulation switch.
Figure 3-47. The demodulation control block.

The rectified signal that is produced by this control and the circuitry described in the previous section passes into a final signal conditioning block in order to reclaim the baseband flow information. This final rectification block is described in the next section.

3.9.2.4 Signal conditioning after rectification

As described in 3.8.2.4 in order to reclaim the baseband information the rectified signal is low pass filtered. The chosen filter is an LTC1563 configured for a cutoff frequency of 20 kHz. This sets the total available sensor system bandwidth for this implementation, but is extendable by changing the supporting resistor values. The LTC1563 is chosen as the cutoff frequency is determined by a single resistor, so it is adjustable without reconfiguring multiple components or layout after it is implemented. The LTC1563 has low dc offset and when configured as a fourth-order low-pass filter has 0.5 dB pass-band ripple, making it ideal for baseband applications. The noise contributed by this portion of circuitry is the noise of low pass filter. No gain is added at this point, as it would provide no benefit in terms of signal to noise ratio. The schematic of the low pass filter is shown in Figure 3-48. Combined with the previous sections, a full schematic, parts list, and noise model is constructed and is shown in Appendix E.
3.9.3 Summary of the First-Generation Synch MOD/DMOD

Following the first-generation circuitry fabrication the system is characterized. In order to see the impact of noise sources in the modulation portion of the synch MOD/DMOD system, the noise floor of the system is characterized with a sensor attached. The noise floor is shown in Figure 3-49. There is a clear low frequency component, that is dominated by the final low-pass filter stage. The overall noise floor is relatively high. In comparing the resulting noise characteristics to the noise model constructed in Section 3.8.3, implementing the models for the specific construction in 3.9.1-3.9.2, the dominant source is associated with the band-pass filter stage of the demodulation. The low-pass stage of the filter block is of higher order and therefore has higher noise than the high-pass filter stage. By altering the order of these filters and adding gain at the lower noise high pass stage, the overall noise floor is lowered easily.

Figure 3-48. A schematic of the final low pass filter in the Synch MOD/DMOD system.
Figure 3-49. The measured noise floor of the first-generation Synch MOD/DMOD.

Otherwise the overall approach proved feasible and further integration in order to lower the noise floor and remove the dependence on other lab equipment can move into a second-generation Synch MOD/DMOD design.

### 3.10 Second-Generation Synch MOD/DMOD

The second-generation aims to include an on-board oscillator, power management circuitry, and mitigate some of the noise issues seen in the first-generation. In addition to these changes, the bias frequency is shifted to 1 MHz. This bias frequency moves the sensor signal into the lower noise flat-band portion of the immediate interface amplifier. The original 100 kHz bias frequency was only chosen in order to aid in the development in the system, as most of the diagnostic equipment available in a standard fluid dynamics laboratory does not extend into the MHz frequency range. As the overall synch MOD/DMOD topology has been demonstrated the same diagnostic capability is
not required. The design changes to the Synch MOD/DMOD in this second-generation are outlined by section.

### 3.10.1 Modulation

There are two changes to the modulation portion of the Synch MOD/DMOD system in this generation; the addition of an on-board oscillator and the simplification of the bias signal generation.

#### 3.10.1.1 Oscillator design

In order to reduce reliance on bench-top equipment, an on-board oscillator is designed. In designing an oscillator there are two main considerations; phase noise and harmonic generation. In both cases the quantities are to be minimized and are reliant on the overall Q of the oscillator. The frequency in the first-generation was restricted by the availability of diagnostic equipment in the laboratory. As the topology has been proven viable, the bias frequency is increased.

![Circuit schematic of the Colpitts oscillator](image)

Figure 3-50. A circuit schematic of the Colpitts oscillator.
To reduce the requirements on the required in-package bias resistor, the bias frequency is increased by an order of magnitude to 1 MHz. A Colpitts oscillator is chosen due to preferential phase noise performance and ease of implementation [68]. The full oscillator circuit is shown in Figure 3-50. The oscillator is comprised of two sections of circuitry; the bias circuitry and the tank circuit. The bias circuitry, consisting of $R_1$, $R_2$, and $R_b$, set the large-signal transconductance, $G_m$, and small-signal transconductance, $g_m$, of the transistor. The tank circuit, consisting of $L$, $R_{tank}$, $C_1$, and $C_2$, sets the oscillation frequency of the circuit.

The bias circuitry is configured such that when a 12 V dc bias voltage is applied the collector current moving through the 2N222 bipolar junction transistor (BJT) is 5 mA. The small-signal transconductance, $g_m$, of the BJT is set by the threshold voltage of the amplifier and the collector current as

$$g_m = \frac{I_C}{V_t},$$

(3-68)

where $I_C$ is the dc collector current and $V_t$ is the thermal voltage and is approximately 25 mV at room temperature. The large-signal transconductance, $G_m$, is also set by the bias conditions and is

$$G_m = \frac{2I_C}{V_b},$$

(3-69)

where $V_b$ is the dc base voltage. The base voltage is set by the voltage divider between resistances $R_1$ and $R_2$ as

$$V_b = \frac{V_{cc}R_2}{R_1 + R_2}.$$  

(3-70)
The collector current is set by the selection of the 2N222 BJT, that has a base to collector voltage of 0.7 V. This sets the collector current as

\[
I_c = \frac{V_b - V_{BE}}{R_b}.
\]  

(3-71)

The first concern in oscillator design is oscillator start up. Oscillators work on the premise that the noise of the system is gained and filtered into a sinusoid by the transistor and tank circuit. In order for the noise to be amplified at start up, the overall loop gain of the circuit must be greater than one. To achieve this, the small signal transconductance is set so that satisfies [75]

\[
g_m > \frac{1}{R \left( \frac{C_1}{C_1 + C_2} - \frac{C_1^2}{(C_1 + C_2)^2} \right)}.
\]  

(3-72)

The BJT is replaced by a large signal transistor model as shown in Figure 3-50.

Figure 3-51. Simplified model of the Coliptts oscillator shown as A) a small signal model and B) a parallel RLC circuit.
In analyzing the simplified model in Figure 3-51 the oscillation frequency and amplitude are found. The frequency of the oscillator is determined largely by the inductor and capacitive divider and is

$$\omega = \frac{1}{\sqrt{C_1 C_2 (C_1 + C_2)}}. \quad (3-73)$$

The amplitude of oscillations is expressed as

$$V_{osc} \approx 2I_c R_{tank} \left(1 - \frac{C_1}{C_1 + C_2}\right). \quad (3-74)$$

This approximation relies on the assumption that the Q of each component is high. It is important to note that while this equation indicates that increasing the tank resistance will improve the oscillator performance by increasing the output voltage, the tank resistance is also a driving factor of the oscillator Q. This means that if the tank resistance is high, the overall Q of the oscillator is low, and the oscillator performance is degraded. The oscillator is simulated using PSPICE in order to verify that oscillations will start up and to predict the order of magnitude of the oscillator output. With the component values listed in Appendix F the oscillation start up time is approximately 46 \(\mu\)s, the frequency and amplitude of the resulting sinusoid are 0.95 MHz and 1.25 V, respectively.

In order to more carefully control the bias amplitude, an op-amp based gain stage is cascaded with the oscillator. The addition of a gain stage with a trimming resistor allows for the bias voltage to be set at calibration. A coupling capacitor is put at the
output of the oscillator in order to remove the dc offset that is inherent in the oscillator output. The total oscillator block is shown in Figure 3-52.

![Total oscillator block diagram](image)

Figure 3-52. A schematic of the total oscillator circuit including the amplification of the bias signal for increased bias voltages.

### 3.10.1.2 Bias generation

In the first-generation bias generation was implemented with a buffer, inverter, and phase adjust circuitry. As the system is ultimately calibrated the addition of the phase adjust circuitry is an aspect that is overdesigned. The phase errors in the bias signal generation will alter the system sensitivity. However, as shown in 3.8.1, the gain on the bias signals alters the sensitivity more significantly. In the second-generation the gain adjust is maintained but the phase adjust portion is removed. The phase adjust circuitry was only as useful as the packaging is perfect. The mismatch in cable lengths leading to the sensor along with path lengths of leads to the die all contribute to additional phase offsets, that were not accounted for in the original implementation of the bias circuitry.
Figure 3-53. A schematic of the modulation circuitry for the second-generation of the Synch MOD/DMOD circuit.

This simplified diagram for bias generation, including the Colpitts oscillator and associated gain stage, is shown in Figure 3-53. With the change in bias frequency the GBWP of the amplifiers chosen for the modulation circuitry must be considered. In the case of amplifier A1 the largest feasible gain is +10 as the output of the oscillator is expected to be on the order of 1 V. The GBWP of the amplifier A1 must exceed 10 MHz in order to guarantee that the output signal is not distorted. This change in bias frequency will have a larger impact on the demodulation portion of the circuitry.

3.10.2 Demodulation

To accommodate the bias frequency the first two sections of the demodulation circuitry; the input band-pass filter and the demodulation switch, must change significantly. In addition to the new bias frequency the input filter stage is altered in
order to reduce the overall noise floor of the system, as outlined in 3.9.3. Again, the demodulation block is broken down into several smaller blocks; signal conditioning before rectification, rectification, rectification control, and signal conditioning after rectification. Each section is described individually in the following sections.

3.10.2.1 Signal conditioning before rectification

The first stage of the demodulation circuitry is still a band-pass filter, however the order of the low-pass and high-pass stages has been reversed with respect to the first-generation. Immediately following the in-package buffer amplifier is a single pole high-pass filter with gain adjustability. The corner frequency is increased to 100 kHz, that is still a decade down from the bias frequency.

The low-pass component is constructed using a fifth-order elliptic filter in the LT1560 from Linear Technologies. The change in filter components also reduced the complexity of the circuit board layout, as the LT1560 is pre-programmed for a bandwidth of 1 MHz and does not require external components. Additionally, the rms noise of the LT1560 is a factor of two lower than the LT1563 from the first-generation. A schematic of this new circuitry is shown in Figure 3-54. Following this band-pass filter stage the signal is again fed into an active rectifier.

![Figure 3-54. A schematic of the signal conditioning before rectification block in the second-generation Synch MOD/DMOD.](image)

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3.10.2.2 Rectification

![Diagram of rectification block]

Figure 3-55. A schematic of the rectification block of the second-generation Synch MOD/DMOD system.

As with the band-pass stage, the active rectifier components also need to be chosen to accommodate the 1 MHz bias frequency. The signal is split into two paths, one that is inverted and one that is simply buffered. As there is no gain in either path, the GBWP of the amplifiers simply needs to exceed 1 MHz.

The switch that performs the rectification has more stringent requirements in this generation, as the on time for each switch path is reduced from 5 µS to 0.5 µS, that is on the order of some low-resistance switch transition times. A DG419L high-speed SPDT switch is used to rectify the signal. Additionally, a buffer is added between the inverting channel and the switch so that each switch path loads the switch equally and the switching time is nominally symmetric. The demodulation control signal is also re-evaluated for higher frequency performance.
3.10.2.3 Demodulation control

The rectification control for this generation is identical in topology to the control in the first-generation, however the implementation is changed in order to meet the timing requirements of the higher bias frequency. The topology is shown in Figure 3-56.

Figure 3-56. A schematic of the rectification control block.

The buffer, phase adjust, and comparator must all have GBWP greater than 1 MHz. The component that is change between the first and second-generation of the Synch MOD/DMOD circuitry is the inverter, shown in Figure 3-46 as A13. The low output capacitance and high speed performance of the SN74AHCT1G14 make it appropriate for the second-generation. The rectified signal that is produced by this control and the circuitry described in the previous section passes into a final signal conditioning block in order to reclaim the baseband flow information. This final block is described in the next section.

3.10.2.4 Signal conditioning after rectification

As described in 3.8.2.4 in order to reclaim the baseband information the rectified signal is low pass filtered. The chosen filter is again the LTC1563 and is configured for a cutoff frequency of 20 kHz. The cutoff frequency is changed with a single resistor to accommodate larger bandwidth designs.
3.10.3 Integrated Power Management

There are four different voltage potentials required in the system, +12 Vdc, -12 Vdc, +5 Vdc, and -5 Vdc. These voltages are derived from a single ac adapter with a +12 Vdc output. Three active voltage regulators derive the additional required potentials. The +12 Vdc output of the ac adapter is used to source the regulators that create the -12 Vdc and +5 Vdc potentials. The created -12 Vdc rail then goes on to source the -5 Vdc potential.

The -12 Vdc rail is created using several LTC1144 switched capacitor voltage inverters from Linear Technology. This switched capacitor topology is chosen for ease of implementation and lack of external inductors. Limitations on the output current require that several of these converters be used in parallel to source enough current to supply the electronics operating with a -12 Vdc potential as well as the regulator to create the -5 Vdc potential and source the electronics on it.

The -5 Vdc and +5 Vdc potentials are created using the LM7905C and LM7805 linear voltage regulators, respectively. These linear regulators source the entire demodulation chain rather than the switching supplies in order to prevent the feed through of power supply noise into the ultimate sensor system output.

Combining the circuitry described in 3.10.1 through 3.10.3 the second-generation of the synch MOD/DMOD system is constructed. The performance of this new generation is compared to the first-generation in order to verify that the overall noise has been reduced.
3.10.4 Summary of the Second-Generation Synch MOD/DMOD

Following the second-generation circuitry fabrication the system is characterized. In order to see the impact of noise sources in the modulation portion of the synch MOD/DMOD system, the noise floor of the system is characterized with a sensor attached. The noise floor is shown in Figure 3-57.

![Figure 3-57. The measured noise floor of the second-generation Synch MOD/DMOD system compared to the noise floor of the first-generation.](image)

As seen in 3.9.3 there is again a clear low frequency component that is dominated by the final low-pass filter stage however in the flat band region the overall noise level is reduced from 20 nV at 1 kHz in the first generation to 0.01 nV at 1 kHz in the second generation due to the alteration in overall topology. A large peak is present at approximately 4 kHz. This is a switching frequency associated with the power regulation circuitry. Recommendations for eliminating this peak are given in Chapter 7.

The integration of the oscillator and power distribution allows for the circuitry to be packaged into a form factor becoming of a piece of laboratory equipment. It is encased
in an aluminum box approximately 6" x 4" x 1.5" with external BNC connectors to support the sensor, as shown in Figure 3-58. While the system in its entirety is described within this section the portion of interface circuitry that is used to define the sensor performance during the device optimization.

Figure 3-58. A photograph of A) the Synch MOD/DMOD system with a pen as a reference of the final size and B) the internal circuitry.

3.11 Summary

In this chapter the technical challenges of interfacing with a capacitive transducer in order to make a measurement of mean and dynamic capacitance change are outlined. A synchronous modulation/demodulation scheme is chosen and implemented in two generations reducing the noise floor by two orders of magnitude in one generation of development.

An additional advantage to the synchronous modulation/demodulation design shown in Section 3.8 is that only the immediate voltage follower, that is co-located with the sensor, directly impacts the transducer. The noise characteristics of the subsequent demodulation stage will impact the overall signal to noise ratio of the system, but is adjustable as new technology comes onto the market.
The immediate interface with the transducer is included in the optimization problem formulation, as the parasitics and noise characteristics will impact the optimization objective function. Specifically, the noise characteristics of this amplifier, evaluated at the bias frequency, will be used to calculate the minimum detectable shear stress. The AD8022, manufactured by Analog Devices, is chosen for its low input capacitance noise characteristics, as outlined in Section 3.4.3.
CHAPTER 4
OPTIMIZATION

In this chapter, a formal optimization problem is constructed in order to achieve the best possible designs for the physical geometry of the shear stress sensor given the application of fundamental turbulence measurements in a low-speed wind tunnel facility. The optimization uses the minimum detectable signal as an objective function, while fabrication, application, and design based constraints are imposed. The models and constraints have been expanded in order to provide a quantification and optimization of rejection to an input pressure signal to the sensor. In this chapter, the goals of sensor performance are outlined and translated into an optimization objective with constraints. Several design spaces are generated, studied, and the final designs for fabrication are determined.

4.1 System Level Optimization Objectives

Using a built in MATLAB function, fmincon, sequential quadratic programming minimizes the objective function, that is minimum detectable shear stress. Sequential quadratic programming uses a direction seeking algorithm to minimize or maximize a given function. The chosen function, fmincon, uses the Lagrangian formed using the objective and constraint functions\[76\]. The benefits of this local optimization implementation are convergence speed and accuracy. Multiple initialization points will be chosen in order to ensure that a global optimum has been reached.

There are two overall goals for this optimization; a minimization of minimum detectable shear stress and a maximization separation of the operational spaces for sensing pressure and shear. Instead of formulating a multi-objective optimization, a single objective optimization is used, with the secondary goal of pressure mitigation...
implemented as a constraint. The response of the sensor to a pressure input is mitigated in two ways; by altering the frequency response function of the sensor due to a pressure input to effectively filter out the response to pressure in the bandwidth of its operation as a shear stress sensor, or to increase the minimum detectable pressure above the levels expected given the application of turbulent boundary layer measurements. This separation of design spaces is visualized in Figure 4-1.

![Figure 4-1](image)

**Figure 4-1.** A visualization of the operating space for the sensor.

The primary goal of the optimization is to minimize the minimum detectable shear stress. Minimum detectable signal is defined as

\[
MDS_{s_w} [\text{Pa}] = \frac{v_n[V]}{S_{s_w}[V/\text{Pa}]},
\]  

(4-1)
where $v_n$ is the voltage noise described in 3.8.2 given by

$$v_n[V] = \sqrt{S_v[V^2/Hz]}_{\text{bias}},$$

(4-2)

and $S_{tw}$ is the total sensitivity to a shear stress input given by

$$S_{tw} = V_o H_{\text{gap}} \left( \frac{C_{10} - C_{20}}{C_{10} + C_{20} + (C_p + C_i)(1 - \kappa^2)} \right) \frac{\delta(\tau_w) / \tau_w}{g_{01}}$$

(4-3)

that is derived from Equation 3-33. As Chandrasekharan et al. did not implement a synch MOD/DMOD scheme the noise characteristics used in the initial optimization were based on low-frequency amplifier performance. In this generation the synch MOD/DMOD bias frequency will set the point where the noise of the amplifier will be considered. This is advantageous as $1/f$ noise is avoided. Given an AD8022 buffer amplifier, manufactured by Analog Devices, and a bias frequency of 100kHz the voltage noise is 2.3 nV / $\sqrt{\text{Hz}}$ and the current noise is 1 pA / $\sqrt{\text{Hz}}$ [48]. As the noise of the synch MOD/DMOD system is a fixed quantity and does not impact the mechanical design of the sensor it will not be included in the optimization for simplicity, though it does impact the overall minimum detectable signal of the system. This impact is evaluated before designs are chosen in order to verify that the output of the sensor is above the overall noise floor of the electronics.

In order to achieve the secondary goal of separating the shear and pressure operating spaces, a constraint is placed on the ratio of element displacement due to shear and the displacement due to the expected pressure. This estimate of pressure rejection is an underestimation of the total rejection of the pressure signal as it neglects the common mode signal rejection that is due to the device symmetry. If the initial capacitances were perfectly matched, any input pressure signal would result in zero
output signal. The mismatch that is created due to process variation induces an output voltage per input pressure. Estimating using the displacements rather than an estimated mismatch may limit the design space overall, but is a more conservative design technique. In previous generations [29], the mechanical ratio was 1:5 of tether width to tether thickness. Considering a mismatch of approximately 9%, the measured pressure rejection was 80 dB. This data will serve as a check on the optimization results and a metric quantifying the efficacy of the holes is developed. This constraint will be changed and the optimization rerun in order to determine the maximum achievable pressure rejection.

4.2 Optimization Constraints

In order to define the design space for the optimization, there are several constraints that are implemented. Some of the constraints are fabrication based, such as the design variables described in Section 4.2.5, some are application specific, such as bandwidth in 4.2.1 and linearity in 4.2.3, and some are required to ensure proper operation of the transducer, such as pressure rejection in 4.2.2 and pull in voltage in 4.2.4. This section will outline and describe all of the constraints and motivate the necessity for each.

4.2.1 Bandwidth

The bandwidth of the sensor in its operation as a shear stress sensor is determined by the sensor resonance. The bandwidth required for the sensor depends on the application where it will be used as discussed in Section 1.2.2. The sensor resonance and sensor size are related through the sensor mass and compliance, so placing a bandwidth constraint on the optimization will impact the design space. This will also affect the way that the pressure rejection is evaluated.
4.2.2 Pressure Rejection

As explained in Section 2.2.2, the exact voltage output due to a pressure input is difficult to predict as it is dependent on process variation. In order to quantify the pressure rejection achieved by a given design the ratio of in plane and out of plane displacements will be used as a metric. The displacement is linearly related to the output voltage in both sensor operation as a shear stress sensor and as a pressure sensor. In the case of a pressure sensor the actual voltage generated by this displacement will be mitigated somewhat by common mode rejection, and in shear the output voltage will be doubled due to device symmetry. Comparing the displacements will be an underestimation of the total rejection of pressure signals from the desired shear stress signals, but should still allow for a minimization.

The frequency where this constraint is evaluated will also impact is efficacy in separating the operating spaces. Examining the full LEM circuit models, the pressure response has a zero formed by the lumped compliance of the cavity and lumped resistance of the venting structures and a resonance formed by the compliance and mass of the floating element. The shear response has only a resonance formed by the compliance and mass of the floating element. As the pressure resonance will be higher than the shear resonance due to the tether geometry and will have a cut-on, as seen in Figure 4-2. The separation in operating spaces is exaggerated in order to show each frequency response function clearly.

The separation between the response to a shear force and a pressure force is evaluated near the shear resonance, as that determines the bandwidth of the system. It is important to note that the choice of estimating the pressure rejection at a frequency
near resonance is not necessarily a good estimate of the ultimate voltage output of the sensor due to a pressure input for two reasons. First, estimates of the frequency content of a turbulent boundary layer, specifically the Kolmogorov scales, provide more information at low frequencies [3]. Secondly, as pressure is a common mode input to the differential capacitive bridge meaning that in order to calculate an output voltage a mismatch in the bridge impedances is assumed. The implementation of this constraint is simply to minimize the response of the mechanical structure of the sensor to a pressure input. As the pressure model indicates there is a frequency roll-on the magnitude of the response of the sensor structure to pressure will be greater at higher frequencies, so the mechanical displacement of the sensor due to a pressure input compared to the displacement of the sensor due to a shear input is evaluated at this
relative maximum. This metric is understood to be an under-estimation of the pressure rejection in terms of ultimate output voltage.

4.2.3 Mechanical Linearity

As discussed in Section 2.1, the lumped element model assumes a small deflection. As the deflection becomes larger, it will no longer be a linear function of the input force. The static deflection will be constrained such that the maximum deflection is 3% less than the non-linear deflection for a maximum input force. Mathematically this is expressed as

$$\frac{\delta_{\text{non-linear}} - \delta}{\delta} \leq 3\%,$$

where $\delta$ is described in Section 2.1 and $\delta_{\text{non-linear}}$ is found using the Rayleigh-Ritz method as described in Li’s [77] and Chandrasekharan’s [37] work and is expressed as

$$\delta \left(1 + \frac{3}{4} \left(\frac{\delta}{W_t}\right)^2\right) = \frac{\tau_w W_e L_e}{4E L_t} \left(1 + \frac{NW L_t}{W L_e} + 2 \frac{W L_t}{W L_e}\right) \left(\frac{L_t}{W_t}\right)^3. \quad (4-5)$$

4.2.4 Pull In Voltage

As capacitive transduction is reciprocal the bias voltage must be constrained in order to ensure that the bias does not actuate the sensor. Specifically, the voltage providing the bias must not create a field so large the mechanical force that restores the floating element is overwhelmed, pulling the floating element to one side and short-circuiting the sensor.

For a differential capacitance scheme the dynamic pull-in voltage is [78]

$$V_{\text{pull-in}} = \sqrt{\frac{q_0^3}{2C_{\text{ME}} A}}, \quad (4-6)$$
where \( g_0 \) is the smallest gap between two electrodes. For the sensor in this work the pull-in voltage is

\[
V_{\text{pull-in}} = \sqrt{\frac{(g_{01} - \delta)^3}{2C_{\text{ME}} \varepsilon (3L_{\text{teff}} + L_e + (N - 1)L_o)}}.
\]  

(4-7)

During optimization, the bias voltage will be constrained to 85% of the magnitude under where pull-in occurs.

As the bias is required to have frequency content, the frequency of that bias voltage must also be determined. The constraint on this portion of the bias is simply that the frequency must avoid a structural resonance. Lumped element modeling only predicts the system behavior up to the first resonance, and cannot be used to predict appropriate bias frequencies. Additional modeling, such as finite element modeling, must be implemented in order to determine what frequencies are appropriate. As the frequency does not play a part in the determination of minimum detectable shear stress, and instead only allows for dc measurement, it is not an important parameter in the optimization of the mechanical structure and is left out of the optimization variables.

### 4.2.5 Summary of Constraints and Design Variables

In addition to the constraints listed in Sections 4.2.1 through 4.2.4 the different geometries are by traditional MEMS micromachining techniques. In total there are 11 design variables, their upper and lower bounds are shown in Table 4-1. For clarity, the variables are indicated in Figure 4-3. Variables \( V_{\text{bias}} \) and \( n_h \) are not included in the figure and represent the sensor bias voltage and number of holes perforating the sensor floating element respectively.
Missing from the above table are the perforating hole diameter, $d_h$, width of the floating element, $W_e$, and the length of the floating element, $L_e$. Leaving the number and diameter of perforating holes caused the optimization to find multiple local minima and obfuscated the global minimum. In order to constrain the problem and simplify fabrication the diameter of the holes is fixed at $10 \mu m$ and the number of holes is left as an optimization variable.

![Cross Section XX'](image)

Figure 4-3. The physical sensor structure with optimization labels identified.

The dimensions of the floating element are dependent on the scaling analysis outlined in Section 1.1.3, that is justified by an empirical hotwire study [8]. While there are significant differences between hotwires and floating element shear stress sensors there is no existing work studying the scaling for floating element sensors in a turbulent boundary layer. The hotwire study is used here to provide a basis for design generation.
Table 4-1. Design variables used in optimization.

<table>
<thead>
<tr>
<th>Bound</th>
<th>$V_{\text{bias}}$ (V)</th>
<th>$L_t$ (µm)</th>
<th>$W_t$ (µm)</th>
<th>$T_t$ (µm)</th>
<th>$L_o$ (µm)</th>
<th>$W_i$ (µm)</th>
<th>$g_{01}$ (µm)</th>
<th>$g_{02}$ (µm)</th>
<th>$n_h$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower</td>
<td>5</td>
<td>100</td>
<td>10</td>
<td>45</td>
<td>5</td>
<td>4</td>
<td>3.5</td>
<td>3.5</td>
<td>10</td>
</tr>
<tr>
<td>Upper</td>
<td>25</td>
<td>1000</td>
<td>40</td>
<td>50</td>
<td>150</td>
<td>20</td>
<td>15</td>
<td>15</td>
<td>1000</td>
</tr>
</tbody>
</table>

4.2.6 Design Targets

Four different upper bounds for the element width and length are used to generate designs; 1 mm, 500 µm, 200 µm, and 62.5 µm. The 1 mm design performance is comparable to previous floating element work [79] and the 500 µm is chosen for scaling purposes. The 200 µm element size meets the scaling requirements of the largest facility where a floating element shear stress sensor has been successfully installed [80]. The 62.5 µm element size matches the smallest hotwire used in the scaling study.

Table 4-2. The various floating element sizes selected for optimization and their associated friction velocities and bandwidths from the scaling analysis presented in Section 1-3.

<table>
<thead>
<tr>
<th>Floating Element Size</th>
<th>Friction Velocity</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 mm</td>
<td>0.31 m/s</td>
<td>2.1 kHz</td>
</tr>
<tr>
<td>500 µm</td>
<td>0.63 m/s</td>
<td>8.3 kHz</td>
</tr>
<tr>
<td>200 µm</td>
<td>1.57 m/s</td>
<td>52 kHz</td>
</tr>
<tr>
<td>62.5 µm</td>
<td>5.02 m/s</td>
<td>535 kHz</td>
</tr>
</tbody>
</table>

The scaling based design targets are shown in Table 4-2. The size of the floating element sets the friction velocity where it is appropriate. The bandwidth is then derived using that friction velocity.
4.3 Optimization Results

While the primary goal of this optimization is to create optimized designs meeting the theoretical scaling requirements for smaller floating element sizes lower bandwidth designs prove useful for model verification. The ultimate designs for fabrication are then presented in this chapter along with the justification for each design chosen.

4.3.1 Optimization Bounds and Impact on Design Selection

As shown in Table 4-2, the commensurate bandwidth for a sensor 1 mm is 2.1 kHz. Previous generations have fabricated floating elements of this size with a bandwidth of 5 kHz. In order to compare performance directly with previous generations the optimization is performed with a bandwidth of 5 kHz. Design 1 in Table 4-3 is the resulting design of this optimization.

The commensurate bandwidth for a sensor 500 μm is 8.3 kHz, as shown in Table 4-2. To capture this frequency, an optimization is performed with a bandwidth constraint of 10 kHz. Design 2 in Table 4-3 is the resulting design of this optimization.

As the floating element size shrinks to 200 μm, the commensurate bandwidth grows to 52 kHz. As the bandwidth is now an order of magnitude larger than any demonstrated devices, multiple optimizations are performed in order to determine the effect of the increased bandwidth on device performance. At an element size of 200 μm and a bandwidth of 5 kHz the predicted minimum detectable shear stress is 1.05 mPa. At a bandwidth of 50 kHz the minimum detectable shear stress grows to 14.9 mPa. In order to see the trend of the bandwidth constraint on minimum detectable shear stress multiple design spaces are generated and the resulting minimum detectable shear stress values are plotted against the bandwidth constraints that
generated them. The results are shown in Figure 4-4. When the bandwidth constraint is set at or below 20 kHz the minimum detectable shear stress is below 5 mPa. In this case, two devices are selected for fabrication, one with a bandwidth of 20 kHz to produce a relatively low minimum detectable shear stress and another with a bandwidth of 50 kHz to approach the appropriate scaling for the element size.

![Figure 4-4](image)

The results of the study of bandwidth on the minimum detectable signal for the optimized floating element sizes.

The final element size chosen for optimization is 62.5 μm, that matches the smallest hotwire currently presented in literature. The commensurate bandwidth at this element size is 535 kHz. The optimization does not converge for bandwidths above 75 kHz. Again a bandwidth study is conducted and the results are also shown in Figure 4-4. When the bandwidth constraint is set at or below 20 kHz the minimum detectable shear stress is below 5 mPa. In this case, two devices are selected for fabrication, one with a bandwidth of 5 kHz to produce a relatively low minimum detectable shear stress and resonance to assist in model verification and another with a bandwidth of 75 kHz to maximize the bandwidth while still using the formulated optimization.
4.3.2 Optimization Trends and Designs Selected for Fabrication

Despite the multiple design spaces many trends held across all of the finalized designs. First, the nominal capacitance is always maximized. This influences the overlap of fingers, $L_0$, the gaps, $g_{01}$ and $g_{02}$, and the width of the fingers, $W_f$.

Additionally, the sensitivity of each design to variations in the design variables hold across all design spaces. The sensitivity of the device performance to these design variables is shown in Figure 4-5, assuming a 1 mm floating element size, and illustrates that the device performance is most reliant on the gaps and the tether geometries.

![Figure 4-5. The sensitivity of the optimized design on the design variables.](image)

The behavior of the optimization with regards to the pressure constraint manifests in several ways. As the height of the cavity is largely set by the geometries of the material that the sensor is constructed out of there were two channel heights where the
optimization was performed. The cavity height is either 5 \( \mu \text{m} \) or 500 \( \mu \text{m} \), that is set by the geometry of the raw materials. At a cavity height of 500 \( \mu \text{m} \) the pressure rejection constraint forces the design to increase the area of the sensor. The pressure rejection constraint is implemented as a ratio of displacement due to shear to pressure based displacement. The expected response to this constraint is a manipulation of the pressure cut-on that would manifest in an optimal perforation of the floating element. With such a large cavity height the compliance of the cavity overwhelms any possible changes in resistance. The optimization then begins maximizing overall sensor area in an attempt to maximize deflection due to shear stress. When the cavity height is set to 5 \( \mu \text{m} \) the optimization begins to alter the hole structures in order to change the pressure cut-on. The optimization also used the holes to remove mass from the floating element in order to manipulate the resonant frequency.

After changing the cavity height the pressure constraint was not active and the design was bounded by the fabrication bounds and resonant frequency. While the designs produced are predicted to have better rejection of pressure inputs, the sensor cannot be called optimized with respect to the LEM developed for pressure. In order for this to happen a true multi-objective optimization would need to be formulated, that is outside of the scope of this work. The details of each of the designs selected for fabrication are shown in Table 4-3.

4.4 Summary

This chapter presented a system level optimization of the shear stress sensor structure while attempting to minimize the out of plane motion of the floating element structure through the use of an optimization constraint. The operating space of this
optimization is not large enough to implement all of the desired pairs of element size and bandwidth, but a parametric set of designs is available for study of the validity of the scaling analysis presented in Chapter 1. Following design selection sensors are fabricated as described in Chapter 5.

Table 4-3. The optimized geometries chosen for fabrication.

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Design 1</th>
<th>Design 2</th>
<th>Design 3</th>
<th>Design 4</th>
<th>Design 5</th>
<th>Design 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>UB of $L_e$ ($\mu$m)</td>
<td>1000</td>
<td>500</td>
<td>200</td>
<td>200</td>
<td>62.5</td>
<td>62.5</td>
</tr>
<tr>
<td>UB of $W_e$ ($\mu$m)</td>
<td>1000</td>
<td>500</td>
<td>200</td>
<td>200</td>
<td>62.5</td>
<td>62.5</td>
</tr>
<tr>
<td>Bandwidth (kHz)</td>
<td>5</td>
<td>10</td>
<td>20</td>
<td>50</td>
<td>5</td>
<td>50</td>
</tr>
<tr>
<td>$V_{bias}$ (V)</td>
<td>22</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>$L_e$ ($\mu$m)</td>
<td>1000</td>
<td>500</td>
<td>200</td>
<td>200</td>
<td>62.5</td>
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<tr>
<td>$W_e$ ($\mu$m)</td>
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<tr>
<td>$L_i$ ($\mu$m)</td>
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<td>16</td>
<td>11.5</td>
<td>25</td>
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<td>10</td>
</tr>
<tr>
<td>$T_i$ ($\mu$m)</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>45</td>
</tr>
<tr>
<td>$L_o$ ($\mu$m)</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
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CHAPTER 5
SENSOR FABRICATION AND PACKAGING

Given an optimized sensor design from Chapter 4, the sensor die is fabricated and packaged. The fabrication process is a silicon bulk micromachining process with six masks. The process flow is outlined in Section 5.1 with fabrication results presented in Section 5.2. The developed sensor package is then discussed in Section 5.3. The packaging leverages existing printed circuit board technology and a laser machined shim cap to achieve a hydraulically smooth surface capable of interface with additional circuit boards. This shim cap is combined with additional mechanical supports to create a robust package suitable for use in wind tunnel facilities as described in Section 5.4.

5.1 Fabrication Process Flow

The MEMS sensor structure will be fabricated using six masks using bulk micromachining techniques with pre-processed silicon on insulator (SOI) wafers. The final product will be the capacitive floating element structures with metalized backside contacts. Figure 5-1 gives an outline of the process flow. The wafers have a 45 \( \mu \text{m} \) thick highly doped p type device layer and a 5 \( \mu \text{m} \) thick buried oxide layer. Polysilicon through silicon vias (TSVs) are distributed through the wafer, fabricated by IceMos Technology, Ltd, as shown in Figure 5-1(a). The first two masks make contact to the pre-fabricated TSVs creating the pads for the backside contacts and passivating the backside of the device with a nitride coating, as shown in Figure 5-1(b-i). The next two masks make contact with the top side of the TSVs, as shown in Figure 5-1(j-o). The final mask defines the floating element structure, shown in Figure 5-1(p-q). The cavity is formed by removing the BOX layer through the holes placed in the floating element
for enhanced pressure rejection, shown in Figure 5-1(r-s). Appendix G contains the
detailed process traveler for this process flow.

Figure 5-1. Step by step fabrication process.

5.2 Fabrication Results

There are two points to evaluate the fabrication through the process flow; first is
the validation of the through silicon vias, secondly is the deep reactive ion etch (DRIE)
that forms the floating element structure. These are discussed in Sections 5.2.1 and
5.2.2, respectively. The final point of failure for the sensor is the release, that is discussed in Section 5.2.3.

5.2.1 Through-Silicon-Via Validation

After the front and back side of the TSVs are metallized, step (o) in Figure 5-1, they are electrically tested to verify that they conduct through the wafer and that the interface between the deposited aluminum silicon and polysilicon TSV is ohmic. During electrical testing, there was great variability from TSV to TSV. Some TSVs appeared nearly ohmic while others were diodes or even open circuits. By cleaving a portion of an unprocessed TSV wafer the variation in electrical testing is explained. In Figure 5-2, a properly formed TSV is shown. The device layer is at the top of the image, and the buried oxide layer (BOX) is the glowing portion in the middle.

![Figure 5-2. A cross-section of a properly fabricated TSV.](image)
The polysilicon fill that creates the conductive TSV is shown connecting through the BOX. In an adjacent TSV the cross section is vastly different, as shown in Figure 5-3.

![Cross-section of a TSV](image)

Figure 5-3. A cross-section of a TSV that is not connected properly.

Some TSVs are non-conductive as the front and back polysilicon fills do not meet at the interface between the handle and the BOX. Devices in this state can still be wire-bonded, as in previous generations, are not able to be flip-chip bonded into the smooth package.

### 5.2.2 Floating Element Fabrication

The performance of the device is primarily dependent on the device geometry, thus the definition of that geometry is of critical performance. The floating element structure is etched using deep reactive ion etching (DRIE) into the device layer of the SOI wafer, step (q) in Figure 5-1, using the BOX layer as an etch stop.
DRIE is an anisotropic method of etching silicon that an isotropic etchant, in this case SF₆, is alternated with a passivation layer C₄F₈, in an reactive ion etch process. The result is an overall isotropic etch, with the degree of isotropy defined by gas flow rates and cycle times. The DRIE process is highly dependent on exposed area, meaning that areas with larger exposure will etch faster than relatively small features. This phenomena is referred to as RIE lag [81] and is shown in Figure 5-4. This lag is particularly troublesome as the basis of the capacitive transducer structure is a highly asymmetric gap, so by definition there are nearly adjacent areas to be etched with vastly different exposed areas.

Figure 5-4. A demonstration of the RIE lag seen on a representative tether structure during the fabrication of the capacitive shear stress sensor where the large gap is 15 μm and the small gap is 3.5 μm.

The result of etching beyond reaching the BOX layer is that the anisotropic etchant begins to remove the passivation layer at the interface between the device layer and the
BOX and begins to etch isotropically. This is commonly referred to footing. While anti-footing capabilities exist, they are not currently available at the facilities used for fabrication in this work. As the structure is modeled as beams with a rectangular cross section, the etch that defines the floating element must be as anisotropic as possible and footing should be minimized. Some footing did occur during the final etch process however the beam is for the most part as designed, as shown in Figure 5-5. Following the definition of the floating element, the cavity is created to release the device.

![Figure 5-5](image.jpg)

Figure 5-5. A cross section of an unreleased tether showing the footing in the base of the tether structure with symmetric 3.5 μm gaps.

### 5.2.3 Floating Element Release

The cavity is formed by removing the BOX layer in a buffered oxide etchant (BOE) bath. The holes in the floating element serve as a pathway for the wet etchant to react with the oxide beneath the relatively large floating element. The result is a released
structure with a 5 \( \mu \text{m} \) cavity beneath it. A cleaved view of a floating element after the release etch is shown in Figure 5-6. In Figure 5-6, it appears that the oxide has been cleared from beneath the floating element structure, releasing it. From a top-down view, however, it is clear that not all of the material between the fingers has been removed, even after over-etching the oxide by a factor of three and the silicon by several DRIE cycles. This is shown in Figure 5-7. In this figure, the top surface of the floating element is visible, but out of focus, as the remaining strings of material are at the bottom of the trenches between comb drive fingers.

Figure 5-6. A cleaved view of the released floating element, showing partial cross sections of the floating element perforations.

Following device manufacture they are electrically characterized, as described in Section 6.1, to determine nominal capacitance and to verify they are fully released. The residual material between the comb fingers restricts the motion of the floating element.
and as a result Silicon-on-Pyrex devices, fabricated by Sells [35] and described in Section 5.3, are used to validate the performance of the system.

Figure 5-7. Residual material between the comb fingers following the release etch.

### 5.3 Silicon-on-Pyrex Devices

As part of the fabrication of sensors for use in wireless devices, as described in Sells, et al. [35], several designs outlined by Chadrasekharan [37] were also fabricated. The sensors fabricated in this process are used in Chapter 6 to validate the packaging and circuitry developed in this work. The process flow for this sensor is available in [34] and is repeated here for completeness.

This two-mask process is shown in Figure 5-8. The process begins with depositing and patterning chrome on a Pyrex wafer (A-B). A cavity is etched into the Pyrex and the chrome is removed (C-D). An SOI wafer is anodically bonded to the Pyrex wafer and the bulk silicon and BOX layer are removed (E-F). Finally the floating element structure is defined using DRIE (G).
5.4 Sensor Packaging

Packaging a MEMS sensor requires all of the same considerations given to integrated circuit packaging, but with added complexity requiring that the sensor is exposed to the environment. These stringent constraints mean the sensor package can account for up to 95% of the total sensor cost [82].

Most of the development in sensor packaging has been directed towards low frequency pressure sensors and actuators [83–86] as those applications require an exposed die but the rest of the package dimensions are not particularly constrained. These applications also leverage older integrated circuit packaging technologies, such as TO cans, to create singular packaged die. While stacked die and integrated packaging techniques assist in the interconnection of a sensor with its interface...
electronics, the custom molded or ceramic packages that are required to realize such packages are expensive and incur large non-recoverable engineering costs.

The four major considerations that shape the package are induced stress, hydraulic smoothness, sensor installation density, and the proximity of interface electronics. The package concept, in order to keep non-recoverable engineering costs low and still produce a robust and effective package will mimic current packaging techniques for microphones or MEMS pressure transducers, such as Kulites. The transducer will be separated from the interface electronics on an end cap. That end cap will then connect to interface electronics contained within a metal tube, keeping the footprint of the sensor small without sacrificing signal integrity.

The sensor packaging is initially demonstrated using sensors fabricated by Sells using a silicon-on-Pyrex fabrication and front-side wirebond connections [35]. This version of the package is described in 5.3.1. In order to accommodate TSV connections the packaging concept is expanded and described in Section 5.3.1.

5.4.1 First-Generation Packaging Concept

In order to realize a robust package capable of accurate measurement of shear stress with minimal materials and engineering costs, a printed circuit board (PCB) based approach is implemented. Hydraulic smoothness is achieved by milling a recess to the dimensions of the sensor die in order to flush mount it into a PCB. The sensor is then wire bonded to features on the top of the circuit board. A non-scale schematic is shown in Figure 5-9. This PCB forms an end cap that is then placed on an aluminum tube containing the immediate interface circuitry, as shown in Figure 5-10. The aluminum tube is 0.5 inches in outer diameter and has an inner diameter of 0.25 inches. This inner diameter is large enough for a single FR4 circuit board populated
with the interface buffer and supporting passives, described in Chapter 3, to be placed in close proximity to the sensor die.

In order to minimize any induced stress from being transferred from the package to the sensor both the cavity the epoxy used to hold the sensor die in to the cavity and the method used to fix the end cap to the rest of the package must be carefully selected. For the package used by Chandrasekharan et al. in the initial sensor characterization a large PCB was press fit into a Lucite plug. This was effective but quite large and unstable. The thermal properties of Lucite are not favorable for high tolerances and as a result the security of the press fit circuit board changed with the ambient temperature and humidity. The sensor was affixed to the PCB board using Dualbond 707 epoxy that required thermal cycling to cure. The mismatch of the coefficient of thermal expansion of the sensor die and PCB may have caused additional stresses on the sensor die. The current package sought to avoid these issues by epoxying the sensor die using a room temperature curing epoxy and by minimizing the areas where the sensor die is connected to the PCB while still maintaining a secure

**Figure 5-9.** A non-scale schematic showing the assembly of the PCB end cap for flush mounting silicon-on-Pyrex devices.
fixture. This will allow the sensor die and PCB to expand and contract with temperature while minimizing the stress at the epoxy contact points. Additionally, instead of a press fit to the supporting structure for the PCB the sensor plug is instead fit to the end cap by matching the outer diameters and applying epoxy. A picture of the current package and the package used in Chandrasekharan et al. are shown in Figure 5-11.

Figure 5-10. Sensor tube package design (not to scale).
The sensor density and proximity to electronics trade off with one another within the package design. In order to minimize overall sensor footprint while still maintaining close proximity to the buffer electronics, the interface board will be placed such that it is perpendicular to the end cap. This increases the depth of the package but decreases the overall outer dimensions dramatically. The interface circuitry board is then placed into a grounded aluminum tube in order to shield the electronics from EMI. A schematic of this interface is shown in Figure 5-8.

While this generation packaging is an improvement over the design in Chandrasekharan et al. there are still several deficiencies. First, the surface wire bonds are exposed to the flow. This is not ideal as not only does this prevent the sensor from being truly hydraulically smooth but it also provides a point of failure for the device as they are delicate. In order to accommodate the TSV fabrication described in Chapter 4 the end cap, shown in Figure 5-8, is redesigned and a second-generation of tube-based packaging is fabricated.
5.4.2 Second-Generation Packaging Concept

A similar approach to packaging was taken in order to accommodate the TSV devices. Instead of a recess being milled into an end cap instead the sensor die is flip chip bonded onto a PCB and a precision laser machined plastic shim cap is used to make the surface of the sensor package flush. The PCB end cap has several small gold pads that fan out to vias, allowing for connection to the circuitry inside of the tube, as in Section 5.3.1.

![Second-generation end cap components (foreground) and an assembled end cap (background).](image)

The plastic shim cap is manufactured using an Oxford J-355-PS Laser Micromachining system. Plastic is a preferable material to metal due to the exposed sensor electrodes. While ideally there is no physical contact between the shim cap and the side of the die, manufacturing the shim cap out of a non-conductive material allows for some flexibility in the tolerance of the cap dimensions and placement. The shim cap, circuit board, and a 4 mm die are shown assembled and in an exploded view in Figure 5-12. Following the assembly of this new end cap onto the first-generation aluminum tube with enclosed electronics the sensor system is able to be characterized. The overall roughness of the interface between the plastic shim cap and sensor die was
measured using a Dektak profilometer and registered a smoothness of approximately 70 μm.

5.5 Summary

In this chapter a fabrication of optimized sensor designs from Chapter 4 implementing through silicon vias was attempted. Due to errors in the fabrication of the TSVs and the difficulty in the final floating element release the through silicon via devices are not functional as shear stress sensors. Recommendations for improving this fabrication are given in Chapter 7. Devices designed by Chandrasekharan [29] but fabricated in a silicon-on-Pyrex process [35], also outlined in this chapter, are used for validation of the support circuitry, packaging, and to demonstrate the sensor performance in bench top and wind tunnel experiments.

Also in this chapter two generations of sensor packaging were constructed. The first-generation flush mounted a sensor die into a printed circuit board, enabling front-side wirebond connections. The second-generation employed a laser micromachined shim cap to flush mount the sensor. The shim cap and sensor die are bonded onto an FR4 substrate that is compatible with both TSV sensors and sensors requiring front-side wirebonds. Following packaging, the sensor system is calibrated and tested in several wind tunnel facilities.
CHAPTER 6
EXPERIMENTAL CHARACTERIZATION

In this chapter, the sensor system is characterized through a series of bench top and wind tunnel experiments. There are two general categories of characterization for the bench top characterization of the sensor system, electrical and mechanical. Electrical characterization is used to validate the quasi-static electrical model and mechanical characterization is used to validate the mechanical models developed in Chapter 2 and provides a device sensitivity and bandwidth. After bench-top characterization the sensor system is tested in three wind tunnel facilities enabling a comparison between the performance with respect to traditional mean and dynamic shear stress estimation techniques. This chapter is broken into two main sections, the first describes the methods that the sensor is characterized and the second presents the results determined by these characterization methods. The parameters used for data acquisition are grouped with the results.

6.1 Experimental Setup

Prior to packaging the sensors are electrically tested. This prevents the packaging of die that are defective. The impedance measurement technique is described in Section 6.1.1. After packaging, the sensors are tested in two fluidic characterization test beds, described in 6.1.2. The first set up simulates mean flow across the sensor and the second simulates dynamic flow across the sensor. The sensor is tested for environmental sensitivities, described in 6.1.3, before being installed into three different wind tunnels. The wind tunnel facilities used to validate the sensor performance are described in Section 6.1.4. Finally the approach to the estimation of experimental uncertainty is described in Section 6.1.5.
6.1.1 Electrical Characterization

Prior to packaging the impedance of the sensor is measured. The impedance is measured using a Cascade M150 probe station with two MPH-Series MicroProbe manipulators and tungsten probe tips. The probe manipulators are configured for four-point measurement up to the point of the attachment of the probe tip.

Figure 6-1. A schematic of the sensor structure with the probe points for the impedance characterization indicated on A) a TSV device and B) a silicon-on-Pyrex device.

In a four-point measurement the four probes are labeled as $H_p$, $H_c$, $L_p$, and $L_c$ indicating two measurement points, $H$ and $L$, with both potential and current
measurements, indicated by the subscripts P and C, respectively. An Agilent 4294A Impedance Analyzer is used to make the four-point impedance measurement. The predicted contributions to the impedance measurement, including an indication of the configuration of the probes with respect to the sensor electrodes, are shown in Figure 6-1. The two capacitances that make up the sensor differential half-bridge are measured separately. The first measurement is indicated by the probes with the subscript 1 and the second measurement is indicated by the probes with the subscript 2. Following electrical characterization the sensor is packaged and the mechanical performance of the sensor is evaluated.

6.1.2 Fluidic Characterization

There are a total of four testing facilities that will be used in order to characterize the sensor system performance. Two bench top characterizations will test three aspects of sensor performance; static sensor response using a flow cell, dynamic sensor performance using an acoustic plane wave tube, and the response of the sensor to an acceleration input. The other facilities used to characterize system performance are wind tunnels; one small-scale wind tunnel available at the University of Florida, one larger wind tunnel available at NASA Langley Research Center (LaRC), and a tunnel at the Graduate Aeronautical Laboratories at the California Institute of Technology (GALCIT). Each set up, along with the measured sensor property, are described in Sections 6.1.2.1 through 6.1.2.4.

6.1.2.1 Mean flow characterization

The static characterization is achieved using a flow cell. The flow cell is constructed of two aluminum plates separated by a 500 \( \mu \)m shim forming a channel 330 mm long and 100 mm wide. The shim height is varied if desired. An Aalborg
MFC mass flow controller is used to set the flow rate through the channel and pressure taps, separated by 76.2 mm and monitored by a Heise pressure module, are centered on the sensor location measuring the pressure drop along the channel.

![Diagram](image)

Figure 6-2. Laminar flow cell schematic (not to scale), demonstrating the control of airflow through the channel.

The flow through the channel is assumed to be steady, fully developed, two-dimensional flow [87] where the shear stress is

$$\tau_w = \frac{h \, dP}{2 \, dx}, \quad (6-1)$$

where $h$ is the channel height and $dP$ is the pressure drop across a known length of the channel, $dx$, as shown in Figure 6.1. This relationship holds regardless of the state of the flow as long as it is fully developed and incompressible [88]. In addition to characterizing the dc response of the sensor, the effects of pressure gradients across the sensor can also be studied by changing the shim height but maintaining the same wall shear stress.
Dynamic flow characterization

The ac response of the sensor is estimated using an acoustic plane wave tube (PWT). The PWT is an aluminum square duct with a 1 inch x 1 inch cross section. The cut-on of higher order modes in air for this geometry is 6.7 kHz. The acoustic source is a BMS 4590P compression driver with a passive crossover circuit [89].

As an acoustic wave propagates down the PWT under the restriction of the no slip boundary condition at the wall a frequency dependent boundary layer, and thus frequency dependent shear stress, is generated. By changing the acoustic termination at the end of the PWT and the orientation of the sensor many different ac characteristics of the sensor are tested in this setup including dynamic sensitivity, frequency response, and pressure sensitivity.

Dynamic sensitivity is tested by generating an ac shear stress through Stokes’ layer excitation in an acoustic PWT with a sound hard boundary. A speaker is mounted at one end of the PWT and the other end will be terminated with a sound hard boundary. When the speaker is on a standing wave pattern is developed. The sensor is placed at a known location along the wave pattern and the sound pressure level of the excitation signal is swept. The shear stress acting on the sensor is related to the sound pressure levels at both the sensor location and at the arbitrary boundary by

\[
\tau_w = -\frac{1}{c} \sqrt{|j\omega v|} \tanh \left( a \sqrt{\frac{j\omega}{v}} \right) e^{jk_d} \frac{e^{-jk_d} - \text{Re}e^{-jk_d}}{e^{-jk(d-s)} + \text{Re}e^{-jk(d-s)}} p_{\text{measured}} e^{j\omega t} \tag{6-2}
\]

where \(d_s\) is the distance between the sensor and the boundary shown on Figure 6-2, \(\delta\) is the distance between the sensor and the reference microphone, that in this case is equivalent to \(d_s\), \(k\) is the acoustic wave number, \(k = \omega / c\), and \(R\) is the reflection.
coefficient of the boundary. For this set up, an aluminum plate which is a minimum of 1 inch thick is used so that the reflection coefficient is assumed to be 1 [90]. This same configuration is used to determine the pressure sensitivity of the sensor. By changing the excitation frequency such that the sensor is located at a half wavelength instead of a quarter wavelength the sensor will see only a dynamic pressure input. Increasing the sound pressure level within the tube and recording the sensor output a sensitivity curve to dynamic pressure input is generated.

Figure 6-3. Dynamic shear stress sensor calibration experimental setup using an acoustic plane wave tube with a sound hard boundary to set up a standing wave pattern in the tube.

This PWT configuration is limited as the geometry of the tube limits the number of frequencies that meet the half or quarter wavelength requirement. In order to construct a frequency response function of the sensor to a shear or pressure input the frequency that excites the PWT is varied. Using this configuration, the resolution of any constructed frequency response function is poor. In order to improve frequency resolution, a movable sound hard boundary is installed. This movable boundary allows
for any frequency within the operational range of the plane wave tube is usable and the sensor will be at the desired pressure or a shear minimum.

![Diagram of movable back plate PWT configuration](image)

**Figure 6-4.** A schematic of the movable back plate PWT configuration for acquisition of frequency response functions, courtesy of Anup Parikh and Daniel Blood.

The movable back plate has an integrated motor and motor controller to ensure that the back plate is placed appropriately. The motor controller is programmed using an Arduino Uno microcontroller interfaced with LabVIEW. LabVIEW is used to implement a gradient descent algorithm to minimize the pressure at the sensor location and determine the optimal location for acquiring shear stress data. The position of the back plate is determined by a proximity sensor and is reported. In order to place the sensor at a pressure maxima, shear minima, the control loop runs to minimize shear stress and then the frequency is doubled before data acquisition.

An alternate way of obtaining the frequency response function is by attaching an anechoic termination to the end of the PWT, shown in Figure 6-5. The resulting sensor output is a composite sensitivity of shear and pressure, but is tested over the frequency range of the plane wave tube. The result is an approximation of the frequency response.
function of the sensor performance with respect to a shear stress input, and is a predecessor to the setup shown in 6-4. This experiment is quicker and much simpler to perform as there is no active control of the termination. In this case progressive plane waves create an input shear stress given by

\[ \tau_w = -p' \frac{\sqrt{(j\omega)}}{c} e^{(j\omega-t_{kd})} \tanh \left( a \frac{\sqrt{j\omega}}{V} \right). \]  \tag{6-3} 

Figure 6-5. Experimental setup for a combined shear and pressure response testing using an acoustic plane wave tube with an anechoic termination.

In either termination case, the frequency response function of the shear stress measurement system is expressed as

\[ H(f) = \frac{\tau_{\text{sensor}}}{\tau_{\text{input}}} = \frac{V}{\partial V} \frac{\partial \tau}{\partial \tau}, \]  \tag{6-4} 

where \( \tau_{\text{in}} \) is estimated by Equation 3.84 or 3.83, depending on the measurement method, \( V \) is the output voltage of the sensor, and \( \frac{\partial V}{\partial \tau} \) is the magnitude of the sensitivity determined in the experiment shown in Figure 6-3.

6.1.3 Environmental Characterization

As the sensor is exposed to the flow during characterization and ultimately use it is important to understand how the sensor reacts to changes in the ambient environment.
To characterize the response of the sensor to changes in ambient temperature and relative humidity an Espec ESX-3CA Platinous Chamber with an SCP-220 controller is used to cycle through different environmental conditions. The chamber is capable of temperatures from –70°C to 180°C and relative humidities from 10% to 95%. In order to decouple the effects of each environmental input two tests are conducted. First the temperature is cycled at a static relative humidity. After determining sensitivity to temperature the chamber is held at a given temperature and relative humidity is cycled.

Given a full characterization of the static and dynamic sensitivities of the sensor and an estimation of the sensor performance in varying ambient environments, the next stage of verification is installation into characterized flows. This is achieved at the University of Florida in a small scale facility, described in Section 6.1.4, in a larger scale facility at NASA LaRC, described in Section 6.1.5, and finally at the Graduate Aeronautical Laboratories at the California Institute of Technology (GALCIT) in Section 6.1.6.

6.1.4 Wind Tunnel Facilities

Once the mean and dynamic characteristics of the sensor have been tested independently the sensor is placed into a well characterized flow, like laminar or turbulent flow over a flat plate, and compared with other flow measurement techniques to further verify its performance.

6.1.4.1 Facilities at the University of Florida

An existing flat plate model is installed at the University of Florida in an Aerolab low-speed, open-circuit wind tunnel. The flat plate, shown in Figure 6-6, has an elliptic leading edge and blunt trailing edge with a Plexiglas body to enable laser based
measurements at the surface [79]. The model also contains static pressure taps in order to verify the pressure gradient across the model.

Figure 6-6. Dimensioned schematic of the flat plate model for use in UF facilities [79]. Figure courtesy of John Griffin.

The UF facility is capable of freestream velocities of 2 m/s to 30 m/s with a test section cross section of 30.5 cm by 30.5 cm. The flow over the model remains laminar up to freestream velocities of around 20 m/s and then becomes transitional. In order to test turbulent flow conditions trip tape is placed near the leading edge. The resulting shear stress values that are measured in this facility range from (O) mPa to 2 Pa for Laminar flow and (O) mPato 4 Pa for turbulent or transitional flow.

Comparative measurements available in the facility are currently limited to laser based techniques, such as PIV or LDV.

While the UF facility is an appropriate test bed for initial sensor integration a larger facility would be more appropriate for the final stages of testing before deployment into more complicated flow fields and models. The Shear Flow Control Facility at NASA Langley Research Center (LaRC) is an appropriate next step in testing.
6.1.4.2 Experimental characterization at NASA-LaRC

The Shear Flow Control Facility at LaRC is a low-speed open circuit tunnel with a 20 inch by 28 inch cross section capable of free stream velocities of 5 m/s to 45 m/s corresponding to shear stress values up to 3 Pa. A picture of the LaRC tunnel is shown in Figure 6-7.

Installation into the LaRC tunnel is complicated by the overall size of the tunnel and can better characterize the sensor performance as many additional flow measurement techniques have already been implemented in the tunnel. Due to the larger test section the volume of air required to maintain a particular free stream velocity means that non-conditioned air is pulled into the room from the surrounding garage areas. The instability of the ambient environment tests the sensor sensitivity to factors such as relative humidity and temperature in a fully characterized flow field.

Figure 6-7. A photograph of the 20” x 28” shear flow control facility at LaRC.
The large tunnel size also restricts the types of flow fields that are accurately generated. As the sensor is placed far downstream of the leading edge only turbulent flows are capable of being generated. It is difficult to maintain laminar flow on such large scales. A benefit to the large tunnel size is that if the flow is tripped far upstream of the sensor the resulting turbulent boundary layer has a long region to grow so the resolution requirements on the downstream measurement equipment is relaxed.

An additional benefit to testing in the LaRC tunnel is the wide range of measurement capabilities available. While PIV provides a reasonable estimate of the flow field, it is limited by seeding particle size and cannot be performed while the sensor is installed because of the requirement to have a seeding fluid. At LaRC a traverse is installed at the sensor location with the capability of producing profiles acquired using a Pitot static probe or hotwire probe. Additionally Preston tube measurements are available as a comparative measurement matching flow conditions. In this dissertation velocity profiles acquired using a traversing hotwire and near wall hotwire data are considered.

Following evaluation of the performance of the sensor in well characterized flows, the sensor is transitioned to GALKIT. At GALKIT the sensor is integrated into a model specifically designed for the characterization of non-equilibrium turbulence [91].

6.1.4.2 Experimental characterization at GALKIT

Finally the sensor is tested in the Merrill tunnel at GALKIT. In this set of experiments, the sensor is installed into a flat plate with a trip wire near the leading edge to induce turbulence and an additional downstream time varying trip structure. Comparative measurements are taken with a traversing Dantec type 55 hotwire that
extends from the wall on a sting balance. The flat plate is made of Perspex, an optically clear plastic.

6.1.5 Experimental Uncertainty

There are two general categories of data within these experiments; mean data and spectral estimates. The random uncertainty for each type of data is presented in Sections 6.1.5.1 and 6.1.5.2 for mean and spectral estimation data, respectively. The bias errors are described by test bed in Sections 6.1.5.3 and 6.1.5.4. The total error, as these sources are all uncorrelated, is a root sum square of the individual error contributions.

6.1.5.1 Random error in mean measurements

The output of the Synch MOD/DMOD system is a dc voltage for an input mean shear stress, and thus the error in mean measurement is important. Regardless of the distribution of the random error in a voltage signal, the random error in the sample mean is Gaussian as the number of samples used to calculate the mean approaches infinity [92]. The bounds on the estimation of the mean value, $\mu_x$, is given by

$$\bar{x} - \frac{t_{(N-1)\alpha/2} S}{\sqrt{N}} \leq \mu_x \leq \bar{x} + \frac{t_{(N-1)\alpha/2} S}{\sqrt{N}},$$  \hspace{1cm} (6-5)

where $\bar{x}$ is the sample mean, $N$ is the number of samples, the interval for the estimate is $100(1-\alpha)\%$, $t$ is given by the t-distribution, and $S$ is given by

$$s^2 = \frac{1}{N-1} \sum (x_k - \bar{x})^2.$$  \hspace{1cm} (6-6)
6.1.5.2 Random error in spectral estimation

The random error associated with the estimation of spectral estimation is used to
demonstrate the uncertainty in dynamic sensor calibration. Generally the error estimate
in a spectral estimation is given by

$$\epsilon_r = \frac{1}{\sqrt{n_{\text{dav}}}}$$  \hspace{1cm} (6-7)

where $n_{\text{dav}}$ is the effective number of averages and based on the windowing applied
during estimation. The dynamic sensor sensitivity and frequency response function are
acquired using single tones and are estimated using uniform windowing making the
random error in the estimate

$$\epsilon_r = \frac{1}{\sqrt{N}}.$$  \hspace{1cm} (6-8)

For the frequency response function there is an additional source of error associated
with the coherence between the input and output signals. This error manifests in both
the magnitude of the frequency response function as well as the phase. These errors
are

$$\epsilon_r(\text{magnitude}) = \frac{\sqrt{1 - \gamma(f)^2}}{\gamma(f) \sqrt{2N}}$$  \hspace{1cm} (6-9)

and

$$\epsilon_r(\text{rad}) = \frac{\sqrt{1 - \gamma(f)^2}}{\gamma(f) \sqrt{2N}}.$$  \hspace{1cm} (6-10)

where $\gamma(f)$ is the ordinary coherence function estimated as

$$\gamma_{xy}^2(f) = \frac{|G_{xy}(f)|^2}{G_{xx}(f)G_{yy}(f)}.$$  \hspace{1cm} (6-11)
The ordinary coherence function is also a metric where the relation between two signals is represented. The coherence function varies between zero and one where a coherence of zero indicates that the two measurements are unrelated and a coherence of one indicates perfect correlation.

6.1.5.3 Bias Error in the Laminar Flow Cell Experiments

There are many sources of bias error associated with measurement in a flow cell. The error analysis presented by Chandrasekaran [93] is adapted for the case of pressure driven flow in a channel. Mean shear stress is related to a pressure drop in fully developed, steady, pressure driven flow in a channel by

\[
\tau_w = \frac{h}{2} \frac{dP}{dx}. \tag{6-12}
\]

There are two sources of geometric error that contribute to errors in the estimated shear stress, variations in the channel height, \(h\), and variations in the distance between pressure measurements, \(dx\). The total error in shear stress measurement is expressed as a root mean square addition of these individual error sources as

\[
\left( E_{\tau_w} \right)^2 = \left( \frac{\partial \tau_w}{\partial h} E_h \right)^2 + \left( \frac{\partial \tau_w}{\partial dx} E_{dx} \right)^2. \tag{6-13}
\]

In both cases the error in the dimension is 0.005 inches, or 0.127 mm, and is the machining tolerance of the flow cell. The height of the flow cell is 0.5 mm and the distance between pressure taps is 76.2 mm. The error in the estimate of mean shear stress due to variations in these geometries is 25.4%. This is most likely an overestimation of the error due to geometry and is used to generate a conservative estimate of sensor performance.
6.1.5.4 Bias Error in the Plane Wave Tube Experiments

There are several sources of bias error associated with measurement in the plane wave tube. The error analysis presented by Chandrasekaran [93] is again adapted for the case of ac shear stress resulting from a standing wave pattern. Given the relationship between input pressure and output shear stress,

$$\tau_w = -\frac{1}{c} \sqrt{j\omega \nu} \tanh\left(a \sqrt{\frac{j\omega}{\nu}}\right) \frac{e^{ikd_s} - Re^{-ikd_s}}{e^{jk(d_s-\delta)} + Re^{-jk(d_s-\delta)}} p_{\text{measured}} e^{j\omega t},$$  \hspace{1cm} (6-14)

the error in the estimation of wall shear stress is induced by two dimensions, the dimension of the duct and the distance from the sensor to the sound hard boundary.

This equation simplifies as $d_s = \delta$ to

$$\tau_w = -\frac{1}{c} \sqrt{j\omega \nu} \tanh\left(a \sqrt{\frac{j\omega}{\nu}}\right) \frac{e^{ikd_s} - Re^{-ikd_s}}{2} p_{\text{measured}} e^{j\omega t}. $$ \hspace{1cm} (6-15)

These errors are expressed as the sensitivity to the dimension multiplied by the expected value of the dimension, as

$$(E_{\tau_w})^2 = \left(\frac{\partial \tau_w}{\partial a} E_a\right)^2 + \left(\frac{\partial \tau_w}{\partial d_s} E_{d_s}\right)^2. \hspace{1cm} (6-16)$$

The sensitivity to the dimensions are given by

$$\frac{\partial \tau_w}{\partial a} = -\frac{1}{c} j\omega \text{sech}^2\left(a \sqrt{\frac{j\omega}{\nu}}\right) \frac{e^{ikd_s} - Re^{-ikd_s}}{e^{jk(d_s-\delta)} + Re^{-jk(d_s-\delta)}} p_{\text{measured}} e^{j\omega t}, \hspace{1cm} (6-17)$$

and

$$\frac{\partial \tau_w}{\partial d_s} = -\frac{1}{c} \sqrt{j\omega \nu} \tanh\left(a \sqrt{\frac{j\omega}{\nu}}\right) \frac{e^{ikd_s} - Re^{-ikd_s}}{2} p_{\text{measured}} e^{j\omega t} = 0. \hspace{1cm} (6-18)$$

The total error in the estimation of shear stress becomes
The error in the dimensioning of the duct is assumed to be 0.005 inches. The duct cross section is 1 inch. The resulting error is a maximum of 7.07% of the estimated value of wall shear stress.

6.1.5.5 **Error Analysis of PIV Based Shear Stress Estimation**

The uncertainty in the shear stress derived from PIV measurements uses a Monte-Carlo simulation with 10,000 iterations where the average velocities and distance from the wall are perturbed based on the uncertainty of the PIV data. The resulting boundary layers are fit to estimate wall shear stress. The uncertainty in the wall normal distance is the spatial resolution of the PIV data. The uncertainty in the velocity includes both bias and random uncertainty. The bias uncertainty is also a uniform probability density function, where the magnitude of the bounds is determined [94]. The random uncertainty in the streamwise velocity is assumed to be normally distributed as shown in [95].

6.1.5.6 **Error Analysis of Hotwire Profile Based Shear Stress Estimation**

As was done in the PIV error analysis previously, Monte Carlo techniques are used to perturb the components of the boundary layer measurement. The velocities and distance from the wall are perturbed independently within the standard deviation of the acquired data 10,000 times creating 10,000 unique velocity profiles. The perturbed boundary layers are then fit to Spalding’s law and Musker’s equation for a turbulent boundary layer and the errors are propagated to an error in shear stress.
6.1.5.7 Monte Carlo Analysis of Measured Sensitivities

Given the error sources associated with the deduction of shear stress, a Monte Carlo simulation is performed to establish the bounds of the sensitivity of the sensor system. The Monte Carlo assumes a Gaussian profile for the uncertainty at each measured value and performs 50,000 iterations within the 95% confidence intervals. This assumes that the errors in each point are uncorrelated. The resulting confidence interval of the sensitivity is reported.

6.2 Experimental Results

This section outlines the results of the characterization experiments described in Section 6.1. The results are broken down into two categories; the results associated with the first-generation of synch MOD/DMOD circuitry, Section 6.2.1, and the results associated with the second-generation of synch MOD/DMOD circuitry in Section 6.2.3. The results of the fabricated TSV sensor electrical characterization are shown in Section 6.2.2.

6.2.1 First-Generation Synch MOD/DMOD

The first-generation of the synch MOD/DMOD system is demonstrated with previously fabricated sensors in order to demonstrate the viability of the interface circuitry and packaging techniques. As the sensors in this generation were not built as a part of this work, their electrical properties are described for completeness. The characterization of this generation consists of mechanical properties and wind tunnel demonstrations.

6.2.1.1 Electrical properties

The sensor used in this section of testing is fabricated using a silicon-on-Pyrex fabrication in conjunction with the effort to demonstrate a passive wireless shear stress
sensor [35]. In this case the parasitic capacitances associated with the structure supporting the sensor are practically eliminated; however the sensor still suffers from the requirement of front-side wirebonds. The sensor capacitance is approximately the nominal 1.5 pF [34]. The sensor is packaged with a 2 MΩ bias resistance and then mechanically characterized.

6.2.1.2 Mean flow characterization

The laminar flow cell described in Section 6.1.2.1 is used for two purposes in this installation; the determination of the sensor sensitivity to a mean shear stress input, and the sensitivity of the sensor to angular misalignment. The flow cell is configured with a 0.5 mm tall shim machined to a tolerance of 0.127 mm. The flow through the flow channel is controlled via an Aalborg GFC47 mass flow controller, allowing the flow rate to be set via an analog voltage. The control signal is generated via a LabVIEW controlled dc power supply.

The sensor output is split into two channels and is acquired using a NI PCI-6034E data acquisition system with a BNC-2110 breakout box. Using LabVIEW, the first is an ac coupled version of the sensor output, and the second is the sensor output passed through an SRS560 low noise amplifier with unity gain and two pole low pass filter. The sensor data is taken using the sampling parameters shown in Table 6-1. The data is heavily over sampled as an unfiltered channel is simultaneously acquired for spectral analysis for use in debugging the Synch MOD/DMOD system.

Table 6-1. The sampling parameters used with the flow cell.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Number of samples per block</td>
<td>100,000</td>
</tr>
<tr>
<td>Number of blocks acquired</td>
<td>5</td>
</tr>
</tbody>
</table>
Figure 6-8. The sensitivity of the first-generation Synch MOD/DMOD with a silicon-on-Pyrex sensor acquired using the laminar flow cell.

Figure 6-9. The results of the Monte Carlo simulation of the sensor sensitivity determined by the flow cell experiments.
After acquisition, the data is further down-sampled to an effective sampling rate of 50 Hz and only one block of data is used. The control voltage to the Aalborg Mass Flow Controller is swept from 0 V to 3 V in 0.25 V increments, resulting in 13 flow conditions spanning shear stress values from 0 Pa to 3.2 Pa. The results of this static calibration are shown in Figure 6-8.

It is clearly shown that the large uncertainty in the flow cell measurement technique decreases the confidence in the sensitivity determined using this method. Using the Monte Carlo techniques described in 6.1.5.7, the sensitivity is determined to be 4.6 mV/Pa at an 8Vac bias. The large error in the estimation of mean shear stress results in a large spread of $R^2$ values and thus large uncertainty in the estimation of sensitivity, as shown in Figure 6-9.

![Normalized Sensitivity vs Angle](image)

Figure 6-10. The normalized sensitivity of the shear stress measurement system compared with the incident angle of mean flow across the sensor.
Following static calibration, the sensor plug is rotated relative to the mean flow direction in order to ascertain the error induced by misalignment. A sensitivity to mean shear stress is measured for each relative angle. The sensitivities are then normalized against the 180 degree case and plotted in Figure 6-10. The sensor alignment has a geometrically predicted cosine dependence on sensitivity, indicating that alignment is not critical during installation into wind tunnel facilities. Small variations in angle around the nominal position do not result in large changes in sensor sensitivity.

Following this demonstration of mean performance, the sensor is moved to the plane wave tube where the dynamic sensitivity and frequency response function are measured.

6.2.1.3 Dynamic flow characterization

Using the PWT excitation described in Section 6.1.2.2 the sensor is calibrated using two different bias excitations and the Synch MOD/DMOD system described in Section 3.6.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFT mode</td>
<td>Zoom</td>
</tr>
<tr>
<td>Window</td>
<td>Uniform</td>
</tr>
<tr>
<td>Overlap</td>
<td>0%</td>
</tr>
<tr>
<td>Span</td>
<td>200 Hz - 6.4 kHz</td>
</tr>
<tr>
<td>FFT lines</td>
<td>400</td>
</tr>
<tr>
<td>Acquisition Time</td>
<td>62.5 s</td>
</tr>
<tr>
<td>Bin Width</td>
<td>16 Hz</td>
</tr>
<tr>
<td>Number of linear spectral averages</td>
<td>1000</td>
</tr>
</tbody>
</table>
The resulting calibration for an 8 Vac bias case is shown in Figure 6-10. Comparing this calibration to the mean calibration, the sensitivities are nominally the same, as seen in Figure 6-12. This sensitivity, however, is not optimal given the performance of the Synch MOD/DMOD circuitry. By adjusting the balance of the bias voltages, as described in Section 3.8.1, and the rectification control signal, as described in Section 3.9.2.3, the sensitivity is increased from the 0.6 mV / V / Pa observed in Figures 6-10 and 6-11 to 1.4 mV / V / Pa, as shown in Figure 6-13. This improved sensitivity is the configuration the sensor is used in for the duration of the first-generation Synch MOD/DMOD tests, including the wind tunnel entries. The normalized sensitivity of the whole system, including the Synch MOD/DMOD gain and noise contributions, is 1.359 mV / V / Pa. The sensor is run at a bias voltage of 8 Vac the sensitivity of the system is 10.9 mV / Pa.
Figure 6-12. Combined static and dynamic calibration plots indicating nominally the same sensitivity.

Figure 6-13. Normalized sensitivity of the first-generation Synch MOD/DMOD sensor system as used for further characterization.
Figure 6-14. The combined shear and pressure frequency response function of the shear stress measurement system.

The PWT is terminated in an anechoic wedge to estimate the frequency response function of the system prior to the construction of the moving backplate. The results are shown in Figure 6-14. While the resonance of the sensor system is identifiable in phase and magnitude, the lack of a true flat band region indicates that the pressure input to the sensor is not negligible and this combined measurement results in a combined output. In this case, the pressure at the sensor location is on the order of 100 Pa while the shear stress input is on the order of 1 Pa. As seen in Chandrasekharan, et al. [29] the pressure sensitivity is several orders of magnitude lower than the shear sensitivity, however for this experiment the estimated incident shear stress is on the order of pascals while the input pressure is on the order of hundreds of pascals. The resulting
output signals will be within an order of magnitude of each other resulting in a combined output voltage. While this cannot be called a true frequency response function of the sensor output with respect to an input shear stress, it can provide an estimate in order to use the sensor in a real flow environment.

Following mean and dynamic calibration, the first-generation sensor system is tested in three wind tunnel facilities, the first at the University of Florida, the second at NASA Langley Research Center, and the third at GALCIT.

6.2.1.4 UF wind tunnel comparisons

As discussed in Section 6.1.4.1 the UF Aerolab tunnel is equipped with a flat plate model capable of Laminar and turbulent flows. The tunnel was characterized using PIV for comparison with the mean component of the sensor output. The sampling parameters used for the acquisition of the sensor data are shown in Table 6-3. The sensor data was acquired using The mean shear stress is estimated in three ways; in the case of a laminar boundary layer Blasius’ solution [96] is used, in the case of a turbulent boundary layer the resulting velocity profile is fit to Musker’s equation [97] for a turbulent boundary layer and Spalding’s Law [98]. The estimated shear stress for all cases is shown in Figure 6-15.

The PIV based velocity profile estimation of shear stress was performed by John Griffin along with the error analysis described in 6.1.2.5, that is used to generate the error bars on the PIV data. Within this figure the true advantage to the sensor is illustrated. For a given freestream condition, the sensor is capable of distinguishing a turbulent boundary layer from a laminar boundary layer. Indirect measurement techniques require the flow state to be known a priori and are unable to make this distinction.
Figure 6-15. Comparison of the estimated shear stress produced by the shear stress sensor system and velocity profile estimates measured using PIV [79].

Table 6-3. The sampling parameters used for the UF wind tunnel entry

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency</td>
<td>50 kHz</td>
</tr>
<tr>
<td>Number of samples per block</td>
<td>50,000</td>
</tr>
<tr>
<td>Number of blocks acquired</td>
<td>5</td>
</tr>
</tbody>
</table>

In the laminar case the velocity profile based estimate and shear stress sensor estimate have very good agreement. In the case of the turbulent velocity profiles not only is there noticeable disagreement between the sensor data and either the estimates provided by Musker or those provided by Spalding, but there is disagreement between those two estimates. The comparative measurement in this case is PIV that relies on seeding particles in order to calculate a velocity field. Physically the seeding does not transport to the wall easily and thus the amount of near wall data is limited such that the closest point to the wall that is measured is at a height of 23 mm. This is further limited
by the 0.12 mm spatial resolution of the PIV data. In order to obtain time-resolved near wall data and to better resolve the velocities near the wall a larger facility is used.

6.2.1.5 LaRC wind tunnel comparisons

Following the promising results in the small-scale UF facility, an entry at the NASA LaRC 20”x28” Shear Flow Control Facility was conducted. The flow conditions spanned Reₙ values from 5,100 to 13,000 with freestream speeds spanning 15 m/s to 40 m/s.

Table 6-4. The sampling parameters used for the NASA LaRC study.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Frequency</td>
<td>25.6kHz</td>
</tr>
<tr>
<td>Number of Samples per Block</td>
<td>128,000</td>
</tr>
<tr>
<td>Number of Blocks</td>
<td>50</td>
</tr>
<tr>
<td>Window</td>
<td>Hanning</td>
</tr>
<tr>
<td>Overlap</td>
<td>75%</td>
</tr>
</tbody>
</table>

The sensor data is acquired with an Agilent E1432A VXI bus with VXI-1394 cards. The sampling parameters are shown in Table 6-4. A traversing hotwire were used to estimate the velocity profile used to estimate mean shear stress. The shear stress is elucidated from the resulting velocity profile using Spalding’s law and Musker’s equation for a turbulent boundary layer are shown in Figure 6-16. There is larger disagreement in both the fits and between the velocity profile based shear stress estimate and the sensor output as freestream velocity increases. Another way to view this information is in terms of the coefficient of friction against the boundary layer height based Reynolds number. The spread of shear stress values determined by the Monte Carlo error analysis are shown in Figure 6-17. The profiles are given in Appendix H.
Figure 6-16. Comparison of sensor output to the shear stress determined by a traversing hotwire study with a solid line indicating unity.

Figure 6-17. The result of the Monte Carlo analysis for the determination of shear stress for a freestream velocity of 43 m/s demonstrating the distribution of error in the shear stress estimate as well as the finite difference between two velocity profile based estimation methods.
In order to verify the ac performance of the sensor, a near wall hotwire with an active area of the same approximate size as the floating element was installed. A near wall hotwire is used to estimate wall shear stress by placing it within the viscous sublayer of the boundary layer at a known height from the wall. When in the viscous sublayer the velocity is related to the wall shear stress by

$$\tau_w = \frac{\nu u}{h}$$  \hspace{1cm} (6-20)

where \(u\) is the measured velocity, \(h\) is the height from the wall, and \(\nu\) is kinematic viscosity. The output of the hotwire system is simultaneously acquired with the sensor output and processed using the parameters in Table 6-4. Again varying freestream velocity the output of the hotwire and the output of the sensor displayed similar trends. This is shown in Figure 6-18 for a freestream velocity of 40 m/s with additional cases given in Appendix H. Moving to a larger facility where the boundary layer is thicker and more near wall data is available, the estimates provided by velocity profile fits improve and the agreement with the sensor improves as well. Ideally the hotwire is placed 20 \(\mu m\) from the wall, translating to a maximum \(y^+\) of 2. By using the boundary layer profile to estimate the \(y\) intercept using the no-slip condition the real height from the wall is estimated to vary from 13 \(\mu m\) to 102 \(\mu m\), or from \(y^+\) of 5 to 110. In this case, the upper bounds clearly lie outside of the viscous sublayer leading to additional errors in this estimation technique.

There are several sources of error associated with the nature of a temperature based measurement [99] in this estimate that could account for the difference in magnitude. First, the exact height of the hotwire is unknown. While the traverse was set to a specific height, slip in the traverse drive is a cause of uncertainty. Additionally,
the plate itself is made of metal. As the wire approaches the plate, heat transfer to the cold metal wall would induce a perceived velocity change [100].

Following these measurements, a 3.5 inch diameter cylinder is installed upstream of the sensor and hotwire. The shedding off of the cylinder has a characteristic frequency based on the Strouhal number of the flow where

$$St = \frac{fD}{U_\infty}$$

(6-21)

where D is the diameter of the cylinder and the Strouhal number is 0.2 [5]. The resulting spectra of the shear stress sensor and near wall hotwire are shown in Figure 6-19. While the hotwire and shear stress sensor agree, the frequency is slightly lower than what is predicted by the Strouhal analysis. While imperfect, this demonstrates the ability of the sensor to see a well-characterized oscillating phenomenon in a wind tunnel environment.
After demonstrating the sensor performance in a mean and dynamic sense, the sensor is installed into a facility at CalTech in order to demonstrate the application of the sensor to measure a complex, time varying shear stress field.

### 6.2.1.6 GALCIT wind tunnel comparisons

In the Merrill tunnel at GALCIT the sensor is compared to traversing and near wall hotwires. The traversing hotwire probe is initially placed at a height of 450 μm from the wall and the freestream velocity is set to 24 m/s. The hotwire is traversed to a final height of 50 mm. The resulting boundary layer is fit to Spalding's law and Musker's equation for a turbulent boundary layer resulting in mean shear stress values of 1.11 Pa and 1.06 Pa, respectively. These fits are shown in Figure 6-20. The sensor reports a mean wall shear stress of 1.1 Pa. Unfortunately, the first-generation Synch MOD/DMOD system was destroyed during testing due to a faulty power supply, so no dynamic roughness boundary layer measurements were completed.
Figure 6-20. The velocity profile measured at GALCIT shown in wall units.

6.2.2 TSV Sensor Characterization

Due to the fabrication issues discussed in Chapter 5, the TSV sensors cannot be mechanically characterized, however the electrical properties are still of possible interest. The structure is shown in Figure 6-21 with predicted impedances indicated. Ideally, an impedance measurement when the electrodes are shorted together would result in an approximation of the parasitic impedances of the TSVs. On each TSV die are sixteen TSVs. While not all of these TSVs are intended for use in the final structure the numerous TSVs per die increase the chance that one was faulty, as shown in Chapter 5. A TSV that is not fabricated correctly creates an additional conduction path to the handle wafer that is at worst resistive and at best a diode. In order to make truly meaningful measurements to characterize the TSV performance, a new set of TSV wafers must be fabricated. To validate the design, TSVs are dice off of a 500 \( \mu \text{m} \)
floating element design, and the resulting impedance is measured. The results of that measurement are shown in Figure 6-21.

![Graph](image)

**Figure 6-21.** The impedance of a 500 μm floating element TSV device after the TSVs are removed by dicing.

The impedance measurement is conducted by exciting the sensor with a 500 mV sinusoid of varying frequency in order to build up this C-f curve. The sensor is measured over a bandwidth of 0.5 MHz to 10 MHz as the modulated sensor output will fall within that frequency range. In the results, the mis-match due to fabrication inaccuracies is clearly seen and is 0.1 pF. Additionally, the impedance appears to roll off with frequency. This phenomenon was previously noted by Chandrasekharan [37] and was confirmed by Sells [34] as a phenomenon relating to the presence of the bulk silicon beneath the sensor structure.
6.2.3 Second-Generation Synch MOD/DMOD Characterization

While the fabrication of the TSV devices was not useful for integration into a completely new sensor system, the previous generation of sensors are integrated with the new packaging technology and Synch MOD/DMOD in order to validate those portions of the design work.

6.2.3.1 Dynamic flow characterization

The sensor is again installed into the acoustic plane wave tube in order to determine the dynamic sensitivity and frequency response function of the sensor. The data is acquired using an NI PXI-5122 analog to digital converter housed in an NI PXI-1045 chassis. The sensor and microphone data are simultaneously acquired and the spectra of the ac shear stress is estimated using the parameters in Table 6-5. The movable backplate configuration described in Section 6.1.2.2 is used to measure sensitivity of the sensor system to both shear stress and dynamic pressure as well as estimate the frequency response function of the sensor to shear stress and separately to pressure.

Table 6-5. The sampling parameters used for the acquisition of the frequency response function

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Frequency</td>
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<tr>
<td>Number of Samples per Block</td>
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<td>Number of Blocks</td>
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<td>Window</td>
<td>Uniform</td>
</tr>
<tr>
<td>Overlap</td>
<td>0%</td>
</tr>
</tbody>
</table>

The sensitivity to shear stress is measured by using the gradient descent algorithm to set the backplate such that the sensor is located at a pressure minimum when the tube is excited at 1 kHz. The sound pressure level is increased in order to
build up a sensitivity, shown in Figure 6-22 as is 6.5 mV/Pa. The bias is set by the on-board oscillation and gain circuit to 8 Vac.

![Graph showing shear stress sensitivity](image)

Figure 6-22. The shear stress sensitivity acquired using the variable back plate.

The frequency response function of the sensor with respect to an input shear stress is determined by sweeping the excitation frequency from 300 Hz to 6.3 kHz in 64 Hz steps. For each frequency, the plane wave tube is excited with a single tone and the termination is moved using the gradient descent algorithm. The transfer function between the shear stress predicted by the pressure seen by the microphone in the travelling boundary and the shear stress seen by the shear stress sensor using the sensitivity in Figure 6-22 is estimated. This transfer function is shown in Figure 6-23 in magnitude and phase along with the coherence between the sensor and microphone signals. The expected resonance is demonstrated by the peak in the output magnitude of the sensor and the 180° phase shift. While there is expected to be large error
around resonance [89], the improved coherence (>0.98) between the sensor output and microphone signals estimate little error.

![Graphs of frequency response function, phase, and sensitivity](image)

Figure 6-23. The measured frequency response function of the sensor system to an input shear stress using the variable back plate plane wave tube set up.

The sensitivity and frequency response function for a dynamic pressure input are tested using the same experimental setup. The same gradient descent algorithm is used in order to place the wall such that the sensor is located at a pressure null and then the frequency is doubled in order to change the standing wave pattern such that the sensor is at a pressure maxima and a velocity minimum. The estimated pressure sensitivity is shown in Figure 6-22. Comparing Figures 6-22 and 6-24 it is clear that the minimum detectable pressure is orders of magnitude higher than the minimum.
detectable shear stress. The sensitivity to pressure is $0.34 \, \mu V / Pa$, however this may also be due to additional error sources observed in floating element sensors [99].

![Graph](image)

Figure 6-24. The sensitivity of the sensor to dynamic pressure.

The frequency response function of the sensor output with respect to a pressure input can also be determined using this method, but is more limited. Again, the termination is set using the control algorithm and then doubled in order to set the sensor at a pressure maximum instead of a pressure minimum. The coherence reduction near the first resonant mode of the sensor provides a large estimate of error around the primary resonance of the structure. Additionally, the frequency response function shown in Figure 6-25 does not align with the expected first-order system described in Chapter 4. There are two likely explanations for this behavior.

First, the sensitivity of the device acting as a pressure sensor is significantly lower than the device as a shear stress sensor. In order to exceed the minimum detectable signal in pressure the plane wave tube is driven to 150 dB SPL at the
termination. This high drive signal creates harmonic distortion in the tube at the harmonics of the excitation signal, so while the sensor is at a pressure maxima for a given frequency $f$, it is at a velocity maxima for the second harmonic of that frequency. Particularly as the sensor approaches resonance the motion of the sensor is not purely out of plane. This also explains why the coherence remains near unity, as the microphone will see this non-linearity as well. An additional source of acoustic error is scattering. As the sensor is a released structure there are finite gaps in the sensor surface. These gaps possibly result in acoustic scattering and transverse forces.

Figure 6-25. The measured frequency response function when the sensor is placed at a velocity minimum and pressure maximum.
Secondly, non-idealities in the mechanical sensor structure could lead to coupled motion. The DRIE etch does not result in perfectly straight tether side walls. Given imperfect tethers out of plane displacement results in slight in plane motion.

6.2.3.2 Environmental characterization

The sensor system is designed to be implemented in multiple flow facilities ranging from flow cells sourced with clean dry air to a large tunnel in a garage environment. Therefore, the impact of changes in the ambient environment on the sensor performance must be quantified. In an attempt to decouple environmental parameters, the sensor is first placed in an environment with nominally controlled humidity and swept temperature, and then in an environment with nominally controlled temperature and swept humidity. Prior to both tests, the sensor is held at 25°C and 30% relative humidity for 30 minutes before each test begins. The sensor, packaged in the aluminum housing with the immediate interface electronics attached, is placed into the chamber, and cabling is run out of a port to the Synch MOD/DMOD circuitry. The Synch MOD/DMOD box is not intended to be co-located with the sensor therefore it is not placed in the chamber. Both Pyrex and TSV devices are tested with the second-generation Synch MOD/DMOD circuitry. The ESPEC environmental chamber is controlled using GPIB and reports the chamber temperature and relative humidity. The sensor data is acquired using a NI PCI-6034E data acquisition system with a BNC-2110 breakout box. The sampling parameters and timing is shown in Table 6-6.

First, the temperature sweep is performed from 20°C to 40°C in 5°C increments, while controlling the relative humidity at 30%. In the case of the Pyrex sensor and the TSV sensor there is little dependence on changes in temperature, as shown in Figures
6-26 and 6-27, respectively. Horizontal error bars are also plotted indicating the 95% confidence interval of the data.

Table 6-6. The sampling parameters used with the environmental chamber

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensor sampling frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Number of samples per block</td>
<td>50</td>
</tr>
<tr>
<td>Dwell between blocks</td>
<td>30 seconds</td>
</tr>
<tr>
<td>Acquisition time at a given condition</td>
<td>10 minutes</td>
</tr>
</tbody>
</table>

Following temperature calibration, the sensor is exposed to varying relative humidity. The same sampling parameters are used and the temperature is held at 25°C while the humidity is swept from 40% to 80%. The results for the Pyrex device and the TSV device are shown in Figures 6-28 and 6-29, respectively.

The error in shear stress measurement due to environmental drift is quantified as

$$\text{Error [dB]} = 20\log_{10} \left( \frac{\text{predicted full scale output [mV]} - \text{maximum error [mV]}}{\text{predicted full scale output [mV]}} \right).$$  \hspace{1cm} (6-22)

The predicted full scale output is generated by using the sensitivity of the Pyrex sensors in the second-generation packaging and interfaced with the second-generation synch MOD/DMOD and the predicted full scale shear stress input of 5 Pa. The errors are quantified in Table 6-7.

Table 6-7. Results of the environmental calibration.

<table>
<thead>
<tr>
<th>Measured Quantity</th>
<th>Maximum dc Error [mV]</th>
<th>Error [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pyrex. Temperature</td>
<td>0.6</td>
<td>0.16</td>
</tr>
<tr>
<td>Pyrex. Humidity</td>
<td>0.7</td>
<td>0.19</td>
</tr>
<tr>
<td>TSV. Temperature</td>
<td>0.5</td>
<td>0.13</td>
</tr>
<tr>
<td>TSV. Humidity</td>
<td>0.8</td>
<td>0.22</td>
</tr>
</tbody>
</table>
Figure 6-26. Temperature calibration of Pyrex device.
Figure 6-27. Temperature calibration of TSV device.
Figure 6-28. Humidity calibration of Pyrex device.
Figure 6-29. Humidity calibration of TSV device with 95% confidence intervals shown.

6.3 Summary

In this chapter, the sensor system was built and tested in two generations. First a silicon-on-Pyrex sensor was interfaced with the first generation synch MOD/DMOD system and calibrated using a laminar flow cell to estimate mean sensitivity, an acoustic
plane wave tube with a sound hard boundary to estimate dynamic sensitivity, and an acoustic plane wave tube with an anechoic termination to estimate frequency response function. The sensor system demonstrated a sensitivity of 10.9 mV/Pa and a resonance of 4.7 kHz. After calibration the silicon-on-Pyrex sensor and first generation synch MOD/DMOD was demonstrated in three wind tunnel facilities, one at the University of Florida, one at NASA LaRC, and one at GALCIT.

In the second generation of testing, two new sensor calibration techniques were demonstrated and a new generation of synch MOD/DMOD was constructed. The first new calibration technique was designed to improve estimation of the frequency response function of the sensor and the second to extend sensor calibrations into the higher order effects of environmental impacts on sensor performance.

The second generation synch MOD/DMOD was then constructed and interfaced with a silicon-on-Pyrex sensor for fluidic and environmental characterization. The sensitivity of the sensor system was demonstrated as 6.5 mV/Pa. An improved frequency response function estimate was also acquired using the new variable back plate set up, demonstrating a sensor resonance of 4.9kHz and a phase shift of 180 degrees. The sensitivity of the sensor system to changes in ambient temperature or relative humidity was estimated to be less than 0.2dB full scale.

Additionally, the second generation synch MOD/DMOD was interfaced with the TSV sensors in order to validate that the humidity sensitivity of the device was eliminated by the hydrophobic coating deposited during the floating element definition. The resulting sensitivity to changes in relative humidity was estimated as 0.22 dB full
scale, indicating that the hydrophobic coating was effective in mitigating changes in sensor output due to environmental changes.

While the second-generation synch MOD/DMOD was overall successful, there are many opportunities for improvement in the current state of the sensor system as well as advancement. In the next chapter some design changes are presented for the next generation of sensor systems.
CHAPTER 7
CONCLUSIONS AND FUTURE WORK

This final chapter summarizes the contributions of this work and provides some recommendations for future efforts with this sensor.

7.1 Conclusions

The time-resolved, direct measurement of mean and dynamic wall shear stress remains one of the most elusive but important measurements in fluid dynamics. By extending upon two previous generations developed at the University of Florida, as described in Chapter 1, a shear stress measurement system capable of use in a wind tunnel environment was realized.

The design of the sensor die was extended in two ways and the fabrication of the newly designed sensor die was attempted. First, the mechanical model of the sensor was extended to include the response to out-of-plane forcing. Secondly, the floating element size and bandwidth were scaled in order to meet scaling requirements for a turbulent boundary layer. These additional components of the sensor modeling were fed into an optimization, resulting in multiple designs for fabrication. The fabrication of these optimal designs, including through silicon vias, was attempted and while unsuccessful resulted in a greater understanding of the technical challenges of this sensor production.

In order to enable the use of the sensor in a wind tunnel facility robust packaging and interface circuitry were developed. The new packaging minimizes packaging stress while decreasing the overall size of the installation to a 0.5 inch diameter, 0.75 inch long cylinder. The interface circuitry was developed making the sensor system a stand-alone instrument.
Two new calibration techniques were demonstrated in this work. The first enables a better estimation of the frequency response function of the shear stress sensor as compared to previous techniques. Additionally, the environmental impact on the sensor was characterized. The sensor system was then demonstrated in three different wind tunnel facilities. The mean sensor data was compared to multiple velocity profile based estimations of mean shear stress and the dynamic data was compared to near wall hotwires.

Finally the sensor was demonstrated in three different wind tunnel facilities. The ability of the sensor to discern between laminar and turbulent flow conditions for the same freestream velocity emphasized the importance of direct measurement. Additionally, the dynamic response of the sensor was demonstrated beyond the application of broad band turbulence and is able to detect the shedding frequency of a cylinder upstream of the sensor. The multitude of comparative measurements and flow facilities also demonstrated the success of the sensor packaging and circuitry as an adoptable wind tunnel instrument. The performance of this sensor system compared to prior work is shown in Table 7-1.

Table 7-1. Comparison of this work with selected prior MEMS floating element based shear stress measurement methods

<table>
<thead>
<tr>
<th>Sensor System</th>
<th>Element Size [mm]</th>
<th>Shear Stress Range [Pa]</th>
<th>Sensitivity [mV/Pa]</th>
<th>Calibration Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meloy</td>
<td>1</td>
<td>6.5e-3 – 3</td>
<td>6.5 - 11</td>
<td>ac/dc</td>
</tr>
<tr>
<td>Sells [35]</td>
<td>1</td>
<td>4e-3 – 3.9</td>
<td>2729 ppm/Pa</td>
<td>dc</td>
</tr>
<tr>
<td>Chandrasekharan [29]</td>
<td>2</td>
<td>14.9e-6 – 1.9</td>
<td>7.66</td>
<td>ac</td>
</tr>
<tr>
<td>Zhe [32]</td>
<td>3.2</td>
<td>0.04 – .16</td>
<td>337</td>
<td>dc</td>
</tr>
<tr>
<td>Padmanabhan [23]</td>
<td>0.5</td>
<td>1.4e-3 – 10</td>
<td>320</td>
<td>ac/dc</td>
</tr>
<tr>
<td>Schmidt [101]</td>
<td>0.5</td>
<td>0.01 – 13</td>
<td>0.47</td>
<td>dc</td>
</tr>
</tbody>
</table>
These results demonstrate that use of floating element shear stress sensors in government and academic wind tunnel environments is feasible as an instrument grade shear stress measurement system is feasible. There are still several points of the sensor and circuitry design that need improvement.

7.2 Recommendations for Future Work

There are several areas that would enhance the sensor system performance greatly. Improvements in the sensor design, fabrication, and interface circuitry are discussed in the following sections.

7.2.1 Sensor Design

To improve the sensor design, the modeling for the pressure sensitivity of the sensor and the optimization should be reevaluated. The pressure models that were developed were adapted from microphone studies [86] and do not capture the extent of the perforation of the floating element structure. This may lead to an under-prediction of the efficacy of the perforation of the element as a pressure rejection mechanism. The addition of the pressure constraint did not vary the design space of the sensor significantly. This could be due to the models used, but could also demonstrate that a single objective function does not provide enough control over the design. A multiple objective function optimization would be more capable of mapping the design space and producing truly optimal designs.

7.2.2 Sensor Fabrication

There were two major points of failure; the through silicon vias and the device release. The issue with the through silicon vias is the difficulty of aligning the TSVs through the device layer to the bulk silicon. As the device layer is configured as electrodes, there is no need for the TSVs to continue completely through the wafer.
Instead, the TSVs can extend through the BOX layer during SOI fabrication and the TSVs can simply make contact with the bottom of the device layer. Additionally, the BOX layer in this work was set at 5 μm, which is excessively large. Thinning this oxide layer to 1 μm or less and using traditional TSV fabrication techniques would also be an improvement.

This bonding approach will also assist in the release, as the cavity is formed before bonding the device layer, that will contain the sensor structure, and the bulk silicon that contains TSVs. A cross section of the final structure is shown in Figure 7-1. The difficulty in this design lies in the quality of the interface between the TSVs and the device layer and in the deep etch to form the TSVs and minimizing the uncertainty in their placement.

![Figure 7-1. A proposed sensor structure to avoid the issues found during TSV device fabrication.](image)

### 7.2.3 Third Generation Synch MOD/DMOD and Packaging

As shown in Chapter 3, there is a large source of contamination associated with the power regulation circuitry, though the overall noise floor of the system is reduced from the first-generation to the second-generation. This peak is removed through a redesign of the power distribution circuitry. The second-generation of the Synch MOD/DMOD proved that this in-package power regulation is required as the design of the system moves forward, however a more optimized power section is needed.
The packaging also requires additional design and consideration. While the cylindrical aluminum housing is a good initial point, most models and actual applications require thinner form factors. By moving to a smaller form factor buffer amplifier and possible a planar package design this thickness is minimized, but at the expense of possible sensor density.
Lumped element modeling provides a computationally simple method of predicting the dynamic response of mechanical structures. In this appendix, the details for the dynamic response of an H-bar floating element structure are derived.

**A.1 Lumped Elements for Shear Stress**

This section will derive in detail the in plane response of an H-bar floating element structure. First, the mechanical compliance will be found, followed by the mechanical mass. Finally additional components of the model will be derived, including the coupling coefficient that describes the transfer of energy from the mechanical structure into the electrical domain. A circuit diagram of the model is shown in Figure A-1.

![Circuit Diagram](image)

**Figure A-1.** Full lumped element model of the floating element response to an input shear stress

**A.1.1 Lumped Mechanical Compliance**

The mechanical compliance of the structure is lumped by evaluating the total potential energy of the system,
\[ W_{PE} = \int dW'_{PE} = \int_0^q e dq = \frac{1}{2} \frac{w^2 (L_t)}{C_{ME}}, \]  

(A-1)

where \( e \) is effort, or the total force, \( F \), acting on the beam and \( q \) is displacement, \( w(x) \).

The total force acting on the beam is

\[ F = \int_0^L \left( Q + \frac{P}{2} \delta(x - L_t) \right) dx. \]  

(A-2)

The potential energy of one tether can then be represented as

\[ W_{PE} = \int_0^L \int_0^{w(x)} \left( Q + \frac{P}{2} \delta(x - L_t) \right) dw(x) dx \]  

(A-3)

or

\[ W_{PE} = \int_0^L \int_0^{w(x)} \tau_w \left( \tau_0 + \left( \frac{W_e L_t}{4} + \frac{NW_0 L_t}{4} \right) \delta(x - L_t) \right) dw(x) dx. \]  

(A-4)

Substituting in for \( \tau_w \)

\[ W_{PE} = \int_0^L \int_0^{w(x)} \frac{4ET_0 W_t^2}{w(x)} \left( \tau_0 + \left( \frac{W_e L_t}{4} + \frac{NW_0 L_t}{4} \right) \delta(x - L_t) \right) dw(x) dx \]  

(A-5)

or

\[ W_{PE} = \int_0^L \frac{4ET_0 W_t^2}{2} \left( \tau_0 + \left( \frac{W_e L_t}{4} + \frac{NW_0 L_t}{4} \right) \delta(x - L_t) \right) \frac{w^2(x)}{2} dx. \]  

(A-6)

To remove the \( w(x) \) dependence, combine and equate in terms of shear to produce
\[
\begin{align*}
    w_{tw}(x) &= w_{tw}(L_t) \left( \frac{3(L_e W_e L_t + NW_i L_i L_t) + 8W_i L_t^2}{L_e W_e L_t^3 + NW_i L_i L_t^3 + 2W_i L_t^4} \right) x^2 \\
    &\quad - \left( \frac{2L_e W_e + 2NW_i L_t}{L_e W_e L_t^3 + NW_i L_i L_t^3 + 2W_i L_t^4} \right) x^3 + \frac{2W_i x^4}{L_e W_e L_t^3 + NW_i L_i L_t^3 + 2W_i L_t^4}.
\end{align*}
\]  

(A-7)

This is used to simplify the integration to give

\[
W_{PE} = \int_0^L \left( \frac{3(L_e W_e L_t + NW_i L_i L_t) + 8W_i L_t^2}{L_e W_e L_t^3 + NW_i L_i L_t^3 + 2W_i L_t^4} \right) \frac{w_{tw}^2(L_t)}{2} dx
\]

(A-8)

and an integration over \( x \) results in.

\[
W_{PE} = \frac{ET_i W_t^3}{W_e} \left( W_t + \left( \frac{W_e L_e}{4} + \frac{NW_i L_i}{4} \right) \right) \left( \frac{3(L_e W_e L_t + NW_i L_i L_t) + 8W_i L_t^2}{L_e W_e L_t^3 + NW_i L_i L_t^3 + 2W_i L_t^4} \right) \frac{w_{tw}^2(L_t)}{2}.
\]

(A-9)

The total system potential energy will be four times the above \( W_{PE} \) as until now only one tether has been considered. The total potential energy is described by

\[
W_{PE} = 4ET_i \left( \frac{W_t}{L_t} \right)^3 + \frac{4NW_i L_i W_t L_t + (NW_i L_t)^2}{W_e} + \frac{65}{15} (W_i L_t)^2 \]

(A-10)

\[
\left( 1 + \frac{NW_i L_t}{W_t L_t + 2 \left( \frac{W_t}{W_e} \right)^2} \right) \frac{w_{tw}^2(L_t)}{2}.
\]

From this the compliance is found,
A.1.2 Lumped Mechanical Mass

The mass of a system is lumped by evaluating the total kinetic energy of the moving beam and equating it to the kinetic energy stored in a mass

\[
W_{KE} = \int dW_{KE} = \int_0^b pf \, df = \frac{1}{2} M_{ME} f_0^2,
\]

where \( p \) represents momentum and \( f \) represents flow.

For this floating element sensor, kinetic energy is stored in both the tethers and the floating element. The total lumped mass is found by finding the kinetic energy stored in each structure. This is achieved by finding the lumped element associated with the floating element and the tethers separately by the above equation and then summing those two masses

\[
M = M_{ME\text{lumped}} + M_{ME\text{element}}.
\]

The flow in this is velocity that is represented as

\[
v(x) = j\omega w(x)
\]

and the velocity at \( x = L_t \) is

\[
v(L_t) = j\omega w(L_t).
\]

Combining these to remove dependence on \( \omega \) shows
\[ v(x) = \frac{v(L_i)}{w(L_i)} w(x). \quad (A-16) \]

Considering a differential element of the tether that has a differential mass,

\[ dm = \rho T_t W_t dx, \quad (A-17) \]

the momentum of that differential element is

\[ p = dm v(x) = \rho T_t W_t v(x) dx. \quad (A-18) \]

The differential kinetic co-energy is therefore

\[ dW^*_{KE} = \rho T_t W_t dx v(x) dv(x) \quad (A-19) \]

or

\[ W^*_{KE} = \int_0^L \rho T_t W_t dx v(x) dv(x) \quad (A-20) \]

or

\[ W^*_{KE} = \int_0^L \rho T_t W_t \frac{v^2(x)}{2} dx. \quad (A-21) \]

Substituting for \( v(x) \)

\[ W^*_{KE} = \int_0^L \rho T_t W_t \frac{v^2(L_i) w^2(x)}{2w^2(L_i)} dx \quad (A-22) \]

or

\[ W^*_{KE} = \rho T_t W_t \frac{v^2(L_i)}{2w^2(L_i)} \int_0^L w^2(x) dx. \quad (A-23) \]

Equating this to the generalized form for kinetic co-energy the lumped mass of the tethers is

\[ M_{ME,\text{tether}} = \frac{\rho T_t W_t}{w^2(L_i)} \int_0^L w^2(x) dx. \quad (A-24) \]
Again, this is only considering one tether. In order to find the total kinetic co-energy the above value is multiplied by 4 to give

\[ M_{\text{ME tether}} = 4 \int_0^{L_t} \frac{\rho T_i W_i L_i}{W^2(x)} dx. \]  \hfill (A-25)

The kinetic co-energy of the floating element is more straight-forward as

\[ M_{\text{ME element}} = \rho (W_e L_e + NW_i L_i) T_i. \]  \hfill (A-26)

Combining these two masses the total lumped mass of the system is

\[ M_{\text{ME}} = M_{\text{ME tether}} + M_{\text{ME element}} = 4 \int_0^{L_t} \frac{\rho T_i W_i L_i}{W^2(L_t)} w^2(x) dx + \rho (W_e L_e + NW_i L_i) T_i. \]  \hfill (A-27)

Substituting for \( w(L_i) \) and evaluating the integral using MATLAB.

\[
M_{\text{ME}} = \rho T_i L_e W_e \left( \frac{1}{2} + \frac{192}{35} \left( \frac{W_i L_i}{W_e L_e} \right) + 3 \left( \frac{NW_i L_i}{W_e L_e} \right) + \frac{384}{35} \left( \frac{W_i L_i}{W_e L_e} \right) \left( \frac{NW_i L_i}{W_e L_e} \right) \right) \\
+ \frac{1072}{105} \left( \frac{W_i L_i}{W_e L_e} \right)^2 + 3 \left( \frac{NW_i L_i}{W_e L_e} \right)^2 + \frac{1072}{105} \left( \frac{W_i L_i}{W_e L_e} \right)^2 \left( \frac{NW_i L_i}{W_e L_e} \right) \\
+ 3 \left( \frac{NW_i L_i}{W_e L_e} \right)^2 \left( \frac{W_i L_i}{W_e L_e} \right) + \frac{2048}{315} \left( \frac{W_i L_i}{W_e L_e} \right)^3 + \frac{NW_i L_i}{W_e L_e} \right)^3 \\
\right). \]  \hfill (A-28)

\textbf{A.2 Two-Port Model}

In this section, the method where transduction is accounted for in the lumped element model is discussed. The characteristic equations of a linear transducer are

\[ V = Z_{\text{EB}} I + T_{\text{EM}} U \]
\[ F = T_{\text{ME}} I + Z_{\text{MO}} U \]  \hfill (A-29)

In a reciprocal transducer \( T_{\text{EM}} = T_{\text{ME}} \). In a direct transducer \( Z_{\text{EB}} = Z_{\text{MO}} \).
These equations are represented as a transformer with either an open mechanical impedance and free electrical impedance or a blocked electrical impedance and a shorted mechanical impedance as seen in Figure A-2.

The impedances are related by

$$Z_{MS} = (1 - \kappa^2)Z_{MO}$$  \hspace{1cm} (A-30)

and

$$Z_{EF} = (1 - \kappa^2)Z_{EB}$$  \hspace{1cm} (A-31)

where

$$\kappa^2 = \frac{T^2}{Z_{EB}Z_{MO}}.$$  \hspace{1cm} (A-32)

Figure A-2. Generalize circuit representation for a two-port transducer model

For this implementation, the sensor is modeled as a parallel plate capacitor with varying gap, \( g \). Nominally the gap is \( x_0 \) and the change in gap is represented as

$$x(t) = x_0 - x'(t).$$  \hspace{1cm} (A-33)

The capacitance as a function of time can therefore be represented as

$$C_E(t) = \frac{\epsilon_0}{x(t)} = \frac{\epsilon_0 A}{x_0 - x'(t)} = \frac{\epsilon_0 A}{x_0} \left( 1 - \frac{x'(t)}{x_0} \right)^{-1} = C_{EB} \left( 1 - \frac{x'(t)}{x_0} \right)^{-1},$$  \hspace{1cm} (A-34)
where \( C_{EB} \) is the capacitance when the plate has zero displacement.

The total force on the movable plate is the sum of the electrostatic force and the mechanical restoring force

\[
F_{\text{total}} = F_M + F_E. \tag{A-35}
\]

The electrostatic force of two plates with constant charge is

\[
F_E = -\frac{1}{2} \frac{Q^2}{C_{EB} x_0}. \tag{A-36}
\]

The voltage due to this charge is expressed by

\[
V(t) = -\frac{Q(t)}{C_E(t)} = \frac{Q(t)}{C_{EB}} \left( 1 - \frac{x'(t)}{x_0} \right). \tag{A-37}
\]

The mechanical restoring force is related to the compliance of the system as

\[
F_M = k x'(t) = \frac{x'(t)}{C_{MO}}. \tag{A-38}
\]

This brings the total force to

\[
F_{\text{total}} = F_M + F_E = \frac{x'(t)}{C_{MO}} - \frac{1}{2} \frac{Q^2}{C_{EB} x_0}. \tag{A-39}
\]

The equations for force and voltage are linearized by assuming a small perturbation and then representing the resulting equations as a two-port network in terms of Fourier components to

\[
V(t) = \frac{Q'(t)}{C_{EB}} - \frac{V_0 x'(t)}{x_0} \tag{A-40}
\]

\[
F(t) = \frac{x'(t)}{C_{MO}} - \frac{V_0 Q'(t)}{x_0}
\]

This shows that the transducer is reciprocal, but not direct. For a reciprocal transducer the impedance transformation factor is
\[
\phi = \frac{T}{Z_{EB}} \quad \text{(A-41)}
\]

or

\[
\phi' = \frac{T}{Z_{MO}} = -\frac{V_0}{X_0} C_{MO} \cdot \text{(A-42)}
\]

In order to fit to the two-port chosen, \( Z_{EB} \) must be transformed to a blocked electrical impedance by the electromechanical coupling factor

\[
\kappa = \frac{T^2}{Z_{EB} Z_{MO}} = \frac{V^2}{X_0^2} C_{EB} C_{MO} \cdot \text{(A-43)}
\]

So \( C_{EB} \) is transformed into a series impedance \( C_{EF} \) as

\[
\frac{1}{j\omega C_{EF}} = (1 - \kappa^2) \frac{1}{j\omega C_{EB}}. \quad \text{(A-44)}
\]
Lumped element modeling provides a computationally simple method of predicting the dynamic response of mechanical structures. In this appendix, the details for the dynamic response of an H-bar floating element structure are derived.

B.1 Lumped Element Parameters

This section will derive in detail the out of plane response of an H-bar floating element structure. First, the mechanical compliance will be found, followed by the mechanical mass. Finally additional components of the model will be derived, including the coupling coefficient that describes the transfer of energy from the mechanical structure into the electrical domain. A circuit diagram of the model is shown in Figure B-1.

Figure B-1. Circuit representation of the lumped element model for the out of plane response of an H-bar structure.
B.1.1 Lumped Mechanical Compliance

The derivation of the lumped compliance given a pressure input closely follows the method used to derive the response to shear. Under pressure, as under shear, the floating element is considered perfectly rigid. This means that each pair of tethers are viewed as a clamped-clamped beam with the floating element motion represented as a point force in the middle.

The force on one set of tethers with respect to pressure, \( p \), is represented as a distributed force, \( Q \), and a point force, \( P \), that is the result of the floating element.

\[
P = \frac{pW_xL_t}{2} + \frac{pNW_iL_t}{2} \quad \text{(B-1)}
\]

From the analysis of beam deflection the total displacement equation with respect to pressure is nearly identical to that of shear

\[
\begin{align*}
 w(x) = & -\frac{p}{EI} \left[ \frac{3 (L_x W_x L_t + NW_i L_t L_t)}{48} x^2 + \frac{(L_x W_x + NW_i L_t + 4W_i L_t)}{24} x^3 + \frac{W_i x^4}{24} \right], \\
 & \text{with the exception that the expression for the moment of inertia changes to.} \\
 & I = \frac{W_i T_t^2}{12}. \quad \text{(B-3)}
\end{align*}
\]

Making the displacement equation with respect to pressure.

\[
\begin{align*}
 w(x) = & -\frac{p}{4E W_i T_t^3} \left[ (3(L_x W_x L_t + NW_i L_t L_t) + 8W_i L_t^2) x^2 -(2L_x W_x + 2NW_i L_t + 8W_i L_t) x^3 + 2W_i x^4 \right],
\end{align*}
\]

where maximum displacement occurs at \( x = L_t \)

\[
\begin{align*}
 w(L_t) = & -\frac{p}{4E W_i T_t^3} \left[ L_x W_x L_t^3 + NW_i L_t^3 + 2W_i L_t^4 \right]. \quad \text{(B-5)}
\end{align*}
\]

The displacement equation in terms of this maximum displacement is.
Pressure in terms of the displacement equation is

\[ p = \frac{-w(x)4EW_iT_i^3}{(3(L_wW_i + NW_iL_i) + 8W_iL_i^2)x^2 - (2L_wW_i + 2NW_iL_i + 8W_iL_i)x^3 + 2W_i x^4}. \] 

In order to find the lumped mechanical compliance of the structure with respect to incident pressure the potential co-energy is evaluated as was done in the case for a response to shear. Following the same procedure results in

\[ W_{PE} = \int_0^{L_w} \int_0^{w(x)} \left\{ \begin{array}{l} -w(x)4EW_iT_i^3 \left( 4W_i + W_eL_e + NW_iL_i \right) \\ \left( 3(L_wW_i + NW_iL_i) + 8W_iL_i^2 \right)x^2 \\ \left( -2L_wW_i + 2NW_iL_i + 8W_iL_i \right)x^3 + 2W_i x^4 \end{array} \right\} \delta(x - L_i) dw(x) dx . \] 

Substituting in for pressure shows

\[ W_{PE} = \int_0^{L_w} \int_0^{w(x)} \frac{-w(x)4EW_iT_i^3 \left( 4W_i + W_eL_e + NW_iL_i \right)}{\left( 3(L_wW_i + NW_iL_i) + 8W_iL_i^2 \right)x^2} \delta(x - L_i) dw(x) dx . \] 

Integrating over \(w(x)\) and simplifying produces

\[ W_{PE} = \frac{\left( 3(L_wW_i + NW_iL_i) + 8W_iL_i^2 \right)x^2}{2 \left( -2L_wW_i + 2NW_iL_i + 8W_iL_i \right)x^3 + 2W_i x^4} \] 

and integrates to

\[ W_{PE} = \frac{-4EW_iT_i^3 \left( 4W_i + W_eL_e + NW_iL_i \right)}{W_eL_e^2 \left( 1 + \frac{NW_iL_i}{W_eL_e} + \frac{2W_iL_i}{W_eL_e} \right)^2} \frac{w^2(L_i)}{2} \left[ \frac{L_wW_iL_i^4}{4} + \frac{NW_iL_i^4}{4} + \frac{22W_iL_i^4}{15} \right] \] 

or

\[ W_{PE} = \frac{-4EW_iT_i^3 \left( 4W_i + W_eL_e + NW_iL_i \right)}{W_eL_e^2 \left( 1 + \frac{NW_iL_i}{W_eL_e} + \frac{2W_iL_i}{W_eL_e} \right)^2} \frac{w^2(L_i)}{2} \left[ \frac{L_wW_iL_i^4}{4} + \frac{NW_iL_i^4}{4} + \frac{22W_iL_i^4}{15} \right]. \]
\[ W_{PE} = \frac{1}{2} w^2 (L) \left\{ -4EwT^3 \left( 4w + w_L + NW_L \right) [15(w_L w_e + NW_L w_e) + 88w_L w_e] \right\}. \] \tag{B-12}

The negative sign is just a function of the sign convention chosen when choosing the deflection direction and is disregarded. By comparing this to the original expression for potential energy

\[ C_{ME_{\text{pressure}}} = \frac{60w^2L^2}{4EwT^3 \left( 4w + w_L + NW_L \right) [15(w_L w_e + NW_L w_e) + 88w_L w_e]^2} \]. \tag{B-13}

**B.1.2 Lumped Mechanical Mass**

The lumped mass of the sensor response with respect to pressure directly follows the derivation for that of shear. The final solution for lumped mass is repeated below for thoroughness.

\[
M_{ME_{\text{pressure}}} = M_{ME} = \frac{\rho T_L w_e}{1 + \frac{192}{35} \left( \frac{w_L}{w_e} \right) + 3 \left( \frac{NW_L}{w_e} \right) + \frac{384}{35} \left( \frac{w_L}{w_e} \right) \left( \frac{NW_L}{w_e} \right) + \frac{1072}{105} \left( \frac{w_L}{w_e} \right)^2 + 3 \left( \frac{NW_L}{w_e} \right)^2 + \frac{1072}{105} \left( \frac{w_L}{w_e} \right)^2 \left( \frac{NW_L}{w_e} \right) + 3 \left( \frac{NW_L}{w_e} \right)^2 \left( \frac{w_L}{w_e} \right) + \frac{2048}{315} \left( \frac{w_L}{w_e} \right)^3 + \left( \frac{NW_L}{w_e} \right)^3 \left( 1 + \frac{NW_L}{w_e} \right)^2 + 2 \left( \frac{w_L}{w_e} \right)^2 \right) \]. \tag{B-14}

**B.1.3 Lumped Acoustic Compliance**

The lumped approximation for cavity compliance is \[ ] \tag{B-15}
where $V$ is the volume of the cavity.

**B.1.4 Lumped Acoustic Dissipation**

The squeeze film damping of the fluid moving through the perforations in the floating element and the spaces between the comb fingers will act as a resistive element. Following the procedure used to develop a perforated diaphragm capacitive microphone, that uses models developed by Skvor [39] and Homentcovschi [40] to predict the resistance,

$$R_{AC} = \frac{72 \mu_{t_{air}} T n_h}{(L_e W_o)^2 A_r^2}$$  \hspace{1cm} (B-16)

where $n_h$ is the number of holes in the element and $A_r$ is the ratio of the area of the holes to the area of the floating element.

**B.2 Two-Port Model**

The characteristic equations of a linear transducer are

$$V = Z_{EB} I + T_{EM} U$$

$$F = T_{ME} I + Z_{MO} U.$$  \hspace{1cm} (B-17)

In a reciprocal transducer $T_{ME} = T_{EM}$. In a direct transducer $Z_{EB} = Z_{MO}$.

For this implementation, the sensor is modeled as a parallel plate capacitor with varying overlapping area. Nominally the area is $A_0$ and the change in area is represented as

$$A(t) = A_0 - A'(t) = ab_0 - ab'(t)$$  \hspace{1cm} (B-18)

Where $a$ is the width of the overlapping area and $b'(t)$ is the height of the overlapping area, that is what is changing in time. The capacitance as a function of time is
where \(C_{EB}\) is the capacitance when the plate has zero displacement.

The total force on the movable plate is the sum of the electrostatic force and the mechanical restoring force

\[
F_{\text{total}} = F_M + F_E. \tag{B-20}
\]

The electrostatic force of two plates with constant charge is

\[
F_E = -\frac{1}{2} \frac{Q^2}{\varepsilon A_0}. \tag{B-21}
\]

The voltage due to this charge is expressed by

\[
V(t) = -\frac{Q(t)}{C_E(t)} = \frac{Q(t)}{C_{EB}} \left(1 - \frac{A(t)}{A_0}\right)^{-1} = \frac{Q(t)}{C_{EB}} \left(1 - \frac{b'(t)}{b_0}\right)^{-1}. \tag{B-22}
\]

The mechanical restoring force is related to the compliance of the system as

\[
F_M = k b'(t) = \frac{b'(t)}{C_{MO}}. \tag{B-23}
\]

This brings the total force to

\[
F_{\text{total}} = F_M + F_E = \frac{b'(t)}{C_{MO}} \frac{1}{2} \frac{Q^2}{\varepsilon A_0}. \tag{B-24}
\]

The equations for force and voltage are linearized by assuming a small perturbation and then representing the resulting equations as a two-port network in terms of Fourier components to

\[
V(t) = \frac{Q(t)}{C_{EB}} + \frac{V_0 b'(t)}{b_0}, \tag{B-25}
\]

\[
F(t) = \frac{b'(t)}{C_{MO}} + \frac{V_0 Q(t)}{b_0}
\]

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This shows that the transducer is reciprocal, but not direct. For a reciprocal transducer the impedance transformation factor is

\[ \phi = \frac{T}{Z_{MO}} = -\frac{V_a}{b_0} C_{MO}. \]  

(B-26)

In order to fit to the two-port chosen \( Z_{EB} \) must be transformed to a blocked electrical impedance by the electromechanical coupling factor

\[ \kappa = \frac{T^2}{Z_{EB} Z_{MO}} = \frac{V^2}{b_0^2} C_{EB} C_{MO}, \]  

(B-27)

so \( C_{EB} \) is transformed into a series impedance \( C_{EF} \) as

\[ \frac{1}{j\omega C_{EF}} = (1 - \kappa^2) \frac{1}{j\omega C_{EB}}. \]  

(B-28)
APPENDIX C
DERIVATION OF PARASITIC CONTRIBUTIONS FOR UNITY GAIN AMPLIFIER

The output voltage of this system is found using superposition. The effects of the amplifier parasitics will become evident in this analysis. In this representation $C_p$ represents parasitic capacitances of bondpads, packaging, and any other capacitance that does not contribute to the sensor or is due to the amplifier input stage, $C_i$ represents the input capacitance of the chosen op amp and is specified by the manufacturer, and $R_b$ is a discrete resistance value that is required in order for the op amp to define a quiescent point around where it operates.

First, consider the contribution of the positive bias voltage on the output voltage. Considering the positive bias only results in

\[
V_{\text{out}1} = V_{\text{bias}} \frac{C_i}{C_1 + C_2 + C_p + C_i + \frac{1}{j\omega R_b}}.
\]

(C-1)

Figure C-1. Contribution of positive bias to output
Now considering contributions from the negative bias voltage

\[ V_{out2} = -V_{bias} \frac{C_2}{C_1 + C_2 + C_p + C_i + \frac{1}{j\omega R_b}}. \]  

(C-2)

Combining these equations results in

\[ V_{out} = V_{bias} \frac{C_1}{C_1 + C_2 + C_p + C_i + \frac{1}{j\omega R_b}} - V_{bias} \frac{C_2}{C_1 + C_2 + C_p + C_i + \frac{1}{j\omega R_b}}. \]  

(C-3)

or

\[ V_{out} = V_{bias} \frac{j\omega R_b (C_1 - C_2)}{j\omega R_b (C_1 + C_2 + C_p + C_i)} + 1. \]  

(C-4)

This shows the output voltage has a high pass characteristic based on device capacitance and bias resistance. Past the system cut-on, \( \omega R_b (C_1 + C_2 + C_p + C_i) \gg 1 \), the output voltage simplifies to

\[ V_{out} = V_{bias} \frac{C_1 - C_2}{C_1 + C_2 + C_p + C_i}. \]  

(C-5)
Now considering that $C_1$ and $C_2$ is described as $C_1 = C_0 - \Delta C$ and $C_2 = C_0 + \Delta C$
equation C.5 is further reduced to

$$V_{out} = V_{bias} \frac{(C_0 - \Delta C) - (C_0 + \Delta C)}{C_0 - \Delta C + C_0 + \Delta C + C_p + C_i} \quad (C-6)$$

or

$$V_{out} = V_{bias} \frac{2\Delta C}{2C_0 + C_p + C_i} \quad (C-7)$$
There are three noise sources present; the thermal noise of a required external bias resistor, the input referred voltage noise of the amplifier, and the current noise of the amplifier. Again, superposition is used to determine the contribution of each source.

First, consider the voltage noise of the amplifier.

Figure D-1. Total noise model for a unity gain amplifier with bias resistor

Figure D-2. Noise circuit for amplifier voltage noise.
In this case the impedance at the input of the amplifier does not contribute to the output and $V_{out1} = v_n$.

Next, consider the current noise of the amplifier.

![Noise circuit for amplifier current noise.](image)

Figure D-3. Noise circuit for amplifier current noise.

In this case, $Z_{in}$ will shape the output voltage of the amplifier due to the input noise source. The noise current, $i_n$, flows through the impedance seen at the input of the op amp,

$$Z_{in} = \frac{R_b}{j\omega R_b(C_i + C_p + C_1 + C_2) + 1}$$  \hspace{1cm} (D-1)

creating a voltage at the non-inverting op-amp input. The output due to the current noise of the op amp is

$$V_{out2} = i_n \frac{R_b}{j\omega R_b(C_i + C_p + C_1 + C_2) + 1}.$$  \hspace{1cm} (D-2)

The final noise source is the thermal noise of the bias resistor and is

$$V_{out3} = v_r \frac{1}{j\omega R_b(C_i + C_p + C_1 + C_2) + 1}.$$  \hspace{1cm} (D-3)
Figure D-4. Noise circuit for resistor thermal noise.
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<th>Value</th>
<th>Digike Part No</th>
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APPENDIX E
PARTS LIST AND FULL SCHEMATIC FOR FIRST-GENERATION SYNCH MOD/DMOD

Table E-1. Parts list for the first-generation Synch MOD/DMOD circuitry.
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<th>Description</th>
<th>Value</th>
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Figure E-1. Schematic for the first-generation Synch MOD/DMOD circuitry.
## APPENDIX F

PARTS LIST AND FULL SCHEMATIC FOR SECOND-GENERATION SYNCH MOD/DMOD

Table F-1. Parts list for the second-generation Synch MOD/DMOD circuitry.

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Figure F-1. Schematic for the second-generation Synch MOD/DMOD circuitry.
APPENDIX G
PROCESS TRAVELER FOR FABRICATION OF TSV DEVICES

In this appendix, the details of device fabrication, including a description of the raw materials used, is given. Each step is shown in Figure G-1 and indicated by a letter a-s, which corresponds to a specific step in the process traveler. This fabrication was performed at the Nanoscale Research Facility at the University of Florida.

Wafer Details.

Processing begins with 100 mm +/- 0.1 mm diameter <1−0−0> +/- 0.5 degree SOI wafer with overall thickness of 595 μm +/- 10 μm. The device layer is 45 μm +/- 1μm thick and doped with Boron for a resistivity of 0.001 Ω-cm - 0.005 Ω-cm. The buried oxide layer (BOX) is a 5 μm +/- 5% thick thermal oxide grown on the handle. The handle wafer is 550 μm +/- 10 μm thick and doped with Boron for a resistivity of > 1,000 Ω-cm. The wafers are purchased from Ultrasil Corporation and shipped to Icemos Technology for fabrication of the TSVs. Following this fabrication there is a 1 μm oxide on the front side of the wafers and a 5 μm oxide on the back side of the wafer. The fabrication included in this section assumes wafers at this state of development.

Masks.

1) Back-side Oxide Etch
2) Back-side Aluminum Etch
3) Back-side Nitride Etch
4) Front-side Oxide Etch
5) Front-side Aluminum Etch
6) Floating Element Etch

Figure G-1. The process flow for fabricating the capacitive shear stress sensors with TSVs (not to scale).

**Process Steps.**

1) Clean Wafers (a)
   
   a. SC1 clean. $5:1:1 \text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{NH}_4\text{OH}$ at 75 C for 10 minutes followed by a triple rinse in deionized (DI) water.
b. SC2 clean. 5:1:1 H₂O:H₂O₂:NH₂OH at 75 C for 10 minutes followed by a triple rinse in DI water.

2) Define Back-Side Aluminum Pads

a. Remove native oxide over TSVs (b)

i. Protect front-side of wafer

1. HMDS coat wafer.
   a. 3 minute dehydration bake on hot plate.
   b. 30 second HMDS vapor dispense.
   c. 2 minute post bake on hot plate.

2. Spin 1.23 μm Shipley 1813 photoresist using Delta 80 on front of wafer.

3. Hard bake at 120C for 20 minutes in Despatch oven.

ii. Spin Photoresist.

1. HMDS coat wafer.
   a. 3 minute dehydration bake on hot plate.
   b. 30 second HMDS vapor dispense.
   c. 2 minute post bake on hot plate.

2. Spin 1.23 μm Shipley 1813 photoresist using Delta 80.

3. Soft bake photoresist on hot plate for 2 minutes.

iii. Align and Expose with Mask 1.

1. Front-to-back alignment to Icemos alignment marks.

2. Expose using EVG620 for 2.6 seconds.

3. Develop for 1 minute in AZ 300MIF developer.
iv. Etch oxide.
   1. Etch in 6.1 Buffered Oxide Etch (BOE) for 8 minutes.

v. Strip Photoresist.
   1. Place in PG Photoresist Remover at 75 C for 15 minutes.
   2. Triple Rinse in DI water.

b. Deposit and pattern metal pads.
   i. Protect front-side of wafer (c)
      1. HMDS coat wafer.
         a. 3 minute dehydration bake on hot plate.
         b. 30 second HMDS vapor dispense.
         c. 2 minute post bake on hot plate.
      2. Spin 1.23 µm Shipley 1813 photoresist using Delta 80 on front of wafer.
      3. Hard bake at 120C for 20 minutes in Despatch oven.
   ii. HF Dip to remove native oxide
      1. Dip in 50:1 DI:HF for 30 seconds.
   iii. Deposit aluminum/silicon 2% (d)
      1. Deposit 0.5 µm Al/Si 2% using recipe G4_200_5 on the KJL CMS-18 Sputter Deposition tool.
   iv. Strip Photoresist.
      1. Place in PG Photoresist Remover at 75 C for 15 minutes.
      2. Triple Rinse in DI water.
   v. Pattern Aluminum pads (e)
1. Spin Photoresist.
   a. HMDS coat wafer.
      i. 3 minute dehydration bake on hot plate.
      ii. 30 second HMDS vapor dispense.
      iii. 2 minute post bake on hot plate.
   b. Spin 1.23 μm Shipley 1813 photoresist using Delta 80.
   c. Soft bake photoresist on hot plate for 2 minutes.

2. Align and Expose with Mask 2.
   a. Front-to-back alignment to Icemos alignment marks.
   b. Expose using EVG620 for 2.6 seconds.
   c. Develop for 1 minute in AZ 300MIF developer.

3. Etch Al/Si 2%.
   a. Etch in Transene 80 Type A for 8 minutes while agitating bath.

vi. Strip Photoresist. (f)
   1. Place in PG Photoresist Remover at 75 C for 15 minutes.
   2. Triple Rinse in DI water.

c. Deposit and pattern nitride passivation on back-side of wafer.
   i. Deposit 600 Å of SiN using mn500a.set on the STS 310PC PECVD.
      (g)
   ii. Spin Photoresist.
      1. HMDS coat wafer.
         a. 3 minute dehydration bake on hot plate.
b. 30 second HMDS vapor dispense.

c. 2 minute post bake on hot plate.

2. Spin 1.44 μm Shipley 1813 photoresist using Delta 80.

3. Soft bake photoresist on hot plate for 2 minutes.

iii. Align and Expose with Mask 3. (h)

1. Front-to-front alignment to alignment marks in bottom metal.

2. Expose using MA6 for 2.6 seconds for a final dose of 115 mJ/cm².

3. Develop for 1 minute in AZ 300MIF developer.

4. Hard bake in Despatch oven for 20 minutes at 120C.

iv. Etch nitride. (i)

1. Clean edges of wafer using acetone

2. Etch using “slow nitride” recipe on Trion RIE for 102 seconds.

v. Strip Photoresist. (j)

1. Place in PG Photoresist Remover at 75 C for 15 minutes.

2. Triple Rinse in DI water.

3) Define Front-Side Aluminum Pads

a. Remove native oxide over TSVs (k)

i. Protect back-side of wafer

1. HMDS coat wafer.

a. 3 minute dehydration bake on hot plate.

b. 30 second HMDS vapor dispense.

b. 2 minute post bake on hot plate.
2. Spin 1.23 μm Shipley 1813 photoresist using Delta 80 on back of wafer.

3. Hard bake at 120C for 20 minutes in Despatch oven.

ii. Spin Photoresist.
   1. HMDS coat wafer.
      a. 3 minute dehydration bake on hot plate.
      b. 30 second HMDS vapor dispense.
      c. 2 minute post bake on hot plate.
   2. Spin 1.23 μm Shipley 1813 photoresist using Delta 80.
   3. Soft bake photoresist on hot plate for 2 minutes.

iii. Align and Expose with Mask 4.
   1. Front-to-back alignment to Icemos alignment marks.
   2. Expose using EVG620 for 2.6 seconds.
   3. Develop for 1 minute in AZ 300MIF developer.

iv. Etch oxide. (k)
   1. Etch in 6.1 Buffered Oxide Etch (BOE) for 8 minutes.

v. Strip Photoresist.
   1. Place in PG Photoresist Remover at 75 C for 15 minutes.
   2. Triple Rinse in DI water.

b. Deposit and pattern metal pads.
   i. Protect back-side of wafer
      1. HMDS coat wafer.
         a. 3 minute dehydration bake on hot plate.
b. 30 second HMDS vapor dispense.

c. 2 minute post bake on hot plate.

2. Spin 1.23 \( \mu m \) Shipley 1813 photoresist using Delta 80 on back of wafer.

3. Hard bake at 120C for 20 minutes in Despatch oven.

ii. HF Dip to remove native oxide (l)

1. Dip in 50:1 DI:HF for 30 seconds.

iii. Deposit aluminum/silicon 2% (m)

1. Deposit 0.5 \( \mu m \) Al/Si 2% using recipe G4_200_5 on the KJL CMS-18 Sputter Deposition tool.

iv. Pattern Aluminum pads

1. Protect back-side of wafer

   a. HMDS coat wafer.

      i. 3 minute dehydration bake on hot plate.

      ii. 30 second HMDS vapor dispense.

      iii. 2 minute post bake on hot plate.

   b. Spin 1.23 \( \mu m \) Shipley 1813 photoresist using Delta 80 on back of wafer.

   c. Hard bake at 120C for 20 minutes in Despatch oven.

2. Spin Photoresist.

   a. HMDS coat wafer.

      i. 3 minute dehydration bake on hot plate.

      ii. 30 second HMDS vapor dispense.
iii. 2 minute post bake on hot plate.
   
   b. Spin 1.23 μm Shipley 1813 photoresist using Delta 80.

   c. Soft bake photoresist on hot plate for 2 minutes.

3. Align and Expose with Mask 5. (n)
   
   a. Front-to-back alignment to alignment marks in backside aluminum.

   b. Expose using EVG620 for 2.6 seconds.

   c. Develop for 1 minute in AZ 300MIF developer.

4. Etch Al/Si 2%. (o)
   
   a. Etch in Transene 80 Type A for 8 minutes while agitating bath.

5. Strip Photoresist.
   
   1. Place in PG Photoresist Remover at 75 C for 15 minutes.

   2. Triple Rinse in DI water.

4) Electrical test and anneal
   
   a. Electrically characterize TSV connections using an Agilent 4155C.

   b. Anneal at 450C in forming gas until ohmic.

5) Define and release floating element
   
   a. Protect back-side of wafer and attach carrier wafer

      i. HMDS coat blank test wafer.

         1. 3 minute dehydration bake on hot plate.

         2. 30 second HMDS vapor dispense.

         3. 2 minute post bake on hot plate.
ii. Spin $10.7 \, \mu m$ AZ 9260 on test wafer.

iii. Attach back side of processed wafer to test wafer and bake on a hotplate at 112C for 5 minutes.

b. Pattern floating elements

i. Spin Photoresist.

1. HMDS coat wafer.
   a. 3 minute dehydration bake on hot plate.
   b. 30 second HMDS vapor dispense.
   c. 2 minute post bake on hot plate.

2. Spin $1.89 \, \mu m$ Shipley 1813 photoresist using Delta 80.

3. Soft bake photoresist on hot plate for 2 minutes.

ii. Align and Expose with Mask 6. (p)

1. Front-to-front alignment to alignment marks in aluminum.

2. Expose using MA6 for 19.5 seconds.

3. Develop for 1 minute in AZ 300MIF developer.

4. Hard bake in Despatch oven at 120C for 20 minutes

5. Ash hard baked wafer in Anatech barrel asher for 60 seconds at 300W and 300 sccm.

c. Etch floating element (q)

i. DRIE for 66 cycles using recipe MELOY_FE

ii. Inspect and proceed in increments of 5 cycles if additional etching is needed.

d. Floating element release
i. Etch oxide. (r)
   1. Etch in 6.1 Buffered Oxide Etch (BOE) for 180 minutes.

ii. Strip Photoresist. (s)
   1. Place in PG Photoresist Remover at 75 C for 15 minutes.
   2. Triple Rinse in DI water.
   3. Gently blow dry with nitrogen gun and place in oven at 120 C for 20 minutes to remove additional water from released structures.
   4. Ash wafer in Anatech barrel asher for 60 seconds at 300W and 300 sccm.

6) Die separated using ADT dicing saw.
APPENDIX H
BOUNDARY LAYER PROFILES AND NEAR WALL DATA FROM NASA LARC

In this appendix, all of the turbulent boundary layer data acquired as part of the experiments conducted at NASA LaRC is shown. Section H.1 shows the traversing Hotwire Results, H.2 the Monte Carlo error results for the traversing Hotwire study, and H.3 the near wall hotwire results. The relevant tunnel conditions for each freestream velocity are given in Table H-1.

There are several sources of error associated with the nature of a temperature based measurement [99] in this estimate that could account for the difference in magnitude. First, the exact height of the hotwire is unknown. While the traverse was set to a specific height, slip in the traverse drive is a cause of uncertainty. Additionally, the plate itself is made of metal. As the wire approaches the plate, heat transfer to the cold metal wall would induce a perceived velocity change [100].

### Table H-1. Results of hot-wire profiles at NASA LaRC.

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<th>$\delta$ [cm]</th>
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<th>$u^*$ [m/s] (Spalding)</th>
<th>$C_f$ (Musker) [$^{*1e-3}$]</th>
<th>$C_f$ (Spalding) [$^{*1e-3}$]</th>
<th>$\Pi$</th>
<th>$Re_\delta$ [$^{*1e4}$]</th>
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**H.1 Traversing Hotwire Profiles**

To obtain these profiles, a Dantek Type 150 hot-wire is fouled to the metal plate at LaRC. The hot-wire is then moved to a height of 20 $\mu$m using a traverse and attached to an anemometer system. The hot-wire probe is then traversed through the boundary layer to a final height of 98 mm. Using the boundary layer profile to estimate the $y$
intercept using the no-slip condition the real height from the wall is estimated to vary from 13 \( \mu \text{m} \) to 102 \( \mu \text{m} \), or from \( y^+ \) of 5 to 110.

Figure H-1. The hotwire profile and relevant fits for a freestream velocity of 16 m/s.

Figure H-2. The hotwire profile and relevant fits for a freestream velocity of 22 m/s.
Figure H-3. The hotwire profile and relevant fits for a freestream velocity of 28 m/s.

Figure H-4. The hotwire profile and relevant fits for a freestream velocity of 33 m/s.
Figure H-5. The hotwire profile and relevant fits for a freestream velocity of 38 m/s.

Figure H-6. The hotwire profile and relevant fits for a freestream velocity of 43 m/s.
H.2 Monte Carlo Results for the Traversing Hotwire Study

In order to determine the spread in shear stress values given a specific freestream velocity a direct Monte Carlo simulation is used. In this process the velocities within an acquired profile are perturbed within the 95% confidence intervals independently. The resulting profile is then fit using Musker’s equation and Spalding’s law for a turbulent boundary layer. The spread of the resulting shear stress values are plotted against each other for each freestream velocity.

Figure H-7. The results of the Monte Carlo analysis for a freestream velocity of 16m/s.
Figure H-8. The results of the Monte Carlo analysis for a freestream velocity of 22 m/s.

Figure H-9. The results of the Monte Carlo analysis for a freestream velocity of 28 m/s.
Figure H-10. The results of the Monte Carlo analysis for a freestream velocity of 33 m/s.

Figure H-11. The results of the Monte Carlo analysis for a freestream velocity of 38 m/s.
Figure H-12. The results of the Monte Carlo analysis for a freestream velocity of 43 m/s.

**H.3 Near Wall Hotwire Spectra**

As was done in the case of the profiles, a Dantek Type 150 hot-wire is fouled to the metal plate at LaRC. The hot-wire is then moved to a height of 20 \( \mu \text{m} \) using a traverse and attached to an anemometer system. Near wall data is acquired. Following that acquisition, the hot-wire probe is then traversed through the boundary layer to a final height of 98 mm. Using the boundary layer profile to estimate the \( y \) intercept using the no-slip condition the real height from the wall is estimated to vary from 13 \( \mu \text{m} \) to 102 \( \mu \text{m} \), or from \( y^* \) of 5 to 110.
Figure H-13. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 16 m/s.

Figure H-14. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 22 m/s.
Figure H-15. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 28 m/s.

Figure H-16. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 33 m/s.
Figure H-17. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 38 m/s.

Figure H-18. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 43 m/s.
H.4 Near Wall Hotwire Spectra with an Upstream Cylinder

After installation of the upstream cylinder, a Dantek Type 150 hot-wire is fouled to the metal plate at LaRC. The hot-wire is then moved to a height of 20 μm using a traverse and attached to an anemometer system. Near wall data is acquired. No profile is acquired while the cylinder is installed and the spread in actual y values is assumed to be similar to the cases without the cylinder.

Figure H-19. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 16m/s when the cylinder is installed.
Figure H-20. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 22 m/s when the cylinder is installed.

Figure H-21. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 28 m/s when the cylinder is installed.
Figure H-22. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 33 m/s when the cylinder is installed.

Figure H-23. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 38 m/s when the cylinder is installed.
Figure H-24. The spectral estimates of the shear stress sensor and near wall hotwire for a freestream velocity of 43 m/s when the cylinder is installed.
LIST OF REFERENCES


BIOGRAPHICAL SKETCH

Jessica Caitlin Meloy was born in 1983 in Brandon, Florida, a suburb of Tampa. She graduated from Tampa Preparatory School in 2002 and then began her time at the University of Florida (UF) in Gainesville, Florida. Jessica received her bachelor of science in electrical engineering at UF in May 2007. After joining IMG in January 2008 she received her master of science in electrical engineering in May 2009. In June 2009 she received a Graduate Student Researchers Program Fellowship from NASA Langley Research Center. She completed her doctoral degree in 2012 and relocated to Seattle, Washington to begin a career at The Boeing Company.