CARBON NANOTUBE ENABLED VERTICAL FIELD EFFECT TRANSISTORS AND THEIR DEVICE DERIVATIVES

By

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To my Grandma
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<td>Alq3</td>
<td>Tris(8-hydroxyquinolinato)aluminium</td>
</tr>
<tr>
<td>ATO</td>
<td>Aluminum-titanium oxide</td>
</tr>
<tr>
<td>BCB</td>
<td>Benzo[cyclobutene</td>
</tr>
<tr>
<td>CNT</td>
<td>Carbon nanotube</td>
</tr>
<tr>
<td>CN-VFET</td>
<td>Carbon nanotube enabled vertical field effect transistor</td>
</tr>
<tr>
<td>CN-VOLET</td>
<td>Carbon nanotube enabled vertical organic light emitting transistor</td>
</tr>
<tr>
<td>DOS</td>
<td>Density of electronic states</td>
</tr>
<tr>
<td>HOMO</td>
<td>Highest occupied molecular orbital</td>
</tr>
<tr>
<td>I_D</td>
<td>Drain current</td>
</tr>
<tr>
<td>ITO</td>
<td>Indium-tin oxide</td>
</tr>
<tr>
<td>Lower BSC</td>
<td>Lower back sweep current</td>
</tr>
<tr>
<td>LUMO</td>
<td>Lowest unoccupied molecular orbital</td>
</tr>
<tr>
<td>MCE</td>
<td>Mixed cellulose esters</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-oxide-semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal–oxide–semiconductor field effect transistor</td>
</tr>
<tr>
<td>NPD</td>
<td>N,N'-di(1-naphthyl)-N,N'-diphenyl-1,1'-diphenyl-1,4'-diamine</td>
</tr>
<tr>
<td>ODCB</td>
<td>ortho-dichlorobenzene</td>
</tr>
<tr>
<td>OFET</td>
<td>Organic field effect transistor</td>
</tr>
<tr>
<td>OLED</td>
<td>Organic light emitting diode</td>
</tr>
<tr>
<td>OTFT</td>
<td>Organic thin film transistor</td>
</tr>
<tr>
<td>P(NDI2OD-T2)</td>
<td>poly][N,N0- bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6- diyl]-alt-5,50-(2,20-bithiophene})</td>
</tr>
<tr>
<td>P3HT</td>
<td>Poly(3-hexylthiophene)</td>
</tr>
<tr>
<td>PCBAM</td>
<td>n-type fullerene derivative [6,6]-phenyl-C61-butyric acid methyl ester</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
</tr>
<tr>
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<tr>
<td>PECVD</td>
<td>Plasma-enhanced chemical vapor deposition</td>
</tr>
<tr>
<td>PF-9HK</td>
<td>poly[(9,9-dioctyl-fluorenyl-2,7-diyl)-alt-co-(9-hexyl-3,6-carbazole)]</td>
</tr>
<tr>
<td>PLV</td>
<td>Pulsed laser vaporization</td>
</tr>
<tr>
<td>SAM</td>
<td>Self assembled monolayer</td>
</tr>
<tr>
<td>SWCNT</td>
<td>Single wall carbon nanotube</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission electron microscopy</td>
</tr>
<tr>
<td>TFB</td>
<td>Poly(9,9-dioctyl-fluorene-co-N-(4-butylphenyl)-diphenylamine)</td>
</tr>
<tr>
<td>$V_D$</td>
<td>Drain voltage</td>
</tr>
<tr>
<td>$V_G$</td>
<td>Gate voltage</td>
</tr>
<tr>
<td>$V_{th}$</td>
<td>Threshold voltage</td>
</tr>
<tr>
<td>VFET</td>
<td>Vertical field effect transistor</td>
</tr>
<tr>
<td>VOLET</td>
<td>Vertical organic light emitting transistor</td>
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A carbon nanotube enabled vertical field effect transistor (CN-VFET) utilizes a dilute carbon nanotube (CNT) random network as the source electrode, and features a stack gate-dielectric-source-channel-drain structure as opposed to the lateral channel between the source and drain structure found in a conventional organic thin film transistor. The structural and electronic properties of the single wall carbon nanotubes help to fully unlock the potential of this new device architecture. The high aspect ratio of the CNTs allows a percolating random network to be made easily with open areas between the CNTs that the electric field can penetrate without much penalty on the conductivity. The low density of states of the CNTs permits the electric field tuning of their Fermi level, while their well passivated surface inhibit covalent bond formation that can cause Fermi level pinning, leaving the barrier height predisposed to gate field modulation.

By adding an electroluminescent layer and modifying the top contact to allow electron injection, a carbon nanotube enabled vertical organic light emitting transistor (CN-VOLET) is demonstrated. The luminance is controlled by the gate field which
modulates the source-drain current by modulating the hole injection barrier at the CNT source electrode. Such gate control should permit new pixel drive schemes and affords the potential for increased device lifetimes.

Returning to the base CN-VFET a non-volatile memory element is realized by adding a charge storage layer on top of the dielectric. The memory element demonstrates a large, fully gate sweep programmable, hysteresis in the cyclic transfer curves exhibiting on/off ratios > 4 orders of magnitude. The carbon nanotube random network source electrode facilitates charge injection into the charge storage layer, realizing the strong memory effect without sacrificing mobility in the vertical channel. Given their intrinsically simple fabrication and compact size CN-VFETs could provide a path to cost-effective, high density organic memory devices.

By utilizing a blend of p-type and n-type organic semiconductors as the channel material an ambipolar CN-VFET is demonstrated. By the virtue of their short channel lengths (without the need for high resolution patterning) the organic blend, ambipolar CN-VFET has important potential advantages that are discussed. Inverters based on ambipolar CN-VFETs are demonstrated. In contrast to inverters made from lateral channel ambipolar transistors, inverters made using the ambipolar CN-VFETs exhibit low leakage currents due to a diode-like transport characteristic in the devices.
CHAPTER 1
INTRODUCTION

1.1 Structure and Electronic States of Single Wall Carbon Nanotubes

A single wall carbon nanotube (SWCNT) is a long slender cylindrical molecule with the wall made of a single layer of carbon atoms. In this single atomic layer each carbon atom forms $sp^2$ bonds with its three nearest neighbors, resulting in a hexagonal lattice structure. One can visualize a single wall carbon nanotube as a long narrow graphene sheet that is rolled up and to let the long edges meet and bond to form a seamless tube. The unit cell of a SWCNT can be specified by two vectors from the unwrapped graphene sheet. Figure 1-1 showed these two vectors: the chiral vector $\mathbf{C}_h$ and the translational vector $\mathbf{T}$ that naturally define a unit cell of the SWCNT.

Figure 1-1. The way to roll a graphene sheet into a SWCNT. Showing in long blue arrows are the chiral vector $\mathbf{C}_h$ and the translational vector $\mathbf{T}$. The chiral vector $\mathbf{C}_h$ can be constructed by the unit vectors of the real space hexagonal lattice $a_1$ and $a_2$. In the case showing $\mathbf{C}_h = (4, 2)$, so that the SWCNT rolled up will be a $(4, 2)$ nanotube. OAA'B defines the unit cell of this nanotube. If $\mathbf{C}_h$...
takes the direction of OP, the resulting SWCNT will be a zigzag nanotube. If $C_h$ goes along OQ direction, an armchair SWCNT will be formed.

When the real space unit vectors $a_1$ and $a_2$ are used to represent the chiral vector $C_h$, the coefficients $n$ and $m$ for $a_1$ and $a_2$ can be used alone to describe $C_h$. So a specific SWCNT can also be described by this pair of integers $(n, m)$.

$$C_h = na_1 + ma_2 \equiv (n, m) \quad (n, m \text{ are integers, } 0 \leq |m| \leq n)$$

Different combination of $n$ and $m$ results in different structure of SWCNT.

SWCNTs can be classified by the edge structure of a cut made along a direction that is perpendicular to the nanotube axis (i.e. along the $C_h$ direction). If this edge shows a zigzag shape, the nanotube is classified a “zigzag nanotube”. If this edge is parallel to bonds between adjacent carbon atoms the CNT is classified an “armchair nanotube”.

The structural type of SWCNT is dictated by their $n$ and $m$ index. When $m = 0$, the chiral vector lies along a zigzag edge of hexagons, yielding a so called zigzag nanotube. On the other hand, when $n = m$, the chiral vector goes parallel to the line between adjacent carbon atoms resulting in an armchair nanotube. For all the other $n$ and $m$ values, the edges don’t have a regular shape and the resulting SWCNTs are called “chiral nanotubes”.

The structural similarities between graphene sheets SWCNTs leads to their closely related electronic states.\(^1\) Tight binding calculation of a single layer graphene sheet gives a semi-metallic band structure, with $\pi$ band and $\pi^*$ bands touching at six K points on the boundaries of the first Brillouin zone. For a nanotube, because of the confinement and periodicity along the circumferential direction, the corresponding reciprocal lattice vectors can take only a discrete set of values, while along the axial direction because the nanotube is very long (compared to its diameter) it is generally
taken to be infinitely long resulting in a continuum of states. Accordingly the first Brillouin zone of a nanotube is made up of a set of parallel line segments that cut the 2-D energy dispersion surfaces of single layer graphene. If a cut line crosses a K point where the \( \pi \) and \( \pi^* \) bands touch, the nanotube has zero band gap making it metallic. If no cutting line goes through a K point, a band gap appears making the nanotube semiconducting.

![Figure 1-2](image)

**Figure 1-2.** The density of states of CNTs. Shown here are the density of states of a metallic (8, 0) and a semiconducting (5, 5) SWCNT. For (8, 0) tubes there are finite states at the intrinsic Fermi level, making it a metallic SWCNT. While for (5, 5) tubes there is no state at the intrinsic Fermi level, rendering it a semiconducting SWCNT.

The Density of electronic states of a metallic and a semiconducting nanotube based on the energy dispersion relations of graphene discussed above are shown in Figure 1-2. The 1-D nature of the nanotubes results in the sharp Van Hove singularities. The intrinsic Fermi level is at \( E = 0 \) with states such that \( E < 0 \) filled and states such that \( E > 0 \) empty. For the metallic nanotube there are states at the Fermi level (\( E = 0 \)), but
for the semiconducting nanotube there is a bandgap such that no states exist in the vicinity of the intrinsic Fermi level \( (E = 0) \).

1.2 Synthesis, Purification and Thin Film Fabrication of Single Wall Carbon Nanotubes: A Brief Review

Various methods have been developed to synthesize SWCNTs, each with its own advantages and drawbacks.\(^2\) Among them pulsed laser vaporization (PLV) is known to generate high quality, low defect density SWCNTs.\(^2,6\) In this method, a target (containing a mixture of graphitic carbon material and metal catalysts) is bombarded by laser pulses, causing a plume of vaporized target material ejected from the target surface. Single wall carbon nanotubes grow in the vapor phase and are the primary reaction product with an optimized yield of \(~70\%\). The diameters of the synthesized SWCNTs are relatively narrowly distributed, in the range of 1.1 to 1.6 nm but peaked at \(~1.4\) nm. These tend to aggregate and bond by van der Waals forces forming bundles during the synthesis, which are hard to separate in subsequent procedures.

For subsequent use in electronic and electro-optic applications the nanotubes must be purified. As the first step of purification, an acid reflux is performed in 2.6 M nitric acid for 45 hrs wherein the less robust (sp\(^3\) bonded) carbonaceous species are consumed by the strong oxidizing acid. After the reflux centrifugation is used to separate the nanotubes from the acid solution. By repeatedly sedimenting the nanotubes decanting off the acid and resuspending the nanotubes in DI water until the pH level reaches about 4.5 the major fraction of the acid is eliminated. The SWCNT material at this stage is suspended in a surfactant solution (normally 1\% Triton X-100 solution). To aid in dispersing the SWCNT shear homogenization can be utilized. The last step of purification is a cross-flow filtration process, where the SWCNT suspension
is circulating through a hollow fiber filter through which particles smaller than the hollow fiber filter pore size permeate out, leaving a cleaner SWCNT suspension. Surfactant buffer solution must be replenished during this process to compensate for the loss of the permeated solution or the nanotubes are concentrated and clog the hollow pore fiber. The purification step is finished when the permeation is clear. The SWCNT suspension is collected for future use.  

![Figure 1-3](image)

Figure 1-3. AFM image of CNT films. (a) AFM image of a 25 nanometer thick nanotube film, and (b) a “2 nanometer thick” nanotube network (scales are in microns). The thickness for “2 nanometers” just means that the amount of material used is one twenty fifth of a 50 nanometer thick nanotube film.

A vacuum filtration method is used to fabricate SWCNT thin films. In this process a controlled amount of diluted SWCNT suspension is filtered through a Mixed Cellulose Esters (MCE) membrane of 100 nm pore size. SWCNTs are trapped by the membrane, forming a uniform thin film on its surface. The desired film thickness is controlled by the concentration of nanotubes in the suspension and the volume of the suspension filtered. After washing away residual surfactant with water, the MCE membrane with the SWCNT film on it is dried and stored for future use. To transfer the SWCNT films onto desired substrate, the SWNT film with the MCE membrane backing is cut to the desired shape, and pressed against the substrate with the SWCNT film side in contact with the
substrate. The MCE membrane is subsequently dissolved away in an acetone bath, leaving just the SWCNT films transferred on the substrate. The great utility of this method has been demonstrated by its ability to transfer SWCNT films on a variety of different substrates, including glass, silicon dioxide, sapphire and flexible transparent plastic sheets like Mylar. Figure 1-3 shows typical atomic force microscopic images of transferred SWCNT films with different thicknesses.
2.1 Schottky Barrier Formation and Schottky Barrier Height

When a metal contacts a semiconducting material, the requirements of thermal equilibrium can induce a charge transfer between the two that finds representation in the alignment of their Fermi levels. Within the Schottky-Mott model the Fermi level of the semiconducting material is shifted by an amount equal to the difference between the bulk work function of the metal and the semiconductor. This Fermi-level shift occurs almost entirely in the semiconductor because for typical metals the comparatively large density of electronic states forms such a large reservoir that the Fermi level shift in the metal is negligible. Denote the work function of the metal by \( q\phi_m \), and the electron affinity measured from the bottom of the semiconductor conduction band by \( q\chi \). For an n type semiconductor, under an ideal case where there is no surface state at the interface between the metal and the semiconductor, the contact potential between them is \( q\phi_m - q(\chi + V_n) \), where \( qV_n \) is the energy difference between the bottom of the conduction band and the Fermi level of the semiconductor. Because of this potential, an amount of positive charge will be built up near the contact region inside of the semiconductor, and an equal amount of negative charge will be built up at the metal surface. The charge redistribution on thermal equilibration aligns the Fermi levels resulting in a potential barrier for electron injection from the metal to the semiconductor having barrier height:

\[
q\phi_{bn} = q(\phi_m - \chi)
\]  

(2.1)
This barrier is called a Schottky barrier. Similarly, the Schottky barrier height for injecting holes from a metal to a p type semiconductor is:

$$q\phi_{bn} = E_g - q(\phi_m - \chi)$$  \hspace{1cm} (2.2)

where $E_g$ is the band gap of the semiconductor.

The forgoing assumed no surface states. The opposite extreme first discussed by Bardeen\textsuperscript{9} considers a reservoir of surface states that is so large that the thermalization between the metal and the semiconductor occurs with electrons in those states. In that case the barrier height is determined by the maximum in the density of the electronic surface states making the barrier height insensitive to the metal work function. In such cases the metal Fermi level is effectively pinned at the maximum in electronic density of surface states (frequently around the mid-gap of the semiconductor). This behavior is called Fermi level pinning.

The sources of surface states are several-fold. Firstly, for bulk inorganic semiconductors the termination of the bulk crystal lattice at the surface alone modifies the local (surface) band structure. Secondly there is generally some degree of atomic reconstruction at a surface to minimize the energy. There can be chemical interactions between atmospheric constituents and surface atoms (taking up the terminal dangling bonds). Finally, when the metal is put into contact with the semiconductor, surface chemical interactions can occur between them. Small molecule organic and polymeric semiconductors do not have a well defined crystal lattice to be subject to the first of these processes however they are subject to interface dipoles due to chemical interactions with the metals that lead to similar Fermi-level pinning like effects. Most metal-semiconductor junctions fall between the Schottky-Mott and Bardeen models with
some semiconductors evidencing contact barriers having appreciable sensitivity to the work function of the metals and others being virtually insensitive to the work function of the contacting metal.

There are good reasons to believe that the carbon nanotubes used as contact “metals” to organic and polymeric semiconductors will not be subject to such Fermi-level pinning like phenomena. The carbon atoms making up the nanotube sidewalls are well satisfied (chemically), making chemical interactions with the nanotubes unlikely. Moreover experiment has provided evidence for a lack of Fermi level pinning at the carbon nanotube-metal contact.\(^{10}\)

### 2.2 Charge Injection Cross A Schottky Barrier

The injection of charges from a metal electrode through a Schottky barrier into a semiconductor can be a complex process. For injection into inorganic materials,\(^8\) which have very high mobility, it is believed that thermionic emission constitutes the main part of the injection current. Other components of the injection current include the diffusion current and tunneling current. Organic semiconductors present greater challenges. Because of the relatively disordered structure of organic semiconducting materials, their electronic states are tend to be localized with hopping being the dominant charge transport mechanism. Accordingly it has been argued that thermionic emission theory, which treats the transport in the semiconductor as ballistic, is not appropriate to describe the carrier injection.\(^{11,12}\)

Instead, models have been developed that try to take into account the energetic disorder of organic semiconductors to evaluate the charge injection. Arkhipov et al. considered the injection to be a two step process.\(^{13-16}\) In the first step a charge tunnels from the metal into one of the localized states of the organic material. In the second
step the charge escapes from that state and enters the bulk. The total rate of injection is the product of the tunneling rate and the escaping rate. Because the process is intrinsically complicated and is related to many factors such as the type of bonding between the metal and the organic semiconductor and the level of interfacial disorder of the organic material, which are poorly controlled and understood, it is still hard to give it an accurate quantitative description. In lieu of a good comprehensive theory the concept of a Schottky barrier (borrowed from inorganic semiconductor junctions) is often used to describe the junctions with organic semiconductors. This is the approach taken in this thesis.

2.3 Experimental Evidence of Shifting the Fermi Level of Single Wall Carbon Nanotubes by Electric Field Effect Gating

A feature of the nanotubes important to the work discussed here is their low density of electronic states (DOS) compared to conventional contact metals. This low DOS implies that the nanotube Fermi level can readily be shifted upon changing their electronic occupancy either chemically, by charge transfer doping, or electronically, by field effect gating. Strong evidence for appreciable Fermi level shifting by field gating was demonstrated by Wu et al. via optical transmittance measurements. For bulk nanotube materials having a diameter distribution peaked near 1.35 nm the optical transmittance spectrum in the visible and near IR shows three principle absorption bands. These absorption bands are understood as being due to symmetry allowed electronic transitions between symmetric van Hove singularity peaks in the DOS of the nanotubes. Figure 2-1 shows the lowest allowed transitions for the semiconducting (12, 8) nanotube (solid Van Hove singularities) and the metallic (10, 10) nanotube (dashed Van Hove singularities) labeled S1, S2 and M1. The filled states are indicated in blue,
with the Fermi level being the line separating the blue (filled) region and white (unfilled) region underlying the curves. The S1 transition is indicated as a dotted line because this transition occurs if the ground state singularity is filled, but vanishes if the Fermi level shifts below the singularity (as shown) depleting the ground state for the transition.

Figure 2-2 shows transmittance spectra from the work of Wu et al. of a nanotube film under distinct electrolytic gate voltages that modulate the electronic population on the nanotubes. The ability to go from a complete S1 absorption to a fully depleted M1 absorption means that the Fermi level was shifted in these studies by at least 0.7 eV.

Figure 2-1. The DOS for the semiconducting (12, 8) nanotube and the metallic (10, 10) nanotube. S1, S2 and M1 are allowed transitions between the corresponding Van Hove singularities. The filled levels are painted blue. The position of the Fermi level can be deduced from either a certain transition will occur.

Figure 2-2. Transmittance spectra shows the modulation of the absorption from transition between Van Hove singularities due to electrolytic gate voltage control over the electronic population on the nanotubes.
2.4 Organic Field Effect Transistors

Filed effect transistors based on organic materials have been the focus of research since they were first demonstrated more than two decades ago.\textsuperscript{17,18} The most common form of organic field effect transistors (OFET) is the so called organic thin film transistors (OTFTs).\textsuperscript{19} This thesis is concerned with a new architecture organic field effect transistor that we have designated the carbon nanotube enable vertical field effect transistor (CN-VFET). The structure and working mechanisms of CN-VFETs are very different from those of conventional lateral channel OTFTs.\textsuperscript{20} To offset the differences and advantages of the CN-VFET a brief review of the structure and operation of OTFTs is given first.

Figure 2-3 shows the typical structure of an OTFT in cross-section. We discuss only the so called bottom gate, top contact TFT. On top of a substrate, a metal gate electrode is covered with a thin dielectric layer. A thin organic semiconductor is deposited directly onto the gate dielectric. Two metal electrodes, designated the source and drain electrodes, separated by a uniform distance are deposited onto the organic layer. The region between the source and the drain electrodes is called channel with the distance between the inner edges of the electrodes designated the channel length and the length of the electrodes that includes the semiconductor between them designated the channel width. The channel length times channel width equals channel area, which is the active area of the OTFT device. With the source electrode held at ground the potential applied to the drain electrode is $V_d$ and the gate is at a potential $V_g$. 
An OTFT works as a voltage controlled current valve. For constant drain voltage $V_d$, the current flowing through the device (injected from the source electrode, passing through the channel and collected by the drain electrode) is modulated by the applied gate voltage $V_g$. The modulation is realized in the following manner. The OTFT we consider works in accumulation mode, which means there are few intrinsic mobile carriers available in the organic semiconductor that fills the channel area. So at this time no current will flow even though $V_d$ is applied. When the gate voltage is turned on, carriers are induced in the channel semiconductor. These carriers are of the opposite sign of those ones accumulated in the gate, so charges in the channel are attracted to lie in a very thin layer adjacent to the gate dielectric. However, this thin layer of charges is free to move in the XY direction. At the same applied $V_d$, current will flow in this case from the source electrode, through the channel to be collected at the drain. This current is noted as $I_d$. Negligible current should flow through the gate dielectric. If appreciable current flows through the gate in the steady state then there is gate leakage, probably
due to the low quality of the gate dielectric material, or because there is a dielectric breakdown due to high gate voltage.

In normal cases the electric field perpendicular to the dielectric surface (the current flow direction) is much larger than the electric field parallel to the dielectric surface. This is called gradual channel approximation.\textsuperscript{21} For long channel OTFTs this is valid and current voltage characteristics can be described as follows. The charge $Q_m$ induced in the channel per unit area for a given gate voltage $V_g$ is:

$$Q_m = C_i(V_g - V_{th})$$  \hspace{1cm} (2.3)$$

where $C_i$ is the capacitance per unit area of the dielectric, and $V_{th}$ is the threshold voltage. When the drain voltage $V_d$ is applied, the actual potential at point $x$ in the channel is $V(x)$, so the charge density becomes:

$$Q_m(x) = C_i(V_g - V_{th} - V(x))$$  \hspace{1cm} (2.4)$$

The source-drain drift current $I_d$ is:

$$I_d = W\mu Q_m(x)E_x$$  \hspace{1cm} (2.5)$$

where $W$ is the channel width, $\mu$ is the charge mobility and $E_x$ is the electric filed at $x$. Because $E_x = dV(x)/dx$, we get:

$$I_d dx = W\mu C_i(V_g - V_{th} - V(x))dV$$  \hspace{1cm} (2.6)$$

Integrating the equation from $x = 0$ to the channel length $L$, we get the expression for $I_d$:

$$I_d = \frac{W}{L}\mu C_i \left[(V_g - V_{th})V_d - \frac{1}{2}V_d^2\right]$$  \hspace{1cm} (2.7)$$

In the linear regime where $V_d \ll V_g$, we can simplify the expression and get:
As $V_d$ is further increased, once $V_d = V_g - V_{th}$ is reached, the drain current won't increase any further and the transistor enters the saturation regime. Because the difference between $V_g$ and $V_d$ now is below $V_{th}$, in the part of the channel region near the drain electrode there will be no mobile charges induced making this part of the channel region actually depleted. Any charge enters this region will be quickly swept out by the electric field. Further increase of the drain voltage won't make drain current any larger, under the assumption that channel is long and the channel length shortening effect is ignored. This is because the increased voltage will be dropped on the depleted channel region, leaving the voltage across the channel region where there are induced charges constant. This is called channel pinch off. In such case the saturation current is:

$$I_d = \frac{W}{L} \mu C_t (V_g - V_{th}) V_d$$  \hspace{1cm} (2.8)

$$I_{ds} = \frac{W}{2L} \mu C_t (V_g - V_{th})^2$$  \hspace{1cm} (2.9)
CHAPTER 3
CARBON NANOTUBE ENABLED ORGANIC VERTICAL FIELD EFFECT TRANSISTORS AND LIGHT EMITTING TRANSISTORS

3.1 Motivation

The promise of inexpensive, solution based processing techniques, inkjet patterning and construction on flexible plastic substrates has focused much research over the past 20 years on organic semiconductors for transistor applications. There now exists a broad range of small molecule organic and polymeric compounds that have demonstrated transconductance. Unfortunately, the electronic mobilities of these compounds, which were initially about 5-6 orders of magnitude too low to be commercially useful, remain about an order of magnitude too low. Such low mobility can be compensated for by bringing the source and drain electrodes closer together, reducing the semiconductor channel length, but that greatly raises the cost of patterning the devices, removing much of the motivation.

In 2004 Yang’s group demonstrated a new TFT architecture that they suggested could circumvent the mobility limitations of present organic semiconductors. Their devices relied however on an ultra thin (<20 nm) aluminum source electrode that required careful partial oxidation. While the optimized device exhibited ~6 orders of magnitude current modulation, the low work function aluminum source electrode required an n-type active channel restricting the devices to the use of C\textsubscript{60} as the channel material. Recently the more conventional organic semiconductor pentacene was demonstrated however this required the additional complication of a 7 nm vanadium oxide layer atop the partially oxidized aluminum source electrode. Most recently they found that this architecture affords important new opportunities in how organic light emitting diodes (the likely successor to liquid crystal displays) are
electronically driven. This is impressive work however the requisite partly oxidized, ultra thin aluminum source electrode would be difficult to produce commercially, constrains the choices for the organic active layers and would be susceptible to electromigration, limiting device lifetimes. Working independently, using single wall carbon nanotubes as the source electrodes, we have arrived at a similar departure from the conventional TFT architecture and also used them to develop a gate controlled light emitting diode. Here we describe the devices, highlighting the important advantages presented by carbon nanotubes, and communicate some, previously un-remarked, relevant features in the physics of the nanotubes.

### 3.2 Structures: CN-VFET vs OTFT

Figure 3-1a and 3-1b compare, in schematic form, a conventional TFT and the new architecture. In contrast to the conventional TFT in which the source, active layer and drain are co-planar with respect to the dielectric and gate, the new architecture stacks the source, active layer and drain vertically relative to the gate, hence the designation as a vertical field effect transistor (VFET). For the VFET architecture a continuous metal source electrode would completely screen the gate field from the active layer, hence a necessary requirement for its operation is that the source electrode be in some sense perforated, making it porous to the gate field. The source electrode shown as a regular grid in Figure 3-1b is meant to convey this idea but should not be taken literally. Yang’s group achieved their gate-field-porous source electrode by the partial oxidation of the very thin aluminum film. Our gate-field-porous source electrode is a dilute, network of single wall carbon nanotube possessing a surface density well above the percolation threshold. Note that for the VFET the channel length
$C_L$ is simply the active layer film thickness, which can be made almost arbitrarily thin, without the need for high resolution electrode patterning.

![Diagram of standard TFT and VFET architectures](image)

Figure 3-1. the standard TFT (a) and the VFET (b & c) architectures. An AFM image of our percolating nanotube network source electrode (scale $\sim 1/2 \times 1 \mu m$) is shown in (c). Also shown is the wiring diagram for the device. A short channel length, $C_L$, in the standard TFT requires tight patterning of the source and drain electrodes, an issue circumvented in the VFET. The current in the standard TFT (red arrows and lines indicate paths) scales with the channel width $C_W$, while in the VFET this scales with the overlap area between the source and drain electrodes, CA.

### 3.3 Basic Electronic Characteristics of CN-VFETs

#### 3.3.1 Typical Transfer Curves

Figure 3-2 and 3-3 shows the typical transfer curves of devices using two different organic semiconductors poly[(9,9-dioctyl-fluorenyl-2,7-diyl)-alt-co-(9-hexyl-3,6-carbazole)] (PF-9HK) and N,N'-di(1-naphthyl)-N,N'-diphenyl-1,1'-diphenyl-1,4'-diamine)
(NPD) as the active materials. Transfer curves are measured by sweeping the gate voltage while keeping the source-drain voltage constant. For different organic materials, different source-drain voltages are needed to get a similar magnitude of source-drain current, which (as elaborated below) is due to the differences of the HOMO levels of these materials resulting in different Schottky barrier height with the nanotube source electrode. The on/off ratios of the PF-9HK and NPD devices at the source-drain voltages indicated on the plots are over 2 orders of magnitude at 215 and 199, respectively. Both of the devices showed substantial hysteresis, which may be caused by charge traps in the active layer. The hysteresis is significantly smaller for the NPD device over the PF-9HK device.

![Graph showing transistor characteristics of the hole only VFET built with the organic semiconductor PF-9HK. Plotted is the source-drain current as a function of gate voltage.]

Figure 3-2. Transistor characteristics of the hole only VFET built with the organic semiconductor PF-9HK. Plotted is the source-drain current as a function of gate voltage.
Figure 3-3. Transistor characteristics of the hole only VFET built with the organic semiconductor NPD. Compare with Figure 3-2 it is clear that the PF-9HK device have noticeably larger hysteresis than the NPD device.

3.3.2 Typical Output Curves

Figure 3-4a and 3-4b shows the typical output curves of devices using PF-9HK and NPD as active materials, respectively. Output curves are measured by sweeping source-drain voltage for different applied gate voltages. The NPD device has a much larger on-current compared with PF-9HK device (312 mA/cm² for NPD device versus 33 mA/cm² for PF-9HK device) at 10V source-drain voltage, but the on/off ratio of NPD device is less than that of PF-9HK device (11.4 for NPD device while 28.9 for PF-9HK device).
Figure 3-4. Typical output curves of CN-VFETs. Devices were built with PF-9HK and NPD as the organic channel materials, respectively.
3.4 The Working Mechanisms of CN-VFETs

In a standard TFT the Fermi levels of the source and drain electrodes are selected to be closely aligned with either the highest occupied molecular orbital (HOMO) or the lowest unoccupied molecular orbital (LUMO) of the active layer material, leading to a hole carrier (p-type) or an electron carrier (n-type) device, respectively. For some nominal source-drain voltage the gate field modulates the carrier density in a thin region at the active-layer/dielectric interface thus modulating the current that flows between the source and drain. Our experiments and theoretical modeling show that the principle mechanism by which the VFET operates is different. While modulation of the carrier density throughout the bulk of the active layer is possible in the VFET geometry for very thin active layers, the resulting current modulation would be a steep function of the active layer thickness. This arises because carriers generated nearest the gate electrode tend to screen the gate field from deeper regions of the active layer. For active layer thickness >100 nm such screening would result in only a small response of the source-drain current to the gate field. The large modulation observed for the >100 nm active layers used and only weak dependence of the gate-field lever arm on the active layer thickness (as observed in our experiments) strongly implicates a gate induced modulation of the contact barrier between the nanotubes and the active layer. Since gated nanotube networks have demonstrated transconductance²⁵ it might be thought that this phenomena is relevant here, but achieving appreciable current modulation across nanotube networks requires the nanotube surface density be very near percolation²⁶ such that the threshold percolation pathways bridge across semiconducting nanotubes (i.e. the metallic nanotubes, considered alone, must lie below the percolation threshold). Well above percolation in the metallic tubes (our
range), with typically 1/3 metallic and 2/3 semiconducting nanotubes the turn on of the semiconducting nanotubes can account for a factor of ~2/3 or ~0.67 of the modulation, not the factor of >100 observed. This indicates that the devices function as p-type, Schottky barrier FETs in which the current modulation is due to a gate field induced modulation of the contact barrier at the nanotube/active layer interface.

The operation of CN-VFETs can be qualitatively described as follows (Figure 3-5 provides a schematic to aid the description). To simplify the argument we assume that the Fermi level of the nanotube sits at the symmetric point of π band and π* band (the Dirac point), i.e. we consider metallic nanotubes. The qualitative result will not change if the assumption is not satisfied. At thermal equilibrium, the Fermi level of a nanotube in the network and that of the organic semiconductor will line up, forming a Schottky barrier with a barrier height given by the difference between the organic HOMO level and the nanotube Fermi level. When negative bias is applied to the gate, the Fermi level of the nanotube will be shifted down from its original position at the Dirac point, so that when holes are injected from the Fermi level of the nanotube to the HOMO level of the organic semiconductor, they experience a lowered Schottky barrier, i.e. the shifting of the nanotube Fermi level is equivalent to a lowering of the barrier height.

Simultaneously, the HOMO level of the organic semiconductor bends towards its Fermi level. The band bending thins the barrier width, further enhance the hole injection. This is when the device at its ON state. On the other hand, when positive bias is applied to the gate the Fermi level of the nanotube shifts upwards, increasing the barrier height. At the same time, band bending makes the barrier thicker, both processes hindering hole injection, placing the device in its OFF state. Figure 3-5 shows the CNT Fermi level
position and organic semiconductor band bending during the operation of the CN-VFET schematically. Detailed electrostatic modeling of the injection barrier and the effect of gate field on it performed by UF Prof. Jing Guo and his graduate student Youngki Yoon indeed shows this to be the case.

Figure 3-5. (a) At negative gate bias, the Fermi level of a CNT is moved downward, resulting in a reduced injection barrier height for holes. The HOMO level of the organic semiconductor also bends toward the CNT Fermi level, thinning the hole injection barrier. (b) Under positive gate bias, the Fermi level of a CNT is moved upward, getting a increased hole injection barrier height. The organic semiconductor HOMO level bending thickens the barrier, making the hole injection even harder.
A two-dimensional Poisson equation was solved self-consistently with the equilibrium carrier statistics of the polymer channel and the nanotube contact for a structure as shown in the inset of Figure 3-6.

Figure 3-6. The HOMO vs. the horizontal position $x$ at different gate voltages, $V_G = -1V$, -10V, and -20V taken at the vertical position $y = 1$ nm, where the interface between the gate oxide and the polymer channel is defined as $y = 0$. The equilibrium Fermi level in both the polymer channel and the nanotube contact is $E_F = 0$ (horizontal dotted line). Vertical arrows indicate the barrier height $\phi_{bp}$ at each voltage. The nanotube diameter is 5 nm with its center located at $x = 0$ and $y = 2.5$ nm. The inset shows the simulated structure and the coordinates. Inside the nanotube ($|x| < 2.5$ nm) the electron potential energy (the symmetric point of the $p_z$ orbital bands) is plotted.

To simplify the modeling and capture the essential physics, the following assumptions were made: (i) The nanotube network is sparse so that an individual nanotube is studied for electrostatics in each region. (ii) A 2D cross-section in a vertical
plane perpendicular to a nanotube long axis is simulated. (iii) The nanotube is an individual single-walled metallic tube. A semiconducting nanotube or a small bundle has a different density of states but does not change the qualitative results. Figure 3-5 shows the band bending at the nanotube/active layer interface as a function of the gate field, displaying the barrier modulation.

3.5 Performance of CN-VFETs with Different Device Parameters

In this chapter parameters that are relevant to the performance of the CN-VFETs are tested. Following these tests, insights were gained which lead to further optimization of device.

3.5.1 Effect of Different Metal for Drain Electrode

Devices with different metal top drain electrodes were built to analyze the effect of drain metal work function on the performance of the vertical TFT. Three different metals were used: Al, Au and Pt. Other than the drain electrode material these devices are identical. PF-9HK was used as the organic active material. Table 1 shows the performance of these devices (measured with source-drain voltage at -5 V). Figure 3-7 shows the transfer curves for this group of devices.

Table 3-1. Performance of CN-VFETs with different metal for drain electrode.

<table>
<thead>
<tr>
<th>Device No.</th>
<th>Drain electrode material</th>
<th>Drain metal work function (eV)</th>
<th>On state drain current density (mA/cm²) at Vg=-60V</th>
<th>Off state drain current density (mA/cm²) at Vg=100V</th>
<th>on/off ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>#31</td>
<td>Au</td>
<td>5.1[18]</td>
<td>0.192</td>
<td>0.00165</td>
<td>116</td>
</tr>
<tr>
<td>#32</td>
<td>Al</td>
<td>4.28[18]</td>
<td>0.100</td>
<td>0.00564</td>
<td>18</td>
</tr>
<tr>
<td>#33</td>
<td>Pt</td>
<td>5.65[18]</td>
<td>0.410</td>
<td>0.00075</td>
<td>547</td>
</tr>
</tbody>
</table>
Figure 3-7. The transfer curves of CN-VFETs with different metals as the top drain electrode. Pt, Au and Al were used.

From the data it can be seen that the lower the work function of drain electrode, the better the device performs—not only is the on current larger, but the off current smaller—so the on/off ratio is better. The explanation for the larger on current for lower work function metal is that, a hole extraction barrier forms between the active layer and the drain electrode, due to the Fermi level equilibration of these two and the band bending of the organic active material. Figure 3-8 shows the hole extraction barriers for metals with different Fermi level contacting the same semiconductor. For metals with work function shallower than the HOMO level of the active material, the lower the work function of the drain metal is, the smaller the hole extraction barrier will be, and the higher the source-drain current will be. PF-9HK has a HOMO level of 5.6 eV, so device
with Pt drain electrode has best performance, and device with Al drain electrode has worst performance.

**Mechanism for hole extraction barrier**

- Large work function metal (e.g. Pt)
- Small work function metal (e.g. Al)

Figure 3-8. Hole extraction barrier mechanism. Depending on the drain electrode material, a hole extraction barrier may exist which can limit the source-drain current for given drain voltage.

It is not clear why lower work function metal (Pt) drain electrode gave lower off current, while higher work function metal (Al) drain electrode gave higher off current. One possible explanation is that although it is not easy, very little amount of electrons can be injected from the drain electrode to the LUMO of the organic semiconductor to form electron current, which is not controlled by gate voltage. So the lower the drain metal work function is, the harder it is to inject electrons, resulting in the lower off current.

Although Pt gave the best drain electrode results, the comparatively high temperature needed to get deposition vapor pressure from Pt makes it difficult to
evaporate. On the other hand, Au worked reasonably well and is easy to grow so Au was became the standard top drain material. Later efforts showed that a thin doping layer (doping the organic material) between the organic and the Au drain electrode was effective in reducing the drain contact barrier and improved the device performance.

### 3.5.2 Effect of Carbon Nanotube Network Density

Devices were made using nanotube networks of different density to analyze the effect on the device performance. Nanotube networks of equivalent thickness of 2 nm, 5 nm and 10 nm were used for the devices. Note that the thickness here is just an equivalent value. For example, the 2 nm “thick” network just means that the amount of material used to make this network is 1/25 of the amount used to make a 50 nm nanometer thick film (the latter of which could be measured by AFM to yield the average height of the film surface above the substrate at a stepedge). Other than the source electrode these devices are identical. PF-9HK was used as the organic active material and Au was used for the drain electrode. Figure 3-9 shows AFM images of the 5 nm and 10 nm thick networks (scales are in microns).

![Figure 3-9](image)

Figure 3-9. CNT random networks of different densities. Showing here is 5 micron by 5 micron scan of AFM images of “5 nm” and “10 nm” thick CNT random networks.
As shown in the Figure 3-10, 2 nm network gave the best performance. The 5 nm network gave similar on current, but the off current was not as low as that of the 2 nm network. The 10 nm network gave the poorest performance with the lowest on current and highest off current.

Figure 3-10. The impact of CNT random network density on the CN-VFETs. Shown here are the transfer curves of CN-VFETs built on different densities of CNT random networks.

It may seem counterintuitive that the thinner network, which has higher sheet resistance, would give a larger on-state current than the thicker network which is more conductive. However, based on considerations of electrostatic screen this becomes reasonable. The 2 nm network has a better balance of conductivity and open area, which allows the penetration of the gate electric field to act on greater portions of
interface between organic channel material and the carbon nanotubes, giving the high on-state current and the low off-state current. The 5 nm network is more conductive, so the on-state current is comparable with 2 nm one, but due to screening, the off current cannot go as low as the 2 nm network device. Screening dominates for the 10 nm device, giving the worst performance.

3.5.3 Effect of Dielectric Surface Treatment

Dielectric surface treatments are known to play a critical role in organic TFT performance.\(^{27}\) The channel conductance in the ON state of organic TFTs relies on the thin layer of charges accumulated by the gate field at the organic-dielectric interface. The mobility of the organic semiconductor is heavily influenced by its ordering and other conditions (e.g. traps) at that interface. Generally a hydrophobizing self assembled monolayer (SAM) applied to the dielectric layer before deposition of the organic has been found to create a trap-free interface for better device performance.\(^{28,29}\)

CN-VFETs work differently from lateral channel organic TFTs.\(^{20}\) The principle role of the gate field is no longer the generation of a continuous layer of charge in the now vertical channel. Instead, charge is injected from the CNT source electrode and the principle role of the gate field is to modulate the Schottky barrier between the nanotubes and the channel material. It does this by shifting the Fermi level of the nanotubes, which it can do efficiently because of their intrinsic low density of states. However, this gate field modulation of the injection barrier happens principally in the vicinity of the surface of the dielectric layer on which the CNTs sit, so the surface conditions of the dielectric can also have a large impact on the CN-VFET device operation.

To test such impact three CN-VFET samples with different dielectric surface treatment were prepared. All three samples used a 200 nm thermal grown silicon oxide
as the dielectric. The control sample device was built on the bare silicon oxide without any treatment. One treatment was to hydrophobize the silicon oxide by applying a commercially available water repellent Rain-X (essentially a polysiloxane compound in an alcohol base). The other treatment was to spin-coat on a thin layer of a cross-linking, low dielectric constant polymer Benzocyclobutene (BCB). Poly(9,9-dioctyl-fluorene-co-N-(4-butylphenyl)-diphenylamine) (TFB) was used as the charge transport material. Au was used to form the drain electrode. Figure 3-11 shows the transfer curves of these samples.

Figure 3-11. The effect of dielectric surface treatment on the CN-VFETs performance. Showing are transfer curves of CN-VFETs with different dielectric surface treatment.

From the transfer curves of the control sample built on bare SiO$_2$ one can see the large and off-set hysteresis. When the gate voltage was scanned from its positive
maximum towards negative, the source-drain current turned on almost immediately. It is known that electrochemical trapping of electrons occurs on SiO$_2$ surfaces originating from SiOH silanol groups$^{31,32}$. So this behavior suggested a large quantity of electron traps existing on the dielectric layer. At large positive gate voltage these traps were filled, compensating the electric field from the gate. On return towards the negative direction the charge empties from the nanotubes before the traps begin to empty, resulting in early turn-on of the source-drain current when gate voltage was scanned back to negative direction. On the other hand, the OFF-to-ON curve did not initiate nearly as early as its ON-to-OFF counterpart, indicating a much lower concentration of positive (hole) traps.

The water-repellent Rain-X treated sample showed a reduced hysteresis compared with the control sample. But interesting to see is that the reduction happened almost entirely on the OFF-to-ON scan side, which agreed with the previous analysis. The primary active ingredient polysiloxanes in the Rain-X has functional groups that bond to the hydroxyl groups on the SiO$_2$ surface passivating the dielectric surface, so that the quantity of electron traps on the surface was greatly reduced. This results in the delayed turn-on on in the OFF-to-ON gate scan for Rain-X treated sample, but its ON-to-OFF scan is almost identical to the control device.

The spun coat 12 nm thick BCB layer creates an interface that is reported to be completely free of hydroxyl groups,$^{31}$ but surprisingly the device built on the BCB coated substrate returned the most hysteresis. This large hysteresis has a minor left-shift of the OFF-to-ON scan (relative to the control), but now acquires a very large left-shift of the ON-to-OFF scan compared with the control device. These results indicated that for the
BCB coated device, the quantity of electron traps was slightly reduced (not as much as the reduction in the Rain-X treated device); but there was now a large increase of hole traps. Considering the thickness of the BCB layer (12 nm), it was hard to believe that the electrons could cross the BCB layer to be trapped by the native SiOH silanol groups on the underlying SiO$_2$ surface. The OFF-to-ON scan of the BCB device also presented a different slope from that of the bare SiO$_2$ and Rain-X treated device, indicating a different trapping/de-trapping process. It was reasonable to speculate that in addition to the elimination of the electron traps on the SiO$_2$ surface, the BCB layer also introduced its own charge traps both for electrons and for holes. Indeed support for this view was found in the literature. It has been shown that BCB films can work as electrets$^{33}$ (a material that exhibits a quasi-permanent charge storage ability).

From Figure 3-11 it is also clear that the dielectric surface treatment had an effect on the ON/OFF ratio of the device. The BCB sample had the largest ON/OFF ratio, followed by the Rain-X treated sample, with the device built on bare SiO$_2$ the lowest ON/OFF ratio. The greater ON/OFF ratios were due to the lower OFF state current for BCB and Rain-X devices. The Schottky barrier based operational mechanism of the CN-VFET suggests that there should be a relationship between the OFF current level and the dielectric surface electron trap density in the vicinity of the junction. For a p-type CN-VFET the source-drain current is turned off by applying a positive gate voltage that increases the hole injection barrier between the CNTs and the organic semiconductor. In the presence of electron traps negative charge also fills the traps on the surface of the dielectric in response to the gate electric field. This layer of negative charge can screen the gate field, resulting in a reduced effectiveness of the gate field in modulating
the injection barrier, compromising the ability of gate voltage to turn the source-drain current off. With the greatest dielectric surface electron trap density, the device on bare SiO$_2$ showed the lowest ON/OFF ratio. By passivating the SiO$_2$ surface, the Rain-X treated device showed a lower OFF source-drain current and thus a higher ON/OFF ratio.

The fact that the BCB coated device exhibited the highest ON/OFF ratio seems contradictory to the argument that the BCB coating introduced both positive and negative charge traps, evident from its having the largest hysteresis. This can be explained however by differences in the charge trap depths between the SiO$_2$ and the BCB surfaces. The electron traps on bare SiO$_2$ are shallow, allowing them to be filled and unfilled easily.$^{31}$ Accordingly the response of the device to a change in the gate voltage is to first fill the traps leaving the device on top hard to turned off. The Rain-X treatment partly passivated the dielectric surface reducing the quantity of electron traps, yielding the smaller hysteresis and the larger ON/OFF ratio. However, for the BCB device, the thick BCB layer (12 nm) has effectively eliminated all the influence of the native electron traps on the bare SiO$_2$ layer. The new positive and negative charge traps introduced are completely due to the BCB layer. These are inferred to be deeper traps that require larger energy to be filled/unfilled. When the gate voltage is changed, the CN-VFET device reacts first, being turned ON or turned OFF, depending on the scanning direction of the gate voltage. The deep traps in the BCB can only be filled/unfilled if the gate voltage scans beyond a certain value. So the BCB coated device showed the largest ON/OFF ratio, while still retaining (enhancing even) the large hysteresis. This hysteresis is well controlled so it is possible to take advantage of it to
build a non-volatile memory element. Chapter 4 will give detailed information on non-volatile memory elements based on CN-VFETs with a BCB charge storage layer and provide data that further supports the inferences about charge traps discussed here.\textsuperscript{34}

### 3.6 Further Discussion

A new and important feature demonstrated here stems from the intrinsic low density of states (DOS) for the nanotubes: a direct consequence of quantum confinement in these quasi-1D objects. In contrast to metals, which possess a high DOS, the Fermi level of the low DOS nanotubes can undergo an appreciable shift in response to a gate field. Hence in addition to the thinning of the contact barrier due to the gate induced band bending, the barrier height ($\phi_{bp}$) is also lowered. Literature descriptions of contact barrier modulation at metallic Schottky contacts are often mislabeled as barrier height modulation when what is really meant is barrier width modulation due to band bending. The high DOS of metals simply does not permit the Fermi level shift necessary for a change in the barrier height. The first report of a true barrier height modulation (of which we are aware) is the electrochemically induced barrier height modulation in an air sensitive, polymer/inorganic (poly(pyrrole)/n-indium phosphide) contact barrier first demonstrated by Lonergan in 1997\textsuperscript{35} (although the polymer is not a true metallic system, as are the nanotubes). The nanotubes exhibit this characteristic, as an air stable material permitting its exploitation in ambient atmosphere.

Further distinction between the nanotubes and metallic contacts bears mention. Metals are susceptible to bond formation with active layers that possess a covalent character. Such covalent bonds are implicated in a frequently observed insensitivity of
the barrier height formed to the work function difference between the metal and semiconductor (Fermi level pinning). Pristine nanotubes by virtue of their highly passivated, graphene-like surface do not readily form covalent bonds, leaving the barrier height predisposed to gate modulation. Defects on the sidewalls of real world nanotubes may modify this picture however, a) measures can be taken to minimize or heal defects, and b) whether or not defects in a quasi-1D system can engender Fermi-level pinning is an interesting open question that such devices can begin to address. Other advantages afforded by the nanotubes are that the strength with which carbon atoms are held within the nanotube sidewall lattice is such that nanotubes are impervious to electromigration,⁷ a key lifetime limiting mechanism in most metal contact based electronic and electo-optic devices. Finally, the quasi-1D geometry of a nanotube contact results in a favorable junction electrostatics. The electric field at the surface of the nanotube is significantly enhanced due to its nanometer-scale radius. The barrier thickness is therefore reduced, which further facilitates carrier injection from the nanotube contact into the active channel.

The gate induced band bending and barrier height modulation shown in Figure 3-6 of above are a result of the simulation at a distance of 1 nm from the gate dielectric surface. The degree to which these effects occur also depends on the distance from the gate. Self screening by the nanotubes reduces the gate lever arm in going from the bottom side of a nanotube, nearest the dielectric layer, to its top side. This has the implication that individual nanotubes are preferred over nanotube bundles since the top nanotubes in a bundle are screened from the gate field by underlying nanotubes and participate substantially less in the modulation. Our nanotube networks are formed by a
filtration/transfer method from pulsed laser vaporization synthesized nanotubes. All high yield nanotube synthesis methods produce bundles of varying diameter and while ultrasonication in surfactants provides a measure of bundle disassembly, excess ultrasonication can also damage and shorten nanotubes. AFM imaging and height analysis statistics shows our networks to be comprised of a bundle distribution ranging in diameters from 1 to 9 nm with a peak centered at ~ 5 nm (Section 3.8).

A requirement that constrains the useful active layer materials in such devices is that the HOMO lies within reach of the nanotube Fermi level for rationally applicable gate fields. If the active layer HOMO lies above the nanotube Fermi level the gate field must generate a barrier at the accumulation layer (anti-barrier) for holes, while if the active layer HOMO lies below the nanotube Fermi level the gate must reduce the pre-existing barrier. Bundled nanotubes in the network impose more severe constraints on the active layer materials that will yield useful transconductance. For active layers possessing a normally on (anti-barrier) band line-up, the top nanotubes in a bundle screened from the gate, cannot switch their barriers off. Because those nanotubes permit current flow independent of the gate field, such normally on devices cannot be turned off effectively, greatly reducing the on/off ratio. For active layers possessing a normally off band line-up, the current is switched on by the nanotubes near the bottom of the bundles. Although the top nanotubes in the bundles participate little in the switching, they do not degrade the on/off current ratio. Figure 3-12 illustrates these points schematically. These inferences are supported by the large on-off ratios observed for PF-9HK and NPD (HOMOs ~5.6 eV and ~5.5 eV, respectively, versus our acid purified p-doped SWNT, work function ~ 4.9 eV) in contrast with a poor on/off
ratio observed when regio-regular poly(3-hexylthiophene) (HOMO ~ 5.0 eV\textsuperscript{38,39}) was used for the active layer (Figure 3-13). However, unlike metals, the nanotubes can have their Fermi level tuned by charge transfer doping (or dedoping). With this ability the CN-VFETs can make use of organic semiconductors with a broader range of HOMO level.

Figure 3-12. Schematic of the restriction imposed on useful organic semiconductors due to the CNT bundles. (a1) Organic semiconductors with a HOMO level higher than CNTs’ Fermi level will be a normally ON device. (a2) The normally ON device cannot be turned fully OFF due to the screening of CNT bundles. (b1) Organic semiconductors with a HOMO level lower than CNTs’ Fermi level will be a normally OFF device. (b2) The normally OFF device can be turned on, while still maintain a high ON/OFF ratio.
Figure 3-13. Restriction of the organic semiconductor HOMOs useful for CN-VFETs due to bundled nanotubes. Show is the transfer curve of a CN-VFET fabricated with a regio-regular P3HT active layer possessing a HOMO too close to that of the nanotube work function and thus demonstrating a very low ON/OFF ratio.

3.7 CN-VOLETs

PF-9HK, initially selected for its low lying HOMO, is also an electroluminescent polymer. This led naturally to the idea that simple modification of the top contact to an electron injecting, small work function metal could turn the formerly hole-only device into a gated, organic, light emitting diode (OLED), where electrons injected from the top contact and holes from the nanotubes combine across the polymer bandgap to produce light. Such devices indeed work, allowing control of the emitted light intensity by the
applied gate voltage suggesting the nomenclature: vertical organic light emitting transistor (VOLET). Unfortunately devices using the PF-9HK as the electroluminescent layer exhibited very short lifetimes (too short to measure useful characteristics). The design is however more general than a single material. Figure 3-14 shows gated light emission in a different system: Alq$_3$ as the photoactive layer, NPD as the hole transport layer and PF-9HK as the gated, hole barrier layer. To permit light extraction the gate electrode is ITO on a transparent substrate with a 160 nm, atomic layer deposited, aluminum-titanium oxide (ATO) gate dielectric on which the nanotube network lies. For devices in which the NPD layer directly contacted the nanotubes, for reasons yet to be determined, light was initially emitted but with a quickly decaying luminance (despite long term stable operation of the hole only VFETs using NPD in direct contact with the nanotubes). This lifetime issue was resolved by addition of the PF-9HK as the layer contacting the nanotubes. A schematic of the device is shown in Figure 3-14b. In this hybrid polymer/small molecule device the 200 nm PF-9HK layer was spun onto the nanotubes from toluene, and the NPD (100 nm), Alq$_3$ (50 nm), LiF (1 nm), Al (100 nm) layers were all thermally evaporated. The inset of Figure 3-14a shows the gated light emission from the device at the gate voltages indicated (drain voltage –7 V in all cases). The corresponding current density versus drain voltage plot at these gate voltages is shown in Figure 3-15. Figure 3-16 shows the measured luminance and current density transfer curves. The pixel here is 2x2 mm. At a drain voltage of –30 V (where there is little gate modulation possible because the large source-drain voltage overcomes the major fraction of the barrier) the luminance is 540 Cd·m$^{-2}$, at a current of 17.3 mA·cm$^{-2}$, for a quite reasonable current efficiency of 3.1 Cd·A$^{-1}$ (comparable to typical ITO anode,
NPD/Alq₃ based devices). It is worth noting that the device shown is among the first such devices constructed with substantial room for optimization. Bright spots in the pixel zoom are likely due to particulates that underlie the nanotube network resulting in a local thinning of the source-drain channel length. This is supported by the principal failure mode in the devices of direct electrical shorts between the source-drain electrodes as we thinned the electroactive layers (for the fabrication controls at that time). This issue also limited the performance of the VFETs and highlights the need for ultra high purity nanotube material and cleanliness of the environment in the network fabrication. However it also indicates that there are improvements to be had from thinning the electroactive layers.

Figure 3-14. CN-VOLET device schematic and luminance curves. (a) Luminance versus drain voltage at the indicated gate voltages for the VOLET stack illustrated in (b). The inset to (a) shows photographs of the light emitted by a 2 x 2 mm pixel for -7 V drain voltage at the gate voltages indicated in green, with a zoom on the pixel in the center image.
Figure 3-15. Current density versus drain voltage at the gate voltages indicated beside each curve for the pixel of the VOLET shown in Figure 3-14.

Figure 3-16. (a) Luminance and (b) current density transfer curves for the VOLET at three distinct source-drain voltages. Arrows indicate the gate voltage sweep direction.
3.8 Experimental details

Hole Only VFETs

Nanotube networks were formed on nanoporous mixed cellulose ester membranes.\(^7\) Pieces of the membrane with the associated nanotube networks were cut into the desired shape and size before transfer of the networks to a 200 nm thermal SiO\(_2\) gate dielectric on heavily p-doped, < .005 ohm-cm, prime silicon (Silicon Quest International), which provided the back gate.

Several distinct active layers were used: 1) poly[(9,9-dioctyl-fluorenyl-2,7-diyl)-alt-co-(9-hexyl-3,6-carbazole)] (PF-9HK, American Dye source ADS238BE) deposited by spin coating at a speed of 750 rpm from toluene (2.5%wt solution) onto the nanotube networks, followed by vacuum drying, resulting in a thickness of ~250 nm, 2) N,N’-di(1-naphthyl)-N,N’-diphenyl-1,1’-diphenyl-1,4’-diamine) (NPD, Lumtec Corporation) thermally evaporated at 2 Å/s to a thickness of ~250 nm, or 3) poly(9,9-dioctyl-fluorene-co-N-(4-butylphenyl)-diphenylamine) (TFB, American Dye Source ADS259BE) 4%wt toluene solution spun coat at 1000 rpm speed, followed by 1 hour of hotplate annealing at 130 °C in an argon glovebox, resulting in a thickness of ~350 nm. The well known regio-regular poly(3-hexylthiophene) (P3HT) (Sigma-Aldrich) was also thoroughly explored for the active layer, never giving better than a factor of 1.5 current modulation in the VFET architecture when measured in ambient atmosphere, attributed to its HOMO line-up with the nanotube Fermi level (P3HT devices built and measured in inert atmosphere with a baked CNT dilute network electrode subsequently demonstrated orders of magnitude transconductance. The bake dedoping the nanotubes, modifying their work function to their intrinsic value of ~4.6 eV). Figure 3-17 shows the molecular
structure of these organic semiconductors. The top contact in all cases was 20 nm of thermally evaporated gold.

![Chemical structures of organic semiconductors](image)

**Figure 3-17.** Structures of organic semiconductors used for CN-VFETs.

Physical layout of a typical device is shown in Figure 3-18. Substrates were 15x15 mm square p\(^{++}\)-Si with 200 nm of thermal oxide. The oxide was etched from one corner and Pd sputtered for the gate contact pad (split contact to confirm ohmic behavior). Gold contact pads to provide the source contact (to the SWNT network) were evaporated through a mask that included a nearby slot bisected by a 32 \(\mu\)m diameter wire to define the source-drain terminals of what would become a side-by-side, bottom contact, conventional, planar, FET. The nanotube network was transferred to lie across
the Au source contacts (the two contacts to permit confirmation of ohmic contact between the network and pads). The active layer PF-9HK and TFB (spun coated) or NPD (thermally evaporated) was deposited over the entire substrate atop the nanotube network. Finally, Au was evaporated onto the active layer through a TEM grid shadow mask (inset photograph). The TEM grid shadow mask defined 0.035mm² drain contacts that could be probed individually. Gold coated needle probes were used to make electrical contact to pads and a soft gold wire to make contact to the top drain contact to avoid piercing through the active layer.

![Diagram of SWNT network](image)

**Figure 3-18.** Physical layout of a CN-VFET device.

**VOLETs**

Figure 3-19 shows the device layout for the VOLETs. Substrates were 160 nm of atomic layer deposited aluminum-titanium oxide (ATO) on ITO glass (Planar Systems) onto which the nanotube networks were deposited. PF-9HK was deposited by spin
coating from toluene followed by drying for one hour on a 95 °C hot plate in a nitrogen
glove box, yielding a 200 nm thick film.

Figure 3-19. Physical layout of the CN-VOLET device.

NPD and Alq3 (Lumtec Corporation, Figure 3-20 for structure) were deposited at 2
Å/s to thicknesses of 100 nm and 50 nm, respectively. These were followed by thermal
evaporation of LiF (1 nm) and Al (100 nm). Gate contact was made by scratching
through to the ITO layer and pressing onto the scratch an indium dot.

Figure 3-20. Structure of the photoactive material Alq3.
Nanotube Bundle Diameter Distribution

Atomic force microscopy images of single wall carbon nanotube (SWNT) networks were recorded on a Digital Instruments Multi-Mode AFM in tapping mode at low scan speeds with the tapping force minimized by keeping the amplitude set point at a setting very near the free-space amplitude. Scan sizes were 1x1 μm. SWNT and nanotube bundle measurements were recorded along the long sections between overlapping tubes. The resulting bundle diameter distribution is shown in Figure 3-21, exhibiting a median bundle diameter of 4.3 nm, an average diameter of 5.0 nm a standard deviation of 3.2 nm.

![Figure 3-21. SWNT bundle diameter distribution from AFM height measurements](image)

Device Measurement

VFETs (PF-9HK and NPD devices) and VOLETs transport characteristics were measured with a homebuilt transconductance measurement system with source-drain
and gate leakage currents read by Keithley model 414s and 485 picoammeters and
signals provided and read by a National Instruments PCI-MIO-16XE-10 multifunction
card controlled by a program written in LabVIEW. Drain and gate voltages were
amplified by a low noise amplifier built in the UF Physics Electronics Shop. To ensure
reliability system performance was validated by comprehensive measurement of the
same test devices on the system against an Agilent model 4284A semiconductor
parameter analyzer. VOLET luminance was measured with a Minolta LS-100 luminance
meter. Later VFETs built with TFB transport characteristics were measured with
Keithley model 2612A sourcemeter controlled by a program written in LabVIEW.
CHAPTER 4
NON-VOLATILE ORGANIC MEMORY ELEMENTS BASED ON CARBON NANOTUBE ENABLED VERTICAL FIELD EFFECT TRANSISTORS

4.1 Field Effect Transistor Based Non-Volatile Memory Elements

Organic electronics promises opportunities for next generation inexpensive and flexible devices. A key component in digital electronics is a non-volatile memory element. The great success of inorganic transistors in non-volatile memory applications (flash memory)\(^\text{40}\) has led to demonstration of memory elements based on organic thin film transistors (OTFTs).\(^\text{41-43}\) While our topic is non-volatile memory elements based on organic field effect transistors (and CN-VFETs), it is beneficial to give a brief introduction to the flash memories before discussing their organic counterparts. Each memory cell inside of a flash memory is basically a MOSFET, with the exception that it has two gates instead of one.

Figure 4-1 shows the schematic structure of a flash memory cell. In addition to the top control gate as in other MOS transistors, there is a floating gate that interposes between the control gate and the transistor channel. The floating gate can store charges that screen the gate field from the control gate, so that the threshold voltage of the cell is modulated. Because the floating gate is isolated all around by dielectrics, under normal conditions the charge trapped on the floating gate won’t leak out for years. To read a memory cell, the control gate is set to a read voltage that falls below the write or erase voltages. Depending on the charging state of the floating gate, the transistor is either ON or OFF. So by measuring the drain current level of the transistor the binary state of the cell is read.
Figure 4-1. Schematic showing of a flash memory cell. Charge stored in the floating gate can act to change the threshold voltage of the transistor.

The floating gate is charged up by a process called hot-electron injection. This is done by applying to the control gate an elevated ON voltage that is higher than the normal read voltage, so that a high current flows through the channel. The current is so high that there will be electrons with sufficient energy to jump across the thin dielectric between the channel and the floating gate to be stored in the floating gate, hence the name hot-electron injection. To discharge the floating gate, a large voltage that has the opposite polarity of the ON state is applied to the control gate so that the electrons trapped in the floating gate escape by quantum tunneling. The dielectric layer between the floating gate and the channel is made thin (20 nm is a typical value) to ensure that both hot electron injection and quantum tunneling processes can occur.

For non-volatile memory elements based on organic thin film transistors, instead of using a floating gate structure, generally a layer of an electret, or a ferroelectric material
has been used, in addition to the traditional gate dielectric, or itself as the gate
dielectric, to provide charge storage capability thus realizing the non-volatile
characteristics in OTFT based memories. The solution processable charge storage
layer promises easy manufacture of non-volatile memory arrays at lower cost.

4.2 CN-VFET Based Non-volatile Memory Elements

4.2.1 Motivation

The CN-VFET acts as an excellent platform for a non-volatile memory element.
The vertical architecture affords potential advantages in the relative packing density
compared to conventional lateral channel OTFT memories, and unlike for the latter,
where the intimate coupling of the charge storage and current carrying layer can
degrade the on–state performance of the devices, the vertical architecture decouples
the processes.

Field effect transistors that use semiconducting carbon nanotubes (CNTs) as the
active channel have been extensively investigated. Memory elements based on
carbon nanotube FETs have also been demonstrated. However, the need to
eliminate metallic nanotubes remains a major impediment to progress in these devices.
In our CN-VFET, a random network of single wall carbon nanotubes forms the source
electrode rather than the active channel so that the devices perform well, despite the
metallic nanotubes in the mix.

Benzocyclobutene (BCB) is a cross-linking, low dielectric constant polymer that
finds application in high performance electronics. BCB has also been used as a
polymeric dielectric in OTFTs. It has been shown that BCB films act as electrets with
excellent charge storage capability and relatively high stability. Here we utilize a 12
nm thick BCB film as the charge storage layer on top of the SiO$_2$ gate dielectric to realize the non-volatile switching operations of CN-VFET based memory elements.

4.2.2 Device Structure

The structure of the CN-VFET based memory is shown in Figure 4-2. A degenerately doped p-type Si wafer with a 200 nm thick thermal oxide was used as the substrate. BCB was spun onto the SiO$_2$ and annealed to form a 12 nm thick film. After a cross-linking hard bake the polymer film is impervious to all solvents.

![Diagram of CN-VFET memory element]

Figure 4-2. Schematic of the CN-VFET based memory element. The CNT random network source electrode shown is a 5x5 $\mu$m$^2$ AFM image of the typical density of CNTs used in these devices. Also shown is the wiring diagram for the device. The current, injected from the source electrode, flows vertically through the charge transport layer to be collected by the top drain electrode.

CN-VFETs were constructed on top of the BCB following procedures detailed in chapter 3. Briefly, a random CNT network was used as the source electrode, on top of which an organic active layer was deposited, serving as the charge transporting channel. In this case poly(9,9-dioctyl-fluorene-co-N-(4-butylphenyl)-diphenylamine)
(TFB) was used as the charge transport material. A gold top drain electrode was evaporated onto the active layer through a TEM grid with hexagonally tiled apertures used as a shadow mask to define individual pixels of area 0.035 mm$^2$. Each such pixel comprised an individual memory element, addressed electrically via a soft gold wire probe that made electrical contact with the top gold drain electrode.

**4.2.3 Device Performance**

Figure 4-3 shows the cyclic transfer curve of a CN-VFET based memory element. The very large gate voltages used here are merely to demonstrate how large the hysteresis can be. As shown below far smaller gate voltages can be used to drive the memory. The ON/OFF ratio of the memory element is more than 4 orders of magnitude. At -5 V drain voltage, the ON state current is about 0.8 μA for the 0.035 mm$^2$ pixel size, corresponding to a current density of 2.3 mA/cm$^2$. Because injection into the TFB layer occurs over the entire overlap area between the CNT network source electrode and the gold drain electrode, an areal current density is sensibly defined, just as for OLEDs and organic solar cells. The low driving voltage highlights one of the advantages of the CN-VFET against conventional OTFTs for device applications. Although the CNT random network source electrode of the CN-VFET was processed in a class-100 clean room, sub–micron particulates in our nanotube source material limit how thin the TFB layer can be made before direct shorts between the source and drain render the devices inoperable. A TFB layer of ~350 nm thickness avoided such direct shorts. Note that for a conventional, lateral OTFT a 350 nm channel length would require expensive high resolution patterning. Once source material particulate issues are resolved the active layer can be made thinner still. This should permit higher current densities, which will benefit device operation because low on-state resistance (as indicated by the ability to
drive higher currents) is an important parameter for improving the read speed of a memory element.\textsuperscript{54}

![Cyclic transfer curve of a CN-VFET based memory element for large gate voltage range.](image)

**Figure 4-3.** The cyclic transfer curve of a CN-VFET based memory element for large gate voltage range. Arrows indicate the direction of the current change during the gate voltage sweep. The “anticlockwise” or “lower back sweep current (lower BSC)”\textsuperscript{19} hysteresis indicates the charge storage origin of the hysteresis observed. The amount of hysteresis is about 157 V in the -100 V to 100 V $V_G$ scan range. The right axis shows the drain current of the 0.035 mm² pixel while the left axis shows the current density.

From the cyclic transfer curve a hysteresis of 157 V is shown for the -100 V to 100 V gate voltage scan. Large hysteresis is essential for non-volatile memory applications. Control experiments excluding the BCB layer show a much smaller hysteresis of 64 V shifted to positive gate voltages and understood as being due to electron traps in the SiO$_2$ at the nanotube/SiO$_2$ interface (Figure 3-11 in chapter 3.5.3).
A fundamental requirement of a non-volatile memory element is temporal stability in each of its states. Figure 4-4 shows the stability of the CN-VFET based memory element for both ON and OFF states, respectively. To set the memory element to its ON state, the gate voltage was scanned to 100 V, and then scanned back to 0 V. The OFF state was set by scanning gate voltage to -100 V first and back to 0 V. After 30 minutes the ON state $I_D$ was still more than 3 orders of magnitude higher than the OFF state $I_D$, indicating the relatively good charge storage stability of the BCB layer.

Figure 4-4. Memory retention characteristics of a CN-VFET based memory element. The ON state was set by scanning $V_G$ to 100 V, then back to 0 V. The OFF state was set by scanning $V_G$ to -100 V, then back to 0 V.

However, BCB is not a dedicated charge storage material. Charge relaxation leads to charge loss in the storage layer, which can be seen from the gradual decay of the ON state $I_D$ and corresponding increase in the OFF state $I_D$. A more stable memory can be
expected with the use of a charge storage material that exhibits a greater barrier to charge exchange with the CNTs.

Figure 4-5 shows the hysteresis as a function of cycle number for cyclic gate voltage excursions between ±100V from the first to the 2400th cycle recorded continuously over 23 hr of cycling. The line is a fit to a single exponential decay \( H = Ae^{-x/cycle} + y_0 \) having a correlation coefficient of 0.9897 that saturates at a value of \( y_0 = 119 \) V. Hence, while there is some decay in the hysteresis with cycling this stabilizes at a still large value.

Figure 4-5. Cycle stability of the hysteretic behavior over 2400 cycles. Plotted is the magnitude of the hysteresis for cyclic gate voltage excursions between ±100 V. The line is a least squares fit to a single exponential decay \( H = Ae^{-x/cycle} + y_0 \) having a correlation coefficient \( R = 0.9897 \) that saturates at a value of \( y_0 = 119 \) V.
The write/erase speed of the device was measured by the following protocol. To restore the ON-state the gate voltage was set to +V for 2 seconds. At the end of the 2 seconds the gate voltage was set to 0 V and the ON-state drain current was measured thus verifying the device ON-state. To switch the ON-state to OFF a negative gate voltage pulse -V and duration t was applied to the gate and the drain current was again interrogated at 0 V.

Figure 4-6a shows the ON and OFF state drain currents as a function of the OFF pulse amplitudes and durations. In all cases the restore and write pulse had the same magnitude. The minimum pulse duration of 1 ms is a limitation of our pulse amplifier which cannot slew fast enough to achieve the programmed pulse voltage for shorter durations. The ±50 V ON-state and OFF pulses are insufficient to fully turn the device ON or OFF. At the larger pulse amplitudes the devices are written at the 1 ms limit of our instrumentation with the 75 V pulses beginning to show minor degradation in the write speed at 10 ms. Figure 4-6b shows the corresponding data for the OFF-state to ON where the OFF-state is prepared by spending 2 s at -V before providing the ON pulse.

There is an asymmetry evident in the ON-to-OFF versus the OFF-to-ON state write speed that likely reflects differences in BCB’s charge storage mechanism for positive versus negative charge. The slower OFF-to-ON write speed can be compensated by using a larger voltage pulse for the latter. As shown in the case of the -75 V restore pulse followed by the 125 V write pulse.
Figure 4-6. Write/erase speeds for the non-volatile memory devices. Drain currents measured at 0 V after 2 s at a preparatory restore voltage (stars) and after the indicated equal but opposite polarity voltage pulse of duration $\Delta t$. Drain currents following the restore voltage varied negligibly from each other so only one representative current point is shown for each voltage. a) From the on-state to off for the indicated pulse voltage and duration, b) from the off-state to on for the indicated pulse voltage and duration.
4.3 Discussion

4.3.1 Mechanism of the Hysteresis

Hysteresis in organic field effect transistors is complicated by the several distinct physical processes that can cause shifts in the threshold voltage during transfer scans. Among these, hysteresis generated by charge storage in a layer near the channel has been most exploited in OTFT memory applications. In the CN-VFET based memory elements, the 12 nm thick BCB layer was designed to serve as the charge storage layer. BCB was selected because it is commercially available, easy to process and very stable after cross-linking. As a Si-based polymer containing Si-O bonds and aromatic rings, BCB has been shown to have excellent ambipolar charge storage capability. The direction of the cyclic transfer curves indicates the origin of the hysteresis. For a p-type transistor, an “anticlockwise” or “lower back sweep current (lower BSC)” hysteresis is generated by charge storage in dielectrics near the channel. Indeed, strong lower BSC hysteresis can be seen in the cyclic transfer curves of the CN-VFET based memory elements, indicating that charge storage is the origin of the hysteresis.

To further confirm that the hysteresis is due to charge storage in the BCB layer, we measured cyclic transfer curves over distinct gate voltage ranges (Figure 4-7). An obvious trend there is a shift of the threshold voltages that follow the “turn back point” gate voltage in the scan.

A similar phenomenon has been reported in OTFT memory elements with donor-polymer blend thin films used as the charge storage layer. The shift of threshold voltage there was explained by the charge balance between the channel, the charge storage layer and the gate. For the CN-VFET devices the mechanism can be
understood on the basis of electrostatics as follows. Suppose, without loss of generality, that the gate voltage is at its most negative value. To balance the negative charge accumulated on the gate, both the CNT source electrode and the charge storage layer must contain a compensating amount of positive charge. The positive charge on the CNTs depresses the contact barrier with the TFB allowing for hole injection so that the p–type device is in its ON state. Now scan the gate voltage towards zero, but only to -50 V (red curve in Fig. 4-7a). In response to the decreasing gate voltage the negative charge on the gate and the corresponding positive charge on the combined CNT-BCB layer is reduced, but the charge on the BCB layer is trapped and less easily drained. To maintain electrostatic charge balance, the positive charge on the CNTs is preferentially drained, raising their contact barrier with the TFB, resulting in the rapid turn off of the device. At the first turn back point (–50 V) the trapped charge has largely remained in the storage layer so as the gate voltage becomes more negative again the positive charge in the CNT layer is quickly replenished, rapidly turning the device back on again. If we return to –100 V in each excursion, this behavior occurs for any turn back point so that the apparent threshold voltage at which the device turns on shifts to lie near the voltage where the scan changes direction and turns back. BCB can store negative charge as well as positive charge so this behavior holds for both negative and positive gate voltage turn-back points (Fig. 4-7a). Symmetric behavior is shown for $V_G$ scans that always return to +100 V (Fig. 4-7b). There the apparent threshold voltages at which the device turns off shifts to lie near the turn back point. The hysteresis in the device is thus fully programmable, depending on the gate voltage turn back points and can even be made zero by restricting the scan range (Fig. 4-7c).
Figure 4-7. Non-volatile memory cell cyclic transfer curves for various gate voltage scan ranges that start from -100 V (a) and 100 V (b). All curves show "lower BSC" hysteresis. For different gate voltage scan ranges, the threshold for turning on or turning off follows the "turn back point" of the gate voltage. (c) Cyclic transfer curves for limited gate voltage scan ranges (25 V) centered at 3 different voltages demonstrating, by its virtual elimination, the programmability of the hysteresis.
From those plots we see that the gate voltage scan range for 3 orders of magnitude current modulation is ±12.5 V. This gate voltage range could be reduced further still by use of a thinner gate dielectric than the 200 nm thermal oxide we use here to avoid gate leakage.

### 4.3.2 Advantages Afforded by the CN-VFET Structure

Similarly programmable thresholds were reported by Baeg et al. in a conventional architecture OTFT memory using pentacene as the active transport layer and poly(α-methylstyrene) as the charge storage layer on an SiO$_2$ gate dielectric.$^{56}$ There they showed that a critical gate voltage was needed to program the OTFT threshold, i.e. gate voltage changes below a critical value resulted in no hysteresis. This critical voltage they concluded reflects an energy barrier for charge injection into the charge storage.
layer. For our BCB on 200 nm thick SiO$_2$ dielectric devices the critical gate voltage was ~25 V. In the Baeg et al. devices the critical gate voltage was greater than 50 V for a 100 nm dielectric layer. This larger critical voltage (50 vs. 25 V) despite the thinner dielectric layer (100 vs. 200 nm, respectively) suggests that the barrier for charge injection in the CNT/BCB devices is substantially lower than that for the pentacene/poly($\alpha$-methylstyrene) devices. This difference could reflect a difference in the Fermi-level offsets between the actors in these distinct material systems, however we suspect a different cause.

In our devices charge transferred to the storage layer is injected and drained by the CNT source electrode. It stands to reason that these processes are enhanced by the quasi-1-D aspect of the CNTs, which enhance the local gate fields for such charge exchange at their narrow line contact with the layer on which they lie. Indeed hysteresis is commonly observed in conventional carbon nanotube based field effect transistors (CNFETs) that use semiconducting single wall carbon nanotubes as the active channel. This is generally ascribed to charge injection into traps on the surface of the (typically) SiO$_2$ gate dielectric layer (likely assisted by the presence of water and oxygen at the CNT/dielectric interface).$^{57-59}$ Our purposely deposited BCB charge storage layer can provide additional evidence for this origin of the hysteresis in conventional CNFETs. For this purpose we constructed an otherwise conventional CNT network FET on the 12 nm BCB layer (atop the 200 nm SiO$_2$ gate dielectric and p++ Si gate electrode) using gold source and drain electrodes to contact opposite ends of the CNT network (Figure 4-8a).
Figure 4-8. (a) Schematic of the CNT random network thin strip transconductance measurement. The thin strip is about 0.9 mm wide and 6 mm long. (b) Hysteresis in the transconductance of the of CNT random network thin strip. The curved arrows indicate the direction of the current change during the gate voltage sweep. 10 V was applied across the strip. About 35% change in the current was induced over the V_G scan between -100 V and 100 V. A mixed

The purpose of this experiment was to explore the effect of the BCB charge storage layer rather than making a high on/off ratio CNFET. We accordingly used a
CNT network density typical for our CN-VFETs, which is well above the percolation threshold for the metallic nanotubes in the mixed metallic/semiconducting nanotube source material. Since only the conductance of the semiconducting nanotubes can be switched by the gate our resulting on/off ratio is expectedly small (only 1.6) in scanning the gate voltage between ±100 V (Figure 4-8b) but note the enormous hysteresis: >100 V. The very large hysteresis in this case of a good trapping layer purposely contacting the nanotubes provides strong support for the role of incidental traps in the hysteresis of conventional CNFETs.

The field enhancement around the quasi-1-D CNTs that makes conventional CNFETs susceptible to hysteresis (generally undesired in transistors) provides advantages for the CN–VFETs over conventional lateral channel OTFTs as memory elements. The latter, to achieve high mobility require a very flat channel/dielectric interface but a flat interface provides no field enhancement to aid in charge injection to the charge storage layer. Indeed, unless a carefully selected charge storage layer is used, lateral channel OTFTs don’t generally exhibit a sufficiently large hysteresis to be useful as memory elements. This dilemma is naturally resolved in the CN-VFET based memory element: The vertical current path and readily controlled short channel length does not require a particularly flat channel/dielectric interface, while the CNT source electrode is an intrinsically good charge injector. Such field enhancement can also serve to explain the apparent smaller barrier to charge injection for the CNT/BCB devices versus that in the Baeg et al. pentacene/poly(α-methylstyrene) devices. While difference in the relative barriers as dictated by the relative Fermi-level offsets in the two
systems perhaps plays a role, more likely is that the field enhancement in the nanotube based devices allows charge injection at lower applied potentials.

Because the CN-VFET relies on the gate field modulation of the Schottky barrier between the nanotubes and the vertical channel material it is particularly sensitive to charge that is trapped in the vicinity of the nanotubes. The gate field enhancement around the quasi-1-D nanotube profile meanwhile enhances the likelihood of charge exchange into charge traps of whatever dielectric layer they contact. This makes the CN-VFET especially prone to hysteresis even without a purposely employed charge storage layer (detailed in chapter 3.5.3). This could severely limit its utility as a transistor. Almost paradoxically, as shown in Figure 4-7c, the addition of the BCB layer, meant to increase the hysteresis, resolves this problem, so long as the gate field sweep range is limited. A fundamental requirement of the charge storage layer to be useful in this regard is that the charge traps in the storage layer be sufficiently deep that the barriers for charge exchange between the nanotubes and the charge storage layer are not overcome for gate voltages swept within the limited range (while still providing an adequate on/off ratio over the limited gate range). The center of the sweep range is programmed by a gate voltage excursion that exceeds the critical voltage needed to load or unload the traps to the desired degree (placing the sweep center point at the desired gate voltage) followed by limiting the gate voltage excursions to less than the critical voltage. These experiments with the charge storage layer have thus also expanded our understanding of the CN-VFET transconductance behaviors and provide clues to their improvement. One improvement that will enhance both the CN-VFET and the memory element described here is raising the capacitance of our gate dielectric
either by thinning and/or switching to a higher dielectric constant material. This will greatly reduce the operating voltage of the devices.

**4.4 Experimental**

A heavily p-doped, < .005 ohm·cm, prime silicon wafer with a 200 nm thermal SiO₂ gate dielectric (Silicon Quest International) was used as the substrate. Dow Adhesion Promoter AP3000 was spun onto the substrate at 2500 RPM prior to the BCB layer deposition. BCB (Dow Cyclotene 3022-35) was diluted in Rinse T1100 solvent (Dow) in a 1:30 ratio and spun on at a speed of 2000 RPM. After spin coating the substrate was baked on a hotplate at 100 °C for 20 minutes to stabilize the BCB layer, followed by a 250 °C hard bake for 1 hour to fully cure the BCB. This yielded a 12 nm thick charge storage layer (film thickness was measured by a Digital Instruments Multi-Mode AFM in tapping mode). These steps were performed in an argon glove-box with < 0.1 ppm oxygen and water. A dilute layer of nanotubes (well above the percolation threshold) was transferred onto the BCB layer by procedures described in reference 8. CNT film transfer occurred outside the glove-box, following which the samples were returned to the glove-box for further processing. The organic active material TFB (ADS259BE, American Dye Source) was dissolved in toluene at 4 weight% stirred overnight and filtered through a 0.2 μm PTFE filter. The TFB solution was spun onto the BCB/CNT electrode at a speed of 1000 RPM, followed by a 130 °C hotplate bake for 1 hour. This resulted in a TFB layer of 350 nm thickness. Using an evaporator integrated into the glove-box (i.e. without ambient air exposure) the 20 nm thick gold top drain contacts were evaporated onto the TFB layer through a TEM grid used as a shadow mask.

The transport characteristics of CN-VFET based memory elements were measured with a homebuilt transconductance measurement system with source-drain
and gate leakage currents read by Keithley model 414s and 485 picoammmeters and signals provided and read by a National Instruments PCI-MIO-16XE-10 multifunction card controlled by programs written in LabVIEW. Drain and gate voltages were amplified by a low noise amplifier built in the UF Physics Electronics Shop. To ensure reliability this system’s performance was validated by comprehensive measurement of test samples on the system against an Agilent model 4284A semiconductor parameter analyzer. Write pulses for the switching speed measurements were generated by an Agilent 33120A Function/Arbitrary Waveform Generator, controlled by a Labview program. Pulses were amplified by a KEPCO Model BOP 1000M bipolar operational power supply/amplifier.
CHAPTER 5
AMBIPOlar CARBON NANOTUBE ENABLED VERTICAL FIELD EFFECT TRANSISTORS AND INVERTERS

5.1 Organic CMOS Technology and Ambipolar Organic Transistors

By the virtue of low static power consumption, high noise immunity and robustness, complementary technology is the mainstream technology for silicon based integrated circuits (ICs). Organic integrated circuits will similarly benefit if complementary technology were to be used. In a complementary circuit both p-channel transistors and n-channel transistors are needed. Historically p-channel organic transistors had much higher performance than their n-channel counterparts but recently air stable, high performance n-channel organic transistors were also realized, and simple complementary circuits incorporating both p-channel and n-channel organic transistors have been demonstrated. However, unlike silicon technology, the integration of n-channel and p-channel organic transistors in ICs of a reasonable integration scale remains challenging.

The ambipolar organic transistor is a promising candidate to solve this problem. Controlled by the gate voltage, either a p-channel or an n-channel can be formed from an ambipolar organic transistor. A complementary circuit can be fabricated simply by using ambipolar organic transistors, which can greatly reduce the patterning complexity. A major challenge in realizing good ambipolar transport in an organic transistor is the effective injection of both electrons and holes from the same metal electrode. A means to overcome this challenge is to either use a small bandgap organic semiconductor or a mixture of two organic semiconductors with appropriately positioned HOMO and LUMO levels so that the injection barriers for both holes and electrons are reasonably small. Good performance has been observed in bi-layer
ambipolar organic transistors consisting of sequential thermally evaporated n-type and p-type material thin film channel layers.\textsuperscript{67,68}

However, solution processability is desired for organic electronic devices to benefit from low-cost manufacturing approaches like ink-jet printing and roll-to-roll fabrication.\textsuperscript{69} Unfortunately, bilayer films from solution processing heavily constrains the materials that can work together because the materials must be soluble in orthogonal solvents to avoid dissolution of the first layer when the second layer is deposited. On the other hand, thin films of organic semiconductor blends deposited from a mixture of a p-type and an n-type organic semiconductor dissolved in a common solvent can be a good alternative.\textsuperscript{70,71} The materials have a tendency to phase segregate while drying so they tend to retain their individual HOMO and LUMO levels.\textsuperscript{71} It has been shown that organic semiconductor blend transistors indeed exhibit gate controlled ambipolar transport, however, even in the best such devices to date both the p-channel and the n-channel exhibit a mobility that is two to three orders of magnitude lower than channels made of either the pure p-type or n-type material. For example, this year (2010) Szendrei et al. demonstrated ambipolar polymer blends transistors with naphthalene-bis(dicarboximide) (NDI) based poly\{[N,N0- bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6- diyl]-alt-5,50-(2,20-bithiophene)} (P(NDI2OD-T2)) as the n-type material and regioregular poly(3-hexylthiophene) (rr-P3HT) as the p-type material.\textsuperscript{72} Their device gave mobilities of 4x10\textsuperscript{-3} cm\textsuperscript{2}/V-s for electrons and 2x10\textsuperscript{-3} cm\textsuperscript{2}/V-s for holes, which are the highest reported so far for polymer blends, however these values are still very low compared with the pure P(NDI2OD-T2) device mobility of 0.45 cm\textsuperscript{2}/V-s and rr-P3HT's 0.1 cm\textsuperscript{2}/V-s. A likely reason for the poor mobility in the organic semiconductor
blend transistors is that many crystalline grain boundaries are induced to nucleate in the mixed phase material leading to high impedance as charge must cross these boundaries. The long channel lengths of conventional lateral channel TFTs of tens to hundreds of microns makes the problem particularly severe with very low on-state currents the result. The CN-VFET architecture by virtue of its short channel length can provide a solution for this problem. In principle the channel length can be made so short that single crystalline grains of each material component phase extend all the way from the nanotube source electrode to the overlying drain electrode such that the bulk mobility of the materials is obtained. This criterion can be satisfied by a film within which a lateral phase segregation of the two components occurs. Indeed, lateral phase segregations were observed in many organic blends systems.\textsuperscript{73-77} This concept is illustrated in Figure 5-1.

![Figure 5-1](image)

**Figure 5-1.** Due to its thin channel layer a phase segregated film can provide single crystal pathways across the channel layer in an ambipolar CN-VFET. In the figure red and blue blocks represent these two phase segregated components.
5.2 Ambipolar Carbon Nanotube Enabled Organic Vertical Field Effect Transistors

5.2.1 Electronic Characteristics of Ambipolar CN-VFETs

When a blend of p-type and n-type organic semiconductors with appropriate HOMO and LUMO levels is used as the channel material in a CN-VFET, ambipolar transport is achieved. Different organic blend systems have been tested. In one experiment, a blend of a p-type fluorene based copolymer poly(9,9-dioctyl-fluorene-co-N-(4-butyphenyl)-diphenylamine) (TFB) and n-type fullerene derivative [6,6]-phenyl-C61-butyric acid methyl ester (PCBM) at a weight ratio of 1:2 was dissolved in ortho-dichlorobenzene (ODCB) and spin-coated to form the channel active layer. Au was used to form the top drain electrode. The transfer curves of the p-channel and n-channel behavior are plotted in Figure 5-2. The output curves for this system are plotted in Figure 5-3.

![TFB:PCBM blends](image)

Figure 5-2. The transfer curves of TFB:PCBM blends ambipolar CN-VFET.
Figure 5-3. The output curves of TFB:PCBM blends ambipolar CN-VFET at extreme gate voltages.

In another experiment, a blend of p-type copolymer TFB and n-type polymer P(NDI2OD-T2) (Polyera ActivInk N2200) at a weight ratio of 1:1 was dissolved in chloroform and spin-coated to form the channel layer. Again Au was used for the drain. Plotted in Figure 5-4 are the transfer curves of the p-channel and n-channel behaviors.

Figure 5-4. The transfer curves of TFB: P(NDI2OD-T2) blends ambipolar CN-VFET.
Figure 5-5 shows the output curves of the TFB:P(NDI2OD-T2) device at the extreme gate voltages.

![Graph showing output curves of TFB:P(NDI2OD-T2) blends.](image)

Figure 5-5. Output Curves of TFB:P(NDI2OD-T2) blends ambipolar CN-VFETs. Only curves for the most positive and most negative gate voltages are shown.

### 5.2.2 Discussion

The output curves for the two devices exhibit a behavior that is indicative of an interesting new feature of the ambipolar CN-VFET. There is evidently a Schottky diode formed at the drain electrode between the gold and each of the p-type and n-type materials. This is shown schematically in Figure 5-6. Figure 5-7 explains schematically how this diode behavior comes about. There is a significant barrier for hole injection into the HOMO of the TFB from the top Au drain electrode, as well as a significant barrier for electron injection into the LUMO of the PCBM or the P(NDI2OD-T2). Unlike the injection barrier between the CNTs and the organic semiconductors, this injection barrier between top Au drain electrode and the two semiconductors is unaffected by the gate
electric field. Neither holes nor electrons can be injected from the drain electrode due to this barrier, but both holes and electrons can pass to the drain electrode from one or the other of the semiconducting materials (depending on the gate and the drain polarity). The result is that high currents flow only for simultaneously positive gate and positive drain or for simultaneously negative gate and negative drain with the current switching direction in the two cases. This behavior gives the ambipolar CN-VFET further important advantages over the ambipolar lateral channel transistor on device applications as discussed in the next section.

Figure 5-6. Equivalent circuit of an ambipolar CN-VFET.
Figure 5-7. Mechanism of diode behavior in the ambipolar CN-VFET. (a) The gate voltage is positive so n-channel is turned on. In this case electrons can only be injected from the CNT source electrode resulting in current flowing from drain to source when drain voltage is positive. (b) The gate voltage is negative so p-channel is turned on. In this case holes can only be injected from the CNT source electrode resulting in current flowing from source to drain when drain voltage is negative.
5.3 Digital Inverters Base on Ambipolar CN-VFETs

The diode-like behavior of the ambipolar CN-VFET has advantage for the device application in logic circuits. An inverter circuit outputs a voltage that is the opposite logic-level of its input. The digital inverter forms the base building block for all digital electronics. Figure 5-8 shows a CMOS inverter. An input at $V_{dd}$ returns ground while an input at ground returns $V_{dd}$.

![CMOS inverter circuit diagram]

Figure 5-8. A CMOS inverter is made up of a p-channel transistor and a n-channel transistor.

5.3.1 Energy Consumption Issue with Lateral Channel Ambipolar Organic Transistors

A digital logic inverter built with two ambipolar lateral channel organic transistors has the recognized problem that it consumes excess energy due to the fact that neither transistor can ever be fully switched off so that there is always leakage current passing through the device.\(^{21,64,66,70}\) The diode-like characteristics of the ambipolar CN-VFET discussed above can minimize this leakage current to achieve a lower energy
dissipation. The problem for the ambipolar lateral channel transistor comes about as follows. For a unipolar lateral channel organic transistor, only one type of charge can be attracted to form the accumulation layer. But for an ambipolar transistor, both holes and electrons can accumulate and form their respective conducting paths as a function of the gate polarity. Accordingly an inverter formed by coupling two lateral channel ambipolar organic transistors will inevitably have leakage issue even at static state due to the fact that neither of the transistor can be fully turned off. Figure 5-9 shows schematically how this comes about.

![Diagram](image)

**Figure 5-9.** Schematic drawing of the operating and leakage mechanism of the ambipolar lateral channel transistor based inverter when the $V_{in}$ (common gate voltage) is (a) grounded and (b) equal to $V_{dd}$. 
As shown in Figure 5-9a, when $V_{in}$ is grounded, because the source electrode of transistor 1 is connected to $V_{dd}$, there will be a lot of holes induced in transistor 1 and the impedance across transistor 1 is small. The source electrode of transistor 2 is grounded, so almost no charge is induced near that region, however, across the channel the potential increases gradually, resulting in more and more induced holes along the channel towards the drain electrode of transistor 2. So transistor 2 is also partially turned on. The impedance of transistor 2 is still much larger than that of transistor 1, leading to a high output voltage that's almost equal to $V_{dd}$. But constant current will flow through the inverter due to the fact that transistor 2 is not completely off. Similarly, as shown in Figure 5-9b, when the input voltage is set to $V_{dd}$, transistor 2 will be fully on but transistor 1 will also be partially on, resulting in a constant current flowing through the inverter.

**5.3.2 Low Leakage Current Inverters Based on Ambipolar CN-VFETs**

![Schematic layout of ambipolar CN-VFET based inverter](image)

**Figure 5-10.** Schematic layout of ambipolar CN-VFET based inverter. In the inverter two identical ambipolar CN-VFETs are connected in a back-to-back fashion with drain electrodes connected as the output electrode.
Digital inverters were built by coupling two identical ambipolar CN-VFETs. Figure 5-10 shows a schematic of the layout. Because of the diode-like behavior in the characteristics of the ambipolar CN-VFET, leakage current in an ambipolar CN-VFETs based inverter can be very small.

The source electrode of CN-VFET 1 is connected to $V_{dd}$, while the source electrode of CN-VFET 2 is grounded. When the gate is grounded, the hole injection barrier between the CNT source electrode and the organic channel is lowered for CN-VFET 1, making CN-VFET 1 a low impedance path for holes to travel from its source to the drain. While for CN-VFET 2, the gate is at the same potential as its grounded source electrode, so the electron injection barrier is still high, making CN-VFET 2 a high impedance path for electrons. Note that for either CN-VFET in the inverter, because of the built-in schottky diode present at the semiconductor-drain contact, neither electrons nor holes can be injected from the drain electrode into the semiconductor layer, leaving the current through the CN-VFETs fully controlled by the source injection. On the other hand, the built-in schottky diodes readily pass holes or electrons from the semiconductor layer into the drain electrode. Back to the inverter device operation, the low impedance of CN-VFET 1 and high impedance of CN-VFET 2 give an output voltage very near $V_{dd}$. The drain-to-channel diodes meanwhile minimize the leakage currents. Similarly, when the input is connected to ground, CN-VFET 1 will be turned off while CN-VFET 2 turned on, leading to an output voltage near zero at the output terminal. And again the leakage current through the inverter is at minimum.

### 5.3.3 Electronic Characteristics of Ambipolar CN-VFETs based Inverters

Figure 5-11 shows the output characteristics of the inverter based on TFB:P(NDI2OD-T2) ambipolar CN-VFETs. Shown in Figure 5-11a are the first quadrant
characteristics where $V_{dd}$ and $V_{in}$ is positive. Shown in Figure 5-11b are the third quadrant characteristics where $V_{dd}$ and $V_{in}$ are negative. The leakage currents for these cases are plotted in Figure 5-11c and Figure 5-11d, respectively. The leakage currents are very low minimizing the static power consumption.

![Figure 5-11](image.png)

Figure 5-11. Showing in (a) and (b) are the transfer characteristics of ambipolar CN-VFET based inverter working at the 1st and 3rd quadrant, respectively. (c) and (d) plot the leakage current through the inverter in the above mentioned situations.

An ideal inverted has infinite gain at the transition between the two states (i.e. $dV_{out}/dV_{in} = \infty$). A real world non-ideal inverter has a finite gain. However, a gain at least larger than 1 is needed for the inverter to be useful and larger gain is preferred to give
the device better noise rejection.\textsuperscript{60} Plotted in Figure 5-12 is the gain of the inverter for operation at increasing $V_{dd}$ in the 1\textsuperscript{st} and 3\textsuperscript{rd} quadrant, respectively. Evidently this inverter can be useful at $V_{dd}$ greater than 5 volts.

![Figure 5-12](image)

Figure 5-12. Gain of the ambipolar CN-VFET based inverter working at (a) the 1\textsuperscript{st} quadrant and (b) the 3\textsuperscript{rd} quadrant, respectively.
5.4 Experimental

Figure 5-13 shows the design layout of the ambipolar CN-VFET sample. A 0.6” by 0.6” glass chip was cleaned as the substrate. The fabrication process progressed as follows.

Figure 5-13. (a) Schematic showing of a 6” by 6” glass substrate with 4 ambipolar CN-VFET based inverters fabricated. (b) detailed illustration of the components in a ambipolar CN-VFET based inverter.
Gate patterning. A cleaned glass substrate was coated with LOR 3B (spin coat at 4000 rpm for 1 min, then hotplate bake for 5 min at 150 °C) resulting in a film thickness of ~350 nm. On top of LOR 3B a layer of photoresist Shipley S1813 was deposited (spin coat at 3000 rpm for 1 min, hotplate bake for 2 min at 112 °C). Sample was exposed for 40 seconds under a power of 7.9 mW/cm² on a Karl Suss MA6 mask aligner using the gate electrode mask, then developed for 40 seconds in AZ 300MIF developer. 50 nm Al was thermally evaporated on the substrate at a rate of 0.2 nm/sec. Lift-off was done using 2 sonication baths in MicroChem Remover PG for 30 min each, followed by an isopropanol bath for 5 min, then a thorough DI water rinse and blown dry.

Dielectric growth. Substrate was ashed under oxygen plasma in an Anatech SCE600 Barrel asher for 10 min using 600 W power and 700 sccm gas flow rate. This resulted in a roughly 4.8 nm thick AlOₓ layer on top of the Al gate electrode. The substrate was then taken to a STS 310PC PECVD system to grow a roughly 62 nm thick silicon nitride (as measured by a Filmetrics F40 spectrophotometer).

Source contact patterning. A layer of 5 nm Cr and 40 nm Au was evaporated on photolithographically defined patterns and lifted off resulted in the Au source contact. Shipley S1813 photoresist and the Karl Suss MA6 were used during the process.

Dielectric surface treatment. Dow Chemical Cyclotene 3022-35 (BCB) was diluted in Dow Rinse T1100 solvent at a ratio of 1:40 and spun coat on the substrate at a spin speed of 4000 rpm following a Dow Adhesion Promoter AP3000 pretreatment, and baked on a hotplate at 100 °C for 20 min followed by a 1 hr 250 °C hardbake inside a Ar glovebox. The resulting BCB film was roughly 8 nm thick (as measured by AFM).
CNT patterning. 2 nm thick CNT random network was transferred to cover the device area of the sample. MicroChem Nano 950 A4 PMMA was spun on at 2500 rpm and baked on a hotplate at 180 °C for 90 sec. The use of PMMA in direct contact with CNT is because of the observation that commonly used photoresist S1813 tends to leave residues on the CNT (unpublished result from Jennifer Sippel). On top of PMMA a layer of S1813 was coated. The sample was exposed in a Karl Suss MA6 mask aligner using the nanotube source electrode mask and developed in AZ 300MIF developer for 1 min. Then the sample was put into an Anatech SCE600 Barrel asher for 22 min at a power of 600 W and gas flow rate of 700 sccm. The oxygen plasma ate away the expose part of CNT network, leaving the patterned CNT network on the substrate. Three acetone baths and one isopropanol bath were used to remove the PMMA and S1813 film and clean up the sample. The substrate with CNT on it can be baked on hotplate inside Ar glovebox to tune the CNT doping level so as to shift the CNT Fermi level. 78

Semiconductor deposition. For TFB:PCBM system TFB and PCBM were mixed at a 1:2 weight ratio and dissolved in ODCB at a concentration of 20 mg TFB and 40 mg PCBM per ml ODCB overnight. TFB was bought from American Dye Source (ADS259BE) and PCBM was bought from SES Research (99%) and both were used as received. The solution was filtered through a 200 nm pore size PTFE syringe filter before use. The solution was spun onto the substrate at a speed of 650 rpm. In order to increase the film thickness, a Sylvania 250W heat lamp was used to heat up the substrate surface while doing the spin coating. For the TFB: P(NDI2OD-T2) system TFB and NDI2OD-T2 were weighed in a 1:1 weight ratio and then dissolved and mixed
overnight in chloroform at a concentration of 10 mg TFB and 10 mg P(NDI2OD-T2) per ml chloroform. P(NDI2OD-T2) was bought from Polyera (ActivInk N2200) and used as received. The solution was filtered through 200 nm pore size PTFE filter before use. The solution was spun onto the substrate at a speed of 1800 rpm. The substrate was baked on a hotplate at 110 °C 30 min in an Ar glovebox after spin coating.

Drain electrode deposition. The Au drain electrode was evaporated through a mask. A fixture registered the mask such that the deposited drain electrode would be in good alignment with the rest of the device on the substrate. Figure 5-14 shows an AutoCAD drawing of the fixture.

Figure 5-14. AutoCAD drawing of the fixture for holding sample and aligning evaporation mask for the drain electrode deposition.
The ambipolar CN-VFET transport characteristics were measured with a Keithley model 2612A sourcemeter controlled by a program written in LabVIEW. The ambipolar CN-VFET based inverter characteristics were driven by a Keithley model 2612A and the output voltages were measured by a Keithley model 2400 sourcemeter controlled by a program written in LabVIEW.
CHAPTER 6
CONCLUSIONS

In this dissertation a novel type of transistor—a carbon nanotube enabled vertical field effect transistor (CN-VFET) has been described. Measurements characterizing the CN-VFET performance characteristics and elucidating its operational mechanism were discussed. The CN-VFET architecture lends itself to the development of several related devices with distinct potential applications. The derivative devices demonstrated were a carbon nanotube enabled vertical organic light emitting transistor (CN-VOLET), a non-volatile memory element and an ambipolar CN-VFET based digital inverter.

The CN-VFET works as a gate field controlled Schottky barrier transistor. Fabricated on top of a substrate consisting of a back gate and a dielectric layer, it features a source-channel-drain vertical stack structure, as opposed to the coplanar structure found in lateral channel TFTs. In the CN-VFET carriers are injected from the carbon nanotube (CNT) source electrode, passing vertically through the thin film channel and collected by the top drain electrode. The gate controls the source-drain current by modulating the injection barrier between the carbon nanotubes in the source random network and the organic semiconductor. Both p-channel and n-channel transistors have been demonstrated in this configuration. In a p-channel CN-VFET, holes are injected from the Fermi level of the CNTs into the HOMO of the organic semiconductor, while in an n-channel CN-VFET, electrons are injected from the Fermi level of the CNTs into the LUMO level of the organic semiconductor. In addition to a gate field induced band bending that thins the barrier between the CNTs and the organic semiconductor the gate field modulates the Fermi level position of the CNTs in the source random network to control the injection barrier height. In order to make sure
that a rationally applicable gate field can turn the source-drain current ON and OFF, the HOMO level of the organic semiconductor for p-channel applications and LUMO level of the organic semiconductor for n-channel applications need to lie reasonably near to the Fermi level of the CNTs (within ~ ±0.5 eV).

By coupling an electroluminescent structure on top of the basic CN-VFET a carbon nanotube enabled vertical organic light emitting transistor (CN-VOLET) was demonstrated. A typical electroluminescent structure includes an electroluminescent layer, an electron transporting layer and an electron-injection electrode. Gate voltage controlled light emission was realized by controlling the hole injection from the CNT source electrode. The initial device demonstrated two orders of magnitude light contrast ratio between the ON and OFF states. The CN-VOLET has the potential advantage of simplifying the drive circuitry of an active matrix light emitting display device.

The dielectric surface treatment was found to have a strong impact on the CN-VFET device performance. By adding a crosslinking polymer layer (BCB) on top of the dielectrics the hysteresis of the CN-VFET could be enhanced due to charge storage inside of the BCB layer. A non-volatile memory was demonstrated by utilizing this controllable hysteresis, where threshold voltage of the memory element can be set precisely over a broad, continuous range of values. The CN-VFETs may turn out to be a better candidate for memory applications than traditional lateral channel OTFTs, thanks to their unique structure that enhances the charge exchange between the source electrode and the charge storage layer without compromising the channel mobility.

Ambipolar transport was achieved by using a channel material consisting of a blend of p-channel and n-channel organic semiconductors. The ambipolar CN-VFETs
showed a novel diode-like behavior on their transfer curves, due to the limited injection from their drain electrode. This unique characteristic means that when used in pairs to form a complimentary p-type/n-type inverter the device exhibits a very low leakage current (in contrast to similar devices based on ambipolar lateral channel transistors). Inverters built with two identical ambipolar CN-VFETs demonstrated typical inversion behavior at different $V_{dd}$ values with a maximum gain of 5 with a leakage current on the order of nanoamps.

In conclusion, the CN-VFET provides a new organic transistor platform that provides the foundation for a number of electronic devices, some of which were explored in this thesis. These devices exhibit interesting and novel characteristics with demonstrated advantages over conventional lateral channel TFTs. Although further optimization is needed to further push the performance of the CN-VFETs and their derivatives, the studies contained herein should provide a good starting point and new opportunities should abound.
LIST OF REFERENCES


BIOGRAPHICAL SKETCH

Bo Liu was born in 1982 in Puyang, Henan, P. R. China. Bo has always been a keen kid who was curious about any new stuff around and eager to figure out the way how stuff works. Bo’s first favorite toy was an electric motor he got out from his father’s tape recorder. And only after several years did Bo realize how great his Dad was—Instead of being grounded for days by turning a then-valued equipment into a pile of parts, Bo got the motor as a gift from his Dad. Bo’s dream was to become a great scientist, just like most of the Chinese kids at that time. But not like the others, Bo’s still pursuing this dream right now.

Bo went to the city of Zhengzhou to attend one of the best high schools in Henan province at the age of 15. He took part in the High School Physics Competition there and found himself fall in love with physics. After 3 years study in Zhengzhou Bo got enrolled into Fudan University in Shanghai. Bo decided to study physics there. Bo’s college life was busy and fantastic. He learned to play violin, taught himself making 3D motion pictures, practiced taekwondo and did a lot of physics. During the fall semester of his junior year Bo got an opportunity to go to the University of Hong Kong as an exchange student. He made a lot of new friends during his half-year-stay in Hong Kong, and experienced himself in working with ultra high vacuum systems. After back to Shanghai Bo joined Dr. Hou Xiaoyuan’s group where he did calculation works on optimizing the optical thin film transmittance.

In the fall of 2005 Bo came to the University of Florida to pursue his PhD degree in physics. He joined Dr. Rinzler’s lab in the spring of 2006. There Bo worked on combining carbon nanotubes and organic semiconductors for the application of novel
electronic devices. Bo liked his research field a lot and decided to continue his research career in nano-technology after graduation.

During a visit back to China Bo met Lei Zhang, a daughter of Bo’s parents’ good friends, and fell in love with her. Bo and Lei were married in March of 2010.