TECHNIQUES FOR CRYSTALLESS OPERATION OF WIRELESS INTER-CHIP DATA COMMUNICATION SYSTEMS

By

KYUJIN OH

A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2010

1
To my family
ACKNOWLEDGMENTS

I would like to begin by thanking my advisor, Professor Kenneth K. O, whose constant encouragement and patient guidance provided a clear path for my research. I would also like to thank Dr. Gijs Bosman, Dr. William Eisenstadt and Dr. Nam Ho Kim for helpful suggestions and serving on the Ph.D. committee.

I would like to thank the former SiMICS members Yanping Ding, Eunyoung Seok, Kwangchun Jung, Chikuang Yu, Haifeng Xu, Jau-Jr Lin, Changhua Cao, Yu Su and Shashank Nallani Kiron. I have been quite fortunate to have worked with my colleagues Swaminathan Sankaran, Hsinta Wu, Dongha Shim, Tie Sun, Ruonan Han, Wuttichai Lerdositomboon, Chuying Mao, Dr. Choongyul cha, Kyungsun Seol and Ning Zhang. The discussions with them and their advice were immensely helpful for completing this work.

Much appreciation goes to TOYOTA Motor Corporation for funding this work. My special thanks go to Eric Schwartz at Agilent Technologies for help in BER measurements and Al Ogden for bonding and dicing chips. I would also like to acknowledge Dr. Hyeopgoo Yeo and Dr. Jonksick Ahn for helpful technical discussions.

I am deeply grateful to my family for their unconditional love, guidance, encouragement, and support which are the source of my strength. I dedicate this work to my family.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACKNOWLEDGMENTS</td>
<td>4</td>
</tr>
<tr>
<td>LIST OF TABLES</td>
<td>7</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>8</td>
</tr>
<tr>
<td>ABSTRACT</td>
<td>14</td>
</tr>
</tbody>
</table>

**CHAPTER**

1 WIRELESS INTERCONNECTS IN ENGINE CONTROLLER BOARDS | 16

1.1 Introduction | 16
1.2 System Overview | 17
1.3 Organization of Dissertation | 22

2 OVERVIEW OF CLOCK AND DATA RECOVERY CIRCUIT | 24

2.1 Introduction | 24
2.2 Non Return to Zero (NRZ) Test Pattern | 25
2.3 Clock and Data Recovery (CDR) Overview
   - 2.3.1 Linear Phase Detector for Random Data | 27
   - 2.3.2 Linear Model of CDR | 31
   - 2.3.3 Choosing a Bandwidth of CDR | 35
2.4 Summary | 37

3 CLOCK AND DATA RECOVERY CIRCUIT AS AN LO GENERATOR | 38

3.1 Introduction | 38
3.2 New CDR Structure
   - 3.2.1 Loop Filter | 40
   - 3.2.2 Voltage Controlled Oscillator (VCO) | 41
   - 3.2.3 Divider Chain (Divide-by-60) | 42
   - 3.2.4 Phase Detector | 43
   - 3.2.5 Charge Pump (CP) | 45
3.3 Simulation Results | 46
3.4 Measurement Results | 49
3.5 The Influence of Phase Noise of CDR on ASK Modulation | 56
3.6 Conclusion | 59

4 FDMA TRANSMITTER AT MOTOR SIDE | 61

4.1 Introduction | 61
4.2 Evolution of Transmitter at Motor Side | 61
<table>
<thead>
<tr>
<th>Table</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Frequency plans for transmitter and receiver at the motor side</td>
<td>19</td>
</tr>
<tr>
<td>1-2</td>
<td>Frequency plan for transmitter and receiver at deadtime controller</td>
<td>20</td>
</tr>
<tr>
<td>1-3</td>
<td>Link margin analysis for FDMA</td>
<td>22</td>
</tr>
<tr>
<td>1-4</td>
<td>Link margin analysis for CDMA</td>
<td>22</td>
</tr>
<tr>
<td>2-1</td>
<td>Summary of jitter specification</td>
<td>36</td>
</tr>
<tr>
<td>3-1</td>
<td>Summary of measured CDR performance</td>
<td>54</td>
</tr>
<tr>
<td>3-2</td>
<td>Comparison of jitter performance</td>
<td>55</td>
</tr>
<tr>
<td>4-1</td>
<td>IF signal generation</td>
<td>65</td>
</tr>
<tr>
<td>4-2</td>
<td>Simulated power consumption in TX at motor node</td>
<td>73</td>
</tr>
<tr>
<td>4-3</td>
<td>Simulated and measured duty cycle of IF signals</td>
<td>77</td>
</tr>
<tr>
<td>4-4</td>
<td>Summary of TX output power level at motor side</td>
<td>79</td>
</tr>
<tr>
<td>4-5</td>
<td>Power consumption of transmitter at motor side</td>
<td>91</td>
</tr>
<tr>
<td>5-1</td>
<td>Summary of measurement results of baseband amplifier</td>
<td>100</td>
</tr>
<tr>
<td>5-2</td>
<td>Summary of RX chain measurement results</td>
<td>106</td>
</tr>
<tr>
<td>5-3</td>
<td>Summary of measured jitter performance</td>
<td>110</td>
</tr>
<tr>
<td>5-4</td>
<td>Summary of measured BER performance of RX chain at motor side</td>
<td>111</td>
</tr>
<tr>
<td>5-5</td>
<td>Summary of measured RMS jitter and BER performance</td>
<td>113</td>
</tr>
<tr>
<td>A-1</td>
<td>Summary of measured CDR performance</td>
<td>132</td>
</tr>
<tr>
<td>B-1</td>
<td>Summary of TX output power level at motor side with an external IF signal source</td>
<td>133</td>
</tr>
</tbody>
</table>
### LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Engine controller board for a HEV. D1 and D2 communicate with M1<del>M6 and M7</del>M12, respectively. (Courtesy of TOYOTA).</td>
<td>18</td>
</tr>
<tr>
<td>1-2</td>
<td>Signaling scheme for the up (FDMA) and down (CDMA) links.</td>
<td>19</td>
</tr>
<tr>
<td>1-3</td>
<td>Frequency bands and data rate in deadtime controller and motors.</td>
<td>19</td>
</tr>
<tr>
<td>1-4</td>
<td>Frequency plans for the transceiver at the motor side.</td>
<td>20</td>
</tr>
<tr>
<td>1-5</td>
<td>Frequency plan for transceiver at deadtime controller side.</td>
<td>20</td>
</tr>
<tr>
<td>2-1</td>
<td>PRBS signal (a) waveform in time domain, (b) autocorrelation, and (c) power spectral density in frequency domain [20].</td>
<td>26</td>
</tr>
<tr>
<td>2-2</td>
<td>Block diagram of CDR.</td>
<td>27</td>
</tr>
<tr>
<td>2-3</td>
<td>A linear phase detector (a) block diagram, and (b) waveform under the locked condition.</td>
<td>28</td>
</tr>
<tr>
<td>2-4</td>
<td>Waveform of phase detector for (a) early clock and (b) late clock.</td>
<td>28</td>
</tr>
<tr>
<td>2-5</td>
<td>Input-output characteristic of linear phase detector.</td>
<td>30</td>
</tr>
<tr>
<td>2-6</td>
<td>Input-output characteristic of tri-state phase and frequency detector (PFD).</td>
<td>30</td>
</tr>
<tr>
<td>2-7</td>
<td>Linear model of PLL based CDR circuit.</td>
<td>31</td>
</tr>
<tr>
<td>2-8</td>
<td>The 2\textsuperscript{nd} order passive lead-lag filter (a) schematic and (b) transfer function.</td>
<td>32</td>
</tr>
<tr>
<td>2-9</td>
<td>Bode plot of the open loop gain for a CDR circuit.</td>
<td>34</td>
</tr>
<tr>
<td>2-10</td>
<td>Linear model of second order CDR and its jitter plot.</td>
<td>36</td>
</tr>
<tr>
<td>3-1</td>
<td>Block diagram of conventional CDR.</td>
<td>39</td>
</tr>
<tr>
<td>3-2</td>
<td>Block diagram of new CDR.</td>
<td>39</td>
</tr>
<tr>
<td>3-3</td>
<td>Schematic of the 24GHz LC VCO.</td>
<td>42</td>
</tr>
<tr>
<td>3-4</td>
<td>Block diagram of divider chain (divide-by-60).</td>
<td>43</td>
</tr>
<tr>
<td>3-5</td>
<td>Block diagram of divide-by-2 and implementation of latch circuit.</td>
<td>43</td>
</tr>
<tr>
<td>3-6</td>
<td>Block diagram of (a) phase detector and (b) implementation of each DFF using DCVSL logic circuits.</td>
<td>44</td>
</tr>
</tbody>
</table>
3-7 Schematic of charge pump. .................................................................45
3-8 Plot of current mismatch between up and down current in the charge pump. 46
3-9 Simulated VCO tuning range plot with 3-bit digital control for coarse tuning. 47
3-10 Simulated CDR settling behavior at the VCO control voltage. ..........................48
3-11 Input data signal versus recovered clock under the locked condition. ..................48
3-12 Die photograph of 24GHz CDR. ..............................................................49
3-13 Measured tuning range plot with 3 bits digital control for coarse tuning. ............50
3-14 VCO tuning range and gain at digital bits 111. ..................................................50
3-15 Jitter histogram of the recovered clock at 400MHz for a PRBS $2^{31}-1$ input. ....51
3-16 Spectrum of the recovered clock at 24GHz for a PRBS $2^{31}-1$ input. ..............52
3-17 Spectrum of 400Mbps PRBS $2^n-1$ signal (top), PNRZ signal after edge detection in the phase detector (middle), and recovered clock at 24GHz (bottom). ....................52
3-18 Phase noise plot of the recovered clock at 24GHz for a PRBS $2^7-1$ input. .......53
3-19 Phase noise plot of the recovered clock at 24GHz for a PRBS $2^{31}-1$ input. ........53
3-20 Plots of (a) amplitude and (b) phase spectra for $x(t)$ and corresponding waveform in time domain. ..................................................................................58
4-1 Block diagram of original transceiver at a motor section. ......................................62
4-2 Block diagram of transmitter at motor side. ..........................................................62
4-3 Block diagram of the interface between a CDR and a mixer. .................................63
4-4 Block diagram of IF generator ..............................................................................64
4-5 Block diagram and waveform of (a) divide-by-2.5 and (b) divide-by-1.5. ..............66
4-6 Block diagram of (a) DETFF and schematic of (b) MUX, (c) LATCH, and (d) AND plus LATCH ........................................................................................................67
4-7 Block diagram of 8-to-1 MUX and attenuator .......................................................68
4-8 Schematic of capacitor bank .................................................................................68
4-9 Schematic of three stage LO buffer .......................................................................70
<table>
<thead>
<tr>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-10</td>
<td>Schematic of up-conversion mixer.</td>
</tr>
<tr>
<td>4-11</td>
<td>Generation of undesired interferers by mixing harmonics of IF signal with LO signal.</td>
</tr>
<tr>
<td>4-12</td>
<td>Schematic of power amplifier.</td>
</tr>
<tr>
<td>4-13</td>
<td>Die photograph and testing PC board of IF generator.</td>
</tr>
<tr>
<td>4-14</td>
<td>Spectrum and waveform of IF signals at (a) 400MHz, (b) 800MHz, (c) 1.2GHz, (d) 1.5GHz, (e) 2.0GHz, (f) 2.4GHz, and (g) 3.0GHz.</td>
</tr>
<tr>
<td>4-15</td>
<td>Generation of undesired interferers due to the mixing of 2nd, 3rd, and 5th order harmonics of IF signals with LO signal.</td>
</tr>
<tr>
<td>4-16</td>
<td>Die photograph of crystalless transceiver at motor section.</td>
</tr>
<tr>
<td>4-17</td>
<td>Block diagram of transmitter at motor side.</td>
</tr>
<tr>
<td>4-18</td>
<td>Spectrum of TX motor 1 with attenuator.</td>
</tr>
<tr>
<td>4-19</td>
<td>Spectrum of TX motor 1 without attenuator.</td>
</tr>
<tr>
<td>4-20</td>
<td>Zoomed-in spectrum of TX motor 1.</td>
</tr>
<tr>
<td>4-21</td>
<td>Spectrum of TX motor 2 with attenuator.</td>
</tr>
<tr>
<td>4-22</td>
<td>Spectrum of TX motor 2 without an attenuator.</td>
</tr>
<tr>
<td>4-23</td>
<td>Spectrum of TX motor 3 with attenuator.</td>
</tr>
<tr>
<td>4-24</td>
<td>Spectrum of TX motor 3 without attenuator.</td>
</tr>
<tr>
<td>4-25</td>
<td>The impact of interferer signals on desired channels with attenuator on.</td>
</tr>
<tr>
<td>4-26</td>
<td>Waveform and spectrum of (a) un-modulated carrier and (b) ASK modulated carrier.</td>
</tr>
<tr>
<td>4-27</td>
<td>Waveform and spectrum of square wave with 50% duty cycle.</td>
</tr>
<tr>
<td>4-28</td>
<td>Spectrum of TX output at motor 5 (26GHz) before and after ASK modulation with 25-MHz square signal.</td>
</tr>
<tr>
<td>4-29</td>
<td>Waveform of TX output at motor 5 after ASK modulation with 25-MHz square signal.</td>
</tr>
<tr>
<td>4-30</td>
<td>Spectrum of TX output at motor 5 before and after the ASK modulation with 50Mbps PRBS $2^{31}-1$ data signal.</td>
</tr>
<tr>
<td>4-31</td>
<td>Eye diagram output at motor 5 after ASK modulation with a 50Mbps PRBS $2^{31}-1$ data signal.</td>
</tr>
</tbody>
</table>
4-32 \hspace{1em} Setup of wireless link demonstration at TX motor side.....................................................89

4-33 \hspace{1em} Spectrum of TX output (a) before modulation (b) after ASK modulation with 25-MHz square clock signal. (c) Waveform of TX output after ASK modulation with 25MHz square clock signal. (d) Spectrum of received 26-GHz carrier signal amplitude modulated by 25-MHz square signal (with metallic cover).........................90

5-1 \hspace{1em} Block diagram of receiver chain at motor section. ............................................................92

5-2 \hspace{1em} Positive feed back path due to parasitic inductors in multistage single-ended amplifiers. ..........................................................................................................................93

5-3 \hspace{1em} Schematic of baseband amplifier.......................................................................................95

5-4 \hspace{1em} Schematic of the wide-swing cascode current mirror..........................................................96

5-5 \hspace{1em} Die photograph and baseband amplifier PC board for testing...........................................97

5-6 \hspace{1em} Waveform of a single-ended square wave input at 200MHz. Differential outputs when input voltage level is (a) 6.8mV_{pp}, (b) 20mV_{pp} and (c) 30mV_{pp}. .........................................................99

5-7 \hspace{1em} Measured 3-dB bandwidth of baseband amplifier in frequency domain.........................100

5-8 \hspace{1em} Block diagram of RX chain at motor section and measurement setup. .........................101

5-9 \hspace{1em} RX output power as function of input single sideband power and input carrier power (AM modulation index of 100%). .................................................................102

5-10 \hspace{1em} Measured BER versus input power.....................................................................................103

5-11 \hspace{1em} Plots of (a) Amplitude modulated 16.8-GHz carrier with 200-MHz square wave at LNA input. (b) Spectrum of demodulated 200MHz signal at BB output. (c) Waveforms of demodulated 200MHz signal at BB output and 400MHz recovered clock at CDR output. (d) Jitter histogram of recovered clock at 400MHz. .........................104

5-12 \hspace{1em} Plots of (a) Amplitude modulated 16.8-GHz carrier with 400-Mbps PRBS 2^{31}-1 at LNA input. (b) Spectrum of demodulated 400Mbps signal at BB output. (c) Waveforms of demodulated 400Mbps signal at BB output and 400MHz recovered clock at CDR output. (d) Jitter histogram of recovered clock at 400MHz. .........................105

5-13 \hspace{1em} Block diagram of TRX at motor section and measurement setup. .................................107

5-14 \hspace{1em} Spectrum of demodulated baseband signal in RX when (a) TX is off, (b) TX is on and a modulating signal for TX is a 50-MHz clock, and (c) TX is on and a modulating signal for TX is a 50-Mbps PRBS 2^7-1 signal. The plots on the right side are the zoomed-in plots. ........................................................................................................108
5-15 RMS jitter plots of recovered clock with and without turning on TX for (a) 200-MHz square clock, (b) 400-Mbps PRBS $2^7$-1, (c) 400-Mbps PRBS $2^{23}$-1, and (d) 400-Mbps PRBS $2^{31}$-1 modulating signal for RF input. .................................................................110

5-16 BER plots (a) 400-Mbps PRBS $2^7$-1 modulation signal for RF input with TX on and off, (b) 400-Mbps PRBS $2^{31}$-1 with TX on and off, (c) TX on with 400-Mbps PRBS $2^7$-1 and $2^{31}$-1 modulation signal, and (d) TX off with 400-Mbps PRBS $2^7$-1 and $2^{31}$-1.................................................................................................111

5-17 RMS jitter plots at RF input power of -47dBm with TX on and off for (a) 200MHz square clock, (b) 400Mbps PRBS $2^7$-1, (c) 400Mbps PRBS $2^{23}$-1, and (d) 400Mbps PRBS $2^{31}$-1. The connection between the LNA and duplexer is not laser cut.................113

5-18 BER plots at RF input power of -47dBm for (a) 400Mbps PRBS $2^7$-1 with TX on and off, and (b) 400Mbps PRBS $2^{31}$-1 with TX on and off. The connection between LNA and duplexer is not laser cut. ..................................................................................................114

5-19 Measurement setup for the duplex operation of TRX at motor side.............................114

5-20 Spectrum of both RX and TX band at motor side .........................................................115

5-21 Measurement set up for link demonstration and block diagrams of TX and RX ..........116

5-22 Waveform of (a) amplitude modulated signal by a 400Mbps pattern 060606 at TX output, (b) demodulated signal at BB out, and recovered clock at CDR output with total 39dB attenuation between the PA output and LNA input. ........................................117

5-23 Waveform of (a) amplitude modulated signal by a 400Mbps pattern 01506250 at TX output, (b) demodulated signal at BB out, and recovered clock at CDR output with total 39dB attenuation between the PA output and LNA input. ........................................118

5-24 Waveform of (a) amplitude modulated signal by a 400-Mbps 060606 pattern at TX output, (b) demodulated signal at BB out, and recovered clock at CDR output with total 20dB attenuation between the PA output and LNA input. ........................................118

5-25 Waveform of (a) amplitude modulated signal by a 400-Mbps 01506250 pattern at TX output, (b) demodulated signal at BB out, and recovered clock at CDR output with total 20dB attenuation between the PA output and LNA input. ........................................119

5-26 Waveform of demodulated signal (varying amplitude levels 01506250) at BB output when the data rate of modulating signal is (a) 200Mbps and (b) 100Mbps with total 20dB attenuation between the PA output and LNA input. ........................................119

5-27 Waveform of (a) amplitude modulated signal by a 400-Mbps 0241353246 pattern at TX output, (b) demodulated signal at BB output, and recovered clock at CDR output with total 20dB attenuation between the PA output and LNA input. ........................................121
Waveform of demodulated signal (varying amplitude levels 0241353246) at BB output when the data rate of modulating signal is (a) 200Mbps and (b) 100Mbps with total 20dB attenuation between the PA output and LNA input ..................................................122

Jitter histogram of (a) demodulated signal at BB out and (b) recovered clock at CDR output for a modulating signal at 400Mbps with total 20dB attenuation between the PA output and LNA input ................................................................................................122

Block diagram of CDR test structure ................................................................................................126

Schematic of the 5.84GHz LC VCO .............................................................................................127

Die photograph of 5.84GHz CDR. ..............................................................................................129

Photograph of CDR testing printed circuit board ........................................................................129

Plot of VCO tuning range and gain at digital bits 0000000 ..........................................................130

Plot of recovered clock at 365MHz and jitter histogram for a PRBS 2^31-1 .........................131

Spectrum of recovered clock at 5.84GHz for a PRBS 2^31-1 input signal ...............................131

Plot of phase noise of recovered clock at 5.84GHz for a PRBS 2^31-1 input signal ...............132

Measurement setup for the transmitter at motor side using an external IF source ..........133

Spectrum of TX motor 1 driven with an external IF signal source ......................................134

Zoomed-in spectrum of TX motor 1 driven with an external IF signal source .....................134

Spectrum of TX motor 7 driven with an external IF signal source ......................................135

Zoomed-in spectrum of TX motor 7 driven with an external IF signal source .....................135
Use of wireless inter-chip data communication to isolate return paths of high voltage motor drive sections and a low voltage digital control section in an engine controller board of a Hybrid Electric Vehicle (HEV) is presented. The return voltage levels can differ by several hundreds of volts. Presently, the board utilizes numerous photo-couplers that can support ~1 Mbps data rate. Use of conventional radio architecture for this application requires a frequency reference for each high voltage section. This increases cost and board area that makes the approach impractical. Cost effectively providing frequency reference and clock is a fundamental challenge in two way wireless inter-chip communication systems for this type of isolation applications.

A fully integrated merged 400-Mbps clock data recovery (CDR) local oscillator (LO) generation circuit which provides both 24-GHz LO signal for a TX and 400-MHz clock for a RX has been demonstrated in a 130-nm foundry CMOS process. A voltage controlled oscillator (VCO) operation at higher than the input data rate at 400Mbps by using a divider (divide-by-60) in the feedback loop enables generation of 24-GHz LO signal for TX and integration of an LC-VCO that uses an inductor with practical size and Q. Including the divider in the feedback loop provides additional degree of freedom for reducing the size of loop filter capacitors for integration. The jitter performance of recovered clock at 400MHz is the lowest among fully
integrated CDR’s with the similar data rate (~400Mbps) in the literature. The phase noise of LO signal generated in a CDR with a PRBS $2^{31}-1$ input is ~10dB worse than that with a clock input.

A fully integrated FDMA TX chain at motor side incorporating a CDR, an up conversion mixer, a power amplifier, an IF-generator and an attenuator is demonstrated in the UMC 130-nm CMOS technology. The TX output powers range from the minimum of -4.6dBm to the maximum of 2.3dBm. The target output power is 0dBm. The increased phase noise of LO generated by a CDR does not degrade the performance of ASK systems using a square law detector in the receiver. It should also be possible to use the LO for wide bandwidth systems with other low order modulation schemes. The feasibility of establishing a wireless link within the controller board is also demonstrated using the TX. This indicates that a TX integrated with an RX incorporating a CDR can bypass the need for an external frequency reference. The wireless link demonstration on the board suggests communication range of 15cm should be possible. TX consumes ~192mW of power.

An entire RX chain including a new differential baseband amplifier is demonstrated. The RX chain has IP$_{1dB}$ of -45dBm and sensitivity of ~-45dBm for BER of $10^{-12}$ and 400-Mbps data rate. Furthermore, full-duplex operations of TRX at motor side with an on-chip antenna are investigated by comparing BER performance of RX chain and RMS jitter of recovered clock with TX on and off. The BER degradation due to the TX turned on is small when the input power is sufficiently large to achieve BER of less than $10^{-12}$. RMS jitters of recovered clock increase by no more than ~1ps from ~2.5ps when TX is turned on. These suggest the feasibility of full-duplex operation for CMOS radios with an on-chip antenna. The receiver is also used to detect multi-level AM signals.
CHAPTER 1
WIRELESS INTERCONNECTS IN ENGINE CONTROLLER BOARDS

1.1 Introduction

Design of an interface in engine controller board of a Hybrid Electric Vehicle (HEV) [1]-[4] where high voltage motor drive sections and a low voltage digital control section coexist is challenging. The return voltage levels for the sections can differ by greater than 300 volt (V). Presently, the two sections have been electrically isolated using photo-couplers to protect the low voltage section from overvoltage damages. However, the use of more than 10 photo couplers increases cost not to mention the low data transmission rate of less than 1Mpbs. In order to replace photo-couplers used in the hybrid engine controller board, silicon based solutions have been utilized to suggest the feasibility to lower cost and increase data rate.

As an alternative to photo-coupler, an electronic isolator that isolates the ground level of high and low voltage sections by coupling signals has been investigated. Several isolators using capacitive coupling method in silicon on insulator (SOI) technology are reported in [5]-[7]. The isolator can achieve 2.3kV ac isolation and 100-MHz signal transmission in an area of 1.5mm² [7]. This approach, however, requires a large external coupling capacitor. The electronic isolator can also be realized using inductive coupling [8]. Such an isolator implemented in 130-nm CMOS technology achieves only 70-V DC isolation due to the low breakdown voltage which is not suitable for the hybrid engine controller board.

Wireless interconnects using single chip radios including an on-chip antenna can be another lower cost, and high data rate (faster than 100’s of Mbps) alternative to the photo-couplers. Unlike the others, it can be fully realized in foundry CMOS. An on-chip antenna is a key block to implement this. On-chip antennas have been extensively studied [9], [10] in both indoor and outdoor environment and integrated in a 20-GHz down converter [11] and a 24-GHz
transmitter [12] for wireless communication. The feasibility of on-chip antennas used for wireless communication in the hybrid engine controller board has been verified [8].

Two separate integrated wireless transceiver circuits can operate with two different ground potentials to handle the large voltage difference. Use of wireless interconnects can also reduce the PC board area by removing metal traces for making connections from and to the photo-couplers. The frequency bands and channels can be allocated without satisfying the emission rules of the Federal Communications Commission (FCC) because the board is contained inside a metallic cover. Incidentally, wireless interconnects using ZigBee could be another wireless solution. However, ZigBee supports very low data rate and requires external crystal references for implementation.

### 1.2 System Overview

Figure 1-1 shows a hybrid engine controller board with two low voltage control nodes (D1, D2) and 12 high voltage motor nodes (M1~M12). Control nodes D1 and D2 called deadtime controllers located at the low voltage section transmit phase information to six motor drivers M1~M6 or M7~M8 in the high voltage sections. The fault status of each driver is transmitted back to the deadtime controller. There are also two links that transmit the motor temperature to the deadtime controller. Among multiple access schemes, Code Division Multiple Access (CDMA) [13] is chosen for downlink from a deadtime controller to each of 6 motors. For a data rate of 50Mbps per channel, spreading spectrum is achieved by multiplying 8-bit Walsh codes with each data bits, which results in a chip rate of 400Mcps per channel. Total 6 encoded waveforms for motor 1~6 are added together in time domain and formed multi-level signal with a chip rate of 400Mcps for transmission [8]. The deadtime controller needs only one transmitter to support the six channels, thereby dramatically reducing RF circuit complexity. For an uplink from the motor to the deadtime controller, Frequency Division Multiple Access (FDMA) is
chosen. Each of two deadtime controllers has a CDMA transmitter and a FDMA receiver supporting 7 channels. Each of six motors has a CDMA receiver and a FDMA transmitter.

Figure 1-1. Engine controller board for a HEV. D1 and D2 communicate with M1~M6 and M7~M12, respectively (Courtesy of TOYOTA).

Figures 1-2 and 1-3 show signaling scheme for the up and down links and frequency bands in the transmitter and receiver, respectively. The transmission and reception bands are separated by 6GHz to improve isolation between the two bands. The system requires duplex operation with a data transmission rate of 400Mcps from the low voltage digital control section to the high voltage motor drive section and a data transmission rate of 50Mbps from the high voltage motor to the deadtime controller in the low voltage section. The transmission from the low voltage section utilizes a 15.6-18GHz band and the transmission from the high voltage section utilizes a
24.2-27.2GHz. More detailed system specifications can be found in [14]. The frequency plans of transmitter and the receiver at the motor side are summarized in Table 1-1 and depicted in Figure 1-4. In addition, the frequency plans of transmitter and receiver at the deadtime controller side are summarized in Table 1-2 and shown in Figure 1-5.

![Diagram](image-url)

**Figure 1-2.** Signaling scheme for the up (FDMA) and down (CDMA) links.

![Diagram](image-url)

**Figure 1-3.** Frequency bands and data rate in deadtime controller and motors.

**Table 1-1.** Frequency plans for transmitter and receiver at the motor side

<table>
<thead>
<tr>
<th>TX channel</th>
<th>Freq. Band (GHz)</th>
<th>RX channel</th>
<th>Freq. Band (GHz)</th>
<th>Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>24.2~24.6</td>
<td>1</td>
<td>15.6~18.0, C1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>24.6~25.0</td>
<td>2</td>
<td>15.6~18.0, C2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>25.0~25.35</td>
<td>3</td>
<td>15.6~18.0, C3</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>25.35~25.7</td>
<td>4</td>
<td>15.6~18.0, C4</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>25.8~26.2</td>
<td>5</td>
<td>15.6~18.0, C5</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>26.2~26.6</td>
<td>6</td>
<td>15.6~18.0, C6</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>26.8~27.2</td>
<td></td>
<td></td>
<td>7</td>
</tr>
</tbody>
</table>
Figure 1-4. Frequency plans for the transceiver at the motor side.

Table 1-2. Frequency plan for transmitter and receiver at deadtime controller

<table>
<thead>
<tr>
<th>TX channel</th>
<th>Freq. Band (GHz)</th>
<th>RX channel</th>
<th>Freq. Band (GHz)</th>
<th>Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>15.6~18.0, C1</td>
<td>1</td>
<td>24.2~24.6</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>15.6~18.0, C2</td>
<td>2</td>
<td>24.6~25.0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>15.6~18.0, C3</td>
<td>3</td>
<td>25.0~25.35</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>15.6~18.0, C4</td>
<td>4</td>
<td>25.35~25.7</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>15.6~18.0, C5</td>
<td>5</td>
<td>25.8~26.2</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>15.6~18.0, C6</td>
<td>6</td>
<td>26.2~26.6</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 1-5. Frequency plan for transceiver at deadtime controller side.
It should be noted that the frequency plans for motor 4 and motor 7 have been slightly changed from the original one where the center frequency of motor 4 and motor 7 are located at 25.6GHz and 26.8GHz respectively. The frequency of motor 4 is shifted down by 100MHz and motor 7 is shifted up by 200MHz in the updated frequency plan. This is because the 25.5GHz and 27GHz are generated by mixing 24GHz with 1.5GHz and 3GHz intermediate frequencies (IF) respectively. This is much simpler than mixing 24GHz with 1.6GHz and 2.8GHz. The IF-frequency generation will be discussed in Chapter 4. Because of this change, the overall required TX bandwidth at motor side or, equivalently, RX bandwidth at deadtime controller was changed from 2.8GHz to 3GHz.

To evaluate the ability of system to detect the transmitted signal, with an acceptable error probability, in the presence of noise, link budget analyses are necessary first step. For a separation of 15cm, the link budget analysis for an individual channel of the FDMA links is summarized in Table. 1-3. The output TX power is 0dBm and propagation loss at 27GHz is 45dB. An on-chip dipole antenna on a 100-µm thick substrate has gain of -8 dB [15]. The required $E_b/N_o$ for BER of $10^{-13}$ of a system using non coherent ASK modulation is 14.5dB [16]. The bandwidth of RX is 50MHz and noise figure of RX is assumed 8dB. With all these information taken into account, the required receiver sensitivity is -74.3dBm and link margin is greater than 15dB for the FDMA link. The link budget analysis for CDMA is also shown in Table 1-4, where sensitivity is -74.3dBm and link margin is 21.3dB.

Lastly, if these wireless links were implemented using conventional radio architecture, the system would require 12 crystal references on motor nodes to provide TX LO signals. This would make implementing a wireless interconnect system impractical due to increased cost.
overcome this challenge, this dissertation research explored system and circuit techniques for crystalless operation of wireless inter-chip data communication.

Table 1-3. Link margin analysis for FDMA

<table>
<thead>
<tr>
<th>FDMA (From TX motor to RX deadtime controller)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Range (R)</td>
<td>15 cm</td>
</tr>
<tr>
<td>TX power</td>
<td>0 dBm</td>
</tr>
<tr>
<td>Propagation Loss @ 27 GHz ((\lambda/4\pi R)^2)</td>
<td>45 dB</td>
</tr>
<tr>
<td>Antenna Gain (0.25(\lambda = 3.2\ mm)</td>
<td>-7 dB</td>
</tr>
<tr>
<td>Received power</td>
<td>-59 dBm</td>
</tr>
<tr>
<td>Thermal Noise [kT (°K)]</td>
<td>-173.8 dBm/Hz</td>
</tr>
<tr>
<td>Bandwidth (50 MHz)</td>
<td>77 dB</td>
</tr>
<tr>
<td>(E_b/N_o) for BER of 1x10^{-13} for ASK</td>
<td>14.5 dB</td>
</tr>
<tr>
<td>RX noise figure</td>
<td>8 dB</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>-74.3 dBm</td>
</tr>
<tr>
<td>Link margin</td>
<td>15.3 dB</td>
</tr>
</tbody>
</table>

Table 1-4. Link margin analysis for CDMA

<table>
<thead>
<tr>
<th>CDMA (From TX deadtime controller to RX motor)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Range (R)</td>
<td>15 cm</td>
</tr>
<tr>
<td>TX power (Total power ~10dBm)</td>
<td>2 dBm</td>
</tr>
<tr>
<td>Propagation Loss @ 18 GHz ((\lambda/4\pi R)^2)</td>
<td>41 dB</td>
</tr>
<tr>
<td>Antenna Gain (0.25(\lambda = 3.2\ mm)</td>
<td>-7 dB</td>
</tr>
<tr>
<td>Received power</td>
<td>-53 dBm</td>
</tr>
<tr>
<td>Thermal Noise [kT (°K)]</td>
<td>-173.8 dBm/Hz</td>
</tr>
<tr>
<td>Bandwidth (50 MHz)</td>
<td>77 dB</td>
</tr>
<tr>
<td>(E_b/N_o) for BER of 1x10^{-13} for ASK</td>
<td>14.5 dB</td>
</tr>
<tr>
<td>RX noise figure</td>
<td>8 dB</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>-74.3 dBm</td>
</tr>
<tr>
<td>Link margin</td>
<td>21.3 dB</td>
</tr>
</tbody>
</table>

1.3 Organization of Dissertation

The emphases of research are the design of clock and data recovery circuit, crystalless transmitter in motor sections, investigation of the impact of full-duplex operation of TRX with an on-chip antenna, and demonstration of a wireless link between TX at deadtime controller and RX at motor side.

In Chapter 1, the system overview of wireless inter-chip data communication on an engine controller board of hybrid electric vehicles (HEV) for signal return path isolation is presented.
Chapter 2 discusses the general properties of such data format as pseudo random binary sequence (PRBS) that a CDR is typically used to characterize. Properties of a phase detector (PD) in comparison to a phase frequency detector (PFD) are described. A linear model of CDR is presented to evaluate the stability of the CDR loop. Finally, the choice of CDR loop bandwidth is discussed.

Chapter 3 is dedicated to the proposed CDR design and measurement results. The circuit design of each block making up the CDR and simulation results are described. A fully integrated CDR based 24-GHz LO generation circuit is demonstrated in the UMC 130-nm CMOS technology. Qualitative analysis for the impact of phase noise from the recovered clock to ASK systems using a square-law detector is presented.

In Chapter 4, the circuit designs of all TX building blocks at motor side, which include an up-conversion mixer, 3-stage LO buffers, IF generator, attenuator, 8-to-1 multiplexer, and power amplifier are discussed. Compared to the original TX architecture, the new TX architecture adopts a modified CDR structure described in Chapter 3, which enables the system to be simpler and more power efficient. The stand-alone test structure of IF generator followed by an entire TX chain supporting 7 different channels are characterized. Finally, the feasibility of establishing a wireless link using the TX is demonstrated in the UMC 130-nm CMOS technology.

In Chapter 5, full RX chains with an improved baseband amplifier for the motor side are fully characterized. The full-duplex operation of TRX at motor side with an on-chip antenna is investigated by comparing BER performance of RX and RMS jitters of recovered clocks. Finally, multiple level AM detection is demonstrated using the RX. The measurements indicated that further work will be needed to make the RX fully support the multiple level signals. Finally, the dissertation is summarized and future works are suggested in Chapter 6.
CHAPTER 2
OVERVIEW OF CLOCK AND DATA RECOVERY CIRCUIT

2.1 Introduction

Use of wireless interconnection to isolate the return paths of multiple high voltage motor drive sections and low voltage digital control section in an engine controller board of a Hybrid Electric Vehicle (HEV) is described in Chapter 1. The system requires duplex operation with a data transmission rate of 400Mbps from the low voltage digital control section to the high voltage motor drive section and a data transmission rate of 50Mbps from a high voltage section. Transmission from the low voltage section utilizes a 15.6-18GHz band and transmission from the high voltage section utilizes a 24.2-27.2GHz band. The return level for these sections can differ by several hundreds of volts. Use of conventional radio architecture for this application requires a frequency reference for each high voltage section which increases cost and board area. To mitigate this, the system has been architected so that the receiver and transmitter for the high voltage motor sections require no external frequency reference.

The conventional LO generation scheme such as a phase lock loop (PLL) cannot be adopted. Instead, clock and data recovery circuit (CDR) is used as a perfect candidate for internal clock generation from incoming data, which is one of unique features of CDR. In the crystalless transceiver architecture, the choice of non-coherent ASK detection as well as CDR obviates the need for the use of external frequency references. Diode detection in RX removes a frequency synthesizer and mixer drivers which simplify the RX and reduce the power consumption. Furthermore, CDR internally recovers clocks, which can be viewed as the frequency reference for the system if the jitter or phase noise of recovered clock can be kept to the minimum.

Chapter 2 describes the basics of clock and data recovery circuit (CDR). Among many CDR structures, a phase locked loop (PLL) based CDR with a linear phase detector such as
Hogge detector [17] is emphasized. The serial data stream whose format is called “non-return-to-zero” is transmitted without an accompanying additional timing reference in many digital systems. A receiver is then required to process this data stream and generate synchronous clock. It is the CDR in the receiver that recovers the clock. Generally, a CDR first produces clock from an internal VCO and then phase-aligns the clock to the transitions of incoming data stream with the help of feedback loop in a PLL. The challenge of clock and data recovery is that data could be a long sequence of ONEs or ZEROs without a transition. During a no-transition period, the voltage controlled oscillator in the PLL may drift or vary in the clock frequency due to the absence of additional correction signal provided by the feedback loop. To ensure frequent transitions, coding schemes are often used.

In Chapter 2, the non return to zero data (NRZ) format is first described. A phase detector suited to handle the data format is then introduced. A CDR loop analysis using a linear model for determination of loop stability information by calculating phase margin is presented. Finally, Chapter 2 describes how to choose the CDR bandwidth which is critical for improving the jitter performance of CDR.

2.2 Non Return to Zero (NRZ) Test Pattern

NRZ test patterns [18] have been created for system test and verification in digital communication systems. In NRZ signaling, the signal is either high (one) or low (zero) during the entire bit period with equal probability regardless of the state of preceding bits. There is a change in level whenever data change from a high to low or from a low to high. It is therefore possible to have a binary sequence with a long string of consecutive ones or zeros. This situation is referred as having “low transition density” [18]. Since low transition density data contain low frequency contents, it is difficult to implement ac coupling function and to recover low jitter clock.
It is difficult to generate a completely random binary sequence. Commonly used are pseudo random binary sequences (PRBS) [19]. The PRBS is in fact deterministic and repeats. A PRBS is typically expressed as a PRBS $2^X-1$, which creates a pattern $2^X-1$ bit long (called length, L), that repeats every $2^X-1$ bits. The maximum run length defined by the number of maximum consecutive ones or zeros is equivalent to X.

![PRBS signal diagram](image)

Figure 2-1. PRBS signal (a) waveform in time domain, (b) autocorrelation, and (c) power spectral density in frequency domain [20].

Figure 2-1(a) shows the waveform in time domain for a PRBS $2^3-1$ signal. A pattern repeats itself every 7 bits and the maximum run length is equal to 3. Figure 2-1(b) shows the autocorrelation functions for each component of test patterns shown in Figure 2-1(a). The autocorrelation of 7-bit test pattern approximates a triangle and the accuracy improves with increasing pattern length. Figure 2-1(c) shows the Fourier transform of autocorrelation functions to calculate the power spectral density. There are straightforward relationships between the time
domain characteristics of PRBS test patterns and their frequency domain characteristics. Important observations are as follows [20].

1. The nulls in the sinc^2(f) envelop occur at integer multiples of the data rate.
2. Spectral lines are evenly spaced at an interval inversely proportional to pattern length.
3. The sinc^2(f) envelop flattens out as the data rate and/or pattern length increases.

In the limit, as the pattern length approaches infinity, the spacing between the spectral lines becomes infinitesimally small and the spectrum shape approaches a continuous sinc2(f) function.

2.3 Clock and Data Recovery (CDR) Overview

A CDR employing a phase locked loop (PLL) to tune the frequency and phase of a VCO to match that of the input data is of focus. Figure 2-2 shows a block diagram of the PLL-based CDR circuit which consists of a phase detector, a charge pump, a loop filter, and a VCO. The phase detector (PD) compares the phase and frequency of the input data with that of a voltage controlled oscillator (VCO) and generates UP/DOWN pulsed signals for phase and frequency correction to the charge pump which is followed by a loop filter. A control voltage from the loop filter adjusts the phase and frequency of an oscillator to match that of the input data. The following subsections overview the fundamentals of CDR blocks.

![Block diagram of CDR](image)

Figure 2-2. Block diagram of CDR.

2.3.1 Linear Phase Detector for Random Data

A topology of a linear phase detector [17], [21] and its output waveform under locked condition are shown in Figure 2-3. Under this condition in which the rising edge of clock
samples exactly the center of incoming data, UP signal and DN signal produce the same pulse widths. Retimed data can be either signal A or signal B. Signal A is a half clock delayed and signal B is a clock delayed compared to the input data, DIN.

![Linear phase detector diagram](image1)

**Figure 2-3.** A linear phase detector (a) block diagram, and (b) waveform under the locked condition.

![Waveform diagram](image2)

**Figure 2-4.** Waveform of phase detector for (a) early clock and (b) late clock.

Figure 2-4 shows the waveform of (a) early and (b) late clock in the linear phase detector. When the rising edge of clock samples the data before the center point (“early clock”), the area
under the UP signal is smaller than the DN signal such that the VCO delays the phase of clock, thereby CDR eventually gets driven to the locked condition. On the other hand, when the rising edge of clock samples the data after the center point (“late clock”) the area under the UP signal is bigger than the DN signal so that VCO pulls the phase of clock forward thereby once again driving the CDR to the locked condition.

Unlike a tri-state PFD operation [22] in a PLL, where UP and DN signals turn on simultaneously under the locked condition, DN signal is produced a half clock cycle after the UP signal. This offset in time of the UP and DN signals under locked condition perturbs VCO control line every time data transition occurs, which degrades VCO phase noise.

Figure 2-5 shows the characteristic of linear phase detector assuming the maximum transition density of 100%. As $\Phi_{\text{DIN}} - \Phi_{\text{CLK}}$ becomes zero, the output of phase detector which is an average value of UP-DN equals zero consistent with Figure 2-3(b). Here, $\Phi_{\text{DIN}} - \Phi_{\text{CLK}}$ being zero means the locked case where the rising clock samples the center of data bit period. When $\Phi_{\text{DIN}} - \Phi_{\text{CLK}}$ becomes negative (-$\pi$<$\Phi_{\text{DIN}} - \Phi_{\text{CLK}}$<0), it corresponds to the early clock case shown in Figure 2-4(a). Conversely, when $\Phi_{\text{DIN}} - \Phi_{\text{CLK}}$ becomes positive (0<$\Phi_{\text{DIN}} - \Phi_{\text{CLK}}$<$\pi$), it corresponds to the late clock case shown in Figure 2-4(b). A linear phase detector as its name implies has limited frequency tracking capability which can be explained using Figure 2-5. Considering the case where large initial frequency difference between DIN and CLK exits, the resulting large phase/frequency error causes the output of phase detector to be quickly swept across different regions (i.e. from point A to point B in Figure 2-5). This is so called “cycle slipping” [23], [24]. This phase detector output alternating between regions can be averaged to zero by a loop filter. When this occurs, slipping, recovered clock frequency oscillates without getting proper correction information from the feed back loop.
On the other hand, a typical tri-state PFD in a PLL possesses input-output characteristic such that certain polarity, positive or negative rather than zero is provided when being swept across different regions as shown in Fig 2-6. That is why a PFD in a PLL can track frequency not to mention phase.

Figure 2-5. Input-output characteristic of linear phase detector.

Figure 2-6. Input-output characteristic of tri-state phase and frequency detector (PFD).
2.3.2 Linear Model of CDR

Figure 2-7. Linear model of PLL based CDR circuit.

Figure 2-7 shows a linear model of CDR circuit. A conventional CDR circuit does not have a divider in the feedback loop. Since frequency division decreases phase by the division ratios, N, a phase divider block is added in the loop. A linear phase detector can be modeled as \((1/2) \cdot (1/\pi)\), where \((1/2)\) represents the average transition density for a PRBS (Pseudo Random Bit Sequence) pattern which is the typical input data format for CDR circuit [25] and \((1/\pi)\) represents the gain of linear phase detector or the slope of curve in Figure 2-5. Including \((1/2)\) in the phase detector model reveals that the gain of phase detector depends on the data transition density.

A charge pump can be simply modeled as a charge pump current \(I_{cp}\). In general, a VCO produces a frequency output which is the input voltage, \(v_{in}(t)\) multiplied by VCO gain, \(K_{VCO}\).

\[
f_{out}(t) = K_{VCO} \cdot v_{in}(t)
\]

The unit of \(K_{VCO}\) is Hz/V. Integration of output frequency \(f_{out}(t)\) leads to phase output as a function of input voltage and VCO gain.
Therefore, the corresponding Laplace model of VCO is simply expressed as \( \frac{2\pi K_{\text{VCO}}}{s} \). The representation of frequency divider in time domain is represented as

\[
\phi_{\text{out}}(t) = \int_{-\infty}^{\infty} 2\pi \cdot f_{\text{out}}(\tau) \, d\tau = \int_{-\infty}^{\infty} 2\pi \cdot K_{\text{VCO}} \cdot v_{\text{in}}(t) \, d\tau
\]

where \( N \) is the division factor. If this is expressed in terms of phase, then \( \phi_{\text{out}}(t) \) is

\[
\phi_{\text{out}}(t) = \int_{-\infty}^{t} 2\pi \cdot f_{\text{out}}(\tau) \, d\tau = \int_{-\infty}^{t} 2\pi \cdot \frac{1}{N} \cdot f_{\text{in}}(\tau) \, d\tau = \frac{1}{N} \cdot \phi_{\text{in}}(t).
\]

This means the phase transfer function of a frequency divider is as mentioned simply modeled as \( 1/N \).

For a loop filter model, the simplest form is chosen, which is a 2nd order passive lead-lag filter whose schematic and transfer function are shown in Figure 2-8.

Figure 2-8. The 2\textsuperscript{nd} order passive lead-lag filter (a) schematic and (b) transfer function.

In order to characterize the stability of feedback loop with phase margin (PM), the open loop gain of CDR needs to be computed. Using the linear model of each block described above, the open loop transfer function is
The open loop transfer function (2.1) is for a type-two, third-order system. Among the three poles, two poles are at the origin and the third pole $\omega_p$ and one zero $\omega_z$ are located at

$$\omega_p = \frac{C_z + C_p}{R_z C_z C_p} \quad \text{and} \quad \omega_z = \frac{1}{R_z C_z}.$$  \hfill (2.2)

A Bode plot of the open loop gain is depicted in Figure 2-9. The intersection of magnitude plot and 0dB occurs at $\omega_t$, which is referred to as the gain bandwidth of CDR circuit. As indicated in Figure 2-9, phase margin (PM) is defined as the difference between the phase angle at $\omega_t$ and $-180^\circ$. From (2.1), PM can be written as

$$PM = \text{phase} \, @ \, \omega_t - (-180^\circ)$$

$$= \tan^{-1}\left(\frac{\omega_t}{\omega_z}\right) - 90^\circ - 90^\circ - \tan^{-1}\left(\frac{\omega_t}{\omega_p}\right) - (-180^\circ)$$

$$= \tan^{-1}\left(\frac{\omega_t}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_t}{\omega_p}\right).$$ \hfill (2.3)
Figure 2-9. Bode plot of the open loop gain for a CDR circuit.

To maximize the phase margin, $\omega_t$ should be chosen when $\frac{\partial \text{PM}}{\partial \omega_t}$ is equal to 0.

$$\frac{\partial \text{PM}}{\partial \omega_t} = \frac{1}{1 + \left(\frac{\omega_t}{\omega_z}\right)^2} \cdot \frac{1}{\omega_z} - \frac{1}{1 + \left(\frac{\omega_t}{\omega_p}\right)^2} \cdot \frac{1}{\omega_p} = 0 \quad (2.4)$$

Solving (2.4) for $\omega_t$, the maximum phase margin occurs when

$$\omega_{t, PM} = \sqrt{\omega_z \omega_p} \quad (2.5)$$

$\sqrt{\omega_z \omega_p}$ is the geometric mean and is located in the center point between the zero $\omega_Z$ and the third pole $\omega_P$ on a log scale. Typically, phase margin of $60^\circ$ or higher is preferred for stability. If
$\omega_Z$ is defined as a factor $\alpha$ below $\omega_{t,PM}$ and $\omega_P$ a factor $\beta$ above $\omega_{t,PM}$, the unity gain frequency, $\omega_t$ can be derived from (2.1) by replacing $s = j\omega$ and setting the open loop gain $H_{OL}(S)$ as 1. The $\omega_t$ is then expressed as,

$$\omega_t = \frac{I_{CP} \cdot K_{VCO} \cdot R_Z}{N} \cdot \frac{C_Z}{C_Z + C_p} \cdot \frac{\beta}{\alpha} \cdot \sqrt{\frac{1 + \alpha^2}{1 + \beta^2}}$$

(2.6)

In addition, the size of passive elements in the loop filter can be calculated.

$$R_Z = \frac{N}{I_{CP} K_{VCO}} \cdot \omega_t$$

(2.7)

$$C_Z = \frac{\alpha}{R_Z \omega_t} = \frac{I_{CP} K_{VCO}}{N} \cdot \frac{1}{\omega_t^2} \cdot \alpha$$

(2.8)

$$C_p = \frac{I_{CP} K_{VCO}}{N} \cdot \frac{1}{\omega_t^2} \cdot \frac{1}{\alpha} \cdot \sqrt{\frac{1 + \alpha^2}{1 + \beta^2}}$$

(2.9)

To achieve sufficient phase margin, both $\alpha$ and $\beta$ should be equal and higher than $\sqrt{10}$ [18].

2.3.3 Choosing a Bandwidth of CDR

For conventional CDRs for wire line applications, many standards such as SONET/SDH (synchronous optical network /synchronous Digital Hierarchy) are already well established and they include detailed jitter specifications. Two important jitter specifications related to choosing the bandwidth of CDR in this proposal is jitter transfer and jitter tolerance. The jitter transfer is defined as the ratio of the output to input jitter of the CDR. This measures how much jitter from the input data signal is present on the output clock signal. A low-pass response is required to suppress jitter. The jitter tolerance is defined as the maxim amount of jitter allowed on the data input signal while still achieving the necessary bit error rates (BER) in detecting the data. It is desired to have a large jitter tolerance bandwidth to track jitter on the data input. Figure 2-10
shows a jitter plot for a simple second order CDR circuit where a loop filter consists of a resistor in series with a capacitor.

![Diagram of CDR circuit](image)

**Figure 2-10.** Linear model of second order CDR and its jitter plot.

**Table 2-1. Summary of jitter specification**

<table>
<thead>
<tr>
<th>Rate</th>
<th>Corner frequency (f&lt;sub&gt;C&lt;/sub&gt;)</th>
<th>Jitter tolerance</th>
<th>Jitter transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>OC-1</td>
<td>20kHz</td>
<td>40kHz</td>
<td></td>
</tr>
<tr>
<td>OC-3</td>
<td>65kHz</td>
<td>130kHz</td>
<td></td>
</tr>
<tr>
<td>OC-12</td>
<td>250kHz</td>
<td>500kHz</td>
<td></td>
</tr>
<tr>
<td>OC-48</td>
<td>1MHz</td>
<td>2MHz</td>
<td></td>
</tr>
</tbody>
</table>

Table 2-1 shows the corner frequency of the SONET/SDH (synchronous optical network/synchronous Digital Hierarchy) jitter specification [27], [28]. The SONET/SDH bit rates are multiples of 51.84Mbps. For instance OC-3 signal would have a data rate of 3×51.84Mbps which is 155.2Mbps. The OC-12 rate is therefore 12×51.84Mbps or 622.08Mbps.

The conflicting requirement between the jitter transfer requiring a narrow band CDR and the jitter tolerance requiring a wide band CDR suggests that the bandwidth must be chosen in the half way between the corner frequencies of two jitter specifications [29]. For example, the bandwidth of CDR should be chosen between 250 kHz and 500 kHz for OC-12 data rate.
2.4 Summary

Chapter 2 described the basics of clock and data recovery circuits. Since a CDR circuit recovers clock from a digital data stream whose format is NRZ type, the characteristics of NRZ data format are first discussed. The circuit description and operation of linear phase detector are then followed by loop analysis on linear model of CDR. Finally, the discussion for the choice of CDR bandwidth is presented.
CHAPTER 3
CLOCK AND DATA RECOVERY CIRCUIT AS AN LO GENERATOR

3.1 Introduction

The CDR circuit in the transceiver for the motor side takes in 400-Mbps data to generate 400-MHz and 24-GHz LO signal. Moderate data rate (100~1000 Mbps) CDR’s use a voltage controlled oscillator (VCO) based on a relaxation oscillator (R.O.) [30]-[34], and typically jitter performance is not good compared to the LC-VCO because of low Q and many noisy transistors used in the circuits. In addition, these CDR’s require a large external capacitor for the loop filter except in [32] which requires an external crystal frequency reference.

Use of an LC-VCO with better phase noise and jitter performance at moderate data rates is challenging due to a low quality factor (Q) and large size of required inductors. A new CDR structure allows use of an LC-VCO and fully integrated loop filter capacitor despite moderate input data rate (400Mbps). Since the incoming data for CDR is 400Mbps, a conventional CDR structure will generate recovered clock at only 400MHz. However, the new CDR structure generates recovered clocks at both 400MHz and 24GHz. This 24-GHz clock can be used as an LO signal to drive an up-conversion mixer at TX side. RMS phase error of LO signal would be an important performance parameter in digital communication systems, especially those using phase modulation. However, since the transmitter utilizes amplitude shift keying (ASK), the phase noise issue is bypassed. Qualitative analysis on the impact of phase noise on ASK modulated signal at TX output is presented.

3.2 New CDR Structure

Figure 3-1 and 3-2 show a block diagram of a conventional CDR structure and the new LO generation circuit merged into a CDR circuit, respectively. The new CDR structure allows use of an on-chip LC-VCO at input data rate of 400 Mbps. Different from the conventional CDR
structure which consist of a phase detector, a charge pump, a loop filter, and a VCO, the new CDR circuit includes a frequency divider in the feedback path, which is similar to continuous-rate CDR’s [29], [30], [33].

![Figure 3-1. Block diagram of conventional CDR.](image1)

![Figure 3-2. Block diagram of new CDR.](image2)

Even if structural similarity between proposed CDR and continuous-rate CDR’s exists, none of the continuous-rate CDR’s have been used as an LO generator. By choosing a division
ratio of 60, the VCO is made to operate at 24 GHz. At this frequency, the VCO needs a 352-pH center tapped inductor. The Q of such an on-chip inductor is ~18. These easily make the architecture suitable for integration.

A conventional CDR often incorporates a large off-chip capacitor to realize a small loop bandwidth, thereby low-pass filtering the high frequency noise/jitter of incoming data. The capacitor $C_Z$ in the loop filter in Figure 3-2 is typically sized as [35]:

$$C_Z \approx \frac{K_{VCO} \times I_{CP}}{N \times (W_{BW})^2}$$

(3.1)

where $K_{VCO}$, $I_{CP}$, $N$, $W_{BW}$ are VCO gain, charge pump current, division ratio, and loop bandwidth, respectively. The CDR structure that contains a divider after a VCO gives the second benefit of providing an additional control factor to size and reduce the capacitor. In general, as VCO frequency increases, $N$ should increase proportionally assuming the input data rate is fixed. $K_{VCO}$ also increase accordingly. However, since the amount of $K_{VCO}$ increase compared to that of $N$ increase can be made smaller, the size of capacitor $C_Z$ can be reduced.

Considering the fact that smaller $K_{VCO}$ leads to better phase noise performance, $K_{VCO}$ is already minimized to begin with. For this reason, $K_{VCO}$ itself is not a free knob of reducing $C_Z$. Incidentally, $I_{CP}$ in the numerator of Equation (3-1) can not be arbitrarily lowered to reduce the size of capacitor $C_Z$, either. When $I_{CP}$ is lowered, the resistor $R_Z$ of loop filter increases, which typically degrade the phase noise and jitter performance of the recovered clock [35].

3.2.1 Loop Filter

A loop filter in Figure 3-2 is a 2nd order passive filter formed with one silicide blocked p$^+$ polysilicon resistor and two polysilicon/n-well MOS capacitors [36]. The resulting CDR is then a type-two, third order system [37]. The loop bandwidth of 500-kHz, charge pump current of 60µA, divide ratio of 60 and VCO gain of 1GHz/V are chosen. Equations (2.7) ~ (2.9) are used
to compute $C_Z$, $C_P$, and $R_Z$ whose values are 288pF, 32pF and 3.5kΩ, respectively. The biggest capacitor $C_Z$ occupies 180µm×213µm. The simulated phase margin of CDR loop is 55°.

3.2.2 Voltage Controlled Oscillator (VCO)

Figure 3-3 shows a circuit schematic of a 24GHz VCO, which consists of an LC-tank, an NMOS cross coupled pair, noise filter inductor and capacitor, a pair of accumulation mode varactors [38], [39] for continuous fine tuning, a digitally tuned capacitor bank for discrete coarse tuning, a PMOS tail current source, and a pair of inductively loaded buffers. The capacitor bank supports 3-bit digital tuning to keep the VCO gain low for reduced phase noise and loop filter capacitor values, while maintaining an adequate tuning range. To increase inductor Q, L0 is drawn as a single center tapped spiral inductor [40] using top two copper layers shunted together. The total metal thickness is ~1.5µm. The metal spacing, width, and number of turns are 3µm, 4µm, and 3, respectively. The inductance for L1 is 352pH, and the inductor including a polysilicon pattern ground shield [41], [42] occupies 72µm×72µm. The simulated Q [43] of inductor is about 18 at 24GHz.

The Q of MOS varactor at 24GHz is 13 in the accumulation region and 32 in the depletion region [44]. Since the Q of varactor at 24GHz is almost comparable to the inductor Q, assuming VCO oscillates at 24GHz at the control voltage of 0.6V, the overall tank Q is ~9. The capacitor bank consists of three parallel binary-scaled MOS varactors whose control voltages are connected to either $V_{DD}$ for $C_{min}$ or ground for $C_{max}$. The measured $C_{max}/C_{min}$ is around 3.5. A large capacitor C1 in parallel with the current source M3 shunts noise frequencies around the 2$^{nd}$ harmonic to ground. A bottom inductor L4 also provides high impedance at the tail in order to block the 2$^{nd}$ harmonic current from flowing through the switching pair (M1 and M2) to ground, which de-Qs the original LC tank [45].
Figure 3-4 shows the divide-by-60 circuit which starts with a divide-by-2 stage in front followed by a two stage tapered inductor loaded buffers to reduce the load seen by the first divide-by-2 stage. A divide-by-2 stage is used to restore 50% duty cycle for the output of divide-by-5 stage. For the final stage, rather than using a divide-by-3 stage, a divide-by-1.5 followed by a divid-by-2 stage is used to generate recovered clock with a 50% duty cycle. Since the phase detector uses both rising/falling edges of clock to determine the phase difference, keeping a 50% duty cycle is important. All the divider blocks are designed using current mode logic (CML) static frequency dividers with the bottom current source omitted [46] for low voltage operation and a PMOS load with grounded gate [47] except for the divide-by-5 stage where poly silicon
resistor loads are used to increase the maximum operating frequency. Careful transistor sizing for the 1st divide-by-2 circuit handling 24GHz is required [48].

![2 Stage Buffer Diagram](image)

Figure 3-4. Block diagram of divider chain (divide-by-60).

The divide-by-5 stage consists of three differential D-flip-flops and one AND gates. The first and second flip flops form a divide-by-4, while the third flip-flop adds an extra delay of a clock period to divide-by-5 [49]. Divide-by-1.5 is realized using a conventional divide-by-3 in which a single-edge triggered D-flip-flop is simply replaced by a double-edge triggered D-flip-flop. The circuit schematic of divide-by-2 and each latch circuit is shown in Figure 3-5 [50]. The divide-by-5 and divide-by-1.5 circuits will be discussed in details in Chapter 4.

![Block Diagram of Divide-by-2 and Latch Circuit](image)

Figure 3-5. Block diagram of divide-by-2 and implementation of latch circuit.

### 3.2.4 Phase Detector

Among popular phase detectors, the linear (Hogge) phase detector has some advantages over non-linear (Alexander) phase detector [51]. One advantage is that a CDR loop adopting a
linear phase detector and a charge pump can be understood using the linear loop theory in a straightforward manner. The other advantage is that a CDR shows less jittery behavior on the VCO control line under the locked condition. Most CDR circuits for multi-Gb/s applications use a non-linear phase detector because a linear phase detector usually poses serious speed bottleneck for high frequency operation in the interface between a linear phase detector and a charge pump. The CDR only needs to support 400-Mbps data rate which is sufficiently low to use a linear phase detector.

Figure 3-6. Block diagram of (a) phase detector and (b) implementation of each DFF using DCVSL logic circuits.
Figure 3-6 shows (a) the block diagram of the Hogge phase detector and (b) the circuit schematic of the D flip-flop (DFF), respectively. The Hogge phase detector consists of two flip-flops, one XOR and one XNOR. In real implementation of DFF1 and DFF2, differential signaling is utilized although only positive signal is drawn for simplicity in the block diagram. Since DFFs operate with differential signals, differential-cascode-voltage-switch-logic gates (DCVSL) [52] are employed.

3.2.5 Charge Pump (CP)

The schematic of charge pump is shown in Figure 3-7 [53], [54]. The “UP” in the M11 and M12 are directly connected to the output of XNOR gate in the phase detector, and “DN” in the M15 and M16 are connected to the output of XOR gate in the phase detector. The output node of charge pump is followed by a loop filter.

The charge pump current is chosen to be 60µA. Since 60µA is relatively small, it could be sensitive to process and temperature variations. In order to mitigate this, the length and width of
MOS transistors are intentionally chosen to be large, which also helps to alleviate the mismatch and channel-length modulation problem of mirror transistors. M2 is added to facilitate external current control. C1 and C2 are both 10-pF capacitors to bypass current spikes when M11 and M16 switch between on and off. M12 and M15 are charge removal transistors, which help to cut out long current tail when switch M11 and M16 turn off. As CP output voltage deviates from \( V_{DD}/2 \), the current mismatch between up and down path becomes pronounced due to the finite output resistance at the CP output node.

### 3.3 Simulation Results

Figure 3-8 shows a current mismatch between up and down current as the output voltage of charge pump sweeps from 0V to \( V_{DD} \). With the \( V_{DD} \) of 1.2V, the mismatch between UP and DN current gets bigger as the output voltage deviates from 0.6V. Therefore, under the locked condition, VCO must be designed to oscillate at 24GHz at the control voltage of \(~0.6V\) so that the charge pump optimally operates around 0.6V at which the UP and DN current mismatch is the least.

![Figure 3-8. Plot of current mismatch between up and down current in the charge pump.](image)
Figure 3-9 shows the plot of VCO tuning range with 3-bits digital control for coarse tuning. The gain decreases as the control voltage deviates from center because of the saturation of varactor capacitance. As seen in Figure 3-9, a set of digital bits 000 corresponds to the target tuning curve, which generates 24GHz at VCO control voltage of 0.6V. The lowest digital bits (000) for the target frequency of 24GHz are used in simulations is because based on the previous UMC 130-nm tape-out, the a measured frequency would shift down by ~2GHz compared to the simulation frequency.

![VCO control voltage (V) vs Frequency (Hz)](image)

Figure 3-9. Simulated VCO tuning range plot with 3-bit digital control for coarse tuning.

The plot in Figure 3-10 is the transient response of VCO control voltage. Around 3.5µs, the CDR enters the locking region, where recovered clock samples the center of incoming data.

Figure 3-11 shows the input data versus recovered clock that is locked. The simulation indicates that the recovered clock almost keeps a 50% duty cycle and the rising edge of clock samples the center of bit period as expected.
Figure 3-10. Simulated CDR settling behavior at the VCO control voltage.

Figure 3-11. Input data signal versus recovered clock under the locked condition.
3.4 Measurement Results

The CDR has been fabricated in the UMC 130-nm logic CMOS technology with eight copper layers. Shown in Figure 3-12 is a die photograph. The chip area without the bond pads occupies 0.79mm×0.58mm. The CDR has been measured on a PC board with the chip directly mounted on the board (chip-on-board). The measured CDR locking range is from 395 to 405Mpbs.

![Figure 3-12. Die photograph of 24GHz CDR.](image)

Figure 3-12 shows the measured 3-bit VCO tuning characteristics. The VCO can be tuned from 21.5GHz to 24.5GHz. In order to generate the 24-GHz LO signal, digital tuning bit setting, 111 was selected which covers from 23.5GHz to 24.5GHz. Compared to the simulation result in Figure 3-9, the measured tuning curves shifted down by ~2GHz such that digital tuning bit 111 covers the target frequency around 24GHz. Figure 3-14 shows a VCO tuning range and the corresponding VCO gain for digital tuning bit setting, 111. The measured VCO gain is ~1.3GHz/V around the control voltage of 0.6V in comparison to the designed VCO gain of
1GHz/V. The supply voltage is 1.2V. The VCO draws 6.6mA. The total power consumption of CDR excluding that of the buffers for driving an external 50Ω load is 18.3mW.

Figure 3-13. Measured tuning range plot with 3 bits digital control for coarse tuning.

Figure 3-14. VCO tuning range and gain at digital bits 111.
Figure 3-15 shows the jitter histogram of recovered clock at 400MHz with a PRBS $2^{31}-1$ input. The measured RMS and peak to peak (p-p) jitters are 2.6ps (rms) and 22.2ps (p-p), which are 0.1% and 0.89% of bit period, respectively. Figure 3-16 shows the spectrum of recovered clock at 24GHz with a 400-Mbps PRBS $2^{31}-1$ input when the CDR is locked. The spectrum of peak near the center frequency is broadened besides the higher in-band phase noise. This broadening originates from the 400-MHz peak extracted during the edge detection process [55] in the linear phase detector. The PRBS NRZ signal with a null at the data rate frequency is converted in the phase detector into pseudo non return to zero (PNRZ) signal with a peak at the data rate frequency [55]. The broadened spectrum near the center frequency results from the densely spaced spectral lines in the PNRZ spectrum. The spacing of spectral lines is scaled by $2^n-1$. For $n$ of 31, the spacing between spectral lines is ~0.2 Hz. Figure 3-17 illustrates how the peaks of spectrum for the source PRBS signal manifest in the CDR output spectrum through the CDR loop.
Figure 3-16. Spectrum of the recovered clock at 24GHz for a PRBS $2^{31}-1$ input.

Figure 3-17. Spectrum of 400Mbps PRBS $2^n-1$ signal (top), PNRZ signal after edge detection in the phase detector (middle), and recovered clock at 24GHz (bottom).
Figure 3-18. Phase noise plot of the recovered clock at 24GHz for a PRBS $2^7-1$ input.

Figure 3-19. Phase noise plot of the recovered clock at 24GHz for a PRBS $2^{31}-1$ input.
Wider span phase noise plots for a PRBS $2^7$-1 and $2^{31}$-1 are shown in Figure 3-18 and 3-19, respectively. In Figure 3-18, spurs at integer multiples of $\sim 3.15$MHz from 24-GHz output signal result from the spectral lines $\sim 3.15$-MHz spacing ($400 \text{ MHz} / (2^7-1)$) in the 400-MHz PNRZ spectrum. Although, the spurs are out of the loop bandwidth of CDR of $\sim 500$ kHz, they are too big for the CDR low-pass loop filter to completely suppress them. In the case of 400Mbps PRBS $2^{31}$-1, the phase noise plot does not show any discrete spurs. This is because the spacing between spectral lines is so close ($\sim$less than 0.2Hz) that the resolution bandwidth of 10 kHz for the measurements spreads and averages them.

Table 3-1. Summary of measured CDR performance

<table>
<thead>
<tr>
<th>Technology</th>
<th>Input data rate</th>
<th>CDR lock range</th>
<th>VCO tuning range</th>
</tr>
</thead>
<tbody>
<tr>
<td>UMC 130-nm</td>
<td>400-Mbps</td>
<td>395-Mbps ~ 405-Mbps</td>
<td>21.5-GHz ~ 24.5-GHz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>24-GHz clock phase noise (dBc/Hz)</th>
<th>PRBS $2^7$-1</th>
<th>PRBS $2^{23}$-1</th>
<th>PRBS $2^{31}$-1</th>
<th>clock input @200MHz</th>
<th>VCO</th>
</tr>
</thead>
<tbody>
<tr>
<td>@ 60-KHz offset</td>
<td>-62.3</td>
<td>-61.0</td>
<td>-61.1</td>
<td>-70.9</td>
<td>-53.4</td>
</tr>
<tr>
<td>@ 1-MHz offset</td>
<td>-92.1</td>
<td>-90.0</td>
<td>-88.7</td>
<td>-92.6</td>
<td>-96.2</td>
</tr>
<tr>
<td>@ 10-MHz offset</td>
<td>-</td>
<td>-112.2</td>
<td>-111.0</td>
<td>-115.2</td>
<td>-115.8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>400-MHz clock jitter (ps)</th>
<th>RMS rising</th>
<th>Peak to peak</th>
<th>Input data jitter (RMS rising)</th>
</tr>
</thead>
<tbody>
<tr>
<td>with PRBS $2^7$-1</td>
<td>2.19</td>
<td>16.22</td>
<td>1.67</td>
</tr>
<tr>
<td>with PRBS $2^{23}$-1</td>
<td>2.36</td>
<td>21.11</td>
<td>1.89</td>
</tr>
<tr>
<td>with PRBS $2^{31}$-1</td>
<td>2.58</td>
<td>22.22</td>
<td>1.93</td>
</tr>
</tbody>
</table>

| BER | Less than $10^{-13}$ with 95% confidence for PRBS $2^{31}$-1 |
| Chip size (w/o pad) | $789 \times 584 \mu m^2$ |

<table>
<thead>
<tr>
<th>Power consumption (V$_{DD}$:1.2V)</th>
<th>Phase detector (µW)</th>
<th>Charge pump (µW)</th>
<th>VCO (mW)</th>
<th>Divider (mW)</th>
<th>Total (w/o buffer) (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>501.6</td>
<td>248.4</td>
<td>7.92</td>
<td>9.64</td>
<td>18.31</td>
<td></td>
</tr>
</tbody>
</table>

The phase noise performance is measured with PRBS $2^7$-1, $2^{23}$-1 and $2^{31}$-1 data streams, and clock input at 200MHz. The phase noise performance is also measured without locking the 24-GHz VCO. These results as well as other measured characteristics of CDR are summarized in Table 3-1. For a PRBS $2^{31}$-1 input, in-band phase noise at 60-kHz offset is -61dBc/Hz. The
phase noise at 1-MHz offset is -89dBc/Hz and the out-of-band phase noise at 10-MHz offset is -111dBc/Hz. The in-band phase noise at 60 kHz increases by ~9 dB when PRBS data are used instead of a 200-MHz clock. The phase noise at 10-MHz offset increases by 3.0, and 4.2 dB for PRBS $2^{23}$-1 and $2^{31}$-1 input, respectively compared to the clock case. The BER performance has been measured using an Agilent N4906A BERT. At 400 Mbps, a total number of $3.456 \times 10^{13}$ bits was monitored over a 24-hour period. The measured BER with 95% confidence is less than $10^{-13}$.

The actual data pattern for the wireless communication system in a hybrid engine controller board is random. The system uses code division multiple access with 8-bit long Walsh codes [14]. The receiver limits (Figure 4-2) the CDMA waveforms to generate an NRZ data fed to the CDR. Because of this, the long sequences of ones or zeros in the PRBS $2^{31}$-1 are not present in the real NRZ data, and the jitter performance and phase noise performance of the actual system should be better than that for the PRBS $2^{31}$-1 input case.

Table 3-2. Comparison of jitter performance

<table>
<thead>
<tr>
<th>Ref No.</th>
<th>VCO type / Tech</th>
<th>Off-Chip</th>
<th>PRBS</th>
<th>Output RMS clock jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>[30]</td>
<td>R.O / 0.18µm CMOS</td>
<td>CAP</td>
<td>$2^{31}$-1</td>
<td>23.4ps (1.46% UI) @622MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>80.4ps (1.25% UI) @155MHz</td>
</tr>
<tr>
<td>[31]</td>
<td>R.O / 0.35µm CMOS</td>
<td>CAP</td>
<td>$2^{31}$-1</td>
<td>10.9ps (0.68% UI) @622MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>18.8ps (0.38% UI) @200MHz</td>
</tr>
<tr>
<td>[32]</td>
<td>R.O / 0.25µm CMOS</td>
<td>Ext. CLK</td>
<td>-</td>
<td>4.5ps (0.23% UI) @500MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8.3ps (0.21% UI) @250MHz</td>
</tr>
<tr>
<td>[33]</td>
<td>R.O / Bipolar</td>
<td>CAP</td>
<td>$2^{7}$-1</td>
<td>5.2ps (0.32% UI) @622MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>14.4ps (0.22% UI) @155MHz</td>
</tr>
<tr>
<td>[34]</td>
<td>R.O / Bipolar</td>
<td>CAP</td>
<td>$2^{7}$-1</td>
<td>62.7ps (0.97% UI) @155MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[56]</td>
<td>R.O / Bipolar</td>
<td>Ext. VCO</td>
<td>$2^{23}$-1</td>
<td>17.2ps (0.27% UI) @155MHz</td>
</tr>
<tr>
<td>This work</td>
<td>0.13µm CMOS</td>
<td>On-Chip</td>
<td>$2^{31}$-1</td>
<td>2.6ps (0.1% UI) @400MHz</td>
</tr>
</tbody>
</table>
Table 3-2 summarizes the jitter performance of CDR’s in the literature with moderate data rates between 100 and 600 Mbps. The jitter of only fully integrated CDR reported here is the lowest by almost factor of two. The measurement results of another CDR test structure that recovers clock at 400MHz and at 5.84GHz for TX LO signal are also presented in Appendix A.

3.5 The Influence of Phase Noise of CDR on ASK Modulation

A TX employing an unconventional LO from CDR must deal with the effects of LO phase noise since the LO phase noise from a CDR using jittery incoming data as essentially a frequency reference is worse than that from a PLL using a crystal oscillator as a frequency reference. The effects of phase noise on ASK modulation can be analyzed qualitatively.

Referring to TX in Figure 4-2, the LO signal from the CDR can be expressed as

\[ s(t) = A \cos(\omega_c t + \phi_n(t)) \]

\[ = A \cos(\omega_c t) \cos(\phi_n(t)) - A \sin(\omega_c t) \sin(\phi_n(t)) \]

\[ \cong A \cos(\omega_c t) - A \phi_n(t) \sin(\omega_c t) \]

\[ = A \sqrt{1 + (\phi_n(t))^2} \cos(\omega_c t + \theta(t)) \]

where \( A \) denotes amplitude of LO signal, \( \omega_c \) is LO frequency, \( \phi_n(t) \) is phase noise, \( \phi_n(t) \ll 1, \cos\phi_n(t) \approx 1, \sin\phi_n(t) \approx \phi_n(t), \) and \( \theta(t) = \tan^{-1}\phi_n(t) \) are assumed. The impact of phase noise, \( \phi_n(t) \) on the amplitude change is negligible. As discussed, IF signals are generated by frequency dividers. For instance, if 2-GHz IF signal is chosen, the original 24-GHz CDR output is frequency divided by 12. After the division, the overall phase noise improves by

\[ 20\log(24\text{GHz}/2\text{GHz}) \approx 21.6\text{dB} \] [57].

The LO signal from the CDR output and the IF signal from the divider output are mixed together. The former signal consists of desired input signal, \( S_{\text{CDR}} \) and undesired input noise, \( N_{\text{CDR}} \) Likewise the latter signal consists of desired input signal, \( S_{\text{DIV}} \) and undesired input noise, \( N_{\text{DIV}} \).
The mixer output is comprised of $S_{\text{OUT}}$, desired output signal, and $N_{\text{OUT}}$, undesired output noise:

$$S_{\text{OUT}} + N_{\text{OUT}} = S_{\text{CDR}}S_{\text{DIV}} + S_{\text{CDR}}N_{\text{DIV}} + S_{\text{DIV}}N_{\text{CDR}} + N_{\text{CDR}}N_{\text{DIV}}, \quad (3.3)$$

where the mixer is assumed noiseless, $N_{\text{CDR}}N_{\text{DIV}}$ can be neglected, and the first term is the desired signal and the second and the third terms constitute undesired noise at the mixer output.

The overall SNR at mixer output then can be approximated as [58]

$$\text{SNR}_{\text{OUT}} = \frac{S_{\text{CDR}} \times S_{\text{DIV}}}{S_{\text{CDR}} N_{\text{DIV}} + S_{\text{DIV}} N_{\text{CDR}}} = \frac{S_{\text{CDR}}}{N_{\text{CDR}}} \times \frac{S_{\text{DIV}}}{N_{\text{DIV}}} = \frac{\text{SNR}_{\text{CDR}} \times \text{SNR}_{\text{DIV}}}{\text{SNR}_{\text{CDR}} + \text{SNR}_{\text{DIV}}}. \quad (3.4)$$

The SNR at mixer output is dominated by the lower SNR among two input signals. Therefore, Equation (3.2) is the expression for the mixer output with phase variations mainly due to the CDR phase noise. Finally, the signal is amplitude modulated by the on-off switch in the power amplifier. If a square clock is assumed to be the modulating signal, then the modulating signal and modulated signal can be expressed as [59], [60]:

$$g(t) = \frac{1}{2} + \frac{2}{\pi} \left( \cos \omega_0 t - \frac{1}{3} \cos 3\omega_0 t + \frac{1}{5} \cos 5\omega_0 t - \frac{1}{7} \cos 7\omega_0 t + \cdots \right)$$

$$\leftrightarrow \quad G(\omega) = \sum_{k=-\infty}^{\infty} \frac{2}{\pi} \frac{\sin \pi k}{k} \delta(\omega - k\omega_0)$$

$$x(t) = g(t) \times s(t) = g(t) \times A \cos[\omega_c t + \theta(t)]$$

$$\leftrightarrow \quad X(\omega) = \frac{A}{2} \left[ G(\omega - \omega_c) e^{j\theta(t)} + G(\omega + \omega_c) e^{-j\theta(t)} \right] \quad (3.6)$$

where $G(\omega)$ and $X(\omega)$ are the Fourier transforms of $g(t)$ and $x(t)$, respectively, $\omega_0$ is the modulation angle frequency, $\omega_c$ is the carrier angle frequency.
The amplitude and phase spectra for x(t) and corresponding waveform in time domain are shown in Figs. 3-20(a), (b), and (c) in order. In Equation (3.6), θ(t) due to the phase noise from CDR manifests itself as phase variations of each spectral component of modulated signal in the phase spectrum in Figure 3-20(b), These are translated into the phase variations of carrier in the modulated signal in time domain as depicted in Figure 3-20(c). The modulating signal which carries the information is not affected by the phase variation θ(t).

Figure 3-20. Plots of (a) amplitude and (b) phase spectra for x(t) and corresponding waveform (c) in time domain.
When this amplitude modulated signal is demodulated by squaring and low pass filtering in the receiver, the effects of phase variations or LO phase noise is removed. The received amplitude modulated signal with phase variations is
\[ r(t) = A(t) \cdot \cos[\omega_c t + \theta(t) + \delta(t)], \]  
(3.7)
where \( \delta(t) \) represents the additional phase variations due to the transmission path between a transmitter and a receiver. If the ASK waveform of (3.7) is applied to the input of the square-law detector, the output signal \( r_1(t) \) is
\[ r_1(t) = \alpha \cdot r(t)^2 = \alpha \cdot (A(t) \cdot \cos[\omega_c t + \theta(t) + \delta(t)])^2 \]
\[ = \alpha \cdot A(t)^2 \cdot \left( 1 + \cos[2\omega_c t + 2\theta(t) + 2\delta(t)] \right), \]
(3.8)
where \( \alpha \) is a constant. After low pass filtering, the output \( r_2(t) \) is
\[ r_2(t) = \beta \cdot \alpha \cdot \frac{A(t)^2}{2} = \kappa \cdot \frac{A(t)}{2}, \]
(3.9)
where \( \beta \) and \( \kappa = \beta \cdot \alpha \) are constant, and \( A(t)^2 = A(t) \) when \( A(t)=0 \) or 1. As shown in Equation (3.9), LO phase noise has no effect in ASK systems using a square-law detector.

### 3.6 Conclusion

A merged 400-Mbps fully integrated CDR and 24-GHz LO generation circuit, a key component for a transceiver that can operate without a crystal frequency reference for wireless data communication in a hybrid engine controller board is proposed. The circuit fabricated in 130-nm logic CMOS achieves phase noise of -88.7dBc/Hz at 1MHz offset for the 24-GHz LO signal, RMS jitter of 2.6ps for the 400-MHz recovered clock and BER of less than \( 10^{-13} \) with a PRBS \( 2^{31}-1 \) input. The jitter and phase noise performance with the actual data pattern for the system should be better.
To accomplish this at the moderate data rate, the CDR architecture has been modified to include a frequency divider and an LC-VCO with reduced phase noise. The VCO operation at the frequency (24 GHz) 60 times higher than the 400-Mbps input data rate enables generation of LO signal for transmitter with an integrated LC-VCO that uses an inductor with practical size and Q. Including the divider provides additional degree of freedom for reducing the size of loop filter capacitors for integration. The LO signal at 24GHz from the CDR should be suitable for wireless communication systems using simple ASK modulation. It should also be possible to use it as an LO for wide bandwidth systems with other low order modulation schemes. The jitter of this fully integrated CDR reported here is the lowest by almost factor of two compared to the other CDR’s for similar data rate. Lastly, it is also reported the phase noise performance of LO signal generated in a CDR and the effects of PRBS input data on phase noise performance.

Finally, qualitative analysis of the impact of phase noise on ASK modulated signal at TX output and at RX baseband is presented. The increased phase noise of the LO generated by a CDR does not degrade the performance of ASK systems using a square law detector receiver.
CHAPTER 4
FDMA TRANSMITTER AT MOTOR SIDE

4.1 Introduction

The feasibility of implementing the receiver for the motor section in CMOS that supports 400Mbps is already demonstrated [61]. The receiver successfully non-coherently detected an amplitude modulated 400Mbps data stream using Schottky barrier diodes (SBD) [61]. Chapter 4 describes a FDMA transmitter that radiates ASK signal without using an external crystal reference.

Before delving into the main discussion of transmitter blocks, first, evolution of transmitter at a motor section for a simplicity and higher power-efficiency eliminating functionally redundant blocks is discussed. The circuit implementation of TX blocks, IF generator, 8 to 1 multiplexer, 3-stage LO buffers, up-conversion mixer, and power amplifier are then presented in order. In the sections 4.5 and 4.6, measurement results of IF generator and entire TX chain fabricated in UMC130-nm CMOS technology are presented. Finally, the feasibility of wireless link from a TX motor to the low voltage section within the controller board is demonstrated.

4.2 Evolution of Transmitter at Motor Side

A block diagram of the original transceiver at a motor section is shown in Figure 4-1. A CDR recovers the clock at 400MHz from an incoming 400-Mbps data. The recovered clock signal at 400MHz is followed by a divider that generates the low frequency reference signal for a PLL. The clock at 24GHz is then synthesized by the PLL and used as the LO signal in an up-conversion mixer. The recovered clock is also used to synchronize ADC and decoder operation.

This original transceiver has been simplified without compromising the performance of original transceiver. The main distinctive modification is that the phase locked loop (PLL) of transmitter no longer exists in the architecture shown in Figure 4-2. This becomes possible
because a new CDR structure that merges the PLL function into the VCO of CDR can directly provide the 24-GHz LO signal. Omitting the PLL greatly reduces the circuit complexity, area, and power consumption. Details of the new CDR architecture are already presented in Chapter 3. The CDR provides the frequency references for both 24-GHz LO signal in TX and 400-MHz clock for ADC and decoder in RX, which makes the transceiver a reference-less radio. With the choice of an appropriate modulation scheme such as non-coherent amplitude modulation, detrimental impact of phase noise degradation can be completely eliminated.

Figure 4-1. Block diagram of original transceiver at a motor section.

Figure 4-2. Block diagram of transmitter at motor side.
4.3 Circuit Topology of Transmitter at Motor Side

A block diagram of the updated transceiver at a motor section is shown in Figure 4-2. The transmitter is comprised of a CDR, an up-conversion mixer, 3 stage LO buffers which are not shown, an IF frequency generator, an attenuator and an 8-to-1 multiplexer, a power amplifier, a duplexer, and a 4-mm on-chip dipole antenna.

Figure 4-3. Block diagram of the interface between a CDR and a mixer.

The interface between a CDR and an up-conversion mixer is shown in Figure 4-3. A TX chain starts from the CDR which generates a 24-GHz LO signal. One branch from the CDR drives the IF frequency generator which produces 7 channels ranging from 400MHz to 3GHz. The IF generator is followed by an attenuator for harmonic control, and an 8-to-1 multiplexer for selecting one out of 7 possible channels. The 7th port is for direct connection to an external signal generator. The other branch from a CDR directly drives a mixer LO port through 3-stage inductor loaded cascode buffers. Because of the large layout separation (0.75mm) from the CDR output to the mixer LO port, these buffers must be inserted in order to maintain sufficient drive. An up-conversion mixer is followed by a class-E type power amplifier [62] that is amplitude
modulated using simple on-off switches. Finally, a duplexer following the power amplifier is connected to a 4mm on-chip dipole antenna.

4.3.1 IF Generator

Figure 4-4 shows a block diagram of an IF frequency generator. The grey divider blocks use $V_{DD}$ of 1.5V for improved driver operation. All the rest of blocks use $V_{DD}$ of 1.2V. Considering the fact that seven 350-µm long metal 8 lines from the output of IF generator are closely spaced (width: 1-µm and space: 0.5-µm), crosstalk [63] among signals is a concern. To alleviate this problem, only one selected branch carries signal, thereby eliminating the effects of crosstalk.

![Block diagram of IF generator](image)

Figure 4-4. Block diagram of IF generator.

A switch shown as a black box at the end of each branch is a simple shunt NMOS transistor which controls the signal flow. When the switch is “on” in a branch, signal is bypassed through the switch to the ground, and the branch is deactivated. On the other hand, when the
switch is “off”, the branch is able to pass signal onto the next block. Therefore, the switch for the selected is “off” to let the signal pass onto the next block while the switches for the other IF branches are on. The switch control can easily be achieved with the help of a 3-bit decoder implemented inside the 8 to 1 multiplexer. Since the outputs of a 3-bit binary decoder are “one-hot encoded” [64], adding an inverter after a decoder can provide the necessary control signals for the switches.

Table 4-1. IF signal generation

<table>
<thead>
<tr>
<th>Signal</th>
<th>Frequency</th>
<th>Generation</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO</td>
<td>24GHz</td>
<td>24GHz VCO at CDR</td>
</tr>
<tr>
<td>IF1</td>
<td>0.4GHz</td>
<td>LO/2/2/2.5/1.5/2/2</td>
</tr>
<tr>
<td>IF2</td>
<td>0.8GHz</td>
<td>LO/2/2/2.5/1.5/2</td>
</tr>
<tr>
<td>IF3</td>
<td>1.2GHz</td>
<td>LO/2/2/2.5/2</td>
</tr>
<tr>
<td>IF4</td>
<td>1.5GHz</td>
<td>LO/2/2/2</td>
</tr>
<tr>
<td>IF5</td>
<td>2.0GHz</td>
<td>LO/2/2/3</td>
</tr>
<tr>
<td>IF6</td>
<td>2.4GHz</td>
<td>LO/2/2/2.5</td>
</tr>
<tr>
<td>IF7</td>
<td>3.0GHz</td>
<td>LO/2/2</td>
</tr>
</tbody>
</table>

Table 4-1 summarizes the seven IF signal generation schemes from the 24-GHz LO of CDR. If IF signal does not keep 50% duty cycle, the output of up-conversion mixer will contain the undesired harmonic frequency contents that are generated by mixing of LO with harmonics of IF signal. In particular, the 2nd order harmonics of IF signal mixed with LO cause undesired frequency contents that fall in the neighboring motor channels.

Assuming the duty cycle of input clock is equal to 50%, the duty cycle of divide-by-1.5 and divide-by-2.5 output are 2:1 and 3:2, respectively. Therefore, divide-by-1.5 and divide-by-2.5 stages need to be followed by a divide-by-2 stage to restore the duty cycle to 50%. Among the seven IF generation circuits, IF5 (2GHz) and IF6 (2.4GHz) do not have 50% duty cycle. The 2nd order harmonics of these mixed with the 24-GHz LO signal produce signals at 20GHz and
28GHz for IF5, and at 19.2GHz and at 28.8GHz for IF6. Since these frequencies are, however, all out of 24.2-27.2GHz TX band, the deviation from 50% duty cycle for IF5 and IF6 is allowed.

Since the first divide-by-2 block must operate at the highest frequency of 24GHz, careful design attention is required especially when it is realized by a CML type static divider [48]. All divider blocks in the IF generator are the CML type static dividers. Figure 4-5 shows the schematic and waveform of divide-by-2.5 and divide-by-1.5 circuits. The divide-by-2.5 and divide-by-1.5 circuits are implemented using divide-by-5 and divide-by-3 circuits in which the conventional single-edge-triggered flip flops are simply replaced by double-edge-triggered flip flops (DETFF) [65].

Figure 4-5. Block diagram and waveform of (a) divide-by-2.5 and (b) divide-by-1.5.

A block diagram of DETFF and its circuit schematics are shown in Figure 4-6. In Figure 4-6(a), when CLK is high, the value stored in LATCH1 is multiplexed to the output while
LATCH2 is transparent. When CLK is low, the value stored in LATCH2 is multiplexed to the output while LATCH1 is transparent. Hence, DETFF samples the input data at both the rising and falling edges of clock signal. On the other hand, SETFF (single edged triggered flip flop) is triggered at only either the rising or the falling edge of clock signal. As shown in Figure 4-6(d), a DETFF can incorporate AND function by merging the AND function [66] and the DETFF. This increases the switching speed and reduces the power consumption.

Figure 4-6. Block diagram of (a) DETFF and schematic of (b) MUX, (c) LATCH, and (d) AND plus LATCH.
4.3.2 8-to-1 Multiplexer and Attenuator

Figure 4-7 shows an 8-to-1 multiplexer (MUX) and an attenuator. The seven frequency channels from 400MHz to 3GHz of IF generator are assigned to seven ports in the MUX and the last one port is allocated for an external signal source. The purpose of an attenuator block is both to reduce signal amplitude, and filter out high order harmonics from the incoming square wave so that the $g_m$ stage of up-conversion mixer can properly deal with the incoming IF signal.

The attenuator consists of three stage programmable RC low pass filters. Since the frequency of incoming signal can be one of seven different frequencies ranging from 400MHz to 3GHz, the corner frequency of a low pass filter should vary depending on the frequency of incoming signal. Each RC low pass filter is comprised of a 1-kΩ silicide blocked p$^+$ poly silicon resistor and a capacitor bank, where four digital bits synthesize the required corner frequency.

![Figure 4-7. Block diagram of 8-to-1 MUX and attenuator.]

![Figure 4-8. Schematic of capacitor bank.]

68
A schematic of capacitor bank is shown in Figure 4-8. There are 4 different sized capacitors with each branch connected to ground through a switching transistor. When the transistor is turned on by connecting the gate of transistor to $V_{DD}$, the capacitor connected to the transistor is activated. Thus, depending on the particular IF frequency selected by the 8-to-1 MUX, the control bits $b_1$, $b_2$, $b_3$, and $b_4$ can be connected to either $V_{DD}$ or GND to synthesize appropriate corner frequency for the RC low pass filter.

For $N$ identical stages, overall 3-dB bandwidth is given by [19]

$$\omega_{3\text{dB}} = \omega_{3\text{dB0}} \sqrt[N]{2} - 1$$

(4-1)

where $\omega_{3\text{dB0}}$ is the 3-dB bandwidth of each stage. For three identical stages, overall 3-dB bandwidth is then $\sim 0.5 \omega_{3\text{dB0}}$. For example, in the case of 400MHz IF signal, the 3-dB bandwidth of each stage ($\omega_{3\text{dB0}}$) should be 800MHz rather than 400MHz. With a resistor 1K$\Omega$, the total capacitance required to achieve the bandwidth of 800MHz for each stage is then $\sim 200fF$. This capacitance can then be synthesized by assigning $b_1$ $b_2$ $b_3$ $b_4$ of either 0 0 0 1 or 1 1 1 0.

A metal to metal capacitor using metal 5-8 layers is used for the capacitors in the bank. The width and length of all transistors shown in Figure 4-8 are 5$\mu$m and 120nm, respectively. Illustrated in Fig 4-7, there are two extra switches (switch1 and switch2) that enable incoming signal to bypass the RC stages for measurement purpose. When both switch1 and switch2 are turned on, signal would undergo smaller attenuation. Due to the large area of capacitor banks, the area occupied by the 8 to 1 MUX and attenuator is 320$\mu$m by 264$\mu$m.

### 4.3.3 Three Stage LO Buffer

The three stage LO buffer that interconnects the 24GHz output of CDR and the LO port of up-conversion mixer separated by $\sim 600\mu$m is shown in Figure 4-9. Since the operating frequency is as high as 24GHz, the inductance of metal lines between LO buffer stages should be properly
accounted. The width of line inductors $M_{L1}$, $M_{L2}$, and $M_{L3}$ are $2\mu m$, $1.2\mu m$ and $3\mu m$, respectively. The lengths of $M_{L1}$, $M_{L2}$ and $M_{L3}$ are $220\mu m$, $200\mu m$, and $160\mu m$, respectively. $M_{L1}$, $M_{L2}$, and $M_{L3}$ are all made of metal 8. The simulated corresponding inductance values from $M_{L1}$, $M_{L2}$, and $M_{L3}$ are around $220pH$, $200pH$, and $160pH$, respectively. The Q-factor of L1, L2, and L3 are chosen to be around 5 to accommodate the process variation. The size of all transistors $M_{n1}$~$M_{n6}$ is $14\mu m/120nm$. The supply voltage for the buffer is 1.5V.

![Schematic of three stage LO buffer.](image)

### 4.3.4 Up-conversion Mixer

Figure 4-10 shows the schematic of an up-conversion mixer which is configured as a double balanced mixer to reduce the LO feedthrough. Because of the voltage head room limitation, the bottom current source is taken out. The LO port is driven by the 24-GHz CDR output through the 3-stage LO buffers. The IF port of mixer is connected through the 8:1 MUX and attenuator to the IF frequency generator. IF signals should be sufficiently small such that transistors $M_{n1}$ and $M_{n2}$ can function as the $g_m$ stage of mixer without being distorted. In addition, harmonic control of IF signal is required in order to prevent unwanted harmonics of selected signal from falling into the neighboring channel as interfering signals.
The size of transistor $M_{n1}$ and $M_{n2}$ in the $g_m$ stage is 200µm/120nm. The size of transistors $M_{n3}$~$M_{n6}$ in the switching stage is all 30µm/120nm. The simulated conversion gain is around 0dB. The supply voltage of up-conversion mixer is 1.5V. The simulated power consumption is 17.6 mW.

![Schematic of up-conversion mixer.](image)

Figure 4-10. Schematic of up-conversion mixer.

Figure 4-11 shows how a mixing process generates undesired interferers from the harmonics of IF signal and how the undesired interferes affect signals in the neighboring channels. For instance, the 3rd harmonic of IF1 signal mixed with LO signal produces an interferer at 25.2GHz, which happens to be the same desired RF frequency of motor 3 at 25.2GHz. The 5th harmonic of IF1 signal mixed with LO signal also generates an interferer at 26.0GHz, which is the same frequency as the desired RF frequency of motor 5 at 26.0GHz. The interferer at 26.0GHz due to the 5th harmonic of IF1 signal should be negligible because of small signal power. However, an interferer at 26GHz is amplified by the higher gain in the following
Because the power amplifier following the mixer has a tuned gain response with a peak gain occurring at around 25.6GHz, the interferer at different frequencies are amplified with varying gains. Finally, the 3rd harmonic of IF2 mixed with LO produces an interferer at 26.4GHz, which is the same frequency as the desired RF frequency of motor 6 at 26.4GHz. Other harmonics of IF signal mixed with LO are all out of band of interest. In summary, it is important to have IF generator to be followed by an tunable filter that also attenuates the IF signal.

![Table and Diagram](image_url)

**Figure 4-11.** Generation of undesired interferers by mixing harmonics of IF signal with LO signal.

### 4.3.5 Power Amplifier

A single ended schematic consisting of three pre-amplifying stages and a class-E type power amplifier [67], [68] is shown in Figure 4-12. The pre-amplifying stages help to increase the signal swing thereby resulting in complete switching in the PA at the last stage. In the schematic, there are two NMOS switches. With the help of these two NMOS switches at the 2nd and 3rd stages, the LO signal can be amplified and quenched based on Data_in signal. The 50-Mbps amplitude modulating signal applied in the “Data_in” terminal generates ASK modulated
signal at the PA output. For L3~L6, circular shaped inductors with top two metal layers (metal 7 and metal 8) shunted together are used to increase inductor Q.

Figure 4-12. Schematic of power amplifier.

The PA is designed to generate 7dBm output power at all frequencies from 24.4 to 27 GHz with \( V_{DD} \) of 1.5V. The PA efficiency at the last stage is 33%. The overall PA efficiency is 27%. OP-1\text{dB} is designed to be around 7.4dBm. The PA consumes 50mW and the PA chip size is 634µm by 700µm. The designs and measurement results of a duplexer and a 4mm on-chip dipole antenna are described in [8], [15]. Finally, the simulated power consumption of each block in TX is summarized in Table 4-2. The PA dissipates ~38% of the total power in TX.

<table>
<thead>
<tr>
<th>Block</th>
<th>CDR</th>
<th>MIX</th>
<th>PA</th>
<th>IF generator</th>
<th>LO buffer</th>
<th>MUX &amp; Div2 &amp; Div2 buffer</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (mW)</td>
<td>20</td>
<td>7.6</td>
<td>50</td>
<td>20.4</td>
<td>22.7</td>
<td>12.2</td>
<td>132.9</td>
</tr>
<tr>
<td>Percentage (%)</td>
<td>15</td>
<td>5.7</td>
<td>37.6</td>
<td>15.3</td>
<td>17.1</td>
<td>9.2</td>
<td>100</td>
</tr>
</tbody>
</table>
4.4 Measurement Results of IF Generator

The standalone test structure of an IF generator together with an 8 to 1 MUX has been fabricated in the UMC 130-nm CMOS technology. Shown in Figure 4-13 are a die photograph and a testing PC board. IF generator has been measured on a PCB with the chip directly mounted on the board (chip-on-board). Sinusoidal signal at 12GHz from a signal generator is applied to the input of the IF generator by probe-landing directly on the chip. Output signal selected by the 8 to 1 MUX is then measured in the frequency and time domain through a SMA connector.

Figure 4-13. Die photograph and testing PC board of IF generator.

Figure 4-14 shows the spectrum and waveform of all seven IF signals. The violation of 50% duty cycle in the waveform manifests itself as a growth in the second order harmonic in the spectrum. In the simulation, only IF signals at 2GHz and 2.4GHz violate 50% duty cycle, which is acceptable because harmonics fall out of TX bands. However, the measured results reveal that IF signals at 800MHz and 1.2GHz also do not have 50% duty cycle in addition to the IF signals at 2GHz and 2.4GHz.
Figure 4-14. Spectrum and waveform of IF signals at (a) 400MHz, (b) 800MHz, (c) 1.2GHz, (d) 1.5GHz, (e) 2.0GHz, (f) 2.4GHz, and (g) 3.0GHz.
Figure 4-14. Continued

Figure 4-15 shows interferer generation including the effects of unexpected 2nd order harmonics of IF signals at 800MHz and a 1.2GHz. In particular, the 2nd order harmonic of 800MHz signal at 1.6GHz mixed with 24GHz generates an interferer at 25.6GHz that is only 100MHz away from the RF frequency of motor 4 at 25.5GHz. In addition, the 2nd order harmonic of 1.2GHz at 2.4GHz mixed with 24GHz generates an interferer at 26.4GHz which is
the RF frequency of motor 6. Table 4-3 summarizes the simulated and measured duty cycles of IF signals. The problems of non 50% duty cycle of IF signals at 800MHz and 1.2GHz result from the fact that output waveforms of divide-by-1.5 and a divide-by-2.5 that have originally 40% and 33% duty cycle respectively are not often fully restored to the 50% duty cycle by a subsequent single divide-by-2 circuit. Since the amount of duty cycle violations in the output waveforms are small, adding a simple duty correction circuit after a divide-by-2 is suggested to fix these problems.

Figure 4-15. Generation of undesired interferers due to the mixing of 2nd, 3rd, and 5th order harmonics of IF signals with LO signal.

Table 4-3. Simulated and measured duty cycle of IF signals

<table>
<thead>
<tr>
<th>IF number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF Frequency (GHz)</td>
<td>0.4</td>
<td>0.8</td>
<td>1.2</td>
<td>1.5</td>
<td>2.0</td>
<td>2.4</td>
<td>3.0</td>
</tr>
<tr>
<td>Simulated Duty Cycle (%)</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>33.3</td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>Measured Duty Cycle (%)</td>
<td>53.2</td>
<td>59.4</td>
<td>60.8</td>
<td>50.2</td>
<td>27.1</td>
<td>45.3</td>
<td>49.4</td>
</tr>
</tbody>
</table>
4.5 Measurement Results of TX Chain

The TRX at motor side has been fabricated in the UMC 130-nm logic CMOS. Shown in Figure 4-16 is a die photograph of a transceiver. All the circuits and components are fully integrated. The chip area without the bond pads and 4mm on-chip dipole antenna occupies 1.54mm×2.22mm. The transmitter has been measured on a PCB with the chip directly mounted on the board (chip-on-board). To characterize the clock recovery and LO generation at the proposed CDR circuit followed by mixing, modulation, and amplification at the TX chain, the output spectrum and waveform of ASK modulated signal at the duplexer output are measured while applying 400Mbps PRBS $2^{31}-1$ signal to the limiter input in the back end of RX. For this measurement, the antenna was cut off.

![Figure 4-16. Die photograph of crystalless transceiver at motor section.](image)

4.5.1 Spectrum of TX Output and Harmonic Control

The block diagram of TX at motor side and measurement setup are shown in Figure 4-17. An antenna was cut off to eliminate the additional measurement loss and mismatch. The power is
monitored at the duplexer output. This is because only the antenna side has no bond wire the probe landing is possible only in this direction. Measured power at the duplexer output is around 7dB lower than that of power amplifier output due to the high duplexer loss [8] in the frequency band from 24.2GHz to 27.2GHz. Table 4-4 summarizes TX power level at the duplexer output for the 7 motor channels. In the table, power\(^1\) specifies TX output power after de-embedding the cable and balun losses. Measured TX power ranges from the minimum of -4.6dBm to maximum of 2.3dBm, which are close to the target power of 0dBm. Spectrum of TX output with an external IF source are presented in Appendix B.

Figure 4-17. Block diagram of transmitter at motor side.

Table 4-4. Summary of TX output power level at motor side

<table>
<thead>
<tr>
<th>Motor</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel (GHz)</td>
<td>24.4</td>
<td>24.8</td>
<td>25.2</td>
<td>25.5</td>
<td>26.0</td>
<td>26.4</td>
<td>27.0</td>
</tr>
<tr>
<td>Power (dBm)</td>
<td>-10.6</td>
<td>-8.6</td>
<td>-4.6</td>
<td>-8.4</td>
<td>-4.0</td>
<td>-6.8</td>
<td>-4.84</td>
</tr>
<tr>
<td>Cable &amp; balun loss (dB)</td>
<td>6.0</td>
<td>6.4</td>
<td>5.9</td>
<td>6.4</td>
<td>6.3</td>
<td>6.8</td>
<td>7.1</td>
</tr>
<tr>
<td>Power(^1) (dBm)</td>
<td>-4.6</td>
<td>-2.2</td>
<td>1.3</td>
<td>-2.0</td>
<td>2.3</td>
<td>0</td>
<td>2.3</td>
</tr>
</tbody>
</table>

*Power\(^1\): output power after de-embedding the cable and the balun loss.
Figure 4-18. Spectrum of TX motor 1 with attenuator.

Figure 4-19. Spectrum of TX motor 1 without attenuator.

Figure 4-18 shows the output spectrum of TX for motor 1 at the duplexer output with harmonic control using an attenuator. The peak power level at 24.4GHz is -4.6dBm (-10.6dBm before de-embedding the balun and cable losses). Since the 3rd and the 5th order harmonics of IF
signal at 400MHz fall into the motor 3 (25.2GHz) and 5 (26GHz), the harmonic control is imperative to limit this problem.

The 3rd and 5th harmonics of 400MHz mixing with 24GHz turn out to be -28.5dBm at 25.2GHz and -42.7dBm at 26GHz, respectively. The power difference between the undesired interferer at 25.2GHz and the desired signal of motor 3 at 25.2GHz is 30dB (=1.3dBm-(-28.5dBm)), which should be sufficiently large enough to ignore the contribution of the interferer. For comparison, the spectrum of TX motor 1 at the duplexer output without attenuator is shown in Figure 4-19. In this case, the power difference between the undesired interferer at 25.2GHz and the desired signal at 25.2GHz is only 9.8dB (=1.3dBm-(-8.5dBm)), which is not negligible. For the 5th order harmonic of 400MHz, the power difference between the undesired interferer at 26.0GHz and the desired signal at 26.0GHz is 45dB (=2.3dBm-(-42.7dBm)), which should be sufficiently large. The power difference without an attenuator is 14.2dB (=2.3dBm-(-11.9dBm)). Figure 4-20 shows a zoomed-in spectrum at the TX motor1 with span of 100MHz.

Figure 4-20. Zoomed-in spectrum of TX motor 1.
Figure 4-21. Spectrum of TX motor 2 with attenuator.

Figure 4-22. Spectrum of TX motor 2 without an attenuator.

Figure 4-21 and 4-22 show the output spectrum of TX for motor 2 at the duplexer output with an attenuator and without an attenuator, respectively. The unexpected 2\textsuperscript{nd} harmonic of the IF signal at 800MHz falls into the 25.6GHz which is only 100MHz away from the RF frequency for motor 4. The power difference between the undesired interferer at 25.6GHz and the desired
signal at 25.5GHz is 15.6dB (=-2dBm-(-17.6dBm)) for the case with an attenuator, and 9.3dB (=-2dBm-(-11.3dBm)) for the case without an attenuator. The power differences in both cases are not large, which may cause desired signal at motor 4 to experience distortion. The 3rd order harmonic of IF signal at 800MHz falls into the motor 6 (26.4GHz). The power difference between the undesired interferer at 26.4GHz and the desired sinal at 26.4GHz is 26.5dB (=0dBm(-26.5dBm)) for the case with an attenuator. Without an attenuator, the power difference is only 8.2dB (=0dBm(-8.2dBm)), which should not be acceptable.

The output spectrums of TX for motor 3 at the duplexer output with an attenuator and without an attenuator are shown in Figures 4-23 and 4-24, respectively. Similar to the motor 2 case, the unexpected 2nd order harmonic of the IF signal at 1.2GHz mixed with the LO at 24GHz falls into the 26.4GHz which is the RF frequency of motor 6. The power difference between the undesired interferer at 26.4GHz and the desired signal in the channel for motor 6 is 19.4dB (=0dBm(-19.4dBm)) for the case with an attenuator. The power difference is only 9.4dB (=0dBm(-9.4dBm)) for the case without an attenuator, which may not be large enough. Figure 4-25 summarizes the impact of interferer signals on desired channels for the case with attenuator.

![Figure 4-23. Spectrum of TX motor 3 with attenuator.](image-url)
Figure 4-24. Spectrum of TX motor 3 without attenuator.

Figure 4-25. The impact of interferer signals on desired channels with attenuator on.

4.5.2 ASK Modulation (Carrier at 26GHz Amplitude-modulated by 25MHz Modulating Square Signal)

A transmitter that radiates an un-modulated carrier power will send out half of the power when it is ASK modulated by a data with 100% transition. For instance, a 26-GHz transmitter that radiates 1mW of un-modulated carrier power will radiate only 0.5mW of power when it is ASK modulated by the 01010101 data pattern. Furthermore, of 0.5mW, 0.25mW will be in the carrier lobe and the other 0.25mW will be divided among the side lobes. Therefore, the carrier of
ASK modulated signal has 6dB lower power than un-modulated carrier power as shown in Figure 4-26.

![Figure 4-26. Waveform and spectrum of (a) un-modulated carrier and (b) ASK modulated carrier.](image)

As shown in Figure 4-27, when a square signal with 50% duty cycle is used as an amplitude modulating signal, the power difference between the carrier lobe and the 1st side lobe of ASK modulated signal is 4dB. Thus, the 1st side lobe of ASK modulated signal has 10dB lower power than un-modulated carrier power.

![Figure 4-27. Waveform and spectrum of square wave with 50% duty cycle.](image)

To characterize the ASK modulation of the TX output, one of the seven TX channels, especially motor 5 (26.0GHz), is selected due to its highest output power. Since a 25MHz
square signal with a 50% duty cycle corresponds to a 50Mbps data with 100% transition density. A 25MHz square clock is applied for amplitude modulation.

Figure 4-28 shows the spectrum of TX output for motor 5 before and after the ASK modulation with a 25MHz square wave. Once ASK modulated by on-off keying the signal path in the Power amplifier, the overall TX power level decreases by ~6dB from -7dBm to -12.65dBm, This is consistent with the illustration in Figure 4-26. In addition, after modulation, the power difference between the carrier lobe at 26GHz and the 1st side lobe at 25.975GHz or 26.025GHz is 4dB, which means the modulation index is 100%. This can be easily verified by looking at the waveform in Figure 4-29. The modulation index appears to be indeed 100%.

Figure 4-28. Spectrum of TX output at motor 5 (26GHz) before and after ASK modulation with 25-MHz square signal.
Figure 4-29. Waveform of TX output at motor 5 after ASK modulation with 25-MHz square signal.

4.5.3 ASK Modulation (Carrier at 26GHz Amplitude-modulated by 50Mbps PRBS $2^{31}-1$ Modulating Signal)

Figure 4-30 shows the spectrum of TX output at motor 5 before and after the ASK modulation with 50Mbps PRBS $2^{31}-1$ data signal. Since the modulating signal is a PRBS data rather than a clock signal, a spectrum after the modulation shows nulls at the integer multiples of 50MHz from the carrier frequency at 26GHz, which is the typical property for a PRBS signal. A common way of visualizing long sequences of random data waveform is an eye diagram, which displays an accumulation of edges and levels of data by folding all of the bits into a short interval, e.g., typically two or three bits wide. Figure 4-31 shows a waveform of TX output at motor 5 after ASK modulation with 50Mbps PRBS $2^{31}-1$ data signal. Accumulation of all of the bits into a short interval creates this waveform in which each data bits are filled with the carrier signal 26GHz. Vertical bit boundaries are colored in darker tone.
Figure 4-30. Spectrum of TX output at motor 5 before and after the ASK modulation with 50Mbps PRBS $2^{31}-1$ data signal.

Figure 4-31. Eye diagram output at motor 5 after ASK modulation with a 50Mbps PRBS $2^{31}-1$ data signal.
4.5.4 Wireless Link Test at the Motor TX

The feasibility of establishing a wireless link at the TX motor within the controller board is demonstrated. A metallic cover is placed ~3.5cm above the controller board to emulate the operation environment, which increases the received signal power [61]. As shown in Figure 4-32, a 4mm on-chip dipole antenna separated by 5cm from the TX picks up the 26-GHz carrier signal amplitude modulated by 25-MHz square signal. The CDR was driven with 400-Mbps PRBS $2^{31}-1$ signal.

![Setup of wireless link demonstration at TX motor side.](image)

Figure 4-32. Setup of wireless link demonstration at TX motor side.

Figure 4-33(a) shows an output spectrum of un-modulated 26GHz carrier signal (CDR output at 24GHz mixed with IF at 2GHz (24GHz/2/3/2)) at the duplexer output without modulation. Figure 4-33(b) shows the spectrum of TX carrier signal at 26GHz modulated by 25-MHz square signal. The ~4-dB amplitude difference between the carrier and the first harmonics
at 26GHz +/- 25MHz in Figure 4-33(b) indicates the AM modulation index of 100%. This is also consistent with the time domain waveform in Figure 4-33(c) where the peak to peak voltage level is ~320mV and off level is ~10mV. Since the noise level should be less than the off level, SNR should be greater than 30dB. Incidentally, the signal power of -11.4dBm (-17.7dBm + cable/balun loss of 6.3dB at 26GHz) for the 1st side lobe at 26.025GHz in Figure 4-33(b) is ~10dB lower than the un-modulated carrier signal power of -2.15dBm in Figure 4-33(a).

![Figure 4-33. Spectrum of TX output (a) before modulation (b) after ASK modulation with 25-MHz square clock signal. (c) Waveform of TX output after ASK modulation with 25MHz square clock signal. (d) Spectrum of received 26-GHz carrier signal amplitude modulated by 25-MHz square signal (with metallic cover).]

With the measured TX signal power at the duplexer output of -11.4dBm (-17.7dBm + cable/balun loss of 6.3dB at 26GHz) at 26.025GHz, the measured signal power at 5 cm separation shown in Figure 4-33 (d) is -56.4dBm (-62.68dBm + cable/balun loss of 6.3dB at 26GHz) or -53.4dBm (2 ASK sidebands). For the case of 15cm separation, received power is expected to be ~-64.7dBm. This is ~10 dB higher than the sensitivity target for BER of $10^{-13}$. This margin can be utilized to accommodate the variations of propagation loss and implementation...
loss of receiver. Table 4-5 summarizes the TX power consumption. The measurement results suggest that a transmitter integrated with a receiver incorporating a CDR can bypass the problem of providing external frequency reference, which is a fundamental technique needed for a two-way wireless inter-chip data communication for return path isolation applications.

Table 4-5. Power consumption of transmitter at motor side

<table>
<thead>
<tr>
<th>TX blocks</th>
<th>CDR</th>
<th>MIX</th>
<th>PA</th>
<th>IF generator</th>
<th>LO buffer</th>
<th>MUX &amp; DIV2 &amp; DIV2 buffer</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (mW)</td>
<td>18.3</td>
<td>17.6</td>
<td>91.2</td>
<td>25.8</td>
<td>22.7</td>
<td>16.3</td>
<td>191.9</td>
</tr>
</tbody>
</table>

4.6 Conclusion

The integrated circuit implementation of the FDMA transmitter at the motor section is presented in Chapter 4. The original transmitter architecture has been simplified by the new CDR architecture that merges the PLL function into the VCO of CDR, thereby reducing the circuit complexity, chip area and power consumption. Individual TX blocks such as an IF generator, an 8-to-1 multiplexer, 3-stage LO buffers, an up-conversion mixer, and a power amplifier are described in both circuit and system levels.

The measured duty cycles of IF signals at 800MHz and 1.2GHz are off from 50%. This generates unexpected interfering signals at the other channels. Un-modulated TX carrier powers at the duplexer output are measured for all 7 motor channels. The output Power ranges from the minimum of -4.6dBm to maximum of 2.3dBm. The output powers for motor 3, 5, 6, and 7 satisfy the target power of 0dBm. Finally, the feasibility of establishing a wireless link using the transmitter is demonstrated. A 4mm on-chip dipole antenna separated by 5cm from the TX successfully picks up the 26GHz carrier signal amplitude modulated by a 25MHz square signal. The total TX power consumption is ~192mW where PA dissipates 48% of the total TX power consumption.
CHAPTER 5
DUPLEX OPERATION AND LINK DEMONSTRATION

5.1 Introduction

A link between the TX at a deadtime controller and RX at a motor side is demonstrated in Chapter 5. To fulfill the link demonstration, ensuring the satisfactory performance in both TX and RX is the first priority. Furthermore, at a motor side, the feasibility of a full-duplex capability of TRX with an on-chip antenna should be verified to make sure the TX operations do not significantly degrade or, in worst case, disrupt RX performance.

A block-level schematic of RX chain at motor side is illustrated in Figure 5-1. The differential LNA output is changed to a single-ended signal using an active current-mirror balun, which is followed by multiple filter stages and amplification stages along the RF signal path. The schottky barrier diode (SBD) is connected in shunt as a half-wave rectifier for signal detection [14]. The down-converted signal is then filtered using a 2nd order 1.2-GHz wide Chebychev low-pass filter. The filter is followed by a 3-stage differential baseband amplifier and a buffer for driving 50Ω.

![Block diagram of receiver chain at motor section.](image)

Figure 5-1. Block diagram of receiver chain at motor section.
In the 1st version of chip, only the RX was integrated. A PC board for the RX measurement was designed and fabricated to characterize the RX chain. Later, however, when both RX and TX at motor side are integrated in the same chip, the increased number of bond pads resulted in longer bond wire between chip and PCB pads. In addition, increased PCB size resulted in longer FR4 traces on the PCB, that increased the parasitic inductance. These can cause stability problems.

A main cause of oscillation in the presence of parasitic inductance comes from a single-ended multistage baseband amplifier within the original RX chain. Two examples of instability due to parasitic inductance are illustrated in Figure 5-2.

Figure 5-2. Positive feedback path due to parasitic inductors in multistage single-ended amplifiers.

In Figure 5-2(a), transient current thorough a parasitic inductor $L_{\text{par}}$ due to bond wires and FR4 traces develops voltage at node P. This voltage feeds back to node Q through R1, possibly driving the following common-source stages into oscillation. A positive feedback path is shown using a dotted line. In Figure 5-2(b), a positive-feedback path drawn using a dotted line is created due to the ground bond wire, $L_{\text{par}}$. By contrast, for differential amplifier, voltage developed at node Q and P in Figure 5-2 (a) appears as a common-mode disturbance. The ground inductance

93
in Figure 5-2(b) does not affect the primary positive feedback path in the differential structure [19].

In Chapter 5, a newly designed baseband amplifier is first introduced and the measurement results of the amplifier by itself are presented. The performance of entire RX chain at motor side including the new baseband amplifier is characterized. Furthermore, a full-duplex operation of TRX at motor side is verified. Finally, a wire-line link between the TX at deadtime controller and the RX at motor side is demonstrated.

5.2 A Differential Baseband Amplifier

5.2.1 Circuit Description

The original baseband amplifier suffered from the oscillation problem under the nominal \( V_{DD} \) and bias condition. Because of this, the original RX was characterized at non-optimum \( V_{DD} \) and bias conditions, which degraded gain, and compromised all RX measurement. Therefore, the baseband amplifier has been modified from a single-ended to a differential structure which is less vulnerable to the oscillation problem. However, the differential amplifier also poses the following design challenges.

An ideal single to differential conversion at the first stage is supposed to generate balanced differential outputs, showing identical gain and 180° phase difference between the two differential outputs. In practical circuits, however, this cannot be achieved. For instance, a bias current source with finite output impedance and the parasitic capacitor at common-source node results in imbalance. In addition, the AC gate to drain voltage of the input ports are different because one is grounded.

Increasing the output impedance of a current source using cascoded transistors reduces the imbalance. Additional cascaded fully differential stages following the single to differential conversion at the first stage suppress the magnitude and phase error further. Simulations indicate
both errors become less than 1% by the time single-ended input signal reaches the differential outputs of final stage.

Another concern of the baseband design is DC offset problem due to the mismatch of differential pair and load resistors. Inserting AC coupling capacitors between stages could prevent the DC offset problem. However, choosing a huge capacitor to avoid “DC wander” in high pass configuration for AC coupling always accompanies the parasitic capacitor, which reduces the bandwidth of a baseband amplifier below the requirement. Since a baseband amplifier needs to process 400-Mbps data stream (same as 200MHz for 100% transition), accounting for the 3rd order harmonic of 200MHz, the overall bandwidth of amplifier should be at least 600MHz. Thus the bandwidth of each stage must be at least ~1.4GHz according to Equation (4-1).

Figure 5-3 shows the schematic of a single to differential baseband amplifier. The transistor sizes of a differential pair in each stages are chosen to be as big as possible in order to limit the mismatch induced DC offset while satisfying bandwidth requirement. An earlier stage is
sensitive to the DC offset problem than later stages because signal amplitude increases as signal propagates through the stages. Thus, progressive sizing is employed such that the transistor width of differential pair is 40µm, 30µm, and 20µm for the 1st, the 2nd, and the 3rd stage, respectively. To reduce mismatch, a common centroid layout is adopted for the differential pair and silicide blocked P⁺ poly resistors in each stage. The last stage is a buffer stage that drives the 50-Ω input impedance of equipment, limiter and ADC.

Figure 5-4. Schematic of the wide-swing cascode current mirror.

As shown in Figure 5-4, a wide-swing cascode current mirror provides gate bias voltages for current sources in the baseband amplifier. The idea of this circuit is to bias the drain to source voltages of transistor M8 on the edge of the triode region by setting the gate voltage of M7 at 2V_{DSAT}+V_{TH} such that the cascoded transistors M7 and M8 drop only 2V_{DSAT}, while operating in the saturation region. In practical short-channel designs, since the output resistance of a MOSTFET heavily depends on the drain to source voltage, it is imperative to bias M8 deeper into the saturation region by using a larger gate voltage in M7 in order to increase the output.
resistance of cascoded current sources. To raise the gate voltage of M7, and thus increase the drain voltage of M8, the length of M5 is chosen to be 18 times larger than that of M7 instead of 4~5 times in long-channel designs. The bias circuit generates 100µA of current flow through the mirror transistor M5. The first three stages of baseband amplifier mirrors 5 times of this current when \( V_{DD} \) is 1.5V. The buffer stage draws 20mA at \( V_{DD} \) of 1.5~1.8V. Additionally, \( V_{cont} \) is included for adjusting the current, thus the overall voltage gain of baseband amplifier.

5.2.2 Measurement Results

The standalone test structure of baseband amplifier has been fabricated in the UMC 130-nm CMOS technology. A die photograph and a testing PC board are shown in Figure 5-5. The baseband amplifier has been measured on a PCB with the chip directly mounted on the board (chip-on-board). Input and output are terminated with SMA connectors, and 50Ω. Thus, the voltage gain and power gain are the same.

![Die photograph and baseband amplifier PC board for testing.](image)

Figure 5-5. Die photograph and baseband amplifier PC board for testing.

Figure 5-6 shows the waveforms of square inputs at 200MHz with different amplitudes and corresponding differential outputs. Under the nominal \( V_{DD} \) and bias condition, the output
waveforms confirm that the circuit does not suffer from the oscillation problem and generates balanced differential outputs, also indicating the gain and phase difference between the differential outputs are negligible. When the input voltage level is above ~10mV_pp, the measured duty cycle difference between differential outputs exhibits less than 1% error from 50%, which implies nearly 180°-phase difference between the differential outputs is achieved. As the input level increases, the balance improves.

The voltage gain of baseband amplifier is 34dB when the input voltages of 6.8-mV_pp in Figure 5-6 (a) and 20-mV_pp in Figure 5-6(b) are applied. For larger input voltage of 30-mV_pp in Figure 5-6(c), measured gain is reduced to 32dB. Thus, IP1dB of baseband amplifier occurs at the input power level somewhere between 20mV_pp (-30dBm) and 30mV_pp (-26.5dBm). By changing V_cont, the voltage gain can be varied by at least +/- 3dB from 34dB.

The measured worst case rise/fall time (10% to 90%) shown in Figure 5-6(b) is 573ps, which is 11.5% of a data period of 5ns. The rise time of 573ps can be used to estimate the signal bandwidth [69].

$$\text{freq}_{-3\text{dB}} = \frac{0.35}{\text{rise time}}$$  \hspace{1cm} (5-1)

From Equation (5-1), the estimated signal bandwidth is equal to 611MHz, which is close to bandwidth design target of 600MHz. The measured frequency response in Figure 5-7 shows that the 3-dB bandwidth is 670MHz. The V_DD of bias circuit and first 3stages of baseband amplifier are 1.5V. The circuit draws 2.2mA. The buffer stage has a separate V_DD of 1.8V and consumes 22mA. The total power consumption is 43mW. Table 5-1 summarizes the measurement results.
Figure 5-6. Waveform of a single-ended square wave input at 200MHz. Differential outputs when input voltage level is (a) 6.8mV<sub>pp</sub>, (b) 20mV<sub>pp</sub> and (c) 30mV<sub>pp</sub>.
Figure 5-7. Measured 3-dB bandwidth of baseband amplifier in frequency domain.

Table 5-1. Summary of measurement results of baseband amplifier

<table>
<thead>
<tr>
<th>Single-ended input power (dBm)</th>
<th>-33.3</th>
<th>-30</th>
<th>-26.5</th>
<th>-24.9</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-ended input voltage (mV_{pp})</td>
<td>6.8</td>
<td>20</td>
<td>30</td>
<td>36</td>
</tr>
<tr>
<td>Single-ended output voltage (mV_{pp})</td>
<td>170</td>
<td>550</td>
<td>580</td>
<td>610</td>
</tr>
<tr>
<td>1. Rise/fall time (ps)</td>
<td>581/560</td>
<td>566/552</td>
<td>552/543</td>
<td>491/479</td>
</tr>
<tr>
<td>2. Rise/fall time (ps)</td>
<td>602/427</td>
<td>573/463</td>
<td>553/493</td>
<td>484/445</td>
</tr>
<tr>
<td>1. Duty cycle (%)</td>
<td>52.2</td>
<td>50.2</td>
<td>50.3</td>
<td>50.4</td>
</tr>
<tr>
<td>2. Duty cycle (%)</td>
<td>49.3</td>
<td>49.2</td>
<td>49.4</td>
<td>49.7</td>
</tr>
<tr>
<td>Single to differential Voltage Gain (dB)</td>
<td>34</td>
<td>34</td>
<td>32</td>
<td>30.6</td>
</tr>
<tr>
<td>3-dB bandwidth (MHz)</td>
<td>670</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP_{1dB} (dBm)</td>
<td>Somewhere between -30 ~ -26.5</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power dissipation</th>
<th>Bias circuit &amp; first 3 stages</th>
<th>Last buffer stage</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3.3mW (1.5V / 2.2mA)</td>
<td>39.6mW (1.8V / 22mA)</td>
<td>43mW</td>
</tr>
</tbody>
</table>

*1 and 2 indicate each waveform of differential output signals.

5.3 Measurement Results of Full RX Chain for Motor Section

The entire RX chain including an updated baseband amplifier at motor side is characterized with a 2-level amplitude modulated signal. Without the oscillation problem under
the nominal $V_{DD}$ and bias condition, RX successfully demodulated the baseband data at 400Mbps from an incoming ASK signal in which the carrier frequency at 16.8GHz is amplitude modulated by PRBS $2^{31}-1$ signal. Furthermore, the CDR locked to the incoming 2 level data at 400Mbps, and generated the clock and LO signals at 400MHz and 24GHz.

In Figure 5-8, a block diagram of RX chain at motor side and measurement setup are illustrated. An antenna and a duplexer are laser-cut. The amplitude modulated RF signal is externally generated using a commercial double side band (DSB) passive mixer. Mixing an LO signal at 16.8GHz and an IF signal at 200MHz square signal or 400Mbps PRBS signal produces a double-sideband large-carrier (DSB-LC) AM signal. Since the designed RX architecture utilizes square-law detection (non-coherent rectifier), to avoid signal distortion, the amplitude modulated signal should contain carrier signal with DSB, ensuring the modulation index is always less than 100%. The RF signal from the mixer output is connected to a balun through the cable, followed by a GSSG probe landing on the bond pads at the input of LNA.

![Block diagram of RX chain at motor section and measurement setup](image_url)

Figure 5-8. Block diagram of RX chain at motor section and measurement setup.
The output power, $P_{out}$ versus the input power, $P_{in}$ of RX chain is plotted in Figure 5-9 by applying ASK signals with varying power level to the LNA input while maintaining 100% modulation index. The carrier frequency is 16.8-GHz and amplitude modulating signal is 200-MHz single tone sine wave. In this plot, the power gain of the amplifier is given by the ratio of the output power to the input power. The carrier power does not directly contribute to the output power after demodulation because it does not contain any modulation information. Thus, the practical power gain should be computed by subtracting the input side band power from the output power rather than the input carrier power in a dB scale. The 1 dB compression point, $IP_{1dB}$, occurs at input sideband power of $\sim$45dBm. The slope of plots indicates a 2-decade output power increase for an 1-decade input power increase because of the square-law detection.

![Figure 5-9. RX output power as function of input single sideband power and input carrier power (AM modulation index of 100%).](image)

The BER of RX chain is measured to figure out the sensitivity of RX chain. The BER measurement setup is described in section 5.4.1 (Figure 5-13). As shown in Figure 5-10, the
measured sensitivity of RX chain for BER of $10^{-12}$ and 400-Mbps data rate is $\sim$-45dBm. The high sensitivity of RX chain is due to the low gain of RF section in the RX chain. Compared to the design target of RF section gain of $\sim$40dB for sensitivity of less than $\sim$60dBm, measured gain of RF section is $\sim$15dB [14], which results in the significant degradation of RX sensitivity. In order to achieve BER of $10^{-12}$ at even lower sensitivity, RF section should be updated to meet the design target of $\sim$40dB gain.

Figure 5-10. Measured BER versus input power

The performance of an entire RX chain was characterized by applying ASK signal to the LNA input and monitoring the spectrum and waveform at the end of receiver chain. The carrier frequency is 16.8-GHz and amplitude modulating signal is 200-MHz square wave signal. The RMS jitters of recovered clock are also characterized. In the case of the 1st input sideband power of -45dBm in Figure 5-11(a), demodulated signal output power at BB out is -6.5dBm at 200MHz in Figure 5-11(b). Waveforms of demodulated data and recovered clock are shown in Figure 5-11(c). The peak-peak voltage of data is 400mV. A rising edge of a recovered clock at 400MHz in
CDR samples close to center of demodulated data bits. The jitter histogram of recovered clock at 400MHz shows RMS jitter of 1.78ps in Figure 5-11(d).

![Figure 5-11](image-url)

Figure 5-11. Plots of (a) Amplitude modulated 16.8-GHz carrier with 200-MHz square wave at LNA input. (b) Spectrum of demodulated 200MHz signal at BB output. (c) Waveforms of demodulated 200MHz signal at BB output and 400MHz recovered clock at CDR output. (d) Jitter histogram of recovered clock at 400MHz.

For the following RX chain measurement results, 400-Mbps PRBS \(2^{31}-1\) is used to amplitude modulate 16.8-GHz carrier. Total input power level is kept same as the previous case. This ASK modulated signal is applied at the LNA input, and output spectrum and waveform are monitored. Furthermore, a CDR locks to the 400-Mbps data stream from the BB out, and recovers clock and LO signal at 400MHz and 24GHz. Figure 5-12 shows (a) the spectrum of ASK modulated signal at LNA input, (b) the spectrum of output demodulated signal at BB out,
(c) the waveform of demodulated data and recovered clock at CDR output, and (d) jitter histogram of recovered clock.

The jitter performance of recovered clock at 400MHz is measured in the cases of 400Mbps PRBS $2^{31}-1$, $2^{23}-1$, and $2^7-1$. The RMS jitters are 2.5ps, 2.5ps, and 2.2ps, respectively. For the first version of RX chip with the oscillation issues, the measured RMS jitters of recovered clock for 400Mbps PRBS $2^{31}-1$, $2^{23}-1$, and $2^7-1$ were 29ps, 28.5ps, and 10.3ps, respectively. Thus, a significant jitter reduction is achieved in the updated RX chain to provide TX with more stable and purer LO signal. Table 5-2 summarizes the RX measurement results. The total RX power consumption is 53mW.

![Graphs and plots](image)

Figure 5-12. Plots of (a) Amplitude modulated 16.8-GHz carrier with 400-Mbps PRBS $2^{31}-1$ at LNA input. (b) Spectrum of demodulated 400Mbps signal at BB output. (c) Waveforms of demodulated 400Mbps signal at BB output and 400MHz recovered clock at CDR output. (d) Jitter histogram of recovered clock at 400MHz.
<table>
<thead>
<tr>
<th>Input Power (dBm)</th>
<th>Carrier: -48</th>
<th>Carrier: -44</th>
<th>Carrier: -39</th>
</tr>
</thead>
<tbody>
<tr>
<td>*modulation index less than 100%</td>
<td>1st sideband: -54</td>
<td>1st sideband: -50</td>
<td>1st sideband: -45</td>
</tr>
<tr>
<td>Output power (dBm) @200MHz</td>
<td>-22.7</td>
<td>-14.7</td>
<td>-6.5</td>
</tr>
<tr>
<td>Output Voltage (mV&lt;sub&gt;pp&lt;/sub&gt;)</td>
<td>~60</td>
<td>~120</td>
<td>~240</td>
</tr>
<tr>
<td>RX Power Gain in terms of 1st sideband input power (dB)</td>
<td>31</td>
<td>35.3</td>
<td>38.5</td>
</tr>
<tr>
<td>IP&lt;sub&gt;1dB&lt;/sub&gt;</td>
<td>-45dBm</td>
<td>-45dBm</td>
<td>-45dBm</td>
</tr>
<tr>
<td>Sensitivity for BER of 10&lt;sup&gt;-12&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power dissipation</td>
<td>RF section 49.5mW (1.5V/33mA)</td>
<td>SBD ~0.1mW (0.6V/0.13mA)</td>
<td>BB amp (w/o buffer) 3.3mW (1.5V/2.2mA)</td>
</tr>
<tr>
<td>RMS Jitter of clock at 400MHz (ps)</td>
<td>with PRBS 2&lt;sup&gt;31&lt;/sup&gt;-1 4.70</td>
<td>3.13</td>
<td>2.51</td>
</tr>
<tr>
<td></td>
<td>with PRBS 2&lt;sup&gt;23&lt;/sup&gt;-1 4.59</td>
<td>3.06</td>
<td>2.48</td>
</tr>
<tr>
<td></td>
<td>with RRBS 2&lt;sup&gt;7&lt;/sup&gt;-1 4.46</td>
<td>2.65</td>
<td>2.20</td>
</tr>
<tr>
<td></td>
<td>with clock input @ 200MHz 2.90</td>
<td>1.98</td>
<td>1.78</td>
</tr>
</tbody>
</table>

5.4 Duplex Operation of TRX at Motor Side

On-chip antennas in low-cost silicon IC technologies have been verified for use in communication within a chip as well as a beacon (antenna and an oscillator) [10], [70]-[72]. A 20GHz down-converter with an on-chip antenna [11] and a 24GHz transmitter with an on-chip antenna [12] have been reported. However, there have been no reports of duplex communication using CMOS transceivers with on-chip antennas. For a two-way wireless inter-chip data communication for return path isolation application, a full-duplex capability allows for a communication in both directions simultaneously using RX bands from 15.6~18GHz and TX bands from 24.2~27.2GHz. This sub-section 5.4 mainly verifies the impacts of concurrent TX operation on the performance of RX by investigating the degradation of RX BER and RMS jitters of recovered clock.
5.4.1 Characterization of RX with TX On and Off

A successful duplex operation of TRX requires sufficient reduction of the leakage signal or noise from TX to RX. The impact of signal/noise coupled from TX on the RX through the substrate, V_{DD}, GND and bond-wires is investigated by comparing the BER performance of RX and RMS jitter of recovered clock from the CDR when TX is “on” and “off”.

![Figure 5-13. Block diagram of TRX at motor section and measurement setup.](image)

Figure 5-13. Block diagram of TRX at motor section and measurement setup.

Shown in Figure 5-13 is a measurement setup where a duplexer is laser cut off from the LNA input to inject input signal while avoiding the 50Ω mismatch loss. Similar to the measurement setup in Figure 5-8, the input ASK signal is externally generated and up converted using a commercial DSB passive mixer. Mixing LO signal at 16.8GHz and 200-MHz square wave or 400-Mbps PRBS IF signal produces DSB LC AM signal. For BER measurements, a pattern generator function of BERT is used to transmit the PRBS modulating signals to the external mixer which generates the ASK signal. On the RX side, an analyzer of BERT compares the demodulated baseband signals from the output of receiver chain with the transmitted signals.
from the generator. The recovered clock from CDR is used as clock signals in the analyzer where clock signals are synched to the received signals.

In the transmitter, a carrier signal is selected from 24.4GHz to 27GHz based on the choice of IF signal. The carrier is on-off keyed by a simple switch circuit in the PA. Since a PRBS pattern resembles the actual modulating signal format used in the system, a 50-Mbps PRBS signal rather than a clock signal should be applied to the switch input as amplitude modulating signal.

Figure 5-14. Spectrum of demodulated baseband signal in RX when (a) TX is off, (b) TX is on and a modulating signal for TX is a 50-MHz clock, and (c) TX is on and a modulating signal for TX is a 50-Mbps PRBS $2^7$-1 signal. The plots on the right side are the zoomed-in plots.
It is observed that demodulated baseband signals depend on the type of TX modulating signal, i.e., clock or PRBS signal. Figure 5-14 shows the spectrum when ASK signal (carrier frequency at 16.8GHz is amplitude modulated by a 200-MHz square clock with the 1st sideband RF input signal of ~-45dBm) is applied to LNA input.

Compared to the case when TX is off in Figure 5-14(a), the spectrum of baseband signal with TX on reveals a bunch of undesired spurs coupled from the TX side. If the harmonic power levels are comparable to or exceed the desired baseband signal at 200MHz, CDR fails to lock. On the other hand, when TX modulating signal is 50-Mbps PRBS signal, the spectrum of baseband signal is affected much less by the harmonic contents associated with TX as shown in Figure 5-14(c). This is because the spectrum of PRBS signal is flattened due to spreading.

So far, the demodulated baseband signal at RX is assumed to be a 200-MHz square wave. However, since the real baseband signal is 400-Mbps data stream similar to the PRBS signal, the 50-Mbps PRBS signal from TX must affect the 400-Mbps demodulated RX PRBS signal differently because spectra of their signals overlap even though the coupled TX PRBS signal is relatively smaller than the RX PRBS signal.

In order to quantify these, the RX chain was first characterized by applying ASK signal to the LNA input and monitoring the RMS jitter of recovered clock in CDR with TX turned on. In order to characterize the jitter performance in terms of different RF input power, the 1st sideband power of the ASK signal (an LO at 16.8GHz modulated by an IF at 200MHz square signal) is varied from -45dBm (IP_{1dB} point) to -58dBm (CDR locking sensitivity), below which the CDR fails to lock. The measured RMS jitter versus the RF input sideband power is summarized in Table 5-3. The 200-MHz square clock and 400-Mbps PRBS signals are used as the modulating signal of RF input. The results show that as RF input power decreases, RMS jitters increase.
However, it is noted that the RMS jitter of recovered clock at each RF input power increases by no more than ~1ps when TX is turned on. Figure 5-15 shows the plots of RMS jitters summarized in Table 5-3.

Table 5-3. Summary of measured jitter performance

<table>
<thead>
<tr>
<th>Modulating Signal</th>
<th>RMS Jitter (ps) TX off</th>
<th>RMS Jitter (ps) TX on</th>
<th>RMS Jitter (ps) TX off</th>
<th>RMS Jitter (ps) TX on</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF input 1\textsuperscript{st} side band power (dBm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200MHz clock</td>
<td>8.43</td>
<td>9.38</td>
<td>2.90</td>
<td>3.60</td>
</tr>
<tr>
<td>400Mbps PRBS 2\textsuperscript{23}-1</td>
<td>9.36</td>
<td>10.43</td>
<td>4.46</td>
<td>5.54</td>
</tr>
<tr>
<td>400Mbps PRBS 2\textsuperscript{23}-1</td>
<td>9.58</td>
<td>10.53</td>
<td>4.59</td>
<td>5.64</td>
</tr>
<tr>
<td>400Mbps PRBS 2\textsuperscript{31}-1</td>
<td>9.76</td>
<td>10.64</td>
<td>4.70</td>
<td>5.96</td>
</tr>
</tbody>
</table>

Figure 5-15. RMS jitter plots of recovered clock with and without turning on TX for (a) 200MHz square clock, (b) 400-Mbps PRBS 2\textsuperscript{23}-1, (c) 400-Mbps PRBS 2\textsuperscript{23}-1, and (d) 400Mbps PRBS 2\textsuperscript{31}-1 modulating signal for RF input.
Secondly, the BER performance of RX chain versus RF input powers are compared to further investigate the impact of simultaneous operation of TX and RX.

Table 5-4. Summary of measured BER performance of RX chain at motor side

<table>
<thead>
<tr>
<th>RF Input 1ˢᵗ side band power (dBm)</th>
<th>PRBS 2⁷-1</th>
<th></th>
<th>PRBS 2³¹-1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TX off</td>
<td>TX on</td>
<td>TX off</td>
<td>TX on</td>
</tr>
<tr>
<td>-44</td>
<td>Less than 1.0×10⁻¹²</td>
<td>Less than 1.0×10⁻¹²</td>
<td>2.3×10⁻¹²</td>
<td>5.8×10⁻¹²</td>
</tr>
<tr>
<td>-45</td>
<td>2.2×10⁻¹²</td>
<td>5.3×10⁻¹²</td>
<td>6.3×10⁻¹¹</td>
<td>5.4×10⁻¹⁰</td>
</tr>
<tr>
<td>-46</td>
<td>3.3×10⁻⁷</td>
<td>7.1×10⁻⁶</td>
<td>1.3×10⁻⁶</td>
<td>8.4×10⁻⁶</td>
</tr>
<tr>
<td>-48</td>
<td>6.7×10⁻⁵</td>
<td>4.7×10⁻⁴</td>
<td>1.1×10⁻⁴</td>
<td>4.1×10⁻⁴</td>
</tr>
<tr>
<td>-50</td>
<td>1.1×10⁻²</td>
<td>1.9×10⁻²</td>
<td>2.5×10⁻²</td>
<td>4.3×10⁻²</td>
</tr>
</tbody>
</table>

Figure 5-16. BER plots (a) 400-Mbps PRBS 2⁷-1 modulation signal for RF input with TX on and off, (b) 400-Mbps PRBS 2³¹-1 with TX on and off, (c) TX on with 400-Mbps PRBS 2⁷-1 and 2³¹-1 modulation signal, and (d) TX off with 400-Mbps PRBS 2⁷-1 and 2³¹-1.
As shown in Table 5-4, the measurements indicate that BER is lower when smaller PRBS length is used such as PRBS $2^7-1$. BER is less than $10^{-12}$ if the RF input power is larger than -44dBm regardless of the PRBS length. When RF input power is less than -45dBm, BER degrades rapidly. At each RF input power level, running TX along with RX indeed degrades BER performance. However, the extent of degradation due to the TX is less than a factor of 10. Especially, when input power is greater than -45dBm, the difference is small. In addition, the degradation of BER is more strongly dependent on the RX input powers than having the TX on or off. This suggests that the degradation is related to the low gain problem of receiver. If the gain is increased, the impact of having TX on should be reduced at even low RX input levels. Figure 5-16 shows BER plots based on the measured data in Table 5-4.

5.4.2 Characterization of RX with TX On and Off using the Chip without Laser Cut

So far, the impact of TX operation to RX performance has been investigated using chips with the connection between duplexer and LNA input laser cut. However, a concern of this setup is that the impact of coupling or leakage of TX signal/noise via the duplexer and the on-chip antenna to the LNA side is not fully captured because of the laser cut. To investigate the effects of this, circuits without the laser cut are characterized. The new measurement setup is exactly same as Figure 5-13 except the laser cut. When a probe lands on the chip pads at the LNA input to apply the RF signal, higher power should be applied to compensate for the mismatch loss resulting from the probe load. By observing the output signal power at the baseband output, the RF input power can be estimated using the $P_{\text{in}}$ versus $P_{\text{out}}$ plot in Figure 5-9.

The RMS jitter of recovered clock and the BER performance of RX chain are measured using RF input 1st side band power of -47dBm. RMS jitter and BER with TX on are measured and compared to the cases with TX off, and summarized in Table 5-5. In addition, the new measured data are overlaid in the RMS jitter plots and BER plots in Figure 5-17 and 5-18,
respectively. The measurements indicate the impact of coupling or leakage of TX signal/noise via the duplexer and the on-chip antenna to the LNA side is negligible. These indicate that full duplex operation using on-chip antennas are possible.

Table 5-5. Summary of measured RMS jitter and BER performance

<table>
<thead>
<tr>
<th>Modulating Signal</th>
<th>200MHz square clock</th>
<th>400Mbps PRBS 2(^7)-1</th>
<th>400Mbps PRBS 2(^{23})-1</th>
<th>400Mbps PRBS 2(^{31})-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMS Jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TX off</td>
<td>1.86ps</td>
<td>2.37ps</td>
<td>2.44ps</td>
<td>2.46ps</td>
</tr>
<tr>
<td>TX on</td>
<td>2.45ps</td>
<td>2.78ps</td>
<td>2.80ps</td>
<td>2.96ps</td>
</tr>
</tbody>
</table>

BER performance with TX on and off

<table>
<thead>
<tr>
<th>RF input 1(^{st}) side band power of -47dBm</th>
<th>PRBS 2(^7)-1</th>
<th>PRBS 2(^{23})-1</th>
<th>PRBS 2(^{31})-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX off</td>
<td>2.5\times10^{-7}</td>
<td>6.8\times10^{-6}</td>
<td>3.2\times10^{-6}</td>
</tr>
<tr>
<td>TX on</td>
<td>9.5\times10^{-6}</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 5-17. RMS jitter plots at RF input power of -47dBm with TX on and off for (a) 200MHz square clock, (b) 400Mbps PRBS 2\(^7\)-1, (c) 400Mbps PRBS 2\(^{23}\)-1, and (d) 400Mbps PRBS 2\(^{31}\)-1. The connection between the LNA and duplexer is not laser cut.
5.4.3 Wireless Demonstration of Duplex Operation at Motor Side

A full-duplex operation of TRX at motor side is observed by picking up signals from both TX and RX bands at the same time as shown in Figure 5-19.

A 4-mm on-chip dipole antenna separated by 5-cm from the TRX radiates the 16.8-GHz carrier signal amplitude modulated by 400-Mbps PRBS signal. The radiated ASK modulated
signals are picked up by the RX on the other side via a 4-mm on-chip dipole antenna and by an external horn antenna placed ~7cm above the surface. The received ASK signal in RX is rectified and fed to CDR. Internally generated TX LO signal at 24GHz from CDR mixed with IF signal at 1.5GHz generates a carrier signal at 25.5GHz that is amplified and amplitude modulated by a modulating signal, i.e. 50Mbps PRBS signal, in PA. Finally, the ASK modulated TX signal is fed to a duplexer and radiated via the on-chip dipole antenna. Figure 5-20 shows the captured spectrum in both RX band (15.6~18GHz) and one of TX channels (25.35~25.7GHz).

![Figure 5-20. Spectrum of both RX and TX band at motor side](image)

5.5 Detection of Multiple Level ASK Signal

For the wireless communication in the hybrid engine controller board, the RX must detect multi-level ASK signals. To evaluate this, multi-level AM signal is generated using a stand alone coder and PA [62] combination for the TX of the deadtime controller side. A carrier signal at 16.8-GHz is amplitude modulated by 400-Mbps multi-level signal from the output of coder generates AM signals with seven different levels. Block diagrams of RX and the PA at TX along with the measurement setup is shown in Figure 5-21. A single-ended PA output at TX is
connected to differential LNA input in RX through a GS probe landed on the PA output, an RF
cable followed by a variable attenuator emulating propagation loss, a balun converting single to
differential signal and a GSSG probe landed on differential LNA inputs. The antenna and
duplexer are laser-cut off to avoid the mismatch loss. Unlike wireless channels that are random
and difficult to analyze, the wired interconnection in this setup provides stationary and
predictable channel behaviors.

![Diagram](attachment:image.png)

Figure 5-21. Measurement set up for link demonstration and block diagrams of TX and RX

Demodulated multi-level data signal at the baseband output is followed by a limiter in
which each level of incoming data is compared with a threshold voltage set to the middle
between level 6 and level 0. If the incoming level is bigger than the threshold voltage, signal is
railed up to $V_{DD}$ otherwise signal is railed down to GND. Thus, a CDR following the limiter
recovers clocks by processing 2-level input signal. This allows use of conventional CDR
architecture. It is important to mention that 2-level signals converted from multi-level signals
should not change the minimum data bit period of 2.5ns. For example, if a varying amplitude level such as 012456 repeats itself at a data rate of 400-Mbps, then it becomes 000666 after the limiter and the repetition of this pattern changes original data rate at 400Mbps to one third of 400Mbps, which results in a failure of CDR locking to 400Mbps input signal.

An initial measurement setup uses 39dB attenuation (GS probe/cable loss of 3dB, 35dB attenuator, balun/GSSG probe loss of 1dB) between the TX and RX. In case of wireless link, given a pair of antenna loss of 16dB and a duplexer loss of 3dB for TX and RX side, the remaining 17-dB corresponds to a channel loss in free space. This 17dB is equivalent to ~1-cm separation at 16.8GHz. Shown in Figures 5-22 and 5-23 are a carrier signal at 16.8GHz amplitude modulated by an alternating pattern between level 0 and level 6 similar to the 2-level modulating pattern and a 01506250 input pattern, respectively. Each data bit period is 2.5ns. Measured waveforms of demodulated signals at BB out are also shown. For the 39dB attenuation setup, the amplitude of the baseband signal is ~220mV which should fit the ADC input requirement of 300mV. However, it is difficult to clearly distinguish each level.

![Figure 5-22](image)

Figure 5-22. Waveform of (a) amplitude modulated signal by a 400Mbps pattern 060606 at TX output, (b) demodulated signal at BB out, and recovered clock at CDR output with total 39dB attenuation between the PA output and LNA input.
Figure 5-23. Waveform of (a) amplitude modulated signal by a 400Mbps pattern 01506250 at TX output, (b) demodulated signal at BB out, and recovered clock at CDR output with total 39dB attenuation between the PA output and LNA input.

The 2nd measurement setup uses 20dB attenuation between the TX and RX. As shown in Figure 5-24, a carrier signal at 16.8GHz amplitude modulated by an alternating pattern between level 0 and level 6 is captured in time domain. Each data bit period is equal to 2.5ns. The measured waveform of demodulated signal at BB out and 400MHz recovered clock at CDR output are also shown. A rising edge of recovered clock samples the data near the center.

Figure 5-24. Waveform of (a) amplitude modulated signal by a 400-Mbps 060606 pattern at TX output, (b) demodulated signal at BB out, and recovered clock at CDR output with total 20dB attenuation between the PA output and LNA input.
Figure 5-25. Waveform of (a) amplitude modulated signal by a 400-Mbps 01506250 pattern at TX output, (b) demodulated signal at BB out, and recovered clock at CDR output with total 20dB attenuation between the PA output and LNA input.

In Figure 5-25(a), waveform of signal is generated using 400Mbps 01506250 pattern. The carrier frequency is 16.8GHz. The waveform of demodulated signal at BB output and 400-MHz recovered clock at CDR output are shown in Figure 5-25(b). The output waveform of demodulated signal follows the negative envelope of amplitude modulated signal, which is consistent with the detector design.

Figure 5-26. Waveform of demodulated signal (varying amplitude levels 01506250) at BB output when the data rate of modulating signal is (a) 200Mbps and (b) 100Mbps with total 20dB attenuation between the PA output and LNA input.
In comparison to the waveform of baseband signals from the 1st measurement setup using 39dB attenuation, bigger baseband signal (~500mV_{pp}) results in more recognizable levels. However, the signal amplitude already exceeds the acceptable ADC input range. Thus, in order to accommodate large baseband signals, the ADC should be modified.

When the data rate of modulating signal is lower than 400Mbps, demodulated waveform shows clearer distinction between levels. Figure 5-26 shows the waveforms of demodulated signal at 200Mbps and 100Mbps. The results suggest that increasing the bandwidth of baseband amplifier in RX to include up to 5th order harmonics of 200MHz signal improves the signal quality.

An amplitude modulated signal that includes the combination of all 7 levels is chosen and the corresponding baseband output is measured. The varying amplitude levels such as 024135246 cause the malfunction of the comparator of limiter when level-3 is compared. The level-3 located at the center between level 0 and 6 is exactly identical to the threshold voltage that is set at the middle between level 0 and 6. Therefore, level 3 cannot be resolved. This failure results in a long drift of rising edge and disturbing the decision of comparator in the subsequent bit. This eventually increases the jitter of recovered clock and in the worst case CDR fails to lock or generate clock at wrong frequency. As a temporary solution, the threshold voltage could be externally adjusted to create difference between the threshold and level-3. However, this solution is no longer useful when detected baseband signal level is small. If the overall signal level is smaller, the amplitude difference between levels become smaller so that the comparator easily falls into the meta-stable state because setting the threshold voltage slightly above or below the center makes the threshold to be close to another level. In other words, the limiter cannot operate.
without generating unacceptably high jitters of recovered clock or CDR locking to wrong data rate when incoming signal consists of a series of middle levels.

Figure 5-27. Waveform of (a) amplitude modulated signal by a 400-Mbps 0241353246 pattern at TX output, (b) demodulated signal at BB output, and recovered clock at CDR output with total 20dB attenuation between the PA output and LNA input.

Figure 5-27 shows the modulated signal with a 400-Mbps 0241353246 pattern, and demodulated signal at BB output and corresponding recovered clock at 400MHz. Figure 5-28 shows the waveform of demodulated signal at 200Mbps and 100Mbps. When the data rate of modulating signal is at 100Mbps, demodulated waveform shows clear distinction of levels and sharper rising/falling time during level transitions. In Figure 5-29, measured RMS jitter of recovered clock is as high as 47.6ps, which is due to the frequent occurrence of middle levels such as level 3 and 4 in the input pattern. In this case, even though multi-level signals are detected at 400Mbps in the baseband output, CDR generates a recovered clock at 399.4MHz instead of 400MHz because of the malfunction of limiter stage.

In order to avoid the meta-stability problem in the limiter and hence the failure of clock recovery in the CDR, the middle levels of multi-level signals at TX should be readjusted before signal transmission. In the PA at deadtime controller, level 3 and 4 should be set as far away as
possible from the middle point between level 6 and level 0 such that, in the RX at motor side, the
comparator of limiter has greater margin between the threshold voltage and level 3 or 4.

Figure 5-28. Waveform of demodulated signal (varying amplitude levels 0241353246) at BB
output when the data rate of modulating signal is (a) 200Mbps and (b) 100Mbps with
total 20dB attenuation between the PA output and LNA input

Figure 5-29. Jitter histogram of (a) demodulated signal at BB out and (b) recovered clock at
CDR output for a modulating signal at 400Mbps with total 20dB attenuation between
the PA output and LNA input.

5.6 Conclusions

The single-ended baseband amplifier from the previous implementation is updated to a
differential structure to eliminate the oscillation problem of RX chain. The measurements of
stand alone test structure indicate that under the normal $V_{DD}$ and bias condition, the oscillation problem has been eliminated. The gain of amplifier is 34dB. The 3dB bandwidth is 670MHz that satisfies the design target of 600MHz. The amplifier including the bias circuit consumes 3.3mW of power.

The entire RX chain including an updated baseband amplifier at motor side is characterized with 2-level amplitude modulated signals. RX chain has $IP_{1db}$ of -45dBm and sensitivity of -45dBm for BER of $10^{-12}$ and 400Mbps data rate. Full-duplex operations of TRX with an on-chip antenna are verified by comparing the BER performance of RX chain and RMS jitters of recovered clock for the cases with TX on and off. The BER degradation due to the TX on is less than a factor of 10. Especially, when the output signal is near the design target, the difference is almost negligible. The jitters of recovered clock increase by no more than ~1ps when TX is on. In addition, the full-duplex operation of TRX at motor side is observed by picking up signals from both TX and RX bands at the same time using an external horn antenna. This work has demonstrated that full-duplex operation of CMOS transceivers with an on-chip antenna is possible.

Finally, the feasibility of the detecting multi-level CDMA signal is demonstrated using 7-level AM signals. Due to the major malfunction in the limiter with middle data levels, i.e. level 3 and 4, the jitter of recovered clock increases to ~48ps from ~2ps. In addition, the CDR recovers the clock at wrong frequency, and in the worst case, loses lock. Some possible solutions to this problem are suggested.
CHAPTER 6
SUMMARY AND FUTURE WORK

6.1 Summary

A fully integrated CDR based LO generation circuit which provides both 24-GHz LO signal for a TX and 400-MHz clock for a RX has been demonstrated in UMC 130-nm CMOS process. A VCO operation 60 times higher than the input data rate at 400Mbps by using a divider in the feedback loop enables generation of 24-GHz LO signal for TX and integration of an LC-VCO that utilizes an inductor with reasonable size and Q. Including the divider in the feedback loop provides additional degree of freedom for reducing the size of loop filter capacitors for integration. The jitter performance of recovered clock at 400MHz is the lowest among fully integrated CDR’s with the similar data rate (~400Mbps) published in the literature.

A fully integrated FDMA TX chain for motor side in the hybrid engine controller board is demonstrated using the UMC-130nm CMOS technology. The increased phase noise of LO generated by a CDR does not degrade the performance of ASK systems using a square laws detector in the receiver. It should also be possible to use a recovered clock from a CDR as an LO for a wide band width systems with other low order modulation schemes. The feasibility of establishing a wireless link using the transmitter within the controller board is also demonstrated. This indicates that a TX integrated with a RX incorporating a CDR can bypass the problem of having an external frequency reference. A wireless link demonstration on the board suggests the target communication range of 15cm should be possible.

An entire RX chain including an updated single to differential baseband amplifier is characterized. More importantly, full-duplex operations of TRX for motor side with an on-chip antenna are demonstrated for the first time. Finally, the feasibility of detecting multiple level AM signal is also demonstrated.
6.2 Future Work

The following efforts that extend the work predicted in this dissertation should be considered for future efforts.

(a) For successful link demonstration between TX at deadtime controller and RX at motor side, the RF gain of RX front end at motor side should be increased to improve its sensitivity. The RX chain should be demonstrated with a 3-bit 800-Msample/s ADC. The middle levels such as level 3 and 4 of multi-level signals at TX should be readjusted before transmission so as to avoid the meta-stability problem in the limiter that can cause the failure of clock recovery, and increase jitter. In the PA at the deadtime controller side, level 3 and 4 should be positioned to be away from the middle point between level 6 and level 0 so that, in the RX for the motor side, the comparator of limiter can have large amplitude margins between the threshold voltage and level 3 or 4. A wireless link that supports multiple amplitude modulation should be demonstrated.

(c) Once the RX chain at deadtime controller is verified, a wireless link between TX at motor side and RX at deadtime controller side should be demonstrated.

(b) In the IF generator, waveforms of IF signals at 800MHz and 1.2GHz violate 50% duty cycle. For this reason, the increased 2\textsuperscript{nd} harmonics of these IF signals mixed with LO signal create interfering signals that fall into the desired neighboring channels. Approaches to reduce the deviation should be incorporated.
A block diagram of a CDR test structure which consists of a phase detector, a charge pump, a loop filter, a 5.84-GHz LC VCO, and a divide-by-16 block is shown in Figure A-1. This CDR test structure outputs both 365-MHz clock and 5.84-GHz LO signal. A loop filter can be fully integrated with a reasonable capacitance value. Since this CDR test structure was a prototype design, more than the necessary digital control bits (up to 7 bits) are incorporated in the VCO to increase the likelihood of satisfying the frequency target.

A.1 Circuit Description of CDR Test Structure

Much of the circuit topology is the same as the CDR circuit mentioned in section 3.2. The loop bandwidth of 500kHz, charge pump current of 70µA, divide ratio of 16 and VCO gain of 300MHz/V are chosen. For the loop filter, two capacitors $C_Z$, $C_P$, and one resistor $R_Z$ are 324pF, 31pF and 3.1kΩ respectively. The biggest capacitor $C_Z$ occupies 200µm×210µm. The simulated phase margin of CDR loop is 55°.
Figure A-2. Schematic of the 5.84GHz LC VCO.

Figure A-2 shows a circuit schematic of the 5.84GHz LC VCO, which consists of an LC-tank, a PMOS cross coupled pair, a pair of accumulation mode varactors for continuous fine tuning, a digitally tuned capacitor bank for discrete coarse tuning, an NMOS tail current source, and a pair of inductively loaded buffers. The capacitor bank supports 7-bit digital tuning to keep the VCO gain low for reduced phase noise while maintaining an adequate tuning range. To increase the inductor Q, L1 is drawn as a center tapped spiral inductor [40] using the top two copper layers shunted together. The total metal thickness is ~1.6µm. The estimated series
resistance of inductor is 2.3 Ω. The metal spacing, width, and number of turns are 2.9µm, 4.8µm, and 3, respectively. The inductance for L1 is 0.9nH, and the inductor including a polysilicon pattern ground shield [41], [42] occupies 100µm×100µm. The simulated Q [43] of inductor is ~15 at 5.84GHz. The capacitor bank consists of seven parallel binary-scaled MOS varactors whose control voltages are connected to either $V_{DD}$ for $C_{\text{min}}$ or GND for $C_{\text{max}}$. The $C_{\text{max}}/C_{\text{min}}$ is around 3. To implement a divide-by-16, four divide-by-2 circuits are cascaded in series.

### A.2 Measurement Results of CDR Test Structure

The CDR has been fabricated in the UMC 130-nm logic CMOS technology with eight copper layers. Shown in Figure A-3 is a die photograph. The chip area without the bond pads is 0.88mm×0.67mm. This includes the area for a pair of inductor loaded buffers (0.11mm×0.11mm) for the VCO measurements. The CDR has been measured on a PC board with the chip directly mounted on the board (chip-on-board) illustrated in Figure A-4. The size of PCB is 4.8cm by 4.8cm. Direct probe landing is performed to measure the LO at 5.84GHz. The recovered clock at 385MHz and the retimed data are both measured via SMA connectors. The measured CDR locking range is from 360.4 to 369Mpbs. Figure A-5 shows the VCO tuning range and corresponding VCO gain change for digital tuning bit 0000000. The measured VCO gain is ~300MHz/V which is the same as the design target of 300MHz/V around the control voltage of 0.4V. However, the gain decreases as the control voltage deviates from this point due to the saturation of varactor capacitance. The supply voltage is 1.2V. The VCO draws 12mA. The power consumption of CDR excluding that of buffers for driving an external load is ~16mW.
Figure A-3. Die photograph of 5.84GHz CDR.

Figure A-4. Photograph of CDR testing printed circuit board.
Figure A-5. Plot of VCO tuning range and gain at digital bits 0000000.

Figure A-6 shows the measured waveform of recovered clock at 365MHz and jitter histogram in response to a PRBS $2^{31}-1$ input, respectively. The measured RMS and peak to peak jitters are 8.9ps (rms) and 76.9ps (p-p), respectively, which are 0.32% and 2.8% of a clock period. The BER performance has been measured using an Agilent N4903 J-BERT. Since a BER measurement must be statistically valid, a CDR should be tested long enough to have a certain confidence level in its BER results [73]. BER testing time must be at least 23 hour 37 min if the desired BER is $10^{-13}$, and desired confidence level is 95% when input data rate is 356-Mbps. During BER measurements, $3.154 \times 10^{13}$ bits were checked for 24 hours. The measured BER is less than $10^{-13}$.

Figure A-7 shows the spectrum of the recovered clock at 5.84GHz with 365-Mbps PRBS $2^{31}-1$ input signal when the CDR is locked. Since the CDR loop bandwidth is designed to be 500-kHz, the noise shaping within the loop bandwidth can be observed in the spectrum. The phase noise performance at the offset frequency of 60kHz, 1MHz, and 10MHz are measured with RBS
$2^7$-1, $2^{23}$-1, $2^{31}$-1 and clock input at 182.5-MHz. Figure A-8 shows the phase noise plot for PRBS $2^{31}$-1. The in-band phase noise at 60-kHz offset is -74.5dBc/Hz. The phase noise at 1-MHz offset is -94.1dBc/Hz and the out-of-band phase noise at 10-MHz offset is -113.0dBc/Hz. The measured CDR characteristics are summarized in Table A-1. This work has demonstrated the LO generation circuit can be incorporated with a clock and data recovery circuit.

Figure A-6. Plot of recovered clock at 365MHz and jitter histogram for a PRBS $2^{31}$-1.

Figure A-7. Spectrum of recovered clock at 5.84GHz for a PRBS $2^{31}$-1 input signal.
Figure A-8. Plot of phase noise of recovered clock at 5.84GHz for a PRBS $2^{31}-1$ input signal.

Table A-1. Summary of measured CDR performance

<table>
<thead>
<tr>
<th>Technology</th>
<th>UMC 130-nm 365-Mbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input data rate</td>
<td>360.4-Mbps ~ 369-Mbps</td>
</tr>
<tr>
<td>CDR lock range</td>
<td>5.7-GHz ~ 7.12-GHz</td>
</tr>
<tr>
<td>VCO tuning range</td>
<td></td>
</tr>
<tr>
<td>5.84-GHz clock</td>
<td>PRBS $2^7$-1, PRBS $2^{23}$-1, PRBS $2^{31}$-1</td>
</tr>
<tr>
<td>Phase noise (dBc/Hz)</td>
<td></td>
</tr>
<tr>
<td>@ 60-KHz offset</td>
<td>-74.6, -73.0, -74.5</td>
</tr>
<tr>
<td>@ 1-MHz offset</td>
<td>-100.6, -93.3, -94.1</td>
</tr>
<tr>
<td>@ 10-MHz offset</td>
<td>-118.3, -113.1, -113.0</td>
</tr>
<tr>
<td>365-MHz clock jitter (ps)</td>
<td>RMS rising, Peak to Peak</td>
</tr>
<tr>
<td>with PRBS $2^7$-1</td>
<td>6.1, 45.8</td>
</tr>
<tr>
<td>with PRBS $2^{23}$-1</td>
<td>8.8, 66.7</td>
</tr>
<tr>
<td>with PRBS $2^{31}$-1</td>
<td>8.9, 76.9</td>
</tr>
<tr>
<td>with clock input @182.5MHz</td>
<td>4.3, 41.1</td>
</tr>
<tr>
<td>BER with 95% confidence for PRBS $2^{31}$-1</td>
<td>Less than $10^{-13}$</td>
</tr>
<tr>
<td>Chip size (w/o pad)</td>
<td>0.88×0.67 mm$^2$</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>PD 0.5, CP 0.25, VCO 14.4, DIV(simulation) 1.2</td>
</tr>
</tbody>
</table>
APPENDIX B
SPECTRUM OF TX OUTPUT WITH AN EXTERNAL IF SIGNAL SOURCE

Figure B-1 shows the measurement setup with an external IF frequency source. The antenna was cut off to eliminate the additional measurement loss and mismatch. The TX power is measured at the duplexer output. Since the sinusoidal IF signals produced by an external signal generator is squared with 50% duty cycle after a few inverter stages, when the IF signal is mixed with LO signal, the contribution of even order harmonics within the TX band is negligible and hence only odd harmonics are taken into consideration.

Table B-1. Summary of TX output power level at motor side with an external IF signal source

<table>
<thead>
<tr>
<th>Motor</th>
<th>Channel (GHz)</th>
<th>Power (dBm)</th>
<th>Cable &amp; balun loss (dB)</th>
<th>Power¹ (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>24.4</td>
<td>24.8</td>
<td>25.2</td>
<td>25.5</td>
</tr>
<tr>
<td></td>
<td>-8.5</td>
<td>-8.9</td>
<td>-5.4</td>
<td>-6.6</td>
</tr>
<tr>
<td></td>
<td>6.0</td>
<td>6.4</td>
<td>5.9</td>
<td>6.4</td>
</tr>
<tr>
<td></td>
<td>-2.5</td>
<td>-2.5</td>
<td>0.5</td>
<td>-0.2</td>
</tr>
</tbody>
</table>

*Power¹: output power after de-embedding measurement cable and balun loss.

With an external IF signal source, the generation of undesired interferers from motor and their influence on the neighboring channels well agree with the diagram in Figure 4-11. Table B-1 summarizes the TX output power levels for seven motor channels. In this table, power¹ specifies TX output power after de-embedding the cable and balun losses.
A spectrum of TX motor 1 at the duplexer output with antenna cut off is shown Figure B-2. The peak power level at 24.4GHz is -2.5dBm (-8.53dBm before de-embedding the balun and cable losses). Since the 3rd and 5th order harmonics of 400MHz signals fall into motor 3 (25.2GHz) and motor 5 (26GHz) channels, harmonic control is once again important for reducing the interference. The 3rd and 5th harmonics from 400MHz are ~-20dBm at 25.2GHz and ~-32dBm at 26GHz, respectively. Proper attenuator settings can further minimize the harmonic contribution, though this will reduce the desired output power level. Figure B-3 shows a zoomed in spectrum of the TX motor 1.

Figure B-2. Spectrum of TX motor 1 driven with an external IF signal source.

Figure B-3. Zoomed-in spectrum of TX motor 1 driven with an external IF signal source.
Figure B-4 shows a spectrum of motor 7 at the duplexer output. The peak power level at 27GHz is 1.5dBm (-5.6dBm before de-embedding the balun and cable losses). The 2nd order harmonic from 3GHz mixed with 24GHz is -31dBm at 30GHz, which is outside of the TX bands. Figure B-5 shows a zoomed in spectrum of the TX motor 7.

Figure B-4. Spectrum of TX motor 7 driven with an external IF signal source.

Figure B-5. Zoomed-in spectrum of TX motor 7 driven with an external IF signal source.
LIST OF REFERENCES


BIOGRAPHICAL SKETCH

Kyujin Oh was born in Busan, South Korea, in 1974. He received the B.S. degree in electrical engineering from Yonsei University, Seoul, South Korea in 2001 and M.S. degree in electrical engineering from University of Southern California, Los Angeles in 2004. Currently, he is a Ph.D. candidate in the Department of Electrical and Computer Engineering at the University of Florida, Gainesville and has been with the Silicon Microwave Integrated Circuits and Systems (SIMICS) research group since 2006.

During the summer of 2007, he interned at Samsung Electronics where he was involved in VCO and divider design of a phase locked loop (PLL) for 4G wireless communication (LTE). His current research interests are in analysis and design of RF circuits, wireless transceiver, and high-speed analog circuits in CMOS.