SIGNAL PROCESSING TECHNIQUES AND DSP HARDWARE STRUCTURES FOR
DYNAMIC ESTIMATION AND COMPENSATION OF ABSOLUTE AND RELATIVE
GAIN/PHASE VARIATIONS IN MOBILE DEVICES

By

PRAVINKUMAR PREMAKANTHAN

A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2010
Quest for knowledge, the learning, and the humility that accompanies it
ACKNOWLEDGMENTS

I am immensely grateful to my research advisor and mentor Dr. John Harris for his encouragement and support during my PhD research. I feel extremely fortunate to work under his guidance over the past 6 years. I would like to extend my sincere thanks to my committee members Dr. Fred Taylor, Dr. Janise McNair and Dr. Oscar Crisalle. I greatly appreciate their generosity in devoting their time to serve on my research committee. I am equally grateful to my managers Dr. Mahib Rahman, and Dr. Bing Xu and Vivek Bhan for their encouragement towards my research effort. I would like to thank my wife for her selfless support and understanding. Greatest thanks to my parents for providing the path towards the quest for knowledge. Finally, I am grateful to Ms. Shannon Chillingworth for her advice and support during this research effort.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>ACKNOWLEDGMENTS</th>
<th>page</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIST OF TABLES</td>
<td>8</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>9</td>
</tr>
<tr>
<td>LIST OF ABBREVIATIONS</td>
<td>15</td>
</tr>
<tr>
<td>ABSTRACT</td>
<td>16</td>
</tr>
</tbody>
</table>

## CHAPTER

### 1 INTRODUCTION

1.1 Motivation: Need for Power Control and Gain Tracking Inside Mobile Device ....... 18
1.2 Power Control Techniques in Mobile Devices .................................................. 22
1.3 Present Day Techniques and Prior Art ........................................................... 23

#### 1.3.1 Use of Fixed Calibrated Digital Gain Offset and Error Values ............. 23
#### 1.3.2 Use of Pre-Calibrated Analog Bias Signal for Constant Envelope Modulation .............................................................................. 24
#### 1.3.3 Use of RF Feedback and Analog Bias Control ........................................ 24
#### 1.3.4 Use of RF Feedback and Temperature Compensation Circuit Based Gain Control ................................................................. 25
1.4 Limitations of Prior Art .................................................................................. 25
1.5 Research Effort Comparisons ......................................................................... 26
1.6 Organization of Thesis .................................................................................... 26

### 2 DIGITAL DSP TECHNIQUES AND EFFICIENT HARDWARE TOPOLOGIES FOR ABSOLUTE GAIN TRACKING

2.1 Problem Statement ............................................................................................ 37
2.2 Reasons for Signal Gain Variations in Mobile Devices ..................................... 38

#### 2.2.1 Gain variations due to Manufacturing Processes .................................... 38
#### 2.2.2 Power Gain Variations due to Change in Junction Temperature .......... 39
#### 2.2.3 Change in Power Gain Due to Different Operating Paths Depending on Power Level .............................................................................. 39

#### 2.2.4 Variation in Gain Due to Different Operating Frequencies and Supply Voltage .............................................................................................. 40
2.3 DSP Based Dynamic Gain Tracking Algorithm (DSP-DGT) ................................ 40

#### 2.3.1 System Architecture of the DSP-DGT Algorithm ..................................... 40
#### 2.3.2 Feedback Path ........................................................................................ 41
#### 2.3.3 Forward Reference Path .......................................................................... 42
2.4 Algorithm Theory ............................................................................................ 42
2.5 DSP Hardware Structures for the DSP-DGT Algorithm ..................................... 47
2.5.1 Digital Calibration Signal Pattern Generator ................................................. 47
2.5.2 Digital Sample Rate Adjust Logic ............................................................... 47
2.5.3 Magnitude Estimator .................................................................................. 48
2.5.4 Fast Exponential Averager ........................................................................ 51
2.5.5 Digital PID controller ................................................................................ 53
2.5.6 Cross-Correlator Hardware ....................................................................... 54
   2.5.6.1 Simulations with the cross-correlation DSP hardware ...................... 56
   2.5.6.2 Correlation estimates at varying sample rates ..................................... 58
2.6 Top Level System Simulations and Measured Lab Results ............................. 59
   2.6.1 System Simulations ................................................................................ 59
   2.6.2 Mobile Testing and Lab Measurements .................................................... 61
2.7 Summary ............................................................................................................ 62

3 DSP BASED DYNAMIC ESTIMATION AND COMPENSATION OF
DIFFERENTIAL GAIN NONLINEARITY AND RANDOM PHASE SHIFTS .......... 100

   3.1 Demands for Relative Gain and Phase Accuracy in Mobile Devices .......... 100
   3.2 Analytical Expressions for Non Linear Distortions in an Analog RF Device .. 101
   3.3 Reasons for Relative Power Level Accuracy Impairment ......................... 105
   3.4 Reasons for Phase Discontinuity ................................................................... 107
   3.5 DSP based Relative Gain/Phase Estimation Algorithm Theory (DSP-GPE). 108
      3.5.1 Theory of Operation ............................................................................ 108
      3.5.2 Gain and Phase Estimation Steps ....................................................... 112
      3.5.3 Gain and Phase Compensation Implementation and Equations .......... 113
      3.5.4 Derivation of Equations for Gain and Phase Estimation and
                     Compensation .................................................................................... 114
   3.6 DSP Hardware Structures for Relative Gain/Phase Estimation and
                     Compensation .......................................................................................... 116
      3.6.1 Phase Compensation DSP Structure .................................................. 116
      3.6.2 DFT Based Gain Estimation Structure ................................................. 116
   3.7 System Simulations and Lab Measurement Results ..................................... 119
      3.7.1 System Simulations of the DSP-GPE Algorithm ................................. 121
      3.7.2 Lab Measurement Results .................................................................. 121
   3.8 Summary ........................................................................................................... 123

4 DYNAMIC GAIN/POWER CONTROL USING ADAPTIVE DSP TECHNIQUES ... 143

   4.1 Introduction ..................................................................................................... 143
   4.2 System Architecture for the DSP-GC Algorithm ......................................... 144
   4.3 Loop Tuning Techniques ................................................................................ 150
      4.3.1 Method I - Reference Model Based Loop Tuning ............................... 150
      4.3.2 Method II- Open Loop Tuning Based On Unknown Plant Transfer
                     Function ............................................................................................... 152
      4.3.3 Method III - Loop Tuning Based on Closed-loop Cycling .................... 152
      4.3.4 Method IV - Implemented Loop Tuning Technique Based on
                     Closed-loop Stability Constraint ...................................................... 154
   4.4 Closed-loop Delay and Loop Gain Margin Analysis ..................................... 157
<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Comparison of New Techniques</td>
<td>35</td>
</tr>
<tr>
<td>2-1</td>
<td>Estimation of best $\alpha$ and $\beta$ factors for magnitude estimation</td>
<td>96</td>
</tr>
<tr>
<td>2-2</td>
<td>Signal gain implementation</td>
<td>97</td>
</tr>
<tr>
<td>2-3</td>
<td>Multiplexor selection logic for the 12 tap cross-correlator</td>
<td>98</td>
</tr>
<tr>
<td>3-1</td>
<td>Approximate THD requirements for a few applications</td>
<td>137</td>
</tr>
<tr>
<td>3-2</td>
<td>DNLE and INLE Definition</td>
<td>138</td>
</tr>
<tr>
<td>3-3</td>
<td>Measured High Frequency Amplifier gain across temperature and frequency</td>
<td>139</td>
</tr>
<tr>
<td></td>
<td>bands of operation</td>
<td></td>
</tr>
<tr>
<td>3-4</td>
<td>Measured DNLE with mid channel as the reference for a 16 stage gain</td>
<td>140</td>
</tr>
<tr>
<td></td>
<td>amplifier</td>
<td></td>
</tr>
<tr>
<td>3-5</td>
<td>Simulation results of estimated DFT of I channel</td>
<td>141</td>
</tr>
<tr>
<td>3-6</td>
<td>Simulation results of estimated ratio of DFT's</td>
<td>141</td>
</tr>
<tr>
<td>3-7</td>
<td>Simulation results showing error in estimation</td>
<td>141</td>
</tr>
<tr>
<td>3-8</td>
<td>Simulation results of phase estimate error</td>
<td>142</td>
</tr>
<tr>
<td>4-1</td>
<td>Weight update for the LMS filter</td>
<td>185</td>
</tr>
<tr>
<td>4-2</td>
<td>Estimated Poles based on $K_{I_{\text{max}}}$</td>
<td>185</td>
</tr>
<tr>
<td>4-3</td>
<td>Feedback path delay calculation</td>
<td>186</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>1-1</td>
<td>Power control signaling from base-station to mobile device</td>
<td>28</td>
</tr>
<tr>
<td>1-2</td>
<td>Occupancy of mobile users in frequency domain without power control</td>
<td>28</td>
</tr>
<tr>
<td>1-3</td>
<td>Ideal gain control with no error in correction after power control</td>
<td>29</td>
</tr>
<tr>
<td>1-4</td>
<td>Gain errors introduced due to analog/RF circuit imperfections as a function of operating conditions</td>
<td>29</td>
</tr>
<tr>
<td>1-5</td>
<td>Measured adjacent channel interference due to abrupt power control without signal shaping captured by Agilent N9020A MXA signal analyzer</td>
<td>30</td>
</tr>
<tr>
<td>1-6</td>
<td>Lower spectral leakage due to power control with signal shaping captured by Agilent N9020A MXA signal analyzer</td>
<td>30</td>
</tr>
<tr>
<td>1-7</td>
<td>System level overview of a mobile device</td>
<td>31</td>
</tr>
<tr>
<td>1-8</td>
<td>Reduction of signal power from the mobile device captured by Rhode and Schwartz CMU 2000 analyzer</td>
<td>32</td>
</tr>
<tr>
<td>1-9</td>
<td>Multiple power changes of the mobile device captured by Rhode and Schwartz CMU 2000 analyzer</td>
<td>32</td>
</tr>
<tr>
<td>1-10</td>
<td>Prior art that uses fixed digital gain offsets and errors to perform digital gain control</td>
<td>33</td>
</tr>
<tr>
<td>1-11</td>
<td>Prior art that adopts pre-calibrated analog bias levels for gain control and tracking</td>
<td>33</td>
</tr>
<tr>
<td>1-12</td>
<td>Prior art that adopts RF feedback and coarse analog bias adjust</td>
<td>34</td>
</tr>
<tr>
<td>1-13</td>
<td>Prior art that uses RF feedback and temperature compensation circuit for bias adjust</td>
<td>34</td>
</tr>
<tr>
<td>2-1</td>
<td>Primary sections of a mobile device transmitter</td>
<td>63</td>
</tr>
<tr>
<td>2-2</td>
<td>Absolute RF Power variation in dB due to temperature variations averaged over three parts</td>
<td>63</td>
</tr>
<tr>
<td>2-3</td>
<td>Pout variations across frequency bands over temperature</td>
<td>64</td>
</tr>
<tr>
<td>2-4</td>
<td>Absolute RF power variations in dB due to frequency of operation</td>
<td>64</td>
</tr>
<tr>
<td>2-5</td>
<td>Pout variations across frequency bands over supply voltage</td>
<td>65</td>
</tr>
</tbody>
</table>
2-6  System level block diagram of the DSP-DGT architecture.................................66
2-7  Controller adopted for the closed-loop DSP-DGT algorithm .............................67
2-8  Second-order closed-loop PID controller ..............................................................68
2-9  Closed-loop dynamics when the controller compensates for undesired positive gain change ...............................................................................................69
2-10 Closed-loop dynamics when the controller compensates for an undesired negative gain change .............................................................................................70
2-11 Flow chart of the steps involved in the DSP-DGT algorithm ...............................71
2-12 Linear Feedback shift register for a 6 tap pseudo random signal generator .......72
2-13 Timing signal to generate 6 times faster sample rate at the output .................72
2-14 Output pseudo random bit stream from a 6 tap linear feedback shift register. ....73
2-15 DSP implementation of sample rate logic .............................................................74
2-16 In-phase and quadrature phase signal swings whose magnitude has to be estimated. ...............................................................................................................74
2-17 Instantaneous error (linear) vs. input signal swing function as a function of $\alpha$ and $\beta$ factors ......................................................................................................75
2-18 Simple absolute value estimator logic .................................................................75
2-19 Digital DSP hardware structure for magnitude comparator .............................76
2-20 Digital DSP hardware structure for the magnitude estimator .............................77
2-21 System simulations with quantized I and Q random signals and mean error in estimation. ...........................................................................................................78
2-22 Ideal and obtained signal magnitude ....................................................................79
2-23 Magnitude error in dB as a function of buffer hardware length .......................79
2-24 DSP structure of the exponential averager ..........................................................80
2-25 Settling times of the averager as a function of filter factor ...............................80
2-26 Dynamic varying filter factor depending for noise and response time trade offs. .........................................................................................................................81
2-27 Magnitude response of the averager .................................................................81
<table>
<thead>
<tr>
<th>Page</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-28</td>
<td>Cascaded structure for the fast average circuit</td>
<td>82</td>
</tr>
<tr>
<td>2-29</td>
<td>Output of second filter vs. time in sec.</td>
<td>82</td>
</tr>
<tr>
<td>2-30</td>
<td>DSP structure for PID controller with programmable gains</td>
<td>83</td>
</tr>
<tr>
<td>2-31</td>
<td>Controller gain programming hardware</td>
<td>83</td>
</tr>
<tr>
<td>2-32</td>
<td>Digital implementation of 12 taps cross-correlation DSP hardware</td>
<td>84</td>
</tr>
<tr>
<td>2-33</td>
<td>Cross-Correlation of calibration signal</td>
<td>85</td>
</tr>
<tr>
<td>2-34</td>
<td>Simulation to show the correlation estimate between the calibration signal and the feedback signal</td>
<td>85</td>
</tr>
<tr>
<td>2-35</td>
<td>Signal buffer of baseband signal envelope</td>
<td>86</td>
</tr>
<tr>
<td>2-36</td>
<td>Detected Signal at the output of the ADC at the signal sample rate (no downsampling)</td>
<td>86</td>
</tr>
<tr>
<td>2-37</td>
<td>Normalized signal correlation between baseband signal envelope and detected signal.</td>
<td>87</td>
</tr>
<tr>
<td>2-38</td>
<td>Time aligned gain scaled baseband signal envelope and detected signal</td>
<td>87</td>
</tr>
<tr>
<td>2-39</td>
<td>Correlation estimate of baseband signal envelope and feedback signal with downsample ratio of N=2</td>
<td>88</td>
</tr>
<tr>
<td>2-40</td>
<td>Correlation estimate of baseband signal envelope and feedback signal with downsample ratio of N=5</td>
<td>88</td>
</tr>
<tr>
<td>2-41</td>
<td>Correlation estimate of baseband signal envelope and feedback signal with downsample ratio of N=10</td>
<td>88</td>
</tr>
<tr>
<td>2-42</td>
<td>Correlation estimate of baseband signal envelope and feedback signal with downsample ratio of N=20</td>
<td>89</td>
</tr>
<tr>
<td>2-43</td>
<td>Simulation to show injected 6dB gain variation and the reference signal level</td>
<td>89</td>
</tr>
<tr>
<td>2-44</td>
<td>Simulation to show the controller output adaptation for a positive 6dB gain variation in multiple steps</td>
<td>90</td>
</tr>
<tr>
<td>2-45</td>
<td>Simulation to show the closed-loop response with respect to different integral gains for a positive 6dB gain variation</td>
<td>90</td>
</tr>
<tr>
<td>2-46</td>
<td>Simulation of the closed-loop circuitry adaptation until error signal becomes zero.</td>
<td>91</td>
</tr>
</tbody>
</table>
2-47 Simulation to show the controller correction for +6dB, +5.5dB and -6.5dB gain variation. .............................................................................................................. 91

2-48 Simulation to show the controller output to track for +10dB, +3.5dB and -5.5dB gain variation. ............................................................................................. 92

2-49 System interface for mobile device testing ............................................................ 92

2-50 Analog version of the controller compensation by multiple steps to reach to
the desired power as captured by Tektronix oscilloscope ........................................ 93

2-51 Analog version of the controller compensation by a single step to reach to the
desired power level captured by Tektronix oscilloscope ........................................ 93

2-52 Analog response of the controller output shows oscillations due higher value
of integral gains captured by Tektronix oscilloscope .............................................. 94

2-53 Analog response of the controller output to shows over damped condition
due lower value of integral gains captured by Tektronix oscilloscope ..................... 94

2-54 Measured (FSIQ) plots of RF output at the power amplifier output as a
function of controller gains .................................................................................... 95

3-1 System block diagram of a wireless transmitter showing gain change and
phase change ............................................................................................................. 123

3-2 Measured amplifier bias vs. output characteristics with respect to
temperature and frequency bands of operation ..................................................... 124

3-3 Measured DNLE (dB) with respect to change is frequency bands of operation 124

3-4 Measured INLE with respect to change is frequency bands of operation .......... 125

3-5 Absolute phase variations of an RF device due to capacitive loads .............. 125

3-6 Gain and phase estimation A) System block diagram of the mobile device
with the DSP-GPE algorithm. B) Implemented frequency location of the
calibration signal during the algorithm .................................................................... 126

3-7 Frequency location of the calibration signal during the algorithm .................... 128

3-8 Flowchart of the DSP-GPE algorithm for relative gain and phase change
estimation ............................................................................................................... 129

3-9 Baseband signal phase compensation DSP hardware structure .................... 130

3-10 Simulation of baseband signal phase compensation by using the DSP
hardware structure ................................................................................................. 131
3-11 DSP Hardware structure to estimate the absolute gain change..........................131
3-12 DSP Hardware structure to estimate the absolute gain and phase change ......132
3-13 Simulation plots to show that $R_{x_{BB}}(t)$ with frequency of 400 KHz and
$\omega_{IF} = 300 KHz$ over the 8 RF gain settings .....................................................132
3-14 Simulation of FFT magnitude of $R_{x_{BB}}(t)$ with $\omega_{IF} = 300 KHz$ over the 8 RF
gain settings ..............................................................................................................133
3-15 Simulated DFT magnitude of I and Q channel for $K = 13, 14, 15, 16, 17$ ........133
3-16 Ideal gain change $\Delta G_{ref}$, estimated gain change $\Delta G$ (dB) and DNLE(dB)
$|\Delta G_{ref} - \Delta G|$..................................................................................................134
3-17 Ideal phase change $\Delta \lambda_{ref}$, estimated phase change $\Delta \lambda$ (deg) and
$\phi_{err} = |\Delta \lambda_{ref} - \Delta \lambda|$ ......................................................................................134
3-18 Averaged INLE error measured on three RFIC after the gain error
compensation. ..............................................................................................................135
3-19 Absolute phase variation in the mobile device after phase compensation ....135
3-20 Relative phase variation in the mobile device after compensation ...............136
3-21 Measured plots to show the 90 degrees phase compensation performed by
the DSP hardware ......................................................................................................137
4-1 Power control A) Measured transmit power to show the PAR and PTN of a
LTE signal captured by Rhode and Schwartz CMU 2000 B)System
architecture of the DSP-GC algorithm implemented in a mobile device .......167
4-2 DSP hardware implementation of the adaptive filter and 1st order integrator ....169
4-3 System constraints in selecting the controller gains .........................................170
4-4 Simplified closed-loop model ............................................................................170
4-5 Open loop based tuning technique .....................................................................170
4-6 Closed-loop based tuning technique .................................................................171
4-7 Closed-loop system with an integral controller ................................................171
4-8 Discrete model of closed-loop system at steady state .....................................171
4-9 Flow chart to estimate integral gain ..................................................................172
4-10 Step response of the unknown open loop system .............................................172
4-11 Plot of poles of the transfer function with $K_f = K_{f_{\text{max}}}$ .................................................................173
4-12 Closed-loop system simulations with appropriate integral gains .......................173
4-13 Simplified model for loop delay and gain margin analysis .....................................174
4-14 Pole-zero location with loop delay, $D = 1, 3, 7$ and $9$ samples at sample rate $s.$ ...........................................................................................................................174
4-15 Pole-zero location with loop delay, $D = 13, 17, 19$ and $21$ samples at sample rate $F_s.$ ........................................................................................................................................175
4-16 Pole-zero location with loop delay, $D = 24, 26, 28$ and $31$ samples at sample rate $F_s.$ ........................................................................................................................................175
4-17 Pole-zero location with loop delay, $D = 39, 45, 52$ and $58$ samples at sample rate $F_s.$ ........................................................................................................................................176
4-18 Closed-loop step response with respect to varying plant delays. .........................176
4-19 Pole-zero location with loop delay, $D = 13$ samples and integral gains of -36 dB, -32dB, -30dB and -26dB. ..................................................................................................................177
4-20 Pole-zero location with loop delay, $D = 13$ samples and integral gains of -22 dB, -20dB, -6dB and 9dB. ..................................................................................................................177
4-21 Power detector and feedback path input-output characteristics.............................178
4-22 Loop gain margin with varying loop delay as a function of antenna power .........179
4-23 Simulation to show the closed-loop dynamics for a positive power change ..... 180
4-24 Simulation to show the closed-loop dynamics for a negative power change..... 181
4-25 Simulation to show the adaptation of the LMS algorithm with weights and error signal .......................................................................................................................182
4-26 Simulation to show the rate of change of error signal and the feedback as a function of convergence factor ........................................................................................................183
4-27 Analog response of the closed-loop system with the adaptive filter captured by Tektronix oscilloscope ...........................................................................................................183
4-28 Analog closed-loop response for multiple steps with the adaptive filter captured by Tektronix oscilloscope ...........................................................................................................184
4-29 Transmit power of the mobile device captured by CMU 2000.........................184
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>BPSK</td>
<td>Binary Phase Shift Keying</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processing</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential Nonlinearity</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EDGE</td>
<td>Enhanced Data rates for GSM Evolution</td>
</tr>
<tr>
<td>GSM</td>
<td>Global Systems for Mobile Communications</td>
</tr>
<tr>
<td>I</td>
<td>In-phase</td>
</tr>
<tr>
<td>INL</td>
<td>Integral Nonlinearity</td>
</tr>
<tr>
<td>LMS</td>
<td>Least Mean Square</td>
</tr>
<tr>
<td>OFDM</td>
<td>Orthogonal Frequency Division Multiplexing</td>
</tr>
<tr>
<td>PID</td>
<td>Proportional, Integral and Derivative Controller</td>
</tr>
<tr>
<td>Q</td>
<td>Quadrature Phase</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>QPSK</td>
<td>Quadrature Phase Shift Keying</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RFIC</td>
<td>Radio Frequency Integrated Circuit</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
</tr>
<tr>
<td>SIR</td>
<td>Signal to Interference Ratio</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage controlled oscillator</td>
</tr>
<tr>
<td>VGA</td>
<td>Variable Gain Amplifier</td>
</tr>
<tr>
<td>Wi-MAX</td>
<td>Worldwide Interoperability for Microwave Access</td>
</tr>
<tr>
<td>WCDMA</td>
<td>Wideband Code Division Multiple Access</td>
</tr>
</tbody>
</table>
We introduce system architectures and algorithms with related DSP hardware structures to dynamically estimate and compensate for relative/absolute gain variations in any analog or digital signal processing paths. In addition, the presented techniques are used to calibrate and compensate for relative signal phase shifts occurring in a mobile device. The techniques described in this thesis are implemented in a mobile device to dynamically estimate and compensate for absolute and relative signal power variations from the desired power levels. These techniques help to prolong battery life of the mobile device and to reduce signal-to-interference ratio (SIR) at the base-station. In addition the described system algorithms are implemented using efficient digital circuitry which eliminates the bulky analog components which were originally used for this purpose. The digital circuit implementation makes the mobile device less susceptible to variations in temperature, frequency of operation and manufacturing processes. The digital area of the implemented digital circuitry is found to be around 22K gates and the digital current drain is approximately 20mA. System lab measurements show that the
mobile system is able to compensate better than 0.1dB absolute and relative power level accuracy and also result in phase estimation accuracy better than 1 degree.
CHAPTER 1
INTRODUCTION

The demand for mobile access and high data rate communications services such as video teleconferencing, real time video streaming, internet access, music download and file transfers continues to grow rapidly for a wide variety of military as well as commercial mobile applications. It is highly essential for all the mobile standards to co-exist without any of the mobile devices degrading signal quality of the other devices. In order to accomplish this, present day mobile communications networks employ power control techniques wherein the base-station sends control commands to each of the mobile devices to ensure that each of the mobile users transmits only the required amount of signal power to maintain a good quality transmission and reception link. These power control techniques not only help prolong battery life for the mobile device, but also dramatically reduce SIR [23] in the system.

The base-station estimates the amount of power change required by the mobile device using various power control algorithms [50] depending on the mobile standard. Similarly, each mobile user employs various techniques to respond to the commands from the base-station with the help of analog and digital signal processing circuits implemented inside the mobile device. In this thesis, we focus on techniques that are implemented in each mobile device that provide absolute/relative gain control and compensation as dictated by the base-station.

1.1 Motivation: Need for Power Control and Gain Tracking Inside Mobile Device

In response to dictated power level commands from the base-station, each mobile device must dynamically alter the absolute transmit power level and keep track of relative power level changes. This is accomplished with the help of digital, analog and
radio frequency (RF) circuitry present inside the mobile IC. The design and performance of these circuits within each mobile device determines the precision of the power control. This thesis work describes system algorithms and corresponding digital circuit implementations used inside mobile devices to dynamically estimate and compensate for any power change commands from the base-station. In addition, these circuits can be used to track the gain variations of the mobile device and to automatically compensate for gain and phase errors. This helps in maintaining absolute and relative power level accuracy. The described algorithms have been implemented in a mobile device and lab measurements are provided to validate the system performance.

The primary reasons for dynamic gain control circuitry inside any mobile device or in any base-station transmitter are to

1. Increase system capacity by reducing signal interferences within an operating cell.
2. Improve transmit signal quality by accurately scheduling and allocating desired power levels.
3. Dynamically compensate for gain variations caused by local analog/RF circuits.
4. Perform gain changes and corrections in a spectrum-friendly manner to reduce interference to neighboring users.
5. Provide finer gain control updates. (0.1dB accuracy).
6. Increase co-existence of various mobile schemes such as Worldwide Interoperability for Microwave Access (Wi-Max), Blue-tooth, Cellular, and Digital Video Broadcasting (DVB) such that all these features available in a single mobile device.
7. Maintain system gain accuracy until the next power change commands arrive from the base-station.

Figure 1-1 illustrates how the base-station signals the mobile users within a cell site to either increase or decrease the transmit signal power depending on their
location. Based on the signal quality estimate, power control commands are sent to each mobile user to instruct the mobile to raise or lower its transmitted power in allotted decibel (dB) steps. If the received signal power at the base-station is low, then a “1” is transmitted to signal the mobile user to increase its mean power level. If the received signal power at the base-station is high, the base-station signals a “0” to reduce the power level of the user.

To understand the gain control mechanism and the issues faced, assume a mobile system with eleven users and each assigned a separate frequency band of operation as shown in Figure 1-2. The red dotted line in Figure 1-2 indicates the desired signal power the base-station must receive from each mobile user to preserve signal quality irrespective of the mobile user’s distance from the base-station. Figure 1-2 indicates that in the absence of power control from the base-station, the received power levels at the base-station from certain mobile users do not meet the desired SIR. The weaker signals are completely degraded by the stronger signals and result in dropped calls. In order to solve this issue, the base-station sends power control commands to the mobile device to increase or decrease the transmit power levels depending on the location of the mobile device with respect to the base-station.

As an example, assume that the base-station signals a mobile user to raise its power level by 4dB. Based on this command, it is the responsibility of the circuitry inside the mobile device to raise its power level by the desired 4dB. The amount of gain error between the ideal and the obtained power level change is called as power tolerance allowance and is a critical factor that influences relative power level accuracy.
Figure 1-3 shows ideal power control without any gain errors introduced during the gain control process. However, it is very difficult to achieve such precise control practically due to imperfections of the analog and RF circuit as a function of operating conditions. The performance of analog and RF circuits with respect to operating temperatures, frequency bands of operation, battery voltage causes gain and phase errors which degrade gain control accuracy. This is discussed in detail in Chapter 2. As shown in Figure 1-4, in present day cellular standards, the power tolerance allowance for gain variations is around +/-3dB. For advanced protocols such as LTE (Long Term Evolution) and 2G Evolution, the margin for gain variations is less than 0.2dB to support different mobile standards to co-exist. These stringent power accuracy requirements demand for precise and efficient dynamic digital gain correction techniques to yield gain corrections better than 0.2 dB accuracy.

Another issue in present day circuits is that the gain correction is performed instantaneously and hence leads to spectral leakage into [7],[39] bands. This in turn causes reduction of system capacity. Figure 1-5 and Figure 1-6 shows the transmit spectrum measured at the output of the mobile device operating at 2.5GHz band. The communication testing equipment used to capture this measurement is Agilent N9020A MXA signal analyzer [82]. As shown in Figure 1-5, an uncontrolled instantaneous rapid gain change performed in the mobile device leads to spectral leakage and causes interference to the adjacent user[1]. This degrades the SNR of the adjacent user and hence reduces system capacity. The gain change or gain compensation applied to the analog or the digital stages of the mobile device must be controlled in a spectrum-friendly profile to reduce out of band spectral emissions as shown in Figure 1-6. These
issues demand for dynamic signal gain tracking and gain control algorithms which will help adjust the rate of gain correction in a spectrum-friendly manner and reduce out of band spectral emissions.

1.2 Power Control Techniques in Mobile Devices

Before we discuss various techniques employed by a mobile device to alter its power level, this section describes the various components of a mobile device and the process by which the mobile device responds to commands from the base-station. Figure 1-7 describes the primary sections of any mobile device. The device consists of a Radio Frequency IC (RFIC) also known as the transceiver, the baseband modem processor which interacts with the base-station commands and is responsible for any audio-video, data decoding and encoding and modulation algorithms. The RFIC's transmitter section receives the data bits from the modem and passes it through digital filtering stages for pulse shaping and upsampling. The digital data is then converted into analog signals by the digital to analog converter (DAC) and then modulated into RF frequencies. The modulated signal passes through the variable gain driver amplifier (VGA) and transmitted to the base-station through the power amplifier (PA).

When the signal is received from the base-station to the mobile device, the received RF signal is passed through a low-noise amplifier, and demodulated into a baseband signal. The analog signal is then converted to a digital signal by the analog to digital converter (ADC) [3] and passed into receive digital filter stages for further processing. The output bit stream from the filter stages is sent to the baseband processor for further decoding. Depending on the nature of the signal (audio/video/data), the baseband processor performs the decoding algorithms and outputs the signal through the speaker or on the display.
Figure 1-8 and Figure 1-9 show measured transmit power changes, captured by communication testing equipment Rhode and Schwartz CMU 2000 [79] at the output of the mobile device. In Figure 1-8, the mobile device is moving close to a base-station and hence the transmit power is decreased. Figure 1-9 shows a mobile responding to commands from the base-station to increase or decrease its transmitting power level due to varying channel quality.

1.3 Present Day Techniques and Prior Art

The following approaches are adopted in present day mobile devices to dynamically provide gain change in response to commands from the base-station. These approaches are either used in the mobile devices or in the base-station amplifiers to perform dynamic power control in order to increase signal quality and system capacity. Each of the approaches is explained below.

1.3.1 Use of Fixed Calibrated Digital Gain Offset and Error Values

In this prior art [57], as a measure of power levels required for transmission and the signal quality requirements of the base-station, pre-calibrated digital gain factors and offsets are applied to the digital signal paths to compensate for any gain errors in the transmit path. These calibrated values of gain and phase offsets are a function of desired power levels, operating frequency bands, battery voltage and temperature. The pre-calibrated gain and phase offsets are stored in digital memory look up tables and applied to the transmitter during signal transmission [4], [47]. This is a popularly adopted method to perform transmit power change in the mobile device or in base-station transmitters. In addition to the need for extensive calibrations, this approach places a huge demand on memory storage requirements. Also, this technique is an open loop...
method and cannot account for slow varying gain errors due to temperature unless separate temperature compensation circuits are used.

1.3.2 Use of Pre-Calibrated Analog Bias Signal for Constant Envelope Modulation

In this prior art [65], the bias setting of the power amplifier or the driver amplifier is altered by digital control. The digital control can be as simple as a ROM look up table or can be a ramp pattern that can be programmed with respect to operating power levels. This is a very popular technique which is still adopted for constant envelope modulation schemes such as GMSK (Gaussian Minimum shift keying). The bias voltage of the power amplifier is changed in order to effect a power change in the desired direction at the PA output. However, the final digital value needs to be calibrated as a function of desired power levels. As a limitation, this technique can only be used for constant envelope modulations schemes to satisfy linearity and efficiency trade-offs [21], [36]. This technique is also an open loop method and cannot account for temperature based drifts in the signal power level unless temperature compensation circuits are used.

1.3.3 Use of RF Feedback and Analog Bias Control

In this prior art [75], the transmitted RF power is fed back to a device called power detector which converts RF power into equivalent voltage signal. This feedback analog voltage signal is compared with an analog reference signal which is equivalent to the desired power level. The error between the reference signal and the feedback signal is used to alter the bias setting of the variable gain amplifier by using digital logic and decoder control [31], [53], [59-64]. This technique can be used for real-time gain control when the mobile device is transmitting signal power by monitoring the gain variations.
Although this technique is widely used in present day mobile devices and base-station transmitters, it suffers from a few limitations. It requires calibration of the bias correction factor for the VGA based on the error signal’s magnitude. The complexity of the analog circuits which generates the reference signal voltages increases with increase in the desired amount of dynamic range of gain control.

1.3.4 Use of RF Feedback and Temperature Compensation Circuit Based Gain Control

In this technique [74], the RF power is looped back and sent into a receiver network which demodulates the RF signal and converts it to an equivalent analog voltage signal. The analog voltage signal is compared with an output signal generated by a temperature compensation circuit. Based on the error signal generated, a digital logic circuit is used to perform bias compensation on the driver amplifier or VGA. Thus, as a function of generated bias compensation, the transmit power of the mobile device is adjusted to account for the variation of any power change caused by circuit anomalies. Though this circuit controls the power based on temperature changes, it cannot guarantee very fine resolution of gain control.

1.4 Limitations of Prior Art

To summarize, the limitations of the prior art techniques are as described below

1. They do not solve the spectrum leakage issue. Since the gain correction is applied as a static compensation either at the digital or at the analog sections, these techniques can only provide instantaneous gain change and hence will cause spectrum splatter [41-42], [48-49], [51] as described in earlier sections.

2. There is no ability to control the rate at which the gain change is performed and hence there is no control on the amount of the time in which the power change has to be performed.

3. Local RF loop back solution does not provide infinite precision and cannot provide fine gain control accuracy due to analog circuits.
4. The prior art lack compensation for any random phase variations. Any random phase shift caused in the signal paths will lead to gain error and hence will degrade power accuracy. There is no dynamic compensation for relative phase shifts.

5. The prior art uses fixed correction techniques. Existing prior art techniques are static correction techniques and will need extensive calibration of gain and phase correction parameters.

1.5 Research Effort Comparisons

Table 1-1 describes the three new techniques and the compares their significance and applications.

1.6 Organization of Thesis

The organization of this thesis is described as follows:

Chapter 2 describes the possible causes for variations in both transmit and receive signal power levels of a mobile device. It describes DSP based absolute gain/power monitoring technique (DSP-DGT) using digital control loop and signal correlation circuitry to correct for gain variations introduced due to analog circuit imperfections. The DSP-DGT technique is implemented using digital signal processing hardware and system lab measurements are provided to validate the performance. The DSP-DGT technique is found to dynamically monitor gain fluctuations in a mobile device introduced by analog circuit imperfections.

Chapter 3 introduces a Discrete Fourier Transform (DFT) based DSP technique and hardware structures to compensate for the relative gain and phase errors and hence maintain relative power control accuracy (DSP-GPE). The DSP-GPE technique uses digital signal processing circuits to estimate the relative gain error (differential nonlinearity error, DNLE) caused by the analog RF gain amplifier. In addition to relative gain error compensation, this chapter also describes a method to calibrate the carrier.
phase changes that happen in any mobile device due to change in the capacitive load impedances on the RF analog path. The estimated relative carrier phase change is then applied as compensation when the mobile device transmits signal to the base-station. This technique maintains the transmit power accurately by compensating for gain error introduced due to differential gain nonlinearity and relative phase shifts errors. System lab measurements are provided to illustrate the performance of the DSP-GPE technique.

Chapter 4 describes a technique and DSP hardware structures to dynamically control the absolute signal power of any mobile device by using an adaptive DSP control along with an integral controller (DSP-GC). The primary goal of the DSP-GC technique is to reduce the signal variances at input to the controller which are caused due to higher order modulation schemes. Reduction of signal variance makes the response of the closed-loop system more predictable and faster. A new loop tuning algorithm based on stability constraint method is defined and the controller gains are estimated for an unknown plant transfer function. The DSP-GC technique has also been implemented in a mobile device and lab measurements are provided.

Chapter 5 provides the summary and conclusions of the thesis work. It also provides other areas where these techniques can be applied. In addition, it outlines the scope for further work and improvements that can be made depending on the applications.
Power is increased to as the distance is large

Base-station signal user to increase power level

Transmit Power is increased to as the distance is large

Base-station signal user to increase power level

No change in user power level

User is signaled to reduce Power level

User is signaled to Transmit higher power

Figure 1-1. Power control signaling from base-station to mobile device

Signal energy at the base-station

Without power control in a 11 user cell

Figure 1-2. Occupancy of mobile users in frequency domain without power control
Figure 1-3. Ideal gain control with no error in correction after power control

Figure 1-4. Gain errors introduced due to analog/RF circuit imperfections as a function of operating conditions
Abrupt power control without signal shaping leads to out of band spectrum leakage and leads to adjacent channel interference.

Figure 1-5. Measured adjacent channel interference due to abrupt power control without signal shaping captured by Agilent N9020A MXA signal analyzer

Controller Power control based on signal shaping (Reduce out of band spectrum)

Signal image

Carrier leakage

Figure 1-6. Lower spectral leakage due to power control with signal shaping captured by Agilent N9020A MXA signal analyzer
Figure 1-7. System level overview of a mobile device
Upon signaling from base-station, the transceiver reduces the power level transmitted.

Figure 1-8. Reduction of signal power from the mobile device captured by Rhode and Schwartz CMU 2000 analyzer

Due to varying channel quality, the base-station could signal the mobile to increase or decrease the transmit signal power to maintain constant SIR.

Figure 1-9. Multiple power changes of the mobile device captured by Rhode and Schwartz CMU 2000 analyzer
Figure 1-10. Prior art that uses fixed digital gain offsets and errors to perform digital gain control.

Figure 1-11. Prior art that adopts pre-calibrated analog bias levels for gain control and tracking.
Figure 1-12. Prior art that adopts RF feedback and coarse analog bias adjust

Figure 1-13. Prior art that uses RF feedback and temperature compensation circuit for bias adjust
**Table 1-1. Comparison of New Techniques**

<table>
<thead>
<tr>
<th>Significance and system comparison metrics</th>
<th>Digital DSP Techniques and Efficient Hardware Topologies for Absolute Gain Tracking (DSP-DGT)</th>
<th>DSP Based Dynamic Estimation and Compensation of Differential Gain Nonlinearity and Random phase shifts (DSP-GPE)</th>
<th>Dynamic Gain/Power Control Using Adaptive DSP Techniques (DSP-GC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Motivation</td>
<td>Estimate and compensate for relative gain variations due to differential nonlinearity’s and also helps to compensate for relative random phase shifts to preserve signal phase variations</td>
<td>Adaptive algorithm that minimizes the signal variances at the input to the controller and dynamically compensates for instantaneous gain variations and helps to perform signal power change based on desired reference power.</td>
</tr>
<tr>
<td>2</td>
<td>Underlying theory and principle</td>
<td>Sliding DFT based signal energy and random phase shift estimation</td>
<td>- N Tap adaptive filter with programmable convergence factor for instantaneous gain tracking and reducing signal variance</td>
</tr>
<tr>
<td>3</td>
<td>Targeted system performance metrics</td>
<td>Baseband digital gain and phase compensation</td>
<td>- Integral controller for average gain tracking and control.</td>
</tr>
<tr>
<td>4</td>
<td>Modulation schemes supported</td>
<td>Mobile specifications</td>
<td>Mobile specifications</td>
</tr>
<tr>
<td>5</td>
<td>Loop stability</td>
<td>Relative phase accuracy requirements.</td>
<td>- Absolute gain change/control requirements.</td>
</tr>
<tr>
<td></td>
<td>Function of integral gains and the delay estimate based on cross-correlation.</td>
<td>Relative gain accuracy and distortion nonlinearity requirements (between baseband processor and RFIC)</td>
<td>- Absolute power level accuracy</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Linearity requirements. (Power change vs. obtained command).</td>
<td>- Gain change and settling time requirements.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cell capacity requirements</td>
<td>- Cell capacity requirements</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Enhances battery life by performing mobile power tracking and compensation</td>
<td>- Enhances battery life by performing mobile power tracking and compensation</td>
</tr>
</tbody>
</table>

**Table 1-1 continued**

<table>
<thead>
<tr>
<th>Modulation schemes supported</th>
<th>Loop stability</th>
<th>Function of integral gains and the delay estimate based on cross-correlation.</th>
</tr>
</thead>
<tbody>
<tr>
<td>GMSK, WCDMA (QPSK, QAM, BPSK) (independent of modulation schemes)</td>
<td>Loop stability is not a concern. The main concern is quantization error that leads to gain errors.</td>
<td>Function of the loop latency introduced and convergence factor programmed along with integral gains</td>
</tr>
<tr>
<td>GMSK, WCDMA (QPSK, QAM, BPSK) (independent of modulation schemes)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Significance and system comparison metrics</td>
<td>Digital DSP Techniques and Efficient Hardware Topologies for Absolute Gain Tracking (DSP-DGT)</td>
<td>DSP Based Dynamic Estimation and Compensation of Differential Gain Nonlinearity and Random phase shifts (DSP-GPE)</td>
</tr>
<tr>
<td>------------------------------------------</td>
<td>------------------------------------------------------------------------------------------</td>
<td>---------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>6 System DSP hardware requirement &amp; estimated gate count</td>
<td>- Existing external RF detector - PID controller hardware - DSP cross-correlator - Fast Signal Averager - Fast magnitude estimator - Delay buffer - Sample rate adjust logic - Pseudo random code generator 22K, 20mA</td>
<td>- Sliding DFT magnitude and phase estimator - Baseband phase compensation DSP hardware - RF loop back with existing demodulation path &lt;10K gates, 12mA</td>
</tr>
<tr>
<td>7 System lab measurements and performance</td>
<td>Lab measurements show that the DSP-DGT technique is able to compensate up to 0.1dB gain accuracy. Settling time of 50usec</td>
<td>Lab measurements show that the DSP-GPE technique is able to compensate up to 0.1dB of gain accuracy and phase accuracy of &lt;1 degree.</td>
</tr>
</tbody>
</table>
CHAPTER 2
DIGITAL DSP TECHNIQUES AND EFFICIENT HARDWARE TOPOLOGIES FOR ABSOLUTE GAIN TRACKING

2.1 Problem Statement

As mentioned in Chapter 1, power change commands are sent by the base-station to the mobile device to either increase or decrease its transmit power level. The base band processor present inside the mobile device decodes the command received from the base-station and provides internal gain change commands to either the digital or analog RF sections of the transmit path to provide the desired gain corrections. The desired gain correction can be performed by either changing the bias level of the VGA/PA or by changing the digital gains of the transmit path. There are three primary concerns associated with any gain control techniques adopted on a mobile device which requires analysis.

1. The gain changes performed by the mobile device must not be an instantaneous change to avoid spectral leakages to the neighboring user.

2. In addition to this issue, in mobile devices, there is always an error between the desired gain change and the actual gain change that occurred due to the circuit imperfections and performance variations of RF circuits as a function of temperature, frequency and battery voltages.

3. Another primary concern in any mobile device is to perform the desired power change as requested by the base-station and maintain the desired power level accuracy until the next power change is requested by the base-station. For example on a WCDMA [23],[35] (wideband code division multiple access) system, a mobile user can be on a signal transmission for 4-5 hours continuously while moving around with respect the base-station. During these conditions, it is very critical for the mobile device to guarantee the desired gain accuracy and the power error allowance until a next power change command occurs.

This chapter describes a DSP-based absolute gain/power monitoring and tracking technique (DSP-DGT) using digital control loop and signal correlation circuits to correct for gain variations introduced due to analog circuit imperfections. The DSP-DGT
technique has been implemented using digital DSP hardware and system lab
measurements have been provided to validate the performance. DSP hardware
structures employed in this algorithm are described along with system measurements.

**2.2 Reasons for Signal Gain Variations in Mobile Devices**

Before we introduce solutions, it is important to investigate and understand the
reasons for signal gain variations in any mobile device. The reasons for gain variations
are discussed in the following section.

**2.2.1 Gain variations due to Manufacturing Processes**

The performance of the baseband and RF components is a function of variations in
manufacturing process. Although the components are manufactured according to a
particular set of design specifications using defined manufacturing processes, non-
uniform results may be obtained due to uncontrolled deviations in the processes used to
fabricate the constituent semiconductor components. Typical cellular telephone designs
attempt to locate the baseband DAC, ADC and RF components in different physical
locations in the cellular telephone to avoid interference. One drawback of this design
approach is that the process variations in the manufacturing phase of the components
do not track one another. In a worst case scenario, the DAC, the ADC and RF
components have a maximum variation in the same direction which results in a
maximum total transmit gain deviation from the nominal transmit gain value.

The measurements were performed inside a temperature chamber and averaged over
three IC’s. Figure 2-2 shows that the measured RF power level drops as the
temperature increases. This drop in RF output power will eventually degrade
communication link performance and ultimately lead to lower signal to noise ratio [57,
60, and 62].
2.2.2 Power Gain Variations due to Change in Junction Temperature

In amplifier design, the power gain of transistors used in an RF amplifier decreases with increasing junction temperature of the transistors. Power transistors dissipate large amounts of power in the collector – base junctions[26]. Apart from change in ambient temperature, similar gain delta responses can also be induced by a change in the junction temperature of the power amplifier. The increase in junction temperature is usually associated with high output power operation. For example, at an output power of 28 dBm, the junction temperature of the power transistors will be increased due to higher dissipated DC power, while the junction temperature of the same power transistors will be lower at a lower output power (e.g. 16dBm).

Figure 2-3 shows measured data of absolute RF power variations over low, mid and high frequency bands of operation across cold (-35 degrees), room(+25degrees) and hot (+85 degrees) temperatures. The experiment reveals that as temperature increases the gain drops and the gain drop is not exactly same across frequency bands of operation. However, the gain drop due to frequency bands of operation is relatively less as compared to gain drop due to temperature variations. The measurement results illustrated here is average of three IC’s.

2.2.3 Change in Power Gain Due to Different Operating Paths Depending on Power Level

Another reason for gain variations in multi-mode amplifiers is due to the presence of parallel power paths. In the state of art of multi-mode amplifier design, there exists independent parallel path to support different power levels, lower power and higher power paths. The higher power path may be used where the design requires an output power from about 16 to 28 dBm, and the lower power path may be used for power less
than 16 dBm. One direct effect of the two (or more) power path design is that the device characteristics associated with each path are different since the electronic components in each path are different. For example, the active transistor sizes and DC currents in each path are different due to different power handling requirement for each path. These result in different electrical and thermal responses between the two paths. More specifically, the two paths experience different gain variations over temperature, resulting in a gain mismatch between the two paths.

2.2.4 Variation in Gain Due to Different Operating Frequencies and Supply Voltage

Change in frequency and supply voltage of operation of any baseband or RF device will lead to change in DC operating point of the device, change in input impedances and change in the matching network. These will ultimately lead to gain variations due to supply voltage and frequency bands of operation. Figure 2-4 and Figure 2-5 shows measured data that characterizes the gain drop across frequency bands of operation and battery voltage variations.

2.3 DSP Based Dynamic Gain Tracking Algorithm (DSP-DGT)

2.3.1 System Architecture of the DSP-DGT Algorithm

The system algorithm described in this chapter dynamically compensates for absolute gain variations that are caused in any mobile system due to performance variations of RF and analog circuits based on different manufacturing process, temperature and frequency bands of operation. The algorithm uses the magnitude of the digital base band signal as the reference input to the algorithm. The transmitted power is feedback and compared to the desired reference signal. An error signal is generated based on the difference between the average magnitude of the reference and the feedback signal. The error signal is used to drive a controller to generate a
control signal that compensates for the gain differences between the reference path and the feedback path. A cross-correlation circuit is used to time align the reference and the feedback path before the start of the controller operation. The introduced technique not only helps to compensate for gain variations but also helps in shaping the power change in a spectrum friendly way and avoids adjacent channel interference.

The system block diagram of the DSP-DGT algorithm is shown in Figure 2-6. The digital IQ samples pass through the digital filtering stage and get converted to an analog signal by the DAC. The differential DAC output goes to the baseband reconstruction filters. The baseband filter outputs are converted to RF/IF frequencies depending on the applications (Cellular, Wireless local are network (WLANS) or Audio signal paths) and passes through an RF gain amplifier stage and transmitted through a power amplifier. There are two signal paths for the introduced system architecture, namely the feedback path and the feed forward path.

2.3.2 Feedback Path

The output of the RF amplifier is feedback into a power detector [45],[56],[70] which takes in RF Power (dBm) and gives out corresponding DC voltage. The detector output is feedback into a variable gain block with an anti-aliasing filter. The output of the filter is quantized into digital word by an analog-digital converter (ADC). The variable feedback gain is chosen and implemented based on the input signal dynamic range of the ADC. Varying the feedback gain as a function of the RF power levels improves the signal-to-noise ratio of the feedback signal. The quantized digital word is then buffered and averaged by employing a digital fast averaging circuit as will be described in section 2.5.4.
2.3.3 Forward Reference Path

As shown in Figure 2-6, the digital signal is tapped before the DAC and used as the reference signal for the algorithm. The magnitude of the in-phase signal component and the quadrature signal component signals are estimated by the fast averaging hardware. The magnitude is then averaged by using the exponential average DSP hardware and used as a reference signal to the proportional and integral controller. As shown in Figure 2-6, the closed-loop feedback loop controller tracks for any change in gain variations between the feedback and the reference signal paths.

As the ideal gain of the feedback path and the forward path is known, the gain of the reference signal path is calibrated accordingly. A digital cross-correlation circuit is employed to estimate the cross-correlation between the reference signal and the feedback signal to calibrate the delay buffer in the reference signal path. This helps in dynamically calibrating the delay between the reference and the feedback signal paths before the gain estimation and tracking is performed. The buffer control logic also adjusts for the sample rate differences between the forward path and feedback path signals.

2.4 Algorithm Theory

The block diagram of the described system architecture is shown in the Figure 2-6. The components of the algorithm are described as follows.

1. Buffer control for sample rate and block size adjustment (DSP hardware)
2. Fast exponential averaging circuit (DSP hardware)
3. Fast magnitude estimation (DSP hardware)
4. Gain controller with proportional, integral and differential control (DSP hardware)
5. Digital calibration signal pattern generation circuit. (DSP hardware)
6. Signal cross-correlation circuit. (DSP hardware)
7. Feedback path power detector (RF discrete component)
8. Analog feedback gains (analog baseband)
9. Ant-aliasing filter and ADC (analog baseband)
The baseband modem sends the information bits from the base band processor into the digital path stages inside the RFIC. The digital stages have pulse shaping filters to reduce inter-symbol interference (ISI) [23] and multi-rate filters to alter the sampling frequency of the filters in accordance to the available clock rates and the DAC operating rates.

As shown in Figure 2-6, assume that the base band I channel and Q channel signals are represented by

\[ I(n) = d_1 \cos(\omega_{bb} n) \quad (2-1) \]
\[ Q(n) = d_1 \sin(\omega_{bb} n) \quad (2-2) \]

where \( d_1 \) is the digital gain, \( \omega_{bb} \) is the baseband signal frequency. The signals \( I(n) \) and \( Q(n) \) are converted to analog signals \( I(t) \) and \( Q(t) \) by the DAC present in the transmit path. The signals are then up converted by the RF modulator. The input to the modulator is then up converted to RF frequency and can be expressed as

\[ \text{modout}(t) = d_1 \times [(\cos(\omega_{bb} t) + j \sin(\omega_{bb} t + \phi))] e^{j\omega_{RF} t} \quad (2-3a) \]

where \( \omega_{RF} \) is the up conversion frequency. The output of the modulator is amplified by the PA and transmitted over the antenna. The signal transmitted over the antenna can be represented as

\[ \text{PA}(t) = G_1 \times d_1 \times [(\cos(\omega_{bb} t + \phi) + j \sin(\omega_{bb} t + \phi))] e^{j\omega_{RF} t} \quad (2-3b) \]

where, \( G_1 \) is the power amplifier gain. The magnitude of the power in dBm (dB with respect to 1mW) at the output of the PA is represented as

\[ P_{\text{out}}(\text{dBm}) = 10 \log(G_1 d_1 \sqrt{I^2 + Q^2}) + 30 \text{ dBm} \quad (2-4) \]
The output of the power amplifier is converted into an equivalent DC voltage signal by using an RF power detector which converts RF power (dBm) into average DC voltage. The power detector outputs linear DC voltage for RF input power in dBm. The output of the detector in volts is approximated to be the envelope of the signal power and denoted as

\[ v(t) = \beta \left\lfloor \text{abs}(I^2 + Q^2) \right\rfloor \] \hspace{1cm} (2-5)

where, \( \beta \) is the feedback path gain.

**Controller theory, Flow chart of the algorithm.** The algorithm employs a PID controller to dynamically track for any absolute gain variations in any closed-loop feedback system. Literature about any PID controller can be found in [71]. In our applications, we exploit the benefits of this controller to dynamically track gain variations. A second-order closed-loop PID controller is shown in Figure 2-8. The plant transfer function for a second-order system is is given by

\[ D(s) = \frac{G_p}{(s + p_1)(s + p_2)} \] \hspace{1cm} (2-6a)

where \( p_1 \) and \( p_2 \) are system poles

Replacing \( s = j\omega \), in Equation 2-6(a) results in

\[ D(s) = \frac{G_p}{(j\omega + p_1)(j\omega + p_2)} \] \hspace{1cm} (2-6b)

The reference signal input to the system is defined by \( R(s) \) and the system output is represented by \( Y(s) \) and \( \beta \) is the feedback gain. The proportional, derivative and the integral gains are represented by \( K_p \), \( K_D \) and \( K_I \). The error signal between \( R(s) \) and the feedback signal \( \beta Y(s) \) is represented by \( E(s) \). Hence,
\[ E(s) = R(s) - \beta Y(s) \]

The controller output \( P(s) \) is represented by

\[ P(s) = (sE(s)K_D) + KpE(s) + \frac{1}{s}K_I E(s) \quad (2-7) \]

Solving for the time constants,

\[ Y(s) = P(s)A(s) \frac{G_p}{(s + p_1)(s + p_2)} \]

\[ P(s) = E(s)[(sK_D) + Kp + \frac{1}{s}K_I] \]

\[ Y(s) = E(s)[(sK_D) + Kp + \frac{1}{s}K_I] A(s) \frac{G_p}{(s + p_1)(s + p_2)} \]

\[ Y(s) = E(s)[(s + \tau_1)(s + \tau_2)] s AG_p K_D \frac{1}{(s + p_1)(s + p_2)} \]

where \( \tau_1, \tau_2 = \frac{1}{2} \left( \frac{K_p}{K_D} + \sqrt{\left( \frac{K_p}{K_D} \right)^2 - 4\left( \frac{K_I}{K_D} \right)} \right) \quad (2-8) \]

\[ Y(s) = E(s)[(s + \tau_1)(s + \tau_2)] s AG_p K_D \frac{1}{(s + p_1)(s + p_2)} \]

\[ E(s) = \frac{s(s + p_1)(s + p_2)Y(s)}{(s + \tau_1)(s + \tau_2) AG_p K_D} \]

\[ E(s) = R(s) - \beta Y(s) \]

\[ Y(s) = \left[ \frac{s(s + p_1)(s + p_2)}{(s + \tau_1)(s + \tau_2) AG_p K_D} + \beta \right] Y(s) = R(s) \]

\[ Y(s) = \frac{(s + \tau_1)(s + \tau_2) AG_p K_D}{s(s + p_1)(s + p_2) + \beta (s + \tau_1)(s + \tau_2) AG_p K_D} \quad R(s) \quad (2-9) \]
Assume that the input $R(t)$ is a unit step, and can be represented as

$$R(t) = Ru(t)$$

$$R(s) = \frac{R}{s} \quad (2-10)$$

$$Y(s) = \left[ \frac{(s + \tau_1)(s + \tau_2)AG_pK_D}{s(s + p_1)(s + p_2) + \beta(s + \tau_1)(s + \tau_2)AG_pK_D} \right] \left( \frac{R}{s} \right)$$

At steady state the final value

$$y(t) |_{t \to -0} = sY(s) |_{s \to -0} = s \left[ \frac{(s + \tau_1)(s + \tau_2)AG_pK_D}{s(s + p_1)(s + p_2) + \beta(s + \tau_1)(s + \tau_2)AG_pK_D} \right] \left( \frac{R}{s} \right)$$

$$sY(s) |_{s \to -0} = \left[ \frac{(\tau_1)(\tau_2)AG_pK_D R}{\beta(\tau_1)(\tau_2)AG_pK_D} \right]$$

$$Y_{ss}(t) = sY(s) |_{s \to 0} = \left[ \frac{R}{\beta} \right] \quad (2-11)$$

Equation 2-11 shows that the steady state value of $y(t)$ is equal to the ratio of the amplitude of the input and the feedback gains. When the system reaches steady state, the error signal $e(t) = 0$ and the feedback signal $\beta Y(s) = R(s)$. In the presence of external disturbances in gain $G_p + \Delta g$ due to temperature and operating conditions, the controller tries to track for any additional gain variations $\Delta g$ as described in the above Equations. The system simulation with a simple controller proves the theory of operation. The rise time, the maximum peak overshoot and the settling time depend on the controller gains selected and the application. A detailed illustration of the controller operation and corresponding loop dynamics for a positive and a negative gain change is shown in Figure 2-9 and 2-10 respectively. The flowchart of the DSP-DGT technique is described in Figure 2-11.
2.5 DSP Hardware Structures for the DSP-DGT Algorithm

The following sections describe the DSP hardware structure adopted to implement the algorithm.

2.5.1 Digital Calibration Signal Pattern Generator

In order to calibrate the delay between the reference path and the feedback path signals, signal cross-correlation hardware is employed in the described algorithm. As a part of the cross-correlation operation, a digital calibration signal is applied as the reference input signal. This results in a corresponding feedback signal through the transmit path. Signal cross-correlation between the reference path and the feedback path signals is estimated based on which the group delay is estimated. Figure 2-12 shows the hardware used to generate the digital calibration signal by using a linear feedback shift register topology.

The DSP hardware uses a 6 stage flip flop bank. The circuit consists of flip flops with load capability as shown in Figure 2-12. An initial binary value is loaded into the flip flop. As described in [72] for a 6 stage linear feedback shift register, the output of the 6th and the 5th flip flop is fed back to an XOR gate. The output of the XOR gate feeds the 1st flip flop. The output of each flip flop is tapped serially by using a multiplexer which is controlled by a clock signal which is operating at 6 times faster than the flip flop clocks. This results in tapping out the output as a 6 bit word serially as shown in Figure 2-14.

2.5.2 Digital Sample Rate Adjust Logic

In the described DSP-DGT algorithm, it is essential to bring the forward path signal and the feedback path signal to the same sample rate before cross-correlation is estimated. In our system architecture, we assume that the sample rate of the ADC present in the feedback path higher than the forward path signal. Hence, to
downsample the forward path signal downsample hardware is required. The DSP hardware with programmable downsample factor is shown in Figure 2-15. The circuit adopted consists of a modulo- \( N \) counter, (where \( N \) is the downsample ratio), a multiplexer, a flip-flop and a couple of comparators. As shown in Figure 2-15, when the output of the counter reaches 0, a control signal is generated and used to control the multiplexer which pipes in the input data into the flip flop, when the control signal is 0, and then the current data sample is held. This repeats the data at the output of the flop and hence performs downsample operation by losing every \( N \) samples.

### 2.5.3 Magnitude Estimator

The signal magnitude of the forward reference path is estimated by the fast magnitude estimator circuit [73]. This is a linear approximation to the vector-magnitude problem that requires determining which of the orthogonal vector, I or Q, has greater absolute value. If the maximum absolute value of I or Q is designated by Max and the minimum value of either I or Q is designated as Min, an approximation of \(|Mag(I, Q)|\) is expressed as

\[
|Mag(I, Q)| = a \text{Max} + b \text{Min} \quad (2-12)
\]

There are several pairs for \( a \) and \( b \) constants that provide varying degrees of vector-magnitude approximation accuracy to within 0.1dB [73]. If I and Q are the in-phase and quadrature phase signals, then the magnitude of the I and Q is represented by

\[
Mag(I, Q)_\text{est} = \sqrt{I^2 + Q^2} = a \text{max}(|I|, |Q|) + b \text{min}(|I|, |Q|) \quad (2-13)
\]

The DSP implementation of the fast magnitude estimator is shown in Figure 2-20. The adopted hardware structure is a combinational logic and designed without any multiplier to make the area smaller. The adopted structure includes shift registers and
adders and hence reduces digital gate area. The DSP hardware designed for this purpose consists of the following four individual blocks.

**Absolute value estimation.** The hardware to calculate the absolute value is implemented as described below. Assume that the signal $x(n)$ is a 14-bit signed number represented as $<14, 0, t>$ (14 bits, 0 integers and 1 sign bit). The digital hardware takes in the signed number and if the sign bit is set, then number is inverted and incremented by 1.0, else the same signed number is sent at the output.

**Bitwise compare.** The DSP hardware for bitwise compare is described in Figure 2-19. The input signal which has to be compared is subtracted and the most significant bit (MSB) is extracted and used to control a multiplexer. If the MSB is set to 1, then the output of the multiplexer is $\text{abs}(I)$ which the maximum of the two numbers is, else if the MSB is zero, then the multiplexer outputs $\text{abs}(Q)$.

**Multiplication and Division By $\alpha$ and $\beta$.** The multiplication by factors are implemented by shift right or shift left logic. In our case, the values for $\alpha$ and $\beta$, we selected are $\alpha = \frac{61}{64} = \frac{64+1}{64}$ and $\beta = \frac{12}{32} = \frac{32+0}{32}$. The multiplication by $\alpha = \frac{61}{64}$ and $\beta = \frac{12}{32}$ can be realized by representing 61 as

$$
\alpha = \frac{61}{64} = \frac{(60 + 1)}{64} = \frac{(5 \times 2 \times 2 \times 3)}{64} = \frac{(4 \times (4 + 1) \times (2 + 1))}{64}
$$

and

$$
\beta = \frac{12}{32} = \frac{(4 \times 3)}{32} = \frac{(4 \times (2 + 1))}{32}
$$

Multiplication by 4 is implemented by shifting the input signal left by 2, and multiplication by $(4+1)$ can be implemented by again shifting the input signal left by 2 and adding the signal to it as shown in the Figure 2-20. Division of a number by 64 and 32 is realized by
shifting the input signal right 6 and 5 respectively. Let $I$ and $Q$ be uniformly distributed random signals with mean 0 and variance of 0.335. The magnitude of $I$ and $Q$ is estimated by the above hardware.

$$\text{Mag}(I, Q)_{\text{est}} = \sqrt{I^2 + Q^2} = \frac{61}{64} \max(|I|, |Q|) + \frac{12}{32} \min(|I|, |Q|) \quad (2-14)$$

Figure 2-21 shows the ideal signal magnitude and the estimated signal magnitude. If the ideal magnitude is defined by $|\text{Mag}(I, Q)|_{\text{ideal}}$ and the estimated signal magnitude is defined by $|\text{Mag}(I, Q)_{\text{est}}|$, then the Magnitude error is calculated by

$$\text{Mag-error} = \frac{(|\text{Mag}(I, Q)|_{\text{ideal}} - |\text{Mag}(I, Q)_{\text{est}}|)^2}{(|\text{Mag}(I, Q)|_{\text{ideal}})^2} \quad (2-15)$$

The plot of $\text{Mag-error}$ is shown in the Figure 2-21 for 1000 samples of $I$ and $Q$ random vector. The DSP-DGT algorithm requires block based magnitude estimation rather than instantaneous magnitude. Depending on the size of the input buffer, the magnitude estimator calculates the signal magnitude and updates the register at every block rate. Figure 2-22 shows the magnitude of quantized $I$ and $Q$ samples of 12 bits each. Also, shown in Figure 2-22 is the estimated block magnitude for every 200 sample buffer length. The block-based magnitude estimation error is found to be within the system specification of 0.08dB. The simulations show the magnitude error in dB for 5 consecutive buffers of 200 samples of $I$ and $Q$ signals is within the desired specifications. The simulation shows that the magnitude error reduces with increase in buffer sizes. Hence, the selection of the buffer sizes based on the signal variances is an important aspect of this system topology. Simulations show that as the buffer size increases, the error in magnitude estimation decreases. Hence depending on the loop
operating sample rate and the rate of adaptation, an appropriate buffer size can be chosen.

2.5.4 Fast Exponential Averager

The fast average DSP hardware employs an exponential averaging technique. The hardware is used to estimate the magnitude of the digital I channel and Q channel signals. Although other types of signal averaging techniques exists [37],[44],[50], the primary reasons for adopting this structure to perform fast average are

1) Capability to vary the amount of noise reduction and the response time by changing the value of the filter factor.
2) Easy to implement with one or two flip flops, shift registers and an adder.

The system block diagram of the adopted exponential averager is shown Figure 2-24. The input \( x(n) \) is scaled by a factor \( a \), known as the filter factor. The multiplied input is added to the delayed version of output scaled by \( (1-a) \) as expressed in Equation 2-17. By adopting this structure depending on the variance of the input signal, the final average estimate is either made dependent on the last averaged sample or on the new input sample by selecting proper values of \( a \). Assuming that the value of \( a \) must be within 0 and 1, if the value chosen for \( a \) is close to 0, then the output average estimate is more dependent on the past average estimate else it is more dependent on the new input sample.

\[
y(n) = ax(n) + (1-a)y(n-1)
\]  
(2-17)

To estimate the transfer function, we take \( z \) transform.

\[
Y(z)[1-(1-a)z^{-1}] = aX(z)
\]

\[
Y(z) = \frac{a}{X(z)} \frac{1}{1-(1-a)z^{-1}}
\]  
(2-16)
The transfer function reveals that the system has no zeros and clearly shows that it is a low pass filter. The value of the filter factor decides the settling time of the filter and also the amount of noise reduction. The smaller the value of $a$, the more noise reduction is obtained. However, with smaller values of $a$, the averager responds slower. Hence the trade-off of this structure is that the more noise reduction we need, the more sluggish the averager will respond. The following plot describes the settling time of the averager to a random varying input signal whose mean is 0.195. The signal-noise (SNR) performance of the averager as a function of the filter factor $a$, can be described as [73]

$$\frac{\text{Filter Output noise Variance}}{\text{Filter Output noise Variance}} = \text{SNR} = \frac{a}{2 - a} \quad (2-17)$$

Due to the above mentioned trade-offs between settling time and SNR, a more appropriate method of varying the filter factor has been described as follows. A relatively large filter factor is used at the beginning of the measurement so that the averager immediately responds to the filter’s input and then the filter factor is reduced slowly to improve noise performance of the averager. The filter factor can be reset to zero at the end of every signal transmission. This is illustrated in Figure 2-26 for a random input signal with mean of 0.195. Figure 2-26 illustrates the use of the varying filter factor in the exponential averager. A higher filter factor is used at the start of measurement, and the value is decreased as the measurement proceeds. This results in faster averager response time at the start of the measurement and as the measurement proceeds the averager is slowed down by using a lower filter factor for better noise reduction. The frequency response of the single stage averager is illustrated in Figure 2-27. The bandwidth of the averager reduces as the filter factor
reduces. This means that the step response of the averager has a slower response time at lower filter factors.

An alternate strategy that can be adopted is by having a two stage filter structure with timer enables. The first filter is enabled at time \( t_1 \) with a filter factor, \( a \) and after the filter settles, a second filter is enabled at time \( t_2 (t_2 > t_1) \) with a filter factor \( b \). This cascade architecture will also help in meeting the response time and noise trade-offs. Once the first filter settles, the second filter will be enabled to reduce the variance at the first filters output. The block diagram is illustrated in Figure 2-28.

The input-output equation of the second filter is represented as

\[
y_2(n) = by(n) + (1-b)y_2(n-1)
\]  

(2-18)

Applying z transform, the transfer function of the cascade is represented by

\[
\frac{Y_2(z)}{X(z)} = \frac{a*b}{[1-(1-a)z^{-1}][1-(1-b)z^{-1}]} 
\]  

(2-19)

Equation 2-19 shows that the filter output is a function of the two filter factors \( a \) and \( b \).

This structure helps in better average estimate if the input signal has relatively higher variances. The output of the second averager is shown in Figure 2-29.

2.5.5 Digital PID controller

The hardware implementation of the PID controller is shown in Figure 2-30. This circuit is used to integrate the error signal between the reference path and the feedback signal path and the controller output is used to adjust the digital or the analog gain stage of the transmit path. If \( e(n) \) is the input to the controller and \( K_p, K_i \) and \( K_d \) are the proportional, integral and derivative gain, then the output of the controller, \( p(n) \) is represented as
\[ p(n) = [e(n) \cdot K_p] + \left[ e(n) \cdot K_i \cdot \left( \frac{z^{-1}}{1 - z^{-1}} \right) \right] + \left[ e(n) \cdot K_d \cdot (1 - z^{-1}) \right] \] (2-20)

The PID controller is implemented with three adders and two flip flops clocked at the desired sample rate. To avoid the use of multipliers, the integral, derivative and the proportional gain stages are implemented by shift add depending on the required gain values. The DSP hardware segment for the gain blocks are shown in the Table 2-2 and Figure 2-31. The integral, proportional and derivative gains for the PID controller are implemented based on shift and add logic [24]. For a gain of -6dB, the signal is shifted right by a factor of 2 and for a gain of -8.53dB, the signal is separately shifted right by 4 and shifted right by 8 and then added together to get -8.53dB. Depending on the 4 bit signal gain_cont<4>, the required gain values are selected and applied to the input signal. The values of the shift and the combination of the additions can be changed to get different desired gain values.

2.5.6 Cross-Correlator Hardware

Before the gain tracking algorithm is enabled, it is essential to calibrate the delays between the forward and the feedback path. Calibration of the delay will help in aligning the feedback and the reference path signals. In addition it will help to preserve loop stability and enhance the settling time of the algorithm. As a first step, a calibration signal is fed into the digital path and the cross-correlation between the outputs of the forward path signals and the feedback path signals due to the calibration signal is estimated. The time of occurrence of the maximum correlation estimate is dynamically found by the time-delay counter and based on the time index estimate the delay is calculated with the knowledge of the operating sample rate. This calculated delay is then applied to the reference path delay buffer as shown in the Figure 2-7. If \( x(n) \) is the
To calibrate the delay buffer, a known calibration signal can be used before the actual gain tracking algorithm. The hardware to generate the calibration signal was described in section 2.5.12 and shown in the Figure 2-13. Also, as an alternate strategy, depending on the type of modulation employed, the actual transmitted signal can be used to dynamically calibrate the delay buffer by finding the cross-correlation between the forward path and the feedback signals.

The implemented digital DSP hardware structure for the \( k = 12 \) sample lag correlator is shown in Figure 2-32. The digital circuit consists of delay logic, multipliers, adders and multiplexers. The input signal \( x(n) \) from the reference path passes through a bank of delay registers clocked at the sampling frequency \( F_s \). The reference path signals \( x(n), x(n-1), \ldots x(n-k) \) are then simultaneously multiplied by the feedback signal \( y(n) \), which will be delayed and the scaled version of the reference path signal. The outputs of the respective multipliers are denoted as \( x(n-k)y(n) \) corresponding to the respective signal lag \( k \). Each of the multiplier outputs is accumulated over \( M \) sample to result in the signal \( R_{xy}(k) = \sum_{n=0}^{M-1} x(n-k)y(n) \). The output is then scaled by \( \frac{1}{M} \) which is implemented by a shift right block. The final output values of each of the signal lags are latched into flops and stored. The latched values are then used by the
software code and the correlation index corresponding to the maximum value is estimated. Thus, the maximum correlation index $k_{\text{max}}$ can be estimated as follows

$$k_{\text{max}} = \max(R_x y(k)) = \max(\sum_{n=0}^{M-1} x(n-k)y(n)) \quad (2-22)$$

The estimated delay index $\frac{k_{\text{max}}}{F_s}$ is the calibrated feedback path delay at the instant of maximum correlation as shown in the simulations. The detailed DSP hardware structure adopted for a 12 tap cross-correlator [17-19],[25] is shown in Figure 2-32. The corresponding multiplexer logic is shown in Table 2-3. The assumption of this correlation approach is to use either a calibration signal generated from the random signal generator hardware or to use the actual transmit signal by itself. These two approaches are simulated and the results are presented in the following sections.

2.5.6.1 Simulations with the cross-correlation DSP hardware

Figure 2-33 shows the calibration signal (blue) and the feedback signal (in red). The calibration signal in the reference path is delayed at every clock cycle and the correlation estimate is calculated. The size of the correlator is decided based on the maximum expected lag based on system simulation and the application. The delay tracking counter keep track of the time at which the maximum correlation estimate occurs and based on the sampling frequency, the delay estimate is calculated corresponding to the maximum estimate. This delay estimate is then applied to the delay buffer to align the forward and feedback paths.

Figure 2-34 shows the correlation estimate at the output of correlator based on system simulations. Apart from using the calibration signal to detect the delay between the forward path and the feedback paths, we can exploit the correlation properties of the
baseband signal and perform dynamic cross-correlation to estimate the delay between the reference and the feedback signal paths. Hence, depending on the type of modulation schemes used, the baseband signal can be adopted and the cross-correlation between the forward path and the feedback path signals can estimated to calibrate the delay dynamically.

Figure 2-35 shows a buffer of 120 samples of baseband signal envelope. The data is simulated from a typical WCDMA channel case according to the mobile device specifications. The sample rate is 62.4MHz and each of the buffer size is 120 samples, which is about 1.92usec of data. As described in earlier sections the baseband analog signal passes through the RF mixer, amplified by the PA and transmitted at the output of the mobile device. The transmitted RF power output is feedback through the power detector as described in earlier sections.

The detected power from the PA is feedback through the analog gain stages and sampled with the ADC depending on the sample rate selected. Figure 2-36 shows the detected signal at the output of the ADC. This signal can be assumed as a delayed and scaled version of the baseband signal envelope as the feedback signal passes through an envelope detector and gets scaled by feedback gains. Figure 2-37 shows the signal cross-correlation between the baseband signal envelope and the detected signal. Signal correlation is performed between the block of the baseband signal envelope and the delayed and the scaled feedback signal. The correlation index results in peak estimate when the signal pattern overlaps. Based on the signal correlation estimate, the delay between these two paths is estimated. Figure 2-38 shows the gain and time aligned version of the detected and the reference baseband signal envelope. The estimated
time delay can be employed in any of the conventional system architecture or integrator based closed-loop power control architecture. The red curve in Figure 2-38 is the baseband signal envelope and the blue curve is the gain scaled and time aligned detected signal after delay and gain estimation. This shows accurate prediction of the delay and gains based on the signal correlation algorithm.

2.5.6.2 Correlation estimates at varying sample rates

Depending on the operating rates of the ADC, the detected signal has to be downsampled before performing signal correlation. The difference in the operating sample rates between the reference path and the feedback path will alter the correlation estimate. Hence for desired correlation accuracy there will be a limitation placed on the downsample limit. The digital logic circuit described in section 2.5.2 shows how the reference signal is downsampled. Hence the sample rates of either the forward path signal or the feedback path signal will be adjusted before estimating the correlation. Figure 2-39 – 2-42 illustrates the performance of the correlation circuit at different downsample rations of 2, 5, 10, 15 and 20.

If $x(n)$ is the forward path signal at sample rate $F_s$ and $y(n)$ is the feedback path signal at sample rate $\frac{1}{N}F_s$, then the factor $N$ is the oversampling/downsampling factor. In these situations, the sample rates of the signals are adjusted to be the same before the correlation is estimated. If $x(n)_N$ denotes the signal $x(n)$ downsampled by $N$, and $y(n)$ is the feedback signal, then the correlation estimate between the downsampled $x(n)$ and $y(n)$ is represented as

$$R_{x_N,y}(k) = \frac{1}{M} \sum_{n=0}^{M-1} x(n-k)y(n), \text{ where } k = 0, \ldots, M-1 \quad (2-23)$$
Simulations reveal that we can derive normalized cross-correlation estimate even with sample rate differences of 1/20 between the baseband signal envelope and the feedback signal. Based on the signal correlation estimate, the peak of the signal and hence the delay between the baseband and the feedback signal can be calculated.

### 2.6 Top Level System Simulations and Measured Lab Results

#### 2.6.1 System Simulations

System simulations for the DSP-DGT algorithm have been performed in Matlab and fixed point digital tools known as Signal Processing Workstation (SPW). The detailed system parameters and simulation conditions are as follows:

1. Baseband analog system models such as baseband filters, DAC with quantization and noise models [20],[21].
2. Digital fixed point filter models for the pulse shaping and multi-rate digital filter stages.
3. Phase noise models for the voltage controlled oscillators.
4. Power amplifier and RF discrete driver amplifier model with non-linear ties such as 1dB compression point, third and second intercept products.
5. Measured data of power detectors, PA and driver amplifier including slope variations based on temperature and frequency of operation.
6. Phase and gain variation response for the analog RF circuitry.
7. Digital fixed point models for the described DSP hardware.
8. Different modulation formats as input signals such as GSM, WCDMA, EDGE[36] and OFDM[15].

Figure 2-43 shows the magnitude of the reference path signal $x(n)$ in blue and the magnitude of the feedback signal $y(n)$ with injected gain variation of +6dB. The mean of the reference signal is shown in black. As shown in Figure 2-46, the closed-loop system can track for gain variations and compensate for the positive gain variation.
Figure 2-44 shows the response of the closed-loop system which tries to compensate for the positive 6dB gain variation injected into the system. The error signal between the reference path and the feedback signal magnitude is calculated and the controller is updated based on the buffer rate selected. The rate of change of the error signal, the peak overshoot and the steady state error is decided by the selected integral, derivative and proportional gains. This controller output is either digitally applied to the forward path signal or converted to an analog equivalent signal and applied as gain control on to the RF amplifier stages as bias control. Figure 2-45 shows the response of the closed-loop system for a single gain step as a function of integral gains. The philosophy adopted in the described DSP-DGT algorithm is to fix the derivative and the proportional gains and vary the integral gains as a function of variance of the error signal, the desired settling time and desired steady state error. Figure 2-46 shows the convergence of the closed-loop system to track out a positive 6dB gain variation injected into the system. As the closed-loop system is enabled, the averaged value of the error signal between the reference path and the feedback path is inputted into the controller. As shown in earlier equations at steady state the controller output provides a compensation signal in response to the sign of the error signal. In this simulation, a 6dB gain variation is added onto the feedback path and hence this provides a negative error signal. The negative error signal input into the controller make the controller output provide a compensation signal which tries to bring the error back to zero at steady state. The controller update is shown in Figure 2-44 brings back the signal power to the desired level as shown in Figure 2-46.
2.6.2 Mobile Testing and Lab Measurements

In order to measure the transmit power at the output of the RF IC, the mobile IC is mounted on a 7 layer evaluation radio board. The transmit RF ports are connected to communication testing equipments to measure the signal power. In order to measure the digital signal, a signal oscilloscope is used. Digital test ports which are present on the mobile are connected to the digital oscilloscope and the internal reference signals are used as trigger to perform single shot capture. National Instrument's LabView [81] is the software tool which was used to send commands to the RF IC that will mimic the baseband processor and the base-station controller. This software is installed to the computer and the evaluation board was connected to the computer using a Universal Serial Bus (USB) interface. Figure 2-49 describes the interface between the mobile IC, the external PA, the computer and the testing equipments.

The digital controller outputs are converted to analog signal by either an internal or an external DAC and the applied as bias voltages for the PA. The analog signals are captured by an analog oscilloscope and the RF power is monitored by using communication testing equipments. The make and the model numbers of communication testing and measurement equipments used in this work are:

- Rhode and Schwartz (R&S) CMU200 Universal Radio Communication Tester [79]
- Rhode and Schwartz (R&S) FSQ Signal Analyzer [80]
- Tektronix TDS3034B Oscilloscope [83].
- Agilent N9020A MXA signal analyzer [82].

Figures 2-50 to Figure 2-53 captures the measured analog signal at the output of the loop controller. This signal is applied as a bias control signal either to the PA or the VGA.
to provide gain control depending on the adopted transmit path architecture. In other applications, the digital controller output is used to alter the digital gain of the transmit signal path. Figure 2-54 shows the measured output of the mobile device (using FSIQ testing equipment) whose RF power changes from a lower power level to 22dBm employing the DSP-DGT algorithm. It is clear from Figure 2-54 that the rate of change of signal power ramp is determined by the controller gains used. Depending on the application and based on the peak overshoot and steady state error requirements, the controller gains are selected. In addition of dynamic absolute gain tracking this circuit can also be used to perform a power change as will be described in Chapter 4.

2.7 Summary

1. The DSP-DGT technique provides gain monitoring and compensation of absolute power variations in mobile devices due to imperfections introduced due to analog and RF circuits inside a mobile device.

2. System simulations and lab measurements show that the algorithm is provides gain control better than 0.1dB accuracy

3. Approximate gate count of the implementation is within the allotted 22K.

4. The described approach does not require separate reference generation circuitry as the base band signals are used as self reference.

5. The implemented algorithm is found to be independent of modulation schemes employed.

6. This technique however does not compensate for relative gain and phase error introduced by RF circuits which will be dealt in Chapter 3
Figure 2-1. Primary sections of a mobile device transmitter

Figure 2-2. Absolute RF Power variation in dB due to temperature variations averaged over three parts
Figure 2-3. Pout variations across frequency bands over temperature

Figure 2-4. Absolute RF power variations in dB due to frequency of operation
Figure 2-5. Pout variations across frequency bands over supply voltage
Figure 2-6. System level block diagram of the DSP-DGT architecture
Figure 2-7. Controller adopted for the closed-loop DSP-DGT algorithm
Figure 2-8. Second-order closed-loop PID controller
Figure 2-9. Closed-loop dynamics when the controller compensates for undesired positive gain change
Figure 2-10. Closed-loop dynamics when the controller compensates for an undesired negative gain change
Enable digital clocks
Set the digital baseband gain to be $D_1$

Enable calibration generator and send signal into I channel and the Q channel

Set RF upconversion frequency to be $WT_x$

1) Enable cal_enable signal
This forces the calibration signal into the I channel and the Q channel
This cuts off any signal into the reference path.
2) Enable Power detector
3) Enable ADC
4) Enable Cross correlator hardware
5) Enable magnitude estimator

Estimate Cross Correlation between reference path $x(n)$ and feedback path signals $y(n)$

$$R_{xy}(k) = \frac{1}{M} \sum_{n=0}^{M-1} x(n-k)y(n)$$

Detect peak of correlation and apply the delay in the reference path to align feedback and reference path signals

1) Disable cal_enable signal
2) Start Transmission of data bits into I and Q channels, depending on modulation
3) Disable cross correlator path
4) Enable signal averager DSP hardware
5) Enable Controller after programming nominal loop gains

Control timing accurately for average enables and loop update rate.
1) Loop can update every sample
2) Loop can update every $M$ samples

Loop adapts and Additional disturbances are tracked and hence gain dynamic gain compensation is performed as loop error signal goes to zero

Figure 2-11. Flow chart of the steps involved in the DSP-DGT algorithm
Figure 2-12. Linear Feedback shift register for a 6 tap pseudo random signal generator

Figure 2-13. Timing signal to generate 6 times faster sample rate at the output
Figure 2-14. Output pseudo random bit stream from a 6 tap linear feedback shift register.
Figure 2-15. DSP implementation of sample rate logic

Figure 2-16. In-phase and quadrature phase signal swings whose magnitude has to be estimated.
Figure 2-17. Instantaneous error (linear) vs. input signal swing function as a function of \( \alpha \) and \( \beta \) factors

Figure 2-18. Simple absolute value estimator logic
Figure 2-19. Digital DSP hardware structure for magnitude comparator
Figure 2-20. Digital DSP hardware structure for the magnitude estimator
Figure 2-21. System simulations with quantized I and Q random signals and mean error in estimation.
Figure 2-22. Ideal and obtained signal magnitude

Figure 2-23. Magnitude error in dB as a function of buffer hardware length
Figure 2-24. DSP structure of the exponential averager

Figure 2-25. Settling times of the averager as a function of filter factor
Figure 2-26. Dynamic varying filter factor depending for noise and response time trade-offs.

Figure 2-27. Magnitude response of the averager
Figure 2-28. Cascaded structure for the fast average circuit

![Cascaded structure for the fast average circuit](image)

Figure 2-29. Output of second filter vs. time in sec

![Output of second filter vs. time in sec](image)
Figure 2-30. DSP structure for PID controller with programmable gains

\[ P(s) = (s \cdot E(s) \cdot K_D) + KpE(s) + \frac{1}{s}K_iE(s) \]

Figure 2-31. Controller gain programming hardware
Figure 2-32. Digital implementation of 12 taps cross-correlation DSP hardware
Figure 2-33. Cross-Correlation of calibration signal

Figure 2-34. Simulation to show the correlation estimate between the calibration signal and the feedback signal
Figure 2-35. Signal buffer of baseband signal envelope

Figure 2-36. Detected Signal at the output of the ADC at the signal sample rate (no downsampling)
Figure 2-37. Normalized signal correlation between baseband signal envelope and detected signal.

Figure 2-38. Time aligned gain scaled baseband signal envelope and detected signal.
Figure 2-39. Correlation estimate of baseband signal envelope and feedback signal with downsample ratio of N=2

Figure 2-40. Correlation estimate of baseband signal envelope and feedback signal with downsample ratio of N=5

Figure 2-41. Correlation estimate of baseband signal envelope and feedback signal with downsample ratio of N=10
Figure 2-42. Correlation estimate of baseband signal envelope and feedback signal with downsample ratio of N=20

Figure 2-43. Simulation to show injected 6dB gain variation and the reference signal level
Figure 2-44. Simulation to show the controller output adaptation for a positive 6dB gain variation in multiple steps

Figure 2-45. Simulation to show the closed-loop response with respect to different integral gains for a positive 6dB gain variation
Figure 2-46. Simulation of the closed-loop circuitry adaptation until error signal becomes zero.

Figure 2-47. Simulation to show the controller correction for +6dB, +5.5dB and -6.5dB gain variation.
Figure 2-48. Simulation to show the controller output to track for +10dB, +3.5dB and -5.5dB gain variation.

Figure 2-49. System interface for mobile device testing
Figure 2-50. Analog version of the controller compensation by multiple steps to reach to the desired power as captured by Tektronix oscilloscope

Figure 2-51. Analog version of the controller compensation by a single step to reach to the desired power level captured by Tektronix oscilloscope
Figure 2-52. Analog response of the controller output shows oscillations due to the higher value of integral gains captured by the Tektronix oscilloscope.

Figure 2-53. Analog response of the controller output shows an over-damped condition due to the lower value of integral gains captured by the Tektronix oscilloscope.
Figure 2-54. Measured (FSIQ) plots of RF output at the power amplifier output as a function of controller gains
| time index | alpha*max(|I|,|Q|)  | beta*min(|I|,|Q|)  | ideal magnitude | a=61/64,b=12/32 | a=15/16,b=15/32 | a=122/128,b=31/32 | a=31/32,b=12/32 |
|------------|--------------------|--------------------|----------------|----------------|----------------|------------------|------------------|
| 0          | 0.952892           | 9.16E-05           | 0.999755       | 0.952984       | 0.937386       | 0.952991         | 0.937363         |
| 1          | 0.771094           | 0.220419           | 1              | 0.991514       | 1.033978       | 1.009882         | 0.978873         |
| 2          | 0.906476           | 0.115881           | 1              | 1.022357       | 1.036467       | 1.032014         | 1.007497         |
| 3          | 0.906476           | 0.115881           | 1              | 1.022357       | 1.036467       | 1.032014         | 1.007497         |
| 4          | 0.771094           | 0.220419           | 1              | 0.991514       | 1.033978       | 1.009882         | 0.978873         |
| 5          | 0.952892           | 9.16E-05           | 0.999755       | 0.952984       | 0.937386       | 0.952991         | 0.937363         |
| 6          | 0.771094           | 0.220419           | 1              | 0.991514       | 1.033978       | 1.009882         | 0.978873         |
| 7          | 0.906476           | 0.115881           | 1              | 1.022357       | 1.036467       | 1.032014         | 1.007497         |
| 8          | 0.906476           | 0.115881           | 1              | 1.022357       | 1.036467       | 1.032014         | 1.007497         |
| 9          | 0.771094           | 0.220419           | 1              | 0.991514       | 1.033978       | 1.009882         | 0.978873         |
| 10         | 0.952892           | 9.16E-05           | 0.999755       | 0.952984       | 0.937386       | 0.952991         | 0.937363         |
### Table 2-2. Signal gain implementation

<table>
<thead>
<tr>
<th>shift right factor</th>
<th>linear gain</th>
<th>dB gain</th>
<th>$M_3M_2M_1M_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0.5</td>
<td>-6.0206</td>
<td>1</td>
</tr>
<tr>
<td>(1/2+1/4)</td>
<td>0.75</td>
<td>-2.49877</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>0.25</td>
<td>-12.0412</td>
<td>3</td>
</tr>
<tr>
<td>(1/4+1/8)</td>
<td>0.375</td>
<td>-8.51937</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>0.125</td>
<td>-18.0618</td>
<td>5</td>
</tr>
<tr>
<td>(1/8+1/16)</td>
<td>0.1875</td>
<td>-14.54</td>
<td>6</td>
</tr>
<tr>
<td>16</td>
<td>0.0625</td>
<td>-24.0824</td>
<td>7</td>
</tr>
<tr>
<td>(1/16+1/32)</td>
<td>0.09375</td>
<td>-20.5606</td>
<td>8</td>
</tr>
<tr>
<td>32</td>
<td>0.03125</td>
<td>-30.103</td>
<td>9</td>
</tr>
<tr>
<td>(1/32+1/64)</td>
<td>0.046875</td>
<td>-26.5812</td>
<td>10</td>
</tr>
<tr>
<td>64</td>
<td>0.015625</td>
<td>-36.1236</td>
<td>11</td>
</tr>
<tr>
<td>(1/64+1/128)</td>
<td>0.0234375</td>
<td>-32.6018</td>
<td>12</td>
</tr>
<tr>
<td>128</td>
<td>0.0078125</td>
<td>-42.1442</td>
<td>13</td>
</tr>
<tr>
<td>(1/128+1/256)</td>
<td>0.01171875</td>
<td>-38.6224</td>
<td>14</td>
</tr>
<tr>
<td>256</td>
<td>0.00390625</td>
<td>-48.1648</td>
<td>15</td>
</tr>
<tr>
<td>Mux selection</td>
<td>Xcorr_out&lt;4&gt;</td>
<td>$B_3 B_2 B_1 B_0$</td>
<td>$R_{xy}(k)$</td>
</tr>
<tr>
<td>---------------</td>
<td>--------------</td>
<td>---------------------</td>
<td>--------------</td>
</tr>
<tr>
<td>MuxA 0</td>
<td>0</td>
<td>0000</td>
<td>$\sum_{n=0}^{M-1} x(n) y(n)$</td>
</tr>
<tr>
<td>MuxA 1</td>
<td>0</td>
<td>0001</td>
<td>$\sum_{n=0}^{M-1} x(n-1) y(n)$</td>
</tr>
<tr>
<td>MuxA 2</td>
<td>0</td>
<td>0010</td>
<td>$\sum_{n=0}^{M-1} x(n-2) y(n)$</td>
</tr>
<tr>
<td>MuxA 3</td>
<td>0</td>
<td>0011</td>
<td>$\sum_{n=0}^{M-1} x(n-3) y(n)$</td>
</tr>
<tr>
<td>MuxB 4</td>
<td>0</td>
<td>0100</td>
<td>$\sum_{n=0}^{M-1} x(n-4) y(n)$</td>
</tr>
<tr>
<td>MuxB 5</td>
<td>0</td>
<td>0101</td>
<td>$\sum_{n=0}^{M-1} x(n-5) y(n)$</td>
</tr>
<tr>
<td>MuxB 6</td>
<td>0</td>
<td>0110</td>
<td>$\sum_{n=0}^{M-1} x(n-6) y(n)$</td>
</tr>
<tr>
<td>MuxB 7</td>
<td>0</td>
<td>0111</td>
<td>$\sum_{n=0}^{M-1} x(n-7) y(n)$</td>
</tr>
<tr>
<td>MuxC 8</td>
<td>0</td>
<td>1000</td>
<td>$\sum_{n=0}^{M-1} x(n-8) y(n)$</td>
</tr>
<tr>
<td>MuxC 9</td>
<td>0</td>
<td>1001</td>
<td>$\sum_{n=0}^{M-1} x(n-9) y(n)$</td>
</tr>
<tr>
<td>MuxC 10</td>
<td>0</td>
<td>1010</td>
<td>$\sum_{n=0}^{M-1} x(n-10) y(n)$</td>
</tr>
<tr>
<td>MuxC 11</td>
<td>0</td>
<td>1011</td>
<td>$\sum_{n=0}^{M-1} x(n-11) y(n)$</td>
</tr>
</tbody>
</table>
Table 2-3. Continued

<table>
<thead>
<tr>
<th>Mux selection</th>
<th>$X_{\text{corr_out}&lt;4&gt;}$</th>
<th>$B_3B_2B_1B_0$</th>
<th>$R_{xy}(k)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>MuxD</td>
<td>12</td>
<td>1100</td>
<td>$\sum_{n=0}^{M-1} x(n-12)y(n)$</td>
</tr>
<tr>
<td>NA</td>
<td>13</td>
<td>1101</td>
<td>NA</td>
</tr>
<tr>
<td>NA</td>
<td>14</td>
<td>1110</td>
<td>NA</td>
</tr>
<tr>
<td>NA</td>
<td>15</td>
<td>1111</td>
<td>NA</td>
</tr>
</tbody>
</table>
CHAPTER 3
DSP BASED DYNAMIC ESTIMATION AND COMPENSATION OF DIFFERENTIAL GAIN NONLINEARITY AND RANDOM PHASE SHIFTS

3.1 Demands for Relative Gain and Phase Accuracy in Mobile Devices

Wireless communication devices employ multistage gain amplifiers and RF driver amplifiers to perform output power control in transmitters. Most of the wireless communication standards impose stringent requirements on the relative power accuracy and phase continuity specifications to enhance system capacity and signal quality. More specifically, wireless transmitters which adopt advanced communications standards such as CDMA 2000, WCDMA, LTE [31-34] require the output power accuracy specifications to be better than 0.2dB. This implies that when a transmit power change happens in a mobile system the final value of the desired power level must be within +/-0.2dB accuracy. In addition, it also requires the phase continuity specification to be within +/-3 degrees between adjacent transmissions. This implies that the phase variation of the signal carrier between consecutive RF step changes must be within +/-3 degrees.

These standard requirements [28-30] pose great challenges for any wireless device design and manufacturing. The relative power accuracy specifications help to maintain system capacity, and avoid signal interference from nearby users, while the carrier phase discontinuity specifications help to preserve signal quality and easier demodulation at the base-station receivers. The technique presented in this Chapter uses DSP circuits to estimate the relative gain error (Differential Nonlinear Error, DNLE) of the analog RF gain amplifier and compensate for the accumulated nonlinearities introduced. In addition, this Chapter also introduces a method to calibrate the carrier phase changes in which happens in a mobile device due to change in the capacitive
load impedances on the RF analog path. Along with the system architecture, this chapter also describes the corresponding DSP hardware implementation topologies, system simulations and measurement results. Figure 3-1 shows the block diagram of a wireless transmitter and the nodes at which the nonlinear impairments get added into the system which will degrade system performances. The phase changes associated in any high frequency wireless system can be either due to the phase shifts introduced by the RF modulators or due to phase response variations of the analog filters in the signal path. The phase variations are also a result of change in capacitive loads [16] during different stages of operation of any RF device. The presented technique is found to estimate and compensate for gain errors better than 0.1 dB accuracy and phase errors less than 1 degree accuracy.

3.2 Analytical Expressions for Non Linear Distortions in an Analog RF Device

Before we try to find a solution to compensate for gain and phase nonlinearities that originate in a RF analog circuit, it is important to understand the origin of nonlinear distortions and the distortion metrics to address the problems which are introduced into the system. Assume an RF amplifier used either in a mobile device or at the base-station that operates in a weakly nonlinear range. The input and output of any memoryless nonlinear system can be described by the following power series.

$$S_o = a_1S_i + a_2S_i^2 + a_3S_i^3 + a_4S_i^4 + \ldots$$  \hspace{1cm} (3-1)

where $S_o$ is the output of the system, $S_i$ is the input to the system and the coefficients $a_k$ are the $k^{th}$ order coefficients depending on the degree of system nonlinearity. These coefficients are independent of the input signal level but primarily a function of the
device bias characteristics [5], [10-13], [40]. The coefficient \( a_i \) is known as the small signal gain. For very small input signal levels, \( S_i \) the coefficient \( a_i \) dominates and the higher order terms are negligible. Assume the signal \( S_i = S_i \cos \omega t \) is the input to a non-linear system. The output of the non-linear system is defined by

\[
S_{\text{out}} = a_1 S_i (\cos \omega t) + a_2 S_i^2 (\cos^2 \omega t) + a_3 S_i^3 (\cos^3 \omega t) + \ldots \ldots \ldots \ldots (3-2)
\]

The second term \( a_2 S_i^2 (\cos^2 \omega t) \) is expanded as

\[
a_2 S_i^2 (\cos^2 \omega t) = a_2 S_i^2 \left( \frac{1}{2} [\cos(\omega_1 + \omega_2) t + \cos(\omega_1 - \omega_2) t] \right)
\]

\[
= a_2 S_i^2 \left( \frac{1}{2} [1 + \cos 2\omega_1 t] \right) \quad (3-3)
\]

The cubic term \( a_3 S_i^3 (\cos^3 \omega t) \) is expanded as

\[
a_3 S_i^3 (\cos^3 \omega t) = a_3 S_i^3 \left( \cos^2 \omega_1 t \cos \omega_2 t \right)
\]

\[
= a_3 S_i^3 \left( \frac{1}{2} \cos \omega_1 t + \frac{1}{4} [\cos 3\omega_1 t] + \cos \omega_1 t \right)
\]

\[
= a_3 S_i^3 \left( \frac{3}{4} \cos \omega_1 t + \frac{1}{4} \cos 3\omega_1 t \right) \quad (3-4)
\]

The first term in the Equation 3-4 is the fundamental and the second term is the third harmonic term which was generated by the device nonlinearity. This component appears at the output of the device at three times the input frequency. To analyze the sum total distortions caused in a transceiver it is also essential to better understand the 5\(^{th}\) order term as they determine the out of band spectrum emission requirements. More specifically, this is responsible for the spectrum leakage at alternate channels (2
channels away) due to a mobile user in a particular channel. The pentic term

\[ a_5 S_1^5 (\cos^5 \omega_t t) \] can be expressed as

\[ a_5 S_1^5 (\cos^5 \omega_t t) = (\cos^2 \omega_t t)(\cos^3 \omega_t t) \]

\[ = a_5 S_1^5 \left[ \left( \frac{3}{4} \cos \omega_t t + \frac{1}{4} \cos 3\omega_t t \right) \left( \frac{1}{2}[1 + \cos 2\omega_t t] \right) \right] \]

The output \( S_{o(d)} \) is represented by

\[ S_{o(d)} = a_1 S_1 (\cos \omega_t t) + a_2 S_1^2 (\cos^2 \omega_t t) + a_3 S_1^3 (\cos^3 \omega_t t) + \ldots \]

\[ = a_1 S_1 (\cos \omega_t t) + a_2 S_1^2 \left( \frac{1}{2}[1 + \cos 2\omega_t t] \right) + a_3 S_1^3 \left( \frac{3}{4} \cos \omega_t t + \frac{1}{4} \cos 3\omega_t t \right) + \ldots \ (3-5) \]

From the above analysis we observe the following

- The term \( a_i S_1 (\cos \omega_t t) \) is the desired term with the amplified /attenuated gain.
- The higher-order harmonics generate distortions and the coefficients are independent of the input signal.
- The second-order terms produces DC shift and hence an undesired DC value is added to the input signal. It is obvious from this observation that the even order terms generate a DC component.
- The third power [3] produces the fundamental term \( \omega_t \) and the third harmonic term, \( 3\omega_t \). The phase of the \( \omega_t \) is most important because it can produce a signal totally out of phase of the input desired signal and can cause undesired amplitude change of the output signal. Depending on the phase of this term it can generate either gain compression or gain expansion of the output signal.
- Taylor series expansion of an odd function \( f(-s) = -f(s) \) only has odd components, while an expansion of even functions \( f(-s) = f(s) \) generates DC components.
- The rate at which the first harmonic grows is slower than the second and the third harmonic.
In practice an amplifier used in transceivers will operate either in the linear region or within the 1dB compression point. Hence, Taylor series can be used for our analysis. Since the total output signal power is a function of power of the independent harmonics, it is important to understand the distortion metrics analytically, and it’s nonlinear effects on the desired signal power. Considering the second power term, the harmonic distortion \( HD_2 \) can be defined as

\[
HD_2 = \frac{\text{Amplitude of second harmonic}}{\text{Amplitude of the fundamental}}
\]  

Equation (3-6)

From expression Equation 3-4 we can calculate

\[
HD_2 = \frac{1/2 a_2 S_1^2}{a_1 S_1} = \frac{1}{2} \left( \frac{a_2}{a_1} \right) S_1
\]

Hence, it is obvious that \( HD_2 \) is proportional to the input signal level. \( HD_2 \) is an important factor in distortion analysis because it generates DC components which will degrade the signal quality unless eliminated.

Considering the third power term, the harmonic distortion component is described as

\[
HD_3 = \frac{\text{Amplitude of third harmonic}}{\text{Amplitude of the fundamental}}
\]  

Equation (3-7)

From expression (3-5) we can calculate

\[
HD_3 = \frac{a_3 S_1^3}{a_1 S_1} = \frac{1}{4} \left( \frac{a_3}{a_1} \right) S_1^2
\]

Equation (3-8)

The expression clearly shows that \( HD_3 \) is proportional to square of the input signal.

Considering the 5\textsuperscript{th} order term, the harmonic distortion due to the 5\textsuperscript{th} order term is defined as
\[ HD_5 = \frac{\text{Amplitude of fifth harmonic}}{\text{Amplitude of the fundamental}} \] (3-9)

From expression (3-6) we can calculate the total harmonic distortion (THD) as

\[ THD = \frac{\text{Power in the distortion}}{\text{Power in the fundamental}} = \sqrt{HD_2^2 + HD_3^2 + HD_4^2 + ..} \] (3-10)

The total harmonic distortion is equal to the square root of sum of square of independent harmonic distortions. Approximate THD requirements for certain applications are denoted in Table 3-1. The presence of these nonlinearities will cause relative gain and phase errors when changing power levels in a mobile device. These will dictate the need to perform gain and phase shift compensation to maintain relative power accuracy specifications and to perform accurate power control.

### 3.3 Reasons for Relative Power Level Accuracy Impairment

One of the primary impairments of the relative power level accuracy specifications is the DNLE associated with the high frequency RF and analog components [6],[8]. In any high frequency amplifiers, if \( G_{1g1} \) and \( G_{1g2} \) are the gains in dB of two successive stages of an amplifier and if \( G_{2g1} \) and \( G_{2g2} \) are the gains in dB of the same amplifier at different operating conditions (frequency bands of operation, voltage and temperature), then DNLE between the two gains stages is expressed as

\[
DNLE(g_1, g_2)(dB) = |(G_{1g1} - G_{1g2}) - (G_{2g1} - G_{2g2})| \] (3-11)

\[
DNLE(g_k, g_l)(dB) = |(G_{1gk} - G_{1gl}) - (G_{2gk} - G_{2gl})| \] (3-12)

These non-linear terms get accumulated and leads to integral gain error which are represented by integrated nonlinearity (INL). The INL for a \( n^{th} \) stage gain amplifier can be expressed as
\[ \text{INLE}(1,n)(dB) = \text{DNLE}(g_1,g_2) + \text{DNLE}(g_2,g_3) + \ldots + \text{DNLE}(g_{n-1},g_n) \text{ or} \]

\[ \text{INLE}(1,n)(dB) = \sum_{n} \text{DNLE}(g_{n-1},g_n) \]

(3-13)

where \( n \) is the desired stage up to which the nonlinearity is measured.

The INL leads to gain errors and degrades the relative power level accuracy unless compensated. Figure 3-2 shows measured gain changes of a 16 step RF amplifier with respect to low, mid and high frequency bands of operation and at room (25 degree), hot (85 degree) and cold (-30 degree) temperatures. The DNLE for a 16 stage amplifier is calculated based on the measured data as described in Equation 3-13. Figure 3-3 shows measured DNLE in dB for a 16 stage high frequency gain amplifier. The calculated DNLE are based on mid channel and room temperature as the reference. Any error from this ideal reference is attributed as DNLE. The red line in Figure 3-3 is the desired specification for the selected mobile application.

In addition, any gain variations due to temperature and supply voltage changes will add to the DNLE and will degrade the system power accuracy unless compensated. Tables 3-3 and 3-4 shows measured power level and the corresponding DNLE in dB for successive gain steps for a 16 stage high frequency amplifier. Figure 3-4 shows measured INLE curves for a 16 stage driver amplifier as a function of different frequency bands of operation. As shown in Figure 3-3 the DNLE associated with each step change is accumulated when the mobile device performs a power change. The accumulated INL errors lead to integral gain errors and create relative power offsets at the output of the power amplifier.
3.4 Reasons for Phase Discontinuity

In systems operating at high frequencies such as cellular, WiMax the relative phase change of the signal occurs due to

- carrier phase shifts that occur due to change in capacitive impedances during an RF power change in multi-stage amplifiers. This is because the gain control in the majority of present day RF amplifiers is based on altering the current through capacitive segments.
- random signal phase changes due to the baseband analog filters stages
- random carrier phase offsets caused every time the RF VCO[69] is enabled.
- temperature compensation circuits in RF circuits such as mixer and VCO’s which cause unknown carrier phase changes.

For the sake of analysis, assume that the primary cause of the phase shifts introduced into a mobile system is due to change in RF gain stage of the amplifier within the system. If $\lambda_1$ and $\lambda_2$ are the absolute phase changes (degrees) when the RF gain amplifier is at step $G_1$, and $G_2$ respectively, then the relative phase change is defined as $\Delta\lambda_{(1,2)} = \lambda_1 - \lambda_2$. This change in-phase angle will lead to unknown random phase shifts of the RF carrier signal. Figure 3-5 shows measured results of relative phase shifts for a discrete 16 stage gain RF amplifier. The relative phase changes between two consecutive stages $m$ and $n$ are represented by $\Delta\lambda_{(m,n)}$. The change in carrier phase shift must be compensated so that the transmitted signal does not undergo relative phase shift changes when stepping through the gain amplifier stages. The introduced carrier phase shifts are either due to changes in capacitive impedances of the high frequency amplifier or due to frequency dependent phase drifts introduced by analog circuits in the transmit path.
3.5 DSP based Relative Gain/Phase Estimation Algorithm Theory (DSP-GPE)

The goal of DSP-GE algorithm is to estimate the relative gain changes and random signal phase shifts introduced by the RF and analog components of the mobile system. The estimated gain and phase values are then used to compensate for the gain errors by providing digital gain and phase correction at the baseband signal processing path of the mobile device. This helps in reducing the relative gain error and maintaining the phase information of the signal. The primary idea of the introduced technique is to estimate successive gain and phase variations by employing DFT based detection of relative change in signal energy and phase information.

3.5.1 Theory of Operation

As explained in chapter 2, Figure 3-6a describes system architecture of any quadrature signal based mobile transmit path. The theory behind the algorithm can be described by assuming tone inputs as the in-phase \( I(t) \) and quadrature phase signal \( Q(t) \). Based on this assumption, the complex baseband signal is represented as

\[
C(t) = I(t) + jQ(t),
\]

where

\[
I(t) = \cos(\omega_{bb}t + \phi) \quad \text{and} \quad Q(t) = \sin(\omega_{bb}t + \phi),
\]

Where, \( \omega_{bb} \) is the digital baseband frequency of the tone and \( \phi \) is the phase angle of the baseband signal vector. The complex signal is generated at the baseband and passes through the DAC and modulated by the RF mixer and transmitted through an RF gain amplifier. The transmitted signal can be represented as

\[
g(t) = D_1 G[I(t) + jQ(t)]e^{j\beta} e^{j\omega_{bb}t}, \quad (3-14)
\]
where, $D_1$ is the digital gain, $G$ and $e^{j\lambda}$ is gain and phase shift introduced by the RF VGA for that gain step. The modulated transmit RF frequency introduced by the modulator is denoted by $e^{\omega_{tx} t}$.

During the algorithm operation, the output of the transmit gain amplifier $g(t)$ is looped back into the pseudo-receiver [22] section which has an RF gain and a demodulator stage. The RF signal $g(t)$ is demodulated back to baseband frequency depending on the frequency offset between the RF modulator and the demodulator. Depending on the frequency offsets between transmit and receive VCO’s the desired baseband signal frequency can be altered. Assume $e^{j(\omega_{tx} t)}$ is the transmitting frequency and $e^{j(\omega_{rx} t)}$ is the demodulation frequency and the frequency difference is defined by $e^{j(\omega_{fr} t)}$. Based on this assumption, the received demodulated baseband signal is represented by

$$Rx_{BB}(t) = g(t).G(e^{j(\omega_{rx} t + \theta)}), \text{ where } e^{j(\omega_{rx} t + \theta)} = (e^{j(-\omega_{tx} t + \omega_{fr} t + \theta)})$$

$$= D_1 G[I(t) + jQ(t)]e^{j\lambda} e^{\omega_{rx} t} G(e^{j(-\omega_{tx} t + \omega_{fr} t + \theta)})$$

$$= D_1 G[I(t) + jQ(t)]e^{j\lambda} G(e^{j(\omega_{fr} t + \theta)})$$

$$= D_1 [I(t)G(e^{j(\omega_{fr} t + \theta)}) + jQ(t)G(e^{j(\omega_{fr} t + \theta)})] \quad (3-15)$$

Hence, the demodulated baseband signal has a frequency of $\omega_{fr}$ and can be represented as described in the Equation 3-15.

Expanding the 1st term of Equation (3-15), can be expressed as

$$I(t)D_1 G(e^{j(\omega_{fr} t + \theta)}) = D_1 G \cos(\omega_{bb} t + \phi)(e^{j(\omega_{fr} t + \theta + \lambda)})$$

$$= D_1 G(e^{j(\omega_{fr} t + \theta + \lambda)}) \cos(\omega_{bb} t + \phi)$$
\[= D_1 G[\cos(\omega_{IF} t + \theta + \lambda) + j \sin(\omega_{IF} t + \theta + \lambda)] \cos(\omega_{BB} t + \phi)\]

\[= D_1 G[(\cos(\omega_{IF} t + \theta + \lambda) \cos(\omega_{BB} t + \phi)) + j(\sin(\omega_{IF} t + \theta + \lambda) \cos(\omega_{BB} t + \phi))]\]

\[= D_1 \frac{G}{2} [(\cos(\omega_{IF} + \omega_{BB}) t + \theta + \lambda + \phi) + (\cos(\omega_{IF} - \omega_{BB}) t + \theta + \lambda - \phi) + j(\sin(\omega_{IF} + \omega_{BB}) t + \theta + \lambda + \phi) + (\sin(\omega_{IF} - \omega_{BB}) t + \theta + \lambda - \phi))\]

Let \( P = (\omega_{IF} + \omega_{BB}) \) and \( Q = (\omega_{IF} - \omega_{BB}) \), this results in

\[I(t) D_1 G(e^{j(\omega_{IF} t + \theta)}) = D_1 \frac{G}{2} [(\cos(P t + \theta + \lambda + \phi) + (\cos(Q t + \theta + \lambda - \phi) + j(\sin(P t + \theta + \lambda + \phi) + (\sin(Q t + \theta + \lambda - \phi)))] \tag{3-16}\]

Expanding the 2\(^{nd}\) term of Equation (3-15), we get

\[= jQ(t) G D_1 (e^{j(\omega_{BB} + \theta)})\]

\[= jG D_1 [\cos(\omega_{IF} t + \theta) + j(\sin(\omega_{IF} t + \theta)] \sin(\omega_{BB} t + \phi)\]

\[= \frac{G}{2} D_1 [j \sin(P t + \theta + \phi) - j \sin(Q t + \theta - \phi) - (\cos(Q t + \theta - \phi) + \cos(P t + \theta + \phi)]\]

\[= \frac{G}{2} D_1 [\cos(P t + \theta + \phi) - (\cos(Q t + \theta - \phi) + j(\sin(P t + \theta + \phi) - \sin(Q t + \theta - \phi))]] \tag{3-17}\]

Adding (3-15) and (3-17), results in

\[= \frac{G}{2} D_1 [(\cos(P t + \theta + \lambda + \phi) + \cos(Q t + \theta + \lambda - \phi) + \cos(P t + \theta + \phi) - (\cos(Q t + \theta - \phi) + j(A \sin(P t + \theta + \lambda + \phi) + (A \sin(Q t + \theta + \lambda - \phi) + (\sin(P t + \theta + \phi) - \sin(Q t + \theta - \phi)))] \tag{3-18}\]

where, \( P = (\omega_{IF} + \omega_{BB}) \) and \( Q = (\omega_{IF} - \omega_{BB}) \)

The DSP-GPE technique uses a single baseband tone through the \( I \) channel. The blue plot in Figure 3-7 shows the spectrum of transmit baseband signal \( C(t) = I(t) \).
whose frequency $\omega_{BB}$ is 100 KHz. The black plot in Figure 3-7 shows the complex baseband signal $g(t)$ up converted to RF frequency, assumed to be 5MHz. Hence the up converted signal frequency will fall at 5.1MHz. The red plot in Figure 3-7 shows the down converted signal $R_{x_{BB}}(t)$ to a 400 KHz baseband frequency and effectively, in this simulation, the demodulator frequency is assumed to be 300 KHz. If a DFT operation is performed at the signal bin $Q = (\omega_{RF} - \omega_{BB})$, all the terms of Equation 3-18 except the component vectors containing $Q$ will equate to zero. Hence, the DFT of $I$ and $Q$ channel can be expressed as

$$I_{-DFT} = \frac{D G}{2} \left[ \frac{1}{2} e^{j(\theta + \lambda - \phi)} - \frac{1}{2} e^{j(\theta - \phi)} \right] \quad (3-19)$$

$$Q_{-DFT} = \frac{D G}{2} \left[ -\frac{A}{2} j e^{j(\theta + \lambda - \phi)} + j \frac{1}{2} e^{j(\theta - \phi)} \right] \quad (3-20)$$

If the input to the $Q$ channel is 0, then the second term becomes zero and hence, Equations 3-19 and 3-20 can be represented as

$$I_{-DFT} = \frac{D G}{2} \left[ \frac{1}{2} e^{j(\theta + \lambda - \phi)} \right] \quad (3-21)$$

$$Q_{-DFT} = \frac{D G}{2} \left[ -\frac{A}{2} j e^{j(\theta + \lambda - \phi)} \right] \quad (3-22)$$

Assume the RF VGA gain stage is changed from Gain stage $G_1$ to $G_1$ which introduces a complex phase shift from $e^{j\lambda_1}$ to $e^{j\lambda_2}$. The goal of the algorithm is to find the relative phase shifts and compensate for them by predistorting the $I$ and the $Q$ channel signals.
3.5.2 Gain and Phase Estimation Steps

Based on a tonal input into \( I \) channel or \( Q \) channel of the mobile transmit signal path, the estimation of the gain variation and phase drifts can be described in three steps.

Step 1:
Calculate the first DFT corresponding to a complex gain and phase shift applied at the VGA. Let this applied gain step at the VGA result in gain \( G_1 \) and a phase shift of \( \lambda_1 \).

The composite gain and phase change is represented as \( G_1 e^{j\lambda_1} \). From Equation 3-19, the \( I \) channel DFT can be computed as

\[
I_- DFT(G_1 e^{j\lambda_1}) = \frac{D}{2} \left[ \frac{1}{2} e^{j(\theta_1 + \lambda_1 - \phi)} \right]
\]  
(3-23)

Step 2:
Increment the VGA gain to the next state, to \( G_2 e^{j\lambda_2} \), then the corresponding \( I \) channel DFT is computed similarly as

\[
I_- DFT(G_2 e^{j\lambda_2}) = \frac{D}{2} \left[ \frac{1}{2} e^{j(\theta_2 + \lambda_2 - \phi)} \right]
\]  
(3-24)

Step 3:
The ratio of the magnitude of the corresponding DFT’s are calculated.

\[
Ratio(2,1) = \frac{|I_- DFT(G_2 e^{j\lambda_2})|}{|I_- DFT(G_1 e^{j\lambda_1})|}
\]  
(3-25)

\[
= \frac{D}{2} \frac{1}{2} \left[ e^{j(\theta_2 + \lambda_2 - \phi)} \right] = \frac{G_2}{G_1} \left[ e^{j(\lambda_2 - \lambda_1)} \right]
\]  
(3-26)

\[
= \Delta G \left[ e^{j(\lambda_2)} \right]
\]
where, \( \Delta G \) and \( \Delta \lambda \) is the estimated gain and the phase shift. Hence the estimated gain change is calculated as the absolute value of the ratios of consecutive DFT measurements. On observing Equation 3-26, it is clear that the result is a function of \( \theta \) and \( \phi \). The angle \( \theta \) is a random phase angle between transmit and receive VCO’s. The angle \( \phi \) is the phase angle of the injected baseband calibration signal. Based on measurements it is found that transmit and the receive VCO’s have only a frequency error of less than 2Hz and hence does not degrade the accuracy of this algorithm. In order to make this algorithm less susceptible to frequency and additional phase errors, the frequency of the calibration signal is selected in such a way that there is no phase imbalance introduced between both the quadrature paths I and Q from one iteration to the next. Based on the above mentioned criteria the assumption of \( \theta \) and \( \phi \) being constant is valid.

The DSP-GPE algorithm is used to estimate the relative gain and phase shifts dynamically. The estimated gain and phase shifts are then used to correct for relative DNL errors and phase shifts. Depending on the application, the DSP-GPE algorithm can be used as a calibration sequence before the signal transmission. The estimated values are be stored in ROM lookup tables and applied as correction factors during normal transmit operations.

### 3.5.3 Gain and Phase Compensation Implementation and Equations

Assume that \( \Delta G_{\text{ref}} \) and \( \Delta \lambda_{\text{ref}} \) are the ideal gain and phase changes between two consecutive gain steps of the VGA according to circuit design. Let \( \Delta G, \Delta \lambda \) be the actual estimated gain and phase changes between the same consecutive steps. The DNLE is then calculated as
\[ DNLE = \gamma = |\Delta G_{\text{ref}} - \Delta G|, \quad (3-27) \]

and the phase error is calculated as
\[ \phi_{\text{err}}(\text{deg rees}) = |\Delta \lambda_{\text{ref}} - \Delta \lambda|. \quad (3-28) \]

The phase error is then applied as correction to the digital baseband signal to compensate for the amount of phase change to meet the phase discontinuity of the signal transmitted. The gain error is then applied to the baseband signal to meet relative power level accuracy specifications.

### 3.5.4 Derivation of Equations for Gain and Phase Estimation and Compensation

The complex signal at the input of the modulator is given by the Equation
\[ D_1[\cos(\omega_{bb}t + \phi) + j\sin(\omega_{bb}t + \phi)], \quad (3-29) \]

where \( D_1 \) is the digital gain at the baseband and \( \phi \) is the phase angle of \( I \) and the \( Q \) channel signals. The \( \text{DNLE} \) (dB) is represented by a linear value of \( \gamma \). The phase of \( I(t) \) and \( Q(t) \) has to be compensated by the estimated phase error term \( \phi_{\text{err}} \). Hence the gain and phase compensated signal can be represented as
\[ I(t)_{\text{comp}} = \gamma \cos(\omega_{bb}t + \phi + \phi_{\text{err}}) \quad (3-30) \]
\[ Q(t)_{\text{comp}} = \gamma \sin(\omega_{bb}t + \phi + \phi_{\text{err}}) \quad (3-31) \]

To realize this in hardware, we need to find a way mathematically to convert \( I(t) \) and \( Q(t) \) to \( I(t)_{\text{comp}} \) and \( Q(t)_{\text{comp}} \).

Multiply \( I(t) \) by \( \cos(\phi_{\text{err}}) \) and \( Q(t) \) by \( \sin(\phi_{\text{err}}) \)
\[ I(t)\cos(\phi_{\text{err}}) = \cos(\omega_{bb}t + \phi)\cos(\phi_{\text{err}}) \quad (3-32) \]
\[ Q(t)\sin(\phi_{\text{err}}) = \sin(\omega_{bb}t + \phi)\sin(\phi_{\text{err}}) \quad (3-33) \]

Initially, on expanding \( I(t)\cos(\phi_{\text{err}}) \), results in
\[ I(t) \cos(\phi_{err}) = \frac{1}{2} \cos(\omega_{bb}t + \phi_{err}) - \frac{1}{2} \sin(\omega_{bb}t + \phi_{err}) \]

\[ = \frac{1}{2} \cos(\omega_{bb}t + \phi_{err}) + \frac{1}{2} \cos(\omega_{bb}t + \phi_{err}) \]

But, we know that

\[ I(t)_{comp} = \cos(\omega_{bb}t + \phi_{err}) \], disregarding the gain DNL term for now. Adding the required terms results in

\[ I(t)_{comp} = \cos(\omega_{bb}t + \phi_{err}) \]

\[ = \frac{1}{2} \cos(\omega_{bb}t + \phi_{err}) + \frac{1}{2} \cos(\omega_{bb}t + \phi_{err}) - \frac{1}{2} \cos(\omega_{bb}t + \phi_{err}) \]

Substituting in Equation 3-34 results in

\[ = I(t) \cos(\phi_{err}) - Q(t) \sin(\phi_{err}) = \cos(\omega_{bb}t + \phi_{err}) \]

On similar lines, we can prove that

\[ Q(t) \cos(\phi_{err}) + I(t) \sin(\phi_{err}) = \sin(\omega_{bb}t + \phi_{err}) \]

Hence, to compensate the signal by \( \phi_{err} \), the following implementation can be adopted.

\[ I(t)_{comp} = I(t) \cos(\phi_{err}) - Q(t) \sin(\phi_{err}) \]

\[ Q(t)_{comp} = Q(t) \cos(\phi_{err}) + I(t) \sin(\phi_{err}) \]

The brief overview of the algorithm is described in by the flow chart in Figure 3-8.
3.6 DSP Hardware Structures for Relative Gain/Phase Estimation and Compensation

Most of the basic hardware employed in Chapter 2 can be adopted for this algorithm. In addition, this section describes two DSP hardware structures adopted for relative gain and phase estimation and compensation. The following section describes the equations and the DSP implementation of the phase compensation circuit and the gain estimation digital circuit.

3.6.1 Phase Compensation DSP Structure

Based on descriptions in earlier sections, it is understood that the relative phase shifts estimated can be used as baseband compensation factors to correct the unknown phase shifts introduced in a mobile system.

\[ I(t)_{\text{comp}} = I(t)\cos(\phi_{\text{err}}) - Q(t)\sin(\phi_{\text{err}}) \]  
\[ Q(t)_{\text{comp}} = Q(t)\cos(\phi_{\text{err}}) + I(t)\sin(\phi_{\text{err}}) \]

The cosine and sine of an angle are implemented with an 8X8 ROM. This has 8 bits each and 256 entries. Prior knowledge of the maximum amount of phase compensation that a system application will need helps in limiting the size of the ROM. For our application, the maximum amount of phase shift required is +/-25 degrees. Adopting an 8 bit input ROM will result in accuracy of \(25/256 = 0.09765\) degrees. Hence, 8 bit registers will give us an output accuracy of \(1/256 = 0.0039625\) degrees.

3.6.2 DFT Based Gain Estimation Structure

The DFT of a signal \(x(n)\) is represented as

\[ X(k) = \sum_{n=0}^{N-1} x(n)(e^{-j2\pi nk/N})^n, \text{ where } k = 0, 1, 2, \ldots N - 1 \]

where, the frequency of interest is located in the \(k^{th}\) bin.
Let \( W_k = e^{\frac{j2\pi k}{N}} \), then

\[
X(k) = \sum_{n=0}^{N-1} x(n)(e^{-\frac{j2\pi k}{N}})^n = \sum_{n=0}^{N-1} x(n)W_k^{(N-n)} = W_k^N x(0) + W_k^{N-1} x(1) + \cdots W_k^2 x(N-2) + W_k^1 x(N-1)
\]

The transfer function of the system that estimates the DFT is represented as

\[
H(z) = \frac{1}{1 - e^{\frac{j2\pi k}{N}} z^{-1}}
\]

\[
\frac{Y(z)}{X(z)} = \frac{1}{1 - e^{\frac{j2\pi k}{N}} z^{-1}} \quad (3-41b)
\]

\[
y(n) = x(n) + y(n-1)e^{\frac{j2\pi k}{N}} = x(n) + y(n-1)W_k \quad (3-41c)
\]

Expanding 3-41c results in

\[
y(n) = x(n) + x(n-1)W_k + x(n-2)W_k^2 + \cdots x(0)W_k^N \quad (3-41d)
\]

Comparing Equations 3-41c and 3-41d it is clear that the required transform is obtained when

\[
X(k) = y(N)
\]

Multiplying the numerator and denominator by the conjugate, results in

\[
H(z) = \frac{1}{(1-W_k z^{-1})} \cdot \frac{(1-W_k^{-1} z^{-1})}{(1-W_k^{-1} z^{-1})} \quad (3-41e)
\]

Hence,

\[
H(z) = \frac{(1-W_k^{-1} z^{-1})}{(1-(W_k + W_k^{-1})z^{-1} + z^{-2})}
\]

\[
H(z) = \frac{Y(z)}{X(z)} = \frac{(1-W_k^{-1} z^{-1})}{1 - 2\cos \frac{2\pi k}{N} z^{-1} + z^{-2}}
\]
where \((W_k + W_k^{-1}) = e^{\frac{2\pi k}{N}} + e^{-\frac{2\pi k}{N}} = 2 \cos\left(\frac{2\pi k}{N}\right)\)

Based on this, the DFT \(X(k) = y(N) - W_k^{-1}y(N-1)\)

\[
DFT = Y(N) - Y(N-1)\cos\left(\frac{2\pi k}{N}\right) - jY(N-1)\sin\left(\frac{2\pi k}{N}\right)
\] (3-41f)

where, \(X(k) = y(N)\) at the final iteration \(N\) which is the DFT length.

\[
X(k) = y(N) - W_k^{-1}y(N-1)
\] (3-41g)

Taking the square of the Equation 3-41g, we obtain

\[
|X(k)|^2 = X(k)X^*(k)
\]

\[
X(k) = y(N) - W_k^{-1}y(N-1)
\]

\[
X^*(k) = y(N) - W_k^{-1}y(N-1)
\]

\[
|X(k)|^2 = [y(N) - W_k^{-1}y(N-1)][y(N) - W_k^{-1}y(N-1)]
\]

\[
|X(k)|^2 = y^2(N) + y^2(N-1) - (W_k^{-1} + W_k^{-1})y(N)y(N-1)
\]

\[
|X(k)|^2 = y^2(N) + y^2(N-1) - 2 \cos\left(\frac{2\pi k}{N}\right)y(N)y(N-1)
\] (3-42)

Equation 3-42 can be used as the single point power spectral density estimator.

Depending on the value of \(k\), the frequency bin of interest, the value of the DFT is estimated. The DSP hardware structure adopted to estimate the single point magnitude of DFT is shown in Figure 3-11. The DSP hardware that estimates the gain and phase estimate of the signal is shown in Figure 3-12.

Assume that the number of samples of the DFT is \(N = 512\), and the sampling frequency of the DSP hardware is \(F_s = 5MHz\) and \(F_{tone} = 146.51kHz\). In our algorithm,
\( F_{\text{tone}} = 146.51 \text{KHz} \) will be the final baseband frequency at the receiver. The DFT index \( K \) corresponding to this frequency is calculated by

\[
K = \frac{F_{\text{tone}}}{F_s} N
\]

\[
K = \left( \frac{146.51 \text{KHz}}{5 \text{MHz}} \right) 512 = 15
\]

This DSP hardware in Figure 3-12 calculates the real and complex DFT for a real signal stream. In our algorithm this DSP hardware is present in both \( I \) channel and the \( Q \) channel. For our application, the \( I \) channel is employed and the output of the filter has a real part and an imaginary part. The absolute value is then estimated to result in \( I \_DFT \) and \( Q \_DFT \).

### 3.7 System Simulations and Lab Measurement Results

The system architecture was modeled in tools such as Matlab and Signal Processing work station (SPW). System simulations were performed with the following parameters. Figure 3-13 shows the time domain waveforms of demodulated \( I \) channel at the receiver. The simulation frequencies used are \( \omega_{\text{IF}} = 300 \text{KHz}, \omega_{\text{BB}} = 100 \text{KHz} \), \( \omega_{\text{TX}} = 5 \text{MHz} \) and \( \omega_{\text{RX}} = 5 \text{MHz} + 300 \text{KHz} \). Hence the demodulated baseband signal frequency is 400 KHz. Each stage results in a RF gain and a phase change \((G_k e^{i \lambda k})\), where \( k = 1, 2 \ldots 8 \). Figure 3-13 shows plots for \( k = 1, 2 \ldots 4 \). Figure 3-14 shows system simulation performed with \( \omega_{\text{IF}} = 300 \text{KHz}, \omega_{\text{BB}} = 100 \text{KHz} \) and by stepping the eight stages of the RF gain amplifier. Each stage results in a RF gain and a phase change of \((G_k e^{i \lambda k})\), where \( k = 1, 2 \ldots 8 \). Figure 3-15 shows measured DFT magnitude for \( I \) channel signal. The measurement shows that the peak of the magnitude appears at
\( K = 15 \) which corresponds to 146.51 KHz \( (\omega_f + \omega_{bb}) \), where \( \omega_f = 100 \text{KHz} \) and \( \omega_{bb} = 46.51 \text{KHz} \). The frequency of the tone \( \omega_{bb} \) has to be selected so that the DFT bin falls exactly on an integer multiple of \( K \).

\[
K = \left( \frac{146.51 \text{KHz}}{5 \text{MHz}} \right) \times 125 = 15
\]

The following descriptions explain the basic steps involved in the gain and phase estimation algorithm.

Step 1

By employing the DSP hardware, calculate the first \( I \_ DFT \) with the complex gain and phase shift applied at the VGA to be \( (G_1 e^{j\lambda_1}) \). The \( I \_ DFT \) is calculated as

\[
I \_ DFT(G_1 e^{j\lambda_1}) = \frac{D_1 G_1}{2} \left[ \frac{1}{2} e^{j(\theta + \lambda_1 - \phi)} \right]
\]

Step 2:

Increment the VGA gain to the next state, to \( (G_2 e^{j\lambda_2}) \), then the corresponding \( I \_ DFT \) is computed in the same way as

\[
I \_ DFT(G_2 e^{j\lambda_2}) = \frac{D_2 G_2}{2} \left[ \frac{1}{2} e^{j(\theta + \lambda_2 - \phi)} \right]
\]

Step 3: The ratio of the magnitude of the corresponding DFT’s are calculated.

\[
Ratio(2,1) = \frac{|I \_ DFT(G_2 e^{j\lambda_2})|}{|I \_ DFT(G_1 e^{j\lambda_1})|}
\]

\[
Ratio(2,1) = \frac{D_1 G_2}{2} \left[ \frac{1}{2} e^{j(\theta + \lambda_2 - \phi)} \right] = \frac{G_2}{G_1} \left[ e^{j(\lambda_2 - \lambda_1)} \right]
\]

\[Ratio(2,1) = \Delta G \left[ e^{j(\Delta \lambda)} \right] \] is the estimated gain and the phase shift.
3.7.1 System Simulations of the DSP-GPE Algorithm

The performance of the DSP-GPE algorithm is analyzed by system simulations. Table 3-5 shows the estimated DFT by using the fixed point model of the DFT estimator hardware. At each RF gain amplifier step, the absolute magnitude of I_DFT is estimated by assuming $N = 512$ samples. To avoid spectrum leakage, it has to be taken care that the DFT measurement has to start at the proper time instants to capture periodic cycles of $x(n)$. The complex I_DFT output is tabulated in Table 3-5.

After eight periodic measurements, the DSP algorithm calculates the ratio of successive I_DFT measurements. Thus the ratios $\text{Ratio}(m, n) = \frac{|I_{\text{DFT}}(G_ne^{j2\pi n})|}{|I_{\text{DFT}}(G_me^{j2\pi m})|}$ is calculated by the DSP algorithm. Table 3-6 shows measurements tabulated that correspond to ratios of consecutive eight DFT measurements. The ratio

$$\frac{|I_{\text{DFT}}(G_ne^{j2\pi n})|}{|I_{\text{DFT}}(G_me^{j2\pi m})|}$$

will lead to a gain and a phase component $\Delta G$ and $\phi_{\text{err}}$ respectively. The desired gain change, $\Delta G_{\text{ref}}$, and the difference $DNLE = \gamma = |\Delta G_{\text{ref}} - \Delta G|$ is calculated and applied to the baseband signal. The amount of phase change estimated $\phi_{\text{err}}$ is directly applied to the baseband signal as a pre-distorted phase to maintain signals phase continuity specifications. The simulation results show the performance of the algorithm with the introduced gain and phase error. Simulations performed over worst case process variations reveal that the algorithm predicts the gain error better than 0.1dB and phase error better than 1 degree accuracy.

3.7.2 Lab Measurement Results

Figure 3-18 shows measured INLE curves for the 16 stage driver amplifier after baseband gain error compensation. The DSP-GPE algorithm is performed as a part of
the mobile radio calibration for a single RFIC for a mid frequency band of operation assuming room temperatures. The estimated DNLE values are stored in ROM look up tables based on frequency of operation and are applied to the baseband signal during normal transmission. The measurement shown in Figure 3-18 is average INLE over three different RFIC. The technique compensates for relative gain errors caused due to differential nonlinearities in a high frequency amplifier. Figure 3-19 shows the estimated phase change in degrees across different sections of the high frequency amplifier by calibrating using a tonal input at the $I$ and the $Q$ channel as described earlier. The algorithm is run only at room temperature (+25 degrees) and at mid frequency conditions.

The phase estimation is then stored in the ROM look up tables after the calibration is performed. The estimated phase values are applied as baseband compensation as described in earlier sections. Figure 3-20 shows measured relative phase change in degrees across different sections of the high frequency amplifier after the estimated phase compensation is applied at the baseband signal path. The algorithm is able to estimate the relative phase change effectively and the applied phase correction helps to preserve system phase discontinuity specifications. System lab measurements and simulations prove that the described technique can estimate DNLE better than 0.1dB accuracy and a phase shift less than 0.5 degrees and hence, reducing relative gain and phase error to within 0.1dB and 1 degree accuracy. Figure 3-21 shows lab measurements with a sinusoidal input into the mobile system and a phase angle compensation of +/-90 degrees applied on $I$ and $Q$ channels. In order to improve the range of correction angle and reduce area, DSP-software is used to implement fixed
point level algorithms. The above mentioned measurements and system simulations prove the functionality and system performance of the DSP-GPE system algorithm.

### 3.8 Summary

- The DSP-GPE algorithm is implemented in a mobile device for the gain and phase estimation.

- System lab measurements and simulations prove that the DSP-GPE technique can estimate DNLE better than 0.1dB accuracy and phase shifts better than 0.5 degrees accuracy. This helps to maintain relative gain and phase errors to be within 0.1dB and 1 degree accuracy respectively.

- The approximate gate count is less than 10K as the DSP hardware includes the DFT filter and the gain and phase compensation circuits.

- The DSP-GPE algorithm is either used a pre-calibration technique to initially estimate the gain and phase error or used dynamically by interleaving periodic tone signals as a part of the baseband signals to be transmitted.

- The obtained gain and phase error estimates are stored in a ROM table and then applied during normal signal transmission.

---

**Figure 3-1.** System block diagram of a wireless transmitter showing gain change and phase change
Figure 3-2. Measured amplifier bias vs. output characteristics with respect to temperature and frequency bands of operation.

Figure 3-3. Measured DNLE (dB) with respect to change in frequency bands of operation.
Figure 3-4. Measured INLE with respect to change in frequency bands of operation

Figure 3-5. Absolute phase variations of an RF device due to capacitive loads
Figure 3-6. Gain and phase estimation A) System block diagram of the mobile device with the DSP-GPE algorithm. B) Implemented frequency location of the calibration signal during the algorithm.
Figure 3-6. Continued
Figure 3-7. Frequency location of the calibration signal during the algorithm
Enable digital clocks
Set the digital baseband gain to be D₁

Send Baseband signal I(t) and Q(t) with
tone frequency Wbb
\[ I(t) = \cos(w_{bb}t + \phi) \]
\[ Q(t) = \sin(w_{bb}t + \phi) \]

Set RF upconversion frequency to be WTx
\[ e^{j\theta} e^{w_{x}t} \]
Set RF downconversion frequency to be WRx=WTx+WIF
\[ e^{j\theta} e^{w_{x}t} \]
\[ e^{j0} = e^{j\theta} e^{w_{x}t} \]

Set the RF gain amplifier to G₁ state \((G_e^{j\lambda})\)

The transmitted signal is
\[ g(t) = D₁G[I(t) + jQ(t)]e^{j\theta} e^{w_{x}t} \]

The demodulated received signal is \(Rx_{bb}(t)\)
\[ Rx_{bb}(t) = D₁G[I(t) + jQ(t)]e^{j\theta} G(e^{i(w_{x}t+\phi)}) \]

Estimate complex DFT for real I signal
\[ I_{DFT}(G_e^{j\lambda}) = \frac{1}{2} \left[ e^{j\theta} + e^{-j\theta} \right] \]

Increment the VGA gain to the next state, \((G_e^{j\lambda})\)

Re-Estimate complex DFT for real I signal
\[ I_{DFT}(G_e^{j\lambda}) = \frac{1}{T} \left[ e^{j\theta} + e^{-j\theta} \right] \]

Compute ratio of consecutive DFT’s
\[ \text{Ratio}(2,1) = \frac{I_{DFT}(G_e^{j\lambda})}{I_{DFT}(G_e^{j\lambda})} = \frac{G_e^{j\lambda}}{G_e^{j\lambda}} \]
\[ \text{Ratio}(2,1) = \Delta G_e^{j\lambda} \]

Estimate Gain DNL Error and Phase offset error
\[ \text{DNL} = \gamma = |\Delta G_e^{j\lambda} - \Delta G| \]
\[ \phi_{err} = |\Delta \phi_{ref} - \Delta \lambda| \]

\[ DNLE = \gamma \quad \phi_{err} = |\Delta \phi_{ref} - \Delta \lambda| \]

Figure 3-8. Flowchart of the DSP-GPE algorithm for relative gain and phase change estimation
Figure 3-9. Baseband signal phase compensation DSP hardware structure
Figure 3-10. Simulation of baseband signal phase compensation by using the DSP hardware structure

Figure 3-11. DSP Hardware structure to estimate the absolute gain change
Figure 3-12. DSP Hardware structure to estimate the absolute gain and phase change.

Figure 3-13. Simulation plots to show that $R_{x_{BB}}(t)$ with frequency of 400 KHz and $\omega_{IF} = 300 KHz$ over the 8 RF gain settings.
Figure 3-14. Simulation of FFT magnitude of $R_{BB}(t)$ with $\omega_{IF} = 300$KHz over the 8 RF gain settings.

Figure 3-15. Simulated DFT magnitude of I and Q channel for $K = 13, 14, 15, 16, 17$. 

133
Figure 3-16. Ideal gain change $\Delta G_{ref}$, estimated gain change $\Delta G$ (dB) and DNLE(dB) $|\Delta G_{ref} - \Delta G|$

Figure 3-17. Ideal phase change $\Delta \lambda_{ref}$, estimated phase change $\Delta \lambda$ (deg) and

\[ \phi_{err} = |\Delta \lambda_{ref} - \Delta \lambda| \]
Figure 3-18. Averaged INLE error measured on three RFIC after the gain error compensation.

Figure 3-19. Absolute phase variation in the mobile device after phase compensation.
Figure 3-20. Relative phase variation in the mobile device after compensation
Figure 3-21. Measured plots to show the 90 degrees phase compensation performed by the DSP hardware

Table 3-1. Approximate THD requirements for a few applications

<table>
<thead>
<tr>
<th>Applications</th>
<th>THD %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Telephone</td>
<td>&lt; 10%</td>
</tr>
<tr>
<td>High Quality Audio</td>
<td>&lt; 1%</td>
</tr>
<tr>
<td>Video</td>
<td>&lt; 5%</td>
</tr>
<tr>
<td>Analog Repeaters</td>
<td>&lt;0.001%</td>
</tr>
<tr>
<td>RF Amplifiers</td>
<td>&lt;0.1%</td>
</tr>
<tr>
<td>Amplifier gain stages (3 bits decoder)</td>
<td>Gain in dB Operating condition 1</td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>---------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>$G_{1g1}$</td>
</tr>
<tr>
<td>2</td>
<td>$G_{1g2}$</td>
</tr>
<tr>
<td>3</td>
<td>$G_{1g3}$</td>
</tr>
<tr>
<td>4</td>
<td>$G_{1g4}$</td>
</tr>
<tr>
<td>5</td>
<td>$G_{1g5}$</td>
</tr>
<tr>
<td>6</td>
<td>$G_{1g6}$</td>
</tr>
<tr>
<td>7</td>
<td>$G_{1g7}$</td>
</tr>
<tr>
<td>8</td>
<td>$G_{1g8}$</td>
</tr>
</tbody>
</table>
Table 3-3. Measured High Frequency Amplifier gain across temperature and frequency bands of operation.

<table>
<thead>
<tr>
<th>Conditions</th>
<th>-30 degrees (low,mid,high) channels</th>
<th>+25 degrees (low,mid,high) channels</th>
<th>+85 degrees (low,mid,high) channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain Stage</td>
<td>low_chG2g(1-16)_cold</td>
<td>mid_chG1g(1-16)_cold</td>
<td>high_chG3g(1-16)_cold</td>
</tr>
<tr>
<td>G1</td>
<td>-64.5208</td>
<td>-64.74</td>
<td>-64.7999</td>
</tr>
<tr>
<td>G15</td>
<td>-0.436</td>
<td>-0.593</td>
<td>-0.772</td>
</tr>
<tr>
<td>G16</td>
<td>1.787</td>
<td>1.619</td>
<td>1.442</td>
</tr>
</tbody>
</table>
Table 3-4. Measured DNLE with mid channel as the reference for a 16 stage gain amplifier

| Gain steps | |mid_ch-mid_ch| |mid_ch-low_ch| |mid_ch-high_ch| |mid_ch-mid_ch| |mid_ch-low_ch| |mid_ch-high_ch| |mid_ch-mid_ch| |mid_ch-low_ch| |mid_ch-high_ch| |
|------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 1          | 0              | -0.008         | 0.001          | -0.119         | -0.119         | -0.121         | 0.113          | 0.097          | 0.126          |
| 2          | 0              | 0.014          | 0.002          | -0.054         | -0.041         | -0.076         | 0.077          | 0.096          | 0.078          |
| 3          | 0              | 0.01           | -0.02          | -0.036         | -0.017         | -0.029         | 0.018          | 0.028          | 0.014          |
| 4          | 0              | 0.002          | 0.005          | -0.013         | -0.022         | -0.04          | 0.025          | 0.023          | 0.018          |
| 5          | 0              | -0.01          | -0.004         | 0.004          | 0.006          | 0.015          | 0.001          | -0.01          | -0.014         |
| 6          | 0              | 0.0698         | 0.1157         | -0.037         | 0.0418         | 0.0787         | -0.045         | -0.0092        | 0.0567         |
| 7          | 0              | 0.004          | -0.002         | 0.073          | 0.075          | 0.056          | -0.093         | -0.069         | -0.081         |
| 8          | 0              | -0.003         | 0.003          | -0.009         | -0.005         | 0.01           | 0.011          | 0.008          | -0.003         |
| 9          | 0              | -0.013         | 0.017          | -0.165         | -0.172         | -0.157         | 0.147          | 0.137          | 0.172          |
| 10         | 0              | -0.002         | -0.008         | 0.009          | -0.002         | 0.024          | 0.014          | 0.011          | 0.003          |
| 11         | 0              | 0.007          | 0.002          | -0.007         | -0.002         | -0.014         | 0.004          | -0.002         | 0.001          |
| 12         | 0              | -0.006         | -0.005         | 0.002          | -0.01          | -0.001         | 0.01           | -0.003         | 0.003          |
| 13         | 0              | -0.011         | 0.018          | -0.121         | -0.135         | -0.134         | 0.118          | 0.108          | 0.137          |
| 14         | 0              | -0.009         | 0.007          | -0.106         | -0.114         | -0.071         | 0.094          | 0.076          | 0.089          |
| 15         | 0              | -0.032         | -0.005         | -0.011         | -0.022         | -0.013         | 0.01           | -0.019         | 0.006          |

<table>
<thead>
<tr>
<th></th>
<th>max DNLE</th>
<th>min DNLE</th>
<th>spec</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>0.0698</td>
<td>0.02</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>0.1157</td>
<td>0.165</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>0.073</td>
<td>0.172</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>0.075</td>
<td>0.157</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>0.0787</td>
<td>0.093</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>0.147</td>
<td>0.147</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>0.137</td>
<td>0.137</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>0.172</td>
<td>0.172</td>
<td>0.1</td>
</tr>
</tbody>
</table>
Table 3-5. Simulation results of estimated DFT of I channel

<table>
<thead>
<tr>
<th>DFT</th>
<th>Complex output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_1 \text{DFT}(G_1 e^{j\lambda})$</td>
<td>3.445e+02-5.786e+01i</td>
</tr>
<tr>
<td>$I_2 \text{DFT}(G_2 e^{j\lambda})$</td>
<td>5.096e+02-1.091e+03i</td>
</tr>
<tr>
<td>$I_3 \text{DFT}(G_3 e^{j\lambda})$</td>
<td>1.548e+02-1.848e+03i</td>
</tr>
<tr>
<td>$I_4 \text{DFT}(G_4 e^{j\lambda})$</td>
<td>-3.14e+02-5.57e+02i</td>
</tr>
<tr>
<td>$I_5 \text{DFT}(G_5 e^{j\lambda})$</td>
<td>-3.98e+03-4.45e+03i</td>
</tr>
<tr>
<td>$I_6 \text{DFT}(G_6 e^{j\lambda})$</td>
<td>-8.33e+04-8.8598e+04i</td>
</tr>
<tr>
<td>$I_7 \text{DFT}(G_7 e^{j\lambda})$</td>
<td>-1.314e+06-4.947e+05i</td>
</tr>
<tr>
<td>$I_8 \text{DFT}(G_8 e^{j\lambda})$</td>
<td>-3.141e+05-9.84e+04i</td>
</tr>
</tbody>
</table>

Table 3-6. Simulation results of estimated ratio of DFT’s

| Ratio                  | $\frac{|I_1 \text{DFT}(G_n e^{j\lambda})|}{|I_1 \text{DFT}(G_n e^{j\lambda})|}$ |
|------------------------|------------------------------------------|
| Ratio(1,0)             | 3.497e-01 - 1.428e-02i                    |
| Ratio(2,1)             | 1.956e+00 - 2.84i                         |
| Ratio(3,2)             | 1.444e+00 - 5.326e-01i                    |
| Ratio(4,3)             | 2.852e-01 - 1.941e-01i                    |
| Ratio(5,4)             | 9.124 - 1.996i                            |
| Ratio(6,5)             | 2.033e+01 - 5.1499e-01i                   |
| Ratio(7,6)             | 1.0363e+01 - 5.081i                       |
| Ratio(8,7)             | 2.341e-01 - 1.320e-02i                    |

Table 3-7. Simulation results showing error in estimation

| Ratio                  | $\frac{|I_1 \text{DFT}(G_n e^{j\lambda})|}{|I_1 \text{DFT}(G_n e^{j\lambda})|}$ |
|------------------------|------------------------------------------|
| Ratio(1,0)             | 3.497e-01 - 1.428e-02i                    |
| Ratio(2,1)             | 1.956e+00 - 2.84i                         |
| Ratio(3,2)             | 1.444e+00 - 5.326e-01i                    |
| Ratio(4,3)             | 2.852e-01 - 1.941e-01i                    |
| Ratio(5,4)             | 9.124 - 1.996i                            |
| Ratio(6,5)             | 2.033e+01 - 5.1499e-01i                   |
| Ratio(7,6)             | 1.0363e+01 - 5.081i                       |
| Ratio(8,7)             | 2.341e-01 - 1.320e-02i                    |
Table 3-8. Simulation results of phase estimate error

| Ratio    | \[ \frac{|I_\text{DFT}(G_n e^{j\lambda})|}{|I_\text{DFT}(G_n e^{j\lambda})|} \] |
|----------|----------------------------------------------------------------------------------|
| Ratio(1,0) | 3.497e-01 - 1.428e-02i                                                          |
| Ratio(2,1) | 1.956e+00 - 2.84i                                                                |
| Ratio(3,2) | 1.444e+00 - 5.326e-01i                                                           |
| Ratio(4,3) | 2.852e-01 - 1.941e-01i                                                           |
| Ratio(5,4) | 9.124 - 1.996i                                                                   |
| Ratio(6,5) | 2.033e+01 - 5.1499e-01i                                                          |
| Ratio(7,6) | 1.0363e+01 - 5.081i                                                               |
| Ratio(8,7) | 2.341e-01 - 1.320e-02i                                                            |
4.1 Introduction

As a continuation of system architectures presented in Chapter 2 and Chapter 3, this Chapter describes a DSP technique that alters the transmit signal power of a mobile device depending on the request from the base-station. To recall, Chapter 2 describes a technique to dynamically track for gain variations caused due to analog and RF circuit imperfections at different operating conditions. Chapter 3 presents a technique to compensate for gain errors caused due to differential nonlinearities and relative phase shifts in the RF components of the mobile device and hence preserving the relative power level accuracy for any mobile device. This chapter describes a Dynamic Gain Control technique (DSP-GC) along with corresponding hardware implementation details to dynamically control the absolute signal power of any mobile device. The primary motivation of this technique is to make the system converge faster by making the closed-loop system resilient to large signal variances which are introduced due to higher order modulation schemes. Another motivation for this approach is to adopt possible DSP structures to reduce gate area.

As a function of increasing data rates, adoption of higher order modulation schemes and rapid changes in channel conditions from voice to data and video, the variance of the signal transmitted increases drastically. This result in both higher peak to average ratio (PAR) [43], [46] and peak to null (PTN) ratio at the output of the mobile device as shown in Figure 4-1a. As an example in WCDMA modulation scheme, a mobile device transmitting voice information has a PAR of 3.2dB while the PAR of the transmit signal increases to 4.2dB when data is being transmitted. As mentioned in
Chapter 2 in systems employing closed-loop controller [52-55],[65-68], to track for average level of gain variations, the loop dynamics will be dramatically influenced by the transmit signal variance. This is because when an RF feed back is applied, the error signal between the reference signal and the feedback signal will have the corresponding large variances which will affect loop stability.

To preserve both the closed-loop stability and to meet the settling time requirements during these higher signal variance conditions, there is a need for minimizing the signal variance at the input to the controller. This will make the loop less responsive to abrupt signal shifts and hence provide more predictable gain control. The described DSP-GC system architecture makes use of an adaptive filter to reduce the signal variance of the error signal between the reference and the feedback path. The output of the adaptive filter is then fed into an integral controller with programmable gains to accumulate the error signal and provide the controller output. This approach reduces abrupt signal fluctuations at the input to the controller and makes the loop more predictable. The integral controller is used to perform average gain tracking while the adaptive filter is used to perform instantaneous sample filtering.

**4.2 System Architecture for the DSP-GC Algorithm**

The system architecture [14] of the DSP-GC algorithm to perform absolute gain and power change is shown in Figure 4-1b. As described in earlier chapters, a wireless transmitter is used as an application on which the DSP-GC algorithm is implemented.

As shown in Figure 4-1b, assume that the base band I channel and Q channel signals are represented by

\[ I(n) = dI \cos(\omega_{bb}n) \]  

(4-1)
\[ Q(n) = d1 \times \sin((\omega_{bb})n) \]  \hspace{1cm} (4-2)

Where \( d1 \) is the digital gain, \( \omega_{bb} \) is the baseband signal frequency. The signals \( I(n) \) and \( Q(n) \) are converted to analog signals \( I(t) \) and \( Q(t) \) by the DAC present in the transmit path. The signals are then up converted by the RF modulator. The complex signal at the input to the RF modulator is represented as

\[ \text{modin}(t) = d1 \times [(\cos((\omega_{bb})t) + j \sin((\omega_{bb})t))] \]  \hspace{1cm} (4-3)

The input to the modulator is then up converted to RF frequency and can be expressed as

\[ \text{modout}(t) = d1 \times [(\cos((\omega_{bb})t) + j \sin((\omega_{bb})t + \phi))] e^{j\omega_{rf}t} \]  \hspace{1cm} (4-4)

where \( \omega_{rf} \) is the up conversion frequency. The output of the modulator is amplified by the PA and transmitted over the antenna. The signal transmitted over the antenna can be represented as

\[ PA(t) = G1 \times d1 \times [(\cos((\omega_{bb})t + \phi) + j \sin((\omega_{bb})t + \phi))] e^{j\omega_{rf}t} \]  \hspace{1cm} (4-5)

where, \( G1 \) is the power amplifier gain.

The magnitude of the power in dBm (dB with respect to 1mW) at the output of the PA is represented as

\[ P_{out}(dBm) = 10 \log(G1d1[\sqrt{I^2 + Q^2}]) + 30 \text{ dBm} \]  \hspace{1cm} (4-6)

The output of the power amplifier is converted into an equivalent DC voltage signal by using an RF power detector which converts RF power (dBm) into average DC voltage. The power detector outputs linear DC voltage for RF input power in dBm. The input vs. output transfer function is shown in Figure 4-15. The detector chosen in this technique
is an envelope detector and hence the output of the detector in volts is approximated to be the envelope of the signal power and denoted as

\[ v(t) = \beta \left[ \text{abs}(I^2 + Q^2) \right] \]

where, \( \beta \) is the feedback path gain. The analog signal gets digitized by the ADC present in the feedback path. The RF signal is feedback through a power detector and converted into a digital equivalent signal \( A_k \). The digital signal \( A_k \) is compared to a reference signal, \( D_k = pwr \times d_k \) where \( pwr \) corresponds to the amplitude of the reference signal in accordance to the desired power level at the antenna and \( d_k \) is the adopted reference signal. The reference signal \( d_k \) is either a step input or a normalized raised cosine ramp signal whose final value is dictated by \( pwr \). When \( pwr \) is changed the steady state value of the loop output is changed as described by Equations 2-11. The error signal between the reference signal and the feedback signal, denoted by \( E_k = D_k - A_k \) is fed into a \( N \) tap adaptive filter whose output is fed into an integral controller. The adaptive filter acts as a sample based moving average filter that reduces the large signal variances of the error signal which are introduced due to higher order modulation schemes. As the variance of the signal is filtered out dynamically, before entering into the integral controller, this technique is found to yield faster convergence and more predictable closed-loop performance. A price that is paid for is reduction in gain margin as the loop delay increases when an adaptive filter is used. The gain margin for the system under consideration is defined as the difference between the maximum and minimum controller gains that can be used to maintain closed-loop stability. The goal is to have a large gain margin as that will make the closed-loop system less sensitive to
changes in controller gains. As will be described in later sections, increase in loop delay
decreases the loop gain margin. However, sufficient gain margin can be maintained by
appropriately choosing the number of taps of the adaptive filter and the operating
sample rate of the closed-loop system. The components of the DSP-GC technique
hardware are

- $N$ Tap adaptive filter [27]
- Integral controller with programmable loop gains $K_i$
- Coefficients update block
- Multi-rate conversion logic.
- Signal multipliers.

The operation of the algorithm is described as follows. Assume that the reference
signal level is represented by $D_k = pwr \times d_k$, where $pwr$ is the signal magnitude of the
desired reference and $d_k$ is a unit step input. The error at every sample $k$ is defined as
the difference between the desired signal level and the feedback signal level.

$$E_k = D_k - A_k,$$  

Equations. Figure 4-2 shows a detailed schematic of the adaptive DSP hardware that
employs the LMS tracking technique. The error signal $E_k$ feeds a $N$ tap FIR filter, whose
taps are updated on a sample by sample basis. The number of taps are programmable
to $N = 2, 3, 4, 5$, or 6 taps.

It is found that the modulation PAR of the feedback signal was as high as 7.2dB
when higher order modulation schemes such as WCDMA, CDMA and OFDM was used.
Hence it is critical to reduce the variance of the error signal to result in faster convergence. The difference \( E_k = D_k - A_k \) is calculated on a sample by sample basis.

For each iteration, \( k \) the output of the filter \( S_k \) is updated. The output of the adaptive filter \( S_k \) passes through an integral controller that accumulates the error signal to generate a gain correction signal \( acc(k) \) as the loop output signal. The gain correction signal is applied to the transmit path to perform the desired amount of gain change as signaled by the baseband processor.

Based on simulations performed, it was found that the trade-off between the loop stability, gain margin and loop settling time was reached by choosing appropriate integral gains \( K_j \), the convergence factor \( \mu \) and the number of taps of the adaptive filter. Assume at iteration \( k = 0 \), each of the registers of the adaptive filter is initialized to zero. Hence for \( k = 2 \) taps filter, the weight update equations can be represented as shown in Table 4-1. Assume for tap \( N = 1 \), the first weight vector at iteration \( k = 0 \) is represented as

\[
 w_{i0} = 0 \quad \text{for} \quad N = 1, k = 0.
\]

For filter tap \( N = 1 \), iterating \( k \), results in

\[
 w_{11} = w_{10} + \mu E_0^2 = \mu E_0^2 \\
 w_{12} = w_{11} + \mu E_1^2 = \mu E_0^2 + \mu E_1^2 = \mu [E_0^2 + E_1^2] \\
 w_{13} = w_{12} + \mu E_2^2 = \mu E_0^2 + \mu E_1^2 + \mu E_2^2 = \mu [E_0^2 + E_1^2 + E_2^2] \\
 \vdots \\
 w_{1n} = w_{1(n-1)} + \mu E_{n-1}^2 = \mu [E_0^2 + E_1^2 + E_2^2 + \ldots E_{n-1}^2] \quad (4-10a)
\]

In general for \( n \) samples, in general the weights are represented as
The output of the adaptive filter $S_k$ for a 2 tap filter ($N = 2$) can be represented as

$$S_k = w_{(1)k}^T E_k + w_{(2)k}^T E_{k-1}$$  \hspace{1cm} (4-10c)

Iterating $k$ in Equation 4-10c results in

$$k = 0, \quad S_0 = w_{10}^T E_0 + w_{20}^T E_{-1}$$
$$k = 1, \quad S_1 = w_{11}^T E_1 + w_{21}^T E_0$$
$$k = 2, \quad S_2 = w_{12}^T E_2 + w_{22}^T E_1$$
$$\ldots$$
$$S_n = [w_{(1)n}^T E_n + w_{(2)n}^T E_{n-1}]$$

Substituting Equation 4-10b in 4-10c results in

$$S_n = \mu \left( \sum_{k=0}^{n-1} E_k^2 E_n + \sum_{k=0}^{n-1} E_k^2 E_{n-1} \right)$$  \hspace{1cm} (4-11)

$$= \mu \left[ \sum_{k=0}^{n-1} E_k^2 (E_n + E_{n-1}) \right]$$

Equation 4-11 shows that the input to accumulator at every iteration is weighted average of past samples of error signal and thus reducing the variance of the error signal. The output of the adaptive filter $S_n$ is multiplied by the integral gain $K_i$ before it reaches the accumulator. Hence, the input to the accumulator at iteration $n$ is represented as $\text{acc}_\text{in}(n)$ which can be defined as

$$\text{acc}_\text{in}(n) = K_i S_n$$

$$\text{acc}_\text{in}(n) = K_i \mu \left[ \sum_{k=0}^{n-1} E_k^2 (E_n + E_{n-1}) \right]$$  \hspace{1cm} (4-12)

Equation 4-12 shows that the effect of convergence factor on the output of the integrator is same as the integral gains. It was found that higher the integral gains and the convergence factor, faster is the rate of convergence but lower is the loop stability.
4.3 Loop Tuning Techniques

The three primary system constraints that require attention while designing closed-loop system are convergence time, loop stability and gain margin. As shown in Figure 4-3, the critical loop system parameters which influence the above mentioned constraints are

- Feedback loop delay
- Integral gains
- Feedback gains
- Amplitude of the reference signal (depends on the power levels at the antenna).
- Operating regions of the power detector curve. (feedback path linearity).

The system specifications for which this algorithm is used are as described below.

- Peak overshoot specification of less than 3dB.
- Loop settling time of less than 40usec.
- Rise time of closed-loop response is less than 10usec.

The goal of this control loop is to reduce the average of the error signal between the reference signal and the feedback signal. Hence an integral controller with programmable gains is chosen for this application. However this algorithm has also been studied with proportional, integral and derivative controllers. Sections 4.3.1 and 4.3.2 describe briefly about the classical open loop and closed-loop techniques that help in determining the appropriate controller gains that will guarantee system stability.

4.3.1 Method I - Reference Model Based Loop Tuning

This method of loop tuning is used when the open loop plant transfer function \( G(s) \) and the closed-loop reference transfer function \( H(s) \) is known. Based on the knowledge of \( H(s) \) and \( G(s) \) the controller transfer function \( G_c(s) \) can be estimated as described below. Assume a system as shown in Figure 4-4. Let the input to the system is \( R(s) \), \( Y(s) \) is the system output, \( G_c(s) \) is the controller transfer function and \( G(s) \) is the
known plant transfer function. The goal is to estimate the controller gains which is a part
of \(G_c(s)\). The closed-loop transfer function is represented by 
\[
H(s) = \frac{G G_c}{1 + G G_c}
\]
and hence
\[
H(s) = \frac{Y(s)}{R(s)} = \frac{G G_c}{1 + G G_c} \quad (4-14)
\]
Assume that the known open loop plant transfer function is a second order system and can be represented as
\[
G(s) = \frac{k}{(1 + T_1 S)(1 + T_2 S)}
\]
and the closed-loop reference model transfer function is represented by
\[
H(s) = Y(s) = \frac{1}{1 + T_c S} \quad (4-15)
\]
Equating (4-14) and (4-15), we get
\[
\frac{1}{1 + T_c S} = \frac{G G_c}{1 + G G_c}
\]
\[
1 + G G_c = G G_c (1 + T_c S)
\]
\[
G_c(s) = \frac{1}{s T_c G(s)}
\]
\[
G_c(s) = \frac{1 + s(T_1 + T_2) + s^2 T_1 T_2}{s T_c K}
\]
\[
G_c(s) = \frac{T_1 + T_2}{K_c} \left[ 1 + \frac{1}{(T_1 + T_2)s} + \frac{(T_1 T_2)s}{(T_1 + T_2)} \right] \quad (4-16)
\]
Hence by knowing the desired system open loop transfer function, \(T_1, T_2\) we can estimate the value for integral, derivative and proportional gains. This is simple method to estimate the controller parameters when the open loop and desired closed-loop response is known.
4.3.2 Method II- Open Loop Tuning Based On Unknown Plant Transfer Function

In most of the cases, both the plant transfer function and the closed-loop transfer function of the system are unknown. In such situations, one of the classical methods adopted was to break the loop open and determine the step response of the open loop plant. Figure 4-5 shows the step response of the open loop transfer function. From this empirical result the slope $M$, the time delay $T_d$ and $k$, the final value of the response is calculated. This method was described by Zeigler Nicholas [76].

$$K_p = \frac{0.9}{MT_d} \quad (4-17a)$$

$$K_i = 3.33T_d$$

and by using Cohen Coon’s method [77]

$$K_p = \frac{1}{MT_d} \left[ 0.9 + \frac{T_d}{12\tau} \right]$$

$$K_i = 3.33T_d \left[ \frac{1 + \frac{T_d}{11\tau}}{1 + \frac{11T_d}{8\tau}} \right] \quad (4-17b)$$

Hence the proportional and the integral gains are calculated.

4.3.3 Method III - Loop Tuning Based on Closed-loop Cycling

In certain situations, the loop cannot be broken for analysis and will be available as a closed-loop black box where an input can be applied and the system response can be obtained. In these cases, another closed-loop tuning loop tuning technique was described by Zeigler and Nicholas [76]. The approach is defined as follows. Assume that a closed-loop system is implemented using a PID controller.

- Decrease the integral gains and the derivative gains.
- Apply a suitable proportional gain
• Apply a step response as the input and observe the system output.

• Change the proportional gain iteratively until loop oscillates with a period \( T \) and amplitude \( A \) as shown in Figure 4-6.

• The smallest proportional gain that makes the output of the loop to oscillate is called as the ultimate gain, \( K_u \).

Based on the estimation of \( K_u \) and the time period of oscillation \( T \), the integral and the derivative gains are calculated as described. Let \( K_u = K_{p\_ultimate} \), is the smallest proportional gain used when the loop response starts to oscillate. Let the amplitude of the oscillation is given by \( A \) and the time period is represented by \( T \). By characterizing \( K_u, A \) and \( T \) based on Ziegler and Nicholas approach the PID control parameters are calculated as described below.

\[
K_p = 0.6K_u \\
Ki = 0.5T \\
Kd = 0.125T
\]  

(4-18)

The above mentioned techniques can be used to determine a nominal loop gain settings and further manual automation and simulations should be used to determine the most accurate settings. In the described DSP-GC technique a combination of the above mentioned techniques are used to estimate nominal values for the integral gains and convergence factors analytically. The values calculated are then used as initial estimates in system simulations based on which the final accurate value of integral gains and convergence factors were obtained. The following section describes a novel method to predict the controller gains for an unknown \( N^{th} \) order closed-loop system.
4.3.4 Method IV - Implemented Loop Tuning Technique Based on Closed-loop Stability Constraint

This section describes a novel method by which the controller gains are estimated based on pole placement stability constraint. Figure 4-7 shows a generic block diagram of a closed-loop system with an integral controller. In $z$ domain, the closed-loop parameters involved in the analysis are represented as follows.

- The unknown open loop plant transfer function is denoted as $G_p(z)$,
- $K_i$ is the integral gain of the controller employed,
- $R(z)$ is the system input represented in Z domain,
- $Y(z)$ is the system output,
- $E(z)$ is the error between the reference signal $R(z)$ and the feedback signal $Y(z)$.
- $\beta$ is the feedback gain
- $DZ^{-D}$ is the delay through the feedback path.

The primary goal of this method is to estimate the maximum value of integral gain $K_{i,max}$ above which the system become unstable. The significance of adopting this approach is that this technique does not require prior knowledge of the open loop system transfer function. The steady state gain and the delay can be characterized as a lab experiment by applying a unit step input to the open loop system $G_p(z)$ and by monitoring the system output. At steady state, irrespective of the order of the open loop plant transfer function $G_p(z)$, it can be represented as $G_p(z)=G_{ss}z^{-L}$, where $G_{ss}$ is the open loop steady state gain of the plant and $z^{-L}$ is open loop delay. Hence the open loop plant gain ($G_{ss}$) and the delay ($z^{-L}$) can be computed based on a step input analysis. Based on the estimated values for $G_{ss}$ and $z^{-L}$, the system block diagram at steady state can be represented as shown in Figure 4-8. The next step is to derive the expression of the closed-loop transfer function $H(z)$. The system output is represented as

$$H(z) = \frac{Y(z)}{R(z)}$$
\[ Y(z) = \left[ \frac{E(z)K_i z^{-1} G_{ss} z^{-L}}{1 - z^{-1}} \right] \quad (4.19a) \]

where the error signal \( E(z) \) and the feedback signal \( A(z) \) is represented as
\[ E(z) = R(z) - A(z) \quad (4.19b) \]
\[ A(z) = Y(z) \beta z^{-D} \quad (4.19c) \]

Combining Equation 4.19b, 4.19c results in
\[ E(z) = R(z) - \beta z^{-D} Y(z) \quad (4.19d) \]

Using equations, 4.19a, 4.19d, the closed-loop system output \( Y(z) \) is represented as
\[
Y(z) = \left[ R(z) - A(z) \right] \left[ \frac{K_i z^{-1} G_{ss}}{1 - z^{-1}} \right] \\
Y(z) = \left[ R(z) - Y(z) \beta z^{-D} \right] \left[ \frac{K_i z^{-1} G_{ss}}{1 - z^{-1}} \right] \\
Y(z) - z^{-1} Y(z) = \left[ R(z) G_{ss} K_i z^{-L-1} \right] - \left[ Y(z) \beta G_{ss} K_i z^{-D-L-1} \right] \\
Y(z)[1 - z^{-1} + \beta G_{ss} K_i z^{-D-L-1}] = R(z) G_{ss} K_i z^{-L-1} \\
\frac{Y(z)}{R(z)} = H(z) = \frac{G_{ss} K_i z^{-L-1}}{[1 - z^{-1} + \beta G_{ss} K_i z^{-D-L-1}]} \quad (4.19e)
\]

In order to represent 4.19e in powers of \( z \), we multiply the numerator and denominator by \( \left[ \frac{z^{(D+L+1)}}{z^{(D+L+1)}} \right] \). This result in
\[
\frac{Y(z)}{R(z)} = H(z) = \frac{G_{ss} K_i z^{-L-1}}{[1 - z^{-1} + \beta G_p K_i z^{-D-L-1}] \left[ \frac{z^{(D+L+1)}}{z^{(D+L+1)}} \right]} \\
= \frac{G_{ss} K_i z^{D}}{[z^{D+L+1} - z^{D+L} + \beta G_p K_i]} \quad (4.20)
\]

Based on the \( z \) domain closed-loop stability constraint, the system \( H(z) \) as described by Equation 4.20 is stable if the poles of the transfer function lie within the unity circle.
Based on this constraint, the absolute value of the roots of the denominator of $H(z)$ should be less than 1. If this condition is true, then the system will have bounded output $y(n)$ for an input $x(n)$. The poles of the transfer function are estimated by equating the roots of the denominator part of Equation 4-20 to zero. Equating the denominator to be equal to 0 results in

$$z^{D+L+1} - z^{D+L} + \beta G_{ss} K_I = 0$$  \hspace{1cm} (4-21)

The values for $\beta, G_{ss}, D$ and $L$ are substituted based on open loop system characterization. In order to solve Equation 4-21 for the $K_{I_{\text{max}}}$, a random initial estimate of $K_I$ is assumed. The roots of the Equation 4-21 are found by known numerical methods [78]. These calculated roots represent the poles $p_k, (k = 0, ..., D + L + 1)$ of the system function $H(z)$. Once the poles are estimated, the magnitude of the maximum pole $P_{\text{max, abs}} = \text{magnitude}(\text{max} \ p_k)$ is calculated. If $P_{\text{max, abs}} > 1.0$, then the integral gain $K_I$ is decreased and the process is repeated. If $P_{\text{max, abs}} < 1.0$, then the corresponding integral gain $K_I$ is denoted as the maximum value of integral gain $K_{I_{\text{max}}}$ above which the system becomes unstable. The DSP algorithm than can be implemented in the radio software is described in Figure 4-9.

As an example, assume that the plant transfer function is

$$G_p(s) = \frac{250.23(s + 0.8782)(s + 0.1212)(s + 0.4523)(s + 0.4912)}{(s + 0.2)(s + 0.892)(s + 0.9235)(s^3 + 0.9235s^2 + 0.234s + 0.02)(s^2 + 0.891s + 0.9234)}$$ \hspace{1cm} (4-22)

As a first step, the steady state gain and the delay of the unknown transfer function is found by a step input to the open loop system. The step response of the open loop system $G_p(s)$ is shown in Figure 4-10. Based on this measurement, the steady state
gain $G_{ss}$ is found to be 44.67 and the open loop delay is found to be $L = 18$ samples. Hence, the estimated system parameters are

- Steady state open loop gain, $G_{ss} = 44.67$,
- Forward path delay, $L = 18$
- Feedback path delay, $D = 10$ (feedback path delay is known based on the digital filters used).
- Programmed feedback gain $\beta = 0.5$ (-6dB)

Substituting the values in the characteristic Equation $z^{D+L+} - z^{D+L} + \beta G_{ss} K_f$ results in

$$z^{29} - z^{28} + (0.5)(44.67)(K_f) = 0$$

(4-23)

By employing the algorithm as illustrated in Figure 4-9, the value of $K_f$ for which $P_{max_{abr}} = \text{magnitude}(\max p_k) < 1.0$ is estimated. The value of $K_{I_{max}}$ below which the system becomes stable is found to be 0.0014 (-57.07dB). The 29 estimated poles corresponding to $K_{I_{max}}$ as the controller gain are tabulated in Table 4-2. Figure 4-11 shows the plot of 29 poles which lie inside the unit circle. Figure 4-12 shows the reference and the feedback signal, the loop error signal and the closed-loop step response with the predicted controller gains of $K_f < K_{I_{max}}$. Depending on the system overshoot requirements, the integral gains can be further adjusted.

**4.4 Closed-loop Delay and Loop Gain Margin Analysis**

After estimating suitable controller gains $K_f$, the effect of additional loop delay on the stability of the closed-loop system is studied. The system architecture as described by the DSP-GC algorithm can be simplified into a block diagram shown in Figure 4-13. The reference signal $R(z)$ is compared with the feedback signal $A(z)$. The error signal $E(z)$
between the reference signal and the feedback signal goes into the controller \( G_c(z) \). The output of the controller drives the unknown plant \( G_p(z) \). The unknown plant in the system under consideration consists of the gain amplifier and the analog components in the transmit path of the mobile. When the closed-loop power control occurs these components are already enabled and the transient behavior can be neglected. Thus, considering the steady state behavior of the unknown plant, we can model this as a gain stage. The feedback path which consists of the power detector, the digitizer, the analog filter can be modeled as a gain stage \( \beta \) and a delay \( D \). Hence the feedback path can be represented as \( \beta z^{-D} \).

### 4.4.1 Effect of Loop Delay

Analysis of the loop stability with increasing loop delay is essential to decide the operating sampling frequency of the ADC, the digital components and the appropriate bandwidths of the analog filters in the feedback path. Assume an integral controller is used for the sake of analysis. Hence, the transfer function of the integral controller can be represented as

\[
G_c(z) = K_i \frac{z^{-1}}{1 - z^{-1}}, \text{ where } K_i \text{ is the integral gain.}
\]

The closed-loop system equations with the integral controller can be described as follows.

\[
Y(z) = \left[ \frac{E(z)K_i z^{-1}G_p}{1 - z^{-1}} \right]
\]

\[
E(z) = R(z) - A(z)
\]

\[A(z) = Y(z) \beta z^{-D}\]
Hence,

$$Y(z) = [R(z) - A(z)] \left[ \frac{K_f z^{-1} G_p}{1 - z^{-1}} \right]$$

$$\frac{Y(z)}{R(z)} = H(z) = \frac{K_f G_p z^{-1}}{1 + \beta G_p K_f z^{-D-I-1} - z^{-1}} \tag{4 - 24b}$$

It is evident from Equation 4-24b that the closed-loop stability is a function of the feedback loop delay, $D$ the integral gain $K_i$ and the feedback gain $\beta$. The loop delay depends both on the operating digital sample rate sample rate $F_s$ and on the delay introduced by the analog components along the path. Typical loop delay calculations for the implemented architecture are shown in Table 4-3. It is essential to estimate the minimum value of $D = D_{\text{min}}$ above which the system will reach the verge of instability.

The loop stability with increasing loop delays is analyzed by estimating the poles of the transfer function as described in Equation 4-24b. Figures 4-14, 4-15, 4-16 and 4-17 shows the pole zero plot for the closed-loop transfer function with the feedback loop delay $D = 1, 3, 7, 9, 13, 17, 19, 21, 24, 26, 28, 31, 39, 45, 52$ and $58$ samples at the chosen sample rate $F_s$ for the transfer function represented by

$$\frac{Y(z)}{R(z)} = H(z) = \frac{K_f G_p z^{-1}}{1 + \beta G_p K_f z^{-D-I-1} - z^{-1}}, \text{ where}$$

$$K_i = -26dB,(0.046), G_p = 20dB,(9) \text{ and } \beta = -16dB,(0.16).$$

As shown in Figure 4-14, 4-15, 4-16 and 4-17 it is clear that for a fixed integral gain, the system stability decreases with increasing loop delay because the magnitude of the poles increases starts moving away from the center of the unit circle. The calculated delay through the loop is around $750nsec$ based on calculations as shown in Table 4-3. Extensive simulations have been performed to guarantee the loop stability in the presence of additional delays. Figure 4-
The steps response of the closed-loop system with increasing loop delay. As we can observe that the delay increases the loop stability decreases. Based on system simulations and empirical analysis it has been found that the loop can handle up to a maximum delay of 2.5 usec to meet the 40 usec settling time and the 3dB overshoot specifications. The adaptive filter implemented was used to reduce the signal variance and the integral controller was used to perform average gain tracking. As the goal of this loop was to perform average power tracking an appropriately tuned integral controller was efficient enough to result in the desired system metrics. This also reduced both the tuning process and the implementation complexity.

### 4.4.2 Gain Margin Analysis

Once a nominal value of loop delay $D$ which will guarantee loop stability is known, for that particular value of loop delay, there exists a maximum and a minimum value of integral gain over which the system is stable. Figure 4-19 and Figure 4-20 shows the pole zero plot for a system with a loop delay of $D = 13$ samples and as a function of varying integral gains. It is clear from Figure 4-19 and Figure 4-20 that as the integral gains are increased, the closed-loop stability decreases. Based on this observation it can be concluded that system becomes over damped and sluggish when the programmed integral gain is below a certain value (err_gain_min) and the loop becomes unstable and oscillates when the programmed gain is greater than a certain value (err_gain_max). As defined earlier section, the range of values of integral gains between the err_gain_min and err_gain_max for which the system is stable is known as the gain margin. The integral gains $K$, and the convergence factor $\mu$ employed in the tracking algorithm determine the rate of convergence and the stability of the closed-loop
system. Depending on the settling time requirements of the system protocol, the integral gains of the controller and the convergence factor of the adaptive filter are selected that will result in the desired peak overshoot, the settling time and the steady state error. It can be observed from Figure 4-20 that as the integral gains are increased above -20dB, the system becomes unstable.

Figure 4-21 shows the measured transfer function of the power detector which plots the input $P_{out}$ (dBm) vs. quantized feedback signal. Based on the measured characteristics, it is clear that the slope of the power detector is smaller at lower input power levels and larger at higher power levels. In the presence of such non-linear systems within the closed-loop function, appropriate loop gain programming strategies have to be adopted to meet the desired system performance. As a strategy, in order to compensate for sluggish response at lower power levels, a higher integral gain (less attenuation) is used to make the loop respond faster. As the slope increases at higher power levels, a relatively lower integral gain (higher attenuation) is used to satisfy the desired system requirements of less than 3dB overshoot and 40usec settling time. Hence the closed-loop operating range is sub-divided into low, high and mid power control regions. As a result of the non-linear open loop characteristics there are three regions over which the integral gains are chosen over the power control range of 0dBm to 24dBm transmit power level.

System simulations and lab measurements conclude that for power levels between 0dBm and 6dBm, an integral gain of -20dB is used and for the range of power levels between 6dBm to 11dBm an integral gain of -40dB is used. Similarly, for a range of power levels between 12dBm to 15dBm an integral gain of -50dB is used. In addition to
this, as was explained analytically in Chapter 2, depending on the amount of power change, the controller gains are adjusted to maintain similar loop stability and gain margin over the entire range of closed-loop operation.

Based on simulations and lab measurements it has been found that the loop gain margin decreases with increasing loop delay. Figure 4-22 shows the range of values for integral gain allowed for particular target power decreases as the loop delay increases. It is clear from Figure 4-22 that the gain margin is around 20 dB when the feedback loop delay 200nsec and the gain margin decreased to around 14dB when the loop delay increases to 1.92usec. In this application the introduction of adaptive filter adds 4 samples of delay into the system. However this additional delay is tolerated based on the fact that faster settling time is obtained when the adaptive filter is used.

4.5 System Simulation and Lab Measurement Results
System simulations were performed for the implemented DSP-GC technique with the system models including

- RF analog circuitry
- Analog feedback path
- Additive noise
- Digital transmit path models
- Digital implementation of the system architecture.

Sections 4.5.1 and 4.5.2 describe the system simulations and lab measurement results obtained by implementing the DSP-DGT algorithm.

4.5.1 System Simulations of the DSP-GC Method

The system simulations were performed with simulation tools Matlab and SPW. The simulation models assumes that the modulation format was either constant envelope such as Gaussian minimum shift keying (GMSK) or non-constant envelope
schemes such as code-division-multiple access. (CDMA). The reference signal is assumed to be a digital ramp signal stored in a look up table ROM implementation. In these system simulations a raised cosine signal is used as a reference signal $d_k$. The desired target power $D_k = pwr * d_k$ corresponding to the required mobile output power level is known based on prior calibration. The DAC is assumed to operate at 62.4MHz. The simulations were performed with the fixed point digital circuits, the RF and analog system models in the presence of noise and non-linear impairments. Various signal sources employing modulation schemes such as Binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), Gaussian minimum shift keying (GMSK) were used to simulate the implemented algorithm. By employing various modulation schemes with various PAR [23] the closed-loop dynamics such as the loop stability and steady state error is analyzed. Figure 4-23 shows the reference signal $D_k$ which is a ramp signal multiplied by the desired power value, $pwr$. The corresponding feedback signal $A_k$ is shown to track the reference signal $D_k$. The error signal $E_k$ which is the difference between the reference signal and the feedback signal $E_k = D_k - A_k$ is found to settle to zero depending on the integral gains and the convergence factor programmed in the loop. The integral controller accumulates the output of the adaptive filter as described by $acc(k)$. This signal is then converted to analog signal and either used to perform gain tracking on the digital baseband signal or can be used to control the bias voltage on the variable gain amplifier [9],[38]. Figure 4-23 illustrates that the error signal is positive because the reference signal is greater than the feedback signal. This denotes that more gain has to be added to the loop to increase the transmit power of the mobile device, thus resulting in power change in the positive direction.
Figure 4-24 shows a situation where the mobile device has been signaled to ramp down the target power. Hence the reference signal has a ramp down profile from the present reference value to a lower reference value. Since the feedback signal always lags the reference signal, the error between the feedback signal and the reference signal becomes negative and the closed-loop system tries to bring the error back to zero at steady state. Since the error signal is averaged and accumulated the closed-loop system provides an output which reduces the gain of the forward path and hence reduces the output power of the mobile device. Based on simulations, it was found that the loop takes 30-35 usec to adapt for +/- 7.5 dB of power change. Figure 4-25 shows the antenna power as a function of the LMS adaptation. The plot shows that transmit power ramp up and ramps down, the area under the error signal is minimized by the adaptive filter on a sample by sample basis. The filter weights are cleared after the power transition ends. Figure 4-26 show the loop dynamics of the feedback signal and the closed-loop error signal as a function of the convergence factor. The goal of the adaptive algorithm is to dynamically compensate for the analog gain changes introduced on a sample by sample basis. The plot s5 in Figure 4-26 shows the adaptation of the error signal as a function of convergence factor.

4.5.2 Lab Measurements of the DSP-GC Adaptive Algorithm

The measurement set up as explained in Chapter 2 is used to capture the output of the controller on the Tektronix oscilloscope and the CMU2000 is used to capture the RF power output of the mobile device. Figure 4-27 shows the analog output of the closed-loop system captured by the Tektronix oscilloscope. The analog output is used to control the bias of the PA or the VGA to perform gain control. Figure 4-27 shows that the closed-loop system responds to two consecutive power change commands. The
controller and the loop operation corresponding to the two cases are described below in detail.

Case 1: Mobile Power change in the positive direction - As explained in earlier sections, when the mobile is requested to increase its transmitted power, the reference power programmed will be greater than the actual feedback power. During the closed-loop adaptation, this will result in a positive error signal. This positive error signal is then accumulated by the adaptive filter and integrated by the first order integrator. The accumulated signal is then used to perform gain control by either multiplying this loop output to the digital gain stage or the controlling by the bias of the driver amplifier. By accumulating positive error signal the loop response increase and hence increasing the gain in the loop.

Case 2: Mobile Power change in the reverse direction- When the mobile is requested to decrease its transmitted power, the reference power programmed will be lesser than the actual feedback power. During the closed-loop adaptation, this will result in a negative error signal. The negative error signal is then accumulated by the adaptive filter and integrated by the first order integrator. The accumulated signal is then used to perform gain control by either multiplying this loop output to the digital gain stage or the controlling by the bias of the driver amplifier. By accumulating negative error signal the loop response decreases and hence decreasing the gain in the loop.

As a second example, Figure 4-28 describes three consecutive gain adjustments made by the mobile device to change the transmission signal power level. Figure 4-28 shows the analog bias signal increases the first two times to provide gain to the transmit path. At the third power change request, the bias signal decreases as the base-station
has signaled the mobile device to decrease the transmit power. Figure 4-29 captured RF power at the output of antenna using CMU equipment. The carrier frequency is 1800MHz GSM band. As shown in Figure 4-29, the transmit power of the mobile device is increased from a lower power level to 0dBm. The implemented DSP-GC algorithm not only helps the mobile device to change the transmit power from a lower level to 0dBm, but also helps in maintaining the desired power of 0dBm until the end of signal transmission.

4.6 Summary

- The DSP-GC technique employs an adaptive filter to reduce the variance of the error signal at the input to the controller.

- System stability and gain margin analysis is performed as a function of loop delays. Based on the stability constraint approach, the maximum delay the loop can handle is estimated to be 2.4usec.

- Based on the knowledge of steady state delay, the gain of the unknown plant transfer function, the feedback loop delay a novel loop tuning technique is used to estimate the controller gains for an $N^{th}$ order unknown plant.

- System simulations and lab measurements show that the DSP-GC algorithm performs gain changes upto 90 dB dynamic range with a resolution of 0.1dB power accuracy.

- Since the variance of the error signal is minimized, lab measurements prove that the settling time improved by 15usec compared to DSP-DGT algorithm at the slight expense of gain margin reduction.

- The DSP-GC digital technique uses only 17K digital gates and the current drain is 22mA.
Figure 4-1. Power control A) Measured transmit power to show the PAR and PTN of a LTE signal captured by Rhode and Schwartz CMU 2000 B) System architecture of the DSP-GC algorithm implemented in a mobile device
Symbols from Modem 10101010101

Figure. 4-1. Continued
\[ D_k + A_k <10,0,u> \]

\[ E_k <10,0,u> \]

\[ lms\_clr \]

Upsample by 4

Sample and hold by 4

\[ E_k <19,1,u> \]

\[ lms\_sel \]

\[ kEWW \]

\[ Sk \]

\[ acc(k) <10,0,u> \]

\[ 2u_{E_k} \]

\[ Z^{-1} \]

\[ MUX \]

\[ W_k \]

\[ 2u_{E_k} \]

\[ E_k <20,0,u> \]

\[ W_1 W_2 W_3 W_4 W_5 W_6 W_7 \]

\[ E_2k \]

\[ \mu \]

\[ E_2k \]

\[ <19,1,u> <20,1,u> \]

\[ <10,0,u> <20,0,u> \]

\[ T \]

\[ += \]

\[ = \]

\[ E_k W_1 = S_k \]

\[ W_{k+1} = W_k + 2\mu E_k^2 \]

Figure 4-2. DSP hardware implementation of the adaptive filter and 1st order integrator
Figure 4-3. System constraints in selecting the controller gains.

Figure 4-4. Simplified closed-loop model

Figure 4-5. Open loop based tuning technique
Closed loop response to a step input

Figure 4-6. Closed-loop based tuning technique

Figure 4-7. Closed-loop system with an integral controller

Figure 4-8. Discrete model of closed-loop system at steady state
Set values for D, L and Gss
Set initial value of KI
Form Equation
\[ z^{D+L+1} - z^{D+L} + \beta G_s K_I = 0 \]
Find the (D+L+1) roots, P_k
\[ P_{\text{max, abs}} = \text{magnitude}(\text{max } p_i) \]
Decrease KI
Y
N
Output KI
\[ K_{I, \text{max}} \]

Figure 4-9. Flow chart to estimate integral gain

Figure 4-10. Step response of the unknown open loop system
Figure 4-11. Plot of poles of the transfer function with $K_I = K_{I_{\text{max}}}$

Figure 4-12. Closed-loop system simulations with appropriate integral gains
Figure 4-13. Simplified model for loop delay and gain margin analysis

Figure 4-14. Pole-zero location with loop delay, D = 1, 3, 7 and 9 samples at sample rate Fs.
Figure 4-15. Pole-zero location with loop delay, $D = 13, 17, 19$ and $21$ samples at sample rate $F_s$.

Figure 4-16. Pole-zero location with loop delay, $D = 24, 26, 28$ and $31$ samples at sample rate $F_s$. 
Figure 4-17. Pole-zero location with loop delay, D = 39, 45, 52 and 58 samples at sample rate Fs.

Figure 4-18. Closed-loop step response with respect to varying plant delays.
Figure 4-19. Pole-zero location with loop delay, D = 13 samples and integral gains of -36 dB, -32 dB, -30 dB and -26 dB.

Figure 4-20. Pole-zero location with loop delay, D = 13 samples and integral gains of -22 dB, -20 dB, -6 dB and 9 dB.
Figure 4-21. Power detector and feedback path input-output characteristics.
Figure 4-22. Loop gain margin with varying loop delay as a function of antenna power
Figure 4-23. Simulation to show the closed-loop dynamics for a positive power change
Figure 4-24. Simulation to show the closed-loop dynamics for a negative power change
Figure 4-25. Simulation to show the adaptation of the LMS algorithm with weights and error signal
Figure 4-26. Simulation to show the rate of change of error signal and the feedback as a function of convergence factor

Figure 4-27. Analog response of the closed-loop system with the adaptive filter captured by Tektronix oscilloscope
Figure 4-28. Analog closed-loop response for multiple steps with the adaptive filter captured by Tektronix oscilloscope

Figure 4-29. Transmit power of the mobile device captured by CMU 2000.
Table 4.1. Weight update for the LMS filter

<table>
<thead>
<tr>
<th>Iteration</th>
</tr>
</thead>
<tbody>
<tr>
<td>$w_{1k}$ ($N = 1$)</td>
</tr>
</tbody>
</table>

$k = 0$

\[ w_{10} = 0 \quad \text{and} \quad w_{20} = 0 \]

$k = 1$

\[ w_{11} = w_{10} + \mu E_0^2 \quad \text{and} \quad w_{21} = w_{20} + \mu E_0^2 \]

$k = 2$

\[ w_{12} = w_{11} + \mu E_1^2 \quad \text{and} \quad w_{22} = w_{21} + \mu E_1^2 \]

$k = 3$

\[ w_{13} = w_{12} + \mu E_2^2 \quad \text{and} \quad w_{23} = w_{22} + \mu E_2^2 \]

$k = 4$

\[ w_{14} = w_{13} + \mu E_3^2 \quad \text{and} \quad w_{24} = w_{23} + \mu E_3^2 \]

\[ \quad \ldots \]

$k = n$

\[ w_{1n} = w_{1(n-1)} + \mu E_{(n-1)}^2 \quad w_{2n} = w_{2(n-1)} + \mu E_{(n-1)}^2 \]

Table 4.2. Estimated Poles based on $K_{\ell_{\text{max}}}$

<table>
<thead>
<tr>
<th>k</th>
<th>Poles $p_k$</th>
<th>$P_{\text{max, abs}} = \text{magnitude}(\max p_k)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.9851 + 0.0438i</td>
<td>0.9861</td>
</tr>
<tr>
<td>2</td>
<td>0.9851 - 0.0438i</td>
<td>0.9861</td>
</tr>
<tr>
<td>3</td>
<td>0.8939 + 0.2434i</td>
<td>0.9264</td>
</tr>
<tr>
<td>4</td>
<td>0.8939 - 0.2434i</td>
<td>0.9264</td>
</tr>
<tr>
<td>5</td>
<td>0.8011 + 0.4266i</td>
<td>0.9076</td>
</tr>
<tr>
<td>6</td>
<td>0.8011 - 0.4266i</td>
<td>0.9076</td>
</tr>
<tr>
<td>7</td>
<td>0.6790 + 0.5852i</td>
<td>0.8964</td>
</tr>
<tr>
<td>8</td>
<td>0.6790 - 0.5852i</td>
<td>0.8964</td>
</tr>
<tr>
<td>9</td>
<td>0.5291 + 0.7138i</td>
<td>0.8885</td>
</tr>
<tr>
<td>10</td>
<td>0.5291 - 0.7138i</td>
<td>0.8885</td>
</tr>
<tr>
<td>11</td>
<td>0.3572 + 0.8070i</td>
<td>0.8826</td>
</tr>
<tr>
<td>12</td>
<td>0.3572 - 0.8070i</td>
<td>0.8826</td>
</tr>
<tr>
<td>13</td>
<td>0.1707 + 0.8612i</td>
<td>0.8779</td>
</tr>
<tr>
<td>14</td>
<td>0.1707 - 0.8612i</td>
<td>0.8779</td>
</tr>
<tr>
<td>15</td>
<td>-0.0221 + 0.8740i</td>
<td>0.8742</td>
</tr>
<tr>
<td>16</td>
<td>-0.0221 - 0.8740i</td>
<td>0.8742</td>
</tr>
<tr>
<td>17</td>
<td>-0.2123 + 0.8450i</td>
<td>0.8713</td>
</tr>
<tr>
<td>18</td>
<td>-0.2123 - 0.8450i</td>
<td>0.8713</td>
</tr>
<tr>
<td>19</td>
<td>-0.3912 + 0.7759i</td>
<td>0.869</td>
</tr>
<tr>
<td>20</td>
<td>-0.3912 - 0.7759i</td>
<td>0.869</td>
</tr>
<tr>
<td>21</td>
<td>-0.8641</td>
<td>0.8641</td>
</tr>
<tr>
<td>22</td>
<td>-0.8433 + 0.1892i</td>
<td>0.8643</td>
</tr>
<tr>
<td>23</td>
<td>-0.8433 - 0.1892i</td>
<td>0.8643</td>
</tr>
<tr>
<td>24</td>
<td>-0.7819 + 0.3695i</td>
<td>0.8649</td>
</tr>
<tr>
<td>25</td>
<td>-0.7819 - 0.3695i</td>
<td>0.8649</td>
</tr>
<tr>
<td>26</td>
<td>-0.6828 + 0.5324i</td>
<td>0.8658</td>
</tr>
<tr>
<td>27</td>
<td>-0.6828 - 0.5324i</td>
<td>0.8658</td>
</tr>
<tr>
<td>28</td>
<td>-0.5505 + 0.6700i</td>
<td>0.8672</td>
</tr>
<tr>
<td>29</td>
<td>-0.5505 - 0.6700i</td>
<td>0.8672</td>
</tr>
<tr>
<td>Delay component</td>
<td>Description</td>
<td>Delay</td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>-------------------------------------------------------</td>
<td>------------</td>
</tr>
<tr>
<td>Anti-aliasing filter after (AAF) ADC</td>
<td>1 Pole RC F3dB = 1.3 MHz</td>
<td>$\frac{1}{2\pi f_{3dB}} \approx 122\text{ns}$</td>
</tr>
<tr>
<td>ADC + Digital filter stages after ADC</td>
<td>Through simulations and implementation structures</td>
<td>300nsec</td>
</tr>
<tr>
<td>DAC reconstruction filter response</td>
<td>F3dB = 1.3 MHz Second order butter worth filter</td>
<td>$\frac{1.414}{2\pi f_{3dB}} \approx 230\text{ns}$</td>
</tr>
<tr>
<td>time that controls the VGA output</td>
<td>change</td>
<td></td>
</tr>
<tr>
<td>AAF Bandwidth variation due to</td>
<td></td>
<td>100nsec</td>
</tr>
<tr>
<td>Process/temperature</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PA and power detector</td>
<td>Enabled long before and hence not significant delay</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>contributor</td>
<td></td>
</tr>
<tr>
<td>Total possible delay</td>
<td></td>
<td>752nsec</td>
</tr>
</tbody>
</table>
CHAPTER 5
CONCLUSIONS, APPLICATIONS & SCOPE FOR FUTURE DIRECTIONS

5.1 Thesis Summary

The research work describes techniques to control and compensate for absolute and relative gain variations caused in mobile devices due to imperfections in RF and analog circuits. It also clarifies the difference between the power control techniques employed at the base-station and in mobile devices. Real time analyses with ongoing cellular projects are used to describe the various steps involved in any mobile-based gain control. Past, present and recent methods of power controls are described in Chapter 1. A clear distinction of the functions of RFIC, base band processor and the base-station has been made and described in detail.

Chapter 2 describes a novel DSP technique to track for absolute gain variations in any mobile device caused by the performance degradation of analog and RF circuits as a function of operating voltages, temperature and frequency bands. This DSP-DGT technique employs a digital PID controller and a signal correlation circuit to track for gain variations in the transmit signal path of a mobile device. The digital technique has been found to use only 22K gates and the current drain is 20mA. Since this technique is a complete digital implementation, it reduces bulky analog circuitry and complex power amplifier bias circuitry requirements. System simulations and lab measurements prove that the DSP-DGT algorithm compensates for absolute gain variations better than 0.1dB accuracy independent of modulation schemes adopted.

Chapter 3 outlines a method to compensate for the relative gain and phase errors to maintain power control accuracy requirements. The DSP-GPE technique uses DSP circuits to estimate the relative gain error of the analog RF gain amplifier and provides
DNL gain error compensation. In addition, this technique is used to calibrate the carrier phase changes that happen in any mobile device due to change in the capacitive load impedances on the RF analog path. System lab measurements and simulations prove that the implemented DSP-GPE algorithm estimates and compensates for gain errors better than 0.1dB accuracy and phase errors better than 1 degree accuracy. The digital technique uses less than 10K gates and the current drain is 12mA.

Chapter 4 presents the DSP-GC technique and corresponding hardware structures to dynamically control the absolute signal power of a mobile device by using an adaptive filter along with an integral controller. The DSP-GC technique makes the closed-loop system robust to higher signal variances. In addition to reducing the gate area, the DSP-GC algorithm also employs a novel control loop tuning technique based on stability constraints. This technique is used as a systematic method to estimate the controller gains of a closed-loop system with an unknown $N^{th}$ order plant transfer function. System stability of the implemented architecture as a function of variations in loop delays is analyzed. System simulations and lab measurements show that the DSP-GC technique can perform gain changes up to 90 dB dynamic range with a resolution of 0.1dB accuracy. The convergence time of the loop is reduced to 35usec from 50usec. The DSP-GC digital technique uses only 17K gates and the current drain is 22mA.

Table 5-1, Table 5-2 and Table 5-3 differentiates between the industrial and academic focus involved in the DSP-DGT, DSP-GPE and the DSP-GC techniques respectively.
5.2 Other Areas of Applications

The algorithms and system implementation presented and implemented can be employed in base-station transmitters along with the existing power control techniques. The DSP hardware implementations on base-station receivers and transmitters can be further analyzed. Suitable techniques can be used to track the random carrier phase shifts offsets introduced by the voltage control oscillators in mobile devices. The DSP-DGT and GPE gain tracking techniques can be employed to any power regulation circuit where precise signal tracking accuracy is desired. The correlation DSP-DGT algorithm can be used in RF applications such as power amplifier droop compensation, signal power correction during gain compression and saturation of RF amplifiers. The DSP-GC technique can also be applied to adaptively control the tune line voltage of any voltage control oscillators used in mobile devices.
LIST OF REFERENCES


[70] Linear-In-dB RF Power detector in WCDMA User Equipment, National Semiconductor, AN1375, April 2005.


BIOGRAPHICAL SKETCH

Pravinkumar Premakanthan was born on Feb 3, 1979 in Chennai, India. He graduated from State Bank Officers Association (S.B.O.A) high school in Anna Nagar, Chennai, India in 1996. He obtained his bachelor's in Electrical and Electronics Engineering (EE) from College of Engineering, Guindy (C.E.G) Anna University, Chennai in the year 2000. He pursued his master’s degree in EE under the research guidance of Dr. Wasfy Mikhael at the University of Central Florida, Orlando and graduated in the year 2002. Upon completing his master’s degree, he worked as wireless system engineer with Motorola Semiconductors from 2002-2005. During these three years, he had the opportunity to design and develop wireless ICs for cellular phones. In 2004, while working at Motorola Semiconductors, he started to pursue his PhD with the Computational Neuro Engineering laboratory (CNEL), University of Florida, (UF) under the guidance of Dr. John Harris. He joined as a full-time student at the Department of EE, UF in Aug 2005. After spending a year and half at CNEL, he rejoined wireless team with Freescale Semiconductors and pursued active research and development work while still continuing his doctorate studies. He is presently working as a wireless system lead engineer with Fujitsu Microelectronics in Tempe, Arizona. He holds five U.S. patents in the area of wireless transceivers. Upon completion of his doctorate degree he will continue his present role as wireless system lead at Fujitsu Micrelectronics. He lives with his wife, Manjula in Chandler, Arizona. Pravin’s greatest mentor and role model in life is his PhD advisor, Dr. John Harris.