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DEVELOPMENT OF ALTERNATIVE DIFFUSION BARRIERS FOR ADVANCED COPPER INTERCONNECTS

By
Lii-Cherng Leu

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Chair: David Norton
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The advance in silicon semiconductor processing has driven the minimum feature size towards 32 nm node. Copper has replaced Al as the dominant interconnect metal owing to its lower resistivity and better electromigration resistance. The diffusion of Cu into dielectrics or Si results in deteriorating device performance. To avoid copper diffusion, an effective barrier layer needs to be integrated to protect the device. Ta/TaN bilayer liner is currently used for Cu damascene process. As conventional electrodeposition of Cu requires a sputter deposited Cu seed layer, the continual shrinking in the minimum metal pitch width and increasing high aspect ratio will bring difficulty in conformal step coverage. This work firstly focused on investigating new possible liner replacement for Ta in order to achieve direct copper electrodeposition, and then studied on other possible nitride barrier candidates for Cu metallization.

As a liner material for direct copper electroplating with excellent conformity and high quality copper texture, the diffusion barrier properties of 5 nm iridium thin films for Cu metallization on Si were examined. To avoid iridium silicidation with the underlying Si and to enhance barrier properties against copper diffusion, the Ir/TaN bilayer approach was also studied. As the failure temperature for 5 nm iridium barrier was 400 °C, the addition of TaN layer
strongly improved the barrier performance. The utilization of Pd as a catalyst for Cu electroless deposition along with TaN to form a bilayer barrier was also investigated. The Pd/TaN bilayer structure was shown to prevent copper diffusion up to 550 °C for 1 h.

Ternary refractory metal nitride W-B-N thin films were also studied as a candidate diffusion barrier for Cu metallization on Si. W-B-N thin films were amorphous with low resistivity ranging from 159.92 to 240.4 μΩcm. The W-B-N thin films deposited at 5 % N2 flow ratio can block Cu diffusion after 500 °C annealing for 1 h. As one of the interesting refractory metal nitrides for Cu diffusion barrier application, the comparative study between ZrN and Zr-Ge-N thin films as diffusion barriers was also examined.
CHAPTER 1
INTRODUCTION

The integrated circuit (IC) fabrication technology has progressed according to the statement made by Gordon Moore, known as Moore’s law. As the number of transistors approximately doubles every 24 months, this empirical observation has driven the minimum IC feature size down to the 32 nm node or beyond. Figure 1-1 shows how the transistors in Intel microprocessors have increased according to Moore’s law in the past three decades.

The manufacturing of ICs can be divided in two phases: front-end-of-line (FEOL) processing and back-end-of-line (BEOL) processing. FEOL is the initial processing to build devices such as transistors and resistors on semiconductor wafers. BEOL processing includes all the steps involved in connecting the active components of the circuitry via metal wiring. Various devices built up during FEOL processing are connected to each other via a three dimensional network of metal wires. The formation of these connecting wires in integrated circuits is known as metallization. The metal lines are separated from one another by dielectric materials with low dielectric constant such as silicon dioxide or fluorine doped silicon dioxide glass (FSG). Interconnects can be either local interconnects or global interconnects depending on their functions. Local interconnects primarily refer to interconnects that connect the gate, source, and drain in a transistor. Typical local interconnects are heavily doped polysilicon or refractory metal silicide. Local interconnects can have higher resistivity because the current in them travels for very short distances. However, local interconnects need to be able to withstand higher processing temperature. Global interconnects, on the other hand, travel long distances and need to have lower resistivity. Typical global interconnect metals are aluminum and copper.

In earlier years of device fabrication, the speed of an IC was primarily determined by the speed of the transistors as a result of the improvement in front end process. Much of the speed
increase achieved in transistors was by scaling the transistor dimensions such as gate oxide film thickness, active channel length and width. Scaling of the device resulted in a higher transistors density per chip for a given chip area, lowering the cost per transistor and increasing speed. The disadvantage of scaling is the higher current density in the transistors. For earlier generation devices with large feature size, the gate delay dominated the overall device performance. With the continual shrinking of device dimensions, interconnect delay becomes more and more important. In fact, interconnect delay has become the dominant factor in determining the device speed for sub-100 nm devices.

As device and circuit dimensions shrink towards 100 nm, the interconnect delay, also called the RC delay, where R is the resistance of the interconnects and C is the associated total capacitance, is becoming one of the most important factors in determining the device and circuit performance [1]. Figure 1-2 shows the effect of RC time delay as the result of decreasing the feature size. For a MOS circuit, the RC delay can be defined in terms of the circuit response [2]:

\[ V_{out}(t) = V_{out (max)} \left[ 1 - \exp \left( \frac{-t}{RC} \right) \right] \]

where \( V_{out}(t) \) is the output voltage of the circuit at time \( t \), \( V_{out (max)} \) is the maximum output voltage, \( R \) is the resistance of interconnects and \( C \) is the total capacitance of the circuit. The resistance of the interconnects is defined in terms of its dimensions and resistivity as following equation:

\[ R = \rho \frac{L}{Wt} \]

where \( \rho \) is the resistivity, \( L \) is the interconnect length, \( W \) is the interconnect width, and \( t \) is the interconnect thickness. The capacitance between two metal lines separated by distance \( d \) is defined as:
\[ C = \varepsilon \frac{tL}{d} \]

where \( \varepsilon \) is the permittivity of the dielectric. Combing R and C yields the RC delay:

\[ RC = \frac{\rho \varepsilon L^2}{Wd} \]

To reduce RC delay, copper has replaced aluminum as the dominant metal wiring due to its low bulk resistivity 1.67 \( \mu \Omega \text{cm} \), (about 40 \% lower than aluminum, 2.65 \( \mu \Omega \text{cm} \)) and better electromigration resistance [3]. As a result of high current density in the integrated circuits, electromigration becomes a serious reliability issue, particularly for Al interconnects. Electromigration is a phenomenon by which high current density in interconnects leads to the movement of the metals atoms in the direction of the electron flow. When high energy electrons transfer their momentum to these mobile metal atoms, there is a movement of metal atoms in the direction of the electron flow, resulting in the formation of void on one side and hillocks on the other side. Therefore, it could either open the circuits or short the circuits. Having a stronger metallic bonding, Cu have higher melting point than Al, yielding a higher energy barrier for lattice and grain boundary diffusion than Al, thus better electromigration resistance. As a result, the interconnects reliability in regard to electromigration was greatly improved by integrating Cu into Si backend process.

However, Cu integration is not without significant challenges. On the one hand, as the metal pitch continues to scale down, the effect of surface scattering and grain boundary scattering would cause the resistivity of Cu to increase. On the other hand, copper diffuses easily into Si, SiO\(_2\) and other dielectrics, resulting in deteriorating device performance. Under high electrical field, Cu also drifts through oxide and accumulates in the dielectrics as Cu\(^+\) space charge, resulting in dielectric breakdown and large leakage current. Copper is known to form deep level
traps in silicon (acceptor levels at 0.24, 0.37 and 0.52 eV above the valence band) [4]. Therefore it has required the insertion of a barrier layer between Cu and underlying dielectrics to prevent the diffusion of copper into the dielectric material and active region. Another principle function of the barrier layer is to provide good adhesion, in particular to the dielectric materials since Cu has poor adhesion to most dielectric materials.

For polycrystalline thin films, rapid diffusion almost occurs via grain boundaries, dislocations and surface defects. According to Fick’s law, diffusion is a temperature dependent process. The temperature dependence of diffusion coefficient ($D$) is given by the following equation:

$$D = D_0 \exp\left(-\frac{Q_d}{RT}\right)$$

Where $D_0$ is temperature-independent pre-exponential factor, $Q_d$ is the activation energy, $k$ is the Boltzmann constant and $T$ is the temperature. The activation energy for grain boundary diffusion is approximately half the activation energy required for lattice diffusion. As a result, grain boundary diffusion dominates at lower temperatures [2]. For polycrystalline thin films, diffusion through grain boundaries and dislocations is the fastest. This mode of diffusion can be stopped by two approaches. The grain boundaries and/or dislocations can be “stuffed” by impurity atoms which would hinder diffusion through them. Another approach is to eliminate the grain boundaries. The ideal microstructure for a diffusion barrier should be single crystal since it does not have any microstructure defects or grain boundaries. However, due to lattice mismatch and thermal budget limitations, the growth of single crystal barriers is not applicable [5]. Another consideration would be amorphous barriers. The amorphous phase has no long range order, therefore eliminating the formation of grain boundary for Cu diffusion.
The chemical or metallurgical reactivity with copper and underlying dielectric material, its density, and its microstructure are the three major materials properties that determine the degree of barrier failure. First of all, a viable material should not react with copper or the underlying dielectrics. It should be able to resist thermal, mechanical, and electrical stress encountered in subsequent processing steps or normal operating conditions. Also, its density should be as close to ideal as possible so as to eliminate diffusion across voids, defects, or loosely packed grain boundaries upon high temperature processing. In this respect, an appropriate liner material for Cu interconnects must meet some stringent criteria, which [6] include:

(i) high thermal and structural stabilities in contact with Cu and underlying dielectrics
(ii) excellent adhesion between adjacent layers
(iii) good thermal and electrical conductivities
(iv) suitable texture to facilitate the nucleation and growth of subsequent Cu films
(v) strong mechanical strength under thermal and mechanical stresses
(vi) good conformality and uniformity of step coverage over small device features.
(vii) excellent compatibility with subsequent processing flow and facilities

Materials with high melting point often yield high activation energy for diffusion. As a result, refractory metals and their nitrides are widely studied as barrier materials for back end interconnects process. For example, the Ti/TiN bilayer barrier structure is employed in W and Al based interconnects. Current Cu metallization uses Ta/TaN bilayer structure as its diffusion barrier. With continual shrinking of the minimum feature size in the integrated circuits, the Ta/TaN liner for copper metallization would eventually reach its scaling limits. In addition, conventional copper electrodeposition for integrated metal wiring required a sputtered deposited Cu seed due to the poor nucleation of Cu on Ta. [7] With decreasing metal pitch width and increasing high aspect ratio, the growth of uniform and conformal Cu seed with good step coverage becomes more and more challenging. In this regard, the proposal of replacing Ta with noble metal to achieve direct copper electrodeposition is emerging [8]. Several noble metals
have been demonstrated with the feasibility for direct copper electrodeposition with excellent conformality [8-11]. However, most of their properties relative to serving as a copper diffusion barrier have not yet been investigated or addressed. Therefore, the motivation for the first part this dissertation research is to investigate the diffusion barrier properties of ultra thin iridium films, as described in chapter 4. To enhance the overall barrier properties against copper diffusion, a bilayer approach combining with TaN thin films was studied in chapter 5. To achieve copper superfilling in damascene process, one can also employ Cu electroless deposition using Pd as a catalyst. Chapter 6 discusses the thermal stability of Pd/TaN bilayer structure as a template for electroless Cu plating. Chapter 7 describes the barrier properties of amorphous and low resistive W-B-N thin films with 10 nm thickness deposited by reactive magnetron sputtering using a W₂B target. A comparative study of barrier properties and performance of ZrN and Zr-Ge-N thin films is discussed in chapter 8. Finally, chapter 9 will give the conclusion of this dissertation.
Figure 1-1. Scaling of transistors for Intel microprocessors.

Figure 1-2. RC and overall delay vs. technology node.
CHAPTER 2
LITERATURE REVIEW

This chapter will present the background and literature review of various diffusion barriers, their properties and the methods of synthesis.

As mentioned previously, diffusion often occurs through either lattice or grain boundary. Both lattice and grain boundary diffusion depend on temperature. A cross over occurs where the mechanism of diffusion changes from one to the other. The temperature at which this crossover occurs is known as the Tammann temperature. It is widely believed that the Tammann temperature is between one-half or two-thirds of the melting temperature $T_m$ of the solid [6]. As such, high melting temperature materials often yield high activation energy for diffusion. The dependence of diffusion processes on the melting temperature of the host lattice makes it desirable to select liner materials with a high melting point. Accordingly, refractory metallic systems with characteristically high melting points and chemical inertness are considered as viable candidates for diffusion barriers. Various refractory metals and their binary and ternary compounds have been suggested for such applications [12]. Some have been successfully applied in the industry, for example, Ti/TiN for Al metallization, and Ta/TaN for Cu metallization.

Basically, we can roughly classify these materials into several groups [3]:

- Refractory metals such as Cr, Ti, Ta, W, Mo, Zr, Pd, and Nb.
- Refractory metallic alloys, including $\text{Ti}_x\text{W}_{1-x}$, $\text{Fe}_x\text{W}_{1-x}$, $\text{Ni}_x\text{Nb}_{1-x}$, $\text{Ni}_x\text{Mo}_{1-x}$.
- Refractory metal silicides, such as $\text{TiSi}_2$, $\text{CoSi}_2$, $\text{Mo}_x\text{Si}_{1-x}$, $\text{W}_x\text{Si}_{1-x}$, $\text{TaSi}_2$.
- Refractory metal-nitride, carbide and boride such as $\text{TiN}_x$, $\text{HfN}$, $\text{ZrN}$, $\text{W}_x\text{N}$, $\text{TiC}$, $\text{TaC}$, $\text{TaN}_x$, $\text{TiB}_2$.
- Refractory metal based ternary nitride barriers, such as $\text{Ti-Si-N}$, $\text{W-Si-N}$, $\text{Ta-Si-N}$, $\text{Zr-Si-N}$, $\text{W-Ge-N}$, and $\text{W-B-N}$.
Of all these, Ti-, Ta-, W-, and Zr-based diffusion barrier are the most interesting owing to their desirable physical, chemical and electrical properties.

2.1 Titanium and Titanium Nitride Diffusion Barrier

Ti/TiN has been widely used in aluminum- and tungsten- based interconnects systems. However, they are not suitable for copper barrier performance for thickness at or below 20 nm [13].

2.1.1 Titanium Diffusion Barrier

A Ti barrier fails primarily through a metallurgical reaction with copper, which occurs readily at 350 °C [12]. Ohta et al. reported failure of Ti diffusion barrier at 400 °C, as indicated by an increase in resistivity after annealing. The resistivity increase was attributed to Cu diffusion through Ti and subsequent reaction with Si to form Cu silicides [14].

2.1.2 Titanium Nitride Diffusion Barrier

As a liner material for Al interconnects, the properties of TiN films greatly depend on the deposition conditions which affect the microstructure, density and other relevant barrier properties. The reported resistivity values range from 20 – 2000 \(\mu\Omega cm\) and density ranges from 3.2 – 5.0 (g/cm\(^3\)) [15]. Although a considerable effort had been made to utilize the existing knowledge and processing methods of TiN for Cu based metallization, TiN deposited by both physical vapor deposition (PVD) and chemical vapor deposition (CVD) methods often result in a columnar grain structure in which grain boundaries exist through the entire thickness of the barrier film [16-19]. Under elevated temperatures Cu easily diffuses through these columnar grain boundaries and reacts with Si to form silicides. An observation was reported for better TiN barrier performance in Al interconnects after exposing TiN to air before Al deposition [20]. This improved TiN barrier properties was attributed to the diffusion of oxygen into columnar grain boundary region upon exposure to air. The oxygen occupied the grain boundary and stuffed the
diffusion paths. The subsequent reaction of oxygen with aluminum and the formation of an amorphous aluminum oxide phase blocked any further material that transported through TiN liner. In comparison, the mechanisms involved in the copper reduction of native oxide on air-exposed TiN were shown to be appreciably different from those for aluminum. As a result, the benefit of enhanced diffusion barrier performance through oxygen stuffing cannot be realized for copper metallization [21]. Amorphous TiN films could be realized using metal organic chemical vapor deposition (MOCVD), thus providing improved barrier performance due to the absence of grain boundary as pathways for fast Cu diffusion [22-24]. However, the incorporation of contamination from the precursor such as carbon, oxygen and hydrogen often made the films porous and high resistive [25]. Several attempts to remedy this problem included the use of plasma-assisted MOCVD growth [26, 27] and post-deposition annealing treatments, in the presence or absence of a plasma environment [28, 29]. Unfortunately, these attempts did not yield the optimized TiN barrier performance needed for Cu metallization. Atomic layer deposition (ALD) techniques were also implemented for TiN barrier deposition with focus on the influence of microstructure, resistivity and impurity content on film barrier properties [30]. However, the barrier film failed after annealing at 500 °C for 1 h.

2.2 Tantalum and Tantalum Nitride Diffusion Barrier

Tantalum and Ta-based compounds have been widely used as high-performance liners for current Cu interconnections.

2.2.1 Tantalum Diffusion Barrier

The two major advantages of using Ta as a diffusion barrier in comparison to Ti are its high melting temperature (3017 °C compared to 1668 °C for Ti) and thermal (interface and solubility) stability with Cu at very high temperatures. Both Cu and Ta are insoluble in each other even at high temperatures [31-33]. The Ta-Cu phase diagram shown in Figure 2-1 indicated that Cu and
Ta are almost completely immiscible up to their melting points and do not react to produce any compounds [34]. Moreover, the Ta/Si interface was shown to maintain its integrity up to 650 °C, with tantalum silicides generally being more stable than their Cu silicide counterparts [32, 35]. The metastable tetragonal β-Ta barrier [36] with resistivity 150-220 Ω cm [37], which is normally formed when Ta is deposited directly on the dielectrics was first shown to be an excellent barrier in 1986 by Hu et al [38]. As mentioned earlier, for reduced copper interconnect dimensions, thinner liners with low in-plane resistivity are required [4]. When Ta is deposited on TaN, the low-resistivity α-Ta phase (bcc) [39] with a resistivity of 15-30 Ω cm [37, 40] is spontaneously formed. This phenomenon occurs on TaN film at least as thin as 2 nm [40]. However, grain boundary diffusion of Cu atoms becomes relevant at elevated temperature due to polycrystalline structure of Ta [41]. One way to improve the thermal stability of Ta barrier is the addition of oxygen or nitrogen during the deposition process [42]. Oxygen impurities in Ta films are believed to decorate grain boundaries and consequently block the diffusion paths along grain boundaries.

### 2.2.2 Tantalum Nitride Diffusion Barrier

TaN is also used for Cu diffusion barrier applications due to its high melting temperature and thermal stability. Among the various phases of Ta-N, stoichiometric TaN has a melting temperature of 3087 °C and heat of formation (ΔHf = -120 kJ/mol) [43], making it more stable than Ta2N which has a melting temperature of 2050 °C and heat of formation of ΔHf = -98 kJ/mol. The TaNx/Si interface is more stable than its Ta/Si counterpart, in view of the higher activation energy needed for silicide formation in the case of the nitride. This property could be attributed to the increased thermal budget required to ensure the dissociation of Ta-N bonds prior to the formation of Ta-Si bonds [44]. From a structural perspective, all TaNₓ phases can be
simply described as close-packed arrangements of Ta atoms, with the smaller N atoms inserted into interstitial sites. The resulting structure has significantly higher resistance to copper diffusion than does the pure metal. Most experimental trends suggest that the diffusion barrier effectiveness of tantalum-based liners increases with higher nitrogen content, at least up to a N to Ta stoichiometry of 1:1.

To improve conformal step coverage for high aspect ratio trench, significant effort has been invested to develop chemical vapor deposited TaNx barrier [45-49]. The three major inorganic precursors that have been employed to deposit TaNx thin films are TaCl5, TaF5 and TaBr5. Chemical vapor deposition of TaNx from TaCl5 and NH3 at the low deposition temperature of 350 °C is not suitable for diffusion barrier application because the films had very high resistivity (> 10,000 $\mu\Omega cm$) and high Cl contamination (4.5 at. %). Since the Ta-Cl bond is very strong, higher energy is required to cleave the bond. When TaNx films are deposited using TaF5 and NH3 at 350 °C, films have a relatively low resistivity of 1650 $\mu\Omega cm$. However, considerable contamination of F (4.0 at. %) was observed and the step coverage of the film was poor. Chen et al. [46] reported deposition of TaNx films between 350 and 500 °C using TaBr5, H2 and NH3. The films were N-rich with N:Ta ratio varying between 1.75:1 and 1.87:1 for deposition between 350 and 500 °C. The N-rich film deposited with TaBr5 indicates that film is possibly Ta3N5 and not TaN. The O and C contamination in the film was below the detection limit of AES. Films contained Br as an impurity and the Br content in the film decreased with increasing deposition temperature. The highest Br content of about 5 at. % was observed for deposition at 350 °C, while the Br content in film was below the detection limit of AES for deposition at 500 °C. The film crystallinity was strongly dependent on deposition temperature. Films deposited at 350 and 425 °C were amorphous whereas films deposited at 500 °C were polycrystalline with tetragonal
Ta$_3$N$_5$ and hexagonal TaN phases. Film resistivity also showed a strong dependence on deposition temperature with the lowest resistivity of $5040 \, \mu\Omega\text{cm}$ observed at 500 °C. The resistivity of the films basically decreased with increasing deposition temperature. Metal organic sources have also been explored as Ta source for CVD of TaN$_x$ [50-55]. Like most CVD grown films, these TaN$_x$ are very resistive, limiting their usefulness in barrier application. As such, due to high resistivity, tantalum nitride films deposited by CVD were not suitable for copper diffusion barrier applications.

A bi-layer structure of Ta/TaN is currently used to overcome the obstacle of adhesion problem. TaN does not adhere well to Cu [56], but it does adhere to SiO$_2$ [57]. However, with device dimensions shrinking, conformality of high aspect ratio has become a challenging issue. PVD [58] has been used until now for deposition of liner and Cu seed layer, with ionized PVD (I-PVD) [59] being the latest in the technology that has been able to extend the functionality to lower dimensions. As the overall liner-Cu seed layer thickness requirement continues to decrease, either some major modifications have to be done to the I-PVD process or a switch to a better conformal process, like atomic layer deposition (ALD) has to be adopted [60-65].

2.3 Tungsten Nitride Diffusion Barrier

Tungsten and its nitrides are also chemically and thermodynamically stable with respect to copper. In particular, tungsten nitride (WN$_x$) presents a potentially viable diffusion barrier solution, given its attractive properties as a highly refractory material with excellent mechanical and physical properties. Additionally, it can be easily deposited in amorphous form, which is highly desirable given that an amorphous structure is inherently free of grain boundaries [66]. As in the case of TaN$_x$, stoichiometry of WN$_x$ plays a pivot role in determining the diffusion barrier performance. In particular, highly metal-rich amorphous WN$_x$ films (0.5) tend to recrystallize into W and W$_2$N phases at temperatures as low as 450 °C, thus leading to premature barrier
failure because of grain boundary diffusion [67]. High nitrogen content on the other hand, yields high recrystallization temperature but also significantly higher resistivity (>1000 $\mu\Omega cm$). Various researchers reported on the development of PVD-based techniques for the deposition of WN$_x$. Uekubo et al. reported that an 8-nm thick PVD grown W$_2$N barrier with a “disordered polycrystalline” microstructure could prevent copper diffusion even after annealing at 600 °C for 30 minutes [68].

In addition to PVD deposition, WN$_x$ barrier films were also synthesized via CVD using tungsten hexafluoride (WF$_6$) as the source precursor [69, 70]. In particular, thermal CVD WN$_x$, using WF$_6$ and NH$_3$ as co-reactants, yielded films with excellent conformality. However, the process required high deposition temperatures (>500 °C), which limited its integration with metallization structures that use thermally fragile low k materials [71]. To lower the deposition temperature, Plasma-enhanced CVD (PECVD) was employed with the reaction of WF$_6$ and either NH$_3$ or a mixture of H$_2$ and N$_2$ as co-reactant. Plasma application allowed film deposition at 350 °C, but typically with less conformal step coverage compared with thermal CVD [72]. In order to eliminate the typical processing and integration issues related to the use of fluorine-based source precursors, various researchers investigated the development of MOCVD WN$_x$. The three main metal organic precursors that have been used to deposit WN$_x$ thin films are bis(tert- butylimido)bis(tert-butylamido) tungsten (TBTBW), tungsten hexacarbonyl and pentacarbonyl tungsten(1-methylbutylisonitrile). Chiu et al. examined the applicability of bis(tertbutylimido) bis(tertbutylamido) tungsten (BTBTW) for the MOCVD deposition of WN$_x$ without the use of a separate nitrogen source [73]. Similar to MOCVD TiN and TaN, the resulting films exhibited high resistivity, above 6000 $\mu\Omega cm$ for films deposited at 450 °C and included significant contamination from the organic ligand [73]. Kelsey et al. studied an
alternative thermal MOCVD WN_x approach that employed the reaction of the non-fluorinated W source tungsten-hexacarbonyl, W(CO)_6, with NH_3. This process yielded an amorphous W_2N-phase films with low resistivity (<250 μΩcm) at temperatures as low as 210 °C [74]. Films exhibited viable step coverage in aggressive device geometries. Another precursor, pentacarbonyl tungsten (1-methylbutylisonitrile), has also been used with NH_3 to deposit WN_x thin films [75]. The films were stoichiometric W_2N with amorphous microstructure. Detailed film characterization or diffusion barrier testing for this precursor has not been reported.

2.4 Zirconium Nitride Diffusion Barrier

As one of the refractory metal nitrides, zirconium nitride has a high melting point of 2960 °C. In addition, among the transition metal nitrides, ZrN has the lowest electrical resistivity of 13.6 μΩcm in bulk [76]. A heat of formation of ΔH=-87.3 kcal/mol [77] is even negatively larger than that of TiN (-80.4 kcal/mol) and TaN (-60.3 kcal/mol), suggesting the thermodynamical stability of the ZrN compound to be better than other refractory metal nitrides.

The stability of ZrN_x in contact with Si or Cu at high temperatures has been reported by Takeyama and Chen in their work on the diffusion barrier properties of ZrN_x films [78-81]. The absence of any Cu-Zr and Zr-Si compound formations is probably ascribed to the stability of the ZrN compound in that it has the negatively largest heat of formation among those of possible compounds under consideration. (CuZr_2: -5.37, CuZr: -7.91, ZrSi: -12.3, ZrSi_2: -12.7, ZrN: -87.3 kcal/mol) [77, 82, 83]. ZrN_x deposited at high temperature consisting of nano-crystalline grains of several to 10 nm in size and amorphous like regions at some grain boundaries was reported [79]. The crystallite size did not change upon annealing at 600 °C. However, the reason why copper does not penetrate through those grain boundaries at high temperature is uncertain. The authors presumed that the absence of copper penetration at a temperature as high as 750 °C may
depend on the specific bonding, stuffed nitrogen atoms and thermo-energetic (atomic arrangement) conditions at the grain boundary. In recent work by Sato et al. on 5 nm thick, slightly N-rich ZrN\textsubscript{x} barrier deposited by reactive sputtering showed thermal stability between Cu and SiOC upon annealing at 500 °C for 30 min. [81]. Despite the unknown mechanism, these results show that ZrN\textsubscript{x}, with low electrical resistivity and high thermodynamical stability, could be an excellent material for copper diffusion barrier.

2.5 Ternary Nitride Diffusion Barrier

As mentioned previously, the amorphous structure is highly desirable for diffusion barrier application. However, amorphous phase is thermodynamically unstable and tends to crystallize at elevated temperatures. The adding of a third element to the binary metal nitrides matrix could frustrate the binary lattice structure and delay or avoid the recrystallization process upon annealing at high temperatures. Elements such as B, C, Si and Ge have been widely applied in making amorphous ternary refractory metal nitrides with excellent barrier performance.

2.5.1 Carbon Incorporated Ternary Nitride Diffusion Barrier

The addition of C to refractory metal nitrides has two general purposes. One is to increase the amorphous tendency or recrystallization temperature, the other is to decrease film resistivity related to its binary nitride. The C and N basically sit on the interstitial sublattice of the host metal matrix, resulting in a structure that is similar to the nitrides or carbides.

TaC\textsubscript{x}N\textsubscript{y} deposited via reactive sputtering using TaC target exhibited a relative low resistivity (~300 \(\mu\Omega cm\)) [84]. The barrier is able to prevent Cu diffusion upon annealing at 600 °C for 30 min. TaC\textsubscript{x}N\textsubscript{y} has also been synthesized via MOCVD using pentakis(diethylamido)tantalum as a precursor. However, the film was too resistive (> 6000 \(\mu\Omega cm\)) and failed as a barrier at 500 °C after 1 h annealing [85]. Although TaC\textsubscript{x}N\textsubscript{y} synthesized
using pentakis(dimethylamido)tantalum and pentakis(diethylamido)tantalum was able to prevent Cu diffusion at 500 °C [86], nevertheless, the film was still quite resistive and was not applicable for diffusion barrier application.

The bulk resistivity of $\beta$-WC$_x$ is somewhat lower than $\beta$-WN$_x$, given the possibility of making lower resistive WN$_x$C$_y$ than WN$_x$. The properties of W-C-N films deposited by atomic layer deposition (ALD) using WF$_6$, NH$_3$, and triethyl boron were reported [87]. The films deposited at 313 °C showed resistivity of about 350 $\mu\Omega cm$ with a density of 15.4 g/cm$^3$. The film composition measured by Rutherford backscattering spectrometry showed W, C, and N of approximately 48, 32, and 20 atom %, respectively. The films were nanocrystalline and the microstructure was kept until annealing at 700 °C, although some amount of simple hexagonal $\alpha$-WC was formed and the $\beta$-W$_2$N phase disappeared. The barrier at 12 nm thickness failed after annealing at 700 °C for 30 min by the evidence of copper silicide formation.

2.5.2 Silicon Incorporated Ternary Nitride Diffusion Barrier

Although the addition of Si to metal nitrides promotes amorphous film growth and improves Cu adhesion, most films are quite resistive depending on the amount of Si incorporated. The failure mechanism of these Si based ternary nitrides was mainly attributed to grain boundary diffusion after barrier recrystallization and Si out-diffusion into, and reaction with, the neighboring Cu layer.

Ti-Si-N has been studied using reactive sputtering on a Ti-Si alloy target in Ar/N$_2$ gas mixture [88, 89]. Reid et al. deposited amorphous Ti$_{0.34}$Si$_{0.23}$N$_{0.43}$ barrier films with a resistivity of 680 $\mu\Omega cm$ [89]. After thermal test, the barrier was shown to be thermally stable upon annealing at 650 °C for 30 min. Similarly, Iijima et al. also reported sputter deposited Ti-Si-N
barrier films with similar stoichiometry, namely Ti$_{0.31}$Si$_{0.19}$N$_{0.50}$. The films had a resistivity of 500 $\mu\Omega cm$ and were able to resist Cu diffusion after a 30 min anneal at 600 °C [88].

Several reports were given on Ta-Si-N deposited by reactive sputtering using Ta-Si alloy targets in Ar/N$_2$ mixture gases [90-92]. The adhesion of these Ta-Si-N barriers to Cu was found better than the Ta/TaN dual barrier structure. The films prepared by Lee et al. had the stoichiometry of Ta$_{0.43}$Si$_{0.04}$N$_{0.53}$ with a high resistivity of 1419 $\mu\Omega cm$ [90]. After thermal anneal test, the barriers failed at 825 °C due to chemical decomposition. Kim et al. did research on varying the N content of Ta-Si-N films in order to determine the impact of N content on the barrier performance [91]. Films with N content greater than 40 at. % can prevent Cu diffusion up to 800 °C, while those with lower N levels failed after 700 °C anneal.

Amorphous W-Si-N has also been synthesized via reactive sputtering using Ta-Si alloy targets in Ar/N$_2$ mixture gases [93]. The WSi$_{0.6}$N films were kept amorphous below 850 °C. Above 850 °C, W microcrystals with an average grain size of 3 nm in amorphous W-Si-N were present. The SIMS results showed that the Cu diffusion was successfully blocked by the amorphous WSi$_{0.6}$N films up to 600 °C for 30 min. W-Si-N could also be deposited by CVD using WCl$_6$, SiH$_4$, NH$_3$ and H$_2$/Ar at 500 °C [94]. The films had a stoichiometry of W$_{0.54}$Si$_{0.12}$N$_{0.34}$, and a high resistivity of $\sim$1000 $\mu\Omega cm$. Cu diffusion was prevented after a 600 °C anneal for 1 min.

### 2.5.3 Germanium Incorporated Ternary Nitride Diffusion Barrier

Rawal et al. compared the diffusion barrier properties between WN$_x$ and W-Ge-N [95]. The W-Ge-N films were synthesized by cosputtering W and Ge targets at room temperature. Nitrogen was incorporated into the films by leaking a mixture of Ar and N$_2$ gases. The addition of Ge into WN$_x$ matrix frustrated the recrystallization behavior of WN$_x$. AES Cu depth profile indicated
that while the WNₓ films failed as a barrier due to recrystallization at 600 °C, the W-Ge-N barrier was able to prevent Cu diffusion at 600 °C. However, the films were too resistive to be applicable for Cu metallization. The comparison between Ta-Ge-N and TaNx films for Cu diffusion barrier was also reported [96]. The films were deposited via reactive magnetron sputtering using Ta and Ge targets at N₂ +Ar gas mixture at room temperature. X-ray diffraction patterns showed that the addition of Ge to the binary TaNx matrix causes the diffusion barrier failure temperature to increase by at least 100 °C as compared to TaNx. The AES depth profile showed significant Cu diffusion through TaNx diffusion barriers and into the Si substrate after annealing at 400 °C, while no Cu diffusion occurs at similar temperature through the Ta–Ge-N diffusion barrier. Significant amounts of oxygen were also incorporated into the films as detected by AES.

**2.5.4 Boron Incorporated Ternary Nitride Diffusion Barrier**

Several reports of W-B-N thin films as Cu diffusion barrier have been given. Rei et al. deposited W-B-N thin films with a variety of stoichiometries via reactive sputtering using a W₂B target in various N₂/(Ar+N₂) flow ratios [97]. The resistivity of the films basically increased with increasing N₂/(Ar+N₂) flow ratio and ranged from 190 to 1360 μΩcm. A 100 nm thick W₀.₆₄B₀.₂₀N₀.₁₆ film deposited at 3 % N₂/(Ar+N₂) flow ratio was found to have the best resistance to Cu diffusion and low resistivity of 220 μΩcm. W-B-N thin films synthesized by PECVD at 350 °C were also studied [98-100]. The reported resistivity ranged from 100 to 844 μΩcm depending on film stoichiometry. The best film performance against Cu diffusion was found to be at 800 °C.
Figure 2-1. Ta-Cu binary phase diagram.
CHAPTER 3
EXPERIMENTAL DETAIL AND CHARACTERIZATION

3.1 Sputter Deposition

Sputter deposition is a physical vapor deposition (PVD) method of depositing thin films by sputtering. When a charged particle bombards the target surface, apart from the ejection of neutral atoms of the surface material, charged atoms and electrons are also emitted from the surface. The ejected neutral target atoms condense into thin films on the substrate. The process can be realized by having positive ions, such as Ar\(^+\) strike the target surface, the target being connected to a negative voltage supply and the substrate holder forming the anode and facing the target (Fig. 3-1). The sputtering yield, the most important parameter for characterizing the sputtering process, is defined as the number of atoms ejected from the target surface per incident ion. The sputtering yield depends on the bombarded material, its structure and composition, the characteristics of the incident ion and the experimental geometry. Sputtering is basically a low temperature process, and less than 1 % of the total applied power is used for the ejection of the sputtered material and secondary elections. A considerable amount of energy is dissipated as heat at the cathode by the ions that strike it, and the cathode gets hot. Although the sputtering yield for most materials increases with temperature, it is not generally advisable to set the cathode temperature rise beyond a tolerable level during sputtering because of the possible problems with outgassing.

The understanding of glow discharge is important in order to master the sputter deposition system, since virtually all of the energetic incident particles originate in the plasma. The basic ionization process in a gas discharge is as follows. When the electrons collide with gas molecules, the latter are ionized to become positive ions. The energy of the electron should be higher than the ionization energy of the gas molecules. At the beginning of the discharge, the
primary electrons from the cathode are accelerated by the electric field near the cathode with energy in excess of the ionization energy of the gas molecules. These energetic electrons collide with the gas molecules and generate positive ions before they travel to the anode. The positive ions bombard the cathode surface which results in the generation of secondary electrons from the cathode surface. The secondary electrons increase the ionization of the gas molecules and give rise to a self-sustained discharge. When the discharge current is below $10^{-9}$ A, the secondary electrons are insufficient in number to cause enough ionization to produce a self-sustained discharge, as shown in Fig. 3-2. In a glow discharge, the potential distribution between electrodes is nonuniform due to the presence of the charge. There is a voltage drop near the cathode, which is known as the cathode fall. The cathode fall region corresponds to a so called cathode dark space or Crookes dark space. This spacing corresponds to the region through which the electron gains at least the ionization energy of gas molecules. The glow discharge is maintained by secondary electrons produced at the cathode by positive ion bombardment. In glow discharge sputtering, the energy of the incident ions is close to the cathode fall potential. Since the anode fall, which is generally within 10 to 20 V, and the potential drop across the positive column are much smaller than the cathode fall, the incident ion energy is roughly equal to the discharge potential. The negative glow results from the excitation of the gas atoms by inelastic collisions between the energetic electrons and gas molecules. The abnormal glow discharge is used for sputtering systems and most processing plasmas. In this case, the energy of incident ions is nearly equal to the discharge voltage. The use of magnetic field or high frequency electrical field somewhat extends the controllable range of discharge parameters. Under magnetic field or high frequency electrical field, the electrons in the discharge region will
have cyclic motions and the number of the collisions will increase between the electrons and the
gas molecules, thus increasing the efficiency of the gas discharge.

3.1.1 DC Sputtering

The dc sputtering system is composed of a pair of planar electrodes. One of the electrodes is
a cold cathode and the other is an anode. The top plasma-facing surface of the cathode is covered
with a target material and the reverse side is water-cooled. The substrates are placed on the
anode. When the sputtering chamber is kept in Ar gas as 0.1 Torr and several kilovolts of dc
voltage with series resistance of 1 to 10 kΩ are applied between the electrodes, the glow
discharge is initiated. The Ar ions in the glow discharge are accelerated at the cathode and
sputter the target resulting in the deposition of thin films on the substrates.

3.1.2 RF Sputtering

By simple substitution of an insulator target for the metal target in a dc diode sputtering
system, the sputtering glow discharge can not be sustained because of the immediate build-up of
a surface charge of positive ions on the front side of the insulator. To sustain the glow discharge
with an insulator target, the dc voltage power supply is replaced by a radio frequency power
supply. This system is called rf sputtering system. Sputtering in the rf-discharge was observed by
Robertson and Clapp in 1933 [101]. They found that the glass surface of the discharge tube was
sputtered during the rf discharge. In the 1960’s, sputtering in the rf-discharge has been used for
the deposition of dielectric thin films and a practical rf-sputtering system was developed [102,
103]. A typical sputtering system can be illustrated in Fig. 3-3. The rf sputtering system requires
an impedance matching network between the power supply and the discharge chamber. A typical
network for impedance matching is briefly shown in Fig. 3-4. The impedance of the rf-power
supply is almost always 50 Ω. The impedance of the glow discharge is of the order of 1 to 10 kΩ.
Typical frequency used for rf sputtering is 13.56 MHz. In a rf discharge system, the operating
pressure could be lowered to as low as 1 mTorr, since the rf electrical field in the discharge
chamber increases the collision probability between secondary electrons and gas molecules. In
the rf sputtering system, a blocking capacitor is connected between the matching network and the
target. The target area is much smaller than the grounded anode and the chamber wall. This
asymmetric electrode configuration induces negative dc bias on the target, and this causes
sputtering in the rf system. The dc bias is on the order of one half of the peak-to-peak voltage of
the rf power supply.

3.1.3 Magnetron Sputtering

Magnetron sputtering technology has made significant progress since its development in
early 1970s, for the high rate deposition of metal, semiconductor, and dielectric films. In
comparison to conventional diode sputtering, magnetron sputtering, apart from obtaining high
deposition rates at lower operating pressures, makes it possible to obtain high quality films at
low substrate temperatures. The basic principle of all magnetically enhanced sputtering
technique was discovered by Penning [104] more than 70 years ago and was subsequently
developed by Kay and others [105-108], resulting in the sputter gun [109] and cylindrical
magnetron sources [110]. The magnetron effect can be described as a closed drift path of crossed
electric and magnetic fields for electrons in a plasma discharge. For a simple planar magnetron
cathode, the arrangement consisted of planar cathode (target) backed by permanent magnets that
provide a toroidal magnetic field, with field lines forming a closed path on the cathode surface.
The difference in the mobilities of the ions and the electrons causes a positive ion sheath to be
developed close to the target cathode, floating at a negative potential relative to the plasma.
Because of the field due to the ion sheath at the cathode, ions are extracted from the plasma and
accelerated to strike the target, resulting in the sputtering of the target material. The second
electrons produced, upon entering the region of crossed electric and magnetic fields, are trapped
in orbits that permit long travel distances close to the cathode. In the zones of efficient electron trapping, the electron density reaches a critical value, at which the ionization probability due to the trapped electrons is at a maximum. This means that a higher rate of secondary electron production by high energy positive ions is not necessary for effective sputtering. Most magnetron sources operate in the pressure range from 1 to 20 mTorr and a cathode potential for 300-700 V. The sputtering rates are primarily determined by the ion current density at the target, and the deposition rates are affected by factors such as applied power, source to substrate distance, target material, pressure, and sputtering gas composition.

The preparation of barrier layers for this research work was carried out by a Kurt Lesker CMS-18 multi target sputter deposition system as shown in Figure 3-5. This sputtering system has 4 gas injected magnetron sputter sources, DC, RF and a rotating substrate holder with the ability of heating to 550 °C. The base pressure of the system was on the order of 10^-7 torr. Single crystal Si (100) wafer was used as the substrate. Prior to deposition, the substrates were etched in 7:1 buffered oxide etch (BOE) to remove native oxide, followed by a deionized water rinse for cleaning.

3.2 Sample Characterization

3.2.1 X-ray Diffraction

X-rays are electromagnetic radiation of wavelength about 1 Å, which is about the same size as an atom. The discovery of X-rays in 1895 enabled scientists to probe crystalline structure at the atomic level. X-ray diffraction (XRD) has been in use in two main areas, for the fingerprint characterization of crystalline materials and the determination of their structure. Each crystalline solid has its unique characteristic X-ray powder pattern which may be used as a "fingerprint" (JCPDS database) for its identification. Once the material has been identified, X-ray crystallography may be used to determine its structure. X-ray diffraction occurs when waves
scattering from an object constructively and destructively interfere with each other. The condition for constructive interference is governed by Bragg’s Law:

\[ 2d \sin \theta = n \lambda \]

where \( \lambda \) is the x-ray wavelength, \( d \) is the distance between atomic planes, and \( \theta \) is the angle between these planes and the x-ray source.

Powder X-ray Diffraction is perhaps the most widely used X-ray diffraction technique for characterizing materials. A Philips APD 3720 diffractometer was used to identify materials phases and examine the films microstructure and crystallinity in this work. The Philips system is configured in Bragg-Brentano geometry. The x-ray source is pointed at the sample and held in a fixed position. The sample rotates around the angle \( \theta \), and the detector rotates around \( 2 \theta \). In this \( \theta \)-\( 2 \theta \) geometry, only planes parallel to the sample surface can satisfy the Bragg condition. This provides crystalline orientation information of the deposited film. The intensity of the diffracted X-rays was measured as a function of the diffraction angle \( 2 \theta \). The scan range was set from 30 to 60 degree.

This system uses a Cu x-ray source that emits primarily Cu K\(_{\alpha 1}\) photons with a wavelength of 1.5405 Å. A Ni filter absorbs most of the other characteristic wavelengths from the source, although some Cu K\(_{\alpha 2}\) and K\(_{\beta}\) photons escape toward the sample. These wavelengths are important because they might generate extra diffraction peaks in the collected data.

The full width at half maximum (FWHM) peak in XRD spectra can be used to calculate the grain size of the crystallites by Scherrer’s equation [111]:

\[ d = \frac{0.9 \lambda}{B \cos \theta} \]

where \( d \) is the grain size, \( \lambda \) is the wavelength of x-ray, \( B \) is the full width at half maximum and \( \theta \) is the Bragg angle.
3.2.2 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is one of the major characterization techniques used routinely in materials science. A focus electron beam is swept over the surface of a specimen in a raster pattern, resulting in several emissions from the sample being detected. These emissions include backscattered electrons, auger electrons, secondary electrons, and X-rays. The interaction between beam and sample surface causes elastic and inelastic interactions, resulting in emission of secondary electrons. Due to their low energy, these electrons originate within a few nanometers (50-500 Å) from the surface. These secondary electrons are attracted to a cage by a bias of 50 V and strike the scintillator. Light from the scintillator is led by a light guide to a photomultiplier. To collect only backscattered electrons, the cage is placed in the line of sight of the specimen and secondary electrons are excluded by a negative bias of about 50 V. Topographic contrast can be observed because both backscattering and secondary electron emission depend on the angle of incidence of the electron beam. Differences in topography cause local difference in the angle of incidence and so lead to topographic contrast.

A JEOL 6400 scanning electron microscopy was used to investigate the sample surface topography. The operating voltage was set at 10 keV. Since the barrier samples were deposited with a Cu layer on top already, they were not coated with a carbon layer in order to preserve in its original status for other characterization measurements.

3.2.3 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is one of the most powerful tools to obtain high resolution lattice images and diffraction patterns of electron transparent samples. It provides more detailed information regarding microstructure of materials. The high spatial resolution is due to the fact that high energy electrons are used to probe the sample which have extremely fine structures.
small wavelength (on the order of Å). The wavelength of the electron depends on the energy as per the expression:

\[
\lambda \approx \frac{1.22}{\sqrt{E}}
\]

where \( \lambda \) is wavelength of electrons in nm, \( E \) is energy of electrons in eV.

A typical TEM operates at 200 to 400 keV. A highly coherent beam of monochromatic electrons is focused on the sample using a series of electromagnetic lenses. Image formation and contrast in the image depend on the details of electron scattering in the specimen. Scattering of electrons depends on the interaction of the electrons with electric and magnetic fields of a specimen. Electrons scattered by the field of the nucleus will undergo elastic scattering analogous to Rutherford scattering of heavy ions by nuclei, resulting in the formation of diffraction pattern under Bragg diffraction. Diffraction patterns play a key role in the characterization of crystalline materials by TEM. Such patterns provide a means of identifying phases. Also, diffraction is involved in imaging and analyzing defects. A diffraction pattern of a particular crystal in a polycrystalline array can be obtained by selected area diffraction (SAD).

In this research work, a JEOL 2010 field emission high resolution transmission electron microscopy (HRTEM) with operating electron voltage of 200 keV was used to determine the interfacial stability and intermetallic compound formation. By coupling the powerful imaging capabilities of TEM with energy dispersive X-ray spectrometer (EDS) within the microscope, the Cu diffusion depth profiles were acquired through a cross-section sample line scan.

### 3.2.4 Focused Ion Beam

There are a number of drawbacks to the TEM technique. One of which is that it requires extensive sample preparation to produce a sample thin enough for electron transmit, which makes TEM analysis a relatively time consuming process with a low throughput of samples.
The development of focus ion beam (FIB) makes it possible to prepare ultra-thin samples for TEM imaging with efficiency. The FIB is a scientific instrument that resembles a scanning electron microscope. However, while the SEM uses a focused beam of electrons to image the sample, a FIB instead uses a focused beam of charged ions, such as gallium ions. Gallium is chosen because it is easy to build a gallium liquid metal ion source. Gallium metal is placed in contact with a tungsten needle and heated. Gallium wets the tungsten, and a huge electric field (greater than $10^8$ volts per centimeter) causes ionization and field emission of the gallium atoms. The FIB can also be incorporated in a system with both electron and ion beam columns, allowing the same feature to be investigated using either of the beams. These ions are then accelerated to the energy of 5-50 keV, and then focused onto the sample by electrostatic lenses. Unlike an electron microscope, the FIB is inherently destructive to the specimen. When the high-energy gallium ions strike the sample, they will sputter atoms from the surface. Gallium atoms will also be implanted into the top few nanometers of the surface, and the surface will be made amorphous. In this research work, a FEI V600 focused ion beam system was used to prepare all the cross section HRTEM samples.

3.2.5 Auger Electron Spectroscopy

The Auger electron spectroscopy (AES) involves the analysis of electrons emitted from a sample surface as a result of incident radiation. The surface to be analyzed is irradiated with focus electron beams of sufficient energy, typically in the range of 2-10 keV, to ionize one or more core levels in surface atoms. The removal of core shell electron from the atom results in an excited state. A higher shell electron fills the core shell vacancy and the energy emitted by this transition is transferred in exciting another electron to emit from the atom which is called the Auger electron. Depending on the kinetic energy of the electron measured, the binding energy of the emitted Auger electron can be roughly estimated as the following equation:
\[ KE = (E_K - E_{L1}) - E_{L23} \]

where \( KE \) is the kinetic energy of the Auger electron, and \( E_K, E_{L1}, \) and \( E_{L23} \) are the energies of the K and L shells, respectively. Note that, the kinetic energy of the Auger electron is independent of the energy of the incident photon or electron. Since the production of an Auger electron requires at least three electrons for energy transition, as a result, H and He are undetectable with AES. In addition to Auger electron after ionization, the atom can relax by ejection of a characteristic X-ray photon as well. Although these are competing processes, for shallow core level (\( E_B < 2 \text{ keV} \)) the probability of the Auger process is far higher. Since the Auger energy is a function of atomic energy level only, no two elements have the same set of atomic bonding energies. Analysis of Auger energy provides elemental identification. The AES can be combined with an Ar ion gun, which could sputter the sample surface for surface cleaning. A chemical composition depth profile can be acquired by periodical sputtering of sample surface and detecting the auger electrons. The chemical composition of the barrier thin film via reactively sputter deposition was determined by Perkin-Elmer PHI 660 Scanning Auger Multiprobe.

### 3.2.6 Van der Pauw Measurement and Four Point Probe

The Van der Pauw method is one of the most effective and widely used methods of the four-probe mode in determining the resistivity of materials in the form of thin films. The technique doesn’t depend on the shape of sample. Four ohmic contacts are prepared on the four corners or periphery of a sample. Acceptable sample geometry for this measurement is shown in Fig. 3-6. When a DC current is applied between contacts 1 and 2 (\( I_{12} \)), a voltage is measured along contacts 3 and 4 (\( V_{43} \)) as shown in Figure 3-7. This resistance \( R_A \) is measured as follows:

\[ R_A = \frac{V_{43}}{I_{12}} \]
This is followed by another measurement by applying DC current between contacts 1 and 4 (I_{14}) and voltage is measured between contacts 2 and 3 (V_{23}). This gives resistance $R_B$ as given by the following equation:

$$R_B = \frac{V_{14}}{I_{23}}$$

The sheet resistance $R_S$ is determined in relation to $R_A$ and $R_B$ through the following equation:

$$\exp\left(\frac{-\pi R_A}{R_S}\right) + \exp\left(\frac{-\pi R_B}{R_S}\right) = 1$$

As a result, the bulk resistivity can be calculated by the following equation:

$$\rho = R_S d$$

The four-point probe method is widely used today because it can measure the electrical resistance of semiconductors or metal films easily, without any patterning processes. A four point probe forces a current through the two outside probes and measures the resulting voltage drop across two inside probes as shown in Fig. 3-8.

The resistivity of the barrier films was determined using Van der Pauw method. The sheet resistance of copper before and after annealing was determined by a standard four point probe in this work.
Figure 3-1. Sputter deposition.
Figure 3-2. A classification of gas discharge for various discharge currents.
Figure 3-3. Schematic illustration of rf sputtering system.
Figure 3-4. Impedance matching network for rf-sputtering system.
Figure 3-5. Kurt Lesker CMS-18 multi target sputter deposition system.
Figure 3-6. Sample geometry for Van der Pauw measurements.
Figure 3-7. Schematic of a van der Pauw configuration used in the determination of the two characteristic resistances $R_A$ and $R_B$.

\[ R_A = \frac{V_{43}}{I_{12}} \]

\[ R_B = \frac{V_{14}}{I_{23}} \]
Figure 3-8. Schematic of 4-point probe configuration.
CHAPTER 4
PROPERTIES OF ULTRATHIN IRIDIUM THIN FILM AS A DIFFUSION BARRIER FOR CU INTERCONNECTS

4.1 Introduction

As the device dimensions continue to scale down, the development of new barrier materials will be needed [112-116]. Noble metals, including Ru, Pd, Pt, Rh, Ir, Ag, and Os, have been suggested as replacement materials for the liner [8], and direct copper electroplating with excellent conformity has been successfully demonstrated for Ru [9], Os [10], and Ir [11]. However, recent studies on Ru/Si thin films suggest that Ru itself is not a good barrier against copper diffusion [114-116]. Arunagiri et al. [116] reported that a 5 nm Ru thin film is effective as a copper diffusion barrier only for temperatures up to 300 °C.

As one of the platinum group metals, Ir is potentially attractive as a barrier material. It has a high melting point of 2446 °C and low resistivity of 4.71 \( \mu \Omega \text{cm} \). Iridium is relatively stable in contact with Cu with no intermediate compound formation and negligible solubility at high temperatures as shown in the Cu-Ir binary phase diagram [117]. These excellent physical properties suggest that iridium could be a good candidate for future copper diffusion barrier application. Accordingly, it would be interesting to study the properties of iridium as a barrier against Cu diffusion.

4.2 Experimental Description

Iridium thin films were deposited on Si (100) wafers by magnetron sputtering at room temperature. Film thickness was controlled at 5 nm. Prior to deposition, the substrate was etched in 7:1 buffered oxide etch to remove the native oxide, followed by a deionized water rinse. The base pressure of the chamber was on the order of 5x10^-7 Torr and the working pressure was kept at 5 mTorr throughout the deposition. The DC sputtering power for the 3 inch Ir target was 100
W. Under such conditions, the measured deposition rate was 0.95 Å/sec. During the deposition process, the substrates were rotated at 20 rpm to ensure film uniformity.

A 200 nm thick Cu layer was deposited on top of the iridium barrier in situ at room temperature without breaking the vacuum. The forward sputtering power for Cu deposition was 200 W. The chamber pressure was kept at 5 mTorr Ar throughout the process. Diffusion barrier properties were examined by annealing the structures in vacuum (10⁻⁵ Torr) over a temperature range of 300-600 °C for 1 h. The film crystallinity and intermetallic phase formation were determined using a Philips APD 3720 X-ray diffractometer. The interfacial stability of the film stack and copper depth profile were examined using a JEOL 2010F high resolution transmission electron microscope along with a JEOL Superprobe 733 energy-dispersive spectrometer. For electrical properties characterization, a four point probe was used to measure the sheet resistance of the film stacks.

### 4.3 Results and Discussion

Figure 4-1 shows the X-ray diffraction patterns for the Cu/Ir(5 nm)/Si structures both as-deposited and annealed in the temperature range of 300-600 °C for 1 h in vacuum. As evident from Fig. 4-1, upon annealing at 400 °C, no copper silicide diffraction peaks were present, implying no significant copper diffusion through the iridium barrier. This revealed that the diffusivity of copper in iridium is relatively low at 400 °C. Due to grain growth upon heat treatment, copper film crystallinity improved as evidenced by the sharpening of the Cu (111) and (200) diffraction peaks. Further annealing yielded copper diffusion through the barrier and the formation of copper silicide as indicated by the presence of copper silicide diffraction peaks in the samples annealed at 500 °C and above.

Figure 4-2 shows the HRTEM images of the Cu/Ir (5 nm)/Si film stacks before and after annealing at 400 °C for 1 h. As shown in the as-deposited sample, the thickness of Ir barrier is
approximately 5 nm and is uniform throughout the sample. Note that a 2 nm amorphous interlayer lied between the Ir and Si. This amorphous layer might be amorphous iridium silicide formed at room temperature [118,119] by the diffusion of silicon into iridium [120]. High temperature annealing caused iridium to diffuse further into the adjacent silicon and copper layers as evidenced by the expansion of the dark iridium region shown in Fig. 4-2b. In agreement with the XRD data, no copper silicide formation is seen in the HRTEM image at the interface upon annealing at 400 °C.

The direct means to examine the diffusion of Cu through the barrier is by acquiring chemical depth profile. EDS line scans on the cross section TEM sample were performed to obtain the copper diffusion depth profiles. The EDS atomic depth profiles of the as-deposited film stack are shown in Fig. 4-3. As clearly seen in the depth profile, a narrow and sharp iridium peak lies between copper and silicon. The EDS Cu signal declines sharply at the position of iridium peak, indicating no copper diffusion into silicon at room temperature. However, a noticeable overlap of silicon and iridium signals exists in the profile as a result of the diffusion of silicon into iridium. The formation of iridium silicide occurred at room temperature. For the 350 °C annealed stack shown in Fig. 4-4, the iridium intensity spread slightly towards both silicon and copper. Similar to the Cu depth profile acquired for the barrier stack before annealing, the Cu intensity decreased to its baseline before the Ir/Si interface, indicating no Cu diffusion across the barrier upon annealing at 350 °C. However, further high temperature annealing leaded to perturbation of the iridium bonding, which resulted in the out diffusion of iridium and further silicidation. As shown clearly in Fig. 4-5, the iridium intensity profile broadened, resulted in slight diffusion of Cu into Si substrate. The failure of 5 nm iridium barrier at 400 °C indicates a limited effectiveness for ultrathin iridium film as a copper diffusion blocking layer on Si.
The sheet resistance of Cu for the barrier stack before and after annealing is shown in Fig. 4-6. Due to grain growth upon annealing, Cu sheet resistance decreased slightly with increasing temperature until the copper diffusion through the barriers took place. A noticeable increase of Cu sheet resistance occurred at 500 °C as a result of copper diffusion through the barrier and the formation of more resistive copper silicide.

4.4 Conclusion

In summary, the effectiveness of 5 nm iridium as a diffusion barrier for Cu was investigated. No copper silicide diffraction peaks were present up to annealing at 400 °C for 1 h. HRTEM images and EDS cross section line scans revealed the formation of iridium silicide in the Ir/Si interface at room temperature. The EDS copper depth profile indicated limited blocking of copper diffusion by the iridium barrier upon annealing at 400 °C. Further heating resulted in iridium out-diffusion and the formation of a less dense iridium barrier, which failed as a barrier against copper diffusion. The Cu sheet resistance first decreased due to Cu grain growth after heat treatment, followed by an increase as the result of more resistive Cu silicide formation at 500 °C. Overall, the results indicated that a 5 nm Ir thin film was an effective barrier against copper diffusion at 350 °C. In order to avoid silicidation with Si and to improve its barrier properties against copper diffusion, an additional barrier layer is needed.
Figure 4-1. X-ray diffraction patterns of as-deposited and annealed Cu/Ir(5 nm)/Si (001).
Figure 4-2. HRTEM images of Cu/Ir(5 nm)/Si (001) stack (a) as-deposited and (b) annealed at 400 °C for 1 h.
Figure 4-3. EDS depth profile of as-deposited Cu/Ir(5 nm)/Si (001) stack.
Figure 4-4. EDS depth profile of Cu/Ir(5 nm)/Si (001) stack annealed at 350 °C for 1 h.
Figure 4-5. EDS depth profile of Cu/Ir(5 nm)/Si (001) stack annealed at 400 °C for 1 h.
Figure 4-6. Sheet resistance of Cu vs. annealing temperature for Cu/Ir(5 nm)/Si.
CHAPTER 5
IR/TAN AS A BILAYER DIFFUSION BARRIER FOR ADVANCED CU INTERCONNECTS

5.1 Introduction

There is significant interest in the use of various nitrides as copper diffusion barriers. For example, the bilayer structures Ru/TaN [121] and Mo/WN [122] have been shown to be thermally stable and can provide reasonable adhesion to Cu. As the most common nitride barrier currently used in integrated circuit processing, TaN is an effective barrier even at very small dimensions [123]. In order to avoid iridium silicidation with the underlying Si, one can engineer Ir with TaN so as to achieve direct copper electroplating and enhance barrier properties against copper diffusion.

5.2 Experimental Description

TaN thin films (5 nm thick) were deposited at room temperature on Si (100) wafers by magnetron sputtering using a 3” stoichiometric TaN target. Ir thin films (5 nm) were then deposited in-situ on top of the TaN later to form a bilayer barrier. Prior to deposition, the substrate was etched in 7:1 buffered oxide etch (BOE) to remove the native oxide, followed by deionized water rinse. The base pressure of the chamber was kept on the order of 5x10^{-7} Torr. The working pressure of Ar gas was kept at 5 mTorr throughout the deposition. The RF sputtering forward power for TaN was 200 W with a deposition rate of 0.7 Å/sec. The DC sputtering power for a 3 inch Ir target was 100 W. Under such conditions, the measured Ir deposition rate was 0.95 Å/sec. During the deposition process the substrates were rotated at 20 rpm to ensure film uniformity.

A 200 nm thick Cu layer was subsequently deposited on top of the iridium barrier in-situ at room temperature without breaking vacuum. The DC sputtering power for Cu deposition was 200 W. The chamber pressure was kept at 5 mTorr Ar throughout the deposition process.
Diffusion barrier properties were examined by annealing the structures in vacuum at a base pressure less than $10^{-5}$ Torr over a temperature range of 400-800 °C for 1 h. The film crystallinity and intermetallic phase formation were determined using a Philips APD 3720 X-ray diffractometer. The interfacial stability of the film stack and copper depth profile were examined using a JEOL 2010F high resolution transmission electron microscope along with a JEOL Superprobe 733 energy-dispersive spectrometer. The surface morphology of the films was examined using a JEOL 6400 scanning electron microscope.

5.3 Results and Discussion

Figure 5-1 shows the X-ray diffraction patterns for as-deposited and annealed barrier stacks. Before annealing, a strong Cu (111) and weak Cu (200) peak were present along with Ir (111) crystalline orientation. After heat treatment, the Cu (200) diffraction peak was suppressed and the Cu (111) texture became sharper. Note that the copper electromigration resistance should be enhanced by the realization of a better Cu (111) texture after high temperature annealing. Upon annealing up to 600 °C for 1 h, the integrity of the Ir/TaN was maintained with no copper silicide peaks shown in the X-ray diffraction pattern. This was further confirmed by SEM in which no copper silicide crystallites were observed. The onset of copper diffusion through the barrier occurred upon annealing at 650 °C, as evidenced by the presence of the copper silicide peaks. After annealing at 800 °C for 1 h, no Cu peak was present, indicating complete Cu diffusion through the Ir/TaN barrier into the Si substrate. The high temperature performance of this bilayer as a copper diffusion barrier can be primarily attributed to the thermal stability of the nanocrystalline TaN layer [123], which can effectively block Cu diffusion up to 600 °C.

Figure 5-2 shows the cross section HRTEM images of Cu/Ir/TaN/Si film stacks before and after annealing at 600 °C for 1 h. As shown in the image of the as-grown stack, the barrier thickness is approximately 5 nm for both the iridium and tantalum nitride barriers, which
matches the deposition target thickness. This confirms the precise control of the barrier thickness through sputter deposition. Note that a thin native SiO$_2$ layer at the Si interface presumably formed after BOE etching and subsequent to loading into chamber. For some samples, the time delay between BOE etching and loading into the chamber was 2 h. The thickness of the SiO$_2$ interfacial layer was typically 1-3 nm and did not correlate with barrier layer processing conditions. The interface integrity and abruptness of the barrier stack before annealing is clearly seen in Fig. 5-2(a). After annealing, as a result of out diffusion, the iridium barrier has slightly expanded toward both sides. However, the TaN/SiO$_2$/Si interface remained intact upon annealing at 600 °C, as seen in Fig. 5-2(b). No intermetallic compounds were observed at the interfaces, which is consistent with the XRD data shown previously.

The atomic depth profiles for Cu/Ir/TaN/Si film stacks before and after annealing at 600 °C for 1 h were acquired using EDS on cross-section TEM samples at an accelerating voltage of 200 kV. Note that the EDS detector has limited ability to differentiate between Ta and Cu signals through line scans due to energy peaks overlap in the EDS spectrum. As such, the Ta signal overlapped the Cu signal in the entire region of the Cu layer for both cases. As seen in Fig. 5-3, the Cu intensity profile declined sharply to its baseline as the scan moved into the Si substrate for the as-deposited stack. After annealing at 600 °C for 1 h, the Cu intensity profile showed minimal change as shown in Fig. 5-4. Again, the EDS Cu signal returned to its baseline as the scan moved into the Si substrate, indicating no diffusion through the barrier into Si.

5.4 Conclusion

In summary, the performance of an Ir (5 nm)/TaN (5 nm) bilayer structure as a diffusion barrier for Cu metallization on Si was examined. The XRD data showed that no copper silicide diffraction peaks were present after annealing at 600 °C for 1 h, indicating excellent thermal stability for the Cu/Ir/TaN/Si stack. The HRTEM images showed that the integrity of the stack
interfaces was intact and no intermetallic compound was formed after annealing at 600 °C. Elemental EDS profiles showed a sharp decline in the Cu intensity profile at the barrier/substrate interface for the barrier stacks before and after annealing at 600 °C. The above results indicate that an Ir (5 nm)/TaN (5 nm) bilayer is an attractive liner composition, providing a template for direct copper electrodeposition to achieve Cu superfilling and is thermally stable to block copper diffusion.
Figure 5-1. X-ray diffraction patterns of as-deposited and annealed Cu/Ir(5 nm)/TaN(5 nm)/Si (001) structures. Annealing time was 1 h.
Figure 5-2. HRTEM images of Cu/Ir(5 nm)/TaN(5 nm)/Si (001) (a) as-deposited and (b) annealed at 600 °C for 1 h.
Figure 5-3. EDS depth profile of as-deposited Cu/Ir(5 nm)/TaN(5 nm)/Si (001) stack.
Figure 5-4. EDS depth profile of Cu/Ir(5 nm)/TaN(5 nm)/Si (001) stack annealed at 600 °C for 1 h.
CHAPTER 6
PD/TAN AS A BILAYER DIFFUSION BARRIER FOR CU INTERCONNECTS

6.1 Introduction

The present damascene copper metallization are fabricated by Cu electroplating due to its low processing temperature, good step coverage, high selectivity and low cost [124-126]. However, with the continual shrinkage in interconnection dimensions, it is increasingly difficult to deposit a continual Cu seed layer via sputtering on the sidewalls for lateral electroplating [127]. One possible solution to achieve sufficient gap-filling is by Cu electroless plating with the utilizing of Pd as a catalyst for copper nucleation [128-130]. Copper electroless deposition is a low temperature and low cost process without the consumption of electrical power, providing good gap filling capability with high selectivity. Much research has been conducted in developing uniform and low resistive electroless plated copper through the Pd activation process or electroless plating solution [131-140].

The Cu/Pd/Si structure has been shown to have a rather low thermal stability as a result of interdiffusion and silicidation at low temperatures [141]. Cu is highly mobile in silicon and silicon dioxide. Without introducing a barrier layer to prevent Cu diffusion, Cu would penetrate into underlying dielectrics or Si, resulting in deteriorating device operation. The thermal stability of Pd/Nitirde barrier associated with Cu diffusion has rarely been addressed. As the most common nitride barrier used in current integrated circuit processing, TaN is an effective barrier even at very small dimensions [123]. To avoid Pd silicidation and enhance thermal stability of the contact system, TaN barrier could be engineered with Pd to achieve electroless copper deposition for the fabrication of ultralarge scale integrated interconnects. The object of this work is to examine the thermal stability of Cu/Pd/TaN/Si contact system for the application of electroless Cu deposition for future Cu damascene process.
6.2 Experimental Description

TaN thin films (5 nm thick) were deposited at room temperature on Si (100) wafers by magnetron sputtering using a 3” stoichiometric TaN target. Pd thin films (approximately 5 nm) were then deposited in-situ on top of the TaN film to form a bilayer structure. Prior to deposition, the substrate was etched in 7:1 buffered oxide etch (BOE) to remove the native oxide, followed by deionized water rinse. The base pressure of the chamber was on the order of 5x10^{-7} Torr. The working pressure of Ar gas was kept at 5 mTorr throughout the deposition. The RF sputtering forward power for TaN was 200 W with a deposition rate of 0.7 Å/sec. The DC sputtering power for a 3 inch Pd target was 100 W. During the deposition process the substrates were rotated at 20 rpm to ensure film uniformity.

An approximately 150 nm thick Cu layer was then deposited on top of Pd via electroless deposition. As listed in Table 6-1, the electroless Cu plating bath contains CuSO₄ • 5H₂O (8 g/L), ethylenediaminetetraacetic acid (EDTA, 25 g/L), polyethylene glycol (PEG, Mw 4000, 1 g/L), 2, 2′-bipyridine (0.8 g/L), formaldehyde (HCHO, 37%, 8 g/L) and tetramethyl ammonium hydroxide (TMAH) as a PH controller. The PH of the plating solution was adjusted to between 11 and 12 at the bath temperature 65 °C. Diffusion barrier properties were examined by annealing the structures in vacuum at a base pressure less than 10^{-5} Torr over a temperature range of 400-700 °C for 1h. The film crystallinity and intermetallic phase formation were determined using a Philips APD 3720 X-ray diffractometer. The interfacial stability of the film stack and copper depth profile were examined using a JEOL 2010F high resolution transmission electron microscope along with a JEOL Superprobe 733 energy-dispersive spectrometer. For electrical properties characterization, a standard four point probe was used to measure the sheet resistance of film stacks.
6.3 Results and Discussion

Figure 6-1 shows the X-ray diffraction patterns for as-deposited and annealed Cu/Pd/TaN/Si film stack. Before annealing, both Cu (111) and Cu (200) peaks were present. There was minimum change in the diffraction patterns of the structure up to the annealing temperature of 550 °C for 1 h in vacuum. Note that the intensity of Cu peaks should increase as a result of Cu grain growth after heat treatment. The evidence of no copper silicide peaks present at 550 °C implies no occurrence of significant copper diffusion. Further annealing at higher temperatures induced sufficient copper diffusion through the barrier to react with Si and formed copper silicide, as evidenced by the onset of the copper silicide peaks at 600 °C.

Figure 6-2 shows the cross section HRTEM images of Cu/Pd/TaN/Si film stacks before and after annealing at 550 °C for 1 h. As shown in the image of the as-grown stack, the barrier thickness for both TaN and Pd layer is approximately 5 nm. A thin native SiO₂ layer about 3 nm thick was been at the Si interface, which was presumably formed after BOE etching and subsequent to loading into chamber. The interface integrity and abruptness of the barrier stack before annealing can be roughly seen in Fig. 6-2(a). As a result of out-diffusion into adjacent Cu layer upon high temperature annealing, only TaN layer remained, as seen in Fig. 6-3(b). This revealed the thermal instability of Pd in contact with Cu at elevated temperatures. In fact, the Pd-Cu binary phase diagram revealed that Pd and Cu tend to form complete solid solution [142]. However, the TaN/SiO₂/Si interface remained intact upon annealing at 550 °C and no intermetallic compounds were observed at the interfaces, which is consistent with the XRD data shown previously.

The atomic depth profiles for Cu/Pd/TaN/Si film stacks before and after annealing at 550 °C for 1 h were acquired using EDS line scan on the XTEM samples. Again, because of EDS
detector’s limited ability to differentiate between Ta and Cu signals due to energy peaks overlap in the EDS spectrum, the Ta signal overlapped with the Cu signal in the entire region of the Cu layer. However, both Ta and Cu intensity profiles declined to their baseline before the scan moved into Si substrate for the as-deposited stack, as shown in Fig. 6-3. This provides us a reference to compare with the annealed stack. After annealing, the Cu intensity profile showed minimal change as shown in Fig. 6-4. The Cu intensity returned to its baseline before it reached the TaN/Si interface, indicating that this bilayer barrier structure was able to block Cu diffusion at 550 °C. Compared to the EDS Pd intensity profile before annealing [Fig. 6-3], the Pd intensity peak was greatly suppressed after annealing [Fig. 6-4]. This is consistent with the HRTEM image shown in Fig. 2(b), which showed the absence of Pd layer as a result of diffusion into Cu to form Cu-Pd solid solution.

The sheet resistance of Cu for the barrier stack before and after annealing is shown in Fig. 6-5. As a result of Cu grain growth after heat treatment, the sheet resistance of Cu slightly decreased until 550 °C, implying no resistive copper silicide formed in the stack interfaces since such reaction would cause the increase of the sheet resistance. Note that the diffusion of Pd into Cu matrix did not cause the increase of Cu sheet resistance. The improvement of Cu crystallinity might counteract the influence of Pd diffusion, yielding a less resistive Cu film. Upon annealing at 600 °C, the sheet resistance of Cu increased noticeably due to the onset of the diffusion and the formation of more resistive copper silicide crystallites. Further annealing at 700 °C drove more Cu into Si, resulting in a drastic increase.

6.4 Conclusion

In summary, the thermal stability of Pd (5 nm)/TaN (5 nm) bilayer structure for Cu metallization on Si was examined. The XRD data showed that no copper silicide diffraction
peaks were present after annealing at 550 °C for 1 h, indicating suitable thermal stability for this Cu/Pd/TaN/Si contact system. The HRTEM images showed that the integrity of the TaN/SiO₂/Si interfaces was kept intact and no intermetallic compound was formed after annealing. Pd totally diffused into Cu at 550 °C. Elemental EDS profiles showed the interdiffusion of Pd with Cu, and a sharp decline in the Cu intensity profile at the barrier/substrate interface, indicating no Cu diffusion into the Si substrate. The above results demonstrated that the Pd (5 nm)/TaN (5 nm) bilayer structure is thermally stable up to 550 °C for 1 h and that it is suitable for the application in electoless plated Cu damascene process for future ultralarge scale integrated (ULSI) circuits.
Table 6-1. Solution composition of electroless Cu deposition bath

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>CuSO₄ • 5H₂O</td>
<td>Cu ions provided</td>
<td>6-10 g/L</td>
</tr>
<tr>
<td>EDTA</td>
<td>Chelating agent</td>
<td>23-35 g/L</td>
</tr>
<tr>
<td>TMAH</td>
<td>pH buffer</td>
<td>100-140g/L</td>
</tr>
<tr>
<td>PEG</td>
<td>Surfactants</td>
<td>0.5-1.5 g/L</td>
</tr>
<tr>
<td>2,2'-bipyridine</td>
<td>Stabilizer and surfactants</td>
<td>0.1-1.2 g/L</td>
</tr>
<tr>
<td>HCHO (37%)</td>
<td>Reducing agent</td>
<td>6-10 mL/L</td>
</tr>
</tbody>
</table>
Figure 6-1. X-ray diffraction patterns of as-deposited and annealed Cu/Pd(5 nm)/TaN(5 nm)/Si (001) structures. Annealing time was 1 h.
Figure 6-2. HRTEM images of Cu/Pd(5 nm)/TaN(5 nm)/Si (001) (a) as-deposited and (b) annealed at 550 °C for 1 h.
Figure 6-3. EDS depth profile of as-deposited Cu/Pd(5 nm)/TaN(5 nm)/Si (001) stack.
Figure 6-4. EDS depth profile of Cu/Pd (5 nm)/TaN(5 nm)/Si (001) stack annealed at 550 °C for 1 h.
Figure 6-5. Sheet resistance of Cu vs. annealing temperature for Cu/Pd/TaN/Si stack.
CHAPTER 7
PROPERTIES OF REACTIVELY SPUTTERED W-B-N THIN FILMS AS A DIFFUSION BARRIER FOR CU METALLIZATION ON SI

7.1 Introduction

The low resistive, metallic tungsten boride based ternary materials have led to an interest in developing W-B-N diffusion barriers [97-100]. The barrier thickness for previous reports on W-B-N was too large to be applicable as the demand of liner thickness has been down to few nanometers only. As such, Cu diffusion barrier properties of reactively sputtered 10 nm W-B-N thin films as a function of chemical composition were investigated.

7.2 Experimental Description

W-B-N barrier films were deposited on Si (100) wafers via magnetron sputtering at room temperature using a 3” stoichiometric W$_2$B target. Prior to deposition, the substrates were etched in 7:1 buffered oxide etch (BOE) to remove native oxide, followed by a deionized water rinse. The base pressure of the chamber was kept below 5x10$^{-7}$ Torr. Before deposition, the sputtering target was presputtered at an Ar gas pressure of 15 mTorr for 10 minutes. The forward RF sputtering power for W$_2$B was 200 W. The W-B-N film deposition was carried out at an ambient pressure of 10 mTorr with various N$_2$/(Ar+N$_2$) flow ratios. During the deposition the substrates were rotated at 20 rpm to ensure film uniformity.

After deposition of the nitride films, a 200 nm thick Cu layer was deposited on the barrier \textit{in situ} at room temperature without breaking the vacuum. The forward sputtering power for Cu deposition was 200 W. The chamber pressure was kept at 5 mTorr Ar throughout the process. Diffusion barrier properties were examined by annealing the samples in vacuum at a base pressure less than 10$^{-5}$ Torr over the temperature range 300 to 700 °C for 1h. The chemical composition of the films was determined by Auger electron spectroscopy using a Perkin-Elmer PHI 660 scanning Auger multiprobe. The films resistivity was measured by the Van der Pauw
method. The film crystallinity and intermetallic phase formation were determined using a Philips APD 3720 X-ray diffractometer. The integrity of the stack films and chemical depth profile of Cu through the diffusion barrier were evaluated using a JEOL 2010F high resolution electron transmission microscope along with a JEOL Superprobe 733 energy-dispersive spectrometer. For characterization of electrical properties, a four point probe was used to measure the sheet resistance of Cu layer.

7.3 Results and Discussion

The chemical composition of W-B-N thin films deposited at various N2/(Ar+N2) flow ratios was determined using Auger electron spectroscopy (Table 7-1). Before characterization, Ar ion sputter was performed in situ for 3 minutes for surface cleaning. The N content in the films increased slightly with increasing N2 flow ratio, ranging from 6 to 15 at. % as N2 flow ratio rose from 5 to 25 %. The films contained some oxygen ranging from 11 at. % to 18 at. %, possibly due to exposure to the atmosphere prior to analysis. Table 7-1 also lists the resistivity of the W-B-N films, which ranges from 159.92 to 240.4 $\mu\Omega cm$. The resistivity of the films increased with increasing N2 flow ratio and was strongly composition dependent. Note that the film deposited at 5 % N2 flow ratio had the lowest resistivity of 159.92 $\mu\Omega cm$, which is desirable for a liner material.

Figure 7-1 shows the X-ray diffraction patterns for W-B-N thick films deposited at various N2 flow ratios. Except for the film deposited at 10 % N2 flow ratio, which shows evidence of polycrystalline texture with likely $\beta$-W$_2$N (111) and (200) peaks, the films were amorphous. After high temperature annealing of the barrier stacks, sheet resistance measurements were conducted to examine the failure temperature of the Cu/ W-B-N (10 nm)/Si barrier stack. Figure 7-2 compares the Cu sheet resistance results of the barrier stack after the annealing tests for
materials prepared at different N₂ flow ratios. The Cu sheet resistance first decreased gradually as a result of Cu grain growth as evidenced by the sharpening of the Cu (111) diffraction peaks shown in Fig. 7-3. The onset of the barrier failure can be determined by the increase of the sheet resistance as a result of intermixing at the barrier interfaces and the formation of more resistive copper silicide. The failure temperatures of 10 nm W-B-N barrier stack at various N₂ flow ratios are also summarized in Table 7-1. As expected, because of its polycrystalline texture, which provided grain boundaries as pathways for facile Cu diffusion, the barrier deposited at 10 % N₂ flow ratio began to exhibit increased sheet resistance abruptly at 500 °C, indicating the failure of the barrier. For the barriers deposited at other N₂ flow ratios, the sheet resistance did not increase until 550 °C, because their amorphous structure lacked the grain boundaries that provide paths for fast Cu diffusion.

To further investigate the structural change and intermetallic compound formation upon annealing in relation to sheet resistance change, X-ray diffraction was carried out for as-deposited and annealed Cu/W-B-N(10 nm)/Si barrier stacks prepared at 5 % N₂ flow ratio. As seen in Fig. 7-3, except for the increase of Cu (111) and Cu (200) peaks as a result of Cu grain growth after heat treatment, there was minimal change in the diffraction patterns of the structure up to an annealing temperature of 550 °C. The fact that there is a detectable change of the sheet resistance for the samples annealed at 550 °C but copper silicide peaks could not be observed in the diffraction pattern reveals the limitation of XRD θ/2θ scans in detecting the reaction layer developed in the preliminary intermixing crystallization stage. Further annealing at higher temperature induced Cu diffusion through the barrier into Si to form sufficient copper silicide for XRD detection, as evidenced by the onset of the copper silicide peaks at 600 °C.
To further investigate barrier microstructure, grain size, or any possible intermediate compound formed in the interfaces, HRTEM was carried out on cross-section TEM samples cut by focused ion beam techniques. Figure 7-4 shows the XTEM images of as-deposited and 500 °C annealed Cu/W-B-N (10 nm)/Si barrier stacks prepared at a 5 % N₂ flow ratio. The thickness of the W-B-N layer is approximately 10 nm and is uniform throughout the whole sample. Consistent with the XRD result, the microstructure of the barrier was further confirmed as amorphous through HRTEM images. Note that this amorphous structure did not change after annealing at 500 °C for 1 h, thus effectively blocking the copper diffusion through the barrier. The interface integrity of the barrier before and after annealing showed essentially no difference, indicating suitable thermal stability. The Cu depth profile for this barrier stack was examined through EDS line scan on the XTEM sample. Figure 7-5 shows the atomic depth profile for the 500 °C annealed W-B-N barrier stack prepared at a 5 % N₂ flow ratio. As seen clearly, the Cu signal declines sharply to its baseline before reaching the W-B-N/Si interface, although a small amount of Cu did penetrate into the W-B-N layer. Nevertheless, the Cu signal was undetectable before the scan moved into the Si substrate, indicating no Cu diffusion into Si.

7.4 Conclusions

The properties of 10 nm thick W-B-N thin films deposited via reactive magnetron sputter at various N₂ flow ratios (5 % ~ 25 %) were examined. Films deposited at room temperature were mainly amorphous, yet exhibited very low resistivity, with a minimum value of 159.92 μΩcm for films as-deposited at 5 % N₂ flow ratio. Both sheet resistance and XRD data were consistent with a lack of copper diffusion through the barrier after annealing at 500 °C for 1 h, indicating the thermal stability for the Cu/W-B-N/Si system. The HRTEM images showed that the integrity of the stack interfaces was intact and no intermetallic compound was formed after annealing at 500 °C.


° C. Elemental EDS profiles on the annealed sample showed a sharp decline in the Cu intensity profile at the barrier/substrate interface, indicating no Cu diffusion into the Si substrate. The above results demonstrated that 10 nm W-B-N thin films deposited at 5 % N₂ flow ratio would be a potential candidate as a diffusion barrier for copper metallization schemes.
Table 7-1. Chemical composition, resistivity, and barrier failure temperature of W-B-N thin films deposited at various N2 flow ratios.

<table>
<thead>
<tr>
<th>(N₂/N₂+Ar)</th>
<th>W (at. %)</th>
<th>B (at. %)</th>
<th>N (at. %)</th>
<th>O (at. %)</th>
<th>Resistivity ($\mu\Omega \text{cm}$)</th>
<th>Failure Temperture (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5%</td>
<td>43</td>
<td>33</td>
<td>6</td>
<td>18</td>
<td>159.9</td>
<td>550</td>
</tr>
<tr>
<td>10%</td>
<td>43</td>
<td>32</td>
<td>10</td>
<td>15</td>
<td>217.6</td>
<td>500</td>
</tr>
<tr>
<td>15%</td>
<td>40</td>
<td>32</td>
<td>10</td>
<td>18</td>
<td>240.4</td>
<td>550</td>
</tr>
<tr>
<td>25%</td>
<td>40</td>
<td>34</td>
<td>15</td>
<td>11</td>
<td>209.6</td>
<td>550</td>
</tr>
</tbody>
</table>
Figure 7-1. X-ray diffraction patterns of W-B-N films deposited at various N₂ flow ratios.
Figure 7-2. Sheet resistance of Cu vs. annealing temperature for W-B-N barrier stack deposited at various N$_2$ flow ratios.
Figure 7-3. X-ray diffraction patterns of as-prepared and annealed Cu/W-B-N/Si barrier stack. (W-B-N film was deposited at 5 % N₂ flow ratio)
Figure 7-4. Cross-section HRTEM images of Cu/W-B-N (10 nm)/Si (001) (a) as-prepared and (b) annealed at 500 °C for 1 h. (W-B-N film was deposited at 5 % N₂ flow ratio)
Figure 7-5. EDS depth profile of Cu/W-B-N(10 nm)/Si barrier stack annealed at 500 °C for 1 h.
(W-B-N film was deposited at 5 % N\textsubscript{2} flow ratio)
CHAPTER 8
COMPARATIVE STUDY OF ZRN AND ZR-GE-N THIN FILMS AS DIFFUSION BARRIERS FOR CU METALLIZATION ON SI

8.1 Introduction

Like most refractory metal nitrides, ZrN has a high melting temperature of 2960 °C. The lowest electrical resistivity reported in bulk for ZrN is 13.6 $\mu\Omega \text{cm}$ [76]. The standard heat of formation of ZrN at 298 °K, $\Delta H_f = -87.3 \text{ kcal/mol}$ [77], is more exothermic than that of TiN (-80.4 kcal/mol) and TaN (-60.3 kcal/mol), suggesting greater thermodynamic stability of the ZrN compound as compared to other refractory metal nitrides. The aforementioned properties make it an interesting barrier material for copper metallization application [78-81]. In this research work, the comparison between the diffusion barrier properties of ZrN and Zr-Ge-N thin films for copper metallization was investigated.

8.2 Experimental Description

ZrN and Zr-Ge-N films were deposited on Si (100) wafers via magnetron sputtering at room temperature. A stoichiometric ZrN target was used for ZrN film growth. The Zr-Ge-N samples were prepared by cosputtering of ZrN and Ge targets. Prior to deposition, the substrate was etched in 7:1 buffered oxide etch (BOE) to remove native oxide, followed by deionized water rinse. The base pressure of the chamber was on the order of 5x10^{-7} Torr. Before deposition, the sputtering targets were presputtered at an Ar gas pressure of 15 mTorr for 10 min. The forward sputtering power for ZrN and Ge was 200 and 100 W, respectively. Nitride film growth was carried out at a fixed Ar pressure of 10 mTorr. During the deposition the substrates were rotated at 20 rpm to ensure film uniformity.

After deposition of the nitride films, a 200 nm thick Cu layer was deposited on the barriers in situ at room temperature without breaking the vacuum. The forward sputtering power for Cu
deposition was 200 W. The chamber pressure was kept at 5 mTorr Ar throughout the process. Diffusion barrier properties were examined by annealing the structure in vacuum at a base pressure less than $10^{-5}$ Torr over the temperature range 400 to 700 °C for 1 h. The film crystallinity and intermetallic phase formation were determined using a Philips APD 3720 X-ray diffractometer. The integrity of the stack films and chemical depth profile of Cu through the diffusion barrier were evaluated using a JEOL 2010F high resolution transmission electron microscope along with a JEOL Superprobe 733 energy-dispersive spectrometer. The surface morphology of the films was determined using JEOL 6400 scanning electron microscopy. For characterization of electrical properties, a four point probe was used to measure the sheet resistance of the Cu layer.

8.3 Results and Discussion

Figure 8-1 shows the X-ray diffraction patterns for as-deposited and annealed ZrN and Zr-Ge-N barrier stacks with the thickness of 50 nm. ZrN and Zr-Ge-N films deposited at room temperature were amorphous as evidenced by the lack of associated diffraction peaks in the X-ray diffraction patterns. This amorphous phase is a desirable microstructure for diffusion barrier applications and is also present in thicker ZrN and Zr-Ge-N films. After high temperature annealing of the barrier stacks, the crystallinity of Cu had increased as indicated by the stronger and sharper Cu (111) and Cu (200) peaks. The ZrN barrier stack remained intact upon annealing at 600 °C for 1h. Further annealing at higher temperature led to copper diffusion through the ZrN into Si and the formation of copper silicide [Fig. 8-1(a)]. Note that no ZrN diffraction peaks were evident at failure temperatures, possibly because the amount of barrier material was below the detection limit for XRD. Nevertheless, failure of the barrier upon annealing at temperature $> 600$ °C is consistent with undetectable amounts of recrystallization, as the formation of grain
boundaries would provide fast diffusion paths for Cu. In contrast, the diffraction pattern for the
Zr-Ge-N barrier stack remained unchanged upon annealing at 500 °C for 1h. [Fig. 8-1(b)]. After
600 °C annealing, however, noticeable copper silicide peaks appeared as a result of copper
diffusion, indicating barrier failure.

The surface morphology of the stack films was evaluated by scanning electron microscopy.
For Cu/ZrN/Si stack samples, the Cu grain structure was coarsened after higher temperature
annealing. There is no evidence of delamination or the presence of copper silicide crystallites
after annealing at 600 °C. In comparison, the surface morphology of Cu/Zr-Ge-N/Si stack
samples annealed at 500 and 600 °C is shown in Figure 8-2. Similar to the Cu films on ZrN, the
Cu films are continuous on the Zr-Ge-N barrier after annealing at 500 °C. Noticeable copper
silicide crystallites appeared after annealing at 600 °C: copper silicide was also evidenced by
XRD patterns. The lower failure temperature of Zr-Ge-N could be attributed to the reaction of
Cu with Ge, though there was no evidence of copper germanide within the detection limit for
XRD. The Ge concentration might exceed its solubility limit in the ZrN matrix and caused Ge
segregation in the films resulting in some changes in its structural properties [143]. Krusin et al.
[144] reported that Cu reacts readily with Ge to form a stable copper germanide c-Cu$_3$Ge phase
at low temperature. The failure mechanism of Zr-Ge-N films could be the formation of structural
defects as a result of reaction of Cu and segregated Ge at the Cu/Zr-Ge-N interface. These
defects could facilitate the diffusion of Cu into Si as well as the transport of Si across the barrier
to form copper silicide.

The interface integrity of the barrier stack was examined by cross-section transmission
electron microscopy (XTEM). Figure 8-3 shows the XTEM images of as-deposited and 600 °C
annealed ZrN barrier stacks. The interface integrity of the ZrN barrier before and after annealing
at 600 °C shows essentially no difference, consistent with the XRD data in which no copper silicide peak appeared. The ZrN layer is uniform in thickness and the interfaces of Cu/ZrN/Si are sharp and uniform after annealing, indicating that this system is thermally stable at 600 °C. Note that the texture of as-grown ZrN was amorphous and became nanocrystalline after annealing, which effectively blocks copper diffusion. In contrast, Cu diffusion is clearly seen in Zr-Ge-N films annealed at 600 °C as evidenced by the formation of Cu₃Si crystallites at the interface (Fig. 8-4(b)). The thick black layer on top of Cu is Pt, which functions as a protective layer when preparing XTEM samples via focused ion beam milling. The chemical depth profile (EDS) for the stack films before and after annealing was also examined. Figure 8-5 shows the Cu diffusion depth profile for a ZrN barrier stack before and after annealing at 600 °C for 1 h. Before annealing, the Cu signal declines sharply before the Si substrate can be detected. Similarly, after annealing, the Cu signal also returns to its baseline before reaching the ZrN/Si interface, although a small amount of Cu did penetrate into the ZrN layer. Nevertheless, the Cu signal was undetectable before the scan moved into the Si substrate, indicating no Cu diffusion into Si.

The sheet resistance of the Cu on the nitride barriers was measured via a standard four point probe as shown in Fig. 8-6. Before the barriers started to fail, the Cu sheet resistance decreased with heat treatment for both ZrN and Zr-Ge-N systems due to Cu grain growth. For the ZrN system, the sheet resistance of Cu increased rapidly upon annealing at 600 °C, indicating the onset of the failure process via formation of more resistive copper silicide. Likewise, the Cu sheet resistance on Zr-Ge-N system began to increase at 500 °C, also revealing the onset of barrier failure. The electrical behavior is thus consistent with the previously described microstructure changes.
8.4 Conclusions

In conclusion, the copper diffusion barrier properties of Zr-Ge-N on Si have been examined and compared to ZrN. A 50 nm thick Zr-Ge-N barrier was shown to prevent Cu diffusion at 500 °C for 1 h, as evidenced by the lack of copper silicide peaks in the X-ray diffraction patterns. The ZrN barrier film was more thermally stable as it prevented Cu diffusion at 600 °C for 1 h. SEM and TEM both showed the onset of formation of copper silicide crystallites for Zr-Ge-N barriers annealed at 500 °C. In contrast, XTEM on a ZrN barrier annealed at 600 °C revealed sharp interfaces and showed no intermetallic compound formation. The Cu atomic depth profile on XTEM sample indicated no interdiffusion across the ZrN barrier layer. Before barrier failure, the Cu sheet resistance for both systems decreased with increased anneal temperature due to Cu grain growth, followed by an increase due to the formation of more resistive copper silicide. Overall, the results showed that ZrN is a superior diffusion barrier as compared to Zr-Ge-N for copper metallization on Si.
Figure 8-1. X-ray diffraction patterns of as-deposited and annealed (a) Cu/ZrN(50 nm)/Si (001) for 1 h and (b) Cu/Zr-Ge-N(50 nm)/Si (001) for 1 h.
Figure 8-2. SEM images of Cu/Zr-Ge-N/Si stack (a) annealed at 500 °C and (b) annealed at 600 °C for 1 h.
Figure 8-3. Cross-section HRTEM images of Cu/ZrN(50 nm)/Si (001) (a) as-deposited and (b) annealed at 600 °C for 1 h.
Figure 8-4. Cross-section HRTEM images of Cu/Zr-Ge-N(50 nm)/Si (001) (a) as-deposited and (b) annealed at 600 °C for 1 h.
Figure 8-5. EDS depth profile of Cu/ZrN(50 nm)/Si for (a) as-deposited and (b) annealed at 600 °C for 1 h.
Figure 8-6. Sheet resistance of Cu vs. annealing temperature for Cu/ZrN/Si and Cu/Zr-Ge-N/Si.
CHAPTER 9
CONCLUSIONS

As the minimum trench size in silicon semiconductor backend process continues to scale down, the current Ta/TaN liner would eventually reach its scaling limit. The replacement for both leads to the development of new barrier materials. Noble metals are potential candidates due to their inert reaction with oxygen, given a template for direct copper electrodeposition without using a sputter deposited copper seed, thus simplifying the process.

As one of the noble metals, iridium is potentially attractive as a barrier material for it has a high melting point of 2446 °C and low resistivity of 4.71 μΩcm. In addition, its solid solubility in Cu and vice versa is low. As a diffusion barrier, 5 nm Ir thin films were shown to block Cu diffusion at 350 °C. The failure mechanism can be attributed to silicidation and grain boundary diffusion. In order to enhance the barrier performance, a bilayer approach by combining TaN was examined. The results showed that Ir (5nm)/TaN (5 nm) is an effective liner combination against Cu diffusion up to 600 °C after annealing for 1 h.

A similar approach of Pd (5nm)/TaN (5 nm) was also examined. In addition to providing a template for direct copper deposition, Pd can also serve as a catalyst for Cu electroless plating. In both cases, the superfilling of Cu in high aspect ratio trench can be realized. No copper silicide formation was observed after annealing at 550 °C for 1 h. The as-deposited thickness of Pd is 5 nm and uniform throughout the sample, after annealing, Pd diffused totally into Cu to form Cu-Pd solid solution. However, the EDS copper diffusion depth profile showed no diffusion of Cu into Si upon annealing at 550 °C for 1 h, indicating the effectiveness of this bilayer structure for preventing Cu diffusion.

The addition of Si and Ge into binary nitride matrix can increase the amorphorization tendency and raise the recrystallization temperature. Unfortunately, these nitrides become too
resistive to be useful as a liner for Cu interconnects. In contrast, the incorporation of B into WNₓ matrix yielded a low resistive W-B-N film. By reactively sputtering a W₂B target in N₂+Ar ambient, the low resistive and amorphous W-B-N films were realized. A low resistivity of 159.92 μΩcm for films as-deposited at 5 % N₂ flow ratio showed the best barrier performance.

The 10 nm W-B-N thin films deposited at 5 % N₂ flow ratio were shown to block Cu diffusion at 500 °C for 1 h, rendering a potential candidate as a diffusion barrier for future Cu metallization.

A comparative study of ZrN and Zr-Ge-N thin films deposited on Si was carried out to evaluate their barrier properties and performance. Deposited at room temperature, both films were amorphous. As the 50 nm ZrN thin film kept stable in contact with Cu upon annealing at 600 °C, the 50 nm Zr-Ge-N thin film failed as a barrier. The limited solid solubility of Ge in ZrN might cause the formation of microstructure defects upon annealing, which became the diffusion path for Cu. The formation of Cu₃Si crystallites were observed by both SEM and TEM. In contrast, the interface integrity of the ZrN barrier before and after annealing at 600 °C shows essentially no difference, consistent with the XRD data in which no copper silicide peak appeared. The results indicated that ZrN is a superior barrier as compared to Zr-Ge-N against Cu diffusion.
The binary alloy phase diagrams associated in this work, including copper-iridium phase diagram, copper-palladium phase diagram and palladium-silicon phase diagram were added for readers interested in detailed information regarding temperatures and compositions at which transition between different phases of these elements occur.

Figure A-1. Cu-Ir binary phase diagram.
Figure A-2. Cu-Pd binary phase diagram.
Figure A-3. Pd-Si binary phase diagram.
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142. *ASM Hand Books Online*, Volume 3, Alloy Phase Diagram


BIOGRAPHICAL SKETCH

Lii-Cherng Leu was born in a Christian family in Keelung, Taiwan. Since childhood, he continued getting involved in church activities. After finishing high school education in Taipei, the Lord brought him to Tainan, where he began his undergraduate study in Materials Science and Engineering in National Cheng-Kung University (NCKU). In those four years, the Lord opened Himself to him. And he was captured by the Lord with a group of crazy lovers of Jesus in the church life in Tainan, where he met his wife Linda.

In 1998, he continued his enthusiasm in materials science by attending the graduate school in National Tsing-Hua University (NTHU) in Hsin-Chu. Under Dr. Han-Chang Shih’s guidance, he worked on synthesis of magnetic multilayer thin films and received his master degree in 2000. Soon after his graduation, he went to military service to fulfill his citizen’s duty by joining Army. After 8 months military training, he was commissioned second lieutenant and served as a platoon leader in Army Tank. Beginning in May 2002, he worked as a process integration engineer in United Microelectronic Corporation (UMC), where he enjoyed his first experience working in the industry.

After leaving his first job, he went to the University of Florida for his doctoral degree in August 2004. Under Dr. David Norton’s guidance, he worked on developing epitaxial oxide buffer layer for high-temperature superconductor YBCO in the first two years. Afterwards, he studied on the diffusion barrier properties of several candidate materials for Cu interconnects. Some of the results have been published in three journal articles as a first author, and some are under review.