GROWTH AND CHARACTERIZATION OF NOVEL THIN FILMS ON GALLIUM-V SEMICONDUCTORS FOR ENHANCED FUNCTIONALITY

By

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2008
To my mother
ACKNOWLEDGMENTS

I want to give thanks to the Lord for blessing me with the opportunity, strength, and courage to pursue a Ph.D. During my graduate experience when it seemed like the responsibilities and stress was too overwhelming for my outward man, it was the Lord who renewed my inward man day by day. Dr. Abernathy deserves special recognition for welcoming me into her group and providing me with research direction and purpose. I want to acknowledge Andrew Herrero, Ryan Davies, Dr. Brent Gila, Dr. Kim Allums, Andrew Gerger, and Andrew Scheuerman for help with interpretation of experimental results, conducting the TEM work and most of the AFM characterization of my films. I would also like to give thanks to Dr. Pearton, Dr. Norton, Dr. Ren, and Dr. Hebard for serving on my supervisory committee.

Very few individuals have positively impacted my life as positively professionally and personally as Dr. Nigel Shepherd, currently an assistant professor at the University of North Texas. During my time in graduate school, he made the most significant contribution to my overall intellectual growth as we spent many evenings discussing science and politics. I would also like to thank Joseph Lee, who has been a friend I can rely on for good judgment, relentless encouragement, and therapeutic laughter.

Lastly, I want to give thanks to all of my family members. Their steadfast belief in my abilities to accomplish my goal was apparent in the endless financial support and personal sacrifice endured by them throughout my graduate studies. I want to acknowledge my father and my brother. My father deserves credit for providing my brother and me with an environment and a set of circumstances from which we could prosper. My brother has always provided me with a “blueprint” for success which enabled me to avoid potential pitfalls and setbacks. For this, I am eternally grateful. I want to give a very special thanks to my mother. My mother has inspired me to strive for greatness as she passed on individual gain to ensure that my brother and I had the
best chance at success in life. Her experiences have taught me that life measures perseverance,
perseverance builds character, and character embodies hope. She deserves all the credit for
nurturing my hopes and cultivating my dreams.
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By

Anthony D. Stewart

December 2008

Chair: Cammy Abernathy
Major: Materials Science & Engineering

Compound semiconductor-based devices form a critical component in high speed communications and radar technologies. Future advances in these areas will require integration of multiple functionalities and development of new capabilities. Such development can only occur if precise control of surface and interfacial properties can be achieved. This study represents an experimental study of control of two kinds of interfaces in Gallium-V semiconductors.

Gallium arsenide (GaAs) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices require the use of a gate dielectric to reduce leakage current, passivate surface traps, and provide electrical isolation between devices. A suitable gate dielectric material must satisfy two requirements: (1) the interface between the GaAs substrate and the gate dielectric must have a low interface state density \( (D_{it}) \) to prevent the Fermi level from being pinned; and (2) the gate dielectric must have a high breakdown field to allow a gate voltage to be established. Samarium oxide \((\text{Sm}_2\text{O}_3)\) and samarium gallium oxide \((\text{Sm}_x\text{Ga}_{1-x})_2\text{O}_3\) were investigated as dielectric materials for GaAs MOSFET technology. The growth conditions of were optimized to improve their structural and electrical properties.
Spintronics devices will seek to exploit the spin quantum state of the electron in an effort to sustain the innovation in microchip technology. With the ultimate goal of an electron-spin quantum computing machine becoming practical, a magnetic materials system with strong bonding and a Curie temperature ($T_C$) at or above room temperature (RT) compatible with existing semiconductor technology is a promising candidate. Manganese arsenide (MnAs) was investigated as a spin aligner injection on gallium nitride (GaN) substrates. The growth conditions were optimized to improve their structural and magnetic properties.

All films were deposited by molecular beam epitaxy (MBE) which allows for abrupt cessation and initiation of growth and the potential for in-situ monitoring of film growth. All films were characterized to determine film thickness, crystal structure, and surface roughness. Electrical diodes were fabricated with the Sm$_2$O$_3$/GaAs heterojunction to evaluate it electrically. The magnetic properties of MnAs/GaN were investigated using a Superconducting Quantum Interference Device (SQUID).

Samarium oxide (Sm$_2$O$_3$) and samarium gallium oxide (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ have been proposed as candidate dielectric materials for development of gallium arsenide (GaAs) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology. Growth of thin (20nm-50nm) samarium oxide and samarium gallium oxide layers on GaAs substrates via plasma-assisted molecular beam epitaxy (MBE) has been performed using a range of growth temperatures and samarium cell temperatures. X-ray photoelectron spectroscopy (XPS) of the deposited films showed evidence of residual Sm metal in the films which decreased with decreasing Sm cell temperature, but was relatively independent of substrate temperature. Stoichiometry of the oxide was found to be independent of substrate temperature, but increased in oxygen to metal ratio as the Sm cell temperature was decreased. Decreasing the Sm cell temperature also suppressed the
formation of the monoclinic phase and promoted the growth of the cubic phase. Films grown at higher (500°C) temperature showed the presence of a crystalline interface, but relatively high surface roughness and the presence of multiple crystalline phases. Current-voltage analysis of one hundred micron diameter MOS diodes showed breakdown fields at 1 mA/cm² of up to 4.35 MV/cm. Breakdown field was found to decrease with increasing Sm free metal content in the films. Post-growth annealing under an oxygen plasma in the MBE chamber of films grown at higher temperatures resulted in an increase in the oxygen to metal ratio but effected no change in the crystalline phase distribution. The effect of stoichiometry, phase distribution and microstructure on the interface state density and capacitance-voltage behavior of MOS diodes was also investigated. The effect of Ga incorporation on the electrical properties of the binary oxide was also investigated.

Growth of MnAs on GaN requires a high V/III ratio in the chamber during growth to suppress the formation of Mn-rich compounds. It appears that once a critical thickness is reached the MnAs phase nucleates with excellent crystal quality. $M_S$ and RMS values were markedly improved by increasing the MnAs (004) to Mn$_3$As (217) XRD peak ratio. These results indicate that the structural and magnetic properties of the MnAs/GaN system strongly depend on the V/III ratio in the chamber during growth. A saturation magnetization ($M_S$) as high as 276 emu/cm³ with a $T_C$ of 315K was achieved with MnAs growth at high V-III ratios.
CHAPTER 1
INTRODUCTION

Motivation

With the advent of MOSFET technology, research into dielectrics for semiconductors has risen dramatically. The Si-SiO$_2$ interface forms the basis for current MOSFET technology. A thermally stable, electrically insulating layer of SiO$_2$ with high breakdown electric field ($E_b \sim 10$ MV/cm) and low interface trap density ($D_{it} \sim 1 \times 10^{10}$/cm$^2$eV) readily forms on the Si surface by thermal oxidation. Due to the dimensional scaling requirements predicted by Moore’s Law, Si device technology will require increasingly thinner gate oxides capable of providing the requisite drain current response to a decreasing applied voltage. Eventually, fundamental limitations imposed by the physics and chemistry of the Si-SiO$_2$ interface will prevent further transistor miniaturization and require a new materials system to continue scaling trends predicted by Moore’s Law.

Silicon is an indirect band gap material which makes it an inefficient light emitter. Compared to GaAs, Si has a smaller band gap (1.1 eV) and an electron mobility (1500 cm$^2$/V-s) over 5x smaller. GaAs has a direct band gap material that makes it suitable for optical communications, solar cells, and photonic devices such as IR emitters. Its band gap (1.42 eV) and electron mobility (8500 cm$^2$/V-s) allow it to be used in high temperature and high frequency applications. The capability to produce devices in semi-insulating GaAs substrates provides greatly reduced parasitic capacitances, thus faster devices. Furthermore, it is ideally suited to integrated circuit fabrication because devices made in semi-insulating GaAs by direct ion implantation are self-isolating.

Despite of all the advantages GaAs has as a substrate material for MOSFET technology compared to Si, there is still an urgent need for a technology capable of forming insulating layers
on GaAs with dielectric and interface properties comparable to the Si-SiO\textsubscript{2} system. GaAs-based MOSFET technology is also complicated by the high number of GaAs surfaces states that can lead to a pinning of the Fermi level midgap which is incompatible with complementary MOS (c-MOS) technology. Alternative techniques for native oxide removal and surface passivation of GaAs as well as a deposition technique capable of forming insulating layers on GaAs with dielectric and interface properties comparable to the Si-SiO\textsubscript{2} system are essential for the continued development and realization of practical GaAs MOSFET devices.

Spin-based electronics, also known as spintronics, is another approach used to avoid the looming fundamental limitations of conventional Si-based electronics by seeking to exploit electron spin as well as charge. Spin injection, spin transport, and spin detection must be demonstrated at room temperature before a commercially viable spintronics device can be realized. One materials system used to manipulate spin-based currents is the creation of ferromagnet-semiconductor (FM/SC) heterostructures. Spin injection across heterostructural interfaces at cryogenic temperatures, let alone room temperature, remains challenging. The interface must be free of undesired phases which can act as magnetically dead layers. MnAs is an attractive candidate as a spin injection layer because of its RT-ferromagnetic properties. Current III-Nitride-based visible light emitting diodes represents part of a healthy technology base with which Mn-containing magnetic materials can be integrated. The crystallographic symmetry of MnAs and GaN (hexagonal crystal structure) should lead to the growth of films with good crystal quality resulting in atomic registry at the interface and possibly the growth of epitaxial, single crystal, ferromagnetic MnAs films. Indeed, the growth of a heterostructure with an abrupt interface is ideal for demonstrating spin injection across an interface.
Study Overview

The first objective of this study was to grow a gate dielectric with high breakdown voltage so that it could be used in an enhancement mode GaAs MOSFET. This study also included the optimization of the growth conditions and their effects on stoichiometry, phase distribution and microstructure. The $D_{it}$ value and capacitance-voltage behavior of MOS diodes was used to evaluate the relationship between growth conditions and interfacial quality. The second objective of this study was to grow a magnetic material with room temperature ferromagnetism that could be potentially integrated into a III-Nitride technology base. The growth conditions in this study were also optimized to produce films with high saturation magnetization and low surface roughness.

A brief introduction to MOSFETs and their basic operation was required for the basic understanding essential for investigating the properties of dielectrics. An extensive literature review of GaAs surface passivation techniques and dielectrics on GaAs was carried out to determine the state of the art. A literature review of spintronics devices and magnetic materials used to demonstrate spin injection across a heterointerface was conducted to determine the current state of research. Since the surface properties of the semiconductor will largely affect the properties of the deposited film, initial experiments focused on optimizing a substrate cleaning procedure for obtaining a clean GaAs and GaN surface. Next, the binary oxide, Sm$_2$O$_3$, was deposited at two substrate temperatures and then characterized structurally, morphologically, and electrically. Before beginning the fabrication of electrical diodes, the heterojunction band offset in the Sm$_2$O$_3$/GaAs system was measured by X-ray Photoelectron Spectroscopy (XPS) to determine if Sm$_2$O$_3$ would be useful as a dielectric for GaAs MOSFETs. Next, the ternary oxide, (Sm$_x$Ga$_{1-x}$)$_2$O$_3$, was deposited to investigate the effects of Ga incorporation. Optimization experiments were used to determine the effects of substrate temperature and samarium cell
temperature (i.e. growth rate) on film stochiometry, phase distribution, and microstructure in these films. Since all of the samarium based oxides (i.e. samarium oxide with and without gallium) used in this study were found to have unbonded Sm metal, annealing experiments were carried out in oxygen and forming gas to determine the effects of annealing on film stochiometry. Lastly, the optimal growth conditions for deposition of MnAs on GaN were arrived at through a series of growth runs involving different arsenic sources. In conclusion, recommendations for future work were established for the MnAs/GaN system based on the results of various characterization techniques. A comparison of electrical data for all of the oxide films was investigated and some conclusions and recommendations for future work were determined.
CHAPTER 2
BACKGROUND AND LITERATURE REVIEW

Introduction to MOSFET

The MOSFET is a three terminal device which uses a metal gate to control a conducting channel that electrons or holes (depending on the type of conducting channel) can flow through from a metal source to a metal drain. The two types of MOSFET devices are depletion mode ("normally on") and enhancement mode ("normally off"). In the depletion mode MOSFET, the semiconductor material beneath the oxide is doped with the same type of material as the source and drain regions. A conducting channel is already present at a gate voltage of zero, so a gate voltage must be applied to turn the device off. In the enhancement mode (e-mode) MOSFET, the semiconductor material beneath the oxide is lightly doped to create a region of opposite type to the material under the source and drain regions. A conducting channel is not present at gate voltage zero, so a gate voltage must be applied to create a conducting channel and turn the device on. The e-mode MOSFET is most commonly used as a switch. An e-mode n-channel device will be used for further description regarding the basic operation of a MOSFET.

Basic Operation of e-Mode n-Channel MOSFET Device

An e-mode n-channel device has n+ source and drain regions that have been implanted or diffused into a lightly doped p-type substrate. At a gate voltage of zero, there is no conducting n-channel between the n+ regions, so no current can flow from the drain to the source. At equilibrium, the Fermi level is flat and a potential barrier is present that prevents the flow of electrons from the source to the drain. As a positive bias is applied to the gate, the valence band moves away from the Fermi level and a depletion region begins to form as holes underneath the gate oxide are repelled. A corresponding negative charge (ionized acceptors) is induced in the p-type channel, and the barrier for electrons between the source, channel, and drain is reduced.
Further reduction of the barrier will lead to the formation of a channel in which electrons flow from the source to the drain. The minimum gate voltage required to induce this channel is known as the threshold voltage ($V_T$). Increasing the gate voltage beyond the threshold voltage will induce more negative charges in the channel as minority carrier electrons generated in the bulk will drift across the depletion layer to the surface layer (inversion layer) of charge.

Applying a drain bias initially increases the drain current linearly. However, as more drain current flows in the channel, more ohmic voltage drop occurs along the channel, and eventually a drain bias is reached that causes the conducting channel to pinch-off and the drain current to saturate. Pinch-off will occur when the difference between the gate voltage and drain bias is equal to the threshold voltage. Increasing the drain bias further will move the pinch-off point farther into the channel and closer to the source end\textsuperscript{1}.

The Two-Terminal MOS capacitor

The phenomenal success of the MOS transistor has been driven by the dimensional scaling of the MOS transistor and the stability and reproducibility of the Si-SiO\textsubscript{2} interface. The latter has led to an extensive research effort of the two-terminal MOS structure often referred to as a “MOS capacitor”. The MOS capacitor is a two terminal device that uses a metal gate to determine the number of carriers available for conduction at the surface of the semiconductor substrate. Detailed studies conducted with the three-layer structure has led to the development of better fabrication methods which have greatly reduce the undesirable effects that plagued earlier work.

The Ideal and Real MOS Capacitor

The ideal MOS capacitor has a flatband condition where the energy difference between the metal work function ($\Phi_m$) and semiconductor work function ($\Phi_s$) is zero at an
applied bias of zero. Under an applied bias, three distinct operation modes exist which are known as accumulation, depletion, and inversion. In accumulation, majority carriers accumulate at the surface of the semiconductor, forming a larger carrier concentration than the doping concentration in the bulk of the semiconductor. For a p-type semiconductor, the valence and conduction bands will bend up, and for an n-type semiconductor, the bands will bend down. In both cases, the intrinsic Fermi level ($E_i$) is farther away from the Fermi level ($E_F$) of the semiconductor. In depletion, majority carriers are depleted near the semiconductor surface. The bands will bend down in p-type material and will bend up in n-type material, with the bands bending far enough for $E_i$ to equal $E_F$ at the surface. Under inversion, the bands bend down strongly enough in the p-type material so that $E_i$ lies below $E_F$ at the surface, and the bands bend up strongly enough in the n-type material so that $E_i$ lies above $E_F$ at the surface. Majority carriers at the surface of the semiconductor have been further depleted and minority carriers are collected at the surface\textsuperscript{2,3}.

**Gate Dielectric Properties**

For a material to be an effective dielectric, it needs to possess the following characteristics: chemical and thermal stability, a dielectric constant higher than the semiconductor, a wide band gap with confinement at both edges, and a lattice constant and thermal expansion coefficient close to that of the underlying substrate. Large differences in the lattice constants can create defects such as misfit dislocations in the underlying substrate that can serve as trapping centers. If the growth occurs at high temperatures, large differences in the thermal expansion coefficients can produce stress at the interface during cooling that will relieve itself through the formation and propagation of dislocations. High operating temperatures with wide band gap semiconductor devices makes thermal stability an absolute necessity for the dielectric. In addition to needing a larger band gap than the semiconductor, large valence band and conduction band offsets with
respect to the semiconductor are highly desirable. A higher dielectric constant than the semiconductor is needed to prevent the formation of a high electric field in the dielectric that can lead to potential breakdown of the dielectric.

Effectiveness of the dielectric can also be determined through analysis of the charges at the dielectric/semiconductor interface and in the dielectric itself. Positive or negative charges trapped at the dielectric/semiconductor interface are known as interface trapped charge (or interface state density). The trapped charge is due to structural defects (i.e. dislocations), dangling bonds, and impurities. The $D_{it}$ should have a value less than or equal to $10^{11}$ eV$^{-1}$cm$^{-2}$ for a device to be successful. Charges trapped in the first 2-3 monolayers of the dielectric due primarily to structural defects are known as fixed dielectric charge ($Q_f$). Positive or negative charges in the bulk of the dielectric due to trapped holes or electrons are dielectric trapped charge ($Q_{ot}$). These charges can be injected into the dielectric from the gate or semiconductor under large gate biases. Mobile dielectric charge ($Q_m$) is attributed to ionic impurities that can drift under an applied electric field. It is critical to minimize the amount of charge in the insulator as trapped or mobile charges can cause shorting and effect the depletion of a semiconductor$^3$.

The integrity of the oxide can be determined from current-voltage measurements by calculating the breakdown field of the oxide. The breakdown field (in MV/cm) provides a measure of how much gate voltage can be applied before the oxide breaks down and charges flow freely from the gate to the semiconductor. It is extremely important to limit the number of defects (such as dislocations and pinholes) and charges in the dielectric as they can serve as electrical pathways that can lead to premature breakdown.
Oxide charge is also an important parameter for devices. Oxide charge can alter the threshold voltage of a MOSFET, alter the surface potential of the semiconductor, and alter common emitter current gain at low collector current in a bipolar transistor. Fixed oxide charge can be measured from the capacitance versus voltage (C-V) curves of an MOS capacitor. The simplest and most widely used method for measuring oxide charge density is to infer this density from the voltage shift of the depletion-to-weak inversion portion of the C-V curve (discussed in more detail in APPENDIX A).

**GaAs Surface Passivation**

Preparation of a clean crystalline semiconductor surface under vacuum conditions remains to be one of the most challenging issues in III-V semiconductor technology. A semiconductor surface exposed to air is covered with native oxides which have to be removed in vacuum or in an inert atmosphere before any epitaxial overgrowth can occur. After native oxide removal, a passivation process is used to provide stability against further chemical modification of the surface and better control of the electronic properties (unpinning of the Fermi level and reduced surface recombination). One of the major drawbacks of the III-V semiconductors particularly GaAs has been the high number of surface state defects, and the technological inability to reduce them. A number of passivation techniques both wet and dry have been investigated yet the search for a highly reproducible simple technique for GaAs passivation remains to be urgent.

**Thermal Cleaning of GaAs**

Thermal desorption of surface oxides is perhaps the simplest technique used to obtain a clean semiconductor surface in vacuum. However, careful attention must be paid to surface roughening during oxide removal, as many fabrication processes require smooth, high-quality surfaces for the growth of 3D structures such as quantum dots. Thermal cleaning of GaAs is generally performed by heating the substrate above 580ºC under a group V overpressure. The
GaAs-oxide layer decomposition occurs in a multiple-step process. First the As$_2$O$_5$ is removed by forming volatile AsH$_3$. Then, the decomposition of the gallium oxide layer, which comes off above 580ºC, requires the reduction of the relatively stable Ga$_2$O$_3$ to the more volatile Ga$_2$O. Problems with this technique for GaAs are the high processing temperature around 600ºC which can result in the excessive desorption of arsenic and significant surface roughening$^{4,5}$. Optimal thermal cleaning conditions for GaAs require the use of an arsenic source such as arsine (AH$_3$) or tris(dimethylamino)-arsenic (TDMAA) to obtain a smooth (< 0.2 nm) GaAs surface$^{6,7}$. A model assuming that the oxide layer is removed by void formation and the desorption rate is proportional to the area of void formation has been suggested. This model predicts the GaAs surface inevitably becomes rough after thermal removal of oxides, because the GaAs surface exposed earlier to vacuum through void openings loses more GaAs from the substrate through the As$_2$/As$_4$ desorption and Ga migration to the void perimeter$^8$.

**Sulfur Passivation**

Despite the focus of intensive research efforts for nearly 30 years, the surface chemistry of GaAs after the sulfide treatment remains to be controversial due to a lack of consistency in the experimental results reported in the literature. These inconsistencies in the outcome of the sulfidation of GaAs are reflected in a spread of results in terms of the identification of sulfur bonds to GaAs and the position of the Fermi level within the band gap. A number of sulfide surface treatments involving the immersion of the GaAs wafer in Na$_2$S, (NH$_4$)$_2$S, (NH$_4$)$_2$S, and S$_2$Cl$_2$ solutions under specific conditions have been employed. It is believed that sulfidation of GaAs relies on the elemental forms of Ga and As binding with S to produce Ga-S and As-S bonds which are responsible for the passivation effects of GaAs$^{9,10,11}$ Prior to the sulfur treatment, the GaAs wafer is etched to expose a pristine GaAs surface for which S can strongly bond. These wet techniques have proven to be successful at reducing surface state densities, but
issues with long term stability and reproducibility have resulted in some variation in the interpretation of experimental results. These problems are rooted in the absence of a clear explanation of the chemical processes occurring at the GaAs surface and the mechanism for the changes of electrical properties.

**Atomic Hydrogen**

The need for a dry vacuum technique capable of removing surface oxides at relatively low temperatures has fueled interest in the interaction of atomic hydrogen (AH) with GaAs surfaces. Several AH sources have been employed to generate a flux of atomic hydrogen in vacuum among them are the dissociation of H$_2$ via a hot filament, radio-frequency (rf) plasma discharge, or electron cyclotron resonance. Ideally, the source should provide a high-purity flux of atoms free of high-energy species which would damage the surface. The efficacy of the hydrogen source is directly related to the efficiency of that source to produce AH which reduces GaAs native oxides. Compared to conventional thermal cleaning which requires temperatures in the vicinity of 600ºC, the oxide desorption temperature (between 350ºC-400ºC) is significantly lower in AH cleaning with ECR, an rf discharge plasma, or dissociation of H$_2$ via a hot filament. This substantial reduction in the oxide desorption temperature is particularly beneficial in light of the surface roughening issues associated with conventional thermal cleaning. However, the problem of atomic hydrogen diffusion into bulk GaAs at 200ºC can be problematic in controlling the electronic properties of the surface. In this study, AH was supplied to the GaAs surface by two methods. In the first approach, molecular hydrogen was thermally dissociated on a resistively heated coiled tungsten filament placed at a normal angle to the sample at a distance of 5 cm. AH was generated by passing molecular hydrogen through a tungsten capillary in the second approach. The AH doser was kept about 3 cm away from the sample at 50º normal to the sample surface. The cracking efficiency was estimated to be 10%.
and unity, respectively. It was determined that an AH induced slow decomposition of GaAs occurs after around 700L (Langmuirs) of AH dose even at RT and can result in the pinning of the Fermi level which is associated with an increase in surface states. However, this process occurs very slowly due to the amount of AH dose needed to observe these characteristic changes in the electrical properties.

**Dielectrics on GaAs**

A suitable gate dielectric for GaAs MOSFET technology must have two critical properties. (1) The interface between the III-V surface and the oxide must have a low \( D_{it} \) to prevent the Fermi level from being pinned. (2) The oxide should have a high breakdown field to allow a gate voltage to be established. For nearly four decades, an enormous research effort has been expended to form insulators on GaAs with good dielectric and interface properties suitable for MOSFET applications.

**Gallium Oxide**

As mentioned previously, thermal oxidation of the GaAs surface induces complicated arsenic and gallium oxides at the surface which leads to a large \( D_{it} \) around midgap. For nearly four decades, an enormous research effort has been expended trying to reduce the \( D_{it} \) at the \( \text{Ga}_2\text{O}_3\)-GaAs interface. Prior to the widespread use of MBE, GaAs MOS structures were primarily grown using a thermal oxidation process or an anodic oxidation process. Thermal oxidation of GaAs was undertaken in a simple tube furnace through which pure oxygen gas flowed in a conventional manner yielded oxide films with a microcrystalline nature. Electron diffraction images showed that the film consisted of only \( \beta\)-\( \text{Ga}_2\text{O}_3 \), the most common form of gallium oxide. In this study, an oxidized and unoxidized were simultaneously heated to 950°C in an argon atmosphere overnight. Both samples were reduced to a gallium droplet suggesting the outdiffusion of arsenic in the oxidized sample possibly along the grain boundaries of the
microcrystalline oxide. Therefore, thermal oxidation of GaAs produces films which are not suitable for oxide masking, a key technique in MOSFET device technology. It was believed that the poor electrical properties were due to the chemical composition lacking arsenic trioxide. Based on these considerations native oxide films grown under controlled vapor pressure of As$_2$O$_3$ was proposed$^{34}$. A combination of auger electron spectroscopy (AES) measurements and electron beam diffraction patterns confirmed that the dominant constituents of films grown in arsenic trioxide vapor are represented by a quasibinary solid system As$_2$O$_3$-$\beta$-Ga$_2$O$_3$. The electrical properties of these films were characterized in terms of their breakdown field and leakage current. A breakdown field strength of 5-7 x $10^6$ V/cm and a leakage current density of 1 x $10^{-8}$ A/cm$^2$ per 1000 Å thickness at an applied voltage of 10 V was reported. As compared to thermal oxidation of GaAs in a tube furnace under pure oxygen, oxide films grown under controlled vapor pressure of arsenic trioxide showed significant improvements in terms of their electrical properties. Films grown by this method were found to have incorporated crystalline and amorphous allotropes of arsenic with the amorphous form being found closest to the GaAs substrate. Mobile charge contamination is undesirable from an electrical standpoint as the incorporation of metallic species during growth can adversely affect the insulating properties of the oxide. Comparable results have been achieved with anodizing of GaAs. One approach uses an electrolyte composed of a polyhydric alcohol such as ethylene glycol or propylene glycol, a weak carboxylic acid such as tartaric acid or citric acid, and water was used to produce glassy uniform native oxides with thickness depending linearly on the voltage applied across the formed oxide$^{35}$. Electrical characteristics were reported in terms of breakdown field strength of 4-5 x $10^6$ V/cm and a leakage current density of $10^{-11}$ - $10^{-9}$ A/cm$^2$. However, the very high $D_{it}$ value of $10^{12}$-$10^{13}$ cm$^{-2}$eV$^{-1}$ reported in this system limits its usefulness as a gate dielectric for MOSFET.
applications. Plasma or dry anodizing\textsuperscript{36} was found to decrease the number of surface states at the oxide-GaAs interface but there is still no clear consensus on the growth mechanism of the oxide.

**Gallium Gadolinium Garnet (GGG)**

$\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$ films were deposited by electron-beam evaporation of a single crystal $\text{Gd}_3\text{Ga}_5\text{O}_{12}$ source\textsuperscript{37,38} (also known as GGG Gadolinium Gallium Garnet) under ultrahigh vacuum conditions for gate dielectrics on GaAs. Subsequent to the growth of thick 1.5 $\mu$m n- ($1.6 \times 10^{16}\text{cm}^{-3}$) or p-type ($4.4 \times 10^{16}\text{cm}^{-3}$) GaAs layers on heavily Si or Zn doped GaAs substrates, the wafers with As stabilized (2x4) surfaces were transferred under vacuum of $6 \times 10^{-11}$ Torr from the III-V solid source molecular beam epitaxy chamber (background pressure of $2 \times 10^{-11}$ Torr) to another chamber (background pressure of $1 \times 10^{-11}$ Torr) for oxide deposition. Thus, no surface contamination or oxidation was incurred. The $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$ films were deposited at substrate temperature below 600$^\circ$C. Depositions at temperatures $>600^\circ$C yielded films of poor electrical properties due to chemical reaction with the GaAs substrate. Following oxide deposition, MOS capacitors were fabricated using a standard shadow mask process. A $D_\text{f}$ value in the low $10^{10}\text{cm}^{-2}\text{eV}^{-1}$ range was reported for this heterostructure and the C-V measurements showed evidence of accumulation and inversion, the basic requirements for MOSFET technology\textsuperscript{39}. The films were found to have a nonuniform Gd concentration characterized by an essentially Gd free interfacial region and a peak in Gd concentration at the oxide surface confirmed by x-ray photoelectron spectroscopy. It should be pointed out here that the deposition of $\text{Ga}_2\text{O}_3$ by electron beam evaporation was carried out using a $\text{Gd}_3\text{Ga}_5\text{O}_{12}$ target because there was no single crystal of $\text{Ga}_2\text{O}_3$ available. The $\text{Gd}_3\text{Ga}_5\text{O}_{12}$ source material is composed of $\text{Ga}_2\text{O}_3$ which volatizes at 2000K and $\text{Gd}_2\text{O}_3$ which has a boiling point of 4000K. If the deposition temperature is kept low, films are composed primarily of $\text{Ga}_2\text{O}_3$, with $\text{Gd}_2\text{O}_3$ as a minor phase.
The nonuniform Gd concentration was found to have a significant effect on the \( D_{it} \) value which was found to increase at a distance of 2 nm away from the interface. Oxides grown on air-exposed GaAs epilayers were found to have an interface trap density in the upper \( 10^{10} \text{cm}^{-2}\text{eV}^{-1} \) range. The substrate temperature was 480ºC. In this “ex-situ” process, after the deposition of thick 1.5 µm n-type \((1.6 \times 10^{16} \text{cm}^{-3})\) GaAs epilayers on heavily Si doped \((2 \times 10^{18} \text{cm}^{-3})\) GaAs substrates the wafers were removed from the MBE chamber, exposed to air for three days, and then placed into another chamber for oxide deposition. No surface reconstruction and discontinuous reflective high energy electron diffraction (RHEED) (discussed in Chapter 3) streaks were observed on the “ex-situ” GaAs. The discontinuous streaks suggest the surface has been contaminated with carbon and/or oxygen. As compared to the “in-situ” process, the increase of \( D_{it} \) can be attributed to oxidation which occurred as a result of air exposure.

**Silicon Dioxide**

Silicon dioxide (SiO\(_2\)) films have been deposited on GaAs substrates by an electron beam evaporation method of a single crystal of SiO\(_2\), plasma enhanced chemical vapor deposition (PECVD), photo-chemical vapor deposition (photo-CVD), and a liquid phase deposition (LPD) technique. It was shown that silicon dioxide films with low interface trap density deposited by electron beam evaporation on GaAs cannot be easily obtained. Silicon dioxide films were amorphous for substrate temperatures from RT to 500ºC as observed from TEM and RHEED studies. The SiO\(_2\)-GaAs interface was shown to be intrinsically pinned at the midgap, as demonstrated by PL and C-V measurements. Silicon dioxide films deposited by PECVD have also shown limited success as a dielectric for GaAs. In this study, the GaAs surface was exposed to a hydrogen sulfide plasma for 20 minutes at RT prior to oxide deposition. This RT hydrogen sulfide plasma treatment yields a thin sulfide layer at the interface. Three possible explanations were proposed for the high \( D_{it} \) value obtained for this heterostructure: (1)
Reoxidation of the surface from reactive oxygen from the SiO₂ film, (2) charge trapping in sulfide compounds at the interface, or (3) SiO₂ defects produced by initial reactions with the sulfide layer⁴¹. SiO₂ films deposited by photo-CVD using a deuterium lamp as an excitation source were found to have a $D_\mu$ value of $6.5 \times 10^{11} \text{cm}^{-2}\text{eV}^{-1}$ for the as-deposited native oxide with a breakdown field of 11 MV/cm⁴². The high breakdown field indicates the good crystal quality of the film deposited with this technique; however, the relatively high $D_\mu$ value needs to be reduced for GaAs MOSFET technology. A breakdown field of approximately 7.6 MV/cm was reported for SiO₂ films deposited by the LPD technique⁴³. The electrical properties of LPD-SiO₂ were attributed to the suppression of interdiffusion due to a low processing temperature of 40°C.

**Magnesium Oxide**

Magnesium oxide films (MgO) have been deposited by electron beam deposition on p-GaAs substrates for gate dielectrics. The films were deposited in the range of 200°C between 500°C. Films grown below 250°C had stochiometry problems while films grown above 450°C had significant interdiffusion problems. MgO films deposited at 300°C showed no significant interdiffusion problems with abrupt interfaces. Current-voltage (I-V) and C-V measurements showed MIS behavior of Al/MgO/p-GaAs diodes with a $D_\mu$ value of $1.9 \times 10^{11} \text{eV}^{-1}\text{cm}^{-2}$ and a dielectric constant of 9.06⁴⁴. MgO films have also been deposited by magnetron sputtering on GaAs⁴⁵. In this study, a nucleation mechanism is proposed for the growth of epitaxial MgO on GaAs. Based on the results of Electron Energy Loss Spectra (EELS) and TEM-Energy Dispersive Spectra (TEM-EDS), it was concluded that the native oxide of GaAs volatilized, exposing bare GaAs at pinholes where MgO nucleation can occur. High Resolution Transmission Electron Microscopy (HR-TEM) revealed a composition characterized by excess Ga with respect to stoichiometric GaAs and excess O with respect to stoichiometric MgO. The
presence of excess Ga with respect to GaAs suggests partial volatilization of the native oxide prior to the nucleation of the MgO film, since the oxides of arsenic have higher vapor pressures than the oxides of gallium. Pulsed laser deposition has also been used to deposit MgO on Sb-passivated GaAs. It was previously shown that Sb passivation provides a smooth reconstructed GaAs surface suitable for the growth of epitaxial MgO films with no large-scale interfacial layer. A clockwise hysteresis with a voltage shift of 0.8 V in the C-V curves indicated a trap of density of $7 \times 10^{-11} \text{cm}^{-2}$. In this study, two sets of samples were grown to investigate the effects of residual Sb on the structural and electronic properties of the MgO/GaAs heterostructures. The first set of samples was grown at 380°C five minutes after the appearance of the (1x3) reconstructed RHEED pattern. For the second set of samples, the substrate was heated to 500°C until the (2x4) reconstructed pattern was observed, held at 500°C for five minutes and then rapidly cooled to 380°C for MgO growth. AES measurements confirmed that residual Sb is present at the interface of epitaxial MgO films grown on Sb-passivated GaAs at substrate temperatures between 350°C and 400°C. XPS measurements indicated that the Sb coverage was reduced by a factor of 3.6 during heating from 350°C to 500°C. It was concluded that Sb desorption is necessary to produce a uniform interface and residual Sb at the interface results in increased frequency dispersion in the C-V characteristics, as commonly observed with dielectrics on GaAs.

**Introduction to Spintronic Devices**

Spin-based electronics seek to exploit the spin of an electron for information storage and processing in an effort to further increase IC packing density and switching speed as well as reduce power consumption. One approach to manipulating spin-based currents is the creation of the Dilute Magnetic Semiconductors (DMS). A second approach to manipulating spin-based currents is the creation of ferromagnet-semiconductor (FM/SC) heterostructures. Fe with a $T_C$ of
1043 K has been deposited by MBE on (7 x 7) reconstructed Si(001) and (2 x 1) reconstructed Si(111) but were unsuccessful due to reactive interfaces RT\textsuperscript{48}. Thin films of Fe have been deposited by MBE on GaAs(001) substrates resulting in the absence of magnetic signature at RT due to the formation of a “magnetically” dead layer in the range of the first few monolayers\textsuperscript{49}. By contrast, Fe growth on molecular-beam epitaxy-prepared GaAs(001)-c(2x4) and c(4x4) surfaces result in a relatively abrupt interface with good magnetic properties, suppression of midgap states, and does not pin the Fermi energy (E\textsubscript{F})\textsuperscript{50,51,52}. However, there is concern that mismatches in the E\textsubscript{F} at the interface may preclude efficient spin injection. Alternatively, manganese arsenide (MnAs) which also exhibits RT-ferromagnetism (T\textsubscript{C} = 318K)\textsuperscript{53} has been deposited on GaAs(111) and GaAs(001) oriented surfaces resulting in epitaxial ferromagnetic MnAs layers with promising magnetic properties\textsuperscript{54,55,56}. However, the coexistence of hexagonal ferromagnetic α-MnAs phase and paramagnetic β-MnAs phase which have been stabilized by residual strain\textsuperscript{57,58} has been reported in the literature. This phase coexistence can be attributed to a large lattice mismatch (7.36\%) and a ferromagnetic-paramagnetic transition (at approximately 40°C) during sample cooling from the growth temperature which is accompanied by a (1\%)\textsuperscript{59} change of the lattice parameters. Growth of MnAs on GaAs is complicated by the differences in crystal structure (hexagonal vs. cubic) and by the large lattice mismatch. By contrast, the crystallographic symmetry of MnAs and GaN (hexagonal crystal structure) should lead to improved crystal quality resulting in atomic registry at the interface and possibly the growth of epitaxial, single crystal, ferromagnetic MnAs films.

**Dilute Magnetic Semiconductors**

Dilute Magnetic Semiconductors are semiconductor materials which a have been doped with magnetic ions. The magnetic dopants provide spin magnetic moment associated with the
electron spin. Most notable among this group are GaMnN and InMnN which are predicted to have \( T_c \)’s in excess of 400 and 300 K, respectively. Indeed recent reports have reported epitaxial growth of single phase GaMnN with RT ferromagnetism. However, a fraction (1-36\%) of the total Mn concentration depending on growth conditions could be present as small Mn clusters according to EXAFS measurements. The highest degree of ordering per Mn atom was found for a Mn concentration of 3 atomic percent.

A ZnMnSe/AlGaAs-GaAs spin-polarized LED has been reported. Grown in a dedicated III-V MBE machine, the spin-LED uses the DMS material, n-Zn\(_{0.94}\)Mn\(_{0.06}\)Se, as a spin aligner layer and as a contact to an III-V based LED structure. The III-V structure consists of a 15 nm-thick GaAs QW sandwiched by 50 nm-thick p-doped and n-doped AlGaAs barrier layers on both sides. In this device, spin polarized electrons are injected from the ZnMnSe into the GaAs QW, where radiative recombination of the carriers with unpolarized holes results in the emission of circularly polarized light. These devices are impractical because ZnMnSe is a paramagnetic material and requires a magnetic field to align the spins before spin injection occurs. Furthermore, it has been shown that stacking faults nucleating near the ZnMnSe/AlGaAs interface enhance the spin-flip scattering in this material.

Spin alignment and injection has been reported in ZnMnSe/ZnCdSe quantum structures. The investigated structures consisted of a thin ZnMnSe spin aligner layer and a nonmagnetic 7 nm-thick ZnCdSe QW as a detector for spin injection by monitoring spin-dependent excitonic recombination. A nonmagnetic ZnSe spacer layer (4-10 nm-thick) was inserted between the spin aligner layer and the QW to provide a tunneling barrier. The excitation mechanism of the spin-polarized carriers in this device is optical. In the case of optical spin injection, spin polarization can be created by either circularly polarized optical pumping in a nonmagnetic semiconductor or
by unpolarized optical excitation of a DMS followed by fast spin relaxation to its preferred spin orientation. Spin injection efficiency is rather limited (i.e., typically less than 30%) in this system. Determination of an explanation for the low efficiency has proven to be nontrivial due to the complicated nature of spin and momentum relaxation during optical pumping by high energy photons well above the band gap of both materials.

**Ferromagnetic Metals**

The use of Fe films, grown by MBE on GaAs, to polarize spins of electrons injected into the GaAs has also been reported. These reports were important because theoretical work predicted that spin injection from any metal into a SC should almost be impossible in the diffusive ohmic regime. The LED device structure consists of p-GaAs (001) substrate with 500 nm-thick p+-GaAs buffer layer. The active region consists of two 4 nm-thick In_{0.2}Ga_{0.8}As QWs separated by 10 nm-thick GaAs barrier layers and sandwiched by two 50 nm-thick undoped GaAs spacer layers. The spin injection layer was the ferromagnetic metal, Fe. The circular polarization degree of the emitted light reveals a spin polarization for recombining electrons of about 2% at room temperature. Theoretical predictions limited the spin injection efficiency to less than 0.1% due to the resistance mismatch. The discrepancy has been attributed to Schottky-type contacts, which give rise to tunneling under appropriate bias conditions. It has been reported that a tunneling process can lead to enhanced spin injection efficiency since it is not affected by the resistance mismatch. Indeed experimental evidence to support this has been reported by STM. However, the formation of a magnetically dead layer at the Fe/GaAs interface due to Fe and As interdiffusion has been identified as an obstacle for spin injection in these structures. Spin injection efficiencies of 13% have been reported at 5K across the Fe/GaAs (001) interface, 6% across a Fe/Al_{x}Ga_{1-x}As/GaAs interface at 295K, and 32% at RT for CoFe/MgO injectors grown on p-GaAs (100).
MnAs

MnAs is ferromagnetic below 40°C\textsuperscript{72}. Above 40°C\textsuperscript{72}, in magnetic zero field, the material undergoes a phase transition from the ferromagnetic NiAs hexagonal crystal structure to the paramagnetic MnP orthorhombic crystal structure. The phase transition at 40°C\textsuperscript{72} which is accompanied by some loss in ferromagnetic ordering has been described with an exchange striction model assuming a strongly volume-dependent exchange energy. At about 125°C\textsuperscript{72}, another phase transition occurs resulting in the paramagnetic NiAs hexagonal crystal structure. MnAs like other transition metal pnictides exhibits metallic condition. Conduction is by 3\textit{d} electrons. A band scheme which is based on a molecular orbital approach has been proposed. Mn and As \textit{s} and \textit{p} states form bonding and antibonding \textit{sp} bands\textsuperscript{72}. The bonding band is completely filled and the antibonding band is completely empty. In the gap between these \textit{sp} bands, partially filled Mn \textit{d} orbitals overlap to an extent sufficient to form narrow bands. The peculiar nature of the band structure in this material has led some to characterize MnAs as semimetallic\textsuperscript{72}. These bands have energies about the Fermi energy, thereby giving rise to the metallic conduction band. Mutual repulsions between these bands could cause some bands to rise above and below the Fermi energy, thereby creating a gap with semiconductor behavior. The zinc-blende phase of MnAs has been predicted to be a nearly half-metallic ferromagnet making it an ideal materials system for spintronic applications. Occupancy and width of these \textit{d} bands are strongly influenced by the crystal field, i.e. crystal symmetry and crystal dimensions. Half-metallic ferromagnetism (100\% spin polarization) in the NiAs or related MnP structure of MnAs, if realized, deserves to be studied as these materials can serve as models for future systems. It is well known that transition metal compounds with the NiAs-type crystal structure exhibit a mixture of ionic, covalent, and metallic bonds. Therefore, in MnAs, conduction by Mn \textit{d} states not only is determined by the crystal field but also by the amount of orbital overlap\textsuperscript{72,73}.
MnAs has been deposited on GaAs by MBE with promising results. The magnetic properties of this heterostructure have been characterized by a phase coexistence of the ferromagnetic $\alpha$ and paramagnetic $\beta$ MnAs phases and have been found to depend on the substrate orientation. The impact of different strain states was investigated by characterizing the spatial distribution of these two phases between the isotropically strained MnAs/GaAs(111) and the anisotropically strained MnAs/GaAs(100). The $M_S$ was found to strongly depend on the epitaxial orientation of the substrate and can be improved with post-growth annealing under an As overpressure.
CHAPTER 3
EXPERIMENTAL APPROACH

Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) was used to deposit all films. MBE uses localized beams of atoms or molecules in an ultra-high vacuum environment (UHV) to provide a source of the constituents to the growing surface of a substrate crystal. The beams impinge on the substrate crystal kept at a moderately elevated temperature that provides sufficient thermal energy to the arriving atoms for them to migrate over the surface to lattice sites. The vacuum environment surrounding the growing crystal must be kept as low as possible to avoid contamination that might adversely affect electrical properties, film morphology, and film stoichiometry. These purity constraints required for MBE growth are achieved by the use of liquid nitrogen (LN$_2$) chilled walls surrounding the source ovens and the substrate. The cold chamber walls ensures that the beam flux makes a single pass through the chamber before condensing on the chamber walls, thus keeping the background pressure low in the system. The low background pressure also allows the use of a RHEED system to operate without corrosive damage from residual gases. The advantage of RHEED is that it allows the system to operate while the substrate is exposed to the molecular beams, thus generating a “real time” surface analysis in terms of the growth mechanism, film morphology, and thickness. Other advantages of the MBE include precise thickness control, film stoichiometry, and the ability to rapidly turn beams on and off enabling the growth of atomically abrupt interfaces.

A Riber 2300 MBE system was used for all the oxide growths (Figure 3-1). The growth chamber was pumped down to a range of 1-5x10$^{-9}$ torr using an Oxford Cryo-Torr 8 cryopump. The MBE system is equipped with a RHEED gun to provide in-situ characterization of the oxide film during growth. The MBE system contains six ports with five of them containing Knudsen
cells (3 Riber 125 LK’s with 25 cc crucibles, 1 Varian 0981-4135 with a 40 cc crucible, and 1 EPI 91-734 with a 25 cc crucible) for various (Sc, Ga, Mg, Ca, and Sm) sources and the remaining port for the oxygen plasma source. The temperature of the Knudsen cells is controlled by a FICS 10 controller that adjusts the power output of an external power supply whose power cables are connected to two posts on the cell.

An MDP21 radio frequency (rf) source from Oxford Applied Research was used as the oxygen source for growth. It was operated at a frequency of 13.56 MHz with a forward power of 300W and reflected power of 2-3W. Oxygen (99.995%) was supplied to the plasma head using a high purity 8161c Unit (Celerity) O₂ mass flow controller (MFC) that had a 3 sccm full scale range. The plasma is generated as soon as a high enough voltage is applied between the two electrodes to create an electric field in the reactor that exceeds the breakdown voltage of the gas. The dissociated atoms and undissociated molecules then escape into the vacuum environment through an array of fine holes in the aperture plate. The electrical potential remains low enough so that negligible currents of ions and electrons will escape through the discharge tube.

A Varian Intevac Modular Gen II system was used to deposit all arsenide films (Figure 3-2). The three separate zones of this system are the main growth chamber, the loadlock (for sample introduction), and the conjoining buffer chamber. The main chamber is pumped to high vacuum (~10⁻⁸ torr) using a 2200 L/s turbo pump and a CTI-8 cryogenic pump. Further pumping of the growth chamber (during a growth run) is provided by an LN₂ cryoshroud within the growth chamber. This cryoshroud also provides cooling for the system effusion ovens. Attached to the main chamber source flange are all of the points of injection for the Group III, Group V, and dopant sources used. These sources are angled to converge at a point at the sample heater, which is calibrated to provide controlled temperature growth to over 1000 °C. The
system mass spectrometer and RHEED gun and screen (for in-situ sample characterization) are also attached to the main growth chamber.

The MOMBIE is equipped with gas-based sources to provide reactive As, P, and N. The system is outfitted with arsine (AsH$_3$) and phosphine (PH$_3$) to provide the As and P fluxes. Due to the toxicity of these hydride gases, their bottles are contained in a gas cabinet outside of the system facility, and plumbed into the building through an evacuated conduit to contain the gas in the event of a leak. The hydride gas flow is regulated through a dedicated mass flow controller, and introduced into the chamber through a catalytic-based thermal cracker unit. This injector is operated at high temperature to decompose the hydride gas into its monatomic and diatomic species, plus H$_2$ gas. These species are then free to react at the substrate, while the H$_2$ is pumped out of the system. A gas source for As and P is an alternative to the dual zone solid effusion cells that can be used to provide the monatomic and diatomic species from solid As$_4$ and P$_4$. Through the mass flow controller, it is easier to consistently control the group V flux than through resistive heating and evaporation of a solid. Replenishing the source is also easier, as the bottle simply has to be changed. A dual zone solid effusion cell was also used to evaporate As pellets by resistive heating. The manganese was supplied by evaporating 6N manganese pellets in an effusion oven through resistive heating.

The substrate temperature was measured in both systems using a backside thermocouple. The substrate thermocouple was calibrated by using pieces of gallium antimonide (GaSb) and indium antimonide (InSb), which have melting points of 707°C and 525°C respectively. The pieces of GaSb and InSb were heated in the growth position under a nitrogen plasma to reduce the chance of losing Sb. Loss of the group V species during heating would result in an incorrect melting temperature.
Substrate Preparation

GaAs

A series of surface treatments “ex-situ” and “in-situ” were employed to clean the GaAs substrates prior to oxide deposition. Epi-ready silicon doped (n-type) GaAs wafers from University Wafer were As capped in the MOMBE system by raising the substrate temperature to 770°C for 10 minutes under an As overpressure until a streaky RHEED pattern was observed. Then the substrate was cooled to 50°C also under As overpressure. This process results in a thick amorphous As capping layer with a discontinuous milky appearance. The substrates were then mounted on recessed molybdenum blocks using tantalum wire so as to avoid As removal during sample mounting with indium on the hot plate. The substrate was then placed in the MBE system used for oxide deposition. The substrate temperature was increased to 400°C and held there for 10 minutes. A very faint RHEED pattern with arcs was observed. As the temperature was raised to 500°C and held there for 10 minutes, the pattern became spotty with faint arcs. Lastly, the temperature was raised to 600°C and a spotty RHEED pattern was immediately observed (Figure 3-3). After oxide deposition, the substrate was examined with atomic force microscopy (AFM) measurements which revealed a root mean square (RMS) roughness value of 8.5 nm. A streaky RHEED pattern was never observed with this process.

The second surface treatment employed involved the sulfur passivation of GaAs using a super-saturated ammonia sulfide (NH₄)₂Sₙ solution. The solution was prepared by dissolving precipitated 99.5% sulfur powder purchased from Alfa Aesar in a beaker of ammonium sulfide (NH₄)₂Sₙ solution purchased from Fisher Scientific. Silicon doped (n-type) GaAs wafers from Wacker-Chemitronic GHMB were used in these experiments. First, the substrate was etched with a solution of H₃PO₄:H₂O₂:H₂O (3:1:50) to remove the native oxide. Then, a UVDOCS, Inc. ultraviolet-ozone (UV-O₃) system was used for twenty-five minutes to remove hydrogen on
surface left behind by the acid etch. The samples were then dipped in buffered oxide etch (BOE) to remove the oxide left behind from the oxygen rich environment of the UV-O₃ cleaning. Lastly, the sample was dipped in the (NH₄)Sₓ solution for sulfur passivation, rinsed in deionized water (DI H₂O), and N₂ dried. This process leaves a discontinuous hazy film on the GaAs surface. Then the substrate was immediately placed in the MBE system and the surface analyzed with RHEED at room temperature before oxide deposition. Very faint streaky RHEED patterns (Figure 3-4A) were observed at room temperature and became spotty at 500°C (Figure 3-4B). The very faint RHEED pattern, issues with surface roughening, and difficulty with reproducibility of this pattern made the sulfur passivation process unreliable.

By far, GaAs cleaning with AH was the most effective and reproducible technique. The source of AH was an MDP21 radio frequency (rf) source from Oxford Applied Research. The rf power used to create the discharge was 300W while the equilibrium background pressure of hydrogen in the MBE chamber was 5x10⁻⁷ Torr. Emission lines in the visible spectrum (H₉ (434), H₂ (486), H₂ (650)) characteristic of the hydrogen atom were seen in a typical optical spectrum recorded under standard operating conditions of the source (Figure 3-5). This spectrum is identical to spectra reported in the literature and suggests that a large fraction of the flux emanating from the source is comprised of AH²⁴. Initial experiments produced very bright streaky RHEED patterns of GaAs (1x1) after 60-75 minutes of AH exposure at a substrate temperature of 500°C (Figure 3-6). The recipe was later refined to include an ex-situ wet etching step to remove the native oxide. Wacker-Chemitronic GHMB GaAs substrates were submerged in a H₃PO₄:H₂O (3:80) solution for 2 minutes and then immediately loaded in the system. A very bright spotty-streaky RHEED pattern was observed after 20-30 minutes of AH exposure at a substrate temperature of 500°C. AFM measurements revealed a significant increase in surface
roughness of the as-received substrate (~ 0.35 nm) after the ex-situ etching for 2 minutes and 20 minutes of AH exposure (~ 2.34 nm) (Figures 3-7A and 3-7B). The recipe was refined again to compensate for the increase in surface roughness which was believed to be due to overetching by decreasing the etch time to 90 seconds. Consequently, streaky RHEED patterns were routinely observed around room temperature and 20 minutes of AH exposure. As the substrate temperature was increased to 300ºC the RHEED pattern became increasingly brighter. This recipe was used on an epi-ready Si-doped (7x10⁶) GaAs (100) wafer purchased from Wafer World, Inc. Since the surface of the wafer contains one or two monolayers of oxide the wet etching step was omitted. The wafer was exposed to AH for approximately 35 minutes (Figure 3-8A-D) and a streaky RHEED pattern was never observed.

**GaN**

MOCVD grown gallium nitride (GaN) substrates purchased from Uniroyal were used for these experiments. Prior to being loaded in the system, the substrates were etched with a HCl:H₂O (1:1) solution for five minutes. Then the substrates were exposed to UV-O₃ for twenty-five minutes followed by a BOE for three minutes and N₂ dried. Before loading the samples in the growth chamber, the substrate heater was outgassed for five minutes facing away from the sources. While the cryopanels were being cooled with liquid nitrogen, the As shutter was opened while being heated to temperature to create an As-rich environment in the growth chamber. The substrates were then loaded on the car and the substrate was taken up to 700ºC and held there for five minutes under As-rich conditions until a streaky RHEED pattern was observed. The substrate was then cooled to 300ºC for MnAs growth.

**MOS Capacitor Fabrication**

After the oxide films were deposited and the samples removed from the MBE system and molybdenum block were processed to make MOS capacitors. Before any processing occurs the
oxide thickness was measured by ellipsometry and verified by profilometry. The first processing step involved applying a thin layer (~ 500 nm) of lift-off resist (LOR). The second step was to apply a second layer of thick (~ 1500 nm) photoresist (PR) on top of the LOR. The samples were then exposed in an aligner to open up windows to the oxide. After exposure, the PR was developed and rinsed with DI H2O. To ensure that the PR has been fully developed and washed away the sample was inspected visually with a light microscope. Profilometry was also used to verify the efficacy of this process. The final processing step involved depositing platinum/gold metal gates. Fabrication of the MOS capacitors allowed I-V and C-V measurements to be taken which helped to determine the performance of the oxide. The key processing steps involved etching, photolithography and metallization. These processing steps will be discussed in more detail in the following sections.

Ellipsometry and Profilometry

Ellipsometry is used for determining the thickness and optical constants (n and k) of dielectric films. The technique involves the use of plane-polarized light which reflects off a sample at a given angle and is then analyzed for a change in the polarization. Analysis of the change in polarization yields two parameters (the azimuth and phase difference) from which the optical properties are calculated. A Rudolph V-530044 Auto EL IV ellipsometer was used for characterization of the oxide films. The ellipsometer was programmed to measure the thickness and optical constants of any transparent film on any substrate. Etching experiments were conducted to verify the thickness measurements generated by ellipsometry. A Dektak profilometer was used to measure a step edge in the oxide created by pasting an acid-resistant black wax across one side of sample and submerging the sample in the etch solution. A HCl:H2O (1:400) solution was used for the etching of Sm2O3. It was determined that etching for 50 seconds completely removes a ~ 47.5 nm thick film corresponding to an etch rate of 9.5
Å/sec. A thickness difference of ~2% was found between ellipsometry and profilometry measurements.

**Photolithography**

Shipley 1818 was used as the PR in a bi-layer stack with lift-off resist (LOR 3B). A Laurell WS-400A 6NPP/Lite was used to spin the PR on the samples. First, the LOR 3B was spun on the samples using a Headway Research spinner. The high development rate of the LOR 3B provides an undercut profile (Figure 3-9) of the film below the 1818, making it attractive for metal lift-off. Dynamic dispense was used to apply both resists as they were dispensed individually at 1000 rpm (and acceleration of 1200 rpm/sec) and spun to a final speed of 5000 rpm (and acceleration of 1500 rpm/sec). A spin speed of 5000 rpm corresponded to a thickness range of 2.0–2.2 μm. The samples were then given a soft bake on a Thermolyne hot plate at 105°C for 1 – 1.5 minutes.

A Karl Suss MA6 mask aligner was used to align the sample to the pattern in the mask and then expose the sample with a mercury xenon lamp at a 365 nm wavelength. Hard contact mode was used which presses the sample firmly against the mask to minimize any diffraction effects. A shadow mask was used to deposit metal gates of 100μm diameter (Figure 3-10). Other parameters included an Al gap of 100 μm, WEC offset of 0, and WEC type as contact. The exposure time was calibrated based on the PR thickness and exposure dose.

After exposure, the samples were developed in AZ 300 MIF developer at room temperature. The development time was 30–60 seconds, depending on the exposure time. After developing the samples, they were rinsed in DI water and then blown dry with an N₂ gun.
Metallization

A Kurt Lesker CMS-18 multi target sputter deposition tool was used to sputter the metal gates. Sputtering involves the ejection of atoms from a solid metal target due to the momentum transfer from bombarding energetic ions (i.e., Ar+). A DC voltage is maintained across plane parallel electrodes with the metal target serving as the cathode and the substrate (or sample) serving as the anode. A large supply of energetic ions in the interelectrode region is accelerated to the material target under an applied electric field. Once the energetic ions strike the target, atoms are dislodged from the metal target by momentum transfer. The dislodged metal atoms then deposit on the substrate. The sputter yield depends on the ion flux of the target, the probability that the impact of the energetic ion ejects a target atom, and the transport of the sputtered material across the interelectrode region to the substrate.

Gate contacts on the dielectric included a bi-layer structure of Pt (20 nm)/Au (80 nm). The Pt layer promotes adhesion to the dielectric, and the Au layer is used for making contact to tips since the layer does not oxidize. Gate contact diameters of 100 μm were used for the MOS capacitors.

After metal deposition, metal lift-off was performed in a sonicator. Samples were immersed in a beaker of MicroChem Nano Remover PG, which was then transferred into the sonication bath. Samples experiencing difficulty with lift off were heated up to 50–60°C for 30 minutes on a Thermolyne hot plate before using the sonicator again. Once lift-off was complete, samples were rinsed in isopropanol then DI water and finally blown dry with an N₂ gun.

Materials Characterization

After oxide deposition, all samples were characterized with a repertoire of techniques to determine the effects of varying the growth parameters. This chapter will briefly review the
different characterization techniques used to characterize all films during the course of this study.

All of the characterization tools described in this chapter are located on the campus of the
University of Florida and are available to trained graduate students upon request.

**Powder X-Ray Diffraction**

Structural information was determined using powder X-Ray Diffraction (XRD). Powder x-ray diffraction is a powerful technique used to identify the crystalline phases present and to measure a host of structural properties such as strain state, grain size, and phase composition. The XRD measurements were performed using a Phillips APD 3720 diffractometer. The system uses a copper (Cu) x-ray source which predominantly generates the Cu\textsubscript{Kα1} x-rays with a 1.54056 Å wavelength and, to a lesser extent, the Cu\textsubscript{Kα1} (1.39217 Å) and the Cu\textsubscript{Kα2} (1.54434 Å) x-rays.

In XRD, the incident x-rays are subjected to constructive and destructive interference due to their interaction with atomic planes of the crystalline sample, in accordance with Bragg’s law seen in Equation 3-1\textsuperscript{90}:

\[ n\lambda = 2d \sin \theta \]  

where \( \theta \) is the angle between the incident x-ray beam and an atomic plane and \( d \) is the atomic plane spacing. The Phillips 3720 uses an automated goniometer with an attached photon counter to measure and store digitally the intensity of the diffracted x-rays. A plot of intensity versus \( 2\theta \) yields the diffraction pattern of the sample. Throughout the course of this thesis work, the diffraction pattern is used primarily to identify crystalline phases in the sample.

**Atomic Force Microscopy**

Morphological measurements were done using a Dimension 3100 Atomic Force Microscope (AFM) with a nanoscope IIIa controller. The AFM uses a very sharp tip as a probe moving over the surface of a sample in a raster scan. The tip is attached to the end of a
cantilever which bends in response to a force between the tip and the sample. The cantilever has a spring constant of about 0.1 N/m, which is more than an order of magnitude lower than the typical spring constant between two atoms. A laser light is reflected at an oblique angle from the very end of the cantilever. A force between the tip and the sample is sufficient to cause deflection of the cantilever which can be measured as a function lateral position. A plot of laser deflection versus tip position on the sample surface constitutes the surface topography of the sample.

**Reflection High Electron Diffraction**

Reflection High Energy Electron Diffraction (RHEED) is a powerful tool for investigating the surface structure of crystalline samples in ultrahigh vacuum. Information on the surface symmetry, atomic step density, and evidence of surface roughness are contained in the RHEED pattern. For deposited materials that are lattice-mismatched to a substrate, strain will build up at the interface generating misfit dislocations until eventually it becomes energetically favorable for 3D clusters of the deposited material's relaxed crystal structure to form. Direct evidence on the growth mode of a film lies in the ability of the technique to differentiate between 2D and 3D structure. Surface reconstructions during deposition can be monitored with RHEED to obtain optimal growth conditions. RHEED will be employed *in-situ* to gain all of the useful information regarding film growth stated in this study. A Staib electron gun operating at 15 kV was used to perform all RHEED measurements. RHEED is performed by striking the surface of a sample at a grazing angle (1-2°) with a high energy electron beam. Due to the small angle of incidence, the incident electrons will only diffract from the first few atomic layers, making RHEED useful for observing surface reconstructions and determining the surface growth mode. The diffracted electron beams are made to impinge a phosphor screen opposite the electron gun. This light produces a pattern on the screen which can be recorded by camera. A polycrystalline
film produces a ring pattern, whereas an amorphous film produces no pattern due to a lack of long range order for diffraction. A surface growing layer-by-layer (2D) will produce a streaky pattern. A spotty pattern is indicative of an island growth mechanism (3D). Owing to its grazing angle geometry, RHEED is very sensitive to island formation because the reflected beam is transmitted through island asperities which give rise to new diffraction features. Transmission Electron Microscopy (TEM) was used to verify the absence of second phases in the specimens and it will also be used to investigate the crystal quality of interfaces. However, sample preparation and data interpretation are non-trivial, so TEM was explored only on selected samples.

**Auger Electron Spectroscopy**

Chemical composition information was determined by Auger Electron Spectroscopy (AES). AES involves the detection of electrons emitted from the sample surface due to the interaction of an incident electron beam. Auger electrons are low energy and are released from the first few atomic layers of the sample making AES a very surface-sensitive technique. The basic Auger process involves the production of an atomic shell vacancy, usually by electron bombardment, and the decay of the atom from this excited state by an electronic rearrangement and emission of an electron with characteristic energy. This characteristic energy is the basis for the identification of chemical composition. Spectra are acquired using a cylindrical mirror analyzer (CMA) and a computer-controlled digital signal acquisition system. The resulting detected energy spectrum then allows a qualitative compositional analysis to be obtained of the surface, and through peak height analysis using published elemental sensitivity factors, an approximate analysis can be calculated. The Perkin Elmer 6600 Auger system used in this study is fitted with an Ar sputter gun allowing compositional depth profiling.
X-ray Photoelectron Spectroscopy

A Perkin-Elmer PHI 5100 ESCA system was used for all XPS characterization. This characterization technique was used to look at chemical bonding in the deposited films by measuring the binding energies of atoms in the top few monolayers. It uses x-rays as its source to eject photoelectrons from the sample. Due to the small escape depth (depends on KE of photoelectron and material through which it travels) of the photoelectrons, XPS is limited to surface analysis (top few monolayers). The kinetic energy of the photoelectrons is measured by a hemispherical analyzer and the binding energy is calculated using Equation 3-2:

\[ BE = h \nu - KE - \phi_{SP} \]  

(3-2)

where \( h \nu \) is the energy of the incident x-ray (1486.6 eV for Al and 1256.6 eV for Mg), \( KE \) is the kinetic energy (in eV) of the photoelectron, \( \phi_{SP} \) is the work function of the spectrometer, and \( BE \) is the binding energy (in eV) of the photoelectron. The Mg anode was used in all of these experiments. The electron binding energy is highly influenced by its chemical surroundings. The general trend is that binding energy increases with increasing charge on the atom. The characteristic peaks produced in the spectrum were identified using handbooks containing previously determined standards. The handbooks show the energies of core and valence level electrons and Auger electrons for atoms in their zero-valence state and their different oxidation states when bonded to other chemical species. This information was used to identify the chemical constituents present in the film and whether any of the constituents were bonded to each other.

SQUID

All the magnetic measurements in this dissertation were performed in a Quantum Design magnetic property measurement system superconducting quantum interference device.
magnetometer. In a SQUID, a system of superconducting detection coils is connected to a closed loop of superconducting material containing two Josephson junctions. The measurements are made by moving the sample through these detection coils. As the sample moves through the coils, the magnetism of the sample induces an electric current in the coils. The SQUID device can be configured with its related electronics to produce an output voltage that is proportional to the magnetic moment of the sample. A hysteretic plot of the magnetization of the sample versus applied field (M vs. H) can be obtained to confirm the ferromagnetic behavior of the sample. The system is calibrated with a sample of known magnetism. A superconducting solenoidal magnet is used to produce magnetic fields in the range of 7 T. A superconducting shield is placed between the magnet and the SQUID device to shield the SQUID from the field generated in the magnet and to stabilize the field contained by the shield, due to the high sensitivity of the SQUID device. A SQUID can detect a change of $10^{-15}$ T in a field of up to 7 T. Due to the superconducting nature of the detection system and the magnet, the system is cooled to liquid helium temperatures. The ferromagnetism of the sample can also be confirmed with a field cooled/zero field cooled (FC/ZFC) measurement of magnetization versus temperature (M vs. T). The ZFC part of the measurement consists of first cooling the sample to approximately 10 K with no applied field, turning on the magnet to a predetermined value, and measuring the magnetization at the temperature is increased back to room temperature. With the field still on, the sample is cooled back to 10 K, while measuring the magnetization. This is the FC part. The temperature at which these two curves intersect is a measure of the Curie temperature.

**Electrical Measurements**

All electrical measurements were conducted with a Signatone S-1160 Series General Purpose Analytical Probe Station. The probe station is interfaced with the appropriate equipment for measuring electrical properties such as capacitance, current, and voltage. Although all of the
electrical measurements performed during the course of this study were performed at room temperature, the probe station is equipped with a temperature-controlled stage allowing for temperature-dependent measurements to be collected.

**Current-Voltage Measurements**

Current versus Voltage (I-V) measurements were performed with an Agilent 4155C Semiconductor Parameter Analyzer. Compliance was set at 100 nA, and the voltage was swept in both negative and positive directions until the forward and reverse breakdowns were reached. Voltages were extracted from the I-V plot at 78.5 nA which corresponds to a current density of 1 mA/cm² (typical breakdown voltages are reported at this current density). The extracted voltages were then divided by the dielectric film thickness to determine the forward and reverse breakdown voltages.

**Capacitance-Voltage Measurements**

Capacitance versus Voltage (C-V) measurements collected with an Agilent 4284A 20Hz-1MHz Precision LCR meter connected to a Lab View based PC was used to make capacitance-voltage measurements. The LCR meter supplied a voltage signal of superimposed analog current (AC) and direct current (DC). Devices were cycled at frequencies ranging from 10 kHz to 1 MHz in the series (C<sub>s</sub>-R<sub>s</sub>) mode at an oscillation voltage between 50 mV- 2000 mV. All devices were swept from accumulation to depletion and back to accumulation to investigate the nature of fixed oxide traps. The devices were also swept from depletion to accumulation and back to depletion for comparison. The data from the C-V curve was used to determine the interface state density, flat band voltage shift, and dielectric constant (discussed in more detail in Appendix A).
Figure 3-1. Top view sketch of the Riber 2300 MBE system used for the oxide growth.
Figure 3-2. A top view sketch of the Varian MOD Gen II MBE growth system.
Figure 3-3. Spotty RHEED image of GaAs after thermal cleaning up to 600°C.

Figure 3-4. RHEED image of a Sulfur-passivated GaAs (1x1) at 500°C (A) Faint spotty-streaky RHEED pattern (B) Bright spotty image indicative of surface contamination.
Figure 3-5. Typical optical emission spectrum of the hydrogen plasma operating at a forward power of 200 W and a flow rate 0.12 sccm.
Figure 3-6. Streaky RHEED patterns of GaAs exposed to AH for different times (A) before AH exposure, (B) 15 minutes of AH exposure, (C) 45 minutes of AH exposure, and (D) 60 minutes of AH exposure
Figure 3-7. AFM images of GaAs. (A) as-received substrate. (B) corresponding substrate after 20 minutes of AH exposure.
Figure 3-8. RHEED images of Epi-ready GaAs substrate (A) before, (B) after 12 minutes of AH exposure, (C) after 25 minutes, and after 35 minutes of AH exposure.
Figure 3-9. Schematic of the resist scheme for diode processing. (A) Profile of bi-layer resist showing undercut profile after exposure. (B) Profile of bi-layer resist with deposited metal (black) showing the advantage of undercut profile.
Figure 3-10. Layout of shadow mask used to fabricate diodes with 100µm diameter windows for metallization.
CHAPTER 4
GROWTH AND CHARACTERIZATION OF SAMARIUM OXIDE

Growth Conditions

The objective of this work was to deposit Sm$_2$O$_3$ on GaAs. Sm$_2$O$_3$ has a bixbyite crystal structure which is composed of two interpenetrating face centered cubic. The lattice parameter of Sm$_2$O$_3$ is 5.32 nm representing a lattice mismatch of 3.3% with the zinc blende cubic structure of GaAs (lattice parameter 5.65 nm). Sm$_2$O$_3$ was grown using a Sm cell temperature of 570ºC and the O provided via an oxygen plasma attached to the system. Two substrate temperature were used (100ºC and 500ºC) in attempt to affect the crystalinity (amorphous vs. crystalline) of the oxide.

Growth at Low Substrate Temperature

XRD measurements of Sm$_2$O$_3$ grown on GaAs at a substrate temperature of 100ºC showed an amorphous nature of the film verified by RHEED measurements. The peaks at 32.15º and 66.53º are associated with GaAs (200) and the GaAs (400) of the cubic phase (Figure 4-1). XRD scans of films grown at 100ºC showed no peaks. The RMS roughness value was measured at 1.41 nm (Figure 4-2). XPS measurements confirmed the presence of Sm free metal in the film (Figure 4-3). The small broad peak located at 1082.5 eV represents the Sm free metal peak and the more dominant peak associated with Sm bonded to O. The breakdown field strength was measured at 3.96 MV/cm (Figure 4-4). The C-V characteristics were poor.

Growth at High Substrate Temperature

XRD measurements of Sm$_2$O$_3$ grown on GaAs at a substrate temperature of 500ºC showed a crystalline nature of the film verified by RHEED measurements (Figure 4-5) taken 12 minutes into the growth of Sm$_2$O$_3$. The RHEED image remained streaky for the duration of growth. XRD measurements showed a broad peak at 29.95º which is attributed to the Sm$_2$O$_3$(321) of the
cubic phase (Figure 4-6). The peak at 44.15° is associated with Sm$_2$O$_3$(403) of the monoclinic phase. The very small shoulder at 28.33° is associated with Sm$_2$O$_3$(222) of the cubic phase. The peaks at 32.15° and 66.53° are associated with GaAs (200) and the GaAs (400) of the cubic phase. AFM measurements revealed a smooth film surface with a RMS roughness value of 0.631 nm (Figure 4-7). XPS measurements confirmed the presence of Sm free metal in the film (Figure 4-8). The small broad peak located at 1078.9 eV represents the Sm free metal peak and the peak at 1082.3 represent Sm bonded to O. The breakdown field strength was measured at 3.38 MV/cm (Figure 4-9). The C-V characteristics diodes with this film showed a very small change in capacitance when swept from depletion to accumulation.
Figure 4-1. Amorphous Sm$_2$O$_3$ grown on GaAs at a substrate temperature of 100ºC and a Sm cell temperature of 570ºC (growth rate $\sim$ 6Å/min).
Figure 4-2. Morphology of amorphous Sm$_2$O$_3$ grown on a GaAs at a substrate temperature of 100°C and a Sm cell temperature 570°C (growth rate ~ 6Å/min).
Figure 4-3. Sm $3d_{5/2}$ core level XPS peak from Sm$_2$O$_3$ grown at a substrate temperature 100°C and a Sm cell temperature of 570°C (growth rate ~ 6Å/min) showing evidence of Sm unbonded metal.
Figure 4-4. Electrical characterization of Sm₂O₃ on GaAs at a substrate temperature of 100°C and a Sm cell temperature of 570°C (growth rate ~ 6Å/min).
Figure 4-5. RHEED image taken 12 minutes into the growth of Sm$_2$O$_3$ grown at a substrate temperature of 500°C and a Sm cell temperature of 550°C
Figure 4-6. Crystalline Sm₂O₃ grown on GaAs at a substrate temperature of 500°C and a Sm cell temperature of 570°C (growth rate ~6Å/min).
Figure 4-7. Morphology of crystalline Sm$_2$O$_3$ grown on a GaAs at a substrate temperature of 500ºC and a Sm cell temperature 570ºC (growth rate ~ 6Å/min).
Figure 4-8. XPS narrow scan measurement of the Sm $3d_{5/2}$ core level from Sm$_2$O$_3$ grown at a substrate temperature 500ºC and a Sm cell temperature of 570ºC (growth rate ~ 6Å/min).
Figure 4-9. Current versus voltage plot of crystalline Sm$_2$O$_3$ on GaAs at a substrate temperature of 500ºC and a Sm cell temperature of 570ºC (growth rate ~ 6Å/min).
CHAPTER 5
XPS MEASUREMENT OF THE SAMARIUM OXIDE-GALLIUM ARSENIDE HETEROJUNCTION BAND OFFSET

Core Level Photoemission Method for Determining the Heterojunction Band Offset

One of the major challenges in compound semiconductor device technology has been the development of a thermodynamically stable dielectric technology suitable for use in MOSFETs. For this application, the dielectric must provide good surface passivation, good resistance to breakdown under an applied field and must have a band alignment with the underlying semiconductor such that carriers in both the conduction and valence bands are confined to the semiconductor. For the latter requirement, discontinuities of at least 1 eV are desired. Promising results on GaAs have been obtained using crystalline gadolinium oxide (Gd$_2$O$_3$), in spite of the bond length mismatch with GaAs of ~4.4%. Based on this success with Gd$_2$O$_3$, Sm$_2$O$_3$ would appear to be a promising dielectric material for GaAs substrates based on its higher dielectric constant (18 vs. 11) and lower lattice mismatch with GaAs (3.3% vs. 4.4%).

Also, based on available electron affinity data, the Sm$_2$O$_3$ would be expected to produce better confinement on the valence band, though no data has yet been reported for band offsets with GaAs. Such data is essential if this dielectric is to be considered for use in a GaAs-based c-MOS technology. This section reports an x-ray photoelectron spectroscopy (XPS) study on Sm$_2$O$_3$/GaAs heterostructures for the determination of band discontinuities using a core-level photoemission based method. The oxide material in this study was deposited by plasma assisted molecular beam epitaxy (MBE).

The surfaces of the specimens were examined initially by low-resolution survey scans to determine which elements were present and their respective concentrations. Very-high-resolution spectra were acquired to determine the precise binding energy (i.e., chemical state) of each core-level. As mentioned previously, a core-level photoemission based method was used to
determine the valence band offset. Appropriate core-level peaks were referenced to the top of the valence band for the GaAs and the thick Sm$_2$O$_3$, using a linear extrapolation method to determine the valence band maximum. The resulting binding energy differences between core level and valence band maxima for each layer were combined with the core level binding energy difference of the heterojunction sample (5nm Sm$_2$O$_3$/GaAs) to determine the valence band offset, according to Equation 5-1:

$$\Delta E_V = (\Delta E_{CL})_{A-B} + (E_{CL} - E_V)_B - (E_{CL} - E_V)_A$$ (5-1)

where $\Delta E_{CL}$ is the energy difference of core levels of material A and material B. $E_V$ is the valence band maximum. Core levels were located with Gaussian-Lorentzian curve-fits. To precisely determine peak position, a full width at half maximum (FWHM) method$^{98,99}$ was used to determine the exact binding energy after all peaks have been accounted for over the entire narrow scan region.

### Results of Sm$_2$O$_3$-GaAs Heterojunction Band Offset Measurement

The XPS Ga 3$d_{5/2}$ and Sm 3$d_{5/2}$ narrow scan and valence band spectrum were measured from a sputter-exposed GaAs substrate and the (94 nm) thick Sm$_2$O$_3$ layer, respectively (Figures 5-1 and 5-2). The position of the Ga 3$d_{5/2}$ peak ($E_{CL}$)$_B$ was determined to be 20.07±0.1 eV. The position of the Sm 3$d_{5/2}$ ($E_{CL}$)$_A$ was determined to be 1084.57±0.1 eV. A pass energy of 17.9 eV and a step size of 0.05 eV were used to collect measurements near the valence band maxima of the GaAs substrate and the thick Sm$_2$O$_3$ layer (Figures 5-3 and 5-4). High resolution measurements were taken near the VBM to ensure exact band edge location. The valence band value, $E_V$, was determined by linearly fitting the leading edge of the valence band and linearly fitting the flat energy distribution and finding the intersection of these two lines. The valence band maxima were determined to be 0.405±0.05 eV and 3.04±0.05 eV for the GaAs substrate.
and the thick Sm$_2$O$_3$ layer, respectively. The XPS Ga 3$d_{5/2}$ (top) and Sm 3$d_{5/2}$ (bottom) narrow scans were taken from the thin (5.0 nm) Sm$_2$O$_3$ layer. The Ga 3$d_{5/2}$ and Sm 3$d_{5/2}$ core levels were determined to be positioned at 19.69±0.1 eV and 1083.83±0.1 eV, respectively. The energy difference between the Ga 3$d_{5/2}$ and Sm 3$d_{5/2}$ core levels, $\Delta E_{CL}$, was determined to be 1064.14 eV. The Ga 3$d_{5/2}$ peak can be deconvoluted to give a predominant peak at 19.49 eV which is typical of GaAs$^{100,101}$ (Figure 5-5). The well pronounced asymmetry in the high binding energy (BE) side of the Ga 3$d_{5/2}$ shows the existence of gallium oxides$^{101}$ A low intensity, broad peak on the high BE side associated with the O 2s peak located at 23.33 eV$^{102}$ and a second low intensity, very broad peak at 22.37 eV which is probably associated with a mixture of the compounds GaAsO$_4$ and Ga$_2$O$_3$$^{103,104,105}$ These peaks do not show up in the Ga 3$d_{5/2}$ narrow scan of the GaAs substrate because the substrate was sputtered for nearly ten minutes to remove native oxides. The Sm 3$d_{5/2}$ peak can be deconvoluted to give a predominant peak at 1083.83 eV and a low intensity, broad peak at 1079.8 eV (Figure 5-6). The shoulder to the low BE side of the predominant peak at 1083.83 eV is probably a consequence of strong charge-transfer effects due to unpaired 4$f$ electrons in Sm$_2$O$_3$$^{106}$ Core-level survey spectra of a GaAs substrate, a 94 nm thick Sm$_2$O$_3$/GaAs, and a thin (50 Å) Sm$_2$O$_3$/GaAs sample were taken with a pass energy of 44.75 eV at a takeoff angle of 45° (Figure 5-7). The topmost curve is the XPS survey scan for the thin sample (50 Å) of Sm$_2$O$_3$/GaAs, the bottom curve is the XPS survey scan of a bulk GaAs substrate, and the middle curve is the XPS survey scan of the 94 nm thick Sm$_2$O$_3$/GaAs sample. The Sm 3$d_{5/2}$ and the O 1$s$ have been labeled on the scans of the oxide samples. The Ga 3$d_{5/2}$ and As 3$p_{3/2}$ have been identified on the scan of the GaAs substrate. The substrate was sputtered for approximately ten minutes to remove native oxides. An energy band diagram of the Sm$_2$O$_3$/GaAs system generated using the values obtained in this study (Figure 5-8).
Summary of Heterojunction Band Offset Measurement

The valence band offset, $\Delta E_V$, has been measured in the Sm$_2$O$_3$/GaAs system by XPS for the first time. $\Delta E_V$ was determined to be 2.63±0.1 eV. Given a band gap difference of 3.68 eV, the $\Delta E_C$ was determined to be 1.13±0.1 eV. These results show that good valence and conduction band offsets can be obtained in this materials system.
Figure 5-1. Ga 3d_{5/2} core level XPS peak taken from a sputtered GaAs substrate.
Figure 5-2. Sm $3d_{5/2}$ core level XPS peak taken from a thick (94 nm) Sm$_2$O$_3$/GaAs heterojunction interface.
Figure 5-3. GaAs Valence Band Maximum showing the intersection of a fitted line to the background energy and the first slope past 0 eV.
Figure 5-4. Sm$_2$O$_3$ Valence Band Maximum measurement by XPS showing the intersection of the fitted line to the background energy and the first slope past 0 eV.
Figure 5-5. Narrow scan of the Ga $3d_{5/2}$ core level XPS peak for the thin (50 Å) Sm$_2$O$_3$/GaAs heterojunction interface.
Figure 5-6. Sm $3d_{5/2}$ core level XPS peak taken from the thin (50 Å) Sm$_2$O$_3$/GaAs heterojunction interface showing the unbonded Sm metal peak.
Figure 5-7. Survey scan of a thin (50 Å) Sm$_2$O$_3$/GaAs Heterojunction interface (topmost curve). Survey scan of a thick (100 nm) Sm$_2$O$_3$/GaAs Heterojunction interface (middle curve). Survey scan of sputtered GaAs substrate.
\[
\begin{align*}
\text{GaAs} & \quad \text{Sm}_2\text{O}_3 \\
E_c & \quad E_c^{\text{Sm}_2\text{O}_3} \\
E_G^{\text{GaAs}} & = 1.42 \text{ eV} \\
E_G & = 5.1 \text{ eV} \\
E_v & = 2.63 \pm 0.1 \text{ eV} \\
E_v^{\text{Sm}_2\text{O}_3} & \\
E_{\text{Ga}3d} & \\
E_B = (E_{\text{Sm}3d^{5/2}} - E_{\text{Ga}3d}) & = 1064.5 \text{ eV} \\
= 1064.5 \text{ eV} \\
(\text{E}_{\text{VBM}} - E_{\text{Sm}3d^{5/2}}) & = 1081.53 \text{ eV}
\end{align*}
\]

Figure 5-8. Energy band spectrum of a thin Sm$_2$O$_3$/GaAs Heterojunction interface. $E_B$ is the corresponding core level separation across the interface.
CHAPTER 6
GROWTH AND CHARACTERIZATION OF SAMARIUM GALLIUM OXIDE

Growth and Characterization of Oxides Grown at 100ºC

The objective of this work was to characterize ternary oxides grown by depositing Sm$_2$O$_3$ with GaO$_x$. The degree of crystallinity was investigated to determine a set of growth conditions for growing a thermally and environmentally stable oxide film. A low growth temperature was chosen to promote the growth of an amorphous or fine grained poly-crystalline dielectric film which from previous work has been shown to enhance I-V performance. A low growth temperature is also ideally suited for these experiments due to the delicate nature of the clean GaAs surface. After the substrate was cleaned the sample was rotated out of the growth position. The H$_2$ plasma was discharged and the O$_2$ plasma lit. The O$_2$ plasma conditions were set to 300 W forward power at a flow rate of 0.25 sccm. The background pressure in the chamber was 5.5x10$^{-6}$ Torr. Once the O$_2$ plasma conditions were set, the sample was then rotated back into the growth position. The samarium cell shutter and the O$_2$ plasma shutter were opened simultaneously to initiate oxide growth. Ga present as a contaminant in the Sm cell and was evaporated along with the Sm. For comparison purposes, this growth procedure was also used for the oxides grown at 300ºC and 500ºC.

Powder XRD measurements of films grown at 100ºC with a T$_{Sm}$ of 550ºC (Figure 6-1) revealed no evidence of peaks associated with crystalline oxides, suggesting that the films grown are amorphous or very fine grained poly-crystalline. Peaks located at 31.9º and 66.3º are associated with the GaAs (200) and GaAs (400). The peak at 59.1º could not be identified with JCPDS files, but it consistently shows up in scans of the GaAs substrate. This peak could be attributed to an artifact due to the polychromatic of the x-ray source used in the powder system. The growth rate was 12.9 Å/sec. The RHEED pattern immediately disappears at the onset of
oxide growth and never returns, also suggesting an amorphous film. TEM micrographs confirm
the presence of an amorphous layer, showing an amorphous interfacial region of approximately
65 Å (Figure 6-2). The surface was smooth with an RMS roughness measured by AFM to be
0.366 nm (Figure 6-3). An AES survey scan of the oxide surface revealed Sm, Ga, O
concentrations of 45.1%, 4.0%, and 50.9% respectively (Figure 6-4). A depth profile showed
that the Ga concentration remained constant throughout the thickness of the film, except for a
sharp increase in the O and Ga concentration occurring at 40 cycles which suggests the presence
of gallium oxide at the interface (Figure 6-5). The cycle interval was 0.20 min/cycle. To
confirm that the Ga was being incorporated from the source beam and not from the GaAs
substrate, a depth profile was conducted on a silicon substrate mounted on the same
molybdenum block during the same growth run. This sample also showed the presence of Ga
throughout the deposited film.

Films grown at 100ºC showed a breakdown field strength as high as 3.63 MV/cm. The C-
V characteristics (Figure 6-6) clearly showed accumulation in the forward direction, but full
depletion in the reverse direction was not reached before reverse breakdown occurred. The gate
electrode voltage was swept from depletion to accumulation.

To investigate the effect of Sm cell temperature, films were grown using Sm cell
temperatures ranging from 510ºC to 570ºC. As expected, the growth rate increases with
increasing cell temperature (Figure 6-7). AES indicates that the Ga composition ranges from
1.3% to just over 10% (Figure 6-7). X-ray photoelectron spectroscopy (XPS) of the deposited
films showed evidence of residual Sm metal in the films which was highest at the highest Sm
cell temperature (Table 6-1). This is most likely due to the reduced oxygen to metal ratio present
during growth given that the Sm flux is increasing with increasing cell temperature. As one
would expect, the breakdown field was lowest in the film with the largest amount of free metal (Figure 6-8). The layer grown at a $T_{Sm} = 550^\circ$C showed the highest oxygen to metal ratio, the lowest RMS surface roughness (Figure 6-9 and 6-10) and had a good breakdown field (Figure 6-8). Consequently, subsequent growths were performed using this cell temperature.

**Growth and Characterization of Oxides Grown at Higher Substrate Temperatures**

Films grown at 300$^\circ$C using the same procedure as discussed in the previous section showed streaky-dashed RHEED patterns which appeared around five minutes into the oxide growth corresponding to thickness of $\sim 5.4$ nm (i.e. growth rate of 1.08 nm/sec) (Figure 6-11A). The initial streaky RHEED pattern of the GaAs substrate disappears after one minute of oxide growth. After thirty minutes of oxide growth the RHEED pattern showed a mixture of arcs and lines suggesting the polycrystalline nature of the film at the end of growth (Figure 6-11B). The background pressure in the chamber was $5 \times 10^{-6}$ Torr. Powder XRD measurements revealed a textured morphology (Figure 6-12). Peaks positioned at 28.9$^\circ$, 42.2$^\circ$ and 52.3$^\circ$ are associated with the cubic phase of Sm$_2$O$_3$ (222), Sm$_2$O$_3$ (134), and Sm$_2$O$_3$ (026) orientations, respectively. Peaks located at 47.3$^\circ$ and 54.8$^\circ$ are associated with the monoclinic phase of the Sm$_2$O$_3$ (602) and Sm$_2$O$_3$ (514) orientations. The remaining peaks in the spectrum are attributed the GaAs substrate. An Auger survey scan confirms the Sm, Ga, and O concentrations of 49.7%, 6.5%, and 43.9% respectively (Figure 6-13). Gallium was also detected throughout the thickness of the oxide with a sharp increase in Ga concentration occurring around 25 cycles into the depth profile with a cycle interval of 0.20 min/cycle (Figure 6-14). XPS analysis of the films showed an Oxygen to Sm metal ratio roughly comparable to that obtained in films grown at 100$^\circ$C (Table 6-2). The film showed an RMS roughness of 0.679 nm (Figure 6-15). Electrical characterization of diodes fabricated from the material showed a breakdown field strength was 3.68 MV/cm, and
poor C-V behavior with no indication of accumulation or complete depletion before breakdown occurs (Figures 6-16 and 6-17).

Films grown at 500ºC showed a bright streaky RHEED pattern with thick diffuse lines after twelve seconds of oxide growth (Figure 6-18A). As the growth proceeds, the lines become faint and arcs begin to appear (Figure 6-18B). Sm cell temperatures of 510ºC and 550ºC were investigated. XRD analysis indicated that the 550ºC cell temperature enhanced the formation of the cubic phase (Figure 6-19 and Figure 6-20). Therefore a 550ºC cell temperature was used for subsequent growths.

As compared to the films grown at 300ºC with the same Sm cell temperature, the crystal quality of the cubic phase was enhanced based on an increase in intensity of the peak located at 30.1º (Figure 6-20). This peak is labeled C and shows up only on the XRD scan of (SmxGa1-x)2O3 grown at a substrate temperature of 500ºC and a Sm cell temperature of 550ºC (green curve in Figure 6-20). Auger survey scans show the concentrations of Sm, Ga, and O to be 54.2%, 3.1%, and 42.7% respectively (Figure 6-21). The Ga and O concentration show a sharp increase at 55 cycles of the depth profile with a cycle interval of 0.20 min/cycle (Figure 6-22). XPS analysis of the films showed an O to Sm metal ratio roughly comparable to that obtained in films grown at 100ºC (Table 6-2). The RMS roughness value was 0.992 nm, representing a significant increase with substrate temperature (Figure 6-23). The TEM micrographs clearly show evidence of atomic registry at a crystalline interface (Figure 6-24). The breakdown field strength was 2.95 MV/cm and the C-V characteristics indicated a flat band voltage shift of 1V accumulation in the forward direction and depletion in the reverse direction (Figures 6-25 and 6-26). Since the C-V curves with this sample showed a significant (≥ 3 pF) change in capacitance as the device was swept from depletion to accumulation, hysteretic C-V curves were also collected. Measurements
collected at 10 kHz clearly showed the hysteretic behavior of the C-V curves (Figure 6-27). The gate voltage was swept from depletion to accumulation and back to depletion.

**Growth and Characterization of Bi-Layer (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ Oxide Stack**

A dielectric layer with high breakdown field is desirable from an electrical standpoint allowing for the growth of thinner oxides with less leakage. As mentioned previously, polycrystalline oxide films deposited at low substrate temperatures typically produce better breakdown behavior than more textured or single crystal films deposited at higher substrate temperatures. Conversely, the crystalline interfaces obtained at the higher substrate temperatures typically produce lower interface state densities. One method of combining the best characteristics of both of these microstructures is to grow the interfacial oxide layer at a high temperature and then drop the temperature for the remainder of the layer. Such a bi-layer oxide stack was grown to combine the interfacial properties of oxide growth at 500ºC and the high breakdown field and surface morphology properties of oxide growth at 100ºC. The oxide film grown at 100ºC exhibited an amorphous nature with breakdown field strength of 3.63 MV/cm and rms value of 0.366 nm. Films grown at 500ºC were crystalline at the interface with a breakdown field strength of 2.95 MV/cm. A flat band voltage shift of 1 V for the oxide film grown at 500ºC is an indication of smaller fixed oxide charge and the C-V characteristics clearly showed accumulation and depletion.

The growth procedure used for the growth of each layer was identical the only difference being the substrate temperature. The growth of the bi-layer oxide stack began with a substrate temperature of 500ºC. The substrate temperature remained at 500ºC for 7.5 minutes. The substrate was rotated away from the sources and cooled to 100ºC. The sample was then rotated back into the growth position for the remainder of the growth run. The powder XRD measurements of the bi-layer stack showed the presence of the cubic phase at 30.01º associated with Sm$_2$O$_3$ (321) orientation (Figure 6-28). The remaining peaks in the spectrum were
identified as GaAs peaks. The surface morphology was relatively smooth with an RMS roughness value of 0.545 nm (Figure 6-29). The breakdown field was measured at 3.13 MV/cm (Figure 6-30). The C-V characteristics of the bi-layer oxide were extremely noisy and thus a $D_{it}$ measurement could not be determined.
Table 6-1. List of (Sm\textsubscript{x}Ga\textsubscript{1-x})\textsubscript{2}O\textsubscript{3} films grown with different Sm cell temperatures showing the oxide, metal, and oxygen XPS peak intensities, ratio of XPS peak intensities, breakdown field, and RMS roughness. The substrate temperature was 100ºC for all samples.

<table>
<thead>
<tr>
<th>Samarium Cell Temperature (ºC)</th>
<th>Intensity of oxide peak (counts)</th>
<th>Intensity of Sm metal peak (counts)</th>
<th>Intensity of oxygen peak (counts)</th>
<th>Ratio of peak intensities (Metal:Oxidized Metal)</th>
<th>Ratio of peak intensities (Oxygen: Sm Metal)</th>
<th>Breakdown Field (MV/cm)</th>
<th>RMS (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>510</td>
<td>42,011</td>
<td>6,830</td>
<td>9,150</td>
<td>0.163</td>
<td>0.187</td>
<td>4.35</td>
<td>0.49</td>
</tr>
<tr>
<td>530</td>
<td>41,386</td>
<td>7,373</td>
<td>8,161</td>
<td>0.178</td>
<td>0.167</td>
<td>3.11</td>
<td>0.53</td>
</tr>
<tr>
<td>550</td>
<td>30,467</td>
<td>5,635</td>
<td>6,904</td>
<td>0.185</td>
<td>0.191</td>
<td>3.63</td>
<td>0.37</td>
</tr>
<tr>
<td>570</td>
<td>23,907</td>
<td>9,599</td>
<td>5,759</td>
<td>0.402</td>
<td>0.172</td>
<td>0.114</td>
<td>0.97</td>
</tr>
</tbody>
</table>

Table 6-2. (Sm\textsubscript{x}Ga\textsubscript{1-x})\textsubscript{2}O\textsubscript{3} films grown with different substrate temperatures showing oxide, metal, and oxygen XPS peak intensities, ratio of XPS peak intensities, breakdown field, and RMS roughness. The Sm cell temperature was 550ºC for all samples.

<table>
<thead>
<tr>
<th>Substrate Temperature (ºC)</th>
<th>Intensity of oxide peak (counts)</th>
<th>Intensity of Sm metal peak (counts)</th>
<th>Intensity of oxygen peak (counts)</th>
<th>Ratio of peak intensities (Metal:Oxidized Metal)</th>
<th>Ratio of peak intensities (Oxygen: Sm Metal)</th>
<th>Breakdown Field (MV/cm)</th>
<th>RMS (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>30,467</td>
<td>5635</td>
<td>6,904</td>
<td>0.185</td>
<td>0.191</td>
<td>3.63</td>
<td>0.37</td>
</tr>
<tr>
<td>300</td>
<td>38,376</td>
<td>6490</td>
<td>8,606</td>
<td>0.169</td>
<td>0.192</td>
<td>3.68</td>
<td>0.68</td>
</tr>
<tr>
<td>500</td>
<td>33,236</td>
<td>5905</td>
<td>7,532</td>
<td>0.178</td>
<td>0.192</td>
<td>2.95</td>
<td>0.99</td>
</tr>
</tbody>
</table>
Figure 6-1. Amorphous (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ grown at 100°C and a Sm cell temperature of 550°C.
Figure 6-2. TEM micrograph of (Sm\textsubscript{x}Ga\textsubscript{1-x})\textsubscript{2}O\textsubscript{3} grown at a substrate temperature of 100°C and a Sm cell temperature of 550°C.
Figure 6-3. Morphology of (Sm\textsubscript{x},Ga\textsubscript{1-x})\textsubscript{2}O\textsubscript{3} grown at a substrate temperature of 100ºC and a Sm cell temperature of 550ºC.
Figure 6-4. Auger survey scan of (Sm\textsubscript{x}Ga\textsubscript{1-x})\textsubscript{2}O\textsubscript{3} grown at 100°C and a Sm cell temperature of 550°C.
Figure 6-5. Depth profile of (Sm\textsubscript{x}Ga\textsubscript{1-x})\textsubscript{2}O\textsubscript{3} grown at 100°C and a Sm cell temperature of 550°C obtained with AES.
Figure 6-6. Capacitance versus voltage of (Sm\textsubscript{x}Ga\textsubscript{1-x})\textsubscript{2}O\textsubscript{3} grown at a substrate temperature of 100°C and a Sm cell temperature of 550°C. The frequency was 1 MHz.
Figure 6-7. Growth rate and Gallium Concentration as determined by AES in (Sm,Ga_{1-x})_2O_3 grown at a substrate temperature of 100°C as a function of Sm cell temperature.
Figure 6-8. Plot of breakdown voltages for diodes with \((\text{Sm}_x\text{Ga}_{1-x})_2\text{O}_3\) layers grown at a substrate temperature of 100°C as a function of Sm cell temperature.
Figure 6-9. RMS roughness values of (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ layers grown on GaAs at various Sm cell temperatures.
Figure 6-10. AFM images of (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ layer grown at a substrate temperature of 100°C and a Sm cell temperature of 510°C (A), 530°C (B), 550°C (C) 570°C (D).
Figure 6-11. RHEED images of \((\text{Sm}_{x}\text{Ga}_{1-x})_2\text{O}_3\) layer grown at a substrate temperature 300ºC (A) five minutes into oxide growth (B) at the end of oxide growth.
Figure 6-12. XRD scan for \((\text{Sm}, \text{Ga}_{1-x})_2\text{O}_3\) grown at a substrate temperature of 300°C and a Sm cell temperature of 550°C.
Figure 6-13. Surface survey scan for (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ grown at a substrate temperature 300°C and a Sm cell temperature of 550°C taken by AES.
Figure 6-14. Auger depth profile for \((\text{Sm}_x\text{Ga}_{1-x})_2\text{O}_3\) grown at a substrate temperature 300ºC and a Sm cell temperature of 550ºC.
Figure 6-15. AFM image for (Sm\textsubscript{x}Ga\textsubscript{1-x})\textsubscript{2}O\textsubscript{3} grown at a substrate temperature 300\textdegree C and a samarium cell temperature of 550\textdegree C.
Figure 6-16. Current versus voltage characteristics for (Sm$_{x}$Ga$_{1-x}$)$_2$O$_3$ grown at a substrate temperature of 300°C and a samarium cell temperature of 550°C
Figure 6-17. Capacitance versus voltage measurements for (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ grown at a substrate temperature 300°C and a samarium cell temperature of 550°C. The frequency was 1MHz.
Figure 6-18. RHEED images of (Sm\textsubscript{x}Ga\textsubscript{1-x})\textsubscript{2}O\textsubscript{3} growth at a substrate temperature of 500°C (A) streaky pattern taken twelve seconds into oxide growth (B) streaky pattern at the end of growth.
Figure 6-19. XRD scans of (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ grown at Sm cell temperatures of 510ºC (top red curve) and 550ºC (middle black curve) at substrate temperature of 500ºC. The GaAs substrate scan is shown for comparison (bottom green curve).
Figure 6-20. XRD scans of (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ grown at 500°C (green curve), 300°C (red curve), and 100°C (magenta curve) substrate temperatures, respectively (beginning from the topmost curve). The Sm cell temperature was 550°C for all films. XRD scan of a GaAs substrate is shown for comparison (bottom black curve).
Figure 6-21. Surface scan for $(\text{Sm}_x\text{Ga}_{1-x})_2\text{O}_3$ grown at a substrate temperature 500ºC and a Sm cell temperature of 550ºC.
Figure 6-22. Auger data showing spike in Ga concentration at the interface of $(\text{Sm}_x\text{Ga}_{1-x})_2\text{O}_3$ grown at a substrate temperature 500°C and a Sm cell temperature of 550°C.
Figure 6-23. Morphological image of (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ grown at a substrate temperature 500°C and a Sm cell temperature of 550°C.
Figure 6-24. Microstructural data of $(\text{Sm}_x\text{Ga}_{1-x})_2\text{O}_3$ grown at a substrate temperature 500°C and a Sm cell temperature of 550°C.
Figure 6-25. Current versus voltage measurements for \((\text{Sm}_x\text{Ga}_{1-x})_2\text{O}_3\) grown at a substrate temperature at 500ºC and a samarium cell temperature of 550ºC.
Figure 6-26. Capacitance versus voltage measurements for (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ grown at a substrate temperature 500°C and a samarium cell temperature of 550°C.
Figure 6-27. Hysteretic capacitance versus voltage plot taken at 10 kHz of $(\text{Sm}_x\text{Ga}_{1-x})_2\text{O}_3$ grown at a substrate temperature of 500°C and Sm cell temperature of 550°C.
Figure 6-28. Structural characterization of bi-layer (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ oxide stack. The oxide was grown at substrate temperature of 500°C for the first 7.5 minutes of growth and at 100°C for the remaining 22.5 minutes of growth. The Sm cell temperature was 550°C.
Figure 6-29. AFM image of a bi-layer ($\text{Sm}_x\text{Ga}_{1-x})_2\text{O}_3$ oxide stack. The oxide was grown at substrate temperature of 500ºC for the first 7.5 minutes of growth and at 100ºC for the remaining 22.5 minutes of growth.
Figure 6-30. Current versus voltage measurements for a bi-layer (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ oxide stack. The oxide was grown at substrate temperature of 500ºC for the first 7.5 minutes of growth and at 100ºC for the remaining 22.5 minutes of growth.
Annealing in Oxygen

Annealing in oxygen was attempted to oxidize residual Sm metal in the oxide layer revealed by XPS measurements. Sm$_2$O$_3$ and (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ samples were annealed at 500ºC for thirty minutes while being exposed to the oxygen plasma attached to the system.

The ratio of intensities of the oxidized metal peak to the Sm free metal peak increased while the ratio of the intensities of the Sm free metal peak to the oxidized metal peak decreased as a result of post-growth annealing in oxygen of Sm$_2$O$_3$ films (Table 7-1). XRD measurements were taken of sample grown at a substrate temperature of 500ºC before and after annealing at 500ºC for 30 minutes under an O plasma (Figure 7-1). The crystal quality appears to have degraded as a result of annealing with no change in phase distribution. As result of post-growth annealing in O, the RMS roughness value increased from 1.41 nm to 1.56 nm and 0.631 nm to 0.707 nm for Sm$_2$O$_3$ on GaAs grown at substrate temperature of 100ºC and 500ºC respectively. The very sharp peak around 28º degrees is believed to be an artifact due to the polychromatic nature of the x-ray source.

The post-growth annealing of (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ films resulted in an increase in the oxygen to metal ratio but effected no change in the crystalline phase distribution (Figure 7-2, and Table 7-2). The breakdown field was increased from 2.95 MV/cm to 3.37 MV/cm which is consistent with the increase in the oxygen to metal ratio and it seems to indicate a more insulating film as a result of the post-growth annealing. XRD measurements were taken of a sample grown at a substrate temperature of 500ºC and a Sm cell temperature of 550ºC before and after annealing at 500ºC for 30 minutes under an O plasma (Figure 7-2). It appears that the phase distribution was not affected but the crystal quality of the film is degraded as a result of post-growth annealing in
oxygen. The RMS roughness value increased from 1.008 nm to 1.502 nm for Sm$_x$Ga$_{1-x}$O$_3$ on GaAs grown at a substrate temperature of 500ºC.

**Annealing in Forming Gas**

Rapid Thermal Annealing (RTA) of (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ films was conducted under forming gas at 300ºC for forty five seconds. Annealing in a reducing atmosphere should create more dangling bonds by reacting with the oxygen and should result in an increase in the metal to oxygen ratio (Table 7-3). The metal to oxygen ratio increased from 0.161 to 0.249. The hysteretic C-V characteristics taken at 10 kHz was measured (Figure 7-3) and compared to the hysteretic C-V curve taken at 10kHz before annealing in forming gas(Figure 6-27). Since it was determined that annealing in forming gas results in a film with more unbonded metal, Sm$_2$O$_3$ films were not annealed in forming gas.
Table 7-1. XPS peak intensities and their ratios for a Sm$_2$O$_3$ film grown at a substrate
temperature of 100 ºC and 500ºC and a Sm cell temperature of 550ºC before and after
annealing in oxygen.

<table>
<thead>
<tr>
<th>Substrate Temp (ºC)</th>
<th>Ratio of peak intensities (Metal:Oxidized Metal) before annealing</th>
<th>Ratio of peak intensities (Oxidized Metal:Oxygen) before annealing</th>
<th>Ratio of peak intensities (Metal:Oxidized Metal) after annealing</th>
<th>Ratio of peak intensities (Oxidized Metal:Oxygen) after annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>0.296</td>
<td>1.643</td>
<td>0.198</td>
<td>4.078</td>
</tr>
<tr>
<td>500</td>
<td>0.191</td>
<td>2.088</td>
<td>0.128</td>
<td>4.618</td>
</tr>
</tbody>
</table>
Figure 7-1. XRD scans of Sm$_2$O$_3$ on GaAs at a substrate temperature 500°C and a Sm cell temperature of 570°C (growth rate ~ 6Å/min) before and after annealing under an O plasma for 30 minutes at 500°C.
Figure 7-2. A comparison plot of XRD scans of (Sm$_{x}$Ga$_{1-x}$)$_2$O$_3$ on GaAs at a substrate temperature 500°C and a Sm cell temperature of 550°C before and after annealing under an O plasma for 30 minutes at 500°C.
Table 7-2. Oxide, metal, and oxygen XPS peak intensities, ratios of peak intensities, breakdown field, and rms roughness for a film grown at a substrate temperature of 500ºC and a Sm cell temperature of 550ºC before and after annealing in oxygen.

<table>
<thead>
<tr>
<th>Annealing Conditions (ºC, min)</th>
<th>Intensity of oxide peak (counts)</th>
<th>Intensity of Sm metal peak (counts)</th>
<th>Intensity of oxygen peak (counts)</th>
<th>Ratio of peak intensities (Metal: Oxidized Metal)</th>
<th>Ratio of peak intensities (Oxidized Metal: Oxygen)</th>
<th>Breakdown Field (MV/cm)</th>
<th>RMS (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposited</td>
<td>33,236</td>
<td>5,905</td>
<td>7,532</td>
<td>0.178</td>
<td>4.413</td>
<td>2.95</td>
<td>0.99</td>
</tr>
<tr>
<td>500ºC, 30 min</td>
<td>42,291</td>
<td>6,824</td>
<td>8,765</td>
<td>0.161</td>
<td>4.825</td>
<td>3.37</td>
<td>1.50</td>
</tr>
</tbody>
</table>

Table 7-3. List of oxide, metal, and oxygen XPS peak intensities, ratios of peak intensities, breakdown field, and rms roughness for a film grown at a substrate temperature of 500ºC and a Sm cell temperature of 510ºC before and after RTA annealing in forming gas.

<table>
<thead>
<tr>
<th>Annealing conditions (ºC, min)</th>
<th>Intensity of oxide peak</th>
<th>Intensity of free Sm metal peak</th>
<th>Intensity of oxygen peak</th>
<th>M:OM</th>
<th>OM:O</th>
<th>RMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposited</td>
<td>31,332</td>
<td>5041</td>
<td>5746</td>
<td>0.161</td>
<td>5.453</td>
<td>0.591</td>
</tr>
<tr>
<td>RTA Anneal 300ºC 45 sec in H₂: N₂</td>
<td>3038</td>
<td>755</td>
<td>887</td>
<td>0.249</td>
<td>3.425</td>
<td>0.965</td>
</tr>
</tbody>
</table>
Figure 7-3. Capacitance versus voltage measurements taken after annealing in forming gas for (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ grown at a substrate temperature of 500ºC and a Sm cell temperature of 550ºC.
CHAPTER 8
GROWTH AND CHARACTERIZATION OF MANGANESE ARSENIDE

MnAs Growth Procedure and Conditions

Arsenic was supplied by resistive heating of solid arsenic in an effusion oven and by a catalytic-based thermal cracker unit supplied by a bottle of AsH₃ (discussed in Chapter 3). Before creating an As-rich environment, the cryopanels were cooled with LN₂. In the case where a solid source of As was used, the As-rich conditions were created by allowing arsenic to enter the chamber by opening the shutter while the cell was being heated to temperature. As-rich conditions were created with the gas source by establishing a flow of AH₃ in the chamber. The mass spectrometer was used to monitor the conditions in the chamber. After establishing the As-rich conditions in the chamber, the GaN substrates were loaded and thermally cleaned in-situ by a 700°C anneal for five minutes. Then the substrate temperature was cooled to 300°C under As rich conditions for growth. The manganese shutter was opened to initiate growth. Film growth was monitored in-situ by RHEED. The growth rate was varied by adjusting the cell temperature of the manganese \( T_{Mn} \) from 740°C to 820°C, as measured by the cell thermocouple. Films with thicknesses ranging from 15 nm to 400 nm were grown.

MnAs Growth Using AsH₃

MnAs layers were first grown with AsH₃. An injector was used to decompose the hydride gas into its monatomic and diatomic arsenic species, plus H₂ gas. The injector was outgassed for ten minutes at 1100°C before the growth, then cooled to an operating temperature of 1050°C. Two Mn cell temperatures were investigated, 810°C and 815 °C. The XRD data from the sample grown at 810 °C showed a phase distribution consisting of MnAs and Mn₃As (Figure 8-1). The peaks located at 64.82°, 68.22°, and 69.12° are attributed to the Mn₃As (216), Mn₃As (217), and Mn₃As (220) respectively. The MnAs (004) is located at 65.22°. The XRD peak intensity ratio
of the MnAs (004) peak to the Mn₃As (220) was 1.07. The peaks at 66.08° and 65.02° are attributed to the MnAs (202) and Mn₂As (422). The film thickness was 2767 Å and the growth rate was 45 Å/min. The morphology of the film was quite rough, with an RMS value of 11.2 nm as measured by AFM (Figure 8-2). In light of the mixed phases and the rough morphology, it is not surprising that the magnetic properties of this film were found to be rather poor. The Mₛ, remnant magnetization (Mᵣ), and coercivity (Hᵣ) values were 0.89 emu/cm³, 0.12 emu/cm³, and 123 G (Figure 8-3).

XRD measurements of MnAs grown with a Mn cell temperature of 815°C also showed the presence of the Mn₃As and MnAs phases (Figure 8-4). The XRD peak ratio of the MnAs (004) peak to the Mn₃As (220) was only slightly higher than the previous sample at 2.07. The film thickness was 2532 Å and the growth rate was 55Å/min. Also like the previous sample, the morphology appears to suggest a poly-crystalline film with a very rough surface as shown in Figure 8.5 (RMS roughness of 133 nm). In this sample, however, the morphology does appear to indicate a larger grain size. The Mₛ, Mᵣ, and Hᵣ values were higher than for the film grown at the lower cell temperature, at 8.96 emu/cm³, 0.77 emu/cm³, and 72 G (Figure 8-6). As shown in Figure 8-7, higher ratios of the MnAs (004) XRD peak to the Mn₃As (220) typically correlate with improved magnetic properties as one would expect. Thus the improvement in the magnetic behavior of the film with the higher ratio is not surprising. However, though the magnetic properties are improved in this sample, the Ms is still substantially lower than that reported for films grown on GaAs, where an Mₛ value as high as 580 emu/cm³ at 250 Oe has been obtained.¹⁰⁷

**MnAs Growth with a Solid Arsenic Source**

From the work using AsH₃, it was concluded that significantly higher V/III ratios would be needed in order to suppress the formation of the undesirable Mn-rich phases. Due to limitations in the pumping capacity of the system, further increases in AsH₃ flow were not possible. Thus to
increase the As overpressure present during growth an As effusion cell was added to the growth chamber. A set of conditions for optimizing the structural and magnetic properties of MnAs were arrived at by considering the growth conditions that yielded the highest $M_S$ value and XRD peak ratio of MnAs (004) to the Mn$_3$As (220) orientation. The $M_S$ in films grown using solid As was found to depend on the XRD peak ratio of the MnAs (004) to the Mn$_3$As (220) orientations just as was found for films grown using AsH$_3$ (Figure 8-7), however the $M_S$ appears to saturate at a peak ratio of about 3 or higher. Overall, the $M_S$ as well as the XRD peak ratio were both increased substantially relative to the AsH$_3$ grown films. A similar relationship was found between surface roughness as measured by AFM and XRD peak ratio (Figure 8-8). The RMS roughness value was decreased by increasing the XRD peak ratio, indicative of improved crystallinity, and was lower in the samples grown with solid As, further indication of improved crystal quality relative to the films grown with AsH$_3$.

Initial films were grown with a Mn cell temperature of 800ºC and an As cell temperature of 270ºC. The ratio of the MnAs (004) XRD peak intensity to the Mn$_3$As (220) XRD peak intensity was 118. The broad peak at 66.99º is attributed to a less preferred orientation (202) of the MnAs phase. The peak at 70.25º is the Mn$_2$As (220) (Figure 8-9). The $M_S$, $M_R$, $H_C$ of this film was 148 emu/cm$^3$, 85.2 emu/cm$^3$ and 247 G (Figure 8-10). The film thickness was 913 Å and the growth rate was 30 Å/min The area inside the hysteresis loop indicates that this layer was also a hard magnetic material. The surface is rather rough as shown in figure 8.11, though it represents a significant improvement over the films grown with AsH$_3$.

A slightly lower growth rate was explored by using a Mn cell temperature of 795ºC and an As cell temperature of 260ºC. Both cell temperatures were decreased in an attempt to keep the V-III ratio roughly constant. In this case, the XRD intensity ratio of the MnAs (004) and Mn$_3$As
(220) peaks was 166 (Figure 8-12), a significant improvement over the film grown with a higher growth rate. Similarly, the morphology was substantially improved as well, as shown in figure 8-13, with an RMS roughness of 1.6 nm. SQUID measurements revealed a hysteresis loop with high remnant magnetization and coercive field which indicated the hard magnetic nature of the film (Figure 8-14). The maximum $M_S$ of this film was measured to be 276 emu/cm$^3$ with a coercivity ($H_C$) of nearly 383 G (Gauss). The remnant magnetization ($M_R$) was 182 emu/cm$^3$. The film thickness was 1408 Å and the growth rate was 31 Å/min.

Given the improvement obtained in the previous experiments by increasing the V-III ratio and reducing the growth rate, the final experiment employed a Mn cell temperature of 740ºC and an As cell temperature of 300C. These conditions were expected to yield the highest XRD peak ratio of the MnAs (004) to the Mn$_3$As (220); however the peak ratio was only 2.86 (figure 8-15). Despite the low XRD peak ratio, the $M_S$ was 289 emu/cm$^3$. The $M_R$ and $H_C$ were 103 emu/cm$^3$ and 135 G (Figure 8-16). Magnetization (M) versus temperature measurements reveal a $T_C$ of 315K which is in good agreement with the previously reported value of 318 K$^{53}$ (Figure 8-16). The film thickness was 113 Å and the growth rate was 2.5 Å/min. The surface morphology was the smoothest obtained in this study, with an RMS roughness of 1.3 nm (Figure 8-18). To investigate the interfacial region of this film, a high resolution TEM image of 113 Å thick MnAs thin film on a GaN substrate (Figure 8-19). Evidence of atomic registry can be seen at the interface, though the MnAs film is clearly divided into two regions. Energy Dispersive Spectroscopy (EDS) data (Figure 8-20) indicates that the 2.2 nm layer closest to the GaN is Mn-rich. The presence of an interfacial layer is in agreement with the RHEED data taken during growth which showed a change from streaky to spotty after initial nucleation. Presence of this layer would also explain the multiple phases observed by XRD. Given the poor magnetic properties of Mn-rich MnAs, it is reasonable to assume that spin injection across this interface
would be difficult at best. Thus even though the films deposited in this study appear to be of high quality at some distance from the interface, it is unlikely that efficient spin injection is achievable using this approach.
Figure 8-1. MnAs grown at a substrate temperature of 300ºC, a manganese cell temperature of 810ºC and an arsine injector temperature of 1050ºC. The AsH₃ flow rate was 10 sccm.
Figure 8-2. AFM image of MnAs grown at a substrate temperature of 300°C and a manganese cell temperature of 810°C and an arsine injector temperature of 1050°C.
Figure 8-3. Hysteresis of MnAs grown at a substrate temperature of 300°C and a manganese cell temperature of 810°C and an arsine injector temperature of 1050°C.
Figure 8-4. XRD scan of MnAs grown at a substrate temperature of 300ºC, a manganese cell temperature of 815ºC an arsine injector temperature of 1050ºC.
Figure 8-5. Surface characterization by AFM of MnAs grown at a substrate temperature of 300°C and a manganese cell temperature of 815°C and an arsine injector temperature of 1050°C.
Figure 8-6. Magnetic characterization by SQUID of MnAs grown with 300°C, a manganese cell temperature of 815°C and an arsine injector temperature of 1050°C
Figure 8-7. Saturation magnetization ($M_S$) vs. Ratio of (004) MnAs peak with the Mn$_3$As (220) XRD peak plot of MnAs grown at different V-III ratios. Solid squares were obtained from samples grown with AsH$_3$. Open squares were derived from solid As.
Figure 8-8. RMS roughness versus ratio of the (004) MnAs XRD peak with the (220) Mn$_3$As XRD peak plot of MnAs grown at various V-III ratios.
Figure 8-9. Structural characterization of MnAs grown at a substrate temperature of 300°C and a manganese cell temperature of 800°C and an As cell temperature of 270°C.
Figure 8-10. Hysteresis of MnAs grown at a substrate temperature of 300ºC, a manganese cell temperature of 800ºC and an As cell temperature of 270ºC.
Figure 8-11. AFM image of MnAs grown at a substrate temperature of 300°C and a manganese cell temperature of 800°C and an As cell temperature of 270°C.
Figure 8-12. Structural characterization by XRD of MnAs grown at a substrate temperature of 300°C with a manganese cell temperature of 795°C and an As cell temperature of 260°C.
Figure 8-13. Morphology of MnAs grown at a substrate temperature of 300°C and a manganese cell temperature of 795°C and an As cell temperature of 260°C.
Figure 8-14. SQUID data of MnAs grown at a substrate temperature of 300ºC and a manganese cell temperature of 795ºC and an As cell temperature of 260ºC.
Figure 8-15. MnAs grown at a substrate temperature of 300°C, a manganese cell temperature of 740°C and an As cell temperature of 300°C.
Figure 8-16. Hysteresis curve of MnAs grown at a substrate temperature of 300ºC, a manganese cell temperature of 740ºC and an As cell temperature of 300ºC.
Figure 8-17. Magnetization versus temperature plot of MnAs grown at a substrate temperature of 300°C and a manganese cell temperature of 740°C and an As cell temperature of 300°C.
Figure 8-18. AFM image of MnAs grown at a substrate temperature of 300°C and a manganese cell temperature of 740°C and an As cell temperature of 300°C.
Figure 8-19. HRTEM image of MnAs grown at a substrate temperature of 300°C with a manganese cell temperature of 795°C and an As cell temperature of 260°C.
Figure 8-20. Energy Dispersive Spectroscopy (EDS) data showing an increase in Mn concentration near the interface of MnAs/GaN heterostructure.
Conclusions and Suggestions for Future Work with Sm$_2$O$_3$ Growth on GaAs

GaAs surface cleaning by ex-situ etching with a solution of H$_3$PO$_4$ : H$_2$O (3:80) for 90 seconds and then an in-situ exposure time of 20-30 minutes with a hydrogen plasma is very effective for reproducing a clean GaAs surface under vacuum. Sm$_2$O$_3$ growth at a high temperature (500ºC) yields single crystal films. Sm$_2$O$_3$ growth at low temperature (100ºC) yields amorphous films. Electrical testing of Sm$_2$O$_3$/GaAs diodes show good breakdown fields (3.9 MV/cm) with good capacitance versus voltage behavior ($D_{it}$). Growth of the ternary compound Sm$_x$Ga$_{1-x}$O at 500ºC yields polycrystalline films with a crystalline interfacial layer of approximately 65 Å. Some evidence of Ga segregation at the interface was observed with AES depth profiling. Similar growth at 100C produced films which were amorphous. A significant amount of Sm free metal was also observed in all of these films. In spite of this, breakdown fields as high as 4.35 MV/cm were achieved. Higher growth temperatures produced better CV behavior. Overall however the best leakage currents were obtained in the pure Sm$_2$O$_3$.

Post-growth annealing under an oxygen plasma in the MBE system was successful in oxidizing some of the unbonded Sm metal. However it was not successful in changing the phase composition from a mixture of monoclinic and cubic oxide to one of pure cubic phase. Annealing in an RTA under forming gas did not improve the electrical properties of the material and in fact increased the amount of unbonded Sm metal in the oxide. The leakage current as a function of the breakdown field was compared for films grown under all growth conditions (Figure 9-1). It was determined that the binary oxide grown at 100ºC exhibited the best electrical properties in terms of breakdown field. Ternary oxides grown at 500ºC showed the best CV behavior (Figure 9-2). Future work on this material system should focus on further reducing the
unbonded metal in the oxide which should lead to improved electrical behavior. In its present form, the oxide should be adequate for use as a field plate, but needs further optimization to be useful as a gate dielectric.

**Conclusions and Suggestions for Future Work with MnAs Growth on GaN**

Growth of MnAs on GaN requires a high V/III ratio in the chamber during growth to suppress the formation of Mn-rich compounds. It appears that once a critical thickness is reached the MnAs phase nucleates with improved crystallinity. $M_S$ and rms values were markedly improved by increasing the MnAs (004) to Mn$_3$As (220) XRD peak ratio. These results indicate that the structural and magnetic properties of the MnAs/GaN system strongly depend on the V/III ratio in the chamber during growth. Future experiments should focus on eliminating the interfacial layer which is composed of elemental Mn and Mn-rich compounds such as Mn$_3$As and Mn$_2$As.
Figure 9-1. A comparison plot of the leakage current versus the breakdown field for the Sm$_2$O$_3$ bilayer oxide, Sm$_2$O$_3$ and (Sm$_x$Ga$_{1-x}$)$_2$O$_3$ at substrate temperatures of 100ºC and 500ºC.
Figure 9-2. Family of C-V curves taken at different frequencies for (Sm₉Ga₆₋ₓ)₂O₃ grown at a substrate temperature of 500°C and Sm cell temperature of 550°C.
APPENDIX A
ANALYSIS OF CV CURVES

CV curves

The measured capacitance of a MOS capacitor consists of two capacitors in series. The capacitors include a voltage-independent gate oxide capacitor and a voltage-dependent semiconductor capacitance. In accumulation, the series capacitance is represented by the oxide capacitance shown in Equation A-1:

$$C_{ox} = \frac{\varepsilon_{ox} \varepsilon_o}{t_{ox}}$$

(A-1)

where $C_{ox}$ is the capacitance of the oxide (measured in F/cm$^2$), $\varepsilon_{ox}$ is the dielectric constant of the oxide, $\varepsilon_o$ is the permittivity of free space ($8.854 \times 10^{-14}$ F/cm), and $t_{ox}$ is the thickness of the oxide film (measured in cm).

In depletion, the semiconductor surface becomes depleted of majority carriers under the applied gate bias (holes are depleted in p-type material with increasing gate voltage and electrons are depleted in n-type material with decreasing gate voltage), causing a decrease in the measured capacitance. The overall capacitance is now represented by the series connection of the oxide capacitance ($C_{ox}$) and depletion layer capacitance ($C_d$) seen in Equation A-2:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d}$$

(A-2)

Under strong inversion, minority carriers are generated in the bulk and then drift across the depletion region to form a surface layer charge. However, this will only occur if a low frequency (100 kHz) is applied and if the gate bias is changed slowly. The low frequency and slow changing gate bias allow the minority carriers enough time to respond to the ac probe frequency.
and dc voltage signal. The overall capacitance is now represented by the oxide capacitance once again (Figure A-1a).

For high frequency (1MHz) measurements at slow changing gate bias, the minority carrier generation rate is too low as the carriers do not have enough time to respond to the ac voltage signal. The semiconductor depletion layer capacitance is now at a minimum, corresponding to a maximum depletion width. The overall capacitance is also at a minimum and is represented by the series capacitance of the oxide and the semiconductor depletion layer (Figures A-1b and A-2). For high or low frequency measurements at a large gate bias sweep rate, the generation rate of minority carriers is too low and the measured capacitance can go into deep depletion (Figure A-1c).

**D\text{it} Calculations**

The frequency and gate bias sweep rate can have a significant effect on the response of interface states at the oxide/semiconductor interface. As the applied gate bias changes, the surface potential of the MOS device changes, which causes the interface states (whose positions with respect to the band edges are fixed) in the band gap to move above or below the Fermi level. Since energy levels below the Fermi level have a higher probability of occupying an electron, an interface state moving above the Fermi level would likely give up a trapped electron (or equivalently capture a hole) while an interface state moving below the Fermi level would likely capture an electron (or give up a hole). The stored charge from the interface states gives rise to a capacitance which is in series with the depletion layer capacitor (the combination of the two would be in series with the oxide capacitance). At very high (~1 MHz) frequencies, the interface states do not have time to respond. At low (~1–100 Hz) frequencies and/or low gate bias sweep rates, the interface states can respond quickly to the voltage changes and follow the ac probe frequency. The Terman method was used to calculate the D\text{it} value from the measured
CV data. The method relies on measurements taken at sufficiently high frequencies in which interface traps do not respond. Although the interface traps do not respond to the ac probe frequency, they do respond to slow gate bias sweep rates. As the interface trap occupancy changes with gate bias, the CV curve stretches out along the gate axis (change in slope of real CV curve from ideal curve. The total theoretical capacitance is given by the series capacitance of the oxide and semiconductor. To calculate the theoretical semiconductor capacitance (C_s), the semiconductor flatband capacitance (C_{FBS}) is calculated from Equation A-3:

\[ C_{FBS} = \frac{\varepsilon_s \varepsilon_0}{L_D} \]  

(A-3)

where \( C_{FBS} \) is the semiconductor flatband capacitance (in F/cm²), \( \varepsilon_s \) is the dielectric constant of GaAs (12.85), \( \varepsilon_0 \) is the permittivity of free space (8.854x10^{-14} F/cm), and \( L_D \) is the Debye length (in cm). The Debye length is calculated from Equation A-4:

\[ L_D = \sqrt{\frac{k_B T \varepsilon_s \varepsilon_0}{q^2 N}} \]  

(A-4)

where \( L_D \) is the Debye length (in cm), \( k_B \) is Boltzmann’s constant (1.38x10^{-23} J/k), \( T \) is the temperature (in K), \( \varepsilon_s \) is the dielectric constant of GaAs (12.85), \( \varepsilon_0 \) is the permittivity of free space (8.854x10^{-14} F/cm), \( q \) is the hole or electron charge (1.6x10^{-19} C), and \( N \) is the effective carrier density (in cm^{-3}). The effective carrier density can be calculated from Equation A-5:

\[ N = \frac{2}{q \varepsilon_s \varepsilon_0 A^2} \left[ \frac{1}{\partial (1/C^2) / \partial V} \right] \]  

(A-5)

where \( N \) is the effective carrier density (in cm^{-3}), \( \varepsilon_s \) is the dielectric constant of GaAs (12.85), \( \varepsilon_0 \) is the permittivity of free space (8.854x10^{-14} F/cm), \( q \) is the hole or electron charge (1.6x10^{-19} C).
A is the area of metal gate (in cm), and $\partial(1/C^2)\partial V$ is the slope of the experimental $1/C^2$ vs. $V_g$ plot.

After calculating the flatband capacitance of the semiconductor, the theoretical semiconductor capacitance can be calculated from Equation A-6:

$$C_s = 2^{-0.5} \text{Sgn}(V)C_{\text{FBS}} \left( e^V - I \right)^{-0.5} \left( - (V + 1) + e^V \right)^{-0.5}$$

(A-6)

where $C_s$ is the semiconductor capacitance in (F/cm$^2$); $V$ is the non-dimensional band bending (in V); $\text{Sgn}(V)$ returns a value of 1 for positive values of $V$, 0 for a value of 0 for $V$, and -1 for negative values of $V$; and $C_{\text{FBS}}$ is semiconductor flatband capacitance (in F/cm$^2$). The nondimensional band bending is used in Equation A-7 to calculate the surface potential:

$$\phi_s = \frac{k_BVT}{q}$$

(A-7)

where $\phi_s$ is the surface potential (in eV), $k_B$ is Boltzmann’s constant (8.62x10$^{-5}$ eV/K), $V$ is the non-dimensional band bending (in V), $T$ is the temperature (in K), and $q$ is the hole or electron charge (1.6x10$^{-19}$ C).

After constructing the theoretical curve by plotting the theoretical total capacitance vs. the surface potential, a surface potential value is found for a given capacitance value. The gate voltage from the experimental curve is then found for the same capacitance value. Repeating the procedure for other points allows an $\phi_s$ vs. $V_g$ curve to be constructed. The $D_{it}$ can be determine from this curve using Equation A-8:

$$D_{it} = \frac{C_{\alpha}}{q} \left[ \frac{\partial V_g}{\partial \phi_s} - 1 \right] - \frac{C_s}{q}$$

(A-8)
where $D_{it}$ is the interface state density (in eV$^{-1}$ cm$^{-2}$), $C_{ox}$ is the oxide capacitance (in F/m$^2$), $q$ is the hole or electron charge ($1.6 \times 10^{-19}$ C), $V_G$ is the gate bias (in V), $\phi_s$ is the surface potential (in eV), and $C_s$ is the surface capacitance (in F/m$^2$).

**$V_{FB}$ Determination**

For an ideal MOS capacitor, the metal and semiconductor work functions are equal at a gate bias of 0 V. However, in a real MOS capacitor, there is typically a metal-semiconductor work function ($\Phi_{MS}$) difference and oxide and interface charges that produce a flatband voltage ($V_{FB}$) shift (parallel shift of real plot from ideal plot is seen in Figure A-3). The flatband voltage is the voltage required to achieve the flat band condition where the energy bands are flat. A negative flatband voltage shift indicates a positive oxide charge that induces an equivalent negative charge in the semiconductor. A positive flatband voltage shift indicates a negative oxide charge that induces an equivalent positive charge in the semiconductor.

To determine the flatband voltage shift, the theoretical CV curve must be compared to the experimental CV curve. The first step is to locate the normalized theoretical capacitance ($C/C_{ox}$) at a gate bias of 0 V. The same value is then located on the normalized experimental capacitance curve with the corresponding gate bias value. This gate bias value represents the flatband voltage of the MOS capacitor. Another method that can be used to determine the flatband voltage shift experimentally includes plotting $1/(C_{it})^2$ vs. $V_G$. The gate bias at the lower knee of the curve represents the flatband voltage$^{2,3}$. 
LIST OF REFERENCES


BIOGRAPHICAL SKETCH

Anthony Duane Stewart was born in Baton Rouge, Louisiana. He is the son of Jackie Barrett and Ronald Stewart and brother to Kirby Stewart. He graduated from high school as the valedictorian of his class in 1995. Then, as an honor student, he attended Southern University and A&M College in Baton Rouge, Louisiana. He earned the BS degree with honors (magna cum laude) in 1999. During his undergraduate work, he was fortunate to be a part of a mentoring and research participation program, where he was exposed to scientific research. He then matriculated at the University of Florida in pursuit of the doctoral degree in materials science under the supervision of Dr. Rolf Hummel in 2000. After successful completion of the qualifying examination, he began doing research with gate dielectrics under Dr. Cammy Abernathy. He completed the doctoral degree in December of 2008. Post graduation plans are to pursue employment as a research engineer.