BROADBAND BALUN AND PHASE NOISE MEASUREMENT SYSTEM DESIGN FOR RFIC TESTING

By

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To my Wife, Youn Pil Jeong
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<td>FGBC-CPW</td>
<td>Finite Ground Broadside Coupled Coplanar Waveguide</td>
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<tr>
<td>FGBC-CPS</td>
<td>Finite Ground Broadside Coupled Coplanar Strips</td>
</tr>
<tr>
<td>CPW</td>
<td>Coplanar Waveguide</td>
</tr>
<tr>
<td>CPS</td>
<td>Coplanar Stripline</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>FM</td>
<td>Frequency Modulation</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced Design System</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<td>HFSS</td>
<td>High Frequency Structural Simulation</td>
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<td>PLL</td>
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This research mainly focuses on test cost reduction for RF ICs. First, differential circuit measurements with a two port network instrument are discussed. Many companies and academic researchers use a four port instrument to measure their differential RF chips. This is the simple and accurate method, however, the test instruments are very expensive compared to a two port instrument, especially for high frequency (>20GHz) system. Alternative method is using balun to convert the differential signal into a single-ended signal, and then measures it with a two port instrument. This method can save the cost of the expensive instruments but need at least 6 different test setups. The time is another test part of test cost. By integrating the balun in a RF differential probe, the measurement can be simplified with a two port instrument. Second, for building a balun integrated probe, a new analysis is introduced for the Marchand balun. The new method takes the termination impedance variation into account. Third, a new closed form equation based on conformal mapping method for extracting the broadside coupled transmission line, is introduced and verified with FEM method. Fourth, a balun integrated probe is designed, fabricated, and measured in Cascade probe technology. Finally, the embedded test system or Built-in Self Test (BIST) for the phase noise is discussed. Testing and verification of the RF and microwave components are major parts of the total test cost. Over the years, various methods
have been studied for reducing the test cost. A new method is an on-wafer phase noise measurement which is a very economical method while keeping a high level accuracy. Through the noise and system analysis, the proposed system specifications are determined and implemented in IBM8HP technology. Measurement indicates better performance than the commercial external systems up to 1.5GHz.
CHAPTER 1
INTRODUCTION

1.1. Introduction to RFIC Test

Wireless communication devices, among the semiconductor industry’s most high volume products, are subject to a continually growing number of standards and applications. In today’s competitive market, incorporating a comprehensive testing strategy into a wireless module’s design flow is indispensable to its timely development and economic success [1.1][1.2]. Modern wireless transceivers and receivers are highly integrated systems. Their diverse specifications and components and high frequencies of operation make testing them complex and expensive. Increasing the effectiveness and cost efficiency of analog and RF tests in integrated systems is a complex problem that researchers have addressed at various levels. Recent efforts include defect modeling, automated test algorithms, alternate tests for system specifications, DFT techniques [1.3] and BIST techniques [1.4][1.5][1.6] due to high cost Automatic Test Equipment (ATE) for RF/microwave circuits.

As shown in Figure 1-1, the test cost issue was predicted in the 97’ SIA roadmap in which test capital per transistor was expected to exceed the silicon capital cost. The portion of the test cost in semiconductor manufacturing can not be ignored because of ever-increasing complexity of tests. Although analog and RF circuitry has far fewer transistors than digital circuitry in most modern system-on-chip (SOC), analog and RF circuits require the use of complicated test procedures, increasing the test time and the cost of automatic test equipment (ATE). As a result, the test cost of modern mixed-signal SOC can be as high as 30% of their manufacturing cost [1.7].
A key contributor to the test cost is the cost of external ATE and its interface to the device under test (DUT). Figure 1-2 gives an idea of how basic ATE test cost increase when incorporating mixed signal and RF options to it. In order to reduce the complexity and external ATE cost and its interface to DUT, it is desirable to move some testing function to the test board and into the device under test (DUT) itself.
In the past 30 years, wafer probing above a GHz has progressed to a mainstream very large scale integration (VLSI) topic. With the development of high performance and high frequency on-wafer probes and probe stations, wafer-level test and characterization can be performed before ICs were diced and packaged. Current RFIC testing methodologies require performance-based measurement (i.e. using external instruments), and the complexity of applications increases the number of instruments in a given test system [1.8]. Extremely complex, million-dollar automated test equipment (ATE) systems that integrate all of the functions and provide a much higher throughput capability than typical rack-and-stack equipment have now become readily available from numerous vendors. This trend of increasing instrument numbers, complexity and performance is expected to continue.

1.2. The Test Cost Reduction Method

Conventional test methods use external testers to generate test stimulus and the DUT response is directly measured from the stimulus. High-bandwidth data transfer is done at the operational speed of the DUT. The measurement results include the transmission properties of the interconnection, such as wires, connectors, probe cards path. Extra effort and cost to decouple the response of the interconnection from the actual response of the DUT are needed to ensure accurate measurement results.

Figure 1-3 A) shows a conventional test setup to measure a DUT. The measurement instruments have high cost and the interfaces between the instrument and DUT have high cost as well. Figure 1-3 B) presents one of methods for reducing the test cost [1.9]. This method is proposed to measure the differential circuitry which generates differential signals. By combining and converting the differential signal into a single-ended signal, the number of high-cost interfaces can be reduced and the differential instruments for RF test can be replaced with a cheap instruments such as 2-port network analyzer. Usually, a 4-port instrument like a 4-port
network analyzer is much more expensive than a 2-port instrument like a 2-port network analyzer. Figure 1-3 C) shows that the integration of embedded test circuitry into a DUT, results in a new on-chip and off-chip distribution of test resources compared to conventional test resource partitioning. Embedded test integrates the capability of the high-speed and the high-bandwidth portion of the external ATE circuits directly into the DUTs. With these embedded circuits, high-speed test stimulus and response signature generation functions can be customized as required per test application type, and on-chip test data compression reduces ATE data requirements.

1.3. Challenges and Approach in wafer-level RF Test

Much research has been performed in the effort to reduce test cost, but, many challenges still exist. For the balun integrated probe for differential circuit measurement as shown in Figure 1-3 B), the availability of balun integrated probes is very limited due to the lack of frequency range. Prior to this work, the available balun integrated probes only covered the 10GHz operational range in external board-level implementations [1.9] or with coaxial baluns [1.10]. Since a high frequency (> 20GHz) instrument costs much higher than that of the instrument (<20GHz), the high frequency balun over 20GHz needs to be developed to provide test cost reduction.

Embedded test can improve test coverage at internal nodes in a complex system-on-a-chip (SOC) and reduce the use of high-cost equipments as well. Up to date, many RF building blocks such as the low noise amplifier (LNA) [1.11][1.12] and the power amplifier (PA) [1.13], can be measured using embedded test circuitry. However, the embedded characterization of VCO or PLL blocks has not been researched as much as the amplifier gain blocks are. Particularly, the embedded phase noise characterization of a VCO is incomplete compared with the other RF building blocks.
Figure 1-3. Evolution from A) conventional test with high-cost ATE B) test with balun probe C) embedded test with low-cost ATE
1.4. Study Overview

This thesis focuses on reducing the overall cost for testing RFICs. The test cost reduction approach in this work mainly consists of two methods. The first approach is to reduce the number of the high cost interfaces to the DUT by designing balun integrated RF/microwave probes. Chapter 2 briefly introduces the concept of differential signal and the differential circuit measurement using a conventional 2-port VNA, and not using an expensive 4-port VNA. Chapter 3 introduces a new Marchand balun analysis for finding the design parameters. Chapter 4 and 5 explains design methods for balun integrated RF/microwave probes. The second approach is to build the embedded test circuitry next to an RF circuit for converting the high cost test signal into the low cost test signal. Chapter 2 introduces Built-In-Self-Test (BIST) and past work done by other researchers. Chapter 6 shows the theoretical background for an embedded phase noise measurement system. Chapter 7 shows the circuit implementation and Chapter 8 shows measurement results for embedded phase noise measurement system.
CHAPTER 2
BACKGROUND TO THIS WORK

2.1. Introduction to Differential Circuit

The use of differential circuit topologies is becoming increasingly common in a wide range of microwave/RF applications. Differential circuits have excellent immunity to many noise sources that are generated from power supplies, adjacent circuitry and other external sources that are electrically or electromagnetically coupled [2.1]. Generally, the nature of signal propagation is taught in terms of “single-ended” modes. The “single-ended” mode is distinguished from two other types of signal propagation, differential mode and common mode. Differential mode signals propagate through a pair of traces. One trace carries the signal as we normally understand it, the other carries a signal that is exactly equal and opposite, ideally. Differential and single-ended modes are not quite as different as they may initially appear. All signals have a return, typically the zero-voltage, or ground. Each side of a differential signal would return through the ground circuit, except that since each signal is exactly equal and opposite, the returns simply cancel. Therefore, there is no ground path cancel Common-mode refers to signals that occur on both traces of a differential signal pair or on both the single-ended trace and ground. Common mode signals are most often generated by spurious conditions within a circuit or coupled into a circuits from adjacent or outside sources. Common-mode signals are almost always undesirable and many of current circuit and board design rules are created to prevent them from occurring [2.2][2.3].

Single-ended signals are compared to some kind of “reference” level such as the positive or ground voltage, device threshold voltage, or another signal somewhere on the circuit. On the other hand, a differential signal is referenced only to its port pair. That is, a logical state occurs if
the voltage on one trace is sufficiently higher than on the other trace. Differential signals have several advantages compared to single-ended signals.

- Timing is much more precisely defined because it is easier to control the crossover point on a signal pair than it is to control an absolute voltage relative to some other reference. If the traces are not equal length (the signals arrive at different times at the ends), common-mode noise might result which cause signal timing and EMI issues.

- Differential circuits can normally operate at higher speeds than comparable single-ended circuits since they reference no other signals than themselves. The timing of signal crossover can be more tightly controlled, and the voltage can be greatly reduced.

- The result net signal is twice as large compared to ambient noise since differential circuits react to the difference between the signals on two traces. Therefore, differential signals, all other things equal, have greater signal to noise ratios and performance.

### 2.2. Differential Circuit Measurement

For efficient measurement of a differential circuit without engineering overhead [2.3], a new method was proposed [2.2]. This method uses baluns in order to measure the differential circuit, by which measurement steps greatly are reduced and the measurement setup time also is saved. Figure 2-1 shows the basic concepts of this method. In general, a 4-port equipments is always more expensive than 2-port counterparts. If one measures a differential circuit with 2-port equipment, one must measure it through 6 independent steps. All the steps need different test setup [2.2]. In particular, if on-chip measurement is required for the device-under-test (DUT), the test setup becomes more complicated. However, the number of measurement steps can be reduced by using baluns. Previous research developed a relatively low frequency RF probe embedded probe, which uses separate baluns to connect the DUT ports and coaxial cable for equipment connection [2.2]. In this work, baluns are integrated on a microwave probe structure directly. By integrating the balun on this thin film structure, the balun can operate at very high frequency. Until the operation frequency reaches the cutoff frequency of the transmission line.
structure, the balun can operate. Through designing, implementing and measuring the balun integrated probe, test cost can be reduced compared to using a 4-port network analyzer.

Figure 2-1. Differential system test methods with A) conventional 4-port measurement B) 2-port measurement using baluns.

### 2.3. Baluns

A balun is a device which converts a balanced impedance (differential signal) to unbalanced impedance (single-ended signal) and vice versa. In addition, baluns can also provide impedance transformation, hence the name Balun Transformers. Coaxial cable, microstrip and CPW lines are examples of unbalanced transmission lines, while a two wire transmission line is an example of balanced transmission line as shown in Figure 2-2. Two conductors of the same geometry having equal potential with 180° phase difference constitute a balanced line. When this condition is not satisfied, the transmission line is termed as unbalanced as shown in Figure 2-2 B) (i.e, I₁≠I₂ and I₉≠0) in this case I₉ is finite and flows through the outer side of the grounded shield, since there is also potential voltage at the outer conductor [2.4].
Baluns are required for such circuits as balanced mixers, push-pull amplifiers, balanced frequency multipliers, phase shifters, balanced modulators, and dipole antenna feeds. Several different kinds of balun structures have been developed, such as the coaxial cable baluns, lumped-element baluns, active baluns and Marchand-type baluns. In this work, the focus was on building a planar Marchand balun performing at 60GHz operation for high frequency differential circuit measurements.

There are several types of transmission line based balun topologies. In this section, it is shown how to choose the balun topology for integrated balun probes.

The Marchand balun is one of the most commonly used components in broadband balanced circuit design. As compared with other balun topologies, the Marchand balun structure when implemented using couplers will have a less strict requirement for $Z_{0e}$ (even mode characteristic impedance) [2.4]. To obtain a balun with good performance, it is sufficient to have
$Z_{0e} = 3$ to $5$ times larger than $Z_{0b}$ (odd mode characteristic impedance) [2.5]. A wide bandwidth balun can be obtained by proper selection of the balun parameters. Figure 2-3 shows the original Marchand balun [2.5], which consists of an unbalanced, an open-circuited, and two short-circuited and balanced transmission line sections and equivalent transmission line model.

Figure 2-3. Marchand compensated balun A) Coaxial cross section B) Equivalent transmission line model.

In this work, the Marchand balun is implemented on a microwave/RF probe membrane thanks to its simplicity and potential for wide bandwidth operation. A new Marchand balun analysis is proposed in order to build $1:1$ to $1:4$ impedance transformations with the best achievable response. Through the proposed analysis, a simple design equation is constructed depending on the specific application. Chapter 3 discusses the proposed Marchand balun analysis and Chapter 4 and 5 show an actual balun implementation by using broadside coupled lines on the microwave/RF probe membrane.

2.4. Introduction to Embedded Testing

Traditionally, RF design and silicon manufacturing have contributed the highest overall IC manufacturing cost component, thus the test costs received little attention. Improvements in
manufacturing technology, and relaxed performance requirements of some application domains, lead to high-yield low-area design processes; the cost of manufacturing RF dies has reduced appreciably. However, the test cost has not reduced at the same rate, and indeed has been an increasing percentage of the overall IC manufacturing cost. The first high-volume microwave chip tests were relatively simple, and included the tests of switches, amplifiers, mixers, LNA/mixer combinations, etc. Wafer level tests were used to prune away catastrophically defective dies before packaging and the RF path was completely by-passed in the wafer level test. As IC complexities have increased, the yields are improved, the package costs become an appreciable component of the overall cost, and the need for wafer level RF path test before packaging has arisen. Since 1999, there has been a steady increase in the number of high volume RFICs that are tested on-wafer instead of being tested at package level. In addition, RFIC systems are being built with advanced packages by which require known-good-die (KGD) which are pre-tested. With the development of high-performance and high-frequency on-wafer probes and probe stations, wafer-level test and characterization can be performed before ICs are diced and packaged. Conventional analog/RF IC tests use ATE (automated test equipment) systems. However, the cost associated with ATE systems has significant impact on the total manufacturing test cost. The complexity of the test systems needs to be matched to the complexity of the ICs to be tested and generally the cost of ATE system is proportional to the complexity of the device to be tested. Also, ATE systems are costly to operate and require a complicated test procedure development, which makes the situation even worse [2.6].

In order to overcome the problems mentioned earlier, embedded test is a potential new solution. For example, digital BIST (built-in-self-test) circuits allow lower cost ATE testers to evaluate the quality of the device [2.7]. Since the DUT tests itself using BIST, it lowers the test
cost a lot by requiring less expensive ATE tests. Unfortunately, analog/RF BIST technology has always lagged behind digital BIST due to the required high accuracy of signals generated and measured on chip. Particularly, conventional test methods use external testers to generate test stimuli and the DUT response is directly measured from the stimuli. Thus, the measurement results include all the possible parasitic effects such as the interconnection coupling, transmission properties and matching conditions. However, the integration of embedded test circuitry into the DUTs results in a new on-chip and off-chip distribution of test resources compared to the conventional methods [2.8].

The embedded testing circuits communicate with the ATE through a low-rate digital data interface or DC voltages. Figure 2-4 illustrates an example of an RF BIST concept. From the extracted information at different intermediate stages, catastrophic and parametric faults can be detected and located [2.9].

![Low-cost test of an integrated transceiver through on-chip test circuitry](image)

A loop-back connection between the transmitter and receiver chains is one of the earlier strategies to test the functionality of RF systems [2.10]. On-chip implementation of this technique have been demonstrated [2.11][2.12]. This approach does not require external stimuli
and it is effective in detecting catastrophic faults in the complete signal path. Also, several parametric embedded tests have been proposed for BIST. For example, the center frequency and bandwidth of RF circuits-under-test (CUT) were extracted using a step input signal on chip [2.13]. The noise figure (NF) and the input referred third-order interception point (IIP3) of the DUT were estimated using machine-learning (ML) based methods [2.14][2.15].

Phase noise or jitter performance of a PLL is one of the most critical design parameters in RF systems. While phase noise measures the inaccuracy of a signal source in the frequency domain, jitter shows the clock edge uncertainty in the time domain. Several on-chip schemes that directly measure jitter in the time domain have been proposed [2.16][2.17][2.18]. These schemes are based on time interval analysis, and therefore are limited by the purity of the reference clock and gate delay resolution of the given technology. Phase noise can be a critical parameter that characterizes the RF, analog and digital sources. Timing jitter can be measured indirectly from phase noise by integration of the noise spectrum over a specified frequency range. Generally, phase noise measurement has been limited to off-chip methods, using spectrum analyzers or phase noise analyzers [2.19].
CHAPTER 3
MARCHAND BALUN ANALYSIS

3.1. Introduction to Marchand Baluns

The Marchand balun may be one of the most popular forms of microwave balun used to generate a balanced signal. In particular, the planar coupled-line Marchand balun shows good compatibility with microwave circuits (MIC) and monolithic MICs (MMIC) [3.1]. Numerous studies about its design and analysis have been performed since it was first introduced in 1944 [3.2]. Most designs, however, emphasize maximum power transfer to the balanced load within a specified passband using a quarter wave transmission line equivalent circuit.

A wide bandwidth balun can be obtained by proper selection of the balun parameters. Figure 3-1 (a) shows the original Marchand balun [3.2], which consists of an unbalanced, an open-circuited, and two short-circuited and balanced transmission line sections.

3.2. Basic Operation of Marchand Baluns

The balun basically consists of an unbalanced, an open-circuited, two short-circuited, and balance transmission line sections. Each section is about a quarter-wavelength long at the center frequency of operation. A coaxial version of a compensated Marchand balun is shown in Figure 3-1 A), while its equivalent circuit representation is shown in Figure 3-1 B). The compensation term is used in broadband baluns where the balanced output and reduced phase slope are maintained over a wide bandwidth. As shown in Figure 3-1 A) [3.2], this structure basically consists of two coaxial lines, each λ/4 long at the center frequency. The left-hand line has the characteristic impedance of \( Z_1 \). The second conductors of these transmission line sections with housing mask another two short-circuited \( \lambda/4 \) lines that are in series with each other and shunt the balanced lines, having a characteristic impedance of \( Z_B \), at location \( a \) and \( b \). As shown in the equivalent circuit (Figure 3-1 B)) [3.3], the stubs \( Z_{s1} \) and \( Z_{s2} \) are in series and shunt the balanced
lines. Their characteristic impedance is made as large as possible. These impedances along with the other transmission line impedances determine the impedance transformation and bandwidth.

Figure 3-1. Marchand Compensated Balun A) Coaxial cross section B) equivalent transmission-line model.
Figure 3-2 shows a simplified equivalent circuit of the Marchand balun. Because of the equal shunting effects on the balanced lines, these stubs provide greater bandwidth. The open circuit stub $Z_2$ provides low impedance at the junction of the four different lines and acts like a series resonant circuit. The series resonant circuit with a shunt resonant circuit reduces the phase variation over the designed bandwidth. The ratio of the characteristic impedances of short-circuited stubs determines the bandwidth. The higher the ratio is, the wider the bandwidth is. The transmission line $Z_B$ can be designed with a characteristic impedance of the balanced line or can be used as an impedance transformer between the desired impedance and the balanced-line impedance [3.2].

![Simplified equivalent circuit of a fourth-order Marchand balun.](image)

**3.3. New Analysis Method for Planar Marchand Baluns**

Since the structure of Marchand balun is symmetrical, the four transmission lines can be treated as two sections of coupled lines. Marchand balun analysis in its original paper [3.2] and similar work [3.3][3.4] is based on the calculation of input (unbalanced port) and output (balanced port) impedance for coaxial-based coupled lines. Therefore, it is difficult to use these
analyses for a planar type Marchand balun since the calculated impedance is the impedance of inner and outer conductor in coaxial cable. The following references have been focused on the fabrication and synthesis, including coupled line equivalent circuits models and computer-aided analysis [3.5][3.6][3.7][3.8]. However, using these results, the designer still need to work a lot due to their complex analyses. Since K. S. Ang proposed Marchand balun analysis using scattering matrix [3.9] by assuming the symmetric coupled lines, many researches adapted the scattering matrix based analysis and synthesized the broadband balun on standard Si technology [3.10][3.11][3.12], LTCC [3.13][3.14] or FR4 PCB board [3.15]. Ang’s analysis method can calculate the appropriate coupling factor and simplify the balun design. To get a design solution for a coupling factor for the desired Marchand balun, the coupling factor \( C \) of the coupled line needs to be assumed. This conventional Marchand balun analysis [3.9] did not consider the effect of the coupled line’s electrical length (\( \theta \)). This conventional analysis is optimized exactly at the center frequency. The transmission line’s characteristics vary significantly depending on the transmission line’s physical and electrical length. Therefore, if one considers the effect of the electrical length (\( \theta \)) of the transmission line, the analysis will be more accurate. Also, the response depending on the coupled line’s electrical length (\( \theta \)) illustrates the actual response of the designed Marchand balun.

The start of this new analysis procedure is the same as the conventional case [3.9]. For symmetrical baluns, the scattering matrix of the balun can be derived from the scattering matrix of two identical couplers. First, consider the case where the source and load impedances are equal to \( Z_0 \).
In this case, the coupler’s scattering parameter includes the electrical length of the transmission line as opposed to simplifying it using a quarter wavelength (\( \lambda /4 \)). Figure 3-4 shows geometry and port designations of the coupled line.

When two unshielded transmission lines are close together, power can be coupled between the lines due to the interaction of the electromagnetic fields of each line. Designs usually assume coupled transmission operate in the TEM mode, which is rigorously valid for stripline and coaxial structures and approximately valid for microstrip structure. For the sake of simplicity, the input (port 1) is matched and port 3 is isolated. Equation (3.1) shows the
coupler’s scattering parameter [3.16] with the assumption of a homogeneous case which means the even and the odd mode phase velocity are equal.

\[
[S]_{\text{coupler}} = \begin{bmatrix}
0 & jC \tan \theta & 0 & \sqrt{1-C^2} \\
\frac{jC \tan \theta}{\sqrt{1-C^2} + j \tan \theta} & 0 & \frac{\sqrt{1-C^2}}{\cos \theta \sqrt{1-C^2} + j \sin \theta} & 0 \\
0 & \frac{\sqrt{1-C^2}}{\cos \theta \sqrt{1-C^2} + j \sin \theta} & 0 & \frac{jC \tan \theta}{\sqrt{1-C^2} + j \tan \theta} \\
\frac{\sqrt{1-C^2}}{\cos \theta \sqrt{1-C^2} + j \sin \theta} & 0 & \frac{jC \tan \theta}{\sqrt{1-C^2} + j \tan \theta} & 0
\end{bmatrix}
\]  

(3-1)

Equation 3-1 simplifies into the conventional analysis of [3.9] by substituting the electrical length \( \theta \) with a quarter wavelength \( \theta = \lambda/4 = \pi/2 \). The scattering parameter of the Marchand balun can then be obtained by using the voltage wave’s relationships that are indicated in Figure 3-3, which is derived as equation 3-2.

\[
[S]_{\text{balun}} = \begin{bmatrix}
\frac{x^4 - y^4 - y^2}{1 + y^2} & \frac{x^3 y - xy^3 - xy}{1 + y^2} & -\frac{x^3 y - xy^3 - xy}{1 + y^2} & \frac{1 + y^2}{1 + y^2} \\
\frac{x^3 y - xy^3 - xy}{1 + y^2} & \frac{1 + y^2}{1 + y^2} & \frac{x^2 y^2 + y^2 + y^4}{1 + y^2} & -\frac{x^2 y^2 + y^2 + y^4}{1 + y^2} \\
\frac{x^3 y - xy^3 - xy}{1 + y^2} & -\frac{x^2 y^2 + y^2 + y^4}{1 + y^2} & \frac{1 + y^2}{1 + y^2} & \frac{x^2 y^2 + y^2 + y^4}{1 + y^2} \\
\frac{x^3 y - xy^3 - xy}{1 + y^2} & -\frac{x^2 y^2 + y^2 + y^4}{1 + y^2} & -\frac{x^2 y^2 + y^2 + y^4}{1 + y^2} & \frac{1 + y^2}{1 + y^2}
\end{bmatrix}
\]  

(3-2)

where \( x = \frac{\sqrt{1-C^2}}{\cos \theta \sqrt{1-C^2} + j \sin \theta} \), \( y = \frac{jC \tan \theta}{\sqrt{1-C^2} + j \tan \theta} \)

If the load (balanced port) termination impedance is no longer equal to \( Z_0 \), the balun’s scattering matrix will be modified from \([S]_{\text{balun}}\) to \([S]_{\text{balun}}'\). The relationship between the two matrices is given by equations 3-3 through 3-5.

\[
[S]_{\text{balun}}' = [A]^{-1} \cdot \left( ([S]_{\text{balun}} - [\Gamma]) \cdot ([I] - [\Gamma][S]_{\text{balun}})^{-1} \right) \cdot [A]  
\]  

(3-3)
where \([I]\) is the identical matrix, while \([\Gamma]\) and \([A]\) are in equation 3-4 and 3-5.

\[
[\Gamma] = \begin{bmatrix}
0 & 0 & 0 \\
0 & \frac{Z_L - Z_0}{Z_L + Z_0} & 0 \\
0 & 0 & \frac{Z_L - Z_0}{Z_L + Z_0}
\end{bmatrix}
\tag{3-4}
\]

\[
[A] = \begin{bmatrix}
1 & 0 & 0 \\
0 & 2\frac{\sqrt{Z_L Z_0}}{Z_L + Z_0} & 0 \\
0 & 0 & 2\frac{\sqrt{Z_L Z_0}}{Z_L + Z_0}
\end{bmatrix}
\tag{3-5}
\]

In order to simplify the final equation, the equation 3-2 is converted to the equation 3-6.

\[
[S]_{balun} = \begin{bmatrix}
\frac{x^4 - y^4 - y^2}{1 + y^2} & \frac{x^3 y - x y^3 - x y}{1 + y^2} & \frac{-x^3 y - x y^3 - x y}{1 + y^2} \\
\frac{x^3 y - x y^3 - x y}{1 + y^2} & \frac{1 + y^2}{x^2} & \frac{-x y^2 + y^2 + y^4}{1 + y^2} \\
\frac{x^3 y - x y^3 - x y}{1 + y^2} & \frac{-x y^2 + y^2 + y^4}{1 + y^2} & \frac{-x^2 y^2 + y^2 + y^4}{1 + y^2}
\end{bmatrix}
= \begin{bmatrix}
S_{11} & S_{12} & -S_{12} \\
S_{12} & S_{22} & S_{23} \\
-S_{12} & S_{23} & S_{22}
\end{bmatrix}
\tag{3-6}
\]

Finally,

\[
[S]_{balun}' = \begin{bmatrix}
S_{11}' & S_{12}' & S_{13}' \\
S_{21}' & S_{22}' & S_{23}' \\
S_{31}' & S_{32}' & S_{33}'
\end{bmatrix}
\tag{3-7}
\]

where

\[
S_{11}' = S_{11} + \frac{2S_{12}^2 (Z_L - Z_0)}{(S_{23} - S_{22})(Z_L - Z_0) + (Z_L + Z_0)}
\]
These equations can be reduced to the equations of the quarter wavelength case by replacing the electrical length \((\theta)\) with a quarter wavelength \((\theta = \lambda/4 = \pi/2)\). If the load termination impedance \((Z_L)\) is the same as \(Z_0\), the equation 3-7 is reduced to equation 3-2. Also, in case of the electrical length of coupled lines are equal to a quarter wavelength, equation 3-7 is reduced to equation 3-8.

When the load termination is equal to \(Z_0\), equation 3-8 is the same as equation 3-2.

Equation 3-8 shows that the use of identical coupled sections results in balun outputs of equal amplitude and opposite phase, regardless of the coupling factor and port terminations. To achieve optimum power transfer of -3dB to each balanced port, equation 3-8 is required.
With the equation (3.8) and (3.9), the required coupling factor for optimum balun performance is as followed.

$$C = \frac{1}{\sqrt{\frac{2Z_L}{Z_0} + 1}}$$  \hspace{1cm} (3-10)$$

It is interesting to note that when all the ports are terminated with the same impedance, such as 50 Ω, where the impedance transforming ratio is unity, the required coupling factor is -4.8dB which is different from the well-known result of -3dB. Based on the equation 3-7, the use of commonly assumed -3dB couplers will result in -3.52 dB of the insertion loss (S_{21}, S_{31}) and output isolation (S_{23}, S_{32}). Input and output return loss is -9.54dB at the center frequency.

The proposed analysis can provide an accurate design parameter for the input and output impedance to the balun. With the known impedance, the coupling factor of the coupled line determines the optimum response of the Marchand balun.
3.4. Numerical Results of New Analysis for Planar Marchand Baluns

Equation 3-7 shows the dependence of the coupling factor on the insertion loss as shown in Figure 3-5 while the load (balanced) impedance is the same as the input (unbalanced) impedance ($Z_L = Z_0$).

Figure 3-5. Insertion loss ($S_{21}, S_{31}$) of the planar Marchand Balun as a function of coupler electrical length ($\theta$) depending on the coupling factor ($C$).

As expected in previous section, the optimum response can be achieved with -4.8dB symmetric coupled lines. Tighter coupled lines can increase operation bandwidth while it degrades the response at the center frequency. Therefore, as long as a compensation method is provided, the tighter coupled lines can improve the operational bandwidth. For this work, the microwave/RF probe has a calibration method to make up for its uneven response.

Suppose there is a desired maximum insertion loss at -4 dB in order to quantify the operational bandwidth. Figure 3-6 shows the insertion loss of the marchand balun with different coupling coefficients and shows $f_1$ and $f_2$ which represent the intersection point at -4dB for deriving the normalized bandwidth ($\left(\frac{f_2-f_1}{f_0}\right)$). If the coupling coefficient is greater than the optimized coupling coefficient which is calculated through equation 3-10, the insertion loss at
the center frequency decreases. With more than -3 dB coupling coefficient, the insertion loss at center frequency is less than -4 dB. The maximum bandwidth balun can be designed using the equation 3-11 derived with -4 dB insertion loss at the center frequency.

\[ |S'_{balun,21}| = |S'_{balun,31}| = \frac{1}{\sqrt{2.5}} \]  

(3-11)

Balun operational bandwidth can be maximized around -2.46 dB with 1.23 times the normalized bandwidth while the normalized bandwidth of balun optimized for maximum center frequency response is 0.88. Therefore, the balun design can be divided into two styles. First is the design which has the best response at center frequency. Second is the design which has the widest operational bandwidth for broadband applications.

Figure 3-6. Insertion loss \((S_{21}, S_{31})\) of the planar Marchand Balun as a function of coupler electrical length \((\theta)\) depending on the coupling factor \((C)\).

Figure 3-7 illustrates the balun responses depending on the impedance transforming ratio \((Z_L/Z_0)\) while the coupling factors are decided by equation 3-10. Figure 3-8 illustrates the responses depending on the impedance transforming ratio \((Z_L/Z_0)\) while the coupling factors are
decided by equation 3-11 for the broadband applications. $S_{21}$ ($S_{31}$ = $S_{13}$ = $S_{12}$) represents the insertion loss. $S_{11}$ represents reflection at unbalanced port. $S_{22}$ ($S_{33}$) represents reflection at balanced port. $S_{23}$ ($S_{32}$) represents the isolation between the balanced ports. It is worth noting that as the impedance transforming ratio increases, the operational bandwidth starts to shrink while the response at the center frequency is optimized.

Figure 3-7. Responses of the planar Marchand Balun as a function of coupler electrical length ($\theta$) at A) 1:1 impedance transforming ratio ($Z_0 = Z_L$, $C = -4.78$ dB) B) 1:2 impedance transforming ratio ($Z_0 = 2Z_L$, $C = -7$ dB) C) 1:3 impedance transforming ratio ($Z_0 = 3Z_L$, $C = -8.45$ dB) D) 1:4 impedance transforming ratio ($Z_0 = 4Z_L$, $C = -9.54$ dB) with the optimized coupling factor ($C$).
Figure 3-8. Responses of the planar Marchand Balun as a function of coupler electrical length ($\theta$) at A) 1:1 impedance transforming ratio ($Z_0=Z_L$, $C=-2.46$dB) B) 1:2 impedance transforming ratio ($Z_0=2Z_L$, $C=-4$dB) B) 1:3 impedance transforming ratio ($Z_0=3Z_L$, $C=-5.2$dB) D) 1:4 impedance transforming ratio ($Z_0=4Z_L$, $C=-6.08$dB) with the optimized coupling factor ($C$).

Figure 3-7 shows a reasonable performance for all the responses. Particularly, the input reflection shows a perfect matching at the center frequency. The isolation ($S_{23}$) and the reflection ($S_{22}$) for balanced ports is poor due to the inherent limitations of the Marchand balun. Several studies have been done to improve this poor isolation [3.9][3.17]. All the reported compensations for the isolation need to use lumped elements such as resistors. However, this work limits the balun to a transmission line structure. Figure 3-8 shows the achievable widest operation bandwidth with the sacrifice of input matching at the center frequency. As like the case of Figure 3-7, the operational bandwidth starts to shrink with the increase of the impedance transforming ratio.
3.5. Verification of New Analysis for Planar Marchand Baluns

For verification, numerical results are compared with simulated results using Agilent ADS. Figure 3-9 shows the simulation setup and the simulated structure. In order to find proper parameters for coupled-line structures, LINECAL in ADS is used. The proposed analysis assumes the homogeneous media and TEM mode propagation so that a stripline design is used. The stripline structure can support TEM mode propagation and can be considered to be built in a homogeneous media. In order to achieve tight coupling, the simulation is performed with a broadside coupled stripline.

Figure 3-10 shows the results when the input impedance is 50 Ω and the output impedances are 100 Ω with coupling coefficient is -7 dB while Figure 3-11 shows the results when the input impedance is 50 Ω and the output impedances are 50 Ω with the coupling coefficient as -4.78 dB.

Figure 3-10 and Figure 3-11 show the comparison between the numerical results of the proposed analysis and the simulated results in Agilent ADS. All the responses of both cases show very good agreement. Through the proposed analysis, the design procedure can be simplified by removing time-consuming trial and error when finding the optimum design parameters. With a given input and output impedance, the design equation suggests the proper coupling level to optimize the design.
Figure 3-9. ADS verification A) The schematic diagram for the conventional planar Marchand Balun B) The vertical view of the broadside coupled stripline structure.
Figure 3-10. Numerical results verifications A) Numerical results and B) Simulated result with -7dB of the coupling factor when the impedance transforming ratio is 1:2.

Figure 3-11. Numerical results verifications A) Numerical results and B) Simulated result with -4.78dB of the coupling factor when the impedance transforming ratio is 1:1.

3.6. Conclusion

A new analysis method for a planar Marchand balun is proposed with the consideration of input (unbalanced) port and output (balanced) port termination impedances. The proposed method was verified with Agilent ADS and shows very good accuracy when compared to commercial RF/Microwave simulation tools. In order to achieved optimize designs, conventional methods take much longer time compared to the proposed method. The proposed
analysis method leads the designers to find the optimum balun design parameters for specific application. By this method, a high frequency Marchand baluns are designed and implemented as shown in chapter 4 and chapter 5.
CHAPTER 4
MARCHAND BALUN INTEGRATION USING BROADSIDE COUPLED COPLANAR STRIPINES

In measuring four-port differential circuits, the most convenient method is to use a four-port vector network analyzer (VNA), which has balanced differential source and receivers [4.1]. However, due to the high cost of such test equipment, the balun integrated probe is proposed to measure the differential circuit with commonly available two-port VNA by focusing on measuring the differential mode [4.2].

![RF/microwave dual probe structure](image)

Figure 4-1. RF/microwave dual probe structure A) the overall structure B) cross-sectional view of the probe membrane C) top view of the probe membrane.

In a previous chapter, the new planar Marchand balun analysis method was proposed. By using the previous chapter’s analysis, the optimum design parameters can be derived to build the
Marchand balun integrated differential probe for combining the differential signal into a single ended signal. In order to implement the balun on a RF/microwave probe membrane, probe membrane structure is investigated for the purpose of finding an available transmission line structure to build the optimum coupling coupled line.

Figure 4-1 shows one example of a RF/microwave probe structure. Figure 4-1 A) shows the overall microwave probe structure and Figure 4-1 B) and C) illustrate the probe membrane structure. A microwave membrane probe generally consists of three dielectric layers, two metal layers and a via. For low frequency application (<40GHz), the connection from DUT to COAX uses a microstrip line structure which has 50 $\Omega$ characteristic impedance while for higher frequency applications (<100GHz), a coplanar waveguide structure is used. For the probe membrane, there is no ground shield for the upper and lower layers due to the fact that these are only two available metal layers. Therefore, the available coupled line structures are very limited when implementing balun probe membrane.

Two possible transmission line structures are investigated and used for the balun implementation. This chapter deals with coplanar stripline structure and the next chapter handles coplanar waveguide structures. The two structures do not need a ground plane on an upper or a lower signal line plane. Therefore, they are very good candidates for a two metal layer structure.

4.1. Broadside Coupled Coplanar Striplines (CPS)

4.1.1. Introduction to Coplanar stripline (CPS)

The physical realization of a coplanar strip transmission line (CPS) is illustrated in Figure 4-2. This was first studied by C. P. Wen [4.3]. It is realized by setting two conductor strips of width $w_1$ and $w_2$ in close proximity supported by a dielectric of thickness $h$ while on the other side of the dielectric, there is no ground plane. If $w_1$ is not equal to $w_2$, the structure is called as an asymmetric CPS (ACPS). CPS is a full planar transmission line similar to slot lines or
coplanar waveguide. CPS’s low order propagation mode is not a real TEM mode due to the bottom and top dielectric discontinuity. The fundamental mode is quasi-TEM mode because it resembles a pure TEM mode since the longitudinal field components are smaller than the transverse ones, which can be ignored [4.4]. The advantages of CPS are as follows: (1) both series as well as shunt mounting of devices is possible. (2) The CPS is a balanced transmission line. The main disadvantage of the CPS is that because it lacks a ground plane, the line can support besides the fundamental CPS mode two other parasitic modes, namely the TE₀ and TM₀ dielectric slab waveguide modes. These parasitic modes do not have a cutoff frequency. The TE₀ and TM₀ modes have their electric fields predominantly parallel and perpendicular to the dielectric-air interface, respectively. The electric field of the fundamental CPS mode is predominantly parallel to the dielectric-air interface and hence strongly couples to the TE₀ parasitic mode at discontinuities.

Figure 4-2. Coplanar strips transmission line structure [4.4].
4.1.2. Broadside Coupled Asymmetric Coplanar Striplines (CPS)

Uniform coupled-line circuits are used for many application including filters, couplers, and impedance matching networks. These circuits are usually designed by utilizing the impedance, admittance, chain and other parameters characterizing the coupled-line four-port network. These parameters may be obtained in terms of coupled-line impedances or admittances, and phase velocities for even and odd modes of excitation for the case of pure TEM lines in a homogeneous medium or quasi-TEM lines in an inhomogeneous medium. Recall that even and odd modes of excitation correspond to the cases where the voltages and the currents on the two lines are equal in magnitude and are in phase for the even mode and out of phase for the odd mode [4.5].

Generally, the thin film process for the fabrication of a RF/microwave probe membrane does not support a top and bottom metal layer which works as the shield (or housing) in order to protect against a field disturbance due to an external source. Therefore, the field analysis of a coupled lines structure without a shield is much complicated when compared to the case with a shield. In addition, the optimized balun design requires at least -4.8dB of coupling factor between the coupled lines. A conventional parallel coupled lines structure can not achieve this tight coupling except with a special kind of parallel coupler such as a Lange Coupler. But the Lange coupler needs to connect two separated signal lines by wirebonding or air-bridging to increase the coupling effect. However, the broadside coupled line structure can achieve such tight coupling and be very area-efficient compared to a parallel coupled line structure. Hence, the balun is integrated in a probe membrane structure using a broadside coupled line structure. In addition, the small area for the balun integration requires that the finite ground plane effect should be considered. Generally, a ground plane, which is electrically and physically narrow, typically less than $\lambda_g/5$ wide, where $\lambda_g$ is the signal wavelength [4.6], is considered as a finite
ground. A finite ground can support a great circuit size reduction and can influence higher order mode propagation. Recently, finite ground plane coplanar waveguide and coplanar striplines have received strong attention due to their inherent advantages. However, these applications are limited due to the lack of analysis of these structures. In the next section, broadside coupled coplanar stripline is analyzed for the first time.

4.2. Analysis of Broadside Coupled Coplanar Striplines (CPS)

Figure 4-3. Broadside coupled coplanar stripline (CPS) cross-section with finite ground plane.

Figure 4-3 shows a symmetric finite ground broadside coupled coplanar stripline’s cross-section with three dielectric layers. The signal line width is $a$ and the gap between the signal line and ground is $b-a$. The ground width is $c-a$. Due to the narrow ground, the field distribution will distort a lot, which makes a big difference of the characteristics of both the finite and the infinite ground coupled-line structures. The dielectric constant and the height of the dielectric between the signal lines are $\varepsilon_{r1}$ and $h_1$, respectively. The dielectric constant of the dielectric located on the upper and the lower signal lines are $\varepsilon_{r2}$ and $h_2$, respectively. The detailed analysis of this cross-section is found in Appendix A. In this section, the final results are used for extracting the balun design parameters.
4.2.1 Even Mode

The final even mode capacitance is described by equation 4-1.

\[ C_E = C_{e1} + C_{e2} + C_{e3} = \varepsilon_0 \varepsilon_{r1} \frac{K(k_{e1})}{K'(k_{e1})} + \varepsilon_0 \left(\varepsilon_{r2} - 1\right) \frac{K(k_{e2})}{K'(k_{e2})} + \varepsilon_0 \frac{K(k_{e3})}{K'(k_{e3})} \]  \hspace{1cm} (4-1)

where \( K(k) \) is the complete elliptic integral of the first kind with module \( k \) and \( K'(k) \) its complement.

\[
k_{e1} = \left[ \frac{\exp\left(\frac{\pi \cdot b}{h_1}\right) - 1}{\exp\left(\frac{\pi \cdot c}{h_1}\right) - \exp\left(\frac{\pi \cdot a}{h_1}\right)} \right]^{-1} \left[ \frac{\exp\left(\frac{\pi \cdot c}{h_1}\right) - \exp\left(\frac{\pi \cdot a}{h_1}\right)}{\exp\left(\frac{\pi \cdot b}{h_1}\right) - 1} \right]
\]

\[
k_{e2} = \left[ \frac{\exp\left(\frac{\pi \cdot a}{h_2}\right) - 1}{\exp\left(\frac{\pi \cdot c}{h_2}\right) - \exp\left(\frac{\pi \cdot b}{h_2}\right)} \right]^{-1} \left[ \frac{\exp\left(\frac{\pi \cdot c}{h_2}\right) - \exp\left(\frac{\pi \cdot b}{h_2}\right)}{\exp\left(\frac{\pi \cdot a}{h_2}\right) - 1} \right]
\]

\[
k_{e3} = \sqrt{\frac{a \cdot (c - b)}{b \cdot (c - a)}}
\]

The effective dielectric constant and the characteristic impedance are derived as the equation 4-3 and 4-4.

\[
\varepsilon_{\text{eff}_E} = 1 + \frac{(\varepsilon_{r1} - 1) \frac{K(k_{e1})}{K'(k_{e1})} + (\varepsilon_{r2} - 1) \frac{K(k_{e2})}{K'(k_{e2})}}{\frac{K(k_{e1})}{K'(k_{e1})} + \frac{K(k_{e3})}{K'(k_{e3})}} \]  \hspace{1cm} (4-3)

\[
Z_{0E} = \frac{120\pi}{\sqrt{\varepsilon_{\text{eff}_E} \left[ \frac{K(k_{e1})}{K'(k_{e1})} + \frac{K(k_{e3})}{K'(k_{e3})} \right]}} \]  \hspace{1cm} (4-4)

4.2.2 Odd Mode

The final even mode capacitance is described by equation 4-5.
\[ C_\phi = C_{o1} + C_{o2} + C_{o3} = \varepsilon_0^{\varepsilon_{r_1}} \left( \frac{K(k_{o1-1})}{K'(k_{o1-1})} + \frac{K(k_{o1-2})}{K'(k_{o1-2})} \right) + \varepsilon_0 \left( \varepsilon_{r_2} - 1 \right) \frac{K(k_{o2})}{K'(k_{o2})} + \varepsilon_0 \frac{K(k_{o3})}{K'(k_{o3})} \quad (4-5) \]

where \( K(k) \) is the complete elliptic integral of the first kind with module \( k \) and \( K'(k) \) its complement.

\[
k_{o1} = \sqrt{\left( \frac{\exp \left( \frac{\pi \cdot a}{h_1} \right) - 1}{\exp \left( \frac{\pi \cdot b}{h_1} \right)} \right) \exp \left( \frac{\pi \cdot b}{h_1} \right)}
\]

\[
k_{o1-1} = \frac{1}{\left( \tanh \left( \frac{\pi \cdot W_2}{2H_1} \right) \cdot \tanh \left( \frac{\pi \cdot W_4}{2H_1} \right) \right)}
\]

\[
k_{o1-2} = \frac{1}{\left( \tanh \left( \frac{\pi \cdot (W_1 - W_3)}{2H_1} \right) \cdot \tanh \left( \frac{\pi \cdot (W_1 - W_4)}{2H_1} \right) \right)}
\]

\[
k_{o2} = \sqrt{\left( \frac{\exp \left( \frac{\pi \cdot a}{h_2} \right) - 1}{\exp \left( \frac{\pi \cdot b}{h_2} \right)} \right) \exp \left( \frac{\pi \cdot b}{h_2} \right)} - \exp \left( \frac{\pi \cdot c}{h_2} \right) - \exp \left( \frac{\pi \cdot a}{h_2} \right)}
\]

\[
k_{o3} = \sqrt{\frac{a \cdot (c - b)}{b \cdot (c - a)}}
\]

\[
W_1, W_2, W_3, W_4 \text{ and } H_1 \text{ can be derived as shown in equation } 4-7.
\]

\[
\frac{W_1}{H_1} = \frac{K(k_{o1})}{K'(k_{o1})}
\]

\[
W_2 = F \arcsin \left( \frac{\exp \left( \frac{\pi \cdot b}{h_1} \right) - 1}{\exp \left( \frac{\pi \cdot b}{h_1} \right) \cdot (t_{\infty} - 1)} \right) k_{o1}
\]

\[
W_3 = F \arcsin \left( \frac{\exp \left( \frac{\pi \cdot b}{h_1} \right) - 1}{\exp \left( \frac{\pi \cdot b}{h_1} \right) \cdot \exp \left( \frac{\pi \cdot c}{h_1} \right)} \right) k_{o1}
\]

\[
W_4 = \frac{W_2 + W_3}{2}
\]

\[ (4-6) \]
where $F(\phi,k)$ is the incomplete elliptic integral of the first kind, written in Jacobi’s notation.

The effective dielectric constant and the characteristic impedance are in equation 4-8 and 4-9.

$$\varepsilon_{\text{eff},O} = 1 + \left(\varepsilon_{r1} - 1\right) \left(\frac{K(k_{o1})}{K'(k_{o1})} + \frac{K(k_{o2})}{K'(k_{o2})}\right) + \left(\varepsilon_{r2} - 1\right) \frac{K(k_{o2})}{K'(k_{o2})}$$

$$Z_{\theta0} = \frac{120\pi}{\sqrt{\varepsilon_{\text{eff},O} \left[\frac{K(k_{o1})}{K'(k_{o1})} + \frac{K(k_{o2})}{K'(k_{o2})} + \frac{K(k_{o3})}{K'(k_{o3})}\right]}}$$

### 4.3. Numerical Results of Broadside Coupled Coplanar Striplines (CPS)

The analytic expressions are verified with an aid of MATLAB. The field distribution change will affect the characteristic impedance and the coupling. Figure 4-4 illustrates the characteristic impedance variation as the slot width changes from 10 \(\mu m\) to 50 \(\mu m\) while the ground plane width is 50 \(\mu m\). The thickness of the lower ($h_1$) and the upper ($h_2$) dielectrics are 10 \(\mu m\) and 15 \(\mu m\). As the slot width increases, the characteristic impedances of both even and odd mode excitations increase because the electric field is distributed over a large area. Even mode characteristic impedance increases at a great rate than odd mode characteristic impedance since the electric field distribution under the even mode excitation is more concentrated over the slot area.

Figure 4-5 shows the characteristic impedance variation as the ground width changes from 50 \(\mu m\) to 250 \(\mu m\). The response is similar to that of Figure 4-4. As the ground plane width increases, the electric field converges into ground plane with less loss. Therefore, the characteristic impedance decreases, especially the even mode excitation because the field distribution under the even mode excitation is more concentrated over the slot. For odd mode
excitations, the electric field concentrates on the lower dielectric, intensively. So the odd mode case varies less with ground width variation.

Figure 4-4. Even and odd mode characteristic impedance variation depending on slot width \((b - a)\) as a function of signal line width \((a)\) while the ground plane width \((c - b)\) is 50 um.

Figure 4-5. Even and odd mode characteristic impedance variation depending on GND width \((c - b)\) as a function of signal line width \((a)\) while slot width \((b - a)\) is 30 um.
Through this analysis, the coupling factor can be derived using well-known the equation 4-10.

\[
C = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}}
\]  

(4-10)

Figure 4-6 shows one of example which describes the coupling factor. The coupling factor increases as the ground width gets narrower and slot width gets larger. As explained earlier, the even mode characteristic impedance is affected more than the odd mode characteristic impedance. The even mode field distribution affects the coupling between the signal lines. As the signal line gets wider, more electric field concentrates between the signal lines so that the coupling gets stronger.

![Figure 4-6. Coupling coefficient depending on slot width \((b-a)\) as a function of signal line width \((a)\) when GND widths \((b-a)\) are 50 um and \(\infty\).](image)

Table 4-1 compares the numerical results and simulated results for several cases. The simulation is performed with a 3D EM simulator for the purpose of the verification of the proposed analysis. Through this analysis, the coupling coefficient for the Marchand balun is
extracted and verified with 3D-EM simulator which uses Finite Element Method (FEM). The simulation results are based on the frequency so that the coupling coefficients are chosen by selecting the best value through all frequency responses. Table 4-1 compares the numerical and simulated results of broadside coupled coplanar waveguides. Simulated results and numerical results show less than 0.2 dB difference. However, the simulation takes longer time than the numerical results due to the complex mesh equations. The proposed equation saves the time and effort in finding the initial design parameters.

Table 4-1. Numerical and simulated coupling coefficients

<table>
<thead>
<tr>
<th>Signal width (a)</th>
<th>Gap width (b-a)</th>
<th>GND width (c-b)</th>
<th>Numerical result (dB)</th>
<th>Simulated result (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 um</td>
<td>50 um</td>
<td>200 um</td>
<td>-4.536 dB</td>
<td>-4.427 dB</td>
</tr>
<tr>
<td>50 um</td>
<td>200 um</td>
<td>50 um</td>
<td>-4.745 dB</td>
<td>-4.782 dB</td>
</tr>
<tr>
<td>30 um</td>
<td>50 um</td>
<td>200 um</td>
<td>-3.59 dB</td>
<td>-3.454 dB</td>
</tr>
<tr>
<td>50 um</td>
<td>200 um</td>
<td>50 um</td>
<td>-3.805 dB</td>
<td>-3.755 dB</td>
</tr>
<tr>
<td>30 um</td>
<td>200 um</td>
<td>50 um</td>
<td>-3.477 dB</td>
<td>-3.3836 dB</td>
</tr>
<tr>
<td>50 um</td>
<td>50 um</td>
<td>200 um</td>
<td>-3.688 dB</td>
<td>-3.548 dB</td>
</tr>
<tr>
<td>30 um</td>
<td>200 um</td>
<td>50 um</td>
<td>-2.754 dB</td>
<td>-2.595 dB</td>
</tr>
<tr>
<td>50 um</td>
<td>50 um</td>
<td>200 um</td>
<td>-2.962 dB</td>
<td>-2.797 dB</td>
</tr>
<tr>
<td>30 um</td>
<td>200 um</td>
<td>50 um</td>
<td>-2.827 dB</td>
<td>-2.812 dB</td>
</tr>
<tr>
<td>50 um</td>
<td>50 um</td>
<td>200 um</td>
<td>-3.031 dB</td>
<td>-2.943 dB</td>
</tr>
<tr>
<td>30 um</td>
<td>200 um</td>
<td>50 um</td>
<td>-2.24 dB</td>
<td>-2.206 dB</td>
</tr>
<tr>
<td>50 um</td>
<td>200 um</td>
<td>50 um</td>
<td>-2.437 dB</td>
<td>-2.382 dB</td>
</tr>
</tbody>
</table>

4.4. Marchan Balun Implementation

The basic parameters were extracted from the analytic expression in the previous section. The characteristics of these broadside coupled line, CPS does not affect the frequency variation as long as the coplanar line works in TEM mode. Generally, CPS and CPW can sustain the normal operation without serious loss up to 220GHz. Also, the dispersion of these CPS can be
ignored due to the relatively thick metal layer. Rigid calculation shows 200nm of skin depth in 100GHz operation. But this process metal thickness is around 5um. The broadside coupled CPS’s quarter wavelength is around 500um in 60GHz operation, which is verified through HFSS simulation. The baluns were integrated on a Cascade probe structure (GSSG with 150um pitch). This thin film process has relatively large process variation, especially on dielectric thickness. General application of this process is for the integration of the single or parallel coupled transmission lines with a lower ground plane. So, the ground of this process can not be considered as infinite ground due to the fact that there is no shielding or housing. The basic parameters were extracted from the broadside coupled CPS analysis. The final design verifications were performed with the aid of HFSS because the proposed analysis can not consider the discontinuity causing by transmission line connection to the coaxial cable. In order to check the effect of the coupling coefficient variation in chapter 3, the baluns were fabricated in 30, 50, 70 and 90 \( \text{um} \) coupled line widths with 50 \( \text{um} \) gap width between the signal line and the ground.

4.4.1 The Design Verification using HFSS

Figure 4-7 shows the schematic diagram of the Marchand balun integrated probe using the broadside coupled CPS with finite ground. An unbalanced port connects with coaxial cable for the connection to the test equipment while a balanced port touches the DUT with sharp probe tips.

For an accurate measurement, calibration is essential. The final verifications were performed as closely as possible to the actual probe environment, which means the air encloses this structure. The air region set up as a radiation boundary in simulation.
Figure 4-7. 100GHz Marchand balun structure

Figure 4-8 shows the simulation results. The results include the unbalanced to balanced insertion losses ($S_{31}$, $S_{32}$) and phase difference (target value 180°) to check the balun performance. The operational bandwidth ranges from 20GHz to 100GHz. The coupled line uses -3 dB coupling factor for which the signal line width ($a$) chosen is 50 $\mu$m and the slot width ($b-a$) is 50 $\mu$m with approximately 80 $\mu$m ground plane width ($c-b$).
4.4.2. Layout

Actual layouts of Marchand balun integrated probe using broadside coupled CPS is shown in Figure 4-9. In the actual layout, the ground plane shape varies in order to fit the design into the original GSSG (150 um pitch) probe structure. For 90um signal line design, the gap width becomes smaller. The design of 30 um of the signal line width facilitates -4.8 dB coupling factor to get the best center frequency performance. The designs of 50um and 70um of the signal line widths are taken into account the process variations. These two designs show around -3 dB and -2.5 dB coupling coefficients by the previous analysis. The connections to both DUT and COAX use 50 Ω microstrip lines for easy assembly. Layout was performed with L-Edit.

Figure 4-10 shows the die photographs of the fabricated balun integrated probes. Four rectangular shapes of the bottom of the figure represents the DUT connection tips which usually have very small resistance (<2 Ω).
Figure 4-9. Actual layout of Marchand balun integrated probes using broadside coupled CPS.

Figure 4-10. Die photo of Marchand balun integrated probes using broadside coupled CPS.

Table 4-2 organizes the Marchand balun design parameters fabricated by Cascade Microtech thin film process. The measurement is performed for one design due to the expensive probe combining process such as high frequency coaxial cable, probe tips connection expense etc. For one measurement, at least two prototype designs were assembled to make sure of the measurement accuracy.
Table 4-2 Design parameter of the fabricated balun probe membrane

<table>
<thead>
<tr>
<th>Signal Line Width</th>
<th>Slot Width</th>
<th>Ground Width</th>
<th>Transmission Line Width</th>
<th>Tested Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 um</td>
<td>50 um</td>
<td>80 um</td>
<td>25 um</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>45 um</td>
<td>X</td>
</tr>
<tr>
<td>50 um</td>
<td>50 um</td>
<td>80 um</td>
<td>25 um</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>45 um</td>
<td>O</td>
</tr>
<tr>
<td>70 um</td>
<td>50 um</td>
<td>80 um</td>
<td>25 um</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>45 um</td>
<td>X</td>
</tr>
<tr>
<td>90 um</td>
<td>30 um</td>
<td>80 um</td>
<td>25 um</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>45 um</td>
<td>X</td>
</tr>
</tbody>
</table>

4.5. Marchan Balun Measurement

The balun integrated probes are measured using a dual-through pattern that is connected to a dual-probe, as shown in Figure 4-11. The displayed ports, port1~port3, are measured 2-ports at a time using a 2-port VNA, while the 3rd port is terminated in a matched load. This is followed by a post measurement process that shifts the reference phase plane, as shown in Figure 4-11. In this measurement, the dual through length will be considered seriously due to relatively high frequency configuration. To overcome this problem, the measurement is adjusted by the phase difference due to dual-through on the ISS.

Figure 4-11. Measuring balun integrated probes using a dual-through connected to a dual-probe.
Figure 4-12. Measurement procedure with two port network analyzer.

Figure 4-12 shows the measurement procedure with a two port vector network analyzer. While measuring the two ports, the other port is terminated with 50 Ω. Final scattering parameters are organized with these measurement results.

Figure 4-13 shows the measurement result with a -3 dB coupling factor coupled line. The signal line width \((a)\) chosen is 50 um and the slot width \((b-a)\) is 50 um with approximately 80 um ground plane width \((c-b)\). For the comparison with the simulated results in HFSS in Figure 4-8, all the scales in Figure 4-12 are the same as those in Figure 4-8. The phase imbalance is less than 9° through the entire measured frequency range. Amplitude differences between the balanced ports are less than 1 dB up to 90GHz. As shown in the figure, lower amplitude imbalance indicates lower phase imbalance. The relative bandwidth can be calculated by simply normalizing the frequency at -4dB with the center frequency. In this case, \(f_1, f_2\) and \(f_0\) are equal to 28GHz, 82GHz, and 55GHz, respectively.

Relative Bandwidth\(=\frac{f_2 - f_1}{f_0}\) = 0.98 \hspace{1cm} (4.11)

This design’s coupling factor is less than -3 dB due to process variation. As analyzed in chapter 3, greater than -3 dB coupling factor ensures greater than 1 relative bandwidth. The measured
results verify the previous balun analysis. The difference between the insertion losses is caused by the quasi TEM mode propagation. The designed balun assumes a homogeneous media which can support pure TEM propagation. However, the actual fabricated structure is not a homogeneous media so that an insertion loss difference arises. Also, at higher frequencies, another propagation mode TE0 or TM0 arises. This causes the glitch in the insertion loss response around 90GHz.

Figure 4-13. Measured results of Marchand balun integrated probe.

Figure 4-14. Comparison between the measured and simulated results of Marchand balun integrated probe A) Insertion loss B) Phase Difference
Figure 4-14 compares the measured and simulated results through the specified frequency range. The insertion loss responses show differences at higher frequencies. This phenomenon comes from the other propagation mode excitations such as TE₀ and TM₀. The HFSS simulation is performed for low order propagation modes which only consider TEM mode propagation. However, the measured response can be compensated through a calibration procedure [4.2]. The phase response shows good agreement between the measurement and simulation.

4.6. Conclusion

In this chapter, the Marchand balun integrated probes are designed, fabricated and measured based on a proposed Marchand balun analysis presented in chapter 3 and on the coupled line parameter analysis in Appendix A. The parameter extraction method in Appendix A suggests a closed form equation which is different from the general EM solver solution. Typically, an EM solver use Finite-Difference Time-Domain (FDTD) method or Finite Element Method (FEM) which are solving huge mesh equation to find the differential equation solution. However, the proposed method in Appendix A uses the closed form equation and saves simulation time dramatically while providing an accurate solution.

Measured results and simulated results agree very well as shown in this chapter. Through the proposed design method, the design accuracy and time will be greatly enhanced compared to a trial and error simulation method. Figure 4-15 summarizes the balun design method using a flow chart.
Figure 4-15. Flow chart of the Marchand balun design methods.
CHAPTER 5
MARCHAND BALUN INTEGRATION USING BROADSIDE COUPLED COPLANAR WAVEGUIDE

5.1. Broadside Coupled Coplanar Waveguide (CPW)

5.1.1. Introduction to Coplanar Waveguide (CPW)

The physical realization of a coplanar waveguide is shown in Figure 5-1. This transmission line was first studied by C. P. Wen [5.1]. CPW is a full planar transmission line since in contrast to the microstrip case, there is no bottom ground conductor. Later, coplanar waveguide with the case of a bottom ground conductor was studied. As shown in Figure 5-1, this transmission line is composed of a central conductor of width \( w \), separated from two lateral conductors by a distance \( s \) called the slot. All the conductors of thickness \( t \), are placed on a dielectric slab of height \( h \) and dielectric and magnetic constant \( \varepsilon_r \) and \( \mu_r \).

![Figure 5-1. Coplanar strips transmission line structure [5.2].](image)
Coplanar waveguide has a zero cut-off frequency, but its low order propagation mode is quasi-TEM because it is not a pure TEM mode. However, the error made in evaluating the fundamental propagation mode as a pure TEM is negligible for frequencies up to some tens of GHz [5.3][5.4][5.5]. After this limit, dispersion occurs and the propagation mode gets into nearly TE₀ with the magnetic field elliptically polarized along the longitudinal planes. Since the electric and magnetic field in the air is larger than in the microstrip, the effective dielectric constant of CPW generally is lower than that of microstrip. Consequently, the achievable characteristic impedance is higher than the microstrip value. A coplanar waveguide, together with microstrip, is studied to a great extent due to its quasi-TEM propagation mode and its planar structure [5.6][5.7][5.8][5.9].

5.1.2. Broadside Coupled Coplanar Waveguide (CPW) with finite ground plane.

Many active and passive circuits can be integrated on relatively small IC area. The designer usually uses lumped-element counter parts of transmission line based circuits such as 3dB coupler, branch line couplers and baluns due to their compactness. As RF circuit operation frequency goes higher, the transmission line’s area gets smaller. Therefore, many studies have done to integrate transmission-line-based passive circuits on-chip. In spite of these all contributions, many passive circuits still model limitation due to the lack of a ground plane. Specially, the coplanar waveguide needs a ground plane on the same plane as the signal. For 60GHz circuits, the wavelength will be 5mm. In order to consider the ground as infinitely wide, the ground plane width should be at least \( \lambda_g/5 (=1\text{mm}) \) wide [5.10]. This consumes a huge area in the chip environment. Unless the ground plane is considered as infinitely wide, the conventional analysis will not be matched to reality due to the field distortion, caused by the lack of a very wide ground plane.
Figure 5-2 describes the finite ground broadside coupled coplanar waveguide. In order to extract the characteristic parameters for designing a balun, a new analytic expression for the broadside coupled CPW with finite ground plane is presented for the first time. The detailed derivation procedure and equations are in Appendix B. This method can be used for transmission line circuit modeling in a standard CMOS process due to its simplicity. In this section, numerical simulation results are used for designing a 90GHz Balun.

5.2. Analysis of Broadside Coupled Coplanar Waveguide (CPW)

5.2.1 Even Mode

The effective dielectric constants and the characteristic impedance are derived as equation 5-1 and 5-2.

\[
\varepsilon_{\text{eff, E}} = 1 + \frac{(\varepsilon_{r1} - 1)K(k_{e1})}{K'(k_{e1})} + \frac{(\varepsilon_{r2} - 1)K(k_{e3})}{K'(k_{e3})} \tag{5-1}
\]

\[
Z_{0E} = \frac{60\pi}{\sqrt{\varepsilon_{\text{eff, E}}}} \sqrt{\frac{K(k_{e1})}{K'(k_{e1})} + \frac{K(k_{e2})}{K'(k_{e2})}} \tag{5-2}
\]
where \( K(k) \) is the complete elliptic integral of the first kind with module \( k \) and \( K(k') \) its complement.

The asymptote of these equations when the ground plane width grows infinite (\( c \rightarrow \infty \)) agrees with the infinite ground plane case [5.2].

### 5.2.2 Odd Mode

The effective dielectric constants and characteristic impedance are given in equation 5-4 and 5-5.

\[
\varepsilon_{\text{eff, } O} = 1 + \frac{\left( \varepsilon_r - 1 \right) \left( \frac{K(k_{o1})}{K'(k_{o1})} + \frac{K(k_{o2})}{K'(k_{o2})} \right) + \left( \varepsilon_r - 1 \right) \frac{K(k_{o3})}{K'(k_{o3})}}{\frac{K(k_{o1})}{K'(k_{o1})} + \frac{K(k_{o2})}{K'(k_{o2})}} \quad (5-4)
\]

\[
Z_{00} = \frac{60\pi}{\sqrt{\varepsilon_{\text{eff, } O}}} \frac{1}{\left[ \frac{K(k_{o1})}{K'(k_{o1})} + \frac{K(k_{o2})}{K'(k_{o2})} + \frac{K(k_{o3})}{K'(k_{o3})} \right]} \quad (5-5)
\]

where
\[ k_{o1,1} = \frac{1}{\tanh\left(\frac{\pi \cdot W_2}{2H_1}\right) \cdot \tanh\left(\frac{\pi \cdot W_4}{2H_1}\right)} \]

\[ k_{o1,2} = \frac{1}{\tanh\left(\frac{\pi \cdot (W_1 - W_4)}{2H_1}\right) \cdot \tanh\left(\frac{\pi \cdot (W_1 - W_3)}{2H_1}\right)} \]  \hspace{1cm} (5-6)

\[ k_{o2} = k_{e2} \]

\[ k_{o3} = k_{e3} \]

\[ W_1, W_2, W_3, W_4 \text{ and } H_1 \text{ can be derived.} \]

\[ \frac{W_1}{H_1} = \frac{K(k_{o1})}{K'(k_{o1})} \]

\[ W_2 = F\left(\arcsin\left(\frac{\tanh\left(\frac{\pi \cdot b}{2h_1}\right) \cdot \tanh\left(\frac{\pi \cdot c}{2h_1}\right)}{k_{o1}}\right)\right) \]

\[ W_3 = F\left(\arcsin\left(\frac{\tanh\left(\frac{\pi \cdot b}{2h_1}\right)}{\tanh\left(\frac{\pi \cdot c}{2h_1}\right)}\right)\right) \]  \hspace{1cm} (5-7)

\[ W_4 = \frac{(W_2 + W_3)}{2} \]

where \( F(\phi, k) \) is the incomplete elliptic integral of the first kind, written in Jacobi’s notation.

The expression derived in this section can easily be extended to include infinite ground broadside coupled CPW.

**5.3. Numerical Results of Broadside Coupled Coplanar Waveguide (CPW)**

A even and odd mode characteristic impedance were calculated and compared in order to examine variations of signal line width, slot width, ground width and board dielectric constants. By extracting the even and odd mode characteristic impedance, the coupling factor can be easily determined. The coupling coefficient specification is essential for couplers, filters, transformers and baluns, using coupled line structures.
The analysis was verified with the aid of Matlab. Figure 5-3 shows even and odd mode characteristic impedances with a fixed dielectric height ($h_1 = 10 \, \text{um}$ and $h_2 = 15 \, \text{um}$) on a polyimide substrate ($\varepsilon_r = 3.5$). As the slot width get larger with the fixed ground width (50 \, \text{um}), the characteristic impedance gets higher since the effective dielectric constant get lower because the field distributes less extensively.

![Figure 5-3](image)

Figure 5-3. Calculated even and odd mode characteristic impedance with the slot width variation as a function of signal line width while the ground plane is fixed at 50 \, \text{um}.

Figure 5-4 shows the characteristic impedance variation depending on ground width change while the slot width is fixed at 10 \, \text{um} with a fixed dielectric height ($h_1 = 10 \, \text{um}$ and $h_2 = 15 \, \text{um}$) on polyimide substrate ($\varepsilon_r = 3.5$). For an even mode excitation, the characteristic impedance shows a bigger change than for the odd mode excitation because the electric field distributes more between the signal lines. The odd mode characteristic impedance is less affected since the ground width variation affects more the horizontal field distribution than the vertical field distribution. However, the coupling factor tends to change much rapidly than the variation.
rate of the even and odd mode characteristic impedance. The odd mode characteristic impedance will change to be larger if the signal line is on an inhomogeneous media. By increasing \( c \) to infinity, the equations for the finite ground broadside coupled CPW convert into the equations of the infinite ground broadside coupled CPW [5.10].

\[
\begin{align*}
\text{Slot width (b - a) } &= 20 \text{ um} \\
\text{h}_1 &= 10 \text{ um, } h_2 = 15 \text{ um}
\end{align*}
\]

Figure 5-4. Calculated even and odd mode characteristic impedance as a function of signal line width \((a)\) with 20mm finite slot width.

Figure 5-5 describes the coupling factor variation depending on slot width variation for the ground widths that are 100 um and the infinite ground width case. Slot width affects the coupling factor dramatically. By simple comparison between the finite ground width and infinite ground, Figure 5-5 displays the importance of the finite ground width analysis.
Figure 5-5. Calculated coupling factor with slot width variation as a function of signal line width for the cases of 100 \text{um} finite ground plane and infinite ground.

Table 5-1. Numerical and simulated coupling coefficients

<table>
<thead>
<tr>
<th>Signal width (2a)</th>
<th>Gap width (b-a)</th>
<th>GND width (c-b)</th>
<th>Numerical result (dB)</th>
<th>Simulated result (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 \text{um}</td>
<td>30 \text{um}</td>
<td>100 \text{um}</td>
<td>-4.757 dB</td>
<td>-4.627 dB</td>
</tr>
<tr>
<td></td>
<td>\infty</td>
<td>100 \text{um}</td>
<td>-5.704 dB</td>
<td>-5.604 dB</td>
</tr>
<tr>
<td></td>
<td>70 \text{um}</td>
<td>\infty</td>
<td>-3.129 dB</td>
<td>-3.0235 dB</td>
</tr>
<tr>
<td>50 \text{um}</td>
<td>30 \text{um}</td>
<td>100 \text{um}</td>
<td>-3.708 dB</td>
<td>-3.4836 dB</td>
</tr>
<tr>
<td></td>
<td>\infty</td>
<td>100 \text{um}</td>
<td>-4.237 dB</td>
<td>-4.1223 dB</td>
</tr>
<tr>
<td></td>
<td>70 \text{um}</td>
<td>\infty</td>
<td>-2.442 dB</td>
<td>-2.2295 dB</td>
</tr>
<tr>
<td>70 \text{um}</td>
<td>30 \text{um}</td>
<td>100 \text{um}</td>
<td>-3.06 dB</td>
<td>-2.8692 dB</td>
</tr>
<tr>
<td></td>
<td>\infty</td>
<td>100 \text{um}</td>
<td>-3.418 dB</td>
<td>-3.2188 dB</td>
</tr>
<tr>
<td></td>
<td>70 \text{um}</td>
<td>\infty</td>
<td>-2.02 dB</td>
<td>-1.952 dB</td>
</tr>
</tbody>
</table>
Through this analysis, the coupling coefficient for the Marchand balun is extracted and verified with 3D-EM simulator which uses the Finite Element Method (FEM). The simulation results are based on the frequency so that the coupling coefficients are chosen by the best value through all the specification frequency responses. Table 5-1 compares the numerical and simulated results of broadside coupled coplanar waveguides. Simulated results and numerical results show less than 0.2dB difference. However, the simulation takes a lot longer time than numerical results due to the complex mesh equations. The proposed equation saves the time and effort for finding initial design parameters.

5.4. Marchan Balun Implementation

The basic parameters were extracted from the analytic expression in a similar manner in the chapter 4. The characteristics of these broadside coupled line CPW does not affect on the frequency variation as long as the coplanar line works in the quasi-TEM mode. Generally, CPS and CPW can sustain the normal operation without serious loss up to 220GHz. Also, the dispersion of these CPS can be ignored due to a relatively thick metal layer. Rough calculation shows 200nm of skin depth in 100GHz operation. But this process metal thickness is around 5um. The broadside coupled CPW’s quarter wavelength is around 500um in 60GHz operation, which is verified through HFSS simulation. The baluns were integrated on a Cascade probe structure (GSSG with 150um pitch). This thin film process has relatively large process variation, especially in dielectric thickness. A general application of this process is the integration of the single or parallel coupled transmission lines with a lower ground plane. So, the ground of this process can not be considered as infinite ground due to the fact that there is no shielding or housing. The basic design parameters were extracted from the finite ground broadside coupled CPW’s analytic expression. The final design verification was performed with the aid of HFSS. In order to check the effect of the coupling coefficient variation in chapter 3, the baluns were
fabricated in 30, 50 and 70 \( \mu m \) coupled line widths with a 50 \( \mu m \) gap width between the signal line and the ground.

### 5.4.1 The Design Verification using HFSS

Figure 5-6 shows the schematic diagram of the Marchand balun using a broadside coupled CPW with a finite ground. An unbalanced port connects with coaxial cable for the connection to the test equipment while balanced ports touch the DUT with sharp probe tips. For an accurate measurement, the calibration is essential. The final verification was performed as close as possible to the actual environment, which means that air encloses this structure. The air region is set up as a radiation boundary in simulation.

Figure 5-6. Marchand balun integrated probe structure using finite ground broadside coupled lines

Figure 5-7 shows the simulation results. The results include the insertion loss (\( S_{21} \) and \( S_{31} \)) and the phase imbalance which are the most useful parameters to check the balun performance.
Compared to CPS cases, CPW shows better symmetric characteristic due to its symmetric ground plane at both sides.

Figure 5-7. Marchand balun structure using finite ground broadside coupled lines

5.4.2. Layout

Layouts of the Marchand balun integrated probe using broadside coupled CPW are shown in Figure 5-8. In an actual layout, the ground plane shape varies in order to fit the design into the original GSSG (150 um pitch) probe structure. For a 70 um signal line design, the gap width becomes small. The design of 30 um of the signal line width facilitates a -4.8 dB coupling coupler to get the best center frequency performance. The designs of 50 um and 70 um signal line widths result from considering the process variations. These two designs show around 3 dB and 2.5 dB coupling effects through the previous analysis. The connections to both DUT and COAX use 50 Ω microstrip lines for easy assembly. Layout was performed with L-Edit.
Figure 5-8 Actual layout of Marchand balun integrated probe using broadside coupled CPW.

Table 5-2 summarizes the fabricated design parameters. Transmission line width variation is to verify the width of the 50 Ω transmission line. The characterization is performed for one design due to the expensive probe prototyping expenses such as high frequency coaxial cable, probe tips connection etc. For one, at least two prototype designs are assembled to provide the measurement accuracy.

Table 5-2. Design parameter of the fabricated balun probe membrane

<table>
<thead>
<tr>
<th>Signal Width</th>
<th>Slot Width</th>
<th>Transmission Line Width</th>
<th>Tested Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 um</td>
<td>50 um</td>
<td>25 um</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>45 um</td>
<td>X</td>
</tr>
<tr>
<td>50 um</td>
<td>50 um</td>
<td>25 um</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
<td>45 um</td>
<td>O</td>
</tr>
<tr>
<td>70 um</td>
<td>50 um</td>
<td>25 um</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>45 um</td>
<td>X</td>
</tr>
</tbody>
</table>
5.5. Measured Results

Measurement is performed by the same method in chapter 4. The tested structure is the fabricated balun integrated probes whose signal line width, slot width are 50 \text{um} and 50 \text{um}. As shown in Figure 5-8, the integrated area is relatively small so that the ground width should be varied at specific location. A full wave simulator helps to compensate this discontinuity and helps to consider the transmission line transitions.

![Plot showing measured results of Marchand balun integrated probe.](image)

Figure 5-9. Measured results of Marchand balun integrated probe.

Measured results shows relatively good phase balance ranging through all measured frequencies. Insertion losses ($S_{21}, S_{31}$) from unbalanced to balanced port show a little deviation up to 90GHz and show a relatively large difference at 100GHz. Even though the balun is designed with a 60GHz center frequency, the measured center frequency is around 55GHz. Since the CPW uses twice the ground plane of the CPS, the unwanted parasitic capacitance causes the frequency shift. This effect is similar to capacitive loading. If the balanced port connects to a
capacitor such as large DUT pad, this capacitor increases the electrical length of the coupled line. So the electrical length can be considered longer than the original design in this case.

The relative bandwidth can be calculated by simply adapting the frequency at -4dB with center frequency. In this case, \( f_1, f_2 \) and \( f_0 \) are equal to 20GHz, 90GHz, and 55GHz, respectively.

\[
\text{Relative Bandwidth} = \frac{f_2 - f_1}{f_0} = 1.273
\]  

(5-8)

The homogeneous media which enhance the coupled line directivity and the tighter coupling factor cause this relatively wide bandwidth. This balun uses around a -2.5 dB coupled line to increase the bandwidth.

Figure 5-10 shows the comparison between the measured results and simulated results. The measured results show wider bandwidth than the simulated one does. Also, the measured and simulated \( S_{21} \) show a similar glitch around 80 GHz due to the introduction of another propagation mode than TEM mode. The coplanar waveguide shows a better symmetric characteristic around the center frequency than the coplanar stripline case. Generally, CPW
sustains TEM propagation mode better than CPS does due to its symmetric ground plane. The phase response shows stable behavior in the interested frequency range.

5.6. Conclusion

The Marchand balun integrated probes using broadside coupled coplanar waveguide are designed, fabricated and measured. The design parameters are determined by the proposed balun analysis in chapter 3. With the proposed parameter extraction method in Appendix B, it is possible to make a simple and accurate Marchand balun. A 3D EM simulator is employed to consider the discontinuity between the transmission lines for the final function verification. The measured results show a good agreement to the final simulation.
CHAPTER 6
EMBEDDED PHASE NOISE MEASUREMENT SYSTEM

6.1. Introduction to Phase Noise

Frequency sources include noise that appears to be a superposition of causally generated signals and random, nondeterministic noise. Thermal noise, shot noise, and noise of undetermined origin (such as flicker noise) are considered to be the random noise. The final result is time-dependent phase and amplitude fluctuations in the frequency source. Measurements of these fluctuations characterize the frequency source in terms of amplitude modulation (AM) and phase modulation (PM) noise.

Frequency stability can be defined as the degree to which an oscillating source produces the same frequency throughout a specified period of time. Every RF and microwave source exhibits some amount of frequency instability. This stability can be divided into two components- long-term and short-term stability. It is implicit in this general definition of frequency stability that the given frequency stability decreases if anything except a perfect sine function is the signal wave shape.

Long-term stability describes the frequency variations that occur over long time periods, expressed in parts per million per hour, day, month or year. Short-term frequency stability contains all elements causing frequency changes about the nominal frequency of less than a few seconds duration [6.1].

Phase noise is the term most widely used to describe the characteristic randomness of frequency stability. The spectral purity refers to the ratio of signal power to phase-noise sideband power. Measurements of phase noise and AM noise are performed in the frequency domain using a spectrum analyzer that provides a frequency window following the detector (double
balanced mixer). Frequency stability can also be measured in the time domain with a gated counter that provides a time window following the detector.

Mathematically, an ideal sinewave can be described by

\[ V(t) = V_0 \sin(2\pi f_c t) \quad (6-1) \]

where \( V_0 \), \( 2\pi f_c \) and \( f_c \) are nominal amplitude, linearly growing phase component and nominal frequency, respectively.

However, a real signal is better modeled by

\[ V(t) = (V_0 + \varepsilon(t))\sin(2\pi f_c t + \Delta\phi(t)) \quad (6-2) \]

where \( \varepsilon(t) \) and \( \Delta\phi(t) \) are amplitude fluctuations and randomly fluctuation phase terms (phase noise) [6.2].

---

**Figure 6-1.** RF sideband spectrum from spectrum analyzer with deriving \( L(f_m) \).

This randomly fluctuating phase terms could be observed on an ideal spectrum analyzer (one which had no sideband noise of its own) as shown in Figure 6-1. There are two kinds of
fluctuating phase terms. The deterministic terms are discrete signals appearing as distinct components in the spectral density plot. These signals which usually are called spurious, can be related to known phenomena in the signal source such as power line frequencies, vibration frequencies, or mixer products.

The second kind of phase instability is random in nature, and is commonly considered as phase noise. The source of random sideband noise in an oscillator includes thermal noise, shot noise, and flicker noise. Many terms exist to quantify the characteristic randomness of phase noise. Essentially, all methods measure the frequency or phase deviations of the source under test in either the frequency or time domain. Since frequency and phase are related to each other, all of the terms that characterize phase noise are also related.

One fundamental description of phase instability (phase noise) is the spectral density of phase fluctuations on a per-Hertz basis. The spectral density defines the energy distribution as a continuous function, expressed in units of phase variance per unit bandwidth. Thus $S_{\phi}(f_m)$ may be considered as

$$S_{\phi}(f_m) = \frac{\Delta\phi_{\text{rms}}^2(f_m)}{BW} \text{rad}^2 \text{Hz}$$

(6-3)

where BW(bandwidth) is negligible with respect to any changes in $S_{\phi}$ versus the Fourier frequency or offset frequency $f_m$.

One of useful measure of noise energy is $\mathcal{L}(f_m)$, which is then directly related to $S_{\phi}(f_m)$ by a simple approximation which has generally negligible error if the modulation sidebands are such that the total phase deviations are much less than 1 radian ($\Delta\phi_{pk} \ll 1$ radian).

$$\mathcal{L}(f_m) = \frac{S_{\phi}(f_m)}{2}$$

(6-4)
\( \mathcal{L}(f_m) \) is an indirect measurement of noise energy related to the RF power spectrum which is observed on a spectrum analyzer. Figure 6-1 shows that the U.S. National Bureau of Standards defines \( \mathcal{L}(f_m) \) as the ratio of the power in one phase modulation sideband to the total signal power (at an offset \( f_m \) Hertz away from the carrier). The phase modulation sideband is based on per Hertz of bandwidth spectral density and \( f_m \) equals the Fourier frequency or offset frequency.

\[
\mathcal{L}(f_m) = \frac{P_{ssb}}{P_s} = \frac{\text{power density (in one phase modulation sideband)}}{\text{total signal power}} = \text{single sideband (SSB) phase noise to carrier ratio per Hz}
\]

(6-5)

Phase noise generally uses the logarithm as a spectral density of the phase modulation sidebands in the plot of the phase-frequency domain, expressed in dB relative to the carrier per Hz (dBc/Hz) as in Figure 6-2.

![Figure 6-2. \( \mathcal{L}(f_m) \) which is described logarithmically as a function of offset frequency.](image)

The spectral density of frequency fluctuations \( (S_{\Delta f}(f_m)) \) is also used for quantifying short term frequency instability (phase noise). The spectral density defines the energy distribution as a continuous function, expressed in units of frequency variance per unit bandwidth. Equation 6-6 describes \( S_{\Delta f}(f_m) \).
\[ S_{\Delta f}(f_m) = \frac{\Delta f_{rms}^2(f_m)}{BW \text{ used to measure } \Delta f_{rms}} \]  

(6-6)

where BW is negligible with respect to any changes in \( S_{\phi} \) versus \( f_m \).

Frequency is the time rate of change of phase, so that the three common terms (\( S_{\phi}(f_m) \), \( S_{\Delta f}(f_m) \), and \( S_{\Delta f}(f_m) \)) have a relationship as shown equation 6-7 and 6-8.

\[ S_{\phi}(f_m) = \frac{S_{\Delta f}(f_m) \ rad^2}{f_m \ Hz} \]  

(6-7)

\[ \mathcal{L}(f_m) = \frac{S_{\Delta f}(f_m)}{2f_m^2} \]  

(6-8)

A frequency discriminator outputs a voltage directly proportional to \( S_{\Delta f}(f_m) \). \( S_v(f_m) \) is the power spectral density of the voltage fluctuations out of the detection system. For small BW, may be considered as shown in equation 6-9.

\[ S_v(f_m) = \frac{\Delta V_{rms}^2(f_m)}{BW \text{ used to measure } \Delta V_{rms}} \]  

(6-9)

Because of the large magnitude variations of the phase noise on an oscillator, it is convenient to talk about phase noise in logarithmic terms.

Logarithm expression of \( S_{\Delta f}(f_m) \) is shown in equation 6-10.

\[ S_{\Delta f}(f_m) \left[ \frac{dBHz}{Hz} \right] = 20\log \frac{\Delta f(Hz)}{1(Hz)} \text{ per Hz} \]  

(6-10)

Logarithm expression of \( S_{\phi}(f_m) \) is shown in equation 6-11.

\[ S_{\phi}(f_m) \left[ \frac{dB}{Hz} \right] = 20\log \frac{\Delta \phi(rad)}{1(rad)} \text{ per Hz} \]  

(6-11)

Logarithm expression of \( \mathcal{L}(f_m) \) is shown in equation 6-12.
\[ \mathcal{L}(f_m) \left[ \frac{dBc}{Hz} \right] = 10 \log \frac{P_{noise}}{P_{carrier}} \text{ per Hz} \] (6-12)

Therefore, the relationship between \( S_{\phi}(f_m) \), \( \mathcal{L}(f_m) \), and \( S_{\Delta f}(f_m) \) can be described as shown in equation 6-13 and 6-14.

\[ S_{\phi}(f_m) \left[ \frac{dBr}{Hz} \right] = S_{\Delta f}(f_m) \left[ \frac{dBHz}{Hz} \right] - 20 \log \frac{f_m(Hz)}{1(Hz)} \] (6-13)

\[ \mathcal{L}(f_m) \left[ \frac{dBc}{Hz} \right] = S_{\Delta f}(f_m) \left[ \frac{dBHz}{Hz} \right] - 20 \log \frac{f_m(Hz)}{1(Hz)} - 3 \text{ dB} \] (6-14)

where dBHz/Hz is dB relative to one Hz per Hz bandwidth, dBr/Hz is dB relative to one radian per Hz bandwidth, and dBC/Hz is dB relative to a carrier per Hz bandwidth [6.2].

### 6.2. Phase Noise Modeling of an Oscillator

#### 6.2.1. Basics of Oscillators

![Conventional Oscillator Block Diagram](image)

Figure 6-3. Conventional Oscillator Block Diagram.

The basic idea of an oscillator is to convert dc power to a periodic, sinusoidal RF output signal. Though all oscillators need a nonlinear description of their behavior a linear approach is sufficient for their analysis and design. The block diagram below includes all necessary components of an oscillator. This block diagram is composed of an amplifier with a frequency dependent gain \( G(j\omega) \) and a frequency dependent feedback network \( H(j\omega) \). The feedback network is the resonator circuit with quality factor \( Q \). The resonating circuit has losses due to the
finite quality factor and can be modeled as a parallel RLC resonance circuit as shown in Figure 6-4 [6.3].

![Parallel Resonance Circuit](image)

The inductor $L$ and the capacitor $C$ determine the resonance frequency and the resistor $R$ represents the losses in the circuit. The resistor $R$ determines the $Q$ of the resonator. The impedance of the circuit looking at the input port can be described below.

$$Z_{in} = \left( \frac{1}{R} + \frac{1}{j\omega L} + j\omega C \right)^{-1}$$  \hspace{1cm} (6-15)

The resonance frequency can be established when the imaginary part of equation 6-15 is equal to zero. This means that the maximum amount of energy is oscillating between the inductor and capacitor. The oscillation frequency is below.

$$\frac{1}{\omega_c C} = \omega_c L$$  \hspace{1cm} (6-16)

and the resonance frequency can be described as shown in equation 6-17.

$$\omega_c = \frac{1}{\sqrt{LC}}$$  \hspace{1cm} (6-17)

The $Q$ is defined as the bandwidth of the resonance graph as shown in Figure 6-5. The $Q$ for a resonator with losses described by the resistance $R$ can be modeled as shown in equation 6-18.
$$Q = \frac{R}{\omega L} = \omega CR \quad (6-18)$$

![Figure 6-5. Normalized bandwidth of a resonator.](image)

The transfer function for a conventional oscillator block can be derived as

$$\frac{V_o}{V_{in}} = \frac{G(j\omega)}{1 + G(j\omega)H(j\omega)} \quad (6-19)$$

For an oscillator, $V_o$ is nonzero when $V_{in}$ is equal to zero, the oscillation condition can be extracted as shown in equation 6-20 and 6-21.

$$|G(j\omega)H(j\omega)| = 1 \quad (6-20)$$

$$\arg[G(j\omega)H(j\omega)] = 180^\circ \quad (6-21)$$

These magnitude and phase conditions have to be fulfilled to get stable oscillation at the output of the oscillator [6.4].

### 6.2.2. Leeson’s Phase Noise Model

Dating back to 1966, D. B. Leeson published a model for describing the output noise behavior of a feedback oscillator. This model is historic but still is in use for estimating the output spectral density of the phase noise of an oscillator. Assuming that the output in Figure 6-4...
is the voltage across the tank circuit, the only source of noise is the white thermal noise of the
tank conductance. It can be represented as a current source across the parallel resonance circuit
with a mean-square spectral density of equation 6-22.

\[
\frac{\bar{I}_n^2}{\Delta f} = \frac{4kT}{R} \quad (6-22)
\]

This current noise becomes voltage noise when multiplied by the effective impedance
looking into the current source. By considering that the energy restoration element must
contribute an average effective negative resistance that precisely cancels the positive resistance
of the parallel resonance circuit, the effective impedance looking into the noise current source is
the same as the impedance of a perfectly lossless LC network. But at resonance, this is zero. For
a relatively small offset frequency \(\Delta \omega\) from the center frequency \(\omega_c\), the impedance of an LC
resonance circuit is approximately described by equation 6-23.

\[
Z\left(\omega_c + \Delta \omega\right) \approx -j \frac{\omega_c L}{2\Delta \omega/\omega_c} \quad (6-23)
\]

By using the definition of quality factor \(Q\), the impedance of an LC resonance circuit
yields equation 6-24.

\[
\left|Z\left(\omega_c + \Delta \omega\right)\right| \approx -R \frac{\omega_c}{2Q\Delta \omega} \quad (6-24)
\]

Then, the spectral density of the mean-square noise voltage can be obtained by multiplying
the spectral density of the mean-square noise current with the squared magnitude of the
impedance of an LC resonance circuit.

\[
\frac{\bar{V}_n^2}{\Delta f} = \frac{\bar{I}_n^2}{\Delta f} \left|Z\right|^2 = 4kTR \left(\frac{\omega_c}{2Q\Delta \omega}\right)^2 \quad (6-25)
\]
The power spectral density of the output noise is frequency-dependent. This $1/f^2$ behavior represents the two facts. The first is that the voltage frequency response of an LC resonance circuit rolls off as $1/f$ to either side of the center frequency. The second is the power is proportional to the square of voltage. An increase of an LC resonance circuit’s $Q$ reduces the noise density with all other parameters constant [6.5].

Thermal noise causes fluctuations in both amplitude and phase as shown in equation 6-25. Noise energy would split equally into amplitude and phase noise without amplitude limiting that occurs in real circuits. However, amplitude limiting mechanisms are present in all practical oscillators so that the amplitude noise will be attenuated. In order to quantify this noise level, it is conventional to normalize the mean-square noise voltage density to the mean-square carrier voltage in decibels. This normalization expresses the following phase noise equation.

$$\mathcal{L}(f_m)\left[\frac{dBc}{Hz}\right] = 10\log \frac{P_{\text{noise}}}{P_{\text{carrier}}} \text{ per Hz} = 10\log \left[ \frac{2kT}{P_{\text{carrier}}} \left( \frac{\omega_c}{2Q\Delta\omega} \right)^2 \right]$$ \hspace{1cm} (6-26)

However, equation 6-26 requires many simplifying assumptions so that there are some significant differences between the spectrum by equation 6-26 and the real oscillator spectrum. To solve this discrepancy, a modification to equation 6-26 is shown in equation 6-27. [6.5].

$$\mathcal{L}(f_m)\left[\frac{dBc}{Hz}\right] = 10\log \left[ \frac{2FkT}{P_{\text{carrier}}} \left( 1 + \frac{\omega_c}{2Q\Delta\omega} \right)^2 \left( 1 + \frac{\Delta\omega \sqrt{f_m^2/f^3}}{\Delta\omega} \right) \right]$$ \hspace{1cm} (6-27)

These modifications consist of a factor $F$ to account for the increased noise in the $1/(f_m)^2$ region, an additive factor of unity to account for the noise floor, and a multiplicative factor to provide a $1/|f_m|^3$ behavior at sufficiently small offset frequency. This modification is described in Figure 6-6.
The Leeson’s model is extremely important for intuitive insight. However, it should be noted that the factor $F$ is an empirical fitting parameter and must be determined from measurement, diminishing the predictive power of the phase noise equation. Also, the $1/f$ corner of device noise is not precisely equal to $(f_m)^{1/3}$ in practice.

6.3. Phase Noise Measurement Methods

This chapter describes three different methods for measuring phase noise. The purpose is to show the complexity of the measurement and derive the necessary equation to determine the single sideband phase noise. Finally, the proper method is chosen for an embedded phase noise measurement system.

6.3.1. Direct Measurement

The most simple and straightforward method of phase noise measurement is to input the test signal into a spectrum analyzer, directly measuring the power spectral density of the oscillator. However, this method may be significantly limited by the spectrum analyzer’s
dynamic range, resolution, and LO phase noise. Though this direct measurement is not useful for measurements close-in to a drifting carrier, it is convenient for qualitative quick evaluation on sources with relatively high noise. The measurement is valid if the following conditions are met. The first is that the spectrum analyzer SSB phase noise at the offset of interest must be lower than the noise of the Device-Under-Test (DUT). The second condition is that since the spectrum analyzer will measure total noise power, the amplitude noise of the DUT must be significantly below its phase noise (Typically 10dB will suffice) [6.2]

Figure 6-7 shows a typical display of an oscillator mixed down to DC. The main advantage of this method is its simple test set-up and that it can measure phase noise at high offset frequencies from the carrier. However, there are several disadvantages. One is that the spectrum analyzer can not distinguish a difference between amplitude noise and phase noise when one does not have any idea regarding the noise power in the amplitude and phase of a DUT. Finally, some correction factors have to be incorporated in order to compensate the phase noise power since the phase noise power is normalized to a bandwidth of 1Hz in an ideal rectangular filter but the resolution bandwidth filter of the spectrum analyzer is non-ideal.

Figure 6-7. SSB phase noise with direct measurement method.
6.3.2. PLL-based Measurement (Two oscillator method)

The PLL-based method is the most sensitive of all methods. Two oscillators send signals to the two RF ports of a mixer. The IF signal of a mixer passes through a low pass filter to keep out the sum frequency components and then sends them back in a small bandwidth’s signal to lock one oscillator to the other. The fundamental block diagram is shown in Figure 6-8. The basis of this method is the double-balanced mixer is used as a phase detector.

Figure 6-8. Basic diagram of PLL-based phase noise measurement system

Two signals at identical frequencies and nominally in phase quadrature (90° out of phase) are input to the phase detector (double balanced mixer). At quadrature, the output of the phase detector is a difference frequency of 0 Hz and an average voltage output of 0 V. There is a small fluctuation voltage, $\Delta V$. For small phase deviations ($\Delta \phi \ll 1$ rad), this fluctuating voltage is proportional to the fluctuating phase difference between the two signals. This phase difference represents the combined phase modulation sidebands of the two input signals. When the two input signals are identical in frequency and in phase quadrature, the output of the phase detector is a voltage directly proportional to the combined phase modulation sidebands of the two input signals.

The frequency and amplitude offsets are then removed such that the two input signals are again at identical frequencies, and are set in phase quadrature. It is important to use the mixer in
its linear region where the voltage output is directly proportional to the phase difference of the input signals by a constant \( A \) as shown in equation 6-28.

Figure 6-9 shows a typical mixer-phase detector characteristic. The mixer produces a output voltage \( V(t) \) proportional to the fluctuating phase difference between the two input signals \( \phi_{LO} - \phi_{RF} \). The point of maximum phase sensitivity and the center of the region of most linear operation occur where the phase difference between the two inputs is equals to 90° or phase quadrature.

![Figure 6-9. Conventional double-balanced mixer characteristic.](image)

In order to understand how a mixer operates as a phase detector, we need examination of a normal mixer output as shown in Figure 6-9.

![Figure 6-10. Mixer operation](image)
The output of the mixer $V_{IF}(t)$ is the product of the two signals.

$$V_{IF}(t) = AV_d \cos\left((\omega_r - \omega_d)t + \phi(t)\right) + AV_r \cos\left((\omega_r + \omega_d)t + \phi(t)\right) + ...$$  \hspace{1cm} (6-28)

The low pass filter will remove the higher frequency components, leaving $V(t)$.

$$V(t) = AV_d \cos\left((\omega_r - \omega_d)t + \phi(t)\right)$$  \hspace{1cm} (6-29)

Let the peak amplitude of $V(t)$ be defined as $V_{b,\text{peak}}$ (peak voltage of the beat signal), equal to $AV_d$, where $A$ is the mixer efficiency.

$$V(t) = \pm V_{b,\text{peak}} \cos\left((\omega_r - \omega_d)t + \phi(t)\right)$$  \hspace{1cm} (6-30)

When operating the mixer as a phase detector, the input signals must be at the same frequency and 90 degrees out of phase.

$$\omega_d = \omega_r \text{ and } \phi(t) = (k + 1)\frac{\pi}{2} + \Delta\phi(t), \text{ } k = 1,2,3,...$$  \hspace{1cm} (6-31)

The output of the mixer at quadrature is expressed by

$$\Delta V(t) = \pm V_{b,\text{peak}} \sin\left(\Delta\phi(t)\right) \approx \pm V_{b,\text{peak}} \Delta\phi(t) \text{ for } \Delta\phi_{\text{peak}} \ll 1 \text{ radian}$$  \hspace{1cm} (6-32)

where $\Delta V(t)$ is instantaneous voltage fluctuations around 0 V, and $\Delta\phi(t)$ is instantaneous phase fluctuations.

This yields a direct linear relationship between the voltage fluctuations at the mixer output and the phase fluctuations of the input signals.

$$\Delta V = K_m \Delta\phi$$  \hspace{1cm} (6-33)

where $K_m = V_{b,\text{peak}}$ = mixer constant(volts/radian), which is equal to the slope of the mixer sine wave output at the zero crossings.

The voltage output of the mixer as a function of frequency will be directly proportional to the input phase deviations.
\[ \Delta V(f) = K_m \Delta \phi(f) = \sqrt{2} V_{b,rms} \Delta \phi(f) \]  

(6-34)

Then, \( \Delta \phi_{rms}(f) \) measured on the spectrum analyzer is,

\[
S_{\Delta \phi}(f) = \frac{\Delta \phi_{rms}^2}{\text{bandwidth used to measure } \Delta \phi_{rms}} \left( \frac{\text{rad}^2}{\text{Hz}} \right)
\]  

(6-35)

Therefore,

\[
S_{\Delta \phi}(f) = \Delta \phi_{rms}^2(f) = \frac{1}{2} \frac{\Delta V_{rms}^2}{V_{b,rms}^2} \text{ (in 1 Hz measurement bandwidth)}
\]  

(6-36)

The final phase noise equations is below

\[
\mathcal{L}(f) = \frac{1}{2} S_{\Delta \phi}(f) = \frac{1}{4} \frac{\Delta V_{rms}^2}{V_{b,rms}^2} \text{ (in 1 Hz measurement bandwidth)}
\]  

(6-37)

In this measurement method, the phase quadrature is the point of maximum phase sensitivity and the region of most linear operation. Any small deviation from quadrature results in a measurement error. Table 6.1 shows the typical error table of PLL based phase noise measurement system (Agilent 11729B phase noise measurement system) [6.7],[6.8].

<table>
<thead>
<tr>
<th>Offset from quadrature</th>
<th>Measurement Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>1°</td>
<td>-0.001dB</td>
</tr>
<tr>
<td>3°</td>
<td>-0.01dB</td>
</tr>
<tr>
<td>10°</td>
<td>-0.13dB</td>
</tr>
</tbody>
</table>

The PLL-based method has several advantages and disadvantages.

- A smaller spectrum analyzer dynamic range is necessary after converting the RF signal to the baseband signal.
• The internal noise of the spectrum analyzer is not the limiting factor. A low noise preamplifier is used to amplify the baseband signal to meet the range of the spectrum analyzer.

• The mixer operating as a phase detector is suppressing the amplitude noise due to its quadrature input condition in this setup. Good mixers achieve an AM noise suppression from 30~40dB.

• The measurement result is 3dB higher for the case of two identical sources, since the DUT and reference have the same characteristic.

• The reference source is a high stable oscillator that is the limiting factor of the test setup.

• The only disadvantage is the need for two sources in this test setup.

6.3.3. FM Discriminator (delay-line based) Measurement (One oscillator method)

It is important to first identify the two types of noise present in a frequency source: AM noise and phase noise. Phase noise, generally considered to be the dominant form of random noise, is defined as the noise generated from random fluctuations in the phase of a frequency source. AM noise is simply the noise generated from random fluctuations in the amplitude of a frequency source.

Delay line discriminators are only capable of measuring phase based random noise, and are in fact insensitive to AM noise. This can be an important advantage when measuring the phase noise of sources which do have significant AM noise.

Unlike the PLL based method, a frequency discriminator method (delay line method) does not require a second reference signal phased locked to a DUT. This makes the frequency discriminator method extremely useful for measuring DUTs that are difficult to phase lock. It can also be used to characterize sources with high-level, low-rate phase noise, or high close-in spurious sidebands, which can impose serious problems for the PLL based method.
The delay line implementation of the frequency discriminator converts short-term frequency fluctuations ($\Delta f$) of DUT into voltage fluctuations ($\Delta V$) that can be measured using a baseband analyzer. The conversion is two part process, first converting the frequency fluctuations into phase fluctuations and then converting the phase fluctuations to voltage fluctuations as shown in Figure 6-11.

The frequency fluctuation to phase fluctuation transformation ($\Delta f \rightarrow \Delta \phi$) takes place in the delay line. The nominal frequency arrives at the double-balanced mixer at a particular phase. As the frequency changes slightly, the phase shift incurred in the fixed delay time will change proportionally. The delay line converts the frequency change at the line input to a phase change at the line output when compared to the un-delayed signal arriving at the mixer in the second path. The double-balanced mixer transforms the instantaneous phase fluctuations into voltage fluctuations ($\Delta \phi \rightarrow \Delta V$). With the two input signals 90° out of phase, the voltage output is proportional to the input phase fluctuations [6.2].

In order to understand the function of the delay line as a discriminator, let us investigate the process of differentiation implemented by a time-delay line as shown in Figure 6-12.

The signal $y(t)$, which is the input to the output, is given by equation 6-38.
Figure 6-12. Discriminator implementation using time delay [6.9]

\[ y(t) = x_r(t) - x_r(t - \tau) \]  \hspace{1cm} (6-38)

which can be written

\[ \frac{y(t)}{\tau} = \frac{x_r(t) - x_r(t - \tau)}{\tau} \]  \hspace{1cm} (6-39)

Since, by definition,

\[ \lim_{\tau \to 0} \frac{y(t)}{\tau} = \lim_{\tau \to 0} \frac{x_r(t) - x_r(t - \tau)}{\tau} = \frac{dx_r(t)}{dt} \]  \hspace{1cm} (6-40)

it follows that for small \( \tau \),

\[ y(t) \approx \tau \frac{dx_r(t)}{dt} \]  \hspace{1cm} (6-41)

Through the delay-line discriminator, the voltage fluctuations can then be measured by the spectrum analyzer and converted to phase noise units.

The output voltage of DUT is in equation 6-42.

\[ V_{out,\text{DUT}}(t) = V_m \cos(\omega t + \delta \phi(t)) \]  \hspace{1cm} (6-42)

The signals passing the delay line and phase shifter are shown in equation 6-43 and 6-44 under the assumption that the amplitude fluctuation is negligibly small.

\[ V_{out,\text{delay line}}(t) = A_D V_m \cos(\omega(t - \tau_d) + \delta \phi(t - \tau_d)) \]  \hspace{1cm} (6-43)

\[ V_{out,\text{phase shifter}}(t) = A_p V_m \cos(\omega t + \delta \phi(t) + \phi) \]  \hspace{1cm} (6-44)
After mixing the two signals, the output is the multiplied form of the two signals. After traveling through a low pass filter, the higher order term is removed. By use of a quadrature monitor, \((\omega_0 \tau_d - \phi)\) can be adjusted to 90°. Then the final form can be derived as shown equation 6-45:

\[
V_{out}(t) = A_p A_d A_m V_m^2 \cos(\omega(t - \tau_d) + \delta \phi(t - \tau_d)) \cos(\omega t + \delta \phi(t) + \phi) \\
\approx K_\phi \cos(\omega \tau_d - \delta \phi(t - \tau_d) + \delta \phi(t) - \phi) \\
= K_\phi \left\{ \cos(\omega \tau_d - \phi) \cos(-\delta \phi(t - \tau_d) + \delta \phi(t)) - \sin(\omega \tau_d - \phi) \sin(-\delta \phi(t - \tau_d) + \delta \phi(t)) \right\} (6-45) \\
\approx -K_\phi \sin(-\delta \phi(t - \tau_d) + \delta \phi(t)) = K_\phi \sin\left(\tau_d \frac{d \delta \phi(t)}{dt}\right) \\
= K_\phi \sin(\tau_d \delta \omega(t)) \approx K_\phi \tau_d \delta \omega(t) = K_\phi 2\pi \tau_d \delta f(t)
\]

With the assumption that \(\delta f\) is zero-mean random signal, the mean square value of \(V_{out}\) is below:

\[
V_{out, rms}^2(t) = (K_\phi 2\pi \tau_d)^2 \delta f_{rms}^2(t) \rightarrow V_{out, rms}^2(f_m) = (K_\phi 2\pi \tau_d)^2 \delta f_{rms}^2(f_m) (6-46)
\]

The power spectral density of the frequency noise is below:

\[
V_{out, rms}^2(f_m) = (K_\phi 2\pi \tau_d)^2 \delta f_{rms}^2(f_m) = (K_\phi 2\pi \tau_d)^2 2f_m^2 \left( \frac{\delta f_{rms}^2(f_m)}{2f_m^2} \right) \\
= (K_\phi 2\pi \tau_d)^2 2f_m^2 \mathcal{L}(f_m) (6-47)
\]

Finally, the power spectral density of the phase noise is described in equation 6-48.

\[
\mathcal{L}(f_m) = \frac{V_{out, rms}^2(f_m)}{2(K_\phi 2\pi f_m \tau_d)^2} \text{(in 1 Hz measurement bandwidth)} (6-48)
\]

The system sensitivity is closely related to delay time as shown in equation 6-48. As the delay time increases, the sensitivity is better. In order to get a proper sensitivity, the delay line should be long enough since the delay time is inversely proportional to the phase noise [6.10] [6.11].
6.4. Embedded Phase Noise Measurement System

The delay-line based phase noise measurement method is implemented as the embedded phase noise measurement system on standard CMOS thanks to its simple structure compared to PLL-based system. Building a PLL for the phase noise measurement is considerably more difficult due to the considerations of locking range and large area system components.

However, there are two possible methods to implement a delay line technique. One is that the delay line and phase shifter use separate signal paths. Another is that the delay line and phase shifter use the same signal path. The two possible implementations share the same frequency discriminator transfer response as long as the system uses a passive delay line and a phase shifter, which do not generate additional noise for the whole system. However, if one converts the passive elements into a system with active elements, the two possible implementations show a different system noise floor.

By considering the system noise analysis of the two possible frequency discriminator system implementations, the proposed embedded phase noise measurement system will be design as the superior configuration.

6.4.1. FM discriminator system noise analysis

![Diagram](image)

Figure 6-13. Linearized noise model of a delay line frequency discriminator method in case that the delay line and phase shifter share the same signal path.
\( V^2_{n,\text{out}} \) can be derived by independently summing up the different noise sources. \( V^2_{n,\text{out}} \) is located right after low pass filter.

\[
V^2_{n,\text{out}} = V^2_{n,\text{MIX}} + V^2_s K^2_{\text{mixer}} \left( K^2_{\text{PS}} v^2_{n,\text{DLY}} + v^2_{n,\text{PS}} \right)
\]  

(6-49)

where \( V_s \) is the amplitude of DUT generated signal.

The resulting system noise floor can be described as equation (6.50).

\[
\mathcal{L}_{\text{system}} \left( f_m \right) = \frac{V^2_{n,\text{out}} \left( f_m \right)}{2 \left( K_m 2\pi f_m \tau_d \right)^2} = \frac{V^2_{n,\text{MIX}} + V^2_s K^2_{\text{mixer}} \left( K^2_{\text{PS}} v^2_{n,\text{DLY}} + v^2_{n,\text{PS}} \right)}{2 \left( K_m 2\pi f_m \tau_d \right)^2} = \frac{1}{2 \left( 2\pi f_m \tau_d \right)^2} \left( \frac{V^2_{n,\text{MIX}}}{V^2_s K^2_{\text{mixer}}} + \left( K^2_{\text{PS}} v^2_{n,\text{DLY}} + v^2_{n,\text{PS}} \right) \right)
\]

(6-50)

where \( K_m = V_s K_{\text{mixer}} K_{\text{PS}} \) is the overall system gain, \( K_{\text{mixer}} \) is the mixer gain and \( K_{\text{PS}} \) is the phase shifter gain.

Figure 6-14. Linearized noise model of the delay line frequency discriminator method in case that the delay line and phase shifter use different signal paths.

\( V^2_{n,\text{out}} \) can be derived by independently summing up the different noise sources. \( V^2_{n,\text{out}} \) is located right after low pass filter.

\[
V^2_{n,\text{out}} = V^2_{n,\text{MIX}} + V^2_s K^2_{\text{mixer}} \left( v^2_{n,\text{DLY}} v^2_{n,\text{PS}} \right)
\]

(6-51)
where $V_s$ is the amplitude of DUT generated signal.

The resulting system noise floor can be described as equation 6-52.

$$
\mathcal{L}_{\text{system}}(f_m) = \frac{V_{n,\text{out}}^2(f_m)}{2\left(K_m2\pi f_m\tau_d\right)^2} = \frac{V_{n,MIX}^2 + V_s^2K_m^2\left(V_{n,\text{DLY}}^2 + V_{n,PS}^2\right)}{2\left(K_m2\pi f_m\tau_d\right)^2} = \frac{1}{2\left(2\pi f_m\tau_d\right)^2}\left(\frac{V_{n,MIX}^2}{V_s^2K_m^2} + \left(V_{n,\text{DLY}}^2 + V_{n,PS}^2\right)\right)
$$

(6-52)

where $K_m=V_sK_{\text{mixer}}$ is the overall system gain, $K_{\text{mixer}}$ is the mixer gain.

Equation 6-52 will show lower noise floor than equation 6-50. The multiplication of the noise signal power can reduce the overall noise power compared to the sum of noise signal power with cross-correlation. Particularly, the proposed system uses an active phase shifter which contains an inherent amplification because the active phase shifter adapts a variable delay line structure based on a differential inverting amplifier.

Through the simple noise analysis shown, the FM discriminator system using different signal paths for the delay line and phase shifter is chosen due to its lower system noise floor compared to the case of using the same signal path.

Also, the noise analysis implies system consideration to reduce the system noise floor. The higher mixer gain reduces the system noise floor as shown in equation 6-52.
6.4.2. Proposed Embedded Phase Noise Measurement System

The embedded phase noise measurement system adapts to a delay-line based phase noise measurement system in Figure 6-15. The main difference is that the delay-line is replaced with a delay cell to get enough delay time and save chip area. The transmission line based delay line might be best for this application. However, the transmission line needs a considerably longer line to achieve greater than 1ns delay time with transmission line such as a coaxial cable or a coplanar waveguide. Also, this long line attenuates the signal considerably. Also, a lumped element delay cell (i.e. LC ladder filter) also needs several hundred stages to achieve enough delay time and can add resistive noise. Particularly, a LC ladder filter has a cutoff frequency which is relatively small compared to transmission line. Lower cutoff frequency achieves a bigger delay per stage for the LC ladder filter but the delay time per stage will still be considerably short for this application. By considering chip area and achievable delay time, the differential inverting amplifier is chosen for the delay cell circuit. However, the delay cell circuit
uses active devices which are different from transmission line or LC ladder network. Therefore, the active device noise contribution should be considered for the system operation.

A phase shifter also can be designed as a lumped-element structure with variable capacitance. A lumped-element phase shifter is fixed at a narrow operational frequency and has very limited phase shift capability. This new system aims to achieve DC~2 GHz oscillator phase noise measurement. Thus, a wide phase shifting ability is a key feature so that the phase shifter also is implemented using variable delay cell.

In a commercial measurement system such as an Agilent E5500, the phase quadrature is adjusted manually by watching the quadrature monitor. Thus, this system’s accuracy will be degraded due to the inconvenience of adjusting a perfect quadrature condition at different frequency measurements. Also, the user should watch the quadrature monitor to control it continually during the measurement.

In this work, the system is able to control the phase quadrature automatically. By comparing the output dc voltage level with its reference voltage, the adjustment unit controls the phase shifter to maintain the phase quadrature. If the mixer does not operate in phase quadrature, the output signal power is large enough to make an adjustment at a very small phase discrepancy. The adjustment unit controls the phase shifter (which is a voltage controlled inverting amplifier) depending on the comparator output.

6.5. System Level verification of the Embedded Phase Noise Measurement System

In order to verify the system functionality, a system level simulation is performed with Agilent ADS. The purpose of this effort is to verify the embedded phase noise measurement system. A DUT generates a noisy signal (white noise) at a specific frequency. A delay line (which will be implemented by the CMOS delay cells) and phase shifter generate the planned time delay (which is phase shift at both outputs) and time delayed signal. The mixer works like
analog multiplier to function as a phase detector. A final active low pass filter filters out higher order signals with specific gains. The remaining signal is located at DC with a noisy sideband which is similar to the baseband signal. Therefore, the simulation focuses on exploring this noise sideband. In actual circuitry, this signal is detected as voltage components in time domain. In order to see the noise sideband, a Fourier Transform (FFT or DFT) which consists of an Analog-to-Digital Converter and a DSP module, should follow. In this simulation, a spectrum analyzer block replaces these complex blocks.

Figure 6-16. System level verification of the proposed phase noise measurement system in Agilent ADS.

Figure 6-16 shows the simulated system block. In this simulation, an auto-phase quadrature adjustment block is omitted for simplicity. In order to check the response accuracy, a single-tone FM signal with thermal noise is generated in simulation to represent a noisy source. Therefore, the final output spectrum only contains the $1/f^2$ noise region due to the absence of the flicker noise contribution. Conceptually, the device flicker noise contributes the close-in phase noise ($1/f^3$ region) which is at very low frequencies. So, in this system simulation, the close-in
noise can not be shown. Simulations are performed from a 0.5 GHz carrier frequency to a 2 GHz carrier frequency. As expected, the final output signals are almost same because the same random noise is added to a pure sinusoidal source. Spectrum analyzer will show the output noise spectrum. The final phase noise spectrum is described by equation 6-48.

The measured noise power must be scaled by several constant factors as well as by the square of the frequency, because the display is actually the noise frequency. As a numerical example, let $B$ be 100 Hz (20 dBHz) and $k\phi^22\pi\tau_d$ is $10^{-5}$. Let the power measured over the resolution bandwidth of the spectrum analyzer at 100 kHz be 2 nW (-57 dBm). Then, the phase noise at that 100 kHz offset from the carrier is -110 dBc/Hz.

Figure 6-17 describes the response of the proposed system. Figure 6-17 A) and B) shows the noisy source signal and the responses after the system passes through the delay line and phase shifter. In transient simulations, the delay line output shows the 20ns delayed signal and both spectrums shows almost same response. Figure 6-17 C) shows the transient and spectral response of the output signal of the proposed system. In time domain, there is the only noisy signal since the mixer cancels out all the signal components by adjusting the input phase quadrature. In the transient simulation, the noise is scaled up to properly display it. As shown Figure 6-17 C), the spectrum shows the output noise voltage which should be converted into phase noise representation through equation 6-48, called calibration. Figure 6-17 D) shows the phase noise response by equation 6-53 which is same as equation 6-48 except in dB representation. In equation 6-53, $B$ represents noise bandwidth which is decided by spectrum analyzer’s resolution bandwidth.

$$L\left(f_m\right) = S_v\left(f_m\right) - 20\log(K\phi^22\pi\tau_d) - 20\log\left(f_m\right) - 3 - 10\log(B)$$ (6-53)
Figure 6-17. System simulation results of the proposed phase noise measurement system in Agilent ADS: A) input power spectrum B) delay line and phase shifter output C) the system noise output D) the phase noise result.
The final spectrum after calibration process through equation 6-53, shows the expected results in Figure 6-17 D). In this simulation, the added noise power is relatively small which is around -174 dBm, then the final phase noise output shows very low system noise floor. For the calibration, the second term in right-hand side of equation 6-53 can be obtained through the system gain calculation or through the calibration measurement. The calibration is performed by inserting a single tone FM signal at input, then comparing the output signal with the input signal. Figure 6-18 shows the calibration procedure. A known single tone FM signal is inserted in input of the system. Then, the output signal shows the single tone output in spectral domain since the signal is canceled out through the system. Equation 6-54 through 6-58 shows the derivation of the calibration equation in Figure 6-18 B). This calibration procedure will be applied for the proposed system test.

Figure 6-18. Calibration process A) Calibration test set-up B) Calibration equations and calibration results.

\[
2\pi f_c (K_d - K_a)[dB] = P_{rms} + 10 \log(f_m) + 3[dB]
\]

\[
2(f_m)[dBc/Hz] = S_v(f_m) - K_d - 10 \log f_m - 10 \log B - 3dB
\]

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\[ \frac{P_{\text{xxb}}}{P_{\text{carrier}}} = \frac{\beta^2}{4} = \frac{1}{4} \left( \frac{\Delta f_{\text{calpk}}}{f_{\text{mcal}}} \right)^2 = \Delta S_{\text{cal}} \]  

(6-54)

\[ ; \Delta f_{\text{calpk}} = \text{the peak deviation}, f_{\text{mcal}} = \text{the FM rate of the calibration signal} \]

\[ \left( \Delta f_{\text{calrms}} \right)^2 = \frac{1}{2} \left( \Delta f_{\text{calpk}} \right)^2 = 2 f_{\text{mcal}}^{10} \frac{\Delta S_{\text{cal}}[dB]}{10} \]  

(6-55)

\[ K_d^2 = \frac{\Delta V_{\text{rms}}^2}{\Delta f_{\text{calrms}}^2} = \frac{\Delta V_{\text{rms}}^2}{2 f_{\text{mcal}}^{10} \frac{\Delta S_{\text{cal}}[dB]}{10}} \]  

(6-56)

\[ K_d[dB] = P_{\text{cal}}[dB] - (\Delta S_{\text{cal}}[dB] + 20 \log f_{\text{mcal}} + 3[dB]) \]  

(6-57)

\[ \mathcal{L} \left( f_m \right)[dBc / Hz] = S_v \left( f_m \right) - K_d - 20 \log(f_m) - 3 - 10 \log(B) \]  

(6-58)

For this example, the value of \( K_d \) is -77 dB. The system noise is higher than one in Figure 6-17 D) since the FM modulated signal generates higher noise around the carrier signal. The system output affects on this high noise components so that the system noise floor goes higher than the case in Figure 6-17 D). Interestingly, only white (thermal) noise is added to the generated signal source so that there is no close-in noise component which shows \( 1/f^3 \) slope.

6.6. Conclusion

In this chapter, the phase noise definition and theoretical background are introduced and the conventional phase noise measurement methods also are explained and compared. By the comparison of the conventional phase noise measurement systems, the delay line based FM discriminator system is chosen for the embedded phase noise measurement system.

The design considerations are investigated through the system noise and performance analysis. In order to achieve the best sensitivity of the embedded phase noise measurement system, the noise analysis verifies that the mixer should possess high gain and the system
analysis shows that a longer delay line can reduce the system noise floor which determines the phase noise measurement system sensitivity.

The calibration procedure for the proposed system is presented in order to provide the proper test results after the system measurement data acquisition. The calibration procedure can save the effort to derive the system gain. By measuring the known single tone FM signal, the system gain can be easily obtained.

The next chapter handles the actual system implementation based on the analysis in this chapter using IBM8HP technology.
7.1. System Considerations

The newly developed phase noise measurement system described in this chapter is the Frequency Discriminator Phase Noise measurement system. The key issue is that the discrete components in a large circuit breadboard are converted into a small integration compatible on-chip application. A circuit board-based external discriminator phase noise measurement system, typically, uses passive elements in order not to generate any additional noise in the system; This requires a large test bench and a large circuit area. For example, providing 2 ns of delay requires 40 cm of a standard 50 Ω coaxial cable. When it comes to an on-chip system, it is impossible to implement this long transmission line in a small chip area and not have excessive signal losses. With the new circuits shown in this chapter, the passive components may be converted into active circuits. Also, the DUT signal distortion should be minimized throughout the whole on-chip system, especially in the delay line and in the phase shifter as shown in Figure 7-1.

Figure 7-1. The on-chip phase noise measurement system block diagram.
The next sections explain the new design and the reasons why the specific configurations are chosen for the on-chip discriminator noise measurement system. Then, the simulation results characterizing each component are shown.

7.2. System Implementation

7.2.1. Active Balun

A single-ended signal is defined as one that is measured with respect to a fixed potential, generally a ground, while a differential signal is defined as one that is measured between two nodes that have equal and opposite signal excursions around a fixed potential. An active balun converts a single-ended signal to a differential signal with a $180^\circ$ phase difference. This is used in the discriminator in order to supply signals for differential system components including the delay line and the phase shifter. The differential discriminator circuits have several inherent advantages. An important advantage of the differential circuit operation over a single-ended circuit’s operation is a much higher immunity to environmental noise such as capacitive coupling noise due to adjacent signal lines and same line noise from a noisy power supply. Another useful property of differential circuits is the doubling of maximum achievable voltage swings. Simpler biasing and higher linearity are other advantages of differential circuits over their single-ended counterparts.

Differential circuits may occupy twice as much area and consumed twice as much power as their single-ended counterparts, in practice. These are the major drawbacks over single-ended circuits [7.1].

Passive on-chip baluns for RF and microwave frequencies can consume a large area, especially, at lower frequencies. For this reason, baluns are often realized off-chip, which adds to assembly costs and may degrade the conversion gain or loss. The designer can use transmission-line baluns on-chip, but they are not economically feasible except possibly at very high
frequency (> 60GHz) since their size is proportional to wavelength and on-chip thin metal lines have excessive loss when made long. For example, at 60 GHz, a Marchand type balun requires two 500um long directional coupled lines as shown in Chapter 3.

In this application, active baluns are employed because of their wide-band characteristics in a very small chip area.

There are several types of the active balun topologies published [7.2] [7.3] [7.4] [7.5]. The simplest active balun is a NMOS transistor with resistors in the drain and source as shown in Figure 7-2 [7.2].

![Single NMOS balun schematic.](image)

The amplitude of the two outputs can be made equal by adjusting, appropriately, the resistance value of the drain and source. $V_{out1}$ has a unity gain, ideally, since it is a source follower circuit as shown in equation 7-1. In reality, the gain is about 0.6~0.7.

$$\frac{V_{out1}}{V_{in}} = \frac{g_m R_S}{1 + g_m R_S} \approx 1$$

(7-1)

Therefore, a design equation can be easily obtained for the resistors $R_D$ and $R_S$, to a first order approximation, in order to achieve an equivalent $V_{out2}$ amplitude.
\[
\frac{V_{out2}}{V_{in}} = -\frac{g_m R_D}{1 + g_m R_S} \approx \frac{V_{out1}}{V_{in}} \quad (7.2)
\]

The negative sign of equation 7.2 indicates that \(V_{out2}\) space has a 180° phase shift relative to the input, whereas \(V_{out1}\) has the same phase as the input.

This simple structure has a severe limitation during high frequency operation due to the parasitic capacitance associated with the active device. Particularly, the gate-drain parasitic capacitance seriously degrades the high frequency operation in terms of the Miller effect since the effects of this capacitance are effectively multiplied by the gain of the common-source amplifier.

![Cascaded common source-common gate balun schematic.](image)

Other active balun topologies improve the high frequency cut-off by incorporating several techniques to overcome this Miller capacitance limited high frequency operation. For this noise detection application, the common-source common-gate topology is chosen since it has several advantages over other topologies [7.4]. First, it can achieve broadband input impedance
matching easily through adjusting the input active device size. The input impedance at the gate of an active device in a common source topology is typically very high due to its large capacitive component, the input reflection coefficient of a common gate device can be described approximately by \(1/g_m\). Therefore, the proper selection of device size and biasing can yield a 50 Ω input impedance. The input impedance of the common gate device is in parallel with the very high input impedance of the common source device so that the resulting input impedance is approximately that of the common gate device as shown in Figure 7-3. This means that there is no input matching circuit which typically, is implemented using passive devices like transmission lines, inductors or capacitances. The input matching circuits can limit the balun bandwidth due to their Q or frequency selectivity. Second, there is no need to use on-chip inductors which consume a huge area to provide matching or feedback compensation.

Resistor \(R_B\) should be large enough so that it has a very small impact on the input impedance since it is in parallel with \(1/g_m\). The gate of transistor \(M_1\) is biased at \(V_{dd}\) to avoid additional biasing circuitry and the gate \(M_2\) is biased at a voltage level set by the drop across \(R_B\) which is determined by the DC current through \(M_1\). Also, the AC bypass capacitance at both input and output ports should be large enough to enhance the low frequency performance by establishing a proper low frequency cut-off frequency.

The balun was simulated in the Cadence Spectra simulator. The amplitude response is shown in Figure 7-4 and the difference in amplitude is shown in Figure 7-5. Both responses are plotted on log scale on the x-axis. Amplitude responses show a reasonable amplitude difference \(< 0.5 \text{ dB}\) ranging from 200 MHz to 8 GHz. The narrow range from 300 MHz to 3 GHz shows less than 0.2 dB amplitude difference. The proposed system aims to measure the phase noise
generated a over the range 500 MHz to 2 GHz so the balun design is adequate without calibration. The balun power consumption is less than 6 mW with a 1.2 V power supply.

Figure 7-4. Amplitude response of the active balun.

Figure 7-5. Amplitude difference of the active balun, (S21-S31).
Figure 7-6 shows the phase response. In the range from 300MHz to 3GHz, the figure shows less than 4° error in phase difference. In particular, it shows an exact 180° phase difference at 1GHz which is ideal.

Table 7-1 summarizes the simulated performance of the active balun in this work. The active balun converts the single-ended input signal into a differential signal for the subsequent analog delay line and phase shifter which are presented in the next sections.

<table>
<thead>
<tr>
<th>Table 7-1. Baluns Performance Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Frequency Range</strong></td>
</tr>
<tr>
<td>200MHz ~4GHz</td>
</tr>
<tr>
<td>1.7GHz ~5.8GHz</td>
</tr>
<tr>
<td>5.1GHz ~5.9GHz</td>
</tr>
</tbody>
</table>
7.2.2. Active Delay Line

In a commercial phase noise measurement system, a delay line usually is implemented by a coaxial cable or transmission line which does not amplify or significantly distort the signal. If the delay line imposes an excessive gain or loss to the signal, the output will provide a distorted signal compared to the input signal. Also, if the signal is amplified through the delay line, the noise is amplified as well. A transmission line based delay line can be successful for this application. Ideally, a 0dB loss delay line is the best choice with a wide bandwidth. However, a very long line is needed to achieve greater than a 10ns delay time with a transmission line such as a coaxial cable or a coplanar waveguide. Also, this long line attenuates the signal considerably. A lumped element delay cell (i.e. a LC ladder filter) needs several hundred stages to achieve enough delay time. Moreover, the LC ladder filter has a cutoff frequency which is relatively small compared to a transmission line. The lower cutoff frequency achieves a bigger delay per stage for the LC ladder filter but the delay time per stage is still very small for this application [7.7]. In digital applications, delay is realized by reducing the bandwidth of a switching stage. The subsequent switching of an unloaded stage restores the rise time of the digital waveform [7.8]. However, this approach is not useful in analog applications that are sensitive to signal distortion. An active analog delay stage should demonstrate constant bandwidth at a variety of delay values. After considering chip area and achievable delay time, the basic delay line, a differential inverting amplifier with a output level shifter is chosen.

The delay line uses a differential inverting amplifier configuration which introduces a limited operational bandwidth. Also, in order to achieve enough delay for an accurate phase noise measurement, the delay line consists of a 100 differential inverting amplifier stages in series. The following gain and bandwidth analysis depends on the number of cascaded stages, N. The cascade gain stage design analysis will introduce a gain and bandwidth trade-off [7.6].
In Figure 7-7, each stage has an ideal voltage amplifier with gain \(A_0\), an output resistance \(R_{OUT}\), and a load capacitance \(C_{OUT}\). The overall transfer function is given by equation 7-3.

\[
H(s) = \left( \frac{A_0}{1 + \frac{s}{\omega_c}} \right)^N \quad \text{where} \quad \omega_c = \frac{1}{R_{OUT} C_{OUT}}
\]

(7-3)

where \(\omega_c\) is the -3-dB bandwidth of each stage.

For more than 2 stages, the bandwidth of the overall circuit can be described as shown in equation 7-4 [7.6].

\[
\omega_{3-dB} = \omega_c \sqrt{2} - 1 \approx \frac{0.9}{N} \omega_c
\]

(7-4)

The foregone analysis suggests that each stage in a differential inverting amplifier chain must achieve a very wide bandwidth in order not to distort the signal. Therefore, each stage of delay line circuit is designed to achieve around a 10GHz 3 dB operational bandwidth. Also, the gain of each stage is a major consideration. The cascaded gain stages add the gain of each stage on a logarithmic scale. Therefore, if each stage gain is \(A_0\), the total gain of \(N\) stages is \(N \times A_0\). For example, a 1 dB gain amplifier of 100 stages accumulates 100 dB, which is 100000 in magnitude.
Figure 7-8 shows the impact on the signal response of a high gain amplifier which introduces signal distortion such as clipping. With excessive stage gain, the signal will experience signal distortion shown in Figure 7-8 B. When passed through several gain stages, the pure sinusoidal signal changes into a rectangular wave. So the amplifier stage only amplifies the linear region of the rectangular wave (dotted area) as shown in Figure 7-8 C. Phase noise can be interpreted as jitter in the time domain. So jitter in the time domain also experiences distortion compared to the original input signal. In order to keep the same phase noise through the delay line, each stage gain should be about unity in order not to distort the signal and noise. The gain and bandwidth of each basic delay line circuit should be optimized to achieve a reasonable gain and operation bandwidth depending on the number of stages. The delay time should be large enough to produce accurate measurement results.

Figure 7-8. Cascaded gain stage time response with excessive gain.
In this work, a differential inverting amplifier topology was chosen (differential amplifier with load resistor) because this topology can ensure the maximum operational bandwidth without using an inductive peaking technique. This topology can have a large gain which will degrade the delay line response. To minimize the gain of each stage, a source follower is added to each differential amplifier stage. Figure 7-9 shows the proposed delay line cell topology.

![Figure 7-9. Delay line cell schematic.](image)

The source follower provides two key operations. First, the source follower usually shows less than 0dB gain with a relatively wide bandwidth due to the suppressed Miller capacitance. The second, the source follower can shift down the DC operating point. Therefore, each stage input always experiences the same DC bias point. By adjusting the output DC level of the differential inverting amplifier, the stages are easily cascaded. Figure 7-10 shows the basic concept of this topology that adjusts the differential inverting amplifier. The first stage of the differential inverting amplifier increases the DC level and amplifies the signal as shown in Figure 7-10. The source follower reduces the DC bias level and the signal amplitude. Therefore, the output signal preserves the same amplitude and DC bias as the input signal.
Figure 7-10. Transient response of the proposed differential inverting amplifier.

Transient simulation results of the proposed delay line are shown in Figure 7-11. The first stage of the proposed delay line cell increases the DC bias level and the second stage sends it back to the input DC bias level. This topology can minimize unwanted signal distortion and keep the original signal applied to the output through many cascaded stages. The differential amplifier and source followers share a 1.2 V power supply in order to minimize the power consumption.
and prevent overloading the DUT. The simulated DC power consumption is 60mW for 100 stages.

Figure 7-11. Transient simulation results of the proposed differential inverting amplifier.

Figure 7-12. AC response of the proposed differential inverting amplifier.

The AC simulation shows the 3dB bandwidth of the proposed delay line cell. As explained by equation 7-4, the operational bandwidth should be large enough to minimize unwanted signal
distortion at high frequency. The 3dB bandwidth is set around 8GHz. Without using any feedback compensation element, the circuit achieves the widest bandwidth.

The delay time and operational bandwidth have a trade-off. The delay time is inversely proportional to the operational bandwidth. Therefore, a longer delay sacrifices the operation bandwidth which in turn introduces unwanted signal distortion. For the phase noise measurement system, the delay time should be large enough to ensure an accurate measurement result. In this work, the goal is to provide 2.5 ns delay generation to measure up to a 20 MHz offset frequency. Each delay cell of the proposed inverting amplifier can generate 26 ps delay with 8 GHz 3 dB bandwidth. Therefore, the delay line consists of 100 stages in order to achieve a long delay time. The transient simulation result is shown in Figure 7-13. The delay line generates greater than 3.447 ns delay through 100 stages with minimized signal distortion at 1 GHz frequency.

Figure 7-13. Transient response of the proposed delay line.

Figure 7-14 shows the delay variation of the delay line depending on the operational frequency. At smaller bandwidths, the delay time is increased in the same environment. Through
all the simulations over the entire frequency range, the power consumption is almost the same, around 60 mW, for 100 stages. Gain also varies depending on frequency. For an accurate comparison, the gain of delay line is controlled through the source follower and current source of the first stage of the delay line cell. Delay time is calculated by observing the first rising point of the delayed signal.

Figure 7-14. Delay time variation dependence on the operation frequency of operation.

7.2.3. Active Phase Shifter (Based on Variable Delay Cell)

The phase shifter in a commercial phase noise measurement system is usually an external module which consists of variable capacitors and inductors. This discrete module can have a large tuning range and an accurate tuning sensitivity. When it comes to on-chip applications, the choice of a phase shifter design is very limited due to the available passive elements such as varactors, capacitors and inductors. If the design goal of the phase shifter is for a narrow band operation at a specific frequency, the design can be realized with these passive components. However, the phase shifter in the proposed noise measurement system needs to operate over a
wide frequency range. Thus, the phase shifter is designed using a variable delay line due to the variable delay line’s relatively wide operational frequency range and wide tuning range. A phase shifter in the frequency domain provides the same circuit function as a variable delay circuit in time domain.

This embedded phase noise measurement system is designed for measurements from several hundred MHz up to 2 GHz. To achieve this specification, the phase shifter was implemented with the shifter element to be a variable delay cell. In this case, the variable delay cell can control its output to produce a wide range of delay time to adjust the input to the mixer to be 90° out of phase. Also, the phase shifter keeps the output signal at the same amplitude as the input in order not to produce signal distortion. Thus, the final phase shifter is designed using a variable resistance delay cell with a source follower to adjust the output DC level to the next cell input DC level and prevent signal distortion. In addition, the variable delay line usually experiences a severe DC level change at the output to the mixer so additional DC bias adjustment circuitry is added to produce a stable output DC level.

Figure 7-15 shows the basic variable delay stage of the variable delay line. The load element contains a diode-connected PMOS device in shunt with an equally sized externally biased PMOS device that produces symmetric load characteristics [7.9]. Two PMOS device pairs create a symmetric load in order to make the load resistance looking into M3 and M4 linear and dependent on the control voltage ($V_P$). Ideally, by the standard quadratic model of a long channel MOS, the I-V characteristics of the symmetric loads are completely symmetric about the center of the voltage swing. The load swing is defined from the $V_{dd}$ rail supply to the bias voltage for the M4 and M6 PMOS devices. It is important to see that the effective resistance of a symmetric load is directly proportional to the small signal resistance at the ends of the swing range. This
small signal resistance is just one over the transconductance, $g_m$ for one of the two equally sized devices when biased at $V_p$ as shown in equation 7-5.

$$t_{\text{delay}} = R_{\text{eff}} C_{\text{eff}} = \frac{C_{\text{eff}}}{g_m}$$  \hspace{1cm} (7-5)

where $R_{\text{eff}}, C_{\text{eff}}$ are the effective output resistance and capacitance of the first stage of the variable delay cell, respectively [7.10].

Figure 7-15. Basic cell of the proposed phase shifter.

The PMOS bias voltage for the load element must be controlled so that the load current at the point of symmetry equals one half of the differential pair bias current. The PMOS bias voltage can be generated simply by connecting the bias voltage to the output of a dummy load element biased by a differential pair bias current. This connection will establish the PMOS bias voltage as the lower DC voltage swing limit, the point where the load current equals the differential pair bias current. Alternatively, the differential pair bias current can be established for a given PMOS bias voltage using a replica-feedback bias circuit as shown in Figure 7-16.
The MOS realization of symmetric loads has additional advantages beyond their high dynamic supply noise rejection characteristics. Because the higher gain region always occurs at the center of the voltage swing, the delay cells will provide adequate gain for generating signal delay over a broad frequency range. Furthermore, because the load resistance of symmetric loads decreases towards the ends of the voltage swing, the transient swing limits will always be well defined near the DC swing limits, resulting in reduced noise sensitivity. The IC layout for the differential delay cell will be very compact because the load elements only contain two equally sized PMOS devices.

Figure 7-16. Simplified schematic of the self-biased replica-feedback current source bias for the differential variable delay cell stage [7.9].

A simplified schematic of the current source bias circuit illustrates the basic circuit functions. The bias circuit sets the current through the simple NMOS current source in the delay cells in order to provide the correct symmetric load swing limits. In addition, it adjusts the NMOS current source bias dynamically so that this current is held constant and highly independent of supply voltage in order to counteract the effect of the finite output impedance of the simple NMOS current source and achieve high static supply noise rejection.
Figure 7-17. Schematic of the self-biased replica-feedback current source bias for the differential variable delay cell stage [7.9].

The current source bias circuit is based using a replica of half the buffer stage and a single-stage differential amplifier. The amplifier adjusts the current output of the NMOS current source so that the voltage at the output of the replicated load element is equal to a control voltage, a condition required for correct symmetric load swing limits. The net result is that the output current of the NMOS current source is established by the load element and is independent of the supply voltage. As the supply voltage changes, the drain voltage of the NMOS current source devices varies. However, the gate bias is adjusted by the amplifier to keep the output current constant, counteracting the effects of the current source finite output impedance.

As shown in Figure 7-17, in order for the amplifier not to limit the delay cell supply voltage operating range, it must have low supply voltage requirements. For this reason, an amplifier based on a self-biased PMOS source coupled pair is used. In order for the PMOS current source device in the amplifier to remain in saturation, the current densities of the PMOS source coupled pair devices and the PMOS current source device must be one quarter of that in the PMOS symmetric load devices. The amplifier bias is generated from the same NMOS current
source bias through a stage mirroring the half-delay cell replica so that amplifier supply voltage requirements are similar to those of the buffers and the amplifier bias current is highly independent of supply voltage. This replica bias stage is necessary because otherwise the input offset of the amplifier will vary with supply voltage, causing the output current of the NMOS current source to also change with supply voltage. Because the amplifier is self biased with a potential of multiple operating points, the bias circuit is made stable with the amplifier unbiased and an NMOS current source bias at the negative supply. As a result, an initialization circuit is needed to bias the amplifier at power-up to the exact operating point. This initialization circuit prevents the NMOS current source bias from completely turning off the bias current sources to a stable zero current operating point [7.9].

As shown in Figure 7-17, a compensation for stable operation is required because this current source bias circuit contains a feedback loop with two gain stages and with two significant poles. The pole at the amplifier output will dominate with a much higher output impedance than the pole at the half-delay cell replica output. Therefore, to increase the phase margin of the bias circuit, the design simply limits the capacitive output load of the simple NMOS current source gates in the delay cell stages. The output load should be limited to about ten delay cell stages containing devices of the same size as the corresponding devices in the bias circuit in order to prevent the output recovery time of the bias circuit from limiting the dynamic supply noise rejection of the delay cells. With no required reference voltage, the only external bias is the control voltage ($V_p$). Although no device cascading is used, the resultant static supply noise rejection is equivalent to that achievable by a delay cell stage and a bias circuit with cascading, without requiring an extra supply voltage. The total supply voltage requirement of the buffer
state and bias circuit is slightly less than a series NMOS and PMOS diode voltage drop with identical current densities.

Figure 7-18. Transient simulation results for the proposed 6-stage variable delay cell depending on the PMOS load bias.

Figure 7-18 shows a transient simulation results for the proposed variable delay cell. The source follower produces an output DC level that feeds into the input DC level, which is similar to the delay line architecture except for its symmetric load. In this way, the output level of the proposed variable delay cell can prevent the signal from producing unwanted distortion. By cascading six stages of the proposed variable delay cell, the maximum variable delay is adjusted to 500 ps at 1 GHz. In the frequency domain, the delay module can adjust the phase quadrature up to 500 MHz. All the circuits use a 1.2 V power supply in order to minimize power consumption. The simulated DC power consumption is 12mW.
7.2.4. Double Balanced Mixer (Phase Detector)

7.2.4.1. Passive Ring Mixer (Input Structure)

Most systems which require phase information use mixers somewhere in the measurement for comparison of phase information. Theoretically, any mixer with a dc coupled port could be used as a phase detector. Practically, however, mixers often display some very non-ideal characteristics (e.g., DC offset) when used as phase detectors. The actual mixer chosen for a particular application will often depend on the degree to which these non-ideal characteristics can be tolerated. In this work, a double balanced passive mixer is chosen with an active RC filter following it because the system has high linearity, no flicker noise generation and low power consumption. Normally NMOS transistors have better switch performance than do PMOS transistors because of the higher mobility of electrons than holes. Therefore, NMOS transistors are chosen for the passive mixer elements.

![Figure 7-19. Simplified schematic of the passive ring mixer (bias not shown).](image)

The basic phase detection concept is the application of two identical frequencies, constant amplitude signals to a mixer which results in a dc output which is proportional to the phase difference between the two signals. While it is true that even a single diode can be used as a
mixer, most phase detectors involve the use of double balanced mixers. With this in mind, the theory presented in this chapter focuses on double balanced mixer design.

Figure 7-19 is a schematic of a typical double balanced, four-MOSFET mixer. The main difference between the Gilbert quad mixer and a folded ring mixer is the biasing levels. The Gilbert quad mixers are biased nominally into saturation and have DC current while the passive ring mixers are biased near the FET threshold and have no DC current.

Gilbert mixers which convert an incoming RF voltage into a current through a transconductor, whose linearity and noise figure set a firm bound on the overall mixer linearity and noise figure. This circuit uses voltage-controlled current sources in V-I converter circuit for a voltage-controlled resistance. The resistance of a triode-region MOSFET varies in a manner inversely proportional to the incoming RF signal. If the voltage between the mixer transistor drain and the source is maintained at a fixed value, the current flowing through the device will be a faithful replica of the RF voltage, and if the drain-source voltage varies with the local oscillator, LO then the current will be proportional to the product of the LO and RF signals [7.11].

Table 7-2 summarizes the simulation results of the passive ring mixer.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>This Work</th>
<th>Reference Work [7.12]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.13 um</td>
<td>0.13 um</td>
</tr>
<tr>
<td>Conversion Gain (Gc)</td>
<td>-4.8 dB</td>
<td>-5.5 dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>4.9 dB</td>
<td>6.5 dB</td>
</tr>
<tr>
<td>P1dB (dBm)</td>
<td>-1.5 dBm</td>
<td>N/A</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>7.65 dBm</td>
<td>10 dBm</td>
</tr>
<tr>
<td>LO Power (dBm)</td>
<td>5 dBm</td>
<td>5 dBm</td>
</tr>
</tbody>
</table>
The use of a double balanced structure cancels out the common-mode dc biasing signals and the nonlinear dependence of $g_{ds}$ on $V_{ds}$. The final down-conversion mixer circuit is shown in Figure 7-20.

There are two very important capacitors attached to the virtual ground nodes of this topology. The output stage (the opamp and the feedback resistors), which convert the output current of the mixing transistors back into a voltage, should only be able to produce a low-frequency output signal. However, in order to let the input operate for all frequencies, the virtual ground nodes of the mixer must have no high frequency signals. This is usually done with the feedback structure connected to the opamp which creates the virtual ground at its inputs. The transistors in the input would operate as pass-transistors for high-frequency signals when the frequency capability of the opamp would not be high enough. Therefore, the capacitors $C_f$ have been added. The $C_f$ capacitors make sure that all the high frequency currents injected to the virtual ground nodes are filtered out and not converted into voltages. The opamp still generates a
virtual ground for low frequency signals. The design procedure can split the design of the input
and the opamp by using the structure shown in Figure 7-20.

The input structure (passive ring mixer) can be optimized for high frequency operation
(more than 1 GHz) while the opamp can be designed for low-frequency operation (up to several
hundreds of MHz).

The dc biasing levels of the RF and LO signal must be chosen carefully. There will be
severe distortion when the pass-transistors are not kept in the triode region at all times. The
smallest possible level that can appear at the gates must be at least a $V_T$ higher than the largest
possible source level. Otherwise the transistors will be turned off during the mixing period.
Saturation of the pass-transistors will appear when the largest drain-source voltage $V_{ds}$ becomes
higher than the smallest $V_{gs} - V_T$. However, saturation does not directly result in distortion. The
cross-coupled double balanced structure makes sure that all quadratic components in the voltage-
to-current conversion characteristic of the pass-transistors are cancelled out [7.13].

7.2.4.2. Active RC Filter (Output Structure)

In order to build a reliable double balanced mixer with an active RC filter for down-
conversion, the active RC filter should have several characteristics. First, it should provide low
power consumption. Second, it should have high linearity. Third, it should have a wide
operational bandwidth. The proposed system is targeted to measure phase noise which usually is
measured at several offset frequencies (e.g. 600 kHz, 1 MHz, 3 MHz and 10 MHz) depending on
the test device technology standard. Therefore, the active RC filter should possess at least a 50
MHz 3 dB bandwidth.

The main design challenge lies in designing for a low voltage supply. Generally, integrated
continuous-time high frequency baseband filters employ either $gm$-C or MOSFET-C topologies
with an automatic tuning methods [7.14] [7.15]. However, the trend towards low supply voltage
introduces new challenges in the realization of these techniques. For \( gm \)-C filter types, it is difficult to achieve a broad dynamic range and good linearity performance with low power consumption, whereas CMOS implementations suffer from reduced programmability [7.16]. The MOSFET-C approach may be better than \( gm \)-C in terms of power dissipation and noise performance, but linearity and tuning range may be poor for low supply voltages. The operational amplifiers of the filter operate on a 1.2 V supply and demonstrate a very good compromise between high-frequency performance and current consumption, due to the compensation technique reported in [7.17]. In particular, a 20 times boost is achieved in terms of the dominant pole of the amplifier relative to traditional compensation practices without causing any stability problems in the presence of an output load. The system consists of a differential input stage, an output stage, and a common mode feedback (CMFB) circuit as shown in Figure 7-21.

![Figure 7-21. Operational amplifier schematic (bias not shown).](image)

In order to expand the amplifier’s bandwidth without a loss of a gain, a new compensation technique is adopted, based on [7.15]. The idea is to place two cross-coupled capacitors between the input differential pair and the output buffer. These capacitors act as a negative capacitance,
$C_\mu$ of the input transistors, thus generating an anti-pole-splitting behavior that augments the amplifier’s gain-bandwidth product. The proposed compensation technique uses the anti-pole-splitting method, but in a different way than the technique in [7.16]. The compensation capacitors ($C_F$) are cross connected to the outputs of the first and second stages of the amplifier, which is combined with the classic Miller RC compensation. It provides not only an anti-pole-splitting behavior, but also a phase-controlling action, that holds the output phase away from -180° for frequencies spanning far beyond the unity gain frequency, thus providing extra bandwidth and adequate phase margin [7.17].

![AC modeling of Operational amplifier](image)

Figure 7-22. AC modeling of Operational amplifier.

The simplified AC equivalent model of the amplifier with an output capacitance $C_{load}$ is shown in Figure 7-22. The differential open-loop voltage gain is described in equation (7.6). For the sake of simplicity, a third order term in the denominator is omitted since its contribution is marginal at the frequency range of interest compared to the lower order terms. The impedance of the current source transistor will be very large. By symmetry, $M_1$ and $M_2$, $M_3$ and $M_4$, $M_6$ and $M_9$, $M_7$ and $M_{10}$, $M_8$ and $M_{11}$ are equal.
$$A(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(-g_{m1} + sC_{gd1})\left(R_F C_F \left(C_{gd6} - C_F\right)s^2 + \left(C_F + C_{gd6} - C_{F1} - g_{m6} R_F C_F\right)s - g_{m6}\right)}{D s^3 + \left(C_F C_{F1} \left(4 - g_{m6} R_F\right) + E\right)s^2 + \left(g_{m6} \left(C_F - C_{F1}\right) + F\right)s + \left(g_{d1} + g_{d3}\right)\left(g_{ds6} + g_{ds7}\right)}$$

$$(7.6)$$

$$\approx \frac{(-g_{m1} + sC_{gd1})\left(R_F C_F \left(C_{gd6} - C_F\right)s^2 + \left(C_F + C_{gd6} - C_{F1} - g_{m6} R_F C_F\right)s - g_{m6}\right)}{\left(C_F C_{F1} \left(4 - g_{m6} R_F\right) + E\right)s^2 + \left(g_{m6} \left(C_F - C_{F1}\right) + F\right)s + \left(g_{d1} + g_{d3}\right)\left(g_{ds6} + g_{ds7}\right)}$$

where

$$D = R_F C_F \left((C_{gd1} + C_{gd3} + C_{gd6} + C_{gs6} + C_{F1})(C_{gd6} + C_{gd7} + C_{F1} + C_{\text{load}}) - \left(C_{gd6} - C_{F1}\right)^2\right)$$

$$(7.7)$$

$$E = \left(C_{gd1} + C_{gd3} + C_{gd6} + C_{gs6} + C_{F1}\right)(C_{gd6} + C_{gd7} + C_{\text{load}} + C_{F1}) - \left(C_{gd6} - C_{F1}\right)^2$$

$$+ R_F C_F \left(\left(g_{d6} + g_{d7}\right)\left(C_{gd1} + C_{gd3} + C_{gd6} + C_{gs6} + C_{F1}\right)\right)$$

$$+ \left(g_{d1} + g_{d3}\right)\left(C_{gd6} + C_{gd7} + C_{\text{load}} + C_{F1}\right) + g_{m6} C_{gd6}$$

$$+ C_F \left(C_{gd1} + C_{gd3} + C_{gd7} + C_{gs6} + C_{\text{load}}\right)$$

$$(7.8)$$

$$F = \left(g_{ds6} + g_{ds7}\right)\left(C_{gd1} + C_{gd3} + C_{gd6} + C_{gs6} + C_{F1}\right)$$

$$+ \left(g_{d1} + g_{d3}\right)\left(C_{gd6} + C_{gd7} + C_{\text{load}} + C_{F1}\right) + g_{m6} C_{gd6}$$

$$+ R_F C_F \left(g_{ds1} + g_{ds3}\right)\left(g_{ds6} + g_{ds7}\right) + C_F \left(g_{ds1} + g_{ds3} + g_{ds6} + g_{ds7}\right)$$

$$(7.9)$$

The term $E$ and $F$ depends on parasitic capacitances and output load capacitances. If the output load capacitance is small enough, the term $E$ and $F$ can be ignored. The feedback capacitors $C_F$ and $C_{F1}$ should be substantially greater than the circuit’s parasitic capacitance. The open loop gain indicates that the poles are on the left-half plane as long as the coefficients of the first-order and second-order terms of the denominator are positive. Consequently, two relations must be valid for the circuit stability.

$$R_F < \frac{4}{g_{m6}}$$

$$(7.10)$$

$$C_{F1} < C_F$$

$$(7.11)$$
These relationships are derived under the assumption that the terms $E$ and $F$ are negligible.

In order to verify the zero circuit effects, in the numerator of equation 7-6, it is assumed that $C_{gd3}$ is negligible. Equation 7-6 can be approximated by equation 7-12.

$$\begin{align*}
A(s) &= -\frac{\left(-g_{m1} + sC_{gd1}\right)(R_F C_F^2 s^2 + g_{m6} R_F C_P s + g_{m6})}{(C_F^2 (4 - g_{m6} R_F) + B) s^2 + C s + (g_{ds1} + g_{ds3})(g_{ds6} + g_{ds7})}
\end{align*}$$

(7-12)

As shown in equation 7-12, the transfer response contains 3 zeros. One is located in the right-half plane at extremely high frequencies. The other two lie on the left-half plane and can be described as below.

$$z_{1,2} = -\frac{g_{m6}}{2C_F} \pm \frac{\sqrt{g_{m6} R_F - 4}}{2C_F \sqrt{g_{m6}}}$$

(7-13)

It is obvious that these two zeros are on the real frequency axis if $R_F > 4/g_{m6}$. Now, when it comes to the third order coefficient, $D$, the third pole moves to a lower frequency as $R_F$ increases. Larger values for $R_F$ generate wider bandwidth as the two more significant poles shift to higher frequencies as shown in equation 7-13. By selecting $R_F = 4/g_{m6}$, the circuit creates a double zero at frequency $-g_{m6}/2C_F$. In practice, there might still be a small imaginary part, but it has a negligible effect. Also, this analysis disregards parasitic capacitance and real circuits have these two zeros and the third pole appear at rather lower frequencies than our analysis suggests. One important fact is that the dependence of the zeros on $C_F$ is much stronger than that of the two dominant poles. This gives more flexibility to the positioning of the zeros in a frequency compensation procedure when they can be moved without significantly altering the location of the two poles. Practically, the value of $R_F$ can be a little greater than $4/g_{m6}$ without the sacrifice of stability in simulation.
Figure 7-23. Amplifier A) gain and B) phase accomplished with the proposed compensation and the conventional RC compensation network.

This double zero feature is very important. It adds positively to the phase response, thus moving the -180° intersect to a much higher frequency. Figure 7-22 shows the difference between the pole-splitting compensation method and the proposed compensation method. The amplifier core is identical in both cases except for the circuit feedback elements. The proposed topology offers a 20 times increase in the frequency of the amplifier’s dominant pole with respect to the classic RC approach for the same current dissipation. The unity gain frequency is less important for the filter application. Phase response is non-monotonic, showing a minimum of -150° below the unity gain frequency, but this is not the relevant phase to consider for stability.
The compensation technique drastically improved the amplifier’s frequency behavior for the benefit of the filter performance. The filter’s linearity is improved and so is the frequency response. Simulations revealed that using the amplifier with this compensation technique in the filter, provides significant improvement in both in-band and out-of-band IIP3 performance compared to conventional approaches. More specifically, the performance gain increases as the two input tones move higher in frequency. Another interesting advantage of this work’s compensation technique over conventional pole-splitting methods is that it mitigated the filter’s passband ripple.

The CMFB circuitry is described in Figure 7-21. Voltage, $V_{CM}$ is in the region of half the supply voltage (typically, 600 mV). The same current flows through M12 and M13 only if their $V_G$ is equal. Given the fact that $V_{CM}$ remains constant, then, the half sum of the voltage at the two output stages must equalize $V_{CM}$ for a current equilibrium in M12 and M13. Hence, the loop that closes through M12, M13, M14, M15 and M16 maintains the dc output voltage equal to $V_{CM}$. This loop must have small gain to be wideband and stable. Capacitors $C_1$ and $C_2$ improve the loop phase margin so that common mode oscillations cannot be sustained. $C_1$ also enhances the bandwidth of the CMFB loop in order to have sufficient CMRR at high frequencies.

Table 7-3 summarizes the simulated performance of operational amplifier.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>45 dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>45°</td>
</tr>
<tr>
<td>Gain Bandwidth</td>
<td>600 MHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>3.1 mW</td>
</tr>
</tbody>
</table>
7.2.4.3. Double Balanced Mixer Result

A mixer’s frequency converting action is characterized by conversion gain or loss. The voltage conversion gain is the ratio of the RMS voltages of the IF and RF signals. The power conversion gain is the ratio of the power delivered to the load and the available RF input power. When the mixer’s input impedance and load impedance are both equal to the source impedance, the power and voltage conversion gains, in decibels, are the same. Note, that when the circuit load is a mixer with a high impedance filter, this condition is not satisfied.

The mixer’s conversion gain and output distortion level was simulated and the result is plotted in Figure 7-24. For the main 1 MHz IF signal, the mixer achieves a conversion gain of 10.3 dB. Also, for a 10 MHz IF signal, the mixer produces 8.3 dB of conversion gain. The conversion gain is calculated based on equation 7-14.

Figure 7-24. Double Balanced Mixer output spectrum

As a phase detector, the mixer produces different DC voltages proportional to the difference from the input phase quadrature. Figure 7-25 shows the mixer performance as a phase
detector. As the phase difference increases, the output DC level increases. The response of the phase detector shows a conventional multiplier response. For a small phase difference, the output dc changes rapidly while the output dc changes slowly for a large phase difference (>36°). The simulation is performed for 500MHz, 1 GHz, and 2GHz. Depending on the operational frequency, the responses shows slight difference.

\[
\text{Conversion Gain} = 20 \cdot \log \left( \frac{\text{output voltage}}{\text{input voltage}} \right)
\]

(7-14)

Figure 7-25. Double Balanced Mixer Output as a phase detector.

The double-balanced mixer followed by active RC filter plays a key role in the entire system. Thus, the test circuitry for this part is implemented and measured in a separate test structure IC. The die-photo is shown in Figure 7-26. The test circuit aims to test the mixer function as a phase detector so that the outputs of mixer are combined through a differential to single-ended buffer.
Figure 7-26. Die photo of the Double Balanced Mixer with active RC filter and buffer.

Figure 7-27 describes the test setup for the phase detector functionality. A signal generator is used for sinusoidal signal generation. A balun converts the single-ended signal to differential signal and power splitter divides the signal into two same phase signals. A variable phase shifter changes the phase difference and measurements are performed depending on input phase difference. An Agilent infiniium 54832D is used for displaying the output. The generated signals range from 500MHz to 2GHz for the measurement. Measured data shows similar results in simulation for the entire range of measured frequencies. Figure 7-28 shows the measured and simulated results after passing a buffer with 7dBm LO power and -7dBm RF power. Measured results show very good agreement with the simulated results for two different frequencies. Both simulation and measurement shows the output independent to input power variations.
Conversion gain is measured for different RF input frequencies in order to check the gain stability depending on the input frequency variation as shown in Figure 7-29. A buffer reduces the conversion gain to around 10 dB for the entire frequency range. In order to calibrate the proposed system, the mixer gain should be known as shown in equation 6-48. Conversion gain is
measured for 1MHz IF output since the proposed system calibration is performed for a 1 MHz offset frequency. The conversion gain ranging from 750MHz to 2GHz shows less than 1dB difference.

Figure 7-29. Measured conversion gain for different input frequencies.

Figure 7-30. Measured conversion gain for different LO power.
Figure 7-30 presents the conversion gain as a function of LO power variation for 1 MHz IF output while input RF power is -7 dBm.

7.2.5. Phase Shifter Auto-adjustment

In the system, the mixer acts as an ideal phase detector by forcing the input signals to be in quadrature. Considering the mixer in a standalone operation, any deviation error from quadrature results in an output amplitude error, which is very small when the deviation around quadrature is small. For example, a 1° offset from quadrature results in an amplitude error of -0.001 dB.

However, the situation for the delay-line discriminator is much worse than the standalone mixer case due to the presence of the delay line before the mixer. This problem is inherent in delay-line discriminators. A high phase shift can result when the delay time is much larger than the DUT signal period. In this case, the deviation from a quadrature condition is amplified by the delay, which results in significantly larger dc offset and amplitude detection errors.

![Auto-phase adjustment unit](image)

Figure 7-31. Auto-phase adjustment unit
The proposed calibration circuit shown in Figure 7-31 uses a comparator to measure the dc signal at the mixer output against a zero dc state. A charge pump and reset switch monitors the comparator output and then decides on the proper voltage step to drive the control voltage of the VCDL. This is achieved by the circuitry shown in Figure 7-31.

The auto adjustment unit consists of three main components, which are DC comparator, Charge pump and Reset switch. By comparing the mixer output with a zero DC state, the charge pump achieves the proper dc level. A reset switch works for the case of excessive dc levels. If charge pump accumulates a dc level more or less than the available control voltage (0.45~0.7V), the reset switch turns on and resets dc level in order to avoid system malfunction. The actual implementation is fairly simple because this circuit only controls the dc voltage without any proper bandwidth depending on offset frequency.

7.3. Conclusion

This chapter explains each building block implementation of the embedded phase noise measurement system. All the system components are implemented in standard CMOS technology in order to minimize the test system overload on the DUT system.

In order to minimize unwanted distortion and noise generation in a test signal, the embedded system uses a differential circuitry by converting a single-ended signal into a differential signal through an active balun. The test signal is delayed through the analog delay line which minimizes the unwanted test signal distortion by introducing a level-shifting method to achieve 0 dB gain. The variable phase shifter also adapts the same method to minimize unwanted test signal distortion. The double-balanced mixer suppresses the signal components of the test signal and leaves the noise components which contain the phase noise components. By monitoring the system output level, an auto-adjustment unit cancels out the signal component automatically.
CHAPTER 8
EMBEDDED PHASE NOISE MEASUREMENT SYSTEM RESULTS

8.1. Measurement Setup

A phase noise measurement circuit is fabricated in a 0.13 μm, seven metal CMOS process (IBM8HP) and occupies an active area of 1 mm × 1.5 mm. The die photo for the fabricated system is shown in Figure 8-1. The power supply is 1.2 V for all the components of the fabricated system. DUT’s input is imposed at IN on left center pad and the output is extracted from OUT+ or OUT-. In this work, one of the outputs is utilized for the phase noise evaluation. The other pads on the upper and the lower side are for the DC biasing of individual building blocks.

Active baluns are self-biased by using a biasing resistor at the input port. The active delay line needs three DC biases. One is for the input DC level, VDCIN (≅ 0.4V). Another is for the current source biasing, VCDLY (0.5~1.2V) of the active delay line to control the active delay line gain. Depending on the carrier frequency, the active delay line gain will vary. Thus, the current source biasing controls the active delay line gain. The last one is for the current source biasing, VBDLY (0.35~0.6 V) of a source follower (DC level shifter). By controlling the source follower current, the fine tuning of an active delay line gain is be possible.

The phase shifter also needs biasing. VPVCDL (0.45~0.75V) controls the symmetric load impedance. In this work, it is not necessary to control VPVCDL since an auto-adjustment unit provides DC bias for the symmetric loading of the phase shifter. The magnitude of VCVCDL (≅ 0.5V) is similar to VBDLY in the active delay line.

The passive mixer also needs a DC bias for its input signal. The passive mixer is designed to work in the triode region. So the input signal DC levels are set to operate the passive mixer in the triode region. VLODC (≅ 1V) is for DC biasing the internal gate inputs. The active RC filter
needs three DC biases. The first is for the OPAMP input bias, VAMP (≅ 0.6V) since the OPAMP input DC range can not cover the entire DC bias range. The second is for the OPAMP CMFB reference, VCM (≅ 0.55V). The CMFB of OPAMP needs a reference bias to compare it with the average of OPAMP output bias. Then, CMFB adjusts OPAMP output DC bias to operate correctly. VCAMP (≅ 0.5V) is for the output buffer bias.

Figure 8-1. Layout of the proposed system (1 mm×1.5 mm)

The general test setup used to characterize the embedded phase noise measurement system is illustrated in Figure 8-2. The most accurate method to evaluate the linearity and sensitivity of the phase noise measurement system is the measurement of the response of a known carrier modulated with a single-tone FM signal as explained in Chapter 6.
8.2. System Linearity and Calibration Constants Measurements

An Agilent E8254A signal generator is used to provide a 1 GHz FM-modulated signal at the DUT port for calibrating the system. To produce a single-tone FM signal while suppressing the power in the higher order sidebands, the modulation index ($\beta$) of the DUT signal is set to less than 0.2 rad by adjusting the FM deviation and the FM rate of the Agilent signal generator. The first step in characterizing the phase noise measurement system is to validate the linear gain relation between the output voltage fluctuations and the DUT frequency deviation ($f_m$) [8.1].

In order to avoid a possible confusion between the terms, the single-tone FM signal is described and the terms which are used in system linearity and sensitivity measurement are described in terms of physical definitions.

The sinusoidal modulating signal can be described by equation 8-1.

$$m(t) = A_m \cdot \cos(2\pi f_m t)$$  \hspace{1cm} (8-1)
The instantaneous frequency of the resulting FM signal equals

\[ f_i(t) = f_c + k_f A_m \cdot \cos(2\pi f_m t) = f_c + \Delta f \cdot \cos(2\pi f_m t) \]  
(8-2)

The quantity \( \Delta f \) is called the frequency deviation, representing the maximum departure of the instantaneous frequency of the FM signal from the carrier frequency \( f_c \). A fundamental characteristic of an FM signal is that the frequency deviation, \( \Delta f \), is proportional to the amplitude of the modulating signal and is independent of the modulation frequency (FM rate). The phase of the FM signal is obtained as

\[ \theta(t) = 2\pi \int_0^t f_i(\tau)d\tau = 2\pi f_c t + \frac{\Delta f}{f_m} \cdot \sin(2\pi f_m t) \]  
(8-3)

The ratio of the frequency deviation, \( \Delta f \), to the modulation frequency, \( f_m \), is commonly called the modulation index of the FM signal and is shown in equation 8-4.

\[ \beta = \frac{\Delta f}{f_m} \]  
(8-4)

Figure 8-3 shows the relationship between the FM deviation and the FM rate. The FM deviation is proportional to the signal amplitude and the FM rate defines an offset frequency. The calibration constant is a different name for the system gain as explained in Figure 8-3. Figure 8-3 assumes that the measurement resolution bandwidth is 1 Hz for the simplicity of the equation.

The input signal power is determined by the FM deviation for the case of a small modulation index (\( \beta < 0.2 \)). Thus, a linearity test is performed by checking the output power’s dependance on the input signal variation which is proportional to the FM deviation. The FM deviation represents the amplitude of the voltage of the input signal at a 50Ω system.
The input signal power can be easily determined by equation 8-5 as shown in Figure 8-3.

\[
\text{Input Power } \propto (\Delta f)^2 = (\beta \cdot f_m)^2 \tag{8-5}
\]

\[
\text{Input Power } [dB] \propto \Delta f [dB] = 20 \log (\beta) + 20 \log (f_m) \tag{8-6}
\]

For example, Figure 8-4 shows the linearity test and the calibration procedure for a 1GHz 0dBm carrier signal. Figure 8-4 A shows the input signal with 200kHz FM deviation and 1MHz FM rate. The modulation index is displayed in terms of signal power so the actual input signal power needs to be converted to a more familiar form. In Figure 8-4, the modulation index is 0.2 with 200kHz frequency deviation. In case of a 100kHz of FM rate, 0.2 of the modulation index requires a 20kHz FM deviation. The input signal power seems to be same for both cases. However, the actual input power is determined by the FM deviation as shown in equation 8-6. The actual input power for 20kHz FM deviation is -20 dB less than the one for 200kHz FM deviation. As FM deviation gets smaller at a fixed FM rate, the input power level decreases at a
rate of -20dB/Decade [8.2]. The output signal power can be detected at the same FM rate (offset frequency). The input signal power can be estimated from equation 8-7 to equation 8-10.

\[
(\Delta f_{\text{rms}})^2 = \left(\frac{\Delta f_{\text{rms}}}{\sqrt{2}f_m}\right)^2 \cdot \left(\frac{\sqrt{2}f_m}{2}\right)^2
\]

\[
\frac{P_{\text{ssb}}}{P_{\text{carrier}}} = \left(\frac{\beta}{2}\right)^2 = \left(\frac{\Delta f_{\text{pk}}}{2f_m}\right)^2 = \left(\frac{\Delta f_{\text{rms}}}{\sqrt{2}f_m}\right)^2
\]

\[
\Delta S_{\text{cal}} = P_{\text{ssb}} - P_{\text{carrier}} = 20\log\left(\frac{\beta}{2}\right) = 20\log\left(\frac{\Delta f_{\text{rms}}}{\sqrt{2}f_m}\right)
\]

\[
(\Delta f_{\text{rms}})[dB] = 20\log\left(\frac{\Delta f_{\text{rms}}}{\sqrt{2}f_m}\right) + 20\log\left(\frac{\Delta f_{\text{rms}}}{\sqrt{2}f_m}\right) = \Delta S_{\text{cal}} + 20\log\left(f_m\right) + 3
\]

Thus, the input power for a 200kHz FM deviation at 1MHz offset is 103 dB while the input power for a 20kHz FM deviation at 1MHz is 83 dB. The rough calculation of the system gain is -131 dBm (-28dBm – 103dB) for the case of Figure 8-4.

Figure 8-4. Example of the linearity test for, A) An input test signal (FM dev=200 kHz, FM rate =1 MHz) B) The resultant output signal at 1 MHz.

The linearity test is performed by varying the modulation index. The input power level has a linear relationship to the modulation index as explained in equation 8-5. As shown in Figure 8-
3, both the modulation index and the $f_m$ rate for the input signal are varied with the completion of an auto adjustment process and the discriminator output is displayed with an Agilent E4448A spectrum analyzer. In order to measure the low-level output signal, the spectrum analyzer’s sensitivity is enhanced by the three methods. The first enhancement is by narrowing down the resolution bandwidth (RBW) of the spectrum analyzer up to 1Hz. The second is by turning off or minimizing the input attenuator of the spectrum analyzer. The input attenuator serves to increase the spectrum analyzer’s dynamic range by attenuating the high power input carrier. The last enhancement is through turning on the analyser’s internal preamplifier to increase the weak signal output signal of interest. These techniques effectively lower the displayed average noise level up to around -165 dBm. Thus, the low-level signal is detected.

Figure 8-5 shows the output power as a function of the FM deviation while the modulation index is less than 0.2 rad. Here, the FM deviation on the X-axis represents the input power dependance on the FM deviation. Thus, the x-axis presents the input power with a 20dB/Decade increase. The displayed output shows good linearity up to a 1 MHz offset frequency since the output power shows 20 dB/Decade increase while the input power level increases 20dB/Decade as the FM deviation is proportional to input power level as shown in equation 8-6. The limitation of this measurement mainly comes from the signal generator which can only generate a 1 MHz FM rate ($f_m$).
Figure 8-5. Linearity measurement as a function of FM deviation while the modulation index is less than 0.2 radian.

For a phase noise measurement, the calibration constant should be evaluated for an accurate measurement. As shown in Figure 8-4, the calibration constant derivation procedure is similar to a linearity test. The calibration constant is calculated through equation 8-3 as explained in Figure 8-3. The calibration constants ($K_d$) will be the same as long as the system shows linearity.

$$K_d [dB] = P_{cal} [dB] - (\Delta S_{cal} [dB] + 20 \log f_{mcal} + 3 [dB])$$  \hspace{1cm} (8-11)

Table 8.1 shows the calibration constant extracted from the linearity test. Here $P_{cal}$, $\Delta S_{cal}$ and $f_{mcal}$ represent the output power, the power difference between the carrier and sideband of the input signal, and the measured offset frequency (measured FM rate), respectively. With a fixed
FM rate, the FM deviation is changed to control the input signal level. As the input signal level gets smaller, the output power gets smaller at the same rate. Equations 8-12 and 8-13 show examples of this calculation.

\[
K_d [dBm] = P_{cal} [dBm] - (\Delta S_{cal} [dB] + 20 \log f_{mcal} + 3[dB]) \\
= -28[dBm] - (-20[dB] + 20 \log 10^6 + 3[dB]) \\
= -13 [dBm]; f_{mcal} = 1 MHz, \Delta f = 200 kHz
\] (8-12)

\[
K_d [dBm] = P_{cal} [dBm] - (\Delta S_{cal} [dB] + 20 \log f_{mcal} + 3[dB]) \\
= -40[dBm] - (-32[dB] + 20 \log 10^6 + 3[dB]) \\
= -13 [dBm]; f_{mcal} = 1 MHz, \Delta f = 50 kHz
\] (8-13)

Table 8-1. Calibration Constant Evaluation.

<table>
<thead>
<tr>
<th>$f_m$ rate</th>
<th>$\beta$</th>
<th>$\Delta S_{cal}$ [dB]</th>
<th>$P_{cal}$ [dBm]</th>
<th>$K_d$ [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_m$ rate = 1MHz</td>
<td>0.2</td>
<td>-20 dB</td>
<td>-28 dBm</td>
<td>-131</td>
</tr>
<tr>
<td></td>
<td>0.1</td>
<td>-26 dB</td>
<td>-34 dBm</td>
<td>-131</td>
</tr>
<tr>
<td></td>
<td>0.05</td>
<td>-32 dB</td>
<td>-40 dBm</td>
<td>-131</td>
</tr>
<tr>
<td></td>
<td>0.01</td>
<td>-46 dB</td>
<td>-54 dBm</td>
<td>-131</td>
</tr>
<tr>
<td></td>
<td>0.005</td>
<td>-52 dB</td>
<td>-60 dBm</td>
<td>-131</td>
</tr>
<tr>
<td>$f_m$ rate = 0.1MHz</td>
<td>0.2</td>
<td>-20 dB</td>
<td>-48 dBm</td>
<td>-131</td>
</tr>
<tr>
<td></td>
<td>0.1</td>
<td>-26 dB</td>
<td>-54 dBm</td>
<td>-131</td>
</tr>
<tr>
<td></td>
<td>0.05</td>
<td>-32 dB</td>
<td>-60 dBm</td>
<td>-131</td>
</tr>
</tbody>
</table>

The calibration constant can be derived through the system gain as shown in equation 8-14.

The derivation of equation 8-14 is in Chapter 6.

\[
V_{out,rms}^2 (f_m) = \left( K_\phi 2\pi \tau_d \right)^2 \Delta f_{rms}^2 (f_m) = K_d^2 \cdot \Delta f_{rms}^2 (f_m)
\] (8-14)

The calibration constant is a function of the total system gain and the delay time ($\tau_d$) as shown in equation 8-14. Therefore, this calibration constant will be calculated for each DUT in order to achieve accurate measurement results since the calibration constants will vary depending
on the carrier power and the carrier frequency. This is because the fabricated system’s gain has limitations in the input power and the operational frequency. As explained in chapter 7, the delay line and phase shifter have are limited in input power since their peak-to-peak voltage amplitudes are limited to -3dBm. Also, the delay line gain drops significantly over 1.5 GHz since the 100 cascaded stages of the delay cell reduces the operational frequency of the entire delay line. Also, the mixer shows input power limitations. With a signal input greater than 5dBm, the output shows gain compression which limits the input linear power range of the system. The mixer gain varies depending on the carrier frequency. From 500MHz to 2GHz, the mixer gain variation is less than 2dB. Thus, for up to a 1.5GHz input signal with less than 0dBm power, the calibration constant variation shows little variation (<5dB).

8.3. System Sensitivity Measurement

The phase noise system DC output represents the DUT noise output which contains phase noise information. This noise output should be converted to a phase noise magnitude by using the measured calibration constant. The final phase noise can be obtained through equation 8-15.

\[ L(f_m)[dBc/Hz] = S_v(f_m) - K_d - 20\log(S_v(f_m)) - 3 - 10\log(B) \]  

(8-15)

where \( S_v(f_m) \) is the output power, \( K_d \) is the calibration constant and \( B \) is the resolution bandwidth of the measured output power.

The system sensitivity directly relates to the linearity measurement in terms of noise level since low power input can not be detected at the output due to system generated noise. The sensitivity defines the minimum detectable phase noise level without being affected by the system noise level in this work. Thus, the sensitivity of the fabricated system is calculated based on a linearity measurement. The minimum detectable signal level is set by the noise floor level. The system sensitivity at a 1 MHz offset is derived in equation 8-16 and is based on the response
in Figure 8-6 A). Equation 8-17 shows the system sensitivity at a 100kHz offset. The minimum detectable signal level is almost same while measuring with the same resolution bandwidth with the offset ranging from 100Hz to 1MHz. Thus, the system sensitivity depends on the offset frequency so that the system sensitivity shows a slope of 20dB/Decade. Figure 8-5 B) shows the system sensitivity as a function of offset frequency in log scale.

\[
\mathcal{L}(f_m)[dBc/Hz] = S_v(f_m) - K_d - 20 \log(f_m) - 3 - 10 \log(B) \\
= -140 - (-131) - 20 \log(10^6) - 3 - 10 \log(10^3) \\
= -152 \text{ dBC/Hz} \\
\]

(8-16)

\[
\mathcal{L}(f_m)[dBc/Hz] = S_v(f_m) - K_d - 20 \log(f_m) - 3 - 10 \log(B) \\
= -140 - (-131) - 20 \log(10^5) - 3 - 10 \log(10^3) \\
= -132 \text{ dBC/Hz} \\
\]

(8-17)

Figure 8-6. Sensitivity A) small output test signal (FM dev=2 Hz, FM rate =1 MHz) B) System sensitivity.

Ideally, the system can detect -152 dBC/Hz at 1MHz offset frequency. This calculation did not consider any 1/f device noise since the system noise floor in simulation is less than the sensitivity level up to 1MHz as shown in Figure 8-7.
The output noise shows $1/f$ noise slope of up to 1MHz and over 10 MHz the system noise floor drops 20 dB/Decade since the active RC filter followed by mixer has around a 10MHz operational bandwidth. The main noise source comes from the down-conversion mixer as the noise analysis shows in Chapter 6. In particular, the mixer is implemented by four NMOS devices and followed by an active RC filter. This active RC filter is the main contributor of the system noise floor. However, the noise analysis of this mixer shows less than -110 dB at 100 Hz offset. The mixer noise simulation shows a lower noise floor than the system sensitivity level up to 1MHz. Therefore, the mixer device noise can be ignored in this case. However, other noise sources such as coupling noise and substrate noise can still impact the system.

**8.4. Phase Noise Measurement**

In order to verify the system performance, the proposed system characterized two signal generators and one commercial VCO. The first measurement was performed with an Agilent
E8254A signal generator. The Agilent E8254A is based on a PSA which shows a superior noise floor compared to other types of signal generators. The measured results are compared to the Agilent E4448A spectrum analyzer phase noise measurement results. The signal generator specifications generally provide the noise floor information at specific frequency so that the measured results can be compared the signal generator noise floor specifications. Also, the spectrum analyzer has a noise specification. This noise specification limits the accuracy of the spectrum analyzer measurement results.

Figure 8-8. Phase noise measurement procedure A) input test signal B) system output.
Figure 8-8 shows the measurement procedure and actual output spectrum. The system output is measured by a input filter bandwidth depending on offset frequency. In this series of measurements, the measured resolution bandwidths, RWBs of the spectrum analyzer are set to 1kHz to 10kHz (RBW=82Hz), 10kHz to 100kHz (RBW=820Hz), 100kHz to 1MHz (RBW=8.2kHz) and 1MHz to 10MHz (RBW=82kHz). The RBWs are set at the input stage of the spectrum analyzer. Since spectrum analyzers measure the RF signal power in a specific bandwidth, they can clearly be used to measure phase noise. Most modern analyzers include software functions which will convert a measured signal level from its absolute value to the equivalent noise signal in a 1Hz bandwidth; then, a phase noise measurement can be derived.

The system output shows around 10 dB difference per decade caused by the spectrum analyzer resolution bandwidth. A higher offset frequency requires 10 times bigger resolution bandwidth or measurement time can be excessive. Figure 8-8 shows the measured phase noise for 1GHz 0dBm input signal generated by E8254A.

Phase noise result shows good agreement ranging from 3kHz to 1MHz. Above a 1MHz offset frequency, there is a severe roll-off because the active RC filter which is a part of active mixer has less than a 10MHz operational bandwidth since the active RC filter use a CMOS OPAMP. As shown in Figure 7-23, the gain reduction is around 20 dB per decade above 10MHz. However, the measurement shows a reduced operation bandwidth since there is several parasitic capacitance contributions from RF bonding pads and long connection lines. Up to 10 kHz, spectrum analyzer measurement results show a little change due to its limitations. The discriminator system results can not accurate measure the phase noise results from DC up to 3 kHz since the system noise floor (sensitivity) is higher than DUT’s signal noise. Thus, from DC to 3 kHz, the system shows the system noise floor instead of characterizing the DUT’s phase
noise. This is due to $1/f$ noise and $V_T$ mismatch of the CMOS transistors throughout the discriminator system.

Figure 8-9. Phase noise measurement for 1GHz 0dBm input generated by Agilent E8542A.

Figure 8-10 shows the phase noise measurement results for characterizing an input signal of 500MHz 0dBm from an Agilent E8542A. The measured results show similar behavior to the characterized 1GHz carrier input. The close-in offset frequency (< 3kHz) shows a big deviation due to the discriminator system’s poor sensitivity. However, the discriminator system response ranging from 3 kHz to 1 MHz follows the DUT’s phase noise response. Above 1 MHz offset, the discriminator system response shows a gain roll-off due to the active RC filter bandwidth limitations. The close-in measured phase noise of the proposed system shows lower DUT phase noise response below the system sensitivity. The system sensitivity can be determined by the
spectrum analyzer resolution bandwidth. A smaller offset frequency allows detection of a lower power signal than at a higher offset frequency. In this work, the system sensitivity is calculated in an actual situation, not in ideal situation. Ideally, system simulations in Spectre shows less than -160 dBC/Hz at a 1MHz offset. Thus, there is around 5~10dB deviation in sensitivity calculation from the ideal simulation.

Figure 8-10. Phase noise measurement for 0.5GHz 0dBm input generated by an Agilent E8542A. Figure 8-9 and 8-10 use PSA type signal generator which has superior noise sidebands. The two measured results from the spectrum analyzer are close to the spectrum analyzer noise floor which degrades the measurement accuracy. Thus, an ESA signal generator is also used to generate a noisy input signal. The ESA signal generator usually has a higher noise sideband than the spectrum analyzer.
Figure 8-11 shows the measured results from using both the discriminator system and the spectrum analyzer. The spectrum analyzer measured results shows a higher noise sideband than the spectrum analyzer’s noise floor. Thus, the accuracy of the spectrum analyzer is enhanced when compared to PSA signal generator measurement results.

![Phase Noise Measurement](image)

Figure 8-11. Phase noise measurement for 1GHz 0dBm input generated by Agilent E4421B.

Figure 8-12 shows the proposed system measurement results follow the spectrum analyzer result up to a 1MHz offset frequency. Above a 1MHz offset, the gain is reduced severely.

Figure 8-12 illustrates a 500MHz 0dBm input signal generated by an Agilent E4421B signal generator. The system and spectrum analyzer response show the same behavior as explained in Figure 8-11. The close-in (<10kHz) phase noise measurement of the discriminator system follows the system sensitivity curve since the system sensitivity is higher than the measured phase noise.
Figure 8-12. Phase noise measurement for 0.5GHz 0dBm input generated by Agilent E4421B.

For the final verification of the discriminator system, a commercial external VCO (mini-circuits ZX95-1700W-S) is measured with different tuning voltages (600MHz, 800MHz, and 1GHz). The different tuning voltages show different phase noise performances. So, this measurement provides a good insight into the capabilities of the on-chip discriminator system.

Figure 8-13 shows the 1GHz VCO phase noise measurement results. The close-in phase noise of the external VCO shows very low phase noise performance below the system sensitivity level. However, the noise peaking arises at around a 60 kHz offset frequency. The proposed system shows noise peaking at the same offset frequency.

The phase noise performance over the 10kHz ~ 1MHz band shows good agreement between the proposed system and the spectrum analyzer response.
Figure 8-13. Phase noise measurement for 1GHz 0dBm input generated by the commercial external VCO (mini-circuits ZX95-1700W-S).

Figure 8-14 and 8-15 shows the phase noise measurement results for 800MHz input and 600MHz input signals. The noise peaking happens at different offset frequencies depending on the carrier frequency. The discriminator system shows a similar noise peaking at the same offset frequency as the spectrum analyzer shows. The close-in phase noise in the discriminator system follows the discriminator system sensitivity level due to the external VCO’s superior noise characteristics. For higher offset frequency (>1MHz), the phase noise shows rapid drop as explained in previous measurements.
Figure 8-14. Phase noise measurement for 0.8GHz 0dBm input generated by the commercial external VCO (mini-circuits ZX95-1700W-S).

Figure 8-15. Phase noise measurement for 0.6GHz 0dBm input generated by the commercial external VCO (mini-circuits ZX95-1700W-S).
Figure 8-16 shows 600MHz VCO phase noise measurement results after compensating for the gain roll-off. The gain roll-off compensation is performed by adding \(20\log(f_m/10^6)\) on the phase noise results ranging from 1MHz to 10MHz. With proper compensation of the system response, the proposed system can measure the accurate phase noise of DUT as long as the system sensitivity is low enough.

Figure 8-16. Compensated phase noise measurement for 0.6GHz 0dBm input generated by the commercial external VCO (mini-circuits ZX95-1700W-S).

The measured results for several DUTs demonstrate the possibility of on-chip phase noise evaluation ranging from 3kHz to 2MHz. The main limitations of this system arise from the poor system sensitivity level for low offset frequencies and the operational bandwidth limitation of active RC filter for high offset frequency (> 1MHz). The gain roll-off at higher offset frequencies can be compensated since the gain drop ratio of OPAMP is known (-20dB/Decade). As shown in
Figure 8-6, the system noise floor is lower than the system sensitivity. Thus, the mixer down-conversion noise and the noise generated by active delay line and phase shifter can be ignored up to 1MHz where the sensitivity and the system noise floor intersect. In order to increase the system capability for phase noise evaluation, the whole system is optimized to lower the system noise level by designing each building block not to impose any additive noise. By considering the system noise analysis in Chapter 6, the mixer should be optimized to minimize the noise and the active RC filter needs to be optimized in order not to generate excessive noise. An active RC filter also needs to be designed to have a wide operational bandwidth and not to limit the range of the offset frequency.

8.5. Conclusion

This work demonstrates an on-chip phase noise measurement for the first time. The proposed phase noise measurement system is used to be measured various noisy sources to check the system’s performance. The measurement results show an accurate phase noise performance ranging from 3kHz to 1MHz. The system sensitivity is achieved -135dBc/Hz at 100kHz offset and -155dBc/Hz at 1MHz offset. The measurement limitations are mainly due to the system sensitivity at lower offset frequency and to gain roll-off at higher offset frequencies. For higher offset frequency response, the gain roll-off can be compensated through mathematical manipulation with the consideration of OPAMP gain roll-off in the signal path.

The proposed system measurement shows the possibility of cost reduction by replacing the expensive phase noise test equipments with the simple 1mm x 1.5mm chip. The system sensitivity can be enhanced by increasing the double-balanced mixer gain or by increasing the signal delay time in the discriminator. However, the mixer should be considered a primary source of noise generation since it affects close-in phase noise sensitivity.
CHAPTER 9
SUMMARY AND CONCLUSION

9.1. Summary

In this dissertation, balun integrated RF/Microwave probes and an embedded phase noise measurement system are designed for RF IC’s testing. The balun integrated probe is analyzed first to find the optimum design parameters and is simulated with aid of Ansoft HFSS and Agilent ADS. The final design is fabricated in Cascade Microtech Thin Film Technology. The embedded phase noise measurement system is analyzed in terms of the noise and the system gain and fabricated in the IBM8HP process. A new embedded phase noise measurement system is proposed based on the previously published FM discriminator method.

In chapter 1 and chapter 2, the motivation and inspiration of this Ph.D work are introduced and the background of this work is explained.

Chapter 3 presents a new Marchand balun analysis. The new method introduces the extraction of an optimized design that depends on the input or output termination impedance variation. A full SPICE simulation demonstrates the new analysis. The analysis provides the optimized design equations for a balun integrated probe.

Chapter 4 and 5 shows the integration of a RF/Microwave balun probe using transmission lines finite ground broadside coupled lines based on coplanar strip and coplanar waveguide that create difficulty in the extraction of the structure dimensions. The structures presented make it difficult to extract the characteristic parameters due to the long simulation time and the large effort when one uses a commercial EM solver. In this work, new closed form equations for coplanar strip line and coplanar waveguide are developed to extract the desired design parameters. The analyses are based on the conformal mapping method and verified through a comparison with FEM based simulations. The final designs are simulated with Ansoft HFSS in
Chapter 6 introduces an embedded phase noise measurement system and explains the basic theory of phase noise and conventional phase noise measurement methods. Through the comparison between conventional measurement methods, a delay-line-based phase noise system is chosen for implementing an embedded system. In order to optimize the performance of the embedded measurement system, the proposed system is analyzed in terms of noise and system gain. System design considerations are presented through the analysis. Final system validity is demonstrated through a system simulation performed by Agilent ADS DSP based simulations.

Chapter 7 shows a system implementation in IBM8HP technology. The entire system and its components are optimized, designed and fabricated. The active balun is implemented by common-source/common gate topology. The design is optimized for a 1 GHz operational frequency. The proposed delay line can achieve 0 dB gain and 3 ns delay at a 1 GHz operational frequency by introducing a level shifting technique in order to prevent the signal from distorting. A phase shifter also be used in a circuit module similar to a delay line except that interface to a symmetric load to control signal quadrature and time delay is required. A self-biasing technique makes up for the output DC level variations. The double balanced mixer in this system works as a phase detector while it suppresses all fundamental and harmonic signal components and leaves only the noise response. In order to achieve a flat noise response up to 100 MHz, an active RC filter uses a feedback capacitance to increase the operational bandwidth and the system stability. Chapter 8 shows the final system measurement method which results in a low noise floor and a high sensitivity. Appendix A and B explain the parameter extraction of broadside coupled CPS
and CPW coupled line equations through the conformal mapping method. The closed form equation is presented and verified by 3-D EM simulations (HFSS). Appendix C explains the phase noise system noise floor depending on key circuits in the system causing mismatch due to process variation and mixer input mismatch. Also, Appendix D shows the system’s limitation based on the FM discriminator. The system accuracy dependence on the discriminator delay time is explained.

9.2. Conclusion

RF IC test cost is becoming a major part of chip manufacturing cost thanks to recent mass production technology. In order to reduce the test cost of RF ICs, much research has been performed over the last few decades but further work is needed. This dissertation work is finding test cost reduction methods by using differential probes and embedded test systems.

Many academic and organizations study RFICs to improve their functions. But the same effort is not put into test. Particularly, for the differential circuits, expensive test equipment is required due to the lack of alternative on-chip test.

In this work, by developing the balun integrated probe, expensive differential measurement equipment can be replaced with the conventional two port equipment. A new analysis method for the Marchand balun is introduced that optimizes the balun design for the circuit applications. For example, some designs do not optimize their load terminations to $50 \, \Omega$. The proposed analysis makes it possible to design a balun as a function of the termination impedance variation. Also, in order to build a balun integrated probe, a new field analysis method is presented through the conformal mapping method. The proposed field analysis method introduces a close-form equation for a specific transmission structure. Thus, the design time to find the optimized parameters for a particular circuit application greatly is reduced. The fabricated balun integrated
probe through the proposed analyses achieves superior performance compared to conventional balun designs.

An embedded phase noise measurement system based on FM discriminator methods is developed for RFIC production test. The conventional measurements using this method need a complicated and arduous test set-up and extensive test time to complete device characterization. However, the system in this dissertation can easily convert the phase noise at high frequency carrier into baseband noise. Thus, the required measurement step can be reduced to a simple step which checks baseband noise at DC with a baseband frequency analyzer or an ADC and DSP system. In addition, the system introduces auto-adjustment to find the optimum measurement point by controlling a variable phase shifter. Compared to a conventional external phase noise test system such as the HP E5500, the embedded test system can save test time by removing the input quadrature manual adjustment.

The phase noise system is implemented in IBM8HP technology. The measured system performance shows an effective accuracy from 3kHz to 1MHz without gain compensation. The sensitivity is -155dBc at 1MHz offset frequency.
A.1. Analysis of Broadside Coupled Coplanar Striplines (CPS) with finite ground plane

Figure A-1 shows the symmetric finite ground broadside coupled coplanar stripline’s cross-section with three dielectric layers. Signal line width is $a$ and the gap between the signal line and ground is $b-a$. The ground width is $c-a$. Due to the limited ground, the field distribution will distort a lot, which makes the big difference of the characteristics of both finite and infinite ground coupled-line structures. Dielectric constant and height of the dielectric between the signal lines are $\varepsilon_{r1}$ and $h_1$, respectively. Dielectric constant of the dielectric located on upper and lower signal lines are $\varepsilon_{r2}$ and $h_2$, respectively. Let us call them the intermediate and upper dielectric.

Analysis of this structure starts from the isolation of two different modes [A.1], which are the even mode and the odd mode as shown in Figure A-2.
Figure A-2. Field distribution under A) even mode excitation. B) odd mode excitation.

**A.2. Even Mode**

The field distribution is similar to the case of infinite ground plane as shown in Figure A-2 A). The total even mode capacitance per unit length can be obtained by the sum of the three components, $C_{el1}$, $C_{el2}$ and $C_{el3}$, representing the electric field in the intermediate region, the upper dielectric region and the air region with the partial capacitance method [A.2] [A.3] [A.4] [A.5].
Figure A-3 shows the detailed procedure for the conformal mapping method. By the partial capacitance method, the total capacitance can be divided into three different region capacitances such as the intermediate dielectric region capacitance, the upper dielectric region capacitance and air-filled region capacitance. Two conductor lines form the air region capacitance and the dielectric region capacitances.

The transformation from $Z$-plane to $T$-plane uses equation A-1 through A-2 for the intermediate dielectric region and the upper dielectric region, respectively.

$$t = \exp\left(\frac{\pi \cdot z}{h_1}\right)$$ \hspace{1cm} (A-1)
\[ t = \exp\left(\frac{\pi \cdot z}{h_2}\right) \] (A-2)

The final transformation from \( T \)-plane to \( W \)-plane is performed by Schwarz-Christoffel transformation by equation A-3.

\[
w = \int \frac{dt}{\sqrt{\left(t-t_0\right)\left(t-t_2\right)\left(t-t_3\right)}} \quad (A-3)
\]

The final even mode capacitance is described by equation A-4.

\[
C_E = C_{e1} + C_{e2} + C_{e3} = \varepsilon_0 \varepsilon_{r1} \frac{K(k_{e1})}{K'(k_{e1})} + \varepsilon_0 (\varepsilon_{r2} - 1) \frac{K(k_{e2})}{K'(k_{e2})} + \varepsilon_0 \frac{K(k_{e3})}{K'(k_{e3})} \quad (A-4)
\]

where \( K(k) \) is the complete elliptic integral of the first kind with module \( k \) and \( K'(k) \) its complement.

\[
k_{e1} = \sqrt{\left(\exp\left(\frac{\pi \cdot a}{h_1}\right) - 1\right) \left(\exp\left(\frac{\pi \cdot c}{h_1}\right) - \exp\left(\frac{\pi \cdot b}{h_1}\right)\right)}
\]

\[
k_{e2} = \sqrt{\left(\exp\left(\frac{\pi \cdot a}{h_2}\right) - 1\right) \left(\exp\left(\frac{\pi \cdot c}{h_2}\right) - \exp\left(\frac{\pi \cdot b}{h_2}\right)\right)}
\]

\[
k_{e3} = \sqrt{\frac{a \cdot (c - b)}{b \cdot (c - a)}} \quad (A-5)
\]

The effective dielectric constant and the characteristic impedance are derived as the equation A-6 and A-7.

\[
\varepsilon_{eff,E} = 1 + \left(\varepsilon_{r1} - 1\right) \frac{K(k_{e1})}{K'(k_{e1})} + \left(\varepsilon_{r2} - 1\right) \frac{K(k_{e2})}{K'(k_{e2})} + \varepsilon_0 \frac{K(k_{e3})}{K'(k_{e3})} + \frac{K(k_{e1})}{K'(k_{e1})} + \frac{K(k_{e3})}{K'(k_{e3})} \quad (A-6)
\]
A.3. Odd Mode

With the assumption of an electric wall in the center of the coupled lines, the analytic expression for the odd mode capacitance per unit length can be derived by the sum of three components, $C_{o1}$, $C_{o2}$ and $C_{o3}$, representing the electric field in the intermediate region, the upper dielectric region and the air region with the partial capacitance method. $C_{o2}$ and $C_{o3}$ are similar to the even mode excitation while $C_{o1}$ has another ground plane due to an electric wall, which complicate the analysis. For the derivation of $C_{o1}$, the analysis needs another step by dividing $C_{o1}$ in two parallel rectangular capacitances.

Figure A-4. Detailed conformal mapping procedure for the odd mode excitation
Figure A-4 shows the detailed procedure for the odd mode excitation. The additional procedure for $C_{o1}$ is performed as shown Figure A-5. The transformation from $Z$-plane to $T$-plane uses equation A-8 through A-9 for the intermediate dielectric region and the upper dielectric region, respectively.

\[
t = \exp \left( \frac{\pi \cdot Z}{h_1} \right) \quad \text{(A-8)}
\]

\[
t = \exp \left( \frac{\pi \cdot Z}{h_2} \right) \quad \text{(A-9)}
\]

![Figure A-5. Conformal mapping procedure for the intermediate dielectric region in odd mode excitation.](image)

The final transformation from $T$-plane to $W$-plane for $C_{o2}$ and $C_{o3}$, is performed by Schwarz-Christoffel transformation by equation A-10.
\[ w = \int \frac{dt}{\sqrt{(t-t_0)(t-t_a)(t-t_b)(t-t_i)}}; \quad i = 4 \text{ or } 6 \quad (A-10) \]

After the transformation to W-plane, the rectangular capacitance of \( C_{o1} \) is divided into two parallel capacitances in Figure A-5 by assuming a magnetic wall for the dashed line in Figure A-5 \[ \text{[A.6].} \]

The transformation is performed by equation A-11 and A-12.

\[ t' = \cosh^2 \left( \frac{\pi \cdot z}{2H_1} \right) \quad (A-11) \]

\[ w' = \int \frac{dt'}{\sqrt{(t'-t'_a)(t'-t'_b)(t'-t'_c)(t'-t'_d)}} \quad (A-12) \]

The final even mode capacitance is described by equation A-13.

\[ C_O = C_{o1} + C_{o2} + C_{o3} = \varepsilon_0 \varepsilon_{r1} \left( \frac{K(k_{o1,1})}{K'(k_{o1,1})} + \frac{K(k_{o1,2})}{K'(k_{o1,2})} \right) + \varepsilon_0 (\varepsilon_{r2} - 1) \frac{K(k_{o2})}{K'(k_{o2})} + \varepsilon_0 \frac{K(k_{o3})}{K'(k_{o3})} \quad (A-13) \]

where \( K(k) \) is the complete elliptic integral of the first kind with module \( k \) and \( K'(k) \) its complement.

\[ k_{o1} = \left\{ \begin{array}{c} \exp \left( \frac{\pi \cdot a}{h_1} \right) - 1 \exp \left( \frac{\pi \cdot b}{h_1} \right) \\ \exp \left( \frac{\pi \cdot b}{h_1} \right) - 1 \exp \left( \frac{\pi \cdot a}{h_1} \right) \end{array} \right\} \]

\[ k_{o1,1} = 1 \left\{ \begin{array}{c} \tanh \left( \frac{\pi \cdot W_a}{2H_1} \right) \cdot \tanh \left( \frac{\pi \cdot W_a}{2H_1} \right) \end{array} \right\} \]

\[ k_{o1,2} = 1 \left\{ \begin{array}{c} \tanh \left( \frac{\pi \cdot (W_1-W_a)}{2H_1} \right) \cdot \tanh \left( \frac{\pi \cdot (W_1-W_a)}{2H_1} \right) \end{array} \right\} \]

\[ k_{o2} = \left\{ \begin{array}{c} \exp \left( \frac{\pi \cdot a}{h_2} \right) - 1 \exp \left( \frac{\pi \cdot c}{h_2} \right) - \exp \left( \frac{\pi \cdot b}{h_2} \right) \\ \exp \left( \frac{\pi \cdot c}{h_2} \right) - 1 \exp \left( \frac{\pi \cdot a}{h_2} \right) \end{array} \right\} \]

\[ k_{o3} = \frac{a \cdot (c-b)}{b \cdot (c-a)} \quad (A-14) \]
$W_1, W_2, W_3, W_4$ and $H_1$ can be derived as shown in equation A-15.

$$
\frac{W_1}{H_1} = \frac{K(k_{o1})}{K'(k_{o1})}
$$

$$
W_2 = F \arcsin \left\{ \frac{\exp \left( \frac{\pi \cdot b}{h_1} \right) \cdot \left( t_{\infty} \right) - 1}{\exp \left( \frac{\pi \cdot b}{h_1} \right) \cdot \left( t_{\infty} - 1 \right)} \right\}, k_{o1}
$$

$$
W_3 = F \arcsin \left\{ \frac{\exp \left( \frac{\pi \cdot b}{h_1} \right) \cdot \left( 1 - \exp \left( \frac{\pi \cdot c}{h_1} \right) \right)}{\exp \left( \frac{\pi \cdot b}{h_1} \right) \cdot \left( \exp \left( \frac{\pi \cdot c}{h_1} \right) - 1 \right)} \right\}, k_{o1}
$$

$$
W_4 = \frac{W_2 + W_3}{2}
$$

where $F(\phi, k)$ is the incomplete elliptic integral of the first kind, written in Jacobi’s notation.

The effective dielectric constant and the characteristic impedance are in equation A-16 and A-17.

$$
\varepsilon_{eff \_o} = 1 + \frac{(\varepsilon_{r1} - 1) \left( \frac{K(k_{o1\_1})}{K'(k_{o1\_1})} + \frac{K(k_{o1\_2})}{K'(k_{o1\_2})} \right) + (\varepsilon_{r2} - 1) \frac{K(k_{o2})}{K'(k_{o2})}}{\frac{K(k_{o1\_1})}{K'(k_{o1\_1})} + \frac{K(k_{o1\_2})}{K'(k_{o1\_2})} + \frac{K(k_{o3})}{K'(k_{o3})}}
$$

$$
Z_{0o} = \frac{120\pi}{\sqrt{\varepsilon_{eff \_o}} \left[ \frac{K(k_{o1\_1})}{K'(k_{o1\_1})} + \frac{K(k_{o1\_2})}{K'(k_{o1\_2})} + \frac{K(k_{o3})}{K'(k_{o3})} \right]}
$$

Simple and accurate formulas are available for solving the complete elliptic integral of the first kind [A.7]. These are given in equation A-17.
\[
\frac{K(k)}{K'(k)} = \begin{cases} 
\frac{\pi}{\ln(2 \cdot \left( \frac{1 + \sqrt{k'}}{1 - \sqrt{k'}} \right) / \left( \frac{1 - \sqrt{k'}}{1 + \sqrt{k'}} \right))} 
& 0 \leq k^2 \leq 0.5 \\
\frac{\ln(2 \cdot \left( \frac{1 + \sqrt{k'}}{1 - \sqrt{k'}} \right) / \left( \frac{1 - \sqrt{k'}}{1 + \sqrt{k'}} \right))}{\pi} 
& 0.5 \leq k^2 \leq 1 
\end{cases} 
\quad (A-17)
\]

where \( k' = \sqrt{1 - k^2} \)
APPENDIX B
EXTRACTION OF BROADSIDE COUPLED COPLANAR WAVEGUIDE
CHARACTERISTIC PARAMETERS WITH FINITE GROUND PLANE

B.1. Broadside Coupled Coplanar Waveguide (CPW) with finite ground plane.

A new analytic expression for the broadside coupled CPW with finite ground plane is proposed for the first time. This method can be used on the transmission line circuit modeling in the standard CMOS process due to their simplicity. Figure B-1 shows the cross-section of the analyzed structure. Due to their finite ground plane, the analysis is much complicated compared to infinite ground plane case.

![Figure B-1. Cross-section of broadside coupled coplanar waveguide with finite ground plane.](image)

The field distributions of both even and odd mode are shown in Figure B-2. The finite ground plane causes the field distortion and the final characteristics will be very different from the ones of an infinite ground plane case.

The analysis starts from isolating the even and odd mode excitation. The even mode excitation assume a magnetic wall in the center line while the odd mode excitation assume a electric wall [B.1].
Figure B-2. Field distribution of the broadside coupled CPW under A) an even mode excitation and B) an odd mode excitation with a bottom and top ground plane.

B.2. Even Mode

Figure B-3 shows the field distribution of the upper half of the finite ground broadside coupled coplanar waveguide for even mode excitations. The bottom dashed line describes the magnetic wall while both signal lines carry the same amplitude and phase signals and are symmetrical. This assumption is always true as long as the structure behaves as a coplanar line [B.1]. The half plane of Figure 4-3 will be used to derive the even mode capacitance. The total even mode capacitance per unit length can be obtained by the sum of three components, $C_{e1}$, $C_{e2}$ and $C_{e3}$, representing the electric field in the lower dielectric region, the air region and the upper dielectric region with the partial capacitance method [B.2].
Figure B-3. Field distribution of the finite ground broadside coupled CPW under an even mode excitation.

Figure B-4 describes the detailed procedure for the CPW conformal mapping. The total capacitance can be divided into three different regions; there are the lower dielectric region, the air-filled region and the upper dielectric region. In the air region, two conductor lines form the air region capacitance and the dielectric region capacitance [B.3].

Figure B-4. Detailed conformal mapping procedure for the even mode excitation.
The transformation uses equation B-1 through B-3 for the air region and the dielectric region.

\[
t = \sinh^2 \left( \frac{\pi \cdot z}{2h_i} \right)
\]  
(B-1)

\[
t = z^2
\]  
(B-2)

\[
t = \cosh^2 \left( \frac{\pi \cdot z}{2h_i} \right)
\]  
(B-3)

The Schwarz-Christoffel transformation from \( T \)-plane to \( W \)-plane is in equation B-4.

\[
w = \int \frac{dt}{\sqrt{(t-t_0)(t-t_a)(t-t_b)(t-t_c)}}
\]  
(B-4)

The final even mode capacitance is described by equation (B.5).

\[
C_E = 2\varepsilon_0 \varepsilon_{\text{rr}} \frac{K(k_{e1})}{K'(k_{e1})} + 2\varepsilon_0 \frac{K(k_{e2})}{K'(k_{e2})} + 2\varepsilon_0 \left( \varepsilon_{\text{rr}} - 1 \right) \frac{K(k_{e3})}{K'(k_{e3})}
\]  
(B-5)

where \( K(k) \) is the complete elliptic integral of the first kind with module \( k \) and \( K(k') \) its complement.

\[
k_{e1} = \sinh \left( \frac{\pi \cdot a/2h_i}{2h_i} \right) \sqrt{\frac{1 - \sinh^2 \left( \frac{\pi \cdot b/2h_i}{2h_i} \right)}{1 - \sinh^2 \left( \frac{\pi \cdot c/2h_i}{2h_i} \right)}}
\]

\[
k_{e2} = \frac{a}{b} \sqrt{\frac{1 - b^2/c^2}{1 - a^2/c^2}}
\]  
(B-6)

\[
k_{e3} = \sinh \left( \frac{\pi \cdot a/2h_2}{2h_2} \right) \sqrt{\frac{1 - \sinh^2 \left( \frac{\pi \cdot b/2h_2}{2h_2} \right)}{1 - \sinh^2 \left( \frac{\pi \cdot c/2h_2}{2h_2} \right)}}
\]

The effective dielectric constants and the characteristic impedance are derived as equation B-7 and B-8.
The asymptote of these equation when the ground plane width grows infinite ($c \rightarrow \infty$) agrees with the infinite ground plane case \[B.4\].

### B.3. Odd Mode

The field distribution of Figure B-5 explains the capacitance of the odd mode excitation. There is an electrical wall in the center of the coupled lines. The analytic expression for the odd mode capacitance per unit length can be derived by the sum of three components, $C_{o1}$, $C_{o2}$ and $C_{o3}$, representing the electric field in the lower dielectric region, air region and the upper dielectric region.

![Field distribution of the CPW with finite ground plane under an odd mode excitation.](image)

Figure B-5. Field distribution of the CPW with finite ground plane under an odd mode excitation.

Figure B-6 shows the conformal mapping procedure for the dielectric region. The electrical wall is a virtual ground. The mapping procedure is divided into three parts via the partial capacitance method as shown in Figure B-6. The air region capacitance and the upper dielectric region capacitance are the same as the even mode. But the lower dielectric region capacitance is

\[
\varepsilon_{\text{eff}E} = 1 + \frac{\left[ (\varepsilon_1 - 1) \frac{K(k_{e1})}{K'(k_{e1})} + (\varepsilon_2 - 1) \frac{K(k_{e3})}{K'(k_{e3})} \right]}{\left[ \frac{K(k_{e1})}{K'(k_{e1})} + \frac{K(k_{e2})}{K'(k_{e2})} \right]}
\]

\[
Z_{0E} = \frac{60\pi}{\sqrt{\varepsilon_{\text{eff}E}}} \left[ \frac{K(k_{e1})}{K'(k_{e1})} + \frac{K(k_{e2})}{K'(k_{e2})} \right]
\]
more complicated to analyze due to the finite ground widths. For an odd mode excitation, the lower dielectric region capacitance is needed to extract additional parameters.

\[
\tau = \sinh^2 \left( \frac{\pi \cdot z}{2h_1} \right)
\]  

(B-9)

The remaining steps of the conformal mapping use the Schwarz-Christoffel transformation as shown in equation B-10.
After the transformation to the w-plane, the rectangular capacitance is divided into two parallel rectangular capacitances in Figure B-7 (b) by assuming a magnetic wall for the dashed line in Figure B-7 (a) [B.5].

Equation B-11 and B-12 perform the transformation.

\[
t' = \cosh\left(\frac{\pi \cdot z'}{2H_1}\right)
\]  

\[
k_{o1} = \tanh\left(\frac{\pi \cdot a}{2h_1}\right) / \tanh\left(\frac{\pi \cdot b}{2h_1}\right) \tag{B-10}
\]
\[ w' = \int \frac{dt'}{\sqrt{(t' - t'_0)(t' - t'_a)(t' - t'_b)(t' - t'_c)}} \]  \hspace{1cm} (B-12)

Finally, the odd mode capacitance is derived as shown in equation B-13 to B-15.

\[ C_o = 2\varepsilon_0\varepsilon_r \left(\frac{K(k_{o_1,1})}{K'(k_{o_1,1})} + \frac{K(k_{o_1,2})}{K'(k_{o_1,2})}\right) + 2\varepsilon_0 \frac{K(k_{o_2})}{K'(k_{o_2})} + 2\varepsilon_0 (\varepsilon_r - 1) \frac{K(k_{o_3})}{K'(k_{o_3})} \]  \hspace{1cm} (B-13)

where

\[ k_{o_1,1} = \frac{1}{\tanh\left(\frac{\pi \cdot W_2}{2H_1}\right) \cdot \tanh\left(\frac{\pi \cdot W_4}{2H_1}\right)} \]

\[ k_{o_1,2} = \frac{1}{\tanh\left(\frac{\pi \cdot (W_1 - W_4)}{2H_1}\right) \cdot \tanh\left(\frac{\pi \cdot (W_1 - W_3)}{2H_1}\right)} \]  \hspace{1cm} (B-14)

\[ k_{o_2} = k_{e,2} \]

\[ k_{o_3} = k_{e,3} \]

\[ W_1, W_2, W_3, W_4 \text{ and } H_1 \text{ can be derived.} \]

\[ \frac{W_1}{H_1} = \frac{K(k_{o_1})}{K'(k_{o_1})} \]

\[ W_2 = F\left(\arcsin\left(\frac{\pi \cdot b}{2h_1}\right) \cdot \tanh\left(\frac{\pi \cdot c}{2h_1}\right), k_{o_1}\right) \]

\[ W_3 = F\left(\arcsin\left(\frac{\pi \cdot b}{2h_1}\right) \cdot \tanh\left(\frac{\pi \cdot c}{2h_1}\right), k_{o_1}\right) \]  \hspace{1cm} (B-15)

\[ W_4 = \frac{(W_2 + W_3)}{2} \]

where \( F(\phi, k) \) is the incomplete elliptic integral of the first kind, written in Jacobi’s notation.

The effective dielectric constants and characteristic impedance are in equation B-16 and B-17.
The expression derived in this section can easily be extended to include infinite ground broadside coupled CPW.
APPENDIX C
SYSTEM MISMATCH RESPONSE

C.1. Signal Distortion due to Delay Line and Phase Shifter

It is important to understand the input signal distortion after passing a signal through an analog delay line circuit. A transient simulation of the analog delay line in the discriminator system was performed and the simulation output was converted to the spectral domain in order to see the degree of distortion. An analog delay line will introduce signal distortion, inevitably, even if the analog delay line is designed to minimize the signal distortion. Figure C-1 indicates the displayed simulation points in yellow in order to help understand of the system functionality.

![System simulation block diagram](image)

Figure C-1. System simulation block diagram.

The transient simulation aims to show the input signal spectrum and output signal spectrum at different delay line output points in order to establish signal distortion levels. Figure C-2 shows the physical points in the circuit simulation used to set and detect the input signal and output signals. A sinusoidal waveform is chosen for the input signal in order to generate a clean spectrum at the input. The simulation results show the delay line output distortion level by comparing the input and output spectrums. Figure C-3 A) shows the 0 dBm input signal spectrum at 1GHz and B) shows the delay line output spectrum at the marked point in Figure C-2.
The active delay line has a limited peak-to-peak voltage swing which restricts the maximum output power (around -3dBm). The fundamental output spectrum (-3dBm at 1GHz) in Figure C-3 B) shows the input spectrum with a small loss (-3dB) and includes other higher order harmonics. Compared to the fundamental signal level, the higher order harmonics are negligible since the higher order harmonics are 40 dB lower than the fundamental signal. The analog delay line is designed for minimizing unwanted signal distortion. This simulation results shows a very low level of signal distortion over the 1GHz band of interest. Another important observation of this simulation result comes from looking at the noise level. The input signal noise level is around -70dBm for entire frequency range of simulation. The analog delay line is designed to achieve around 0dB gain so the output signal noise level shows almost the same level of input noise up to 1.5GHz since the operational frequency of the analog delay line is around 1.5 GHz. Beyond 1.5GHz, the signal and noise show lower values since the analog delay line gain has roll-off beyond 1.5GHz.
Figure C-3 Spectrum of A) the input B) the delay line output

For low level signals, the analog delay line achieves around 0 dB gain for 1GHz signals by controlling delay line gain using the inverting amplifier current source bias. Figure C-4 shows the fundamental signal power which depends on input signal power at 1GHz. As in a typical amplifier, the analog delay line shows linear gain. The gain compression occurs at -3dBm input.
power which is the same power level as the maximum achievable output power. For an input power higher than -3dBm, the analog delay line shows gain compression that is shown in Figure C-4.

![Figure C-4](image.png)

**Figure C-4.** Analog delay line output as a function of input power at 1GHz.

Figure C-5 shows the phase shifter input and output power at 1GHz. The phase shifter shows a similar response to the analog delay line except the phase shifter shows a wider operational bandwidth than that of the analog delay line. The higher order harmonics show magnitudes 40 dB lower than the fundamental signal which can be ignored. The variable phase shifter output suppresses even order harmonics so that the transient response will show a little rectangular waveform shape. In this case, the suppression level is relatively small, thus, the signal experiences only a little distortion. The variable phase shifter achieves a very low level of signal distortion. The phase shifter has a 1.8GHz operational bandwidth. Thus, the signal and noise amplify up to 1.8GHz. The phase shifter is in cutoff beyond 1.8 GHz and should not be used at frequencies higher than 1.8 GHz.
Figure C-5. Variable phase shifter A) input spectrum and B) output spectrum

**C.2. System Mismatch Response**

The output response of the discriminator system mainly depends on the input imbalance at the mixer input since the mixer inputs which are not in quadrature, introduce additional noise beside the DUT’s phase noise. A simulation is performed when the mixer input is in quadrature and not in quadrature. The input has the same signal applied as used in the analog delay line.
transient simulation (sinewave of 1 GHz) and phase shifter simulation is shown in Figure C-3 A). The simulation results for the mixer input signal mismatched case (10° mismatch) are displayed in Figure C-6 and for the matched case are displayed in Figure C-7. Figure C-8 shows the noise floor comparison between the matched case and mismatched case and includes the degree of the mismatch.

The mismatched case shows a higher noise floor which impedes low level phase noise signal detection. Thus, the sensitivity of the system will degrade. Equation C-1 shows the sensitivity level of this case. The resolution bandwidth for this simulation is 20MHz and the offset frequency is 20MHz.

\[
\mathcal{L}(f_m)[\text{dBc/Hz}] = S_v(f_m) - K_d - 20 \log(f_m) - 3 - 10 \log(B)
\]

\[
= -57 - (-131) - 20 \log(2 \cdot 10^7) - 3 - 10 \log(2 \cdot 10^7) = -148 \text{ dBc/Hz}
\]

(C-1)

Figure C-6. Output spectrum A) mismatched (input mismatch 10°) on a linear scale B) mismatched in log scale.
The matching condition can be observed by checking the DC power level. In this simulation case, DC level is -9dBm for a matched signal to the mixer while the mismatched case shows higher power level (-2dBm). Figure C-7 shows an important observation. Compared to Figure C-7 A), the signal levels such as 1GHz and higher order harmonics show almost the same signal power but with a lower noise floor. Thus, the mixer input matching conditions determine the noise floor level of the system. For matched case, the system noise floor can be calculated by equation (C.2).

\[
\mathcal{S}(f_m)[\text{dBc/Hz}] = S_\nu(f_m) - K_s - 20 \log(f_m) - 3 - 10 \log(B) = -68 - (-131) - 20 \log(2 \cdot 10^7) - 3 - 10 \log(2 \cdot 10^7) = -159 \text{ dBc/Hz}
\]

The system sensitivity is -159dBc/Hz. The matched case obviously shows great sensitivity enhancement.

Figure C-8 shows the system response as a function of the level of mismatch. If the mixer inputs are in quadrature, the system response shows the lowest noise level since the mixer cancels out the redundant terms in DUT signal. The matched case introduces the lowest system noise floor as shown in Figure C-8. As the mismatch increases, the noise floor level increases to
some extent. More than $10^\circ$ of the mismatch shows almost the same noise floor level. Figure C-9 shows the system response depending on the level of the input mismatch in log scale. The matched case shows very low noise level for closed-in offset frequency ($<300$ MHz).

Figure C-8. System responses depending on the mismatch in linear scale.

Figure C-9. System responses depending on the mismatch in log scale.
APPENDIX D
SYSTEM LIMITATION

The frequency discriminator method has an inherent limitation during measurement of very close-in phase noise and the specific offset frequency which is determined by time delay $(\tau_d)$ of the delay line. In this section, the system limitations and accurate measurement methods are explained.

D.1. The Discriminator Transfer Response

The discriminator system response is derived in chapter 6. Equation D-1 is the typical system transfer response of the FM discriminator.

\[
\Delta V_{\text{out}} \approx K_\phi 2 \frac{\Delta f}{f_m} \sin\left(\pi f_m \tau_d\right)
\]

\[
= K_\phi 2\pi \tau_d \Delta f \frac{\sin\left(\pi f_m \tau_d\right)}{\pi f_m \tau_d} \quad (\text{For } f_m < \frac{1}{2\pi \tau_d}, \quad \frac{\sin\left(\pi f_m \tau_d\right)}{\pi f_m \tau_d} \approx 1)
\]

\[
= K_\phi 2\pi \tau_d \Delta f
\]

A system sensitivity of the frequency discriminator is determined by the transfer response as shown in equation D-1. It is desirable to make both the phase detector constant $K_\phi$ and the amount of delay $\tau_d$ large. Then, the voltage fluctuations out of a frequency discriminator will be measurable for even small frequency fluctuations $\Delta f$.

The magnitude of the sinusoidal output term of the frequency discriminator is proportional to $\sin(\pi f_m \tau_d)/(\pi f_m \tau_d)$. This implies that the output response will have peaks and nulls, with the first null occurring at $f_m=1/\tau_d$. Increasing the rate of a modulation signal applied to the system will cause nulls to appear at frequency multiples of $1/\tau_d$. 

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To avoid having to compensate for the \( \sin(x)/x \) response, measurements are typically made at offset frequency much less than \( 1/\tau_d \). It is possible to measure at offset frequencies out to and beyond the null by scaling the measured results using the discriminator transfer equation. However, the sensitivity of the system gets very poor near the nulls. The transfer function shows that increasing \( \tau_d \) increases the sensitivity of the system. However, increasing \( \tau_d \) also decreases the offset frequencies that can be measured without compensating for the \( \sin(x)/x \) response. The Discriminators with 50ns line are usable to offsets of 10MHz. Increasing the delay also increases the attenuation of the line. While this has no direct effect on the sensitivity provided by the delay line, it does reduce the signal into the phase detector and can result in decreased \( K_\phi \) and decreased system sensitivity.

In the on-chip discriminator system, the delay is chosen to be 3.5ns. However, the discriminator constant is larger than commercial instruments since the proposed system uses an active mixer instead of using a passive mixer in typical systems.
Equation D-2 exhibits the highest offset frequency of interest for the proposed system.

\[
f_{m,\text{high}} \leq \frac{1}{2\pi\tau_d} = 45 \text{ MHz} \quad (D-2)
\]

\[
f_{m,\text{null}} = \frac{1}{\tau_d} \approx 285 \text{ MHz} \quad (D-3)
\]

Equation D-3 indicates the first null of the system. The highest offset frequency of interest means the maximum measurable frequency without compensating this null.
LIST OF REFERENCES


BIOGRAPHICAL SKETCH

Jae Shin Kim received the B.S. degree in electronic engineering from Yonsei University, Seoul, Korea in 2001 and M.S. degree in electrical engineering from Seoul National University, Seoul, Korea in 2003 and is currently working toward the Ph. D degree at University of Florida, Gainesville, FL.

He worked as a Research Assistant for ISRC from 2001 to 2002. He worked as an Analog Design Engineer for Hynix Semiconductor in 2003. During the spring and summer of 2007, he worked for Cascade Microtech, Beaverton, OR, on the 60GHz passive circuit design. He worked on RF IC and module design as a senior engineer for SiRF Technology from Aug 2008.

Mr. Kim was the recipient of Yonsei Outstanding scholarship in 1994 and University of Florida Alumni Fellowship from 2003 to 2006.