OPTIMIZATION STABILITY OF GATE DIELECTRICS ON GALLIUM NITRIDE

By

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To my family and friends
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The application of gallium nitride (GaN)-based devices requires the use of a gate dielectric to reduce gate leakage, passivate surface traps, and provide isolation between devices. It is critical for the insulator to remain chemically and thermally stable at high temperatures (i.e., 1000°C) during device fabrication and operation. More importantly, it must possess good electrical characteristics such as a high breakdown field, low flatband voltage shift, and low interface trapped charge (Dit). A new dielectric material, known as scandium gallium oxide (Sc2O3)x(Ga2O3)1-x, was investigated. Growth conditions of MgSc2O4 and MgO were also optimized to enhance their environmental stability and improve their electrical results.

All dielectric films were deposited by molecular beam epitaxy (MBE), which uses independent sources to precisely control the film thickness and stoichiometry. Initial films on GaN were characterized by using a wide variety of techniques to determine the crystal structure, surface roughness, chemical composition, and film thickness. Electrical diodes were then fabricated for electrical testing such as current-voltage and capacitance-voltage measurements.

Continuous and digital growth techniques for (Sc2O3)x(Ga2O3)1-x revealed segregation of Ga at the surface. The segregation was eliminated by utilizing a growth technique in which the Ga shutter was closed for a set amount of time towards the end of the growth while the O and Sc
shutters remained open. A poor breakdown field of 0.15 MV/cm was obtained due to the presence of free Ga metal in the film.

Growth of Mg$_x$Sc$_y$O$_z$ at low oxygen pressures showed breakdown fields as high as 4 MV/cm and $D_{it}$ values in the low $10^{11}$ ev$^{-1}$cm$^{-2}$ range, but flatband voltage shift values ranging from 3.83-5.30 V were also obtained. The large flatband voltage shifts were attributed to defects generated from the mixed Sc (+3) and Mg (+2) valences.

Optimization of MgO growth parameters at low oxygen pressures and low growth rates showed improved environmental stability and good electrical results on both u-GaN and p-GaN. The use of a new processing scheme in which the ohmic metal is deposited prior to MgO showed good feasibility as it displayed comparable electrical results to the old scheme involving MgO deposition prior to ohmic metallization.
CHAPTER 1
INTRODUCTION

Motivation

The modern microelectronics industry is primarily based on silicon technology. As the demands for increased device speed rise, the semiconductor industry continues to decrease the size of transistors on integrated circuits (ICs) and increase the number of transistors per chip to meet Moore’s law (number of transistors on ICs doubles every 18 months). Although great success has been achieved with silicon based devices, silicon does have a couple limitations.

Due to the low band gap (1.1 eV) of silicon, it cannot be used in devices operating under high temperature and/or high power regimes. It is also an indirect band gap semiconductor, which makes it an inefficient light emitter. Because of these limitations with silicon, much research has been devoted to compound semiconductors to find materials that have direct band gaps for efficient light emission and wide band gaps for high power, high temperature applications. Gallium nitride is a compound semiconductor that has both of these characteristics. The wide band gap (3.4 eV) of GaN allows it to be used in high power RF devices such as military radar and broadband communication links. Its direct band gap allows it to be used in photonic devices such as light emitting diodes (LEDs), laser diodes, and UV detectors. It also has a low sensitivity to ionizing radiation, which makes it suitable for satellite based communication networks.

With all of the potential that GaN has, there is a need for a dielectric in certain GaN-based devices. AlGaN/GaN high electron mobility transistors (HEMTs) typically experience current collapse and rf dispersion (discussed in Chapter 2), which is a decrease in the maximum current and an increase in the knee voltage due to surface and bulk traps. The application of a dielectric serves to passivate the surface traps, allowing a significant increase in the max current under rf
conditions in which the gate bias is pulsed. A second desire for using a dielectric is to reduce leakage current from one device to another by isolating devices and interconnects (Mesa isolation). The dielectric can also be employed underneath the gate to reduce gate leakage into the semiconductor. This allows the fabrication of a metal oxide (or insulator) semiconductor field effect transistor (MOSFET) which can be made into a complementary device that is required for logic circuits.

**Dissertation Outline**

The objective of the study was to grow a novel gate dielectric with a high breakdown voltage so that it could be employed in a stacked gate dielectric in an enhancement mode MOSFET. The study also included optimization of some previously used crystalline dielectrics to enhance the stability and electrical characteristics of the films.

The background and literature review is discussed in Chapter 2. It contains general information on MOSFETs, characteristics of a good dielectric, properties of previously used dielectrics, and a brief overview of rf dispersion and the current collapse effect. A thorough literature review is provided on previously used dielectrics on GaN and various cleaning techniques that have been used on GaN. Chapter 3 discusses the experimental parameters that were used in growing the oxides as well as characterization methods that were used to analyze the deposited thin films. All the major processing steps for the fabrication of MOS capacitors were also provided. Growth and characterization details of \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) are discussed in Chapter 4. Information on different growth techniques and structural and chemical characterization are given. Chapter 4 also includes current-voltage (I-V) results for \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) and the use of various growth conditions to find the optimal conditions that give the best electrical results. Growth optimization of MgO and addition of Sc to MgO to form \(\text{Mg}_x\text{Sc}_y\text{O}_z\) are discussed in Chapter 5. The study includes electrical characterization of new
growth conditions for MgO, and the feasibility of adding Sc to MgO to form a more stable oxide film. A metallization study on u-GaN and electrical results for MgO on p-GaN are provided in Chapter 6. The metallization study includes electrical results for various surface treatments on samples with ohmic pads deposited on GaN prior to oxide deposition. Chapter 7 includes final conclusions and recommendations for future experiments.
CHAPTER 2
BACKGROUND AND LITERATURE REVIEW

Introduction to MOSFET Device

The basic circuit functions performed by the metal oxide semiconductor field effect transistor (MOSFET) are current amplification and controlled switching of the device off and on. Its utilization of an insulating layer (i.e. oxide) between the metal gate electrode and semiconductor layer provides isolation of devices and interconnects, insulation of the gate to reduce gate leakage, and passivation of surface states that induce rf dispersion. The MOSFET device is tolerant of high temperatures and provides better linearity (broader transconductance vs. gate voltage) compared to a metal semiconductor field effect transistor (MESFET).

The MOSFET is a three terminal device which uses a metal gate to control a conducting channel that electrons or holes (depending on the type of conducting channel) flow through from a metal source to a metal drain. The two types of MOSFET devices are depletion mode (“normally on”) and enhancement mode (“normally off”). In the depletion mode MOSFET (Figure 2-1), the semiconductor material beneath the oxide is doped with the same type of material as the source and drain regions. A conducting channel is already present at a gate voltage of zero, so a gate voltage must be applied to turn the device off. The depletion mode MOSFET is most commonly used as a resistor. In the enhancement mode (e-mode) MOSFET (Figure 2-2), the semiconductor material beneath the oxide is lightly doped to create a region of opposite type to the material under the source and drain regions. A conducting channel is not present at a gate voltage of zero, so a gate voltage must be applied to create a conducting channel and turn the device on. The e-mode MOSFET is most commonly used as a switch. An e-mode n-channel device will be used for further description regarding the basic operation of a MOSFET.
Basic Operation of e-mode n-channel MOSFET

An e-mode n-channel device has n+ source and drain regions that have been implanted or diffused into a lightly doped p-type substrate. At a gate voltage of zero, there is no conducting n-channel between the n+ regions, so no current can flow from the drain to the source. This can be understood with the band diagram of the MOSFET (at equilibrium) in Figure 2-3a. At equilibrium, the Fermi level is flat and a potential barrier is present that prevents the flow of electrons from the source to the drain. As a positive bias is applied to the gate, the valence band moves away from the Fermi level and a depletion region begins to form as holes underneath the gate oxide are repelled. A corresponding negative charge (ionized acceptors) is induced in the p-type channel, and the barrier for electrons between the source, channel, and drain is reduced. Further reduction of the barrier will lead to the formation of a channel in which electrons flow from the source to the drain. The minimum gate voltage required to induce this channel is known as the threshold voltage \( V_T \). Increasing the gate voltage beyond the threshold voltage will induce more negative charges in the channel (making it more conducting) as minority carrier electrons generated in the bulk will drift across the depletion layer to the surface layer (inversion layer) of charge.

Applying a drain bias initially increases the drain current linearly (Figure 2-3b). However, as more drain current flows in the channel, more ohmic voltage drop occurs along the channel, and eventually a drain bias is reached that causes the conducting channel to pinch-off and the drain current to saturate. Pinch-off will occur when the difference between the gate voltage and drain bias is equal to the threshold voltage (Figure 2-4). Increasing the drain bias further will move the pinch-off point farther into the channel and closer to the source end.

For GaN MOSFETs, the formation of a conducting channel is completely dependent upon an external source of inversion charge since the minority carrier generation rate is very low for
GaN (the generation rate is too low at even higher temperatures of 300°C). The source of this charge consists of n+ regions in the source and drain created by Si implantation and subsequent activation annealing. The application of a gate bias is then used to draw electrons from the source and drain under the gate region to form a conducting channel.

**Ideal and Real MOS Capacitors**

The ideal MOS capacitor (Figure 2-5) has a flatband condition where the energy difference between the metal work function ($\Phi_m$) and semiconductor work function ($\Phi_s$) is zero at an applied bias of zero. Under an applied bias, three distinct operation modes exist which are known as accumulation, depletion, and inversion (Figure 2-6). In accumulation, majority carriers accumulate at the surface of the semiconductor, forming a larger carrier concentration than the doping concentration in the bulk of the semiconductor. For a p-type semiconductor, the valence and conduction bands will bend up, and for an n-type semiconductor, the bands will bend down. In both cases, the intrinsic Fermi level ($E_i$) is farther away from the Fermi level ($E_F$) of the semiconductor. In depletion, majority carriers are depleted near the semiconductor surface. The bands will bend down in p-type material and will bend up in n-type material, with the bands bending far enough for $E_i$ to equal $E_F$ at the surface. Under inversion, the bands bend down strongly enough in the p-type material so that $E_i$ lies below $E_F$ at the surface, and the bands bend up strongly enough in the n-type material so that $E_i$ lies above $E_F$ at the surface. Majority carriers at the surface of the semiconductor have been further depleted and minority carriers are collected at the surface.

For a real MOS capacitor, a work function difference typically exists between the metal gate and semiconductor, along with various charges in the oxide and at the oxide/semiconductor interface. The combination of these real effects induces a charge (positive or negative depending
on the various oxide charges and metal-semiconductor work function difference) at the surface of the semiconductor and causes band bending to occur at equilibrium ($V_g = 0$). To eliminate the band bending and achieve a flat band condition, a flatband voltage ($V_{FB}$) in Equation 2-1 must be applied to account for these real effects:

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_i}$$  \hspace{1cm} (2-1)

where $V_{FB}$ is the flatband voltage (measured in volts), $\Phi_{ms}$ is the work function difference (measured in volts) between the work function of the metal ($\Phi_m$) and the work function of the semiconductor ($\Phi_s$), $Q_i$ includes the various oxide and interface charges (measured in C/cm$^2$), and $C_i$ is the capacitance of the insulator (measured in F/cm$^2$).

**Properties and Characteristics of Dielectric Materials**

For a material to be an effective dielectric, it needs to possess the following characteristics: chemical and thermal stability, a dielectric constant higher than the semiconductor, a wide band gap with confinement at both edges, and a lattice constant and thermal expansion coefficient close to that of the underlying substrate. Large differences in the lattice constants can create defects such as misfit dislocations in the underlying substrate that can serve as trapping centers. If the growth occurs at high temperatures, large differences in the thermal expansion coefficients can produce stress at the interface during cooling that will relieve itself through the formation and propagation of dislocations. High operating temperatures with wide band gap semiconductor devices makes thermal stability an absolute necessity for the dielectric. In addition to needing a larger band gap than the semiconductor, large valence band and conduction band offsets with respect to the semiconductor are highly desirable. A higher dielectric constant than the semiconductor is needed to prevent the formation of a high electric field in the dielectric that can lead to potential breakdown of the dielectric. Characteristic values of previously used
dielectric materials on GaN are shown in Table 2.14-6 and band offsets with respect to GaN are shown in Figure 2-7.

Effectiveness of the dielectric can also be determined through analysis of the charges at the dielectric/semiconductor interface and in the dielectric itself. Positive or negative charges trapped at the dielectric/semiconductor interface are known as interface trapped charge (or interface state density). The trapped charge is due to structural defects (i.e. dislocations), dangling bonds, and impurities. The interface state density \( (D_{it}) \) should have a value less than or equal to \( 10^{11} \text{ eV}^{-1}\text{cm}^{-2} \) for a device to be successful. Charges trapped in the first 2-3 monolayers of the dielectric due primarily to structural defects are known as fixed dielectric charge \( (Q_f) \). Positive or negative charges in the bulk of the dielectric due to trapped holes or electrons are dielectric trapped charge \( (Q_{ot}) \). These charges can be injected into the dielectric from the gate or semiconductor under large gate biases. Mobile dielectric charge \( (Q_m) \) is attributed to ionic impurities that can drift under an applied electric field. It is critical to minimize the amount of charge in the insulator as trapped or mobile charges can cause shorting and effect the depletion of a semiconductor.

The integrity of the oxide can be determined from current-voltage measurements by calculating the breakdown field of the oxide. The breakdown field (in MV/cm) provides a measure of how much gate voltage can be applied before the oxide breaks down and charges flow freely from the gate to the semiconductor. It is extremely important to limit the number of defects (such as dislocations and pinholes) and charges in the dielectric as they can serve as electrical pathways that can lead to premature breakdown.

**Current Collapse and RF Dispersion**

Two phenomena that are known for limiting the electrical output (i.e. output power, drain current, etc.) of MESFET and HEMT devices includes RF dispersion and current collapse.
Under RF dispersion, the output power and drain current at high frequencies are significantly lower than projected due to trapping states at the surface. In contrast, current collapse is a reduction in the drain current and distortion in the dc I-V characteristics that occurs under a large drain-source voltage due to traps in the bulk of the material.

Surface trapping has typically been identified through gate lag measurements where the drain current is measured while the gate is pulsed from pinch-off to a value where turn-on occurs. The surface traps are typically associated with dangling bonds, ions adsorbed from the atmosphere, and dislocation defects. Under a large negative gate bias, electrons are injected from the gate into surface states between the gate and drain electrodes, which creates a virtual gate. The virtual gate depletes electrons from the conducting channel of a MESFET and the 2DEG of a HEMT, causing a reduction in the output current. Applying a positive bias to the gate will not increase the drain current instantaneously because the change in the potential of the virtual gate is slow. To reduce the effect of rf dispersion, a dielectric can be deposited at the surface of the semiconductor to passivate the surface trapping states. Including the dielectric underneath the gate metal to make a MOSFET or MOSHEMT device allows the dielectric to simultaneously passivate surface traps and reduce gate leakage.

Buffer trapping has typically been identified through drain lag measurements where the drain current is measured while the drain-source voltage is pulsed. Another indicator of buffer trapping is when a shift in the threshold voltage is observed between dc and pulsed I-V measurements. Traps in the buffer layer are typically associated with dislocation defects and vacancies. Under a large drain-source bias, a high electric field builds up and accelerates electrons through the conducting channel of a MESFET or MOSFET and the 2DEG channel of a HEMT. At a high enough electric field, electrons have sufficient kinetic energy to overcome
local potential barriers and are injected (hot electron stress) into deep trapping centers in the GaN buffer layer or AlGaN layer (for a HEMT device).\textsuperscript{7,14,15} The trapped electrons then lead to current collapse by extending the depletion region and reducing the sheet charge in a HEMT or the density of carriers in the MESFET or MOSFET conducting channel. The effect of current collapse is an increase in the knee voltage and a decrease in the max drain current.

The primary way to significantly reduce or eliminate current collapse is to optimize the growth conditions of the GaN buffer layer and AlGaN layer (in a HEMT device) so that both layers are of high crystal quality with very few dislocation defects and vacancies. Illumination with light and elevated temperatures have also shown success in reducing the current collapse effect.\textsuperscript{7,16,17} Temperatures as high as 155°C in GaN MESFETs completely eliminated the current collapse effect as electrons were thermally emitted from deep level traps. Drain characteristics measured at a gate bias of 0 V under a xenon lamp showed an increase in the drain current as the wavelength of light decreased. The increase in drain current with decreasing wavelength (720 to 360 nm) indicated a wide distribution of trap levels instead of a single trap with a defined energy level. Further analysis of the deep level traps in a GaN MESFET by photoionization spectroscopy indicated that the traps were located at 1.8 and 2.85 eV below the conduction band.\textsuperscript{17}

**Crystalline Dielectrics on GaN**

The following sections provide a summary on the most important crystalline dielectrics that have been developed for use as gate oxides on GaN. The general trend shows that a lower $D_{it}$ value is obtained as the lattice mismatch is reduced between the crystalline dielectric and GaN substrate. Oxide films grown at lower (i.e. 100°C) substrate temperatures have typically shown a greater breakdown voltage compared to films grown at higher substrate temperatures.
(i.e. 300°C or greater). All of the crystalline dielectrics discussed below were deposited by gas source molecular beam epitaxy (GSMBE).

**Gadolinium Oxide**

Gadolinium oxide (Gd$_2$O$_3$) films have been deposited by MBE as a gate dielectric in GaN MOSFETs. An elemental Gd source and ECR oxygen plasma source were used to deposit 70 nm thick films. Changes in the substrate temperature did not significantly change the deposition rate and O/Gd ratio. A $D_{it}$ value of $3 \times 10^{11}$ cm$^{-2}$eV$^{-1}$ (obtained from Terman method) and a breakdown field of ~3 MV/cm were measured for a quasi-amorphous film grown at 100°C. However, the film showed poor thermal stability as it re-crystallized and produced a second phase after being annealed to 1000°C in N$_2$ for 30 seconds.

A single crystal film deposited at 650°C showed good thermal stability upon annealing to 1000°C in N$_2$ for 30 seconds. The surface roughness of the annealed sample was 0.60 nm compared to a value of 0.56 nm for the as-grown sample. AES depth profiling also showed an abrupt oxide/nitride interface for the as-grown and annealed samples. A breakdown field of 0.3 MV/cm was measured for the fabricated GaN device structure. TEM showed a high concentration of dislocations in the film that served as leakage paths and were responsible for the low breakdown field. The highly defective single crystal layer was a result of nanometer size voids in the GaN surface and the 20% lattice mismatch between Gd$_2$O$_3$ (111) and GaN (0001).

To reduce the gate leakage and improve the breakdown field of the device, amorphous SiO$_2$ was deposited on top of Gd$_2$O$_3$. The stacked gate dielectric of SiO$_2$ (30 nm)/Gd$_2$O$_3$ (70 nm) maintained the interfacial properties of Gd$_2$O$_3$/GaN while using the SiO$_2$ layer to reduce current leakage by terminating the dislocations in the oxide layer. The breakdown field of the
device improved from 0.3 to 0.8 MV/cm, and modulation was demonstrated up to a gate bias of 7 V. The reverse leakage current was measured at ~10 pA for a gate-source bias (VGS) of –10 V, and it remained below 10 nA past VGS = -70 V. The main limitation of Gd2O3 is its large lattice mismatch with GaN. The larger band gaps and smaller lattice mismatch to GaN make MgO and Sc2O3 dielectric films more desirable to use than Gd2O3 films.

Scandium Oxide

Scandium oxide (Sc2O3) deposited by MBE is another dielectric that has recently been used in GaN MOSFETs24-28 and AlGaN/GaN HEMT4,28-39 devices. An elemental Sc source and RF oxygen plasma source have been used to deposit the films at substrate temperatures ranging from 100-600°C.28 Changes in the substrate temperature, Sc cell temperature, or oxygen pressure have shown no change in the Sc:O ratio. Breakdown fields as high as 3.3 MV/cm (80-100 nm oxide film) and Dit values as low as 5x10¹¹ eV⁻¹cm⁻² (calculated by Terman method) have been measured for GaN MOS capacitors.25,28 A significant flatband voltage shift has also been observed, indicating the presence of fixed oxide charge. N⁺ drain regions were used in a separate Sc2O3/p-GaN device to overcome the low minority carrier generation rate in GaN and provide a source of inversion charge.26

An AlGaN/GaN MOSHEMT was compared to a metal-gate HEMT to observe the effect of Sc2O3 as a gate dielectric. The drain current reached a maximum value over 0.8 A/mm for the MOSHEMT and was ~40% higher compared to the conventional HEMT.36 The device was also modulated to a gate voltage of 6 V, and the threshold voltage shifted to more negative values (from ~4 V to -5.5 V). Pulsed conditions showed a 10% decrease in IDS relative to DC conditions indicating that the Sc2O3 dielectric (10 nm) effectively minimized the current collapse seen in unpassivated devices. Other Sc2O3 MOSHEMT devices have shown significantly better
power-added efficiency (27%) relative to a conventional HEMT (5%). Scandium oxide passivated HEMTs have also shown effective suppression of surface states created by high energy proton irradiation (40 MeV protons at a fluence equivalent to ~10 years in low-earth orbit), making them attractive candidates for space and terrestrial applications experiencing high fluxes of ionizing radiation.

Surface cleaning has played a vital role in obtaining improved electrical characteristics with Sc$_2$O$_3$ passivation. A 25 min UV/O$_3$ treatment, followed by heating at 300°C for 5 min, and then deposition of Sc$_2$O$_3$ (10 nm) at 100°C, provided a greater increase in $f_{\text{max}}$, $f_T$, $I_{DS}$, and $g_m$ compared to depositing Sc$_2$O$_3$ at 100°C without any surface pre-treatment. The only poor result from the pre-treatment was a slight increase in the reverse leakage current, which was attributed partially to thermal degradation of the gate contact. A cleaning temperature of 700°C would be ideal prior to oxide deposition for cleaning the surface more thoroughly, but any pre-cleaning temperatures above 350°C deteriorates the gate metal of the HEMT.

A major advantage with Sc$_2$O$_3$ compared to MgO is that it provides stable passivation over long periods of time. DC characteristics showed no change in GaN-cap HEMT performance over a period greater than 5 months for devices passivated with Sc$_2$O$_3$ while MgO passivated devices lost some of their effectiveness after 5 months. Comparison to a device passivated with PECVD SiN$_x$ showed that Sc$_2$O$_3$ was more effective in restoring the drain current. Scandium oxide produced complete recovery of the drain-source current, and SiN$_x$ provided only ~70-75% recovery. AlGaN/GaN HEMTs (0.5 x 100 μm$^2$) passivated with Sc$_2$O$_3$ led to a 3 dB increase in output power at 4 GHz compared to a 1.8 dB increase for PECVD SiN$_x$. The main limitation with Sc$_2$O$_3$ is its 9% lattice mismatch with GaN. As stated previously, a larger lattice mismatch produces a greater number of defects which can lead to a higher interface trap density.
Magnesium Oxide

Magnesium oxide (MgO) deposited by MBE has also been employed as a gate dielectric in GaN MOSFETs\textsuperscript{28,40-48} and AlGaN/GaN HEMT\textsuperscript{4,28,33-39} devices. An elemental Mg source and RF oxygen plasma source have been used to deposit the films at substrate temperatures of 100°C.\textsuperscript{28} Cross-section TEM images show that the first 4 nm of the deposited film was single crystal, and then it became polycrystalline as the film rotated. Changes in oxygen pressure have shown a significant impact on the growth rate, Mg/O ratio, morphology, and electrical characteristics of the MgO/GaN diodes.\textsuperscript{40} A $D_{it}$ value of 3.4x10\textsuperscript{11} eV\textsuperscript{-1} cm\textsuperscript{2} (Terman method) and a breakdown field of 4.4 MV/cm (90 nm oxide film) were obtained at an oxygen pressure of 1x10\textsuperscript{-5} Torr compared to values of 1.8x10\textsuperscript{12} eV\textsuperscript{-1} cm\textsuperscript{2} and 1.2 MV/cm at a pressure of 7x10\textsuperscript{-5} Torr. The fixed oxide charge was also shown to decrease with decreasing pressure. The low minority carrier generation rate in GaN has made inversion at room temperature difficult in GaN MOS devices. However, inversion was demonstrated in an MgO/p-GaN MOS diode at room temperature in the dark when n$^+$ regions were implanted in the device.\textsuperscript{41} The n$^+$ regions served as the source of the minority carriers needed for inversion at room temperature. Other MgO films were grown at 350°C, but those films were extremely rough (rms of 4.07 nm compared to 1.26 nm for MgO films at 100°C), had a low breakdown voltage, and were too leaky to obtain C-V results from.\textsuperscript{42}

An AlGaN/GaN MOSHEMT was compared to a metal-gate HEMT to observe the effect of MgO as a gate dielectric. The drain-source current for the MOSHEMT was ~20% higher compared to the conventional HEMT.\textsuperscript{29} The pulsed drain current matched the DC drain current indicating that the MgO dielectric (10 nm) effectively eliminated the current collapse seen in unpassivated devices. Magnesium oxide passivated HEMTs have also shown effective suppression of surface states created by high energy proton irradiation (40 MeV protons at a
fluence equivalent to ~10 years in low-earth orbit), making them attractive candidates for space and terrestrial applications experiencing high fluxes of ionizing radiation.37

A comparison between MgO and SiNx passivation films on GaN-capped HEMTs revealed that the MgO film was more effective in mitigating current collapse. The SiNx film produced ~70-75% recovery of the drain-source current while the MgO film produced complete recovery of the current.4 Passivated AlGaN/GaN HEMTs (0.5x100 μm²) with MgO led to a 3 dB increase in output power at 4 GHz compared to a 1.8 dB increase for PECVD SiNx.35

The role of cleaning prior to deposition of MgO passivation on AlGaN/GaN HEMTs has taken on great significance in optimizing the performance of the device.33,34 Deposition of MgO without prior in-situ or ex-situ treatment showed an increase in $I_{DS}$, $g_m$, $f_T$, and $f_{MAX}$, and a reduction in reverse leakage current compared to devices with no passivation or pre-treatment.33 A 25 min UV-O3 treatment, followed by heating at 300°C for 5 min, and then cooling to 100°C for deposition of MgO produced better dc and rf results than the deposited MgO films that did not receive any pre-treatment. Similarly to Sc2O3, the surface treatment and passivation did produce an increase in the gate leakage current.

A major limitation of MgO is its poor environmental stability.43 It has been shown to deteriorate over time when left uncapped due to the reaction with water vapor in the ambient forming MgOH.35 To preserve the stability of MgO, a capping layer, such as Sc2O3 (5-10 nm), can be deposited on top of the MgO immediately following the MgO growth.34 Films grown at lower growth rates (~1 nm/min) have also shown more stability as they have shown no deterioration after being exposed to air over a period of months. The lower growth rate films have not appeared to etch in water in contrast to higher growth rate films which generally etch in water within 10 seconds.
An additional limitation of MgO is its poor thermal stability.\textsuperscript{43} Annealed (1000°C for 2 minutes) MgO/GaN diodes have shown significant roughening at the MgO/GaN interface, degradation of the oxide, and an order of magnitude increase in the \( D_{it} \). This presents severe processing issues as ohmic contacts typically require high annealing temperatures (i.e., 750°C for 30 seconds with n-GaN). It appears that changes in the processing sequence or the use of a \( \text{Sc}_2\text{O}_3 \) capping layer would be needed to prevent these deleterious effects.

**Magnesium Calcium Oxide**

The desire to decrease the lattice mismatch with GaN and improve the passivation effect of the dielectric has led to the development of MgCaO.\textsuperscript{49-51} The films have been deposited by MBE using Mg and Ca elemental sources and an RF oxygen plasma source. Both CaO and MgO have the same rocksalt crystal structure with similar dielectric constants and bandgap energies. However, the (111) plane of MgO has a -6.5% lattice mismatch to the GaN (0001) plane, and the (111) plane of CaO has a 6.8% lattice mismatch to the GaN (0001) plane. Since Vegard’s law can be applied to systems with components that have the same crystal structure, a 50-50 mixture of MgO and CaO should produce a lattice matched oxide to GaN. This is highly desirable as previous results have shown a decreasing \( D_{it} \) value and greater passivation effect for crystalline oxides with decreasing lattice mismatch to GaN. Initial growths at substrate temperatures of 100°C and 300°C with all three (Mg, Ca, and O) shutters open simultaneously showed Ca and O segregation at the surface.\textsuperscript{49} To prevent this segregation from occurring, a digital growth at 300°C was employed which involved repeatedly altering the Mg and Ca shutter sequences at 10 sec intervals during continuous exposure from the oxygen plasma. An Auger depth profile showed a film of uniform composition, and XRD results showed no evidence of phase separation into either binary phase. A shoulder on the right of the GaN (004) peak was observed in the
XRD spectra, indicating the MgCaO (222) plane. The convenient aspect of the digital growth is that it allows the utilization of various shutter sequences so that the lattice constant of MgCaO can be finely tuned to that of GaN. This concept has been seen in passivation studies incorporating MgCaO as the dielectric.

Two MgCaO films with different compositions (Mg$_{0.5}$Ca$_{0.5}$O and Mg$_{0.25}$Ca$_{0.75}$O) were compared to a MgO film regarding their effectiveness in passivating an AlGaN/GaN HEMT. Both of the MgCaO samples showed increases in the drain saturation current with a 4.5% increase for Mg$_{0.5}$Ca$_{0.5}$O and a 1% increase for Mg$_{0.25}$Ca$_{0.75}$O. The MgO sample showed a 10% decrease in the drain saturation current which was attributed to strain applied on the nitride HEMT by the oxide. Successful use of MgCaO as a passivation layer has also been confirmed with Hall measurements. An increase in sheet carrier density of 15% was seen for unprocessed HEMT material that was passivated with MgCaO and used as a Hall effect sample. Thermal testing was then applied to the samples to measure their stability by annealing them at 100°C in a box furnace open to room ambient. No appreciable decrease in the sheet carrier density was observed over the 25 day anneal.

The main limitations of MgCaO are its poor environmental and thermal stability. Although uncapped MgCaO has shown less severe degradation after annealing than MgO, it still requires a capping layer of Sc$_2$O$_3$ (5 nm). The use of the capping layer provided dramatic improvement in the thermal stability of the oxide as XRR results revealed little change in the interface roughness of the MgCaO/GaN interface after a 1000°C anneal for 2 min. In comparison to MgO films, MgCaO films have also been etched in water within 10 seconds. Films with lower growth rates that are richer in Mg have provided better stability than Ca rich or perfectly matched films, but further investigation must be done to grow a more stable film.
Gallium Gadolinium Oxide

Good electrical results with (Ga_2O_3)_x(Gd_2O_3)_{1-x} deposited on GaAs\textsuperscript{54-58} led to the study of (Ga_2O_3)_x(Gd_2O_3)_{1-x}/GaN MOSFETs\textsuperscript{59} and MOS capacitor\textsuperscript{60,61} structures. The oxide layer was deposited by electron-beam evaporation from a single crystal Ga_5Gd_3O_{12} garnet source at \sim550^\circ\text{C}. Characterization with TEM revealed that 2-3 monolayers of Gd_2O_3 initially formed with the remaining oxide film containing a fine-grained polycrystalline mixture of Ga_2O_3 and Gd_2O_3. A breakdown field of 3 MV/cm was achieved for a MOS diode with an oxide thickness of 19.5 nm and film roughness of 3 nm\textsuperscript{60}. A $D_{it}$ value of less than $10^{11}$ eV\textsuperscript{-1}cm\textsuperscript{-2} was estimated from C-V curves for a MOS diode with an oxide film \sim17 nm thick\textsuperscript{61}. No shifts in the flatband voltage appeared with changes in frequency (ranged from 20 Hz to 1 MHz), and negligible capacitance hysteresis loops were found for C-V measurements with biasing voltages sweeping up and down.

An 8.5 nm thick layer that was annealed at 700\textdegree\text{C} showed leakage currents ranging from $10^{-5}$ to $10^{-9}$ A/cm\textsuperscript{2}. The high leakage current was attributed to a rough GaN surface even though the substrate was heated to 650\textdegree\text{C} prior to deposition to remove surface contaminants\textsuperscript{61}. Although the diode showed a high leakage current, XRR results revealed that the (Ga_2O_3)_x(Gd_2O_3)_{1-x}/GaN interface and the integrity of the oxide remained stable for RTA treatments up to 950\textdegree\text{C}. Thermal stability was also seen in a (Ga_2O_3)_x(Gd_2O_3)_{1-x}/GaN depletion mode MOSFET as the I-V characteristics showed improvement upon heating to 400\textdegree\text{C}\textsuperscript{59}. The improvement was attributed to a reduction in the parasitic resistances in the device. A gate breakdown voltage $>35$ V was achieved for the d-mode MOSFET compared to 16 V for a Pt Schottky gate on the same GaN epilayer. The lower breakdown voltage and significant gate leakage current for the Pt Schottky gate diode demonstrated the need for the (Ga_2O_3)_x(Gd_2O_3)_{1-x}...
gate dielectric. A limitation of \((\text{Ga}_2\text{O}_3)_x(\text{Gd}_2\text{O}_3)_{1-x}\) is the control of the stoichiometry which is heavily dependent on the substrate temperature and usage of the garnet source.\(^{57}\)

**Amorphous Dielectrics on GaN**

The next two sections provide a summary on the amorphous dielectrics of SiO\(_2\) and Si\(_x\) on GaN and AlGaN/GaN HEMTs. The majority of research on these two dielectrics has been on Si. Their ease of processing and good chemical stability has led to the attractiveness of utilizing them in GaN-based devices.

**Silicon Nitride**

Plasma enhanced chemical vapor deposition (PECVD) has commonly been used to deposit Si\(_3\)N\(_4\) at 300° C.\(^{62-70}\) A \(D_{it}\) value of \(6.5 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}\) (calculated by the Terman method) and a breakdown field of 1.5 MV/cm were reported for a Si\(_3\)N\(_4\) (100 nm)/n-GaN insulator-semiconductor.\(^{63}\) Electrical measurements also revealed a flatband voltage shift of 3.07 V. Analysis of the insulating layer by XPS revealed that it was slightly silicon rich. A lower \(D_{it}\) value of \(5 \times 10^{10} \text{eV}^{-1} \text{cm}^{-2}\) (calculated by the Terman method) was obtained for a Si\(_3\)N\(_4\)/GaN structure that had an NH\(_4\)OH treatment (15 min) followed by an N\(_2\) plasma treatment (1 min) before deposition of the insulating layer.\(^{64}\) The lower \(D_{it}\) value shows the importance of a clean substrate surface prior to deposition. A similar structure with SiO\(_2\) as the gate dielectric received the same pretreatment as the Si\(_3\)N\(_4\)/GaN structure and it had a higher \(D_{it}\) value of \(3.0 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}\).

Passivating AlGaN/GaN HEMTs with Si\(_3\)N\(_4\) has proven more effective than using SiO\(_2\). This was attributed to the high density of SiO\(_2\)/GaN interface states which is reported to be 10 times higher than that for Si\(_3\)N\(_4\).\(^{65}\) The effectiveness of passivation with SiO\(_2\) and Si\(_3\)N\(_4\) was tested by comparing 10 nm layers deposited by PECVD on AlGaN/GaN HEMTs.\(^{67}\) The SiO\(_2\) MOSHFET showed a greater reduction in dc current with an increase in the input rf drive, and
the Si$_3$N$_4$ MISHFET had an output power that exceeded the SiO$_2$ MOSFET by 3 dB for a large input rf drive. Both results revealed the greater degree of current collapse in the SiO$_2$ MOSFET. Bernat et. al. also showed that Si$_3$N$_4$ has a greater impact on DC performance than SiO$_2$ for AlGaN/GaN HEMTs.$^{65}$ Unpassivated devices had an $I_{DS} = 0.45$ A/mm, passivation with SiO$_2$ gave 0.54 A/mm, and passivation with Si$_3$N$_4$ gave 0.68 A/mm. Hall effect measurements showed a greater increase in sheet carrier density after passivation with Si$_3$N$_4$ than with SiO$_2$.

The use of Si$_3$N$_4$ to prevent gate leakage has shown good results. The leakage current for a MISHFET only increased from 90 pA/mm at room temperature to 1000 pA/mm at 300$^\circ$C, remaining 3-4 orders of magnitude lower than an HFET with identical geometry.$^{67}$ The dc saturation current also remained fairly constant from 25 to 250$^\circ$C. A limitation of PECVD Si$_3$N$_4$ is the incorporation of hydrogen which can migrate into the gate metallization or into GaN.$^{36}$ Another limitation is that it has a lower dielectric constant of 7.5 compared to 9.5 for GaN.

**Silicon Dioxide**

Different techniques such as radio-frequency sputtering$^{71}$, e-beam evaporation$^{63}$, and most commonly PECVD$^{63,72-76}$, have been used to deposit SiO$_2$. E-beam evaporated SiO$_2$ (100 nm thick) yielded a $D_{it}$ value of $5.3 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ (calculated by the Terman method) and a breakdown field of 1.8 MV/cm for an n-GaN MOS structure.$^{63}$ Electrical measurements also revealed a flatband voltage shift of 2.85 V. Analysis of XPS data revealed a peak with a binding energy of 100.14 eV (Si$_2$O), indicating that a silicon-rich oxide layer was deposited. A lower $D_{it}$ value of $2.5 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ and a higher breakdown field of 2.5 MV/cm were obtained using PECVD for a 100 nm thick film.$^{63}$ It also had a lower flatband voltage shift of 1.55 V. The XPS data for the PECVD deposited film showed closer agreement to the reported SiO$_2$ composition.
It was suggested that reduction in the interface state density was due to the composition of the SiO₂ layer.

The use of SiO₂ in AlGaN/GaN MOSFETs has produced extremely low gate leakage currents.⁷⁴-⁷⁶ A MOSFET leakage current of 100 pA was measured at room temperature under a gate bias of –20 V for a 10 nm thick film grown by PECVD.⁷⁴ This value was six orders of magnitude smaller than an HFET with similar gate dimensions. Another MOSFET structure (15 nm thick oxide film grown by PECVD) showed a leakage current of 1 µA/mm at 300 °C, which was approximately four orders of magnitude lower than an HFET with similar gate dimensions.⁷⁶ The MOSFET also showed good thermal stability as the gate leakage remained below 60 pA/mm at 200 °C for 36 h under bias (V_ds = 20 V, V_gs = -2 V, I_sd ~ 0.42 A/mm). After being subjected to an extremely high thermal stress at 850°C for 1 min, the drain saturation current only decreased by 20% and the leakage current increased up to 20 µA. Although SiO₂ has shown good results, its biggest limitation is that its dielectric constant (ε = 3.9) is considerably lower than that of GaN (ε = 9.5). This could cause a large electric field to build up in the dielectric and cause it to breakdown.

**GaN Surface Cleaning**

A clean surface prior to oxide deposition is critical as surface defects and impurities can influence the overall quality of the device (i.e., Dₙ) and the crystal quality of the deposited film. Numerous wet chemical treatments and in-situ methods have been used to obtain clean GaN surfaces prior to deposition. Some of the wet chemistry treatments have included the use of NH₄OH⁶⁴,⁶⁶,⁷⁷,⁷⁹, HF⁷⁸-⁸⁰, and HCl⁷⁸-⁸⁰ to reduce the amount of carbon and oxygen contamination on the surface. In-situ methods have included a N₂ plasma treatment⁶⁴,⁶⁶,⁷⁹, a N₂/H₂ plasma treatment⁷⁹, a H plasma treatment⁸⁰, NH₃ flux annealing⁸⁰,⁸³,⁸⁴, Ga flux annealing⁸⁰-⁸³, and
deposition of Ga followed by annealing to evaporate the grown Ga monolayers\textsuperscript{81-83} from the surface. Ultraviolet-ozone (UV-O\textsubscript{3}) cleaning\textsuperscript{33,79,80,85} is an ex-situ method that has been used to reduce surface carbon contamination.

**UV-O\textsubscript{3} Cleaning**

UV-O\textsubscript{3} has been shown to be very effective in removing both organic and inorganic contamination with the exception of inorganic salts.\textsuperscript{85} The cleaning mechanism begins when the contaminant molecules are excited and/or dissociated with the absorption of short wavelength UV light (i.e., 254 nm). Atomic oxygen and ozone simultaneously form when O\textsubscript{2} absorbs UV light with a wavelength below 245 nm (ozone is primarily formed at 185 nm wavelength). Even more atomic oxygen is formed at higher wavelengths (i.e., 254 nm) when ozone is dissociated by the absorption of UV light. The excited contaminant molecules react with the atomic oxygen to form volatile species such as CO\textsubscript{2}, H\textsubscript{2}O, etc.\textsuperscript{85} Figure 2-8 shows the effectiveness of a 5 min UV-O\textsubscript{3} treatment at removing carbon contamination from the GaN surface following photoresist removal with acetone.

**In-situ Cleaning**

In-situ plasma treatments have shown success in removing carbon and oxygen contamination from the GaN surface. Cleaning with a hydrogen plasma showed effective removal of carbon and halogen species at temperatures as low as 400\textdegree C, but it showed only moderate success in removing oxygen.\textsuperscript{80} The use of an in-situ thermal treatment with an H\textsubscript{2}/N\textsubscript{2} plasma or an N\textsubscript{2} plasma at 750\textdegree C for 5 min produced a clean GaN surface within the detection limits of AES.\textsuperscript{79} However, SIMS data revealed the presence of significant amounts of carbon (\textasciitilde3\times10\textsuperscript{20} cm\textsuperscript{-3}) and oxygen (\textasciitilde2\times10\textsuperscript{22} cm\textsuperscript{-3}) on the surface. These results show that all three
plasma treatments were effective at reducing the carbon and oxygen contamination, but further cleaning studies must be examined to obtain completely clean GaN surfaces.

In-situ vacuum annealing has also been used to remove surface contaminants to less than the AES detection limits. However, annealing at 800°C has shown incomplete removal of oxygen and carbon from the surface as primarily C-H bonded carbon remains at temperatures ranging from 600-950°C. X-ray photoelectron spectroscopy data indicated that complete desorption does not occur until 950°C. Annealing the surface up to 950°C is not an effective process as GaN begins to sublimate at ~800°C. Other in-situ vacuum anneals have been performed in NH₃ (excellent scavenger of hydrocarbons), following Ga deposition at room temperature, and following Ga deposition at temperatures around 600°C.

Ex-situ Cleaning

Ex-situ wet treatments have been used to reduce surface contamination and become even more effective when combined with an in-situ cleaning process. Treatment with a HCl:H₂O (1:1) solution reduced the as-received O/N ratio from 0.39 to 0.21 and the as-received C/N ratio from 0.28 to 0.24. Further in-situ annealing at 650°C for 15 minutes reduced both ratios to 0.14. Treatment with an HF:H₂O (1:1) solution reduced the as-received O/N ratio from 0.39 to 0.26 and the as-received C/N ratio from 0.28 to 0.18. Further in-situ annealing at 650°C for 15 minutes reduced the O/N and C/N ratios to 0.17 and 0.13 respectively. Characterization with AES and XPS has shown the abilities of a warm (50–60°C) NH₄OH solution to significantly reduce the amount of oxygen contamination at the surface. An in-situ N₂ plasma treatment (1 min) following a 15 min NH₄OH treatment was shown to reduce the Dₙ to 5x10¹⁰ eV⁻¹ cm⁻² (calculated by the Terman method) for a Si₃N₄/GaN structure. Since each of these ex-situ wet treatments is effective at reducing the level of oxygen contamination at the surface, either of
these treatments could be used following a UV-O_3 treatment to strip the formed native oxide layer.
Table 2-1. Properties of previously used dielectrics.

<table>
<thead>
<tr>
<th>Material</th>
<th>Structure</th>
<th>Lattice constant (Å)</th>
<th>Band gap (eV)</th>
<th>ε</th>
<th>α (K⁻¹)</th>
<th>Tₘₚ (K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>Amorphous</td>
<td>NA</td>
<td>9.0</td>
<td>3.9</td>
<td>0.5x10⁻⁶</td>
<td>1900</td>
</tr>
<tr>
<td>SiNx</td>
<td>Amorphous</td>
<td>NA</td>
<td>5.0</td>
<td>7.5</td>
<td>3.3x10⁻⁶</td>
<td>2173</td>
</tr>
<tr>
<td>(Ga₂O₃)ₓ-(Gd₂O₃)₁₋ₓ</td>
<td>Polycrystalline</td>
<td>*</td>
<td>4.7</td>
<td>14.2</td>
<td>*</td>
<td>2023</td>
</tr>
<tr>
<td>Ga₂O₃</td>
<td>Hexagonal</td>
<td>a = 0.498, c = 1.343</td>
<td>4.4</td>
<td>10.0</td>
<td>*</td>
<td>2013</td>
</tr>
<tr>
<td>Gd₂O₃</td>
<td>Bixbyite</td>
<td>10.8130</td>
<td>5.3</td>
<td>11.4</td>
<td>1.0x10⁻⁵</td>
<td>2668</td>
</tr>
<tr>
<td>Sc₂O₃</td>
<td>Bixbyite</td>
<td>9.8450</td>
<td>6.3</td>
<td>14.0</td>
<td>*</td>
<td>2678</td>
</tr>
<tr>
<td>MgO</td>
<td>Rock salt</td>
<td>4.2112</td>
<td>8.0</td>
<td>9.8</td>
<td>1.3x10⁻⁵</td>
<td>3073</td>
</tr>
</tbody>
</table>

*Value could not be found
Figure 2-1. Cross-section illustration of a depletion mode n-MOSFET. A) Device is in the "ON" state with $V_G = 0$. B) Device is in the "OFF" state with $V_G < 0$. [Reprinted with permission from B.P. Gila, 2000. Growth and Characterization of Dielectric Materials for Wide Bandgap Semiconductors. PhD dissertation (pg. 21, Figure 2-2). University of Florida, Gainesville, Florida.]
Figure 2-2. Cross-section illustration of an enhancement mode n-channel MOSFET.  
A) Device is in the “OFF” state with $V_G = 0$.  
B) Device is in the “ON” state with $V_G > 0$. 

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Figure 2-3. E-mode n-channel MOSFET. A) 3-D view of MOSFET and equilibrium band diagram along channel. B) $I_D$-$V_D$ curve for MOSFET as a function of gate voltage. [Streetman, Ben; Banerjee, Sanjay, Solid State Electronic Devices, 5th Edition, © 2000, pg. 256, Figure 6-10. Reprinted by permission of Pearson Education, Inc., Upper Saddle River, NJ]
Figure 2-4. N-channel MOSFET. A) Formation of conducting channel with $V_G > V_T$. B) Onset of saturation with $V_G - V_D = V_T$. C) Strong saturation with $V_G - V_D < V_T$.

Figure 2-5. Energy band diagram for ideal p-type MOS capacitor at $V_G = 0$. [Streetman, Ben; Banerjee, Sanjay, Solid State Electronic Devices, 5th Edition, © 2000, pg. 261, Figure 6-12. Reprinted by permission of Pearson Education, Inc., Upper Saddle River, NJ]
Figure 2-7. Valence band and conduction band offsets with respect to GaN for previously researched dielectrics. GGG represents \((\text{Ga}_2\text{O}_3)_x(\text{Gd}_2\text{O}_3)_{1-x}\).
Figure 2-8. Auger peak-to-peak ratios for C:Ga, C:O, and Ga:O on GaN with UV-O$_3$ treatments of 1, 3, 5, and 10 minutes.
CHAPTER 3
EXPERIMENTAL APPROACH

Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) was used to deposit the oxide films. It allows films with abrupt interfaces and very smooth surfaces to be deposited in an ultra-high vacuum environment using high purity sources. The high purity sources can be controlled independently from each other by using ovens called Knudsen cells (Figure 3-1). The flux of atoms emitted from the cell is represented by Equation 3-1:

\[ F = \frac{1.18 \times 10^{22} (P)(a)}{d^2 (MT)^{1/2}} \]  

where \( F \) is the flux (in atoms/cm\(^2\)) of the Knudsen cell, \( a \) is the orifice area (in cm\(^2\)) of the cell, \( P \) is the vapor pressure (in torr) inside the cell, \( T \) is the temperature (in degrees Kelvin) of the cell, \( M \) is the atomic mass (in amu) of the element in the cell, and \( d \) is the distance (in cm) from the cell to the substrate. The ability to change the flux of atoms emitted from the cell allows a high degree of control over the stoichiometry of the deposited film. The purity of the atomic beam emitted from the cell is dependent upon the purity of the source and the vacuum level in the chamber.\(^86\)

The high vacuum inside the chamber is one of the attractive qualities of MBE that provides a clean environment and allows highly pure films to be grown. Precise control of the substrate temperature in MBE also allows control of the microstructure of the deposited films. The growth rate is dependent on the flux of the elements to the substrate, the ratio of the elements, and the substrate temperature. Lower substrate temperatures and higher fluxes can be used to produce amorphous or fine-grained polycrystalline films. Higher substrate temperatures and lower fluxes can be used to produce single crystal films.
A Riber 2300 MBE system (Figure 3-2) was used for all of the oxide growths. The growth chamber was pumped down to a range of $1 - 5 \times 10^{-9}$ torr using an Oxford Cryo-Torr 8 cryopump. The MBE system is equipped with a Reflective High Energy Electron Diffraction (RHEED) gun to provide in-situ characterization of the oxide film during growth. It also provides information on the substrate surface prior to growth. The MBE system contains six ports with five of them containing Knudsen cells (3 Riber 125 LK’s with 25 cc crucibles, 1 Varian 0981-4135 with a 40 cc crucible, and 1 EPI 91-734 with a 25 cc crucible) for various sources (Sc, Ga, Mg, Ca, and Sm) and the remaining port containing the oxygen plasma source. The temperature of the Knudsen cells is controlled by a FICS 10 controller that adjusts the power output of an external power supply whose power cables are connected to two posts on the cell.

An MDP21 radio frequency (rf) source from Oxford Applied Research was used as the oxygen source for the growths. It was operated at a frequency of 13.56 MHz with a forward power of 300 W and a reflected power of 2-3 W. Oxygen (99.995%) was supplied to the plasma head using a high purity 8161c Unit (Celerity) $O_2$ mass flow controller (MFC) that had a 3 sccm full scale range. The plasma is generated as soon as a high enough voltage is applied between the two electrodes to create an electric field in the reactor that exceeds the breakdown field of the gas. As soon as the high voltage arc flashes between the two electrodes, a large number of dissociated atoms are created. The dissociated atoms and undissociated molecules then escape into the vacuum environment through an array of fine holes in the aperture plate. The electrical potential remains low enough so that negligible currents of ions and electrons will escape from the discharge tube.

The substrate temperature was measured using a back side thermocouple in close proximity to the substrate holder. The substrate thermocouple was calibrated by using pieces of
gallium antimonide (GaSb) and indium antimonide (InSb), which have melting points of 707°C and 525°C respectively. The pieces of GaSb and InSb were heated in the growth position under a nitrogen plasma to reduce the chance of losing Sb. Loss of the group V species during heating would result in an incorrect melting temperature.

Substrate Preparation

All substrates received an ex-situ and in-situ surface treatment prior to oxide deposition to remove any surface contamination. A clean surface prior to deposition is critical as surface defects and impurities can influence the overall quality of the device (i.e., $D_0$), the metal contact resistance/stability, the crystal quality of the deposited film, and the epitaxial defects. Prior to treating the surfaces, the substrates were inspected under a microscope, and an RMS roughness was determined by AFM as a reference value. The substrates used for oxide deposition included Si and GaN.

Silicon

Phosphorous doped (n-type) Si substrates from Wacker-Chemitronic GMBH were used for the oxide growths involving initial calibrations. The substrates were 50 mm wafers with a (100) orientation. The low cost and wide availability of Si made it more feasible to use when calibrating the thickness, growth rate, composition, or uniformity of the dielectric films.

Each Si sample received an ex-situ treatment in buffered oxide etch (BOE) solution (6:1 NH$_4$F:HF in water) to remove the native oxide layer. After removing the native oxide, the sample was rinsed in deionized water and blown dry with an N$_2$ gun. An rms value of 0.08 nm was measured with AFM following this surface treatment. After receiving an ex-situ treatment, the Si sample was immediately indium mounted to a molybdenum block and then placed under vacuum inside the load lock of the Riber 2300 MBE system. The sample was then cleaned in-
situ by heating it up to 200°C to drive off any moisture that collected on the surface between the
time it was etched in BOE and placed under vacuum.

**Gallium nitride**

Gallium nitride (GaN) wafers were provided by Uniroyal and the Abernathy group (GaN
wafers were grown using a Veeco MOCVD system). The Uniroyal wafers were used for
calibrations on GaN due to their higher surface roughness and pits (Figure 3-3) that were seen on
the surface by AFM. Some of the pits had a depth as great as ~114 nm which is much greater
than the thickness of the oxide films. The GaN wafers provided by the Abernathy group were
used for oxide growths that involved characterization of the crystal structure of the oxide and
fabrication of the oxide to make MOS capacitors for electrical testing. The Abernathy group
GaN wafers (Figure 3-4) had a lower surface roughness (rms as low as 0.134 nm using a 1 μm
scan) compared to the Uniroyal GaN.

Each GaN sample received an ex-situ treatment starting with a 3 min HCl:H₂O (1:1)
solution to degrease the sample and remove as much oxygen and carbon contamination as
possible. After removing the sample from the solution, it was rinsed in deionized water and
blown dry with an N₂ gun. It was then given a 25 min UV-O₃ treatment in a UVOCs UVO
cleaner (model number 42-220) to remove any residual carbon. The sample was finally placed in
a 5 min BOE solution to remove the native oxide formed from the UV-O₃ treatment and then
rinsed in deionized water and dried with an N₂ gun. Successful removal of the native oxide was
observed with RHEED images of the surface. The RHEED pattern of the surface with the native
oxide showed arcs, and the RHEED pattern of the BOE treated surface showed streaks (Figure 3-5).
After receiving an ex-situ treatment, the GaN sample was immediately indium mounted to a molybdenum block and then placed under vacuum inside the load lock of the Riber 2300 MBE system. The sample was then given an in-situ thermal treatment at 700°C for 10 min to remove any oxygen or carbon contamination on the surface that was not removed during the ex-situ treatments. The room temperature RHEED pattern showed a (1x1) surface (Figure 3-5b), and a (1x3) pattern appeared after the in-situ thermal treatment at 700°C (Figure 3-6).

**Scandium Gallium Oxide Growth**

Scandium gallium oxide films were deposited using a 99.9999% pure Sc rod and 99.9999% pure Ga ingot. The Sc Knudsen cell temperatures ranged from 1170°C to 1200°C and the Ga Knudsen cell temperatures ranged from 700°C to 884°C. A substrate temperature of 100°C was used with an oxygen pressure ranging from 8x10^-6 Torr to 1.1x10^-5 Torr with an Oxford RF plasma source at 300 W forward power and 2–3 W reflective power. Sample rotation was kept constant at 15 rpm during the film growth. Numerous growth techniques were employed to grow a continuous film with good electrical properties. These growth techniques are discussed in chapter 4.

**Magnesium Oxide Growth**

Magnesium oxide films were grown using a 99.99% pure Mg rod at Knudsen cell temperatures ranging from 340°C to 360°C. A substrate temperature of 100°C was used, and films were deposited at low growth rates ranging from 0.8–1.4 nm/min since MgO films at lower growth rates showed more stability during processing. The oxygen pressure was kept below 5x10^-6 Torr with an Oxford RF plasma source at 300 W forward power and 2–3 W reflective power. The samples were rotated during the film growth at 15 rpm.
Magnesium Scandium Oxide Growth

Magnesium scandium oxide films were grown with a fixed Mg cell temperature of 340°C and an increasing Sc cell temperature ranging from 1090°C to 1180°C. A substrate temperature of 100°C was used for all growths. The oxygen pressure was kept below 4x10^{-6} Torr with an Oxford RF plasma source at 300 W forward power and 2–3 W reflective power. The samples were rotated during the film growth at 15 rpm. The thickness and growth rate of the deposited films increased with increasing Sc cell temperature.

Start-Up

After the samples received their ex-situ treatment and were placed under vacuum in the load lock, liquid nitrogen was run through the cryo-panels, which served to decrease the thermal interaction of the Knudsen cells and lower the pressure of the growth chamber. The Knudsen cell for each source that was needed was raised at a rate of 100°C every 10 minutes until the desired temperature was reached. The samples were transferred on a trolley to the buffer chamber, and then a sample was loaded into the growth chamber using the manipulator (or transfer) arm. The sample then received an in-situ thermal treatment facing towards the sources. After receiving the thermal treatment, the sample was cooled to the desired substrate temperature facing away from the sources. Once the substrate temperature was reached, the oxygen plasma was lit and the desired oxygen pressure was adjusted with the O₂ MFC. After reaching 90 mV on the photodiode for the plasma, the shutters for the oxygen source and source material were opened. The sample was then moved into the growth position facing towards the sources and rotated at 15 rpm for the duration of the growth.
MOS Capacitor Fabrication

After the oxide films were deposited and the samples removed from the MBE system and molybdenum block, they were processed to make MOS capacitors seen in Figure 3-7. The first processing step involved opening up ohmic windows so that the exposed oxide could be etched away (Figure 3-8). The second step was used to deposit ohmic contacts in the areas of oxide that were etched away (Figure 3-9). However, a thin ring of GaN between the oxide island and ohmic contact was left open so that the oxide could be electrically isolated from the ohmic pad. The final processing step involved depositing metal gates of 50 μm or 100 μm in diameter on top of the oxide island (Figure 3-10). Fabrication of the MOS capacitors allowed IV and CV measurements to be taken which helped to determine the performance of the oxide. The key processing steps involved photolithography, etching, metallization, and annealing. A complete description of the lithography steps and more detailed information regarding lithography are given in Appendix A.

Photolithography

Shipley 1818 was used as the photoresist (PR) in each lithography step. A Laurell WS-400A 6NPP/Lite was used to spin the PR on the samples. Dynamic dispense was used to apply the PR as it was dispensed at 1000 rpm (and acceleration of 1200 rpm/sec) and spun to a final speed of 5000 rpm (and acceleration of 1500 rpm/sec). A spin speed of 5000 rpm corresponded to a thickness range of 2.0–2.2 μm depending on the conditions of the PR and conditions inside the photolithography room. The samples were then given a soft bake on a Thermolyne hot plate at 125°C for 1.5–2 minutes.

A Karl Suss MA6 mask aligner was used to align the sample to the pattern in the mask and then expose the sample with a mercury xenon lamp at a 365 nm wavelength. Hard contact mode
was used which presses the sample firmly against the mask to minimize any diffraction effects. Other parameters included an Al gap of 100 μm, WEC offset of 0, and WEC type as contact. The exposure time was calibrated based on the PR thickness and exposure dose.

After exposure, the samples were developed in either Rohm and Haas MF-319 developer or AZ 300 MIF developer at room temperature. The development time was 30–60 seconds, depending on the exposure time. After developing the samples, they were rinsed in DI water and then blown dry with an N2 gun. A post bake at 110°C for 1 minute was then applied to samples that were etched in the subsequent processing step. A post bake was not used when the next step was metallization.

For cases in which the metal gates were lifting off the oxide, the use of LOR 3B was used in a bi-layer stack with 1818. The LOR 3B was spun onto the sample at the same dispense and final spin speeds as the 1818 resist. However, it was baked at 150°C for 5 minutes, which produced a thickness of ~0.25 μm (needs to be about 1.2–1.3 times the thickness of the deposited metal). It also received the same exposure and development times as the 1818 since the 1818 was coated over the top of it. The high development rate of the LOR 3B provides an undercut profile (Figure 3-11) of the film below the 1818, making it attractive for metal lift-off.

**Etching**

A wet etching chemistry is desirable for oxide films on p-GaN as dry etching of p-GaN has been shown to cause plasma damage, which can lead to an increase in sheet resistance of the p-GaN and conversion to an n-GaN surface at high ion fluxes or ion energies. Etching times were determined based on numerous samples (with the MOS capacitor patterns) etched at different times which were then analyzed with Auger Electron Spectroscopy (AES) to see if the oxide was completely removed from the GaN substrate. The type of etching chemistry depended
upon the type of oxide. It was found that a 2% H₃PO₄ solution at room temperature could etch a
40–60 nm MgO film in 10–12 seconds. A H₂SO₄:H₂O (1:1) solution was used for etching
(Sc₂O₃)ₓ(Ga₂O₃)₁₋ₓ since it previously showed successful removal of Sc₂O₃ films on GaN. It was
determined that a 12 minute etch could remove a ~33 nm thick film (Figure 3-12).

Dry etching is advantageous for processing of smaller features where the undercut
produced from lateral etching during the wet etch must be limited or completely eliminated.
More importantly, dry etching is desirable for stacked gate dielectrics in which the bottom
dielectric has a much greater selectivity over the top dielectric for a given wet etching solution.
The extremely high selectivity of the bottom dielectric could lead to a situation where over
etching the top dielectric causes etching and complete removal of the bottom dielectric from the
substrate. Finding a dry etch chemistry where the top dielectric etches selectively over the
bottom dielectric would prevent over etching and would allow the bottom dielectric to serve as
an etch-stop layer.

Any dry etching was performed in a Unaxis Shuttlelock Reactive Ion etcher (RIE) with
Inductively Coupled Plasma (ICP) module. The system was equipped with a 2 kW inductively
coupled power supply (13.56 MHz RF) and a 600 W RIE power supply (13.56 MHz RF). The
ICP power is used to generate reactive ions and neutrals in the chamber that chemically react
with species at the surface. This chemical component of the dry etching process leads to
isotropic etching that is selective (gases are chosen for different reactions). The RIE power
(substrate bias) is used to accelerate the energetic ions to the substrate with the purpose of
driving the surface chemical reactions rapidly and physically dislodging atoms from the surface
by sputtering. This physical component leads to anisotropic etching with no selectivity. The
process pressure in the chamber can be increased to increase the density of reactive species, but
an increase in the pressure lowers the mean free path which can affect the energy the ions strike the substrate with.

Samples were transferred and etched on a 4” Si wafer carrier with a number of available gases (SF₆, BCl₃, Cl₂, CHF₃, O₂, Ar, H₂, CH₄, N₂) for etching. A thicker PR (Shipley 1045) was used for patterning since it held up better and longer to stronger dry etching conditions compared to thinner resists. Dry etching chemistries varied depending on the type of oxide due to the volatilities of the etch products involved. A CH₄/H₂/Ar mixture was found to etch (Sc₂O₃)x(Ga₂O₃)1-x at rates ranging from 5–32.5 nm/min at a process pressure of 5 mTorr (Figure 3-13). More importantly, the GaN did not show any detectable etching (given the ~2 nm resolution of the stylus profilometer) at the same etching conditions. Due to the higher selectivity of (Sc₂O₃)x(Ga₂O₃)1-x over GaN in the CH₄/H₂/Ar chemistry, this chemistry is suitable for selective removal of (Sc₂O₃)x(Ga₂O₃)1-x from GaN substrates (Figure 3-14).

**Metallization**

A Kurt Lesker CMS-18 multi target sputter deposition tool was used to sputter the ohmic contacts and metal gates. Sputtering involves the ejection of atoms from a solid metal target due to the momentum transfer from bombarding energetic ions (i.e., Ar⁺). A DC voltage is maintained across plane parallel electrodes with the metal target serving as the cathode and the substrate (or sample) serving as the anode. A large supply of energetic ions in the interelectrode region is accelerated to the material target under an applied electric field. Once the energetic ions strike the target, atoms are dislodged from the metal target by momentum transfer. The dislodged metal atoms then deposit on the substrate. The sputter yield depends on the ion flux of the target, the probability that the impact of the energetic ion ejects a target atom, and the transport of the sputtered material across the interelectrode region to the substrate.
Ohmic contacts on n-GaN or u-GaN consisted of a multi-layer structure of Ti (20 nm)/ Al (80 nm)/ Pt (40 nm)/ Au (80 nm). The Ti layer reacts with nitrogen to form TiN which makes the ohmic, the Al layer controls the TiN reaction, the Pt layer is a diffusion barrier to prevent Al and Au from reacting, and the Au layer is used for making contact to probe tips since the layer does not oxidize. Ohmic contacts on p-GaN consisted of a bi-layer structure of Ni (50 nm)/Au (80 nm). Gate contacts on the dielectric included a bi-layer structure of Pt (30 nm)/Au (120 nm). Gate contact sizes of 50 μm or 100 μm were used for the MOS capacitors.

After metal deposition, metal lift-off was performed in a sonicator. Samples were immersed in a beaker of MicroChem Nano Remover PG, which was then transferred into the sonication bath. Samples experiencing difficulty with lift off were heated up to 50–60°C for 30 minutes on a Thermolyne hot plate before using the sonicator again. Once lift-off was complete, samples were rinsed in isopropanol then DI water and finally blown dry with an N₂ gun.

Annealing

Ohmic contacts on the samples were annealed in the MBE system or an AG Associates HeatPulse 610 RTA system. Annealing conditions were strongly dependent on the doping density of the n- and p-GaN material. Oxides on n-GaN or u-GaN were primarily annealed for 45 seconds at 400°C in the growth chamber. Other samples were annealed at 700°C for 30 seconds in the RTA system under an N₂ ambient. Oxides on p-GaN were annealed at 300°C for 1 min in the RTA system under an N₂ ambient. Indium on the backside of the samples was removed (refer to Appendix A regarding the procedure) prior to annealing the samples in the RTA system.
Materials Characterization

Numerous characterization techniques were used to analyze the deposited oxide films. The four primary areas of characterization included surface, structural, chemical, and electrical analysis. Surface analysis is important for future processing of the material as etching and deposition of metal to form contacts is sensitive to the morphology and roughness of the surface. Structural analysis is critical in determining the crystal structure, crystal phases, and types of defects present within the film. These characteristics are crucial to the effectiveness of the dielectric, as a polycrystalline film with numerous defects would provide multiple pathways for gate leakage to occur. Chemical analysis is extremely important in determining the amount and type of species within the film as well as how the species are bonded. Electrical analysis is critical in measuring the performance of the oxide and determining the optimum growth parameters that produce the best electrical results. Most of the following characterization methods can be found in reference 89.

Scanning Electron Microscopy (SEM)

Scanning Electron Microscopy (SEM) is used for analyzing the topography and surface morphology of samples. High magnifications (up to 500,000x for field emission SEM) and good depth of field make SEM attractive for surface analysis. The technique uses an electron beam as its source with beam energies ranging from 0.5 keV to 30 keV. Interaction of the beam with the sample produces backscattered electrons (BSE) and secondary electrons (SE). Elastic scattering is responsible for backscattered electrons in which the trajectory of the beam electron is changed without altering the kinetic energy of the electrons. Backscattered electrons are used for atomic number or compositional contrast. Inelastic scattering is responsible for secondary electrons in which energy is transferred from the beam electrons to atoms of the specimen, resulting in emitted electrons with energies less than 50 eV. Secondary electrons strongly affect the
topographical image. An important limitation of SEM is that samples must be conductive to prevent charging (causes distortions in image) from occurring. Since the deposited oxide films are not conductive, they can be coated with carbon or a lower beam voltage can be used to minimize the charging.

A JEOL 6400 and JEOL JSM-6335F were used to characterize the oxide films. The JEOL 6400 is a thermionic emission SEM that uses a tungsten filament. Thermionic emission occurs when enough heat is applied to the filament so that electrons can overcome the work function of the material and escape from the material itself. Some of the disadvantages of thermionic emission include relatively low brightness, evaporation of the cathode material, and thermal drift during operation. The JEOL JSM-6335F is a field emission SEM that uses a LaB$_6$ filament. Field emission occurs by applying an electric field (that can be concentrated to an extreme level) to reduce the potential barrier that electrons need to overcome. The primary advantage of the field emission SEM is its high spatial resolution (<2 nm which is 3–6 times better than an SEM utilizing thermionic emission). Both instruments were used for analyzing as-grown oxide films and samples that were processed as diodes for electrical testing. They were useful for detecting obvious defects or pinholes that were attributed to shorting in specific MOS capacitors.

**Atomic Force Microscopy (AFM)**

Atomic Force Microscopy (AFM) can also provide information on the topography and morphology as well as the root mean square (RMS) roughness of the surface. An AFM Dimension 3100 in tapping mode was used for measuring the surface roughness of the oxide films and as-received GaN substrates as well as the surface morphology and topography of as-grown oxide samples and processed diodes. In tapping mode, the tip of the stylus (made of Si$_3$N$_4$) is brought into close proximity to the surface so the van der Waals forces between the probe tip and surface atoms of the sample can be measured. These forces depend on the probe
geometry, the nature of the sample, contamination on the sample surface, and distance between
the probe tip and sample surface. The forces lead to deflection of the cantilever which holds the
tip at the end. The deflection is then measured by a laser spot that is reflected off the tip and
collected with a photodiode. The intensity of the reflected light is processed as the height for
that point on the surface. Rastering the tip across the sample surface allows a 3-D map to be
created, which can be used to calculate the RMS roughness.

Sensitivity of the AFM depends greatly on the sensitivity of the deflection and sharpness
of the tip. The tapping mode tips used to characterize the oxide samples and GaN substrates had
a tip radius of 5 nm and deflection sensitivity of ~0.01 nm. Contact mode is an alternate AFM
method that can be used, but the tip radius is ~20 nm, which greatly reduces the resolution.

**Reflective High Energy Electron Diffraction (RHEED)**

Reflective high energy electron diffraction (RHEED) provides information on the growth
mode (2-D or 3-D), surface crystal structure, surface roughness, and surface orientation. The
surface analysis is a result of an electron beam (5–100 kV) at low impact angles (<5°) which
allows electrons to pass through the top few atomic layers of the surface. After reflecting off the
surface, electrons strike a phosphorescent screen and form a diffraction pattern. The generated
diffraction pattern helps to characterize the substrate surface prior to growth, the growth
initiation mode, and the quality of the deposited films during and after growth.

Analysis by RHEED was conducted in-situ in the modified Riber 2300 MBE system
(mentioned previously) at a beam voltage of 6 kV. Single crystal surfaces showed a spotty or
streaky pattern, polycrystalline surfaces showed a ringed pattern, and amorphous surfaces
showed almost no pattern at all (Figure 3-15). A pattern with streaky lines indicated a smooth
surface growing layer-by-layer (2D), and a spotty pattern indicated a rough surface with islanding growth (3D).

**Ellipsometry**

Ellipsometry is used for determining the thickness and optical constants (n and k) of dielectric films. The technique involves the use of plane-polarized light which reflects off a sample at a given angle and is then analyzed for a change in the polarization. Analysis of the change in polarization yields two parameters (the azimuth and phase difference) from which the optical properties are calculated. A Rudolph V-530044 Auto EL IV ellipsometer was used for characterization of the oxide films.

**Transmission Electron Microscopy (TEM)**

Transmission electron microscopy (TEM) is a valuable instrument for providing microstructural analysis of thin films. Its high lateral resolution (~0.15 nm) allows it to provide detailed analysis of the morphology, defects present in the film, the atomic structure, and an accurate calculation of the lattice constant. The high lateral resolution is obtained by using an extremely thin simple which interacts with a focused beam of electrons. The transmitted and forward scattered electrons form an image on the other side of the sample and a diffraction pattern in the back focal plane. The thin samples are prepared by using a focused ion beam (FIB) instrument which uses a beam of Ga\(^+\) ions to sputter atoms from the surface so the sample can be thinned down or a particular area of interest can be precisely milled. A FIB FEI Strata DB (dual beam) 235 was used to prepare the oxide films, and a TEM 2010F operating at 400 keV was used for high-resolution analysis of the oxide/GaN interface and crystal structure of the oxide films.
X-Ray Diffraction (XRD)

X-ray diffraction (XRD) is used for determining the crystal phases and crystal structure present in bulk films. The principle of XRD is governed by Bragg’s law in Equation 3-2:

\[ n\lambda = 2d \sin \theta \]  \hspace{1cm} (3-2)

where \( n \) is the number of whole wavelengths, \( \lambda \) is the wavelength of the incident x-ray (1.5406 Å for Cu Kα), \( d \) is the spacing between planes (Å), and \( \theta \) is the Bragg angle (degrees). Constructive interference of x-rays for certain atomic planes produces characteristic diffraction peaks. The diffraction spectrum produced from the measurement helps to determine if the film is amorphous, polycrystalline, or single crystal. The full width at half max (FWHM) of a diffraction peak can also be used in determining the crystal quality of the film.

A Philips APD 3720 x-ray powder diffractometer was used to characterize the oxide films. Samples were analyzed using a Cu Kα x-ray source, and a 2\( \theta \) range of 20–85° was scanned using 0.02° increments. Crystal phases were identified by standards taken from the JCPDS Powder Diffraction File. All identified peaks were calibrated to the GaN (004) peak position (2\( \theta \) = 73.078°). A Phillips MPD 1880/HR with a 5-crystal analyzer and Cu Kα x-ray source was used for x-ray reflectivity (XRR) measurements. Measurements included film thickness and interfacial roughness at the air/oxide interface and oxide/GaN interface.

X-Ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) was used to look at chemical bonding in the deposited films by measuring the binding energies of atoms in the top few monolayers. It uses x-rays as its source to eject photoelectrons from the sample. Due to the small escape depth (depends on KE of photoelectron and material through which it travels) of the photoelectrons, XPS is limited to surface analysis (top few monolayers). The kinetic energy of the
photoelectrons is measured by a hemispherical analyzer and the binding energy is calculated using Equation 3-3:

\[
BE = h\nu - KE - \phi_{SP}
\]  

(3-3)

where \(h\nu\) is the energy of the incident x-ray (1486.6 eV for Al and 1256.6 eV for Mg), KE is the kinetic energy (in eV) of the photoelectron, \(\phi_{SP}\) is the work function of the spectrometer, and BE is the binding energy (in eV) of the photoelectron. The electron binding energy is highly influenced by its chemical surroundings. The general trend is that binding energy increases with increasing charge on the atom.

The characteristic peaks produced in the spectrum were identified using handbooks containing previously determined standards. The handbooks show the energies of core and valence level electrons and Auger electrons for atoms in their zero-valence state and their different oxidation states when bonded to other chemical species. This information was used to identify the chemical constituents present in the film and whether any of the constituents were bonded to each other.

Both Mg and Al anodes were used depending on the possible interference of Auger lines with XPS lines. The photoelectron binding energy remains the same regardless of which anode is used, but the binding energy of the Auger electron changes (KE of Auger electron does not change with change in anode). This allows Auger lines to be separated from XPS lines in situations where Auger lines overlap XPS lines. In situations where multiple XPS peaks overlap each other, the peaks must be deconvoluted by using RBD Analysis Suite software. Depth profiles were used to analyze any chemical changes at the bulk or oxide/GaN interface. A Perkin-Elmer PHI 5100 ESCA system was used for all XPS characterization.
Auger Electron Spectroscopy (AES)

Chemical composition and film uniformity was determined by Auger Electron Spectroscopy (AES). Auger electron spectroscopy is a three electron process that uses an electron beam as its source. The electron beam ejects a core electron from an atom, creating an atomic inner shell vacancy which will be filled by an electron from a higher energy (outer) shell. As the electron drops from the higher to lower energy shell, it releases energy as an x-ray or by ejecting electron (the “Auger electron”) from one of the outer shells of the atom. Due to the low energy (typically in the range of 50 eV to 3 keV) of Auger electrons, the escape depth is very small (a few monolayers), limiting AES to surface analysis (Figure 3-16).90

As the kinetic energy of the Auger electrons is measured, a plot forms with peaks characteristic of the atoms and energy levels from which the Auger electrons originated. The kinetic energies and footprint of the peaks can be used to identify elements present in the sample by referring to previously determined standards. The atomic composition of the identified elements can be calculated to ± 10 atomic percent. Film uniformity and analysis of the bulk can be conducted with depth profiles. All depth profiles were taken using the 3-point method. A Perkin-Elmer PHI 660 Scanning Auger Multiprobe was used for all AES characterization.

Current-Voltage (I-V) Measurements

A Hewlett Packard Model 4145 was used to make current-voltage measurements. Compliance was set at 100 nA, and the voltage was swept in both negative and positive directions until the forward and reverse breakdowns were reached. Voltages were extracted from the I-V plot at 19.6 nA for diodes with 50 um gates and at 78.5 nA for diodes with 100 um gates. These currents correspond to a current density of 1 mA/cm² (typical breakdown voltages are reported at this current density) for their respective gates. The extracted voltages were then
divided by the dielectric film thickness to determine the forward and reverse breakdown voltages.

Dielectric breakdown is often characterized in three distinct modes. Mode A failures occur at low breakdown voltages and are attributed to defects within the dielectric, defects at the oxide/substrate interface, pinholes in the dielectric, and scratches. Mode B failures occur at intermediate breakdown voltages and are attributed to dielectric thinning. Mode C failures occur at high breakdown voltages and are attributed to the intrinsic nature of the dielectric.

**Capacitance-Voltage (C-V) Measurements**

A Hewlett Packard Model 4284 LCR connected to a Lab View based PC was used to make capacitance-voltage measurements. The LCR meter supplied a voltage signal of superimposed analog current (AC) and direct current (DC). The width of the bias range was chosen depending on the doping density of the substrate. Higher doped substrates required the use of larger bias ranges (ex. a range from 6 V to -6 V was used on an n-GaN substrate with a doping density of 1x10^{17} \text{ cm}^{-3}) to fully deplete the high concentration of majority carriers. Since high positive or negative gate biases can inject carriers into the oxide (this leads to oxide trapped charge) and/or influence the movement of mobile charges within the oxide, low doped substrates were typically used so that low gate biases could be applied in a small bias range (ex. a range from 2 V to 0 V was used on a u-GaN substrate with a doping density of 1x10^{16} \text{ cm}^{-3}).

Devices were cycled at frequencies ranging from 10 kHz to 1 MHz in both series (C_s-R_s) and parallel (C_p-R_p) modes at an oscillation voltage of 50 mV. Both low and high bias sweep rates were also used. All devices were swept from accumulation to depletion by going from positive to negative voltages for devices on n-type substrates and negative to positive voltages for devices on p-type substrates. The data from the C-V curve was used to determine the
interface state density, flat band voltage shift, and dielectric constant. Information and equations on how to calculate these values can be found in Appendix B.
Figure 3-1. Illustration of a typical Knudsen effusion cell. [Reprinted with permission from B.P. Gila, 2000. Growth and Characterization of Dielectric Materials for Wide Bandgap Semiconductors. PhD dissertation (pg. 37, Figure 3-1). University of Florida, Gainesville, Florida.]
Figure 3-2. Top view sketch of Riber 2300 MBE system used for oxide growth. [Reprinted with permission from B.P. Gila, 2000. Growth and Characterization of Dielectric Materials for Wide Bandgap Semiconductors. PhD dissertation (pg. 38, Figure 3-2). University of Florida, Gainesville, Florida.]
Figure 3-3. AFM images showing pits at surface of as-received Uniroyal GaN.  A) 3-D image of 20 μm scan.  B) 2-D image of 20 μm scan.
Figure 3-4. AFM images showing MOCVD GaN grown by the Abernathy group. A) 3-D image of 5 µm scan. B) 2-D image of 5 µm scan.
Figure 3-5. RHEED images of pre-treated GaN surface. A) After UV-O₃ treatment. B) After BOE treatment of UV-O₃ treated surface. [Reprinted with permission from B.P. Gila, 2000. Growth and Characterization of Dielectric Materials for Wide Bandgap Semiconductors. PhD dissertation (pg. 43, Figure 3-7). University of Florida, Gainesville, Florida.]
Figure 3-6. RHEED photos of GaN surface showing a (1x3) pattern following an in-situ anneal at 700°C. A) <11-20> crystal direction. B) <1-100> crystal direction. [Reprinted with permission from B.P. Gila, 2000. Growth and Characterization of Dielectric Materials for Wide Bandgap Semiconductors. PhD dissertation (pg. 44, Figure 3-8). University of Florida, Gainesville, Florida.]
Figure 3-7. Illustration of MOS capacitors that were fabricated. A) Entire design layout of all 60 diodes made from 3 mask sets. B) Blown-up image of one of the diodes.
Figure 3-8. Diagram of pattern in the mask used to open windows for the ohmic pad. Black region contained oxide that was etched away. Circular white region contained oxide that was protected by PR during the etching.
Figure 3-9. Diagram of pattern in the mask used to deposit ohmic pad. Black region is GaN that metal is deposited on. Circular white region contains thin GaN ring and oxide island protected by PR.
Figure 3-10. Diagram of pattern in the mask used to deposit metal gate. Black region contains ohmic pad, thin GaN ring, and part of oxide island protected by PR. Circular white region contains part of oxide island that metal gate is deposited on top of.
Figure 3-11. Sketches of bi-layer photoresist stack.  A) Undercut profile of LOR 3B underneath the 1818 layer.  B) Discontinuous metal film deposition due to undercut (provides ease for metal lift-off).
Figure 3-12. AES surface scans of as-received and etched $(Sc_2O_3)_x(Ga_2O_3)_{1-x}$ films on GaN. A) As-received. B) 12 minute etch shows complete removal of film.
Figure 3-13. Dry etching of (Sc₂O₃)ₓ(Ga₂O₃)₁₋ₓ on GaN and Si along with a reference piece of GaN in a CH₄/H₂/Ar chemistry.  

A) Fixed ICP power (300 W) with increasing RF chuck power.  
B) Fixed RF chuck power (35 W) with increasing ICP power.

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Figure 3-14. Etch selectivity of (Sc$_2$O$_3$)$_x$(Ga$_2$O$_3$)$_{1-x}$ over GaN for a CH$_4$/H$_2$/Ar etch chemistry.
A) Fixed ICP power (300 W) with increasing RF chuck power.  B) Fixed RF chuck power (35 W) with increasing ICP power.
Figure 3-16. An image of the penetration depth and interaction volume of an electron beam in a material. It shows that Auger electrons only have an escape depth at the top 1.0 nm of the surface. [Reprinted with permission from B.P. Gila, 2000. Growth and Characterization of Dielectric Materials for Wide Bandgap Semiconductors. PhD dissertation (pg. 50, Figure 3-14). University of Florida, Gainesville, Florida.]
CHAPTER 4
GROWTH AND CHARACTERIZATION OF SCANDIUM GALLIUM OXIDE

The objective of this work was to grow \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) as an amorphous film that could be used in a stacked gate dielectric with a crystalline oxide. Previous trends have shown that the smaller the lattice mismatch to GaN, the smaller the \(D_{it}\). However, dislocation defects in the crystalline oxide (due to the lattice mismatch with GaN) act as current leakage paths that limit the breakdown voltage. Depositing an amorphous dielectric on top of the crystalline oxide would allow the properties of the oxide/GaN interface to be maintained while reducing the current leakage by terminating dislocating defects in the crystalline oxide. Previous results of a stacked gate dielectric with SiO\(_2\) deposited on top of Gd\(_2\)O\(_3\) showed improvement of the breakdown field from 0.3 MV/cm to 0.8 MV/cm.\(^{19,20}\)

For \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) to serve as a suitable dielectric in GaN-based devices, it must have a larger band gap and dielectric constant than GaN. There are no electrical properties listed for \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) in literature, so the properties of Gd\(_2\)O\(_3\), Sc\(_2\)O\(_3\), and \((\text{Ga}_2\text{O}_3)_x(\text{Gd}_2\text{O}_3)_{1-x}\) will be discussed to make predictions on the band gap and dielectric constant of \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\). Both Sc\(_2\)O\(_3\) and Gd\(_2\)O\(_3\) have a bixbyite crystal structure, but Sc\(_2\)O\(_3\) has a larger band gap (6.3 eV compared to 5.3 eV) and a larger dielectric constant (14.0 eV compared to 11.4 eV) compared to Gd\(_2\)O\(_3\). Based on the superior electrical properties of Sc\(_2\)O\(_3\), it is believed that using Sc\(_2\)O\(_3\) in place of Gd\(_2\)O\(_3\) will only enhance the properties of the ternary oxide system. The band gap and dielectric constant of \((\text{Ga}_2\text{O}_3)_x(\text{Gd}_2\text{O}_3)_{1-x}\) are 4.7 eV and 14.2 respectively, so any improvement in these values for \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) will place them well above the values for GaN. It will also be critical for the oxide to have confinement with respect to both the valence and conduction bands of GaN. Both Gd\(_2\)O\(_3\) and Ga\(_2\)O\(_3\) are not confined with respect to the valence band of GaN, but \((\text{Ga}_2\text{O}_3)_x(\text{Gd}_2\text{O}_3)_{1-x}\) has confinement with respect to both bands of GaN. Since Sc\(_2\)O\(_3\) also
has confinement at both bands, it is believed that \((\text{Sc}_2\text{O}_3)_{x}(\text{Ga}_2\text{O}_3)_{1-x}\) will have confinement at both bands, and the use of \text{Sc}_2\text{O}_3 might widen the confinement at each band.

**Continuous Growth of \((\text{Sc}_2\text{O}_3)_{x}(\text{Ga}_2\text{O}_3)_{1-x}\)**

The use of Sc and Ga in the oxide films included two purposes. Since previous \text{Sc}_2\text{O}_3 films deposited at 100°C using a high Sc flux were polycrystalline, it was hopeful that adding Ga would frustrate the \text{Sc}_2\text{O}_3 lattice and promote amorphous film growth. The second purpose was using Sc to stabilize Ga in the $3^+$ oxidation state. While Sc has a single oxidation state of $3^+$, Ga has multiple oxidation states of $3^+$, $2^+$, and $1^+$. It is believed that the addition of an electropositive element in a ternary phase will stabilize the higher oxidation state for a metal with multiple oxidation states (examples include \text{KMnO}_4, \text{SrFeO}_4, and \text{BaPbO}_3).55,56

Low substrate temperatures and high growth rates (due to high flux of material) are typically used to foster amorphous film growth in MBE. Therefore, a substrate temperature of 100°C was used, and cell temperatures of 1190°C (corresponding to a \text{Sc}_2\text{O}_3 growth rate of 3.2 nm/min) and 884°C (corresponding to a \text{Ga}_2\text{O}_3 growth rate of 2.3 nm/min) were used for Sc and Ga respectively. The RF oxygen plasma was set at a pressure of $8.0 \times 10^{-6}$ Torr with a forward power of 300 W. A continuous growth was used in which all three shutters were simultaneously open during the growth. During the growth and at the end of the growth, RHEED showed a light arc (Figure 4-1) indicative of polycrystalline film growth. Characterization with TEM also showed arcs in the SAD pattern (Figure 4-2), and a HRTEM image in Figure 4-3 shows the rotation of grains in different directions. Analysis with XRD revealed no peaks (except for those of the \text{GaN} and sapphire), providing further evidence that a fine-grained polycrystalline film was present with no preferred orientation. Characterization with AFM showed an RMS roughness of
5.65 nm for a 1 μm scan and an RMS roughness of 6.78 nm for a 5 μm scan (Figure 4-4). The high surface roughness was associated with the extremely high growth rate of 6.0 nm/min.

An AES surface scan revealed that the films were rich in Sc with a Sc to Ga peak-to-peak ratio of 2.25 (Figure 4-5a). Further analysis with a depth profile revealed surface segregation of Ga (Figure 4-5b). One of the mechanisms that drives surface enrichment is the segregation of the species with the weakest bond.\(^9^2\) The segregation of Ga was attributed to the weaker bond between Ga and O compared to Sc and O. Looking at the electronegativity values for Sc (1.2) and Ga (1.82), it can be seen that Sc is much more electropositive than Ga and has a higher reactivity in forming a compound with O (3.44).\(^9^3\) Segregation is generally eliminated by growing in a kinetically limited regime at low temperatures and high growth rates.\(^9^4-9^6\) Since the surface enrichment of Ga in \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) occurred under these growth conditions, alternative growth techniques were investigated to eliminate the Ga segregation.

**Digital Growth of \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\)**

In an attempt to eliminate the segregation of Ga at the surface, a digital growth technique was used. This technique was previously used for MgCaO to prevent the segregation of Ca.\(^4^7\) The digital growth involved repeatedly alternating the opening and closing of the Sc and Ga shutters at 10 second intervals (10:10) during continuous exposure from the oxygen plasma (Figure 4-6). A polycrystalline RHEED pattern was present for the entire growth, and no peaks appeared in the XRD scan except for peaks from the substrate. AFM showed an RMS roughness of 4.12 nm for a 1 μm scan and an RMS roughness of 5.01 nm for a 5 μm scan (Figure 4-7). The surface roughness was lower compared to the surface roughness for the continuous growth. This was attributed to the lower growth rate of 3.0 nm/min compared to the 6.0 nm/min growth rate.
for the continuous growth. The AES depth profile in Figure 4-8 shows that the digital growth technique did not eliminate the segregation of Ga at the surface of the films.

**Growth with Closure of Ga Shutter**

A third growth technique was employed which involved closing the Ga shutter towards the end of the growth for a certain amount of time while the Sc and O shutters remained open continuously (Figure 4-9). This technique was previously employed to eliminate the segregation of In in the growth of InGaN. The oxygen pressure was also increased to $1.2 \times 10^{-5}$ Torr to increase the VI/III ratio. Various times were investigated to determine the optimal time that would successfully eliminate the surface enrichment of Ga. Table 4-1 and Figure 4-10 show that the Sc:O and Sc:Ga ratios increase with increasing time that the Ga shutter was closed towards the end of the growth, and the Ga:O ratio decreases with increasing time. It was determined that closing the Ga shutter for the final 90 seconds of a 6 minute growth successfully eliminated the segregation of Ga (Figure 4-11).

It can also be seen in the depth profile that the intensities of the Sc and O increase and the intensity of the Ga decreases at the oxide/GaN interface. This same effect was also present in samples with $(\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}$ on Si (Figure 4-12). Further analysis with HRTEM showed a very thin, faint line at the interface (Figures 4-13). This same occurrence was seen in a HRTEM cross-sectional image of $(\text{Ga}_2\text{O}_3)_x(\text{Gd}_2\text{O}_3)_{1-x}$ on GaAs. The thin layer on GaAs (2-3 monolayers) was identified as single crystal Gd$_2$O$_3$. The initial formation of a Gd$_2$O$_3$ layer was attributed to Gd (electronegativity of 1.2) having a higher reactivity with oxygen and being more electropositive compared to Ga (electronegativity of 1.82). Since Sc has the same electronegativity value as Gd and has a much greater value than Ga, it appears that a similar trend is present in the $(\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}$ film with the thin layer at the interface representing Sc$_2$O$_3$ (Figure 4-14).
Characterization with AFM revealed an RMS roughness of 2.98 nm for a 1 μm scan and an RMS roughness of 3.79 nm for a 5 μm scan (Figure 4-15). The large surface roughness was a result of the high 5.5 nm/min growth rate. However, the surface roughness was lower compared to the surface roughness for the continuous and digital growths. This was attributed to the elimination of the Ga surface segregation.

**Electrical Testing of (Sc₂O₃)x(Ga₂O₃)₁₋ₓ**

After fabricating MOS capacitors, current-voltage (I-V) measurements were taken to determine the breakdown voltage. Figure 4-16 shows that the (Sc₂O₃)x(Ga₂O₃)₁₋ₓ film (33 nm) has a poor breakdown field of 0.15 MV/cm at 1 mA/cm². The leakage current is so high that the oxide appears to be more of a conductor. The low breakdown field is indicative of a mode A failure, which is due to defects or pinholes in the oxide or defects at the oxide/semiconductor interface. The film was analyzed further with XPS to determine the root cause of the premature breakdown.

The National Institute of Standards and Technology (NIST) XPS database was used to reference the characteristic binding energies of all the possible chemical species present in the (Sc₂O₃)x(Ga₂O₃)₁₋ₓ film (Table 4-2). The objective of the XPS analysis was to determine if free Ga or Sc metal was present in the film that could act as a dopant atom and create an electrical pathway between the metal gate and GaN substrate. Figures 4-17 to 4-19 indicate the presence of both Ga₂O₃ and Ga metal phases. A 6 eV difference between the two phases is seen for the Ga LMM (Auger) energy level, and a 2 eV difference between the two phases is seen for both the Ga 2p₃/₂ and 3d energy levels. Analysis of the Sc 2p₃/₂ energy level (Figure 4-20) revealed that only the Sc₂O₃ phase is present. A peak at 401.9 eV corresponding to Sc₂O₃ is present, but
no peak appears at 398.3 eV, which is indicative of Sc metal. It can be seen from the XPS data that the free Ga metal present in the film was responsible for the poor breakdown field.

After determining the root cause of the breakdown, \((\text{Sc}_2\text{O}_3)_{x}(\text{Ga}_2\text{O}_3)_{1-x}\) films were grown at lower Ga cell temperatures to eliminate the free Ga metal present in the oxide. The Sc cell temperature was also reduced to make more O atoms available to the Ga atoms and to reduce the overall metal to oxygen ratio, which was higher than desired. Table 4-3 shows that the breakdown voltage increases as the Ga cell temperature decreases. However, the breakdown voltages were still poor. Below a cell temperature of 675°C, Ga was no longer detected in the films using AES. Current-voltage measurements were also taken for digital and continuous films grown at various combinations of high and low Ga and Sc cell temperatures, but the breakdown fields were all lower than 0.5 MV/cm. Because of the poor breakdown voltages for the \((\text{Sc}_2\text{O}_3)_{x}(\text{Ga}_2\text{O}_3)_{1-x}\) films, no C-V measurements were made.

It does not appear that \((\text{Sc}_2\text{O}_3)_{x}(\text{Ga}_2\text{O}_3)_{1-x}\) is a feasible dielectric for GaN-based devices. Previous results with \((\text{Gd}_2\text{O}_3)_{x}(\text{Ga}_2\text{O}_3)_{1-x}\) on GaAs revealed that the breakdown field strength increased as the films became richer in Gd.\(^{55,56}\) A film with a Gd concentration of 14% had a breakdown field of \(\sim1.9\) MV/cm, and the breakdown field increased to 2.5 MV/cm with an increase in the Gd concentration to 20%. However, the best results were obtained with a pure Gd\(_2\)O\(_3\) film as it had an even higher breakdown field of 3.5 MV/cm. It appears that this same trend is present for \((\text{Sc}_2\text{O}_3)_{x}(\text{Ga}_2\text{O}_3)_{1-x}\) as films with increasing amounts of Sc exhibited higher breakdown fields with a pure Sc\(_2\)O\(_3\) film having the highest breakdown field (\(\sim2.70\) MV/cm). It is believed that the incorporation of Ga into the films creates defects that diminish the insulating properties of the oxide.
Table 4-1. Auger peak-to-peak ratios for Ga:O, Sc:O, and Sc:Ga as function of the amount of time that the Ga shutter was closed towards the end of the growth.

<table>
<thead>
<tr>
<th>Ga shutter closure time (sec)</th>
<th>Ga:O</th>
<th>Sc:O</th>
<th>Sc:Ga</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.21</td>
<td>0.48</td>
<td>2.25</td>
</tr>
<tr>
<td>30</td>
<td>0.18</td>
<td>0.54</td>
<td>3.10</td>
</tr>
<tr>
<td>45</td>
<td>0.14</td>
<td>0.56</td>
<td>3.90</td>
</tr>
<tr>
<td>60</td>
<td>0.11</td>
<td>0.59</td>
<td>4.44</td>
</tr>
<tr>
<td>75</td>
<td>0.11</td>
<td>0.60</td>
<td>5.38</td>
</tr>
<tr>
<td>90</td>
<td>0.11</td>
<td>0.61</td>
<td>5.66</td>
</tr>
<tr>
<td>120</td>
<td>0.08</td>
<td>0.65</td>
<td>7.96</td>
</tr>
</tbody>
</table>
Table 4-2. Characteristic binding energies of possible phases present in $(\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}$.

<table>
<thead>
<tr>
<th>Element</th>
<th>Spectral Line</th>
<th>Phase</th>
<th>Binding Energy (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ga</td>
<td>LMM (Auger)</td>
<td>$\text{Ga}_2\text{O}_3$</td>
<td>191.2</td>
</tr>
<tr>
<td>Ga</td>
<td>LMM (Auger)</td>
<td>Ga</td>
<td>185.3</td>
</tr>
<tr>
<td>Ga</td>
<td>2p$_{3/2}$</td>
<td>$\text{Ga}_2\text{O}_3$</td>
<td>20.5</td>
</tr>
<tr>
<td>Ga</td>
<td>2p$_{3/2}$</td>
<td>Ga</td>
<td>18.5</td>
</tr>
<tr>
<td>Ga</td>
<td>3d</td>
<td>$\text{Ga}_2\text{O}_3$</td>
<td>1117.8</td>
</tr>
<tr>
<td>Ga</td>
<td>3d</td>
<td>Ga</td>
<td>1116.5</td>
</tr>
<tr>
<td>Sc</td>
<td>2p$_{3/2}$</td>
<td>$\text{Sc}_2\text{O}_3$</td>
<td>401.9</td>
</tr>
<tr>
<td>Sc</td>
<td>2p$_{3/2}$</td>
<td>Sc</td>
<td>398.3</td>
</tr>
</tbody>
</table>
Table 4-3. Breakdown voltage as a function of decreasing Ga cell temperature.

<table>
<thead>
<tr>
<th>Sample</th>
<th>$T_{Ga}$ (°C)</th>
<th>$T_{Sc}$ (°C)</th>
<th>$t_{ox}$ (nm)</th>
<th>G (nm/min)</th>
<th>$V_{bd}$ (MV/cm) at 1 mA/cm$^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>865</td>
<td>1190</td>
<td>33</td>
<td>5.5</td>
<td>0.15</td>
</tr>
<tr>
<td>2</td>
<td>770</td>
<td>1180</td>
<td>47</td>
<td>2.4</td>
<td>0.70</td>
</tr>
<tr>
<td>3</td>
<td>750</td>
<td>1180</td>
<td>42</td>
<td>2.1</td>
<td>1.00</td>
</tr>
<tr>
<td>4</td>
<td>725</td>
<td>1180</td>
<td>40</td>
<td>2.0</td>
<td>1.40</td>
</tr>
</tbody>
</table>
Figure 4-1. RHEED image of (Sc₂O₃)ₓ(Ga₂O₃)₁₋ₓ on GaN during and after growth.
Figure 4-2. TEM SAD pattern of \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) on GaN.
Figure 4-3. HRTEM image of $\text{Sc}_2\text{O}_3 \times (\text{Ga}_2\text{O}_3)_{1-x}$ on GaN.
Figure 4-4. AFM images of \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) on GaN for a continuous growth. A) 1 \(\mu m\) scan with RMS roughness of 5.65 nm. B) 5 \(\mu m\) scan with RMS roughness of 6.78 nm.
Figure 4-5. AES analysis of continuous growth for \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) on GaN. A) Surface scan. B) Depth profile.
Figure 4-6. Diagram of a digital growth technique in which the Sc and Ga shutters are alternated for a given time sequence while the oxygen shutter is open continuously throughout the entire growth.
Figure 4-7. AFM images of (Sc$_2$O$_3$)$_x$(Ga$_2$O$_3$)$_{1-x}$ on GaN for a digital growth. A) 1 μm scan with RMS roughness of 4.12 nm. B) 5 μm scan with RMS roughness of 5.01 nm.
Figure 4-8. AES analysis of digital growth for \((\text{Sc}_2\text{O}_3)_{x}(\text{Ga}_2\text{O}_3)_{1-x}\) on GaN. A) Surface scan. B) Depth profile.
Figure 4-9. Diagram of growth technique in which the Ga shutter is closed towards the end of the growth for a designated amount of time while the Sc and O shutters are open continuously.
Figure 4-10. Change in Auger peak-to-peak ratios as a function of the amount of time that the Ga shutter is closed towards the end of growth. A) Sc:Ga. B) Ga:O and Sc:O.
Figure 4-11. AES analysis of growth with Ga shutter closure for \((\text{Sc}_2\text{O}_3)_{x}(\text{Ga}_2\text{O}_3)_{1-x}\) on GaN.  
A) Surface scan.  B) Depth profile.
Figure 4-12. AES depth profile of growth with Ga shutter closure for \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) on Si.
Figure 4-13. Low magnification cross-section TEM image of $(\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}$ on GaN with a thin Sc$_2$O$_3$ layer at the GaN/oxide interface.
Figure 4-14. High magnification cross-section TEM image of \((\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}\) on GaN with a thin \text{Sc}_2\text{O}_3 layer at the GaN/oxide interface.
Figure 4-15. AFM images of $(\text{Sc}_2\text{O}_3)_x(\text{Ga}_2\text{O}_3)_{1-x}$ on GaN for a growth with the Ga shutter closed towards the end. A) $1 \mu m$ scan with RMS roughness of 2.98 nm. B) $5 \mu m$ scan with RMS roughness of 3.79 nm.
Figure 4-16. Current-voltage (I-V) plot of (Sc$_2$O$_3$)$_x$(Ga$_2$O$_3$)$_{1-x}$ film deposited at 100°C. Film stoichiometry was rich in Sc.
Figure 4-17. Ga LMM level shows a 6 eV difference between the Ga$_2$O$_3$ and Ga metal peaks.
Figure 4-18. Ga $2p_{3/2}$ level shows a 2 eV difference between the Ga$_2$O$_3$ and Ga metal peaks.
Figure 4-19. Ga 3d level shows a 2 eV difference between the Ga$_2$O$_3$ and Ga metal peaks.
Figure 4-20. Sc 2p_{3/2} level only shows the presence of a Sc_2O_3 phase.
CHAPTER 5
OPTIMIZATION OF MAGNESIUM OXDE

Previous results with MgO showed the best electrical results (i.e., 4.4 MV/cm breakdown field and \(D_{it}\) value of \(1 \times 10^{11}\) eV\(^{-1}\)cm\(^{-2}\)) at low oxygen pressures (high Mg to O ratio) and high growth rates.\(^3\) However, further optimization is needed to make the films more environmentally and thermally stable. Films grown at higher growth rates show deterioration in air after a few days and etch in DI water within 10 seconds. Considering the number of processing steps that require a DI rinse and the fact that most developers are water based (i.e., AZ 300 MIF developer is 97.5% water), it is essential to find a set of growth parameters to improve the environmental stability of MgO.

MgO Growth at Low Growth Rates and Oxygen Pressures

Utilizing both lower growth rates (<1.3 nm/min) and oxygen pressures (<5 \times 10^6 Torr and Mg:O ratio of 0.68) improved the environmental stability immensely. Films showed no deterioration in air over a period of a few months, and fabricated MOS capacitors maintained breakdown fields greater than 3.5 MV/cm (at 1 mA/cm\(^2\)) after receiving a variety of wet processing treatments. The wet treatments included DI water, AZ 300 MIF developer, and PG remover (Table 5-1) since these are the common wet chemicals that samples are treated with during processing. Sixty diodes from an as-received MgO sample were measured, and then the sample was cleaved into 3 separate pieces with each piece receiving one of the three wet treatments. A 1 minute rinse in DI water showed no etching or degrading of the MgO film as the tested diode had a forward breakdown voltage of 14.9 V (3.82 mV/cm) at 1 mA/cm\(^2\) before the treatment and 14.8 V (3.79 MV/cm) after the treatment (Figure 5-1). A 3 minute treatment in developer also revealed no deterioration of the MgO film as the tested diode had a forward breakdown voltage of 14.1 V (3.62 MV/cm) at 1 mA/cm\(^2\) before the treatment and 14.5 V (3.72
MV/cm) after the treatment (Figure 5-2). A 10 minute treatment in PG remover showed no effect on the MgO film as the measured diode had a forward breakdown voltage of 14.1 V (3.62 MV/cm) at 1 mA/cm² before the treatment and 13.8 V (3.54 MV/cm) after the treatment (Figure 5-3). Despite the improved environmental stability, MgO is not thermally stable as high temperature anneals (1000°C for 2 minutes) cause degradation due to increased surface and interfacial roughnesses. The addition of a Sc₂O₃ cap has been shown to provide thermal stability, but the use of the capping layer adds an additional processing step since it must be dry etched prior to wet etch removal of the MgO layer. This provided motivation to determine if the addition of Sc to MgO (MgₓScᵧOₓ was formed) could increase the environmental and thermal stability of the film.

**Results of MgₓScᵧOₓ**

Previous results revealed that MgₓScᵧOₓ degraded and etched at a much slower rate than MgO, but significant degradation occurred after annealing. Since the previous MgₓScᵧOₓ films were grown at high oxygen pressures and growth rates, it was hopeful that lower oxygen pressures and growth rates could enhance the stability of the film as these growth conditions did for MgO. The electrical results of MgₓScᵧOₓ were also investigated to determine if any improvements are made in the breakdown voltage, flatband voltage shift, or Dᵦ with the addition of Sc to MgO.

Three separate films were deposited on u-GaN using a substrate temperature of 100°C, an oxygen pressure less than 4x10⁻⁶ Torr, a Mg cell temperature of 340°C (corresponds to 1.3 nm/min MgO growth rate), and increasing Sc cell temperatures of 1090 °C, 1135 °C, and 1180°C (corresponds to Sc₂O₃ growth rate of 1.1 nm/min). The growth with the Sc cell temperature at 1090°C yielded a growth rate of 1.47 nm/min with a film thickness of 43.7 nm.
Figure 5-4 shows that the film had a forward breakdown voltage of 15.7 V (3.59 MV/cm breakdown field) at 1 mA/cm². Thirty six out of 60 diodes were tested, and 10 of the 36 (28 %) diodes had a breakdown voltage greater than 10 V. A $D_{it}$ of $4.0 \times 10^{11}$ eV⁻¹cm⁻² was calculated at 0.4 eV below the conduction band using the Terman method. Despite the good breakdown voltage and $D_{it}$, the film had an extremely high flatband voltage shift of 5.30 V at a frequency of 10 kHz (Figure 5-5). Besides the presence of fixed oxide charge ($Q_{ox}$) and interface trapped charge ($D_{it}$), oxide trapped charge ($Q_{ot}$) was also present from the large applied gate bias of 12 V (wide scanning range from 12 to 0 V was used to obtain distinct accumulation and depletion regions). When using the same frequency and scanning rate but applying a smaller gate bias of 10 V (scanning range was from 10 V to 2 V), a lower flatband voltage shift of 4.65 V was obtained. Given the flatband voltage shift difference of 0.65 V between the two scans, it appears that the larger bias injected more carriers into the oxide (Figure 5-6). Since a positive flatband voltage shift indicates the accumulation of negative charges in the oxide, it appears that the large positive bias injected electrons from the semiconductor into the oxide.⁸⁹

The deposition with the Sc cell temperature at 1135°C had a growth rate of 1.84 nm/min with a film thickness of 55.1 nm. A forward breakdown voltage of 22.0 V (3.99 MV/cm breakdown field) was obtained at 1 mA/cm² (Figure 5-7). Thirty five out of 60 diodes were tested, and 17 of the 35 (48%) diodes had a breakdown voltage greater than 20 V. A $D_{it}$ of $2.2 \times 10^{11}$ eV⁻¹cm⁻² was calculated at 0.4 eV below the conduction band using the Terman method. The film had a large flatband voltage shift of 4.35 V at a frequency of 10 kHz, and a small hump was present in the C-V curve between 2 V and 4 V (Figure 5-8). The hump is indicative of a specific trap in the oxide that could be a result of a defect incurred during sample preparation from one of the cleaning steps or from In mounting the sample. It is also possible that the solid...
solubility limit of Sc in MgO was reached under these growth conditions, and the formation of two phases (MgO and Sc₂O₃) led to the creation of a trap. A lower flatband voltage shift of 3.89 V was obtained by using a scanning range with a smaller gate bias of 10 V (sweep from 10 V to 0 V). The 0.46 V difference between the two scans was once again an indicator of trapped oxide charge present in the film as the scan using the larger bias injected more carriers into the oxide.

The film deposited with a Sc cell temperature at 1180°C produced a growth rate of 2.26 nm/min with a film thickness of 67.7 nm. A forward breakdown voltage of 26.7 V (3.94 MV/cm breakdown field) was achieved at 1 mA/cm² (Figure 5-9). Twenty seven out of 60 diodes were tested, and 14 of the 27 (52%) diodes had a breakdown voltage greater than 25 V. A Dit of 1.0×10¹¹ eV⁻¹cm⁻² was calculated at 0.4 eV below the conduction band using the Terman method. A flatband voltage shift of 3.83 V was obtained at a frequency of 10 kHz, and a small hump was also present in the C-V curve between 1 V and 3 V (Figure 5-10). A lower flatband voltage shift ($V_{FB} = 2.91$ V) was obtained once again by using a sweep range with a lower applied gate bias (sweep from 10 V to 0 V).

All three MgₓScᵧOₙ films had breakdown fields greater than 3.5 MV/cm and Dit values in the low $10^{11}$ eV⁻¹cm⁻² range, but they also had flatband voltage shifts of ~3 V or greater (Table 5-2). Given the different valences of Sc (3⁺) and Mg (2⁺) and the different crystal structures and lattice constants for MgO and Sc₂O₃, it is expected that the two would have a low solid solubility. It is believed that the low solubility of the two compounds and mixed valences generate a large number of defects within the oxide that are responsible for the large flatband voltage shift.

The previous trend with MgO showed that better electrical results ($V_{bd}$ and Dit) were obtained at higher Mg:O ratios. This same trend is apparent for the MgₓScᵧOₙ films as the
flatband voltage shift and $D_n$ decreased with increasing metal to oxygen ratio due to the increasing Sc cell temperature at constant oxygen pressure and Mg cell temperature (Figure 5-11). Although the films showed high breakdown fields and low $D_n$ values, the large flatband voltage shifts make $\text{Mg}_x\text{Sc}_y\text{O}_z$ a poor dielectric to use on GaN. Because of the large flatband voltage shifts, the thermal and environmental stability of the films at the new growth conditions were not investigated.
Table 5-1. Breakdown field values (at 1 mA/cm\(^2\)) of tested diodes before and after various wet processing treatments.

<table>
<thead>
<tr>
<th>Wet treatment</th>
<th>(V_{bd}) (MV/cm) at 1 mA/cm(^2) before treatment</th>
<th>(V_{bd}) (MV/cm) at 1 mA/cm(^2) after treatment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 min DI H(_2)O</td>
<td>3.82</td>
<td>3.79</td>
</tr>
<tr>
<td>3 min developer</td>
<td>3.62</td>
<td>3.72</td>
</tr>
<tr>
<td>10 min PG remover</td>
<td>3.62</td>
<td>3.54</td>
</tr>
</tbody>
</table>
Table 5-2. Electrical results for Mg$_x$Sc$_y$O$_z$ films on GaN for increasing Sc cell temperatures.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Mg$_x$Sc$_y$O$<em>z$ ($T</em>{Sc} = 1090^\circ$C)</th>
<th>Mg$_x$Sc$_y$O$<em>z$ ($T</em>{Sc} = 1135^\circ$C)</th>
<th>Mg$_x$Sc$_y$O$<em>z$ ($T</em>{Sc} = 1180^\circ$C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{ox}$ (nm)</td>
<td>43.7</td>
<td>55.1</td>
<td>67.7</td>
</tr>
<tr>
<td>$G$ (nm/min)</td>
<td>1.47</td>
<td>1.84</td>
<td>2.26</td>
</tr>
<tr>
<td>$V_{bd}$ (MV/cm) at 1 mA/cm$^2$</td>
<td>3.59</td>
<td>3.99</td>
<td>3.94</td>
</tr>
<tr>
<td>$D_{it}$ (eV$^{-1}$cm$^{-2}$) at $E_c - 0.4$ eV</td>
<td>$4.0 \times 10^{11}$</td>
<td>$2.2 \times 10^{11}$</td>
<td>$1.0 \times 10^{11}$</td>
</tr>
<tr>
<td>$V_{FB}$ (V)</td>
<td>5.30</td>
<td>4.35</td>
<td>3.83</td>
</tr>
<tr>
<td>Diodes tested</td>
<td>36/60 (60%)</td>
<td>35/60 (58%)</td>
<td>27/60 (45%)</td>
</tr>
<tr>
<td>Diodes &gt; 10 V</td>
<td>10/36 (28%)</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>Diodes &gt; 20 V</td>
<td>---</td>
<td>17/35 (48%)</td>
<td>---</td>
</tr>
<tr>
<td>Diodes &gt; 25 V</td>
<td>---</td>
<td>---</td>
<td>14/27 (52%)</td>
</tr>
</tbody>
</table>
Figure 5-1. Current-voltage (I-V) plot of MgO film (39 nm thick) before and after a 1 minute DI water treatment. Breakdown field was 3.82 MV/cm at 1 mA/cm² before the treatment and 3.79 MV/cm after the treatment. Compliance was 100 nA.
Figure 5-2. Current-voltage (I-V) plot of MgO film (39 nm thick) before and after a 3 minute treatment in developer. Breakdown field was 3.62 MV/cm at 1 mA/cm² before the treatment and 3.72 MV/cm after the treatment. Compliance was 100 nA.
Figure 5-3. Current-voltage (I-V) plot of MgO film (39 nm thick) before and after a 10 minute treatment in PG remover. Breakdown field was 3.62 MV/cm at 1 mA/cm² before the treatment and 3.54 MV/cm after the treatment. Compliance was 100 nA.
Figure 5-4. Current-voltage plot of Mg$_x$Sc$_y$O$_z$ film on u-GaN at Sc cell temperature of 1090°C. Breakdown field was 3.59 MV/cm at 1 mA/cm$^2$ for a film thickness of 43.7 nm. Compliance was 100 nA.
Figure 5-5. Capacitance-voltage plot of Mg$_x$Sc$_y$O$_z$ film on u-GaN at Sc cell temperature of 1090°C. Flatband voltage shift of 5.30 V and $D_{it}$ of $4.0 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ was calculated from the C-V curve taken at a frequency of 10 kHz.
Figure 5-6. Capacitance-voltage plot of two different scanning ranges for a Mg$_x$Sc$_y$O$_z$ film on u-GaN at a Sc cell temperature of 1090°C. Flatband voltage shift difference of 0.65 V appears between the two curves with different applied gate biases.
Figure 5-7. Current-voltage plot of Mg$_x$Sc$_y$O$_z$ film on u-GaN at Sc cell temperature of 1135°C. Breakdown field was 3.99 MV/cm at 1 mA/cm$^2$ for a film thickness of 55.1 nm. Compliance was 100 nA.
Figure 5-8. Capacitance-voltage plot of Mg$_x$Sc$_y$O$_z$ film on u-GaN at Sc cell temperature of 1135°C. Flatband voltage shift of 4.35 V and $D_{it}$ of $2.2 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ was calculated from the C-V curve taken at a frequency of 10 kHz.
Figure 5-9. Current-voltage plot of Mg$_x$Sc$_y$O$_z$ film on u-GaN at Sc cell temperature of 1180°C. Breakdown field was 3.94 MV/cm at 1 mA/cm$^2$ for a film thickness of 67.7 nm. Compliance was 100 nA.
Figure 5-10. Capacitance-voltage plot of Mg$_x$Sc$_y$O$_z$ film on u-GaN at Sc cell temperature of 1180°C. Flatband voltage shift of 3.83 V and $D_{it}$ of $1.0 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ was calculated from the C-V curve taken at a frequency of 10 kHz.
Figure 5-11. Normalized capacitance-voltage (C-V) plots of Mg$_x$Sc$_y$O$_z$ films on GaN at Sc cell temperatures of 1090°C, 1135°C, and 1180°C.
CHAPTER 6
METALLIZATION STUDY WITH MAGNESIUM OXIDE

The processing scheme for fabrication of a MOS capacitor (discussed in chapter 2) includes oxide deposition prior to deposition of ohmic metal pads. The disadvantage of this sequence of steps is that the oxide is annealed at extremely high temperatures (i.e., >750°C in RTA) during the ohmic anneal. High temperature annealing of MgO causes deterioration of the MgO/GaN interface and the oxide itself. This problem could be avoided if the sequence of steps was reversed so that the ohmic metal pads are deposited prior to oxide deposition. Besides maintaining the stability of the oxide, the change in the processing scheme would provide other important advantages as well.

Prior to ohmic metal deposition, it is extremely important to remove residual PR from the exposed ohmic windows on the substrate surface since it can effect the contact resistance and possibly lead to removal of the ohmic pad during metal lift-off. Most cleaning steps include an oxygen treatment to remove the residual PR, followed by a wet treatment (i.e., BOE or HCl) to remove the native oxide formed on the substrate surface from the oxygen treatment. With the current processing scheme, no cleaning treatment is applied to the GaN surface prior to ohmic metal deposition. This is done to avoid etching or degrading the oxide (covered by PR from patterning for ohmic metallization) during the wet treatment to remove the native oxide. Considering that MgO etches in a 2% H₃PO₄ solution in 10–12 seconds, a 3–5 minute wet treatment with BOE or HCl would severely degrade and etch the oxide. Depositing the ohmic pads before oxide deposition would allow the GaN surface to be thoroughly cleaned prior to metal deposition since there would be no oxide present that could be affected by the wet treatment.
Another advantage of depositing the ohmic pads prior to oxide deposition would be the simultaneous annealing of the pads and cleaning of the GaN surface. The current GaN surface pre-treatment procedure includes a 700°C in-situ anneal for 10 minutes before the sample is cooled to the desired substrate temperature for oxide deposition. Since the MBE system is at such a low pressure (i.e., 5x10⁻⁹ Torr), the same ohmic contact that is annealed in the RTA (at 760 Torr) at >750°C can be adequately annealed at lower temperatures in the MBE system. The MBE system also provides a much cleaner environment for annealing. An advantage for p-type GaN is that the activation anneal can be performed at the same annealing temperature as that used for the ohmic contacts and GaN surface cleaning treatment. Being able to perform all of these functions in one step would eliminate extra steps in the fabrication process and provide higher throughput.

If the processing scheme is changed so that the ohmic metallization is completed before deposition of the oxide, two critical factors must be met. The first factor is that a surface treatment procedure must be found that can effectively clean the GaN surface without affecting the ohmic contact. Poor cleaning of the GaN surface could lead to a high Dᵣ value and influence the overall quality of the growing film. Typical wet treatments that are used to degrease the substrate surface and remove the native oxide from the surface could lead to etching or degradation of the ohmic contact. The second factor is that a surface treatment must be found that will produce comparable electrical results (i.e., Dᵣ, V₉FB, and V₉bd) with the results previously achieved using the old processing scheme with oxide deposition prior to ohmic metallization. It is extremely important to find a suitable surface treatment since the current processing scheme for the fabrication of an enhancement mode MOSFET includes ohmic metallization prior to oxide deposition.
Metallization Study on u-GaN

Using the new processing scheme, a metallization study was performed on u-GaN ($N_D \approx 5 \times 10^{16}$ cm$^{-3}$ measured by Hall) with deposition of MgO. Cleaning of the GaN surface prior to ohmic metallization included a 25 min UV-O$_3$ treatment followed by a 5 min BOE treatment. After ohmic metal deposition, metal lift-off was performed to remove the excess metal and obtain the patterned ohmic pads. Multiple surface cleaning pre-treatments were then used to determine the one with the best electrical characteristics. Electrical results of the various surface treatments were also compared to the surface treatment that was used in the old processing scheme (standard: 3 min HCl:H$_2$O (1:1), 25 min UV-O$_3$, and 5 min BOE). The following surface treatments were analyzed: 1) 25 min UV-O$_3$, 2) 25 min UV-O$_3$ + 10 min NH$_4$OH, 3) 25 min UV-O$_3$ + 1 min BOE, and 4) 25 min UV-O$_3$ + in-situ anneal at 700°C for 10 min under an N$_2$ plasma. Treatment of the surface with only UV-O$_3$ excluded the use of wet chemicals to remove any possibility of them having an effect on the ohmic contacts. The application of wet treatments such as NH$_4$OH and BOE were used to remove as much of the native oxide formed from the UV-O$_3$ treatment without damaging the ohmic pads. The fourth treatment included the use of an N$_2$ plasma to form volatile species at the surface that would desorb from the surface during the in-situ anneal. The MgO thin films were deposited at a substrate temperature of 100°C, an Mg cell temperature of 340°C, and an oxygen pressure less than $5 \times 10^{-6}$ Torr.

All of the samples had a thickness of 39.0 nm, corresponding to a growth rate of 1.3 nm/min. The sample with the UV-O$_3$ treatment had a breakdown voltage of 15.3 V (3.92 MV/cm) at 1 mA/cm$^2$ (Figure 6-1). Sixty MOS capacitors were tested with 33 out of 60 (55 %) having breakdown voltages greater than 10 V. A $D_{it}$ of $2.0 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ was calculated at 0.4 eV below the conduction band using the Terman method. A flatband voltage shift of 0.46 V was
calculated from the C-V curve in Figure 6-2. The flatband voltage shift was a result of the metal-semiconductor work function difference (calculated as $\Phi_{ms} = 1.43$ eV assuming a work function of 5.6 eV for platinum), interface trapped charge ($D_{it}$), and fixed oxide charge ($Q_{ox}$). The fixed oxide charge was attributed to possible dangling bonds at the GaO$_x$/MgO interface that were formed during oxidation of the GaN surface from the UV-O$_3$ treatment or possible dangling bonds present at grain boundaries or dislocations in the MgO film.

The sample with the UV-O$_3$ and NH$_4$OH treatment included the use of a wet treatment in an attempt to remove the native oxide formed from the UV-O$_3$ step. It had a breakdown voltage of 15.7 V (4.02 MV/cm) at 1 mA/cm$^2$ (Figure 6-3). Sixty diodes were tested with 39 out of the 60 diodes (65%) having a breakdown voltage greater than 10 V. A $D_{it}$ of $1.8 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ at 0.4 eV below the conduction band was calculated using the Terman method. A flatband voltage shift of 0.63 V was calculated from the C-V curve in Figure 6-4. Since this value is comparable to the value obtained from the sample with only the UV-O$_3$ treatment, it is believed that the NH$_4$OH treatment was not successful in removing the native oxide layer formed from the UV-O$_3$.

The combination of a UV-O$_3$ and BOE treatment was then used since BOE is commonly used to strip the native oxide from the GaN surface. However, a short BOE treatment of only 1 minute was used since longer periods of time can lead to degradation or complete removal of the ohmic pads. The sample with this treatment had a breakdown voltage of 14.4 V (3.69 MV/cm) at 1 mA/cm$^2$ (Figure 6-5). Sixty diodes were measured with 32 out of 60 diodes (53%) having a breakdown voltage greater than 10 V. A $D_{it}$ of $2.0 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ was calculated at 0.4 eV below the conduction band using the Terman method. A flatband voltage shift of 0.64 V was determined using the C-V curve in Figure 6-6. Given the comparable flatband voltage shift with
the previous two surface pre-treatments, it is believed that the 1 min BOE treatment was unable
to remove the native oxide layer formed from the UV-O3 treatment. It is desirable to use a
longer BOE treatment, but that could lead to damage of the ohmic contacts.

The sample treated with UV-O3 and an in-situ anneal under an N2 plasma produced a
breakdown voltage of 14.9 V (3.82 MV/cm) at 1 mA/cm² (Figure 6-7). Sixty MOS capacitors
were measured with 38 out of 60 (63%) having a breakdown voltage greater than 10 V. A \( D_{it} \) of
2.0x10^{11} eV^{-1}cm^{-2} was calculated at 0.4 eV below the conduction band using the Terman method.
A flatband voltage shift of 0.41 V was determined from the C-V curve in Figure 6-8.

All four surface pre-treatments had breakdown fields of \(~3.70 MV/cm\) or greater (Figure 6-
9 and Table 6-1), \( D_{it} \) values around 2.0x10^{11} eV^{-1}cm^{-2}, and flatband voltage shifts of 0.63 V or
less (Figure 6-10). Looking at the ohmic contacts for each sample under an optical microscope
revealed that the contacts were not damaged by any of the treatments. It appears that the pre-
treatment with the in-situ N2 plasma anneal is the best surface treatment since it yielded the
lowest flatband voltage shift. However, all of the electrical values were representative of the
best MOS capacitor from each sample and do not represent the entire sampling set. More
capacitors would need to be fabricated and tested to determine a specific trend as to which pre-
treatment offers the best starting surface to grow on. The difference in the flatband voltage shifts
among the samples is also within the error of the measurement and calculations used in
determining the value.

Electrical values for the standard surface pre-treatment were taken from a different GaN
wafer in which MgO was deposited prior to ohmic metal deposition. The values included a
breakdown field of 3.67 MV/cm, a \( D_{it} \) of 1.0x10^{11} ev^{-1}cm^{-2} at 0.4 eV below the conduction band,
and a flatband voltage shift of 0.18 V. Since the results are comparable to the electrical results
obtained from the samples with the different surface pre-treatments, the new fabrication scheme is a feasible process for fabricating future MOS capacitors and e-mode MOSFETs.

**Electrical Results on p-GaN**

A similar study was performed on p-GaN ($N_A \sim 4 \times 10^{17}$ cm$^{-3}$ measured by Hall) with deposition of MgO. However, a suitable ohmic contact was not available that could be annealed in-situ at 700°C for 10 min. Metal stacks of Ni/Au and Pt/Au were researched, but the in-situ anneal caused deterioration of the contacts and extremely high contact resistances (Figure 6-11). Without the availability of a suitable ohmic contact for the in-situ anneal, the study was performed by preparing (includes sample cleaning and mounting) and growing on samples without ohmic metal. However, two different surface treatments, which could be used if ohmic metal was present on p-GaN prior to sample preparation and growth, were analyzed for their feasibility. The following surface pre-treatments on p-GaN were used in comparison to the standard pre-treatment (3 min HCl:H$_2$O (1:1), 25 min UV-O$_3$, and 5 min BOE): 1) 25 min UV-O$_3$ and 2) 25 min UV-O$_3$ + 1 min BOE. Following sample preparation, the MgO thin films were deposited at a substrate temperature of 100°C, a Mg cell temperature of 340°C, and an oxygen pressure less than 5x10$^{-6}$ Torr. Metal gates (Pt/Au) were then sputter deposited, and In metal was soldered along the edge of the sample to make an ohmic contact to the p-GaN.

Since all three samples were grown simultaneously, they had the same thickness of 37.6 nm, which corresponded to a growth rate of 1.25 nm/min. The sample with the standard surface treatment had a breakdown voltage of -15.9 V (4.23 MV/cm) at 1 mA/cm$^2$ (Figure 6-12). Thirty out of 60 diodes were tested with 12 out of the 30 diodes (40%) having a breakdown voltage less than -10 V. The C-V curve in Figure 6-13 shows distinct regions of accumulation and deep depletion as the gate voltage is swept from negative to positive voltages at a frequency of 10
kHz. The broad curve is obtained because of the large bias range that was used to deplete the high density of carriers (apparent carrier concentration was measured as $1.5 \times 10^{18}$ cm$^{-3}$ from C-V curve). These C-V results are in contrast to previous C-V results for p-GaN MOS capacitors with SiO$_2$ as the dielectric. Previous results revealed a curve more representative of results for an n-GaN MOS capacitor as the curve showed an increasing capacitance as the gate bias was swept from negative to positive voltages.$^{102}$ The C-V curve obtained in this study is the typical curve that would be expected for a p-GaN MOS capacitor.

The other two surface treatments yielded similar electrical results. The sample that received the surface pre-treatment with UV-O$_3$ and BOE had a breakdown voltage of -13.4 V (3.56 MV/cm) at 1 mA/cm$^2$ (Figure 6-14). Thirty out of 60 diodes were tested with 17 out of the 30 diodes (56%) producing breakdown voltages less than -10 V. The C-V curve in Figure 6-15 (measured at 10 kHz) shows distinct regions of accumulation and deep depletion. The MgO sample with only the UV-O$_3$ pre-treatment had a breakdown voltage of -13 V (3.46 MV/cm) at 1 mA/cm$^2$ (Figure 6-16). Thirty out of 60 diodes were tested with 15 out of the 30 diodes (50%) having a breakdown voltage less than -10 V. The measured C-V curve (Figure 6-17) showed the same trend as the other two samples with distinct accumulation and deep depletion regions over a wide bias range (-8 V to 7 V).

After comparing the electrical results from the three different surface pre-treatments, it appears that the two metallization surface treatments (25 min UV-O$_3$ + 1 min BOE and 25 min UV-O$_3$) are feasible for the new processing scheme in which ohmic metal is deposited prior to oxide deposition. All three samples had breakdown fields of ~3.5 MV/cm or greater with more than 40% of the tested diodes breaking down at voltages less than -10 V (Figure 6-18). Although the sample with the standard pre-treatment had the highest breakdown voltage out of the three,
its value was representative of one diode and not the whole set of diodes. Looking at the C-V results in Figure 6-19, it can be seen that all three samples have a large negative flatband voltage shift. The large flatband voltage shift is primarily attributed to the high metal-semiconductor work function difference and oxide trapped charge ($Q_{ot}$). Assuming a work function of 5.6 eV for platinum, a work function difference of -1.78 eV was calculated for the samples. Since the flatband voltage shift was negative, it is believed that the large negative gate bias injected holes from the semiconductor into the oxide, resulting in an equivalent negative charge in the semiconductor. It is also a possibility that trapped electrons in the oxide were injected from the oxide into the surface of the semiconductor. Further analysis of the C-V curve reveals that the $D_{it}$ is very similar for all three samples, but the sample with the UV-O$_3$ and BOE treatment appears to have a slightly lower $D_{it}$ based on its steeper slope.
Table 6-1. Electrical results for MgO films on u-GaN with various surface pre-treatments. The oxide was deposited following ohmic metal deposition.

<table>
<thead>
<tr>
<th>Surface pre-treatment</th>
<th>$V_{bd}$ (MV/cm) at 1 mA/cm$^2$</th>
<th>$D_{it}$ (eV$^{-1}$ cm$^{-2}$) at $E_c-0.4$ eV</th>
<th>$V_{FB}$ (V)</th>
<th>Diodes &gt; 10 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 min UV-O$_3$</td>
<td>3.92</td>
<td>$2.0 \times 10^{11}$</td>
<td>0.46</td>
<td>33/60 (55%)</td>
</tr>
<tr>
<td>25 min UV-O$_3$ + 10 min NH$_4$OH</td>
<td>4.02</td>
<td>$1.8 \times 10^{11}$</td>
<td>0.63</td>
<td>39/60 (65%)</td>
</tr>
<tr>
<td>25 min UV-O$_3$ + 1 min BOE</td>
<td>3.69</td>
<td>$2.0 \times 10^{11}$</td>
<td>0.64</td>
<td>32/60 (53%)</td>
</tr>
<tr>
<td>25 min UV-O$_3$ + N$_2$ plasma anneal</td>
<td>3.82</td>
<td>$2.0 \times 10^{11}$</td>
<td>0.41</td>
<td>38/60 (63%)</td>
</tr>
</tbody>
</table>
Figure 6-1. Current-voltage (I-V) plot for MgO on u-GaN with a 25 min UV-O₃ surface pre-treatment. Breakdown field was 3.92 MV/cm at 1 mA/cm² for a film thickness of 39 nm. Compliance was 100 nA.
Figure 6-2. Capacitance-voltage (C-V) plot for MgO on p-GaN with a 25 min UV-O₃ surface pre-treatment. Measurement was taken at a frequency of 10 kHz.
Figure 6-3. Current-voltage (I-V) plot for MgO on u-GaN with a 25 min UV-O₃ and 10 min NH₄OH surface pre-treatment. Breakdown field was 4.02 MV/cm at 1 mA/cm² for a film thickness of 39 nm. Compliance was 100 nA.
Figure 6-4. Capacitance-voltage (C-V) plot for MgO on p-GaN with a 25 min UV-O₃ and 10 min NH₄OH surface pre-treatment. Measurement was taken at a frequency of 10 kHz.
Figure 6-5. Current-voltage (I-V) plot for MgO on u-GaN with a 25 min UV-O₃ and 1 min BOE surface pre-treatment. Breakdown field was 3.69 MV/cm at 1 mA/cm² for a film thickness of 39 nm. Compliance was 100 nA.
Figure 6-6. Capacitance-voltage (C-V) plot for MgO on p-GaN with a 25 min UV-O$_3$ and 1 min BOE surface pre-treatment. Measurement was taken at a frequency of 10 kHz.
Figure 6-7. Current-voltage (I-V) plot for MgO on u-GaN with a 25 min UV-O3 and 10 min in-situ N₂ plasma anneal at 700°C surface pre-treatment. Breakdown field was 3.82 MV/cm at 1 mA/cm² for a film thickness of 39 nm. Compliance was 100 nA.
Figure 6-8. Capacitance-voltage (C-V) plot for MgO on p-GaN with a 25 min UV-O₃ and 10 min in-situ N₂ plasma anneal at 700°C surface pre-treatment. Measurement was taken at a frequency of 10 kHz.
Figure 6-9. Current-voltage (I-V) plot for MgO on u-GaN with four different surface pretreatments. Breakdown field was measured at 1 mA/cm² with a film thickness of 39.0 nm. Compliance was 100 nA.
Figure 6-10. Capacitance-voltage (C-V) plot for MgO on u-GaN with four different surface pre-treatments. Measurements were taken at a frequency of 10 kHz.
Figure 6-11. Current-voltage (I-V) measurements for different ohmic metals on p-GaN. A) Pt/Au (50 nm/80 nm). B) Ni/Au (50 nm/80 nm). Compliance was set at 1 μA for Pt/Au and 100 nA for Ni/Au.
Figure 6-12. Current-voltage (I-V) plot for MgO on p-GaN with a standard surface pre-treatment (3 min HCl:H2O (1:1), 25 min UV-O3, and 5 min BOE). Breakdown field was 4.23 MV/cm at 1 mA/cm$^2$ for a film thickness of 37.6 nm. Compliance was 100 nA.
Figure 6-13. Capacitance-voltage (C-V) plot for MgO on p-GaN with a standard surface pretreatment (3 min HCl:H₂O (1:1), 25 min UV-O₃, and 5 min BOE). Measurement was taken at a frequency of 10 kHz.
Figure 6-14. Current-voltage (I-V) plot for MgO on p-GaN with a 25 min UV-O₃ and 1 min BOE surface pre-treatment. Breakdown field was 3.56 MV/cm at 1 mA/cm² with a film thickness of 37.6 nm. Compliance was 100 nA.
Figure 6-15. Capacitance-voltage (C-V) plot for MgO on p-GaN with a 25 min UV-O₃ and 1 min BOE surface pre-treatment. Measurement was taken at a frequency of 10 kHz.
Figure 6-16. Current-voltage (I-V) plot for MgO on p-GaN with a 25 min UV-O₃ surface pretreatment. Breakdown field was 3.46 MV/cm at 1 mA/cm² with a film thickness of 37.6 nm. Compliance was 100 nA.
Figure 6-17. Capacitance-voltage (C-V) plot for MgO on p-GaN with a 25 min UV-O₃ surface pre-treatment. Measurement was taken at a frequency of 10 kHz.
Figure 6-18. Current-voltage (I-V) plot for MgO on p-GaN with three different surface pre-treatments. Breakdown field was measured at 1 mA/cm² with a film thickness of 37.6 nm. Compliance was 100 nA.
Figure 6-19. Capacitance-voltage (C-V) plot for MgO on p-GaN with three different surface pre-treatments. Measurements were taken at a frequency of 10 kHz.
CHAPTER 7
SUMMARY AND FUTURE WORK

Summary of (Sc₂O₃)ₓ(Ga₂O₃)₁₋ₓ on GaN

Scandium gallium oxide was researched as a candidate dielectric for GaN-based electronic devices. The objective was to deposit the oxide as an amorphous film in a stacked gate dielectric so that it could terminate leakage paths (i.e., dislocations) in the underlying crystalline oxide film. Termination of the leakage paths would enhance the breakdown voltage of the overall stacked gate dielectric while maintaining the properties at the GaN/crystalline oxide interface. Low substrate temperatures and high source temperatures were initially used to drive amorphous film growth. Characterization with RHEED, XRD, and TEM revealed the growth of a fine-grained polycrystalline film under these conditions. Further characterization with Auger showed surface segregation of Ga for the continuous growth technique (all shutters open continuously during the growth). The surface segregation was attributed to the stronger bond between the Sc and O compared to the Ga and O. A digital growth technique (opening of Sc and Ga shutters is alternated while the O is open continuously during the growth) was then employed to eliminate the Ga segregation, but it was unsuccessful. A third growth technique was used which involved closing the Ga shutter for a set amount of time towards the end of the growth while the O and Sc shutters were open continuously. This technique was successful as a uniform film was obtained.

After fabricating MOS capacitors, IV measurements were taken to determine the breakdown field of the oxide film. Initial films (~33 nm) had extremely poor breakdown fields of 0.15 MV/cm at 1 mA/cm². Further analysis with XPS revealed the presence of a Ga metal phase in addition to the Ga₂O₃ and Sc₂O₃ phases. Premature breakdown of the film was attributed to the free Ga metal that was essentially acting as a dopant which made the film conductive. New growth conditions were used to eliminate the free Ga metal by lowering the Ga
cell temperature. As the Ga cell temperature decreased, the breakdown field increased, but the values were still poor as the highest value reached was only 1.40 MV/cm (at 1 mA/cm²). A similar trend has previously been reported for (Ga₂O₃)ₓ(Gd₂O₃)₁₋ₓ on GaAs as the breakdown voltage increased with an increase in the concentration of Gd.\textsuperscript{55,56} The highest breakdown field for that system was achieved for a pure Gd₂O₃ film. The same phenomena is seen for (Sc₂O₃)ₓ(Ga₂O₃)₁₋ₓ on GaN as the highest breakdown field was achieved for a pure Sc₂O₃ film (~2.7 MV/cm at 1 mA/cm²). The addition of Ga to Sc₂O₃ only served to diminish the insulating properties of the film. No further research is recommended for (Sc₂O₃)ₓ(Ga₂O₃)₁₋ₓ on GaN.

**Summary of MgO Growth Optimization**

Previous electrical results for MgO on GaN are very promising as a breakdown field of 4.4 MV/cm (at 1 mA/cm²) and a \(D_{it}\) as low as \(1 \times 10^{11}\) eV\(^{-1}\)cm\(^{-2}\) have been achieved. The disadvantages of MgO are its poor environmental and thermal stability. Its poor environmental stability has made it extremely difficult to process as it can etch in DI water within 10 seconds. Optimization of the film growth was desired to enhance the environmental stability of the film in both water and air. Since the best electrical results have been obtained at low oxygen pressures, new growth conditions (substrate temperature remained at 100°C) included a low oxygen pressure and a low Mg cell temperature to produce a low growth rate. Depositing MgO at a low growth rate was found to significantly enhance its environmental stability. Fabricated MOS capacitors with the optimized growth conditions maintained breakdown field values greater than 3.5 MV/cm (at 1 mA/cm²) after receiving three separate processing wet treatments. The three separate wet treatments included 1 minute in DI water, 3 minutes in AZ 300 MIF developer, and 10 minutes in PG remover. The samples also showed no visible deterioration following their wet treatments. Despite the improved environmental stability, MgO has not shown good thermal
stability at high temperatures. Any high temperature applications will require it to be capped with Sc$_2$O$_3$.

The improved environmental stability of MgO was achieved at an oxygen pressure of 4.5x10^{-6} Torr and a growth rate of ~1.3 nm/min. Previous results showed an increase in the breakdown field and decrease in the Dit as the Mg:O ratio increased with decreasing oxygen pressure. Oxygen pressures lower than 4.5x10^{-6} Torr should be investigated along with lower growth rates to determine if there is any improvement in the electrical results. It will also be critical to maintain a high Mg:O ratio (i.e., 0.68) under these conditions.

Given the lower lattice mismatch for MgO on GaN compared to Sc$_2$O$_3$ on GaN, MgO has shown better electrical results than Sc$_2$O$_3$. Since MgCaO can be perfectly lattice matched to GaN, it is expected that it would have better electrical results than MgO. However, it has shown even worse environmental stability in air and water. Since the growth conditions for MgCaO have not been optimized, new conditions (i.e., low oxygen pressure and low growth rate) should be researched to determine if any improvements can be made to enhance the environmental stability of the film. Results of previous dielectrics (MgO, Gd$_2$O$_3$, and Sc$_2$O$_3$) have been obtained at a substrate temperature of 100°C. Since MgCaO has been primarily deposited at 300°C, growth at 100°C should also be studied for any improvements in the electrical results or stability of the film.

**Summary of Electrical Results for Mg$_x$Sc$_y$O$_z$**

Given the -6.5% lattice mismatch between MgO and GaN and the 9.2% lattice mismatch with Sc$_2$O$_3$, it was hopeful that adding Sc to MgO (to form Mg$_x$Sc$_y$O$_z$) would reduce the lattice mismatch and provide increased stability. Previous research on Mg$_x$Sc$_y$O$_z$ showed improved stability over MgO, but no electrical results were taken. Since MgO showed both good stability
and electrical results at low oxygen pressures and growth rates, Mg$_x$Sc$_y$O$_z$ films were evaluated at these same conditions. Three separate films were grown at increasing Sc cell temperatures (1090°C, 1135°C, and 1180°C) with a constant substrate temperature (100°C), Mg cell temperature (340°C), and oxygen pressure (<5x10$^{-6}$ Torr). All three Mg$_x$Sc$_y$O$_z$ films had breakdown fields greater than 3.5 MV/cm and $D_{it}$ values in the low 10$^{11}$ eV$^{-1}$cm$^{-2}$ range, but they also had flatband voltage shifts of ~3 V or greater. The large flatband voltage shifts were attributed to the different valences of Sc (+3) and Mg (+2) which could generate dangling bonds and defects in the film. Because of the large flatband voltage shift for Mg$_x$Sc$_y$O$_z$, no further studies are recommended for this dielectric.

**Summary of Metallization Study for MgO**

A metallization study was performed in which the feasibility of a new processing scheme was evaluated regarding the deposition of ohmic contacts prior to oxide deposition. The new processing scheme offers numerous advantages such as thorough cleaning of the GaN surface prior to ohmic metal deposition, fewer processing steps the oxide has to undergo, and simultaneous annealing of the ohmic contacts and in-situ cleaning of the GaN surface prior to growth. A variety of surface pre-treatments were evaluated to determine their affect on the ohmic contacts and their effectiveness at cleaning GaN with ohmic pads on the surface. The surface pre-treatments included a 25 min UV-O$_3$ treatment, 25 min UV-O$_3$ and 10 min NH$_4$OH treatment, 25 min UV-O$_3$ and 1 min BOE treatment, and 25 min UV-O$_3$ and 10 min in-situ N$_2$ plasma anneal at 700°C.

All four treatments yielded breakdown fields of ~3.70 MV/cm or greater, $D_{it}$ values around 2.0x10$^{11}$ eV$^{-1}$cm$^{-2}$, flatband voltage shifts of 0.63 V or less, and no damage to the ohmic pads on the GaN surface. Given the small sampling set that was tested, further diodes should be
fabricated and tested to determine which pre-treatment provides the optimal surface to grow on and to look for any observable trends as to which cleaning pre-treatment offers the best starting surface to grow on. The concern of incorporating a new surface pre-treatment in place of the standard pre-treatment was that it would not sufficiently clean the surface, which would result in a higher Dit. All the surface pre-treatments had low Dit values that compared favorably with the value from the standard pre-treatment. However, the values were calculated using the Terman method whose accuracy depends on accurate knowledge of constants and values for the substrate and oxide, graphical differentiation of the \( \phi_s-V_g \) curve, and substrate doping. Closer inspection of the Dit values should be made by taking measurements with more accurate techniques such as the ac conductance method or hi-lo method. Characterization with XPS should also be done to determine the exact nature of the GaN surface following each treatment. An available nitride MBE system that is currently having an XPS/UPS system installed will allow for in-situ monitoring.

The values from the metallization study showed comparable electrical results to the standard surface pre-treatment (3 min HCl:H\(_2\)O, 25 min UV-O\(_3\), and 5 min BOE) that was used in the old processing scheme in which oxide is deposited prior to ohmic metal deposition. These results support the feasibility of the new processing scheme. Further studies should include the optimized MgO growth conditions and incorporation of one of the surface pre-treatments in the fabrication of an e-mode p-GaN MOSFET.

**Summary of Electrical Results for MgO on p-GaN**

Electrical data was obtained from MgO on p-GaN with the use of three different sample pre-treatments. The three sample pre-treatments included a standard treatment (3 min HCl:H\(_2\)O (1:1), 25 min UV-O\(_3\), and 5 min BOE), a 25 min UV-O\(_3\) and 1 min BOE treatment, and a 25 min
UV-O₃ treatment. The latter two treatments were sample pre-treatments that could be used if ohmic metal was deposited prior to sample preparation and oxide deposition. All three samples showed similar electrical results for the breakdown field, flatband voltage shift, and D_it. Since the two surface pre-treatments that would be used with ohmic metal on the surface showed comparable results to the standard surface pre-treatment, it appears that the deposition of ohmic contacts prior to oxide deposition would be a feasible process on p-GaN.

Further analysis of MOS capacitors on p-GaN should be conducted on low doped material to minimize the number of injected carriers, since the use of highly doped material typically requires large gate biases to fully deplete the semiconductor surface of majority carriers. However, a suitable ohmic contact must be found that will remain stable during the 700°C in-situ anneal, and it must provide a low contact resistance to low doped p-GaN. The use of transition metal borides, such as TiB₂ and W₂B, has gained recent attention in ohmic contacts on p-GaN due to their excellent thermal stability and their ability to act as a diffusion barrier in the Ni/Au contact. Reasonable contact resistances were obtained with these transition metal borides at annealing temperatures over 800°C on p-GaN material with a doping density of ~1x10¹⁷ cm⁻³. Further studies should be conducted with p-GaN material having a doping density in the 10¹⁵ cm⁻³ range to determine if minimal contact resistances can be achieved with these transition metal borides. The study should also include 700°C in-situ anneals in the MBE system to investigate the thermal stability of the contact and the effect on the contact resistance.
APPENDIX A
PROCESSING INFORMATION AND DETAILS

Each processing step is critical to the success of the device and overall yield as unwanted defects from a step could lead to premature failure of a device, or poor quality control of one step could lead to problems with the next step. The following sections will include important information related to microlithography as well as more detailed information for the processing steps used in fabricating the MOS capacitors. The information given in the following sections can be found in references 105-107.

**Indium Removal**

Before samples were processed to make diodes, indium (used in mounting the sample to the molybdenum block) was removed from the backside of samples that were going to be annealed in the RTA. This was to prevent indium from possibly contaminating the RTA chamber during the anneal. The first step was to coat the front side (side with oxide) of the sample with photoresist (PR). The sample was then placed in crystal bond on a glass slide (crystal bond is applied to glass slide on a hot plate to create a viscous wax) with the backside of the sample facing up. It is critical to make sure the hot plate is warm enough to melt the crystal bond, but not too warm so that the PR is hard baked to the oxide surface. Once each edge of the sample was covered by the crystal bond, the glass slide was removed and cooled with an N₂ blow gun. A cutip was then soaked with an HCl:H₂O (1:3) solution and applied to the backside of the sample. The combination of rubbing with a cutip and scraping with a razor removed indium from the backside of the sample. After the indium was removed, the glass slide was placed back on the hot plate to melt the crystal bond and allow for the removal of the sample. As soon as the sample was removed, it was placed in acetone to lift off the PR and crystal bond. After the acetone completely removed the PR and crystal bond, the sample was rinsed in isopropanol (15–
30 sec) followed by deionized (DI) water (15–30 sec). The sample was then dried with an N2 blow gun. Before resist was spun on the sample to be patterned, further cleaning of the sample surface was required.

**Surface Preparation**

The primary reasons for cleaning the sample prior to coating it with resist are to enhance the wetting and adhesion of the PR to the surface (critical for developing and etching) and to avoid the formation of pinholes in the PR. The surface tension of the PR must be less than the surface tension of the substrate for wetting to occur. The degree of wettability is given in Equation A-1:

\[ \gamma_{sv} = \gamma_{sl} + \gamma_{lv}\cos\theta \]  

(A-1)

where \( \gamma_{sv} \) (in dynes/cm) is the interfacial energy of the solid-vapor interface, \( \gamma_{sl} \) (in dynes/cm) is the interfacial energy of the solid-liquid interface, \( \gamma_{lv} \) (in dynes/cm) is the interfacial energy of the liquid-vapor interface, and \( \theta \) is the contact angle. Generally, a contact angle less than 90° produces a wettable surface and a contact angle greater than 90° leads to a non-wettable surface (Figure A-1). Although a low contact angle and high surface energy are desirable for wetting, they also produce a hydrophilic surface that is attractive for adsorption of water. Water adsorbed on the surface can lead to poor adhesion of PR to the underlying substrate which could cause lift off during the etch process, undercutting at window edges, or complete loss of small features. In cases of poor adhesion to the surface, the surface can be primed with a silane compound (ex. hexamethyldisilazane-HMDS) which will lower the surface tension of the substrate to match the surface tension of the resist and make the surface hydrophobic.

Typical contaminants that must be removed prior to resist coating include dust particles (in any room or from cleaving sample), metal particles from metal lift-off, residual PR from
previous lithography processes, and solvent or water residue. The process that was used to clean the surface of the samples included the following steps: 1) 3 min soak in acetone with ultrasonic agitation 2) 3 min soak in methanol with ultrasonic agitation 3) 3 min soak in DI water with ultrasonic agitation 4) Blow dry with N\textsubscript{2} gun 5) 125 °C bake on hot plate for 5 min to drive off most of the adsorbed water 6) Cool sample with N\textsubscript{2} blow gun. As soon as the cleaning process was completed, PR was spun onto the sample as quickly as possible to minimize the amount of time for water adsorption.

**Photoresist**

Shipley S1818 (positive resist which develops upon exposure to light) was used to coat all of the samples. It was stored in a refrigerator to extend the life time of the resist as bacterial growth can lead to aging of PR. Before samples were coated, a 20 mL amber bottle containing 1818 was wrapped up in aluminum foil (to prevent possible exposure to UV light) and given 30 minutes to come to room temperature. The final two numbers of the resist indicate the typical thickness that can be spun, which in this case would be 1.8 \( \mu \text{m} \). The use of a thicker resist made metal lift-off easier and reduced the number of pinholes. Although the resolution is lower for thicker resists, it was not an issue in fabricating the MOS capacitors since the feature sizes were so large. Since resist performance (ex. thickness, exposure time, develop time) can change as the PR ages, quality control checks were performed every few months to look for any noticeable changes.

**Surface Coating**

After receiving a thorough cleaning treatment, samples were placed on top of a small opening in the vacuum chuck of the Laurell spinner. The opening allowed an applied vacuum to draw the sample into intimate contact with the vacuum chuck. The desired program was then
selected on the keypad next to the spinner. The program contained two steps, with the first step involving a low spin speed (1000 rpm) for dispensing the resist, and the second step involving a higher spin speed (5000 rpm) to reach the desired thickness of the resist. The application of dispensing the resist at a lower spin speed allowed the resist to spread across the sample before stepping to the higher spin speed. It is critical to step to the final spin speed as soon as the resist is dispensed, so that the amount of solvent evaporation (increased solvent evaporation produces a thicker film of PR) is minimized.

A plastic syringe was used to dispense the resist to the spinning sample. Since the amount of pressure used to dispense the resist is chosen depending on the resist viscosity and surface energy of the sample, a higher pressure is typically used for low energy surfaces and/or high viscosity resists. The higher pressure is used to provide the resist enough force to completely wet the surface. After spinning the sample at 5000 RPM for 30 sec, the samples were removed from the vacuum chuck for a soft bake. Profilometer measurements taken following the soft bake (i.e., 125 °C for 1.5–2.0 minutes) showed that a spin speed of 5000 rpm for 30 seconds yielded a thickness of 2.0–2.2 μm.

## Factors Affecting Resist Thickness

The primary factors that affect the thickness of the resist are the viscosity of the PR and the spin speed. As seen in Equation A-2, the thickness increases for slower spin speeds and higher viscosities:

\[
t = \frac{\eta}{t^* \omega^{0.5}}
\]  

(A-2)

where \( t \) (in \( \mu m \)) is the thickness of the resist, \( \eta \) (in cP) is the viscosity of the resist, \( t^* \) (in seconds) is the spreading time which is usually on the order of seconds, and \( \omega \) (in rpm) is the spin speed.

Figure A1-2 displays a spin speed curve for Shipley 1818 PR that was coated on Si at various
spin speeds (3000, 4000, 5000, and 6000 rpm) to determine the thickness of the resist. Other factors that can influence the final resist thickness include humidity, atmospheric pressure, temperature (resist, chuck, wafer, ambient environment, and soft bake), acceleration, and air flow. Their affect on the resist thickness along with other factors mentioned earlier is shown in Table A-1.

**Acceleration**

An acceleration rate of 1000–1500 rpm/sec was used in transitioning from the dispense speed to the final spin speed. Further optimization of the acceleration rate is needed as it can affect film uniformity and the number of spin-induced defects. Film uniformity generally increases as acceleration is increased, but spin-induced defects are generated at high acceleration rates (i.e., 20000 rpm/sec). High acceleration rates can produce a greater concentration of atomized resist particles (can be minimized with a suitable exhaust) that can re-deposit on the sample surface. Particles that re-deposit on the surface as a spherical shape are usually dry or low in solvent and will block UV light. This creates an island of resist pattern where one should not be present after development. Particles that re-deposit on the surface as half domes (also known as color spots or fish eyes) are rich in solvent and will focus the UV light. This leads to partial development and a crater shaped pattern defect. Since low acceleration rates can also induce defects, there is a narrow operating range that must be found which will produce a resist film of uniform thickness and low defect concentration.

**Spin Defects and Artifacts**

Although acceleration is the main spin defect contributor, other factors can produce defects as well. Some of the factors include surface or resist contamination, air bubbles in the dispensed resist, and very high spin speeds (aerosol particles are generated if a wafer is spun too fast). Contaminants on the surface and particles or air in the resist are common sources of pinholes.
Pinholes pose serious problems as unwanted etching or metal deposition (in later processing steps) can occur through tiny holes in the resist. Some of the methods to reduce the pinhole density include using a thick resist, using a double coat resist process (rely on mismatch of pinholes in each layer), and thorough cleaning of the sample surface.

Striations (radial stripes) or colored bands in the resist are indicative of thickness variations that are primarily due to non-uniform drying of the solvent during the final spin step. Therefore, the spin time must be chosen carefully to allow the solvent concentration enough time to decrease uniformly across the sample. Surface contamination can also cause striations to form due to poor wetting and adhesion. For thick coatings (>2 μm), a recommended technique to reduce the striations includes allowing the resist to sit on the surface for a set time before spinning (ex. 15 seconds for 2 μm thick resist). This technique was not used for any of the sample coatings, but it should be studied in future processing optimization analyses. Another method that can be used to minimize the striations is to make sure the resist is dispensed at the center of the sample and not at multiple locations.

Since the radial velocity is greatest at the edge of the sample, the solvent evaporates there more quickly, producing a thicker amount of resist at the edges. This residual ridge in the resist is known as the edge bead. A recommended method to remove the edge bead is to use an EBR (edge bead removal) solvent that partially dissolves the edge bead away after being spun onto the sample following resist coating. However, this method was not used so that the number of processing steps could be minimized. Any effects the edge bead could have on the exposure or developer times was removed by making sure that only the center of the sample (where the resist thickness was more uniform) was exposed to the pattern. All other types of spin defects and artifacts are included in Table A-2.
Soft Bake

Although the spin coating removes the majority of the solvent (80-90%) from the resist, a soft bake is required to evaporate the residual spinning solvent and densify the resist. If the excess solvent is not removed from the resist, it can make the required exposure dose for pattern transfer unpredictable. Incomplete removal of solvent can also leave the resist tacky, making the sample stick to the mask during pattern alignment and making it more susceptible to particulate contamination. Besides its use to primarily drive out the remaining solvent from the resist film, the soft bake is used for removing internal stresses in the resist, closing voids and/or pinholes, and enhancing the adhesion between the sample surface and resist.

The soft bake step was performed using a Thermolyne hot plate. A hot plate was used since convection ovens can lead to trapping of the solvent in the resist. Entrapped solvent can then form micro bubbles that become pinholes (popped bubbles) during further drying of the PR. Using a hot plate allowed the solvent to outgas before the surface of the resist hardened.

Finding the suitable soft bake temperature and time is critical in determining reproducible exposure and develop times. If the soft bake temperature is too high, the photosensitive component may become partially degraded, requiring a higher exposure dose or longer exposure time. A high soft bake temperature with a short bake time can also lead to the formation of pinholes as the solvent is not given sufficient time to outgas. If the soft bake temperature is too low, the remaining solvent may interfere with the radiation chemistry and development rates (exposed and unexposed areas will dissolve equally), requiring different exposure-development combinations. It is also critical to find soft bake conditions that provide reproducible dissolution rates for the exposed and unexposed regions of the resist. After performing numerous processing
optimization experiments, it was found that a soft bake temperature of 125 °C for a time of 1.5–2 minutes produced the most reproducible exposure and development times.

**Exposure**

After receiving a soft bake, each sample was placed on a 2” Si alignment wafer (held in place by vacuum) which was inserted on top of the sample stage of the mask aligner. Channel 1, corresponding to 365 nm wavelength light, was selected on the constant intensity controller. The exposure dose (in mW/cm²) of the aligner was fixed, so only the exposure time could be varied. The exposure time was initially calibrated by using samples of as-received Si and GaN. The calibrated exposure time was then checked and finalized by using a GaN sample with MBE deposited oxide (each oxide is calibrated). Since different surfaces reflect different fractions of light, the oxide on GaN sample provided the most ideal case for the exposure.

The reflected light at the substrate/resist interface can interfere with the transmitted light from the optical source of the mask aligner to form standing waves. Standing waves produce two undesirable effects with the first one being undesirable horizontal ridges (reflective notching) in the resist sidewalls that correspond to peaks and troughs in the standing wave intensity. The second effect is that standing waves affect the total amount of light captured by the resist. Since the amount of light absorbed by the resist changes dramatically with a slight change in resist thickness, the exposure dose or time is highly sensitive to changes in resist thickness. This results in a swing curve which is a sinusoidal variation of the exposure dose ($E_o$) for varying resist thicknesses. The curves are generated by interference between incoming and outgoing light waves due to a phase difference between them. The swing between the maximum (where destructive interference occurs) and minimum (where constructive interference occurs)
points on the curve is represented by a thickness change of $\lambda/4n$, where $\lambda$ is the exposure wavelength (in nm) and $n$ is the index of refraction of the resist.

There are multiple methods that can be used to reduce the effects of standing waves. One of the methods includes a post exposure bake to reduce or eliminate the horizontal ridges in the resist sidewalls created by the standing waves. However, a post exposure bake will not work to reduce the swing curves. Dyed resists or antireflective coatings (ARC) are recommended for reducing swing curves. Dyed resists utilize a higher optical density to suppress the reflection of light, but too much opacity can reduce the exposure at the bottom of the resist. An ARC is a thin layer of opaque organic material or heavily dyed polymer that is coated on the substrate surface underneath the resist layer. The ARC has a high enough optical absorption to separate the resist from the optical behavior of the substrate by absorbing the reflected light. To avoid adding any complexity to the fabrication process, none of these methods were used to process the samples. Instead of reducing the standing waves, a maximum point on the swing curve was targeted to counter any changes in the resist thickness and prevent any occurrences of underexposure, which can lead to scumming of the resist.

**Development**

Rohm and Haas MF 319 developer or AZ 300 MIF developer (both are metal-ion free) were used to develop the exposed samples. The develop time is a strong function of the exposure dose or time, so any exposure changes will lead to changes in the development time. The development time was generally 30–60 seconds. The amount of time was determined by monitoring the dissolution of the resist in the solution. As the resist was dissolving, a dark cloud would form above the sample. Agitation was used to increase the development rate (kinetics of development are mass transport limited) and remove the dissolved resist (dark cloud) away from
the sample since resist can re-deposit in the features under static development. Once the dark cloud dissipated, the sample was removed from the solution, rinsed in water, and then dried with an N₂ blow gun. The developed features on the sample were then analyzed under a microscope with filtered light to look for any features that had not fully developed.

The profiles of the features are heavily dependent on the combination of the exposure and develop times. Overcut profiles are indicative of overexposure due to reflected exposure rays, and undercut profiles are indicative of overdevelopment due to partial removal of unexposed resist (Figure A-3). The development rate depends on the soft bake conditions, developer temperature, solution agitation, and concentration or type of developer. Causes of insufficient development include use of a high soft bake temperature, weakened developer solution, incorrect exposure dose or time, or incorrect development time.

**Hard Bake**

Following development of the patterned sample, it can be given a hard bake to remove the developer, moisture, and any remaining solvent (complete removal of casting solvent can only be accomplished by baking the resist above its Tₘ). This helps to improve the adhesion of the resist to the substrate for further processing steps such as wet or dry etching. Determining what hard bake conditions to use depends on factors such as the resist thickness, exposure dose, type of resist and developer, etchant and conditions, image profile, and subsequent processing steps (PR removal, volatility, temperature). Since longer and hotter hard bake conditions can make residual PR difficult to remove, a hard bake of 110°C for 60 sec on a Thermolyne hot plate was used. Samples were not given a hard bake when the next processing step was metallization (i.e. metal sputtering) since a soft resist was desired for metal lift-off.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Resist Thickness</th>
<th>Reason</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPM increases</td>
<td>Decreases</td>
<td>Centrifugal force thins the resist as more resist is spun off the substrate</td>
</tr>
<tr>
<td>Viscosity increases</td>
<td>Increases</td>
<td>Less resist is spun off the substrate due to its slower molecular movement, and there is a lower concentration of solvent to evaporate</td>
</tr>
<tr>
<td>Resist temperature increases</td>
<td>Increases</td>
<td>Rate of solvent evaporation increases with an increase in temperature</td>
</tr>
<tr>
<td>Humidity increases</td>
<td>Decreases</td>
<td>Amount of solvent evaporation decreases due to a lower exchange of spinning solvent molecules in an environment abundant with H₂O</td>
</tr>
<tr>
<td>Airflow increases</td>
<td>Increases</td>
<td>Rate of solvent evaporation increases</td>
</tr>
<tr>
<td>Atmospheric (barometric)</td>
<td>Increases</td>
<td>Greater solvent volatility at lower pressures accelerates the rate of evaporation</td>
</tr>
<tr>
<td>pressure decreases</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Acceleration increases</td>
<td>Decreases</td>
<td>Centrifugal force thins the resist as more resist is spun off the substrate</td>
</tr>
<tr>
<td>Soft bake temperature increases</td>
<td>Increases</td>
<td>Rate of solvent evaporation increases</td>
</tr>
</tbody>
</table>
Table A-2. Causes of spin-induced defects or artifacts.

<table>
<thead>
<tr>
<th>Spin Defect or Artifact</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cloudy film</td>
<td>Excess moisture</td>
</tr>
<tr>
<td>Comets</td>
<td>Bubbles or particles from resist dispense</td>
</tr>
<tr>
<td>Swirls</td>
<td>Volatile solvent</td>
</tr>
<tr>
<td>Pinholes</td>
<td>Surface contamination; air or particles in resist</td>
</tr>
<tr>
<td>Striations</td>
<td>Surface contamination; non-uniform solvent drying; dispense at multiple locations</td>
</tr>
</tbody>
</table>
Figure A-1. Diagrams of wetting vs. contact angle. A) Wetting occurs for low contact angle ($\theta$).
B) Non-wetting occurs for high contact angle ($\theta$).
Figure A-2. Resist thickness vs. spin speed for Shipley 1818 PR.
Figure A-3. Sidewall profiles of photoresist features. A) Undercut profile from overexposure. B) Overcut profile from overdevelopment.
APPENDIX B
CV CURVES AND MEASUREMENTS

CV Curves

The measured capacitance of a MOS capacitor consists of two capacitors in series. The two capacitors include a voltage-independent gate oxide capacitor and a voltage-dependent semiconductor capacitor. In accumulation, the series capacitance is represented by the oxide capacitance shown in Equation B-1:

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_o}{t_{ox}}$$  \hspace{1cm} (B-1)

where $C_{ox}$ is the capacitor of the oxide (measured in F/cm$^2$), $\varepsilon_{ox}$ is the dielectric constant of the oxide, $\varepsilon_o$ is the permittivity of free space ($8.854 \times 10^{-14}$ F/cm), and $t_{ox}$ is the thickness of the oxide film (measured in cm).

In depletion, the semiconductor surface becomes depleted of majority carriers under the applied gate bias (holes are depleted in p-type material with increasing gate voltage and electrons are depleted in n-type material with decreasing gate voltage), causing a decrease in the measured capacitance. The overall capacitance is now represented by the series connection of the oxide capacitance ($C_{ox}$) and depletion layer capacitance ($C_d$) seen in Equation B-2:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d}$$ \hspace{1cm} (B-2)

Under strong inversion, minority carriers are generated in the bulk and then drift across the depletion region to form a surface layer of charge. However, this will only occur if a low (~1–100 Hz) frequency is applied and if the gate bias is changed slowly. The low frequency and slow changing gate bias allow the minority carriers enough time to respond to the ac probe frequency.
and dc voltage signal. The overall capacitance is now represented by the oxide capacitance once again (Figure B-1a).

For high (~1 MHz) frequency measurements at slow changing gate biases, the minority carrier generation rate is too low as the minority carriers do not have enough time to respond to the ac voltage signal. The semiconductor depletion layer capacitance is now at a minimum, corresponding to a maximum depletion width. The overall measured capacitance is also at a minimum and is represented by the series capacitance of the oxide and semiconductor depletion layer (Figures B-1b and B-2). For high or low frequency measurements at a large gate bias sweep rate, the generation rate of minority carriers is too low and the measured capacitance can go into deep depletion (Figure B-1c).

**Dit Calculations**

The frequency and gate bias sweep rate can have a significant effect on the response of interface states at the oxide/semiconductor interface. As the applied gate bias changes, the surface potential of the MOS device changes, which causes the interface states (whose positions with respect to the band edges are fixed) in the bandgap to move above or below the Fermi level. Since energy levels below the Fermi level have a higher probability of occupying an electron, an interface state moving above the Fermi level would likely give up a trapped electron (or equivalently capture a hole) while an interface state moving below the Fermi level would likely capture an electron (or give up a hole). The stored charge from the interface states gives rise to a capacitance which is in series with the depletion layer capacitor (the combination of the two would be in series with the oxide capacitance). At very high (~1 MHz) frequencies, the interface states do not have time to respond. At low (~1–100 Hz) frequencies and/or low gate bias sweep rates, the interface states can respond quickly to the voltage changes and follow the ac probe frequency.
The Terman method was used to calculate the $D_{it}$ value from the measured CV data. The method relies on measurements taken at sufficiently high frequencies in which interface traps do not respond. Although the interface traps do not respond to the ac probe frequency, they do respond to slow gate bias sweep rates. As the interface trap occupancy changes with gate bias, the CV curve stretches out along the gate axis (change in slope of real CV curve from ideal curve in Figure B-3 indicates the presence of interface traps). To determine the $D_{it}$, a theoretical CV curve must be constructed and compared to the experimental curve.

The total theoretical capacitance is given by the series capacitance of the oxide and semiconductor. To calculate the theoretical semiconductor capacitance ($C_{s}$), the semiconductor flatband capacitance ($C_{FBS}$) is calculated from Equation B-3:

$$C_{FBS} = \frac{\varepsilon_s \varepsilon_o}{L_D}$$  \hspace{1cm} (B-3)$$

where $C_{FBS}$ is the semiconductor flatband capacitance (in F/cm²), $\varepsilon_s$ is the dielectric constant of GaN (5.3 at high frequencies), $\varepsilon_o$ is the permittivity of free space (8.854x10^{-14} F/cm), and $L_D$ is the Debye length (in cm). The Debye length is calculated from Equation B-4:

$$L_D = \sqrt{\frac{k_B T \varepsilon_s \varepsilon_o}{q^2 N}}$$  \hspace{1cm} (B-4)$$

where $L_D$ is the Debye length (in cm), $k_B$ is Boltzmann’s constant (1.38x10^{-23} J/k), $T$ is the temperature (in K), $\varepsilon_s$ is the dielectric constant of GaN (5.3 at high frequencies), $\varepsilon_o$ is the permittivity of free space (8.854x10^{-14} F/cm), $q$ is the hole or electron charge (1.6x10^{-19} C), and $N$ is the effective carrier density (in cm$^3$). The effective carrier density can be calculated from Equation B-5:

$$N = \frac{2}{q \varepsilon_s \varepsilon_o A^2} \left[ \frac{1}{\partial(1/C^2)/\partial V} \right]$$  \hspace{1cm} (B-5)$$
where $N$ is the effective carrier density (in cm$^{-3}$), $\varepsilon_s$ is the dielectric constant of GaN (5.3 at high frequencies), $\varepsilon_0$ is the permittivity of free space (8.854x10$^{-14}$ F/cm), $q$ is the hole or electron charge (1.6x10$^{-19}$ C), $A$ is the area of metal gate (in cm), and $\partial (1/C^2)/\partial V$ is the slope of the experimental $1/C^2$ vs. $V_g$ plot.

After calculating the flatband capacitance of the semiconductor, the theoretical semiconductor capacitance can be calculated from Equation B-6:\textsuperscript{108}

$$C_s = 2^{-0.5} \text{Sgn}(V) C_{FB} (e^V - 1) \left[ - (V + 1) + e^V \right]^{0.5}$$  \hspace{1cm} (B-6)

where $C_s$ is the semiconductor capacitance in (F/cm$^2$); $V$ is the non-dimensional band bending (in V); $\text{Sgn}(V)$ returns a value of 1 for positive values of $V$, 0 for a value of 0 for $V$, and -1 for negative values of $V$; and $C_{FB}$ is semiconductor flatband capacitance (in F/cm$^2$). The non-dimensional band bending is used in Equation B-7 to calculate the surface potential:

$$\phi_s = \frac{k_B V T}{q}$$  \hspace{1cm} (B-7)

where $\phi_s$ is the surface potential (in eV), $k_B$ is Boltzmann’s constant (8.62x10$^{-5}$ eV/K), $V$ is the non-dimensional band bending (in V), $T$ is the temperature (in K), and $q$ is the hole or electron charge (1.6x10$^{-19}$ C).

After constructing the theoretical curve by plotting the theoretical total capacitance vs. the surface potential, a surface potential value is found for a given capacitance value. The gate voltage from the experimental curve is then found for the same capacitance value. Repeating the procedure for other points allows an $\phi_s$ vs. $V_g$ curve to be constructed. The $D_n$ can be determined from this curve using Equation B-8:

$$D_n = \frac{C_{ox}}{q} \left[ \frac{\partial V_g}{\partial \phi_s} - 1 \right] - \frac{C_s}{q}$$  \hspace{1cm} (B-8)
where \( D_{it} \) is the interface state density (in \( \text{eV}^{-1}\text{cm}^{-2} \)), \( C_{ox} \) is the oxide capacitance (in \( \text{F/m}^2 \)), \( q \) is the hole or electron charge (1.6x10^{-19} \text{C}) , \( V_G \) is the gate bias (in \text{V}), \( \phi_s \) is the surface potential (in \text{eV}), and \( C_s \) is the surface capacitance (in \( \text{F/m}^2 \)).

**V\textsubscript{FB} Determination**

For an ideal MOS capacitor, the metal and semiconductor work functions are equal at a gate bias of 0 V. However, in a real MOS capacitor, there is typically a metal-semiconductor work function (\( \Phi_{ms} \)) difference and oxide and interface charges that produce a flatband voltage (\( V_{FB} \)) shift (parallel shift of real plot from ideal plot is seen in Figure B-3). The flatband voltage is the voltage required to achieve the flat band condition where the energy bands are flat. A negative flatband voltage shift indicates a positive oxide charge that induces an equivalent negative charge in the semiconductor. A positive flatband voltage shift indicates a negative oxide charge that induces an equivalent positive charge in the semiconductor.

To determine the flatband voltage shift, the theoretical CV curve must be compared to the experimental CV curve. The first step is to locate the normalized theoretical capacitance (\( C/C_{ox} \)) at a gate bias of 0 V. The same value is then located on the normalized experimental capacitance curve with the corresponding gate bias value. This gate bias value represents the flatband voltage of the MOS capacitor. Another method that can be used to determine the flatband voltage shift experimentally includes plotting \( (1/C_{ht})^2 \) vs. \( V_G \). The gate bias at the lower knee of the curve represents the flatband voltage.
Figure B-3. Illustration of ideal and real CV plots. Shift in real curve indicates flatband voltage shift, and change in slope of real curve indicates interface traps. [Reprinted with permission from B.P. Gila, 2000. Growth and Characterization of Dielectric Materials for Wide Bandgap Semiconductors. PhD dissertation (pg. 132, Figure A1-5). University of Florida, Gainesville, Florida.]


BIOGRAPHICAL SKETCH

Mark Steven Hlad was born in Great Falls, Montana, and moved to Lynn Haven, Florida, after only a few months old. He is the son of Dennis and Jan Hlad and brother to Paul Hlad. After graduating from Mosley High School in 1998, he attended Gulf Coast Community College for a couple years before attending the University of Florida in 2000. He received his bachelor’s degree in chemical engineering in 2003 and had the opportunity during that time to perform undergraduate research studies with Dr. Omar Bchir on WNₓ thin films as diffusion barriers for copper metallization. He then began to pursue a doctoral degree in materials science and engineering in the summer of 2003 under Dr. Cammy Abernathy with research on gate dielectrics (grown by MBE) on GaN MOSFETs. He completed his philosophy of doctorate in the summer of 2007 in materials science and engineering. Post graduation plans include a job as a packaging engineer with Intel Corporation in Chandler, Arizona.