FULLY INTEGRATED CMOS RECEIVER FOR A 24-GHZ SINGLE CHIP RADIO-MICRONODE

By

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2009

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To my parents and my wife
ACKNOWLEDGMENTS

I would like to begin by thanking my advisor, Professor Kenneth K. O, whose constant encouragement and patient guidance provided a clear path for my research. His great vision led to success of our project. I would like to thank Dr. Robert M. Fox for his guidance in my baseband analog circuits design. I would also like to thank Dr. Khai Ngo and Dr. Gloria J. Wiens for helpful suggestions and their time commitment in serving on my committee.

Much appreciation goes to Defense Advanced Research Projects Agency (DARPA) for funding this work. My special thanks go to Albert Yen at UMC Inc. and Geoff Dawe at Bitwave Semiconductor Inc. for chip fabrication. Also I would like to thank Dr. Jenshan Lin for the use of his group’s measurement equipments. Much appreciation goes to my former TI colleagues, Siraj Akhtar and Chih-Ming Hung for their encouragement and help to finish this dissertation.

I have been quite fortunate to have worked with my colleagues in the μNode project, Changhua Cao, Yanping Ding, and Jau-Jr Lin, whose helpful discussions, recommendations and friendship have speeded up my research. I fondly remember the “crazy” times during tapeouts, struggles and excitements during measurements. It is a great 4-year period to work with them. I wish them best in their future career and I believe they will achieve great success. Li Gao, her elder-sister-style made me get quickly adapted to the new environment when I joined the SIMICS research group. Also, I would like to thank the other former and current colleagues in SIMICS group for their helpful advice and discussions. Some names are listed here: Seong-Mo Yim, Dong-Jun Yang, Zhenbiao Li, Xiaoling Guo, Ran Li, Haifeng Xu, and Chikuang Yu. Aravind. Sugavanam, Jie Chen, Eunyoung Seok, Kwangchun Jung, Swaminathan Sankaran, Chuying Mao, Seon-Ho Hwang, Ning Zhang, Shashank, Myoung Hwang, Wuttichai Levdensitboon, Zhe Wang, Dongha Shim and Kyujin Oh. I also like to thank my friends outside
of the research group. Ashok K. Verma and Xiuge Yang also worked with us on the μNode project. Ming He and Xiaoxiang Gong shared the same passion with me for Gator basketball and football. Tao Zhang, Qizhang Yin, Xiaoqing Zhou and Xueqing Wang had nice BBQ parties with us. Yanming Xiao and Changzhi Li helped me a lot on using measurement equipment.

I am grateful to my parents for their love and encouragement since childhood. I would like to thank my wife, Cuiwei Wang. Her unconditional support and care enabled me to focus on research work over the long period of time. Finally, I would like to thank my two lovely daughters, ShiYing Su and XinYan Su for happiness and joy they bring to me.
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The speed improvement of silicon devices has made implementation of silicon integrated circuits operating at 10GHz and higher feasible. This trend has made it possible to integrate a single chip radio using on-chip antennas. This had led to the proposal of a 24-GHz true single chip CMOS radio. This Ph.D work demonstrated a fully integrated receiver chain, and a transceiver incorporating the receiver, transmitter designed by C. Cao and the frequency synthesizer designed by Y. Ding.

Single-ended and differential LNAs operating at 24GHz have been demonstrated. With 1.2-V supply, the single-ended LNA has 6-dB gain and 5-dB noise figure consuming 2.3-mW power. The differential LNA has 6-dB gain and ~5.3-dB while consuming 4-mW power. From these, it is found that substrate resistance and parasitic capacitance of CMOS devices significantly degrade the gain and power efficiency of LNA. By adding an inductor at the gate of common gate stage of a cascode amplifier, negative resistance can be generated to increase the output impedance and transconductance of LNA. A 26-GHz LNA using this topology achieves 8.4-dB gain and ~5-dB noise figure while only consuming 0.8-mW power.

A 20-GHz RF front-ended including an LNA and a mixer is demonstrated. It achieves 9-dB conversion gain and 6.6-dB noise figure. This RF front-end only consumes 12.8-mW power from a 1.5-V supply. Using this RF front-end with an on-chip antenna as a receiver, AM signal
transmitted by an on-chip antenna 5m away has been successfully picked up and down-converted to intermediate frequency (IF). For the first time, this demonstrated the feasibility of a pair of ICs communicating with each other over free space using on-chip antennas. To increase receiver gain, an IF amplifier is added to the RF front-end. It achieves 29.5-dB gain consuming 17.7-mW power from a 1.5-V supply. These results showed that it is feasible to implement low power 24-GHz communication devices with reasonable performance using a 130-nm CMOS technology.

A fully integrated receiver is demonstrated. It consists of an RF front-end, IF amplifier, passive mixer, variable gain amplifier (VGA) and lower pass filter (LPF). It utilizes dual down conversion which requires one 21.3-GHz frequency synthesizer and a divide-by-8 circuit to generate the second local oscillator signal. A distributed transmitter/receiver switch is used to share the use of one on-chip antenna by the receiver and transmitter. A wireless communication link is demonstrated using fully integrated receiver and transmitter. A ~21.7-GHz single tone generated by the transmitter is successfully picked up and down-converted to baseband by the receiver which is 5m away from the transmitter. This demonstration is a great step toward the realization of a single chip radio.
CHAPTER 1
INTRODUCTION

1.1 Low Power Wireless Network

The rapid evolution of wireless communications technology has resulted in a strong drive toward implementation of high-performance radio frequency (RF) circuits in silicon, particularly Complementary Metal-Oxide-Semiconductor (CMOS), for its lower cost and higher level of integration. With low cost and low power advantage of CMOS, RF products incorporating the standards for cellular phone and ultra wide band standard, as well as Bluetooth and 802.11x for wireless local area network (WLAN) applications are being developed and deployed.

It is now widely acknowledged that these standards are not well suited for a wide range of sensor network applications due to the high cost of nodes as well as the high power consumption resulting from complex protocols. To address this, a standard called ZigBee [1] is proposed. Its main goal is to standardize and enable inter-operability of products within a home or a building. The ZigBee standard builds on the physical communication layers specified by the IEEE 802.15.4 standard [2]. The ZigBee defines the network, security and application software. Zigbee networks operate in the 2.4-GHz Industrial-Scientific-Medical (ISM) band, the same band as 802.11b WLAN networks, Bluetooth and others.

ZigBee networks better address the unique needs of sensors and control devices. Sensors and controls do not need high bandwidth. However, they do need low latency and very low energy consumption for long battery life. The devices are idle for most time. The network supports data transmission rates up to 250kbps at a range of up to 30 meters. This data rate is lower than the 802.11b WLAN (11 Mbps) and Bluetooth (1 Mbps) devices, but the power consumption of Zigbee devices is significantly lower. Users can expect batteries to last many months or even years.
1.2 On-Chip Antenna

For the low power wireless network applications, it is possible to implement a single chip radio which packages both baseband electronics and radio in a single chip [3]. To totally eliminate the potentially costly external transmission line connections, integration of antennas is desirable if their performance is adequate. The research on fabrication of antennas on semi-conducting substrate goes back to the late 1980’s. These early efforts included an on-chip antenna integrated with a 95-GHz IMPATT diode oscillator on a high resistive silicon substrate [4] and an on-chip antenna integrated with a 43.4-GHz IMPATT diode oscillator on a GaAs substrate [5]. High resistive silicon substrates have also been used to fabricate MEMS based antennas operating at 90 to 802GHz [6]. However, the use of IMPATT diode circuits limits the types of radios that can be built. Furthermore, the substrates are not compatible with the low cost mainstream silicon process technologies. The speed improvement of silicon devices has made implementation of silicon integrated circuits operating at 10GHz and higher feasible. At 10GHz, a quarter wave dipole antenna needs to be only 7.5 and ~2.2 mm in free space and silicon, respectively, making integration of an antenna for wireless communication possible.

On-chip antennas could potentially be used to relieve the bottleneck associated with global signal distribution inside integrated circuits. The first proposed uses of an on-chip antenna fabricated in a conventional foundry process are clock distribution [7] and data communication [8], [9]. Several transmitters [10], [11] and receivers [11] with on-chip antennas for wireless clock distribution have been demonstrated. Signal from a transmitter incorporating a 10-GHz VCO, buffer and antenna fabricated in a BiCMOS technology [15] has also been picked up by an external horn antenna. Recently, a clock transmitter [16] and receiver [17] using 2-mm on-chip zigzag antennas for clock distribution have achieved 5-ps peak-peak jitter. These suggested the
potential to communicate over free space using true single chip CMOS and BiCMOS radios with on-chip antennas.

Having the ability to form antennas on-chip with almost no cost penalty provides greater design flexibility. It is no longer necessary to force the antenna interface to be at 50Ω and share the transmitting and receiving antennas. Each interface could be independently optimized. The receiving antenna can be made to have impedance higher than 50Ω which gives better noise performance. The impedance of transmitting antenna can be made lower than 50Ω, releasing the high Q requirement of matching network which can reduce the output signal swing at given output power. Especially in a class E power amplifier, the lower voltage swing reduces the voltage stress on devices. Using passive on-chip components in combination with the freedom to choose impedance level should allow integration of tunable bandpass filters with the relax performance requirements.

1.3 \( \mu \)Node System

Exploiting this new possibility, a sensor node called \( \mu \)Node, which incorporates on-chip antennas, a transceiver, a digital baseband processor, a sensor, and potentially even a battery, has been proposed [18].

Figure 1-1 shows the conceptual diagram of a \( \mu \)Node. It is capable of 100kbps wireless transmission and reception at \( \sim 24\)GHz over a short distance (typically 1 to 5 meters, and the range can be extended to \( \sim 30\)m at the cost of increased transmit power). Groups of \( \mu \)Nodes can form self-organizing wireless communication networks that signal in a wide frequency band (100MHz) at amplitude below the background noise level. Such nodes could help to accelerate the realization of Smart Dust vision [19].
The μNode packaging has the potential of being very simple. The SoC CMOS chip communicates off-chip via wireless signaling. The only wire connections are battery connections. A μNode package only needs to provide mechanical and chemical protection, while allowing RF signal transmission. In contrast, a device with an off-chip antenna must have a package providing well-controlled impedance connection to external passive components including an antenna. Since μNodes are operating at ~24GHz, all the passive components can be easily integrated on-chip. A μNode network can be viewed as a modified Zigbee network operating at 24GHz.

Figure 1-1. A conceptual μNode system.

Figure 1-2. Typical μNode device size.
When packaged with a battery, a μNode can be as small as ~3 mm x 3 mm x 5 mm can have a mass less than 20 milligrams, and has a battery life of 1 to 30 days. The size of μNode device is usually limited by the battery dimensions. Presently, an m&m sized communication node shown in Figure 1-2 is being developed.

1.4 Organization of the Dissertation

This Ph.D work focuses on the design and characterization of receiver chain for the 24-GHz radio. The goals of this work are to develop the receiver in main-stream CMOS technology including an on-chip antenna and integrate it with a transmitter designed by C. Cao and a synthesizer developed by Y. Ding as well as to demonstrate communication using the transceiver.

First, a brief overview of the whole system design is given in Chapter 2. Direct Sequence Spread Spectrum (DS/SS) differential chip detection (DCD) is utilized to mitigate the deleterious effects of frequency offset and phase noise. A low noise amplifier (LNA), the first gain stage in the receiver chain, plays an important role in determining the noise performance of whole system. Its design methodology is discussed in Chapter 3. The low output resistance of short-channel transistors limits the amplifier gain. The excess channel thermal noise and induced gate noise hurt the noise performance. Approaches to achieve the reasonable gain and noise performance while consuming low power are investigated. Three design examples are given in Chapter 3. The conversion gain and noise performance of active mixers are discussed in Chapter 4. Demonstration of a 20-GHz RF front-end with on-chip antenna is also presented in this chapter. The RF front-end is used to receive amplitude modulated (AM) signal transmitted from an on-chip antenna 5-m away and to down-convert this signal to intermediate frequency (IF). For the first time, we demonstrate that it is feasible for two ICs to communicate over free space via on-chip antennas.
Chapter 5 discusses the building blocks in the receiver chain including variable gain amplifier (VGA), low pass filter (LPF), 8:1 frequency divider, image rejection filter in LNA and passive mixer. A distributed switch topology is used to share the use of one on-chip antenna by the transmitter and receiver. Chapter 6 presents a fully integrated receiver implemented in a 130-nm CMOS technology. It is characterized with an external LO source as well as with an on-chip frequency synthesizer. In addition, a wireless communication link over 5m has been established using the fully integrated transmitter and receiver. Finally, this research work is summarized and possible future works are suggested in chapter 7.
An RF receiver has two important performance criteria: sensitivity and selectivity. Sensitivity is defined as the lowest power level at which the receiver can recover the information with a required bit-error-rate (BER). Receiver selectivity is a measure of the receiver’s ability to reject signals in adjacent channels or outside of band while receiving wanted signal.

The receiver sensitivity is critically determined by the noise performance of a system which is specified using noise figure (NF). It is related to the noise factor which measures the degradation of signal-to-noise ratio as the signal is processed through a system.

\[ F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \]  

(2-1)

where noise figure (NF) is an equivalent representation in decibels.

In a system consisting of n-stages, if the individual noise factor and gain of system components are known, the overall noise factor can be calculated by Friis equation [31],

\[ F_{sys} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \cdots + \frac{F_n - 1}{G_1G_2 \cdots G_{n-1}}. \]  

(2-2)

Equation 2-2 shows the overall system noise factor is determined by the first few stages if they have sufficient gain to suppress the noise contribution from the following stages. The sensitivity level of a receiver is defined by

\[ \text{Sensitivity level} = -174dBm/Hz + 10\log10(BW) + NF + \frac{E_b}{N_o}, \]  

(2-3)

where the first three terms represent the noise floor at system input, \( NF \) is the noise figure of receiver, \( E_b/N_o \) is the required energy per data bit over variance of noise at minimum BER requirement. The receiver sensitivity level is directly related to the noise figure of receiver. To
minimize the overall noise figure, the noise figure of individual building blocks in the receiver must be reduced and the distribution of gain along the receiver chain has to be properly chosen. If noise figure of individual blocks is fixed, it is desirable to have high gain in the first few stages to suppress the noise contribution from the following stages. However, such kind of gain distribution degrades receiver selectivity.

Receiver selectivity characterizes the ability of a receiver to pick out the wanted signal in the presence of a strong adjacent channel or alternate band signals. The selectivity is affected by many factors such as linearity of individual blocks and gain distribution along the receiver chain. As discussed before, higher gain used in the early stages of receiver reduces the noise figure. However, this will place a tighter linearity requirement on the subsequent receiver blocks. Power consumption is another performance metric. Noise figure and linearity of a receiver can be improved by increasing the power consumption of receiver. For portable applications, the trade-off is between providing satisfactory receiver performance and power consumption.

We will briefly go over two types of receiver architectures: super-heterodyne and homodyne. Then, we will talk about the dual down conversion structure used in this work. The choice of architectures places different emphases on the trades-offs among performance, power consumption and complexity. Unlike conventional radios which generally use an off-chip crystal frequency reference, the single-chip radio will use an on-chip voltage control oscillator (VCO) which increases the frequency offset between TX and RX, and phase noise. As mentioned, DS/SS DCD is used to mitigate these deleterious effects.

2.2 Super-Heterodyne and Homodyne Receiver

A super-heterodyne receiver can have excellent selectivity. In a super-heterodyne receiver, as illustrated in Figure 2-1, the incoming RF signal is picked up by an antenna and filtered by a band select filter following the antenna to attenuate the out of band signals. The LNA amplifies
the signal while introducing a minimal amount of noise. Then, the signal is first down-converted to intermediate frequency (IF) using a mixer and local oscillator (LO) signal generated by a phase lock loop (PLL). There is an image reject filter between the LNA and mixer. This filter is to significantly attenuate the signals in the image band. The LO signal can be tuned to down convert any wanted in-band channel to a fixed IF. The tuning of the LO signal is achieved by setting the divider ratio of PLL. The IF stages can then use a fixed band pass filter which can attenuate unwanted signals. Selectivity is therefore determined by the IF filter. The signal at IF is down-converted once more to baseband using LO2 with fixed frequency. The baseband circuitry performs additional channel filtering and adds variable gain to reduce the dynamic range requirement of analog-to-digital converter (ADC).

The excellent selectivity of a super-heterodyne receiver is due to the high quality factor Q networks formed using off-chip passive components, which are not available for the receivers integrated in a chip.

![Diagram of Super-heterodyne Structure](image)

Figure 2-1. Super-heterodyne structure.

A direct-conversion receiver can eliminate the need for high-Q off-chip passive components. The receiver directly down-converts in-band signal to baseband using only one LO signal without utilizing an IF stage, as shown in Figure 2-2. Unwanted signal can be easily removed at baseband. Direct-conversion architecture is better suited for integrated receiver. However, there are several problems for this architecture. One problem is DC offset. LO signal
can leak either to the mixer input or to the antenna. The radiated LO signal leaking to the antenna can be reflected and picked up by the receiver. In these situations, LO signals are self-mixed and results in DC offset [24]. The unwanted DC offset is interference to the wanted signal. One approach to eliminate the DC offset is utilizing an AC coupling capacitor between mixer output and baseband circuitry. This method effectively high-pass filter this signal. Applicability of this technique highly depends on the system settling time, modulation scheme and bandwidth. For wide-bandwidth system, the pole of high pass-filter can be set relatively high without significantly degrading SNR. Later on, we will discuss how to deal with the AC-coupling issue in the true single chip radio. Other design issue in direct conversion is I/Q phase accuracy and amplitude mismatch. It’s particularly challenging to provide perfect I/Q signals at higher frequencies. For example, a quarter wavelength in silicon at 24GHz is ~900μm. A 10–μm line length difference between I/Q signal traces will translate to 1-degree phase difference. So it will be challenging to implement a direct conversion receiver with such high RF frequencies.

Figure 2-2. Direct conversion receiver.

A μNode only has one channel for low data rate communication. Unlike most of radios which require variable LO frequencies for different channel selection, a μNode makes use of LO1 and LO2 in super-heterodyne structure with both fixed and they are generated using a single frequency source. Shown in Figure 2-3 is a block diagram of the transceiver. It consists of a transmitter, receiver and frequency synthesizer. The transceiver utilizes dual conversion
Two LO signals are at 21.3GHz and 2.7GHz, respectively. They are generated by using only one 21.3-GHz frequency synthesizer and a frequency divide-by-8 circuit.

Figure 2-3. Simplified RF transceiver block diagram.

On the receiver side, an incoming 24-GHz signal is picked up by an on-chip antenna, amplified by a low noise amplifier (LNA), down-converted to IF at 2.7GHz and then down-converted to baseband to generate quadrature I and Q signals. These two signals are amplified by variable gain amplifiers (VGA), filtered by lower pass filters (LPF) and then digitized by two 100-MHz, 5-bit analog-to-digital converters (ADCs). The receiver frequency plan is depicted in Figure 2-4. The image channel is located at 18.6GHz, which is 5.4GHz away from the desired RF channel. This unwanted image signal can be attenuated by the tuned response of LNA and mixer. On the transmitter side, its frequency plan is the same as the receiver. The baseband I and Q are first modulated to 2.7GHz by a modulator [21] implementing an MSK-like constant envelope phase-shift modulation. The modulated signal is then converted to 24GHz by an up-conversion mixer. The up-converted 24-GHz signal is delivered to the on-chip antenna through
an on-chip power amplifier (PA) [22]. Since the 24-GHz transmitter output signal is 2.7GHz away from the 21.3-GHz operating frequency of the synthesizer, LO pulling by the PA is eliminated [23].

Figure 2-4. Receiver frequency plan.

2.3 Baseline PHY

Unlike most modern communication systems which depend on a stable crystal-based frequency reference, the RF subsystem of µNodes will use an on-chip frequency reference with poor phase noise and large frequency offset. The operating frequency of µNode is 24GHz with relatively low bit rate (100kbps). A subtle LO frequency offset between that of the transmitter and that of the receiver can cause severe performance degradation. To mitigate this, modulation and receiver processing methods were developed. To discuss this, let us consider a BPSK system in which the received signal is given by

\[ r(t) = \pm A p(t) \cos(2\pi f_c t + n(t)), \]  

where \( n(t) \) is Additive White Gaussian Noise (AWGN) process with noise spectral density of \( N_0/2 \). Assuming a receiver uses \( \cos(2\pi f_c t) \) to demodulate the incoming signal, the average bit error probability is given by

\[ P_b = Q\left(\sqrt{\frac{2E_b}{N_0}}\right), \]  

(2-5)
where

\[ \alpha = \frac{1}{T} \int_0^T \cos(2\pi(f_c - \hat{f}_c)t) \, dt \]

\[ = \frac{\sin(2\pi(f_c - \hat{f}_c)T)}{2\pi(f - \hat{f}_c)T} , \]

(2-6)

where \( T \) is the symbol duration time which is 10\( \mu \)S for 100kbps data rate. The frequency offset is defined in terms of ppm,

\[ FreqOff(ppm) = \frac{f_c - \hat{f}_c}{f_c} \times 10^6 . \]  

(2-7)

Figure 2-5. BER for BPSK with frequency offset.

Figure 2-5 shows the average bit error probability (BER) for BPSK coherent demodulation with 0-ppm, 0.5-ppm and 1-ppm frequency offset. To maintain BER of 10\(^{-4}\) with 1-ppm frequency offset, \( E_b/N_0 \) must be increased by more than 3dB from 0-ppm case. Unfortunately, even 1-ppm tolerance which translates to 24 kHz for a 24-GHz carrier is extremely difficult to achieve. One way to mitigate the frequency offset and poor phase noise of on-chip reference
frequency source is to use direct sequence spread spectrum (DS/SS) differential chip detection (DCD) [25].

2.3.1 Direct Sequence Spread Spectrum (DS/SS)

Spread spectrum is a technique to spread the transmitted signal power over a broad spectrum. Spreading spectrum reduces power transmitted at any one frequency so that it would reduce interference to others and make the detection of the presence of signals difficult. It is also less susceptible to interference at any one frequency and makes jamming difficult.

![Diagram of BPSK modulation and BPSK spreading scheme.](image)

Figure 2-6. BPSK modulation and BPSK spreading scheme.

One way to spread signals is to modulate the transmitted data signal by a high rate pseudo-random sequence of phase-modulated pulses before mixing the signal up to the carrier frequency for transmission. This spreading method is called direct sequence spread spectrum [26]. Suppose the data signal is

\[ b(t) = \sqrt{2P} \sum_{k=-\infty}^{\infty} b_k p_T(t-kT), \]  

(2-8)
where $b_s$ is the symbol sequence and $T$ is the symbol duration. We modulate the data signal $b(t)$ by spreading signal $a(t)$ or a PN code, which is

$$a(t) = \sum_{l=-\infty}^{\infty} a_i \psi(t - lT_c), \quad (2-9)$$

where $a_i$ is called signature sequence and $\psi(t)$ is called the chip waveform. We impose the condition that $T = NT_c$ where $N$, referred at the processing gain or the spreading gain, is the number of chips in a symbol and $T_c$ is the chip duration. Then the spread spectrum signal is given by

$$s(t) = b(t)a(t), \quad (2-10)$$

There are many spreading schemes. For example, a spreading scheme with BPSK modulation which means $b_k = \pm 1$ and BPSK spreading which means $a_i = \pm 1$ is illustrated in Figure, where spreading gain is only 4. The power spectrum of the spread signal $s(t)$ is given by

$$\Phi_s(\omega) = PT_c \frac{\sin^2(\omega T_c/2)}{(\omega T_c/2)^2}. \quad (2-11)$$

Compare this to the power spectrum of the original data signal.

$$\Phi_b(\omega) = PT \frac{\sin^2(\omega T/2)}{(\omega T/2)^2}. \quad (2-12)$$

We see that the spectrum is spread $N$ times wider by the multiplication of the PN sequence. This is illustrated in Figure 2-7. This figure shows a wireless link including a transmitter, a channel and a matched filter receiver. One great feature of DS/SS is the low probability of detection. It means that it is hard for an unintended receiver to detect the presence of the signal. When the processing gain is significantly large, the spread spectrum signal can be below the white noise floor, as shown in Figure 2-7. A receiver without the proper PN code can not despread the received signal. The RF subsystems size of only ~3 mm × 3 mm and the signal in a
wide frequency band below background noise level make the radio physically and electrically invisible.

Figure 2-7. DS/SS BPSK system block diagram.

2.3.2 Differential Chip Detection of Direct Sequence Spread Spectrum (DS/SS-DCD)

The RF subsystem for µNode will utilize an on-chip frequency reference to generate the LO signals which could have higher phase noise and larger frequency offset. To mitigate these, DS/SS DCD can be utilized [25]. The application of differential detection at chip level rather than data symbol level significantly improves receiver robustness to large carrier phase drift since the phase variation could be considered negligible within a pair of chip interval.

Figure 2-8 shows the basic processing step used in differential chip detection [27]. The transmitted signal $d_k$ is modulated by random phase $\theta_k$ and frequency offset $\omega$, and corrupted by white noise signal $n_k$. Then the sampled baseband signal is

$$r_k = d_k e^{j(\omega T_c + \theta_k)} + n_k$$

(2-13)

where $T_c$ is the chip rate. The output of differential chip detector is

$$\overline{c_k} = \text{Re}\{r_k^* r_{k-1}^*\}$$

(2-14)
Let’s ignore phase noise $\theta_k$ for this moment to examine effect of the frequency offset. Then Equation 2-14 becomes

$$\overline{c_k} = \text{Re}\{d_k^* e^{j\omega T_c} \} = d_k^* d_{k-1}^* \cos(\omega T_c). \quad (2-15)$$

When the frequency offset $\omega$ is small compared to the chip rate $1/T_c$, $\cos(\omega T_c)$ is approximately equal to 1, then $\overline{c_k}$ is close to the desired differentially detected signal $c_k = d_k^* d_{k-1}^*$.

As the frequency offset increases relative to the chip rate, the cosine factor becomes less than unity and reduces the signal level, which in turn degrades the receiver sensitivity. Frequency-offset tolerance can be made arbitrarily high by simply increasing the chip rate. However, for a fixed data rate, increasing the chip rate requires increasing the processing gain (chips per symbol), which leads to higher implementation cost and degraded sensitivity for DS/SS-DCD.

When the phase drift and noise are considered, assuming that the noise samples, $n_k$ and $n_{k-1}$, and the chip samples, $d_k$ and $d_{k-1}$, are uncorrelated, the input and output chip SNRs are

$$\text{SNR}_{in} = \frac{E_c}{n_k^2} = \frac{E_c}{N_0} \quad \text{(2-16)}$$

$$\text{SNR}_{DCD} = \frac{d_k^2 d_{k-1}^* \epsilon^2}{d_k^2 n_{k-1}^2 + d_{k-1}^2 n_k^2 + n_k^2 n_{k-1}^2} = \frac{\epsilon^2 E_c^2}{2E_c N_0 + N_0^2} = \frac{\epsilon^2 \text{SNR}_{in}^2}{2\text{SNR}_{in} + 1} \quad \text{(2-17)}$$
where $\bar{\varepsilon}$ is the mean energy loss factor due to the frequency offset and phase noise. It will be discussed in detailed later and assumed to be constant for this moment. For large input SNR, the DCD SNR is approximately equal to half of the input SNR which means 3-dB degradation. However, for the low input SNR levels typical in DS/SS receivers (below 0dB), the DCD SNR approaches the square of the input SNR. $SNR_{DCD}$ can be converted to an effective $(E_b/N_0)_{DCD}$

$$\frac{(E_b)}{N_0}_{DCD} = \frac{-2(\bar{\varepsilon})^2(E_b/N_0)^2_{in}}{2(E_b/N_0)_{in} + G_p}, \tag{2-18}$$

where $G_p$ is the processing gain. For large $G_p$, $(E_b/N_0)_{DCD}$ is

$$\frac{(E_b)}{N_0}_{DCD} \approx \frac{1}{G_p} \left(\frac{\bar{\varepsilon}E_b}{N_0}\right)^2_{in}, \tag{2-19}$$

Equation 2-19 shows that each doubling of the processing gain requires a 1.5dB increase in $(E_b/N_0)_{in}$ to maintain $(E_b/N_0)_{DCD}$ the same or bit error probability.

The mean energy loss factor in Equation 2-17 given in [25] is

$$\bar{\varepsilon} = \cos(\omega T_c)e^{-\sigma_{\Delta\theta}^2/2}. \tag{2-20}$$

$\sigma_{\Delta\theta}^2$ is the variance of $\Delta\theta_k$ which is defined by,

$$\Delta\theta_k = \theta_k - \theta_{k-1}. \tag{2-21}$$

It can be written in Z-domain,

$$\Delta\theta(Z) = \theta(Z)H_\theta(Z), \tag{2-22}$$

where $H_\theta(Z)$ is the phase transfer function produced by differential chip detection,

$$H_\theta(Z) = 1 - Z^{-1}. \tag{2-23}$$

The frequency response of $H_\theta(Z)$ is obtained by setting $Z = e^{j2\pi fT_c}$:

$$H_\theta(f) = 1 - e^{-j2\pi f}, \quad |H_\theta(f)|^2 = |2\sin(\pi fT_c)|^2. \tag{2-24}$$
Given the power spectral density $P_\vartheta(f)$ for the LO phase noise,

$$
\sigma_\vartheta^2 = 2 \int_{0}^{\infty} P_\vartheta(f) |H_\vartheta(f)|^2 df.
$$

(2-25)

Since $H_\vartheta(f)$ has a highpass filter nature, it helps to suppress close-in LO phase noise. Assuming that chip matched filter (CMF) effectively limits the bandwidth of the phase noise to $\pm 1/2T_c$, a simple analytical model is (equation (19) in [25]),

$$
\bar{e} = \cos(\phi T_c) \exp(-13.25K),
$$

(2-26)

$$
K = T_c f_0^2 P_\vartheta(f_0) = \frac{f_0^2 P_\vartheta(f_0)}{G_p R_b}.
$$

(2-27)

Figure 2-9. Required $E_b/N_0$ at BER of $10^{-4}$.

Using Equation 2-19 and 2-26, $E_b/N_0$ required at BER=$10^{-4}$ with different processing gain is shown in Figure 2-9 for three different situations: only AWGN channel without frequency offset and phase noise ($\omega = 0$ and $K = 0$), AWGN channel with phase noise ($\omega = 0$ and $K = 0.01$) and AWGN channel with phase noise ($K = 0.01$) and frequency offset of
0.1 \( R_c (\omega = 2\pi R_c / 10) \). Based on Equation 2-18 and 2-26, the presence of phase noise \(( K = 0.01)\) will cause \( \sim 1.2 \)-dB energy loss and frequency offset of 0.1 \( R_c \) will cause additional \( \sim 2 \)-dB energy loss. To achieve the same BER of \( 10^{-4} \), the \( E_b/N_0 \) in the presence of phase noise \(( K = 0.01)\) needs to be increased from 0.7 to 1.2 dB compared to the case with only AWGN. Additional frequency offsets of 0.1 \( R_c \) requires extra from 1 to 1.6 dB increase in \( E_b/N_0 \).

### 2.3.3 Modulation Format

![Figure 2-10. Block diagram of 16-ary orthogonal modulation.](image)

As shown in Figure 2-10, the radio uses a DS/SS in which each data symbol is represented by one of 16 different PN sequences. One PN sequence represents 4 bits. These PN sequences are selected to be approximately orthogonal. The format can be viewed as 16-ary orthogonal modulation. The selected PN sequence which contains 2048 chips is passed to the chip level differential encoder. Then the encoded chip sequence is modulated onto the carrier using Offset QPSK (OQPSK) with half-sine pulse shaping which is Minimum Shift Keying (MSK). The corresponding power spectral density (PSD) is

\[
\phi_b(f) = \frac{16T_b}{\pi^2} \left\{ \frac{\cos^2[2\pi T_b(f-f_c)]}{[1-16T_b^2(f-f_c)^2]^2} + \frac{\cos^2[2\pi T_b(f+f_c)]}{[1-16T_b^2(f+f_c)^2]^2} \right\}, \tag{2-28}
\]
where $T_b$ is the average bit interval. The spectrum for MSK decays roughly as $1/f^4$. Figure 2-11 shows a block diagram of the 16-ary orthogonal demodulator [28]. The demodulator consists of a differential chip detector followed by an optimal coherent detector for orthogonal signaling. The differential chip detector removes phase offsets between transmitter and receiver, and it mitigates the impact of frequency offsets as well as phase noise.

**Figure 2-11.** 16-ary orthogonal detector with DCD.

Similar to Equation 2-18, $E_b/N_0$ at the input of the PN sequence matched filter in Figure 2-Figure 2-11 is

$$
\frac{(E_b)}{N_0}_{\text{DCD}} = \frac{\varepsilon^2 (E_b/N_o)^2_{in}}{2(E_b/N_o)_{in} + G_p / B^4.}
$$

(2-29)

where $G_p$ is the processing gain for one symbol, defined here as the number of chips per symbol and $B$ is the number of bits per symbol. For M-ary orthogonal signaling where each symbol represents B bits, the average symbol error probability ($P_s$) [29] is

$$
P_s = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} \left[ 1 - \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{y} e^{-x^2/2} dx \right]^{M-1} \exp\left(-\frac{1}{2} \left(y - \sqrt{2E_b} \right)^2 / N_0 \right) dy,
$$

(2-30)
\[
\frac{E_s}{N_0} = 4\left(\frac{E_b}{N_0}\right)_{DCD}
\]  
(2-31)

The corresponding bit error probability \( (P_b) \) is

\[
P_b = \frac{M/2}{M-1} P_s
\]  
(2-32)

Using Equation 2-30, 2-31 and 2-32, the required \( E_b/N_0 \) at BER of \( 10^{-4} \) with different processing gain to tolerate different frequency offset in the 16-ary orthogonal detector is shown in Figure 2-12.

Figure 2-12. AWGN performance in 16-ary orthogonal detector.

However, in real implementation, noise and chip samples are not completely uncorrelated. The set of 16 PN sequences are not perfectly orthogonal. All these factors will cause performance degradation. One of the goals for the integrated frequency reference is to \( \pm100\text{ppm} \) stability, which could produce a worst-case frequency offset \( 200\text{ppm} \) between a transmitter and a receiver. At the 24 GHz operating frequency this translates to a 4.8 MHz offset. Using 10\% of the chip rate as our rule of thumb for acceptable offset, then the chip rate must be on the order of
48 Mchip/s. The processing gain $G_p$ required to achieve this chip rate will depend on the desired data rate. For the 100 kpbs assumed here, the 16-ary symbol rate would be 25 k-symbol/second, and a processing gain of $G_p=2048$ would give a chip rate of 51.2 Mchip/s. This is slightly larger than the desired 48 Mchip/s, but it allows $G_p$ to be a power-of-2 which simplifies implementation. It is shown in Figure 2-12, to tolerate 130-ppm frequency offset, processing gain of 2048 and $E_b/N_0$ of 17.5dB are needed. In addition, with $G_p=2048$, the phase noise requirement is greatly relaxed. According to [28], a phase noise level of -65dBc/Hz at 1-MHz frequency offset only causes 0.5dB $E_b/N_0$ degradation. Based on the $E_b/N_0$ of 18dB which tolerates the frequency offset and phase noise, the link budget of receiver is given in Table 2-1.

Table 2-1. Link budget of $\mu$Node.

<table>
<thead>
<tr>
<th>Spec</th>
<th>Targeted Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX Output Power</td>
<td>10 dBm</td>
</tr>
<tr>
<td>Communication Range</td>
<td>5 m</td>
</tr>
<tr>
<td>Antenna Pair Gain</td>
<td>-84 dB</td>
</tr>
<tr>
<td>Antenna Direction Loss</td>
<td>4 dB</td>
</tr>
<tr>
<td>Received Power</td>
<td>-78 dBm</td>
</tr>
<tr>
<td>Thermal Noise</td>
<td>-174 dBm/Hz</td>
</tr>
<tr>
<td>Bandwidth (100 kb/s)</td>
<td>50 dB</td>
</tr>
<tr>
<td>$E_b/N_0$</td>
<td>18 dB</td>
</tr>
<tr>
<td>RX Noise Figure</td>
<td>10 dB</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>-96 dBm</td>
</tr>
<tr>
<td>Link Margin</td>
<td>18 dB</td>
</tr>
</tbody>
</table>

2.4 Summary

This chapter reviewed the communication system for $\mu$Nodes including RF front-end architecture and baseline physical layer. A dual down conversion architecture is selected. This architecture uses only one frequency synthesizer and divide-by-8 circuit to generate two LO signals. Unlike most radios which use crystal frequency reference, reducing the chip area. Unlike
most radios which use a crystal frequency reference, the RF subsystem uses an on-chip VCO as the frequency reference. Poor phase noise and frequency offset of the VCO could significantly degrade the system performance. DS/SS-DCD is utilized to mitigate these effects. This chapter described the relationship between the frequency offset tolerance and processing gain. The tradeoff between the receiver sensitivity and processing gain is also discussed. To tolerate 130-ppm frequency offset and -65dBc/Hz phase noise at 1MHz offset, $E_b/N_0$ of 18dB is required. From this specification, sensitivity target for this radio is -96dBm.
3.1 Introduction

Modern receiving systems must often process very weak signals. The noise added by a receiver corrupts these weak signals. One approach to reduce the effect of the receiver noise is to make the received signal stronger. This can be accomplished by raising the signal power transmitted in the direction of receiver. This is eventually limited by government regulations, engineering considerations, or economics. Another way is to increase the amount of power the receiving antenna can collect, for example, by increasing the aperture of receiving antenna. The other approach is to minimize the noise of receiving system. Lowering receiver noise has the same effect on the output signal-to-noise ratio as improving any one of the other quantities. Increasing the transmitting power or increasing aperture of antenna can be costly compared to the small cost of improving the LNA noise performance.

3.2 Noise Sources in MOS Device

Figure 3-1. Cross section of a MOSFET channel consisting of a gradual channel region (I) a velocity saturation region (II).

The noise in RF building blocks is contributed by the active components (transistors) and passive components such as resistors and inductors. Resistors contribute thermal noise. In MOSFETs, there are two major sources of noise at low frequencies (~1MHz and below): 1/f
noise and thermal noise. 1/f noise is caused by carrier number fluctuation [31], [33] and mobility fluctuation [34] in the channel. It is a low frequency phenomenon. In tuned RF amplifiers designs, due to the high operating frequency, the channel thermal noise is the main concern. Thermal noise is generated by random motion of channel carriers. In short channel devices, due to velocity saturation, the channel can be divided into two sections [38]: a gradual channel region and a velocity saturation region, shown in Figure 3-1.

In gradual region described in [35], the drain current is

\[ I_{ds} = -\mu W Q_i(x) \frac{dV}{dx} \]  \hspace{1cm} (3-1)

where \( \mu \) is the mobility, \( W \) is the channel width and \( Q_i \) is the inversion layer charge per unit width at position \( x \) along the channel. Rewriting Equation 3-1 as

\[ I_{ds} \frac{dx}{\mu W Q_i(x)} = -dV \]  \hspace{1cm} (3-2)

giving the resistance \( \Delta R \) of a small segment \( \Delta x \) in the channel

\[ \Delta R = \frac{\Delta x}{\mu W Q_i(x)} \]  \hspace{1cm} (3-3)

The spectral density of this small resistor is

\[ \frac{\Delta v^2}{\Delta v} = \frac{4kT \Delta x}{\mu W Q_i(x)}. \]  \hspace{1cm} (3-4)

This “local” noise will cause noise in the drain current. Integrating Equation 3-1 along the channel gives

\[ I_{ds} = \frac{W}{L} \mu \int_{0}^{L} Q_i(x) dV(x) \]  \hspace{1cm} (3-5)

Now, let’s assume there is voltage perturb \( \Delta V \) at position \( x \) in the channel, Equation 3-5 is rewritten as
\[ I_{ds} = -\frac{W}{L} \mu \int_{V_{th}}^{V} Q_i(x) dV + \int_{V_{th}}^{V} \mu Q_i(x) dV. \]  

(3-6)

Local conductance is defined from Equation 3-6,

\[ g(x) = \frac{\partial I_{ds}}{\partial \Delta V} = \frac{W}{L} \mu Q_i(x). \]  

(3-7)

which specifies how small voltage change in the channel causes the change of drain current.

Combining Equation 3-4 and 3-7 gives the contribution of small segment \( \Delta x \) in the channel to noise spectral density of drain current in gradual channel region,

\[ \Delta i_d^2 = g(x)^2 \Delta v^2 = 4kT \frac{\mu W Q_i(x)}{L^2} \Delta x. \]  

(3-8)

The total channel thermal noise density is the integral of Equation 3-10 along the channel, giving

\[ i_d^2 = 4kT \frac{\mu W Q_{inv}}{L^2}. \]  

(3-9)

\( Q_{inv} \) is inversion layer charge per transistor width. This equation is valid for any model, provided the appropriate expression is used for \( Q_{inv} \). Particularly, for models using the gradual-channel-approximation (GCA) [36], \( Q_{inv} \) is

\[ Q_{inv} = \frac{2}{3} LC_{ox} (V_{gs} - V_{th}). \]  

(3-10)

Then, it can be rewritten as classic channel thermal noise spectral density [37]

\[ i_d^2 = 4kT \gamma g_m. \]  

(3-11)

where \( \gamma \) is 2/3 and \( g_m \) is the transcondutance of the transistor.

Noise generated in the velocity saturation region (II) is treated differently in various previously reported papers [39]-[40]. Channel resistance in region II is derived in [38] while in [39] the thermal noise of this region is calculated based on inverse charge and excessive electron temperature. However, it is argued in [40] that noise from this region is zero because the carriers do not respond to the finite voltage fluctuation when they travel at saturation velocity. Even
though noise generation mechanism in this region is not clear now, it has been reported that in [30], [41] that short-channel NMOS devices in saturation exhibit noise far in excess of values predicted by long-channel theory. $\gamma$ is typically 2-3. It generally increases with drain current as well as $V_{ds}$. As drain-to-source voltage is increased, the electric field within the channel increases, generating hot carriers. Transistors operating in weak inversion have a spectral density

$$i_g^2 = 2qI_D.$$  (3-12)

assuming $V_{ds} \geq 5kT/q$. It is interesting to observe that the expression for weak inversion is just like that of shot noise [36]. In weak inversion the current in the channel is controlled by the height of source-channel barrier which is lowered by increasing the gate voltage.

![Figure 3-2. Induced Gate Noise.](image)

The MOS can also be viewed as an RC distributed network with $R$ representing channel resistance and $C$ representing the gate capacitance, as shown in Figure 3-2. At high frequencies, the local voltage fluctuation in the channel due to thermal noise couples to the gate through the oxide capacitance, inducing the gate noise current to flow. The spectral density of gate induced noise [37] is

$$i_g^2 = 4kT \cdot \delta \cdot \frac{\omega^2 C_{gs}^2}{5g_m}.$$  (3-13)
where $\delta=4/3$ for long channel device. Since the channel noise and induced gate noise are physically generated by the same noise source, they are correlated. The correlation coefficient is

$$c = \frac{i_{g}-i_{d}}{\sqrt{\left(i_{g}\right)^{2}+\left(i_{d}\right)^{2}}} = -j \sqrt{\frac{5}{32}} = -j0.395.$$  

(3-14)

The gate thermal noise arises from the resistance of gate material. The noise introduced by the intrinsic portion of the gate structure of width $W$ and channel length $L$ is given by

$$\overline{V_{g,i}^2} = 4kT \frac{R_{g,sq}W}{3L}$$  

(3-15)

$R_{g,sq}$ is the sheet resistance of gate material. The factor of three arises from a distributed effect [42]. It will be lowered by a factor of four if the gate is connected from both sides. For ultra deep submicron CMOS, gate current depends mainly on gate-source voltage bias and gate area. Just as any current across the junction, gate leakage exhibits shot noise with current density $i_{G} = 2qI_{G}$, combined with induced gate noise, it will limit noise performance.

### 3.3 Topologies of LNAs

In an RF receiver, the input signal from an antenna is amplified by an LNA. As shown in Friis equation, to sufficiently suppress the noise contribution from following stages, an LNA should have high gain and its noise contribution to the system should be low. In portable devices, the power consumption should also be low. One of LNA’s functions is to provide right input impedance, generally 50Ω, as required by the preceding band-select filter. Otherwise, the insertion loss and pass-band ripple of the filter will be degraded. Even without a preceding filter, the LNA needs to provide proper impedance to the antenna.

However, simply shunting a 50-Ω resistor at the input will significantly degrade the noise performance of the amplifier. Generally used topology is common-gate (CG) and source degenerated common-source (CS) topology, as shown in Figure 3-3.
Figure 3-3. Two types of LNA topologies. A) CG-LNA and B) CS-LNA

The input impedance of the CG-LNA stage is approximately $1/g_{m1}$ of the input transistor M1, while that of the CS-LNA is

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s$$

$$= s(L_g + L_s) + \frac{1}{sC_{gs}} + \omega r L_s. \tag{3-16}$$

$Z_{in}$ is specified by choosing $L_g$ and $L_s$ to resonate with $C_{gs}$ at the operating frequency. Its real part $\omega r L_s$ is set to 50Ω. A fundamental difference between these two input matching networks is that CS-LNA uses a series resonant circuit while CG-LNA employs a parallel resonant circuit. The quality factors of two input networks are

$$Q_{CG-LNA} = \frac{\omega_0 C_{gs} R_s}{2} \quad \Leftrightarrow \quad Q_{CS-LNA} = \frac{1}{2\omega_0 C_{gs} R_s}. \tag{3-17}$$

Typically, $Q_{CG-LNA} < 1$ while $Q_{CS-LNA} > 1$. It is well known that sensitivity of $Z_{in}$ to component variation is proportional to the quality factor of matching network. Hence, CG-LNA with its lower $Q$ parallel resonant network is more robust against typical component variations.
Moreover, parasitic capacitance at the CG-LNA input is naturally absorbed into LC tank. The effective transconductance of the CS-LNA is

\[
G_{m,CS-LNA} = g_mQ = \frac{g_m}{\omega_0C_q(R_s + \omega_f L_s)} = \frac{\omega_f}{\omega_0R_s(1 + \frac{\omega_f L_s}{R_s})}.
\]  

(3-18)

With the input matched to \(R_s\),

\[
G_{m,CS-LNA} = \frac{1}{2R_s} \left( \frac{\omega_f}{\omega_0} \right).
\]  

(3-19)

In contrast, the effective input tranconducance of CG-LNA under perfect input matching conditions is

\[
G_{m,CG-LNA} = \frac{1}{2} g_m = \frac{1}{2R_s}.
\]  

(3-20)

The value of \(\omega_f/\omega_0\) typically is in the range of 3~5, depending on the operating frequency and the technology. Therefore, CS-LNA provides higher gain than its conventional common-gate counterpart. Especially, in high frequency circuits, the gain boosting by input matching network is often utilized.

### 3.3.1 Gain of CS-LNA

To drive the complete gain of CS-LNA, a simplified circuit shown in Figure 3-4 is analyzed. In CS-LNA, the short-circuit transconductance \(G_m\) is given in Equation 3-18, and output impedance is \(Z_{load}\) if \(r_o\) is sufficiently large. However, with CMOS device scaling, \(r_o\) of intrinsic transistor becomes smaller and its effect has to be considered into gain calculation.

Extra-Element-Theorem (EET) [43] is utilized to make calculation much easier. This method is a powerful way to identify the effect of one particular element on whole network. Following the procedure in [43], \(r_o\) is assigned as an extra element and initially it is assumed open. The voltage gain is
\[
\frac{V_{\text{out}}(\omega)}{V_{\text{in}}(\omega)} = \frac{jg_m Z_{\text{load}}(\frac{\omega_0}{\omega} Q_{gs})}{2 + j(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega})Q_{gs}}.
\]  

(3-21)

Where \( \omega_0 = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}} \) and \( Q_{gs} = \frac{1}{\omega_0 C_{gs} R_s} \).

\[
Z_n = \frac{\omega_0^2 C_{gs} L_s}{g_m}.
\]  

(3-22)

The impedance \( Z_n \) seen by \( r_o \) with \( V_{in} \) adjusted to yield \( V_{out}=0 \) is

\[
Z_d = \frac{Z_{\text{load}}}{2} + \frac{sL_s}{2}.
\]  

(3-23)

The impedance \( Z_d \) seen by \( r_o \) with \( V_{in}=0 \) at resonant frequency is

\[
H = \frac{g_m Z_{\text{load}} Q_{gs}}{2} \left( \frac{1 + \omega_0^2 C_{gs} L_s}{g_m r_o} \right) \frac{g_m r_o}{Z_{\text{load}} + j\omega L_s}.
\]  

(3-24)

Figure 3-4. CS-LNA and its equivalent circuit.

The complete voltage gain at resonant frequency is
When \( \frac{\omega^2 C_{gs} L_s}{g_m r_o} \ll 1 \) and \( j\omega L_s \ll|Z_{load}| \), Equation 3-24 can be simplified as

\[
H = \frac{g_m Z_{load} Q_{gs}}{2} \cdot \frac{1}{1 + \frac{Z_{load}}{2r_o}}.
\]

(3-25)

The effect of finite output resistance \( r_o \) on gain of the amplifier is shown in Figure 3-5.

When \( r_o \) is same as \( Z_{load} \), gain drop is 3.5dB compared to an amplifier having an infinite output resistance. Rewriting Equation 3-25 as

\[
H = \frac{g_m Q_{gs} Z_{load}}{2} \cdot \frac{2r_o}{Z_{load} + 2r_o}.
\]

(3-26)

It indicates output node has parallel combination of \( Z_{load} \) and \( 2r_o \). \( 2r_o \) is the output resistance of common-source tuned LNA.

![Figure 3-5. Output resistance effect on gain.](image)

### 3.3.2 Noise Factor of CS-LNA

It is first discussed in [47] that gate induced noise could play an important role in noise performance in high frequency LNAs. Figure 3-6 shows the network including three noise
sources: gate induced noise $i_g$, channel thermal noise $i_d$ and source voltage noise $v_n$. Output short circuit noise current $i_f$ is calculated.

$$i_f = i_{n1} + i_{n2}$$

Figure 3-6. Noise sources in CS-LNA.

It is easy to show that the relationship between the output noise current $i_{n1}$ and gate induced noise $i_g$ and channel thermal noise $i_d$ is given by

$$i_{n1} = \frac{\beta(Z_g + Z_s)}{1/SC_{gs} + Z_g + (\beta + 1)Z_s} \cdot i_g + \frac{Z_g + Z_s + 1/SC_{gs}}{\beta Z_g + Z_g + Z_s + 1/SC_{gs}} \cdot i_d.$$  \hspace{1cm} (3-27)

where $\beta = \omega_r / j\omega_o$ is the MOSFET current gain from gate to drain. If $Z_g$ and $Z_s$ are defined as $R_s + j\omega L_s$ and $j\omega L_s$, Equation 3-27 can be rewritten as

$$i_{n1} = i_g \cdot \frac{1}{1 + \frac{\omega_o L_s}{R_s}} \cdot \left( \frac{\omega_r}{j\omega_o} \right) \cdot \frac{R_s + j\omega(L_g + L_s)}{R_s} + i_d \cdot \frac{1}{1 + \frac{\omega_o L_s}{R_s}}.$$ \hspace{1cm} (3-28)

At the resonant frequency, this relationship can be rewritten as

$$i_{n1} = \frac{1}{1 + \frac{\omega_o L_s}{R_s}} \cdot \left[ i_g \cdot \frac{\omega_r}{\omega_o} \cdot (1 + j\omega o) + i_d \right].$$ \hspace{1cm} (3-29)

Similarly, the output noise current due to input voltage noise source $v_n$ is

$$\frac{i_{n2}}{v_n} = \frac{g_m}{1 + s(g_m L_s + C_{gs} R_s) + s^2 C_{gs} (L_g + L_s)}.$$ \hspace{1cm} (3-30)

At the resonant frequency, it is simplified as
\[ \frac{i_{n2}}{v_n} = \frac{\omega_T}{\omega_0(R_s + \omega_T L_s)} = \frac{g_m Q_{gs}}{2}. \] (3-31)

The total output noise current is
\[ i_1 = i_{n1} + i_{n2}. \] (3-32)

Noise factor of the amplifier will be ratio of total output noise power \( (i_n) \) to the output noise power contributed by input noise source \( (v_n) \).

\[ F = \frac{i_n^2(i_g, i_d)}{i_{n2}(v_n)} = 1 + \frac{i_{n1}^2(i_g, i_d)}{i_{n2}^2(v_n)} \] (3-33)

The detailed derivation is given in Appendix A. It is shown in Equation A-5.

\[ F = 1 + \frac{\delta(1 + Q_{gs}^2)/5 + \gamma - 2\cdot c \cdot \sqrt{\delta \gamma}}{g_m Q_{gs}^2 R_s}. \] (3-34)

The result is the same as that in [47], [48]. Unlike the procedure taken in [47] which calculates uncorrelated and correlated parts in gate induced noise separately, the derivation here directly gives total output noise current spectral density including the correlation between gate induced noise and channel thermal noise. Including gate inductor resistance, noise factor is

\[ F_1 = F + \frac{R_g}{R_s}. \] (3-35)

Noting that

\[ \frac{R_g}{R_s} = \frac{\omega_0 L_s}{Q_{ind}} = \frac{Q_{gs}}{Q_{ind}} \text{ and } R_s \left( \frac{\omega_0}{\omega_T} \right) = \frac{1}{g_m Q_{gs}}. \] (3-36)

Substituting Equation 3-34 and 3-26 into Equation 3-35 results in

\[ F_1 = 1 + \frac{Q_{gs}}{Q_{ind}} \left[ \gamma - 2\cdot c \cdot \sqrt{\gamma \delta / 5} + \delta(1 + Q_{gs}^2)/5 \left( \frac{\omega_0}{\omega_T} \right) \right] \] (3-37)
3.3.3 Noise Factor of Cascode Amplifier

An LNA is generally implemented with a cascode stage to improve the stability by isolating the input port from output port voltage variation, as shown in Figure 3-7. The isolation makes the design more straightforward. At low frequencies, for long channel device which has high output resistance, the noise contribution from the upper transistor M2 is believed to be much lower than that from the bottom transistor M1. It is suggested [49], [50] that optimal choice of M2 is about same as M1. Other author [51] has suggested ratio of width of M2 and M1 ranging from 0.55 to 0.75.

![Figure 3-7. Schematic of cascode amplifier.](image)

For an LNA operating near 20GHz, the effects of drain-to-body capacitance on noise performance and effects of M2 should be more carefully considered. The noise contribution from M2 to output noise can be readily derived using Equation 3-27 where \( Z_g = 0 \) and \( Z_s = 2r_0/(1/sC_{db}) \). Here \( r_0 \) is output resistance of M1.

\[
i_{n,2} = \frac{\beta Z_s}{1/sC_{gs} + (\beta + 1)Z_s}i_g + \frac{Z_s + 1/sC_{gs}}{\beta Z_s + Z_s + 1/sC_{gs}}i_d. \tag{3-38}
\]
At ~20 GHz, $2r_0 \gg |1/sC_{db}|$, giving

$$i_{n-2} = \frac{\beta \cdot i_x + C_r \cdot i_d}{C_r - j \omega r / \omega}.$$  \hspace{1cm} (3-39)

Where $C_r = 1 + C_{db}/C_{gs}$, the spectral density of output noise current due to M2 is

$$\overline{i_{n-2}^2} = \frac{[\beta_2]^2 \overline{i_{g2}^2} + C_r \overline{i_{d2}^2} - 2|\beta_2|C_r \overline{i_x^2} \sqrt{\overline{i_d^2}}}{C_r + |\beta_2|^2}.$$  \hspace{1cm} (3-40)

$\beta_2$ is the current gain of M2.

![Schematic](image)

Figure 3-8. Schematic calculating output noise current from common-source stage.

To calculate the noise contribution from M1 to output, the current derived in Equation 3-27 can be treated as the short circuit current in Norton equivalent network with output resistance of $2r_o$, as modeled in Figure 3-8. It can be shown

$$i_{n-1} = \frac{\beta_2 \cdot i_x}{1 + C_{db}/C_{gs} + \beta_2}.$$  \hspace{1cm} (3-41)

Since the noise from M1 and M2 are uncorrelated, the spectral density (PSD) of total output noise current is superposition of three noise sources: source, M1 and M2.

$$\overline{i_{n}^2} = \overline{i_{n-1}^2} + \overline{i_{n-2}^2} + \overline{i_s^2} = \frac{[\beta_2]^2 \overline{i_{g2}^2} + C_r \overline{i_{d2}^2} - 2|\beta_2|C_r \overline{i_x^2} \sqrt{\overline{i_d^2}} + |\beta_2|^2 \overline{i_x^2} + |\beta_2|^2 (g_{m1}/2Q_{gs})^2 v_n^2}{C_r + |\beta_2|^2}.$$
\[ F = F_1 + 4 \cdot \frac{\delta/5 + \gamma C_r^2 - 2 |\gamma| C_r \sqrt{\gamma \delta/5} \sqrt{W_2/W_1}}{|\beta_1/\beta_2| Q_{gs}}. \] (3-42)

\( F_1 \) is defined in Equation 3-36. \( W_2 \) and \( W_i \) are the width of M2 and M1, respectively. This equation shows there is an optimal selection of \( Q_{gs} \) to minimize noise factor.

![Graph of noise contributions](image)

Figure 3-9. Noise contribution from a cascode amplifier.

To illustrate how \( Q_{gs} \) affects noise factor, Equation 3-41 is used to calculate total noise factor and noise contributions from different noise sources. Since there is no accurately measured \( \gamma \) and \( \delta \) ever reported for a 0.13-\( \mu \)m technology, we assume \( \gamma \) and \( \delta \) in short-channel device are 2 and 4, three times of their counterparts of long channel devices. Here \( Q_{ind} \) is set to be 20, which is the measured value for an inductor test structure around 24GHz. \( C_r \) is assumed to be 2. M2 and M1 are assumed to have same width.

Figure 3-9 shows that noise factor has a minimum point for at optimal \( Q_{gs, opt} \). Noise factor rapidly decreases with increasing \( Q_{gs} \) until reaching the minimum point, then slowly increasing with slope proportional to \( \delta/5 + 1/Q_{ind} \). It indicates that gate induced noise from M1 begins to...
dominate. The noise contribution from M2 monotonically decreases with $Q_{gs}$. Noise figure only varies ~0.1dB for $Q_{gs}$ from 2 to 3. It could be labeled as an “optimal” region since noise factor does not change much due to the $Q_{gs}$ variations resulting from technology variation.

3.4 24GHz CMOS LNA Implementation

Following the theoretical analysis of the LNA design, several circuits have been implemented in the UMC 130-nm CMOS logic process. In BSIM3v3 model, thermal channel noise factor $\gamma$ is fixed to be 2/3 and induced gate noise factor is ignored. These inaccurate modeling parameters will cause selection of $Q_{gs}$ and the noise simulation results inaccurate. $Q_{gs}$ in the design are set to 3.2 and it can tolerate 10% component variations [51]. Higher $Q_{gs}$ means smaller transistor size for a fixed resonant frequency and it also means lower power consumption for a fixed gate bias of M1. In the 130-nm technology, supply voltage is 1.2V and voltage headroom is limited. These LNAs are designed to operate at ~24GHz which is the working frequency of $\mu$Node, while consuming as little power as possible.

3.4.1 A 24-GHz Single-Ended CMOS LNA

Figure 3-10(A) shows the schematic of the single-ended LNA. The CMOS transistors M_1 and M_2 chosen in this circuit are 14 fingers with total width of 14μm. The measured cut-off frequency $f_T$ is about 60~70GHz. Two 6-pF bypass capacitors are put between V_{dd}, V_{g2} and ground to eliminate any inductance effect associated with wires connected to these two nodes. The bypass capacitors are implemented with accumulation-mode MOS capacitors in an n-well with capacitance density of ~11fF/μm$^2$. Since capacitors $C_I$ and $C_2$ in the signal path are for capacitively transforming impedance and de-coupling the dc output of the amplifier, voltage drop across this kind of capacitor may cause capacitance shift. More importantly, the large parasitic capacitance and substrate reactance associated with the n-well will degrade the gain performance, especially that of $C_I$. These two capacitors are implemented with metal-to-metal
capacitor structures. The other benefit of metal-to-metal capacitor is much higher $Q$ than that of MOS capacitors. Using Metal 5-8 gives a capacitance density of $\sim$26fF/100$\mu$m$^2$. The parasitic capacitance to ground is $\sim$20% of desired capacitance. UMC 0.13$\mu$m technology offers 8 copper layers. The skin depth (in $\mu$m) in copper at frequency $f$ (in GHz) is
\[
\delta(\mu m) = \frac{1}{\sqrt{\pi \mu \sigma f}} = \frac{2.1}{\sqrt{f}}.
\] (3-43)

where $\mu=1.26\times10^{-6} \ (H/m)$ and $\sigma = 5.8\times10^7 \ /\Omega \cdot m$ for copper. At 24GHz, the skin depth is 0.42$\mu$m.

To reduce the resistive loss, stacked metal layers are preferred to implement inductors to increase quality factor ($Q$) [55]. Especially, the resistance of $L_g$ degrades the NF of the LNA. However, use of multiple metal layers significantly increases the parasitic capacitance and lowers the self-resonance frequency of the 1-nH gate inductor ($L_g$). Because of this, the inductors are implemented using the 0.8-$\mu$m-thick top metal layer. The metal thickness is twice of the skin depth so that whole vertical dimension of metal layer is conducting AC current. To reduce the resistive loss, a wider inductor trace is preferred. But, once again, increasing parasitic capacitance lowers the self-resonance. To balance these two opposite tendencies, the inductor trace width of 3$\mu$m is used. The space between inductor traces is set to 3$\mu$m to reduce the proximity effect. A polysilicon ground shield is placed underneath the inductor [52]-[54] to reduce the loss resulting from capacitive coupling to silicon substrate. Since the $Q$ of output network is dependent on $Q_d$ of load inductor $L_d$ (0.73nH), to tolerate the process variation, $Q_d$ is set to 14. The trace width is 2$\mu$m for $L_d$. $L_s$ in the circuit is only 120pH and it is designed with a short metal line. Figure 3-10(B) shows the die microphotograph. The chip size is 500$\mu$m $\times$ 320$\mu$m including pads.

The circuit is probed with GGB ground-signal (GS) probes. M1 is biased using an off-chip bias tee. The gate voltage of M2 is set to Vdd. The $S$-parameters are measured with an HP8510C.
network analyzer. The measurement result is shown in Figure 3-11. Biased at 1.9mA from a 1.2-V supply, $|S_{21}|$ has a peak of 6.1dB at 23.5GHz. The minimum NF is 5dB, as shown in Figure 3-12. The linearity is measured with 2 tone input signals at 23.5GHz and 23.51GHz. Input referred third-order intercept point (IIP3) is -6dBm, as shown in Figure 3-13.

Figure 3-10. Single-ended LNA. A) a schematic and B) a die photo.
Figure 3-11. S-parameter of the LNA.

Figure 3-12. Noise figure of the LNA.
3.4.2 A 24-GHz Differential CMOS LNA

A single-ended LNA is sensitive to parasitic ground inductance. The end of the source degeneration inductor ($L_s$) connected to ground is supposed to be at the same potential as the ground bond pad. However, there is always voltage drop between these two points because there is always some finite impedance between them which can have a large effect on amplifier performance. Even worse, it can form a parasitic feedback loop from following stages, and the amplifier can become potentially unstable. Generally, this issue is not severe on-chip since the distance between these two points is sufficiently short. However, at 24GHz and higher, this can no longer be neglected. An alternative is to exploit the virtual ground located at the symmetry point of a differential structure. Any series parasitic impedance connected to common-mode nodes will not affect input matching impedance. Another important advantage of differential topology is common-mode signal rejection. To maximize common-mode rejection at high frequencies, it is important to keep symmetry in layout.
Figure 3-14. Differential LNA (a) Schematic and (b) Die photo.
Figure 3-15. S-parameters of differential LNA.

Figure 3-16. NF of the differential LNA.
Figure 3-17. IIP<sub>3</sub> of the differential LNA.

At the same DC bias, a differential LNA consumes twice as much power of that of a single-ended amplifier with the same gain and NF. The linearity of differential LNA is improved because input power is split and each of input devices only sees half of voltage compared to single-ended counterpart. The schematic of the differential LNA is shown in Figure 3-14(A). An additional inductor $L_{com}$ is added at the common node of input differential pair (M1 and M2) to resonate with parasitic capacitances of $L_{s1}$ and $L_{s2}$. This increases the impedance at resonant frequency and enhances the common-mode rejection. The die photo is shown in Figure 3-14(B). The differential LNA occupies 500 $\mu$m × 660 $\mu$m including bond pads, which is ~2× of the single-ended one.

The LNA is measured with ground-signal-signal-ground (GSSG) probes. The single-ended output of network analyzer is converted to differential signals using a balun. The measured S-parameters are shown in Figure 3-15. At 23.5GHz, $|S_{21}|$ is 6dB at 1.2-V $V_{dd}$. The dc bias current
is 3.3mA. Power consumption is 4mW. The measured NF of the differential LNA is 5.3dB at 23.5GHz, shown in Figure 3-16. Figure 3-17 shows the linearity measurement result. The IIP3 of differential LNA is -2.4dBm, ~3dB higher than that of a single-ended one. Table 3-1 summaries the performance of the single-ended and differential LNAs.

Table 3-1. Summary of performance of single-ended and differential LNA.

<table>
<thead>
<tr>
<th>LNA Topology</th>
<th>Current (mA)</th>
<th>Power (mA)</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
<th>IIP3 (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-ended LNA</td>
<td>1.9</td>
<td>2.3</td>
<td>6.1</td>
<td>5</td>
<td>-6</td>
</tr>
<tr>
<td>Differential LNA</td>
<td>3.3</td>
<td>4</td>
<td>6</td>
<td>5.3</td>
<td>-2.4</td>
</tr>
</tbody>
</table>

3.4.3 Device Characteristic

![Substrate network of a MOSFET. A) Simple substrate network. B) Substrate network model of [45].](image)

Figure 3-18. Substrate network of a MOSFET. A) Simple substrate network. B) Substrate network model of [45].

The measured gain of LNA is significantly lower than that of simulated one which is ~13dB. One major reason of the mismatch is inaccurate device modeling. Although BSIM3 model has been demonstrated accuracy in device’s DC characteristics and sufficiently validated for relatively low frequency applications, it requires modifications for uses at 24GHz [44]. One important factor is that substrate resistance is neglected in BSIM3v3 model. To take account for the effect of substrate resistance, two ways for augmenting the core transistor based on BSIM3v3 model are shown in Figure 3-18. Both models use extrinsic capacitances to account for source/drain body junction capacitances. The diode capacitances of MOSFETs are set to zero. So
bias-dependant capacitance has to be extracted from measurement instead of being defined by simulator. Figure 3-18(A) shows the approach of connecting a resistor to the bulk node. The output impedance consists of \( C_{jb} \) in series with \( R_{sub} \). When the transistor is off (gate bias is zero), \( r_o \) of the transistor is large so that the real part of impedance looking into the drain node is \( R_{sub} \) at low frequencies. It is expected that at high frequencies \( C_{jb} \) tends to bypass the signal, reducing the real part of substrate impedance from \( R_{sub} \) towards zero. However, the measurement shows a constant \( R \) over a large frequency range [44]. Simply adding a substrate resistance to the bulk node of the transistor does not properly model the substrate resistance effect. A new BSIM3v3 RF model [45] is realized by adding \( R_g, R_{db} \) and \( R_{sb} \) as shown in Figure 3-18(B). The substrate resistance and drain junction capacitance can be extracted after converting S-parameters to y-parameters,

\[
R_{db} = \text{real}(1/(y22 + y12)) \\
C_{db} = 1/(\omega \cdot \text{imag}(1/(y22 + y12))).
\]  

(3-44)

Figure 3-19. Extracted \( R_{db} \) and \( C_{db} \).
Since source is connected to ground, \( R_{sb} \) can not be extracted. \( R_{sb} \) and \( R_{db} \) may not be the same since they are determined by the layout. The extracted \( R_{db} \) and \( C_{db} \) are shown in Figure 3-19. At 24GHz, \( R_{db} \) is \( \sim 42 \Omega \) and \( C_{db} \) is \( \sim 18 \text{fF} \), giving an equivalent parallel output resistance

\[
R_{out} = R_{db} \left( \frac{1}{\omega C_{db} R_{db}} \right)^2 = 3.2 K\Omega
\]  

This means \( R_{db} \) further lowers the output resistance of the transistor, considering smaller \( r_o \) of short channel devices. The total output resistance is \( R_{out}/r_o \), which means significant reduction of gain. \( R_{db} \) and \( R_{sb} \) also contribute to output noise. A cascode amplifier is simulated with 14-\( \mu \)m wide common source and common gate transistors.

![Figure 3-20](image.png)

Figure 3-20. \( R_{sb} \) effect on output resistance of a cascode amplifier.

The amplifier output resistance with and without \( R_{sb} \) is plotted in Figure 3-20. At lower frequencies, \( R_{sb} \) does not make much difference. However, at 24-GHz operating frequency, the output resistance drops by \( \sim 30\% \) in the presence of \( R_{sb} \).
3.4.4 A 26-GHz CMOS LNA with Negative Impedance

To achieve higher gain, there are two choices: cascading more stages or boosting single stage LNA gain by consuming more power. However, increasing power is not acceptable for μNode applications. To overcome the loss associated with substrate resistance, negative resistance is generated in the signal path [58]. Cross-coupled VCO-like circuitry has been demonstrated in [46]. But it introduces additional power consumption.

![Figure 3-21. Schemes for generating negative resistance. A) Source follower with capacitive load. B) Gate inductor at a common-gate amplifier.](image)

Figure 3-21(A) shows a source-follower with a capacitive load. The impedance looking into the gate is

\[
Z_{in1} = \frac{1}{j\omega C_{gs}} - \frac{\omega r}{\omega^2 C} + \frac{1}{j\omega C}. \tag{3-46}
\]

The circuit generates negative resistance \(-\omega r/\omega^2 C\). In [57], such a source-follower was used after an amplifier containing an inductive load. The negative resistance compensates the resistive loss in the inductor causing effective Q of the inductor to increase. However, the stability of whole circuit must be ensured which requires proper selection of the value of capacitance C. To implement the source follower it requires one extra stage which means more power consumption. Figure 3-21 (B) shows another means of generating negative resistance. It is
well known that a series gate inductor in a common-gate amplifier introduces negative resistance looking into the source. The impedance looking into the source of transistor, assuming \( r_o \) is relatively large (~3kΩ), is

\[
R_{in} \approx \frac{1}{g_m} - \omega^2 L/\omega T
\]

(3-47)

where \( \omega_T \) is \( g_m/C_{gs} \). In a cascode amplifier, the negative resistance (the second term in right hand side) can be generated without adding an additional stage that consumes power by simply adding a gate series inductor in the common-gate stage as shown in Figure 3-22 (A).

Incidentally, the LNA in [56] is configured in the same way. The resonant frequency of \( L_{g2} - C_{gs2} \) series network is much higher than the tuned frequency and it is proposed to create a notch in \( |S_{12}| \) to improve the stability. Looking at the output impedance of cascode amplifier, when the impedance looking into the drain of M1 is defined as \( Z_{d1} \), the output impedance and transconductance at drain node of M2 are,

\[
Z_{d2} \approx r_0 + \frac{Z_{d1} r_0}{\frac{1}{\omega_T C_{gs}} - \omega^2 L_{g2}/\omega_T + j\omega Z_{d1}/\omega_T}
\]

(3-48)

\[
G_m = \omega_T /((C_{d1} (\omega^2 L_g - 1/C_{gs}) - 1) j\omega - \omega_T).
\]

(3-49)

Increasing \( L_{g2} \) lowers the resistance in the denominator which increases the output impedance and increases transconductance. At a given gain, this allows the transconductance or bias current to be lowered, which further increases \( r_o \) of the transistors and output impedance. At the resonant frequency, the total simulated impedance at M2 drain node including \( Z_{d2} \), impedance of \( L_d \) and impedance looking into capacitive transformer (\( C_1 \), \( C_2 \) and 50-Ω load) is increased to 701 from 492Ω when \( L_{g2} \) of 0.76nH is added, while the short circuit transconductance at this node is increased by ~15%. These increase the gain by 4.1dB despite the slight decrease of the voltage gain of common-source stage. The load inductor \( L_d \) is 0.68nH.
$L_{g2}$ is 0.76nH which gives $L_{g2}$-$C_{gs2}$ series resonant frequency of ~36GHz. A microphotograph of the LNA is shown in Figure 3-22 (B). The chip size is 0.45x0.36mm$^2$ including the bond pads.

The S-parameters of LNA are measured on-wafer using an Agilent E8361A network analyzer and are shown in Figure 3-23(A).

Figure 3-22. The LNA with an inductor at the gate of M2. (A) Schematic and (B) Die photo.
Figure 3-23. S-parameters and NF measurement of the LNA.

The maximum transducer gain (|S_{21}|) is 8.4dB at 26.2GHz, while the reverse isolation |S_{12}| is -19.6dB. |S_{11}| is -8.9dB and |S_{22}| is -5.4dB at 26.2 GHz. S_{22} is mistuned due to the C_1 being ~50% larger. The dc bias current is 0.8mA and V_{DD} is 1.0V. When the supply voltage is increased to 1.2V, |S_{21}| can be increased to 13dB with power consumption of 2.4mW. Noise figures are measured using an HP8970B noise figure meter and an external mixer, and the de-
embedding technique was discussed in [59]. Limited by the instrument, noise figures are measured only up to 26.5GHz. The measured NF is ~5 dB at 26.2GHz, which is shown in Figure 3-23(B).

Figure 3-24. Stability circles of A) input and B) output.

Stability is a serious issue for using negative resistance cancellation techniques. The stability factor, $K$ ranges between 0 and 1 from 26.4 to 31.3GHz. $B1$ is always larger than 0. In this frequency range, the amplifier is not unconditionally stable. This is due to the mismatch between peak $|S_{21}|$ and output matching ($|S_{22}|$) frequencies. The input and output stability circles for 26.3 to 30.5GHz are drawn using the measured S-parameters and shown in Figure 3-24(A) using method in [60]. The LNA is stable in ~75% of the $\Gamma_S$ plane. The LNA input typically sees the output of a filter or an antenna whose impedances can significantly vary, and this is a potential limitation. As shown in Figure 3-24(B), the LNA is stable in ~90% of the $\Gamma_L$ plane. Since the LNA will eventually be integrated with other components that have known and well controlled impedances, it should be possible to make sure the load for the LNA is within the stable region. Simulations indicate that the potential instability near the tuned frequency is not an inherent consequence of using the negative resistance circuit and it should be possible to re-tune
the circuit so that is unconditionally stable over a bandwidth of 10 GHz around the tuned frequency.

Figure 3-25. IIP3 of the LNA.

The input referred third order intercept point (IIP3) of LNA is measured with two-tone input signals at 26.2 and 26.21GHz. IIP3 is -13dBm, as shown in Figure 3-25. This is ~7dB lower than that of the amplifier without the negative resistance circuit. The simulated voltage drop across the gate and source of M2 is 1.8 times of that of M1 and the linearity of this circuit is limited by M2.

Table 3-2 compares the performance of CMOS LNAs working above 20GHz. The LNA with a gate inductor at M2 has reasonable gain and NF performance compared to most of the previously reported LNAs while consuming significantly lower power. Compared to the 24-GHz single-ended LNA without $L_{g2}$ fabricated in the same 130-nm CMOS process, the power gain is ~ 2 dB higher while consuming ~ one-third of the power. It should be possible to achieve gain of
~16dB by using a two stage design and doubling the power consumption. Even after this, the circuit should consume power that is more than 5× lower.

Table 3-2. Performance comparison between LNAs above 20GHz.

<table>
<thead>
<tr>
<th>Circuit Metrics</th>
<th>This work [58]</th>
<th>W/O $L_{g2}$</th>
<th>[62]</th>
<th>[64]</th>
<th>[59]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.13-μm CMOS</td>
<td>0.13-μm CMOS</td>
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<td>54</td>
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</tbody>
</table>

3.5 Summary

In this chapter, the topologies of CG-LNA and CS-LNA are compared. It shows with the same DC bias current, the CS-LNA achieves higher gain because of quality factor of the input network. Because of this, CS-LNA is better suited for low-power applications, like μNode. Then noise figure of CS-LNA and cascode LNA are analyzed. An “optimal” region of quality factor $Q_{gs}$ of input $L-C-R$ network is found to be 2-3 to minimize noise figure. Within this region, the design can tolerate the component variations of $\pm 10\%$.

Single-ended and differential LNAs working at ~24GHz have been implemented in a digital 130-nm CMOS technology. By comparing simulated and measured LNA performance, it is found that the substrate resistance and junction capacitance play important roles in determining the gain of LNA. By judicious use of negative resistance, a 26-GHz LNA achieving
a gain of 8.4dB and a noise figure of ~5dB at DC power consumption of 0.8mW and $V_{dd}$ of 1.0 V is demonstrated. This work has shown that adding a gate inductor to the common-gate stage in a cascode amplifier can significantly improve the power efficiency.
CHAPTER 4
20GHZ RF FRONT END DESIGN

4.1 Introduction

An RF front-end including an LNA and a mixer is key component in modern communication systems. The LNA amplifies weak received signal and suppresses the noise contribution from the mixer. The mixer actually performs frequency translation. This chapter first discusses mixer design in section 4.2. Then a 20-GHz RF front-end implemented in a 130-nm CMOS technology is demonstrated in section 4.3. Using this RF front-end with an on-chip antenna as a receiver, 20-GHz AM signal transmitted from 5-m away is successfully picked up and down-converted to intermediate frequency (IF). An RF front-end with additional IF amplifying stage is presented in section 4.4.

4.2 Active Mixer

A mixer in a wireless receiver down-converts an incoming RF signal to an IF. This allows amplification to take place at lower frequency [65] and relaxes the selectivity of IF filter. The earliest radios used 2nd-order non-linearity in devices and later on used analog multiplication to accomplish the frequency translation. When local oscillator (LO) signal for the multiplication is high enough, it eventually drives the circuit to work in a switching mode. The principle of switching is illustrated in Figure 4-1. RF signal, represented as a sinusoidal \( rf(t) \), is multiplied by a mixing function, an ideal square wave local oscillator, \( LO(t) \) varying between +1 and -1. The LO signal toggles the polarity of RF signal at the output. It is easy to see the frequency translation in the frequency domain. The spurs in the output spectrum can be filtered out. RF signal can be either current or voltage and a mixer can be either active or passive. An active mixer consists of a transconductor (M3) and switching pairs (M1 and M2) for current commutation, as shown in Figure 4-2.
Figure 4-1. Switching mode of mixer.

Figure 4-2. Active mixer. A) Single-balanced mixer. B) Equivalent circuit.
4.2.1 Conversion Gain

In an active mixer, the switches reverse the polarity of the load current at the LO frequency. The transcondutance current is

\[ I_{cf}(t) = g_m V_{cf} \cos(\omega_{cf} t). \]  

The LO is a square wave generating a mixing function, it can be expressed as Fourier series,

\[ V_{LO}(t) = \frac{4}{\pi} \sum_k \left[ \sin(k\pi) \cos(k\omega_{LO} t) \right]. \]

The output current will be the product of the current \( I_{cf}(t) \) and mixing function \( V_{LO}(t) \), then output voltage is this current times output load, \( R_L \).

\[ V_{out}(t) = g_m R_L \frac{4}{\pi} \left[ \cos(\omega_{LO} t) - \frac{1}{3} \cos(3\omega_{LO} t) \cdots \right] V_{cf} \cos(\omega_{cf} t), \]

Ignoring the harmonics of LO gives

\[ V_{out}(t) = g_m V_{cf} R_L \left( \frac{4}{\pi} \frac{1}{2} \cos(\omega_{cf} - \omega_{LO}) t + \frac{1}{2} \cos(\omega_{cf} + \omega_{LO}) t \right). \]

Eliminating the upconverted term, the resulting down-converted signal at output is

\[ V_{out}(t) = g_m V_{cf} R_L \frac{2}{\pi} \cos(\omega_{cf} - \omega_{LO}) t. \]

Therefore, assuming a perfect square wave LO, the voltage conversion gain through the mixer is given by the well known expression

\[ A_v = g_m R_L \frac{2}{\pi}. \]

The expression only holds when the LO voltage is large compared to the \( V_{gs} - V_{th} \) of the switching devices. However, this assumption is barely satisfied in most cases where the LO is driven by the output of an on-chip VCO or PLL, which is generally a sinusoidal wave. More
accurate voltage gain estimation is given in [66]. It takes into account the time when both of switches are conducting current by averaging the voltage gain over one period of the local oscillator. When the differential LO amplitude is sufficient high, only one transistor in the switching pair carries DC current from M3, turning off the other. It is found in [67] that this amplitude is \[ \sqrt{2}(V_{gs} - V_{th})_{SW} \] where \((V_{gs} - V_{th})_{SW}\) is the DC gate overdrive of switching transistors is. If the LO amplitude is less than this critical value, both transistors are conducting current.

Assuming the local oscillator can be represented as a sinusoidal wave, \(V_{LO}(t) = V_{LO} \sin(\omega_{LO}t)\), the time that the switches move from the state when both switches conduct current, denoted \(t_{BAL}\), to another state when only one of the two devices are conducting current can be determined by the following relationship:

\[
V_{LO}(t) = \sqrt{2}(V_{gs} - V_{th})_{SW} = V_{LO} \sin(\omega_{LO}t_{BAL}).
\]

(4-7)

Assuming \(\sin(x) \approx x\) for small \(x\), this gives

\[
t_{BAL} = \frac{\sqrt{2}(V_{gs} - V_{th})_{SW}}{V_{LO}\omega_{LO}}.
\]

(4-8)

During time \(4t_{BAL}\) in one LO period, both switches are on and the RF current appears at the common mode nodes of the differential pair which does not contribute to differential output current. Only the current during the period when one switch is on contributes to output voltage.

So the conversion gain can be rewritten as [66],

\[
A_v = g_m R_L \left( \frac{2}{\pi} \right) \left( 1 - \frac{4t_{BAL}}{T_{LO}} \right) = g_m R_L \left( \frac{2}{\pi} \right) \left( 1 - \frac{2\sqrt{2}(V_{gs} - V_{th})_{SW}}{\pi V_{LO}} \right).
\]

(4-9)

Figure 4-3 shows mixer gain changes from ideal switching in Eq. (4-6) with ratio of LO signal amplitude to \((V_{gs} - V_{th})_{SW}\). To make a mixer work with less than 3-dB gain drop from the ideal switching, an LO signal amplitude should be at least \(3 \times (V_{gs} - V_{th})_{SW}\).
4.2.2 Noise in Active Mixer

The noise analysis in a mixer is different from the traditional white noise analysis for linear and time invariant systems. In a mixer, the frequency domain method is suitable for RF noise in the transconductor, but not for the noise from the switching pair. The noise of switching pair can be solved using a stochastic differential equation (SDE) [68], [69]. However, it involves numerical solution not intuitive. So the mixer noise analysis follows the method in [70].

Let’s assume ideal switching for a mixer. The mixing function in Equation 4-2 only generates signals at fundamental frequency and its odd harmonics. As shown in Figure 4-4, The LO frequency and its odd harmonics will down-convert the respective frequency band of white noise to IF [71]. The noise is uncorrelated at each sideband and frequency, and various noise power contributions can be simply summed. The total output spectral density at IF due to transconductor M3 in Figure 4-2 is

$$\bar{i}_n^2 = \bar{i}_{n3}^2 \cdot 2 \cdot \left( \frac{2}{\pi} \right)^2 \left( 1 + \frac{1}{3^2} + \frac{1}{5^2} + \cdots \right) = \bar{i}_{n3}^2 \cdot 2 \cdot \left( \frac{2}{\pi} \right)^2 \frac{\pi^2}{8} \equiv \bar{i}_{n3}^2.$$  \hspace{1cm} (4-10)
where $i_{n3}^2$ is the channel thermal noise of M3. The first term is the white noise at $f_{LO} \pm f_{IF}$ down-converted by the fundamental of LO, the second term is noise at $3f_{LO} \pm f_{IF}$ down-converted by the third harmonic of the LO, whose amplitude is one third of the main harmonic of the LO, and so on. Equation 4-10 says that the thermal noise current in the transconductor is totally transferred to mixer output, just like in an amplifier. This is due to the fact that the noise is periodically inverted without changing the general properties of noise in time domain [63].

![Diagram](image)

Figure 4-4. Frequency translation of white noise in a transconductor.

### 4.2.3 Thermal Noise from Switching Pair

When LO voltage is much greater than $\sqrt{2(V_{gs} - V_{th})_{SW}}$ of the switches, the LO switches behave like the common gate stage of a cascode amplifier and there is minimal output noise
contribution from the switching transistors. When LO voltage is less than \( \sqrt{2(V_{gs} - V_{th})_{SW}} \) of the switches, the LO switches behave like a differential pair.

![Figure 4-5. Time varying transconductance G(t).](image)

During the time interval \( \Delta \) in Figure 4-5, both M1 and M2 are turned on and contribute to the output noise. It is shown in [70] that the time variant noise PSD at one output port is

\[
4kT \gamma \left( \frac{1}{g_{m1}} \left( \frac{g_{m1}}{1 + g_{m1} / g_{m2}} \right)^2 + \frac{1}{g_{m2}} \left( \frac{g_{m2}}{1 + g_{m2} / g_{m1}} \right)^2 \right) = 4kT \gamma \left( \frac{g_{m1} \cdot g_{m2}}{g_{m1} + g_{m2}} \right).
\]  

(4-11)

The corresponding total output noise PSD of the mixer, which is twice of that at one port, is

\[
\bar{i}_n^2 = 16kT \gamma \left( \frac{g_{m1} \cdot g_{m2}}{g_{m1} + g_{m2}} \right) = 8kT \gamma G(t),
\]  

(4-12)

Where

\[
G(t) = 2 \frac{g_{m1} \cdot g_{m2}}{g_{m1} + g_{m2}}.
\]
is the transconductance of differential pair. As shown in Figure 4-5, the transconductance and output noise is periodic. \( V_x \) is “threshold voltage” which is \( \sqrt{2}(V_{gs} - V_{sb})_{SW} \) determining whether one transistor or both transistors conduct current. When \( V_{LO} > |V_x| \), the differential signal is so strong that only one transistor is on while the other is turned off.

The time-average PSD at the output is

\[
\bar{i_n^2} = 8kT\gamma \left( \frac{1}{T_{LO}} \int_{0}^{T_{LO}} G(t)dt \right) = 8kT\gamma \bar{G}. \tag{4-13}
\]

The output noise is dependent on the average of \( G(t) \). As shown in Figure 4-5, \( G(t) \) can be approximated as a triangle shape with a period of \( T_{LO}/2 \). \( G(t) \) is determined by the smaller of \( g_{m1} \) or \( g_{m2} \). It reaches the maximum when \( g_{m1} \) and \( g_{m2} \) are equal. This point is located at zero crossing of \( V_{LO} \) which means the gate bias of \( M1 \) and \( M2 \) are equal. The average of \( G(t) \) can be calculated by the area of one triangle divided by a half period of \( LO \). The area of triangle is determined by the peak transconductance and turn-on time \( \Delta \) of both transistors.

Considering

\[
V_x = V_{LO} \sin(\omega t) \rightarrow \frac{\Delta}{2} = \arcsin \frac{V_x}{V_{LO}} / \omega \Rightarrow \Delta = \frac{V_x T_{LO}}{\pi V_{LO}}
\]

\[
\bar{G} = \frac{G_{max} \Delta/2}{T_{LO}/2} = \frac{g_m V_x}{\pi V_{LO}} = \frac{2I_R}{\pi V_{LO}}. \tag{4-14}
\]

The total output noise spectral density is given as

\[
\bar{i_n^2} = 4kT\gamma g_m + 8kT\gamma \frac{2I_R}{\pi V_{LO}}. \tag{4-15}
\]

The same conclusion on mixer noise dependence on \( LO \) signal amplitude and bias current is given in [71]. The mixer in [72] is the same as the mixer used in this work. A NF vs. \( LO \) power plot is shown Figure 4-6. It shows that increasing \( LO \) power lowers noise figure.
Figure 4-6. NF vs. LO power of Mixer.

In mixer design, higher bias current increases the transconductance of M3 and therefore the conversion gain. Even though the output noise contributed by M1 and M2 are increased by $I_B$ as shown in Equation 4-15 noise figure of mixer is reduced. A larger LO amplitude increases the conversion gain and reduces the noise contribution of switching pair. Increasing the channel width of M3 is desirable because this increase $g_{m3}$ and therefore the conversion gain and reduces the noise figure. However, larger channel width of M3 introduces parasitic capacitance, which can degrade the performance at high frequencies and increases the load for the circuit driving the mixer.

4.3 A 20-GHz Font End with On-chip Antenna

A 20-GHz RF front-end with an on-chip antenna has been developed to demonstrate the feasibility of µNode concept. To lower the overall power consumption of the receiver, the gain of down-converter is kept as low as possible while achieving sufficiently low noise figure. Fully differential circuits though consume more power are utilized to make the connection to the
dipole antenna without using a balun as well as to better reject the common-mode noise from the digital circuits which will eventually be integrated.

Figure 4-7. Schematic of LNA and Mixer.

Figure 4-7 shows the schematic of the RF Front-end including an LNA and a mixer. The LNA utilizes the cascode topology. Source degeneration is used to generate resistance for input matching. The output of LNA is capacitively coupled to the mixer. The mixer is double-balanced Gilbert cell type. The conversion gain of the mixer is ~1dB. A differential inductor is inserted between the drain nodes of two Tran conductors (M5 and M6) to tune out the capacitance at these two nodes. This increases the mixer gain and improves the image rejection of down-converter [79]. For testing, each IF output is matched to 50Ω. The current sources in the LNA and mixer are replaced by inductors to provide larger voltage headroom. Shielded pads are put underneath both RF and LO ports to prevent the loss of signal and noise coupling associated with
substrate resistance [80]. Ground rings are placed around the transistors at minimum distance to reduce the substrate loss. The gate of LNA and mixer are biased through 5-kΩ polysilicon resistors. The LNA and mixer have separate supplies and large on-chip bypass capacitors are placed between each supply and ground.

Figure 4-8. Die micrograph and antenna cross section.

The performance of wireless communication is critically dependent on antenna. The recent work [81] has shown on-chip antennas built on moderate-resistivity substrates (5-20 Ω) sufficient for use up to 5m and possibly larger separations. The antenna used in this work is a 3mm-long zigzag dipole with a bend angle of 30°, shown in Figure 4-8. The 3-mm length corresponds to ~λ/4 at 20GHz in free space. To reduce the antenna resistance, antenna built with a thick metal layer is preferred. However, the technology only offers 0.34μm-thick metal 1-6 layers. The antenna is implemented in metal 1-4 layers to make the thickness of metal layers used to fabricate on-chip antennas comparable to that of the previous work [81]. The design rule limits the maximum metal width to 10μm. To satisfy the maximum metal-width rule, the antenna is formed with 3-parallel 8μm traces separated by 0.8μm. The antenna is located ~50μm from the
chip edge. It is shown in [81] that closer distance between on-chip antenna and chip edge reduces the attenuation due to lossy substrate. The die micrograph is shown in Figure 4-8. Antenna traces cannot be seen, since they are built with the lowest 4 metal layers. The antenna is drawn to illustrate the size and shape of the whole circuit. The antenna area is 3mm × 120μm while the RF front-end excluding the antenna is 880 × 830μm². The total area is 1.1mm².

![Reflection coefficient at IF and RF ports.](image)

Figure 4-9. Reflection coefficient at IF and RF ports.

To characterize the downconverter performance, the antenna is cut from the LNA and mixer. S-parameters are measured at IF and RF ports by using HP8510C network analyzer. RF, IF and LO ports are probed using ground-signal-signal-group (GSSG) probes. The reflection coefficient is shown in Figure 4-9. At IF port, the reflection coefficient is below -10dB from 2.4GHz to 3.1GHz. At RF port, the reflection coefficient is below -10dB from 19.5GHz to 21.1GHz. The RF input and IF outputs are well matched at their respective frequencies.
The conversion gain and noise figure measurements are performed at 1.5-V and 1.2-V supply voltage. The results are shown in Figure 4-10. The power gain is measured as a function of the RF input frequency. The LO frequency 3GHz below the RF frequency was swept with the RF frequency. The external LO power applied to one LO port is 2dBm, equivalent to a peak-to-peak voltage swing of 0.8V. The power gain of RF image is also measured. It is measured at the corresponding RF image frequency. For instance, the image of 20-GHz RF signal is located at 14GHz, two times IF frequency away from the 20-GHz RF frequency. The image rejection of the front-end is 24dB at 20GHz. This performance is achieved by using large IF and properly tuning LNA and mixer. The single side band (SSB) NF is measured as a function of the RF input frequency with fixed LO frequency of 17GHz.
Figure 4-11. Linearity of down-converter at $V_{dd}$ of A) 1.2V and B) 1.5V.
Besides being the first receiver fabricated in a low cost foundry process to have an on-chip antenna, the circuit achieves 9 and 6.6dB conversion gain and SSB noise figure at 20GHz, while consuming extremely low power of 12.8mW with V_{dd}=1.5V. Compared to the LNA and mixer combination of a 17-GHz front-end fabricated in a 130-nm CMOS technology [62], which has been shown to possess competitive overall performance as receivers fabricated using a 100-GHz f_T SiGe BiCMOS technology [77], [78], the down-converter has comparable noise performance while consuming less than half of the power. When the supply voltage is reduced to 1.2V, the circuit has a maximum power gain of 7dB, minimum NF of 7.2dB. The power consumption is less than 25% of the LNA and mixer in [62]. The linearity is measured with two RF tones at 20GHz and 20.02GHz with LO signal of 17GHz. Figure 4-11 shows the IIP3 measurement with supply voltage of 1.2V and 1.5V. Table 4-1 summaries the measurement results.

<table>
<thead>
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<th>Table 4-1. Performance of the RF front-end</th>
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<tr>
<td>Mixer Current</td>
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<tr>
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</tr>
<tr>
<td>Noise Figure</td>
</tr>
<tr>
<td>Input IP3</td>
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</tbody>
</table>

The operation of RF front-end with an on-chip antenna is demonstrated by transmission of an AM signal and down conversion of this signal to IF. The measurement setup is shown in Figure 4-12(A). The transmitted signal is generated by an Agilent 8254A. A 20-GHz carrier is amplitude modulated with 100-kHz sinewave with modulation depth of 50%. For a given modulation depth: \( m \), the power difference in dB between that for a carrier and the sideband on either side is expressed as,
\[ E_{sub}/E_c = -20\log(m) + 6 \text{ dB}. \] (4-16)

\[ E_{sub} \] represents the power level of an either sideband while \( E_c \) represents carrier power level. For \( m=50\% \), the power level difference between is 12dB.

![Diagram](image)

Figure 4-12. Interchip wireless communication over free space. A) Measurement setup and B) Measurement environment.

The single-ended AM signal is converted to balanced signals using a balun and fed to a transmitting antenna which is a 3-mm on-chip zigzag dipole with a signal-signal (SS) probe. The power delivered to the antenna is 10dBm. The transmitting antenna is placed on a mobile probe stand made of Derlin [81], which is type of plastic with dielectronic constant of ~3.7. The probe stand is located 5m away from the receiver. The receiver is mounted on a thick glass substrate isolating the effect from the metal chuck underneath. The RF, LO and IF biases are provided
using GSSG probes and DC probes. The IF output is amplified using an external amplifier with 26-dB gain. The measurement environment is shown in Figure 4-12(B) which is in the 5th-floor lab.

Figure 4-13. Received spectrum.

The received (resolution bandwidth of 300Hz) spectrum is examined by using an HP8563E spectrum analyzer. The output spectrum is shown in Figure 4-13. The power at 3GHz IF is ~53.8dBm. The power gain between transmitting antenna and receiving antenna is calculated to be ~99dB including the effects of metal structures. The two sidebands 100kHz away from the IF have power levels of ~66.5dBm and -66dBm, which are 12.7 and 12.2dB lower than that of the carrier. Those power levels are close to the theoretical values. This indicates that the transmitting RF signal is picked up by antenna and down-converted by RF front-end. The extra sidebands in the spectrum are due to spurs of signal generator. The background noise is ~2dB higher than that
of spectrum analyzer due to the noise resulting from the thermal noise of received signal and noise of the down-converter.

For the first time, this work [82] shows that a pair of ICs with a compact on-chip antenna can communicate over free space and it is feasible to implement a low-power 20-GHz down-converter using mainstream digital CMOS technology.

4.4 A 20-GHz RF Front End Including LNA, Mixer and IF Amplifier

The previous RF down-converter with LNA and mixer has only 9-dB gain. A two-stage IF amplifier is added to increase the overall gain to better suppress noise contributed by following analog baseband stages such as variable gain amplifier and low pass filter. Its schematic is shown in Figure 4-14. Figure 4-15 shows the diagram of this RF front-end. The circuit was once again implemented using UMC 130-nm CMOS logic technology. The die photograph is shown in Figure 4-15. The input/output reflection coefficients were measured with an HP8510C network analyzer, and shown in Figure 4-16. The circuit was once again implemented using UMC 130-nm CMOS logic technology.

![IF amplifier schematic.](image)

Figure 4-14. IF amplifier schematic.
Figure 4-15. A Front-end with an IF amplifier

Figure 4-16. Measured matching properties at IF and RF ports.
Figure 4-17. Power gains at input and image frequencies.

The conversion gain is measured at varying RF and LO frequencies, keeping the constant 3-GHz IF. As shown in Figure 4-17, the maximum power gain achieved is 24dB at 20.5GHz. The image rejection ratio is ~23dB. At 1.5-V Vdd, this RF front end only consumes 17.7-mW power while achieving 29.5-dB gain. Compared to the front-end with LNA, mixer and IF amplifier reported in [76] which achieves 34.7-dB at 58-mW power consumption, our circuit shows a significant power reduction. Table 4-2 compares the circuit in [76] and our circuit.

Table 4-2. Performance comparison between our down-converter and the one in [76].

<table>
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<th>Circuit metrics</th>
<th>[76]</th>
<th>Our work</th>
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<td>LNA Power (mW)</td>
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<td>3.5</td>
</tr>
<tr>
<td>Mixer Power (mW)</td>
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</tr>
<tr>
<td>IF Power (mW)</td>
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<tr>
<td>Total Power (mW)</td>
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</tr>
<tr>
<td>Gain (dB)</td>
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<td>24</td>
</tr>
</tbody>
</table>

4.5 Summary

This chapter first presented the μNode system requirement, then demonstrated an 20-GHz RF front-end with an on-chip antenna which can receive transmitted AM signal and down-
convert IF. This RF front-end consumes much lower power compared to those previously reported circuits. For the first time, we demonstrated the feasibility of a pair of ICs communicating with each other using on-chip antennas over free space. A RF down-converter including LNA, mixer and IF amplifier which achieves comparable gain performance while consuming much lower power has been demonstrated. These works show that it is feasible to implement low power 24-GHz communication devices.
CHAPTER 5
BUILDING BLOCKS OF RECEIVER

5.1 Introduction

This chapter discusses the design of building blocks in the RF receiver except the RF front-end presented in the previous chapter. Figure 5-1 shows a diagram of the receiver. The passive mixer is briefly described in section 5.2. Variable gain amplifier (VGA) design is discussed in section 5.3. A 2nd-order Butterworth low pass filter (LPF) design is presented in section 5.4. The divided-by-8 circuit is briefly described in section 5.5. The image rejection filter in LNA is discussed in section 5.6. Since the integrated transceiver shares one antenna, to reduce the loss associated with a conventional T/R switch, a distributed switch method described in section 5.7 is utilized. In this section, driving LO from the synthesizer is also briefly described.

![Diagram of µnode receiver.](image)

Figure 5-1. Diagram of µnode receiver.

5.2 Passive Mixer

The second down-conversion in the receiver chain is accomplished with a passive mixer, which consumes no dc power. MOSFETs can be easily used to realize the passive mixer. The advantage of passive mixer over active mixer is its higher linearity and lower 1/f noise. But a passive mixer does not provide conversion gain and isolation between RF and IF ports. Figure 5-2 shows a passive double-balanced mixer consisting of four transistors in a bridge configuration.
The differential signals $LO$ and $\overline{LO}$ turn on and turn off transistors to change the polarity of voltage at IF port. For instance, when $LO$ is high and $\overline{LO}$ is low, M1 and M4 are turned on and IF port has the same polarity as RF port. On the other hand, when $LO$ is low and $\overline{LO}$ is high, M2 and M3 are turned on and IF port has the opposite polarity as RF port.

Figure 5-2. Passive mixer.

Figure 5-3. Gain vs. LO power in a passive mixer.
The passive mixer was designed and implemented in a 130-nm CMOS technology by A. Verma [83]. All four transistors have width of 100 μm. This passive mixer is measured with 2.7-GHz RF and 2.6-GHz LO frequency. This sets IF at 100MHz. The passive mixer conversion gain vs. LO power is plotted in Figure 5-3. It shows that 2-dBm LO power corresponding to 0.4-V voltage amplitude will give ~6-dB loss. This passive mixer was modified for integration into final receiver design.

5.3 Variable Gain Amplifier (VGA)

Figure 5-4. Schematic of the VGA and its basic amplification stage.

A VGA adjusts receiver gain according to the received signal amplitude. The VGA needs to support 8 6-dB steps. A 6-dB amplifier is shown in Figure 5-4. Two R1 resistors form common mode feedback with two upper PMOSs. Two R2 resistors form source degeneration. If R2 is much smaller than the output impedance of two NMOS transistors, amplifier
transconductance is $1/R_2$. If $R_1$ is much smaller than the output impedance of two PMOS transistors, the output resistance of the amplifier is $R_1$. Then, the amplifier gain is defined by $R_1/R_2$. DC offset must be taken care of for circuits with high gain. The baseband circuit will have three high-pass filters, one in front of the VGA to handle offsets from the preceding stages, one in front of the last four stages of the VGA and one in front of the LPF to handle the offsets from the VGA. The poles of filters are located at $\sim 200\text{kHz}$ defined by a 1.5-pF AC coupling capacitor and a $500\text{-k}\Omega$ resistor.

![Gain control scheme](image)

The gain control method is shown in Figure 5-5. There are eight switches attached to the output of eight amplifier stages. These switches are controlled by $b_0$-$b_7$ generated by a 3-bit decoder. At each gain step setting, there is only one gate voltage set to high while all other are set to low. For instance, if the control pattern is “00000001”, only the switch controlled by $b_7$ is on and gain is 48dB. If the control pattern is “10000000” then the only switch controlled by $b_0$ is on and the VGA has the lowest gain of 6dB.
To measure the VGA, differential input signal has to be generated. A Balun used at high frequencies to convert single-ended signal to differential ones is replaced by a discrete differential amplifier (AD8138) [84]. As shown in Figure 5-6, two printed circuit boards (PCBs) are connected to the input and output of VGA by semi-rigid cables and two pairs of GSSG probes.

![Figure 5-6. Measurement setup of the VGA using differential amplifiers as Baluns.](image)

To measure the gain of VGA, two steps are needed. First a THRU structure on a GGB calibration substrate is used to connect two PCBs using the semi-rigid cables and GSSG probes. With a 2-MHz sine wave generated from an Agilent 33120A function generator, the power ($P_{\text{thru}}$) read from the spectrum analyzer is recorded. Then the TRHU structure is replaced by the VGA circuit. The output power ($P_{\text{VGA}}$) at varying gain control selection has been measured. The ratio between $P_{\text{VGA}}$ and $P_{\text{thru}}$ gives the voltage gain. The measured gain are shown in Figure 5-7. The VGA gain ranges from -10dB to 35dB over 8 control steps. However, the overall gain is 13dB lower than the design target.

The gain suddenly drops at step 4. This can be explained using Figure 5-8. When the step 4 is chosen, switch B3 is turned on and it bypasses all the following 4 gain stages and connects $C_{\text{couple}}$ and $C_{\text{load}}$ in series forming a capacitive voltage divider. $C_{\text{load}}$ is single ended input.
capacitance of AD8138 which is 2pF while $C_{\text{couple}}$ is 1.5pF, attenuation is 7.3dB. In normal operation, the VGA will not see such large capacitive load, and no such gain drop occurs.

![Gain Step vs Gain Control Step](image)

**Figure 5-7.** VGA gain vs. gain control step.

![Capacitive Voltage Divider](image)

**Figure 5-8.** Capacitive voltage divider in the configuration for gain step 4.

### 5.4 Baseband Low Pass Filter (LPF)

The LPF implements the functions of the chip matched filter (CMF) and anti-aliasing filter for the ADC. A second-order Butterworth filter provides a good approximation to the spectral
shape of the ideal half-sine chip pulse $\sin(\pi / T_c) P_f(t)$ and is a practical choice for the anti-alias filter. In particular, the Butterworth filter should be designed for a nominal bandwidth of $\sim 0.3R_c$, where $R_c$ is the chip rate of 51.2 MHz. This leads to a filter bandwidth of 15.36 MHz. Figure 5-9 compares the frequency response of the half-sine filter and 2nd-order Butterworth filter. The CMF’s equivalent noise bandwidth is the primary factor that affects the performance, while the output pulse shape has only weak influence. The equivalent two-sided noise bandwidth is $0.62R_c$ for the half-sine filter. For a 2nd-order Butterworth filter, the equivalent noise bandwidth is $1.11 \times BW_{3\text{dB}}$ [85]. Since its 3-dB bandwidth is chosen as $0.3R_c$, the equivalent noise bandwidth for this filter is $\sim 0.67R_c$. Two noise bandwidths would lead to a 0.3-dB difference in output noise power between two filters.

![Frequency response of half-sine and 2nd-order Butterworth filters](image)

**Figure 5-9.** Half-sine and 2nd-order Butterworth filter frequency response.

The LPF can be implemented differentially without employing a common mode feedback (CMFB) loop [86] as shown in Figure 5-10(A). The common-mode voltage is set by adding a diode-connected NMOS at the internal node of a conventional Gyrator.
Figure 5-10. A) A lossy biquad and B) its equivalent circuit.

Impedance looking into the Gyrator is

\[ Z = \frac{sC}{g_m^2} + \frac{1}{g_m}. \]  \hspace{1cm} (5-1)

Effectively, \( Z \) is the series connection of an inductor with value of \( \frac{C}{g_m^2} \) and a resistor with value of \( \frac{1}{g_m} \). The equivalent circuit is shown in Figure 5-10(B). It can be shown that

\[ \frac{V_{LP}}{V_{in}} = \frac{\frac{g_{m0}}{2g_m}}{\frac{s^2C^2}{2g_m^2} + \frac{sC}{g_m} + 1}. \]  \hspace{1cm} (5-2)

When \( g_{m0} \) is chosen to be \( 2g_m \), this expression becomes

\[ \frac{V_{out}}{V_{in}} = \frac{1}{\frac{s^2C^2}{2g_m^2} + \frac{sC}{g_m} + 1}. \]  \hspace{1cm} (5-3)

which can be rewritten as

\[ \frac{V_{out}}{V_{in}} = \frac{1}{\frac{s^2}{\omega_0^2} + \frac{1}{Q\omega_0} + 1}. \]  \hspace{1cm} (5-4)

where \( \omega_0 \) is \( \sqrt{2} \frac{g_m}{C} \) and \( Q \) is \( \frac{1}{\sqrt{2}} \). It is a 2\(^{nd}\) order Butterworth-type LPF.
The feature of this circuit is that every transconductor output voltage is determined by diode-connected circuit. This eliminates the requirement of common-mode feedback circuit. The positive transconductance in Figure 5-10(A) can be implemented using a negative transconductor and a gain stage with -180°-degree phase shift. It turns out that in a differential circuit, it is not necessary to implement such a gain stage. We can connect out-of-phase output signal to the negative transconductor.

![Bias circuitry and Core of the LPF](image)

**Figure 5-11.** Schematic of the LPF.

The pseudo-differential circuit implementation is shown in Figure 5-11. All the NMOS transconductors in the LPF have the same $g_m$. To implement positive $g_m$ in Figure 5-10(A), the negative output is connected to a negative $g_m$. When the value of $C$’s are fixed, the cutoff frequency of LPF is determined by $g_m$ which can be controlled by the bias voltage $V_{gmc}$. The current source in Figure 5-11 is implemented with a PMOS current mirror. The current in whole circuit is determined by $V_{gmc}$, so that the bias voltage for PMOS current mirror should be
controlled by $V_{gmc}$. The filter exploits the near-square-law behavior of long (2μm) NMOSFETs to partially cancel nonlinearity. Considering the long channel drain currents of two input NMOS transistors

$$I_{d}^+ = \frac{\beta}{2} (V_c + \frac{1}{2} V_{id} - V_m)^2$$

with $\beta = \frac{\mu_n C_{ox} W_n}{L_n}$

$$I_{d}^- = \frac{\beta}{2} (V_c - \frac{1}{2} V_{id} - V_m)^2$$

where $V_{id}$ is differential input. Subtraction of $I_{d}^+$ and $I_{d}^-$ results in the differential output current $I_{od}$:

$$I_{od} = I_{d}^+ - I_{d}^- = \beta (V_c - V_m) V_{id}$$

(5-6)

Hence, the differential output current is linear with the differential input voltage.

Figure 5-12. LPF $V_{out}$ and $I_{dd}$ vs. $V_{gmc}$.

A test circuit is fabricated in a 130-nm CMOS technology. The size of NMOS transistors is 1.2μm/2μm and that of PMOS transistors is 2.4μm/2μm. A Long-channel device suffers less channel-modulation effect and works closely in the square-law region. Measured DC
characteristics with a 1.2-V power supply are shown in Figure 5-12. A plot of measured $\sqrt{I_{dd}}$ vs. $V_{gmc}$ from 0.5V to 0.8V is shown in Figure 5-13. The plot clearly shows that the NMOS transistors are working in the square-law region.

![Figure 5-13. Near-square-law of I<sub>dd</sub> vs. V<sub>gmc</sub>.](image)

The AC response is tested with GSSG probes using an Agilent 5230A 4-port PNA. The network analyzer can cover a frequency range from 300 kHz to 20GHz. The calibration steps are to first use E-cal to calibrate four cables and then use port-extension function to calibrate out probe phase delay. Measured 4-port S-parameters are imported into Spectre using an N-port component in analogLib. An AC analysis results in the LPF frequency response in Figure 5-14. Since device $g_m$ is proportional to $\sqrt{I_{dd}}$, Equation 5-4 indicates that LPF corner frequency is proportional to $\sqrt{I_{dd}}$. The measured corner frequency vs. $\sqrt{I_{dd}}$ is shown in Figure 5-15. The corner frequency varies from 24.2 to 44.2MHz by 1.83 times (or ±29% tuning range) when $\sqrt{I_{dd}}$ is changed by 1.91 times. It indicates that the corner frequency is close to linear with $g_m$. 

Figure 5-14. Frequency response and tuning of LPF.

Figure 5-15. LPF cut-off frequency vs. $\text{Sqrt}(I_{dd})$. 

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Equation 5-4 indicates the ideal in-band gain of LPF should be 0dB while both simulation and measurement show in-band loss. The discrepancy can be explained by taking the device output resistance into account. The ideal LPF network in Figure 5-10(A) is redrawn using different diode-connected NMOS transconductance $g_m^a$ and $g_m^b$, as illustrated in Figure 5-16. $g_m^a$ and $g_m^b$ represent the equivalent transconductance combining $g_m$ and the device output resistance.

$$g_m^a = g_m + \frac{1}{r_{out}^a}$$

$$g_m^b = g_m + \frac{1}{r_{out}^b}$$  \hspace{1cm} (5-7)

As shown in Figure 5-16, $r_{out}^a$ is that of a parallel combination of four NMOS and PMOS output resistance, while $r_{out}^b$ is that of a parallel combination of two NMOS and PMOS output resistance.

![Figure 5-16. LPF including device output resistance.](image)

The transfer function in Figure 5-16 can be shown as

$$V_{LP} \left(V_{in}\right) = \frac{2 g_m^2/(g_m^a \cdot g_m^b + g_m^2)}{s^2 c^2 \left(g_m^a \cdot g_m^b + g_m^2\right) + \left(g_m^a + g_m^b\right) s c + 1}.$$  \hspace{1cm} (5-8)
where the in-band gain is

$$A = \frac{2g^2_m}{g^a_m \cdot g^b_m + g^2_m}$$  \hspace{1cm} (5-9)$$

Since $g^a_m$ and $g^b_m$ are both greater than $g_m$, the in-band gain is less than 1. Let’s examine how the in-band gain changes with bias current. To the 1st-order approximation, assuming

$$g_m = a \sqrt{I_{bias}}, \quad 1/r^a_{out} = mI_{bias} \quad \text{and} \quad 1/r^b_{out} = nI_{bias},$$

Equation 5-9 is rewritten as

$$A = \frac{2a^2}{2a^2 + a(m+n)\sqrt{I_{bias}} + mnI_{bias}}$$  \hspace{1cm} (5-10)$$

It shows that the LPF in-band loss increases with bias current. This trend has been verified by the simulation and measurement. Equation 5-8 also indicates that LPF corner frequency and network Q are affected by the device output resistance.

![Graph](image)

Figure 5-17. Simulated LPF IP$_3$.  

IP$_3$ of LPF is simulated by using two input tones at 7MHz and 8MHz with 0.6-V $V_{gmc}$. Output power of fundamental tone at 7MHz and 3rd-order intermodulation distortion tone at 6MHz are plotted in Figure 5-17. Simulated LPF IP$_3$ is 6.4dBm, or -6.6dBVrms and $P_{1dB}$
simulated at 7MHz is -6.8dBm, or -19.8dBVrms. Table 5-1 compares the measured and simulated results of in-band loss and corner frequency.

Table 5-1. Measured and simulated in-band loss and corner frequency of the LPF.

<table>
<thead>
<tr>
<th>$V_{gmc}$</th>
<th>Measured in-band loss (dB)</th>
<th>Measured cut-off frequency (MHz)</th>
<th>Simulated in-band loss (dB)</th>
<th>Simulated cut-off frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.50</td>
<td>0.59</td>
<td>24.2</td>
<td>0.73</td>
<td>24.2</td>
</tr>
<tr>
<td>0.55</td>
<td>1</td>
<td>28.2</td>
<td>0.78</td>
<td>28.2</td>
</tr>
<tr>
<td>0.6</td>
<td>1.34</td>
<td>31.2</td>
<td>0.84</td>
<td>30.2</td>
</tr>
<tr>
<td>0.65</td>
<td>1.76</td>
<td>35.2</td>
<td>0.9</td>
<td>34.2</td>
</tr>
<tr>
<td>0.7</td>
<td>1.95</td>
<td>38.2</td>
<td>0.99</td>
<td>37.2</td>
</tr>
<tr>
<td>0.75</td>
<td>2.3</td>
<td>42.2</td>
<td>1.13</td>
<td>39.2</td>
</tr>
<tr>
<td>0.8</td>
<td>2.8</td>
<td>44.2</td>
<td>1.49</td>
<td>41.2</td>
</tr>
</tbody>
</table>

5.5 Frequency Divider

As shown in Figure 2-3, the radio uses dual down-conversion architecture. The first LO signal is at 21.3GHz generated by a frequency synthesizer and the second LO signal of ~2.7GHz is generated by a frequency divide-by-8 circuit. This divider is implemented by cascading three 2:1 current mode static frequency dividers.

The divider shown in Figure 5-18 was designed by Changhua Cao [87]. For completeness, its function is briefly described. The divider is based on the master-slave D-type flip-flop in which the inverted slave outputs are connected to the master inputs. This type of divider can achieve a wide operating frequency range, consuming a smaller silicon area while generating
quadrature signals. As shown in Figure 5-19, each master-slave flip-flop is implemented using current mode logic (CML). The master and slave stages consist of an evaluate stage (M_{1,3,4}) and a latch stage (M_{2,5,6}). The current sources in conventional CML latches are omitted in Figure 5-19 for low voltage operation.

![Figure 5-19. Schematic of the 2:1 static frequency divider.](image)

5.6 Image Rejection Filter in LNA

The final receiver design includes an extra LNA stage and incorporates image rejection filter in the LNA. To improve the image rejection, two notch filters used in [88] are added in the LNA stage, as shown in Figure 5-20. The impedance looking into the notch filter is

\[
Z(s) = \frac{L(C_1 + C_2)s^2 + 1}{C_1C_2Ls^3 + C_1s} \tag{5-11}
\]

The image frequency is located at the zero of \(Z(s)\) and RF frequency is located at a pole of \(Z(s)\),

\[
\omega_{image} = \frac{1}{\sqrt{L(C_1 + C_2)}} \quad \text{and} \quad \omega_{RF} = \frac{1}{\sqrt{LC_1}}
\]
When the inductor and capacitors are ideal without any loss, at image frequency, the impedance of filter will be zero while at RF frequency the impedance of filter is open. This will provide infinite image rejection. However, in real circuit, passive components have finite Q. The filter impedance $|Z(s)|$ including the resistances of inductor and capacitors is plotted in Figure 5-21. The impedance is not zero at $f_{\text{image}}$ and infinite at $f_{\text{RF}}$. However, the magnitude of impedance
at $f_{image}$ is still much lower than that at $f_{RF}$, which makes the gain at the image much lower than that at RF. The 2-stage LNA combined with notch filters should have image rejection up to 40dB.

### 5.7 Integration of Transceiver

The μNode uses time division duplex (TDD) which means only either the transmitter or receiver is active at a time. This allows the use of one antenna instead of two. This reduces the chip area by ~3mm x 0.12mm.

![Figure 5-22. Distributed switching for the receiver and transmitter.](image)

Generally, a T/R switch is required to control the connection between the receiver and transmitter to the antenna. However, it is difficult to implement 24-GHz single-pole double-throw (SPDT) switches with low insertion loss in bulk CMOS processes. For example, switches implemented in a 130-nm CMOS process achieve 1.8-dB insertion loss at 15GHz [89]. For a
switch operating at 24GHz, the insertion loss can easily go above 2.5dB. The switch will degrade the input SNR and increase noise figure of the receiver chain. Because of this, instead of using a T/R switch, the switching function is merged into the PA and receiver [90], as shown in Figure 5-22. In the transmit mode, varactor $C_{\text{tune}}$ is adjusted to make PA output impedance close to 50Ω. At the same time, TxEn is set high to turn on transistor $M_{\text{tune}}$ to short the gate of M1 to ground. This also reduces voltage swing on the gate of M1. The impedance looking into the receiver will be $\omega Lg$ which is $\sim$150jΩ. This assures the impedance matching between the antenna and PA output to deliver maximum power while protecting the LNA. When the receiver is on, $C_{\text{tune}}$ is adjusted to make the PA output impedance inductive impedance of $\sim$100jΩ at 24GHz and TxEn is low to turn off $M_{\text{tune}}$. In simulations, these increase the noise figure by 1.3dB and decrease output power of PA by 0.8dB.

The synthesizer provides the 21.3-GHz LO signals to the receiver and transmitter. To assure sufficient LO drive, four separate buffers are inserted between the synthesizer and each mixer and divider in the receiver and transmitter. These buffers are implemented with tuned amplifiers. Figure 5-23(A) shows the frequency synthesizer output to these different buffers. Figure 5-23(B) shows the location of these buffers on the chip. Consuming 4-mA DC current from a 1.5-V supply, the frequency synthesizer output buffers provide $\sim$0.4V signal to the TX and RX buffer inputs.

The 8:1 divider of receiver needs to drive the gate of passive mixer at $\sim$2.7GHz. Instead of using a tuned amplifier which consumes too much area, an inverter chain is used as 2.7-GHz buffers, as shown in Figure 5-24. The interconnection between the divider output and passive mixer is longer than 1mm and is modeled as a transmission line. A 3-stage tapered buffer at the divider output drives a transmission line and a large buffer that directly drives the passive mixer.
Figure 5-23. A) Integration of the frequency synthesizer, transmitter and receiver. B) LO buffers between receiver, transmitter and frequency synthesizer.
In this chapter, the key building blocks in a RF receiver implemented in a 130-nm CMOS technology are presented. These blocks are VGA, LPF, frequency divider, passive mixer, LO buffers and image rejection filter in the LNA. Lastly, a distributed switch has been incorporated into the receiver and transmitter to lower switch loss.

5.8 Summary

In this chapter, the key building blocks in a RF receiver implemented in a 130-nm CMOS technology are presented. These blocks are VGA, LPF, frequency divider, passive mixer, LO buffers and image rejection filter in the LNA. Lastly, a distributed switch has been incorporated into the receiver and transmitter to lower switch loss.
CHAPTER 6
FULLY INTEGRATED RECEIVER AND WIRELESS LINK DEMONSTRATION OF μNODE TRANSCEIVER

6.1 Introduction

Following the successful implementation of individual building blocks, the blocks were integrated into a receiver chain. The receiver was also integrated with the transmitter [87] and frequency synthesizer [91]. The receiver has been characterized using an external LO source as well as LO provided by the frequency synthesizer. Using the transceiver [93], wireless communication up to 5m has been demonstrated. This completes the goal of demonstrating the feasibility of implementing a transceiver with on-chip antennas for general purpose communication. This chapter will first present the measurement results of receiver in section 6.2. The frequency synthesizer is briefly described and receiver measurement results with the frequency synthesizer are discussed in section 6.3. Finally, the wireless communication link between the receiver and transmitter that are 5m apart is demonstrated in section 6.4.

6.2 Receiver Measurement Using External LO Source

The receiver as well as the transmitter and frequency synthesizer is implemented in the UMC 130-nm logic CMOS. The die micrograph of μNode transceiver is shown in Figure 6-1. This 5mm × 5mm die also includes a 3mm × 3mm baseband processor developed by S. Hwang. The effective receiver area excluding the bonding pads is ~ 3mm². Similarly, the effective transmitter area is ~1.5mm × 0.8mm and the frequency synthesizer is ~0.8mm × 0.5mm. The on-chip antenna is 3.8mm long and built in metal layers 6-8. A large area of p-well block is placed underneath the on-chip antenna to reduce substrate loss [14].

Among 29 pads of the receiver for outputs and bias, 8 pads are bonded and the rest of the pads are connected using a 21-pin DC probe. Of the 8 wire bonded pads, 4 pads are baseband AC output pads. To drive the 50-Ω load of spectrum analyzer, 0-dB gain buffers using AD8138 on a
Figure 6-1. Die micrograph of the transceiver and baseband processor.

Figure 6-2. Receiver board and die wire bonding.
PCB board are added. The differential input capacitance of AD8138 is 1-pF. The board also facilitates wire bonding of the transmitter and frequency synthesizer. The receiver board and an enlarged photo illustrating receiver bonding are shown in Figure 6-2. The board is fabricated using FR-4 with dielectric constant of ~4.5. The board thickness is 60mil. The surface finish is soft bondable gold for the wire bonding. The outputs of baseband I/Q signal are connected to measurement equipment using standard SMA connectors attached to the board. The ground plane is cut out underneath the die to reduce the reflection problem that can degrade the dipole antenna performance.

The receiver is first characterized using an external LO signal. The single-ended signal output of a signal generator is converted to differential by an off-chip balun and then fed as inputs to the drivers for the RF active mixer and divider. This is done using a GSSG probe. Figure 6-3 shows the baseband output when RF input signal frequency, $f_{rf}$, is 21.605GHz with -90-dBm available power to the input of the receiver. The antenna is connected to the RF input pads of receiver during the measurements. This shifts down the turned frequency response. LO signal frequency, $f_{LO}$, is 19.2GHz. The baseband signal is supposed to be $f_{rf}-f_{LO}/8\times9$ which is 5MHz, as shown in Figure 6-4. This result shows that the receiver has successfully down-converted RF input to baseband using dual down-conversion. The baseband power is -22.2dBm. The corresponding receiver gain is 67.8dB. (This estimation is based on the assumption that the antenna impedance is well matched to 50Ω and the power delivered to the input GSSG pad is evenly divided between the on-chip antenna and the receiver.) When TxEn signal in Figure 5-22 is set to 1.2V, the LNA gate is shunted to ground and the baseband signal disappears. The frequency response is shown in Figure 6-4. RF and LO frequencies are varied to keep the baseband output frequency at 5MHz. The receiver gain peaks between 21.5GHz and 22.5GHz.
Figure 6-3. Receiver baseband signal output spectrum.

Figure 6-4. Gain vs. frequency of the receiver with an on-chip antenna connected to the RF input pads.
The baseband LPF frequency response is characterized by looking at the frequency response of noise floor, as shown in Figure 6-5. This figure spans from DC to 50MHz. There is a dip at DC which shows the high pass filtering of DC offset cancellation. A 5-MHz baseband signal down-converted from RF is also shown. The 3-dB cutoff frequency is ~23MHz. Using an HP8508A vector voltmeter, baseband I/Q signal mismatch is measured. It is found gain mismatch is 1.4dB and phase mismatch is 8.5°. The main cause could be mismatch between LO lines driving I/Q passive mixers, as shown in Figure 6-1. These lines have quite different shapes even though they have the same length. The better way is to route LO lines closely and then split I/Q lines at a symmetric point which has same distance to I/Q mixers. The power consumption of receiver is summarized in Table 6-1. Total receiver power consumption is 58.9mW. The signal path including LNA, mixer, IF amplifier, baseband amplifier, LPF and output buffer consumes 34.9-mW power, while the LO buffers and divider consume 24-mW.
Table 6-1. Power table of the receiver.

<table>
<thead>
<tr>
<th>Receiver blocks</th>
<th>$V_{dd}$ (V)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>1.5</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>Mixer</td>
<td>1.5</td>
<td>3</td>
<td>4.5</td>
</tr>
<tr>
<td>LO1 Driver (for mixer and divider)</td>
<td>1.5</td>
<td>6</td>
<td>9</td>
</tr>
<tr>
<td>IF Amp</td>
<td>1.4</td>
<td>11</td>
<td>15.4</td>
</tr>
<tr>
<td>LO2 Driver (for passive mixer)</td>
<td>1.5</td>
<td>7</td>
<td>10.5</td>
</tr>
<tr>
<td>Divider</td>
<td>1.5</td>
<td>3</td>
<td>4.5</td>
</tr>
<tr>
<td>Baseband</td>
<td>1.5</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Output Buffer</td>
<td>3</td>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
<td>58.9</td>
</tr>
</tbody>
</table>

All the measurements discussed so far are made using receivers with an on-chip antenna. To make accurate gain and NF measurements, on-chip antennas on two boards are cut from the receiver. One board shows that when input RF signal is at 21.605GHz with -83.6-dBm power and LO signal is at 19.2GHz, 5-MHz baseband signal power is -11.3dBm which translates to 72.3-dB Rx gain. Then noise performance s characterized by terminating the external balun at RX input with a 50-Ω resistor. The noise floor at 5-MHz baseband output is -38.2dBm with a 100-kHz spectrum analyzer resolution bandwidth. From these, NF is

$$\text{NF} = -38.2 - (-174 + 72.3 + 50) = 13.5\text{dB}$$

Note this NF number is single side band (SSB) NF. The noise at 5-MHz is contributed by two RF side bands at 21.605GHz and 21.595GHz, respectively. Since signals will also be present at these two side bands, double side band (DSB) NF which is relevant for the system is 10.5dB, or 3dB lower than SSB NF. Figure 6-6 depicts the gain and DSB NF of the receiver on another board as a function of the input frequency, showing a 66.5-dB peak gain and 12.5-dB NF at 21.6GHz. IP$_3$ is tested using a 19.2-GHz LO signal and two RF input signals at 21.605GHz and 21.60502GHz. Figure 6-7 shows the measured IIP$_3$ is -60dBm. These two “blockers” are in band
and no filtering on down-converted baseband “blockers” causes IP₃ limited by last stage. The measured performance is summarized in Table 6-2.

Figure 6-6. Frequency response of RX gain and NF.

Figure 6-7. IP3 measurement of whole RX chain.
Table 6-2. RX performance summary.

<table>
<thead>
<tr>
<th>Circuit metrics</th>
<th>Measured results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak gain</td>
<td>72.3dB</td>
</tr>
<tr>
<td>Noise Figure (DSB)</td>
<td>10.5dB</td>
</tr>
<tr>
<td>IIP3 (two in-band tones)</td>
<td>-60dBm</td>
</tr>
<tr>
<td>Power consumption</td>
<td>58.9mW</td>
</tr>
<tr>
<td>Technology</td>
<td>130-nm logic CMOS</td>
</tr>
<tr>
<td>Area</td>
<td>3mm^2</td>
</tr>
</tbody>
</table>

6.3 Receiver Measurement Using On-chip Frequency Synthesizer

A fully integrated receiver has also been characterized with an on-chip frequency synthesizer. The frequency synthesizer is designed by Y. P. Ding and the synthesizer integration was accomplished with her help. Its design has been discussed in [91]. A simple functional description of frequency synthesizer is given here for completeness.

![PLL-based frequency synthesizer](image)

**Figure 6-8.** PLL-based frequency synthesizer.

Figure 6-8 depicts a block diagram of integer-N PLL-based frequency synthesizer. A phase and frequency detector (PFD) compares the phase and frequency difference between the reference signal and frequency divided VCO output. The PFD generates pulses with width proportional to phase difference. The charge pump (CP) senses the pulse width and injects the corresponding amount of current into the loop filter. The loop filter voltage is used to control the
VCO and the filter also attenuates the unwanted spurious tones produced by the charge pump.

With the PLL locked, VCO output frequency tracks the input reference frequency with a ratio of N:1. N is the divider ratio. For the measurements, N is set to 256. The performance of the frequency synthesizer is summarized in Table 6-3.

<table>
<thead>
<tr>
<th>Circuit metrics</th>
<th>Measured results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prescaler power</td>
<td>6mA @ 1.5V (9mW)</td>
</tr>
<tr>
<td>VCO power</td>
<td>5mA @ 1.2V (6mW)</td>
</tr>
<tr>
<td>VCO buffer power</td>
<td>3mA @ 1.2V (3.6mW)</td>
</tr>
<tr>
<td>PLL output buffer power</td>
<td>10mA @ 1.2V (12mW)</td>
</tr>
<tr>
<td>PLL total power</td>
<td>31.8mW</td>
</tr>
<tr>
<td>VCO tuning range</td>
<td>2.5GHz (13.4%)</td>
</tr>
<tr>
<td>In band phase noise</td>
<td>-65dBc/Hz @ 50kHz</td>
</tr>
<tr>
<td>Out of band phase noise</td>
<td>-121dBc/Hz @ 20MHz</td>
</tr>
<tr>
<td>PLL locking range</td>
<td>17.5GHz-19.7GHz</td>
</tr>
<tr>
<td>Reference spurs</td>
<td>33-37dB below carrier</td>
</tr>
</tbody>
</table>

A 16-pin probe is used to provide bias and reference signal to the PLL. The divide ratio of the PLL is 256. With RF input signal at 21.7GHz and PLL reference signal at 75.33MHz, the baseband output signal is at 21.7GHz - 75.33MHz × 256/8 × 9 = 4.96MHz. The baseband spectrum is shown in Figure 6-9. RF input power is -70dBm. Figure 6-10 shows the output spectrum of the baseband signal with a reduced span. Because the LO is generated by a synthesizer, the baseband signal shows a similar skirt shape spectrum as the synthesizer output.

The measured phase noise of baseband signal is shown in Figure 6-11. This shows that the frequency synthesizer is working properly with the receiver. Measuring the phase noise from baseband signal could be an effective way to evaluate the phase noise performance of an integrated frequency synthesizer if there is no other way to access the PLL output. Outside the
Figure 6-9. The output spectrum the RX when the LO is driving from synthesizer.

Figure 6-10. The output spectrum of RX when the LO is generated using an on-chip synthesizer. The span is reduced to 2MHz to show the skirt.
Figure 6-11. Phase noise of the baseband signal.

Figure 6-12. Baseband power versus different VGA gain setting.
loop bandwidth of the PLL, the noise floor is determined by input and receiver noise shaped by the low pass filter. Integrating phase noise -64dBC/Hz at 50-kHz offset across two 10MHz bandwidth shows a -9-dB RX SNR. Since system $E_b/N_0$ requirement is 18dB and data rate and noise bandwidth are 100kHz and 51.2MHz, respectively, system SNR requirement is -9dB. This means that measured RX SNR meets system requirement. Figure 6-12 shows the output power of bandband signal versus the VGA gain setting. The input RF signal is at 21.7GHz with -70dBm available power while the reference for the frequency synthesizer is at 75.33MHz. When the control bits $B_0B_1B_2$ of VGA change from “110” to “000”, the baseband power changes from -48.7dbm to -16.4dBm. The average gain step is 6.4dB which is close to simulated 6-dB per gain step.

6.4 Wireless Communication Link Demonstration

With the receiver and frequency synthesizer working together, it is feasible to demonstrate a wireless communication link between the transmitter and receiver using on-chip antennas. The transmitter has been designed and characterized by Changhua Cao [87]. Figure 6-13 shows the building blocks in the transceiver. A single-tone signal is generated from TX and delivered to an on-chip antenna by a PA. At 5m away, the receiver picks up the signal and down-converts it to baseband.

Figure 6-15 shows the setup and environment for wireless link demonstration. The receiver is placed on the probe station in a metal cage. A 5-mm thick glass substrate is attached to the bottom of the receiver board to reduce the effect of metal chuck on the on-chip antenna. A 21-pin probe and a 16-pin probe are landed on pads for biasing the receiver and PLL. However, these DC pins could affect receiver antenna by disturbing EM field near the antenna. This effect needs to be further investigated. Out side the cage, the transmitter is placed on a cart 5m away. All the
Figure 6-13. Wireless communication link between the transmitter and receiver.

Figure 6-14. Transmitter on board and die wirebonding.
Figure 6-15. Wireless link measurement setup and environment.

Figure 6-16. Receiver output spectrum.
bias lines are connected by patch cords to dc sources. The transmitter total power consumption is 128mW.

Both TX and RX synthesizers work in integer-N mode with a divide ratio of 256. With a 75.35-MHz TX reference frequency, transmitter board transmits single tone signal at ~21.7GHz. The frequency was limited by the maximum frequency of synthesizer integrated with the transmitter. A horn antenna with 20-dBi gain located at 3m away from the transmitter picks up ~73dBm power. The PLL reference frequency on the receiver side is 75.33MHz. The receiver baseband output is at 4.825MHz with power of -38.30dBm as shown in Figure 6-16. This is the first time a fully integrated CMOS transceiver pair has established a wireless communication link using on-chip antennas.

### 6.5 Summary

A fully integrated 24-GHz CMOS receiver is demonstrated for the first time. One receiver achieves a 72.5-dB peak gain and 10.5-dB NF at 21.6GHz. The whole receiver consumes 58.9-mW power. Working with an on-chip frequency synthesizer, for the first time a wireless communication link has been successfully established between a fully integrated transmitter and a receiver with on-chip antennas that are separated by 5m. The RF portion of μNode has been successfully implemented. This is a major step toward the realization of a true single chip radio.
CHAPTER 7
SUMMARY AND FUTURE WORK

7.1 Summary

Imagine a tiny radio only packaged with a battery! The possibility of a single chip radio has become more realistic than ever with the demonstration of a fully integrated 24-GHz CMOS transceiver communicating using on-chip antennas. This Ph.D work demonstrated a fully integrated transceiver [93] including a receiver, a transmitter [87] and a synthesizer [91].

The receiver chain consists of an LNA, an active mixer, an IF amplifier, a passive mixer, variable gain amplifiers and low pass filters for baseband I/Q signals. All the circuits are differential to reduce the impact of switching noise of digital circuits which will eventually be integrated with the transceiver. High frequency LNA design is analyzed in terms of gain and noise figure. Substrate resistance has been found to be a critical factor which degrades LNA performance. To reduce this effect, a unique topology using an inductor at the gate of common gate stage in a cascode LNA has been demonstrated to boost the gain while greatly reducing the power consumption. The 26-GHz LNA only consumes 0.8-mW power while achieving 8-dB gain. A 20-GHz RF front-end including an LNA and mixer achieves 9-dB gain and 6.6-dB NF while consuming 12.8-mW power from a 1.5-V supply. Using this front-end and an on-chip antenna, AM signal transmitted from 5-m away was successfully picked up and down-converted to IF frequency. Finally, an entire receiver chain is integrated in the UMC 130-nm logic CMOS technology. The receiver achieves 72.5-dB gain and 10.5-dB DSB NF with 58.9-mW power consumption. A 5-m wireless communication link is established using a receiver and a transmitter both working with an on-chip frequency synthesizer and an antenna. ~21.7-GHz single tone signal generated by the transmitter is down-converted to ~5-MHz using the receiver. This is the first time a wireless link is demonstrated between a pair of fully integrated CMOS
transceivers with on-chip antennas. This is a major milestone toward the realization of a single-chip radio. Lastly, this work has shown that 24-GHz RF circuits with acceptable performance and power efficiency can be implemented using the 130-nm CMOS.

7.2 Suggested Future Work

The work presented in this thesis has shown the feasibility of implementing a single chip radio. To incorporate these circuits into real applications and products, there are still much to do. The list of suggested future works includes:

Co-design of an on-chip antenna and circuits: One unique feature of μNode is to integrate an on-chip antenna. However, its advantage has not been fully exploited. The antenna, LNA and PA were treated as separate blocks and make each of them matched to 50Ω. Logic questions are: since now we have the feasibility to control on-chip antenna impedance, is 50-Ω matching an optimum option? Even if the impedance change may have deleterious effect on PA output power and LNA NF, is there an optimum matching impedance for the whole wireless link between a transmitter and a receiver? The answers to these questions will be fundamental contributions from this work.

On-chip bias reference generation: As shown in Figure 6-2, to make the receiver, transmitter and frequency synthesizer work simultaneously, more than 60 DC lines have to be connected from the chips to external DC sources. It takes great efforts to properly connect these wires and it is time consuming. Bias circuits should be incorporated into the chip.

Automatic Gain Control (AGC): The gain control in the current version is implemented using a manually controlled variable gain amplifier. To automatically control the gain, two options can be considered. One is to use commonly used AGC which has a power detector to sense the signal amplitude and adjust the gain settings. Another is to use the baseband processor to sense the BER to adjust the gain settings.
Integration with ADC and baseband processor: This is the last major step toward a fully integrated radio. Since the baseband processor designed by Seon-Ho Hwang is fully functional, integration of the RF transceiver with the baseband processor and ADC should be possible in near future. This will indeed be exciting!
APPENDIX
DERIVATION OF NOISE FACTOR OF CS-LNA

Figure A-1 shows 3 noise sources in CS-LNA: channel thermal noise \( i_d \), induced gate noise \( i_g \) and source voltage noise \( v_n \). To calculate noise factor of CS-LNA, one important step is to calculate correlation between channel thermal noise and gate induced noise. The detailed derivation is given here.

![Figure A-1. Noise sources in CS-LNA.](image)

Noise factor of CS-LNA is

\[
F = \frac{i_d^2}{i_{n2}^2(v_n)} = 1 + \frac{i_{n2}(i_d, i_d)}{i_{n2}^2(v_n)}
\]  

(A-1)

From Equation 3-28 and 3-31, we know that

\[
i_{n2}^2(v_n) = \frac{g_mQ_{gs}^2}{4} \cdot 4kTR_s
\]  

(A-2)

\[
i_{n1}(i_g, i_n) = i_{n1}i_{n1}^* = \left[ i_g \frac{\omega_f}{j\omega_0}((1 + jQ_{gs}) + i_d) \right] \left[ i_g^* \frac{-\omega_f}{j\omega_0}((1 - jQ_{gs}) + i_d) \right] \frac{1}{(1 + \frac{\omega_f}{R_s})^2}
\]

(A-3)

Where

\[
\left[ i_g \frac{\omega_f}{j\omega_0}((1 + jQ_{gs}) + i_d) \right] \left[ i_g^* \frac{-\omega_f}{j\omega_0}((1 - jQ_{gs}) + i_d) \right]
\]
\[
\begin{align*}
&= \overline{i_s^2} \left( \frac{\omega_r}{\omega_0} \right)^2 (1 + Q_{gs}^2) + \overline{i_d^2} + 2 \Re(\overline{i_s^*} \frac{\omega_r}{j\omega_0} (1 + jQ_{gs})) \\
&= \overline{i_s^2} \left( \frac{\omega_r}{\omega_0} \right)^2 (1 + Q_{gs}^2) + \overline{i_d^2} - 2 |c| \sqrt{\overline{i_s^2} \overline{i_d^2}} \frac{\omega_r}{\omega_0} \\
&= 4kT \delta g_m (1 + Q_{gs}^2) / 5 + 4kT \gamma g_m - 4kT \cdot 2 |c| g_m \sqrt{\delta \gamma} \cdot \frac{1}{5}.
\end{align*}
\]

Substituting Equation A-2 and A-3 into Equation A-1, the result is

\[
F = 1 + \frac{4kT \delta g_m (1 + Q_{gs}^2) / 5 + 4kT \gamma g_m - 4kT \cdot 2 |c| g_m \sqrt{\delta \gamma} \cdot \frac{1}{5}}{(1 + \frac{\omega_r L_x}{R_s})^2}
\] (A-4)

When LNA input is matched to source impedance where \(\omega_r L_x = R_s\), the above equation can be rewritten as

\[
F = 1 + \frac{\delta (1 + Q_{gs}^2) / 5 + \gamma - 2 |c| \sqrt{\delta \gamma} \cdot \frac{1}{5}}{g_m Q_{gs}^2 R_s}
\] (A-5)
REFERENCES


BIOGRAPHICAL SKETCH

Yu Su was born in 1974. He received his B.S. degree in 1996 from the Dept. of Electrical Engineering of Xi’an Jiaotong University in Xi’an, China. His specialty was semiconductor device. In 1999, he received his M.S. degree from Tsinghua University. From August 2000 to December 2002, he was with the University of South Florida as a research assistant. Since 2003, he was a Ph.D student in Silicon Microwave Integrated Circuits and Systems (SIMICS) research group of University of Florida. He has been working on radio frequency CMOS circuit design. He received the Analog Device outstanding student designer award in 2003. From March 2007 to March 2009, he has been working as a RFIC designer in Texas Instruments, Inc. He received his Ph.D from the University of Florida in May 2009.