# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIST OF TABLES</td>
<td>v</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>vi</td>
</tr>
<tr>
<td>ABSTRACT</td>
<td>viii</td>
</tr>
<tr>
<td>CHAPTER</td>
<td></td>
</tr>
<tr>
<td>1 INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>2 CONTROL METHODS</td>
<td>4</td>
</tr>
<tr>
<td>Standard Modulation</td>
<td>4</td>
</tr>
<tr>
<td>Non-Standard Modulation Control Methods</td>
<td>5</td>
</tr>
<tr>
<td>One-Cycle Control</td>
<td>5</td>
</tr>
<tr>
<td>Feed Forward Control</td>
<td>7</td>
</tr>
<tr>
<td>LCAM Control</td>
<td>8</td>
</tr>
<tr>
<td>3 HYSTERETIC MODULATOR</td>
<td>12</td>
</tr>
<tr>
<td>Ideal Hysteretic Modulator</td>
<td>12</td>
</tr>
<tr>
<td>Basic Operation</td>
<td>12</td>
</tr>
<tr>
<td>Operating Frequency</td>
<td>14</td>
</tr>
<tr>
<td>Current Sources</td>
<td>14</td>
</tr>
<tr>
<td>Modulation Capacitor</td>
<td>16</td>
</tr>
<tr>
<td>Physical Realization of the Hysteretic Modulator</td>
<td>17</td>
</tr>
<tr>
<td>4 DESIGN ORIENTED MODELING</td>
<td>19</td>
</tr>
<tr>
<td>Realizing the Modulation Frequency</td>
<td>19</td>
</tr>
<tr>
<td>Selection of $C_{MOD}$</td>
<td>20</td>
</tr>
<tr>
<td>Design of I$_{down}$</td>
<td>21</td>
</tr>
<tr>
<td>Design of I$_{up}$</td>
<td>21</td>
</tr>
<tr>
<td>Switching Logic and Level Shifting</td>
<td>22</td>
</tr>
<tr>
<td>Design of the Level Shifter</td>
<td>24</td>
</tr>
<tr>
<td>Selection of the Inverter</td>
<td>25</td>
</tr>
<tr>
<td>Comparators and SR Latch</td>
<td>25</td>
</tr>
<tr>
<td>Comparator and Latch Speed</td>
<td>25</td>
</tr>
</tbody>
</table>
Selection of the Offset Voltage .................................................................27
Design Summary ..............................................................................................28

5 SIMULATION AND VERIFICATION ..............................................................30

Verification Techniques .................................................................................30
  Boost Transfer Function with LCAM ..........................................................30
Simulation Model ...........................................................................................32
Experimental Verification .............................................................................32
Results .............................................................................................................34

LIST OF REFERENCES .....................................................................................39

BIOGRAPHICAL SKETCH ..............................................................................40
### LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-1</td>
<td>Design summary for the hysteretic modulator needed to implement LCAM control on the boost converter</td>
<td>29</td>
</tr>
<tr>
<td>5-1</td>
<td>Boost converter loss term values</td>
<td>31</td>
</tr>
<tr>
<td>5-2</td>
<td>Hysteretic modulator simulation parameters and components</td>
<td>32</td>
</tr>
<tr>
<td>5-3</td>
<td>Boost converter values used in simulation</td>
<td>32</td>
</tr>
<tr>
<td>5-4</td>
<td>Bias and offset voltages</td>
<td>33</td>
</tr>
<tr>
<td>5-5</td>
<td>Bill of materials</td>
<td>38</td>
</tr>
</tbody>
</table>
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Standard PWM boost converter topology.</td>
<td>1</td>
</tr>
<tr>
<td>1-2</td>
<td>Boost transfer function $V_{out}/V_{in}$ vs. $D$ and $D'$.</td>
<td>2</td>
</tr>
<tr>
<td>2-1</td>
<td>Waveforms used to generate the PWM signal for the standard modulation</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>configuration.</td>
<td></td>
</tr>
<tr>
<td>2-2</td>
<td>One-Cycle controlled, constant-frequency switch.</td>
<td>6</td>
</tr>
<tr>
<td>2-3</td>
<td>Waveforms for one-cycle controlled, constant-frequency switch.</td>
<td>7</td>
</tr>
<tr>
<td>2-4</td>
<td>Feed-Forward PWM controller for boost converter.</td>
<td>7</td>
</tr>
<tr>
<td>2-5</td>
<td>Operational waveforms for Feed-Forward PWM controller.</td>
<td>8</td>
</tr>
<tr>
<td>2-6</td>
<td>PWM waveforms with LCAM system.</td>
<td>10</td>
</tr>
<tr>
<td>2-7</td>
<td>Block diagram of the complete system used to realize LCAM control for the</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>boost converter.</td>
<td></td>
</tr>
<tr>
<td>3-1</td>
<td>Ideal hysteretic modulator.</td>
<td>12</td>
</tr>
<tr>
<td>3-2</td>
<td>The voltage across $C_{MOD}$.</td>
<td>13</td>
</tr>
<tr>
<td>3-3</td>
<td>Triangle shapes that can be achieved with a hysteretic modulator.</td>
<td>14</td>
</tr>
<tr>
<td>3-4</td>
<td>Physical realization of the hysteretic modulator using non-ideal components.</td>
<td>18</td>
</tr>
<tr>
<td>4-1</td>
<td>Schematic of the non-ideal hysteretic modulator.</td>
<td>19</td>
</tr>
<tr>
<td>4-2</td>
<td>Current source topology.</td>
<td>22</td>
</tr>
<tr>
<td>4-3</td>
<td>Level shifting implementation.</td>
<td>23</td>
</tr>
<tr>
<td>4-4</td>
<td>$V_{CMOD}$ for the ideal case without delays modulates between the two</td>
<td>26</td>
</tr>
<tr>
<td></td>
<td>hysteretic thresholds.</td>
<td></td>
</tr>
<tr>
<td>4-5</td>
<td>Overshoot of the lower hysteretic limit requires the use of $V_{offset}$.</td>
<td>27</td>
</tr>
</tbody>
</table>
5-1  Boost converter with losses.................................................................30
5-2  Saber schematic used for circuit simulations.................................33
5-3  Boost converter and LCAM system used to measured data........34
5-4  Measured waveforms........................................................................35
5-5  $V_{out}$ vs. $V_{cmd}$ curve with calculated, simulated and measured data........................................36
5-6  A family of $V_{out}$ vs. $V_{cmd}$ curves for several values of $I_{out}$ ......36
5-7  A family of $V_{out}$ vs. $V_{cmd}$ curves for several values of $V_{in}$ ....37
In order to design a robust DC-DC converter, it is essential that the system be controllable. The pulse width modulated (PWM) DC-DC boost converter presents a non-linear system with respect to the PWM duty cycle, and standard linear control techniques cannot be applied.

Typical control methods generate the PWM waveform by comparing a fixed amplitude carrier to a variable magnitude DC reference. This thesis proposes a control method of Linearization through Carrier Amplitude Modulation (LCAM). In LCAM control, the PWM signal is generated by comparing a variable amplitude carrier signal to a fixed DC reference. When this PWM signal is applied to the boost converter, it is shown that the output voltage of the converter is directly proportional to the amplitude of the carrier. The carrier signal is generated by a hysteretic modulator. The amplitude of the carrier from the hysteretic modulator is equal to a reference input signal, and the
output voltage of the boost converter is therefore directly proportional to the reference. Using the hysteretic modulator, the output will linearly track the reference signal.

Operation and design of the hysteretic modulator are examined for LCAM control of the boost converter, and a design metric for the hysteretic modulator is included for constant frequency operation. Sources of delays and hysteretic limit overshoot are examined and their effects on operating frequency are included.

Models of the boost converter with LCAM control are given which predict the linear behavior. For an ideal boost converter, the output voltage is independent of the output current and input voltage. In a second order system with converter parasitics included, these other signals can superimpose small operating-point dependant loss terms. If losses can be minimized, however, the linear terms will dominate. Simulations and measured data are compared with the models in order to verify linear operation of the system. Input voltage and output current are varied to verify the second order effects.
CHAPTER 1
INTRODUCTION

For switching DC-DC converters, controllability is essential for robust circuit design. In a Pulse Width Modulated (PWM) converter topology, the width of a constant-frequency pulse is modulated in order to control one or more of the converter’s variables. For a boost converter, the transfer function, $V_{out}/V_{in}$, as a function of the PWM duty ratio, $D$, is nonlinear. Standard linear control processes, including voltage feedback and current-mode control are more effective on linear systems.

The standard Pulse Width Modulated (PWM) DC-DC boost converter can be seen in Figure 1-1.

![Figure 1-1: Standard PWM boost converter topology.](image)

A switching network comprising $M_1$ and $D_1$ is used to boost the input voltage, $V_{in}$, up to the desired output voltage, $V_{out}$. The output voltage that the converter delivers to the load, $R_L$, is controlled by a pulse-train signal sent to the gate of $M_1$. Control of the output voltage is achieved by modulating the duty cycle, $D$, of the pulse-train. Using volt-second-balance and amp-second-balance [1], it can be shown that the transfer function for steady state operation of the boost converter is
\[ \frac{V_{out}}{V_{in}} = \frac{1}{1-D} = \frac{1}{D'} \]  

(1.1)

where the compliment duty cycle \( D' = 1 - D \)

If the duty cycle is the control variable, the transfer function of (1.1) is non-linear with respect to both \( D \) and \( D' \). This non-linearity can be further seen in Figure 1-2, which plots the relationships established in (1.1).

![Boost Transfer Function (Vout/Vin) vs. D and D'](image)

Figure 1-2: Boost transfer function \( \frac{V_{out}}{V_{in}} \) vs. \( D \) and \( D' \). These functions are highly nonlinear.

Classical linear control techniques cannot be applied to non-linear systems, and stability of such systems is difficult to achieve. The goal of this work is to present a method to linearize the dc relationship between the transfer function of the boost and its control variable. Chapter 2 examines the standard control method used to generate the PWM signal for linear switching converters and shows why it will not work for the boost topology. Other complex methods used to control non-linear converters are also examined. Finally, a new control method, Linearization through Carrier Amplitude Modulation (LCAM) is presented for the boost converter. Chapter 3 explores the
operation of a hysteretic modulator, which is the fundamental building block for the LCAM control system. Chapter 4 presents a detailed design methodology for implementation of the hysteretic modulator. Chapter 5 verifies LCAM control by comparing theory, simulations and measured data.
CHAPTER 2
CONTROL METHODS

Standard Modulation

A standard modulation scheme is often used to generate the PWM signal for switching converters. This method involves comparing a fixed amplitude carrier with a slowly varying, or dc, modulating signal. Making adjustments to the modulating signal controls the duty cycle of the PWM signal. An example of standard modulation with a triangular carrier signal can be seen in Figure 2-1.

Using the similar triangles formed in Figure 2-1 it can be seen that

$$\frac{V_{cmd}}{V_{peak}} = \frac{D \cdot T_s}{T_s} = D$$

Figure 2-1: Waveforms used to generate the PWM signal for the standard modulation configuration.
Since $V_{\text{peak}}$ is fixed, the duty cycle, $D$, is a linear function of the command voltage, $V_{\text{cmd}}$. However, from (1.1), the transfer function of the boost is non-linear with respect to the duty cycle. Therefore, the boost transfer function is non-linear with respect to $V_{\text{cmd}}$, and linear feedback schemes cannot be applied control the output.

**Non-Standard Modulation Control Methods**

For any PWM converter topology, the goal of making a circuit linear is to force it to behave with the following characteristic:

$$V_{\text{out}} = k \cdot V_{\text{cmd}}$$

(2.2)

Here $k$ is a constant and $V_{\text{cmd}}$ is a controllable command signal. The command signal varies slowly compared to the converter switching frequency and can be considered to be quasi-DC in the steady-state. There are two major benefits to achieving the behavior in (2.2). First, the output of the converter can be linearly controlled using only the command voltage. Second, in the ideal case, the output signal is independent of all other input parameters, including $V_{\text{in}}$. This means that changes to the input of the converter will not greatly impact steady-state performance.

Two common methods to achieve the linear behavior of (2.2) are One-Cycle Control [2], and Feed-Forward PWM Control [3]. These are non-linear methods used to achieve large-signal modulation control of switching converters. For each of these methods, however, certain drawbacks can arise due to complexity of the circuits.

**One-Cycle Control**

The schematic for a One-Cycle controlled, constant-frequency switch can be seen in Figure 2-2. In the One-Cycle scheme, operation of the circuit is initiated by the clock
signal which closes the switch. With the switch closed, $y(t) = x(t)$, and $V_{\text{in}}$ ramps up until it reaches $V_{\text{cmd}}$ in the following manner:

$$\int_{0}^{\tau_{x}} x(t)\,dt = V_{\text{cmd}}(t) \quad (2.3)$$

Waveforms from this circuit can be seen in Figure 2-3. The average value of the switch output, $y(t)$ is found to be

$$y(t) = \int_{0}^{\tau_{x}} x(t)\,dt \quad (2.4)$$

and therefore,

$$y(t) = V_{\text{cmd}}(t) \quad (2.5)$$

For the boost converter $y(t) = V_{\text{out}}(t)$. Substituting this into (2.5) yields the desired linear relationship between the command voltage and the output.

$$V_{\text{out}} = V_{\text{cmd}} \quad (2.6)$$

Figure 2-2: One-Cycle controlled, constant-frequency switch.
Figure 2-3: Waveforms for one-cycle controlled, constant-frequency switch.

The integrators needed for this circuit must have a reset, and the integration function can lead to cumbersome control equations. Complicated circuits may also be required to minimize errors due to delays in the reset process.

**Feed Forward Control**

The Feed-Forward PWM (FF-PWM) controller used for a boost converter with leading-edge modulation can be seen in Figure 2-4. As in One-Cycle, the circuit is initiated by the clock, which resets the integrator. The command voltage, $V_{cmd}$, is integrated to create a ramp, which is compared to the converter input voltage. The PWM output created by this system can be seen in Figure 2-5.

Figure 2-4: Feed-Forward PWM controller for boost converter with leading-edge modulation.
Figure 2-5: Operational waveforms for Feed-Forward PWM controller.

It can be shown that for boost converters with PWM signals generated in this manner, the output voltage is proportional to the command voltage

$$V_{out} = kV_{cmd}$$ (2.7)

Like One-Cycle control, integrators with reset are central to FF-PWM control schemes [3]. The integrators are used to realize complex equations necessary to achieve linear behavior. Several other elements are needed to achieve FF-PWM including, a comparator, a mono-stable pulse circuit and a clock signal. Time constants of the integrators and the clock must be closely matched, or a dependence on the input voltage may arise.

**LCAM Control**

The general linearization concept given in (2.2) can be specifically applied to the boost converter using the boost transfer function given in (1.1). Substituting the value of $V_{out}$ from (2.2) into (1.1), it can be shown that

$$\frac{k \cdot V_{cmd}}{V_{in}} = \frac{1}{D'}$$ (2.8)

Solving for $D'$,

$$D' = \frac{V_{in}}{k \cdot V_{cmd}}$$ (2.9)
This means that if the output voltage of the boost is to behave linearly as in (2.2), the switching MOSFET, M1, in Figure 1-1 must be driven with a PWM signal having a compliment duty cycle that obeys the relationship in (2.9).

To achieve a PWM signal where $D'$ satisfies (2.9), the Linearization through Carrier Amplitude Modulation (LCAM) control system is used. The LCAM system is similar to the conventional PWM generator used for standard linear control. Again, a triangular carrier is compared to the modulating signal in order to generate the PWM signal. In this new scheme, however, the amplitude of the carrier is modulated also. The modulating signal, which must not be confused with the amplitude modulated carrier, should not change much within one carrier period. In order to realize (2.9), the LCAM system uses configuration in Figure 2-6(a). The peak of the carrier signal is equal to $k \cdot V_{cmd}$, and $V_{in}$ acts as the modulating signal. Using the similar triangles seen in Figure 2-6(b), it can be seen that

$$\frac{V_{in}}{k \cdot V_{ref}} = \frac{D' T_s}{T_s} = D'$$

(2.10)

Therefore, the PWM signal generated by the LCAM system is that of (2.10). This signal satisfies the requirements of (2.9) and will therefore force the desired linear behavior for the boost converter specified in (2.2).

It is important to realize that the goals and results of One-Cycle, FF-PWM and LCAM are the same. Namely, all of these methods force switching converters to behave linearly as in (2.2). The differences between these concepts arise from their respective derivations and hardware implementations. LCAM does not propose a new concept of linearization, but rather a different method by which to implement it.
The constant $k$ is used as a scaling factor for $V_{cmd}$. If $k = 1$,

$$V_{out} = V_{cmd}$$

(2.11)

For boost converters, the desired $V_{out}$ may be much larger than any available command voltage. By using the factor $k$, a PWM signal with the desired duty cycle can still be produced with a lower command voltage. It will be assumed for the remainder of this paper that $V_{cmd}$ is a nominal voltage that can be easily obtained. For simplicity the scaling factor $k$ is assumed to be equal to one.

A block diagram showing the complete LCAM system applied to the boost converter can be seen in Figure 2-7. The PWM signal is generated by comparing $V_{in}$ to the amplitude modulated triangular carrier. This triangular carrier is generated by a hysteretic modulator whose input is the control reference $V_{cmd}$. The upper hysteretic limit of the modulator determines the amplitude of the triangle wave and is set to $V_{cmd}$. The details of the modulator’s operation are covered thoroughly in Chapter 3.
Figure 2-7: Block diagram of the complete system used to realize LCAM control for the boost converter.
CHAPTER 3
HYSTERETIC MODULATOR

This chapter examines the operation of a hysteretic modulator, both in its ideal form and in a physical circuit realization.

Ideal Hysteretic Modulator

Basic Operation

The hysteretic modulator is used to create a triangular voltage waveform whose amplitude can be directly modulated with the quasi-DC command voltage, $V_{cmd}$. An ideal diagram of the hysteretic modulator is shown in Figure 3-1.

Figure 3-1: Ideal hysteretic modulator.
Operation of the modulator begins with the capacitor $C_{MOD}$ discharged and the current source $I_{up}$ switched off, so it does not conduct. The current source $I_{down}$ draws current from $C_{MOD}$, which lowers the voltage, $V_{CMOD}$, slightly below zero. As this occurs, comparator $COMP_2$ outputs a logic low and the SR latch is reset. The switch control logic causes $I_{up}$ to switch on. For proper circuit operation it is assumed that $|I_{up}| > |I_{down}|$.

With this assumption, $C_{MOD}$ is now charged up with a constant current, $i_{CMOD} = |I_{up}| - |I_{down}|$. The voltage $V_{CMOD}$ ramps up at a constant rate as seen in Figure 3-2.

![Figure 3-2: The voltage across $C_{MOD}$. $V_{CMOD}$ ramps up and down between the two hysteretic limits $V_+$ and $V_-$. $V_+$ is set to $V_{ref}$ and $V_-$ is grounded in this case.](image)

When the magnitude of $V_{CMOD}$ grows slightly larger than $V_{cmd}$, comparator $COMP_1$ outputs a logic low and the SR latch is set. The switch control logic causes $I_{up}$ to turn off, and $C_{MOD}$ is discharged by the current source $I_{down}$. The constant-current discharge of the capacitor causes $V_{CMOD}$ to ramp back down. As $V_{CMOD}$ again falls slightly below zero, the latch is reset and $I_{up}$ is turned back on. The two boundary voltages, $V_{cmd}$ and 0V, form the upper and lower hysteretic limits of the modulator. This process of charging and discharging $C_{MOD}$ continues, and a triangular waveform seen in Figure 3-2 is produced.
Operating Frequency

The operating frequency of the hysteretic modulator is determined by the speed at which the current sources charge and discharge the modulation capacitor $C_{mod}$. With the desired operating frequency known, the relationships between the current sources and modulation capacitor can be derived to achieve the leading edge, trailing edge and symmetrically modulated triangular waveforms in Figure 3-3.

![Figure 3-3: Triangle shapes that can be achieved with a hysteretic modulator.](image)

Current Sources

From basic circuit theory, the relationship between the current and voltage of a capacitor is

$$i_c = C \frac{dv_c}{dt} \approx C \frac{\Delta v_c}{\Delta t}$$  \hspace{1cm} (3.1)

Using this approximation and the signals from Figure 3-1, (3.1) can be rearranged to
For a given modulator design, $C_{MOD}$ is fixed and $|\Delta v_{CMOD}| = V_{cmd}$, which is the same for both charging and discharging events. This is due to the fact that the hysteretic thresholds are relatively fixed within each switching period as long as the carrier amplitude varies slowly compared to the switching period. Substituting $|\Delta v_{CMOD}| = V_{cmd}$ into (3.2), it is seen that

\[
\frac{|\Delta v_{CMOD}|}{\Delta t} = \frac{|I_{CMOD}|}{C_{MOD}} \tag{3.2}
\]

Next, equating (3.3) and (3.4) it is shown that

\[
V_{cmd}C_{MOD} = |I_{CMOD}|_{\text{charging}} t_{\text{rise}} \tag{3.3}
\]
and

\[
V_{cmd}C_{MOD} = |I_{CMOD}|_{\text{discharging}} t_{\text{fall}} \tag{3.4}
\]

for any of the waveforms in Figure 3-.

Next, equating (3.3) and (3.4) it is shown that

\[
|I_{CMOD}|_{\text{charging}} = \kappa |I_{CMOD}|_{\text{discharging}} \tag{3.5}
\]

where $\kappa \equiv \frac{t_{\text{fall}}}{t_{\text{rise}}}$.

As $C_{MOD}$ is being discharged, $I_{up}$ is off, and therefore from Figure 3-1

\[
I_{down} = |I_{CMOD}|_{\text{discharging}} \tag{3.6}
\]

Similarly, as $C_{MOD}$ is charged up

\[
|I_{CMOD}|_{\text{charging}} = I_{up} - I_{down} \tag{3.7}
\]

Combining (3.6) and (3.7)

\[
I_{up} = |I_{CMOD}|_{\text{charging}} + |I_{CMOD}|_{\text{discharging}} \tag{3.8}
\]

Finally, substituting (3.5) into (3.8)

\[
I_{up} = (1 + \kappa)|I_{CMOD}|_{\text{discharging}} \tag{3.9}
\]
or

\[ I_{up} = (1 + \kappa)I_{down} \]  \hfill (3.10)

The ratio \( \kappa \) determines which type of waveform from Figure 3-3 is produced. For a leading edge waveform, where \( t_{\text{fall}} << t_{\text{rise}} \), \( \kappa \) will be a small value. Conversely, for a trailing edge \( \kappa \) will be large. In a symmetrical waveform, \( t_{\text{fall}} = t_{\text{rise}} \) and \( \kappa \) will be unity.

**Modulation Capacitor**

The value of the modulation capacitor, \( C_{\text{MOD}} \), needed to achieve a given frequency is derived from (3.1). Again assuming that \( |\Delta V_{\text{MOD}}| = V_{\text{cmd}} \),

\[ C_{\text{MOD}} = \frac{i_{\text{CMOD}} \Delta t}{V_{\text{cmd}}} \]  \hfill (3.11)

When \( C_{\text{MOD}} \) is discharging, (3.11) becomes

\[ C_{\text{MOD}} = \frac{I_{\text{down}} \Delta t}{V_{\text{cmd}}} \]  \hfill (3.12)

For any of the waveforms in Figure 3-3,

\[ T = t_{\text{rise}} + t_{\text{fall}} \]  \hfill (3.13)

which can be rearranged into

\[ t_{\text{fall}} = T \left( \frac{\kappa}{1 + \kappa} \right) = \frac{1}{f} \left( \frac{\kappa}{1 + \kappa} \right) \]  \hfill (3.14)

During the discharge of \( C_{\text{MOD}} \), \( \Delta t = t_{\text{fall}} \) and (3.12) becomes

\[ C_{\text{MOD}} = \frac{\kappa I_{\text{down}}}{fV_{\text{CMD}} (1 + \kappa)} \]  \hfill (3.15)
While this derivation was done for a discharging event, the same result is achieved from a charging event. Any frequency waveform from Figure 3-3 can now be obtained by the proper choice of $I_{up}$, $I_{down}$, and $C_{MOD}$.

**Physical Realization of the Hysteretic Modulator**

The previous model of the hysteretic modulator provides the means to examine its operation under ideal conditions. Implementation of the circuit requires the use of non-ideal parts and physical realization of the hardware needed for logic control. Figure 3-4 shows the schematic of the modulator with non-ideal components that is used to verify operation in Chapter 5.

Operation of this circuit is similar to the ideal model. A symmetrical triangular waveform, with $\kappa = 1$, is assumed to be used for the circuit of Figure 3-4. As before, $C_{MOD}$ begins discharged, and $I_{up}$ is initially off. $I_{up}$ is realized with the trans-conductance amplifier consisting of $Q_1$ and $U_1$. $V_{CMOD}$ is brought down as the current $i_{CMOD} = I_{down}$ is drawn from the capacitor, and when $V_{CMOD}$ crosses the lower hysteretic limit $COMP_1$ resets the SR latch. The lower hysteretic limit is can be adjusted by the source $V_{offset}$ to account for delays in the comparator and in the switching logic. The reset signal output from the SR latch is then sent to the switching logic that controls $I_{up}$. This switching logic consists of an inverting gate-driver, and a level shifting zener diode. By controlling the voltage at the top of $I_{up}$ the current from this source can be switched on and off. Level shifting of the set and reset signals is necessary to ensure that the active components of $I_{up}$ remain in the correct operating modes.
The reset signal from the SR latch is inverted and $I_{up}$ turns on similar to the ideal case. From (3.10), to achieve a symmetrical triangle wave, $I_{up} = 2I_{down}$. The capacitor voltage, $V_{CMOD}$, is charged up to the upper hysteretic limit, $V_{cmd}$, and COMP$_1$ outputs a logic low to set the latch. The gate driver inverts the set signal from the SR latch causing $I_{up}$ to turn off and $C_{MOD}$ to discharge. As in the ideal case, modulation continues as $C_{MOD}$ is charged and discharged, and a symmetrical triangle is produced. The causes and effects of the various delays associated with non-ideal components are covered in Chapter 4.

![Diagram of hysteretic modulator with non-ideal components](image)

Figure 3-4: Physical realization of the hysteretic modulator using non-ideal components.
CHAPTER 4
DESIGN ORIENTED MODELING

This chapter provides a detailed explanation of the non-ideal hysteretic modulator seen in Figure 4-1. Guidelines for choosing components and component values are also given. All derivations are made assuming a symmetrical triangle waveform.

Figure 4-1: Schematic of the non-ideal hysteretic modulator.

Realizing the Modulation Frequency

Assuming the switching frequency is known, the physical realization of the hysteretic modulator becomes an iterative process. First, the type of triangle waveform, leading-edge, trailing edge or symmetrical, must be chosen. For this circuit, a symmetrical waveform was used and the value of $\kappa = 1$. Next, either the value of $C_{MOD}$ or $I_{down}$ must be selected. The other value is then calculated using (3.15). It is possible that this calculated value will exceed some design constraint and values for both
must be redone. For instance, the value of $I_{\text{down}}$ calculated for a chosen capacitance value may be higher than component tolerances allow. In this case, lower capacitances values can be iterated until an acceptable $I_{\text{down}}$ is achieved. $I_{\text{up}}$ is always larger than $I_{\text{down}}$, and will most likely be unacceptable if $I_{\text{down}}$ is too large.

The relationship between $C_{\text{MOD}}$ and $I_{\text{down}}$ was given in (3.15) and is repeated here for convenience.

$$C_{\text{MOD}} = \frac{\kappa I_{\text{down}}}{f V_{\text{cmd}} (1 + \kappa)}$$  (4.1)

$V_{\text{cmd}}$ is the control signal that modulates the amplitude of the carrier, and it is therefore assumed that $V_{\text{cmd}}$ will vary. If $I_{\text{down}}$ is assumed to be fixed, then for changes in $V_{\text{cmd}}$, the capacitor $C_{\text{MOD}}$ must vary in order for frequency to remain the same. Variable capacitance is difficult to obtain in practice and is not a practical solution. On the other hand, if $C_{\text{MOD}}$ is assumed to be fixed, then for constant frequency operation $I_{\text{down}}$ must vary with $V_{\text{cmd}}$. Rearranging (4.1) shows a linear relationship between $I_{\text{down}}$ and $V_{\text{cmd}}$.

$$i_{\text{CMOD}} = 2 f C_{\text{MOD}} V_{\text{cmd}}$$  (4.2)

A transconductance, $g_m$, found from (4.2) is defined as

$$g_m = \frac{i_{\text{CMOD}}}{V_{\text{cmd}}} = 2 f C_{\text{MOD}}$$  (4.3)

**Selection of $C_{\text{MOD}}$**

The choice of $C_{\text{MOD}}$ must take several factors into account. In order to maintain a reliable modulation frequency, the capacitance value must be stable over the entire voltage range of $V_{\text{cmd}}$ and all possible operating temperatures. Since the controller may be in close physical proximity to the boost converter, there is the possibility of high temperatures generated by power devices. For integrated designs, $C_{\text{MOD}}$ should be as
small as possible, but must remain large enough to overcome parasitic capacitances from
the process. The active devices associated with the current sources can also cause stray
capacitance in parallel with $C_{MOD}$. Small designs may require small components, which
may put a limit on the capacitance. For non-integrated designs, mica capacitors make a
good choice for temperature and voltage stability.

**Design of $I_{down}$**

With a chosen capacitance for $C_{MOD}$, the relationship between $I_{down}$ and $V_{cmd}$ in
(4.3) can be realized using a transconductance current source. A schematic of the source
$I_{down}$ can be seen in Figure 4-2(a). The current produced by $I_{down}$ is a function of the
voltage applied across the bias resistor, $R_{down}$. To set the transconductance of this source,
the value of $R_{down}$ needed is

$$R_{down} = \frac{1}{g_m}$$  \hspace{1cm} (4.4)

Combining (4.3) and (4.4), the resistance needed for the current source $I_{down}$ is

$$R_{down} = \frac{1}{2fC_{MOD}}$$  \hspace{1cm} (4.5)

**Design of $I_{up}$**

The current source $I_{up}$, seen in Figure 4-2(b) is realized with the same circuit
topology as $I_{down}$. There are two differences between these current sources. From (3.10),
it can be shown that for a symmetrical triangle wave, where $\kappa = 1$, that $I_{up} = 2I_{down}$. For
a given value of $V_{cmd}$, the transconductance of $I_{up}$ must twice as large as that of $I_{down}$ to
meet this specification. The bias resistor of $I_{up}$ is then given by

$$R_{up} = \frac{1}{2g_m} = \frac{1}{2(2fC_{MOD})} = \frac{1}{4fC_{MOD}}$$  \hspace{1cm} (4.6)
The other difference between the two current sources is that \( I_{up} \) must be able to quickly switch on and off, while \( I_{down} \) remains constant. The voltage across \( R_{up} \) must therefore be switched quickly between \( V_{cmd} \) in the on state, and zero in the off. It should be noted that in the off state, the voltage across this resistor does not fall below zero. If the terminal \( V_s \) in Figure 4-2(b) were switched to ground instead of \( V_{cc}/2 \), the biasing of the op-amp and BJT would change. When the current source switches back on, there would be a recovery time required to re-bias the circuit. During this recovery time there is no current flowing from \( I_{up} \), and the triangle wave experiences overshoot and flat-spots.

![Current Source Topology](image.png)

Figure 4-2: Current source topology used to generate (a) \( I_{down} \) and (b) \( I_{up} \) in the hysteretic modulator.

**Switching Logic and Level Shifting**

Control circuitry is needed to realize the switching of the node \( V_s \) in Figure 4-2(b), and also to make sure that the op-amp and BJT remained biased in the active region. The sub-circuit seen in Figure 4-3 is used to achieve the switch signal that drives the current source \( I_{up} \). The circuit consists of a zener diode, bias resistor and inverter.
Figure 4-3: Level shifting implementation. Switching circuitry to drive $I_{up}$ and the associated input and output waveforms.

The input to the switching logic is a square wave output from the SR latch. This signal is a standard TTL signal and switches between its power supply voltage and ground. The switching node of the current source, $V_s$, is directly controlled by the inverter, whose power and ground supply rails represent the on and off voltages of $I_{up}$. By biasing the supply rails in this manner, the inverter’s output will swing between the two desired levels and prevent the transistors in the current source from leaving the active region. The zener diode is needed to level shift the TTL latch signal to a level that the inverter can use as an input. Figure 4-3 shows the result of the level shifting with the small delay caused by the inverter.
Design of the Level Shifter

Determining the correct amount of DC level shifting is necessary to ensure that the inverter can input the TTL logic levels from the SR latch. Standard inverters do not respond properly when the input voltage is less than the value of their ground pin. Therefore, the zener voltage of the diode, $V_z$, should be such that it shifts the SR latch TTL signal by an amount equal to the value of the ground pin on the inverter.

$$V_z = \frac{V_{cc}}{2}$$  \hspace{1cm} (4.7)

By doing this, a logic low from the latch will be at the voltage corresponding to a logic low on the inverter.

A bias resistor is required to provide current to the cathode end of the zener diode. Using (4.7), when the input to the zener, $V_{in}$, is high the voltage across the resistor is given as

$$V_{Rbias} = V_{cc} - V_z - V_{in} = \frac{V_{cc}}{2} - V_{in}$$  \hspace{1cm} (4.8)

When the input is low

$$V_{Rbias} = V_{cc} - V_z = \frac{V_{cc}}{2}$$  \hspace{1cm} (4.9)

The resistance $R_{bias}$ must be chosen to provide ample bias current during a high input and still remain lower than the maximum current during a low input. This means

$$\frac{V_{cc} - V_{in}}{2} > I_{min}$$  \hspace{1cm} (4.10)

and

$$\frac{V_{cc}}{2R_{bias}} < I_{max}$$  \hspace{1cm} (4.11)
Here $I_{\text{min}}$ is the minimum current required by the zener diode to function as a voltage level shifter, and $I_{\text{max}}$ is the largest current that the diode can safely conduct.

Combining and rearranging (4.10) and (4.11)

$$\frac{V_{cc}}{2I_{\text{max}}} < \frac{V_{cc} - V_{in}}{2I_{\text{min}}}$$

(4.12)

**Selection of the Inverter**

The inverter must be capable of driving the capacitive load of the current source $I_{up}$ without excessive delay. The amount of delay allowed depends on the modulating frequency of the circuit. The capacitive load of concern is a combination of the capacitances from the BJT emitter and the op-amp minus pin.

To drive this capacitive load, an inverting gate driver can be used for the inverter in Figure 4-3. Gate drivers are designed to quickly charge and discharge the large gates of power MOSFETs, and many can do so in the MHz frequency range.

**Comparators and SR Latch**

Several issues arise in the choice of the comparators and SR latch for the hysteretic modulator. These include the comparator and latch speeds, offset voltage, and supply voltages needed for the latch and comparator.

**Comparator and Latch Speed**

Any delay between the signal $V_{\text{CMOD}}$ and the current source $I_{up}$ can greatly influence the operating frequency of the modulator. Figure 4-4 illustrates two possibilities for the triangular waveform $V_{\text{CMOD}}$. The solid line represents an ideal system with no delays, while the dashed line shows a system where delays are present.
Comparator delay and latch delay both cause the operating frequency to decrease because they slow the propagation of the switching signal to $I_{up}$.

![Diagram](image)

Figure 4-4: $V_{CMOD}$ for the ideal case without delays (solid) modulates between the two hysteretic thresholds. Delays cause $V_{CMOD}$ to overshoot the thresholds (dashed) and change frequency.

With ideal comparators, when the triangle wave crosses a hysteretic threshold the output of the comparator should switch. If no other delays are present in the latch and switching logic, the current source $I_{up}$ will immediately switch and the triangle wave will reverse direction. An ideal system such as this experiences no overshoot of the hysteretic limits. For non-ideal comparators, however, there is a small delay time after the triangle crosses the hysteretic limit, $t_{c-delay}$. During this delay time, the signal telling $I_{up}$ to switch positions has not yet propagated past the comparator. The same current continues to charge or discharge $C_{MOD}$, and $V_{CMOD}$ continues past the hysteretic limit. The overshoot causes the frequency of the triangle to be less than the ideal case.

Similarly, the delay of the SR latch can cause overshoot of the hysteretic limits. For an ideal comparator, the output switches as the triangle reaches a hysteretic limit. Delay in the latch, $t_{l-delay}$, causes $I_{up}$ to remain in the same state, much in the same manner as comparator delay. The voltage will continue in the same direction, either charging or discharging $C_{MOD}$, and will overshoot.
The delays of the comparator and latch can be added to find the total delay encountered before the switching logic.

\[
\text{delay} = \text{delay}_c + \text{delay}_l
\]

In order to achieve the desired operating frequency, the total delay must be much less than the operating period,

\[
t_{\text{delay}} < \frac{1}{f}
\]

or

\[
t_{\text{delay}} \leq 0.01T
\]

**Selection of the Offset Voltage**

Depending on the comparator, there is a chance that there will be some overshoot of the lower hysteretic limit as seen in Figure 4-5. This is due to the fact that the lower limit is set to ground, the same as the lower supply voltage. This type of biasing can cause transistors in the comparator to enter regions of operation that have slower performance. In this case, an offset voltage, \( V_{\text{offset}} \), is used to correct the overshoot. The lower hysteretic limit is set to \( V_{\text{offset}} \), so that even if \( V_{\text{CMOD}} \) overshoots the threshold, the triangle modulates between \( V_{\text{cmd}} \) and zero.

![Diagram](image-url)

**Figure 4-5:** Overshoot of the lower hysteretic limit requires the use of \( V_{\text{offset}} \).
Choosing $V_{\text{offset}}$ is done by assuming that the slope of the voltage waveform is constant and independent of the hysteretic limit. In a time $\Delta t$, the voltage will overshoot zero, which was the original threshold, by an amount equal to $|V_{\text{overshoot}}|$. To remove this overshoot, the waveform must cross the new hysteretic limit, $V_{\text{offset}}$, at a time $\Delta t$ before it crosses zero. For a constant slope, this means that

$$V_{\text{offset}} = V_{\text{overshoot}}$$ \hspace{1cm} (4.16)

The exact amount of overshoot present may not be known in the design stage and may need to be empirically determined. It is therefore a good design practice to leave $V_{\text{offset}}$ as an adjustable parameter.

**Design Summary**

This chapter has examined the design of a hysteretic modulator to be used in an LCAM system. The design procedure is summarized in Table 4-1. Parameters and components selected for the experimental circuit are included in the table, with brief comments on why they were chosen. Those that do not have specific design equations associated with them should be chosen to accommodate the system to which they are being applied. Acceptable component delays depend upon the chosen frequency of operation, and the power supply rails are design-specific.
Table 4-1: Design summary for the hysteretic modulator needed to implement LCAM control on the boost converter.

<table>
<thead>
<tr>
<th>Design Specification</th>
<th>Design Equation</th>
<th>Value/Component</th>
<th>Comments/Selection Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>Specified by converter</td>
<td>~500kHz</td>
<td>T = 2000ns</td>
</tr>
<tr>
<td>Vcc</td>
<td>User Defined</td>
<td>12V</td>
<td>Provides wide voltage range for testing purposes.</td>
</tr>
<tr>
<td>Vee</td>
<td>User Defined</td>
<td>-12V</td>
<td></td>
</tr>
<tr>
<td>CMOD</td>
<td>User Defined</td>
<td>68pF, Mica</td>
<td>temp/current independent</td>
</tr>
<tr>
<td>R\text{down}</td>
<td>(4.4)</td>
<td>5.1kohm</td>
<td></td>
</tr>
<tr>
<td>R\text{up}</td>
<td>(4.6)</td>
<td>2.4kohm</td>
<td></td>
</tr>
<tr>
<td>Zener</td>
<td>(4.7)</td>
<td>1N4735</td>
<td></td>
</tr>
<tr>
<td>R\text{bias}</td>
<td>(4.12)</td>
<td>620ohm</td>
<td>41ohm &lt; 620ohm &lt; 1kohm</td>
</tr>
<tr>
<td>COMP\text{1,2}</td>
<td>(4.15)</td>
<td>LT1720</td>
<td>\tau_{\text{c-delay}} &lt; 10ns \ll T = 2000ns</td>
</tr>
<tr>
<td>SR Latch</td>
<td>(4.15)</td>
<td>DM74S00N</td>
<td>\tau_{\text{t-delay}} &lt; 10ns \ll T = 2000ns</td>
</tr>
<tr>
<td>Inverter</td>
<td>User Defined</td>
<td>ICL7667</td>
<td>\tau_{\text{delay}} &lt; 60ns \ll T = 2000ns (for 1nF load)</td>
</tr>
<tr>
<td>Op-Amp</td>
<td>User Defined</td>
<td>LM837A</td>
<td></td>
</tr>
<tr>
<td>PNP</td>
<td>User Defined</td>
<td>2907</td>
<td></td>
</tr>
<tr>
<td>NPN</td>
<td>User Defined</td>
<td>2N2222</td>
<td></td>
</tr>
<tr>
<td>V\text{offset}</td>
<td>(4.16)</td>
<td>0.84V</td>
<td>Experimentally determined.</td>
</tr>
</tbody>
</table>
CHAPTER 5
SIMULATION AND VERIFICATION

The purpose of this chapter is to verify the operation of the LCAM system applied to the boost converter. The first section includes explanations of the circuits and circuit models used for theoretical calculations, simulations and gathering measured data. The second section examines the measured results of a working LCAM system, and compares them to data from the models and simulations.

Verification Techniques

This section begins with a derivation of the boost transfer function using LCAM from a simplified circuit model. The circuit used for simulations is presented next. Finally, a schematic of the system used to gather measured data is shown and measurement techniques are discussed.

Boost Transfer Function with LCAM

In the steady-state, the output voltage of the ideal boost converter in Figure 1-1 is given in (1.1). A more physical model with losses included can be seen in Figure 5-1.

Figure 5-1: Boost converter with losses.
The output voltage of the boost with losses [1] can be approximated by

\[ V_{out} = \left( \frac{1}{D'} \right) \left( V_{in} - D'V_{diode} \right) \left( \frac{D'^2 R_L}{D'^2 R + R_{ind} + DR_{ds} + D'R_{diode}} \right). \]  

(5.1)

If the output current, \( I_{out} \), is constant, then the load \( R_L \) in (5.1) can be replaced by

\[ R_L = \frac{V_{out}}{I_{out}}. \]  

(5.2)

Substituting equation (5.2) into (5.1) and solving for \( V_{out} \) yields

\[ V_{out} = \frac{I_{out} \left( \frac{1}{D'} \right) \left( V_{in} - D'V_{diode} \right) \left( \frac{D'^2}{I_{out}} \right) - R_{ind} - DR_{ds} - D'R_{diode} \}}{D'^2} \]  

(5.3)

Using the LCAM scheme, the compliment duty cycle produced is given by

\[ D' = \frac{V_{in}}{V_{cmd}}. \]  

(5.4)

Combining (5.3) and (5.4), the new relationship between \( V_{out} \) and \( V_{cmd} \) is found to be

\[ V_{out} = V_{cmd} - V_{diode} - I_{out} \left( \frac{V_{cmd}}{V_{in}} \right)^2 \left[ R_{ind} + \left( \frac{V_{in}}{V_{cmd}} \right) R_{ds} + \frac{V_{in}}{V_{cmd}} R_{diode} \right]. \]  

(5.5)

The new output voltage can be split into three terms, \( V_{cmd} \) and two loss terms. The first loss term is the forward voltage drop of the diode, \( V_{diode} \), which is assumed to be constant to simplify these calculations. This simplification is justified by the previous assumption of a constant output current. The second loss term is dependant on the operating point of the modulator and the losses associated with the converter. The converter losses for this model can be seen in Table 5-1. If the converter losses are removed, (5.5) reduces to the ideal LCAM relationship of (2.2).

<table>
<thead>
<tr>
<th>Loss Term</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{ds} )</td>
<td>10mOhm</td>
</tr>
<tr>
<td>( R_{ind} )</td>
<td>8mOhm</td>
</tr>
<tr>
<td>( V_{diode} )</td>
<td>0.20V</td>
</tr>
<tr>
<td>( R_{diode} )</td>
<td>40mOhm</td>
</tr>
</tbody>
</table>
Simulation Model

The schematic seen in Figure 5-2 is used in Saber to simulate the operation of the boost converter with LCAM control. Component values and operating parameters for the hysteretic modulator are given in Table 5-2. These values and components were chosen using the design methodology of Chapter 4. The values for the boost converter components are given in Table 5-3.

Table 5-2: Hysteretic modulator simulation parameters and components.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value / Part #</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{cc}$</td>
<td>+12V</td>
</tr>
<tr>
<td>$V_{ee}$</td>
<td>-12V</td>
</tr>
<tr>
<td>$R_1$</td>
<td>5.8kOhm</td>
</tr>
<tr>
<td>$R_2$</td>
<td>2.7kOhm</td>
</tr>
<tr>
<td>$V_{os}$</td>
<td>0.048V</td>
</tr>
<tr>
<td>$C_{MOD}$</td>
<td>150pF</td>
</tr>
<tr>
<td>LATCH</td>
<td>ndlch_l4</td>
</tr>
<tr>
<td>Q1</td>
<td>mmbt2222_sl</td>
</tr>
<tr>
<td>Q2</td>
<td>mmbt2907_sl</td>
</tr>
<tr>
<td>U1,2</td>
<td>lm837_sl</td>
</tr>
<tr>
<td>COMP1,2,3</td>
<td>comp_l4</td>
</tr>
</tbody>
</table>

Table 5-3: Boost converter values used in simulation.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_L$</td>
<td>20.1uF</td>
</tr>
<tr>
<td>L</td>
<td>4.6uH</td>
</tr>
<tr>
<td>$R_{ind}$</td>
<td>8mOhm</td>
</tr>
<tr>
<td>$R_{ds}$</td>
<td>10mOhm</td>
</tr>
<tr>
<td>$V_{diode}$</td>
<td>0.20V</td>
</tr>
<tr>
<td>$R_{diode}$</td>
<td>40mOhm</td>
</tr>
</tbody>
</table>

Experimental Verification

Experimental data are gathered from an LCAM system whose schematic is seen in Figure 5-3. The bill of materials at the end of the chapter lists all of the components and component values used to construct this circuit. In order to make the measurements more uniform, the boost converter was loaded with a constant-current active load.
Figure 5-2: Saber schematic used for circuit simulations.

Waveforms were measured with the Tektronix TDS460A 4-channel oscilloscope. The value of $I_{out}$ was verified with a Tektronix TM502A current probe. The bias and offset voltage used to implement the design in Figure 5-3 can be found in Table 5-4.

Table 5-4: Bias and offset voltages

<table>
<thead>
<tr>
<th>Design Specification</th>
<th>Value/Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>12V</td>
</tr>
<tr>
<td>Vee</td>
<td>-12V</td>
</tr>
<tr>
<td>$V_{offset}$</td>
<td>0.84V</td>
</tr>
</tbody>
</table>
Figure 5-3: Boost converter and LCAM system used to measured data.

**Results**

Figure 5-4 shows several of the key operational waveforms taken from the boost converter with the LCAM system. The triangular carrier, $V_{CMOD}$, ramps between the two hysteretic limits. These limits are set to zero and $V_{cmd}$, which is 5V in this case. The square wave is the PWM signal output from COMP3 that drives M1. The output voltage, $V_{out}$, is a DC signal with some switching noise. The average value of $V_{out}$ is approximately 5V, the same as $V_{cmd}$. 
Figure 5-4: Measured waveforms.

Figure 5-5 demonstrates the linearity of the output voltage under LCAM control. The input voltage, $V_{in}$, and output current, $I_{out}$, were kept constant while the reference voltage, $V_{cmd}$, was swept. The close agreement between the calculated, simulated and experimental data suggests that the models of the LCAM system are accurate.

The ultimate goal of the LCAM system is to force the steady-state output voltage of the boost converter to be a linear function of only the command voltage. This ideal behavior can be accomplished in a lossless converter. However, as (5.5) suggests, the effects of the input voltage and output current cannot be ignored.
Figure 5-5: $V_{out}$ vs. $V_{cmd}$ curve with calculated, simulated and measured data.

In Figure 5-6, the measured $V_{out}$ vs. $V_{cmd}$ is plotted for a family of $I_{out}$ values. The value of $V_{in}$ is held constant at a nominal value. As suggested by (5.5), high $I_{out}$ values increase the losses produced by the operating-point dependant term and lead to smaller output voltages.

Figure 5-6: A family of $V_{out}$ vs. $V_{cmd}$ curves for several values of $I_{out}$. 
Figure 5-7 shows the effect that different $V_{in}$ values have on $V_{out}$. For each different value of $V_{in}$, $I_{out}$ is held constant while $V_{cmd}$ is swept. According (5.5) as $V_{in}$ gets larger the second loss term is reduced and $V_{out}$ is higher for a specific value of $V_{cmd}$.

![Graph of $V_{out}$ vs. $V_{cmd}$ with varying $V_{in}$](image)

Figure 5-7: A family of $V_{out}$ vs. $V_{cmd}$ curves for several values of $V_{in}$.

It should be noted that while $V_{in}$ and $I_{out}$ offset the $V_{out}$ vs. $V_{cmd}$ curves in Figure 5-6 and Figure 5-7, the linear relationship between the command and the output is preserved.
Table 5-5: Bill of materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Quantity</th>
<th>Reference</th>
<th>Part</th>
<th>Footprint</th>
<th>Vendor</th>
<th>Vendor Part #</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>L</td>
<td>4.6uH</td>
<td>Axial</td>
<td>Wilco</td>
<td>LFB47G</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>C₁</td>
<td>20.1uF</td>
<td>Radial</td>
<td>OSCON</td>
<td>20SP22M</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>M₁</td>
<td>NMOS</td>
<td>SO-8</td>
<td>Fairchild</td>
<td>FDS6670</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>GD₁</td>
<td>Gate Driver</td>
<td>8PDIP</td>
<td>Texas Instruments</td>
<td>UCC27324</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>D₁</td>
<td>Diode</td>
<td>TO-220AB</td>
<td>International Rectifier</td>
<td>40L15CT</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>R₄</td>
<td>Active Load</td>
<td>N/A</td>
<td>acdc electronics</td>
<td>EL-300</td>
</tr>
<tr>
<td>7</td>
<td>3</td>
<td>COMP₁, COMP₂, COMP₃</td>
<td>Comparator</td>
<td>SO-8</td>
<td>Linear Technology</td>
<td>LT1720</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>C_MOD</td>
<td>68pF</td>
<td>Radial</td>
<td>Various</td>
<td>Various</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>R_down</td>
<td>5.1kOhm</td>
<td>Axial</td>
<td>Various</td>
<td>Various</td>
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LIST OF REFERENCES


BIOGRAPHICAL SKETCH

Alex Phipps obtained his BS degree in Electrical Engineering from the University of Florida in 2004. He has been a research assistant for the Department of Electrical Engineering at UF since 2005 and is currently a Masters candidate. His field of interest is the design of electronic circuits for power management.