ANALOG BASEBAND PROCESSOR
FOR CMOS 5-GHZ WLAN RECEIVER

By

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# TABLE OF CONTENTS

 Acknowledgments .......................................................................................................................... ii  

 List of Tables ................................................................................................................................ vii  

 List of Figures ............................................................................................................................... viii  

 Abstract ........................................................................................................................................ xi  

 Chapter  

 1 Introduction ........................................................................................................................................... 1  

 1.1 Motivation ........................................................................................................................................ 1  

 1.2 Research Goals ............................................................................................................................... 2  

 1.3 Outline of the Dissertation ........................................................................................................ 3  

 2 Background ......................................................................................................................................... 5  

 2.1 IEEE 802.11a Standard .................................................................................................................... 5  

 2.2 System Specifications for WLAN Receiver .................................................................................... 7  

 2.3 Receiver Architecture and Analog Baseband Signal Chain .......................................................... 9  

 2.4 AGC Fundamentals ........................................................................................................................ 12  

 3 OFDM Signal Amplitude Estimation .............................................................................................. 18  

 3.1 OFDM Signal Characteristics ....................................................................................................... 18  

 3.2 OFDM Signal Generation .............................................................................................................. 20  

 3.3 Analog OFDM Signal Amplitude Estimation with Statistical Simulation .................................... 22  

 3.4 Accuracy Boundary for Received OFDM Short Training Symbols ........................................... 26  

 4 Seventh Order Elliptic Low-Pass GM-C Filter .................................................................................. 28  

 4.1 Introduction .................................................................................................................................... 28  

 4.1.1 Specifications ........................................................................................................................... 28  

 4.1.2 Filter Topology ........................................................................................................................ 30
<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1.</td>
<td>Receiver performance requirements</td>
<td>8</td>
</tr>
<tr>
<td>3-1.</td>
<td>Statistical simulation result for 5000 symbols (Max Peak = 0.607)</td>
<td>24</td>
</tr>
<tr>
<td>4-1.</td>
<td>Spreadsheet to compute parasitic capacitance, number of dummy cells, and main capacitor value at each node</td>
<td>39</td>
</tr>
<tr>
<td>4-2.</td>
<td>Summary of characteristics of the two filters</td>
<td>47</td>
</tr>
<tr>
<td>5-1.</td>
<td>Summary of the simulation and measurement results</td>
<td>101</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>2-1</td>
<td>Frequency band allocation in the IEEE 802.11a standard</td>
<td>5</td>
</tr>
<tr>
<td>2-2</td>
<td>PLCP Protocol Data Unit frame format</td>
<td>7</td>
</tr>
<tr>
<td>2-3</td>
<td>Specifications of the minimum sensitivity signal channel with adjacent and</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>alternate adjacent channels for 6 and 54Mbps data rates</td>
<td></td>
</tr>
<tr>
<td>2-4</td>
<td>Architecture for the 5 GHz WLAN receiver</td>
<td>10</td>
</tr>
<tr>
<td>2-5</td>
<td>Baseband signal chain block diagram</td>
<td>11</td>
</tr>
<tr>
<td>2-6</td>
<td>Receiver gain distribution plots for 6Mbps data rate</td>
<td>13</td>
</tr>
<tr>
<td>2-7</td>
<td>Receiver gain distribution plots for 54Mbps data rate</td>
<td>14</td>
</tr>
<tr>
<td>2-8</td>
<td>AGC structure with (a) nonlinear feedback loop and (b) linearized loop</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>representation</td>
<td></td>
</tr>
<tr>
<td>3-1</td>
<td>A typical analog OFDM signal in the time domain</td>
<td>18</td>
</tr>
<tr>
<td>3-2</td>
<td>OFDM modulator</td>
<td>20</td>
</tr>
<tr>
<td>3-3</td>
<td>Short training symbols: (a) I channel one symbol (0.8µs) and 7 symbols, and</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td>(b) Q channel one symbol (0.8µs) and 7 symbols</td>
<td></td>
</tr>
<tr>
<td>3-4</td>
<td>Data symbol generation in the discrete time domain</td>
<td>22</td>
</tr>
<tr>
<td>3-5</td>
<td>Data symbol generation in continuous time domain</td>
<td>23</td>
</tr>
<tr>
<td>3-6</td>
<td>Data distribution plots for 6 detectors</td>
<td>25</td>
</tr>
<tr>
<td>3-7</td>
<td>Standard deviation plot for 6 detectors</td>
<td>25</td>
</tr>
<tr>
<td>3-8</td>
<td>OFDM short training symbol generation with channel effect</td>
<td>27</td>
</tr>
<tr>
<td>4-1</td>
<td>Channel attenuation requirements for the baseband low-pass filter</td>
<td>29</td>
</tr>
<tr>
<td>4-2</td>
<td>Frequency response (magnitude and group delay) for (a) 6th order elliptic,</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>(b) 9th order Chebyshev II, (c) 3rd order elliptic, and (d) 4th order elliptic filters</td>
<td></td>
</tr>
</tbody>
</table>
4-3. LC prototype filters for (a) 3rd order and (b) 4th order elliptic low-pass filters ........31
4-4. 3rd order Gm-C filter ..................................................................................................32
4-5. Internal node voltage plot of the 3rd order Gm-C filter: (a) before scaling and (b) after scaling ..........................................................33
4-6. 3rd order Gm-C filter after voltage scaling for internal nodes .............................33
4-7. Schematics of (a) unit Gm cell and (b) FC with CMFB unit .................................35
4-8. DC transfer characteristics of a unit Gm cell: (a) V-I plot, (b) Gm plot ...............37
4-9. Fully differential 3rd order Gm-C filter .................................................................38
4-10. Avoiding floating capacitor: (a) Gm-C filter with floating capacitor, (b) substitution of floating capacitor at node V1, (c) additional circuit for current source to node V1 .................................................................40
4-11. 3rd order Gm-C filter avoiding floating capacitor ............................................41
4-12. Internal node voltage plot of the 3rd order Gm-C filter avoiding floating capacitor ......................................................................................................................41
4-13. Internal node voltage plot of the 3rd order Gm-C filter avoiding floating capacitor ......................................................................................................................42
4-14. AC response simulation result for Filter 2 ..........................................................43
4-15. AC response simulation result for Filter 2 with tuning ........................................44
4-16. Transient response of the Filter 2 at (a) 8.3 MHz and (b) 12 MHz .......................44
4-17. Noise in dB vs. frequency plot .................................................................................45
4-18. Linearity of 1 % THD vs. input signal voltage for (a) Filter 1 and (b) Filter 2 in nominal case ........................................................................................................46
5-1. Conventional AGC loop composed of VGA, Peak Detector and Loop Filter .......49
5-2. Architecture of the proposed AGC algorithm; (a) block diagram and (b) time line ..50
5-3. Switched Gain Control 1 of the AGC algorithm ....................................................52
5-4. Switched Gain Control 2 of the AGC algorithm ....................................................52
5-5. AGC with One-step Correction: the fine gain-setting step ....................................53
5-6. Schematic of the proposed VGA .............................................................................56
5-7. Schematic of the replica bias circuit for VGA ...........................................................60

5-8. Simulation result for finding operating point in the replica bias circuit. The result verifies that the bias circuit (for $\Delta V = 0.6$ V) can operate only at the single operating point of $V_A = 1.26$ V and $V_B = 0.66$ V.....................................................60

5-9. Schematic of the proposed Differential Difference Amplifier ......................................62

5-10. Schematic of the proposed RMS detector ................................................................64

5-11. DC simulation results of the RMS detector with $V_{CM} = 0.48$ and $v_{in} = -0.25$ $\sim$ 0.25 V: (a) currents $I_{1,2}$ after squarer and (b) currents $I_{3,4}$ after rectifier .................64

5-12. V-to-I and I-to-V converters in (a) differential V to single-ended I, (b) single-ended V-to-I, and (c) single-ended I to differential V modes ........................................66

5-13. Schematic of the proposed analog computation block. The arrows indicate the $V_{GS}$’s that form the translinear loop ........................................................................68

5-14. Switched gain control block implementation using latched comparators and transmission gates ........................................................................................................70

5-15. DC simulation result of the single-ended V-to-I and I-to-differential V converters (single-ended $V_{C1}$ versus differential $V_{C1}$) .................................................71

5-16. Reference voltage generator $V_{INIT}$ has six taps for preset voltages and is implemented as serial and parallel connections of a root component resistor .......72

5-17. Reference voltage generator $V_{TH}$ provides threshold voltages ($V_{-20dBm}$, $V_{-22dBm}$ and $V_{-30dBm}$) either for short training symbol signal or for sine wave signal............73

5-18. Proposed AGC circuitry with 7 test points ................................................................75

5-19. Output voltage buffer ..................................................................................................76

5-20. Test switches; (a) voltage switch, and (b) current switch ............................................78

5-21. DC gain control simulation for the VGA with inverse gain loop ................................79

5-22. DC simulation for $V_{in}$ versus $V_{out}$ of the VGA at (a) –4 dB gain and (b) 16 dB gain ...........................................................................................................................79

5-23. AC response of the VGA; (a) gain and (b) phase .....................................................80

5-24. VGA input and output noise versus gain ..................................................................81

5-25. Linearity of the 2-stage VGA in THD (%) versus input signal voltage plots at (a) –8 dB, (b) 0 dB and (c) 32 dB gain settings .............................................................................81
5-26. Input versus output characteristic of RMS detector; (a) for sine wave signal and (b) for short training symbol ....................................................................................82

5-27. Characteristic of V-to-I converter; (a) input versus output linearity and (b) step response ..........................................................................................................................82

5-28. Input versus output characteristic of I-to-V converter ..........................................................................................................................83

5-29. DC simulation results of the computation block for sine wave signal with the switched gain of (a) –3 dB, (b) 7 dB, (c) 17 dB, and (d) 17 dB ......................................................................84

5-30. DC simulation results of the computation block for short training symbol signal with the switched gain of (a) –3 dB, (b) 7 dB, (c) 17 dB, and (d) 17 dB ......................................................................85

5-31. Transient simulation result (step response) of the computation block ..........................................................................................................................85

5-32. Transient simulation results of the AGC circuit for sine wave signal with final gain of (a) –3 dB, (b) 1 dB, (c) 4 dB and (d) 9 dB ..................................................................................87

5-33. Transient simulation results of the AGC circuit for sine wave signal with final gain of (a) 15 dB, (b) 20 dB, (c) 23 dB and (d) 28 dB ..................................................................................88

5-34. Transient simulation results of the AGC circuit for short training symbol signal with final gain of (a) –3 dB, (b) 1 dB, (c) 4 dB and (d) 9 dB ..................................................................................89

5-35. Transient simulation results of the AGC circuit for short training symbol signal with final gain of (a) 15 dB, (b) 20 dB, (c) 23 dB and (d) 28 dB ..................................................................................90

5-36. Full chip layout floor plan of the AGC circuit including ESD bonding pads and decoupling capacitor between positive supply and ground .....................................................................91

5-37. Die photo of the fabricated AGC circuit ..........................................................................................................................92

5-38. Test board design for the 40-pin AGC circuit package ..........................................................................................................................93

5-39. Test board with a packaged AGC sample plugged in ..........................................................................................................................93

5-40. Bias circuit with external resistor connection: (a) can cause oscillation and (b) can fix the problem ..........................................................................................................................94

5-41. Measurement results on device characteristics with various embedded test point selections: (a) diode-connected NMOS in RMS detector (W/L=5/10 µm), (b) diode-connected NMOS in cascode current mirror (W/L=3/3 µm), (c) threshold voltage extraction (diode-connected NMOS), and (d) measurement plot on bias current versus external resistor ..................................................................................95

5-42. Measurement of on-chip resistor variation: (a) resistors between input nodes and (b) measurement results for 20 samples ..........................................................................................................................96
5-43. Gain control curve for the 2-stage VGA ................................................................. 97
5-44. 2-stage VGA gain with supply voltage variation .................................................... 97
5-45. Stability of VGA gain with (a) bias current and (b) temperature variations ........ 98
5-46. 2-stage VGA characteristic at 12 dB gain: (a) input-output linearity, (b) SFDR .... 99
5-47. Frequency response of the 2-stage VGA: (a) measurement result and (b) simulation result ........................................................................................................... 99
5-48. Measurement result for input-output characteristic of the RMS detector ........... 100
5-49. Measurement result for input-output characteristic of the V-to-I converter ........ 100
5-50. Measurement result for input-output characteristic of the current mode computation block ........................................................................................................... 101
This dissertation discusses the design of an analog baseband processor including channel-select filtering with automatic gain control (AGC) for a 5-GHz CMOS WLAN receiver. Basic concepts and specifications of the IEEE 802.11a standard are reviewed. Coded orthogonal frequency division multiplexing (OFDM), employed in this standard for high data rate capability in multipath environments, degrades signal detection in the receiver due to the high peak-to-average power ratio (PAPR). Statistical simulation shows that RMS detection has the least error variance among several algorithms.

Channel-select filters of the analog baseband processor are implemented as 3rd and 4th order cascaded elliptic lowpass Gm-C filters. The set of filters have been designed and fabricated in a 0.25 μm CMOS process to meet all the specifications under expected process variations.

The AGC part of the analog baseband processor has three variable gain amplifier (VGA) stages. One of them is placed before and the rest after the channel-select filter. A
new gain-control algorithm for the OFDM baseband signal is proposed based on analysis of conventional AGC loops. The new AGC algorithm uses switched coarse gain-setting steps followed by an analog open-loop fine gain-setting step to set the final gain of the VGAs. The AGC circuit is implemented in a 0.18 µm CMOS process using newly designed circuits including linear VGAs, RMS detectors, and current-mode computation circuitry. Experimental results show that the new AGC circuit adjusts OFDM short training symbols to the desired level within settling-time requirements.
CHAPTER 1
INTRODUCTION

1.1 Motivation

Wireless technologies are progressing rapidly, not only for voice, but also for data communications. The growing mobile computing environment combined with the demand for network connectivity has made wireless local area network (WLAN) popular. Since the Institute of Electrical & Electronics Engineers (IEEE) ratified two WLAN standards, 802.11a and 802.11b, in 1999, many WLAN system architectures have been developed to implement them. The IEEE 802.11b standard specifies operation in the 2.4-GHz industrial-scientific-medical (ISM) band using direct-sequence spread-spectrum (DSSS) technology. On the other hand, the IEEE 802.11a standard specifies operation in the recently allocated 5-GHz unlicensed national information infrastructure (UNII) band and uses the orthogonal frequency division multiplexing (OFDM) scheme instead of DSSS. The IEEE 802.11b standard, which supports data rates of up to 11Mbps, was implemented before the IEEE 802.11a standard, which supports data rates of up to 54Mbps, because the latter has more complicated and strict transceiver design specifications than the former [Con01, Lee02].

In addition to the right performance requirement, implementation of the 5-GHz 802.11a RF transceiver with low cost and high power efficiency is another challenge. Along with several other silicon IC technologies, CMOS process technology can be a solution. It provides a low-cost advantage due to its compatibility with high levels of integration. Many CMOS processes also offer multiple metal layers, which enables the
use of integrated inductors and linear capacitors. However, characteristics of these passive devices can be poor, due to process and temperature sensitivities. These drawbacks can be resolved by automatic frequency and gain control (AFC and AGC) algorithms [Zar02].

A typical 5-GHz WLAN receiver with direct conversion consists of RF front end, analog and digital baseband blocks. In this type of architecture, most gain is in the analog baseband except for the gain of a low noise amplifier (LNA) and mixer in the RF front end. An analog baseband processor covers from the mixer’s output to the analog-to-digital (A/D) converter’s input, including baseband lowpass filters and AGC circuits. Therefore, the main function of an analog baseband processor can be described as channel-select filtering with sufficient gain. OFDM signals have a large peak-to-average power ratio (PAPR), which requires wide dynamic range in the receiver [Och01]. In order to deal with the wide dynamic range of the OFDM signal in the analog baseband processor, we need to devise an efficient gain control algorithm.

1.2 Research Goals

The first goal of this research is to design a baseband lowpass filter which meets the specifications of the IEEE 802.11a standard. The CMOS Gm-C elliptic filter can be a good candidate for its good on-chip integration properties. Also, by using a simple Gm tuning scheme, the filter can adjust the transfer function to compensate for process and temperature variations.

The second goal is to propose a gain-control algorithm to provide a constant level of signal to the digital baseband processor. In order to achieve this goal, the effect of PAPR characteristic of the OFDM data signal on the signal amplitude estimation should be simulated statistically, by which one can determine the best detector type for the
OFDM signal. Based on analysis of conventional AGC loops, a new gain-control technique can be obtained.

Finally, the proposed AGC algorithm is to be implemented in the circuit level design. This research completes an analog baseband processor for a CMOS WLAN receiver by making a whole signal chain with a filter and AGC circuits. To achieve experimental results, the AGC design is to be fabricated in TSMC 0.18µm CMOS technology.

1.3 Outline of the Dissertation

This Ph.D. dissertation consists of six chapters. An overview of the research is given in this current chapter (Chapter 1), including the motivation, research goals, and the scope of this work. Chapter 2 reviews some background knowledge on this research. Basic concepts and specifications of the IEEE 802.11a standard are described, and the overall system architecture and analog baseband signal chain blocks are presented. Fundamentals of AGC operation are also reviewed in that chapter.

In Chapter 3, a statistical simulation of OFDM amplitude estimation is presented. An OFDM signal generator (transmitter) is simulated, and signal detectors such as peak, average, RMS and pseudo-RMS detectors are compared based on 802.11a standard using Matlab/Simulink. The simulation results show that given random input OFDM-QAM signals, the RMS detector has the least error variance among detectors.

Chapter 4 describes the design of 7th order elliptic lowpass filters for the baseband processor for a 5-GHz WLAN receiver. The filter employs a technique to avoid floating capacitors which allows setting peak values of all internal node voltages identical, thus improving the maximum input signal level. The circuit’s transconductors are
implemented as sets of “unit gm” cells, by which process-variation effects are reduced. The Gm cells provide reasonable linearity and tunability using degeneration. A spreadsheet to deal with the parasitic capacitance simplifies the design process. Simulation results in a 0.25μm CMOS process verify that the circuit meets all the specifications under expected process variations.

Chapter 5 discusses the AGC part of the analog baseband processor. It has three stages of variable gain amplifiers (VGAs). One of them is placed in front of the lowpass filter to maximize the dynamic range of the signal. A new gain-control algorithm for the OFDM baseband signal is proposed based on analysis of conventional AGC loops. After the switched coarse gain-setting, a fine gain-setting scheme locks the final gain within the specification time. Circuit design for the proposed algorithm is implemented in a 0.18μm CMOS process.

A summary of research work discussed in the dissertation and suggestions for the future work are presented in Chapter 6.
2.1 IEEE 802.11a Standard

The 802.11a standard specifies operation in the 5-GHz unlicensed national information infrastructure (UNII) band with available signal bandwidth of 300 MHz. The allocated frequency band is split into two blocks (5.15 ~ 5.35 GHz and 5.725 ~ 5.825 GHz) with three different power-level working domains as illustrated in Figure 2-1. The bottom 100 MHz domain has a maximum power output restriction of 40 mW, while the next 100 MHz allows up to 200 mW. The top 100 MHz domain, intended for outdoor operation, allows power output up to 800 mW.

![Figure 2-1. Frequency band allocation in the IEEE 802.11a standard](image)
The 802.11a standard employs an encoding technology called coded orthogonal frequency division multiplexing (OFDM). OFDM subdivides a high-speed data carrier into several lower-speed subcarriers, which are then transmitted in parallel. There are four 20 MHz-wide carriers in each 100 MHz domain. Each 20 MHz-wide carrier is subdivided into 52 subchannels, each subchannel with 312.5 KHz bandwidth. 48 of these 52 subchannels are used for data, while the remaining 4 are used for error correction. By using this OFDM scheme with low data rate subchannels, the signal channel is less susceptible to multipath effects during propagation. However, OFDM signals have large peak-to-average power ratio (PAPR) which requires a large power backoff in the transmitter and a wide dynamic range in the receiver. For example, suppose each of the 52 subcarriers of the OFDM signal is a single-tone sine wave. Then the wave form of the composite OFDM signal in the time domain will have large peaks and valleys. In the worst case, if the peaks of all 52 sine waves coincide in time, the peak voltage will be 52 times larger than that of a single sine wave, which results in a peak-to-average ratio of 17 dB ($\approx 10\log(52)$). Although some signal clipping can be accepted with an insignificant performance degrade in practice, this PAPR characteristic of the OFDM signal can complicate transceiver design [Zar02].

The OFDM system uses binary / quadrature phase shift keying (BPSK/QPSK), 16-quadrature amplitude modulation (QAM) or 64-QAM for subcarrier modulation. When BPSK is used, each subchannel carrier encodes data of 125 Kbps, resulting in a 6 Mbps data rate. The data rate doubles to 12 Mbps, 250 Kbps per subchannel with QPSK. Using 16-QAM, the rate increases further to 24 Mbps. It is mandatory for 802.11a systems to provide these data rates. The standard also allows data-rate extension
beyond 24 Mbps. A data rate of up to 54 Mbps in a 20 MHz channel can be achieved by using 64-QAM.

The 802.11 wireless LAN data service is provided by sending and receiving packet frames denoted as PLCP (physical layer convergence procedure) Protocol Data Unit frames. The packet frame format includes PLCP preamble, SIGNAL (header of the frame) and DATA parts as shown in Figure 2-2. The PLCP preamble is composed of 12 symbols: 10 repetitions of a “short training sequence” (used for AGC convergence, diversity selection, timing acquisition, and coarse frequency acquisition in the receiver) and two repetitions of a “long training sequence” (used for channel estimation and fine frequency acquisition in the receiver). The SIGNAL part constitutes a single BPSK coded OFDM symbol which includes the RATE and LENGTH fields required for decoding the DATA part of the packet. The DATA part, which includes the service data units, may consist of multiple OFDM symbols. The design considerations for an analog baseband processor deal with short training symbols of the preamble in this OFDM packet frame format.

<table>
<thead>
<tr>
<th>BPSK coded OFDM</th>
<th>Coded OFDM</th>
</tr>
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<tbody>
<tr>
<td>PLCP Preamble 12 Symbols</td>
<td>SIGNAL One OFDM Symbol</td>
</tr>
<tr>
<td>10 short training symbols + 2 long training symbols</td>
<td>RATE and LENGTH for DATA</td>
</tr>
</tbody>
</table>

Figure 2-2. PLCP Protocol Data Unit frame format

2.2 System Specifications for WLAN Receiver

The receiver specifications for the 5 GHz WLAN system are described as receiver performance requirements in the 802.11a standard. Table 2-1 specifies the receiver
performance requirements with data rates of 6 Mbps through 54 Mbps. The minimum sensitivity is -82 dBm for 6 Mbps data rate and -65 dBm for 54 Mbps data rate. For the baseband signal channel at DC, the adjacent channel (at 20 MHz) rejection should be no less than 16 dB (6 Mbps data rate) or -1 dB (54 Mbps data rate). Similarly, alternate adjacent channel (at 40 MHz) rejection should be no less than 32 dB (6 Mbps data rate) or 15 dB (54 Mbps data rate). The relative constellation RMS error which is known as SIR (Signal-to-Interference Ratio) should not exceed -5 dB (6 Mbps data rate) or -25 dB (54 Mbps data rate). Figure 2-3 shows specifications of the minimum sensitivity signal channel with adjacent and alternate adjacent channels for 6 and 54 Mbps data rates.

Table 2-1. Receiver performance requirements

<table>
<thead>
<tr>
<th>Data rate (Mbps)</th>
<th>Minimum sensitivity (dBm)</th>
<th>Adjacent channel rejection (dB)</th>
<th>Alternate adjacent channel rejection (dB)</th>
<th>Relative constellation error (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>-82</td>
<td>16</td>
<td>32</td>
<td>-5</td>
</tr>
<tr>
<td>9</td>
<td>-81</td>
<td>15</td>
<td>31</td>
<td>-8</td>
</tr>
<tr>
<td>12</td>
<td>-79</td>
<td>13</td>
<td>29</td>
<td>-10</td>
</tr>
<tr>
<td>18</td>
<td>-77</td>
<td>11</td>
<td>27</td>
<td>-13</td>
</tr>
<tr>
<td>24</td>
<td>-74</td>
<td>8</td>
<td>24</td>
<td>-16</td>
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<tr>
<td>36</td>
<td>-70</td>
<td>4</td>
<td>20</td>
<td>-19</td>
</tr>
<tr>
<td>48</td>
<td>-66</td>
<td>0</td>
<td>16</td>
<td>-22</td>
</tr>
<tr>
<td>54</td>
<td>-65</td>
<td>-1</td>
<td>15</td>
<td>-25</td>
</tr>
</tbody>
</table>

From the specifications above, we can get the attenuation requirements for the analog baseband channel selection filter. With the minimum data rate, 6 Mbps, channel rejection should be 16/32 dB for adjacentalternate adjacent channels. Adding 6 dB for SIR and 5 dB for margin, total attenuation should be 27/43 dB for adjacentalternate adjacent channels. Channel rejection with 54 Mbps data rate should be -1/15 dB for adjacentalternate adjacent channels. This results in the total attenuation of 29/45 dB with 25 dB of SIR and 5 dB of margin. If we increase the margin to 10 dB, the filter
attenuation requirements would be 34 dB for the adjacent channel and 50 dB for the alternate adjacent channel.

![Graph showing sensitivity levels at different frequencies for 6 Mbps and 54 Mbps data rates.]

Figure 2-3. Specifications of the minimum sensitivity signal channel with adjacent and alternate adjacent channels for 6 and 54 Mbps data rates

### 2.3 Receiver Architecture and Analog Baseband Signal Chain

The two most common choices in receiver architecture are direct conversion and low-IF dual conversion (superheterodyne). Direct conversion is usually preferred in a fully integrated design because it has a simple architecture. However, it has drawbacks such as 1/f noise sensitivity and DC-offset problems. Dual conversion can reduce the disadvantages of direct conversion, but it requires extra complexity [Raz01].

In this work, we assume that direct conversion is used for the receiver architecture. As depicted in Figure 2-4, the receiver consists of a band-pass filter, low-noise amplifier (LNA), I/Q channel mixers and low-pass filters with automatic gain control (AGC) followed by analog-to-digital converters. The given blocks have fixed gains; -3 dB for band-pass filter, 20/0 dB (selectable) for LNA and 10 dB for mixers. As we know the receiver specifications, we can get the gain budget distribution for the AGC with given RF block gains.
Input signal levels to the filter/AGC blocks can be computed by adding the gains of the BPF, LNA and mixer to the sensitivity. The minimum input signal level for 6 Mb/s data rate is: 

$$-82 \text{ dBm} - 3 \text{ dB} + 20 \text{ dB} + 10 \text{ dB} = -55 \text{ dBm}.$$ 

For 54 Mb/s data rate, the minimum input signal level is: 

$$-65 \text{ dBm} - 3 \text{ dB} + 20 \text{ dB} + 10 \text{ dB} = -38 \text{ dBm}.$$ 

The maximum input signal level of the adjacent and alternate adjacent channels at the AGC inputs are -39 dBm and -23 dBm, respectively.

We assume that the input resistance of the A/D converter is 1 KΩ and that its input signal level should be 1 V<sub>pp</sub> in single ended mode. In differential mode, 1 V<sub>pp</sub> equals to 0.5 V<sub>pp</sub> (0.25 V<sub>p</sub>) and to 0.178 V<sub>rms</sub> for a sine wave. This corresponds to 0.032 mW in 1 kΩ of input resistance, or -15 dBm. For OFDM data signals, however, the ratio between the peak and the RMS voltage varies due to the randomness of data and the effects of the channel. For OFDM short training symbols, which have fixed amplitudes specified in the 802.11a standard, the RMS voltage of a short training symbol with 0.25 V<sub>p</sub> is 0.105 V<sub>rms</sub>. Its power level is computed as 

$$0.105^2 / 1K = 0.011 \text{ mW},$$ 

or -20 dBm. In practice, the effects of a random channel can change this relationship.
The proposed baseband signal chain is composed of three variable gain amplifier (VGA) stages with two AGC blocks plus a 7th order Gm-C filter implemented as shown in Figure 2-5. It also includes DC-offset canceling blocks such as capacitive coupling, high-pass filter and/or feedback loop to remove dc offsets. One AGC block is placed before and one after the channel-selection filter. Since the signals before and after the channel-select filter are different, we applied separate AGC blocks to provide optimum dynamic range (DR) for the filter. The pre-filter AGC block with one selectable-gain VGA stage enables the desired channel to have the maximum gain in the presence of large adjacent channel signals by increasing the gain until the composite (desired channel plus adjacent channels) signal reaches the input saturation point of the filter. This pre-filter AGC provides an approximately constant-level composite signal to the channel-selection filter, thus reducing the input-signal dynamic-range requirement of the filter. The post-filter AGC with two VGA stages sets the gain so that the signal level of the

Figure 2-5. Baseband signal chain block diagram
selected channel gets to the desired output level. If we had used a single post-filter AGC, a low-noise filter with high DR and a high gain-range AGC would have been required in the worst case of low composite input signal. On the other hand, we would have needed an extra gain stage after the filter in the worst case of low desired signal level with high adjacent-channel signal level, if we had used a single pre-filter AGC.

To ensure the operation of the baseband signal chain for all data rates with worst-case levels of adjacent channels, efficient gain distribution is needed for the two AGC blocks as illustrated in Figures 2-6 and 2-7. Given -16 dB as the input saturation point of the filter, the gain of the pre-filter AGC should be 7 dB or more. The gain of the post-filter AGC should be -4 dB (-16 to -20 dBm) for the maximum signal and 28 dB (-48 to -20 dBm) for the minimum signal, which specifies the gain range of each VGA to -2 to 14 dB. The selectable gain of the pre-filter AGC can be set to 7 or 14 dB when all three VGA stages are identical. Adding 4 dB of gain margin, the VGA should be designed to have a gain range of -4 to 16 dB.

2.4 AGC Fundamentals

In this section, a conventional closed-loop AGC is analyzed mathematically based on the AGC loop analysis given by [Kho98] to elucidate AGC function. For the operation of the AGC loop, we assume that the AGC circuit only operates on signal amplitude; hence the AGC input/output signals are represented only in terms of their amplitudes. Another assumption is that the peak detector extracts the peak amplitude of $V_{\text{out}}(t)$ linearly and instantly (much faster than the basic operation of the loop) so that peak voltage equals to the amplitude of $V_{\text{out}}(t)$. This assumption enables omission of the peak detector function model in the analysis.
Figure 2-6. Receiver gain distribution plots for 6 Mbps data rate. (a) Minimum signal 1. (b) Minimum signal 2.

Figure 2-8 (a) shows a common structure of an AGC loop. The AGC loop consists of a VGA, a peak detector, a comparator, and a loop filter. The VGA amplifies the input signal $V_{in}$ by the gain control signal $V_c$. The output of the VGA is extracted by the peak detector and then is compared with the reference voltage $V_{ref}$. The error signal is filtered and fed back to the VGA to adjust the gain. The AGC loop is in general a nonlinear
system because the VGA operates like a mixer: \( V_{\text{out}} = V_{\text{in}} \times f(V_c) \). \hspace{1cm} (2-1)

Thus, we need to linearize the loop to simplify a mathematical analysis of the AGC loop. Figure 2-8 (b) shows a linearized structure of the AGC loop. By taking the natural logarithm of Equation 2-1, we can change the multiplier expression of the VGA to an adder expression: \( \ln(V_{\text{out}}) = \ln(V_{\text{in}} \times f(V_c)) = \ln(V_{\text{in}}) + \ln(f(V_c)) \). \hspace{1cm} (2-2)
To linearize the feedback loop, two function blocks (the exponential block at the VGA output and the logarithm block at the control voltage input of the VGA) must be canceled. Hence, two shaded blocks (the logarithm block at the VGA output and the exponential block at the control voltage input of the VGA) are added in Figure 2-8 (b). We can write the control function to VGA as \( f(V_c) = \exp(k \cdot V_c) \), (2-3) and rewrite Equation 2-2 as

\[
\ln(V_{out}) = \ln(V_{in}) + \ln(\exp(k \cdot V_c)) = \ln(V_{in}) + k \cdot V_c. \tag{2-4}
\]

Let \( \ln(V_{in}) = x \) and \( \ln(V_{out}) = y \), then the Equation 2-4 is \( y = x + k \cdot V_c \). (2-5)
The control function from the loop filter is expressed as

\[ V_c = \frac{g_m}{C} \int_0^t (V_{ref} - \ln(V_{out})) d\tau, \]

and \( \ln(V_{out}) = y \), so

\[ V_c = \frac{g_m}{C} \int_0^t (V_{ref} - y) d\tau. \]  

(2-6)

Take derivative respect to time on Equations 2-5 and 2-6:

\[ \frac{dy}{dt} = \frac{dx}{dt} + k \frac{dV_c}{dt}, \quad \frac{dV_c}{dt} = \frac{g_m}{C} (V_{ref} - y), \quad \therefore \frac{dy}{dt} = \frac{dx}{dt} + k \cdot \frac{g_m}{C} (V_{ref} - y). \]  

(2-7)

And take the Laplace transformation to Equation (2-7):

\[ sy = sx - k \cdot (gm/C) \cdot y, \quad (s + k \cdot gm/C) y = sx. \]

\[ \therefore \frac{y}{x} = H(s) = \frac{s}{s + k \cdot \frac{g_m}{C}} \]  

(2-8)

Equation 2-8 is an input-output transfer function of the linearized VGA with AGC loop.

The transfer function is a 1st order high-pass function and is stable since the pole is in the left half of the s-plane. This means that the gain control voltage of the feedback loop is input signal independent. AGC settling time is inverse proportional to the constant loop bandwidth \( f_c = k \cdot (gm/C) \).

In many AGC systems, the logarithm amplifier in shaded block in Figure 2-8 (b) can be omitted due to its complexity in realization. With this omission, the above condition can still be met under certain small-signal approximations. The assumption is that the AGC loop is operating with the condition that the output amplitude of VGA is near its fully converged state, that is, \( V_{out} \approx V_{ref} \). In this case, the control voltage function can be written as

\[ V_c = \frac{g_m}{C} \int_0^t (V_{ref} - V_{out}) d\tau, \quad \text{and since} \quad V_{out} = \exp(y), \]

\[ V_c = \frac{g_m}{C} \int_0^t (V_{ref} - e^y) d\tau. \]  

(2-9)

Take the derivative respect to time on Equations 2-5 and 2-9:
\[
\frac{dy}{dt} = \frac{dx}{dt} + k \frac{dV_c}{dt}, \quad \frac{dV_c}{dt} = \frac{g_m}{C} (V_{ref} - e^y), \quad \therefore \frac{dy}{dt} = \frac{dx}{dt} + k \cdot \frac{g_m}{C} (V_{ref} - e^y). \quad (2-10)
\]

Equation 2-10 is non-linear because of the exp(y) term. Let \( \ln(V_{ref}) = z \); then \( V_{ref} = \exp(z) \). Under small-signal approximation of \( V_{out} \approx V_{ref} \), we can get \( V_{out} - V_{ref} \approx 0 \), and \( \ln(V_{out}) - \ln(V_{ref}) = y - z \approx 0 \).

So, by Taylor series expansion, we can write

\[
e^y = e^{z+y-z} = e^{z} \cdot e^{y-z} \quad \therefore e^y \approx (1 + y - z) \text{ when } y-z << 1 \quad (2-11)
\]

Combine Equations (2-10) and (2-11):

\[
\frac{dy}{dt} = \frac{dx}{dt} + k \cdot \frac{g_m}{C} (V_{ref} - e^{z+y-z}) = \frac{dx}{dt} + k \cdot \frac{g_m}{C} (V_{ref} - V_{ref} (1 + y - z))
\]

\[
\therefore \frac{dy}{dt} = \frac{dx}{dt} + k \cdot \frac{g_m}{C} \cdot V_{ref} (\ln(V_{ref}) - y) \quad (2-12)
\]

Take the Laplace transformation to Equation 2-12:

\[
sy = sx - k \cdot (gm/C) \cdot V_{ref} \cdot y, \quad (s + k \cdot gm/C \cdot V_{ref}) y = sx.
\]

\[
\therefore \frac{y}{x} = H(s) = \frac{s}{s + k \cdot \frac{g_m}{C} \cdot V_{ref}} \quad (2-13)
\]

Equation 2-13 is the input-output transfer function of the linearized VGA with AGC loop under small-signal approximation. The transfer function is a 1st order high-pass function and is stable since the pole is in the left half of the s-plane. However, since we assumed \( V_{ref} \approx V_{out} = V_{in} \cdot f(V_c) \), this system is fundamentally nonlinear and is input signal-dependent. Loop bandwidth \( f_c = k \cdot (gm/C) \cdot V_{ref} \) is not constant if the difference between \( V_{out} \) and \( V_{ref} \) changes. Therefore, AGC settling time increases linearly with respect to the difference (input step size).
CHAPTER 3
OFDM SIGNAL AMPLITUDE ESTIMATION

3.1 OFDM Signal Characteristics

OFDM is a multi-carrier transmission technique, which divides the available spectrum into many carriers, each one being modulated by a low rate data stream. It is similar to Frequency Division Multiple Access (FDMA) in that the multiple user access is achieved by subdividing the available bandwidth into multiple channels, which are then allocated to users. However, OFDM uses the spectrum much more efficiently by spacing the channels much closer together. This is achieved by making all the carriers orthogonal to one another, preventing interference between the closely spaced carriers. A key drawback of OFDM is its high peak-to-average power ratio (PAPR), that is, its signal in the time domain has noise-like amplitude with a very large dynamic-range [Och01]. Figure 3-1 shows a typical analog OFDM signal in the time domain.

![Figure 3-1. A typical analog OFDM signal in the time domain](image)
OFDM has gained considerable attention with the rapid growth of digital communication in recent years. It has been adopted for digital wireless broadcast and network standards, including IEEE802.11a wireless LAN standard. The 802.11a standard describes the specifications for 5 GHz wireless LAN transceivers using OFDM [IEE99]. As discussed in Chapter 2, it offers support for a combination of other modulation and coding alternatives such as phase shift keying (PSK) or quadrature amplitude modulation (QAM) with convolution encoding to generate data rates of 6 through 54 Mbps.

A typical WLAN receiver consists of LNA, mixer, analog baseband processor and DSP blocks. An analog baseband processor includes AGC and channel-select filter blocks that deal with baseband signals in the time domain. The AGC sets the gain of variable gain amplifiers with respect to the detected output signal strength, which keeps the output signal level to the digital block constant. AGC systems use peak detectors to detect the strength of the output signal assume that its peak amplitude is constant if the signal strength does not change [Kho98]. However, peak detectors may not work properly with non-sinusoidal signals, that is, OFDM signal with high PAPR. Although RMS detectors have been widely used in non-sinusoidal signal amplitude estimation, no specific accuracy comparison among different types of detectors has been reported so far.

In this chapter, an OFDM signal generator for the baseband frequency range is designed based on the 802.11a specifications to estimate amplitude of analog OFDM signal in time domain using Matlab/Simulink. OFDM data symbols are simulated using randomly generated 64-QAM sequences. Various detectors such as peak, average, and RMS detectors are tested by using the statistical simulation method in order to find out
which has less variance for the OFDM amplitude estimate. Signal detectors will show averages of detected symbol amplitudes and statistical variances from multiple simulations.

### 3.2 OFDM Signal Generation

In an OFDM system, the data is split into a number of streams, which are independently modulated on parallel closely-spaced carrier frequencies. An OFDM symbol is a sum of subcarriers that are individually modulated by using binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), 16-QAM, or 64-QAM. Figure 3-2 shows the basic OFDM signal generator with the data symbols \( d(n) = a(n) + jb(n) \). The real and imaginary parts correspond to the in-phase and quadrature parts of the OFDM signal. They have to be multiplied by a cosine and sine of the desired frequency to produce the transmitted OFDM signal represented as [Cim85]:

\[
D(t) = \sum_{n=0}^{N-1} \{a(n)\cos(\omega_n t) + b(n)\sin(\omega_n t)\} . \tag{3-1}
\]

---

Figure 3-2. OFDM modulator
The IEEE 802.11a standard specifies the physical layer convergence procedure (PLCP) which provides a framing format suitable for data exchange and information management. The PLCP preamble consists of 10 repetitions of a ‘short training symbol’ (10 × 0.8µs), 2 guard intervals (2 × 0.8µs), and 2 repetitions of a ‘long training symbol’ (2 × 3.2µs). Seven out of ten short training symbols are used to allow time for signal detection, AGC convergence, and diversity selection. A short training symbol uses 12 subcarriers, which are modulated by the elements of the sequence S, given by:

\[ S_{26,26} = \sqrt{\frac{13}{6}} \times \{0,0,1+j,0,0,0,-1-j,0,0,0,1+j,0,0,0,-1-j,0,0,0,1+j,0,0,0,0,0,0,-1-j,0,0,0,-1-j,0,0,0,1+j,0,0,0,1+j,0,0,0,1+j,0,0,0,1+j,0,0,0,1+j,0,0\} \]

The multiplication factor of \( \sqrt{\frac{13}{6}} \) normalizes the average power of the resulting OFDM symbol, which utilizes 12 out of 52 subcarriers.

![Figure 3-3. Short training symbols: (a) I channel one symbol (0.8µs) and 7 symbols, and (b) Q channel one symbol (0.8µs) and 7 symbols](image)

A short training symbol can be generated by adding 6 signal sources for each I and Q channel using Simulink. The 12 subcarriers, ±4(1.25MHz), ±8(2.5MHz), ±12(3.75MHz), ±16 (5MHz), ±20(6.25MHz), and ±24(7.5MHz), are modulated by the
BPSK sequence as given above. The generated short training symbols (analog signal) for I and Q channels are illustrated in Figure 3-3.

The 64-QAM OFDM data symbols are generated as follows: First, binary input data is encoded, interleaved, and converted to QAM values. The 52 QAM values (48 data values and 4 pilot values) are then zero padded and modulated onto 64 subcarriers by applying the Inverse Fast Fourier Transform (IFFT). The output is converted to a serial symbol in the next stage. The end processing of the digital baseband block adds cyclic extension and window functions. Figure 3-4 shows the block diagram for data symbol generation in the discrete time domain.

The OFDM data symbol signal in the continuous-time domain can be generated for I and Q channels by replacing the IFFT block in Figure 3-4 with a new block that combines the QAM-modulated analog subcarriers as shown in Figure 3-5.

Figure 3-4. Data symbol generation in the discrete time domain

### 3.3 Analog OFDM Signal Amplitude Estimation with Statistical Simulation

The IEEE 802.11a standard reserves seven short training symbols for signal detection, AGC convergence and diversity selection. Since seven identical short training symbols are transmitted through an assumed unchanging channel, all of the available information about signal amplitude is available during each symbol duration. Thus, the short training symbol duration (0.8 µs) is the optimal amplitude-estimation time.
However, due to its high PAPR, detecting the OFDM signal within a time period as short as 0.8µs can lead to high variance in the estimate. Moreover, the received signal might have multi-path fading channel effects, which cause inaccurate amplitude estimation. Therefore, we can consider the variance of the estimated amplitude to compare the accuracy of estimation algorithms. We assume that the detector with lower variance is more accurate. In OFDM amplitude estimation, the accuracy of the estimate can be evaluated by statistical simulation; that is, the smaller the standard deviation is, the better the accuracy of the detector is.

Figure 3-5. Data symbol generation in continuous time domain

In order to compare the variances of the algorithms, we simulate the signal strength estimation using randomly generated data symbols. 64-QAM random data signals are generated and modulated with subcarriers to make OFDM data symbols. Three typical detectors such as peak (PK), average (AVR) and RMS (RMS) detectors are considered for the accuracy analysis. Three pseudo-RMS (PRMS$^{1.5}$, PRMS$^3$ and PRMS$^4$) detectors
are added to find out if they show variances significantly different from that of the exact RMS detector. Six detectors are implemented as follows:

\[
P_{K} = \max(S)_{T} \quad \quad \quad A_{VR} = \frac{1}{T} \int_{T} |S| dt
\]

\[
R_{MS} = \sqrt{\frac{1}{T} \int_{T} S^{2} dt} \quad \quad \quad P_{RMS}^{1.5} = \frac{1}{T} \frac{1}{1.5} \int_{T} |S|^{1.5} dt
\]

\[
P_{RMS}^{3} = \sqrt[3]{\frac{1}{T} \int_{T} S^{3} dt} \quad \quad \quad \quad P_{RMS}^{4} = \frac{1}{T} \int_{T} |S|^{4} dt
\]

where \( S \) is the amplitude of the OFDM signal and \( T (=0.8\mu s) \) is the estimation time.

Table 3-1. Statistical simulation result for 5000 symbols (Max Peak = 0.607)

<table>
<thead>
<tr>
<th>Detector</th>
<th>PK</th>
<th>AVR</th>
<th>PRMS(^{1.5})</th>
<th>RMS</th>
<th>PRMS(^{3})</th>
<th>PRMS(^{4})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arithmetic mean of 5000 results</td>
<td>0.318</td>
<td>0.118</td>
<td>0.129</td>
<td>0.140</td>
<td>0.160</td>
<td>0.176</td>
</tr>
</tbody>
</table>

A total of 5000 random data symbols are simulated for statistical purposes. The arithmetic means of the 5000 simulated outputs for each detector are shown in Table 3-1. Back-off represents the ratio of the maximum peak value to the arithmetic mean value of each detector. The simulation results show that the back-off value for the peak detector is the smallest and that of the average detector is the largest, as expected. Back-off values for RMS and pseudo-RMS detectors decrease slowly from the average detector to the high-order estimation.

Data distribution plots and standard deviation for each detector are shown in Figures 3-6 and 3-7, respectively. The standard deviation of the peak detector is almost twice those of the others, which means that it is not good for estimating OFDM signal strength. The RMS detector has the least standard deviation of all, but the differences between RMS detector and pseudo-RMS detectors are small. Standard deviations of pseudo-RMS detectors \((P_{RMS}^{1.5} \text{ and } P_{RMS}^{3})\) are only 4 to 6 % higher than that of the
true RMS detector (RMS). The simulation results indicate that the RMS detector is the best one for OFDM amplitude estimation. However, a simple pseudo-RMS detector could also be used, because there is no big difference in standard deviation values between an RMS and pseudo-RMS detectors.

Figure 3-6. Data distribution plots for 6 detectors

Figure 3-7. Standard deviation plot for 6 detectors
3.4 Accuracy Boundary for Received OFDM Short Training Symbols

In practice, OFDM symbols are transmitted through a radio link that can be modeled as randomly scrambling the phases and possibly changing the relative amplitudes of the signal [Cho01]. When such a signal is received, the amplitude of the estimated signal can be different from the transmitted one even if all transceiver blocks are assumed ideal. By taking this multipath channel-effect into account, we can estimate the error variance of the received OFDM signal. The RMS detector in the analog baseband processor is used for AGC, which must be performed within the first 7 short training symbol period. The accuracy of AGC is bounded by the error variance in the RMS value of the received short training symbols. So we need to estimate the accuracy boundary for the short training symbols to consider gain margin of the AGC.

Figure 3-8 shows how the OFDM short training symbol generation and channel effect blocks were simulated in the discrete time domain. The short training symbols are generated by using the sequence given in Section 3.2 in the OFDM data symbol generation blocks. Multipath is implemented using Simulink library blocks. The Multipath Rayleigh Fading Channel block multiplies the input signal with samples of a Rayleigh distributed complex random process, while the additive white Gaussian noise (AWGN) block adds noise.

From 100 simulations for short training symbol with channel effects, the average of the estimated RMS amplitudes is 0.266, and its standard deviation is 0.1. These values translate to the accuracy boundary of 5.5dB. This margin should be considered when designing the AGC for an analog baseband processor in 802.11a WLAN receiver.
Figure 3-8. OFDM short training symbol generation with channel effect
CHAPTER 4
SEVENTH ORDER ELLIPTIC LOW-PASS GM-C FILTER

4.1 Introduction

Channel-select filters for the analog baseband processor in a WLAN receiver may be either off-chip passive filters or on-chip active filters. On-chip active filters are preferred for high integration and low cost, in spite of drawbacks such as limited receiver dynamic range, increased power consumption and chip area. Gm-C filters are well suited to high frequency applications as integrated continuous-time active filters. In the Gm-C filter, parasitic capacitances of Gm cells can be merged into the grounded capacitors, thus minimizing their side effects [Kar92].

The channel-select filter must pass only the desired channel to the analog-to-digital (A/D) converter, suppressing adjacent and all other channels. Specifications are given to realize the filter. Elliptic filters are used to meet the given specifications and implemented in a 0.25\(\mu\)m CMOS technology. This chapter describes the design of a CMOS fully differential 7th-order low-pass Gm-C filter for the baseband processor in 5 GHz WLAN receiver. The filter is implemented by cascading 3rd and 4th order elliptic filters.

4.1.1 Specifications

Filter specifications were developed through discussions with the Intersil® wireless group to be consistent with IEEE 802.11a standard for a 5-GHz WLAN transceiver. The specifications of an active filter in a WLAN receiver usually include the following issues [Beh00].
• Frequency response: pass-band ripple, stop-band attenuation, selectivity and group delay
• Input/output signal dynamic range, noise, linearity
• Power consumption or supply voltage with current drain
• Chip area and/or complexity

The structure of the receiver uses I and Q channels for the baseband processing. The cutoff frequency of the low-pass filter can be set to half of the bandwidth. The occupied channel bandwidth is 16.6 MHz within the allocated 20 MHz bandwidth and there is a 3.4 MHz spacing between channels. Thus we can set the pass-band and stop-band edge frequencies to 8.3 MHz and 11.7 MHz, respectively. Other specifications are minimum stop-band attenuation against adjacent channel and alternative adjacent channel, given as \(-34 \text{ dB} @ 20 \text{ MHz}\) and \(-49 \text{ dB} @ 40 \text{ MHz}\), respectively. Figure 4-1 shows the channel magnitude attenuation requirements for the filter. Pass-band ripple should be less than 1dB. Settling time of the system, including AGC settling, should be within 5.6 \(\mu\)s (7 repetitions of the short training symbol), which requires fast settling time of the filter. In addition, less group delay spread would ease the signal processing of the OFDM signals.

![Figure 4-1. Channel attenuation requirements for the baseband low-pass filter](image-url)
4.1.2 Filter Topology

In the light of the required stop-band attenuation and narrow transition-band, the specifications demand a relatively high-order filter. Elliptic filters have high selectivity (steep magnitude response), but require high-Q poles that tend to cause long settling times, large group delay spread, and high sensitivity to element errors. Chebyshev II (Inverse Chebyshev) filters have less group delay variation, but need higher order (9\textsuperscript{th} order) compared to elliptic type (6\textsuperscript{th} order). Other filter types such as Bessel and Butterworth filters would require very high filter orders to meet the selectivity requirements.

Simulations indicated that a cascade of 3\textsuperscript{rd} and 4\textsuperscript{th} order elliptic lowpass sections provided superior trade-offs among delay, settling time and complexity. We can reduce the group delay variation of a high-order elliptic filter by cascading lower-order ones. 3\textsuperscript{rd}- and 4\textsuperscript{th}-order elliptic lowpass filters have 73 - 29 = 44 ns and 127 - 40 = 87 ns of maximum group delay variation in the pass-band, respectively [Men97]. Group delay variation of the cascaded filter is 44 + 87 = 131 ns, whereas that of the required 6\textsuperscript{th} order elliptic filter is 403 - 79 = 324 ns. The cascaded filter shows even better result in group delay than the 9\textsuperscript{th} order Chebyshev II filter which has 142ns of the maximum group delay variation in the pass-band. Graphs of the magnitude and group delay responses for each filter type are shown in Figure 4-2.

The Gm-C filters were designed based on LC passive filter prototypes, with element values provided by a filter data book [Hue80] and by software (Filter solutions v.8.0). Figure 4-3 illustrates prototype circuits of cascaded 3\textsuperscript{rd} and 4\textsuperscript{th} order low-pass elliptic LC passive filters which meet the given specifications. Note that the input and output impedances are assumed to be 5 kΩ.
Figure 4-2. Frequency response (magnitude and group delay) for (a) 6\textsuperscript{th} order elliptic, (b) 9\textsuperscript{th} order Chebyshev II, (c) 3\textsuperscript{rd} order elliptic, and (d) 4\textsuperscript{th} order elliptic filters

Figure 4-3. LC prototype filters for (a) 3\textsuperscript{rd} order and (b) 4\textsuperscript{th} order elliptic low-pass filters
4.2 Filter Design I

4.2.1 Gm-C Filter with Amplitude Scaling

The elliptic Gm-C filters are built from the LC prototype by replacing both resistors and inductors with transconductors elements. The input/output resistance of 5 kΩ sets the transconductance gm to 200 µA/V. The floating inductors are implemented using gyrator-C circuits with $C = L \cdot gm_1 \cdot gm_2$. In order to minimize mismatch, transconductors are composed of “unit gm (gmu)” cells. This also makes it convenient for layout. All the transconductors in the filter are to be an integer multiple of gmu. Transconductor of 200 µA/V is represented by 4gmu with unit gm of 50 µA/V. The transconductors connected to the input will be doubled to remove the 6 dB loss from implementation of equally terminated LC prototype. Figure 4-4 shows the implemented 3rd order Gm-C filter.

![3rd order Gm-C filter](image)

Figure 4-4. 3rd order Gm-C filter

However, in this filter, the amplitude of the signal at internal nodes may be higher than the filter input. These peak voltages can drive internal transconductors into saturation, resulting in distortion of the output signal. This problem can be solved by applying amplitude scaling to the filter. That is, all node impedances are scaled so as to make their peak amplitudes remain near the input signal’s level without changing the
transfer function of the filter. The 3rd order Gm-C filter has 3 nodes (two internal nodes and one output node). The second node n2 peaks at ~2.25 V in SPICE simulation, which is over twice the input voltage (1 V). This peak voltage can be reduced by half without changing the voltage at any other node of the filter. We can achieve this by halving the currents flowing into the capacitor’s node (4gmu → 2gmu) and doubling the currents emitting from the capacitor’s node (4gmu → 8gmu), simultaneously. The scaled internal node voltage plot and resulting Gm-C filter are given in Figures 4-5 and 4-6, respectively.

Figure 4-5. Internal node voltage plot of the 3rd order Gm-C filter: (a) before scaling and (b) after scaling

Figure 4-6. 3rd order Gm-C filter after voltage scaling for internal nodes
4.2.2 Gm Cell Circuit Design

The basic building block of the Gm-C filter is the integrator, which consists of a transconductor (Gm cell) and a capacitor. The characteristics of the filter such as frequency response, linearity, DC gain and tuning range depend on the Gm circuit. Real Gm circuits have a finite output impedance that modifies the transfer function of the integrator, introducing a low frequency pole $p_1$. This low frequency pole $p_1$ limits the dc gain and varies the phase of the integrator, which may introduce distortions in the transfer function of the Gm-C filters [San00]. One general approach to deal with the low frequency pole is to use a folded cascode (FC) output stage. The folded cascode structure increases the output impedance of the Gm circuit, which shifts the low frequency pole to a much lower frequency, reducing effects on the filter’s transfer function. Since the filter will operate in fully differential mode, we need to add common-mode feedback (CMFB) to the folded cascade output stage to stabilize the common-mode output voltage. This circuit senses any change of the common mode output voltage and pushes it back to the reference point by controlling the bias current of the output stage through negative feedback. So the transconductor has two elements: a Gm unit and a FC with CMFB unit.

The schematics of the Gm and FC with CMFB circuits are shown in Figure 4-7. The Gm cell has a p-channel differential pair as input stage. This can move the parasitic pole $p_2$ to a higher frequency with smaller transistor dimensions in the output stage compared to the n-channel input stage case. That is because the parasitic pole $p_2$ is mostly determined by the parasitic capacitance of an n-channel transistor in the FC stage.
The Gm cell uses source degeneration MOS resistors to improve linearity. One more voltage-controlled degeneration transistor (M₅) is added for tuning in parallel with the degeneration pair (M₃,₄) of the well-known four-transistor input stage. In the degeneration scheme, the linearity is increased by reducing the transconductance of the differential pair (gᵅᵣ/2). The transconductance of the linearized Gm cell can be found
with small signal analysis. $V_x \approx V_y$ for small input signals, which makes the degeneration transistors $M_{3,4}$ and $M_5$ operate in the triode region. The degeneration resistance is defined as $R = R_1 \parallel R_2 \parallel R_3$, by which we get the following equation for AC current $i$.

$$V_x - V_y = R \cdot i \quad (4-1)$$

We can also write

$$g_{m1} \cdot (V_{inp} - V_x) = i \quad (4-2)$$

and

$$g_{m2} \cdot (V_{inn} - V_y) = -i \quad (4-3)$$

for the input transistors $M_1$ and $M_2$, respectively, where $g_{m1} = g_{m2}$ and $V_{inp} - V_{inn} = V_{in}$.

From Equations 4-1 through 4-3 we get:

$$g_{m1} \cdot (V_{in} - R \cdot i) = 2 \cdot i \quad (4-4)$$

$$i = \frac{g_{m1}}{g_{m1} \cdot R + 2} \cdot V_{in} \quad (4-5)$$

$$\therefore G_m = \frac{g_{m1}}{g_{m1} \cdot R + 2} = \frac{\frac{g_{m1}}{2} \cdot \frac{1}{R}}{\frac{g_{m1}}{2} + \frac{1}{R}} = \frac{g_{m1}}{2} \| g_{mR} \quad (4-6)$$

Equation 4-6 shows that the transconductance of the proposed Gm cell is the parallel sum of the transconductances of the differential input stage and the degeneration transistors.

The unit Gm cell is designed and simulated to have 50 $\mu$A/V of transconductance through 1 V$_{pp}$ input signal range with 3 V supply voltage. Figure 4-8 illustrates the linear range of the DC transfer characteristics and transconductance.
4.2.3 Dealing with Parasitic Capacitance

The 3rd order filter in Figure 4-5 is redrawn in Figure 4-9 to show the fully differential structure with Gm cells, FC units, and capacitors. In reality, active blocks such as these Gm cells and FC units have parasitic capacitances at their input/output ports. Hence, we need to compute all of the parasitic capacitances of the active blocks connected to each main capacitor nodes, and modify the main capacitor value so that the total capacitance is the desired value. Also, to minimize process and temperature variations all nodes should have the same ratio of parasitic capacitance to main capacitance. An independent block composed of a FC output stage combined with CMFB is placed on capacitor node and used in common for all connected Gm cells. This is much simpler than including these functions in every Gm cell. The CMFB circuit in Figure 4-7 uses two matched differential pairs for good linearity, and all nodes see low impedances to minimize high-frequency phase errors. The inputs remain linear for large
differential signals up to near 1 Vpp, which is consistent with the maximum input signal swing of the transconductors.

In Figure 4-9, we can compute the number of FC units and Gm cells connected to each node. We keep track of the parasitic capacitances at each node for the output of each FC unit and the input of each Gm cell. The parasitic capacitances of each FC output port ($C_{out, FC}$) and Gm input port ($C_{in, Gm}$) are estimated from simulations [Kar92]. The parasitic capacitance at each node is calculated by the equation $C_p = (\text{number of FC}) \cdot C_{out, FC} + (\text{number of Gm}) \cdot C_{in, Gm}$. Let $C_t$ be the total capacitance of each node. For each node, we set the ratio between ‘main’ and ‘parasitic’ capacitances as equal as possible to minimize the effects of process-parameter variations. Let $x$ be the largest value of $C_p/C_t$ for all nodes ($x = 0.14$ at node 5 of 4th order filter). The main capacitance to be placed at each node is $C = C_t \cdot (1-x)$. The difference of the capacitance ($C_d = C_t - C_p - C$) should be realized by parasitic capacitance to provide process-parameter tracking. Therefore, we need to add dummy cells to all nodes with $C_d$ except one. Finally, we can find the number of dummy cells ($\text{dummy#}$) and the main capacitor value ($C_{cap}$) for each node. A spreadsheet was developed to automate these calculations, as an example is shown in Table 4-1.

![Figure 4-9. Fully differential 3rd order Gm-C filter](image)
Table 4-1. Spreadsheet to compute parasitic capacitance, number of dummy cells, and main capacitor value at each node

<table>
<thead>
<tr>
<th>Filter order</th>
<th>Node</th>
<th>C&lt;sub&gt;p&lt;/sub&gt;</th>
<th>C&lt;sub&gt;t&lt;/sub&gt;</th>
<th>C&lt;sub&gt;d&lt;/sub&gt;</th>
<th>dummy</th>
<th>dummy#</th>
<th>dum_diff</th>
<th>C&lt;sub&gt;cap&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 FC1</td>
<td>4 6</td>
<td>5.69E-13</td>
<td>4.45E-12</td>
<td>3.82E-12</td>
<td>6.24E-14</td>
<td>1.16E+00</td>
<td>1.00E+00</td>
<td>1.62E-01</td>
</tr>
<tr>
<td>3 FC2</td>
<td>1 16</td>
<td>3.33E-13</td>
<td>2.96E-12</td>
<td>2.54E-12</td>
<td>8.61E-14</td>
<td>1.60E+00</td>
<td>2.00E+00</td>
<td>-3.96E-01</td>
</tr>
<tr>
<td>3 FC3</td>
<td>3 6</td>
<td>4.47E-13</td>
<td>4.45E-12</td>
<td>3.82E-12</td>
<td>1.85E-13</td>
<td>3.45E+00</td>
<td>3.00E+00</td>
<td>4.45E-01</td>
</tr>
<tr>
<td>4 FC1</td>
<td>4 12</td>
<td>6.48E-13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 FC2</td>
<td>2 8</td>
<td>3.50E-13</td>
<td>4.55E-12</td>
<td>3.90E-12</td>
<td>2.94E-13</td>
<td>5.48E+00</td>
<td>5.00E+00</td>
<td>4.81E-01</td>
</tr>
<tr>
<td>4 FC3</td>
<td>3 6</td>
<td>4.47E-13</td>
<td>4.84E-12</td>
<td>4.15E-12</td>
<td>2.40E-13</td>
<td>4.47E+00</td>
<td>4.00E+00</td>
<td>4.70E-01</td>
</tr>
<tr>
<td>4 FC4</td>
<td>1 16</td>
<td>3.33E-13</td>
<td>3.44E-12</td>
<td>2.96E-12</td>
<td>1.55E-13</td>
<td>2.90E+00</td>
<td>3.00E+00</td>
<td>-1.04E-01</td>
</tr>
<tr>
<td>4 FC5</td>
<td>3 6</td>
<td>4.47E-13</td>
<td>3.15E-12</td>
<td>2.70E-12</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>2.70E-12</td>
</tr>
</tbody>
</table>

4.3 Filter Design II

4.3.1 Avoiding Floating Capacitor

The filter design in the previous section has embedded floating capacitors, which restricts node-voltage scaling and thus limits the input dynamic range. Floating capacitors may also present a problem in the design due to their inaccuracy of the bottom-plate capacitance. Hence, in this section, we designed another version of the filter which avoids floating capacitors. This new filter design replaces floating capacitors with compatible circuit blocks and results in all scalable internal nodes. The improved dynamic range is obtained at the expense of some added complexity.

Figure 4-10 describes the floating capacitor avoidance technique. The 3<sup>rd</sup> order Gm-C filter in Figure 4-4 is repeated here as 4-10 (a), where the floating capacitor is connected between node V<sub>1</sub> and node V<sub>2</sub>. As shown in Figure 4-10 (b), the floating capacitor to the node V<sub>1</sub> can be replaced with a grounded capacitor C<sub>3</sub> and a current source of sC<sub>3</sub>V<sub>2</sub> which flows into the node, because its current is sC<sub>3</sub>(V<sub>1</sub> - V<sub>2</sub>). The
current source of $sC_3V_2$ can be implemented in the following sequence; (i) duplicate all current sources at $V_2$, (ii) drive these currents into $R$, (iii) get the desired current through scaled $gm$. This is illustrated in Figure 4-10 (c). The voltage of the duplicated node $V_{x2}$ is $s(C_2+C_3)V_2/g_{y2}$. Therefore, if we set the scaled $gm$ as $g_{x1} = g_{y2}C_3/(C_2 + C_3)$, then we get the desired current $i = g_{x1}V_{x2} = sC_3V_2$. By applying the above technique to both nodes $V_1$ and $V_2$, the $3^{rd}$ order Gm-C filter which avoids the floating capacitor is implemented, as shown in Figure 4-11.

![Figure 4-10](image_url)

Figure 4-10. Avoiding floating capacitor: (a) Gm-C filter with floating capacitor, (b) substitution of floating capacitor at node $V_1$, (c) additional circuit for current source to node $V_1$

### 4.3.2 Parasitic Capacitance Compensation

All five internal nodes of the filter avoiding floating capacitors are scaled to maximize the input dynamic range of the filter. The internal node voltage plot after scaling is shown in Figure 4-12, where peak voltages of all five internal nodes are equal to 1 V, which is the peak voltage of the input signal.
Although the new filter presents scalability for better dynamic range, the extra circuits introduce two new nodes that are not connected to grounded capacitors. These floating nodes, $V_{x1}$ and $V_{x2}$, depicted in Figure 4-13 (a) can add extra poles or zeros to the transfer function due to their parasitic capacitances. In order to solve this problem,
we can add a ‘negative capacitor’ to the floating nodes of the filter. The negative capacitor circuit shown in Figure 4-13 (b) uses a cross-coupled differential structure to compensate AC current due to the parasitic capacitance by setting $C_c = C_p$. This circuit is applied to each floating node, by which the side effects from the parasitic capacitance are cancelled out [Wak90].

![Figure 4-13](image)

Figure 4-13. Internal node voltage plot of the 3rd order Gm-C filter avoiding floating capacitor

**4.4 Simulation Results**

**4.4.1 AC Response and Tuning Range**

The 3rd-4th order cascaded lowpass filter has been designed in two versions: namely, Filter 1 and Filter 2. Filter 1 includes floating capacitors whereas Filter 2 avoids the floating capacitors. The Cadence Spectre simulation results show that the characteristics of both filters meet the specifications. The following data in the format of value1/value2/value3, which represents the specifications, simulation results for Filter 1, and that of Filter 2, respectively. Pass-band ripple is less than 1/0.75/0.86 dB. Pass-band and stop-band corner frequency attenuations are -1/-0.96/-0.78 dB and -28/-32/-40 dB,
respectively. Stop-band attenuations for adjacent (at 20 MHz) and alternate adjacent (at 40 MHz) channels are -34/-47/-44 dB and -49/-58/-54 dB, respectively.

Worst case simulations with temperature, process and mismatch variations showed that the pass-band cutoff frequency varied from 7.7 MHz to 8.7 MHz for both filters while maintaining the shape of the AC response curve. Simulation results for AC response with tuning voltage of 0.1 ~ 1.9 V showed the pass-band cutoff frequency tuning range of 7.2 ~ 11.7 MHz for both filters. This tuning range covers the worst case variation range. Therefore, these filters can tolerate temperature, process and mismatch variations by using a simple automatic tuning circuitry. Figures 4-14 and 4-15 show the AC simulation results for Filter 2.

![AC Response](image)

Figure 4-14. AC response simulation result for Filter 2

### 4.4.2 Transient Response, Noise and Linearity

Figure 4-16 (a) gives the result of the transient simulation for pass-band signal at the edge frequency of 8.3 MHz. The output signal follows the input signal after initial settling period (~0.6 µs). The plot shows the linear output signal with approximately 90°
phase shift. Figure 4-16 (b) describes the attenuation for the stop-band signal at 12MHz, which suppresses out-of-band signal after settling.

Figure 4-15. AC response simulation result for Filter 2 with tuning

Figure 4-16. Transient response of the Filter 2 at (a) 8.3 MHz and (b) 12 MHz

Noise performance of RF receivers is commonly characterized using the Noise Figure. Noise Figure is commonly defined as [Raz94],

\[
NF = \log_{10} \left( \frac{SNR_{in}}{SNR_{out}} \right)
\]  

(4-7)
where $SNR_{in}$ and $SNR_{out}$ are the signal-to-noise ratios measured at the input and the output, respectively. For a general calculation of the noise figure, the NF is usually specified for a 1-Hz bandwidth at a given frequency. This is called as the “spot” noise figure to emphasize the very small bandwidth. This can be expressed as follows where $A = \alpha A_v$ and $V_{n, out}^2$ represents the total noise at the output.

$$NF = \log_{10} \left( 1 + \frac{(V_n + I_n R_S)^2}{4kTR_S} \right) = \log_{10} \left( \frac{V_{n, out}^2}{A^2} \frac{1}{4kTR_S} \right)$$

(4-8)

In this design, we set $A=1$ and $R_S=5k\Omega$, from which we get the noise figure from the simulation as $NF = V_{n, out}^2/(20.35n)^2$, as shown in Figure 4-17. The NF for the pass-band of the filter (156.25kHz ~ 8.3MHz) is less than 16.8dB.

![Figure 4-17. Noise in dB vs. frequency plot](image)

The linearity of a filter can be specified by either single-tone total harmonic distortion (THD) or two-tone input IP3. In this base-band filter design, the linearity of a filter is characterized by the signal voltage for 1 % THD. This figure of merit is used to quantify the non-linearity of the filter. Filter 1 shows 1 % THD for an input signal of
427 mVp while that of Filter 2 is 451 mVp in the nominal case (Figure 4-18). We can see that Filter 2 tolerates higher input signals than Filter 1, under the same linearity condition. This is the result of a superior amplitude scaling of Filter 2. The best/worst tuned case for the temperature, process and mismatch variation gives the maximum input signal range of 410 ~ 441 mVp and 424 ~ 503 mVp for Filter 1 and Filter 2, respectively.

Figure 4-18. Linearity of 1 % THD vs. input signal voltage for (a) Filter 1 and (b) Filter 2 in nominal case

The comparison between Filter 1 and Filter 2 is summarized in Table 4-2. Filter 1 is superior in power consumption and complexity, while Filter 2 shows better linearity. In conclusion, both 3rd-4th order cascaded elliptic lowpass Gm-C filters satisfy the specifications for the analog base-band filter in a 5 GHz WLAN receiver.
Table 4-2. Summary of characteristics of the two filters

<table>
<thead>
<tr>
<th>Filter structure</th>
<th>Filter 1</th>
<th>Filter 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gm cells</td>
<td>Unit Gm cells (50µA/V)</td>
<td>Unit Gm cells + 10 extras</td>
</tr>
<tr>
<td>number of MOS TRs</td>
<td>1364</td>
<td>2577</td>
</tr>
<tr>
<td>number of Caps</td>
<td>44</td>
<td>36</td>
</tr>
<tr>
<td>$I_{\text{total}}$</td>
<td>21 mA</td>
<td>38 mA</td>
</tr>
<tr>
<td>Max input Vpp</td>
<td>820/854/882 mV</td>
<td>848/902/1006 mV</td>
</tr>
<tr>
<td>In-band rms Noise</td>
<td>739.17 µV/√Hz</td>
<td>870.22 µV/√Hz</td>
</tr>
<tr>
<td>DR (nominal input)</td>
<td>61 dB</td>
<td>60 dB</td>
</tr>
</tbody>
</table>
CHAPTER 5
AUTOMATIC GAIN CONTROL

5.1 Introduction

Automatic gain control (AGC) is an essential function in a WLAN receiver because the power received through the wireless channel is unpredictable. The AGC circuitry provides a known output voltage magnitude from an input signal with variable strength. In the IEEE 802.11a WLAN system, data pass through the channel in packet frames consisting of preamble, header and data segments as discussed in Chapter 2. The receiver estimates corrections for the channel’s characteristics during reception of the preamble. These characteristics are assumed to stay constant throughout the transmission of the whole packet frame, typically up to 1 ms. The preamble consists of 10 repetitions of a predefined data stream called a short training symbol (10 × 0.8 µs) and two repetitions of a long training symbol (2 × 4 µs). In the proposed receiver system, the time for seven of the repeated short training symbols (5.6 µs) is allocated for signal detection, AGC convergence and diversity selection [IEE99]. While multipath can significantly alter the waveform, we assume that the received signal is essentially repeated during each short training symbol duration, and that its characteristics establish the amplitude and phase references for use during the entire packet frame.

Conventional closed-loop analog AGCs use feedback loops to adjust the gain of the variable-gain amplifiers (VGA) to set the desired output signal strength. In such AGC loops, as shown in Figure 5-1, input and output signals are typically represented by their peak amplitudes. This adequately represents signal levels for signals with constant PAPR
such as sinusoids. For proper operation of closed-loop AGCs, the time required to
determine peak amplitude must be much less than the time constant (settling time) of the
loop filter [Kho98]. When the input amplitude changes, the detected output amplitude is
compared to the desired amplitude and the difference error is fed back to adjust the gain
of the VGA to provide constant output amplitude. The negative feedback loop
continuously responds to input amplitude variation.

![Figure 5-1. Conventional AGC loop composed of VGA, Peak Detector and Loop Filter](image)

However, in the 802.11a application, due to the high PAPR of the OFDM signal,
input or output peak amplitude is not a reliable measure of signal strength. The closed-
loop AGC with peak detector will not converge as the peak amplitude of the OFDM
signal changes continuously. As discussed previously, the specifications require AGC
settling within the time for seven short training symbols. Since seven identical short
training symbols are transmitted through an assumed unchanged channel, all of the
available information about signal amplitude is available during each symbol duration.
So the short training symbol duration (0.8 µs) is the optimal signal-averaging time. In the
AGC loop, an average or RMS detector can replace the peak detector because signal
strength can be estimated as an average or RMS over the symbol duration. The closed-
loop AGC with average or RMS detector will converge with the time constant of the loop
filter much longer than the signal estimation time. The resulting AGC settling time is much longer than system specifications allow. These issues preclude the use of a conventional closed-loop AGC in this application. Based on these observations, a new open-loop AGC circuitry is proposed in the following section.

5.2 AGC Algorithm

Figure 5-2 illustrates the operation of the proposed AGC circuitry. The analog baseband circuits include three VGA stages plus a channel-selection filter. VGA stage VGA1, with gain selectable as 7 or 14 dB, precedes the filter. Two VGA stages, with combined gain variable continuously from about -8 dB to about 32 dB, follow the filter.

Figure 5-2. Architecture of the proposed AGC algorithm; (a) block diagram and (b) time line
Separate AGC loops are provided for the pre- and post-filter gain blocks, since they operate on different signals as discussed in Chapter 2.

The AGC algorithm operates in three phases: two switched coarse gain-setting phases, followed by an open-loop fine gain-setting phase. The coarse gain-setting steps ensure that all of the gain and filter stages operate linearly and that the gain is within ±5 dB of its optimal value. The fine step sets the gain for the entire packet to within ±1 dB of its optimal value. Before the reception of each packet, gains are initialized to 20 dB for the LNA, 7 dB for VGA1 and 6 dB for VGA2 and VGA3. During the first short training symbol time ($t_1$: 0 ~ 0.8 µs), RMS detectors RD1 and RD2, located before and after VGA1, estimate the signal amplitude. These values are sampled and held, and used by ‘Switched Gain Control 1’, a logic block that selects the gains of the LNA and VGA1 as shown in Figure 5-3. The LNA gain is set to 0 dB if the output of RD1 is greater than -23 dBm. If the output of RD2 is less than -23 dBm, the gain of VGA 1 is set to 14 dB. Otherwise, they keep their initial gains. After the signals settle down through the filter (the second short training symbol duration is allocated for filter settling), the post-filter AGC loop, ‘Switched Gain Control 2’ (Figure 5-4), selects the overall gain of the second and third VGAs (-3, 7, 17 or 27 dB) based on the signal amplitude detected during the third short training symbol ($t_3$: 1.6 to 2.4 µs) using RMS detectors RD3 and RD4 located before and after the cascade of VGAs. The overall gain of VGA 2 and 3 is set to -3 dB if the output of RD3 is greater than -30 dBm or to 7 / 17 dB if the output of RD4 is greater than -20 / -30 dBm. If the output of RD4 is less than -30 dBm, the overall gain of VGA 2 and 3 is set to 27 dB.
The final open-loop fine gain-setting phase, ‘AGC with One-Step Correction’, is applied to VGA2 and VGA3. The circuits include three main components: an RMS detector, an analog computation block and an inverse-gain block. As discussed in Chapter 3, an RMS detector should be used for the most accurate amplitude estimation of the OFDM signal. In this phase, the RMS detector connected to the output of the third VGA (RD5) detects signal strength during the fifth short training symbol duration.
The output voltage of the RMS detector is sampled and held, and the result, $V_{o1}$, is used in computing the final gain-control signal for VGA2 and VGA3. The analog computation circuitry computes the new control voltage ($V_{c2}$) from $V_{o1}$, the desired reference voltage ($V_{ref}$) and the initial control voltage ($V_{c1}$). The new control voltage is applied to VGA2 and VGA3 through the inverse-gain block [Kho98], which adjusts VGA gain to get the desired level of the output signal. Note that the subscripts 1 and 2 represent previous and new time steps respectively.

Figure 5-5. AGC with One-step Correction: the fine gain-setting step

Designing a VGA with reasonable input-to-output linearity is not too hard. However, accurately predicting the gain for a given gain-control input signal is quite difficult, especially in short-channel CMOS technologies. The inverse-gain block uses feedback to set the predicted switched gain accurately. Op-amp A in Figure 5-5 takes two positive DC voltage inputs, $V_C$ and $V_{C'}$, and uses feedback to find the AGC gain-control voltage $V_{cp}$ required to set the gain of VGA4 to $A_v = \frac{V_C}{V_{dc}}$. When Switch T is
connected to $V_{C1}$ (the switched-gain value set during coarse gain step 2), the gain of VGA4, as well as VGA2 and VGA3, are set to $A_{vl} = V_{C1} / V_{dc}$. \hfill (5-1)

That is, the switched gain of the second coarse gain-setting phase (-3, 7, 17 or 27 dB for 2-stage VGAs) is set by the ratio of the selected voltage $V_{C1}$ and the fixed voltage $V_{dc}$. Note that VGA4 in the inverse-gain block must be matched to VGA2 and VGA3 in the main signal path.

With the input voltage $V_{in}$ applied during the fifth short training symbol time, the detected RMS output voltage is sampled and held: $V_{o1} = A_{vl}^2 \cdot V_{in}$ \hfill (5-2)

The computation block computes the final control voltage:

$$V_{C2} = V_{C1} \cdot \sqrt{\frac{V_{ref}}{V_{o1}}} \quad (5-3)$$

Then, $V_{C2}$ is applied through Switch T to the inverse gain block, where the feedback loop of the op-amp A forces the gain of the VGA to $A_{v2} = V_{C2} / V_{dc}$. \hfill (5-4)

From Equations 5-3 and 5-4: $A_{v2} = V_{C2} / V_{dc} = V_{C1} / V_{dc} \cdot \sqrt{\frac{V_{ref}}{V_{o1}}}$, and from Equation 5-1: $A_{v2} = A_{vl} \cdot \sqrt{\frac{V_{ref}}{V_{o1}}}$ \hfill (5-5)

We can write the final output voltage as follows:

$$V_{o2} = A_{v2}^2 \cdot V_{in} = \left(A_{vl} \cdot \sqrt{\frac{V_{ref}}{V_{o1}}}\right)^2 \cdot V_{in} = A_{vl}^2 \cdot V_{in} / V_{o1} \cdot V_{ref} = V_{ref}$$

This equation shows that the final open-loop fine gain-setting AGC makes the output voltage $V_{o2}$ equal to the desired voltage $V_{ref}$ with one-step gain correction. Note that the final gain is held constant throughout the transmission of the packet frame. We also note that both I and Q channels can use one AGC loop for identical gain control, so the RMS detector can estimate the output amplitude from both I and Q channel signals.

In summary, the proposed AGC algorithm uses a three-step iterative open-loop gain control method (two coarse gain-settings using switches, followed by a final fine gain-
setting using an open-loop computation circuit). The algorithm converges within seven short-training-symbol times, and holds the final gain throughout the whole packet frame. This avoids the settling-time limits of a conventional closed-loop AGC.

5.3 Circuit Design

5.3.1 Variable Gain Amplifier

The transconductance of a MOS differential pair may be varied either with bias current, or by an adjustable degeneration resistor. A Gilbert multiplier-type amplifier is well suited to implement a VGA with large gain and low noise, but its linearity is limited. A differential pair degenerated by a MOSFET resistor can handle large signals given a low power supply resulting in good linearity, because the degeneration does not degrade the voltage headroom in a simple differential pair. However, this degenerated differential pair has limited gain range and poor noise figure [Tad98]. High linearity in a transconductance cell requires the transconductance (Gm) to be independent of input signal.

To cover the required gain range of -4 to 16 dB mentioned in Chapter 2, the VGA gain must be variable over a wide range. Also, it should have good linearity and low noise. To ensure that the VGA can fulfill these requirements, it is designed as a linear transconductance cell combined with cross-coupled differential pairs as in a Gilbert cell for gain control. A source follower with shunt feedback, the so-called flipped voltage follower (FVF), provides a low-impedance output node with a constant current through the input transistor [Car05]. A highly linear transconductance cell can be achieved by placing a fixed resistor RX between the low-impedance nodes of the differential FVF to provide a constant transconductance Gm = 2/RX. Feeding the output current of the transconductor to a fixed-resistor load RL would give a constant gain 2·RL/RX. The
differential pairs of Gilbert cell are used to steer the tuned portion of the transconductor’s output current to the load to make the gain adjustable. This type of VGA structure can provide -4 to 16 dB gain with good linearity.

Figure 5-6. Schematic of the proposed VGA

The proposed VGA consists of a linear transconductance cell (differential FVF with linear resistor), Gilbert cell-type differential pairs and load resistors, as shown in Figure 5-6. In the differential FVF transconductance cell, due to the feedback loop, input signal applied to transistors M1a, b does not affect the transconductance Gm = 2/RX, that is, currents through M1a, b and M3a, b are constant. Instead, the input signal changes voltages at the low impedance nodes X1, 2 and current IX flows through resistor RX sourcing from M3a, b: \[ I_X = (I_1 - I_2)/2 = Gm \cdot V_{in} \], where Gm = 2/RX. \[ (5-6) \]

The output currents (I1 and I2) of the transconductor are mirrored to the differential pairs with a 1:1 ratio: \[ I_1 = I_3 \text{ and } I_2 = I_4 \] \[ (5-7) \]
The cross-coupled structure of the Gilbert cell-type differential pairs yields
\[ I_3 = I_5 + I_6 \text{ and } I_4 = I_7 + I_8. \]
The control voltages (\( V_{C1} > V_{C2} > 0 \)) are provided by a
differential difference amplifier (DDA) and their differences adjust currents to the output
stage: \[ I_5 = I_3 \cdot f(V_{C2} - V_{C1}), \quad I_6 = I_3 \cdot f(V_{C1} - V_{C2}), \quad I_7 = I_4 \cdot f(V_{C1} - V_{C2}), \]
and \[ I_8 = I_4 \cdot f(V_{C2} - V_{C1}), \quad \] (5-8)
where \( 1 > f(V_{C1} - V_{C2}) > 1/2, \) and \( f(V_{C2} - V_{C1}) = 1 - f(V_{C1} - V_{C2}). \) (5-9)

The output stage consists of load resistors (\( R_{L1,2} \)) with common-mode feedback
(CMFB), level-shift resistors (\( R_{S1,2} \)) and current sources (\( M_{8a,b} \)). Since \( I_9 = I_{10}, \)
\[ I_5 + I_7 = I_9 - I_L, \text{ and } I_6 + I_8 = I_{10} - I_L, \] (5-10)
we can get the output current \( I_L = (I_6 - I_7 + I_8 - I_5)/2. \) (5-11)

Using Equations 5-8 and 5-9, we can rewrite the output current
\[ I_L = (I_3 - I_4) \cdot \{2 \cdot f(V_{C1} - V_{C2}) - 1\}/2, \] (5-12)
and from Equations 5-6 and 5-7, \( I_L = I_X \cdot \{2 \cdot f(V_{C1} - V_{C2}) - 1\}. \) (5-13)

The output voltage and voltage gain are
\[ V_{out} = I_L \cdot R_L = 2 \cdot V_{in} \cdot R_L/R_X \cdot \{2 \cdot f(V_{C1} - V_{C2}) - 1\}, \] (5-14)
\[ A_v = V_{out} / V_{in} = 2 \cdot R_L/R_X \cdot \{2 \cdot f(V_{C1} - V_{C2}) - 1\}. \] (5-15)

The maximum gain is achieved when the difference of the control voltages is maximum
\( (f(V_{C1} - V_{C2}) \approx 1), \) that is, \( A_{v,max} \approx 2 \cdot R_L/R_X. \) (5-16)

Since DC biasing for the input stage is provided by output stage of an identical VGA
stage, the output stage has level-shift resistors (\( R_{S1} \) and \( R_{S2} \)) to match the input and output
common-mode voltage ranges.

Voltages in the VGA are highly constrained. For negative input swing \( M_1 \) tends to
go triode and \( M_2 \) tends to go triode for positive input swing. To increase the usable input
range, voltage level-shifter ($I_Y \cdot R_Y$) is added in the shunt feedback path of the FVF, which brings the drain voltages of $M_1$ and $M_3$ closer to the negative supply rail. To optimize the voltage swing of the linear transconductance cell, the appropriate range of the voltage level-shifter is analyzed. If all transistor pairs are well matched and differential inputs are given as $V_{CM} \pm \Delta v_{in}$, we can write: $I_X = 2 \cdot \Delta v_{in}/R_X$, and $\pm \Delta v_{out} \approx \pm \Delta v_{in}$, where $\Delta v_{out}$ represents voltage variation at node $X_1$ (or $X_2$) due to $\Delta v_{in}$. For the worst case of applied maximum input $+\Delta v_{in}$ to the positive input port $V_{in+}$, transistors $M_{2a}$, $M_{1b}$ and $M_{3b}$ should be in the active region. Conditions on $M_{2a}$ and $M_{1b}$ set the lower limit of the level-shift voltage, while $M_{3b}$ condition set the upper limit. At the edge of the active region, $V_{GS1} = V_{T1} + V_{DSAT1}$, $V_{GS2} = V_{T0} + V_{DSAT2}$ and $V_{GS3} = V_{TN} + V_{DSAT3}$, where $V_{TN}$ is NMOS threshold voltage without body effect, and $V_{T0}$ and $V_{T1}$ are PMOS threshold voltages without and with body effect, respectively.

To keep $M_{2a}$ in the active region, the voltage at node $X_1$ must be less than $V_{DD} - V_{DSAT2}$, that is, $V_{X1} < V_{DD} - V_{DSAT2}$. \hspace{1cm} (5-17)

Let the level-shift voltage $\Delta V = I_Y \cdot R_Y$, then $V_{Y1} = V_{DD} - V_{GS2a} - \Delta V$ and $V_{X1} = V_{Y1} + V_{DSAT1} + \Delta v_{out}$. From Equation 5-17, we can get $\Delta V > V_{DSAT1} + \Delta v_{out} - V_{T0}$. \hspace{1cm} (5-18)

Simple calculation with maximum $\Delta v_{out}$ of 0.25 V and nominal values like $V_{DSAT1} = 0.2$ V and $V_{T0} = 0.5$ V shows -0.05 V as lower limit of $\Delta V$. This means that no voltage level-shifter is needed in this case to ensure $M_2$ stage in the active region.

To keep $M_{1b}$ in the active region, the voltage at node $Y_2$ must be less than $V_{G2} + V_{T1}$, that is, $V_{Y2} < V_{G2} + V_{T1}$. \hspace{1cm} (5-19)
Solving Equation 5-19 for $\Delta V$ with $V_{Y2} = V_{DD} - V_{GS2b} - \Delta V$ and $V_{G2} = V_{CM} - \Delta v_{int}$, we can get $\Delta V > V_{DD} - V_{DSAT2} - V_{T0} - V_{T1} - V_{CM} + \Delta v_{in}$ \hspace{1cm} (5-20)

With an input common-mode voltage $V_{CM}$ of about 0.5 V, 1.8 V supply voltage and other nominal values as above, this condition requires a voltage level-shift of more than 0.25 V.

The final condition is for NMOS transistor $M_{3b}$ to be in the active region:

$V_{Y2} > V_{DSAT3}$. \hspace{1cm} (5-21)

Solving this for $\Delta V$ results in $\Delta V < V_{DD} - V_{T0} - V_{DSAT2} - V_{DSAT3}$. \hspace{1cm} (5-22)

With similar rough calculation, this condition limits the voltage level-shift value to less than 0.9 V. Thus, by considering all three conditions, the voltage level-shift value must be selected in the range of $0.25 \, V < \Delta V < 0.9 \, V$.

Since the two conditions for the voltage level-shift value reference the positive supply voltage, we must allow for supply voltage variation of ±10% (1.6 ~ 2.0 V). Although we can select the level-shift value under the worst-case condition $(0.25 + 0.2 \, V < \Delta V < 0.9 - 0.2 \, V)$, to optimize signal swing for all $V_{DD}$ values, $\Delta V$ should be varied along with the variation of supply voltage. The level-shifters are implemented as linear resistors ($R_{Y1}$ and $R_{Y2}$) with current sources ($M_{4a, b}$). The current sources are controlled by a voltage $V_{Y}$ from a replica bias circuit (Figure 5-7). The replica bias circuit finds $V_{Y}$ to make $V_{D,M1}$ match $V_{D,M12}$, referenced to ground rather than supply voltage. In this design, the voltage level-shift value $\Delta V$ is set to 0.6 V and the voltages near the positive supply voltage nodes ($Y_3$ and $Y_4$) vary with $V_{DD}$ while the other nodes ($Y_1$ and $Y_2$) almost keep the same voltage. Inside the replica bias circuit, there are three feedback loops: two negative feedback loops ($V_{Y}-M_{4}-V_{A}-M_{2}-M_{1}-V_{B}-M_{11}-M_{13}$ and $V_{A}-M_{2}-M_{1}-V_{B}-R_{Y}$) and one positive feedback loop ($V_{Y}-M_{4}-V_{A}-R_{Y}-V_{B}-M_{11}-M_{13}$). Due to the
positive feedback loop, there can be multiple operating points [Fox99]. We need to make sure that only one operating point exists in the replica bias circuit design by using DC simulation for $V_A$ and $V_B$ as shown in Figure 5-8.

Figure 5-7. Schematic of the replica bias circuit for VGA

Figure 5-8. Simulation result for finding operating point in the replica bias circuit. The result verifies that the bias circuit (for $\Delta V = 0.6$ V) can operate only at the single operating point of $V_A = 1.26$ V and $V_B = 0.66$ V.

The VGA structure shows good linearity with large gain range. However, there are tradeoffs among gain range, linearity, noise, frequency bandwidth and current consumption in circuit design. Input transistors $M_{1a}$ and $M_{1b}$ have short channels to enhance $g_m$, but increase flicker noise, so PMOS devices were used for this circuitry.
Using long-channel transistors for NMOS output current sources ($M_{8a,b}$) also improves noise performance. Scaling up current along with channel widths reduces noise without changing circuit performance but current consumption had to be limited. Although long-channel devices reduce noise, they tend to degrade bandwidth due to large parasitic capacitances. Thus, short-channel transistors are used for Gilbert cell-type differential pairs and current mirrors to achieve adequate bandwidth. The current-mirror output of the VGA enables removing the PMOS tail current source, which saves voltage headroom. Constant current biasing is maintained by the balanced control voltages from the DDA.

### 5.3.2 Differential Difference Amplifier

A Differential Difference Amplifier (DDA) is used for the amplifier in the inverse gain-control loop because the loop operates in differential mode. A DDA has two differential input pairs and a differential output pair. When used in negative feedback connection with very large open loop gain, the DDA forces the two differential input pairs identical [Hun97]. To ensure a wide output control voltage range, the DDA is implemented as a folded cascade structure as shown in Figure 5-9. It contains two simple differential pairs ($M_1, M_2, M_3$ and $M_4$) which compare the difference of the two differential input signal voltages ($V_{C±}$ and $V_{dca}$). The differential cascode output stages, combined with a common-mode feedback (CMFB) circuit with level-shifters, provide differential output control voltages ($V_{cp1}$ and $V_{cp2}$) which change with the input difference. The CMFB circuit has a simple structure using source followers with level-shift resistors. Source followers $M_{15}$ and $M_{16}$ detect the output voltages of the DDA at their gates, and their corresponding source voltage difference generates current through $R_1$ and $R_2$. This current shifts the common-mode voltage level $V_{CM}$ which is fed back to the gates of the cascode PMOS transistors $M_7$ and $M_{11}$. The differential control voltages
are set by the feedback as the inverse gain loop forces the two inputs to be identical. Since the DDA works with DC control voltages, two compensation capacitors ($C_{C1} = C_{C2} = 10 \text{ pF}$), grounded in series with resistors, are added to the output nodes for stability.

![Figure 5-9. Schematic of the proposed Differential Difference Amplifier](image)

### 5.3.3 RMS Detector

The RMS detector estimates the RMS value of the output signal, integrated throughout one short training symbol duration. The RMS circuit is based on the approximately square-law characteristics of long-channel ($\sim 2 \text{ µm}$) MOSFETs in strong inversion [See87, Han98]. The dynamic range of this circuit is rather narrow, which is acceptable because the coarse gain-setting step ensures the signals are not far from their optimal value. The RMS output voltage is stored as the difference of the $V_{GS}$’s of a pair of diode-connected NMOS transistors ($V_{out^+} - V_{out^+}$). This signal is sampled and held on storage capacitors connected to the gates of NMOS transistors.

The RMS detector in Figure 5-10 uses NMOS transistors in strong inversion as the input squarer. The differential output voltages of the VGA with common-mode voltage
are fed to the gates of the NMOS transistors. Let the input signal $V_{\text{IN}} = V_{\text{CM}} \pm v_{\text{in}}$. The squarer transistor $M_1$ converts input voltage $v_{\text{in}}$ to output current $I_1$ as follows:

$$I_1 = \frac{1}{2} K_n \left( \frac{W}{L} \right)_n \left( V_{\text{GS1}} - V_T \right)^2 = \frac{1}{2} K_n \left( \frac{W}{L} \right)_n \left( V_{\text{CM}} + v_{\text{in}} - V_T \right)^2$$

$$\approx \frac{1}{2} K_n \left( \frac{W}{L} \right)_n v_{\text{in}}^2, \text{ with } V_{\text{CM}} \approx V_T$$  (5-23)

The resulting drain current of $M_1$ is almost proportional to the square of the input voltage if we set $V_{\text{CM}} \approx V_T$. Similarly, the drain current of $M_2$ is almost proportional to the square of the input voltage when the input signal is positive. Above the NMOS squarer are two cross-coupled NMOS differential pairs ($M_3$ ~ $M_6$). They operate like switches to rectify the currents in differential mode. For the differential pairs to work as switches, their gates must be triggered by large signals at the input signal frequency. Hence, the input signals $v_{\text{in}+}$ and $v_{\text{in}-}$ are boosted as $V_n$ and $V_p$ using amplifiers A and B, and supplied to the gates of the differential pairs. The currents $I_1$ and $I_2$ are rectified to $I_8$ when the input signal is positive and to $I_7$ otherwise. Figure 5-11 plots DC simulation results for V-to-I converted currents ($I_1$ and $I_2$) and rectified currents ($I_7$ and $I_8$), which shows that current $I_8$ is nearly proportional to the square of the input voltage.

Currents $I_7$ and $I_8$ are averaged and square-rooted to complete the RMS detection. The averaging of the currents is performed using a cascade of two first-order lowpass filters to meet the estimation time constraint of a short training symbol (0.8 µs). To provide an acceptable trade-off between smoothing and settling time, the on-chip capacitors are set to $C_1 = 4 \ \text{pF}$ and $C_2 = 10 \ \text{pF}$, where $C_2$ is bigger because it also used as a storage capacitor. The output current of the first PMOS lowpass filter is mirrored to the second NMOS lowpass filter. In this second filter, the NMOS implements a square-root function by converting the current to a voltage proportional to the square-root of the
current. The gate of the NMOS transistor and the storage capacitor are connected with a switch S (small geometry NMOS), which is opened after the symbol duration for the capacitor to hold the stored voltage.

Figure 5-10. Schematic of the proposed RMS detector

Figure 5-11. DC simulation results of the RMS detector with \( V_{CM} = 0.48 \) and \( v_{in} = -0.25 \sim 0.25 \) V: (a) currents \( I_{1,2} \) after squarer and (b) currents \( I_{3,4} \) after rectifier

5.3.4 Computation Block

The coarse gain-setting step provides us with a voltage \( V_{C1} \) that is applied to the inverse-gain block (along with \( V_{dc} \)) to set the VGA gains to a value within \( \pm 5 \) dB of their
optimal values. The resulting RMS value $V_{o1}$ of the output is measured during $t_5$ and is sampled and held. An analog computation block compares $V_{o1}$ to the desired value $V_{\text{ref}}$, and computes the new value of $V_{C2} = V_{C1} \cdot \sqrt{(V_{\text{ref}}/V_{o1})}$ as discussed in the previous section. The final control voltage $V_{C2}$ must be applied to the inverse-gain block to force the gain to its optimal value. For the optimal gain after the final control, we assume that the precision of $\pm 1$ dB is acceptable for the system (approximately $\pm 0.5$ dB is achieved by this computation block) as a design target. However, it is not easy to realize the analog computation block with multiplier, divider and square-root function blocks.

The analog computation block is implemented using translinear circuits based on weak-inversion FETs [Mul99], which reduces power dissipation and complexity of the circuit. This requires that the input and output signals be represented as small (~1 $\mu$A) single-ended currents. The single-ended current-mode operation of the computation block tends to be noisier than the differential mode. This reduces the accuracy of the computation, but the noise does not couple into the VGA signal path, since the gain is fixed during transmission of the data packet.

Figure 5-12 shows V-to-I and I-to-V converters with single-ended and/or differential mode terminals. The differential voltage to single-ended current converter in Figure 5-12 (a) is placed between RMS detector5 (RD5) and the computation block, which converts the output differential voltage of RD5 to $I_{o1}$ in the computation block. This V-to-I converter provides a linear output current which is attenuated to around 1 $\mu$A. The NMOS input transistors $M_1$ and $M_2$ have 5 times less transconductance compared to the output NMOS transistors of the RMS detector. PMOS transistors $M_5$ and $M_6$ are connected to the active loads ($M_3$ and $M_4$) of the input devices with shunt feedback, and
Figure 5-12. V-to-I and I-to-V converters in (a) differential V to single-ended I, (b) single-ended V-to-I, and (c) single-ended I to differential V modes work as source followers. The low impedance output nodes of the source followers are connected through a big linear resistor $R$ (30 kΩ). The difference of the two input voltages creates a voltage between sources of $M_5$ and $M_6$, and thus a small amount of current $I_R$ across the resistor $R$. $I_R$ flows through $M_6$, $M_8$ and $M_9$, and is mirrored to $I_{o1}$ via the 4:1 attenuation cascode current mirror ($M_8$, $M_9$, $M_{10}$ and $M_{11}$). This differential-voltage to single-ended current converter/attenuator provides around 1 µA of single-
ended current output to the computation block for a voltage input of about 250 mV from RMS detector.

The single-ended V-to-I converters in Figure 5-12 (b) convert single-ended voltages $V_{ref}$ and $V_{C1}$ to single-ended currents $I_{ref}$ and $I_{C1}$. A low gm NMOS transistor ($M_1$) with degeneration resistor $R_d$ (15 kΩ) converts input voltage $V_{in}$ to current $I_1$. This current is mirrored through a 4:1 attenuation cascode current mirror ($M_2$, $M_3$, $M_4$ and $M_5$) and is mirrored again through the 2:1 attenuation current mirror ($M_6$ and $M_7$) to achieve an output current $I_o$ of around 1 µA for the computation block.

Single-ended current to differential voltage converter in Figure 5-12 (c) converts the output current $I_{C2}$ of the computation block to the input differential voltage $V_{C2}$ of the inverse gain control block. This I-to-V converter amplifies its input current using a 1:4 cascode current mirror ($M_1$, $M_2$, $M_3$ and $M_4$), and the amplified output current $I_o$ creates two equal voltage drops in series-connected resistors $R_1$ and $R_2$. Differential output voltages are supplied at the top of $R_1$ and at the bottom of $R_2$. The gate of the $M_5$ connects to the node between $R_1$ and $R_2$ to set the common-mode voltage. $M_6$ delivers a common-mode current $I_{CM}$ to the drain of $M_5$, which provides a common-mode voltage to the gate of $M_5$ even when there is no input current applied.

Single-ended voltages $V_{C1}$ from the switched gain control block and $V_{dc}$ are converted to differential input voltages of the inverse gain control block through a cascade of a single-ended V-to-I converter and a single-ended current to differential voltage converter to minimize mismatch with the other differential control voltage $V_{C2}$ converted from the current mode computation block.
Figure 5-13. Schematic of the proposed analog computation block. The arrows indicate the \( V_{GS} \)'s that form the translinear loop.

The schematic of the proposed analog computation block is shown in Figure 5-13. Applying the translinear characteristics in weak inversion, we get the desired computation as written in the following equations.

\[
- V_{GS_{C1}} - V_{GS_{C1}} + V_{GS_{o1}} - V_{GS_{ref}} + V_{GS_{C2}} + V_{GS_{C2}} = 0 \quad (5-24)
\]

\[
- \ln I_{C1} - \ln I_{C1} + \ln I_{o1} - \ln I_{ref} + \ln I_{C2} + \ln I_{C2} = 0 \quad (5-25)
\]

\[
\ln I_{C2}^2 - \ln I_{C1}^2 = \ln I_{ref} - \ln I_{o1} \quad (5-26)
\]

\[
\ln \left( \frac{I_{C2}}{I_{C1}} \right)^2 = \ln \left( \frac{I_{ref}}{I_{o1}} \right) \quad (5-27)
\]

\[
\therefore I_{C2} = I_{C1} \sqrt{\frac{I_{ref}}{I_{o1}}} \quad (5-28)
\]

This circuit provides an output current \( I_{C2} \) with expected computation when the input currents \( I_{C1}, I_{o1} \) and \( I_{ref} \) are applied.

To guarantee translinear operation in weak inversion with currents of about 1 \( \mu \)A and lower, PMOS transistors are large sized: \( W/L = 200/1 \) \( \mu \)m for \( M_1, M_2, M_8 \) and \( M_9 \).

For the differential pair \( M_3 \) and \( M_4 \), longer channel with smaller widths are used to provide good matching. \( M_2, M_3, M_4 \) and \( M_9 \) have separate n-wells to remove errors due
to bulk effect. Also, fast and stable operation is achieved by adjusting channel length for inner loop transistors M5, M6 and M7.

5.3.5 Switched Gain Control 2

The switched gain control block is implemented using latched comparators, transmission gate switches, and two reference voltage generators (V\textsubscript{INIT} and V\textsubscript{TH}) as shown in Figure 5-14. A latched comparator which is a folded-cascode differential amplifier with a dynamic latch load compares two inputs, V\textsubscript{in} (output from RMS detector) and V\textsubscript{in} (threshold voltage from the reference voltage generator V\textsubscript{TH}), and yields differential outputs to activate transmission gate switches: either S\textsubscript{A} or S\textsubscript{B}. When the latch signal goes from 0 to 1, the cross-connected positive feedback loop forces the differential output voltages to be latched [Ock99]. The result of the comparison of the two inputs decides the polarity of the output. The output of the latched comparator is connected to the gates of transmission gate switches (S\textsubscript{A} and S\textsubscript{B}) which select between two voltage inputs. The switching connection to select V\textsubscript{C1} is completed when the transmission gate switch S\textsubscript{1} is on. Three sets of latched comparators and transmission gates select gain-control voltage out of four initial voltages by comparing the outputs of the RMS detectors and the threshold voltages, as described in the AGC algorithm section.

The initial voltage and threshold voltage generators provide reference voltages which are preset by resistor banks. The initial voltage generator V\textsubscript{INIT} provides six preset voltages V\textsubscript{3dB}, V\textsubscript{0dB}, V\textsubscript{7dB}, V\textsubscript{12dB}, V\textsubscript{17dB} and V\textsubscript{27dB}. V\textsubscript{3dB}, V\textsubscript{7dB}, V\textsubscript{17dB} and V\textsubscript{27dB} are selectable V\textsubscript{C1} voltages, while V\textsubscript{0dB} and V\textsubscript{12dB} are V\textsubscript{DC} voltage and V\textsubscript{C0} voltage for the initial VGA gain, respectively. As we mentioned before, the inverse gain control loop sets the two-stage VGA gain as A\textsubscript{v} = 40\cdot\log(V\textsubscript{C1}/V\textsubscript{DC}) dB. So, V\textsubscript{C1} can be found such that V\textsubscript{C1} = V\textsubscript{DC} \cdot 10^{A\textsubscript{v}/40}.

(5-29)
With $V_{\text{DC}} = V_{\text{CM}} \pm 35 \text{ mV}$, the differences of the differential $V_{\text{C1}}$ (including $V_{\text{DC}}$ and $V_{\text{C0}}$) voltages for $V_{-3\text{dB}}$, $V_{0\text{dB}}$, $V_{7\text{dB}}$, $V_{12\text{dB}}$, $V_{17\text{dB}}$ and $V_{27\text{dB}}$ are 58.5, 70, 104.8, 139.6, 186.2 and 331.2 mV, respectively. Since single-ended $V_{\text{C1}}$ is converted to a corresponding differential $V_{\text{C1}}$ through V-to-I and I-to-V converters, we can find the single-ended voltages for $V_{-3\text{dB}}$, $V_{0\text{dB}}$, $V_{7\text{dB}}$, $V_{12\text{dB}}$, $V_{17\text{dB}}$ and $V_{27\text{dB}}$ by DC simulation of those two converters. Figure 5-15 shows DC simulation result of the single-ended V-to-I and I-to-differential V conversion for gain control voltage $V_{\text{C1}}$. 

Figure 5-14. Switched gain control block implementation using latched comparators and transmission gates
The corresponding single-ended $V_{C1}$ voltages for $V_{-3dB}$, $V_{0dB}$, $V_{7dB}$, $V_{12dB}$, $V_{17dB}$ and $V_{27dB}$ are 687, 716, 798, 871, 963 and 1279 mV. These preset control voltages for switched gain are implemented using resistor banks as shown in Figure 5-16. Applying an external 1.5 V supply voltage to a branch with total resistance of 15 kΩ enables tapping out the desired voltages with corresponding ratio of tapped resistors (Figure 5-16 (a)). In order to improve matching and to reduce process variations, each section of resistor is made of serial and parallel connections of a root component resistor as shown in Figure 5-16 (b) [Sai02]. For example, by choosing 2.32 kΩ as the root resistor $R_R$, the 0.29 kΩ resistor between $V_{-3dB}$ and $V_{0dB}$ is realized as eight parallel connections of the root component.

Another reference voltage generator $V_{TH}$ provides three threshold voltages ($V_{-20dBm}$, $V_{-22dBm}$ and $V_{-30dBm}$) for latched comparators. The reference voltage $V_{-20dBm}$ is preset to the positive output value of the RMS detector with 500 mV$_{pp}$ input signal (desired output
Figure 5-16. Reference voltage generator $V_{\text{INIT}}$ has six taps for preset voltages and is implemented as serial and parallel connections of a root component resistor.

Other reference voltages $V_{-22\text{dBm}}$ and $V_{-30\text{dBm}}$ are preset to the value of the RMS detector with 397.2 mV$_{pp}$ and 158.2 mV$_{pp}$ input signals which are 2 dB and 10 dB less than the desired one, respectively. These preset voltages are compared with actual output voltages of RMS detectors by latched comparators during the switching gain control step. Applying the same method used for $V_{\text{INIT}}$, the reference voltage generator $V_{\text{TH}}$ is implemented using a resistor bank (Figure 5-17). Note that two different sets of threshold voltages are provided with signal type selection, since RMS values are different between sine wave signal (sine) and short training symbol (STS).
5.4 IC Implementation and Measurement

5.4.1 IC Implementation with Embedded Test Points

The portion of the AGC circuits following the channel-selection filter in Figure 5-2, including two VGAs, switched gain control 2 and AGC with one-step correction, was fabricated using a 0.18 µm CMOS process available through MOSIS. On-chip embedded test points are included in the design for testability. Analog test buses provide access to...
internal nodes using switching structures [Bur01]. Figure 5-18 shows the AGC circuitry with 7 test points (SWT1 ~ SWT7).

The main signal chain of the AGC circuit consists of two VGA stages as described in the previous section. Combined with external coupling capacitors ($C \approx 0.1 \mu F$), input bias voltages for VGA2 are provided by on-chip resistors ($R \approx 240 \, k\Omega$) in a negative feedback loop from the output nodes of VGA3. This feedback loop works as an RC lowpass filter which provides dc bias voltage to the input stage. Output signals can be measured through voltage buffers which reduce the output impedance of the AGC circuit. Simple PMOS source followers are used as voltage buffers as shown in Figure 5-19. Since these buffers are for test purpose, 3 V devices are used to accommodate level shifted DC bias voltage ($0.48 \, V \rightarrow 1.48 \, V$). The current source M2 provides 1 mA of DC bias current for good sourcing capability which enables this buffer to sink a large current from the load concerning large-signal behavior. The bulk of M1 is tied to the source using a separate n-well, which eliminates nonlinearity due to body effect.

As designated in Figure 5-18, seven test point switches are placed as follows: 1) at the output nodes of RD3, 2) between the output nodes of RD5 and the $V_o$ input nodes of V-to-I converter, 3) between the $I_o$ output branch of V-to-I converter and the $I_o$ input branch of computation block, 4) between the $I_{ref}$ output branch of V-to-I converter and the $I_{ref}$ input branch of computation block, 5) between the $I_{c2}$ output branch of computation block and the $I_{c2}$ input branch of I-to-V converter, 6) between the output nodes of $V_c1/V_c2$ time switch and the $V_c$ input nodes of DDA, and 7) between the $V_{dc}$ output nodes of I-to-V converter and the $V_{dc}$ input nodes of VGA4. Test switches 3), 4)
and 5) are current switches implemented using current mirrors with transmission gate switches while others are voltage switches (transmission gate switches).

Figure 5-18. Proposed AGC circuitry with 7 test points
Figure 5-19. Output voltage buffer

All test points are connected with differential in/out test buses through input/output test switches, and the test buses are connected to four pads (Test_in+, Test_in-, Test_out+ and Test_out-). From the test pads, we can access one out of seven test points, selectable using test switches. Internal signal paths are connected as normal when the test switches are off. However, one of the test switches is on, the internal signal path of the point is disconnected and the test point is externally accessible. For example, if we turn the test switches 7_IN and 7_OUT on, then the Vdc output nodes of the I-to-V converter are connected to Test_out+ and Test_out- pads, and the Vdc input nodes of DDA are connected to the Test_in+ and Test_in- pads. In this switch selection, we can monitor internal Vdc from Test_out pads and force an external Vdc value to Test_in pads during measurement.

The voltage switch SWT7 in Figure 5-20 (a) has two selections, that is, SWTi for test input and SWT0 for test output, and eight transmission gates for differential signal paths, where four of them (A, B, C and D) are used for positive signal paths. Two
internal nodes ($V_{ip}$ and $V_{op}$) are connected through transmission gates A and C when both switches are set to 0. Setting SWTo to 1 forces transmission gate A to off and B to on, which changes connection from $V_{ip}$-$V_{op}$ to $V_{ip}$-$T_{op}$. Thus, internal voltage of node $V_{ip}$ can be monitored through the positive test output pad $T_{op}$. Similarly, setting SWTi to 1 makes $V_{op}$ connected to $T_{ip}$, thus external input can be forced into $V_{op}$ node through the positive test input pad $T_{ip}$.

Figure 5-20 (b) shows current switch SWT5, used for testing the Ic2 branch in the computation block. Two selections are SWTi for test input and SWTo for test output. Voltage switch box SW_I connects Vn2 to VN node and ground (0) to VTi and VTo nodes when both switches are off. In this switch connection, the output current flows through the Ic2 branch via the M1-M2-M3-M4 current mirror. When SWTi is set to on, the gate of M4 is switched to ground; hence, the Ic2 branch is disconnected from the computation block. At the same time, the gate voltages of M6 and M9 are switched from ground to Vn2, which enables connection from Tin to Ic2 via M6-M7-M8-M9 current mirror. For the test output, switch sw5To is set to on. This makes transistor M4 off and transistor M5 on, thus the output current flows through Tout branch via M1-M2-M3-M5 current mirror.

5.4.2 Simulation Results

The implemented AGC circuits were simulated using Cadence Spectre with TSMC 0.18 µm models. Figure 5-21 shows DC simulation results for the VGA in the inverse gain control loop. By applying control voltage $V_c$ to the inverse gain loop, we can easily achieve a linear gain control characteristic with desired gain of $A_v = V_c/V_{dc}$. 
With $V_{dc} = 35 \text{ mV}$, we can get the VGA gain of -4 dB by setting $V_c = 22.1 \text{ mV}$, of 0 dB by setting $V_c = 35 \text{ mV}$ and of 16 dB by setting $V_c = 221 \text{ mV}$. When $V_{in}$ is set to 39.6 mV, the simulation result shows that $V_{out}$ changes from 25 mV to 247 mV with $V_c$, a range of -4 to 16 dB. This is just a -0.1 dB gain error at the maximum gain (16 dB). Another DC simulation is for the input-output linearity of the VGA.

Figure 5-20. Test switches; (a) voltage switch, and (b) current switch
Figure 5-21. DC gain control simulation for the VGA with inverse gain loop

Figure 5-22 (a) shows $V_{in}$ vs. $V_{out}$ plot at the minimum gain (-4 dB), while Figure 5-22 (b) shows the plot at the maximum gain (16 dB). The simulation results show that the linearity error for the maximum input (250 mVp) at the minimum gain is 0.36 dB and the linearity error for the maximum output (250 mVp) at the maximum gain is -0.1 dB. AC response plots of the two-stage VGA shown in Figure 5-23 ensure the operation of the VGAs in the channel frequency range (156.25 KHz – 8.3 MHz).

Figure 5-22. DC simulation for $V_{in}$ versus $V_{out}$ of the VGA at (a) -4 dB gain and (b) 16 dB gain
Noise simulation indicates that the total output noise of the VGA for the signal bandwidth (156.25 KHz ~ 8.3 MHz) at 0 dB gain is 221 µV_{rms}. Input referred noise can be derived as: $221 \times 10^{-6} / \sqrt{8.14 \times 10^6} = 77.5 \text{nV/Hz}$. Figure 5-24 shows noise versus gain plot of the VGA. Input referred noise at the minimum gain (-4 dB) is about 120 nV/√Hz due to negative gain, but it goes down to 97 nV/√Hz at the actual minimum gain without margin (-2 dB). Moreover, as VGA1, located before channel-select filter, has 7 or 14 dB selectable gain, the input referred noise of the analog baseband processor would be below 40 nV/√Hz.

The linearity of the 2-stage VGA is specified by single-tone total harmonic distortion (THD) in -8, 0 and 32 dB gain modes in Figure 5-25. The 2-stage VGA shows 0.99 % THD at the maximum gain (32 dB), while it shows 1.03 and 1.36 % THDs at 0 dB and minimum (-8 dB) gains, respectively.
Figure 5-24. VGA input and output noise versus gain

Figure 5-25. Linearity of the 2-stage VGA in THD (%) versus input signal voltage plots at (a) -8 dB, (b) 0 dB and (c) 32 dB gain settings

Figure 5-26 shows the input versus output characteristic of the RMS detector. Plots (a) and (b) are drawn in dB range, where (a) is for a sine wave input and (b) is for a short training symbol. The input versus output characteristics for sine waves and short training symbols have about 21 dB (-18 to 3 dB) of dynamic range with reasonable linearity.
Figure 5-26. Input versus output characteristic of RMS detector; (a) for sine wave signal and (b) for short training symbol

The input voltage versus output current characteristic of the V-to-I converter is shown in Figure 5-27 (a). The V-to-I converter takes the differential voltage from the RMS detector as input and converts it to a single-ended output current which flows into the computation block as $I_{o1}$. To make sure the current mode circuit operate fast enough for the settling time constraints, the V-to-I converter was designed with fast step response (Figure 5-27 (b)). Figure 5-28 shows the input versus output plot of the I-to-V converter.

Figure 5-27. Characteristic of V-to-I converter; (a) input versus output linearity and (b) step response
Figure 5-28. Input versus output characteristic of I-to-V converter

The differential output voltage (0 ~ 500 mVpp) changes linearly along with the single-ended input current (0 ~ 1.5 µA). The small increase (~20 mV) of the common-mode voltage over the range does not affect the differential output voltage of the I-to-V converter.

Simulation results of the proposed analog computation block for sine wave and short training symbol signals are shown in Figures 5-29 and 5-30, respectively. As discussed in the circuit design section, the computation block operates in current mode with three inputs (Io1, Iref and IC1) and generates one output (IC2). The plots show the output (IC2) versus input (Io1) characteristic, since the currents Iref and IC1 are fixed in the final gain setting step. The switched gain control current IC1 is set to one of the four preset values: 256 nA (-3 dB), 452 nA (7 dB), 794 nA (17 dB) and 1.397 µA (27 dB). The reference current Iref is set to 1.025 µA for sine wave or to 631 nA for the short training symbol signal. Again, this computation block corrects the VGA gain, which was set to a switched gain with ±5 dB error range, to the final gain with ±1 dB error. Figure 5-29 shows simulation results for sine wave signals, with Io1 swept from 500 nA (-6.2 dB from Iref) to 2 µA (5.8 dB from Iref). The simulated control current IC2 is plotted in the
black curve while the ideal curve is drawn in gray. The largest error between the simulation and the ideal is -0.36 dB when Io1 is bigger (5.8 dB) than I_ref with -3 dB switched gain. Figure 5-30 shows the simulation results for short training symbol signals, with Io1 swept from 300 nA (-6.5 dB from I_ref) to 1.2 µA (5.6 dB from I_ref). In this simulation, the largest error is -0.4 dB when Io1 is smaller (-6.5 dB) than I_ref with 27 dB switched gain. Figure 5-31 depicts the step response of the computation block, which demonstrates that the current-mode operation in weak inversion should meet the settling time constraints of the system.

Figure 5-29. DC simulation results of the computation block for sine wave signal with the switched gain of (a) -3 dB, (b) 7 dB, (c) 17 dB, and (d) 17 dB
Figure 5-30. DC simulation results of the computation block for short training symbol signal with the switched gain of (a) -3 dB, (b) 7 dB, (c) 17 dB, and (d) 17 dB

Figure 5-31. Transient simulation result (step response) of the computation block

The proposed AGC circuit in Figure 5-18 is simulated using transient response for both sine wave and short training symbol signals. Given a settling time requirement of 7
short training symbol times, the implemented AGC circuit uses symbol time duration from t3 through t7 \((5 \times 0.8 = 4 \, \mu s)\). The initial gain for two-stage VGA is set to 12 dB. The switched gain is selected during t4 and the final gain is adjusted during t6. Figure 5-32 shows output signals with the final gain of (a) -4 dB, (b) 1 dB, (c) 4 dB and (d) 9 dB, where the switched gain of -3 dB for (a) and (b), and 7 dB for (c) and (d) are selected. Simulation results with small sine wave inputs to get the final gain of (a) 15 dB, (b) 20 dB, (c) 23 dB and (d) 28 dB are shown in Figure 5-33. Similar simulations with short training symbol inputs are presented in Figures 5-34 and 5-35. From the simulation results, it can be observed that the AGC circuit adjusts signals to the desired level with gain error less than ±1 dB through the actual gain range of -4 ~ 28 dB.

5.4.3 IC Measurement and Analysis

The proposed AGC circuit in Figure 5-18 was laid out using the TSMC 0.18\(\mu\)m process with 6 metal layers. Figure 5-36 shows the full chip layout floor plan including 40 bonding pads. The total chip area including ESD (Electro-Static Discharge) bonding pads is \(2850 \times 2850 \, \mu m\), whereas the actual AGC circuit area is \(750 \times 750 \, \mu m\). The die photo of the fabricated AGC circuit is shown in Figure 5-37. The fabricated parts are packaged in DIP40 (40-pin ceramic package).

The package samples were measured using a test board to get access to the embedded test points. Figure 5-38 illustrates the test board design for the packaged AGC circuit. The test board includes DIP switches for embedded test point selection and input-output matching connectors. The selectable output buffer stage is also included in the test board to provide matching with the 50\( \Omega \) test equipments. The test board shown in Figure 5-39 was designed and built by the support of Conexant\textsuperscript{®} Systems. A detailed schematic of the test board is attached as an appendix.
Figure 5-32. Transient simulation results of the AGC circuit for sine wave signal with final gain of (a) -3 dB, (b) 1 dB, (c) 4 dB and (d) 9 dB
Figure 5-33. Transient simulation results of the AGC circuit for sine wave signal with final gain of (a) 15 dB, (b) 20 dB, (c) 23 dB and (d) 28 dB
Figure 5-34. Transient simulation results of the AGC circuit for short training symbol signal with final gain of (a) -3 dB, (b) 1 dB, (c) 4 dB and (d) 9 dB.
Figure 5-35. Transient simulation results of the AGC circuit for short training symbol signal with final gain of (a) 15 dB, (b) 20 dB, (c) 23 dB and (d) 28 dB
With all prepared measurement setup including test board, some unexpected problems were found during basic DC measurements. The first one is oscillation in DC bias voltages. The bias circuit, shown in Figure 5-40, consists of simple current mirrors providing gate voltages to cascode structures of PMOS and NMOS transistors.

An external resistor is connected to allow the bias current to be varied. It is designed to provide 30 µA with an external resistor of 7.8 kΩ. A grounded variable resistor (R_{var}) on the test board is connected to the R_{ext} pin of the package and its value can be adjusted to provide the desired bias current in spite of process variations. However, the positive
feedback loop oscillates when the parasitic C reduces the impedance at the $R_{ext}$ port. This oscillation was eliminated by reducing the parasitic C. Instead of using the direct on-board connection of the variable resistor which has high parasitic C, a fixed value of resistor ($R_b$) is added between $R_{ext}$ pin of the package and $R_{var}$. In addition, a ferrite bead was inserted in the $R_{ext}$ pin connection.

Figure 5-37. Die photo of the fabricated AGC circuit

Another problem in the measurement is that the input DC bias voltages in most chip samples were higher than expected. The input DC bias voltages are provided by output bias voltages created from diode-connected NMOS transistors using resistive negative feedbacks. The DC bias voltages were designed to be about 0.48 V, but the measured values are in the range of 0.53~0.56 V. Since this voltage corresponds to
Figure 5-38. Test board design for the 40-pin AGC circuit package

Figure 5-39. Test board with a packaged AGC sample plugged in
Figure 5-40. Bias circuit with external resistor connection: (a) can cause oscillation and (b) can fix the problem.

$V_{GS\_M8} - V_{Rs}$ of the output NMOS devices of the VGA in Figure 5-6, process variations in transistors’ size does not explain the voltage difference. Instead, the variation of the model parameters such as threshold voltage parameter $V_{TH}$ or transconductance parameter $g_m$ may explain the DC voltage differences. Measurements of single-transistor characteristics are possible using embedded test point connections. As shown in Figure 5-41, the measurement results indicate that there exist transconductance differences between simulations and measurements, while extracted threshold voltages $V_{TH}$ are almost identical to the simulation value. Similar analysis can be done through bias current versus voltage measurements in the bias circuit. The measurement results show that a higher external resistor ($\sim 8.5 \, \text{k}\Omega$) than simulated ($\sim 7.8 \, \text{k}\Omega$) is needed to get the desired bias current ($\sim 30 \, \mu\text{A}$), consistent with the lower $g_m$ of the fabricated FETs.
Figure 5-41. Measurement results on device characteristics with various embedded test point selections: (a) diode-connected NMOS in RMS detector (W/L=5/10 μm), (b) diode-connected NMOS in cascode current mirror (W/L=3/3 μm), (c) threshold voltage extraction (diode-connected NMOS), and (d) measurement plot on bias current versus external resistor.

The third problem observed in the measurement of packaged samples is another device parameter shift: the measured resistor values are lower than the simulated values. Figure 5-42 shows the measurement of resistance between the two input nodes. The loop for measurement includes feedback resistors ($R_{fb} = 240$ kΩ), output load resistors ($R_L = 10$ kΩ) and shift resistors ($R_S = 244$ Ω) of the VGA. Although the designed and simulated resistance value of the two input nodes is ~500.5 kΩ, the measured values for 20 samples lie between 428 kΩ and 437 kΩ. The measurement result shows shifted resistance value of -14 %. 

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Figure 5-42. Measurement of on-chip resistor variation: (a) resistors between input nodes and (b) measurement results for 20 samples

After fixing these problems in the measurement environment, the gain control function of the two-stage VGA is measured. As described before, VGA gain is set by the inverse-gain block using two dc voltages: \( A_v = V_C / V_{dc} \). Sine wave signals from an Agilent 33120A were used for input signals. The amplitudes of the output signals are measured to compute gains using Agilent 54622D oscilloscope. Control voltages are applied to the inverse gain loop through test points 6 and 7. Measurement results of the gain control function in Figure 5-43 match simulation results closely. The replica bias circuit in Figure 5-7 minimizes the effects of supply voltage variations on VGA gain as shown in Figure 5-44.
Figure 5-43. Gain control curve for the 2-stage VGA

Figure 5-44. 2-stage VGA gain with supply voltage variation

The stability of the VGA gain with bias current and temperature variations is also measured, as shown in Figure 5-45. The gain errors due to bias current variation are 0.7 dB at 28 µA and -0.87 dB at 33 µA. The temperature variation from 5 to 80 °C
generates gain errors from 0.4 to -1.1 dB. Figure 5-46 shows the input-output linearity and harmonic distortion plots of the chip at 12 dB gain. The VGA output signal was measured 37.5 dB of spurious-free dynamic range (SFDR), which showed only 3.4 dB reduction from 1 MHz sinusoidal input signal (40.9 dB of SFDR). Frequency responses of the 2-stage VGA at -8, 12 and 32 dB gain are shown in Figure 5-47. This verifies the operation of the VGA over the channel bandwidth of 156.25 KHz ~ 8.3 MHz.

Figure 5-45. Stability of VGA gain with (a) bias current and (b) temperature variations
Figure 5-46. 2-stage VGA characteristic at 12 dB gain: (a) input-output linearity, (b) SFDR

Figure 5-47. Frequency response of the 2-stage VGA: (a) measurement result and (b) simulation result

Figure 5-48 shows input versus output plot of the RMS detector. The measurement result agrees well with the simulation result. The small deviation from ideal is reasonable for the simple square-law based RMS detector, and is acceptable in meeting system gain-accuracy specification. The V-to-I converter between the RMS detector and the computation block was measured by applying input voltages to test point 2 and detecting output current from test point 3. The resulting linear conversion plot of the measurement
is shown in Figure 5-49. The measured input-output characteristic of the current-mode computation block is shown in Figure 5-50, which shows that the measurement results agree well with the simulation results. Table 5-1 summarizes the simulation and measurement results.

Table 5-1

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Figure 5-48. Measurement result for input-output characteristic of the RMS detector

Figure 5-49. Measurement result for input-output characteristic of the V-to-I converter
Figure 5-50. Measurement result for input-output characteristic of the current mode computation block

Table 5-1. Summary of the simulation and measurement results

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<th>Measurement</th>
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<td>0.18 µm CMOS 1P6M</td>
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<tr>
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6.1 Summary

WLAN technologies are so popular these days that even casual PC users may have heard about 802.11a, b, or g. While implementing one-chip RF transceivers is a challenge, using CMOS process technology can be a solution due to its high integration capability and low cost. This research focuses on the design of an analog baseband processor for a CMOS 802.11a WLAN receiver. The main functions of an analog baseband processor are channel-select filtering and AGC. Since 802.11a uses OFDM signals, which have a high PAPR, we need to analyze signal estimation for AGC and devise an efficient AGC algorithm for the analog baseband processor design. The following summarizes the major research items.

In Chapter 2, background knowledge and specifications for the IEEE 802.11a standard were described. The standard specifies 20 MHz of channel bandwidth with 52 OFDM subcarriers in a 5-GHz RF frequency range. For data reception of each packet frame, seven short-training-symbol times (5.6μs) of preamble are allocated for AGC convergence. The standard details the receiver performance requirements which guide attenuation specifications for channel-select filtering.

Also, the system architecture for the analog baseband signal chain block was presented. As a sub-block of a direct conversion receiver, the analog baseband signal chain consists of a pre-filter AGC, a channel-select filter and a post-filter AGC block. Design specification for the VGA gain range is obtained by estimating the receiver gain.
distribution. Analysis of a conventional closed loop AGC was given to introduce AGC fundamentals.

In Chapter 3, the statistics of OFDM amplitude estimation were studied through simulation. OFDM signal generators with peak, average, RMS and pseudo-RMS detectors were simulated based on the 802.11a standard using Matlab/Simulink. Given random input OFDM-QAM signals, statistical simulations show that a peak detector can degrade the accuracy of amplitude estimation in OFDM analog baseband processor, leading to a high standard deviation in estimated amplitude. The RMS detector shows the least error variance, and thus the most accuracy among those detectors. However, a simple pseudo-RMS detector could also be used, because there is no big difference in standard deviation values between an RMS detector and pseudo-RMS detectors.

In Chapter 4, a cascade of 3rd- and 4th-order elliptic lowpass Gm-C filters for the baseband processor for a 5-GHz WLAN receiver was designed. Various techniques such as transconductors with unit Gm cells, internal node amplitude scaling, and parasitic-capacitance compensation were implemented to reduce mismatch, process- and temperature-variation effects. Also, a second version of the filter was designed that avoids floating capacitors. The technique to avoid floating capacitors improved linearity by better internal node amplitude scaling, at the expense of increased complexity. Both versions of the filter circuits, designed in TSMC 0.25μm CMOS technology, were verified by Cadence Spectre.

In Chapter 5, some issues on AGC with OFDM signal were discussed and a new analog baseband AGC algorithm for 802.11a WLAN receiver was proposed. As shown in Chapter 3, RMS detectors are recommended for OFDM amplitude estimation. Due to
the stability condition that the system’s time constant be much longer than the estimation time, a conventional closed-loop AGC cannot converge within the required settling-time constraints. The new AGC algorithm uses a three-step iterative open-loop gain control method (two coarse gain-settings using switches, followed by a final fine gain-setting using an open-loop computation circuit). The algorithm converges within seven short-training-symbol times, and holds the final gain throughout the whole packet frame. This avoids the settling-time limits of a conventional closed-loop AGC.

The VGA circuit was designed with a linear transconductance cell using a modified differential FVF with a linear transconductance-setting resistor, Gilbert cell-type differential pairs and linear load resistors. An inverse-gain block uses feedback to achieve an accurate gain-control function. A Differential Difference Amplifier (DDA) is used for the amplifier in the inverse gain control loop so that the feedback loop operates in differential mode. The differential folded cascode output stage of the DDA, combined with a common-mode feedback circuit with level-shifters, provides differential output control voltages.

A simple RMS detector circuit was introduced based on the approximately square-law characteristics of long-channel NMOS transistors in strong inversion. The analog computation block was implemented using translinear circuits based on weak-inversion FETs, which reduced the power dissipation and complexity of the circuit. New circuits such as V-to-I converters with current attenuation and I-to-V converters with current amplification were designed for use with the current-mode computation block.

The switched gain-control block was implemented using latched comparators, transmission-gates, and two reference voltage generators. The initial voltage and
threshold voltage generators provide reference voltages that are preset by resistor banks. The resistor banks were made of serial and parallel connections of a root component resistor to reduce the effect of process variations and mismatch.

The proposed AGC circuit including embedded test points was fabricated, and its performance was verified by simulations and measurements using TSMC 0.18 µm CMOS process models available through MOSIS. The AGC circuit adjusts the VGA gain so that the RMS voltage of the output signal matches the desired level with less than ±1 dB error through the actual gain range of -4 to 28 dB.

6.2 Suggestions for Future Work

Embedded test points with selectable switches as well as a supporting test board provided direct and versatile measurement options. However, most measurements were done using a single function block with a sine-wave generator due to limit in the test environment. For example, an accurate multiple-clock generator would be required for testing the whole signal chain of the AGC circuit including switched gain control. Furthermore, verification of AGC performance with short training symbols was limited to simulation due to lack of a short training symbol generator.

Also, fabrication was limited to the post-filter AGC section. Fabrication of the whole signal chain including filter is left for future work. Furthermore, an unexpected issue is that among 20 packaged samples, only two showed the measurement results consistent with simulation data. This may have been due to some unexpected device parameter shifts, as discussed in Section 5.4.3. To fix unexpected measurement problems and to get better measurement results, fabricating a revised version of the test IC is recommended.
Design of additional function blocks such as automatic Gm tuning and DC-offset cancellation circuits are not covered in this research. Including these implementations would supplement the research work on the design of analog baseband processor for CMOS 5-GHz WLAN receiver. Other applications of the research can be found in gain-control circuits and current-mode circuit areas. The inverse-gain loop with linear VGA and DDA can also be used in conventional closed-loop AGC circuit with peak detectors to achieve a linear-in-dB gain control with a constant settling time. The translinear circuit in the analog computation block can be modified for other computation functions. Combined with the translinear circuit, the new V-to-I and I-to-V converters can easily implement current mode circuits in usually voltage-mode design environments.
LIST OF REFERENCES


109


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BIOGRAPHICAL SKETCH

Okjune Jeon was born in Busan, Korea, in 1964. He received the B.S. degree in electronics engineering from Korea Military Academy, Seoul, Korea, in 1986, and the M.S. degree in electrical engineering from Case Western Reserve University, Cleveland, Ohio, in 1990.

He served in the Republic of Korea Army as a signal officer for 14 years, working on the operation of PCM cable, VHF, M/W and satellite communication systems. Through his military career as a company commander and as a staff officer, he gained his experience in group leadership and project management.

From 1997 to 2000, he was a faculty member of the Department of Electronics Engineering, Korea Military Academy. Since 2001, he has been working on his Ph.D. degree in the analog IC design group at the University of Florida as a graduate research assistant.

During the summer of 2002, he was employed at Intersil Corporation, Palm Bay, Florida, where he worked on the design of analog filters for a CMOS 802.11a WLAN receiver as an internship design engineer. He received an Outstanding Student Designer Award from Analog Devices Incorporated in 2004.

His research interests involve analog and mixed-signal circuit design including CMOS integrated circuits, continuous-time filters, and AGC circuits.