Dedicated to my loving mother and wife for their love and constant support
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<td>2DEG</td>
<td>2-dimensional electron gas</td>
</tr>
<tr>
<td>ALD</td>
<td>Atomic layer deposition</td>
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<tr>
<td>AlGaN</td>
<td>Aluminum gallium nitride</td>
</tr>
<tr>
<td>AIN</td>
<td>Aluminum nitride</td>
</tr>
<tr>
<td>C-V</td>
<td>Capacitance-voltage</td>
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<td>CDLTS</td>
<td>Conductance deep level transient spectroscopy</td>
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<td>DLTS</td>
<td>Deep-level transient spectroscopy</td>
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<td>EDX</td>
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<td>FET</td>
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<td>FIB</td>
<td>Focused ion beam</td>
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<td>HEMT</td>
<td>High electron mobility transistor</td>
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<tr>
<td>ICP</td>
<td>Inductively coupled plasma</td>
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<td>InAlN</td>
<td>Indium aluminum nitride</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium nitride</td>
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<td>LEDs</td>
<td>Light emitting diodes</td>
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<td>MESFETs</td>
<td>Metal semiconductor field effect transistors</td>
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<td>MOCVD</td>
<td>Metal Organic Chemical Vapor Deposition</td>
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<tr>
<td>MOSFETs</td>
<td>Metal oxide semiconductor field effect transistors</td>
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<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>PAE</td>
<td>Power added efficiency</td>
</tr>
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<td>PECVD</td>
<td>Plasma-enhanced chemical vapor deposition</td>
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<td>Photoluminescence</td>
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RELIABILITY STUDY OF GAN-BASED HIGH ELECTRON MOBILITY TRANSISTORS

By

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Compound semiconductors are III-V semiconductor nitrides, such as AlN, GaN and AlGaN, which have attracted plenty of attention due to their extraordinary material properties, such as high mobility, high saturation velocity and power density, and become a promising alternative for microwave power device. They have demonstrated excellent performance in such applications as UV detectors, UV and visible light emitting diodes (LEDs), microwave power amplifications, satellite, radar and wireless communication systems.

However, the main impediment of this technology is lack of reliability. In order to improve the reliability of GaN HEMTs technology, it is essentially important to understand the nature of device degradation. In this dissertation, the effects of source field plates, gate metallization, passivation layers, buffer structures and proton irradiation on the dc/rf performance and reliability of AlGaN/GaN high electron mobility transistors (HEMTs) under off-state stress conditions were investigated using step-stress cycling.

The source field plate alleviated the peak electrical at drain side of gate edge and enhanced the drain breakdown voltage from 55V to 155V and the critical voltage ($V_{cri}$)
for off-state gate stress from 40V to 65V, relative to devices without the field plate. The critical voltage of electrical step-stress was increased more than 100% for HEMTs with Pt/Ti/Au gate metallization as compared to HEMTs with Ni/Au gate metallization. As compared to Al₂O₃ and HfO₂, SiNx was found to be the most effective in reducing current collapse and also reduced $f_T$ and $f_{\text{Max}}$ through additional parasitic capacitance. The HEMTs with the thick GaN buffer layer showed the lowest critical voltage ($V_{\text{cri}}$) during off-state drain step-stress, but this was increased by around 50 and 100% for devices with the composite AlGaN/GaN buffer layers or thinner GaN buffers, respectively. The dependence of dc and rf characteristics and reliability of GaN-based HEMTs on proton irradiation energies and doses were examined. GaN-based HEMTs showed a remarkable resistance to high energy proton-induced degradation and improved device reliability.

In addition, temperature dependent subthreshold slope measurement was developed to study the effect of off-state electrical stress on the trap densities and two traps with different activation energies at temperature range of 300-493K and 493-573K were identified.

Finally, The laser micromachining of SiC by 193nm ArF excimer laser produced much higher etch rates (229-870 µm/min) than conventional dry etching (0.2-1.3 µm/min) and the via entry can be tapered to facilitate subsequent metallization.
1.1 Introduction to GaN-based High Electron Mobility Transistors (HEMTs)

There is increasing need for high power, high efficiency and linearity amplifiers for communication systems and defense radar. III-nitride materials with wide bandgap are promising candidates for these applications. Examples are AlN and GaN with direct bandgaps of 3.4 and 6.2, respectively. The variation of the energy bandgap with corresponding lattice constant for the Group III-V is shown in Figure 1-1. Gallium Nitride (GaN) based high-electron-mobility-transistors (HEMTs) are the next generation of power transistor technology, which was first demonstrated in 1993 and have exhibited impressive attributes and outstanding potential for high voltage and high switching frequency applications. In the past few decades, some aspects including material quality, choice of substrate, epi-layer structures, advanced device designs and processing techniques have been studied intensively. Recently, AlGaN/GaN HEMTs have attracted plenty of attention due to its extraordinary material properties, such as high mobility, high saturation velocity and power density, and have therefore become a promising alternative for microwave power devices. As a result of the large conduction band discontinuity between Al$_{0.25}$GaN (~4.2 eV) and GaN (3.4 eV), high electron mobility and high electron saturation velocity have been demonstrated in AlGaN/GaN material systems. Electron mobility exceeds 1500 cm$^2$/V-s and saturation velocity is around 2.5×10$^7$ cm/s, respectively, and are beneficial for high frequency operation. Thus far, a current-gain cutoff frequency ($f_T$) of 225 GHz with a gate length ($L_G$) of 55 nm and a power-gain cutoff frequency ($f_{max}$) of 300 GHz with a gate length of 60 nm have been demonstrated in AlGaN/GaN HEMTs. In addition, the presence of
strong piezoelectric effect and spontaneous polarization in III-nitride leads to a high carrier concentration (higher than $10^{13}$ cm$^{-2}$). As a result, a high current density can be achieved in AlGaN/GaN heterostructures without conventional doping.\textsuperscript{13, 14} Moreover, GaN has a large band gap of 3.4 eV and a high breakdown electric field (~3 MV/cm), which makes it capable of handling high voltage. A record breakdown voltage of 2200V with a $L_{GD} = 20$ μm has been reported.\textsuperscript{15} The high current density and high breakdown voltage of this material make it an excellent candidate for high power applications. To date, record output power densities of 5.1W/ mm at 31 GHz,\textsuperscript{16} 16.7 W/mm at 10 GHz and 20.7 W/mm at 4 GHz have been reported.\textsuperscript{17} Furthermore, the good thermal stability of GaN-based HEMTs allows operation at high temperatures.\textsuperscript{18}

1.2 Motivation

In spite of the extraordinary material properties of AlGaN/GaN heterostructure systems, such as high mobility, high saturation velocity and high breakdown field, the main impediment to this technology is lack of reliability. During device operation, the main degradation modes observed in previous work are increasing of gate leakage as well as sub-threshold drain leakage, and the worsening of trap-related effects, which result in a reduction in drain current. Recently, some degradation mechanisms have been proposed. They are hot-electron-induced trap degradation\textsuperscript{19}, crystallographic-defect formation through the inverse piezoelectric effect\textsuperscript{20-22} and electric-field driven mechanism under off-state conditions.\textsuperscript{23}

1.3 Background

1.3.1 GaN-based HEMTs

A transistor is a semiconductor device containing three or more terminals, the main functions of which are to switch electronic signals, or to amplify, owing to the fact
that the controlled (output) power can be higher than the controlling (input) power.

In a Field Effect Transistor (FET), there are three terminals, including source (S),
through which the carriers enter the channel, Drain (D), through which the carriers leave
the channel and Gate (G) the terminal that modulates the channel conductivity.
Conventionally, current entering the channel at S is designated by \( I_s \), current entering
the channel at D is designated by \( I_d \), Drain-to-source voltage is \( V_{DS} \). By applying voltage
to G, one can control \( I_d \).\(^2\) The device consists of an active channel through which
charge carriers, electrons or holes, flow from the source to the drain. Source and drain
terminal conductors are connected to the semiconductor through ohmic contacts, and
the gate terminal through Schottky contact. The conductivity of the channel is a function
of the potential applied across the gate and source terminals.

The gate can be separated from the channel by an insulator (as in a MOSFET),
can form a p-n junction (JFET), or a Schottky barrier junction with the channel [Metal
Semiconductor FET (MESFET)]. The High Electron Mobility Transistor (HEMT) is a
modification of FET, also known as as heterostructure FET (HFET), which is
a FET incorporating a junction between two materials with different band gaps as the
channel instead of utilizing a doped region. Currently, commonly used material
combinations are AlGaN, InAlN and AlN with GaN. The schematic of a typical
AlGaN/GaN HEMT device is shown in Figure 1-2. In a HEMT, the current flows between
the source (S) and drain (D) terminals (ohmic contacts) through a channel, which is
called a two-dimensional electron gas (2-DEG) channel. The channel conductance is
modulated by an electric field produced by the voltage between the source and gate.
The 2-DEG channel is located inside the smaller band-gap material (GaN (3.4 eV) < Al0.25GaN (~4.2 eV)) and near the heterostructure interface.

### 1.3.2 Origin of 2DEG

Figure 1-3 shows the conduction band in the AlGaN/GaN heterostructure. The dashed line indicates the position of the Fermi level in the heterostructure. $\Phi_b$ is the barrier height. $\Delta$ is the penetration of the conduction band edge below the Fermi level at the AlGaN/GaN interface, $\Delta E_c$ is the conduction band offset, and $E_0$ is the lowest subband level of the 2DEG. The labels correspond to the ones used in equation-1 and equation-2.

The large polarization difference at the heterostructure interface induces a high electron sheet density, $n_s$. The electron density is affected by the barrier height $\Phi_b$ and the electron sheet density is calculated as

$$n_s(x,d) = \sigma_b(x) \frac{e^{-\epsilon_0 \epsilon(x)}}{e^{2d}}(e \Phi_b(x) + \Delta(x) - \Delta E_c(x))$$  \hspace{1cm} (1-1)

where $\Delta$ is the penetration of the conduction band edge below the Fermi level at the AlGaN/GaN interface, $\Delta E_c$ is the conduction band offset, $\epsilon_0$ is the dielectric constant of vacuum, and $\epsilon$ is the relative dielectric constant of the barrier layer. $\Delta$ is calculated using the expression

$$\Delta(x) = \left(\frac{9 \pi \hbar e^2 \frac{n_s(x,d) \sqrt{8m^*}}{\epsilon(x)}}{8 \epsilon_0 \sqrt{8m^*}} \right)^{2/3} + \frac{\pi \hbar^2}{m^*} n_s(x,d)$$ \hspace{1cm} (1-2)

### 1.3.3 The operation of FET

At small drain-source voltage $V_D$, the drain current $I_D$ linearly increases with $V_D$. As shown in Figure 1-4A, a fully open channel is present when a positive $V_G$ is applied,
when a negative voltage is applied to the gate, the electrons in the channel are partially depleted, and the resistance of the conducting channel increases, as shown in Figure 1-4B. As a negative gate voltage $V_G$ increased, a threshold voltage $V_{th}$ is reached. At the threshold, the electrons in the 2DEG channel are completely depleted and no electrons flow through the channel (the channel is closed). This condition is called *pinch-off*, as shown in Figure 1-4C. The transistor is switched on (the channel is conductive) at zero gate-to-source voltage ($V_G$), and requires a negative gate-to-source voltage to cut off the channel current ($I_{DS}$). This is known as a *depletion mode or normally on transistor*. Conversely, if a transistor, which is off at zero $V_G$, and requires a positive gate voltage to switch the device on, is known as an *enhancement mode or normally off transistor*.

1.3.4 Substrates

One of the key challenges in the development of GaN HEMT technology is the selection of substrate materials which provide high-quality GaN epitaxy with low density of impurities and excellent thermal conductivity in order to dissipate heat generated during device operation. Three substrates that have been widely used as substrates in the GaN technology, including Silicon (Si), sapphire ($\text{Al}_2\text{O}_3$), and silicon carbide (SiC). Recently, diamond and GaN have been employed as substrates as well. The advantage of the diamond is its high thermal conductivity, while the GaN offers a low density of impurities. Table 1-1 summarizes the properties and challenges for $\text{Al}_2\text{O}_3$, SiC, Si, and GaN substrates.\(^{27}\)

1.3.4.1 Silicon (Si)

Si has a reasonable cost and an acceptable thermal conductivity which is similar to bulk crystalline GaN, but is inferior to that of SiC and sapphire. In order to achieve the growth of high quality GaN on Si (111), the lattice misfit (~17%) and thermal expansion
coefficient (TEC) mismatch between Si and GaN must be overcome. In addition, the thermal stability of Si at typical GaN growth temperature is also inferior to SiC and sapphire. GaN grows on Si substrate with a tensile stress since Si has a larger lattice constant than GaN, which leads to the creation of crystal defects, degrading the performance of the device. On order to overcome the impact of the inherent properties in Si on epitaxial crystal quality, a nucleation layer is applied to ensure good GaN-on-Si crystal quality.28-31

1.3.4.2 Silicon Carbide (SiC)

The lattice mismatch between SiC and GaN (~4%) is relatively minor, and allows for the formation of high-quality GaN-on-SiC structures than can be achieved on either GaN-on-Si or GaN-on-Al2O3 counterparts. The density of dislocations in GaN layers grown on SiC substrate is under 3×10⁸ cm⁻². Among all substrates aforementioned, SiC is preferred for high power and high frequency applications. However, it is expensive compared to Si or sapphire and its application in the field is limited due to cost consideration.

1.3.4.3 Sapphire (Al₂O₃)

Sapphire is cheap and available in wafers with large diameters, so it is one of the more commonly employed substrates. However, it has the largest lattice misfit (~14%) and thermal expansion coefficient mismatch with GaN (the thermal mismatch varies from 14 to 26%, depending on the their relative orientation of the crystals). Another main drawback of this substrate is its poor thermal conductivity, which severely limits its use in applications where efficient dissipation of heat is required. The exceptionally high current in 2DEG channel of GaN power devices produces significant amount of heat during device operation. Poor thermal conductivity can cause device overheating and
degrade the device performance, even during I-V sweeps. With the development of GaN epitaxy technology, GaN-on-sapphire is being replaced by GaN-on-Si and GaN-on-SiC for HEMTs fabrication.

1.4 GaN Reliability Issues

1.4.1 Hot-electron Effect

One well-known failure mechanism of early GaAs-based devices was hot electron-induced degradation.\textsuperscript{19,32,33} Under higher drain bias, the accelerated electrons gain a great deal of enough energy in the channel and may be trapped one the device surface, in the AlGaN barrier layer or in the GaN buffer layer. This can lead to a shift in threshold voltage, an increase in drain resistance and a reduction in drain saturation current.\textsuperscript{6,34} Hot-electron induced degradation has been observed in AlGaN/GaN HEMTs with SiNx and SiO\textsubscript{2} passivation on sapphire and SiC substrates under dc and rf stress conditions. With high drain bias and high input drive, hot electrons are created in the region between the gate and drain, and generate permanent traps which cause increased surface depletion, increased series resistance, and reduced gate-drain electric field. Not only can hot-electrons be trapped but they can also induce trap formation at surface region between gate and drain. In a 3000-hour test on AlGaN/GaN HEMT under on-state and off-state conditions, a decrease of the drain current and transconductance, and an increase of the channel resistance were observed by Sozza \textit{et al}. Through the use of low frequency techniques, they were able to attribute the increase in traps density at the surface between the gate and drain to hot-electrons present in the channel.\textsuperscript{35} To avoid degradation by hot-electrons caused by the presence of high electric field in the gate-drain region, proper solutions are needed such as by adopting surface passivation and field plate.
To investigate hot-electron effect, electroluminescence (EL) was conducted at different gate and drain voltages. The information of the amount and energetic distribution of hot electrons can be obtained from EL characterization.\textsuperscript{19,36}

**1.4.2 Inverse Piezoelectric Effect**

Recently, another degradation mechanism was proposed by Joh and del Alamo,\textsuperscript{21,37} crystallographic defects formed through inverse piezoelectric effect in GaN-based HEMTs. Due to the lattice mismatch between AlGaN and GaN, there is a great deal of elastic energy stored in AlGaN/GaN heterostructure even in absence of bias. Typically, AlGaN on GaN is under tensile strain.\textsuperscript{38} When tensile mechanical strain was applied on devices intentionally during electrical stress, a 1-3V lower value of critical voltage was found compared to control samples.\textsuperscript{22} In addition, induced piezoelectric strain/stress in gate-drain region under different bias conditions was evaluated by micro-Raman measurement.\textsuperscript{39} During device operation under high drain bias, a large electric field appears around the drain-side of the gate edge across barrier layer. This induces a large amount of mechanical stress, which would trigger the formation of crystallographic defects and relaxation of the strain when the electric field reaches a certain value. Those defects behave as traps, which degrade carrier transport properties and carrier concentration in the channel, resulting in increasing of drain resistance and decreasing of saturation drain current and transconductance. The gate leakage current is increased as well through trap-assisted tunneling in the barrier layer. Cross sectional transmission electron microscope (TEM) results revealed the formation of pits or cracks in the AlGaN barrier layer close to gate edges.\textsuperscript{40} The degree of physical damage was correlated to the reduction in drain current. As confirmed by TEM, higher degradation in drain current, resulted in the creation of more severe physical defects. Energy dispersive X-ray (EDX)
measurement also found that SiNₓ got into formed pits or cracks and oxidation happened during device degradation. Those results also suggested the reduced strain between barrier layer and buffer layer would improve device reliability. InAlN with an In mole fraction of 0.17 can be grown lattice-matched to GaN, which eliminates the strain present in the AlGaN/GaN heterostructure system and should be beneficial to device reliability.\\n\\n### 1.4.3 Trapping Effect

Another important parameter in the evaluation of device reliability is current collapse, the reduction of drain current after the application of high voltage. This is caused by the trapping effect. This effect limits the performance of HEMTs in high power and high frequency applications. The origin of current collapse was attributed to surface trapping, in the AlGaN barrier layer, or buffer trapping, in the GaN buffer layer, leading to an increase in dispersion between direct current (dc) and pulsed current-voltage (I-V) characteristics, and a decrease in maximum transconductance and saturation drain current. Due to the strong polarization of the material, surface states are unavoidable. The donor-like traps capture electrons tunneling from the gate metal and become neutral. Further accumulation of electrons at the surface would make the surface potential negative and form an extended depletion region, a so-called “virtual gate”, which can deplete electrons in the channel, resulting in a reduction in the drain saturation current reduces.

To determine a detailed degradation mechanism, it is very important to understand the trapping behavior, such as the physical locations, energy levels and trapping/detrapping time constants. So far, a great deal of study has been conducted toward the achievement of that goal. Various trap characterization methods, such as
deep-level transient spectroscopy (DLTS),\textsuperscript{46-48} frequency dependent capacitance and conductance measurements,\textsuperscript{49-51} and capacitance-voltage (C-V)\textsuperscript{52,53} measurements were employed to study trapping effects. The activation energies of detected traps are range from 0.07 to 0.84 eV.\textsuperscript{46,49} The time constant varies between an order of microseconds to milli-seconds for fast and slow traps, respectively.\textsuperscript{49,50} According to reports, trap densities are generally around 10^{12} \text{cm}^{-2}\cdot\text{V}^{-1} and corresponding traps are located either in the AlGaN barrier layer or at the AlGaN/GaN interface.\textsuperscript{49-51,53}

It is well known that surface passivation, such as SiNx, is an effective way to reduce trapping effects.\textsuperscript{54-58} In addition, it benefits devices pinch-off characteristics and reduces gate leakage current.\textsuperscript{55} The addition of a SiNx passivation layer to undoped AlGaN/GaN HEMT’s also increases the saturated power density by up to 100\% at 4 GHz and increased the breakdown voltage by an average value of 25\%.\textsuperscript{54} Compared to un-passivated HEMTs which suffer severe $I_D$ collapse (96\%), passivation suppressed more than 80\% of the $I_D$ collapse. As opposed to surface trapping, bulk/buffer trapping actually reduces $I_D$ in the case of SiNx passivated HEMTs.\textsuperscript{58} Possible mechanisms of the suppression of trapping effects by SiNx passivation are 1) passivation prevents the electrons from tunneling from the gate metal reaching surface states 2) Replacement of surface donors by the incorporation of passivation between Si and surface states.\textsuperscript{45}

1.5 Dissertation Outline

This dissertation covers three main topics, including the reliability study of GaN-based high electron mobility transistors (HEMTs), the radiation effects in GaN-based HEMTs and the micromachining of Silicon Carbide (SiC).

Background knowledge on the III-V compound semiconductor transistors, especially, the properties and current status of gallium nitride (GaN) based high electron
mobility transistors, as well as the reliability issues hindering the further development of GaN HEMTs technology are presented in Chapter 1.

The next several chapters cover intensive research studies on the topics of reliability issues of GaN HEMTs outlined in the Chapter 1, which were performed in the past few years at the University of Florida. Chapter 2 discusses the effect of the source field plate on the dc characteristics and reliability of AlGaN/GaN HEMTs under off-state electrical step-stress. Chapter 3 covers the improvement of dc characteristics and reliability under off-state electrical step-stress of AlGaN/GaN HEMTs which were achieved by employing platinum gate metallization. A method to estimate the trap density of AlGaN/GaN HEMTs by temperature dependent sub-threshold slope measurement is presented in the Chapter 4, and the effect of off-state electrical stress on the trap density is studied. In Chapter 5, the passivation properties, including current collapse and rf performance, of HfO₂, SiNₓ and Al₂O₃ on AlGaN/GaN HEMTs are compared. Chapter 6 investigates the effect of buffer structure on the reliability of AlGaN/GaN HEMTs.

Chapter 7 focuses on the radiation effects in the GaN-based HEMTs, which includes the study of the reliability of proton-irradiated InAlN/GaN and the effects of proton energy and dose on the dc characteristics and reliability of AlGaN/GaN HEMTs. Chapter 8 reports the improvement of drilling rate and via holes profile on SiC using ArF excimer laser. Chapter 9 provides a summary and conclusion for all the topics discussed in this dissertation.
Figure 1-1. The variation of the energy bandgap with corresponding lattice constant for the Group III-V.
Figure 1-2. The schematic of a typical AlGaN/GaN HEMT device
Figure 1-3. The conduction band in the AlGaN/GaN heterostructure.
Figure 1-4. The schematic of device operation, A) A fully open channel presents when a positive $V_G$ is applied. B) Conduction band of a HEMT with negative applied $V_G$, but the channel is still open. C) The negative $V_G$ is larger than the threshold voltage $V_{th}$ and the channel is closed.
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CHAPTER 2
THE EFFECTS OF SOURCE FIELD PLATE ON THE CHARACTERISTICS OF OFF-STATE, STEP-STRESSED ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS

2.1 Introduction to Field Plate

The promising performance of AlGaN/GaN high electron mobility transistors (HEMTs) under high frequency and high output power density conditions has intensified efforts to understand reliability and degradation mechanisms under different operating conditions. At high source-drain biases, crystallographic defects and even cracking can occur as a result of the inverse piezoelectric effect. Under these conditions, the presence of strong electrostatic fields in the piezoelectric GaN and AlGaN layers leads to additional mechanical stress that is concentrated in the AlGaN barrier layer. At high enough field, the change in AlGaN elastic energy can produce extended and point defects. The degradation under off-state conditions is electric-field driven, with devices of different gate length failing at different drain-source biases but similar electrostatic field thresholds.

Field plates have been employed for AlGaN/GaN HEMT and GaAs metal semiconductor field effect transistors (MESFETs) to tailor the electric field profile near the drain edge of the gate for enhancing the breakdown voltage and also reducing the effect of current collapse. It is well recognized that the field plate can improve the gate and drain breakdown voltage, which would improve device reliability. Gate field plates and source field plates are the most common types used for power applications. The gate field plate reduces the peak electric field at the edge of the gate on the drain side. However, the gate field plate increases gate-to-drain capacitance, reduces the saturation current and degrades the rf gain characteristics. The source field plate can
increase the gate and drain breakdown voltage and reduce the gate-to-drain capacitance, and thus improve rf performance.\textsuperscript{71}

In this chapter, the degradation of AlGaN/GaN HEMTs with and without source field plate under step-stressing of the gate reverse bias was reported. The devices exhibit several threshold gate biases for the onset of increased gate leakage. The degradation of gate current is irreversible and is accompanied by a small decrease in drain-source current. Transmission electron microscopy (TEM) imaging and small-probe microanalysis were used to examine the degradation occurring at the metal-AlGaN interface.

2.2 Experimental

2.2.1 Material Growth

The HEMT on Si wafers were grown by metal organic chemical vapor deposition (MOCVD) with conventional precursors in a cold-wall, rotating- disc reactor designed from flow dynamic simulations. The growth process was nucleated with an AlN layer to avoid unwanted Ga-Si interactions. The epitaxial stack consisted of a proprietary AlGaN transition layer,\textsuperscript{72,73} \textasciitilde800-nm GaN buffer layer, and 16-nm unintentional-doped Al\textsubscript{0.26}Ga\textsubscript{0.74}N barrier layer. The nominal growth temperature for the GaN buffer and AlGaN barrier layers was 1030\textdegree C.

2.2.2 Material Growth and HEMTs Fabrication

HEMT fabrication began with Ti/Al/Ni/Au Ohmic metallization and rapid thermal annealing in flowing N\textsubscript{2} at approximately 825 \textdegree C. Contact resistance, specific contact resistivity, and specific on-resistance were 0.45 \textOmega-mm, 5\times10^{-6} \textOmega-cm\textsuperscript{2}, and 2.2 \textOmega-mm, respectively. Inter-device isolation was accomplished by use of multiple energy N\textsuperscript{+} implantation to produce significant lattice damage throughout the thickness of the GaN
buffer layer. The ion implantation step maintains a planar geometry in the fabricated device and reduces parasitic leakage paths that may exist in passivated, mesa-isolated HFETs. Immediately following implantation, the wafers were passivated with 70-nm-thick SiNₓ in a PECVD chamber maintained at a base plate temperature of 300℃. Schottky gate definition was achieved by patterning the gate and selectively removing the SiNₓ passivation layer. The contact windows to the Ohmic contact pads were also opened at the same time as defining the Schottky gate. After SiNₓ etching, wider gate patterns were redefined with another photolithography step and contact windows to the Ohmic contact pads were also opened. Ni/Au-based gate metallization was deposited on the gate and Ohmic contact pads simultaneously. The wafers were then passivated with another 400-nm layer of PECVD SiNₓ at 300℃. The contact windows were opened by dry etching. There was an additional metal deposition for the HEMT with the source field plate. The field plate was connected to the source terminal and extended by 1 µm out over the gate to the gate-to-drain region. The source to gate distance and channel length of the HEMTs with and without the source field plate were kept constant at 1 and 4.7 µm, respectively. A schematic of the HEMT with the source field plate, and optical micrographs of the HEMT with and without source field plate, are shown in Figure 2-1.

2.2.3 Electrical Step-stress

The HEMTs were step-stressed biased in the dark at room temperature with up to -90V reverse gate voltage at a fixed source-drain bias of 5V using an HP 4156C semiconductor parameter analyzer. During the stress, the devices were stressed for 60 seconds at each gate voltage step, while grounding the source electrode and maintaining +5 V to the drain. The stress started at the gate voltage of -5 V, and the voltage step was kept at -1 V. During the step-stress, gate-to-source leakage current,
I_{GS}, and gate-to-drain leakage current, I_{GD}, were also measured. Between each step-stress, drain I-V, extrinsic transconductance, gate forward current biased from 0 to 1.5 V and gate reverse current biased from 0 to -5 V, source and drain resistance were recorded. Self-heating effects were negligible based on the low drain-source currents under our test conditions, as supported by thermal simulations.

2.2.4 Device Characterization and Simulation

Cross sections of some devices were prepared for TEM examination using a Nova 200 focused-ion-beam system. Finally, the Atlas code from Silvaco was used to simulate the electric field for HEMTs with and without source field plate.

2.3 Results and Discussion

Figure 2-2 shows the 2D electric-field simulation results of the electric field distribution around the source, gate, and drain contacts for HEMTs with and without source field plate. The simulator is physically-based and involves solution of the drift/diffusion model using Poisson and carrier continuity equations, also taking into account carrier statistics, impact ionization, lifetime, mobility and generation-recombination. There were two peaks of the electric field at the gate edges, and the drain side of the gate edge exhibited the maximum electric field. The source field plate over the gate electrode reduced the peak electric field at the drain side of the gate edge: this would improve the off-state breakdown voltage of the HEMTs. Figure 2-3 shows the drain I-V characteristics of HEMTs with and without source field plate. Both devices revealed similar saturation current and threshold voltage. The device without the source field plate displayed an off-state drain breakdown voltage of 55 V and a significant increase of the breakdown voltage to greater than 150 V was observed, as illustrated in the insert in Figure 2-3.
Figure 2-4 shows the typical step-stress results of more than 30 HEMTs with and without the source field plate; the gate current, $I_G$, has been plotted as a function of the stressed gate voltage. The critical voltage of the off-state step stress was defined as the onset of $I_G$ increase during the stress. It has been reported$^{20}$ that once the gate voltage of the HEMTs reached a critical voltage, a decrease of saturation drain current and an increases of the source and the resistance were observed. Similar results were obtained in this experiment. The typical critical voltages of HEMTs without the source field plate were around -40 V. This value increased to around -65 V for the HEMTs with the source field plate. This increase of the critical voltage for the HEMT with the source field plate was attributed to the reduced electric field on the drain side of the gate edge, consistent with the simulated electric field results.

Above the critical voltage, there were additional increases of $I_G$ observed at high gate bias voltages, as shown in Figure 2-5. The total gate leakage current, $I_G$, is the sum of the gate-to-source leakage current, $I_{GS}$, and gate-to-drain leakage current, $I_{GD}$. The first onset of $I_G$ increase matched with the increase of $I_{GD}$. This result implied that degradation occurred on the gate edge close to the drain side when the gate bias voltage reached the critical value. This degradation phenomenon has been reported previously by several groups.$^{20,21,37,59,60}$ For the second $I_G$ increase, there was no change for $I_{GD}$, but an increase of $I_{GS}$ was observed. The amount of $I_{GS}$ increase corresponded to the increase of $I_G$. Thus, it seems likely that some degradation also occurred on the gate edge close to the source side. There were some occasions when both $I_{GS}$ and $I_{GD}$ increased under high stress bias voltage.
In order to establish whether there were degradations on either the source or drain sides of the gate edge, TEM was used to examine the gate edges. As shown in Figure 2-6A, the metal/semiconductor interface for the unstressed sample was very sharp, and no reactions between the gate metal contact and semiconductor were observed. A small void was present in the Ni, but this was most likely an artifact of the focused ion beam (FIB) milling. For the stressed sample, a notch was observed on both sides of the gate, as shown in Figure 2-6B and C. These defective regions could be the initial stages of cracking due to the inverse piezoelectric effect, as previously reported.19,59,62 Other regions of the stressed sample showed that Ni had interacted with the underlying nitride layer close to the position of an associated threading dislocation (TD), as further illustrated in Figure 2-7.

Electron energy-loss spectroscopy (EELS) line scans were performed across the gate/AlGaN/GaN heterostructure around the area of the diffused gate metal, as shown in Figure 2-8D. Line scan “a” was made vertically across a pristine interface and no metal diffusion was observed. A thin oxide layer was, however, observed at the metal/semiconductor interface and metal/oxide/semiconductor interfaces was very abrupt. The line scan “b” was made vertically across the region of metal diffusion. The dashed lines across Figure 2-8A and B indicate the interface between the original metal and the AlGaN layer. The scans clearly show that both Ni and O were diffused about 3-4 nm into the AlGaN layer at the site of the TD. As shown by the horizontal EELS line scan “c”, Figure 2-8C. It also appears that the Ni had diffused laterally. Such Ni diffusion regions are likely to be additional sources responsible for the observed increase of the gate leakage current.
2.4 Summary

In this chapter, the effect of source field plates on the reliability of AlGaN/GaN HEMTs under off-state stress was present. With the incorporation of the source field plate, critical voltages of ~65 V were achieved as compared with 40V for HEMTs without the source field plate. These results were consistent with electric field simulations and drain I-V characteristics of HEMTs with and without source field plate; slightly lower peak electric field appeared at the gate edges for the HEMTs and significant higher drain breakdown voltage for the HEMTs with the source field plate. The TEM observations revealed that pits attributed to the inverse piezoelectric effect had appeared on both the source and drain sides of the gate edges, and there was a thin oxide layer between the Ni and AlGaN layer. Nickel and oxygen diffusion were associated with a threading dislocation for the stressed HEMT, which would provide additional pathways for the increased gate leakage current.
Figure 2-1. A) Optical micrograph of a typical HEMT with source field plate. B) Optical micrograph of a typical HEMT without source field plate. C) Schematic of HEMT with source field plate.
Figure 2-2. Two-dimensional simulations of the electrostatic field distribution between source and drain contacts for HEMT with and without source field plate.
Figure 2-3. Drain I-V characteristics of HEMT: A) without; and B) with, the source field plate. The $V_G$ starts from 0V and with a step of +0.5V. (Insert) The off-state drain breakdown voltage of HEMTs with and without field plate, which was measured at $V_G = -8V$. 
Figure 2-4. Off-state gate currents as a function of VGS for HEMT with and without source field plate. The devices were stressed for 60 seconds at each gate voltage step, while grounding the source electrode and maintaining +5 V to the drain. The stress started at the gate voltage of -5 V, and the voltage step was kept at -1 V.
Figure 2-5. Off-state total gate current ($I_G$), gate-to-source current ($I_{GS}$) and gate-to-drain current ($I_{GD}$) as a function of $V_{GS}$ for HEMT with source field plate.
Figure 2-6. Cross section TEM micrographs of gate contact of HEMT before stress A), and after stress B) for the edge of the gate close to the source contact, C) edge of the gate close to the drain contact. The two white arrows indicate regions of Ni and oxygen diffusion and an associated threading dislocation.
Figure 2-7. TEM image of the region with Ni and oxygen diffusion and the associated threading dislocation.
Figure 2-8. The results of EELS analysis. A) Relative compositions of Ni, O, and N distributions for a vertical EELS line scan across gate area without degradation, B) relative compositions of Ni, O, and N distributions for a vertical EELS line scan across gate area with Ni and O diffusion. The dashed line across the top-right and bottom-right indicates the original metal and AlGaN interface, C) relative compositions of Ni, O, and N distributions for a horizontal EELS line scan across the gate area with Ni and O diffusion at the diffused gate contacts. D) TEM image of the region with Ni and oxygen diffusion and the associated threading dislocations, with the locations of EELS line scans as marked.
3.1 Overview of Gate Metallization of AlGaN/GaN HEMTs

AlGaN/GaN High-Electron Mobility Transistors (HEMT) exhibit impressive attributes and outstanding high voltage switching and RF power performance. In spite of the extraordinary material properties of the AlGaN/GaN heterostructure system, such as high mobility, high saturation velocity and good thermal conductivity, the main impediment of this technology is lack of reliability. Recently, a number of degradation mechanisms have been proposed. They are hot-electron-induced trap degradation, crystallographic-defect formation through the inverse piezoelectric effect, electric-field driven mechanism under off-state conditions, gate sinking and Ohmic contact degradation. To date, Ni/Au gate metallization has been the most widely used in AlGaN/GaN HEMTs reliability studies.

Pt contacts have shown promising characteristics for Schottky contacts on AlGaN/GaN, with a reported barrier height of 1.09 eV and improved thermal stability. Pt/Ti/Au contacts provide a barrier height of 1.18 ± 0.07 eV on GaN and 2.0 ± 0.1 eV on Al0.31Ga0.69N and exhibit lower leakage current and higher barrier height than that of Ni-based contacts. The presence of an intermediate Ti layer, which attenuates the Au-Pt interaction, further improves the thermal stability of devices. Pt/Ti/Pt/Au Ohmic contacts were used for AlGaAs/GaAs heterojunction bipolar transistors to achieve a lower contact resistance, due to the reaction of GaAs and Pt to form PtAs2. In addition, the control of threshold voltage to fabricate enhancement (E) mode HEMTs has been realized by using buried platinum-gate technology in the InAlAs/InGaAs/InP and AlGaN/GaN systems.
In this chapter, AlGaN/GaN HEMTs with Ni/Au and Pt/Ti/Au gate metallization were fabricated on the same wafer and the drain and gate characteristics with Ni/Au and Pt/Ti/Au gate metallization before and after off-state stress as well the drain current on/off ratio were compared.

3.2 Experimental

3.2.1 Material Growth and HEMTs Fabrication

AlGaN/GaN heterostructures were grown on c-plane sapphire by metal-organic chemical vapor deposition. The epi-layers consisted of a 1 µm thick carbon doped GaN buffer, followed by a 55-nm-thick undoped GaN channel layer, 21 nm Al_{0.25}Ga_{0.75}N, and 2.2 nm GaN cap layer. The HEMT fabrication included Ohmic contact deposition by lift-off of e-beam deposited Ti/Al/Ni/Au, followed by rapid thermal annealing at 850°C for 30 s in N\(_2\). A contact resistance of 0.6 Ω-mm was measured using the transmission line method. For device isolation, multiple doses and energies of N\(^+\) implantation were used to maintain a planar geometry and reduce parasitic leakage current. Shipley Microposit STR-1045 positive photoresist was employed to protect the active region of the devices. Ni (200 Å) /Au (800 Å) and Pt (100 Å) /Ti (200 Å) /Au (800 Å) Schottky gate metallization was defined by optical lithography and followed with standard lift-off of the e-beam deposited metals. The HEMTs were passivated using 400 nm of SiN\(_x\) with a plasma-enhanced chemical vapor deposition (PECVD) system at 300°C. The metal windows were opened with buffered HF.

3.2.2 HEMTs Characterization

The device DC characteristics were measured with a HP 4156 parameter analyzer. The HEMTs off-state step-stresses were performed in the dark at room
temperature with the gate biased up to -100V reverse gate voltage at a fixed source-drain bias of 5V using the parameter analyzer.

3.3 Results and Discussion

Figure 3-1A and B show the off state step-stress results of more than 15 HEMTs with Ni/Au and Pt/Ti/Au gates. The gate current, $I_G$, has been plotted as a function of the stressed gate voltage $V_{GS}$. The Ni/Au gated devices were stressed for 60 seconds at each gate voltage step, while grounding the source electrode and maintaining constant +5 V on the drain. Some of the Pt gated devices were stressed at +5 V on the drain contact, as well as at higher drain voltages of 15 and 20V. The stress started at $V_{GS} = -10$ V, and the voltage step was -1 V. During the step-stress, gate-to-source leakage current, $I_{GS}$, and gate-to-drain leakage current, $I_{GD}$, were also measured. Between each step-stress, drain I-V, extrinsic transconductance, gate forward current biased from 0 to 1.5 V and gate reverse current biased from 0 to -5 V, source and drain resistance were recorded. Self-heating effects were negligible based on the low drain-source currents under our test conditions, as supported by thermal simulations. The critical voltage of the off-state step stress was defined as the onset of $I_G$ increase during the stress. Typical critical voltages for electrical degradation of the Ni/Au get HEMTs ranged from ~45-65 V, as shown in Figure 3-1A. During the off-state stress, the electric field was highest at the gate edges. The presence of a strong electric field in the piezoelectric GaN and AlGaN led to additional mechanical stress concentrated in the AlGaN barrier layer. At a high enough field, the change in AlGaN elastic energy could produce extended and point defects. Thus it was suggested that the critical voltages are strongly dependent on electrical field. However, no such critical voltage was exhibited for Pt-gated devices fabricated on the same wafer, even the gate was biased to -100V. This
implies something else also controlled the onset of the critical voltage. The thermal stability of Pt on GaN has been studied and Pt only reacted with GaN at the ambient temperature >500°C. Besides the electrical field, the thermal stability of the metal contact may play a role to the occurrence of a critical voltage.

However, no such critical voltage was exhibited for Pt-gated devices fabricated on the same wafer, even the gate was biased to -100 V. This implies something else also controlled the onset of the critical voltage. We previously reported that Ni and interfacial oxides diffused into GaN, threading dislocation generated under the gate contact and pits formed on the edges of the gate contacts for the Ni-gated HEMT after reached the critical voltage via a transmission electron microscopy (TEM) study.82 All these defects could contribute the increase of the gate current. X-ray photoelectron Spectroscopy (XPS) was also used to examine the thermal stability of the Ni and Pt metal contacts deposited on GaN.83 Ni reacted with the interfacial oxide for the HEMT sample annealed at 300°C and no chemical interaction between the Pt and GaN. Pt only reacted with GaN at the ambient temperature >500°C.78 Therefore, besides the electrical field, the chemical and thermal stability of the metal contact may play a role to the occurrence of a critical voltage.

During the off-state stress, before the gate bias voltage reaching the critical voltage, there was no degradation for both gate and drain IVs observed. Once the gate voltage of the HEMTs reaching the critical voltage, not only the gate reverse bias leakage current suddenly increased, as illustrated in Figure 3-1A, but also the saturation drain current and the Schottky barrier height were permanently decreased, as shown in Figure 3-2 and Figure 3-3. This degradation was irreversible when the biased gate
voltage passed $V_{cri}$. As illustrated in Figure 3-2, the saturation drain current was reduced ~15% for the Ni/Au gated HEMTs after the stress, with no obvious changes of the drain current for the Pt gated HEMTs. Similar trends were obtained for gate IV characteristics, as shown in Figure 3-3. There were permanent changes of both forward and reverse gate leakage characteristics for Ni/Au gated HEMTs. The Schottky barrier height was reduced from 1.17 to 0.53 V (Figure 3-3A) and the reverse gate leakage increased three orders (Figure 3-3B). By contrast, no changes in gate reverse and forward characteristics were observed for HEMTs with Pt/Ti/Au gates.

Besides the drain and gate IVs, the effects of the off-state stress on the drain sub-threshold characteristics were also investigated. The sub-threshold leakage current, sub-threshold slope and on/off drain current ratio are essential to the power added efficiency, linearity, noise figure and reliability of power amplifiers. Figure 3-4 shows the drain current as a function of the gate voltage for the unstressed A) Ni/Au gated and B) Pt/Ti/Au gate HEMTs biased at different drain voltage. At 10V drain voltage, the subthreshold leakage was ~mid $10^{-6}$ mA/mm for both devices. However, the subthreshold leakage current gradually increased as the drain voltage increased from 10 to 40V for the Ni/Au gated HEMTs. This was due to high reverse bias gate leakage of the Ni/Au HEMTs, as shown in Figure 3-3B. There were minimal changes of the subthreshold leakage current levels for the Pt-gated HEMTs, as shown in Figure 3-4B, consistent with the low reverse bias gate leakage current as illustrated in Figure 3-3B. Higher subthreshold leakage not only degrades the power added efficiency, linearity, noise figure of power amplifiers, it also significantly reduced the drain current on-off ratio of the HEMT. As shown in Table 3-1, the drain current on-off ratio of the Pt-gate
HEMTs stayed fairly constant around $1.5 \times 10^8$ for the HEMTs biased at different drain voltages and this was due to low reverse bias gate leakage. By contrast, the drain current on-off ratio of the Ni/Au-gate HEMTs decreased from $1.16 \times 10^7$ for the drain voltage of 10V to $6.29 \times 10^5$ for the drain voltage of 40V. This was due to higher subthreshold drain leakage and reverse bias gate current. It was reported that the reverse bias gate current directly affected the subthreshold slope. A subthreshold slope of around 65 mV/dec was achieved for the Pt/Ti/Au gated HEMTs, which was very close to the theoretical number of 60 mV/dec, as illustrated in Table 3-1. These results suggest that Pt/Ti/Au gate metallization maintains excellent reliability during the operating condition mentioned above.

**3.4 Summary**

In conclusion, the significant improvement of AlGaN/GaN HEMT stability by using Pt-based gate metallization instead of the conventional Ni/Au was demonstrated. The off-state critical voltage was increased from around 45-65 to >100V, and changes of the drain current, drain current on/off ratio, Schottky barrier height and reverse bias gate leakage were minimized. The reverse bias gate leakage current and the stability between the gate metal contact and semiconductor contribute to the occurrence of a critical voltage, in addition to the electric field.
Figure 3-1. Off-state gate currents as a function of gate voltage for the HEMTs fabricated with different gate metallization, A) Ni/Au or B) Pt/Ti/Au.
Figure 3-2. Drain IVs of HEMTs fabricated with different gate metallization measured before and after the off-state stress. A) Ni/Au and B) Pt/Ti/Au.
Figure 3-3. Schottky gate characteristics of the HEMTs fabricated with different gate metallization measured before and after the off-state stress. A) Ni/Au or B) Pt/Ti/Au
Figure 3-4. Subthreshold drain current of AlGaN/GaN HEMTs fabricated with different metallization biased at different drain voltage. A) Pt/Ti/Au and B) Ni/Au.
Table 3-1. Summary of sub-threshold slope and ON/OFF ratio of AlGaN/GaN HEMTs with Pt/Ti/Au and Ni/Au gate metallization before and after off-state electric step-stress

<table>
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<tr>
<th>$V_{DS}$ (V)</th>
<th>Subthreshold slope (mV/dec)</th>
<th>ON/OFF ratio</th>
<th>Ideality factor</th>
<th>Schottky barrier height (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pt/Ti/Au</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>64.8</td>
<td>$1.56 \times 10^8$</td>
<td>1.61</td>
<td>1.25</td>
</tr>
<tr>
<td>40</td>
<td>65.3</td>
<td>$1.48 \times 10^8$</td>
<td>1.53</td>
<td>1.26</td>
</tr>
<tr>
<td>Ni/Au</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>78.8</td>
<td>$1.16 \times 10^7$</td>
<td>1.72</td>
<td>1.17</td>
</tr>
<tr>
<td>40</td>
<td>99.1</td>
<td>$6.29 \times 10^5$</td>
<td>4.62</td>
<td>0.53</td>
</tr>
</tbody>
</table>
CHAPTER 4
INVESTIGATING THE EFFECT OF OFF-STATE STRESS ON TRAP DENSITIES IN ALGAN/GAN HIGH MOBILITY TRANSISTORS

4.1 Background

The AlGaN/GaN heterostructure system has attracted a great deal of attention for high-power and high frequency applications. However, some undesirable issues induced by electron trapping at surface states of the semiconductor, such as current collapse and gate leakage effects have not been fully understood. Recently, intensive studies have been carried out to understand and eliminate the trapping effects in AlGaN/GaN high electron mobility transistors (HEMTs). Several different techniques have been utilized, including current-mode deep level transient spectroscopy (DLTS), conductance deep level transient spectroscopy (CDLTS), transient drain current, gate leakage current and threshold voltage measurements at different temperatures as well as frequency dispersion in capacitance and conductance analysis. To date, a number of different trap levels have been reported, such as 70 meV, 0.37 eV and 0.06 eV for donor-like states related to N vacancies in AlGaN/GaN heterostructures, while hole-like traps with activation energies of 0.4 and 0.84 eV were also detected. The estimated trap density by the means of capacitance-voltage (C-V) technique was $1.34 \times 10^{12} /\text{cm}^2$-eV at the pinch-off voltage, and from bias dependent C-V data, the values of $D_t$ ranged from $10^{11}$ to $5 \times 10^{12} /\text{cm}^2$-eV. The density of trap states evaluated on the HFETs was $2.5-10 \times 10^{12} /\text{cm}^2$-eV by frequency dependent capacitance and conductance analysis. However, the investigation of trap states on both fresh and stressed AlGaN/GaN HEMTs has not been reported in detail.

In this chapter, temperature dependent sub-threshold slope measurements of AlGaN/GaN HEMTs in the temperature range from 300 to 573K have been performed.
The increasing of sub-threshold slope at elevated temperatures reveals two trap densities, which are attributed to traps located at the interface between the barrier layer and bulk layer or inside GaN bulk layer, as well as the increase in trap densities after electrical stressing.

4.2 Experimental

The HEMT device structures were grown on semi-insulating 6H-SiC substrates and consisted of a thin AlN nucleation layer, 2.25 µm of Fe-doped GaN buffer, 15 nm of Al$\text{O}_{0.28}\text{Ga}_{0.72}$N, and a 3 nm undoped GaN cap. On-wafer Hall measurements showed sheet carrier concentrations of $1.06 \times 10^{13}$ cm$^{-2}$, mobility of 1907 cm$^2$/V-s, and sheet resistivity of 310 Ω/□. The HEMTs employed dry etched mesa isolation, Ti/Al/Ni/Au Ohmic contacts alloyed at 850°C (contact resistance of 0.3 Ω•mm), and dual-finger Ni/Au gates patterned by lift-off. The gate length was 1µm, and gate width was 2×150 µm. Both source-to-gate gap and gate-to-drain distances were 2 µm. The devices exhibited typical maximum drain currents of 1.1 A/mm, extrinsic transconductance of 250 mS/mm at V$_{DS}$ of 10 V, threshold voltage of -3.6 V. An automated temperature control chuck from Wentworth was used to perform temperature dependent measurements. The base temperature was varied from room temperature to 300°C and held constant during the measurement. The device DC characteristics were measured with a HP 4156 parameter analyzer.

4.3 Results and Discussion

Figure 4-1A shows the room temperature drain and gate current currents as a function of the gate voltage for HEMTs prior to and after off-state drain voltage step-stress at a constant gate bias voltage of -8 V. Figure 4-1B shows the room temperature gate currents, I$_G$, during the drain voltage step-stress with a constant gate voltage of -
8V. The stress conditions were set for holding 60 seconds at each drain voltage step, while grounding the source electrode and maintaining constant -8 V on the gate. The stress started at $V_{DS} = +5$ V, and the voltage step was +1 V. During the step-stress, gate-to-source leakage current, $I_{GS}$, and gate-to-drain leakage current, $I_{GD}$, were also measured. Between each step-stress, drain I-V, extrinsic transconductance, gate forward current biased from 0 to 1.5 V and gate reverse current biased from 0 to -5 V, source and drain resistance were also recorded. The critical voltage, $V_{cri}$, of the off-state step stress was defined as the onset of a sudden $I_G$ increase during the stress. During the off-state stress, once the drain bias voltage reached $V_{cri}$, not only did the gate leakage current suddenly increase, as in Figure 4-1B, but also the saturation drain current decreased, as previously reported. These permanent changes corresponded with pits formed along the edges of the gate electrode and/or gate metal diffusion.

Table 4-1 shows the summary of sub-threshold drain leakage current, the drain current on-off ratio and the slope of the sub-threshold drain current before and after the off-state stress at room temperature. Once the drain bias voltage reached $V_{cri}$, the drain current on-off ratio considerably decreased from $3.8 \times 10^5$ to $5.6 \times 10^3$. The drain current on-off ratio reduction degrades the charge modulation in the two dimensional electron gas channel as well as the power added efficiency, linearity, noise figure and reliability of power amplifiers. Both sub-threshold drain leakage current and the slope of sub-threshold drain current were dominated by gate leakage current. As illustrated in Figure 4-1A, sub-threshold drain leakage current and reverse bias gate leakage current displayed two order increases at $V_G = -4$V after the HEMTs were stressed. The sub-threshold drain leakage current was dominated by the reverse bias gate leakage.
current. As shown in Figure 4-1B, the magnitude of the threshold drain leakage current was equal to the reverse bias gate leakage current. The slope of sub-threshold drain current was reported to be highly dependent on the reverse-bias gate leakage current. The sub-threshold slope almost doubled and increased from 98 to 158 mV/dec after the stress. The drain current sub-threshold slope, S, has also been used to quantify trap densities in the gate modulated region of metal oxide semiconductor field effect transistors (MOSFETs) and AlGaN/GaN HEMTs.

The interface trap density can be extracted from the change of S with temperature. By analogy with Si MOSFETs and treating the AlGaN as the dielectric layer, the equations for trap density are given by:

\[
\frac{\partial S}{\partial T} = \frac{k}{q} \ln(10)(1 + \zeta), \quad \zeta = \frac{C_{it}}{C_{AlGaN}}
\]

(4-1)

\[
D_{it} = \frac{C_{it}}{q}
\]

(4-2)

where T is the temperature, k is Boltzmann’s constant, q is the electron charge, ln is the natural logarithmic symbol, \( \zeta \) is the ratio of capacitance associated with the interface traps and AlGaN layer capacitance, \( C_{AlGaN} \), and \( D_{it} \) is the interface trap density. The trap densities were extracted from the slope of S v.s. T plot, as shown in Figure 4-2. These temperature dependent behaviors of trap densities and gate leakage current in AlGaN/GaN heterostructures were attributed to surface hopping conduction through the traps. As illustrated in Figure 4-2, there was a transition temperature at 500K and two trap densities \( (D_{it-1} \text{ and } D_{it-2}) \) were identified for both reference and stressed devices in the temperature ranges of 300-500K and 500-573K, respectively, based on drain current sub-threshold slopes measured at different temperatures. The estimated
interface trap densities, $D_{it-1}$ and $D_{it-2}$, were $1.6 \pm 0.3 \times 10^{12}$ and $8.1 \pm 0.3 \times 10^{12}$ /cm$^2$-eV for the reference HEMTs, and $3.3 \pm 0.1 \times 10^{12}$ and $9.2 \pm 0.5 \times 10^{12}$ /cm$^2$-eV for the stressed devices, respectively. The increases of trap densities for the stressed HEMTs as compared to the reference samples were due to additional traps generated during the stress providing paths for the gate leakage current, such as dislocation generation, gate metal diffusion, interface oxide intermixing with the semiconductor, and/or notch formation around the gate edges. For the reference HEMTs, the increase of trap densities at higher temperature could be due to other deep traps being activated at the elevated temperatures, creating leakage current paths.

We also noticed that the sub-threshold drain leakage current and reverse bias gate leakage current for the reference HEMT measured at the temperatures above 493K were quite different from the ones measured at room temperature. Figure 4-3 shows the sub-threshold drain leakage current and reverse bias gate leakage current of the reference HEMT measured at 300 and 573K. The sub-threshold drain leakage currents were actually higher than the reverse bias gate leakage current for the reference HEMTs. Thus besides the reverse bias gate leakage current, there were other leakage current paths involved in the increase of the sub-threshold drain leakage currents, which would be the main cause for the increase of the sub-threshold slope and the trap density level from $D_{it-1}$ to $D_{it-2}$. Table 4-2 lists the summary of dc characteristics of the reference and stressed HEMTs measured at room temperature and 573K. The saturation drain current, extrinsic transconductance, and drain current on-off ratio measured at 573K decreased for both reference and stressed HEMTs as compared to the room temperature results. However, there was also a noticeable increase in device
isolation current for the HEMTs measured at 573K using device isolation testers. Since
the source, drain and gate contact pads of the HEMTs were connected through the
active area of the device, the isolation current between the contact pads of the device
could not be directly measured. An isolation tester with two 100 µm × 100 µm Ohmic
pads separated by 15 µm isolated gap using ICP etching was used to examine the
isolation current. Since the size of the contact pads was much smaller that the
dimension of the source, drain and gate contact pads, the isolation current from the real
device should be larger than that of the isolation testers. As shown in Figure 4-4, the
device isolation current increased proportional to the temperature. Below the 493K, the
isolation leakage was less than 0.5 µA and the isolation leakage currents were lower
than the gate leakage current. Thus, there was no impact observed on the sub-
threshold drain leakage. Once the measurement temperature was above 493K, the
device isolation currents were comparable to the gate leakage current. For the
reference HEMTs, at the higher measurement temperatures (>493K), the device
isolation currents dominated the leakage currents of the device and the deep traps
induced by the ion bombardment during the ICP device isolation etching were activated.
Thus, the deep traps created during the mesa isolation etching were the main cause of
the increase of the trap densities from $D_{it-1}$ to $D_{it-2}$ for the reference HEMTs. Proper
thermal annealing after the ICP etching or employing ion implantation-based device
isolation process should reduce the trap density $D_{it-2}$. For the stressed HEMTs, the
reverse bias gate leakage current was only slightly lower than that of the sub-threshold
drain leakage current. Therefore, both traps created during the stress and those
activated at the high temperature played a role in the increase of trap densities.
The effect of drain bias voltage on the trap densities was also investigated. The devices were biased at drain bias voltages of 0.1, 2.5, 5 and 10V. Figure 4-5A shows the trap densities as a function of drain bias voltage. Both the $D_{it-1}$ and $D_{it-2}$ increased with drain voltage, but $D_{it-1}$ was less sensitive to drain bias voltage. At higher drain bias voltage, the maximum electric field on the gate edge close to the drain electrode increased, thus more hot electrons were generated and more traps created. Figure 4-5B shows the device isolation current as a function of the drain bias voltage and temperature. At higher bias voltage or higher temperature the isolation leakage current increased significantly. Therefore $D_{it-2}$ was more sensitive to the drain bias voltage.

4.4 Summary

In conclusion, temperature-dependent sub-threshold slope analyses were performed in order to investigate the trapping effects in AlGaN/GaN high electron mobility transistors (HEMTs). The sub-threshold slope increased with temperature ranging from room temperature to 573K, there are two trap densities of $1.6 \pm 0.3 \times 10^{12}$ and $8.1 \pm 0.3 \times 10^{12}$ /cm$^2$-eV for the reference HEMTs and $3.3 \pm 0.1 \times 10^{12}$ and $9.2 \pm 0.5 \times 10^{12}$ /cm$^2$-eV for the stressed HEMTs, respectively.
Figure 4-1. DC characteristics and electrical stress data. A) Sub-threshold drain current and reverse bias gate leakage before and after the off-state drain bias voltage step-stress. B) Gate currents as a function of step-drain voltage during the off-state stress.
Figure 4-2. Slope of sub-threshold drain current of the AlGaN/GaN HEMTs before and after off-state drain bias voltage step-stress as a function of the ambient temperature.
Figure 4-3. Sub-threshold drain leakage current and reverse bias gate leakage current for reference HEMT measured at the temperatures of 300 and 573K.
Figure 4-4. Device isolation current at a drain bias voltage of 10V and the gate leakage current at a gate voltage of -10V.
Figure 4-5. The results of trap characteristics and device isolation current. A) Trap densities of the HEMTs before and after the off-state stress as a function of the drain bias voltage. B) Device isolation current as a function of drain bias voltage at different temperatures.
Table 4-1. Sub-threshold drain leakage current, the slope of the sub-threshold drain current and drain current on/off ratio of the HEMTs before and after the off-state drain voltage step-stress

<table>
<thead>
<tr>
<th>Sample</th>
<th>Sub-threshold drain leakage current (µA)</th>
<th>Sub-threshold slope (mV/dec)</th>
<th>ON/OFF ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference</td>
<td>0.58</td>
<td>98</td>
<td>$3.8 \times 10^5$</td>
</tr>
<tr>
<td>Stressed</td>
<td>37.2</td>
<td>158</td>
<td>$5.6 \times 10^3$</td>
</tr>
</tbody>
</table>

Table 4-2. Room and higher Temperature drain saturation current, maximum gm, drain current ON/OFF ratio, isolation current at 10V for both reference and stressed samples

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Saturation current (mA)</th>
<th>Maximum Gm (mS/mm)</th>
<th>ON/OFF ratio</th>
<th>Isolation current on isolation pads V=10V</th>
</tr>
</thead>
<tbody>
<tr>
<td>R. T.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ref.</td>
<td>220</td>
<td>72</td>
<td>$3.8 \times 10^5$</td>
<td>2.6 nA</td>
</tr>
<tr>
<td>Stressed</td>
<td>210</td>
<td>65</td>
<td>$5.6 \times 10^3$</td>
<td>3.0 nA</td>
</tr>
<tr>
<td>573 K</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ref.</td>
<td>110</td>
<td>42</td>
<td>$2.5 \times 10^4$</td>
<td>2.6 µA</td>
</tr>
<tr>
<td>Stressed</td>
<td>94</td>
<td>37</td>
<td>$1.5 \times 10^3$</td>
<td>2.7 µA</td>
</tr>
</tbody>
</table>
CHAPTER 5
COMPARISON OF PASSIVATION LAYERS FOR AlGaN/GaN HIGH MOBILITY TRANSISTORS

5.1 Background

Remarkable progress has been made in recent years in high performance AlGaN/GaN high electron mobility transistors (HEMTs) grown on a variety of substrates, including sapphire, SiC and Si. Polarization effects in these structures lead to surface states that can have a significant detrimental impact on device performance. Unless steps are taken to passivate the device, positively charged surface donor states can trap negative charge and lead to the presence of a virtual gate that depletes the 2-dimensional electron gas (2DEG) of carriers, reducing drain current and power performance. The most commonly used passivation layer is SiNx. Such layers are typically deposited by plasma enhanced chemical vapor deposition (PECVD) at temperatures near 300°C. The use of SiNx passivation typically restores 70-80% of the dc current as measured by gate lag measurements. Other dielectric passivation layers such as MgO or Sc2O3 deposited by plasma-assisted Molecular Beam Epitaxy (MBE) can provide even higher levels of current recovery under optimum conditions, but these are difficult to integrate into the device processing sequence. The SiNx layer can also be used to define the T-gate contact in a nitride-first process which has both advantages and disadvantages at the device level. The overlap of gate metallization onto the surface of the SiNx can be employed to create a gate field plate and thereby reduce the peak electric field in the semiconductor, increasing the reverse breakdown voltage. However, the high-k SiNx surrounding the gate also leads to parasitic loading and increases the fringing capacitance, degrading the rf performance.
Bilayer dielectric films consisting of thin SiN$_x$ and an overlayer of a lower
dielectric constant material such as SiO$_2$ have also shown good results.\textsuperscript{117} For
aggressively scaled HEMTs with gate length <100nm, the aspect ratio of SiN$_x$ thickness
to gate length may complicate accurate pattern transfer required for gate length
definition when also used as the gate dielectric.\textsuperscript{118} For such devices, it is advantageous
to make the dielectric very thin. For deposition of thin passivant films, atomic layer
deposition (ALD) has received considerable recent attention. Many high-k passivant
films can be optimized as surface passivation and for use as gate insulators for high
frequency GaN MOS-HEMTs, leading to reduced gate leakage current relative to
traditional Schottky gate HEMTs. In some cases, multi layer passivation structures have
been effective (eg. Al$_2$O$_3$+SiN$_x$),\textsuperscript{119-122} although these add to the process complexity.
Other approaches include AlN films as passivant / gate dielectric and heat spreading
layer.\textsuperscript{119,120}

In view of this past work, it is of interest to compare the passivation properties on
AlGaN/GaN HEMTs of simple, single, thin layers of common oxides (HfO$_2$ and Al$_2$O$_3$)
deposited by ALD with conventional thick SiN$_x$ layers. We find the oxides are not as
effective in passivating the surface states that cause current collapse for this particular
AlGaN/GaN epitaxial structure, but they do create less degradation of rf properties.

5.2 Experimental

The AlGaN/GaN HEMTs were fabricated on 6H SiC semi-insulating substrate,
with the following sequence of epitaxial layers: an AlN nucleation layer, a 1.8 $\mu$m GaN
buffer layer, a 1nm In$_{0.10}$Ga$_{0.90}$N backbarrier, a 15nm GaN channel and a top 22nm
Al$_{0.26}$Ga$_{0.74}$N barrier. On-wafer Hall measurements showed a sheet carrier
concentration, sheet resistance, and mobility of $9.1 \times 10^{12}$ cm$^{-2}$, 410 Ohms/square, and
1670 cm²/V.s, respectively. An inductively coupled plasma mesa etch of ~1000 Å was performed to isolate adjacent devices. Ti/Al/Ni/Au ohmic metallization was annealed at 850°C for 30 sec for source/drain contacts, producing a specific contact resistance of 0.4 Ohm.mm. The HEMTs employed a Ni/Au double gate, π -design with a gate length of 0.2µm and width of 150µm, source-to-gate and gate-to-drain distances of 1 µm. Some control devices were left unpassivated, while others were passivated with either 200 nm of SiNₓ deposited by a Plasma Therm 790 PECVD system or 7.5 nm of HfO₂ or Al₂O₃ deposited by an atomic layer deposition system (Cambridge NanoTech, Inc, Fiji F200). The passivation thicknesses were chosen as being close to standard for the particular deposition process. Standard solvent precleans were done prior to passivation deposition. The passivation thicknesses and their dielectric constants had no measurable effect on the device parameters at these gate lengths. The dc characteristics of the HEMTs were measured with a Tektronix curve tracer 370A and an HP 4156 parameter analyzer. The RF performance of the HEMTs was characterized with an HP 8723C network analyzer. Wafer-scale maps of typical RF (f₁) and dc (threshold voltage, V₉₃) performance are shown in Figure 5-1 for the unpassivated devices.

### 5.3 Results and Discussion

Figure 5-2A shows the gate current-voltage (I-V) characteristics from the devices without passivation and those with the three different passivation layers investigated. The extracted ideality factors on the unpassivated devices were un-physically large (>5 when assuming thermionic emission as the dominant conduction mechanism). Clearly there are multiple mechanisms present, such as tunneling and recombination. The passivated devices showed ideality factors of ~2 in all cases, indicative of recombination
as the dominant transport mechanism in the heterojunctions. The SiNx passivated samples exhibited the highest reverse-bias gate leakage current, although past reports have shown this to be highly dependent on the deposition conditions.\textsuperscript{123-125} The use of ALD Al\textsubscript{2}O\textsubscript{3} has been shown to reduce the gate leakage current.\textsuperscript{125} As shown in Figure 5-2A, both Al\textsubscript{2}O\textsubscript{3} and HfO\textsubscript{2} passivation layers effectively reduced the gate leakage current. The sub-threshold leakage current for unpassivated and passivated devices is shown in the I\textsubscript{DS}-V\textsubscript{G} plots of Figure 5-2B. All the passivation layers lead to a more negative threshold voltage, consistent with less depletion under the gate contact. Similarly, the transconductance and drain current of the passivated devices was higher, as shown in the transfer characteristics of Figure 5-2C.

Typical I\textsubscript{DS}-V\textsubscript{DS} characteristics are shown in Figure 5-3 for the unpassivated device (a) and for one passivated with SiN\textsubscript{x} (b). Fairly similar results were obtained with all the different passivation layers, namely, the drain-source current increased as was observed from the transfer characteristics and there were no kinks or other irregularities introduced that would suggest additional traps being introduced by the deposition process for these passivation films.

Figure 5-4 summarizes the effect of the passivation layers on threshold voltage, V\textsubscript{th}, (a), unity current gain frequency, f\textsubscript{T}, (b) and maximum frequency of oscillation, f\textsubscript{MAX}, (c). There is a larger negative shift in threshold voltage with SiN\textsubscript{x} which suggests it is more effective in reducing the surface depletion. However, the thin oxide films show the best improvement in RF characteristics due to their lower overall capacitance relative to the thick SiN\textsubscript{x}.
We have employed gate lag measurements on the HEMTs as a metric for establishing the effectiveness of the dielectric passivation.\textsuperscript{126} In this method, the drain current ($I_{DS}$) response to a pulsed gate-source voltage ($V_G$) is measured. Figure 5-5 shows the normalized $I_{DS}$ as a function of drain-source voltage ($V_{DS}$) for both dc and pulsed measurements. In this drain pulse data, $V_G$ was 0V, while the measurements used different frequencies and 10\% duty cycle. Data is shown for the unpassivated HEMT (a), for HfO$_2$ (b), and SiN$_X$ (c) passivants. The large differences between dc and pulsed drain currents for the unpassivated HEMT are consistent with the presence of surface traps that deplete the channel in the access regions between the gate and drain contacts. After nitride or oxide deposition, the HEMTs showed an increase in drain-source current in the dc mode which is consistent with passivation of surface states. The percentage reductions in drain current at 3V drain-source voltage are shown in Table 5-1. The SiN$_X$ is the most effective at minimizing the trapping evident from the drain pulse measurements and is due to an increase in positive charge at the passivation layer/AlGaN interface, resulting in an increase in effective sheet carrier density in the channel.

Figure 5-6 shows the corresponding gate-lag measurements, with a marked improvement in drain current response for the passivated devices relative to the unpassivated device. This is clear evidence for the assumption that surface states are the cause of the gate-lag phenomena and also that passivation layers mitigate this problem. Once again, the SiN$_X$ is the most effective at reducing the effect of the surface traps.
We also used double pulse measurements, in which $V_{DS}$ was pulsed from 10V to 5V, while $V_G$ was simultaneously pulsed from -6V to 1 V in steps of 1V, at 10% duty cycle.\cite{127,128} Usually, the drain current at gate bias voltages close to the threshold voltage would not decrease during the gate pulse measurement, as shown in Figure 5-6. This is due to an insufficient population of hot electrons being generated at these conditions (5 V of drain bias voltage and gate voltage pulsed from the pinch off voltage to 1-1.5 V above the threshold voltage). However, during the double pulse measurement, the hot electrons can be generated by the electrons in the gate leakage current being accelerated by the higher field present between the 10 V of drain bias voltage and -6 V of gate voltage during the off state. Thus, enough hot electrons are injected into the surface between the gate and drain electrode and create a virtual gate in this region, suppressing the drain current. The resulting data is shown in Figure 5-7 for unpassivated HEMTs (a) and devices with HfO$_2$ (b) or SiN$_X$ (c) passivation. These pulsing conditions led to there being no current in the unpassivated device, while those with surface passivation showed various degrees of recovery. The double pulse measurement is a valuable method for examining the effectiveness of the device passivation and SiN$_X$ was once again the best choice under dc conditions.

5.4 Summary

Alternatives to the usual thick SiN$_X$ passivation films on AlGaN/GaN HEMTs were examined. Both HfO$_2$ and Al$_2$O$_3$ thin films deposited by ALD produce improvements in drain-source current due to a reduction of surface depletion effects but are less effective than SiN$_X$ for the given AlGaN/GaN epi structure. However, the oxides produce superior RF performance to SiN$_X$ and should offer advantages with respect to gate definition because of their reduced aspect ratios.
Figure 5-1. Wafer scale maps for unpassivated HEMTs. A) $f_T$ and B) $V_{th}$. 
Figure 5-2. DC characteristics of unpassivated and passivated HEMTs. A) Gate I-V, B) $I_{DS}-V_G$ and C) transfer characteristics.
Figure 5-3. $I_{DS}$-$V_{DS}$ characteristics of unpassivated and passivated devices. A) the unpassivated device and B) for one passivated with SiN$_x$. 
Figure 5-4. DC and RF characteristics of HEMTs with different passivation layers. A) Threshold voltage, B) unity current gain frequency, $f_T$ and C) maximum frequency of oscillation, $f_{\text{MAX}}$, as a function of type of passivation film.
Figure 5-5. Drain pulse measurements on unpassivated and passivated AlGaN/GaN HEMTs. A) unpassivated, B) HfO$_2$ passivated and C) SiN$_x$ passivated AlGaN/GaN HEMTs. $V_G$ is 0V at a 10% duty cycle.
Figure 5-6. Gate pulse measurements on unpassivated and passivated AlGaN/GaN HEMTs. A) unpassivated, B) HfO₂ passivated and C) SiNx passivated AlGaN/GaN HEMTs. V_G is switched from -5V to the value shown on the X-axis at a 10% duty cycle.
Figure 5-7. Double pulse measurements with drain pulsed from 10V to 5V while simultaneously pulsing the gate from -6V to the value shown on the x-axis. The plots are for A) unpassivated, B) HfO$_2$ passivated and C) SiN$_x$ passivated AlGaN/GaN HEMTs.
Table 5-1. Summary of dc characteristics of unpassivated and passivated HEMTs. The percentage current losses were calculated from the 500 kHz data.

<table>
<thead>
<tr>
<th>Passivation Layer</th>
<th>Dielectric Constant</th>
<th>Ideality Factor</th>
<th>% current loss drain pulse</th>
<th>% current loss gate pulse</th>
<th>% current loss double pulse</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>1</td>
<td>~5</td>
<td>18</td>
<td>36</td>
<td>100</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>~9</td>
<td>~2</td>
<td>10</td>
<td>26</td>
<td>57</td>
</tr>
<tr>
<td>HfO₂</td>
<td>20-25</td>
<td>~2</td>
<td>5</td>
<td>23</td>
<td>57</td>
</tr>
<tr>
<td>SiNₓ</td>
<td>6-10, 7.5 for ideal value</td>
<td>~2</td>
<td>0</td>
<td>21</td>
<td>21</td>
</tr>
</tbody>
</table>
CHAPTER 6
EFFECT OF BUFFER DESIGN ON THE RELIABILITY OF ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS

6.1 Background

There are increasing needs for high power, high efficiency and linearity amplifiers for communication systems and radars for defense applications. Gallium Nitride (GaN) based High Electron Mobility Transistors (HEMTs) are the basis for the next generation of power transistor technology and have exhibited impressive attributes, such as high mobility, high saturation velocity and power density for high voltage and high switching frequency applications. As a result of the large conduction band discontinuity between Al$_{0.25}$GaN (~4.2 eV) and GaN (3.4 eV), both high electron mobility and high electron saturation velocity have been demonstrated in the AlGaN/GaN material system, with values of over 1500 cm$^2$/V-s and 2.5×10$^7$ cm/s, respectively. These parameters are beneficial for high frequency operation. The presence of both a strong piezoelectric effect and spontaneous polarization in III-nitrides lead to a high carrier concentration (> 10$^{13}$ cm$^{-2}$), and in consequence a high current density can be achieved in AlGaN/GaN heterostructures without conventional doping. Moreover, GaN has a large band gap and consequent high breakdown electric field (~3 MV/cm), which make it capable of handling high voltages. These merits of high current density and high breakdown voltage enable this material to be an excellent candidate for high power applications.

Silicon carbide (SiC), sapphire and free-standing GaN are the most widely used substrates for GaN HEMTs epitaxy. SiC is a good candidate due to its high thermal conductivity. Sapphire substrates have lower cost, but their low thermal conductivity
limits their applications for power transistors. Free-standing GaN technology is still evolving. During heteroepitaxy, impurities are introduced at the growth interface and may cause leakage paths, which degrades on/off ratio and off-state breakdown voltage.\textsuperscript{131,132} Several solutions have been developed to reduce buffer leakage, such as deliberate introduction of deep-level impurities, Fe or C, into the GaN buffer\textsuperscript{133,134} and also different epitaxial structure designs.\textsuperscript{135-137} The dislocation densities due to lattice mismatch between GaN and commonly used SiC or sapphire substrates are on the order of $10^8$ - $10^9$ cm\textsuperscript{-2}, and this generally reduces with GaN buffer thickness. As reported by Hinoki \textit{et al.}\textsuperscript{138,139} the off-state breakdown voltage increased and leakage current decreased with increasing thickness of the GaN buffer layer. It was reported that higher densities of edge-type dislocations contributed to the improvement of breakdown voltage.\textsuperscript{136} It was reported that UV-induced electron detrapping increased the peak electric field around gate edges, resulting in a lower critical voltage, and also suggested that an increased number of traps might improve HEMTs’ reliability.\textsuperscript{140} Ivo and co-workers also studied the effect of buffer designs on the reliability of AlGaN/GaN HEMTs by electroluminescence (EL) and electrical measurements, which indicated that higher robustness could be achieved when Al\textsubscript{0.05}GaN-barrier layers were used.\textsuperscript{141}

In this chapter, the reliability of AlGaN/GaN HEMTs fabricated on SiC substrates with different buffer structures was compared. Thick GaN (2 μm), thin GaN (1 μm) and composite AlGaN/GaN buffers were used in this work. The effect of various buffer structures on device reliability, isolation breakdown voltage and off-state drain breakdown voltage are reported.
6.2 Experimental

AlGaN/GaN HEMTs were grown by Metal Organic Chemical Vapor Deposition (MOCVD) on SiC substrates. The buffer structure was varied while the active layers of the HEMTs were kept the same. The buffers consisted of either 1 or 2 μm of GaN, or a composite structure of 0.2 μm AlGaN/0.8 μm GaN. For composite buffer structure, the growth of AlGaN was followed by GaN. This was followed by a 55nm thick GaN channel, 21nm of Al$_{0.25}$Ga$_{0.75}$N and finally a 2.5nm GaN cap, as shown in Figure 6-1. The nominal growth temperature for the GaN buffer and AlGaN barrier layers was 1030°C. Transistor fabrication began with deposition and patterning of Ti/Al/Ni/Au Ohmic metallization and subsequent RTA in flowing N$_2$ at 850°C. The contact resistance, specific contact resistivity, and sheet resistance were extracted from transmission line measurements (TLM) using 100 × 100 μm$^2$ pads separated by 5, 10, 20, 40 and 80 μm, respectively. Device isolation was accomplished by multiple energy N$^+$ implantation. Schottky contacts were formed by deposition of 1000 Å Ni/Au gates. DC current-voltage (I-V) characteristics were recorded using a HP4156C parameter analyzer.

6.3 Results and Discussion

Figure 6-2 shows the typical transfer characteristics of HEMTs fabricated on different buffer layers, measured at $V_{DS} = +5V$. The drain current at $V_G = 1.5V$ was similar for all types of devices. The threshold voltage of HEMTs fabricated on 1 μm GaN buffer layer was more negative than those with the other buffer designs, while the transconductance peak of the former was higher than others. As illustrated in Figure 6-3, the drain and gate currents as a function of gate voltage for HEMTs fabricated on
different buffer layers were measured at \( V_{DS} = +5V \). Sub-threshold drain leakage current was dominated by reverse gate leakage current with the channel off.

Both sub-threshold drain leakage current and reverse gate leakage current were very similar for all HEMTs with the various buffer designs. Drain current-voltage (I-V) characteristics of AlGaN/GaN HEMTs fabricated on different types of structures are shown in Figure 6-4, which were recorded with \( V_{DS} \) from 0 to 5V and \( V_G \) starting from +1V with a step of -1V. The saturation drain current of HEMTs with thick GaN and composite buffers were around 5-8 % higher than HEMTs with 1 \( \mu \)m GaN buffers.

Figure 6-5 shows gate I-V characteristics of HEMTs fabricated on different buffer structures. No apparent difference of gate I-Vs was observed, the extracted Schottky barrier height (SBH) and ideality factor of HEMTs with thick GaN and composite buffer structures were 1.28 V and 1.85, while they were 1.36 V and 1.61 with the thin GaN buffer layer. The effective barrier heights and ideality were obtained from the relationship as shown in Equation 6-1.

\[
J = A^{**}T^2 \exp\left(\frac{e\Phi_B}{K_B T}\right) \left[ \frac{eV}{nK_B T} - 1 \right]
\]  

(6-1)

Where \( A^{**} \), the Richardson constant, is 29.2 A/cm²-K² for n-GaN, \( J \) the current density, \( T \) the measured temperature, \( \Phi_B \) the barrier height, \( n \) the ideality factor and \( K_B \) is Boltzmann’s constant.

Off-state drain electrical step-stress was employed to evaluate the reliability of HEMTs fabricated on the various buffer layers.²¹ Figure 6-6 shows the gate current during electrical step-stressing. The gate current, \( I_G \), was plotted as a function of stressed drain voltage. Each drain voltage step was constant for 60 seconds, while grounding the source electrode and fixing gate voltage at -6V. The stress started at 5 V
of drain voltage and the voltage step was kept at 1 V. During the step-stress, besides monitoring \( I_G \), gate-to-source leakage current, \( I_{GS} \), and gate-to-drain leakage current, \( I_{GD} \), were also measured. Due to the low drain-to-source current during off-state, self-heating effects were negligible and had no effect on device performance. In the early stage of electrical stress, all \( I_G \) curves almost overlapped, since they were dominated by the reverse gate current (Figure 6-5). The critical voltage, \( V_{cri} \), of the off-state step stress was defined as the onset of a sudden \( I_G \) increase during the stress. As shown in Figure 6-6, once reaching the critical voltage, besides the increase of gate current, drain saturation current was also decreased significantly. This was due to permanent damages formed around the gate electrode. Cracks appeared on both the source and drain sides of the gate edges.\(^{82}\) Diffusions of nickel gate contact and native oxygen layer at metal/AlGaN interface occurred and threading dislocations provided additional pathways for the increased gate leakage current.\(^ {142}\) The \( V_{cri} \) for HEMTs fabricated on 2 \( \mu m \) GaN, 1 \( \mu m \) GaN and composite AlGaN/GaN buffers were 30-50V, 70-90V and 65-80V, respectively. The devices with thicker GaN buffer layers showed a lower critical voltage. Between each step stress, saturation drain I-Vs of the HEMTs with different buffer layer were recorded, as shown in Figure 6-7. Since the unpassivated HEMTs were intentionally employed for this study to compare the effect of buffer layer structures on the device performance, HEMTs with all these three buffer layer structures exhibited serious drain current collapse issue. However, the HEMTs with 2 \( \mu m \) thick GaN buffer only showed around 20% degradation even after the HEMTs been stressed at 40V applied to the drain electrode. HEMTs with 1 \( \mu m \) thick GaN and GaN/AlGaN composite buffer layer structures showed 50% drain current reductions.
Besides off-state drain electrical step-stress, off-state drain breakdown voltage ($V_{\text{off-state}}$) and isolation breakdown voltage ($V_{\text{iso}}$) were characterized as well. The off-state drain breakdown voltage is shown in Figure 6-8A, which was measured far below the typical threshold voltage of $V_G = -8V$. Besides the buffer layer, field plate also played an important role on critical voltage of the off-state step stress as well as off-state drain breakdown voltage. Field plate altered the electrical field distribution around the gate and lowered the electrical field around the gate edges; thus improved both critical voltage of the off-state step stress and off-state drain breakdown voltage. Isolation breakdown voltage measurements were conducted on isolation pads with 5 μm gaps, as shown in Figure 6-8B. To protect devices from breakdown, compliance currents of 100 μA and 1 μA were set for off-state breakdown voltage and isolation breakdown voltage measurements, respectively. Just as the electrical stress results, the devices with thicker GaN buffer layers demonstrated the lowest $V_{\text{off-state}}$ values. The $V_{\text{off-state}}$ for HEMTs with thin GaN and composite buffers were ~100V, however, this value was 50-60V for those devices with thick GaN buffers. A similar trend was observed in the isolation breakdown voltage measurements, with the highest $V_{\text{iso}}$ achieved based on thin GaN or composite buffer designs with a value of 600-700V, while a much smaller $V_{\text{iso}}$ of ~200V was measured on HEMTs with the thick GaN buffer layers.

The critical voltage for electrical degradation is strongly dependent on electric field.$^{142}$ During off-state electrical stress, the peak electric field was located at both sides of the gate edges. Typically, the peak field at the drain side of gate edge was higher than that at source side, since the drain was biased while the source was grounded in device applications. Additional mechanical stress will be induced due to the presence of
this high electrical field in the piezoelectric GaN and AlGaN layers.\textsuperscript{22,39} When the magnitude of the electric field reached threshold levels, a variety of degradation mechanisms such as cracks, notches, gate metal diffusion and corresponding threading dislocations could be created.\textsuperscript{40,62} Finally, irreversible degradation in dc characteristics will be observed when this degradation progresses. When the thickness of the buffer layer is reduced, the defect density will be increased.\textsuperscript{138,139} Those defects act as trap centers, which remove free electrons from the channel and cause the formation of an additional virtual gate,\textsuperscript{45} especially, in the access region between the gate and drain. Consequently, the presence of a higher density of defects further extends the depletion region into the buffer layer, and the peak electric field at drain side of gate edge is reduced. The peak electric field is therefore reduced for HEMTs fabricated with thin buffer layers as compared to those with thick buffer layer at a given drain bias and this leads to a higher critical voltage for the onset of leakage current and better apparent reliability during bias stressing. AlGaN plays as a transition layer between SiC substrate and GaN buffer layer, since the lattice constant of AlGaN is more close to SiC as compared to GaN. By inserting the AlGaN between the substrate and GaN, the dislocation density in the GaN can be reduced. Although the thin and composite buffer structures have the same thickness, the density in the GaN layer is less for the latter, which was also confirmed by pulse measurement in the following paragraph. Therefore, a higher critical voltage was demonstrated by HEMTs fabricated with thin GaN buffer layer.

Gate pulse measurements were also employed to evaluate the material quality of the HEMT with different buffer layer structures. In this study the drain current ($I_{DS}$)
response to a pulsed gate-source voltage ($V_{GS}$) was measured. The normalized $I_{DS}$ as a function of $V_{GS}$ in both pulsed and dc mode for HEMTs is shown in Figure 6-9. During the pulse measurement, the $V_{GS}$ was pulsed from -5V to the values shown on x-axis at different frequencies of 100 and 10 KHz with 10% duty cycle, while drain was kept constant at +5V. The reduction of the drain current in the pulsed mode as compared to the drain current in the dc mode was due to the presence of surface traps in the access region between gate and drain contact. Usually, the traps have some specific time constants and could not respond above certain frequency. Thus the pulsed drain current would be lower than the dc drain current. As shown in Figure 6-9, HEMTs with 1 µm GaN buffer layer exhibited largest reduction of the drain current during the pulse measurement indicating more traps in this structure.

Figure 6-10 illustrates the room temperature photoluminescence (PL) spectra of HEMTs with different buffer layers. All sample exhibited a band edge (BE) emission at around 3.4 eV. A broad yellow luminescence (YL) band associated with deep levels including carbon impurity, Ga vacancy, Ga interstitial, and N antisite at around 2.2 eV (560 nm) was not observed for these samples. This implied that the qualities of the HEMT structures with these three buffer layers were reasonably good. The shoulder of the main BE peak ranging from range 3.25 to 3.35eV was originated from N vacancy. Besides BE emission, there were very low-intensity broad blue luminescence (BL) bands centered at 2.85-2.95 eV. The insert PL spectra illustrated in Figure 6-10 are the enlarged spectra of these BL bands. These bands were often observed in the PL of GaN grown by MOCVD and were attributed to the transitions from the conduction band or a shallow donor. Among these three buffer layer, BL band
showed a lowest intensity for the HEMT structure with 2 µm GaN buffer and these results were consistent with HEMT dc characteristics and pulse measurements.

6.4 Summary

The effect of buffer designs on the reliability of AlGaN/GaN HEMTs by off-state electrical drain step-stress was investigated. Three types of buffer layers were used in this work, 1 µm or 2 µm GaN buffers or a composite AlGaN/GaN buffer layer. The devices fabricated on thicker GaN layers showed the lowest \( V_{\text{cri}} \) of 30-50V, while \( V_{\text{cri}} \) 65-80V was achieved with composite buffers and 70-90V for those with thin GaN buffers. Similar trends were observed in off-state breakdown voltage and isolation breakdown voltage measurements. The depletion region in HEMTs with thinner GaN buffers was extended into the buffer layer due to the presence of a higher density of defects, which was responsible for the improvement of device reliability.
Figure 6-1. Schematic of epitaxial structures of AlGaN/GaN HEMTs.
Figure 6-2. Transfer characteristics of HEMTs fabricated on different buffer layers.
Figure 6-3. Sub-threshold drain I-V characteristics of HEMTs fabricated on different buffer layers.
Figure 6-4. Drain characteristics of HEMTs fabricated on different buffer layers.
Figure 6-5. Gate characteristics of HEMTs fabricated on different buffer layers.
Figure 6-6. Off-state drain step-stress results of HEMTs fabricated on different buffer layers, measurements were conducted at $V_G = -6V$. 

![Graph showing off-state drain step-stress results of HEMTs with different buffer layers. Measurements were conducted at $V_G = -6V$.](image-url)
Figure 6.7. Some of the saturation drain I-Vs recorded between each step stress for HEMTs fabricated on different buffer layers.
Figure 6-8. The results of off-state breakdown voltage and isolation breakdown voltage measurements of HEMTs fabricated on different buffer layers. A) off-state breakdown voltage and B) isolation breakdown.
Figure 6-9. Normalized drain current, $I_{DS}$, as a function of $V_{GS}$ for both pulsed and dc modes.
Figure 6-10. Room temperature photoluminescence (PL) spectra of HMETs with different buffer layers. Insert: Enlarged blue luminescence (BL) bands of those HEMTs with different buffer layers.
CHAPTER 7
EFFECTS OF PROTON IRRADIATION ON GAN-BASED HIGH ELECTRON MOBILITY TRANSISTORS

7.1 The Effects of Proton Irradiation on the Reliability of InAlN/GaN High Electron Mobility Transistors

7.1.1 Background

InAlN/GaN high electron mobility transistors (HEMTs) appear to be an excellent candidate to replace conventional AlGaN/GaN heterostructures in some electronics applications. Promising DC, RF and output power performances of InAlN/GaN HEMTs on Si, sapphire and SiC substrates have been reported, which make them suitable for high power and high frequency applications such as broadband communication and power flow control. InAlN with an In mole fraction of 0.17 can be grown lattice-matched to GaN, which eliminates the strain present in the AlGaN/GaN heterostructure system and this should be beneficial for device reliability. Due to the existence of large spontaneous polarization between InAlN and GaN, a high density two dimensional electron gas (2DEG), above $2.5 \times 10^{13} \text{cm}^{-2}$ can be achieved, leading to higher current densities and higher powers compared to typical AlGaN-based HEMTs.

Recently, a record current density of 2.5 A/mm at $V_G = +2\text{V}$ was reported with 6.9 nm barrier thickness and gate length ($L_G$) of 100 nm. In addition, a thin barrier layer assists in reducing short channel effects in high frequency applications.

For space applications, devices are always exposed to harsh conditions, including high energy proton, gamma ray and X-ray fluxes. Thus far, the effect of proton irradiation on InAlN/GaN device performance has been investigated by several groups. Lo et al. reported the degradation of DC performance of InAlN/GaN HEMTs after 5 MeV proton irradiation with doses varying from $2 \times 10^{11}$ to $2 \times 10^{15} \text{cm}^{-2}$. Kim et al. studied
the influence of proton irradiation on InAlN/GaN HEMTs grown on SiC substrates, which were subjected to 5 to 15 MeV high energy protons with a fixed $5 \times 10^{15}$ cm$^{-2}$ fluence. Irradiation at lower energy was found to degrade the direct current (DC) current-voltage (I-V) characteristics more severely than higher-energy irradiation, because more defects were formed in the vicinity of the 2-dimensional electron gas when lower energy was applied. The main degradation mechanism by proton irradiation is displacement damage. Defect centers are introduced during the collisions between incident protons and nuclei of the lattice atoms. These defect centers have significant capture cross-sections for free carriers, resulting in the reduction of carrier density and conductivity of irradiated HEMTs. The mobility is strongly affected by interface roughness and the scattering from defect centers in the vicinity of the channel can also degrade mobility.

Analyses of degradation of lattice-matched InAlN/GaN under different conditions have been reported. InAlN/AlN/GaN heterostructure field effect transistors were stressed under high electric field at room temperature. The degradation was attributed to the buildup of hot phonons, which caused local heating and defect generation. A comprehensive study, including off-state stress, semi-on stress and negative gate bias stress were performed by Kuzmik et al. Irreversible damage was found for the off-state biasing and for the semi-on stresses when drain-gate voltage was over 38V. The damage was considered as being due to hot electrons, which were injected into the GaN buffer layer underneath the gate and either created defects or ionized existing defect states. There have also been reports of improvement of breakdown voltage in
AlGaN-based HEMTs by proton irradiation. However, there is no report on the reliability of proton irradiated InAlN/GaN HEMTs.

In this chapter, the drain and gate I-V characteristics of reference and proton-irradiated InAlN/GaN HEMTs as well as the resultant performance of the HEMTs after off-state drain-voltage step-stress biasing cycles were reported.

7.1.2 Experimental

The HEMT structures were grown with a Metal Organic Chemical Vapor Deposition (MOCVD) system, starting with a thin AlGaN nucleation layer, followed with a 1.9 µm low-defect carbon-doped GaN buffer layer, 50 nm undoped GaN layer, 10.2 nm undoped InAlN layer with a 17% of In mole fraction, and capped with a 2.5 nm undoped GaN layer. The samples were all grown on three inch diameter, c-plane sapphire substrates. Hall measurements on the as-grown structures showed sheet carrier densities of $2.1 \times 10^{13}$ cm$^{-2}$ and the corresponding electron mobility of 1000 cm$^2$/V-s. Device fabrication began with the Ohmic contact deposition with the standard lift off e-beam evaporated Ti/Al/Ni/Au based metallization, and the samples were subsequently annealed at 800°C for 30 s under a N$_2$ ambient. A typical contact resistance of 0.6 Ω-mm was obtained using the transmission line method (TLM). Multiple energy and dose nitrogen implantation was used for the device isolation and photoresist AZ1045 was used as the mask to define the active region of the devices. Isolation currents were less than 10 nA at 40 V of bias voltage across two 100 µm × 100 µm square Ohmic contact pads separated by a 5 µm implanted gap. 1-µm gates were defined by lift-off of e-beam deposited Pt/Ti/Au metallization. Ti/Au metallization was utilized for the interconnect metals for source, gate, and drain electrodes. The
transistors were passivated using 400 nm of the plasma-enhanced chemical vapor deposited (PECVD) SiNx at 300°C, followed by opening of contact windows using fluorine-based plasma etching. The DC characteristics of the HEMTs were measured with a Tektronix curve tracer 370A and an HP 4156 parameter analyzer.

All the samples were proton irradiated in a vacuum chamber at room temperature with the MC-50 Cyclotron at the Korea Institute of Radiological and Medical Sciences. Proton beam energy was controlled from 15 to 5 MeV by inserting an aluminum degrader. The samples were mounted with carbon tape, where the front face aimed at the proton beam, which means that growth direction of the samples is parallel to the direction of the proton beam. The dc characteristics of the HEMTs were measured with HP 4156 parameter analyzer.

7.1.3 Results and Discussion

Figure 7-1 shows the gate current during typical off-state step-stresses of InAlN/GaN HEMTs prior to and post proton irradiation. The gate current, $I_G$, was plotted as a function of stressed drain voltage. The devices were stressed for 60 seconds at each drain voltage step, while grounding the source electrode and a constant voltage of -6V applied to the gate electrode. The stress started at 5 V of drain voltage and the voltage step was kept at 1 V. During the step-stress, besides monitoring $I_G$, gate-to-source leakage current, $I_{GS}$, and gate-to-drain leakage current, $I_{GD}$, were also measured. Between each step stress, drain I-V, extrinsic transconductance, gate forward current biased from 0 to 1.5 V and gate reverse current biased from 0 to -10 V, were recorded. Self-heating effects were negligible based on the low drain-source currents under our test conditions. The critical voltage, $V_{cri}$, of the off-state step stress was defined as the onset of a sudden $I_G$ increase during the stress. Typical $V_{cri}$ for electrical degradation of
virgin (un-irradiated) HEMTs ranged from 45 to 55 V. By sharp contrast, no such critical voltage was detected for devices after proton irradiation even the drain was biased to +100 V, which is the limit of our apparatus. The same results were observed for devices post 10 and 15 MeV proton irradiation as well as the HEMTs exposed with different doses ranging from \(2 \times 10^{11}\) to \(2 \times 10^{15}\) cm\(^{-2}\) of protons at fixed energy of 5 MeV.

During the off-state stress, before the gate bias voltage reached the critical voltage, there was no degradation observed for both gate and drain I-Vs. Once the drain bias voltage reached \(V_{cri}\), not only did the gate reverse bias leakage current suddenly increase, as illustrated in Figure 7-1, but also the saturation drain current decreased, as previously reported in AlGaN/GaN\(^{21}\) and InAlN/GaN structures.\(^{172}\) As shown in Figure 7-2, the saturation drain current was reduced \(~12\%\) for the un-irradiated HEMTs after the stress. There were no obvious changes of the drain current for irradiated HEMTs, as illustrated in Figure 7-3.

Besides drain I-V characteristics, the gate I-V characteristics exhibited a similar trend, as shown in Figure 7-4. Although the gate current of the irradiated HEMT was much higher as compared to the un-irradiated HEMTs, there were no changes in gate reverse and forward characteristics after the off-state stress. The decrease of drain saturation current and increase of reverse bias gate leakage current of irradiated devices were attributed to the reduction of sheet carrier concentration and carrier saturation velocity caused by the defects generated during the proton implantation.\(^{163-167}\) On the contrary, the un-irradiated HEMTs exhibited permanent changes of both forward and reverse gate leakage characteristics for reference HEMTs after the stress. The reverse gate leakage increased more than two orders of magnitude.
Figure 7-5 shows the measured off-state breakdown voltages of reference and proton-irradiated InAlN/GaN HEMTs. The breakdown voltage increased from 100 V in the reference device to 160 V in the proton-implantation one, which was irradiated with an energy of 5 MeV and dose of $5 \times 10^{15}$ cm$^{-2}$.

It was previously reported that the degradation in DC characteristics after off-state stress in GaN-based HEMTs was irreversible. Those permanent changes were related to gate contact metal diffusion beneath the gate fingers, along with associated threading dislocation formation, which provided extra leakage paths. It was previously reported that the degradation in DC characteristics after off-state stress in GaN-based HEMTs was irreversible. Those permanent changes were related to gate contact metal diffusion beneath the gate fingers, along with associated threading dislocation formation, which provided extra leakage paths. For un-irradiated devices, there were many such spots, which were visible as dark features in electroluminescence (EL) spectra and likely the origin of degradation and could be related to the metal diffusion into the semiconductor or formation of defects under the gate. However, for those irradiated HEMTs, lots of defects were created during the proton irradiation process. Based on SRIM simulation, the estimated vacancies around 2DEG channel ranged from $5 \times 10^8$ to $2 \times 10^{10}$ cm$^{-2}$ when the conditions of implantation energy of 5-15 MeV and dose of $5 \times 10^{15}$ cm$^{-2}$ was applied, and an increase in defects that behave as trap sites are expected in the GaN buffer below the channel. These defects were reported to be deep acceptor-like traps with high capture cross sections for both carrier types. These traps can capture free electrons and in consequence, the vertical electric field beneath gate metal was increased and extended into the buffer layer. In other words, the depletion mode was modified, increasing the vertical depletion at the expense of lateral depletion. Therefore, the peak electric field in the x-direction at drain-side gate edge of the irradiated HEMT was reduced and the reliability of the irradiated HEMT at a similar drain voltage improved as compared to the reference
HEMT. It was reported that higher breakdown voltage was measured in samples with
more edge-type dislocations.\textsuperscript{136} In addition, the relationship between breakdown voltage
and density of traps formed by threading dislocations was also demonstrated, which
concluded that larger trap density led to higher breakdown voltage.\textsuperscript{175}

7.1.4 Summary

In conclusion, this section demonstrated significant improvement of reliability of
InAlN/GaN HEMTs exposed to proton irradiation. The critical voltage for off-state
electrical step-stress was increased from \(\sim+50\) V to above +100 V. Minimal changes of
gate and drain I-V characteristics were observed for the HEMTs post proton
implantation. The large change in critical voltage was tentatively attributed to the
modification of depletion mode under gate, which increases the tendency for vertical
depletion instead of lateral depletion. Hence, the peak electric field in the x-direction at
the drain-side gate edge was reduced.
7.2 The Effects of Proton Energy on the Degradation of AlGaN/GaN High Electron Mobility Transistors

7.2.1 Background

AlGaN/GaN high-electron mobility transistors (HEMTs) are well suited for high power and high frequency broadband communication systems either on the ground or in space. High radiation resistance is required for applications in satellites and space technology because of the presence of large fluxes of high-energy electrons, protons and heavy ions. The initial work on effect of proton irradiation on GaN-based heterostructures involved light-emitting diodes,\textsuperscript{176} while subsequent work has focused on AlGaN/GaN HEMTs.\textsuperscript{165-167,177-182} For a proton fluence of $10^{14}$ cm$^{-2}$ at 1.8 MeV energy, reductions of saturation drain current ($I_{DSS}$) and transconductance ($g_m$) in HEMTs from 260 to 100 mA/mm and from 80 to 26 mS/mm, respectively, were reported.\textsuperscript{177} Similar proton energy studies at different energies were performed by Hu \textit{et al.}\textsuperscript{165} and White \textit{et al.},\textsuperscript{178} which found little degradation and good radiation tolerance of the device channel at fluences up to $10^{14}$ cm$^{-2}$. For proton irradiation energy of 5 MeV and doses of $2 \times 10^{15}$ cm$^{-2}$, which is equivalent to roughly 1000 years in low earth orbit, the $I_{DSS}$ of AlGaN/GaN HEMTs was decreased by 43%,\textsuperscript{166} while at 17 MeV at doses of $2 \times 10^{16}$ cm$^{-2}$, the reductions were 43% and 29% in $I_{DSS}$ and $g_m$, respectively.\textsuperscript{180} To simulate the environment in space, Sonia and co-workers also irradiated devices with 2 MeV protons, carbon, oxygen, iron and krypton ions with fluences ranging from $1 \times 10^9$ cm$^{-2}$ to $1 \times 10^{13}$ cm$^{-2}$.\textsuperscript{181} The energy dependence of proton-induced degradation was studied by Hu \textit{et al.},\textsuperscript{182} little degradation was observed at 15, 40 and 105 MeV, while 10.6% and 6.1% reductions of drain saturation current and maximum transconductance were obtained at 1.8 MeV energy and fluences of $10^{12}$ cm$^{-2}$, due to much larger non
ionizing energy loss. Roy et al. studied the radiation response of GaN/AlGaN HEMTs grown by Molecular Beam Epitaxy (MBE) to 1.8-MeV proton fluences. HEMTs grown under ammonia-rich conditions were more susceptible to proton-induced degradation, compared to devices grown under Ga-rich or N-rich conditions. Proton irradiation caused positive shifts in pinch-off voltage for all three kinds of devices. N vacancies were suggested to be responsible for an increase of 1/f noise after irradiation.

To understand the energy dependence of irradiation-induced degradation in AlGaN/GaN at higher fluence, a proton source with energies of 5, 10 and 15 MeV at a fixed fluence of $5 \times 10^{15}$ cm$^{-2}$ was employed in this study. The measurement of HEMT gate and drain I-V characteristics as well as small and large signal rf measurements were conducted prior to and after the proton irradiation. The dependencies of mobility and carrier concentration on irradiation energy were also investigated.

### 7.2.2 Experimental

The AlGaN/GaN HEMTs were grown on 6-H SiC semi-insulating substrates by metal organic chemical vapor deposition, with the following sequence of epitaxial layers: an AlN nucleation layer, a 1.8 μm GaN buffer layer, a 1 nm In$_{0.10}$Ga$_{0.90}$N backbarrier, a 15 nm GaN channel and a top 22 nm Al$_{0.26}$Ga$_{0.74}$N barrier. On-wafer Hall measurements showed a sheet carrier concentration, sheet resistance, and mobility of $9.1 \times 10^{12}$ cm$^{-2}$, 410 Ω/□, and 1670 cm$^2$/V•s, respectively. An inductively coupled plasma mesa etch of ~1000 Å was performed to isolate adjacent devices. Ti/Al/Ni/Au Ohmic metallization patterned by lift-off was annealed at 850°C for 30 sec for source/drain contacts, producing a specific contact resistance of 0.4 Ω•mm. The HEMTs employed a Ni/Au double gate, π-design with a gate length of 0.2 μm and width of 50 μm. The source-to-
gate and gate-to-drain distances were 1 µm. The devices were passivated with 200 nm of SiNₓ deposited by a Plasma Therm 790 PECVD system. Figure 7-6 shows a schematic of the AlGaN/GaN HEMT.

The dc characteristics of the HEMTs were measured with HP 4156 parameter analyzer. Off-state drain-voltage step-stress was also performed on the reference and proton irradiated samples. The HEMTs were stressed for 60 seconds at each drain voltage step, while grounding the source electrode and applying a constant -6V to the gate electrode. The stress started at 5 V of drain voltage and the voltage step was kept at 1 V. During the step-stress, a number of parameters were measured, including gate current, I_G, gate-to-source leakage current, I_GS, and gate-to-drain leakage current, I_GD. Between each step stress cycle, the drain I-V characteristics, extrinsic transconductance, gate forward current biased from 0 to 1.5 V and gate reverse current biased from 0 to -10 V were also recorded. The RF performance of the HEMTs was characterized with an HP 8722C network analyzer. Load pull measurements were conducted with a Maury microwave system at 10 GHz at room temperature. Stopping and range of ions in matter (SRIM) simulations were used to estimate the penetration depth of the protons into the AlGaN/GaN HEMT structures at various proton energies.

### 7.2.3 Results and Discussion

As shown in Figure 7-7A and 7-7B, the SRIM data indicate that the majority of the nuclear stopping damage induced by the high energy protons occurs deep in the substrate, 105, 335, and 672 µm for 5, 10 and 15 MeV, respectively. The two dimension electron gas channel (2DEG) of the HEMT is located 22 nm below the sample surface and the vacancy densities at the 2DEG are several orders lower than the peak of the
damage. The energy loss of protons is primarily due to stopping until near the end-of-range. As shown in Figure 2a, the 15 MeV protons can penetrate the entire AlGaN/GaN/SiC wafer, which is approximately 500 µm thick. For the deeper the proton penetration, the less displacement damage is generated around the 2DEG, as shown in Figure 7-7C. Therefore, based on SRIM analysis, 5 MeV protons should degrade the AlGaN/GaN HEMT more severely as compared with higher energy protons (10 and 15 MeV) if the main degradation mechanism is related to creation of defects by nuclear stopping.

Figure 7-8A shows transfer characteristics from the HEMTs before and after irradiation at 10 MeV. The extrinsic transconductance, $g_m$, was reduced by 22 % and there was a positive shift of 0.34 V for the threshold voltage, $V_{th}$. These changes were mainly due to the displacement damage induced by the ion bombardment reducing both the carrier density and electron mobility. As shown in Figure 7-8B, more severe degradation of the $g_m$ and a larger positive $V_{th}$ shift were observed on HEMTs irradiated with a lower energy of 5 MeV, with the $g_m$ decreased around 40% and $V_{th}$ shifted by almost 1V. The non-ionizing energy loss in the actual 2DEG region increased with decreasing proton energy and thus more trap states and scattering centers were created around the AlGaN/GaN interface. A similar trend was observed for the effect of proton energy on extrinsic transconductance reduction, with 38 % and 22 % reductions after 5 and 10 MeV irradiation, respectively, and less than 12% for 15 MeV. There was a positive shift of threshold voltage of 0.98 V after 5 MeV proton irradiation, while the HEMT irradiated with a 15 MeV protons exhibited a much smaller shift of 0.05 V.
The reverse and forward gate I-V characteristics of the HEMTs before and after proton irradiation at 10 MeV are illustrated in Figure 7-9. The reverse gate leakage current at $V_G = -10\text{V}$ decreased more than one order of magnitude and similar results were observed for the HEMTs irradiated with 5 and 15 MeV protons. The gate forward characteristics of the proton irradiated HEMTs also improved, and the Schottky barrier height (SBH) increased around 5-8 % while ideality factor decreased 30-40%, as summarized in Table 7-1. Besides the gate forward and reverse characteristics showing significant improvements, there were two other features related to the Schottky gate that were also enhanced, namely gate critical voltage during the off-state drain-voltage step-stress and off-state drain breakdown voltage, as shown in Figure 7-10A and B. The critical voltage, $V_{\text{cri}}$, of the off-state step-stress was defined as the onset of a sudden $I_G$ increase during the stress.\textsuperscript{187} During the off-state stress, before reaching the $V_{\text{cri}}$, there was no degradation observed for both gate and drain I-Vs. Once the drain bias voltage reached $V_{\text{cri}}$, not only did the gate current suddenly increased, but the HEMTs showed permanent degradation involving much higher reverse bias gate leakage current and forward gate current, and reductions in Schottky barrier height, drain saturation current, transconductance and drain current on-off ratio.\textsuperscript{142,187} The typical $V_{\text{cri}}$ of the reference HEMTs was around 12 to 15 V, by sharp contrast, those of the proton irradiated HEMTs ranged from 45 to 50 V. Thus, the gate electrode of the proton irradiated HEMTs could sustain 50V (-6V applied on the gate during the stress plus 45V of drain voltage) as compared to 18V for the reference samples. As illustrated in Figure 7-10B, the off-state drain breakdown voltage of the proton irradiated HEMTs also increased significantly. The gate electrode electrical field did not evenly distribute around the gate, the highest
electrical fields were located at the edges of the gate.\textsuperscript{82} A possible explanation is that the proton induced defects that formed a virtual gate in the buffer layer, changing the gate electrical field profile of the gate and reducing the maximum field. Similar results of improving drain breakdown voltage were also reported for the HEMTs grown with lower quality buffer layer.\textsuperscript{136,175} It was suggested that the charged traps in the low quality buffer layer modified the depletion region by increasing the vertical depletion at the expense of decreasing lateral depletion.

Table 7-2 summarizes the effect of proton irradiation energy on saturation drain current, sub-threshold drain leakage current, drain current on-off ratio and sub-threshold slope. Sub-threshold leakage current, sub-threshold slope and on/off drain current ratio are essential to power amplifier performance in power added efficiency, linearity, noise figure and reliability. Although the change in saturation drain current was inversely proportional to the proton energy as a result of trap formation reducing the free carrier density in the HEMT channel, other properties, such as sub-threshold drain leakage current, drain current on-off ratio and sub-threshold slope, improved significantly as a result of the lower gate leakage current. Figure 7-11 shows drain and gate currents as a function of the gate voltage prior to and post 10 MeV proton irradiation. The drain current was slightly reduced, while the sub-threshold drain leakage currents were reduced 2 orders of magnitude and the drain current on/off ratio increased more than 2 orders of magnitude. The sub-threshold slopes also decreased 40\% and were closer to the ideal theoretical number of $\sim$60 mV/dec. These sub-threshold characteristics were highly dependent on the reverse bias gate leakage current, and significant improvements were observed after the proton irradiation.
Figure 7-12A shows the drain current-voltage (I-V) characteristics of AlGaN/GaN HEMTs before and after irradiation with 10 MeV protons. Although all the irradiated AlGaN/GaN HEMTs exhibited good pinch-off characteristics, the amount of saturation drain current reduction was dependent on the irradiation energy. For the 10 MeV irradiated HEMTs, the reduction of saturation drain current at $V_G = 0V$ was 24%. A much larger saturation drain current reduction, 46%, was observed for the HEMTs irradiated with 5 MeV protons energy and only 11.5% drain current reduction for the HEMTs irradiated with 15 MeV protons, as illustrated in Figure 7-12B. The effect of proton irradiation on the saturation drain current was consistent with the transfer characteristics results. The drain I-V characteristics in the low field linear region were used to extract the electron mobility by treating the undoped AlGaN layer as a gate insulation layer. There were 34 - 78% reductions in electron mobility observed for the irradiated HEMTs, depending on the proton energy. The electron mobility, carrier concentration and sheet carrier concentration, as well as the carrier removal rate of the proton irradiated HEMTs are summarized in Table 7-3. C-V measurements were carried out to estimate the carrier concentrations of these samples. The carrier removal rates were defined as the ratio of carrier concentration decrease divided by the fluence of irradiated protons. As illustrated in Figure 7-13, the carrier removal rate was inversely proportional to the irradiated proton energy, $R_{NC} = -21.5 \cdot E \ (MeV) + 441.7$, where $R_{NC}$ is carrier removal rate and $E$ is proton energy.

Gate pulse measurements were employed to evaluate traps created during proton irradiation. In this technique, the response of the drain current ($I_{DS}$) to a pulsed gate-source voltage ($V_{GS}$) was measured. The normalized $I_{DS}$ as a function of $V_{GS}$ in
both pulsed and dc modes for HEMTs before and after 5 MeV proton irradiation at a fluence of $5 \times 10^{15}$ cm$^{-2}$ is shown in Figure 7-14A. In this case, the $V_{GS}$ was pulsed from -5V to the values shown on x-axis at different frequencies of 100, 10 K and 100 KHz with 10% duty cycle, while the drain voltage was kept constant at +5V. The reduction of the drain current in the pulsed mode as compared to the drain current in the dc mode was due to the presence of surface traps in the access region between gate and drain contacts. The comparison of $I_{DS}$ reduction in pulsed mode after irradiation at various energies is illustrated in Figure 7-14B. Larger gate-lag was produced at higher frequency for HEMTs irradiated at 5MeV, which indicated more shallow traps close to device surface produced at lower irradiation energy.

Double pulse measurements were also performed, in which the drain was pulsed from +10 to +5V, while simultaneously pulsing the gate bias from -5V to the values shown on the x-axis at different frequencies of 100, 10 K and 100 KHz with 10% duty cycle. As illustrated in Figure 7-15A, the dispersion between dc and pulsed data at gate bias close to threshold voltage was due to the formation of an virtual gate resulting from the injection of hot electrons into the surface between gate and drain electrodes during off state biases. The normalized double pulsed $I_{DS}$ as a function of irradiation energy is shown in Figure 7-15B. A similar trend was observed in the gate-lag result, as a result of more defects created close to the surface in the access region between gate and drain after lower energy irradiations.

Besides DC characterization, small and large signal rf measurements were also performed. The small signal measurements on proton irradiated HEMTs were performed from 50 MHz to 40 GHz. Figure 7-16A shows the microwave performance of
devices exposure to 15 MeV proton irradiation, with the HEMTs biased around the $g_m$ peak and $V_{DS} = +5V$. $f_T$ and $f_{MAX}$ can be extracted from the extrapolation of $h_{21}$ and of Mason’s maximum unilateral gain $U$ with a slope of -20 dB/dec. $f_T$, $f_{MAX}$ and $G$ as a function of irradiation energy were plotted in Figure 7-16B. Proton irradiation decreased both $f_T$ and $f_{MAX}$, and lower energy proton irradiations produced more degradations in rf characteristics.

Load pull measurements were conducted at 10 GHz. Both load and source tuners were tuned to optimum states for the device under test (DUT), RF input power was swept from 0 to 15 dBm to record load pull characteristics, as shown in Figure 7-17A. The output power ($P_{out}$) and power added efficiency (PAE), $G_t$ and $G_p$ referred in Figure 7-17B were measured at peak of PAE. As with the dc and rf results, HEMTs irradiated with lower energy showed more degradation in power performances due to more severe proton-induced displacement damage induced in the HEMT channel at lower irradiation energy.

7.2.4 Summary

The effect of proton irradiation energies at 5, 10 and 15 MeV at fixed fluence of $5 \times 10^{15}$ cm$^{-2}$ has been studied with dc, rf and power measurements in section 7.2. After irradiation, sub-threshold drain leakage current and reverse gate I-V decreased more than one order of magnitude for all cases due to the increase of resistivity of the HEMT channel. The increase in device degradation with decreasing proton energy is due to the increase in linear energy transfer and corresponding increase in non-ionizing energy loss with decreasing proton energy in the active region of the HEMTs.
7.3 The Effects of Proton Dose on the Degradation of AlGaN/GaN High Electron Mobility Transistors

7.3.1 Background

The properties of the AlxGa1-xN material system, such as large bandgap, high electron mobility and breakdown field, make it a promising candidate for applications in high power and high frequency communication systems.\cite{190,192} For space-based applications, electronic components of satellites may suffer radiation damage from high fluxes of energetic particles in the van Allen belts, such as protons, electrons and heavy ions caused by solar flares and primary cosmic rays.\cite{193} As compared to GaAs, GaN demonstrates several orders of magnitude higher radiation tolerance. Recently, attention has been focused on the effects of proton irradiation of GaN-based high electron mobility transistors (HEMTs) at energies in the range 5-15 MeV and relatively high doses of $5 \times 10^{15} \text{ cm}^{-2}$.\cite{194,195} These results have shown larger degradation of dc (saturation drain current, $I_{DSS}$ and transconductance, $g_m$) and rf (unit gain cutoff frequency, $f_T$, maximum oscillation frequency, $f_{max}$ and power added efficiency, PAE) characteristics for HEMTs irradiated at the lower range of these proton energies because of the higher nuclear stopping energy loss of these protons at the shallow depths around the 2-dimentional electron gas channel (2DEG). Hu et al. studied the effects of proton energy with a wide range of 1.8, 15, 40 and 105 MeV at a fluence up to $10^{13} \text{ cm}^{-2}$.\cite{196} In this case, the devices exhibited little degradation when irradiated with 15, 40, and 105 MeV protons, while the greatest degradation was measured at the lowest proton energy, due to the larger nonionizing energy loss of the 1.8 MeV protons.\cite{196} The effects of proton dose on dc characteristics of InAlN/GaN HEMTs were
reported by Lo et al.,\textsuperscript{197} which revealed that more degradation was induced at higher irradiation dose, with reductions of $g_m$ of 1\% and 15\%, and increase of channel resistance of 6\% and 28\% for HEMTs exposed to $2\times10^{11}$ and $2\times10^{15}$ cm$^{-2}$ protons, respectively. In addition, it was also reported that there was little degradation at doses below $10^{14}$ cm$^{-2}$ in III-nitride HEMTs.\textsuperscript{165} The proton radiation introduces point defects in the GaN, which can decrease sheet carrier mobility due to increased carrier scattering and decreased sheet carrier density by carrier removal.\textsuperscript{165} Experimental results demonstrate several types of defects after proton radiation, including N vacancies ($V_N$ donor) near $E_c - (0.04 – 0.06)$ eV,\textsuperscript{198} Ga vacancies ($V_{Ga}$ acceptor) near $E_v + 1$ eV,\textsuperscript{199} nitrogen interstitials ($N_i$ acceptors) near $E_c - 1$ eV and Ga interstitials ($Ga_i$ donors) near $E_c - 0.8$ eV.\textsuperscript{200,201} Recently, the accompanying improvement of the reliability of proton-irradiated AlGaN/GaN HEMTs at energies of 5, 10 and 15 MeV was reported.\textsuperscript{195}

In this chapter, an investigation of the effects of radiation dose on dc characteristics of irradiated HEMTs was reported. The AlGaN/GaN HEMTs were irradiated with 5 MeV protons at doses ranging from $1\times10^9$ to $2\times10^{14}$ cm$^{-2}$. The dependencies of mobility, sheet carrier concentration and carrier removal rate on irradiation energy were also investigated.

\textbf{7.3.2 Experimental}

The AlGaN/GaN HEMT device structures were grown on semi-insulating 6H-SiC substrates and consisted of a thin AlN nucleation layer, 2.25 $\mu$m of Fe-doped GaN buffer, 15 nm of Al$_{0.28}$Ga$_{0.72}$N, and a 3 nm undoped GaN cap. On-wafer Hall measurements showed sheet carrier concentrations of $1.06\times10^{13}$ cm$^{-2}$, mobility of 1907 cm$^2$/V-s, and sheet resistivity of 310 $\Omega$/$\square$. The HEMTs employed dry etched mesa isolation, Ti/Al/Ni/Au Ohmic contacts alloyed at 850$^\circ$C (contact resistance of 0.3 $\Omega$•mm),
and dual-finger Ni/Au gates patterned by lift-off. The gate length was 1µm, and gate width was 2×150 µm. Both source-to-gate gap and gate-to-drain distances were 2 µm. The devices exhibited typical maximum drain currents of 1.1 A/mm, extrinsic transconductance of 250 mS/mm at VDS of 10 V, threshold voltage of -3.6 V. The devices were passivated with 200 nm of SiNₓ deposited by a Plasma Therm 790 PECVD system.

Proton irradiations were performed at the Korean Institute of Radiological & Medical Sciences (KIRAMS) using a MC 50 (Scanditronix) cyclotron. The proton energy at the exit of the cyclotron was 30 MeV. The proton energy at the sample was 5 MeV after passing through two aluminum degraders. The thickness of each aluminum degrader was 2.7mm. The beam currents were measured using Faraday-cup to calculate flux density. In this study, the proton dose was varied from 1×10⁹ to 2×10¹⁴ cm⁻². Stopping and Range of Ions in Matter (SRIM) simulator was used to estimate the penetration depth of the protons into the AlGaN/GaN HEMT structure. The device DC characteristics and device reliability test were performed with a HP 4156 parameter analyzer.

### 7.3.3 Results and Discussion

Figure 7-18 illustrates the sheet resistance (Rₛ), contact resistivity (R_C) and transfer resistance (R_T) of the AlGaN/GaN HEMTs extracted from transmission line measurements (TLM) prior to and post proton irradiation as a function of proton dose. For the dose of 10⁹ cm⁻², there was no change for all those parameters. The threshold of R_C and R_T degradation was at a proton dose of 5×10⁹ cm⁻², and the R_C and R_T increased linearly proportional to the proton dose until the proton dose reached at 2×10¹³ cm⁻², exhibiting 3 and 5.5% increases for R_T and R_C, respectively. However, the
threshold of the proton dose for $R_S$ degradation was much higher at $2 \times 10^{13} \text{ cm}^{-2}$ as compared to those for $R_T$ and $R_C$. There was no degradation for $R_S$ detected for the lower dose protons irradiation, in which the density of irradiation-induced defects was still negligible as compared to the native defect density. For the condition of the highest proton dose of $2 \times 10^{14} \text{ cm}^{-2}$ used in this study, $R_S$, $R_C$ and $R_T$ increased 7.9, 6.7 and 7.5%, respectively. The increase of $R_T$ and $R_C$ under the Ohmic contacts could be due to more defects created by proton irradiation in these disordered regions. It is well known that significant increases of edge- and mixed-type threading dislocations (TDs) are induced by metal contact inclusions after high temperature (>850°C) Ohmic contact annealing. Similar trend was reported by Karmarkar et al. Ohmic contact metal regions were more prone to proton irradiation damage, consistent with SRIM simulations shown in Figure 7-19. Figure 7-19A shows the SRIM simulation of ion energy loss as a function of proton penetration depth into the HEMT structure grown on the SiC substrate. The majority of the energy loss was through nuclear stopping deep in the SiC substrate around 145 µm below the HEMT structure. The simulated penetration depth of 5 MeV protons was around 150 µm, and Ohmic metal contact was too thin to affect the penetration. Due to light mass of protons, the nuclear energy loss was minimal in the HEMT surface region, where energy loss was dominated by the electronic stopping mechanism, as illustrated in Figure 7-19B. The 2-dimensional electron gas (2DEG) region is located around 25-30 nm below the surface, thus, there was no damage detected for $R_S$ until the proton dose reached $2 \times 10^{13} \text{ cm}^{-2}$. However, as illustrated in Figure 7-19C, more energy loss was in the Ohmic metal stack region due to nuclear stopping of protons with heavier-mass Au atoms in the Au-based Ohmic
metallization. Those scattered protons from the collisions with Au atoms could damage nearby lattices in the 2DEG region. Thus \( R_C \) and \( R_T \) showed a tendency to be more affected by high energy irradiation than \( R_S \). To simplify the simulation, the scheme of the Ohmic metallization prior to the high temperature annealing was used. After annealing, the top Au layer would diffuse to the metal/AlGaN interface, which could induced more proton scattering and create even more defects in the 2DEG channel.\(^{204}\)

The changes of reverse gate leakage current, threshold voltage, and extrinsic transconductance, \( g_m \), were within the measurement errors for the HEMTs irradiated with a proton dose less than \( 2 \times 10^{13} \text{ cm}^{-2} \), as shown in Table 7-4. Figure 7-20 illustrates drain and gate currents as well as the typical transfer characteristics of HEMTs as a function of gate voltage prior to and after \( 2 \times 10^{14} \text{ cm}^{-2} \) proton irradiation, respectively. These measurements were conducted at a fixed drain voltage of +5V. As shown in Figure 7-20A, the sub-threshold drain leakage current was dominated by the reverse gate leakage current when the channel was pinched-off. There was minimal change of reverse gate leakage current, while there was a reduction of extrinsic transconductance \( (g_m) \) of 10\% and a positive shift of threshold voltage \( (V_{th}) \) of 95 mV after irradiation, as shown in Figure 7-20B. These degradations could be attributed to the displacement damage, resulting in the reduction of carrier concentration and mobility.\(^9\)

Figure 7-21 illustrates the drain I-V characteristics of AlGaN/GaN HEMTs before and after proton irradiations with different doses, measured with \( V_G \) starting from 0 V with a step of -1V. The \( I_{DSS} \) of HEMTs irradiated with a dose less than \( 2 \times 10^{13} \text{ cm}^{-2} \) showed minimal change, however, a degradation of 13\% was observed when a higher dose of \( 2 \times 10^{14} \text{ cm}^{-2} \) was employed. Table 7-5 summarizes the \( I_{DSS} \), the reduction of
2DEG mobility, sheet carrier concentration and carrier removal rate as a function of proton irradiation dose. Hall measurements were used to determine the 2DEG mobility and sheet carrier concentrations were estimated from these electron mobilities and the sheet resistances measured with TLM. The carrier removal rates were defined as the ratio of carrier concentration decrease divided by the fluence of irradiated protons. There were no apparent changes of mobility and sheet carrier concentration for those HEMTs irradiated with low doses. The HEMTs irradiated with a dose less than $2 \times 10^{13}$ cm$^{-2}$ showed minimal changes of mobility and sheet carrier concentration, however, decreases of 10% and 41% in sheet carrier concentration and mobility, respectively, were observed for the HEMTs exposed to $2 \times 10^{14}$ cm$^{-2}$ proton dose. The carrier removal rate was determined to be 810 cm$^{-1}$.

In contrast to the trends in $I_{DSS}$, HEMTs irradiated with higher doses of protons exhibited higher drain breakdown voltages, $V_{BR}$, as illustrated in Table 7-6. Below a threshold dose of $2 \times 10^{13}$ cm$^{-2}$, the $V_{BR}$ was fairly constant around 30 ± 1 V. However, the $V_{BR}$ of HEMTs irradiated with higher doses increased by 20% and 37% for the HEMTs irradiated at $2 \times 10^{13}$ cm$^{-2}$ and $2 \times 10^{14}$ cm$^{-2}$ protons, respectively. The $V_{BR}$ was highly dependent on the electrical field distribution around gate edges. The electrode electrical field does not evenly distribute around the gate, with the highest electrical fields located at the edges of the gate and field plate used to reduce the peak electrical field on the edges of the gate electrode.\textsuperscript{82} It was proposed previously that proton induced defects form a virtual gate in the buffer layer, changing the gate electrical field profile of the gate and reducing the maximum field.\textsuperscript{195} Similar results of improving drain breakdown voltage were also reported for the HEMTs grown with lower quality buffer
It was suggested in that work that the charged traps in the low quality buffer layer modified the gate depletion region by increasing the vertical depletion at the expense of decreasing lateral depletion. Rather than creating the defects in the GaN buffer layer by epitaxial growth as in past reports, in our work the high energy proton irradiation was used to create defects in the GaN layer and enhance the drain breakdown voltage.

To illuminate the trap characteristics, gate pulse measurement was conducted. In this study, the drain current (I_Ds) response to a pulsed gate-source voltage (V_GS) was measured. The normalized I_Ds as a function of V_GS in both pulsed and dc mode for the HEMT prior to proton implantation is shown in Figure 7-22A. During the pulse measurement, the V_GS was pulsed from -5V to the values shown on x-axis at frequencies of 100Hz, 10KHz and 100KHz with a duty cycle of 10%, while drain was kept constant at +5V. The reduction of the drain current in the pulsed mode as compared to the drain current in the dc mode was due to the presence of surface traps in the access region between gate and drain contact. Usually, the traps have some specific time constants and could not respond above certain frequency. Thus, the pulsed drain current would be lower than the dc drain current. As shown in Figure 7-22B, there was apparent reduction of I_Ds for the HEMTs irradiated at proton doses higher than 2×10^{12} cm^{-2}, which meant more traps were introduced for the implanted HEMTs. Drain pulse measurements were also performed on the reference and proton irradiated HEMTs by pulsing the drain from 0 to different voltages up to 15 V. Figure 7-23A and B illustrate normalized dc and pulsed drain current at three different frequencies for the reference and HEMT irradiated with a dose of 2×10^{14} cm^{-2} protons.
respectively. Both the drain current measured at dc mode for both HEMTs exhibited
20% reduction due to heating effect, but not for the pulsed measurements. Figure 7-23C
shows the drain current reduction of HEMTs as a function of proton implantation dose at
different frequencies. Similar trend was observed as in gate pulse measurements that
more traps generated for the HEMTs irradiated with higher doses of the protons. Higher
reduction of the drain current was detected with higher pulse frequency due to slow
response of the traps as compared to the pulsed drain voltage.

Off-state drain-voltage step-stress was also conducted on AlGaN/GaN HEMTs
prior to and after proton irradiation to evaluate device reliability.\textsuperscript{21} The HEMTs were
constantly biased for 60 s at each drain-voltage step, while grounding the source
electrode and fixing the gate voltage at -8V. The stress started at 5 V of drain voltage
and drain voltage step was 1 V. To protect devices, a compliance of 50 μA was set
during electrical stress. Figure 7-24 shows gate current, I_G, as a function of stressed
drain voltage. During the step-stress, besides monitoring I_G, gate-to-source leakage
current, I_{GS}, and gate-to-drain leakage current, I_{GD}, were also measured. Due to the low
drain-to-source current during off-state, self-heating effect was negligible and had no
effect on device performance. The critical voltage, V_{crit}, of the off-state step stress was
defined as the onset of a sudden I_G increase during the stress. As previous work
reported, permanent damage in the devices may be created upon exceeding V_{crit},
including the formation of cracks on both source and drain sides of gate edges, the
diffusion of gate metal and native oxide layer at the interface between metal and AlGaN
barrier layer, as well as associated threading dislocations, all of which could provide
possible leakage paths.\textsuperscript{40,82} These mechanisms also cause the irreversible degradation
of dc characteristics of GaN-based HEMTs. There was no difference in $V_{cri}$, $22 \pm 1$ V, detected for the pristine and proton-irradiated HEMTs with a dose less than $2 \times 10^{13}$ cm$^{-2}$, as shown in Table 7-6. However, larger $V_{cri}$ values of 28 and 32 V were observed for HEMTs irradiated with higher doses of $2 \times 10^{13}$ and $2 \times 10^{14}$ cm$^{-2}$, respectively. The improvement of $V_{cri}$ could be ascribed to the previously described mechanism for the improvement of drain breakdown voltage. A virtual gate was formed in the buffer layer for the proton irradiated HEMTs, which reduced the maximum electric field by extending the depletion region into the buffer layer.

7.3.4 Summary

In this section, the effects of proton doses on dc characteristics of irradiated AlGaN/GaN HEMTs by dc measurement and off-state electrical stress was reported. There were less degradation in saturation drain current ($I_{DSS}$), transconductance ($g_m$), mobility and sheet carrier concentration at doses below $2 \times 10^{13}$ cm$^{-2}$. As irradiation dose increased, the increase of $V_{BR}$ were 20% and 37%, $V_{cri}$ were 27% and 45% at doses of $2 \times 10^{13}$ and $2 \times 10^{14}$ cm$^{-2}$, respectively. The improvements of $V_{BR}$ and $V_{cri}$ could attribute to the modification of depletion region due to the introduction of a higher density of defects after irradiation at a higher dose.
Figure 7-1. Off-state gate currents as a function of drain voltage for the un-irradiated and proton-irradiated HEMTs. The protons had energy of 5 and 10 MeV and dose of $5 \times 10^{15}$ cm$^{-2}$. 
Figure 7-2. Drain I-Vs of un-irradiated HEMTs prior to and after off-state electrical step-stress. The devices were stressed with \( V_G = -6 \) V for 60 s at each drain voltage step until sudden increase of IG was observed.
Figure 7-3. Drain I-Vs of HEMTs irradiated with 5 MeV and $5 \times 10^{15}$ cm$^{-2}$ doses of protons prior to and after off-state electrical step-stress. The devices were stressed with $V_G = -6$ V for 60 s at each drain voltage step until drain voltage reached +100V.
Figure 7-4. Gate characteristics of un-irradiated and proton-irradiated (with 5 MeV and $5 \times 10^{15}$ cm$^{-2}$ dose) HEMTs prior to and after off-state electrical step-stress. Un-irradiated devices were stressed with $V_G = -6$ V for 60 s at each drain voltage step until sudden increase of $I_G$ was observed. The same condition used for irradiated HEMT except the drain voltage reached +100 V.
Figure 7-5. Off-state breakdown measurement result of un-irradiated and proton-irradiated HEMTs. The incident protons had energy of 5 MeV and dose of $5 \times 10^{15} \text{ cm}^{-2}$.
Figure 7-6. A schematic of the AlGaN/GaN high electron mobility transistors.
Figure 7-7. SRIM simulation results at the AlGaN/GaN interface of the AlGaN/GaN HEMT structure. A) Energy loss and B) Vacancy density as a function of target depth C) Vacancy density.
Figure 7-8. DC characteristics of HEMTs pre- and post-proton irradiation with energy of 10 MeV at a fluence of $5 \times 10^{15}$ cm$^{-2}$. A) Transfer characteristics. B) Threshold voltages shift and transconductance reduction as a function of irradiation energies.
Figure 7-9. Gate I-V of HEMTs pre- and post-proton irradiation with an energy of 10 MeV at a fluence of $5 \times 10^{15}$ cm$^{-2}$. 
Figure 7-10. Off-state drain-voltage and off-state drain breakdown voltage of HEMTs pre- and post-proton irradiation. A) Off-state drain-voltage step-stress gate current as a function of drain voltage. B) Off-state drain breakdown voltage of HEMTs pre and post proton irradiation.
Figure 7-11. $I_{DS}$ and $I_G$ as a function of $V_G$ of HEMTs pre- and post-proton irradiation with an energy of 10 MeV at a fluence of $5 \times 10^{15}$ cm$^{-2}$. 

$V_{DS} = +5V$
Figure 7-12. Drain I-Vs of HEMTs pre- and post-proton irradiation with an energy of 10 MeV. A) Drain I-Vs. B) Saturation current at $V_{DS} = +5V$ as a function of irradiation energies.
Figure 7-13. Carrier removal rate as a function of proton irradiation energies at a fixed fluence of $5 \times 10^{15}$ cm$^{-2}$. 

The carrier removal rate, $R_{NC}$ (cm$^{-1}$), can be described by the following equation:

$$R_{NC} = -21.5E(\text{MeV}) + 441.7$$
Figure 7-14. The result of Gate pulse measurement. A) Gate pulse measurements on HEMTs pre- and post- proton irradiation with energy of 10 MeV at a fluence of $5 \times 10^{15}$ cm$^{-2}$. $V_G$ is switched from $-5V$ to the values shown on the x-axis at a 10% duty cycle. B) $\Delta I_{DS}$ as a function of irradiation energies.
Figure 7-15. The result of double pulse measurement. A) Double pulse measurements on HEMTs pre- and post- proton irradiation with energy of 10 MeV at a fluence of $5 \times 10^{15}$ cm$^{-2}$. Drain was pulsed from +10 to +5V, simultaneously pulsing the gate from -5V to the values shown on the x-axis at a 10% duty cycle. B) $\Delta I_{DS}$ as a function of irradiation energies.
Figure 7-16. The results of small signal measurement. A) Small signal measurements on HEMTs after proton irradiation with an energy of 10 MeV at a fluence of $5 \times 10^{15}$ cm$^{-2}$. B) $f_T$ and $f_{\text{max}}$ as a function of irradiation energies.
Figure 7-17. The results of large signal measurement. A) Power measurements at 10 GHz on HEMTs after proton irradiation with an energy of 10 MeV at a fluence of $5 \times 10^{15}$ cm$^{-2}$. B) Load-pull characteristics as a function of irradiation energies.
Figure 7-18. Percent increases of sheet resistance ($R_s$), contact resistivity ($R_c$), and transfer resistance ($R_t$) after 5MeV proton irradiation with different doses.
Figure 7-19. The result of SRIM simulation. A) SRIM simulation of proton ion energy loss and proton penetration depth into the HEMT structure grown on the SiC substrate. B) SRIM simulation of proton ion energy loss and proton penetration depth near the surface of the AlGaN/GaN HEMT structure. C) SRIM simulation of proton ion energy loss and proton penetration depth in the Ohmic metal contact region of an AlGaN/GaN HEMT.
Figure 7-20. DC characteristics of HEMTs before and after 5 MeV proton irradiation. A) Drain and gate currents as a function of gate voltage. B) Typical transfer characteristics.
Figure 7-21. Drain characteristics of HEMTs prior to and post 5MeV proton irradiation with various doses.
Figure 7-22. The results of Gate pulse measurements. A) Gate pulse measurements performed on reference HEMT by switching $V_G$ from -5V to the values shown on the x-axis at different frequencies and a duty cycle of 10%. B) Drain current reduction as a function of irradiation doses during the gate pulse measurements.
Figure 7-23. The results of Drain pulse measurements. A) Drain pulse measurements performed on reference HEMT and B) the irradiated device with a dose of 2×10^{14} \text{ cm}^{-2} by sweeping $V_{DS}$ from 0V to 15V at different frequencies and a duty cycle of 10%. C) Drain current reduction as a function of irradiation doses during the drain pulse measurements with $V_{DS}=15V$. 
Figure 7-24. Off-state drain step-stress of HEMTs prior to and post 5MeV proton irradiation with various doses.
Table 7-1. Summary of $I_G$ at $V_G = -10V$, Schottky barrier height before and after 5, 10 and 15 MeV proton irradiation with a dose of $5 \times 10^{15}$ cm$^{-2}$.

<table>
<thead>
<tr>
<th>Samples</th>
<th>Condition</th>
<th>$I_G$ at $V_G = -10V$ (mA/mm)</th>
<th>Schottky barrier height (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 MeV</td>
<td>Pre-irrad.</td>
<td>$1.3 \times 10^{-2}$</td>
<td>730</td>
</tr>
<tr>
<td></td>
<td>Post-irrad.</td>
<td>$4.5 \times 10^{-4}$</td>
<td>788</td>
</tr>
<tr>
<td>10 MeV</td>
<td>Pre-irrad.</td>
<td>$1.6 \times 10^{-2}$</td>
<td>709</td>
</tr>
<tr>
<td></td>
<td>Post-irrad.</td>
<td>$3.3 \times 10^{-4}$</td>
<td>740</td>
</tr>
<tr>
<td>15 MeV</td>
<td>Pre-irrad.</td>
<td>$1.7 \times 10^{-2}$</td>
<td>664</td>
</tr>
<tr>
<td></td>
<td>Post-irrad.</td>
<td>$1.7 \times 10^{-3}$</td>
<td>694</td>
</tr>
</tbody>
</table>

Table 7-2. Summary of the dependence of ON/OFF ratio, saturation drain current, sub-threshold drain leakage current and sub-threshold slope on proton irradiations.

<table>
<thead>
<tr>
<th>Samples</th>
<th>Condition</th>
<th>ON/OFF ratio</th>
<th>Saturation drain current (mA/mm)</th>
<th>Sub-threshold drain leakage current (mA/mm)</th>
<th>Sub-threshold slope (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 MeV</td>
<td>Pre-irrad.</td>
<td>$6.3 \times 10^{-4}$</td>
<td>999</td>
<td>$1.6 \times 10^{-2}$</td>
<td>179</td>
</tr>
<tr>
<td></td>
<td>Post-irrad.</td>
<td>$1.3 \times 10^{-6}$</td>
<td>536</td>
<td>$4.2 \times 10^{-4}$</td>
<td>159</td>
</tr>
<tr>
<td>10 MeV</td>
<td>Pre-irrad.</td>
<td>$4.9 \times 10^{-4}$</td>
<td>986</td>
<td>$2.0 \times 10^{-2}$</td>
<td>202</td>
</tr>
<tr>
<td></td>
<td>Post-irrad.</td>
<td>$1.3 \times 10^{-6}$</td>
<td>754</td>
<td>$5.6 \times 10^{-4}$</td>
<td>124</td>
</tr>
<tr>
<td>15 MeV</td>
<td>Pre-irrad.</td>
<td>$4.2 \times 10^{-4}$</td>
<td>980</td>
<td>$2.3 \times 10^{-2}$</td>
<td>190</td>
</tr>
<tr>
<td></td>
<td>Post-irrad.</td>
<td>$9.9 \times 10^{-5}$</td>
<td>885</td>
<td>$8.9 \times 10^{-4}$</td>
<td>172</td>
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</table>
Table 7-3. Summary of the dependence of normalized mobility, carrier concentration, 
sheet carrier concentration and carrier removal rate on the proton irradiations.

<table>
<thead>
<tr>
<th></th>
<th>Pre-irrad.</th>
<th>5 MeV</th>
<th>10 MeV</th>
<th>15 MeV</th>
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</thead>
<tbody>
<tr>
<td>Normalized mobility</td>
<td>1</td>
<td>0.23</td>
<td>0.38</td>
<td>0.66</td>
</tr>
<tr>
<td>Carrier concentration (cm$^{-3}$)</td>
<td>5.8 x 10$^{18}$</td>
<td>4.3 x 10$^{18}$</td>
<td>4.9 x 10$^{18}$</td>
<td>5.1 x 10$^{18}$</td>
</tr>
<tr>
<td>Sheet carrier concentration (cm$^{-2}$)</td>
<td>7.0 x 10$^{12}$</td>
<td>5.2 x 10$^{12}$</td>
<td>5.9 x 10$^{12}$</td>
<td>6.1 x 10$^{12}$</td>
</tr>
<tr>
<td>Carrier removal rate (cm$^{-1}$)</td>
<td>–</td>
<td>336</td>
<td>224</td>
<td>121</td>
</tr>
</tbody>
</table>

Table 7-4. Summary of threshold voltage shift, the reduction of extrinsic 
transconductance, sheet carrier concentration and mobility, as well as carrier 
removal rate of HEMTs prior to and post 5MeV proton irradiation with various 
doses.

<table>
<thead>
<tr>
<th>Irradiation Dose (cm$^{-2}$)</th>
<th>$\Delta V_{th}$ (mV)</th>
<th>$\Delta g_m$ (%)</th>
<th>Reverse Gate Leakage at $V_G = -5V$ and $V_{DS} = 5V$ (µA/mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 x 10$^9$</td>
<td>0</td>
<td>0</td>
<td>3.6</td>
</tr>
<tr>
<td>5 x 10$^{10}$</td>
<td>0</td>
<td>0</td>
<td>3.8</td>
</tr>
<tr>
<td>2 x 10$^{12}$</td>
<td>0</td>
<td>0</td>
<td>3.5</td>
</tr>
<tr>
<td>2 x 10$^{13}$</td>
<td>10</td>
<td>5</td>
<td>5.6</td>
</tr>
<tr>
<td>2 x 10$^{14}$</td>
<td>95</td>
<td>10</td>
<td>8.1</td>
</tr>
</tbody>
</table>
Table 7-5. Summary of $I_{DSS}$, sheet carrier concentration and mobility, as well as carrier removal rate of HEMTs as a function of proton irradiation doses.

<table>
<thead>
<tr>
<th>Irradiation Dose (cm$^{-2}$)</th>
<th>$I_{DSS}$ (mA/mm)</th>
<th>Reduction of Sheet Carrier Concentration (%)</th>
<th>Reduction of Mobility (%)</th>
<th>Carrier Removal Rate (cm$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$5 \times 10^9$</td>
<td>726</td>
<td>0</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>$5 \times 10^{10}$</td>
<td>725</td>
<td>0</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>$2 \times 10^{12}$</td>
<td>725</td>
<td>0</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>$2 \times 10^{13}$</td>
<td>716</td>
<td>1</td>
<td>7</td>
<td>850</td>
</tr>
<tr>
<td>$2 \times 10^{14}$</td>
<td>630</td>
<td>10</td>
<td>41</td>
<td>810</td>
</tr>
</tbody>
</table>

Table 7-6. Summary of the dependence of drain breakdown voltage ($V_{BR}$) and critical voltage ($V_{cri}$) during the off-state drain-voltage step-stress as a function of irradiation dose.

<table>
<thead>
<tr>
<th>Irradiation Dose (cm$^{-2}$)</th>
<th>Drain Breakdown Voltage $V_{BR}$ (V)</th>
<th>Critical Voltage, $V_{cri}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pristine</td>
<td>30</td>
<td>22</td>
</tr>
<tr>
<td>$10^9$</td>
<td>31</td>
<td>23</td>
</tr>
<tr>
<td>$5 \times 10^9$</td>
<td>30</td>
<td>22</td>
</tr>
<tr>
<td>$5 \times 10^{10}$</td>
<td>29</td>
<td>22</td>
</tr>
<tr>
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<td>31</td>
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<td>36</td>
<td>28</td>
</tr>
<tr>
<td>$2 \times 10^{14}$</td>
<td>41</td>
<td>32</td>
</tr>
</tbody>
</table>
CHAPTER 8
LASER ABLATION OF SILICON CARBIDE

8.1 Background

Silicon Carbide is an attractive wide energy bandgap semiconductor being used in microelectronics on account of its excellent mechanical strength, thermal conductivity, and breakdown field as microwave power electronics, sensors, actuators, resonators and as a substrate for growing GaN based light emitting diodes as well as AlGaN/GaN based high-electron mobility transistors (HEMTs). Vertical through-wafer electrical interconnects (vias) between the metal contacts on the front side of the wafer and the common ground in the back of the wafer are highly desirable to reduce the source inductance, improve thermal conductivity and device reliability. The low inductance vias result in the enhancement of the transistor’s performance in silicon carbon based electronics, such as SiC metal-semiconductor field effect transistors (MESFETs), SiC power metal oxide semiconductor field effect transistors (MOSFETs), and AlGaN/GaN HEMTs grown on SiC substrates. These devices have uses in high power, high temperature commercial applications in telecommunications, hybrid electric vehicles, power flow control and remote sensing. In addition, military applications for RF transmitters and receivers include all-weather radar, surveillance, reconnaissance, electronic attack and communications systems. GaN and SiC can potentially operate from VHF through X-band frequencies while providing higher breakdown voltage, better thermal conductivity and wider transmission bandwidths than conventional devices.

It is well known that Silicon Carbide is one of the most difficult machining materials, due to its chemically inert properties involving the high energy Si-C bond. Currently, inductively couple plasma etching is widely used to etch vias in the SiC
substrate selectivity of the etching mask and time-consuming preparation required for
plasma processing even when the thickness of the silicon carbide substrates is reduced
down to 100 μm by polishing. In addition, there can be formation of pillars caused by
micromasking during ICP etching, which will hinder the subsequent metallization in the
via holes. It has reported that the mechanism of the formation of pillars was
redeposition of the nonvolatile etching products NiSiF, generated by a chemical
combination of Ni from the commonly used metal mask and SiFx species during
etching. Although the micromasking effect can be minimized by introducing an Ar
pretreatment as well as mixed CF₄ with SF₆/He gases, the low etching rate is still an
obstacle for efficiency and large scale production of via holes on SiC substrates. So far,
the highest etching rate reported is approximate 2 μm/min. The typical plasma etch
rates for 4H and 6H SiC substrates are 0.2-1.2 μm/min, therefore, even for a thinned-
down substrates of 100 μm, the etch time is generally long (1.4 - 6 hours).

There is an interest in developing laser drilling processes for creating through-
wafer vias in SiC substrates for devices as an attractive alternative to traditional
microelectronic fabrication processing, such as wet chemical and plasma-based dry
etching. Laser drilling can create via holes in substrates without having a metal
mask fabricated on the wafer and in particular for standard thickness substrates would
give added flexibility for creating custom patterns in the substrates through computer
control of the laser drilling location and would also eliminate the need for wafer thinning
prior to via formation. Moreover, there are no pillars formed during laser ablation
process. Via holes with diameter 60-200 μm demonstrated. In order to increase
circuit density, there is a need to form via holes with smaller diameter. It is also possible
to drill the via hole directly under the source contact metallization of the FETs with the smaller dimension via hole technology, and this would effectively decrease the junction temperature and also the reduce the inductance of the via holes. In this chapter, the fabrications of via holes with diameter ranging from 10 to 70 µm and also rectangular via holes in SiC substrate were demonstrated. The dependence of drilling rate and the shape of via holes on the diameter of via holes were studied.

8.2 Experimental

2 in. diameter undoped Silicon Carbide substrates were used in this work and the samples were drilled with a JPSATM IX-260 ArF excimer laser system (λ= 193 nm). A convex/convex/convex tripler objective lens with a meniscus corrector was used to correct the spherical aberration and the focal length of the tripler was 10 cm. A metal mask was installed in the light path and the openings on the mask were imaged onto the target surface with a demagnification of 23. If the same size via holes are drilled, there is no need to change this metal mask. Thus, the steps of standard photolithography and metal deposition of thick Ni layer used to form the dry etch mask can be skipped. However, the laser drill system is equipped with a computer controlled motor-driven mask holder to produce via holes of different sizes on the same wafer. 4-6 different via hole patterns can be fitted on the same metal mask and the patterns can be changed automatically.

A schematic diagram of experimental set-up is shown in Figure 8-1. In the beam delivery viewing image of the drilled surface, the CCTV could be automatically adjusted parfocally and coaxially to the focused laser beam spot. The CCTV consisted of a multi-element objective lens with coarse/fine focus barrel, a kinematic mirror mount, a CCD high resolution camera with lens and corrective optics, and a 15” monitor with electronic
crosshair. The sample stage was designed to accommodate 6 inch wafers. Two He-Ne lasers were used to guide the high-accuracy air-bearing x-y linear-motor sample stage, and the minimum stage movement was 0.1µm/step. The stage had an accuracy of +/- 3 µm over a full range of motion with a stage velocity of 6-8 inches per second; the stage position could be programmed with a resolution of +/- 1 µm and stage movement repeatability of +/- 1 µm.

The laser pulse duration was fixed at 25 ns and the repetition rate was set at 100 Hz in this study. The energy density of the focused processing beam was in the range 3-12 J/cm². Microposit 1045 photoresist was coated on the SiC samples prior to the laser drilling as a blank mask to protect the surface from the debris around the drilling zone. The resist was removed after the drilling by dipping the sample in acetone. Circular via holes with diameters of 10, 25, 50, and 70 µm as well as rectangular via holes with the dimension of 10 µm × 100 µm, 20 µm × 100 µm and 30 µm × 100 µm were drilled using circular and rectangular metal masks installed in the light path as shown in Figure 8-1. The shape and depth of the drilled via holes and trenches were studied by dicing across the openings, and then examined with a scanning electron microscopy (SEM).

### 8.3 Results and Discussion

Figure 8-2 illustrates the drilling rate of 4H-SiC as a function of A) opening size and B) diameter via hole, which were around three orders of magnitude faster than the rate of etching SiC with conventional ICP. A drill rate of 10.2 µm/sec corresponds to an ablation rate of 0.1 µm/pulse at 100 Hz. When the diameter of the via holes was decreased, the drilling rate increased and reached a maximum at around 18 µm/sec for the 10 µm via opening employed. The system utilized was a research type equipment
and the maximum focused image of the UV laser light on the drill surface was limited to around 220 μm × 320 μm. With such a small field size, it would take an unreasonable long drill time, 456 days, to process a 3” wafer. However, there are several higher powered lasers commercially available, such as Coherent’s LPX Pro series, which can deliver similar fluences with much larger beam spot size, around 1.2 cm × 0.5 cm for 450 mJ. With production type systems, only seventy-six of 24-second exposures, or 30 minutes, are needed to process a 3” wafer. Thus, multiple via holes can be fitted within the larger field dimension and can be drilled at the same time to enhance the throughput.

In the previous work, the drilling rate of via holes were strongly dependent on the opening size of the via hole in glass substrates was observed. This drilling rate increase for the smaller via hole was attributed to the reflected laser light from the side wall of the via hole dominating the drilling process. The reflected laser light focused on the bottom of the via hole and enhanced the drilling rate. It was also reported that the diminished screening of the plume, when the size of drilled hole was decrease, also increased the drilling rate.

The via hole drilling rate increased linearly with the fluence, regardless with the with 50 μm opening size. The rate increased from 2.3 to 12.4 μm/sec, when the fluence was raised from 3.18 to 11.93 J/cm². Laser drilling with 193 nm light has two kinds of laser-matter interaction in the drilling process, namely photochemical ablation (PCA) and photothermal ablation (PTA), which will simultaneously affect the drilling rate of the material. During the ablation process, the target material absorbed laser energy initially, resulting in the melting of the top layer of the SiC. The molten material continues to absorb laser energy, causing the vaporization of the drilled region.
Following the vaporization of the material surface and the formation of saturated vapor pressure (recoil pressure), the local pressure was enhanced greatly, which led to extraction of molten material from the ablation zone. After pushing out the debris, the surface of solid SiC on the bottom of via hole was again exposed to the laser beam and absorbed energy, becoming molten again. The via hole was produced by repeating above process many times. The debris generated by laser drilling was recast around the via hole, most of it just loosely attached on the SiC surface, which could be removed easily in the presence of photoresist followed by acetone rinse in ultrasonic bath. Figure 8-3 shows a photograph of arrays of via holes ranging from 10, 25, 50, and 70 μm drilled on the SiC surface after the photoresist removal and the debris generated by laser drilling left on the SiC were not observed after this cleaning.

Figure 8-4 shows the cross sectional view of circular via holes with the diameter of 10, 25, 50, and 70 μm and depth around 100 μm. There were some common and distinct features among these via holes. The side wall of all these via holes had inclined slopes around 4-6 degrees. When the via hole depth became deeper, the drilled surface moved away from the created the inclined sidewall. The debris observed inside the 10 μm via hole was left from the dicing of the via holes. Because of this inclined side wall, once the drilled depth extended beyond 50 μm, a pointed bottom was observed for the 10 μm diameter via hole, unlike the larger diameter via holes, which exhibited a flat bottom. This problem was corrected by moving up the sample stage during the drilling to put the drilling on the laser focus plane. However, it was very difficult to obtain a cross-sectional view of via holes showing a flat drilled bottom surface with the 10 μm via hole. We have confirmed the effect of stage movement on improving the shape of the via hole.
with the rectangular via hole, which is described below. The dimension of the typical via hole for III-V compound semiconductor devices is > 70-80 μm, and the width of the source contact metal of the FET is less than 25-30 μm. Thus, the via holes are usually fabricated under the source contact pads outside the device active area and the metal air-bridge is used to connect the source contacts of the discrete devices in the multiple finger power device. If the via hole can be fabricated smaller enough and fitted directly under the source metal contact of the FET, this approach offers significant advantages, such as simplifying the power device fabrication process by eliminating the metal air-bridge, improving the device heat dissipation by moving the via hole closer to the gate area, reducing the die size by eliminate the front side source contact pad. With this approach, the source contacts of the discrete FETs are directly connected to the back-side ground plan and no air-bridge is needed.

Figure 8-5 shows a photograph of three different sizes of rectangular via holes drilled on via holes and the circular via holes. The via holes with 10 μm × 100 μm, 20 μm × 100 μm, and 30 μm × 100 μm were drilled using a metal mask with an opening of 10 μm × 100 μm installed in the path of the UV beam, which was de-magnified and focused on the SiC substrate. Multiple exposures were used to drill the larger rectangular via holes. For the 20 μm × 100 μm and 30 μm × 100 μm via holes, the sample stage was programmed to move 10 μm for 20 μm × 100 μm via hole and two 10 μm steps for 30 μm × 100 μm via holes during the exposure, as illustrated in Figure 8-6. As described above, due to the inclined side wall, via holes with an opening of 10 μm showed a pointed bottom once the drilled depth beyond 50 μm, unlike the larger diameter via holes, which exhibited a flat bottom, shown in Figure 8-7B. This problem
was corrected by moving up the sample stage during the drilling. As shown in Figure 8-7A, cross-sectional SEMs of via hole with a flat bottom and almost no inclined slope were achieved by raising the sample stage 30 μm three times after the via hole been drilled 30 μm. This stage movement was automatically controlled and programmed to move back the original height and to the new location before drilling the next set of via holes.

8.4 Summary

In this chapter, the relationship between the via hole entrance diameter and laser drilling rate as well as energy density applied during processing of SiC substrates was investigated. The laser ablation approach for SiC via hole formation exhibits a very high drilling rate, accompanied with a smooth side wall and hole bottom, which will benefit subsequent metallization. The laser drilling approach exhibits advantages in via holes fabrication, and is an efficient and via holes showed a uniform size and spacing, which means the laser micromachining is attractive for large scale production in the processing of SiC microelectronic device manufacture.
Figure 8-1. Schematic of the excimer laser drilling system.
Figure 8-2. The drilling rate of SiC. A) Drilling rate of 4H-SiC as a function of opening size at energy density is 11.93 J/cm$^2$. B) Drilling rate as a function of energy density for the vias with the diameter of 50 μm.
Figure 8-3. Photograph of a SiC sample drilled with four different sizes of circular via holes ranging from 10, 25, 50, and 70 μm.
Figure 8-4. Cross-sectional view of SEM images of via holes with different diameters. A) 70 μm, B) 50 μm, C) 25 μm and D) 10 μm.
Figure 8-5. Photograph of arrays of rectangular via holes with the dimension of (column on the left) 10 μm × 100 μm, (column in the middle) 20 μm × 100 μm and (column on the right) 30 μm × 100 μm drilled on the SiC wafer.
Figure 8-6. Cross-sectional view of SEM imagines of rectangular via holes with 90-100 μm in depth and top opening dimension of 10 μm × 100 μm, 20 μm × 100 μm and 30 μm × 100 μm (From left to right).
Figure 8-7. The cross-sectional view of rectangular via hole with width of 10 μm and depth around 90 μm. A) with and B) without stage-moving process, the latter one shows a pointed bottom.
CHAPTER 9
CONCLUSIONS

In Chapter 2, the effects of source field plates on AlGaN/GaN High Electron Mobility Transistor reliability under off-state stress conditions were investigated using step-stress cycling. The source field plate enhanced the drain breakdown from 55V to 155V and the critical voltages for off-state gate stress from 40V to 65V, as compared to the devices without the field plate, these results were consistent with the electric field simulation and drain IV characteristics of HEMTs with and without source field plate. Transmission electron microscopy (TEM) analysis was used to examine the degradation of the gate contacts and revealed the presence of cracking due to the inverse piezoelectric effect that appeared on both source and drain side of the gate edges. In addition, the existence of a thin oxide layer between the Ni gate contact and AlGaN layer was apparent, and both Ni and oxygen diffused into the AlGaN donor layer. After the step-stress cycling, new threading dislocations, which provided additional passage for the gate leakage current, were also observed.

The significant improvement of AlGaN/GaN HEMT stability by using Pt-based gate metallization instead of the conventional Ni/Au was demonstrated in Chapter 3. The off-state critical voltage was increased from around 45-65 to >100V, and changes of the drain current, drain current on/off ratio, Schottky barrier height and reverse bias gate leakage were minimized. There was no degradation observed for the HEMTs with Pt/Ti/Au gate metallization. Besides electrical field, the reverse bias gate leakage current and the stability between the gate metal contact and semiconductor contribute to the occurrence of a critical voltage. The better thermal stability and higher Schottky
barrier height of Pt to GaN (1.23 eV compared to 1.09 eV for Ni) benefits such improvement.

The effects of off-state stress and sample temperature on the trap densities in AlGaN/GaN high electron mobility transistors (HEMTs) were studied in Chapter 4. Two different trap densities were obtained using the slope of sub-threshold drain current measurements. The trap density dominated at the lower temperature range almost doubled from $1.64 \times 10^{12}$ to $3.3 \times 10^{12} /\text{cm}^2\text{-eV}$ after HEMTs reached a critical voltage for a permanent sudden-increase of the gate current during the off-state drain voltage step-stress. The trap density at the higher temperature range was created by the ion bombardment during inductively coupled plasma (ICP) etching for device isolation etching, which only slightly increased from $8.1 \times 10^{12}$ and $9.2 \times 10^{12} /\text{cm}^2\text{-eV}$ after the device stress. The trap densities were also strongly dependent on drain bias voltage. Measurements conducted at higher drain bias voltages exhibited larger trap density due to more hot electrons generated at these conditions.

In Chapter 5, the passivation properties, including current collapse and rf performance, of HfO$_2$, SiN$_x$ and Al$_2$O$_3$ on AlGaN/GaN HEMTs were compared. Both HfO$_2$ and Al$_2$O$_3$ thin films deposited by ALD produce improvements in drain-source current due to a reduction of surface depletion effects but are less effective than SiN$_x$ for the given AlGaN/GaN epi structure. However, the oxides produce superior RF performance to SiN$_x$ and should offer advantages with respect to gate definition because of their reduced aspect ratios.
Chapter 6 investigated the effect of buffer layer on AlGaN/GaN high electron mobility transistor reliability (HEMTs). Three different types of buffer layers were used in this experiment including an 1 or 2 μm of GaN buffer layer and a AlGaN/GaN composite buffer layer beneath the two dimensional electron gas channel. The reliability of AlGaN/GaN HEMTs was improved significantly by employing the thinner and the composite buffer layer. The HEMTs with the thick GaN buffer layer showed the lowest critical voltage ($V_{\text{cri}}$) during off-state drain step-stress, which was increased by around 50 and 100% for devices with the composite AlGaN/GaN buffer layers and thinner GaN buffers, respectively. In addition, a similar trend was observed in the isolation breakdown voltage ($V_{\text{iso}}$) measurements, with the highest $V_{\text{iso}}$ achieved based on thin GaN or composite buffer designs (600-700V), while a much smaller $V_{\text{iso}}$ of ~200V was measured on HEMTs with the thick GaN buffer layers. Those improvements are attributed to the increasing of defect density, which consequently modifies the electric field at the drain side of the gate edge by using different buffer structures.

The radiation effects in the GaN-based HEMTs, including the studies on the reliability of proton-irradiated InAlN/GaN and the effects of proton energy and dose on the dc characteristics and reliability of AlGaN/GaN HEMTs were reported in Chapter 7.

The reliability of InAlN/GaN high electron mobility transistors (HEMTs) was improved significantly after proton irradiation. The critical voltage ($V_{\text{cri}}$) of off-state drain step stress and the drain breakdown voltage ($V_{\text{BR}}$) were increased more than 100% and 50%, respectively for the HEMTs irradiated with protons. The typical critical voltage for un-irradiated devices was 45 to 55 V. By sharp contrast, no critical voltage was detected for proton irradiated HEMTs up to 100 V, which was limited by the instrument used in
the experiment. In addition, the drain breakdown voltages were below 100 V in the reference devices and increased to above 150 V after 5 MeV proton irradiation with a dose of 5×10^{15} cm^{-2}. In this study, HEMTs were subjected with different energies of 5-15 MeV at a fixed dose of 5 × 10^{15} cm^{-2}, or to a different doses of 2 × 10^{11}, 5 × 10^{13} or 2 × 10^{15} cm^{-2} of protons at a fixed energy of 5 MeV. After electrical stressing, no degradation was observed for the drain or gate current-voltage characteristics of the proton-irradiated HEMTs. On the contrary, for the un-irradiated HEMTs, there were the drain current decrease around ~12%, and the reverse bias gate leakage current increase more than two orders of magnitude as a result of electrical stressing.

AlGaN/GaN HEMTs were irradiated with proton irradiation energies of 5, 10 and 15 MeV at fixed fluence of 5 × 10^{15} cm^{-2}. Sub-threshold drain leakage current and reverse gate I-V decreased more than one order of magnitude for all cases due to the increase of resistivity of the HEMT channel after proton irradiation. More severe degradation with decreasing proton energy is due to the increase in linear energy transfer and corresponding increase in non-ionizing energy loss with decreasing proton energy in the active region of the HEMTs.

The dc characteristics as well as critical voltage of the drain-voltage electrical step-stress of AlGaN/GaN high electron mobility transistors (HEMTs) were measured prior to and post 5 MeV proton irradiation at doses from 10^9 to 2×10^{14} cm^{-2} to evaluate the feasibility of AlGaN/GaN HEMTs for space applications, which need to demonstrate radiation hardness of various irradiations. On-chip transmission line method (TLM) was used to extract contact and sheet resistances. The threshold of contact resistivity (R_C) and transfer resistance (R_T) degradation was at a proton dose of 5×10^9 cm^{-2}, however,
the threshold for sheet resistance ($R_s$) degradation was much higher at $2 \times 10^{13}$ cm$^{-2}$ as compared to those for $R_T$ and $R_C$. For the dc characteristics, minimal degradations of saturation drain current ($I_{DSS}$), transconductance ($g_m$), electron mobility, and sheet carrier concentration were observed for the samples irradiated with proton dose below $2 \times 10^{13}$ cm$^{-2}$, while the reduction of these parameters were 15%, 9%, 41% and 16.6%, respectively, for the device irradiated with $2 \times 10^{14}$ cm$^{-2}$ of protons. Drain breakdown voltage ($V_{BR}$) and of critical voltage ($V_{cri}$) unexpectedly increased 37% and 45%, respectively for the devices irradiated with $2 \times 10^{14}$ cm$^{-2}$ of protons. Gate and drain pulse measurement were also conducted to study the trap characteristics. Both measurements showed apparent reduction of $I_{DSS}$ for the HEMTs irradiated at proton doses higher than $2 \times 10^{12}$ cm$^{-2}$, which meant more traps were introduced for the implanted HEMTs. The improvements of drain breakdown voltage ($V_{BR}$) and critical voltage ($V_{cri}$) were attributed to the modification of the depletion region due to the introduction of a higher density of defects after irradiation at a higher dose.

In Chapter 8, Ar/F$_2$ based UV laser drilling ($\lambda = 193$ nm) with a pulse width of $\sim 30$ nsec and a pulse frequency of 100 Hz has been used to fabricate vertical electrical interconnects (vias) for AlGaN/GaN high electron mobility transistor (HEMTs) devices on silicon carbide (SiC) substrate. The relationship between the via hole entrance diameter and laser drilling rate as well as energy density applied during processing of GaN HEMTs on SiC substrates was demonstrated. A high yield of SiC through wafer via holes with a diameter of 10-50 $\mu$m without trenching or micromasking, which will benefit the subsequent metal plating and get a good electrical connection, can be achieved using an inductively coupled plasma etch under SF$_6$/O$_2$ + Ar plasma. The laser drilling
approach for SiC via hole formation exhibits not only the high drilling rate (229-870 µm/min), but also generate a smooth side wall and hole bottom without extended defects, micro pillars. It is an efficient and economical alternative to conventional SiC via holes processing. Furthermore, the array of via holes showed a uniform size and spacing, which means the laser micromachining is attractive for large scale production in the processing of SiC based GaN HEMTs manufacture.
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BIOGRAPHICAL SKETCH

Lu Liu was born in Beijing, China. He began his higher education at Beijing University of Technology in China and earned his Bachelor of Engineering in 2005. From 2005 to 2008, Lu Liu served as research assistant at Beijing University of Technology and Peking University under the guidance of Dr. Hong He, Dr. Haichao Liu and Dr. Jun Ma, his major was heterocatalysis. In December 2009, Lu Liu joined Dr. Fan Ren’s research group at University of Florida and received a Master of Engineering in Chemical Engineering in December 2010. In spring 2011, Dr. Lu Liu enrolled in the Ph.D. program and continued the research in Dr. Fan Ren’s group to further explore his horizon in the field of compound semiconductor microelectronics. Since joining the group Dr. Lu Liu’s research has focused mainly on the development of GaN HEMTs technology, including the fabrication, characterization as well as the study on the reliability and radiation effects in GaN-based HEMTs. After an intensive learning and research study, Dr. Lu Liu graduated in December 2013, with a Doctor of Philosophy in chemical engineering.