HIGH VOLTAGE SWITCHED-MODE STEP-UP DC-DC CONVERTERS IN STANDARD CMOS PROCESS

By

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2013

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To my Mom and Dad

ACKNOWLEDGMENTS

First of all I would like to thank my academic advisors, Dr. Rizwan Bashirullah for his valuable guidance over the course of the last six years. I would also like to thank Dr. David Arnold, Dr. Robert Fox, and Dr. Loc Vu-Quoc for their advice and their willingness to be in my dissertation committee. Thanks are also given to Brian Morgan and Army Research Laboratory for funding support. Thanks to UMC for chip fabrication.

Special thanks are given to Chris Meyer, Christopher M. Dougherty, Deepak Bhatia, Pengfei Li, and Qiuzhong Wu for having useful design related discussions. I would also like to thank Jikai Chen, Yan Hu, Hong Yu, Chunming Tang, Walker Turner, Zhiming Xiao, and Pawan Sabharwal for always being open to answer any question at any time, let it be day or night. Speaking about the classes at UFL, I would like to thanks Dr. Bashirullah for his excellent Advanced VLSI class, Dr. Fox for his Bipolar and MOS design class, especially the simple design related approach and second order analysis, Dr. O for his excellent Microwave IC design class.

Finally, I would like to thank my mom, dad for all their love and support till date.

TABLE OF CONTENTS

page

ACKNOWLEDGMENTS 4

LIST OF TABLES 8

LIST OF FIGURES 9

LIST OF ABBREVIATIONS 15

ABSTRACT 16

CHAPTER

1 INTRODUCTION 18

1.1 Research Background 18
1.2 Recent Progress towards Miniaturization of Step-Up Voltage Converters 20
1.2.1 High-Voltage Step-Up Converters Using Discrete Components 20
1.2.2 Integration of Step-Up Voltage Converters in CMOS Processes 22
1.3 Dissertation Organization 24

2 REVIEW ON SWITCHING STEP-UP VOLTAGE CONVERTERS 25

2.1 Introduction of Switching Step-Up Converters 25
2.2 Basic Switching Step-Up Converter Topologies 25
2.2.1 SI Boost Converter 25
2.2.2 Flyback Converter 28
2.2.3 Switched Capacitor Step-Up Converters 31
2.2.3.1 Ladder (Cockcroft-Walton) 32
2.2.3.2 Dickson charge pump 33
2.2.3.3 Fibonacci converter 34
2.2.3.4 Series-parallel converter 36
2.2.3.5 Summary of SC converters 37
2.3 Averaged Switching Network 37
2.3.1 Averaged L-S-D Network in CCM 37
2.3.2 Averaged L-S-D Network in DCM 39
2.3.3 Small-Signal Analysis of SI Boost Converter in CCM 41
2.3.4 Small-Signal Analysis of SI Boost Converter in DCM 42
2.4 Control Scheme of DC-DC Converters 44
2.4.1 Voltage Mode Pulse Width Modulation (PWM) 44
2.4.2 Current Mode PWM 45
2.4.3 Pulse Frequency Modulation (PFM) 47

3 CUSTOM HIGH VOLTAGE POWER DEVICES IN STANDARD CMOS PROCESS 49

3.1 Introduction of High Voltage Devices 49
3.2 Voltage Limit Effects in Standard CMOS Process 49
3.2.1 Channel Hot Carrier Effects 49
3.2.2 Gate Oxide Breakdown 51
3.2.3 Avalanche Breakdown 51
3.2.3.1 Planar junction edge effects 52
3.2.3.2 Layout improvement techniques 54
3.2.3.3 Open-base transistor breakdown 56
3.2.4 Electromigration 57
3.3 Schottky Barrier Diodes 57
3.3.1 Schottky Barrier Contact in CMOS 57
3.3.2 Guard Rings for SBDs 58
3.3.3 Measurement Results and Parameter Extraction 59
3.4 Power Switches 62
3.4.1 Extended-Drain MOSFET 63
3.4.2 Stacked MOSFET 67
3.5 Performance Comparison 72

4 50-100MHZ 8X HRBRID SI-SC AND SI-FLYBACK CONVERTER IN 130NM CMOS PROCESS 74

4.1 Introduction of Hybrid Converters 74
4.2 Hybrid Converter Topologies 74
4.2.1 SI-SC Converter 76
4.2.2 SI-Flyback Converter 78
4.3 Microfabricated Air-Core Power Magnetics 80
4.3.1 Layout Design 81
4.3.2 Process Flow 82
4.4 Current Mode PWM Controller 83
4.4.1 Voltage Feedback Loop 83
4.4.2 Current Feedback Loop 85
4.5 Experimental Results 89
4.5.1 Microfabricated Air-Core Inductor and Transformer 89
4.5.2 Hybrid SI-SC Converter 91
4.5.2.1 Open loop measurement results 91
4.5.2.2 Close loop measurement results 93
4.5.3 Hybrid SI-Flyback Converter 95
4.6 Die Photo and Performance Summary 97

5 MODELING AND PERFORMANCE ANALYSIS OF HYBRID SI-SC STEP-UP CONVERTERS 100

5.1 Introduction of Hybrid SI-SC Converter 100
5.2 Hybrid SI-SC Step-Up DC-DC Converter 102
5.2.1 Generalized Hybrid SI-SC Converter Topology 102
5.2.2 Analysis Model 104
5.3 Model Validation 111

5.4 Experimental Results 115
5.5 Modeling and Analysis Conclusions 122

6 MINIATURE HIGH VOLTAGE HYBRID STEP-UP POWER CONVERTER FOR SMART PIEZOELECTRIC MICROSYSTEMS 123

6.1 Introduction of High Voltage Converters in Microsystems 123
6.2 High Voltage Hybrid SI-SC Step-Up Converter 125
6.2.1 Optimal Design Procedure 127
6.3 Hysteretic Controller 132
6.4 Experimental Results 137
6.5 Preliminary Demo of a Smart Piezoelectric Microsystem 142

7 CONCLUSIONS AND FUTURE WORKS 145

7.1 Research Summary and Contributions 145
7.2 Future Works 147

APPENDIX

A D_2 DERIVATION FOR SI AND HYBRID SI-SC CONVERTER IN DCM 149

A.1 Derivation of D_2 for SI Step-Up Converter in DCM 149
A.2 Derivation of D_2 for Hybrid SI-SC Converter (N_{SC}-Stage) 150

B SMALL SIGNAL AC ANALYSIS FOR SI BOOST IN CCM 152

C SMALL SIGNAL AC ANALYSIS FOR SI BOOST IN DCM 155

D MSP430L092 CODE FOR SMART PIEZO MICROSYSTEM DEMO 157

LIST OF REFERENCES 164

BIOGRAPHICAL SKETCH 171

LIST OF TABLES

Table		page
2-1	Summary of CCM-DCM characteristics for the SI boost	28
2-2	Summary of CCM-DCM characteristics for the flyback converter	31
2-3	Summary of steady state characteristics for SC step-up converters	37
3-1	Extracted parameters for n- and p-type SBDs with and without guard rings in 130nm CMOS	62
3-2	Summary of measured DC parameters for fabricated extended-drain and stacked MOSFETs	71
4-1	Performance summary and comparison for implemented SI-SC and SI-flyback converter	98
4-2	Performance Summary and Comparison for the hybrid SI-SC converter	99
5-1	Defined charge and duty cycle vector for the hybrid SI-SC step-up converter	108
5-2	Summary of steady state model equations for the hybrid SI-SC step-up converter	110
5-3	Important device parameters used in SPICE simulation for SI converter (N_{SC}=0)	111
5-4	Important device parameters used in SPICE simulation for hybrid SI-SC converter (N_{SC}=1)	111
5-5	Important device parameters used in SPICE simulation for hybrid SI-SC converter (N_{SC}=4)	111
5-6	Characteristic summary of stacked NMOS switches	116
5-7	Characteristic summary of schottky barrier diodes	116
6-1	Defined charge and duty cycle vector for the hybrid SI-SC step-up converter	129

LIST OF FIGURES

Figure page

1-1 Average power and energy required for mobile microsystems (<10W) [3] 18

1-2 Power and voltage requirements for subsystems under development in MAST [3] 19

1-3 CMOS process scaling trends 20

1-4 A hybrid boost / switched capacitor converter and push-pull high voltage driver implemented on 3mil standard PC board for micro-robotics 21

1-5 A bidirectional flyback converter for piezoelectric micro-robots 21

1-6 A SoC implemented in a 0.13µm SiGe CMOS technology for a moving microrobot [13] 22

1-7 Envisioned power management platform for autonomous microsystems 23

2-1 An ideal SI boost converter 25

2-2 SI boost converter equivalent circuits and waveforms 26

2-3 SI boost converter equivalent circuit and waveforms in DCM 27

2-4 An ideal flyback converter 29

2-5 Flyback converter equivalent circuits and waveforms 30

2-6 Flyback converter equivalent circuit and waveforms in DCM when inductor current is zero 30

2-7 An ideal SC ladder converter 32

2-8 Equivalent circuits of the SC ladder converter 32

2-9 An ideal Dickson charge pump (*n* is even) 33

2-10 Equivalent circuits of the Dickson charge pump 34

2-11 An ideal SC Fibonacci converter (*k* is odd) 35

2-12 Equivalent circuits of the SC Fibonacci converter (*k* is odd) 35

2-13 An ideal SC series-parallel converter 36

2-14 Equivalent circuits of the SC series-parallel converter 36

2-15 L-S-D network and its DC and AC averaged model in CCM 38

2-16 L-S-D network and its DC and AC averaged model in DCM 40

2-17 Small-signal model of the SI boost converter in CCM 41

2-18 Small-signal model of the SI boost in DCM 42

2-19 Voltage mode PWM controller and waveforms 45

2-20 Current mode PWM control for SI boost 46

2-21 Block diagram of PFM control loop for SI boost 47

3-1 Channel hot carrier effects in the cross-section of a saturated nMOS 50

3-2 Typical bias-lifetime behavior for minimum length MOS transistors [33] 50

3-3 Electrical field and potential distribution for an abrupt parallel-plane P+/N junction 51

3-4 The planar junction created by diffusion through a window in a silicon dioxide mask [36] 53

3-5 Breakdown voltages of cylindrical and spherical junctions normalized to the parallel-plane junction [36] 54

3-6 The planar junction with a floating field ring 55

3-7 Comparison of the normalized breakdown voltages of cylindrical junctions with and without a single floating field ring [36] 55

3-8 A planar junction with metal field plate over the edges 56

3-9 A parasitic PNP transistor in CMOS process 56

3-10 Layouts and cross-sections of n-type and p-type SBDs 58

3-11 Layouts and cross-sections of n-type and p-type SBDs with p^+/n^+ guard rings .. 59

3-12 Measured current densities versus bias voltage for n-type and p-type SBDs with and without p^+/n^+ guard rings (GR) 60

3-13 Extracted slopes and zero-bias current density for n- and p-type SBDs in 130nm CMOS 61

3-14 Extracted piecewise linear model parameters V_D, R_D for n- and p-type SBDs in 130nm CMOS 62

3-15 The layout, cross-section, symbol and cell parameters of tested thin-oxide extended-drain MOSFET 64

3-16 Measured leakage current densities for tested thin-oxide extended-drain MOSFET cells with V_{GS}=0V 65

3-17 Measured current densities for tested thin-oxide extended-drain MOSFET cells with V_{GS}=1.2V 65

3-18 The layout, cross-section, symbol and cell parameters of tested thick-oxide extended-drain MOSFET 66

3-19 Measured leakage current densities for tested thick-oxide extended-drain MOSFET cells with V_{GS}=0V 66

3-20 Measured current densities for tested thick-oxide extended-drain MOSFET cells with V_{GS}=3.3V 67

3-21 On-state and off-state gate biasing stacked NMOS switches 68

3-22 The layout and cross-section of a switch stacking a thick-oxide NMOS on the top of a thin-oxide NMOS 69

3-23 Measured on-state and off-state current density of the stacked switch with a 3.3V thick-oxide NMOS on the top of a 1.2V thin-oxide NMOS 70

3-24 The layout and cross-section of a switch stacking a thick-oxide NMOS on top of a thick-oxide low-V_T NMOS in T-WELL 70

3-25 Measured current density of the stacked switch with a 3.3V thick-oxide NMOS on the top of a 3.3V thick-oxide low-V_T NMOS 71

3-26 The silicon limit and performance comparison for developed power devices 72

4-1 Voltage conversion ratio of a SI boost converter considering inductor resistive loss [24] 75

4-2 A hybrid SI/SC converter implemented in 130nm CMOS 76

4-3 Representative waveforms for the hybrid SI/SC converter 77

4-4 Schematic of a hybrid SI/flyback converter implemented in 130nm CMOS 78

4-5 Representative waveforms for the hybrid SI/flyback converter 80

4-6 General layout of fabricated inductors and transformers 81

4-7 Cross-sectional view of the microfabrication process flow 82

4-8 A current mode PWM controller for the hybrid SI/SC converter 83

4-9 Schematic of the error amplifier in the current mode controller 85

4-10 Demonstration of loop instability in a current mode controller 87

4-11 Schematic of the current sensing circuit 88

4-12 Schematic of the oscillator (OSC) and current ramp generator 89

4-13 Microfabricated inductor and measured characteristics [56] 89

4-14 Microfabricated transformer and measured characteristics 90

4-15 Measured waveforms of the hybrid SI/SC converter at 100MHz 91

4-16 Measured efficiencies with external driving clocks and a 24nH commercial inductor 92

4-17 Wire bonding for the 14nH microfabricated inductor on a custom PCB for the hybrid SI/SC converter 93

4-18 Measured time-domain waveforms of the output voltage and switching node voltage V_X when measured with the microfabricated inductor at ~100MHz 93

4-19 Measured efficiencies for the close-loop hybrid SI/SC converter with microfabricated and commercial inductor respectively 94

4-20 Transient response for the SI/SC converter using a commercial 43nH inductor 95

4-21 Measured waveforms of the SI/flyback converter using a commercial transformer 96

4-22 Measured efficiencies using external driving clocks for the hybrid SI/flyback converter 96

4-23 Die photo of the hybrid SI/SC and SI/flyback converter in a 130nm CMOS process 97

5-1 Schematic of the generalized hybrid SI-SC step-up converter with an N_{SC}-stage SC ladder. 102

5-2 Ideal switching voltage and current waveforms in SI stage 103

5-3 A general circuit model that accounts for non-ideal conduction and dynamic switching losses. 105

5-4 Simplified models of passive components and high-voltage devices. 106

5-5 Charge flows in the hybrid SI/SC converter 107

5-6 Power efficiency obtained from model and SPICE simulation for the three hybrid SI/SC converters 112

5-7 Output voltage obtained from model and SPICE simulation for the three hybrid SI/SC converters 114

5-8 Schematics of three fabricated hybrid SI-SC converters 117

5-9 Die photos of three hybrid converters 119

5-10 Measurement and model results of the first hybrid converter (N_{SC}=0) with V_{IN}=1.2V and D_1=0.8 120

5-11 Measurement and model results of the second hybrid converter (N_{SC}=1) with V_{IN}=1.2V and D_1=0.8 121

5-12 Measurement and model results for the third hybrid converter (N_{SC}=4) with V_{IN}=1.2V and D_1=0.8 121

6-1 Power requirements for various autonomous microsystems 125

6-2 Implementation detail of the high voltage hybrid SI-SC step up converter 127

6-3 A DC circuit model for performance analysis 129

6-4 Charge flow analysis of the hybrid SI-SC step up converter in the two switching phases 129

6-5 Optimal design procedure for the hybrid SI-SC step up converter 132

6-6 Hysteretic controller designed for the hybrid SI-SC step up converter and its sample waveforms 135

6-7 Conditioning circuit for V_{BL} and V_{BH} and hysteretic comparator with programmable window 136

6-8 Onchip linear regulator to generate internal power supply for the controller 137

6-9 Testing board for the hybrid SI-SC step up converter and zoomed-in die photos of the hysteretic controller with stacked NMOS switch and the SC multiplier. 138

6-10 Open loop measurement results with D=0.5 and V_{IN}=3V and power loss distribution when f_s=25MHz and L=1µH 139

6-11 Measured close loop timing waveforms when the hybrid SI-SC converter is tested with L=1µH and V_{IN}=3V 141

6-12 Measured timing waveforms of the hybrid step up converter for positive load transient response with L=1µH and V_{IN}=3V. 141

6-13 Measured timing waveforms with a pseudo piezo load of 1MΩ and 100pF when the reference is modulated 142

6-14 A smart piezoelectric microsystem using the hybrid SI-SC step up converter and a commercial MSP and measurement results 144

A-1 Representative waveforms of the SI step-up converter 149

A-2 Simplified circuit model for the hybrid SI/SC step-up converter 151

B-1 The configuration of a SI boost converter and equivalent circuits in subinterval I and II when operating in CCM 152

B-2 Small signal circuit model and duty-to-output transfer function for the SI boost in CCM 153

C-1 Derived small-signal circuit model and duty-to-output transfer function for the SI boost in DCM 155

LIST OF ABBREVIATIONS

CCM	Continuous current mode
D	Duty cycle of the converter
DCM	Discontinuous current mode
DPWM	Digital Pulse width modulator
ESR	Equivalent series resistance
FOM	Figure of Merit
MAVs	Micro Air Vehicles
PWM	Pulse width modulator
PFM	Pulse-frequency-modulation
RMS	Root mean square
SBD	Schottky Barrier Diode
SC	Switched Capacitor
SI	Switched Inductor
SoC	System-on-Chip
STI	Shallow Trench Isolation
TDDB	Time-Dependent Dielectric Breakdown
T_S, f_s	Switching time period and frequency
UAV	Unmanned Aerial Vehicles
V_{IN}, I_{IN}	Input voltage and input current of the converter
V_{OUT}, I_{OUT}	Output voltage and output current of the converter
VRM	Voltage regulator module

Abstract of Dissertation Presented to the Graduate School
of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Doctor of Philosophy

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December 2013

Chair: Rizwan Bashirullah
Major: Electrical and Computer Engineering

Onchip integration of switched-mode step-up converters in CMOS can be attractive for portable devices powered from single-cell batteries. For instance, some autonomous microsystems, such as life-sized robotic insects that roll, crawl, jump, or fly, require specialized high voltage converters to electrically drive piezoelectric actuators for transforming power into locomotion. In such applications power converters must meet stringent mass and volume requirements, a reality that has led to increasing interest in onchip high-frequency step-up converters.

This work begins with an overview of basic step up converter topologies and CMOS compatible high voltage tolerant device techniques. Analysis shows output voltage is limited by breakdown of critical devices. Three high voltage tolerant devices and two hybrid topologies are then presented, all in 1.2V CMOS. Without adding any extra masking steps, output voltage is extended to 10V, 8x larger than the input. Moreover, microfabricated inductors and transformers are also demonstrated with the two converters for comparable performance but much smaller footprint than commercial counterparts.

Performance of hybrid step-up converters are further analyzed with a general circuit model proposed which uses a theoretic network methodology to evaluate output impedance and to account for various sources of switching loss prevalent at high operating frequencies and in onchip implementations. Unlike previous approaches, ours divides dynamic switching loss into output unrelated and related. It then uses two equivalent input and output resistive loads to model them separately. Comparisons with SPICE simulations and experimental results demonstrate that the proposed approach is accurate for evaluating power efficiency and output voltage.

A complete hybrid SI-SC step up converter with a 4-stage SC ladder multiplier and an inherently-stable hysteretic controller is developed in a 1.2V CMOS process with minimal post-process steps for piezoelectric microsystems. An optimal design procedure based on theoretic network analysis is also presented. Experimental results show the hybrid converter achieves maximum output of 35V at 200μA. Moreover, the hybrid converter is employed with a commercial microprocessor to form a smart piezoelectric microsystem demo for successfully driving a 25Hz resonant piezo fan.

CHAPTER 1
INTRODUCTION

1.1 Research Background

Bug-sized autonomous microrobots that crawl, jump, flap or fly have been developing for 20 years [1][2] to provide a combination of stealth and accessibility to restricted areas, as well as improve portability and enable cooperative group behavior for superior mission capability in possible tasks involving transportation, exploration, surveillance, guidance, inspection, etc. Numerous challenges have been introduced, one of which is to develop a suitable powering system, which at small scales poses a remarkably daunting task. Both a power source (battery) and voltage converter are necessary, and their size and mass are of critical importance to the overall system design.

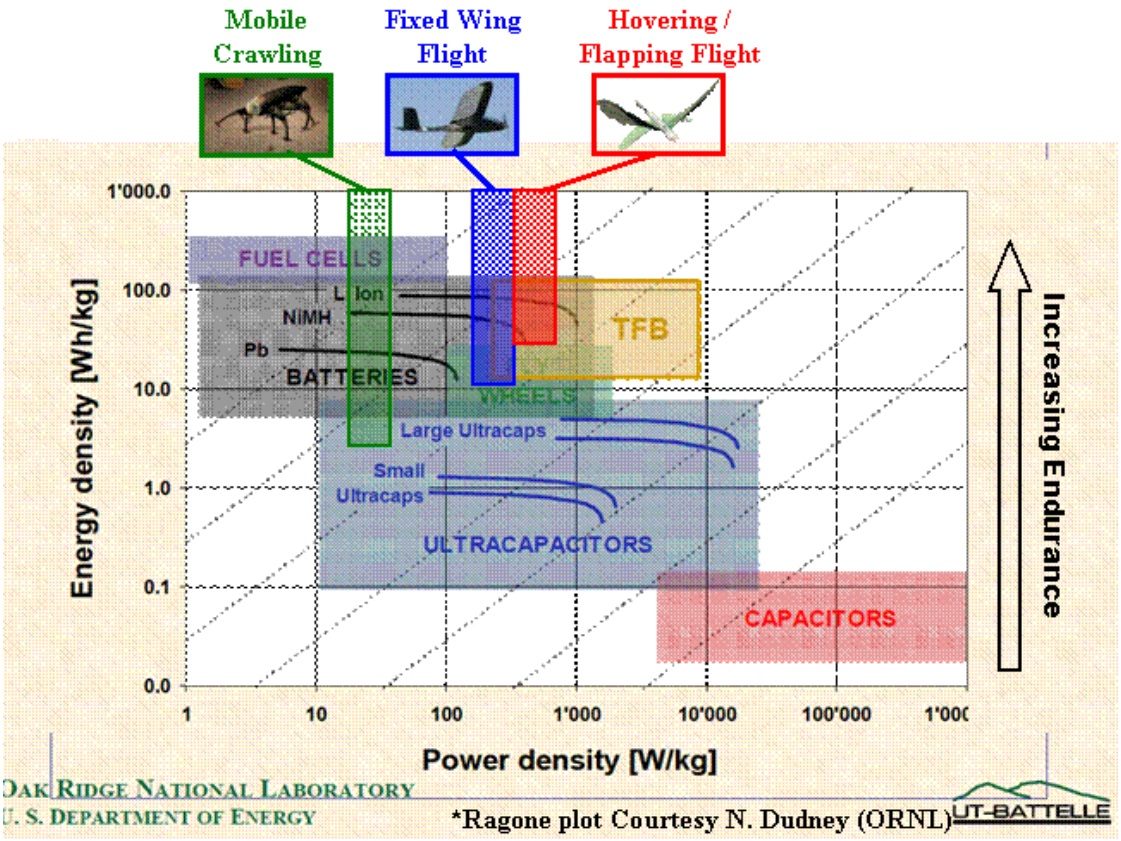


Figure 1-1. Average power and energy required for mobile microsystems (<10W) [3].

Figure 1-1 graphically shows envisioned power and energy densities required for the three locomotion modalities, mobile crawling, fixed wing flight, and hovering / flapping flight [3]. The targeted approximate power density range is estimated as 10-1000 W/kg by assuming ~25-50% of the power source to the total system weight and 50% of overall power delivery/transmission efficiency. Lithium polymer (LiPo) batteries, fuel cells, and energy harvesters are demonstrated as attractive power sources for targeted microsystems [3].

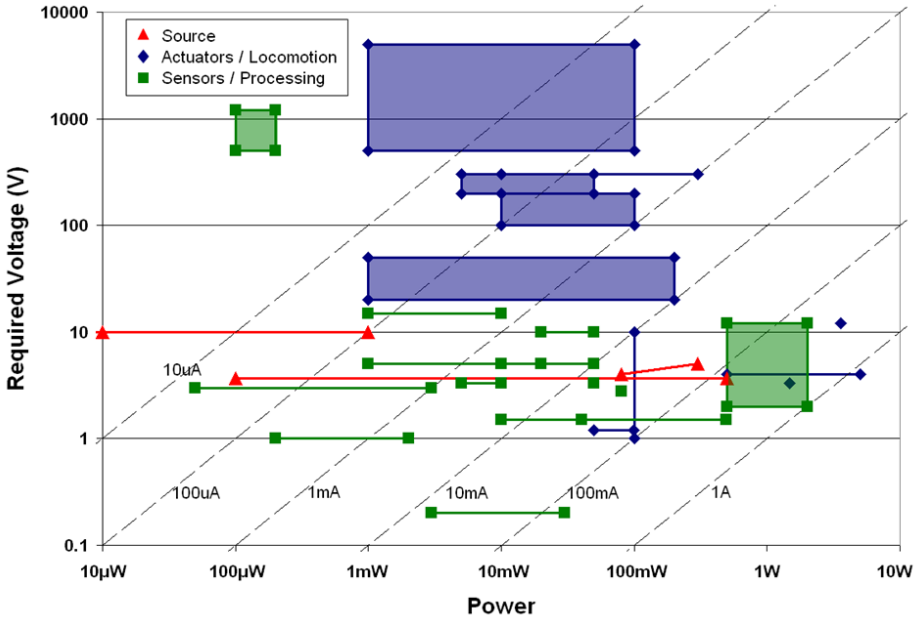
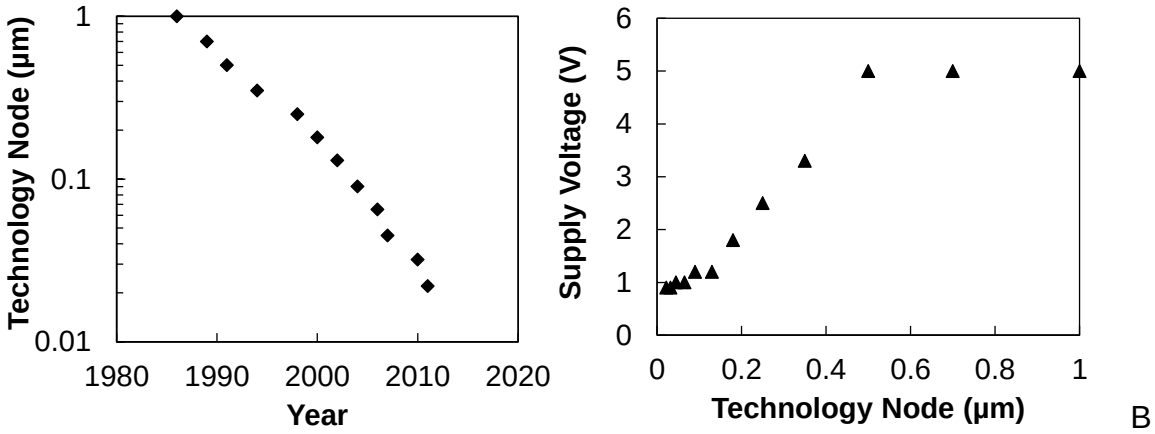


Figure 1-2. Power and voltage requirements for subsystems under development in MAST [3].

Figure 1-2 shows the results of an informal survey (conducted by ARL) concerning the anticipated power and voltage needs for the subsystems under development in the U.S. Army Research Laboratory's Micro Autonomous Systems & Technology (MAST) program. In general, high voltages are required to run piezoelectric [4] or dielectric elastomer [5] actuators for mobility towards the few grams & below range, and low voltages from close to typical battery voltages (within 2-3X of a 3.7V LiPo battery) to as low as 0.2V are needed for very efficient sensing and processing approaches.

Therefore both step-up and step-down voltage converters are required in mm-scale microrobots.

Extensive studies [6][7][8] have been done regarding monolithic step-down buck converters since they are intrinsically easier to be integrated in standard CMOS technologies, thus achieving better performance, smaller footprint, and lower cost as the CMOS technology scales down. Conversely, since the supply and breakdown voltage of the CMOS technology are continuously decreasing as illustrated in Figure 1-3, integration and miniaturization of high-voltage step-up converters become a much more challenging problem. This dissertation is motivated to investigate techniques of miniaturizing step-up voltage converters.



A B

Figure 1-3. CMOS process scaling trends. A) Technology node, B) Supply voltage.

1.2 Recent Progress towards Miniaturization of Step-Up Voltage Converters

1.2.1 High-Voltage Step-Up Converters Using Discrete Components

Several miniature high-voltage step-up converters have been developed using discrete components for micro-robotic applications [4][9][10]. As shown in Figure 1-4, a hybrid boost / switched capacitor converter and push-pull high voltage driver were implemented on 3mil standard PC board utilizing a 22µH inductor, a controller of LT1615-1, 0402 22nF capacitors, high voltage transistors, and 0402 resistors [9]. The

converter achieves an output of 250V and efficiency of ~60%, and the total weight of two populated boards is ~854mg. Figure 1-5 shows another example, a bidirectional flyback converter implemented with a custom transformer [10]. Although the weight is reduced to ~90mg with the same output and efficiency, the converter employs a large number of discrete components and a bulky transformer core, causing its power and energy density insufficient for the stringent power demands of flying micro-robots.

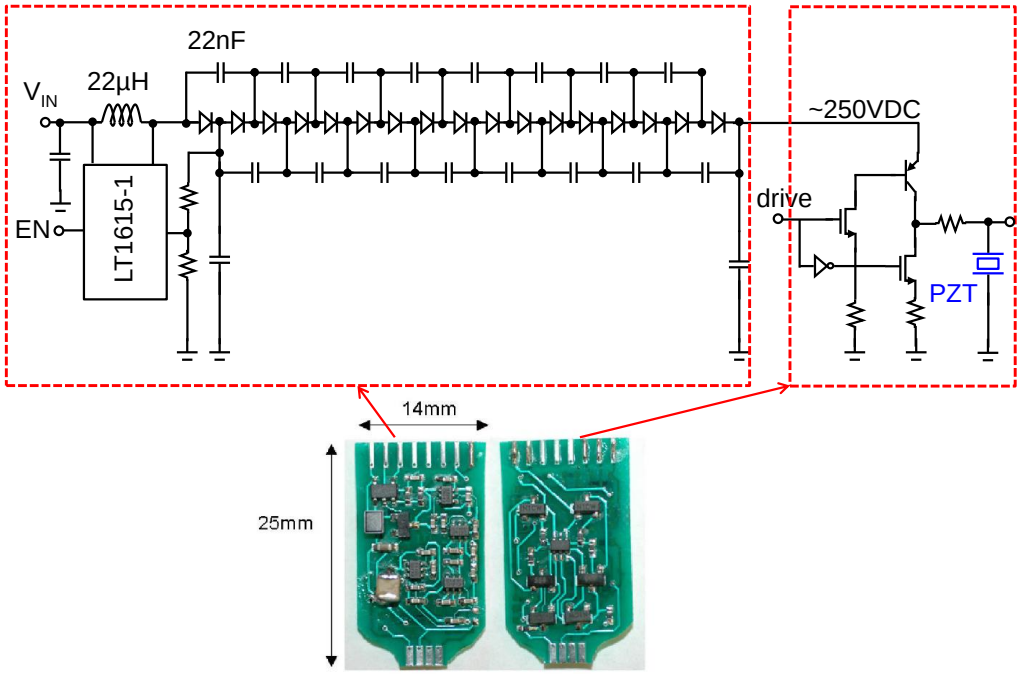


Figure 1-4. A hybrid boost / switched capacitor converter and push-pull high voltage driver implemented on 3mil standard PC board for micro-robotics.

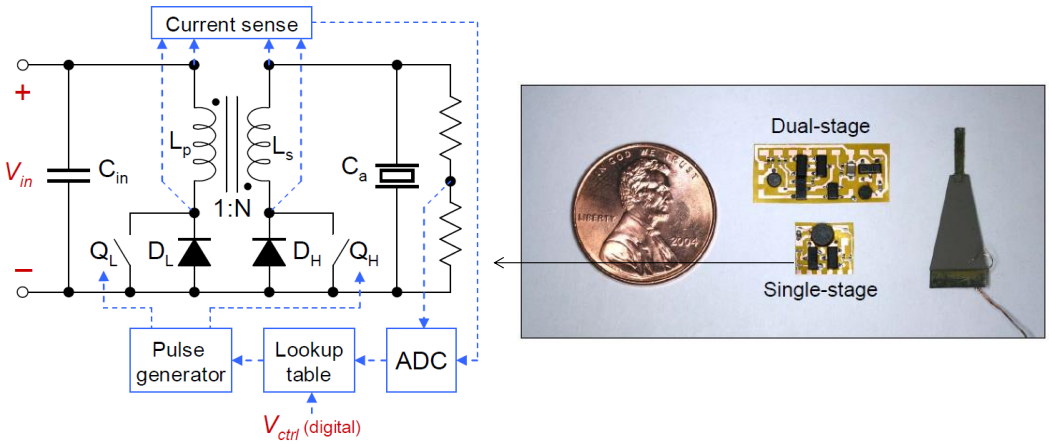


Figure 1-5. A bidirectional flyback converter for piezoelectric micro-robots.

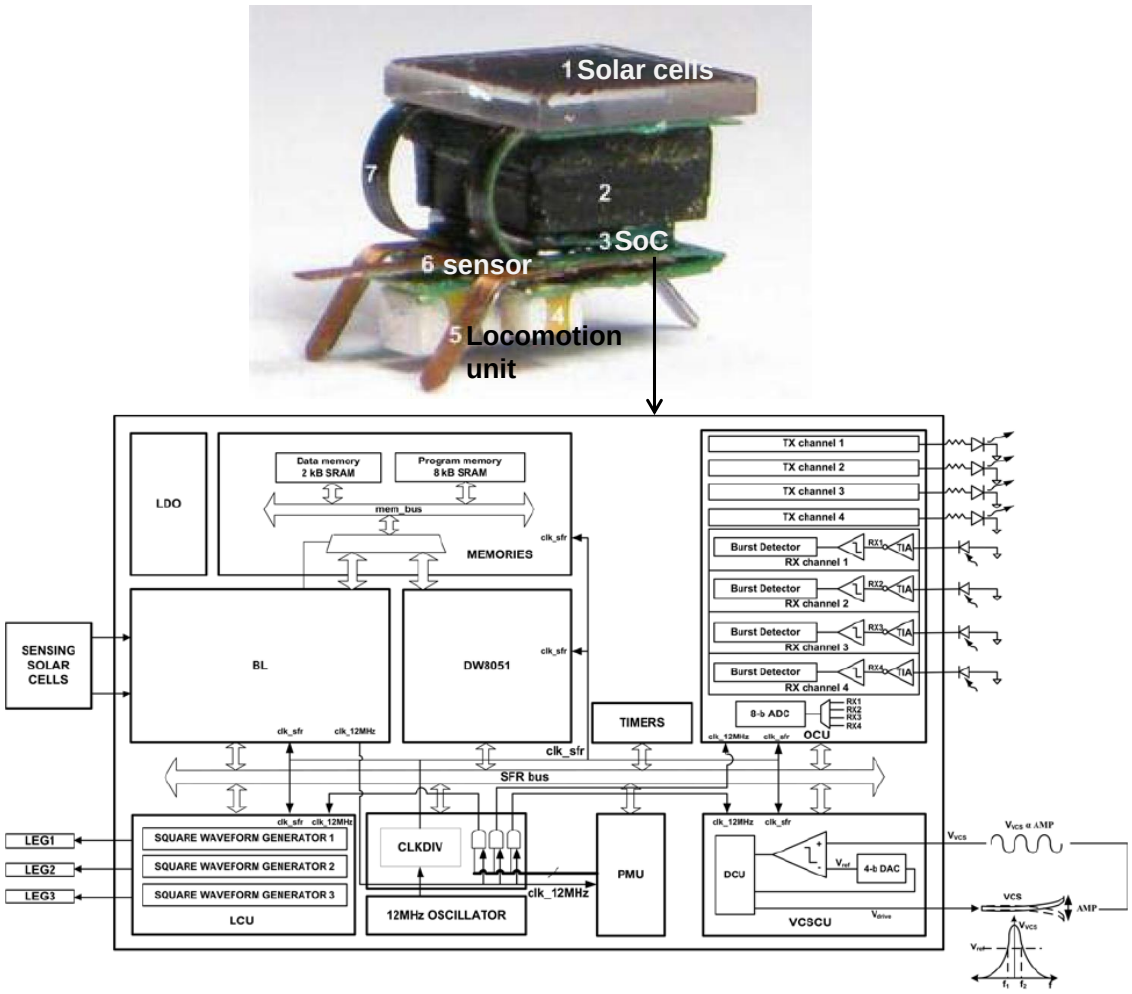


Figure 1-6. A SoC implemented in a 0.13µm SiGe CMOS technology for a moving microrobot [13].

1.2.2 Integration of Step-Up Voltage Converters in CMOS Processes

Step-up voltage converters have been further minimized by fabricating ASIC in high voltage CMOS processes [11][12]. P. Basset et al. have implemented a Cockcroft-Walton rectifier/quadruplor as well as digital control circuitry for capacitive actuators in a single die with total area of 5mm X 3mm in the 100V Alcatel-Mietec I2T100 technology [11]. The step-up converter switches at 10 kHz and achieves a maximum output voltage of 100V. C.L. Bellew et al. have employed a HV SOI technology and integrated the power source, solar cells, and buffers into a same die [12], which has be demonstrated successfully powering a jumping microrobot for a height of 1.2cm. R. Casanova et al.

have realized a system on chip (SoC) by embedding all power electronics, buffers, ADCs, DACs, control unit, analog transducers, and an oscillator in a 0.13µm SiGe CMOS technology to manage sensors and actuators for a moving microrobot as shown in Figure 1-6 [13]. The SoC converters the 1.4V generated by the solar cell to 3.6V to drive the actuators and sensors and takes area of 2.6mm X 2.6mm. All above-mentioned miniature powering systems require very expensive special CMOS technologies thereby economically not practical.

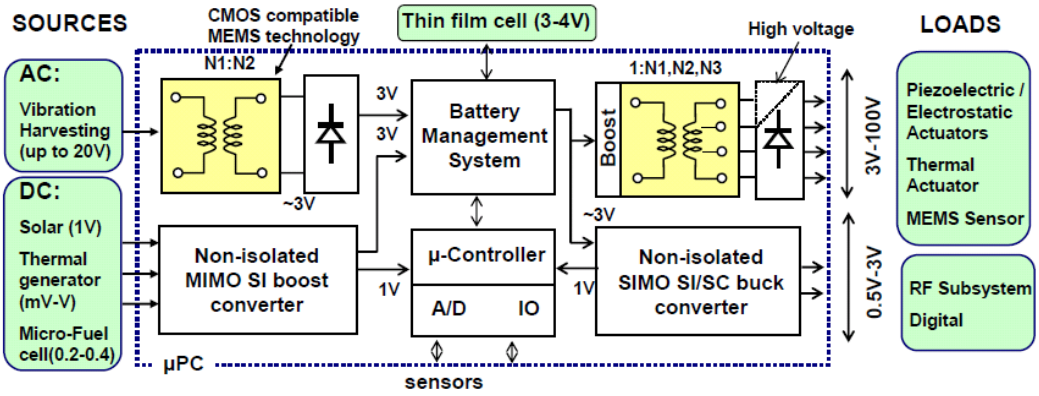


Figure 1-7. Envisioned power management platform for autonomous microsystems.

This dissertation is motivated to investigate low-cost techniques to implement miniature switching step-up voltage converters in standard CMOS processes. The fine feature sizes of scaled CMOS technologies allow for leveraging high switching frequencies to further reduce the sizes of passives required in voltage converters. Moreover, a system on chip can be realized to include both step-up and step-down voltage converters, RF communication subsystems, and digital processing, all on the same die and helps reduce the total size and weight of an autonomous microrobot. The envisioned SoC platform is illustrated in Figure 1-7, which is projected to integrate CMOS compatible MEMS devices, microprocessors, low and high voltage converters on a single die.

1.3 Dissertation Organization

The focus of this dissertation is to investigate high voltage tolerant devices and miniature switching step-up converters in a standard 0.13µm CMOS process for possible applications in microrobots. The dissertation is organized to seven chapters. Chapter 1 introduces research background and motivation for miniature switching step-up converters. Chapter 2 presents a literature review of switching converter topologies, and discusses their possibilities and limitations when integrating in the standard CMOS technology. Chapter 3 describes voltage limits and breakdown mechanisms in CMOS and develops three custom high-voltage-tolerant power devices, schottky barrier diodes (SBD), stacked NMOS switches, and extended-drain MOS devices without adding any masking steps. The block voltage is extended to be 2-3X larger than the standard thick-oxide devices. Chapter 4 evaluates a hybrid switched inductor (SI) / switched capacitor (SC), and SI/flyback converter implemented in the 0.13µm CMOS process and obtains a maximum output of 10V and maximum efficiency of 37% from 1.2V input. Chapter 5 proposes a simplified steady state circuit model for hybrid SI-SC DC-DC step-up converters for design-oriented analysis. SPICE simulations and experimental results are then employed to demonstrate the proposed models are valid with average errors of <30%. Chapter 6 describes a hybrid SI-SC step up converter implemented in a 1.2V CMOS process with minimal post-process steps. An optimal design procedure and a hysteretic controller were also designed and presented. In the end, experimental results are provided to demonstrate that the fabricated converter generates output voltage up to 35V for driving a resonant piezo fan. Finally, conclusions and continuing work are presented in Chapter 7.

CHAPTER 2
REVIEW ON SWITCHING STEP-UP VOLTAGE CONVERTERS

2.1 Introduction of Switching Step-Up Converters

The key principle in switching voltage converters is energy conservation. A power source firstly stores some energy in an inductor, transformer, or capacitor in one phase, and then the same amount of energy will be transferred from those energy reservoir components to the output in the other phase, thus allowing for generating a different voltage from the power source. Switching step-up voltage converters can be divided into three basic groups, switched inductor boost, flyback, and switched capacitor. This chapter will review some basic switching step-up converter topologies, discussing their possibilities and limitations for miniaturizing and integrating in standard CMOS processes. Moreover, some basic control techniques will also be presented.

2.2 Basic Switching Step-Up Converter Topologies

2.2.1 SI Boost Converter

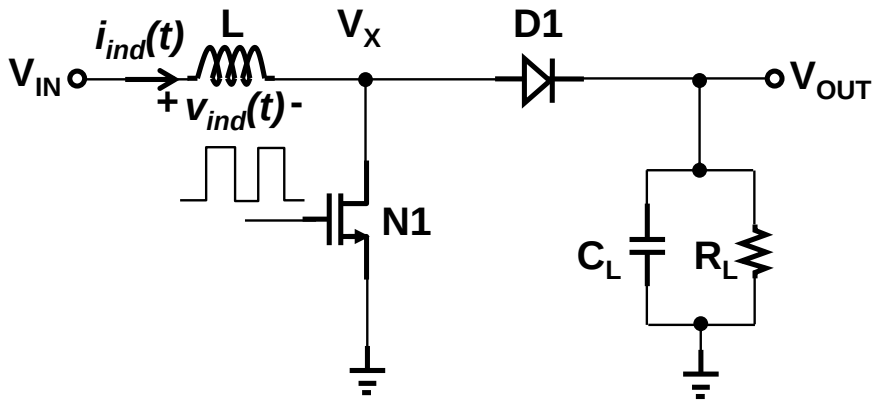


Figure 2-1. An ideal SI boost converter.

Figure 2- shows an ideal SI boost converter (i.e. $V_{OUT}>V_{IN}$). The steady state waveforms and equivalent circuits are provided in Figure 2-2. When the active switch, N1, is turned on by the gating signal, V_X is grounded providing a charging path from the input power source through the inductor L to the ground. The inductor current level

increases in this phase storing energy in L. In Figure 2-2(b), when the active switch N1 is turned off during $D'T_s=(1-D)T_s$, the inductor resists its current changes thus charging V_X to be equal to V_{OUT} (neglecting diode forward voltage drop) and turning on the diode D1. The inductor transfers its stored energy to the output load. The inductor voltage $v_{ind}(t)$ becomes negative, and $i_{ind}(t)$ decreases continuously as shown in Figure 2-2(c).

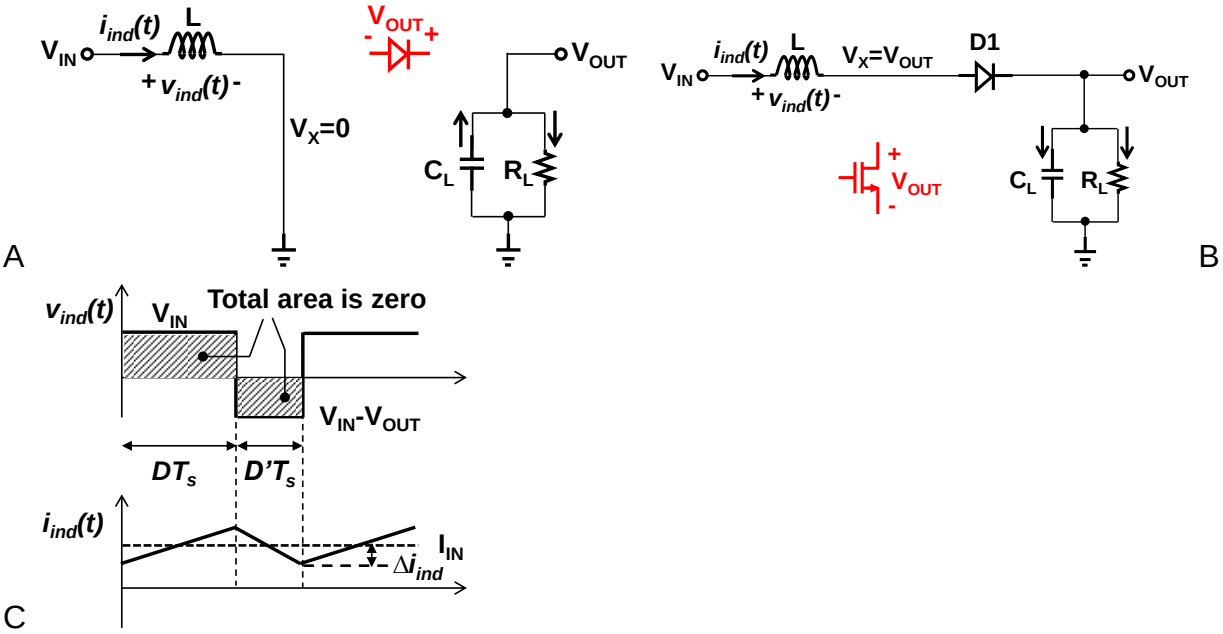


Figure 2-2. SI boost converter equivalent circuits and waveforms. A) N1 is on, B) N1 is off, C) Voltage and current waveforms of the inductor L.

Figure 2-2(c) shows that the net change of the inductor current over a switching cycle is zero, leading to inductor volt-second balance, that is, the net volt-seconds applied to an inductor (i.e. the total area) must be zero in steady state. Therefore the output voltage can be derived as:

$$V_{OUT} = \frac{V_{IN}}{1-D} \tag{2-1}$$

Figure 2-2 also shows the blocking voltage of the switch N1 and diode D1 when they are off (red color labels), which is equal to V_{OUT}. The breakdown voltage of N1 and D1 must be greater than their blocking voltage.

In Figure 2-2(c), the inductor current is always positive (i.e. $I_{IN}>\Delta i_{ind}$), which is called continuous conduction mode (CCM). However, when input current decreases (depending on the output load) and becomes equal to or smaller than the inductor current ripple peak amplitude Δi_{ind}, the inductor current will turn to zero for a short period of time, as shown in Figure 2-3, which is then called discontinuous conduction mode (DCM). In DCM, both the switch N1 and diode D1 will turn off, and the equivalent circuits of the SI boost is shown in Figure 2-3(a).

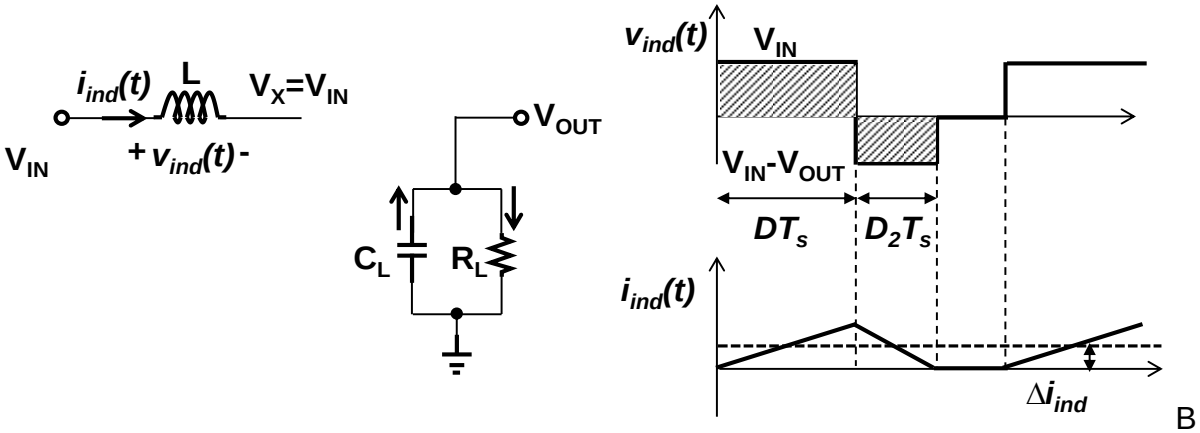


Figure 2-3. SI boost converter equivalent circuit and waveforms in DCM. A) Inductor current is zero, B) Voltage and current waveforms of the inductor L.

The boundary between the CCM and DCM for the SI boost can be derived by calculating the average input current (I_{IN}) and the inductor current ripple peak amplitude (Δi_{ind}). When the inductor current ripple is greater than the average input current, the converter is in DCM. Large ac conduction loss will be seen in DCM. But large output voltage can also be achieved in DCM. A dimensionless parameter K is defined as $K=2L/R_LT_s$, and the mode boundary is given by

$$K = \frac{2L}{R_L T_s} > K_{crit} = D(1-D)^2 \qquad \text{for CCM} \qquad (2\text{-}2a)$$

$$K = \frac{2L}{R_L T_s} < K_{crit} = D(1-D)^2 \qquad \text{for DCM} \qquad (2\text{-}2b)$$

Here, R_L is the load resistance, D is the duty cycle, and T_s is the switching period. In DCM, the output voltage is larger than that in CCM, and the resulting value is then derived using the inductor volt-second balance as

$$V_{OUT} = \frac{V_{IN}}{\frac{1+\sqrt{1+4D^2/K}}{2}} \qquad \text{when } K < K_{crit} \qquad (2\text{-}3)$$

The above results are summarized in Table 2-1.

Table 2-1. Summary of CCM-DCM characteristics for the SI boost

SI boost	Condition $K=2L/R_LT_S$ $K_{crit}=D(1-D)^2$	V_{OUT}	Voltage stress for N1	Voltage stress for D1
CCM	$K>K_{crit}$	$\frac{V_{IN}}{1-D}$	V_{OUT}	V_{OUT}
DCM	$K<K_{crit}$	$\frac{V_{IN}}{\frac{1+\sqrt{1+4D^2/K}}{2}}$	V_{OUT}	V_{OUT}

2.2.2 Flyback Converter

A flyback converter is developed from the buck-boost topology to realize high voltage conversion ratio by utilizing large-turns-ratio transformers. Figure 2-4 shows an ideal flyback converter with a transformer equivalent circuit model. The magnetizing inductance L_M functions as an energy storage element in the same manner as the inductor in boost or buck-boost. During subinterval 1, while the transistor N1 conducts, the converter circuit reduces to Figure 2-5(a). The inductor voltage $v_{ind}(t)$ is positive, and the inductor current $i_{ind}(t)$ increases, as shown in Figure 2-5(c). In this phase, the diode D1 is reverse biased, and the load current is provided by the load capacitor C_L. In subinterval 2, the transistor N1 is off, and the converter circuit is simplified as Figure 2-5(b). The inductor voltage $v_{ind}(t)$ is negative, and the inductor current $i_{ind}(t)$ is decreasing.

Energy stored in the magnetizing inductor is transferred to the output. From the inductor volt-second balance, the output voltage can be calculated as:

$$V_{OUT} = \frac{nDV_{IN}}{1-D} \tag{2-4}$$

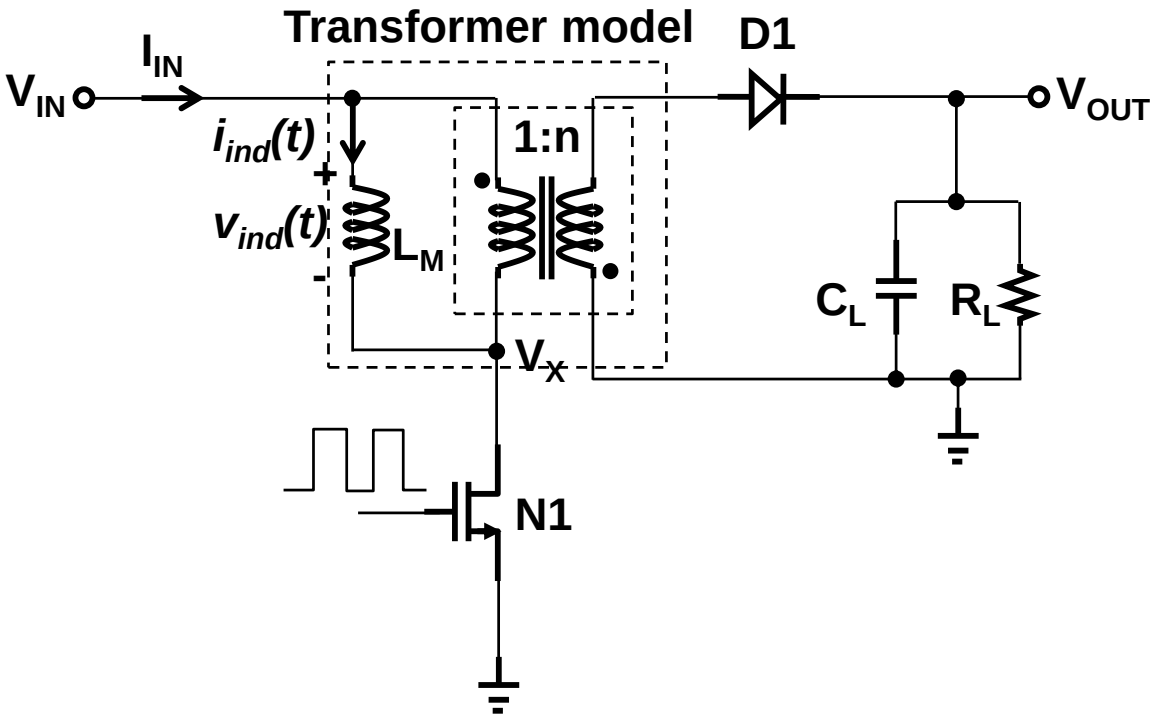


Figure 2-4. An ideal flyback converter.

Figure 2-5 only shows the blocking voltage when the transistor N1 and diode D1 are off. The voltage stress of D1 is $V_{OUT}+nV_{IN}$, which is much larger than the voltage stress of N1.

The expression of the output voltage in equation (2-4) only applies to CCM. When the flyback converter works in DCM, the inductor current might decrease to zero, as shown in Figure 2-6. In subinterval 1, the inductor current can be written as:

$$i_{ind}(t) = \frac{V_{IN}}{L_M} t \tag{2-5a}$$

$$2\Delta i_{ind} = \frac{V_{IN}}{L_M} DT_s \tag{2-5b}$$

In subinterval 2, the inductor current is derived as:

$$i_{ind}(t) = -\frac{V_{OUT}}{nL_M}\left(t - DT_s\right) \tag{2-6a}$$

$$2\Delta i_{ind} = \frac{V_{OUT}}{nL_M} D_2 T_s \tag{2-6b}$$

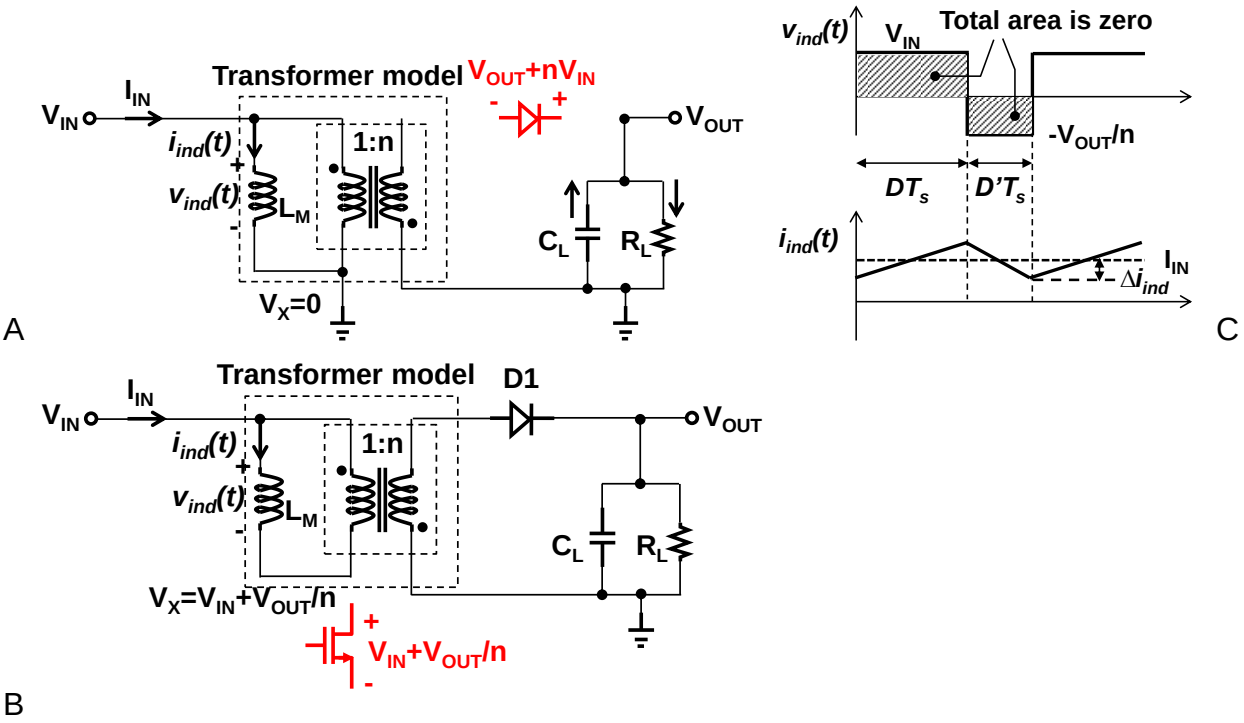


Figure 2-5. Flyback converter equivalent circuits and waveforms. A) N1 is on, B) N1 is off, C) voltage and current waveforms of the magnetizing inductor L_M.

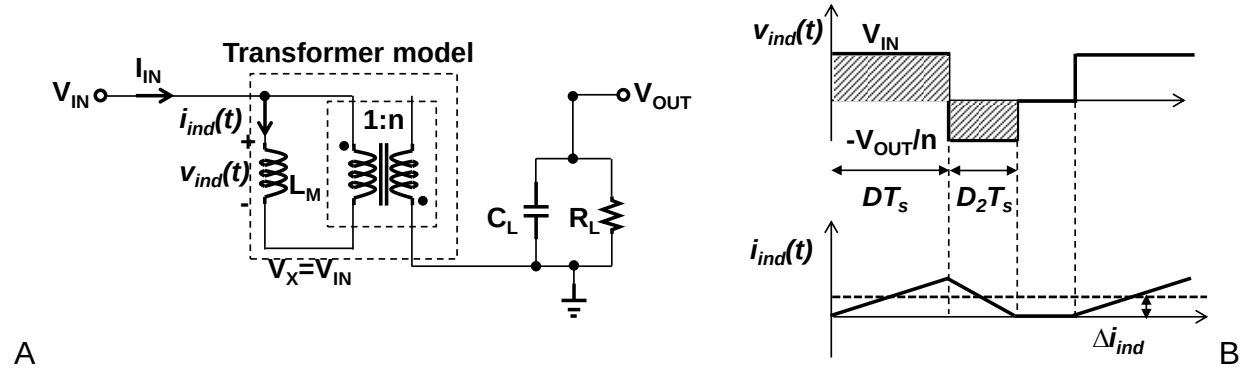


Figure 2-6. Flyback converter equivalent circuit and waveforms in DCM when inductor current is zero. A) Equivalent circuits, B) Voltage and current waveforms of the magnetizing inductor.

The output current can be derived as:

$$I_{OUT} = \frac{1}{2n} 2\Delta i_{ind} D_2 = \frac{V_{OUT}}{2n^2 L_M} {D_2}^2 T_s = \frac{V_{OUT}}{R_L} \tag{2-7}$$

From equation (2-7), the duty cycle D_2 can be derived as:

$$D_2 = n\sqrt{\frac{2L_M}{R_L T_s}} = n\sqrt{K} \tag{2-8}$$

Here we define $K=2L_M/R_L T_s$ and $K_{crit}=(1-D)^2/n^2$, and we can know the output voltage is

$$V_{OUT} = n\frac{D}{D_2} V_{IN} = \frac{DV_{IN}}{\sqrt{K}} \tag{2-9}$$

The CCM-DCM characteristics of the flyback converter are summarized in Table 2-2. Comparing to the SI boost, the flyback can realize a larger output voltage with the same duty cycle by using a transformer, and the voltage stress of the switch N1 is decreased if the output voltage is the same. The drawback of the flyback converter is the voltage stress of D1 is enlarged.

Table 2-2. Summary of CCM-DCM characteristics for the flyback converter

Flyback	Condition $K=2L_M/R_L T_S$ $K_{crit}=(1-D)^2/n^2$	V_{OUT}	Voltage stress for N1	Voltage stress for D1
CCM	$K>K_{crit}$	$\frac{DV_{IN}}{1-D}$	$V_{IN}+V_{OUT}/n$	$nV_{IN}+V_{OUT}$
DCM	$K<K_{crit}$	$\frac{DV_{IN}}{\sqrt{K}}$	$V_{IN}+V_{OUT}/n$	$nV_{IN}+V_{OUT}$

2.2.3 Switched Capacitor Step-Up Converters

A variety of SC step-up topologies have been developed in literature [14][19]. This section will present SC ladder (Cockcroft-Walton), Dickson, series-parallel, Fibonacci, doubler, and discuss their voltage conversion ratios and voltage stresses.

2.2.3.1 Ladder (Cockcroft-Walton)

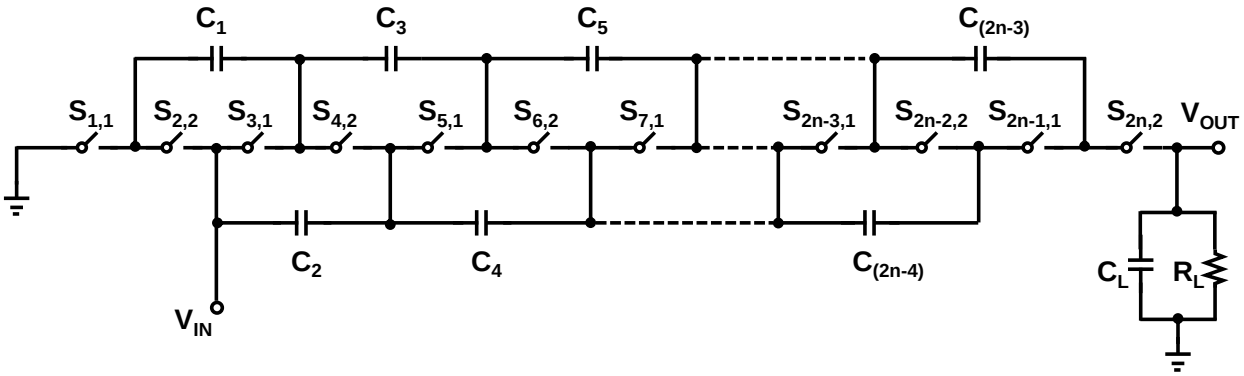


Figure 2-7. An ideal SC ladder converter.

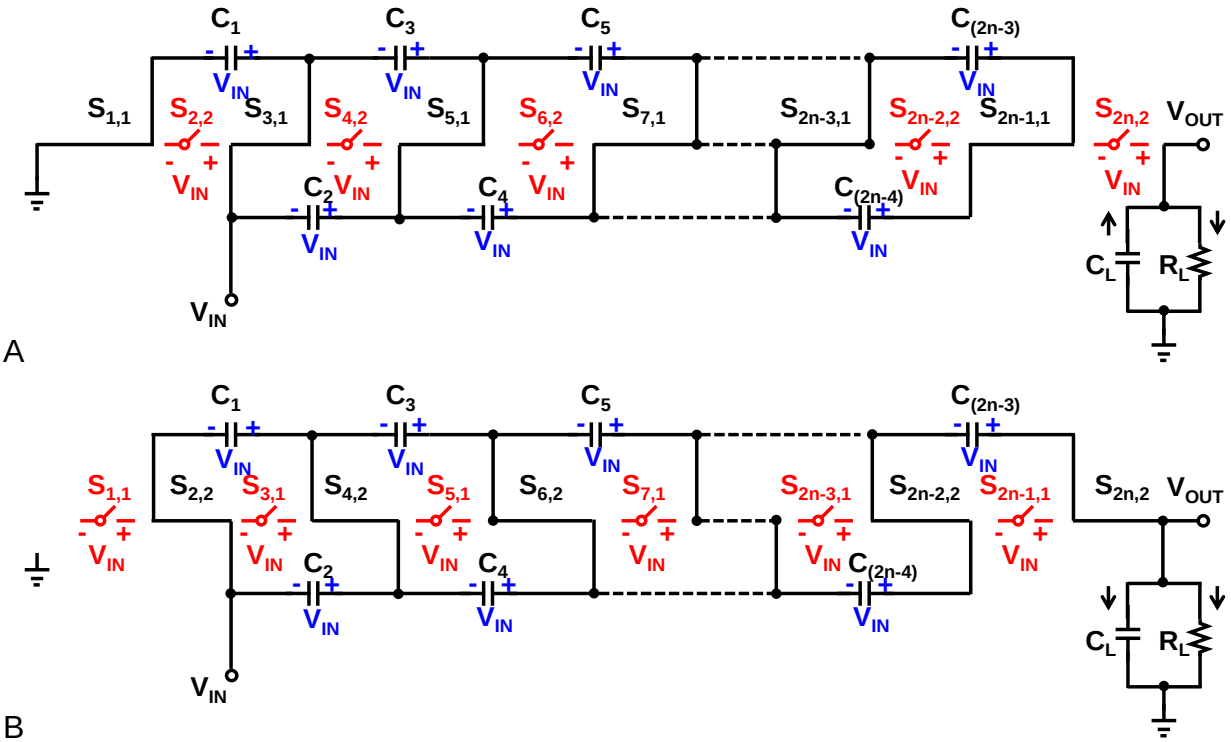


Figure 2-8. Equivalent circuits of the SC ladder converter. A) $S_{1,1}$, $S_{3,1}$, … $S_{2n-1,1}$ are on, $S_{2,2}$, $S_{4,2}$, … $S_{2n,2}$ are off, B) $S_{1,1}$, $S_{3,1}$, … $S_{2n-1,1}$ are off, $S_{2,2}$, $S_{4,2}$, … $S_{2n,2}$ are on.

Figure 2-7 is an ideal two-phase SC ladder comprised of (n-2) holding capacitors C_2, C_4,…, $C_{(2n-4)}$, (n-1) flying capacitors C_1, C_3,…, $C_{(2n-3)}$, and (2n) power switches $S_{1,1}$, $S_{2,2}$,…, $S_{2n,2}$. In phase I, switches with even subscript numbers conduct, and the input power source charges flying capacitors. In phase II, the flying capacitors supply charges

to the output load. The equivalent circuits of the SC ladder in phase I and II are described in Figure 2-8. Ideally, voltage across each capacitor is the same as V_{IN}, therefore the output voltage is derived as

$$V_{OUT} = nV_{IN} \tag{2-10}$$

Moreover, blocking voltages over non-conducting switches are also shown in Figure 2-8, which are all equal to V_{IN}.

2.2.3.2 Dickson charge pump

Figure 2-9 shows an ideal Dickson charge pump, which consists of (n-1) flying capacitors C_1, …, $C_{(n-1)}$, and (n+4) switches $S_{1,1},\ldots,S_{n+4,2}$. The equivalent circuits of the Dickson charge pump is illustrated in Figure 2-10, where voltages across capacitors and non-conducting switches in steady state are analyzed and labeled. Assuming *n* is even, the output voltage can derived as

$$V_{OUT} = nV_{IN} \tag{2-11}$$

And the maximum voltage stress for the capacitors and switches are $2V_{IN}$.

When n=2, the Dickson charge pump simplifies as a voltage doubler, which is the same as the SC ladder with n=2. Voltage doubler is the most commonly used charge pump in circuit community.

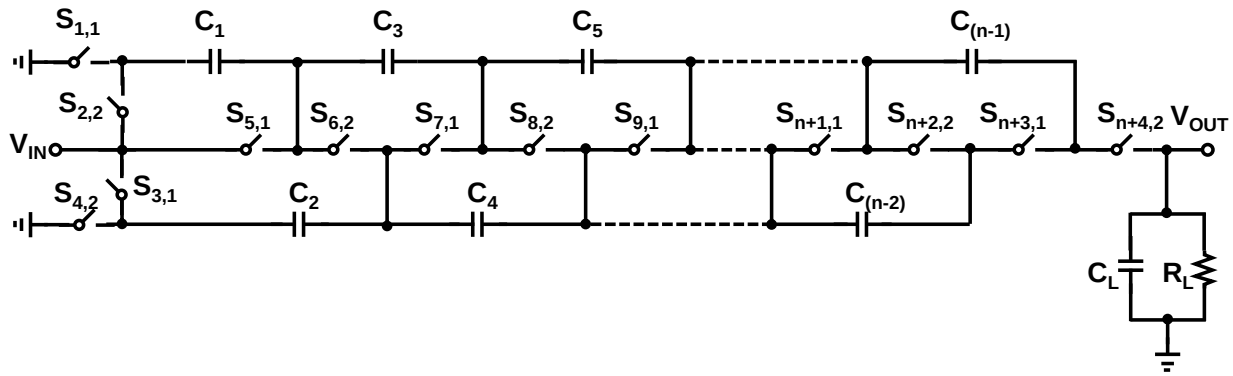
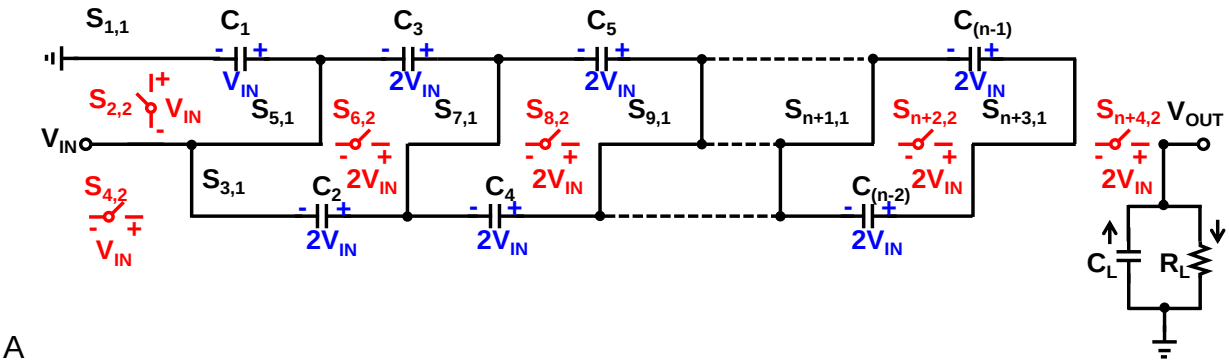
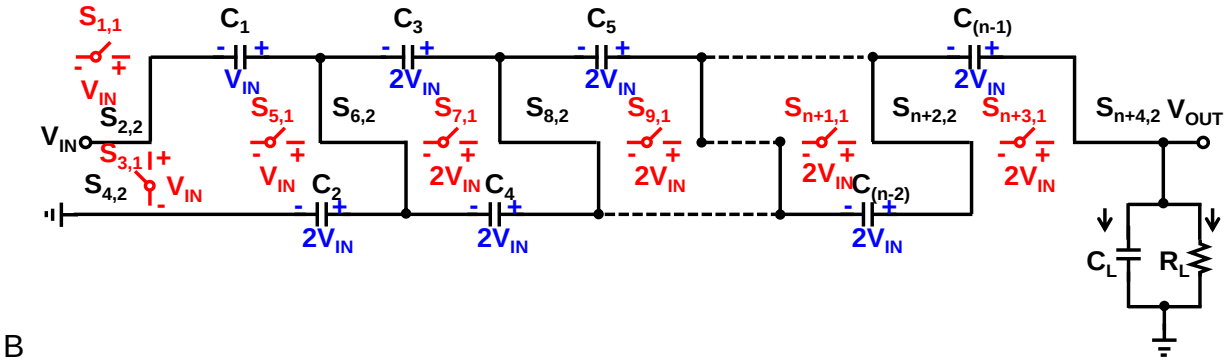


Figure 2-9. An ideal Dickson charge pump (*n* is even).



A



B

Figure 2-10. Equivalent circuits of the Dickson charge pump. A) $S_{1,1}$, $S_{3,1}$, … $S_{n+3,1}$ are on, $S_{2,2}$, $S_{4,2}$, … $S_{n+4,2}$ are off, B) $S_{1,1}$, $S_{3,1}$, … $S_{n+3,1}$ are off, $S_{2,2}$, $S_{4,2}$, … $S_{n+4,2}$ are on.

2.2.3.3 Fibonacci converter

Figure 2-11 shows an ideal k-stage SC Fibonacci converter and Figure 2-12 shows its equivalent circuits. The input power source firstly charges C_1 to V_{IN} in phase I, and then in next phase, the power source in series with C_1 charges C_2 to $2V_{IN}$. In the next switching cycle, the power source in series with C_1 and C_2 charges C_3 to $3V_{IN}$. Therefore voltage over capacitor C_k will be a Fibonacci number F_{k+1}, which is defined as:

$$F_k = \begin{cases} 1, & if \quad k = 1 \\ 1, & if \quad k = 2 \\ F_{k-2} + F_{k-1}, & if \quad k > 2 \end{cases} \tag{2-12}$$

The output voltage is then derived as

$$V_{OUT} = V_{IN} + V_{c1} + V_{c2} + ... + V_{ck} = (F_1 + F_2 + F_3 + ... + F_{k+1})V_{IN} = F_{k+2}V_{IN} \quad (2\text{-}13)$$

Figure 2-12 also illustrates blocking voltages of non-conducting switches, and the maximum voltage stress for switches is $F_{k+1}V_{IN}$. Fibonacci converter can realize high step-up ratio with few components, but large voltage stress is a drawback. Fibonacci converter is more suitable for implementation using high voltage discrete components.

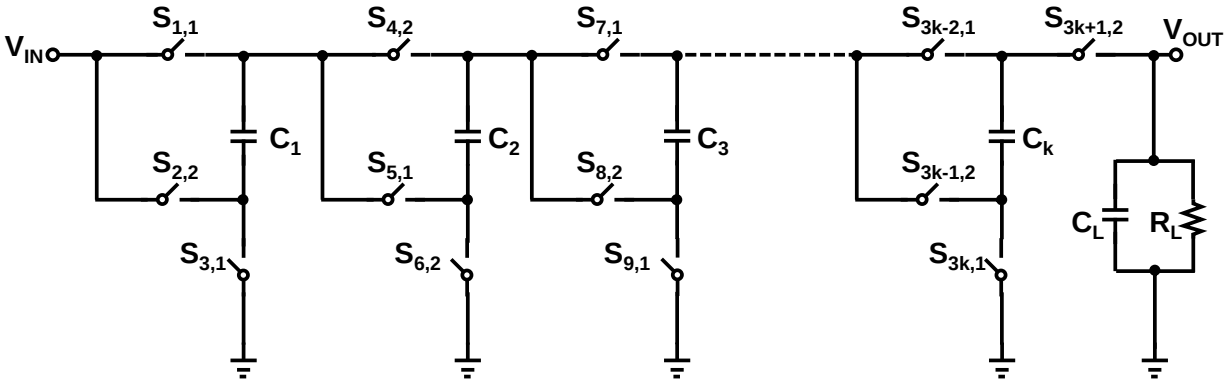


Figure 2-11. An ideal SC Fibonacci converter (*k* is odd).

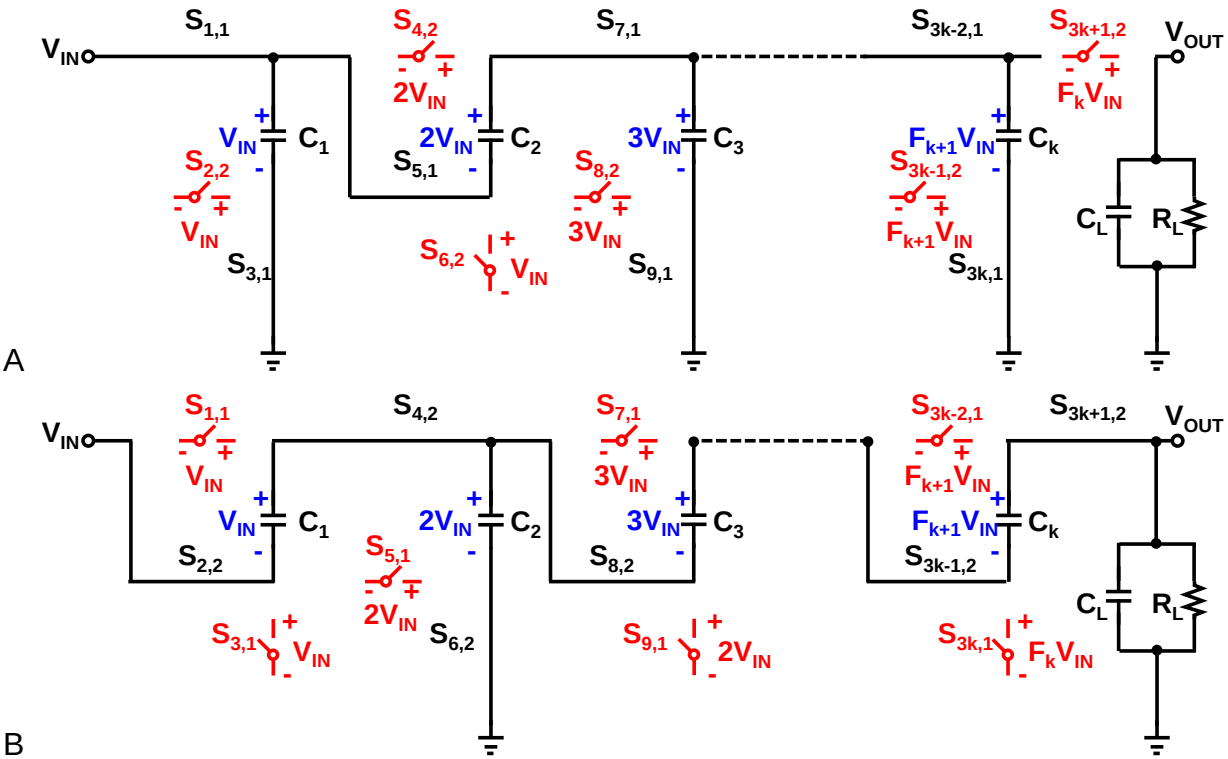


Figure 2-12. Equivalent circuits of the SC Fibonacci converter (*k* is odd). A) $S_{i,1}$ is on, B) $S_{i,2}$ is on (i=1,2,…).

2.2.3.4 Series-parallel converter

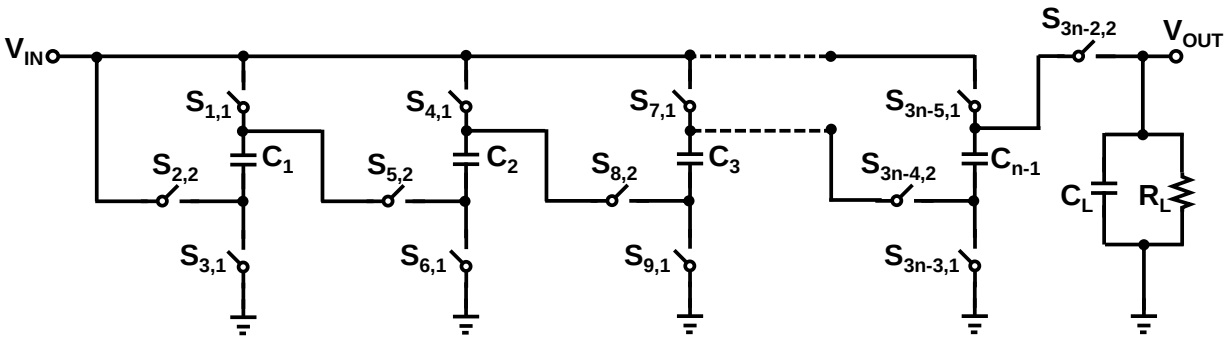


Figure 2-13. An ideal SC series-parallel converter.

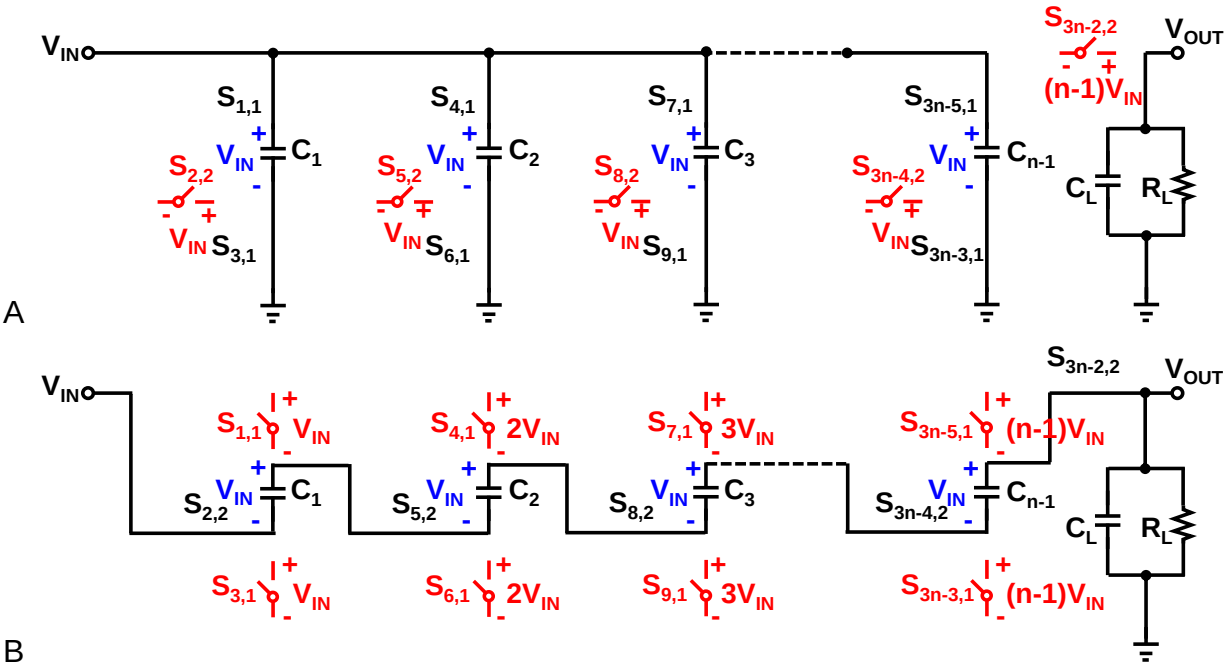


Figure 2-14. Equivalent circuits of the SC series-parallel converter. A) $S_{i,1}$ is on, B) $S_{i,2}$ is on (i=1,2,…).

Figure 2-13 shows an ideal SC series-parallel converter including (n-1) capacitors and (3n-2) switches. The equivalent circuits of the series-parallel converter in two phases are illustrated in Figure 2-14. The input power source firstly charges all capacitors in parallel, and then the capacitors are connected in series with the input and provide charges to the output. Therefore the output voltage is derived as

$$V_{OUT} = nV_{IN} \tag{2-14}$$

Figure 2-14 also shows blocking voltages across non-conducting switches, and the maximum voltage stress is $(n-1)V_{IN}$. Power switches close to V_{OUT} have to block large voltages.

2.2.3.5 Summary of SC converters

Table 2-3 summarizes steady state characteristics of SC step-up converters. For the same voltage conversion ratio, the ladder converter requires the maximum number of switches and capacitors, while the Fibonacci converter needs the least number of devices. The ladder and Dickson charge pump, voltage stresses are approximately equally distributed across switches and diodes, which makes these two topologies more suitable for integration in deep-submicron CMOS technologies. For the series-parallel converter, voltage stress of capacitors is small but voltage stress of switches is the biggest. The Fibonacci converter has large voltage stress for both capacitors and switches, which makes it the most difficult topology for integration.

Table 2-3. Summary of steady state characteristics for SC step-up converters

	V_{OUT}	Voltage stress over switches						Voltage stress over capacitors				
Ladder	nV_{IN}	$S_{1,1}$-$S_{2n,2}$ V_{IN}						C_1-C_{2n-3} V_{IN}				
Dickson	nV_{IN}	$S_{1,1}$-$S_{5,1}$ V_{IN}				$S_{6,2}$-$S_{n+4,2}$ $2V_{IN}$		C_1 V_{IN}		C_2-$C_{(n-1)}$ $2V_{IN}$		
Fibonacci	$F_{k+2}V_{IN}$	$S_{1,1}$-$S_{3,1}$ V_{IN}	$S_{4,2}$-$S_{5,1}$ $2V_{IN}$	$S_{6,2}$ V_{IN}	…	S_{3k-2}-S_{3k-1} $F_{k+1}V_{IN}$	S_{3k}-S_{3k+1} F_kV_{IN}	C_1 V_{IN}	C_2 $2V_{IN}$	C_3 $3V_{IN}$	…	C_k $F_{k+1}V_{IN}$
Series-Parallel	nV_{IN}	$S_{1,1}$-$S_{3,1}$ V_{IN}	$S_{4,1}$ $2V_{IN}$	$S_{5,2}$ V_{IN}	…	$S_{3n-4,1}$ V_{IN}	$S_{3n-3,1}$-$S_{3n-2,1}$ $(n-1)V_{IN}$	C_1-$C_{(n-1)}$ V_{IN}				

2.3 Averaged Switching Network

2.3.1 Averaged L-S-D Network in CCM

Various approaches have been proposed to facilitate analyzing switching DC-DC converters [20]-[23], such as state-space averaging [20], averaged switching network

[22]. The averaged switching network approach is physically more meaningful to circuit designers and will be introduced in this section. Figure 2-15a shows the ideal L-S-D switching network that is common in switched-inductor DC-DC converters (buck, boost, buck-boost). The switch and diode in this network will be turned on and off alternatively, resulting in pulsating currents and voltages and introducing difficulties in DC and AC analyses. However, after these pulsating currents and voltages are averaged and linearized over switching periods, they are converted to traditional continuous analog signals and can be analyzed easily.

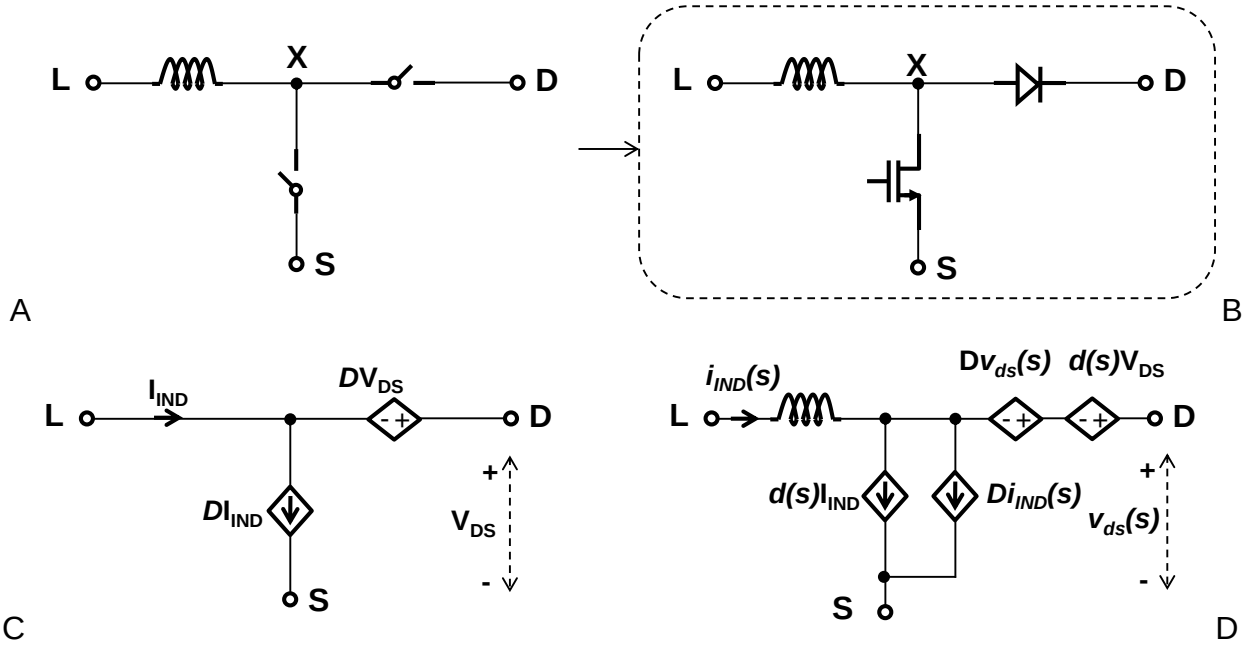


Figure 2-15. L-S-D network and its DC and AC averaged model in CCM. A) Ideal L-S-D network that is common in SI DC-DC converters, B) Its physical implementation example, C) DC and D) AC averaged circuit for the ideal L-S-D switching network in CCM.

Assuming switches and diodes are ideal, the following large-signal relationships can be obtained.

$$\begin{cases} \overline{i_S} = d_T i_{IND} \\ \overline{v_{DX}} = d_T v_{DS} \end{cases} \tag{2-15}$$

Assuming small perturbations and ignoring higher-order terms, the above equation can be linearized as follows.

$$\begin{cases} I_S + i_s = DI_{IND} + dI_{IND} + Di_{ind} \\ V_{DX} + v_{dx} = DV_{DS} + dV_{DS} + Dv_{ds} \end{cases} \tag{2-16}$$

Therefore, from equation 2-16, the ideal L-S-D switching network is identical to the DC averaged circuit shown in Figure 2-15c and AC averaged circuit in Figure 2-15d. However, the AC circuit is only accurate at low frequencies.

2.3.2 Averaged L-S-D Network in DCM

When the L-S-D switching network operates in DCM, it can be averaged in the same way that is done in section 2.3.1. However, since the duty cycle when the diode is on is unknown, resulted averaged circuit is much more complicated. The following derivation was firstly discussed in [22].

The peak inductor current is calculated as

$$i_{PK} = \frac{v_{LS}}{L} d_T T_S \tag{2-17}$$

The averaged switch and diode current can then be derived as

$$\begin{cases} \overline{i_S} = \dfrac{{d_T}^2 T_S}{2L} v_{LS} \\ \overline{i_D} = \dfrac{{d_T}^2 T_S}{2L} \dfrac{{v_{LS}}^2}{v_{DL}} \end{cases} \tag{2-18}$$

Voltage at the intermediate node *X* is

$$v_X = \begin{cases} v_S, 0 < t < d_T T_S \\ v_D, d_T T_S < t < (d_T + d_{2T}) T_S \\ v_L, (d_T + d_{2T}) T_S < t < T_S \end{cases} \tag{2-19}$$

Therefore, the averaged voltages $\langle v_{XS} \rangle$ and $\langle v_{DX} \rangle$ are represented as

$$\begin{cases} \langle v_{XS} \rangle = v_{DL} d_{2T} + v_{LS}(1 - d_T) \\ \langle v_{DX} \rangle = v_{DL}(1 - d_{2T}) + v_{LS} d_T \end{cases} \tag{2-20}$$

From 2-37, voltages v_{DL} and v_{LS} can be represented using the averaged voltages $\langle v_{XS} \rangle$ and $\langle v_{DX} \rangle$ as follows

$$\begin{cases} v_{LS} = \dfrac{1 - d_{2T}}{1 - d_{2T} - d_T} \langle v_{XS} \rangle - \dfrac{d_{2T}}{1 - d_{2T} - d_T} \langle v_{DX} \rangle = \langle v_{XS} \rangle \\ v_{DL} = \dfrac{1 - d_T}{1 - d_{2T} - d_T} \langle v_{DX} \rangle - \dfrac{d_T}{1 - d_{2T} - d_T} \langle v_{XS} \rangle = \langle v_{DX} \rangle \end{cases} \tag{2-21}$$

After applying perturbation and linearization, we have

$$\begin{cases} I_S + i_s = \dfrac{V_{LS}}{R_e} + \dfrac{DT_S}{L} V_{LS} d + \dfrac{v_{ls}}{R_e} \\ I_D + i_d = \dfrac{{V_{LS}}^2}{V_{DL}} \dfrac{1}{R_e} + \dfrac{{V_{LS}}^2}{V_{DL}} \dfrac{DT_S}{L} d + \dfrac{2V_{LS}}{V_{DL}} \dfrac{1}{R_e} v_{ls} - \dfrac{{V_{LS}}^2}{{V_{DL}}^2} \dfrac{1}{R_e} v_{dl} \end{cases} \tag{2-22}$$

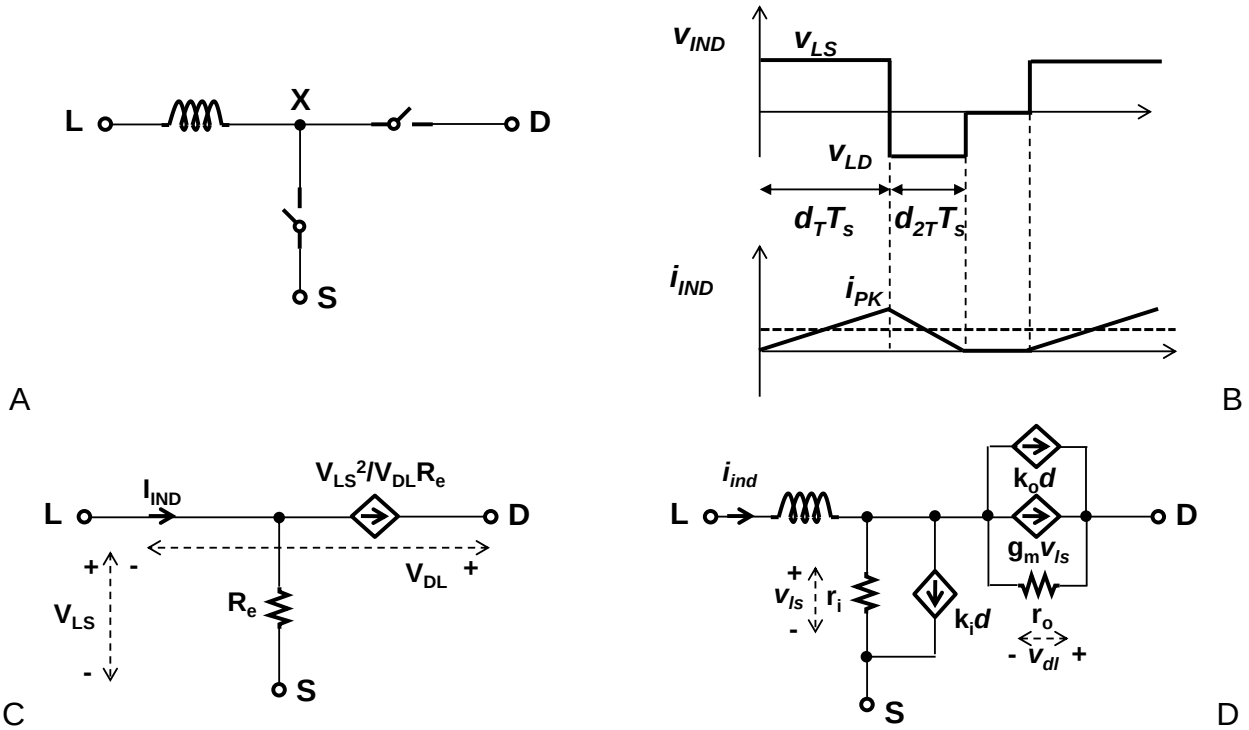


Figure 2-16. L-S-D network and its DC and AC averaged model in DCM. A) Ideal L-S-D network, B) Its example voltage and current waveforms in DCM, C) DC and D) AC averaged circuit for the ideal L-S-D switching network in DCM.

From 2-19, DC and AC averaged circuits are then derived and illustrated in Figure 2-16c and d. Parameters that are used in Figure 2-16 are defined as below.

$$R_e = r_i = \frac{2L}{D^2 T_S} \tag{2-23}$$

$$r_o = \frac{V_{DL}^{\ 2}}{V_{LS}^{\ 2}} R_e \tag{2-24}$$

$$k_i = \frac{DT_S}{L} V_{LS} \tag{2-25}$$

$$k_o = \frac{DT_S}{L} \frac{V_{LS}^{\ 2}}{V_{DL}} \tag{2-26}$$

$$g_m = \frac{2V_{LS}}{V_{DL}} \frac{1}{R_e} \tag{2-27}$$

2.3.3 Small-Signal Analysis of SI Boost Converter in CCM

The averaged switching network is applied to the SI boost converter, resulting in the small signal model as shown in Figure 2-17. From it, the duty-to-output transfer function can be derived as

$$T_p = \frac{R_L\left(V_{OUT}(1-D) - sLI_{IND}\right)}{s^2 LC_L R_L + sL + R_L(1-D)^2} = -\frac{V_{OUT}}{(1-D)R_L C_L} \frac{s-\omega_z}{(s-\omega_{p1})(s-\omega_{p2})} \tag{2-28}$$

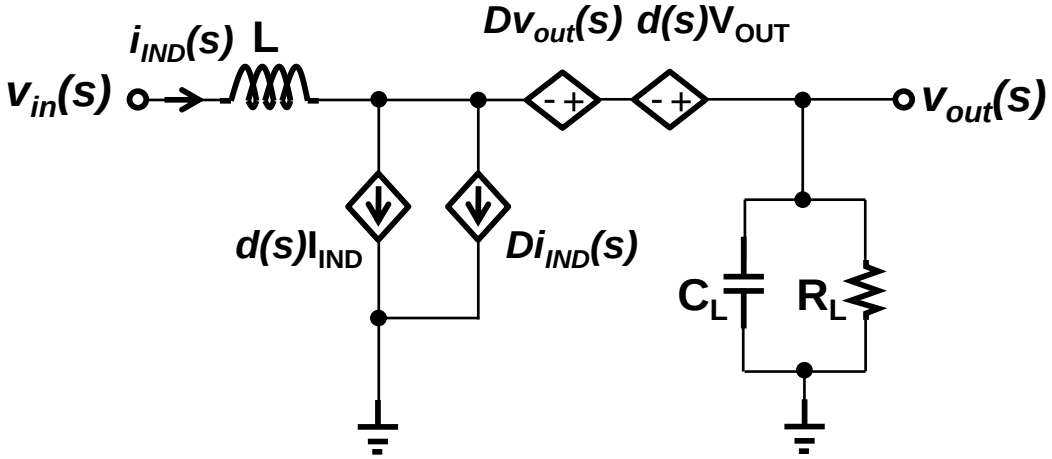


Figure 2-17. Small-signal model of the SI boost converter in CCM.

The transfer function contains a RHP zero and two LHP poles, which are represented as

$$\omega_z = \frac{R_L(1-D)^2}{L} \tag{2-29}$$

$$\omega_{p1}, \omega_{p2} = -\xi\omega_0 \pm j\omega_0\sqrt{1-\xi^2} \tag{2-30}$$

where

$$\omega_0 = \frac{1-D}{\sqrt{C_L L}} \tag{2-31}$$

$$\xi = \frac{1}{2R_L(1-D)}\sqrt{\frac{L}{C_L}} \tag{2-32}$$

2.3.4 Small-Signal Analysis of SI Boost Converter in DCM

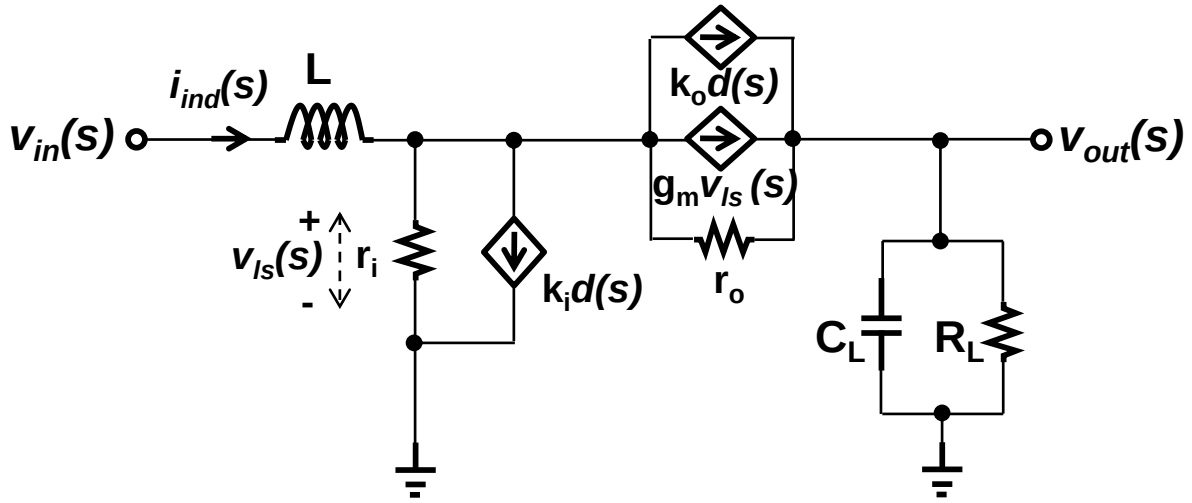


Figure 2-18. Small-signal model of the SI boost in DCM.

Applying the derived averaged switching network to the SI boost in DCM, the small signal model is obtained and described in Figure 2-18. From it, the duty-to-output transfer function is derived as

$$T_p = -\frac{R_L\left(sL\left(k_i r_i + g_m r_o k_i r_i - k_o r_o\right) - k_o r_o r_i\right)}{s^2 L C_L R_L\left(r_o + r_i + g_m r_o r_i\right) + s\left(L\left(R_L + r_o + r_i + g_m r_o r_i\right) + C_L R_L r_o r_i\right) + \left(R_L + r_o\right) r_i}$$

$$= \frac{k_o r_o - k_i r_i - g_m r_o k_i r_i}{(r_o + r_i + g_m r_i r_o) C_L} \frac{s - \omega_z}{(s - \omega_{p1})(s - \omega_{p2})} \tag{2-33}$$

The duty-to-output transfer function contains a possible RHP zero and two LHP poles, which are represented as

$$\omega_z = \frac{k_o r_o r_i}{L(k_i r_i + g_m r_o k_i r_i - k_o r_o)} \tag{2-34}$$

$$\omega_{p1}, \omega_{p2} = -\xi\omega_0 \pm j\omega_0\sqrt{1-\xi^2} \tag{2-35}$$

where

$$\omega_0 = \sqrt{\frac{(R_L + r_o) r_i}{L R_L C_L (r_i + r_o + g_m r_o r_i)}} \tag{2-36}$$

$$\xi = \frac{C_L R_L r_o r_i + L(R_L + r_o + r_i + g_m r_o r_i)}{2\sqrt{L C_L R_L r_i (r_o + r_i + g_m r_o r_i)(R_L + r_o)}} \tag{2-37}$$

The averaged L-S-D model is derived based on that the small signal ac voltage across the inductor is zero, meaning the model is only accurate in low frequencies. Therefore, the above transfer function can be simplified as follows

$$T_p = \frac{k_o (R_L \parallel r_o)}{s C_L (R_L \parallel r_o) + 1} \tag{2-38}$$

which contains a single pole. It means that the boost in DCM is easier to be stabilized that in CCM.

More accurate results [24] shows that the SI boost in DCM contains a low-frequency dominant pole, a high-frequency second pole, and a high-frequency RHP zero. However, the second pole and RHP zero are higher than the switching frequency in general and can be neglected in stability analysis.

$$\omega_{p1} = \frac{1}{C_L (R_L \parallel r_o)} \tag{2-39}$$

$$\omega_{p2} = \frac{2(M-1)f_s}{D} \tag{2-40}$$

$$\omega_z = \frac{2f_s}{D} \tag{2-41}$$

Here M is the voltage conversion ratio $M=V_{OUT}/V_{IN}$.

2.4 Control Scheme of DC-DC Converters

2.4.1 Voltage Mode Pulse Width Modulation (PWM)

Voltage mode PWM is the first used approach for switching regulator design, and its configuration for a SI boost is shown in Figure 2-19. The control loop senses the output voltage V_{OUT} through feedback resistors R_1 and R_2, and subtracts the feedback voltage V_{FB} from a reference voltage V_{REF} to establish an error signal (V_{ERR}). This error signal is then compared to a fixed frequency sawtooth waveform (V_{SAW}), resulting in a PWM clock to drive the power switch N_1 and generate a dc output V_{OUT}. This negative feedback loop regulates the feedback voltage V_{FB} to be the same as V_{REF}. As shown in Figure 2-15b, duty cycle of the driving clock from PWM generator can be calculated as

$$D = \frac{V_{ERR} - V_{SAW_MIN}}{V_{SAW_MAX} - V_{SAW_MIN}} \tag{2-42}$$

Voltage mode PWM control is easy to design and analyze, and has been used in industry for many years. The modulation is stable and provides a good noise margin. The feedback loop has low output impedance and allows better cross-modulation for multiple outputs. The drawback of this control scheme is its slow loop response. Moreover, complicated compensation circuit is often necessary for loop stability, which makes the loop dynamics even slower [20]. When employing voltage mode PWM in boost converters, right half plane zero may further reduce the loop band width, causing

transient response of boost converters very and very slow. Complicated compensation network is required especially for boost converters.

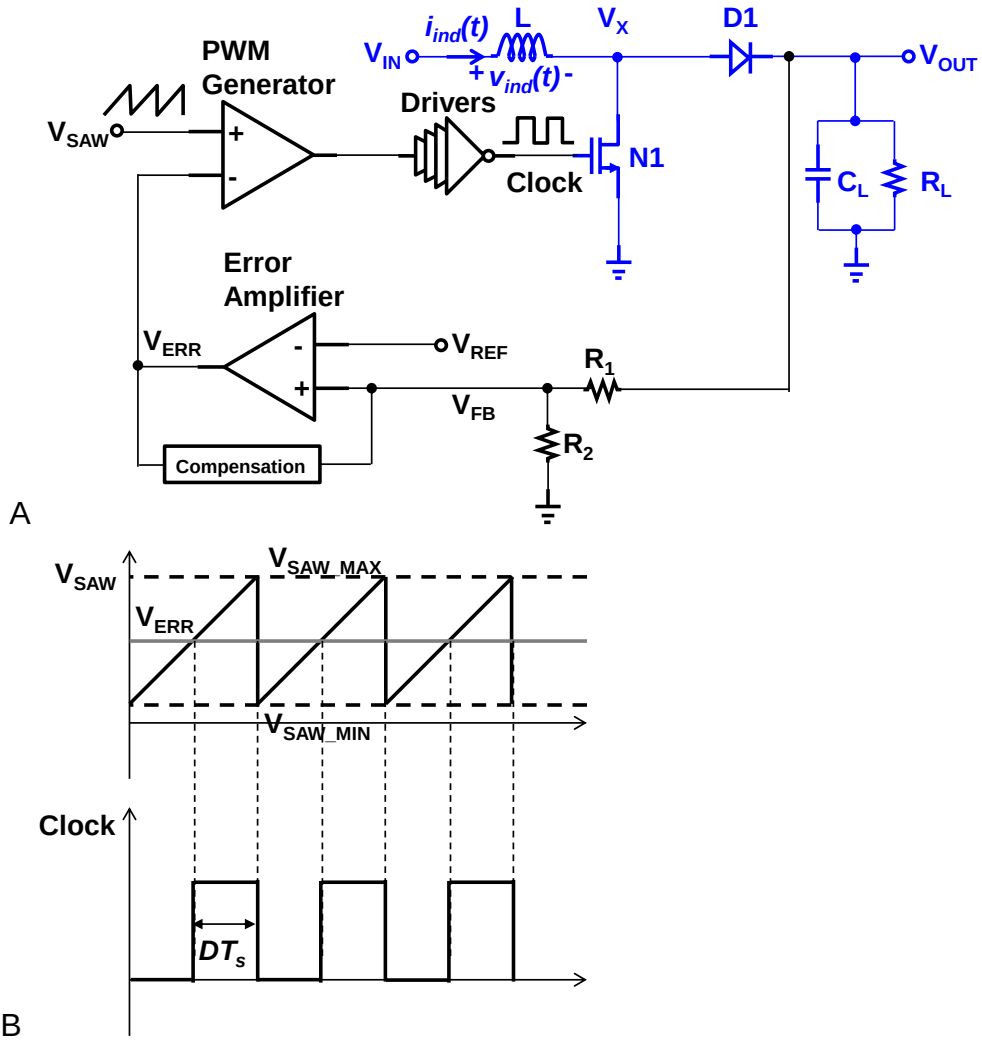


Figure 2-19. Voltage mode PWM controller and waveforms. A) Block diagram, B) representative waveforms.

2.4.2 Current Mode PWM

Current mode PWM was proposed in history to alleviate the drawbacks of voltage mode PWM. As seen in the diagram of current mode PWM in Figure 2-20, besides the voltage feedback loop, another loop which senses inductor current is added. An error voltage V_{ERR} from the voltage feedback loop is compared to the inductor current. As shown in Figure 2-20b, whenever the peak inductor current hits the value determined by

V_{ERR}, pulses are created at R, turn off the switch N_1 and transfer energy from the inductor to the output. Duty cycle of the driving clock is modulated by both the error voltage and the inductor current, and the loop frequency is determined by a fixed-frequency pulse V_{pulse} which sets the S-R latch (PWM generator) constantly.

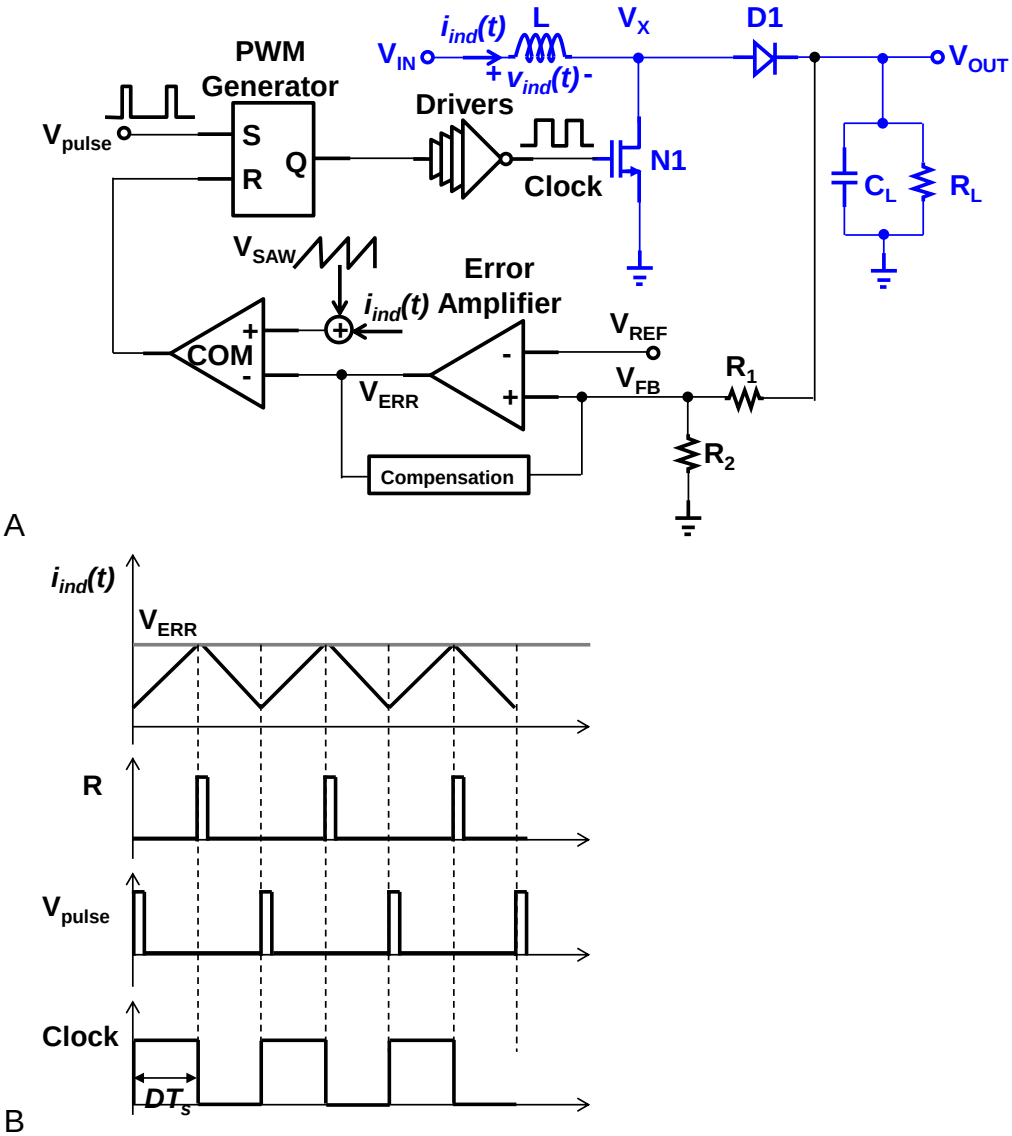


Figure 2-20. Current mode PWM control for SI boost. A) Block diagram, B) Representative waveforms.

Improvements in loop dynamics of the voltage mode PWM is impressive. The inductor current rises with a slope determined by V_{IN} and V_{OUT}, the current feedback

loop will respond immediately to line and load voltage changes. The error amplifier is used to modulate the output current rather than voltage, the effect of the inductor is minimized and the filter offers only a single pole [26]. Therefore simpler compensation and high gain bandwidth can be achieved compared to voltage mode PWM. The drawback of current mode PWM is that an extra ramp V_{SAW} is required for slope compensation as shown in Figure 2-20 [26].

2.4.3 Pulse Frequency Modulation (PFM)

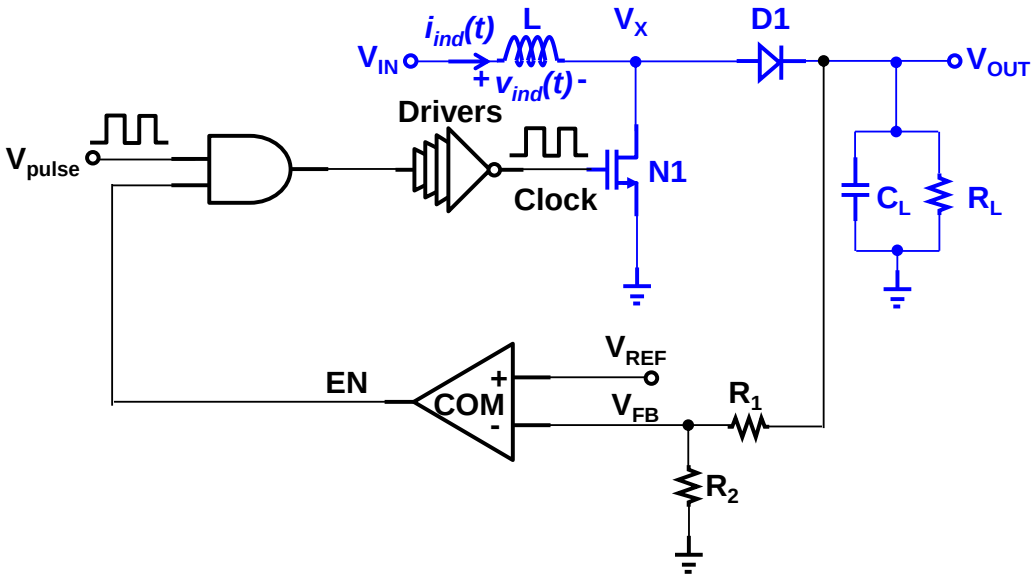


Figure 2-21. Block diagram of PFM control loop for SI boost.

A voltage or current mode PWM controller employs a fixed switching frequency, and will cause large switching power loss and yield a low efficiency at light load. To maintain good efficiencies over a wide load range, PFM control is usually used. Figure 2-21 shows block diagram of a simple PFM control loop. The feedback voltage V_{FB} is compared to the reference voltage V_{REF} and the output EN determines the number of pulses passed to drive the switch N1. Whenever V_{FB} is greater than V_{REF}, EN turns to low and stops clocking the drivers. In general, some hyteresis is designed with the comparator to provide better noise margins.

PFM control is very simple to design, and improves efficiency at light load. But its loop response is very slow. Moreover, the constant duty cycle of V_{pulse} limits the maximum output power, and is not usually utilized in heavy load. PFM is more commonly used for SC converters.

CHAPTER 3
CUSTOM HIGH VOLTAGE POWER DEVICES IN STANDARD CMOS PROCESS

3.1 Introduction of High Voltage Devices

When integrating switching step-up voltage converters in a standard CMOS process, high voltage stresses will be seen across power switches and rectifiers and then induce various undesirable effects such as channel hot-carrier effects, punch through breakdown, avalanche breakdown, gate-oxide breakdown. These effects will cause degradation of the device characteristics or even destruction and therefore investigation of these effects is necessary to determine the voltage limit for the integrated converters. This chapter will first introduce the mechanisms of the undesirable effects, and then present developed power rectifiers and switches in the standard 130nm CMOS process and investigate their voltage limits.

3.2 Voltage Limit Effects in Standard CMOS Process

3.2.1 Channel Hot Carrier Effects

In MOSFETs, as minority carriers flow from the source to the drain along the channel, they acquire a continuous increase in kinetic energy and become energetic in the high field region of the drain junction. These energetic carriers are known as channel hot carriers. At certain circumstances, the carriers may gain enough energy to cause impact ionization or even enter into the gate oxide and degrade the transistors' performance. Figure 3-1 illustrates the channel hot carrier effects in the cross-section of a saturated NMOS [1]. When impact ionization occurs, secondary electron-hole pairs are generated and constitute the drain-source current I_{ds} and the substrate current I_{sub}. The substrate current will create a local ohmic voltage drop in the substrate and forward bias the substrate-source junction resulting in a snapback breakdown [1]. When hot

carriers have too much energy to overcome the energy barrier of the Si-SiO_2 interface, they inject into the gate oxide, get trapped in the oxide or form the gate current I_g. The trapped carriers will shift the device threshold, damage the gate oxide, reduce the lifetime of the transistors [30][31], which is also called time-dependent dielectric breakdown (TDDB) [32].

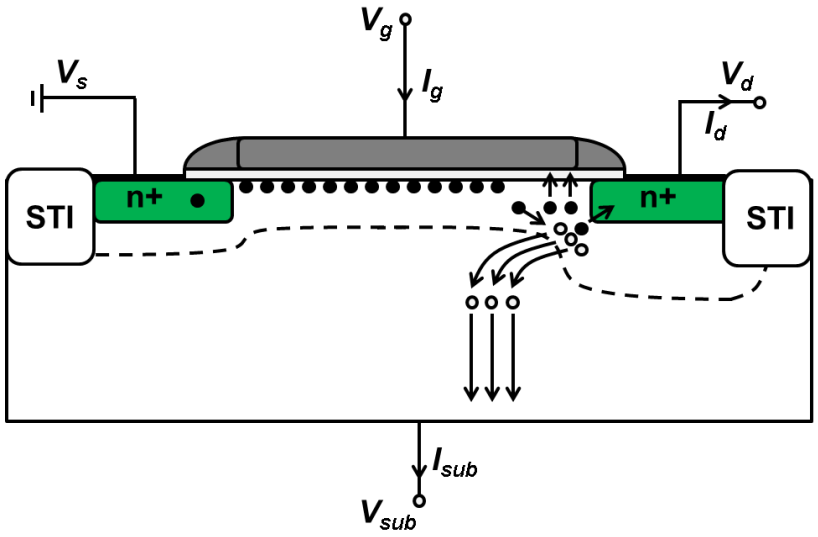


Figure 3-1. Channel hot carrier effects in the cross-section of a saturated nMOS.

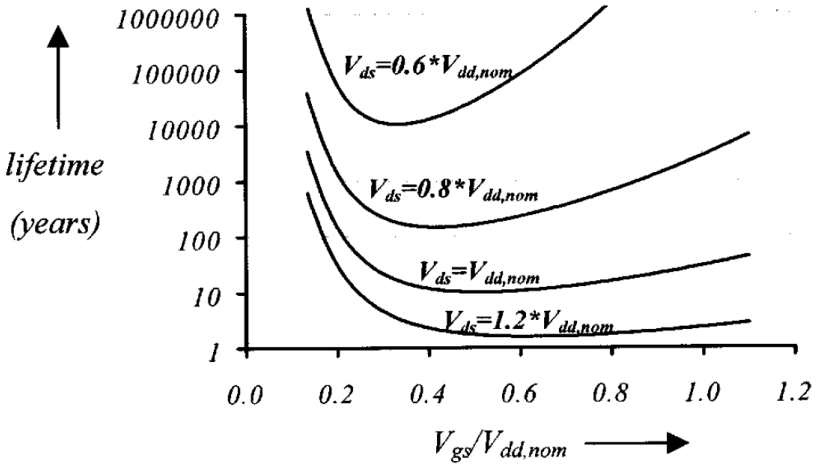


Figure 3-2. Typical bias-lifetime behavior for minimum length MOS transistors [33].

Figure 3-2 is a typical hot-carrier-based lifetime versus biasing plot for a minimum length transistor [33]. $V_{dd,nom}$ in the figure is the nominal supply voltage of the process.

Longer transistors have larger lifetime. As an extremely crude rule of thumb, the ratio of gate voltage to oxide thickness must be kept under approximately 0.7V/nm to satisfy the lifetime requirement of 10 years at 125ºC [34].

3.2.2 Gate Oxide Breakdown

As CMOS technology node is developing smaller and smaller, gate oxides are getting thinner and secondary carriers will be more easily collected by the gate electrode rather than stay trapped in the oxide. TDDB is less severe and the gate voltage is primarily limited by gate oxide breakdown, which occurs for gate fields exceeding about 1V/nm, as another crude rule of thumb [34].

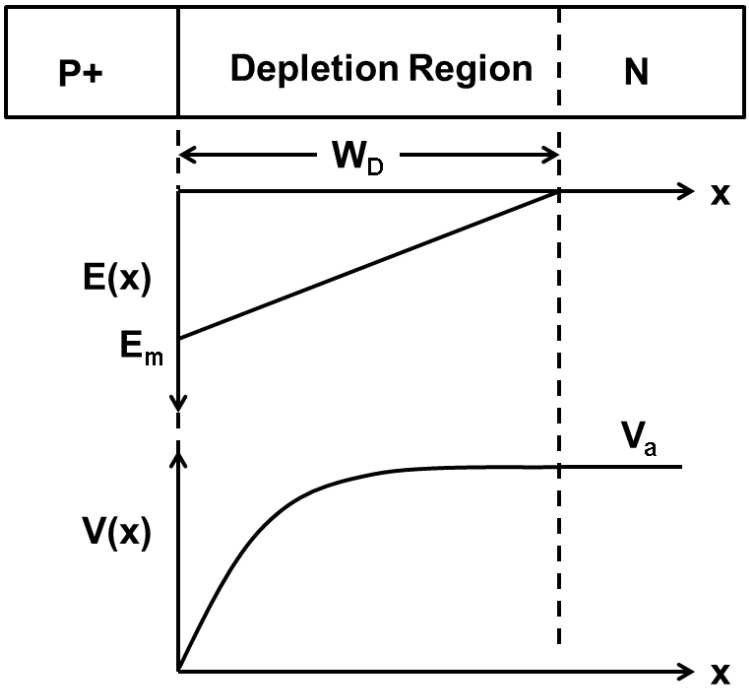


Figure 3-3. Electrical field and potential distribution for an abrupt parallel-plane P+/N junction.

3.2.3 Avalanche Breakdown

Maximum allowable voltage across a junction is mainly determined by avalanche breakdown mechanism. In a reverse biased junction, the high electric field sweeps out any electron or hole in the depletion region. When the energy of the electron or hole is

high enough to cause the impact ionization process reach an infinite rate, current increases rapidly and avalanche breakdown occurs.

Take an abrupt one-dimensional P+/N junction diode as an example. Figure 3-3 illustrates its electric field and potential distribution when reverse biased. From Poisson's equation, the thickness of the depletion region (W_D) is derived as [36]:

$$W_D = \sqrt{\frac{2\varepsilon_s V_a}{qN_D}} \tag{3-1}$$

where V_a is the applied reverse bias, ε_s is the dielectric constant for the semiconductor, q is the electron charge, and N_D is the donor concentration in the uniformly doped N-region.

The maximum electric field at the junction is then obtained:

$$E_m = \sqrt{\frac{2qN_D V_a}{\varepsilon_s}} \tag{3-2}$$

As the applied bias voltage increases, the maximum electric field approaches values at which significant impact ionization begins to occur. From Chynoweth's law and Fulop's power law [36], analytical solutions for the breakdown voltage and the corresponding maximum depletion layer width can be derived for silicon:

$$BV_{PP}(Si) = 5.34 \times 10^{13} N_D^{-3/4} \tag{3-3}$$

and

$$W_{PP}(Si) = 2.67 \times 10^{10} N_D^{-7/8} \tag{3-4}$$

3.2.3.1 Planar junction edge effects

In modern CMOS process, a planar junction is formed by the diffusion of impurities through a window in a silicon dioxide mask, as shown in Figure 3-4. As dopants migrate

vertically to produce a parallel-plane junction, lateral diffusion creates cylindrical-shaped junctions at the edges and spherical junctions at the corners of the diffusion window. These edge curvatures reduce the breakdown voltage of the planar junction [37].

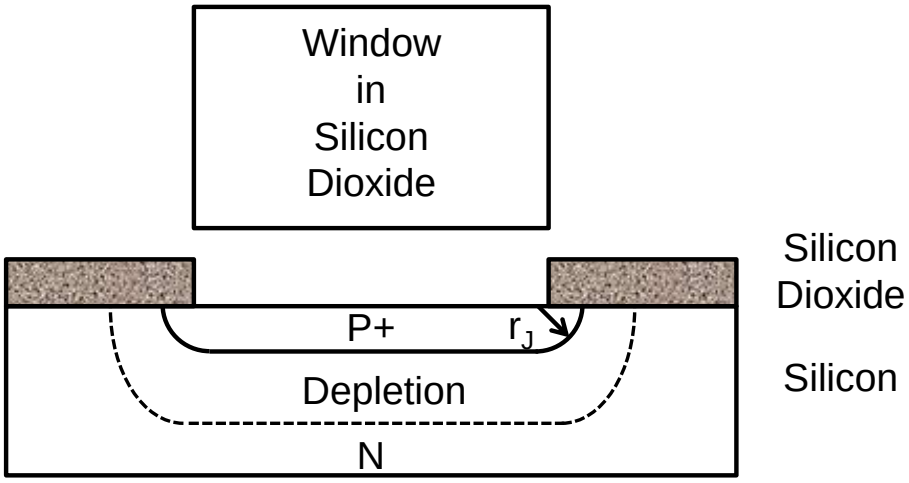


Figure 3-4. The planar junction created by diffusion through a window in a silicon dioxide mask [36].

Edge effects are very important in CMOS process. As shown in Figure 3-4, assume the junction depth is r_J. Analysis of the breakdown voltage BV_{CYL} for the cylindrical junction and the breakdown voltage BV_{SP} for the spherical junction gives the normalized results to the breakdown voltage BV_{PP} for the parallel-plane junction as follows [36]:

$$\frac{BV_{CYL}}{BV_{PP}} = \frac{1}{2}\left[\left(\frac{r_J}{W_{PP}}\right)^2 + 2\left(\frac{r_J}{W_{PP}}\right)^{6/7}\right]\ln\left[1+2\left(\frac{W_{PP}}{r_J}\right)^{8/7}\right] - \left(\frac{r_J}{W_{PP}}\right)^{6/7} \tag{3-5}$$

and

$$\frac{BV_{SP}}{BV_{PP}} = \left(\frac{r_J}{W_{PP}}\right)^2 + 2.14\left(\frac{r_J}{W_{PP}}\right)^{6/7} - \left[\left(\frac{r_J}{W_{PP}}\right)^3 + 3\left(\frac{r_J}{W_{PP}}\right)^{13/7}\right]^{2/3} \tag{3-6}$$

The normalized breakdown voltages predicted by equations (3-5) and (3-6) are plotted in Figure 3-5 as a function of the normalized radius of curvature [36]. As seen in

Figure 3-5, the junction breakdown voltages increase with the radius of curvature. However, in reality, it is impractical to obtain a normalized radius of curvature of more than 0.4, making it difficult to raise the normalized breakdown voltage for the cylindrical junction to above 50% of the parallel-plane case [36].

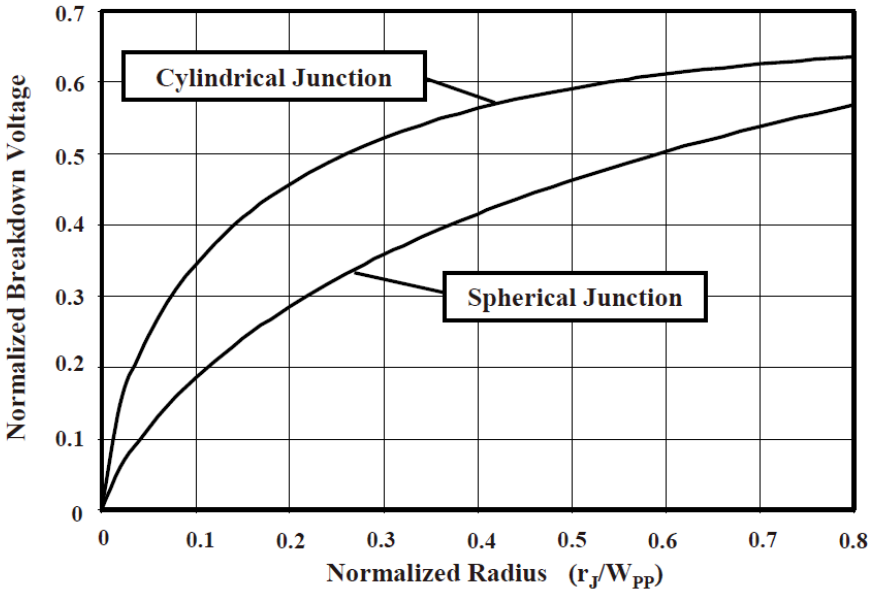


Figure 3-5. Breakdown voltages of cylindrical and spherical junctions normalized to the parallel-plane junction [36].

3.2.3.2 Layout improvement techniques

To improve the breakdown voltage of planar junctions, floating field rings can be employed to surround the junction window without additional process steps. The top view and the cross-section of this technique are illustrated in Figure 3-6. Floating field rings must be placed within the depletion region of the main junction with an optimal spacing to perturb the electric field and provide an improvement in the breakdown voltage. Analysis shows the breakdown voltage of a cylindrical junction with an optimal floating field ring BV_{FFR} is obtained as [36]:

$$\frac{BV_{FFR}-BV_{CYL}}{BV_{PP}}=\frac{1}{2}\left(\frac{r_J}{W_{PP}}\right)^2-0.96\left(\frac{r_J}{W_{PP}}\right)^{6/7}+1.92\left(\frac{r_J}{W_{PP}}\right)^{6/7}\ln\left[1.386\left(\frac{W_{PP}}{r_J}\right)^{4/7}\right] \qquad (3\text{-}7)$$

Analytical solutions calculated from equations (3-5) and (3-7) are plotted in Figure 3-7 and the normalized breakdown voltage of the planar junction with a floating field ring is 2X larger than that of the cylindrical junction. The breakdown voltage can even be further improved by using multiple floating field rings [36].

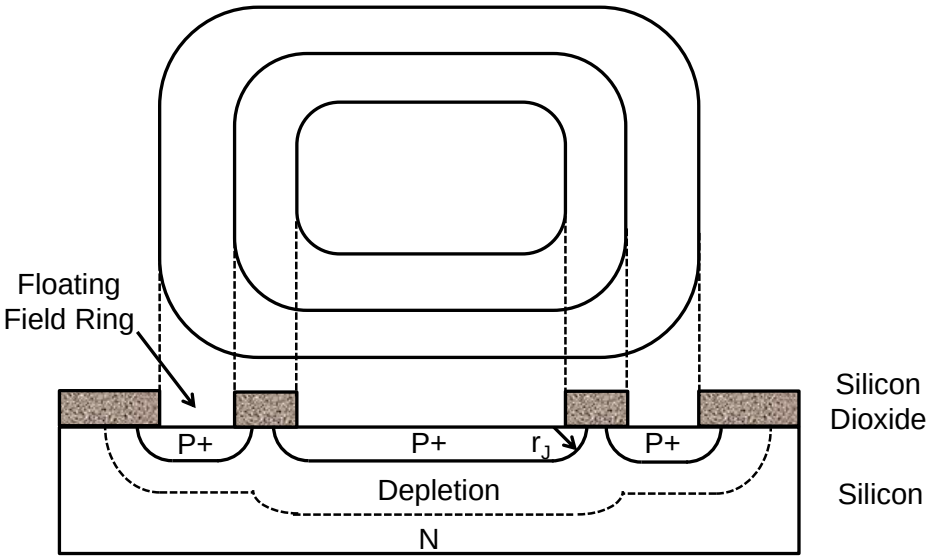


Figure 3-6. The planar junction with a floating field ring.

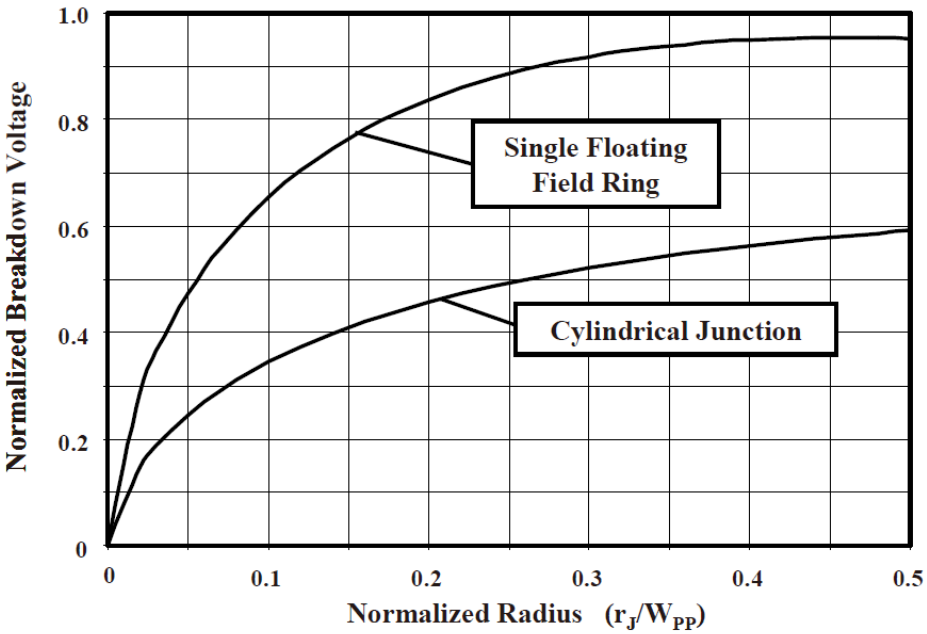


Figure 3-7. Comparison of the normalized breakdown voltages of cylindrical junctions with and without a single floating field ring [36].

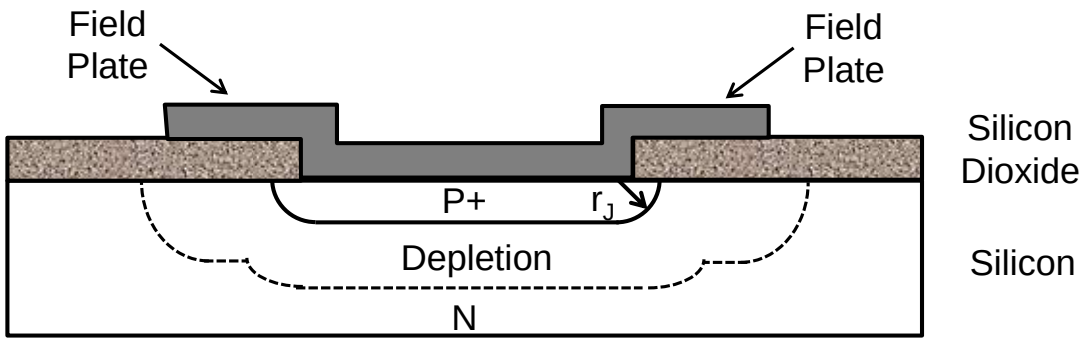


Figure 3-8. A planar junction with metal field plate over the edges.

Another layout technique to minimize the edge effects is by using field plate [36], which is illustrated in Figure 3-8 for a P+/N diode. The contact metal for P+ region is extended to form a field plate at the edges. The negative potential in the metal field plate pushes extends the depletion region and the breakdown voltage of the planar junction is increased. Furthermore, floating field rings and field plates can be utilized together to achieve highest breakdown voltages.

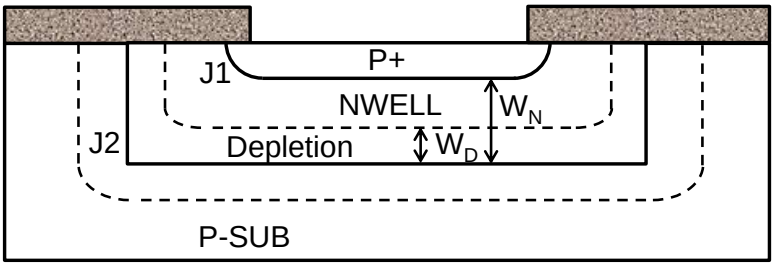


Figure 3-9. A parasitic PNP transistor in CMOS process.

3.2.3.3 Open-base transistor breakdown

In modern CMOS processes, especially when multiple wells exist, power devices may contain parasitic back-to-back junctions. The breakdown voltage for the parasitic structure is further reduced because the impact ionization can be amplified by the gain of the bipolar transistor, which is called open-base transistor breakdown [38].

Figure 3-9 shows a parasitic PNP structure in CMOS process with junctions J1 and J2. W_N denotes the depth of the NWELL minus the depth of the P+ region, and W_D

is the width of the depletion region in NWELL. When W_N is much bigger than the maximum depletion width when avalanche breakdown happens at J2, the breakdown voltage of this PNP structure is the same as the planar junction J2. However, if the depletion region reaches P+ region before avalanche breakdown happens, holes from P+ region enter the depletion region and are amplified to generate a big current flow, which is called reach-through breakdown. The open-base transistor breakdown voltage can be approximated by the reach-though breakdown voltage BV_{RT} which is derived as

$$BV_{RT} = \frac{qN_D W_N^{\ 2}}{2\varepsilon_s}\left(1+\frac{N_D}{N_A}\right) \tag{3-8}$$

3.2.4 Electromigration

As current flows through a conductor, metal atoms will be transported from one point to another creating voids and hillocks or extrusions in the conductor. This mechanism is called electromigration. Electromigration might induce short or open circuit if voids and extrusions are big enough. To prevent this mechanism, a width of 1μm per 1mA DC current for metal lines is used as a rule of thumb [45].

3.3 Schottky Barrier Diodes

Schottky barrier diodes (SBDs) are commonly utilized as rectifiers in switching power converters because of their high cut-off frequency and low forward voltage drop [39]. Silicon SBDs can be fabricated in standard CMOS process without extra process steps [41] thus leading to lower cost and monolithic integration. SBDs with cut-off frequency over 1THz have been demonstrated in standard 130nm CMOS process [42].

3.3.1 Schottky Barrier Contact in CMOS

Schottky barrier contact is not generally available in standard CMOS process. However, salicidation, which is primarily used to improve the conductivity of poly and

n^+/p^+ regions, can be employed to form Schottky barrier contacts by blocking n^+/p^+ implantation in the selected active regions (NWELL or PWELL). In 130nm CMOS process, Co is generally used as the transition layer for salicidation, therefore $CoSi_2$-Si schottky contacts can be formed. Figure 3-10 shows the layouts and cross-sections of n-type and p-type SBDs that were fabricated in 130nm CMOS process. Shallow trench isolation (STI) around the schottky contacts are used to separate the two terminals and reduce the leakage currents.

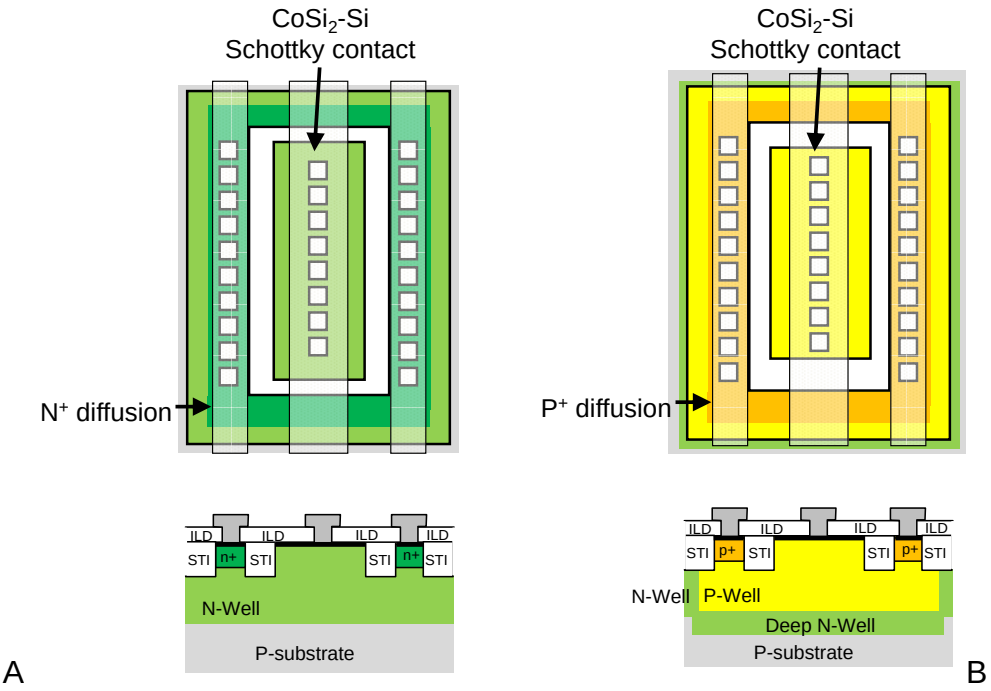


Figure 3-10. Layouts and cross-sections of n-type and p-type SBDs. A) SBD of n-type, B) SBD of p-type.

3.3.2 Guard Rings for SBDs

At the perimeter of the schottky contacts, large electric fields will be induced due to small barrier height and the edge effects, and hence large reverse leakage currents exist. Diffused guard rings can be employed to further reduce the reverse leakage currents and therefore the breakdown voltage can be improved. Figure 3-11 shows the

layouts and corresponding cross-sections of n-type and p-type SBDs with p^+/n^+ guard rings that were fabricated in 130nm CMOS process. The presence of p+/n+ guard rings avoids formation of spherical junctions at the corners of the diodes and creates parasitic parallel P-N junctions. To preserve the fast switching behavior, the SBDs with guard rings should not be biased above 0.6V so that the parasitic parallel P-N junctions are not turned on and only majority carriers are injected into the drift regions.

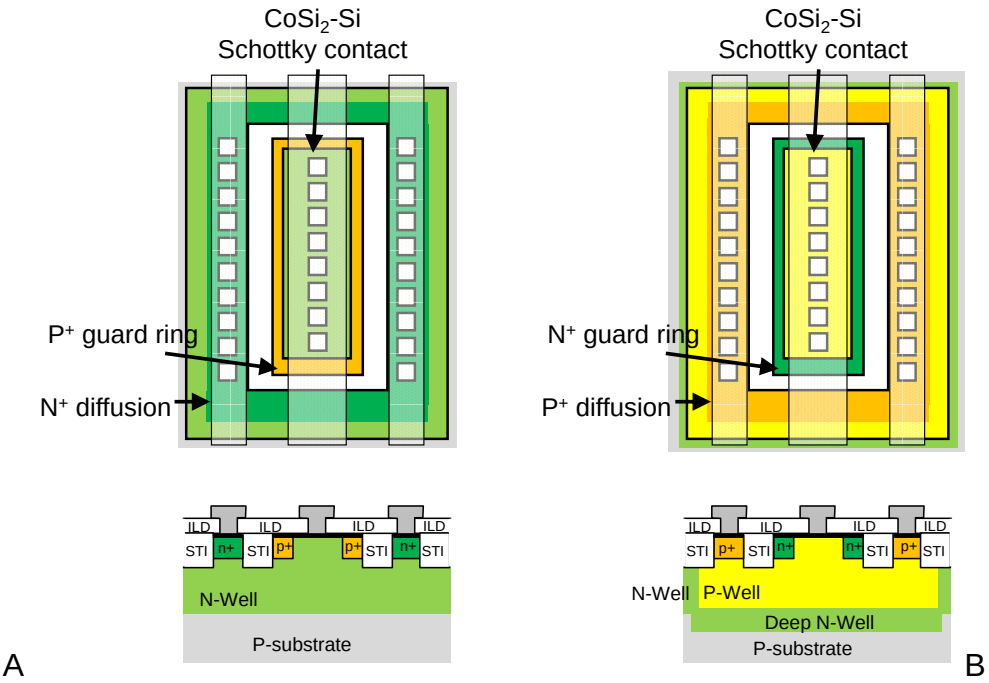


Figure 3-11. Layouts and cross-sections of n-type and p-type SBDs with p^+/n^+ guard rings. A) SBD of n-type with p+ guard ring, B) SBD of p-type with n+ guard ring.

3.3.3 Measurement Results and Parameter Extraction

N-type and p-type SBD test kits with and without p^+/n^+ guard rings have been fabricated in the standard 130nm CMOS process. Measured current densities versus bias voltage for them are plotted in Figure 3-12. As shown in Figure 3-12, measured reverse bias voltages at the reverse current density of $1A/cm^2$ are 8.5V for n-type and 0.1V for p-type SBDs when no guard rings are presence. In contrast, the reverse bias

voltages are improved to be 11.5V for n-type and 12V for p-type SBDs when guard rings are used.

From the thermionic emission model, the current density (J) for SBD with moderately doped semiconductor and forward bias voltage $V_F>3kT/q$ is [42],

$$J = A^* T^2 \exp\left(\frac{-q\phi_{BI}}{kT}\right)\exp\left(\frac{qV_F}{\eta kT}\right) \tag{3-9}$$

where J is the current density, A^* is the effective Richardson constant for metal-semiconductor interface, T is the absolute temperature, q is the electron charge, k is the Boltzmann constant, Φ_{BI} is the barrier height, and η is the ideality factor. From equation (3-9), the barrier height Φ_{BI} can be extracted as,

$$\phi_{BI} = \frac{kT}{q}\ln\left(\frac{A^* T^2}{J_s}\right) \tag{3-10}$$

where J_s is the extrapolated saturation current density at 0V bias.

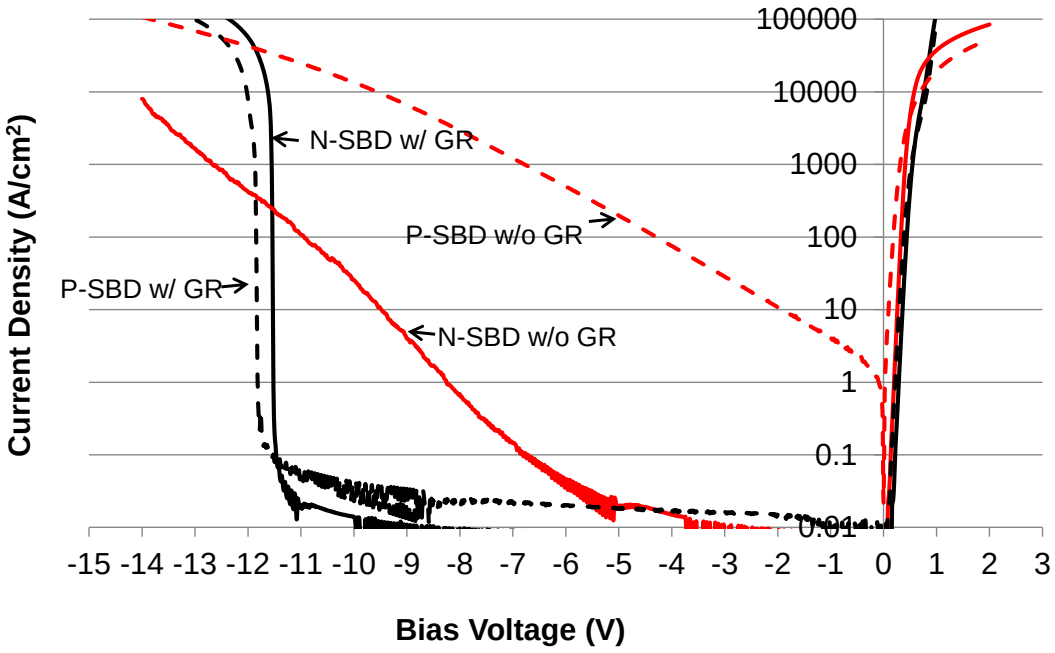


Figure 3-12. Measured current densities versus bias voltage for n-type and p-type SBDs with and without p^+/n^+ guard rings (GR).

Figure 3-13 shows extracted slopes and extrapolated current densities at 0V bias. From the extracted slopes, the ideality factors can be calculated as 1.05 and 1.75 for n-type SBDs w/o and w/ guard ring, 1.44 and 1.75 for p-type SBDs w/o and w/ guard ring. Furthermore, from equation (3-10) and the extrapolated current densities at 0V in Figure 3-13, the barrier heights are also derived as 608mV and 659mV for n-type SBDs w/o and w/ guard ring, 393mV and 566mv for p-type SBDs w/o and w/ guard ring. Here, the effective Richardson constants used are assumed to be 1.12 $\mu A/\mu m^2K^2$ for electrons and 0.32 $\mu A/\mu m^2K^2$ for holes [43]. Figure 3-14 shows extracted the specific on-resistance R_D for fabricated SBDs.

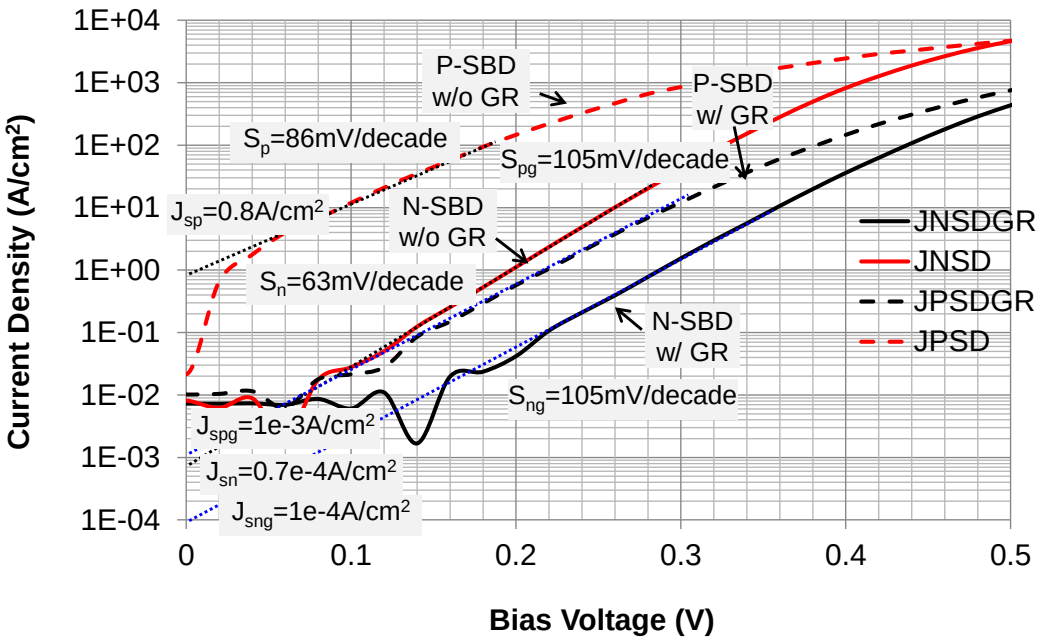


Figure 3-13. Extracted slopes and zero-bias current density for n- and p-type SBDs in 130nm CMOS.

Small signal capacitances of SBDs were also measured using Agilent network analyzer, from which cutoff frequency of the SBDs were calculated. All important DC and AC parameters for measured SBDs are summarized in Table 3-1. Generally, n-type devices have higher cut off frequency than their p-type counterparts due to electrons

have large mobility than holes. Moreover, guard rings add parasitic capacitance to the devices, so that cut off frequency is lower. A commercial SBD from Diodes Inc. is also shown in Table 3-1 for comparison.

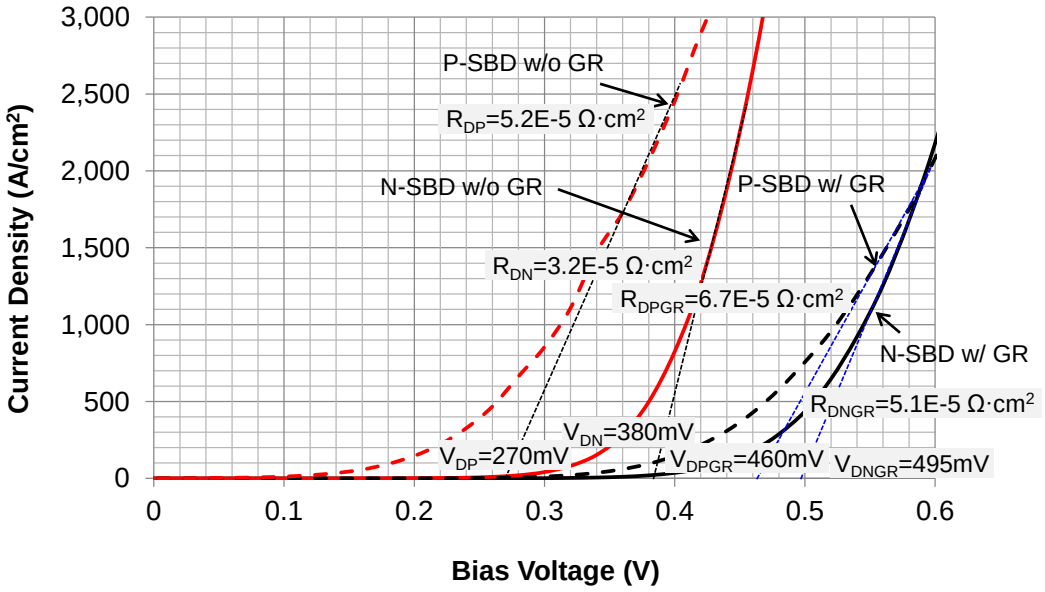


Figure 3-14. Extracted piecewise linear model parameters V_D, R_D for n- and p-type SBDs in 130nm CMOS.

Table 3-1. Extracted parameters for n- and p-type SBDs with and without guard rings in 130nm CMOS

	BV	η	Φ_{BI}	V_D	$A \cdot R_D$	f_T
Unit	(V@1A/cm^2)		(mV)	(mV@1A/cm^2)	(Ω·cm^2)	(GHz)
n-type SBD w/o guard ring	8.5	1.05	608	200	3.2e-5	26
p-type SBD w/o guard ring	0.1	1.44	393	30	5.2e-5	15
n-type SBD w/ guard ring	11.5	1.75	659	280	5.1e-5	12
p-type SBD w/ guard ring	12.0	1.75	566	220	6.7e-5	8
ZLLS410 [44]	10.0 (@200μA)	-	-	285 (@10mA)	-	6*

* Estimated from datasheet

3.4 Power Switches

In 130nm CMOS process, 1.2V thin oxide (3nm) and 3.3V thick oxide MOSFETs (7.3nm) are genuinely available and can be used as power switches. However,

integration of step-up voltage converters demands power switches with higher breakdown voltage. Lateral extended-drain MOSFETs and stacked MOSFETs have been investigated and demonstrated as two good candidates [29][45], and more importantly, they can be integrated in standard CMOS process without extra masking steps thus can keep integration of low cost. This section investigates the layout techniques of these two devices and then presents measurement results in 130nm CMOS.

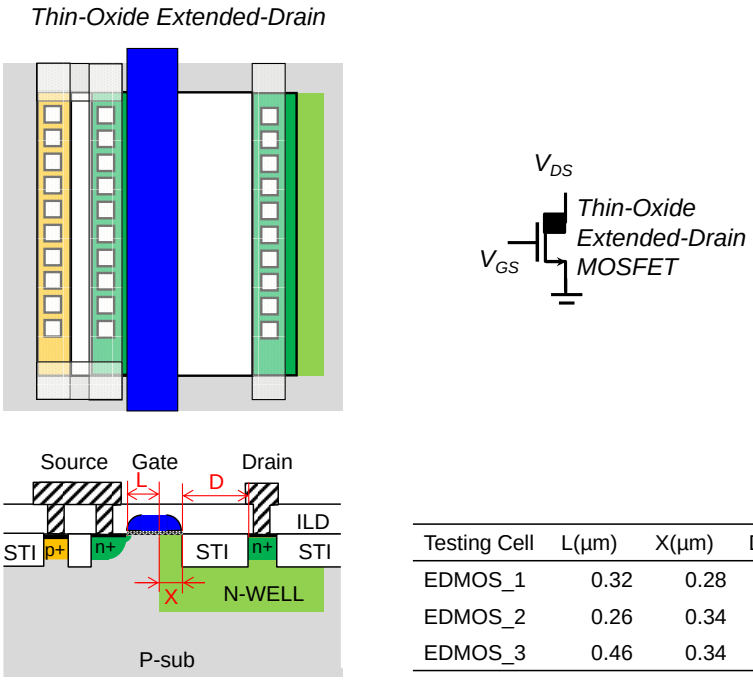
3.4.1 Extended-Drain MOSFET

Extended-drain MOSFET is an asymmetric device which is realized by replacing the normal highly-doped drain region with a lightly-doped either pwell or nwell standard layer. Therefore the extended drain allows a large depletion region and reduced electric field across the gate oxide, which yields a high breakdown voltage while maintaining a low on-resistance.

Extended-drain MOSFETs can be realized with only standard mask layers. Figure 3-15 illustrates the layout and cross-section of a thin-oxide extended-drain NMOS. A lightly-dope drift region (nwell) is placed underneath the gate oxide with an overlap length of *X*. The physical gate length is annotated as *L*. STI is used between the gate and the drain contact and its length is denoted as *D*. Testing cells with various dimensions of *L, X, D* are fabricated in 130nm and the variations are listed in Figure 3-15.

Figure 3-16 shows measured leakage current densities (J_{DS}) for the fabricated thin-oxide EDMOS cells when $V_{GS}=0$. Firstly, Figure 3-16 tells us that the leakage current density decreases with the increased gate length. Secondly, the breakdown voltages for all testing cells are very close to each other, which is $V_{BV}=9.83V$ at the

current density of *1A/cm*^{2}. Figure 3-17 shows measured on-state current densities for the thin-oxide testing cells when V_{GS}=*1.2V*, from which the on-resistances are obtained as 2.2e-4 Ω·cm^2, 1.4e-4 Ω·cm^2, 2.6e-4 Ω·cm^2 for EDMOS_1, EDMOS_2, EDMOS_3 respectively.



Testing Cell	L(μm)	X(μm)	D(μm)	W(μm)
EDMOS_1	0.32	0.28	0.245	12
EDMOS_2	0.26	0.34	0.245	12
EDMOS_3	0.46	0.34	0.490	12

Figure 3-15. The layout, cross-section, symbol and cell parameters of tested thin-oxide extended-drain MOSFET.

In contrast to the thin-oxide EDMOSs in Figure 3-15, extend-drain MOSFETs with thick gate oxide (7.3nm) are also designed and fabricated with the same dimensions of *L, X, D*. Figure 3-18 shows the corresponding layout, cross-section, symbol and the variations of the dimensions. Figure 3-19 plots measured leakage current densities for the testing cells. Compared to the thin-oxide EDMOSs, smaller leakage current densities are observed for the thick-oxide EDMOSs. Measured breakdown voltages for the thick-oxide EDMOSs are slightly higher, V_{BV}=*9.87V* at the current density of *1A/cm*^{2}. Figure 3-20 shows measured on-state current densities for the thick-oxide EDMOSs

and the corresponding on-resistances are extracted as 1.3e-4 Ω·cm^2, 1.6e-4 Ω·cm^2, 3.0e-4 Ω·cm^2 for EDMOS_4, EDMOS_5, EDMOS_6 respectively.

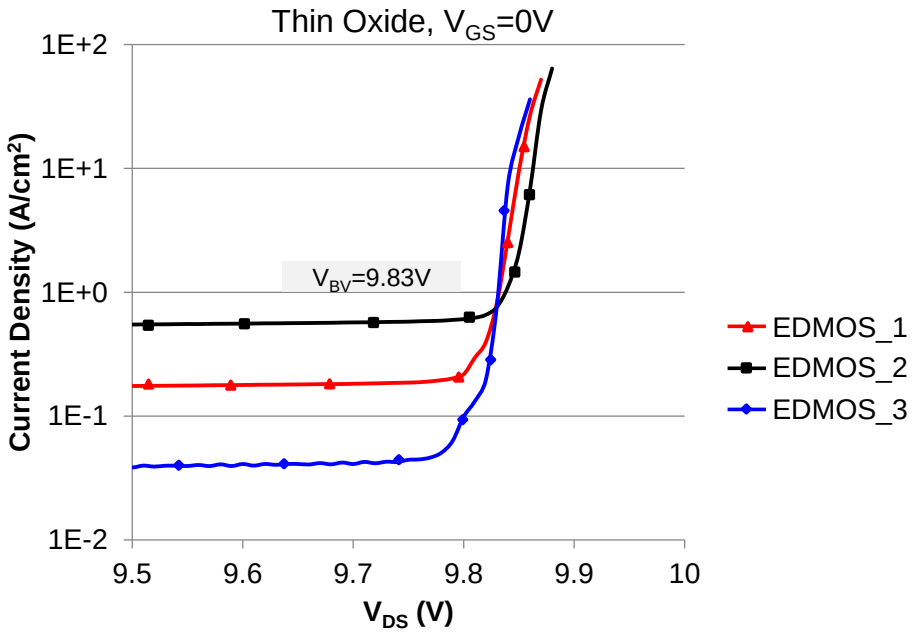


Figure 3-16. Measured leakage current densities for tested thin-oxide extended-drain MOSFET cells with V_{GS}=0V.

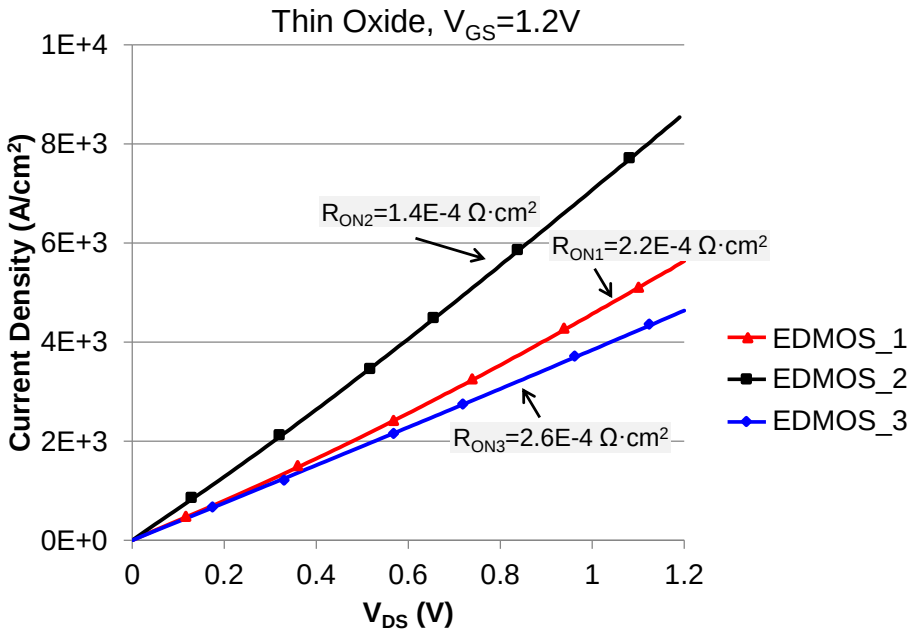
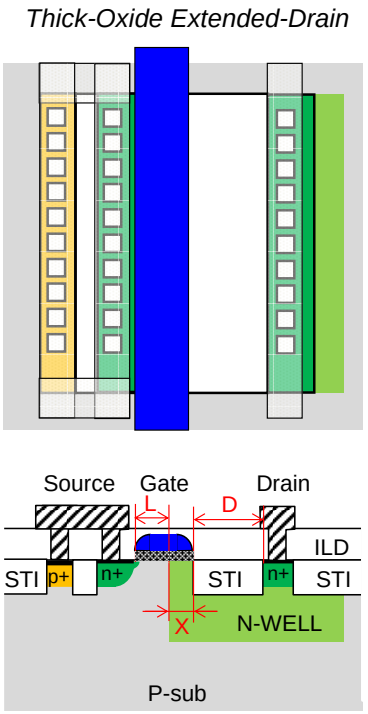
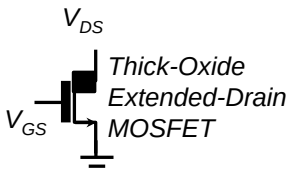


Figure 3-17. Measured current densities for tested thin-oxide extended-drain MOSFET cells with V_{GS}=1.2V.





Testing Cell	L(μm)	X(μm)	D(μm)	W(μm)
EDMOS_4	0.32	0.28	0.245	12
EDMOS_5	0.26	0.34	0.245	12
EDMOS_6	0.46	0.34	0.490	12

Figure 3-18. The layout, cross-section, symbol and cell parameters of tested thick-oxide extended-drain MOSFET.

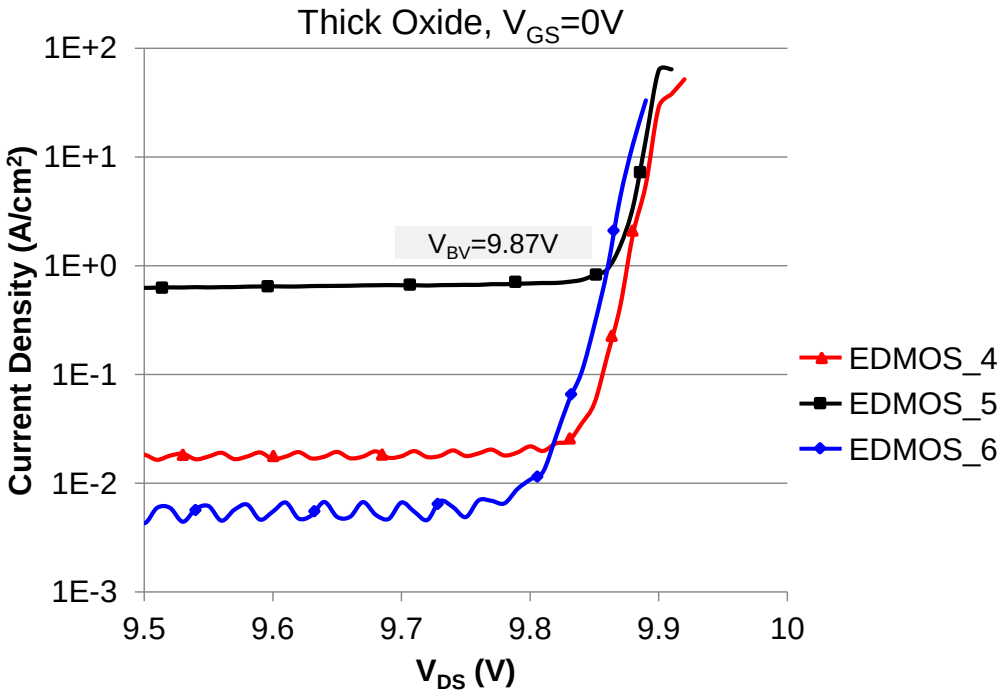


Figure 3-19. Measured leakage current densities for tested thick-oxide extended-drain MOSFET cells with V_{GS}=0V.

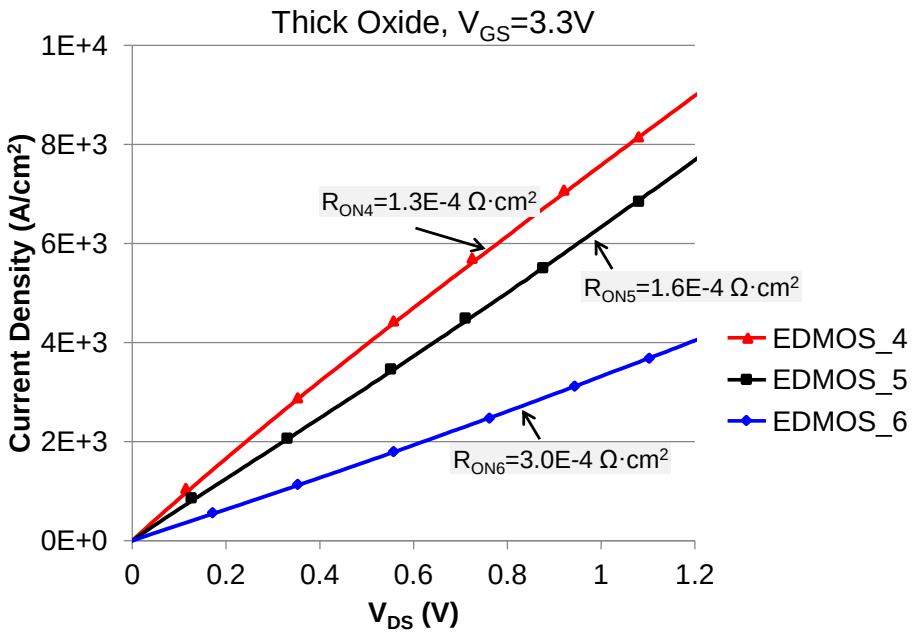


Figure 3-20. Measured current densities for tested thick-oxide extended-drain MOSFET cells with V_{GS}=3.3V.

3.4.2 Stacked MOSFET

Stacked MOSFET, which means that the source of one transistor is connected to the drain of another, can reliably sustain a multiple of the nominal supply voltage by distributing the voltage stress across the chain of the MOSFETs. Gate biasing is extremely important to maintain the lifetime of these devices. Figure 3-21 illustrates proper gate biasing when two and *n* NMOS are stacking. When the stacked switch in on, the drain and the source terminals are all connected to ground, and all the gates should be biased at V_{DD}; when the stacked switch is off, each NMOS blocks one V_{DD}, therefore the gate biases must increase from 0 for the lowermost NMOS to (n-1)VDD for the uppermost NMOS. Moreover, when PMOSs are stacking, the gates should be biased similarly.

In 130nm CMOS, two stacking structures have been investigated. The first structure consists of a 3.3V thick-oxide NMOS stacking on the top of a 1.2V thin-oxide

NMOS and Figure 3-22 shows its representative layout and cross-section. With a fixed bias for the top device, this composite switch only requires one single driving clock, thereby providing a better figure of merit in terms of gate capacitance per drain current. This structure also eliminates level conversion circuits and reduces the time delay in the control loop, thereby yielding faster transient responses. Minimum lengths of 340nm for thick-oxide devices and 120nm for thin-oxide devices are used to save area. The widths are chosen as 13µm, 14µm respectively and multiple fingers can be used in parallel to reduce its on-resistance.

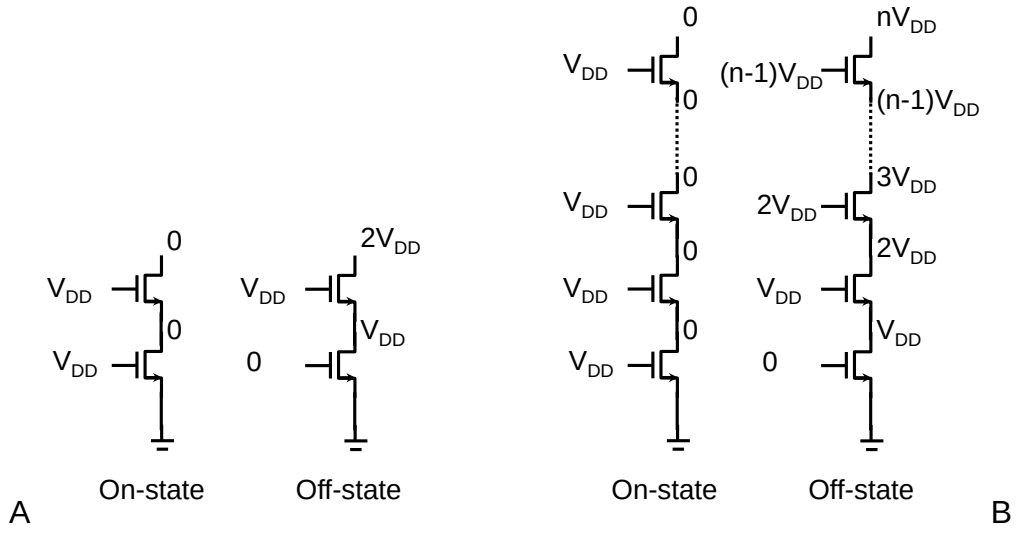


Figure 3-21. On-state and off-state gate biasing stacked NMOS switches. A) Two stacked NMOS, B) Stacked NMOS with n>2.

The bias voltage for the top NMOS has to be selected carefully to ensure 10-year life time at 125°C, which indicates that the electrical field across the gate oxide must be less than 0.7V/nm. Therefore the gate-oxide thickness of 2.5nm and 7nm for the bottom and the top NMOS results in the maximum gate-drain voltage as ~1.7V and ~5V respectively. Considering the threshold voltage of 0.63V and the body effect for the top NMOS, the bias voltage is chosen as 2.5V. Figure 3-23 plots measured current

densities when the stacked switch is on and off. As shown in Figure 3-23, the measured off-state breakdown voltage is ~10V and the on-state resistance is ~1.9e-5 Ω·cm^2. The total switched gate charge, estimated via simulations to be ~25nC/mm^2, yields a figure of merit (FOM) [46]of ~48mΩ-nC at V_D=6V. However, considering time dependent dielectric breakdown, the block voltage for this switch is recommended as ~6V and safe operation duration of ~1 month has been observed in our experiments. An improvement of roughly 1.8x over a standard 3.3V thick-ox device is achieved. Compared to core 1.2V devices, voltage improvement is 5x.

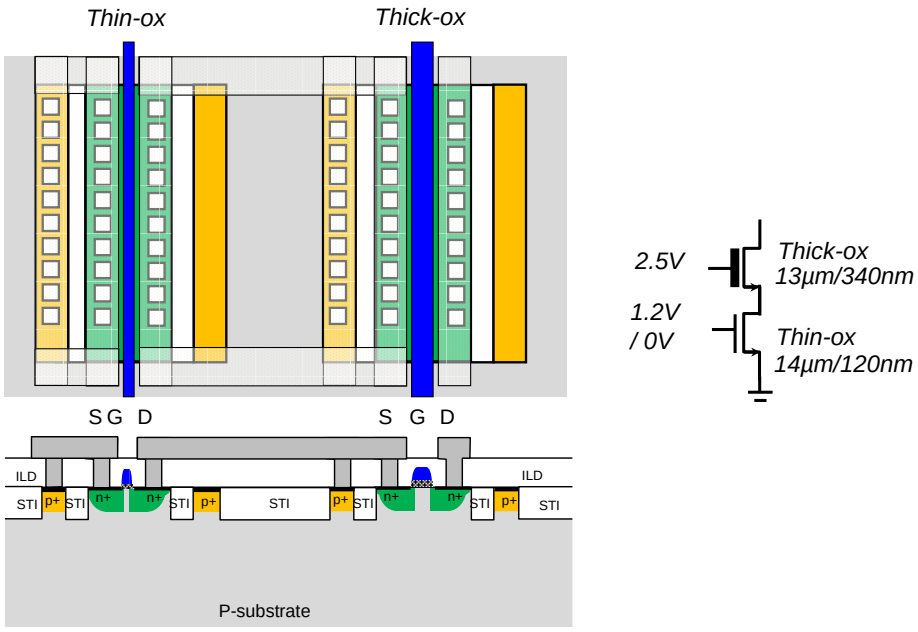


Figure 3-22. The layout and cross-section of a switch stacking a thick-oxide NMOS on the top of a thin-oxide NMOS.

The second high-voltage tolerant synchronous switch that has been investigated is shown in Figure 3-24 with representative layout and cross-section. This switch is composed of a 3.3V thick-ox NMOS in T-WELL and a 3.3V thick-ox low-V_T footer NMOS. Compared to the first stacking structure, the footer transistor is able to handle higher blocking voltages therefore a larger bias of 3V is chosen for the top transistor.

This switch can also be directly driven by 1.2V clocks and turns on and off very quickly.

Width/length ratios are chosen as 13µm/340nm for both transistors.

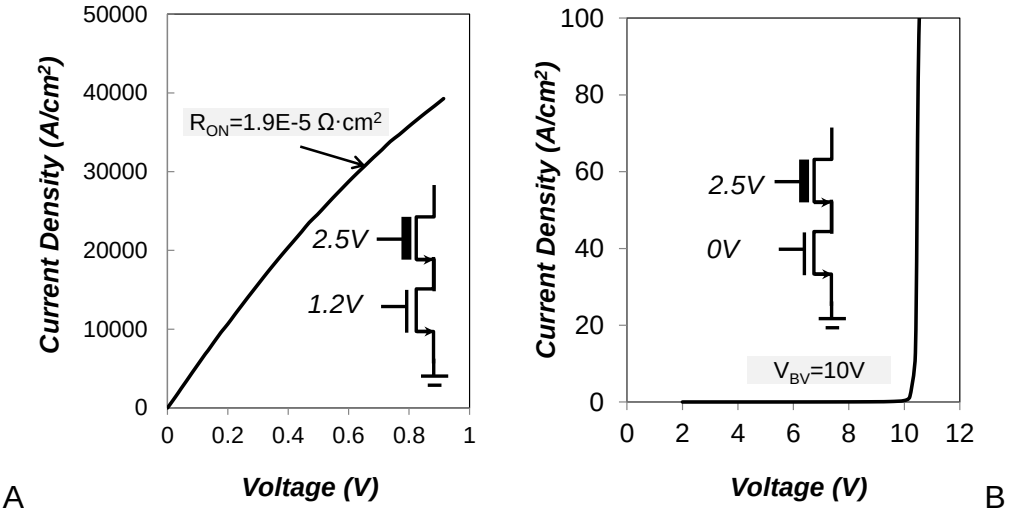


Figure 3-23. Measured on-state and off-state current density of the stacked switch with a 3.3V thick-oxide NMOS on the top of a 1.2V thin-oxide NMOS. A) On-state current density, B) Off-state current density.

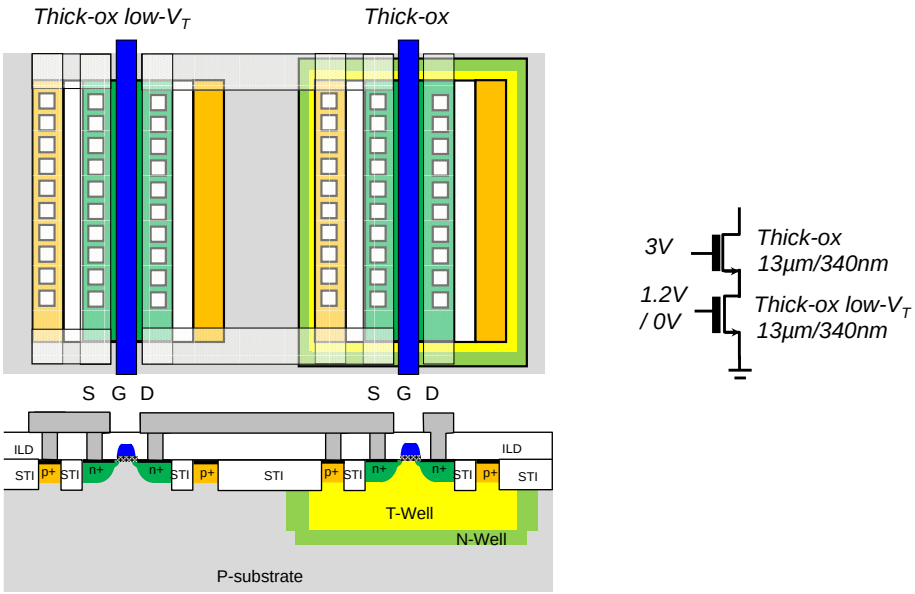


Figure 3-24. The layout and cross-section of a switch stacking a thick-oxide NMOS on top of a thick-oxide low-V_T NMOS in T-WELL.

Figure 3-25 shows measured on-state and off-state current densities for the second stacking switch. As shown in Figure 3-25, the measured off-state breakdown

voltage is also ~10V and the on-state resistance is ~1.5e-4 Ω·cm^2, which is ~8x larger than the first switch. However, considering time dependent dielectric breakdown, the block voltage for this switch is recommended as ~8V and safe operation duration of ~1 month has also been observed in our experiments, which achieves an improvement of roughly 2.5x over a standard 3.3V thick-ox device. Table 3-2 gives the summary of the measured important parameters for the fabricated extended-drain and stacked MOSFETs.

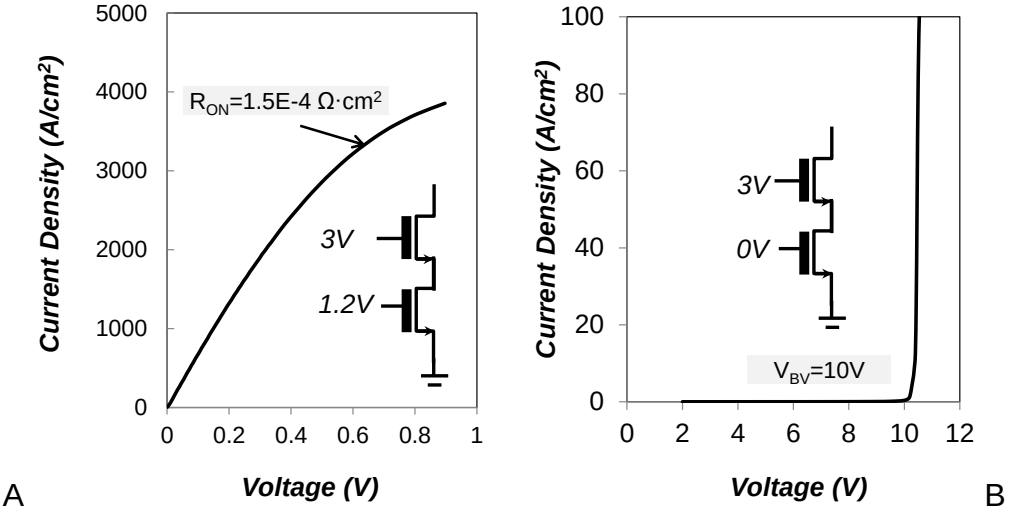


Figure 3-25. Measured current density of the stacked switch with a 3.3V thick-oxide NMOS on the top of a 3.3V thick-oxide low-V_T NMOS. A) On-state current density, B) Off-state current density.

Table 3-2. Summary of measured DC parameters for fabricated extended-drain and stacked MOSFETs

	BV (V@1A/cm^2)	A·R_{ON} (Ω·cm^2)	FOM (mΩ·nC)
EDMOS-1	9.83	2.2E-4	-
EDMOS-2	9.83	1.4E-4	-
EDMOS-3	9.83	2.6E-4	-
EDMOS-4	9.87	1.3E-4	-
EDMOS-5	9.87	1.6E-4	-
EDMOS-6	9.87	3.0E-4	-
Stacked-Switch w/ thin-ox transistor	10.00	1.9E-5	48
Stacked-Switch w/ thick-ox LVT transistor	10.00	1.5E-4	345

3.5 Performance Comparison

For silicon devices, there is always a tradeoff between the breakdown voltage and the specific on-resistance, which is defined as the product of the on-resistance and the area of the device. Theoretical analysis [46] gives a performance envelop for power devices, which is called the silicon limit and can be presented with the equation below:

$$R_{on-sp} = 5.9 \times 10^{-9} V_{BV}^{2.5} (\Omega \cdot cm^2) \quad (3\text{-}11)$$

where $R_{on\text{-}sp}$ is the specific on-resistance, V_{BV} is the breakdown voltage.

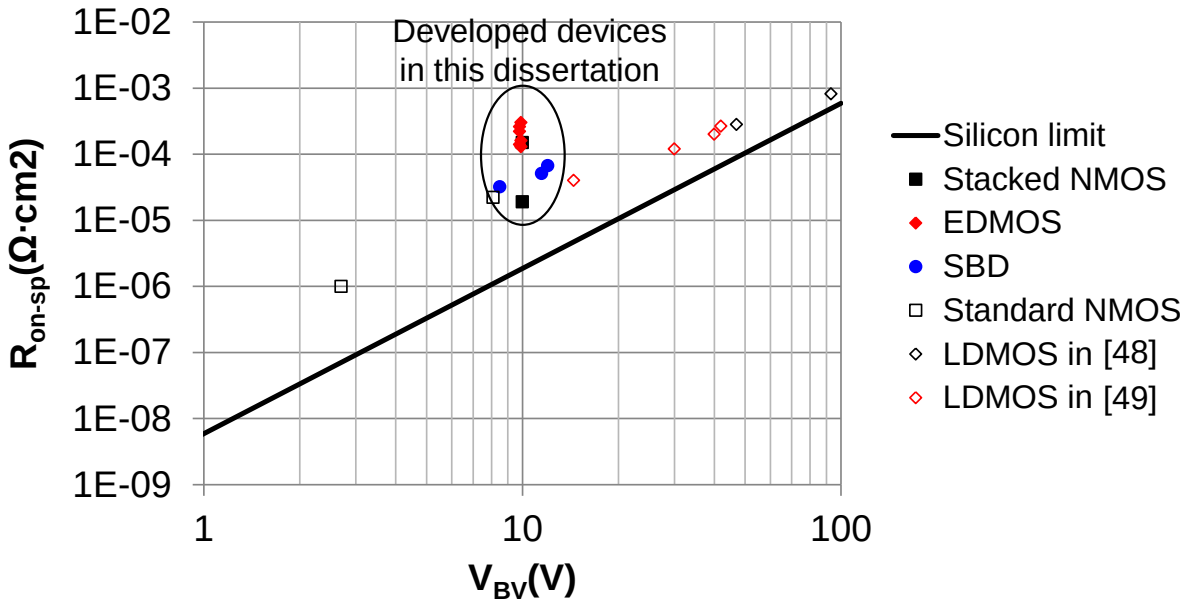


Figure 3-26. The silicon limit and performance comparison for developed power devices.

For illustrative purpose, the specific on-resistance $R_{on\text{-}sp}$ and the breakdown voltage V_{BV} for developed power devices in this chapter are plotted in Figure 3-26. Standard NMOS available in 130nm CMOS process and LDMOSs developed in [48][49] are also included in Figure 3-26 for comparison. Firstly, developed power devices, stacked NMOSs, EDMOSs and SBDs have improved breakdown voltages (~8-10V) compared to standard NMOSs in 130nm CMOS; Secondly, the stacked NMOSs have

better performance than the EDMOSs, which are further away from the silicon limit in Figure 3-26; Thirdly, by modifying the process parameters, LDMOSs could achieve better performances, closer to the silicon limit, as presented in [48][49]. Our developed stacked NMOS switches have comparable performance with LDMOSs in [48][49].

CHAPTER 4
50-100MHZ 8X HRBRID SI-SC AND SI-FLYBACK CONVERTER IN 130NM CMOS PROCESS

4.1 Introduction of Hybrid Converters

Numerous benefits exist for integrating switched-mode step-up converters in modern CMOS technologies. A highly integrated system, including power, RF communication subsystems, and digital processing, all on the same die, enables the development of microsystems for applications wherein scale and mass are of critical importance [3]. By utilizing the fine feature sizes of modern processes, designers can leverage high switching frequencies, resulting in the desired minimization of passives [7]. The primary challenge then becomes that of creating and processing large voltages within an inherently voltage limited process.

In this chapter, we will introduce and evaluate two hybrid boost converter topologies, SI/SC and SI/flyback, which are capable of sustaining nearly 8x the rated voltage using custom high-voltage devices developed in a standard 130nm CMOS process without additional process masks or modifications. These two topologies have been chosen to leverage the increased voltage handling capability of developed Schottky diodes (~10V) and stacked NMOS switches (~7V) when compared to standard and thick-oxide MOS switches with 1.2V and 3.3V ratings, respectively. These architectures also limit the maximum voltage stress across the switches, diodes, and passive components while still allowing for large output voltages.

4.2 Hybrid Converter Topologies

Conventional SI boost and flyback converters are not suitable for integration in low voltage processes due to large voltage stresses imposed on switches and diodes. The output voltage will be limited by the rating voltage of the process. Moreover, step-up

ratio may be further limited by realizable duty cycles and parasitic losses of the inductor and power stage [24]. Figure 4-1 shows calculated voltage conversion ratio of a SI boost converter considering inductor resistive loss. As R_{IND}/R_L increases, the maximum conversion ratio drops significantly, which is ~5 when R_{IND}/R_L=0.01. Larger conversion ratio may be realized using cascaded switched-inductor boost converters [50]. However, this method requires two sets of power devices and typically places large voltage levels across rectifiers nearest to the output, complicating or removing the possibility of full integration in standard CMOS processes.

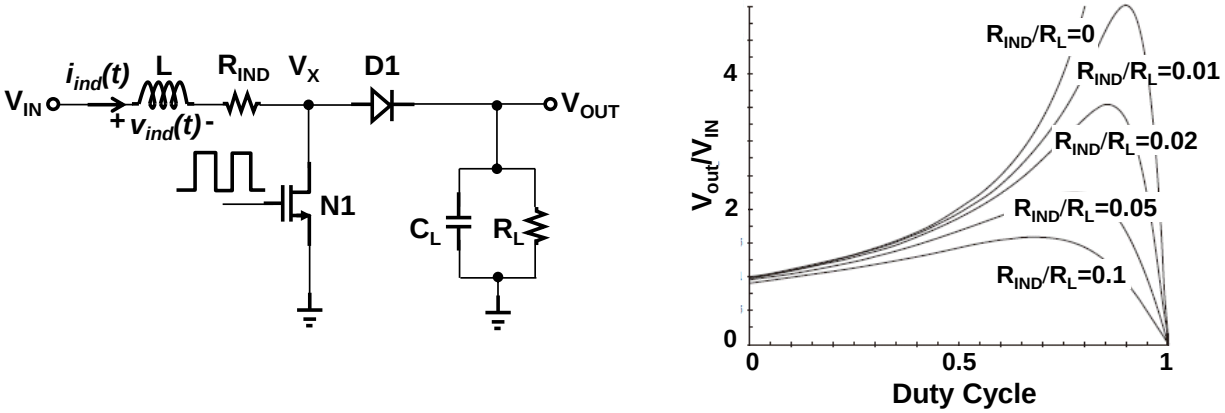


Figure 4-1. Voltage conversion ratio of a SI boost converter considering inductor resistive loss [24].

One promising solution for onchip high voltage generation is using SC converter topologies [51][52]. Voltage stress in SC converters is minimized and distributed, thereby enabling integration in low voltage processes. However, power efficiency of SC converters will drop significantly when voltage conversion ratio is non-integer, which complicates control loop design and voltage regulation.

Hybrid converters which combine the benefits of SI boost, flyback and SC converters have been demonstrated using discrete components [53][54]. However, their

integration in CMOS technologies has not been done before. This section will evaluate them in a 130nm CMOS technology and discuss their challenges and benefits.

4.2.1 SI-SC Converter

Figure 4-2 shows the configuration of a hybrid SI/SC converter composed of a switched-inductor (SI) stage followed by a switched capacitor (SC) voltage doubler. In the SI stage, a custom stacked switch comprised of a 3.3V thick-oxide and 1.2V thin-oxide footer transistor is used. Measurement has shown the blocking voltage of the stacked NMOS switch can be ~7.5V. In the SC stage, n-type SBDs with a guard ring and metal-in-metal (MIM) capacitors with density of ~1fF/μm^2 are used. Breakdown voltage of the SBDs and capacitors are >10V. Total capacitance in the SC stage is ~54pF.

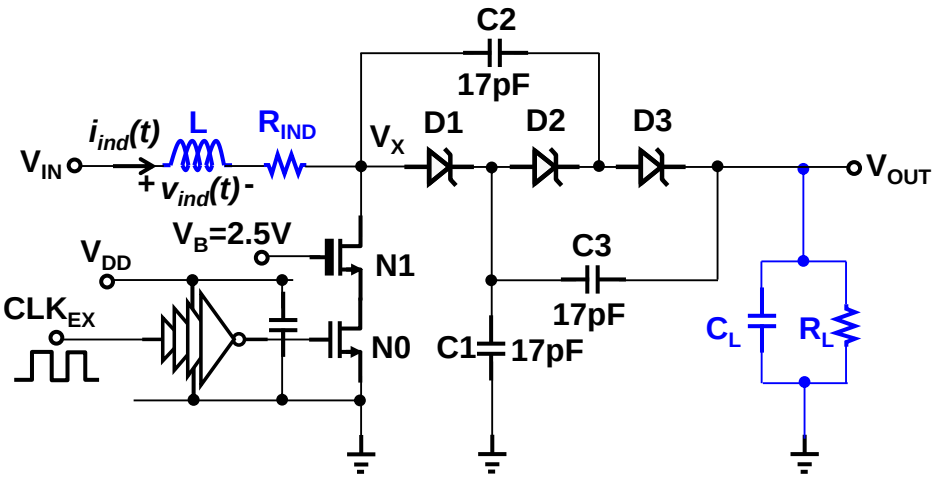


Figure 4-2. A hybrid SI/SC converter implemented in 130nm CMOS.

An Agilent 81250 Parallel Bit Error Ratio Tester is employed to create an external clock CLK_{EX} with variable frequency and duty cycle. The external clock is then fed into the driver for the synchronous stacked switch. As shown in Figure 4-3, when the composite switch is on, the inductor voltage is equal to V_{IN}, and the inductor current rises with a slope of V_{IN}/L. When the composite switch is off, the inductor voltage turns

to be negative as V_{IN}-V_C. Here V_C is the voltage over the capacitors, and can be calculated as V_{IN}/(1-D) when the inductor is continuous. Ideally, a square wave with magnitude of V_C will be seen at V_X, which drives the voltage doubler. The square wave first charges C1 to the peak voltage of VX (ignoring diode drops), charges C2 in the subsequent phase, and finally places the boosted voltage on output capacitor C_L when V_X peaks at the start of the next cycle. C3 assists in maintaining the output voltage, functioning similarly to C_L. In CCM, the output voltage is derived as

$$V_{OUT} = \frac{2V_{IN}}{1-D} \tag{4-1}$$

And voltage stresses for the stacked NMOS switch and SBDs are all equal to V_{OUT}/2, which is a half of that for a traditional SI boost. The voltage doubler could be replaced by other n-stage SC converters, which increases the output voltage nX larger while maintaining the same voltage stress for switches and diodes.

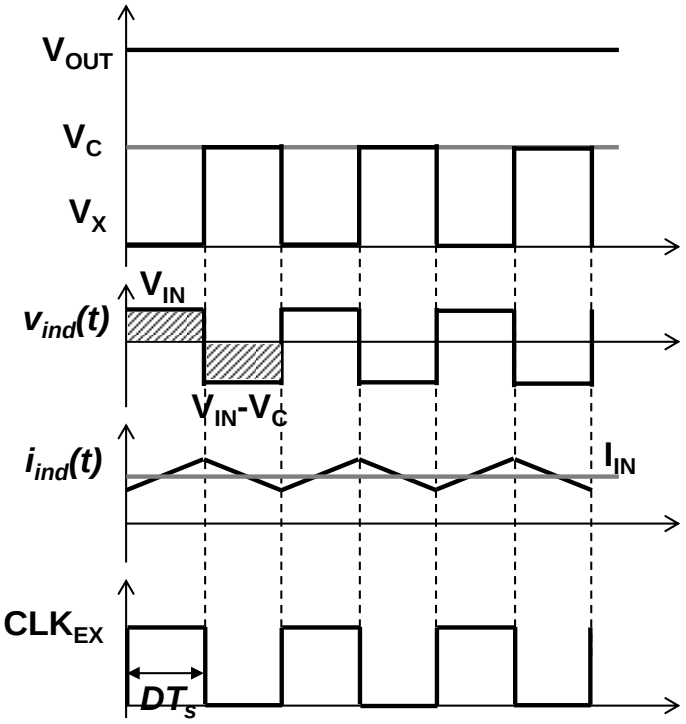


Figure 4-3. Representative waveforms for the hybrid SI/SC converter.

4.2.2 SI-Flyback Converter

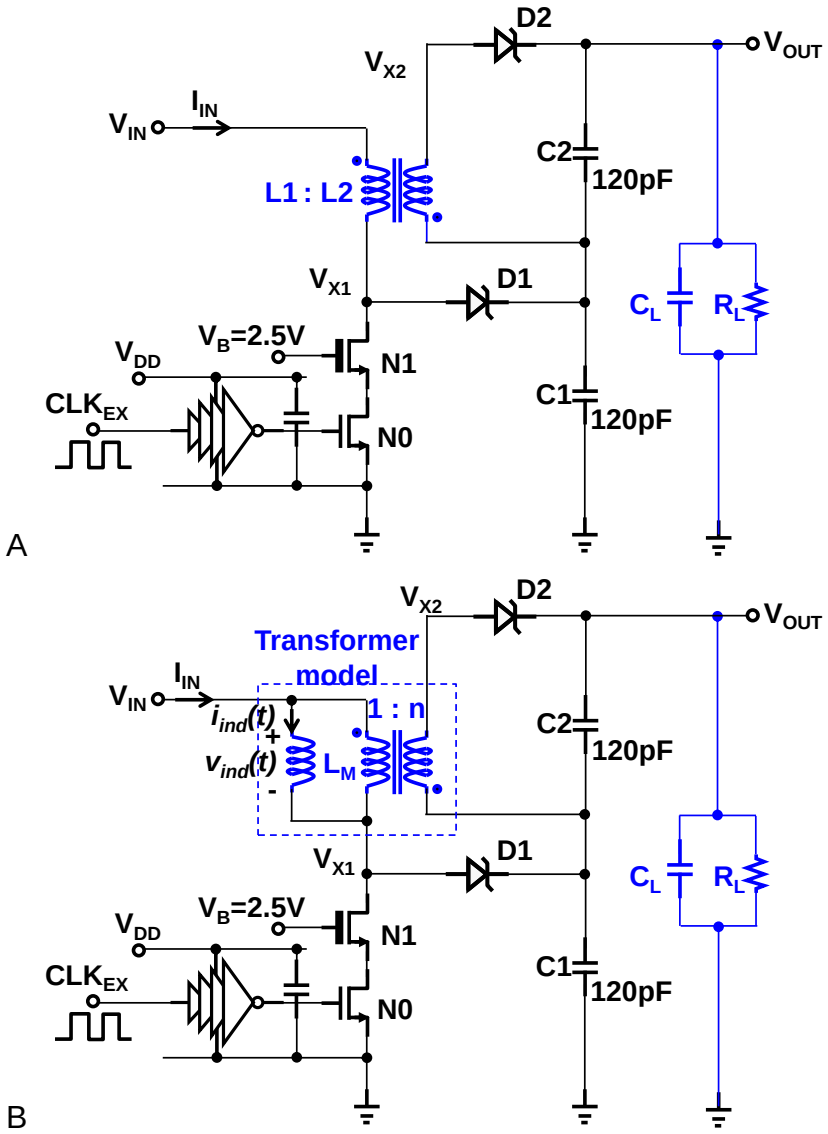


Figure 4-4. Schematic of a hybrid SI/flyback converter implemented in 130nm CMOS. A) Real Schematic, B) Schematic with transformer model for analysis.

Figure 4-4 shows the schematic of a hybrid SI/flyback converter that has been designed and fabricated in a 130nm CMOS process. A transformer (L1:L2) is utilized and its model with magnetizing inductance of L_M=L_1 and turns ratio of n is represented in Figure 4-4b. This hybrid topology can be viewed as stacking a flyback converter on a SI boost, thus realizing high conversion ratio with reduced voltage stress when comparing to flyback and SI boost. Figure 4-5 illustrates representative waveforms of

the SI/flyback converter in steady state. In subinterval I, the synchronous switch turns on by the external clock CLK_{EX}, and V_{X1} is connected to ground. The voltage $v_{ind}(t)$ across the primary inductor is V_{IN}, which is amplified by the transformer and causes V_{X2} to be equal to V_{C1}-nV_{IN}. Here we assume voltages over capacitors C1 and C2 are steady and annotated as V_{C1} and V_{C2}. Both diode D1 and D2 are reverse biased, and energy is stored in the magnetizing inductance L_M. In subinterval II, the synchronous switch turns off, the magnetizing inductance L_M starts charging V_{X1} and V_{X2} up and turns on diode D1 and D2. Voltage V_{X1} and V_{X2} in this subinterval are then derived as

$$V_{X1} = V_{C1} \tag{4-2a}$$

$$V_{X2} = (n+1)V_{C1} - V_{IN} = V_{C1} + V_{C2} = V_{OUT} \tag{4-2b}$$

Voltage $v_{ind}(t)$ in this subinterval becomes negative as V_{IN}-V_{C1}, as shown in Figure 4-5. From inductor volt-second balance, we can get:

$$V_{C1} = \frac{V_{IN}}{1-D} \tag{4-3a}$$

$$V_{C2} = \frac{nDV_{IN}}{1-D} \tag{4-3b}$$

$$V_{OUT} = \frac{1+nD}{1-D}V_{IN} \tag{4-3c}$$

Blocking voltages for the stacked NMOS switch (N1, N0) and diode D1 are calculated as V_{C1}, while voltage stress for the diode D2 is bigger as V_{C2}+nV_{IN}. Comparing to flyback and SI boost, maximum voltage stress is reduced. Both D1 and D2 are implemented using n-type SBDs. Since larger voltage stress is seen over D2, guard rings are used for D2 to reduce its leakage. C1 and C2 are implemented using onchip MIM capacitors as 120pF respectively.

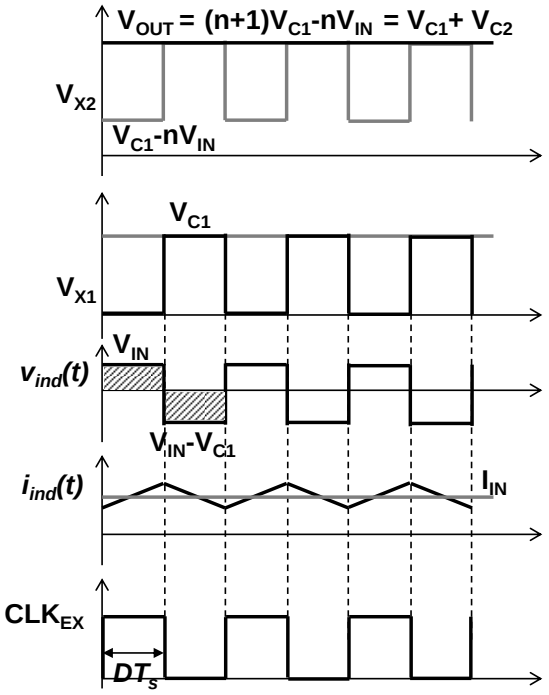


Figure 4-5. Representative waveforms for the hybrid SI/flyback converter.

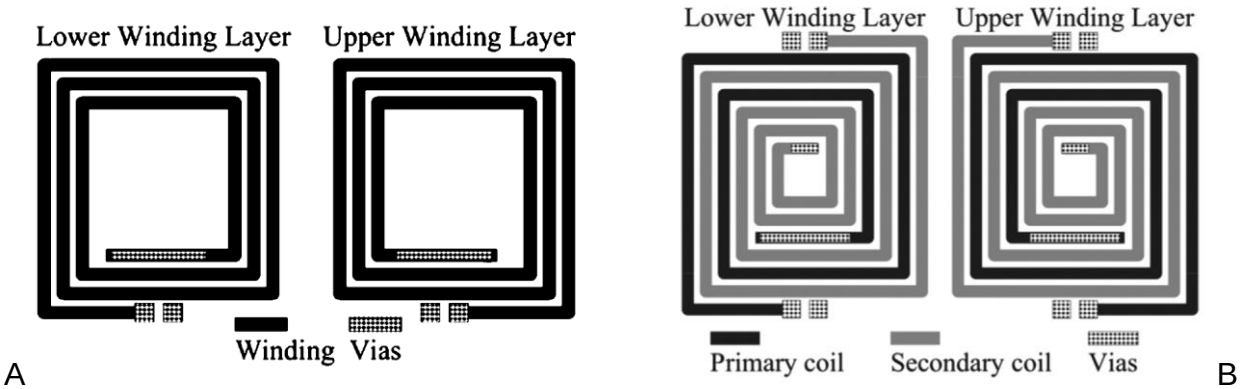
4.3 Microfabricated Air-Core Power Magnetics

Integration of power magnetics is generally more difficult than other components in switched-mode power converters due to their large physical area and low quality factor. A 2nH onchip spiral inductor with diameter of 600μm and quality factor of 4.6 at 170MHz has been demonstrated for a buck converter [55]. High-performance discrete inductors and transformers are more commonly used in tradition, however their bulky footprints are not suitable for applications such as flying microrobots where high power density is critical. How to improve power density and how to decrease the footprint of passives are becoming more and more important.

A microfabrcation process aimed for implementing air-core inductors and transformers with high inductance density and moderate quality factors in the range of 10MHz-1GHz was developed [56]. This process utilizes three-dimensional molding of thick copper traces for low resistance and high mutual coupling, and manipulates

photolithographic techniques to use photoresist as an insulating structural support element. This microfabrication process enables system-in-package integration with silicon electronics, e.g., via wire bonding or flip chip attachment.

4.3.1 Layout Design



A B

Figure 4-6. General layout of fabricated inductors and transformers. A) Inductors, B) Transformers.

Figure 4-6 shows general layout design for fabricated air-core inductors and transformers. Square spiral layout and layer stacking were chosen for inductance density maximization and quadratic gains through mutual coupling [57][58]. As shown in Figure 4-6a, inductor layout consists of upper and lower planar spiral winding layers stacked on top of each other with vias for electrical connection between the windings. The copper windings of designed inductors are nominally 50µm in width and 10µm in height and have a lateral separation of 10µm. Transformer layout design follows that of inductors as illustrated in Figure 4-6b. The two outermost windings of the primary and secondary spirals are laterally interleaved on each layer in a bifilar manner, and the secondary spiral additionally contains nine inner nested turns on each layer for voltage gain. Outer dimension of designed transformer is 1.5mm X 1.5mm, and the copper traces are nominally 30µm in width, 10µm in height, and 10µm in lateral separation. These two design masks have been used in microfabrications.

4.3.2 Process Flow

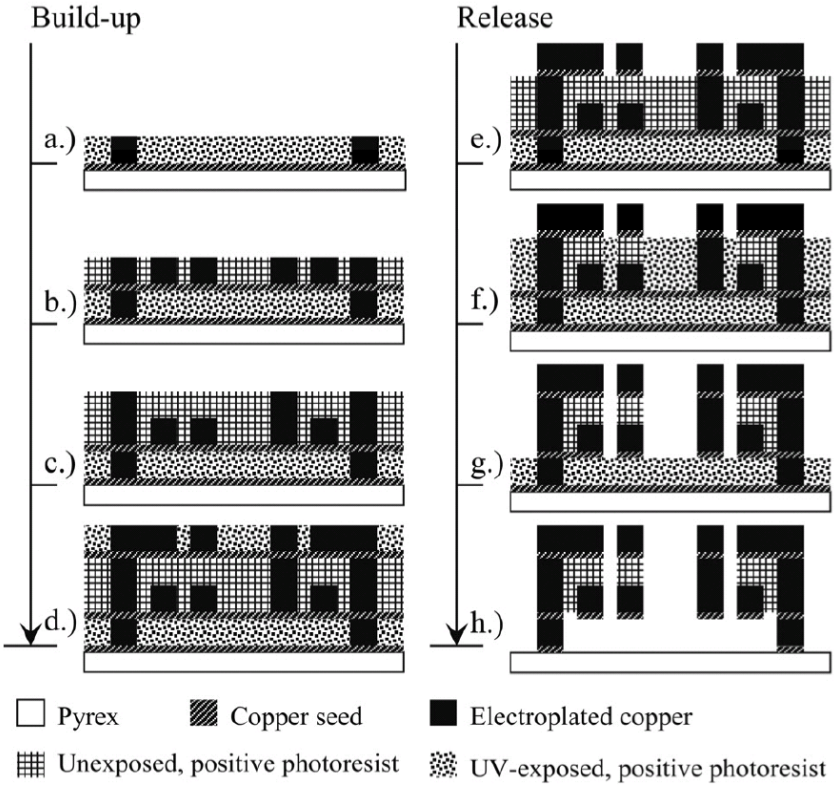


Figure 4-7. Cross-sectional view of the microfabrication process flow.

The microfabrication process, as illustrated in Figure 4-7, consists of two main steps: 1) the build-up of a four-layer stack copper electroplated within photoresist molds, followed by 2) removal of the molds to release the devices. Copper seed layers were each deposited 200-nm-thick and served as the conductive starting surface onto which thicker copper layers would be electroplated. Positive-tone photoresist was patterned on top of the seed layer to form the plating mold. These photoresist molds were each spun to a thickness of 10 µm per layer. After all layers of copper were electroplated, the final multilayer structure was released in photoresist developer. The function of the developer was to selectively etch certain exposed regions of photoresist while leaving unexposed regions in the structure as structural elements separating the upper and lower copper windings.

4.4 Current Mode PWM Controller

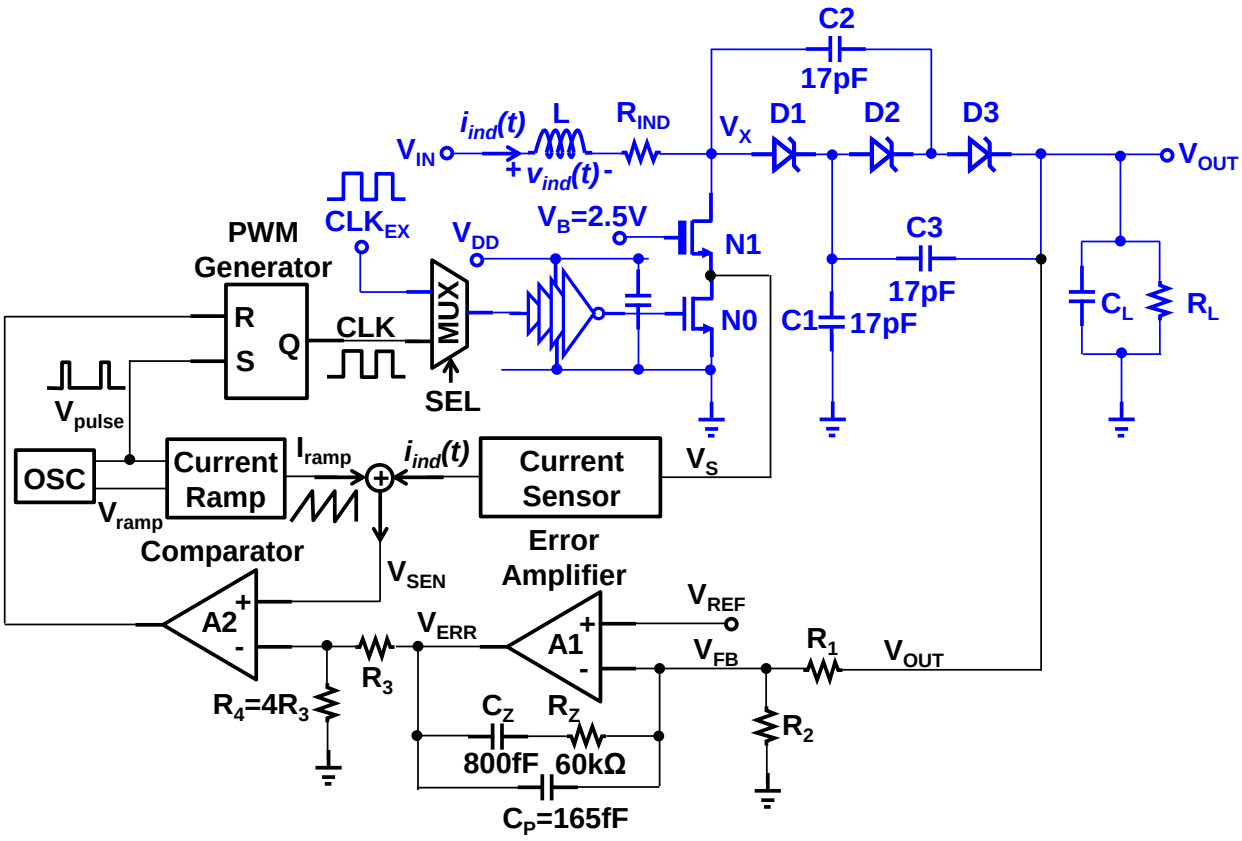


Figure 4-8. A current mode PWM controller for the hybrid SI/SC converter.

Figure 4-8 illustrates the block diagram of the current mode PWM controller designed for the hybrid SI/SC converter. The current-mode PWM has two feedback loops: a voltage feedback loop to regulate the output voltage V_{OUT}, and a current feedback loop to regulate the inductor current $i_{ind}(t)$. In this current mode PWM, the inductor current modulates the control signal CLK directly through comparator A2 for a faster transient response compared to the conventional voltage mode PWM [59].

4.4.1 Voltage Feedback Loop

The voltage feedback loop, which is composed of resistive divider R_1-R_2, compensator (A1), modulator (A2), and RS latch, is stabilized using the classical type-II compensation network (i.e. C_P, C_Z, R_Z) with voltage error amplifier shown in Figure 4-9.

The transfer function for the compensated error amplifier can be approximated as [60][61]:

$$A(s) = \frac{1 + \frac{s}{\omega_{ZC}}}{(C_Z + C_P)(R_1 \parallel R_2) \cdot s \cdot \left(1 + \frac{s}{\omega_{PC}}\right)} \tag{4-4}$$

The compensated amplifier introduces a pole at dc for high dc gain and a single pole-zero pair with the zero and non-origin pole given by $\omega_{ZC}=1/R_ZC_Z$ and $\omega_{PC}=1/(R_Z(C_Z//C_P))$, respectively. The pole-zero pair provides a constant gain and a reduced phase lag between the zero frequency ω_{ZC} and the pole frequency ω_{PC}. The loop gain of the hybrid SI/SC converter in DCM operation can be approximated as [62][63]:

$$T(s) = A(s) \cdot \beta \frac{2V_{OUT}}{V_{PP_RAMP}(2M-1)} \sqrt{\frac{R_L T_S}{2L} \frac{M-1}{M}} \frac{1}{1 + \frac{s}{\omega_{P1}}} \tag{4-5}$$

where $\beta=R_2/(R_1+R_2)$, V_{PP_RAMP} is the amplitude of the voltage ramp, $M=V_{OUT}/V_{IN}$ is the voltage conversion ratio, and R_L is the output load resistance. ω_{P1} is the pole introduced the boost converter operated in DCM, which can be written as $\omega_{P1}=1/(R_LC_L(M-1)/(2M-1))$, where C_L is the load capacitance. To ensure stability, the zero ω_{ZC} is placed near the lowest frequency pole ω_{P1}, which corresponds to the lightest load or when R_L is largest [63].

The error amplifier A1 consists of a two-stage design, as shown in Figure 4-9. The input stage combines two folded-cascode amplifiers with NMOS and PMOS differential input for rail-to-rail input common-mode range, and is followed by an active loaded differential pair for a total gain of ~50dB and 3dB bandwidth of ~21MHz. A R_3-R_4 voltage

divider (see Figure 4-8) is inserted at the output of A1 to limit the maximum value of V_{ERR} to ~ $0.8V_{DD}$. This ensures that V_{SEN} crosses V_{ERR} when the hybrid SI/SC converter turns on for proper system start-up. The modulator/comparator A2 was designed for higher gain and bandwidth of ~55dB and ~100MHz, respectively, to process V_{SEN} from the current sensor. It employs the same input structure as A1 with additional gain provided by two differential amplification stages and an output buffer inverter.

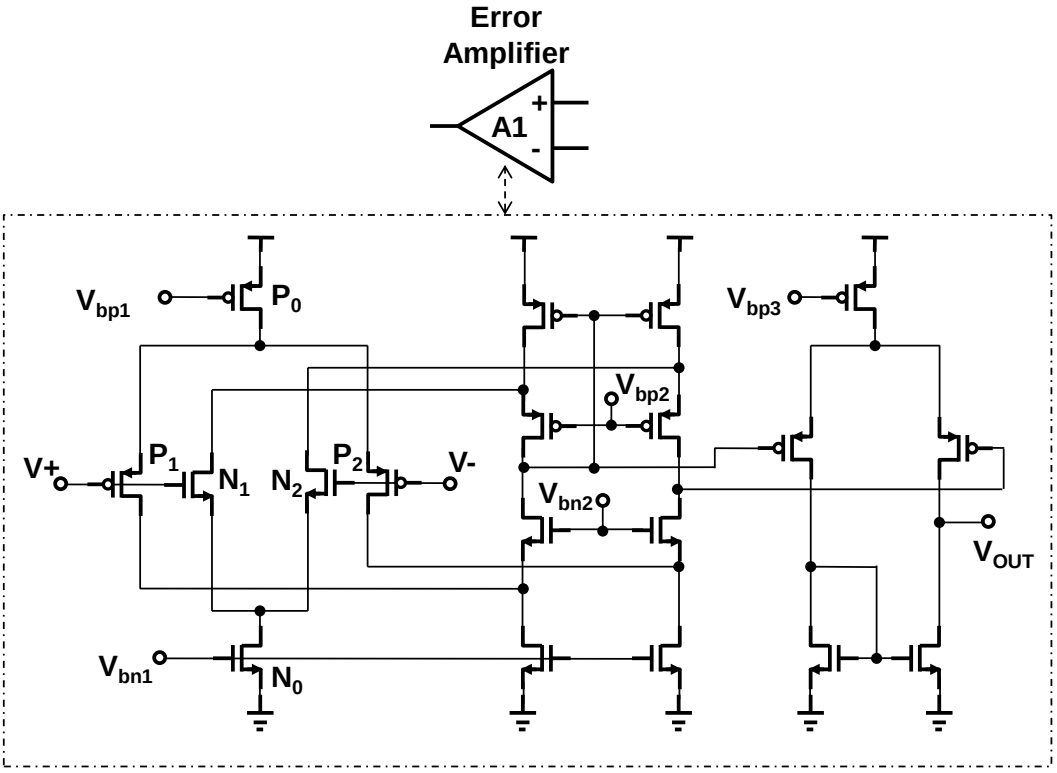


Figure 4-9. Schematic of the error amplifier in the current mode controller.

4.4.2 Current Feedback Loop

The current-mode feedback loop is composed of a current-sensor, ramp generator, modulator A2 and RS latch. This current feedback loop is open loop unstable for duty cycles greater than 50% (D>0.5), regardless of the state of the voltage feedback loop - a well-known problem with the current-mode PWM [24]. Figure 4-10 illustrates the inductor current $i_{ind}(t)$ controlled by the error voltage V_{ERR} to detect the

peak current and set the duty cycle D. An initial perturbation in the duty cycle ΔD_0 will decrease over time when D<0.5 (Figure 4-10a) and increase when D>0.5 (Figure 4-10b). This duty cycle instability in the current loop causes sub-harmonic oscillations of the converter, as shown in Figure 4-10c. In this case, the inductor current error affects the output voltage and the error voltage via the voltage feedback. As a result, the error voltage V_{ERR} oscillates at one-half the switching frequency, showing a duty cycle variation ΔD in consecutive pulses. To avoid this sub-harmonic problem, a linear ramp signal with slope $m_c>0.5m_2$ can be applied to the error voltage to force the duty cycle error to decrease over time, as shown in Figure 4-10d. This slope compensation may either be added to the current waveform or subtracted from the error voltage [64]. In this design, the linear slope compensation signal is generated by an on-chip oscillator (OSC) and ramp generator, and added to the sensed inductor current output of the current sensor. By adding the slope compensation, inductor current ripple and output voltage ripple will become much cleaner to avoid noise coupling and performance degradation to other circuits.

The current sensor operates by sensing the power switch N0 drain current (see Figure 4-8) to emulate the rising slope of the inductor current [65]. As shown in Figure 4-11, N_0 is the 1.2V thin-gate power switch, while N_2 is a sensing transistor whose size is K_N times smaller than that of N_0. When the control signal CLK turns on the switch N_0, N_2 and N_3 simultaneously due to the balanced signal path design, the switches N_4 and N_5 are turned off. Since the current I_{MIN} is very small, the drain voltage of N_3 can be neglected, letting the drain voltage of N_0 (V_S) almost equal to V-. The drain voltage of the sensing transistor N_2 (V+) also equals to V- due to the high gain comparator A0.

Therefore, with the same drain voltages, N_2's drain-current is K_N times smaller than N_0's drain current I_{N0} and equal to i_{ind}/K_N. This emulated inductor current is then reproduced by the P_0-P_1 current mirror with a factor K_P and generates a sense voltage $V_{SEN}=R_{SEN}I_{SEN}=R_{SEN}i_{ind}K_P/K_N$. During the OFF period of CLK, N_2 and N_3 are turned off to disconnect the current sensing circuit from the power switch. Switches N_4 and N_5 are turned on, supplying P_0's drain current with I_{MIN}, thereby setting the sensing voltage as $V_{SEN}=R_{SEN}I_{MIN}K_P$. Moreover, since both input nodes of A0 have low impedance due to the low on-resistances of switches N_2-N_5, there is only one high-impedance node at the output of A0. Stability is therefore easily achieved using slightly large sizes for P_0 and P_1 to provide dominant-pole compensation.

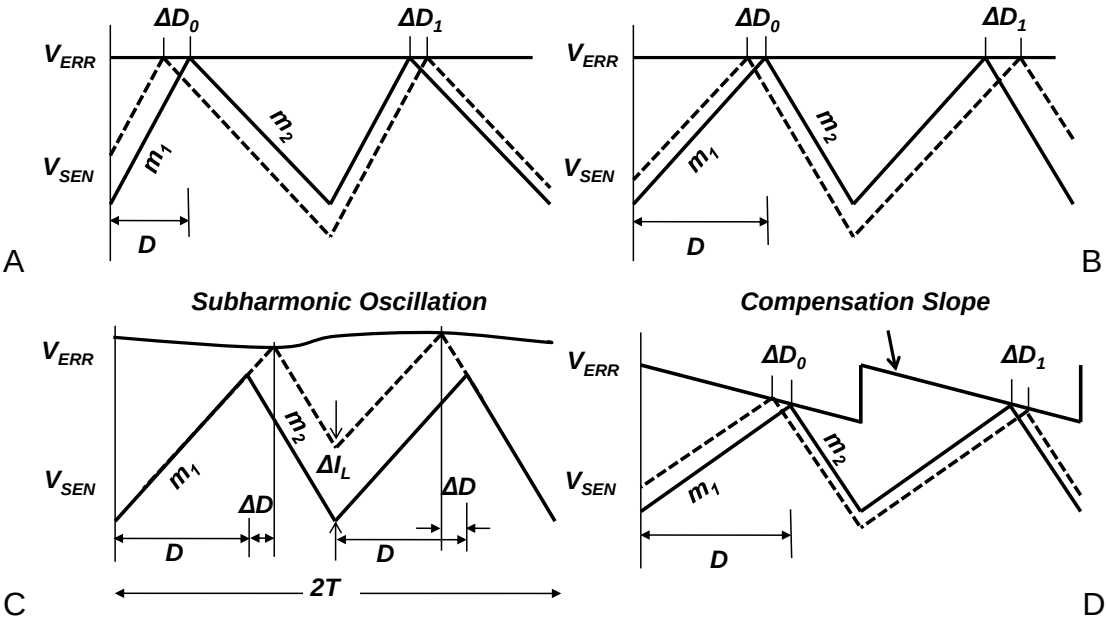


Figure 4-10. Demonstration of loop instability in a current mode controller. A) D>0.5, B) D<0.5, C) Subharmonic oscillation, D) D>0.5 with slope compensation.

An RC oscillator based on [65]is modified for digital control and high frequency operation to generate a trigger signal (V_{pulse}) and compensation slope (I_{RAMP}), as shown in Figure 4-12. A digitally programmable current source generates V_{RAMP} on the

capacitor C_F. When V_{RAMP} reaches a threshold set by the R_H-R_L divider, A1 outputs a short pulse to reset V_{RAMP} to ground with switch N_1. An inverter chain is inserted before N_1 to set the desired pulse width of ~500ps, and N_2 adds a hysteresis to the comparator A1 for stable operation. The frequency of the short pulses V_{pulse} (i.e. the frequency of the switching converter) is designed to range from 40MHz to 200MHz, and controlled by F[1:5] to vary the rising slope of V_{RAMP}. A current ramp generator translates V_{RAMP} in OSC to I_{RAMP}, which provides slope compensation to V_{SEN}, the output from the current sensing circuit. A voltage follower comprised of A2, P_2 and R_A recreates the ramp voltage on R_A, thus P_2's current is V_{RAMP}/R_{SEN} by setting R_A=R_{SEN}. P_1 and N_3 are used for fast discharge of the ramp signal to enable high frequency operation. The resulting current is copied via a programmable current mirror S[1:4] to generate and control the slope of I_{RAMP}, which is added to I_{SEN} for slope compensation.

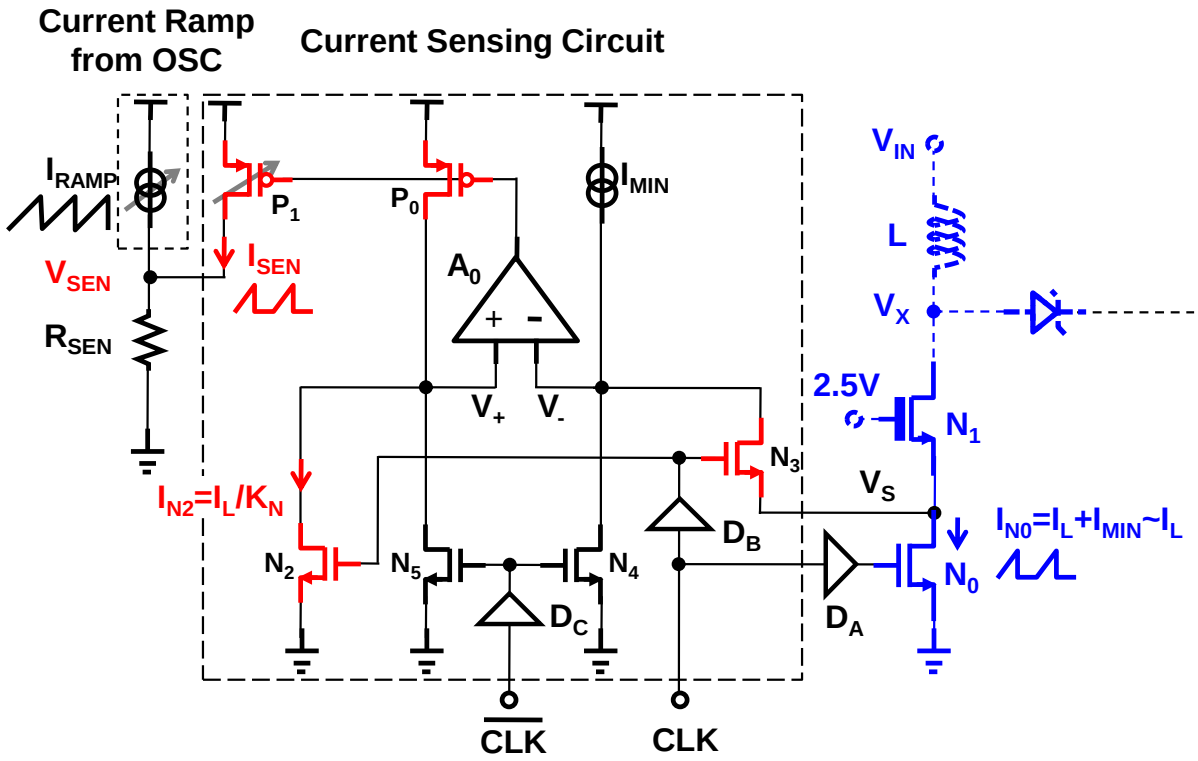


Figure 4-11. Schematic of the current sensing circuit.

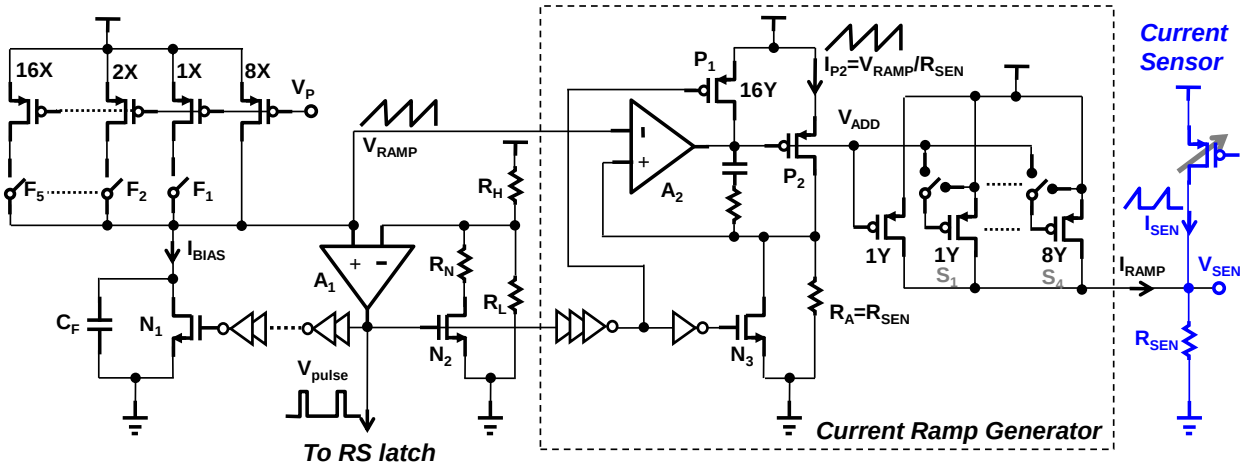
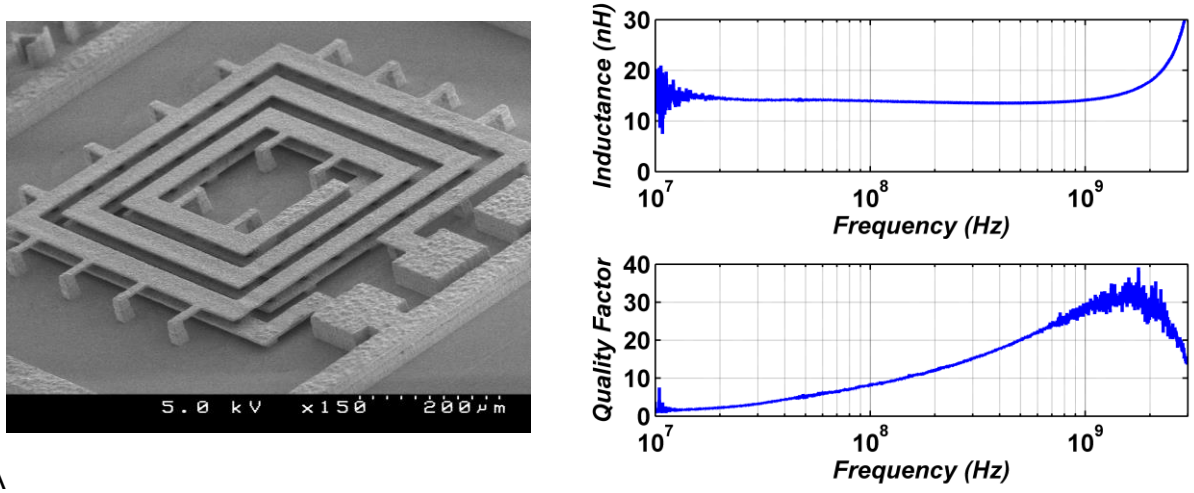


Figure 4-12. Schematic of the oscillator (OSC) and current ramp generator.

4.5 Experimental Results

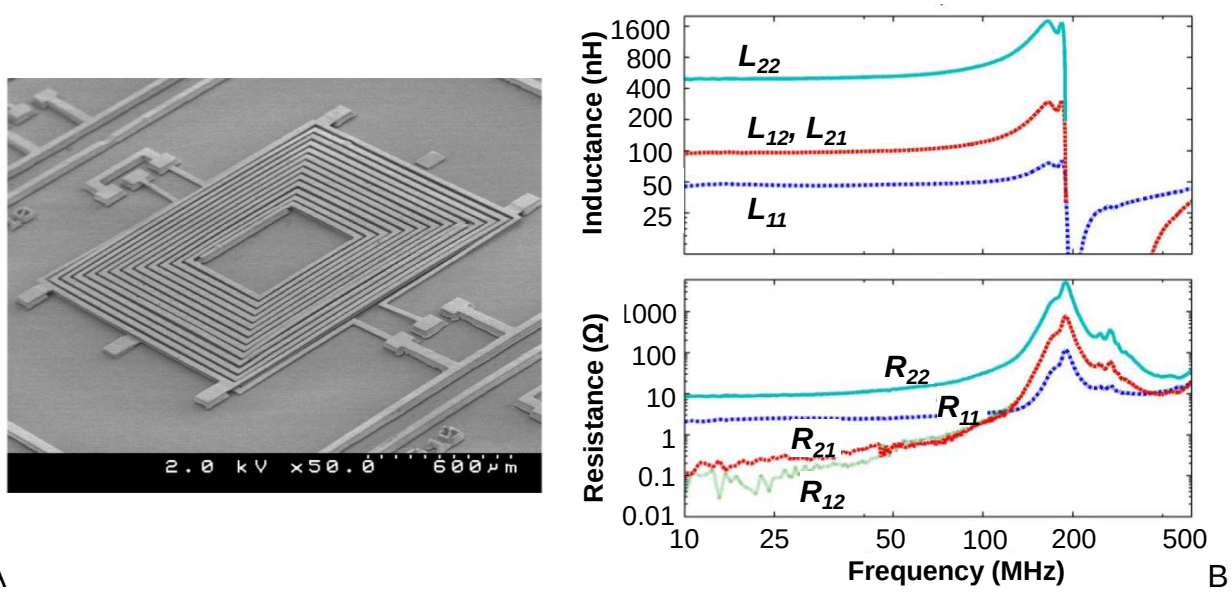
4.5.1 Microfabricated Air-Core Inductor and Transformer

Figure 4-13a shows a SEM image of a microfabricated fully-released inductor [56]. Its dc resistance was measured with four-point probes using an HP 3478A multimeter, and ac behavior was characterized using an Agilent E8361A network analyzer. Measured scattering parameters were then transformed to complex impedance parameters from which inductance and quality factor were obtained over a wide range of frequencies.



A B

Figure 4-13. Microfabricated inductor and measured characteristics. A) SEM perspective image, B) Measured inductance and quality factor [56].



A B

Figure 4-14. Microfabricated transformer and measured characteristics. A) SEM perspective image, B) Measured inductance and resistance values of each element.

The microfabricated inductor had a measured dc resistance of 0.8 Ω and a maximum current capacity of ~450 mA. Figure 4-13b shows its measured ac characterization. Measured ac inductance value was ~14nH from 10 MHz – 1 GHz and peak quality factor was >30 at around 1.5 GHz. At a frequency of 100 MHz (the tested switching frequency of the converter), the quality factor of the inductor was 8. The area of the inductor measured to be 0.5 mm × 0.5 mm, which corresponded to an inductance density of 56 nH/mm^2.

Figure 4-14a shows a SEM image of a microfabricated transformer [56]. Inductance and resistance were extracted from each element of the impedance matrix and plotted in Figure 4-14b. At frequencies much lower than the resonant frequency, the plots show L_{11}=46 nH for the primary, L_{22}=500 nH for the secondary, and L_{21}=L_{12}=96 nH for the mutual inductance—equivalently expressed as a coupling coefficient of 0.63. The equivalent turns ratio, expressed as SQRT(L_{22}/L_{11}), was calculated at 3.3 and indicated

the nominal voltage gain of the transformer. Operating frequency of these two microfabricated devices were designed between 10-100MHz.

4.5.2 Hybrid SI-SC Converter

4.5.2.1 Open loop measurement results

External driving clocks with variable frequency and duty cycle were employed in open loop measurements for the hybrid SI/SC converter. Time domain waveforms when using a 24nH air-core inductor from coilcraft and switching at 100MHz are illustrated in Figure 4-15 for 7V and 10V output respectively.

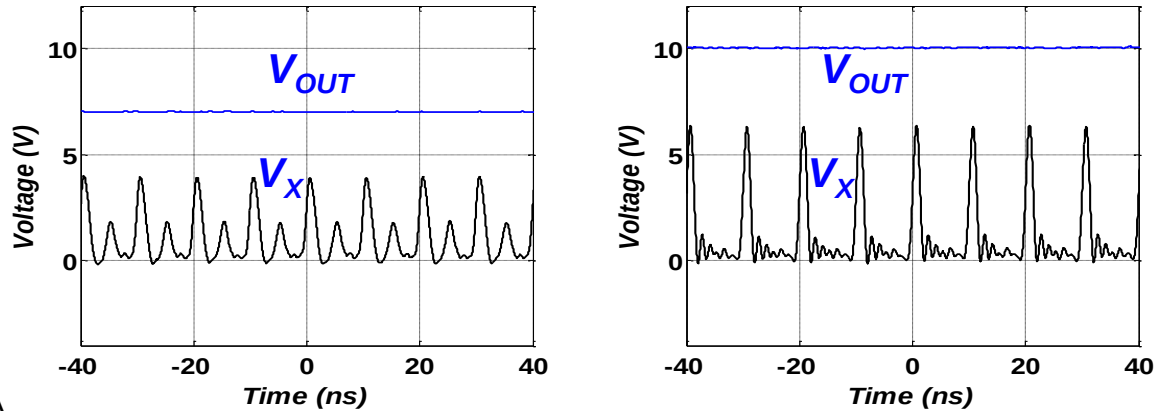


Figure 4-15. Measured waveforms of the hybrid SI/SC converter at 100MHz. A) 7V output and 0.96mA load when D= 37.3%, B) 10V output and 0.58mA load when D=83%.

As shown in Figure 4-15a, the V_X waveform is not an ideal square-wave but a relatively complex waveform with ringing in between which means the converter was operating in DCM. First, when the clock voltage is small enough such that the stacked switch turns off, the inductor voltage spikes, activating D1 and transferring charge to the SC stage. The inductor current, and thus diode current, immediately and sharply falls, depleting the stored energy in the inductor (for DCM operation) and causing the diode to turn off, leaving the V_X node floating. During this time, V_X behaves similarly to an RLC circuit and rings from ~0V up to nearly half the peak voltage, limited by dampening

through various leakage paths and series resistance. The output voltage is ~7V. For Figure 4-15b the hybrid SI/SC operates in continuous conduction mode (CCM) and the output is ~10V. The peak voltage of V_X is proportionally higher and the large amplitude ringing is no longer present since the inductor current is continuous and either the diode or the stacked NMOS switch is always active. A smaller amplitude and higher frequency ringing behavior still occurs, possibly due to parasitic inductance of devices, package, and PCB traces.

Figure 4-16 shows the corresponding measured efficiencies for 7V and 10V outputs and 50MHz and 100MHz switching frequencies. The hybrid SI/SC converter exhibits a higher efficiency at 100MHz for both 7V and 10V output voltages. This behavior indicates that the SC stage operates in the slow switching limit and would therefore benefit from larger pump capacitors to increase overall efficiency [66]. Peak efficiency for this converter is 42% at 1.9mA of load current for a 7V output, and 17.5% at 2.4mA for a 10V output.

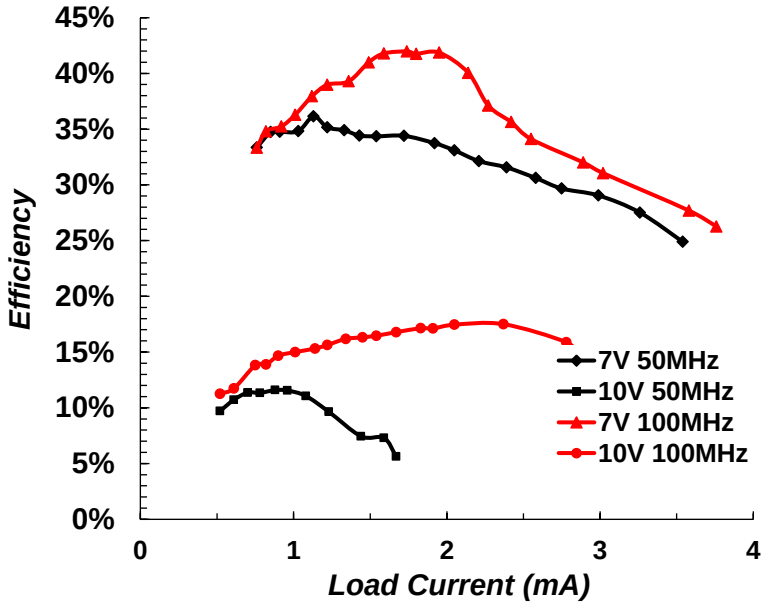
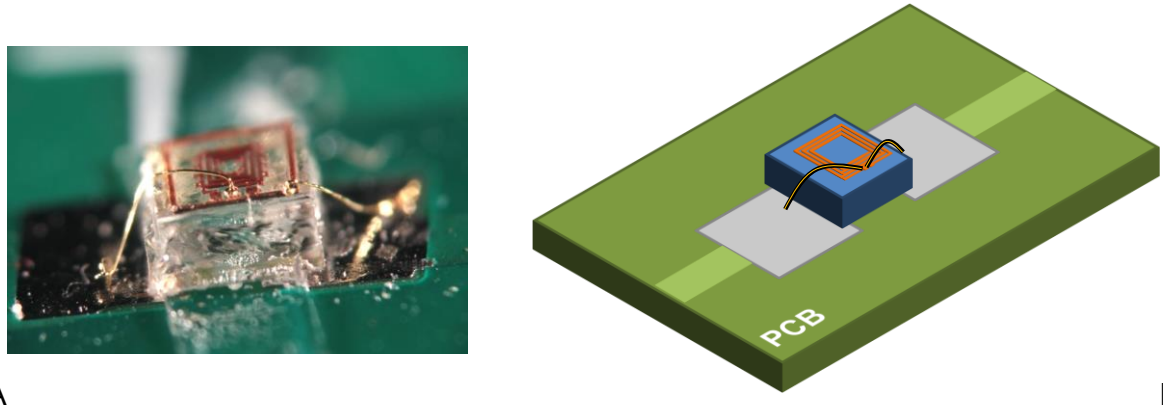


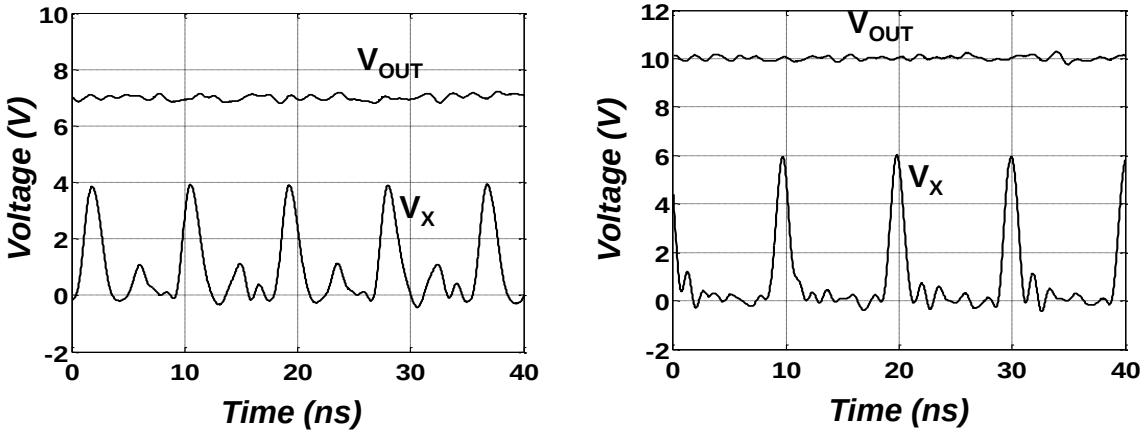
Figure 4-16. Measured efficiencies with external driving clocks and a 24nH commercial inductor.

4.5.2.2 Close loop measurement results



A B

Figure 4-17. Wire bonding for the 14nH microfabricated inductor on a custom PCB for the hybrid SI/SC converter. A) Real photograph, B) Envisioned PCB connection.



A B

Figure 4-18. Measured time-domain waveforms of the output voltage and switching node voltage V_X when measured with the microfabricated inductor at ~100MHz. A) V_{OUT}=7V, B) V_{OUT}=10V.

The microfabricated inductor was packaged and assembled using wire bonding on a custom printed circuit board for testing within the current-mode PWM controlled hybrid boost converter circuit. Figure 4-17 shows the pictures of the packaged inductor with bonding wires. Envisioned PCB connection of the microfabricated inductor is also shown in Figure 4-17b for better illustration. The bonding wires introduce extra inductance, which causes measured total inductance 25nH after wire bonding. Figure 4-18 shows measured time-domain output voltage (V_{OUT}) and switching node voltage (V_X)

waveforms for 7V and 10V output, respectively. A high impedance probe was utilized to measure voltage V_X in order to minimize any noise or extra load brought in by the probe. For 7V output, the converter operates in discontinuous conduction mode (DCM) since voltage ringing is seen. The switching frequency is ~115MHz. Similar waveforms are obtained for 10V output except the converter operates in continuous conduction mode (CCM) and the switching frequency is ~100MHz.

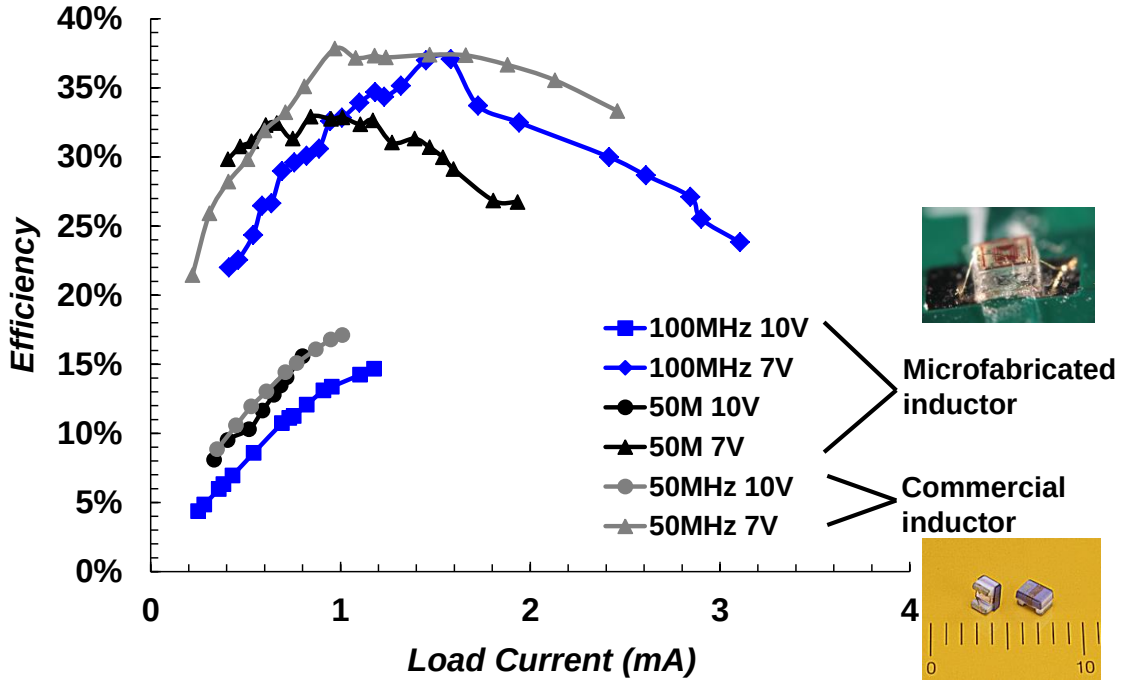


Figure 4-19. Measured efficiencies for the close-loop hybrid SI/SC converter with microfabricated and commercial inductor respectively.

Figure 4-19 shows the measured power efficiency versus load current for the hybrid SI/SC converter with the microfabricated inductor (25nH after wire bonding) and a commercial inductor (43nH). With the microfabricated inductor, the hybrid converter delivers a maximum load current of ~3 mA and a peak efficiency of 37% at 1.6 mA for 7 V output, while for 10 V output, the converter can only deliver a maximum current of ~1

mA and a peak efficiency of 15%. The lower maximum current at 10 V is a consequence of the duty cycle reaching its extreme boundaries at lower current for higher voltage. Comparing to the commercial inductor, the microfabricated inductor achieves comparable efficiencies while having a much smaller footprint.

Figure 4-20 shows the transient response for a 50% load step. In all cases the worst-case voltage variation caused by current step is less than 7%.

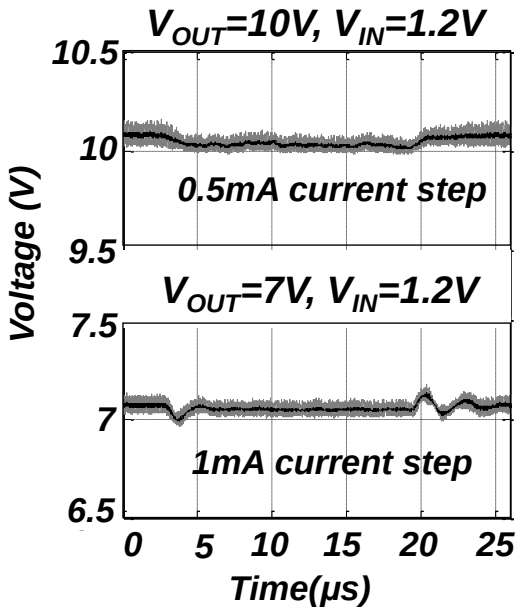


Figure 4-20. Transient response for the SI/SC converter using a commercial 43nH inductor.

4.5.3 Hybrid SI-Flyback Converter

The hybrid SI/flyback converter was tested with a commercial transformer (25nH/200nH) and the microfabricated transformer (47nH/496nH shown in Figure 4-14) separately. Primary and secondary DC resistances of the commercial and microfabricated transformer are measured as 0.12Ω/0.31Ω and 2.9Ω/10.18Ω respectively. External driving clocks were used. Figure 4-21 shows time-domain waveforms of the SI/Flyback converter using the commercial transformer with 7V and

10V outputs. Ringing at the switching node V_X is observed from Figure 4-21b, which means the SI/Flyback converter operates in DCM for 10V output and 0.58mA load.

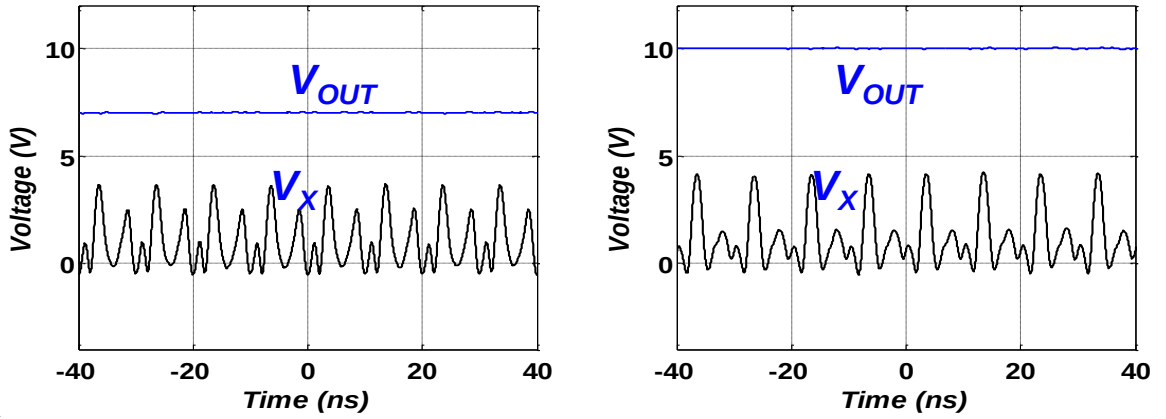


Figure 4-21. Measured waveforms of the SI/flyback converter using a commercial transformer. A) 7V output and 0.97mA load when D=43.5%, B) 10V output and 0.58mA load when D=61%.

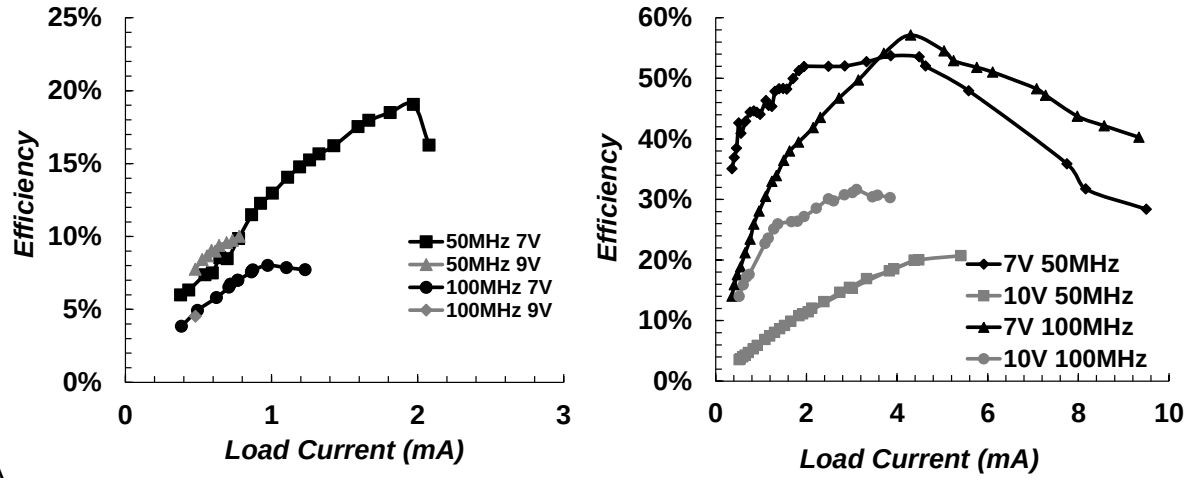


Figure 4-22. Measured efficiencies using external driving clocks for the hybrid SI/flyback converter. A) Tested with the microfabricated transformer, B) Tested with a commercial transformer.

The efficiency of the SI/flyback converter configured with the microfabricated and commercial transformer is shown in Figure 4-22. With the microfabricated transformer, a peak efficiency of 20% is achieved for a 7V output and a 1.9mA load at 50MHz. The maximum output voltage is 9V for both 50MHz and 100MHz switching frequencies. When the converter is tested with the commercial transformer, at 100MHz, peak

efficiency of 57% is achieved for a 4.3mA load current and 7V output, whereas a 32% peak efficiency at 4.3mA load current is seen for an output of 10V. The microfabricated transformer has much higher DC resistances, causing lower efficiencies at shown in Figure 4-22.

4.6 Die Photo and Performance Summary

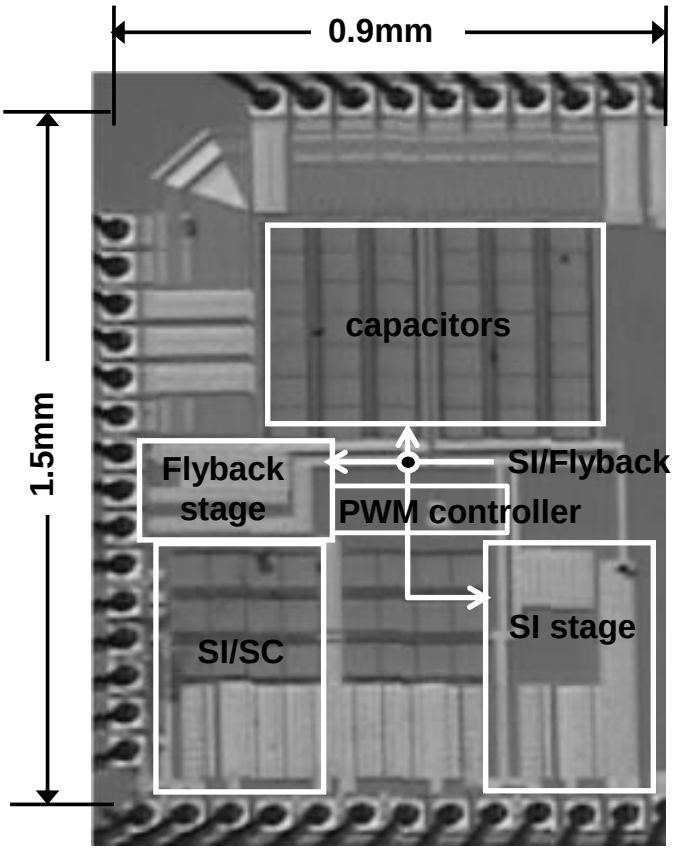


Figure 4-23. Die photo of the hybrid SI/SC and SI/flyback converter in a 130nm CMOS process.

Figure 4-23 shows the chip micrograph fabricated in UMC 130nm CMOS process. The area of the SI/SC converter is 0.2mm^2, while that of SI/flyback is 2.25mm^2 including onchip 240pF decoupling capacitors. Table 4-1 illustrates performance summary of the hybrid SI/SC and SI/flyback converter with the microfabricated and commercial inductor / transformer. Compared to the fully integrated boost converter in [67], the hybrid SI/SC and SI/flyback converter achieve larger voltage conversion ratio of ~9 and higher

efficiency of 37% and 57% for 7V output respectively. When microfabricated inductors and transformers are employed, the hybrid SI-SC converter achieves a larger output voltage and a better power efficiency, which the hybrid SI-flyback has a worse efficiency due to the large resistance of the transformer. In terms of power density, the hybrid SI-SC converter with the microfabricated inductor is the best and its power density is 47mW/mm2, which accounts for both the area of the converter and the microfabricated inductor. More up-to-date converters are shown in Table 4-2 for performance comparison with our hybrid SI-SC converter. Though the SI boost converter in [68] achieves the same output voltage, ~10V, with a very good power efficiency of ~81%, it uses a discrete diode and a very large decoupling capacitor.

Table 4-1. Performance summary and comparison for implemented SI-SC and SI-flyback converter

Topology	SI-SC		SI-Flyback		[67]
Technology	130nm		130nm		180nm
Rectifier	SBD		SBD		PN junction
Input Range	1.2V		1.2V		1.8V
Converter Area	0.2mm^2		0.4mm^2		2.7mm^2 (w/ coil)
Output Capacitor	4.4nF		240.0pF (onchip)		N/A
Output Range	7V-10V	7V-10V	7V-9V	7V-10V	6V-9V
Coil Area	0.25mm^2	N/A	2.25mm^2	N/A	N/A
Total Area	0.45mm^2	N/A	2.65mm^2	N/A	2.70mm^2
Frequency	50/100MHz	45MHz	50/100MHz	50/100MHz	60MHz
Coils	25nH (w/ bonding wires)	43nH	49nH/496nH (micro-fabricated)	25nH/ 200nH	20nH
Output Ripple	<400mV	<80mV	N/A	N/A	450mV
Max. Power	~21.0mW	17.5mW	14.0mW	63.0mW	N/A
Max. Power Density	47mW/mm^2	N/A	5mW/mm^2	N/A	N/A
Max. Step-Up Ratio	~9.0 @ 10.0mW	~9.0 @ 10.0mW	~7.5 @ 11.0mW	~9.0 @ 56.0mW	5.0 @ 0.8mW
Peak Efficiency	37% @ V_{out}=7V 15% @ V_{out}=10V	37% @ V_{out}=7V 15% @ V_{out}=10V	19% @ V_{out}=7V 10% @ V_{out}=9V	57% @ V_{out}=7V 31% @ V_{out}=10V	28% @ V_{out}=6V

Table 4-2. Performance Summary and Comparison for the hybrid SI-SC converter

	[67]	[68]	[52]	this work
Topology	SI	SI	Dickson	Hybrid SI-SC
Node (nm)	180	180	180	130
Rectifier	PN Junction	Discrete	MOS	SBD
V_{IN} (V)	1.8	3.3	1.8	1.2
V_{OUT} (V)	6~9.0	9.9	6~10.0	4~10.0
Freq. (MHz)	60	1	50-150	25
L (nH)	20	4700	N/A	820
C_O (nF)	N/A	10000.00	0.03	2.20
A (mm2)	1.7	1.4**	N/A	0.2*
Max. V_{OUT}/V_{IN} (@mW)	5@0.8	3@1500.0	5.6@4.0	8.0@6.7
η_{peak} (@mW)	28%@3.6	81%@1500.0	50%@3.5	41%@8.6
P_{out}/A @η_{peak} (mW/mm^2)	0.5	~1000.0*	N/A	43.0
Level of Integration	Full	Offchip L&C	Full	Offchip L&C

* Excluding pad area
** Estimated area

CHAPTER 5
MODELING AND PERFORMANCE ANALYSIS OF HYBRID SI-SC STEP-UP CONVERTERS

5.1 Introduction of Hybrid SI-SC Converter

Autonomous micro-systems [3][69], such as life-sized robotic insects that roll, crawl, jump, or fly require specialized high voltage converters to electrically drive the piezoelectric actuators that transform power into locomotion. These power converters must meet stringent mass and volume requirements, a reality that has led to increased interest in hybrid switched inductor switched capacitor (SI-SC) step-up converters [9][72]. Hybrid SI-SC converters are good at generating large voltage conversion ratio while distributing large voltage stress across many of its constituent devices. Since no high voltage devices are required, hybrid SI-SC converters could be potentially integrated in a low voltage CMOS process. Doing this allows the power module, RF communication subsystem, and digital processor to reside all on a single die, thus enabling extremely small scale and low mass microsystem implementations. The primary challenge then becomes how to analyze and design a high performance hybrid SI-SC step up converter.

Performance analysis and design of a hybrid SI-SC step up converter is usually more complicated than a single SI or SC converter. The main reason is because a hybrid SI-SC converter usually involves many constituent devices including both inductors and capacitors. Moreover, device current in different switching phases (i.e. charging or discharging) might be highly nonlinear, causing conventional analysis methods (i.e. state space averaging) inaccurate and less applicable [14]. Though some hybrid step up converter examples have been presented and analyzed in [72][70][71], most of them focus on ideal switching behavior only and don’t account for important

parasitic resistive and capacitive losses in performance analysis. Thus those results are less accurate and less optimal in real applications. To deal with the difficulties above, section II of this paper firstly presents a generalized hybrid SI-SC converter and then proposes a revised DC circuit model that consists of a DC transformer and several equivalent resistances to represent all important non-ideal losses for accurate performance analysis. More specifically, this paper uses a theoretic network methodology based on charge multiplier vectors, expanding on previous work [66][73][74], to evaluate important model parameters such as the output impedance and to account for various sources of switching loss which are prevalent at high operating frequencies and in on-chip implementations. Unlike previous approaches, ours divides dynamic switching loss into output-unrelated (i.e. gate-drive loss) and output-related (i.e. capacitive loss of diodes) contributions. Accordingly, in addition to the conventional output resistance, two equivalent resistive loads are included in the modified circuit model to separately represent the two forms of dynamic loss. Moreover, device metrics are also incorporated in deriving those important model parameters so that the proposed circuit model is more straightforward and friendly to circuit designers.

The rest of this chapter is organized as follows: Section III employs SPICE simulation to examine the accuracy of the proposed DC circuit model for three specific hybrid converter design examples with N_{SC}=0, 1, and 4 and various design parameters swept. Section IV describes three real hybrid converters that are implemented in a 1.2V CMOS process and shows open loop experimental results of each topology for comparison with their respective model results for further evaluation and verification. Finally, section V offers some concluding remarks and design guidelines.

5.2 Hybrid SI-SC Step-Up DC-DC Converter

5.2.1 Generalized Hybrid SI-SC Converter Topology

Figure 5-1 illustrates a generalized SI-SC step-up converter that is selected in this paper for further performance analysis and circuit modeling. The hybrid converter is composed of a SI stage with an N_{SC}-stage SC ladder multiplier (N_{SC}=0,1,2,…). The SC multiplier could also be implemented using other topologies such as Dickson, serial-parallel, etc. [66]. The SC ladder multiplier is employed over others because large voltage stress is equally distributed across all power devices so that the whole power converter could be implemented in a single low voltage process. In addition, the generalized hybrid converter involves 1 power switch (M), $2N_{SC}$+1 power diodes (D1, D2, …, D($2N_{SC}$)), NSC flying capacitors (C2, C4, …, C($2N_{SC}$)), and N_{SC} holding capacitors (C1, C3, …, C($2N_{SC}$-1)). When N_{SC}=0, the hybrid converter simplifies the same as a SI boost converter.

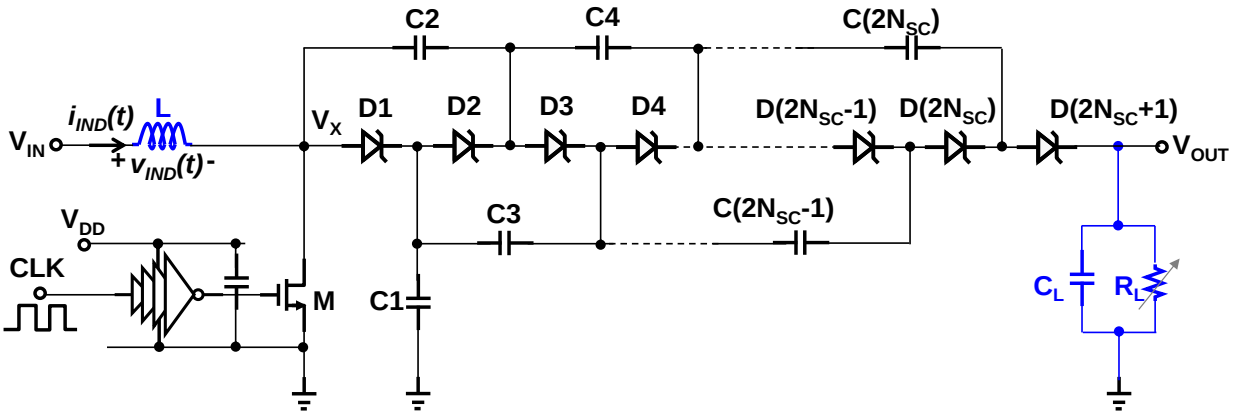


Figure 5-1. Schematic of the generalized hybrid SI-SC step-up converter with an N_{SC}-stage SC ladder.

The generalized hybrid SI-SC converter works as follows: Firstly when the power switch (M) is on, the input power source stores energy in the inductor; then when the switch is off, the inductive energy transfers to the holding capacitor C1. Ideally if C1 is

large enough, a boosted square wave is generated at node V_X with its amplitude determined by the inductor volt-second balance [24]. Then the square wave at node V_X propagates along the SC ladder multiplier in every each switching and places the boosted voltage from the SI stage to all flying and holding capacitors. After reaching steady state, the output voltage of the generalized hybrid SI-SC converter is N_{SC}+1 times larger than a single SI boost. Voltage stress for the power switch and diodes are the same as $V_{OUT}/(N_{SC}+1)$.

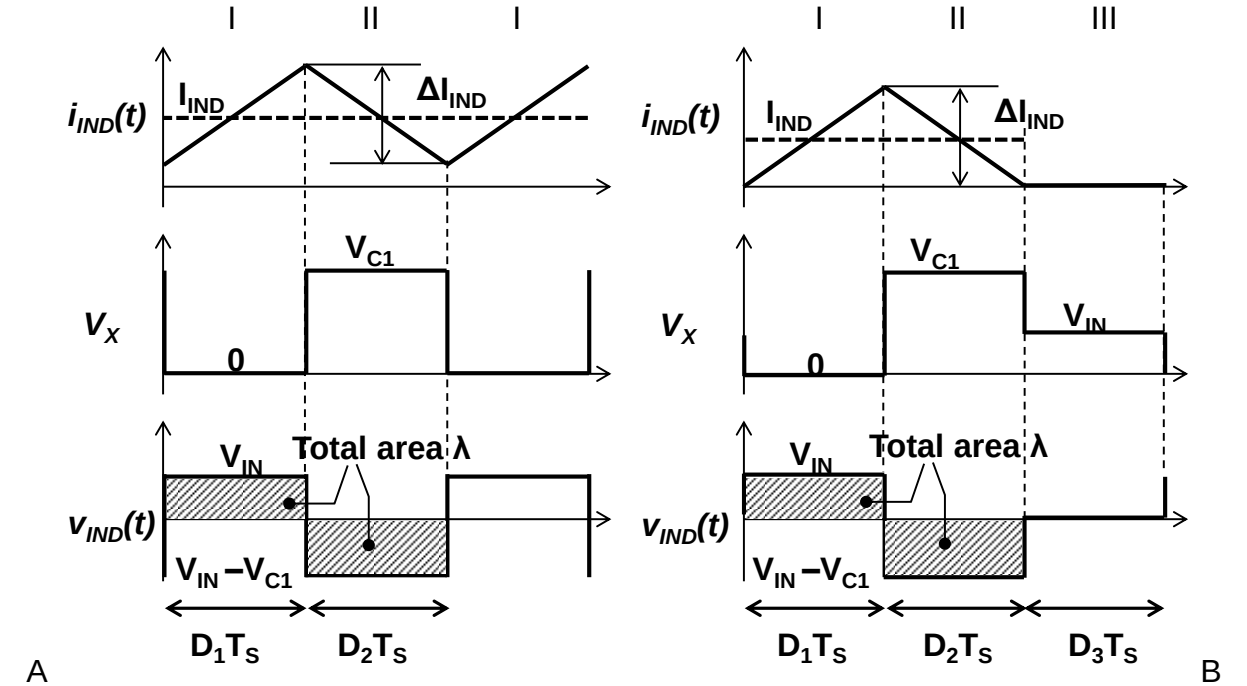


Figure 5-2. Ideal switching voltage and current waveforms in SI stage. A) CCM, B) DCM.

One important thing that needs to be mentioned here is that the SI stage of the hybrid SI-SC converter may work in continuous conduction mode or discontinuous conduction mode, depending on the value of the inductor and resistive load. Figure 5-2 illustrates the difference of switching voltage and current waveforms in these two modes. Here, D_1 is the duty cycle when the switch M is on, and D_2 is the duty cycle when there is a current going through the diode D1. When the hybrid converter works in

DCM, there is an addition subinterval III when the inductor current is always zero, and its duty cycle is represented as D_3 as in Figure 5-2. Conventionally, two sets of equations are utilized to model the performance at these two modes for SI boost. However, analysis shows that during the additional subinterval III, the voltage at switching node V_X drifts to input voltage level and charge stops flowing within the hybrid topology except the decoupling capacitor at the load end. Thus power loss related to this additional subinterval in DCM could be ignored. Therefore we could conclude that considering subintervals I and II only is enough to analyze the hybrid converter regardless of its mode of operation and to determine its performance using a single set of equations. More details will be described in the following section.

5.2.2 Analysis Model

Figure 5-3 illustrates the revised DC circuit model that will be used for performance analysis of the generalized hybrid converter. The model employs a DC transformer (1:N) to represent the ideal DC voltage conversion function [24]. N is the ideal voltage conversion ratio when circuit load is open. Conduction loss generated by device on-resistances and diode turn-on voltages are modeled by an equivalent output resistance (R_O) and an equivalent output voltage drop V_{DE}, respectively. High frequency dynamic switching loss—traditionally viewed as output-independent [66][73]—is divided into output-unrelated (i.e. gate-drive loss) and output-related loss (i.e. capacitive loss of diodes), which we model using two equivalent resistive loads R_{SWI} and R_{SWO} as shown in Figure 5-3.

Using the DC circuit model, the output voltage V_{OUT} can be written as

$$V_{OUT} = \left(N \cdot V_{IN} - V_{DE}\right)\frac{(R_L \parallel R_{SWO})}{R_O + (R_L \parallel R_{SWO})} \tag{5-1}$$

The power efficiency η is then calculated as

$$\eta = \frac{\frac{V_{OUT}{}^2}{R_L}}{\frac{V_{IN}{}^2}{R_{SWI}} + NV_{IN}\frac{NV_{IN} - V_{DE}}{R_O + (R_L \parallel R_{SWO})}} \tag{5-2}$$

where R_L is the load resistance.

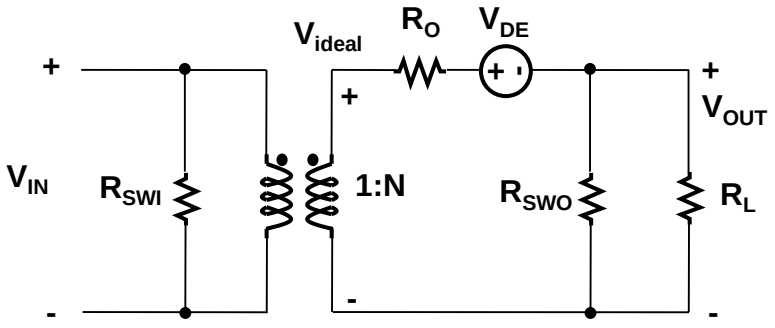


Figure 5-3. A general circuit model that accounts for non-ideal conduction and dynamic switching losses.

The model parameters (R_O, V_{DE}, R_{SWI}, R_{SWO}) shown in Figure 5-3 are used to represent the non-idealities generated by device and component parasitic resistances and capacitances. To help derive these model parameters, Figure 5-4 shows the non-ideal device models with important resistive and capacitive losses. As Figure 5-4 illustrates, inductor L has a parasitic series resistance (R_{IND}) which is generally modeled by $R_{IND}=\omega L/Q$. Here Q is the quality factor at radian frequency ω. The storage capacitors (i.e. C1, …, C($2N_{SC}$)) are assumed ideal in Figure 5-4 since they have relatively high quality factors. For the diodes, we model them by using turn-on voltage V_D, on-resistance R_D, and parallel parasitic capacitance C_D. For a given technology, the cutoff frequency f_T of the diodes could be assumed to be constant, thus diode capacitance C_D can be expressed as

$$C_D = \frac{1}{2\pi \cdot f_T R_D} \tag{5- 3a}$$

The MOSFET switch in Figure 5-4 is modeled by on-resistance R_M and gate-to-source, gate-to-drain, and drain-to-source parasitic capacitances C_{GS}, C_{GD}, C_{DS}. For a given technology, if assuming C_{GD}~C_{GS}, the figure-of-merit (FOM) [46] of the MOSFET can be expressed as FOM~(1+n)$C_{GS}V_{GS}R_N$, where n=V_{DS}/V_{GS} and where V_{GS} and V_{DS} are the gate and drain to source voltages, respectively. Because V_{GS} for the proposed switch equals V_{DD}, C_{GS} can be expressed as

$$C_{GS} = \frac{FOM}{(1+n)R_M V_{DD}} \tag{5-3b}$$

and C_{DS} can be written in terms of C_{GS} as

$$C_{DS} = \gamma \cdot C_{GS} \tag{5-3c}$$

where γ is a technology parameter (γ is typically 0.8-1) [75].

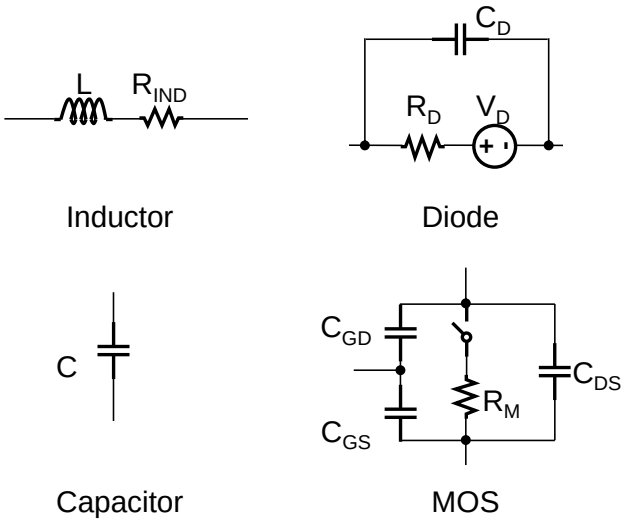


Figure 5-4. Simplified models of passive components and high-voltage devices.

By analyzing all the important conduction and switching losses of the devices in the generalized hybrid SI-SC converter, all analysis model parameters in Figure 5-3 can be derived. Firstly, the ideal voltage conversion ratio can be easily analyzed by assuming all devices are ideal. Considering inductor volt-second balance for the SI

stage and assuming small voltage ripple on capacitors, the total ideal voltage conversion ratio is then derived as

$$N = \frac{D_1 + D_2}{D_2} \cdot (N_{SC} + 1) \tag{5-4}$$

where N_{SC} is the stage number of the SC ladder. D_2 is the duty cycle of subinterval II in Figure 5-2, which can be approximately expressed as

$$D_2 = \begin{cases} \dfrac{1 - D_1}{2D_1 / K_m} & \text{CCM} \\ \dfrac{B_m + \sqrt{B_m{}^2 + 4D_1{}^2 / K_m}}{2D_1 / K_m} & \text{DCM} \end{cases} \tag{5-5}$$

Appendix A gives further details about D_2 in DCM. When N_{SC}=0, the hybrid converter is the same as the SI boost converter. Analysis has proved that equation (5) applies to SI boost as well (N_{SC}=0) [24].

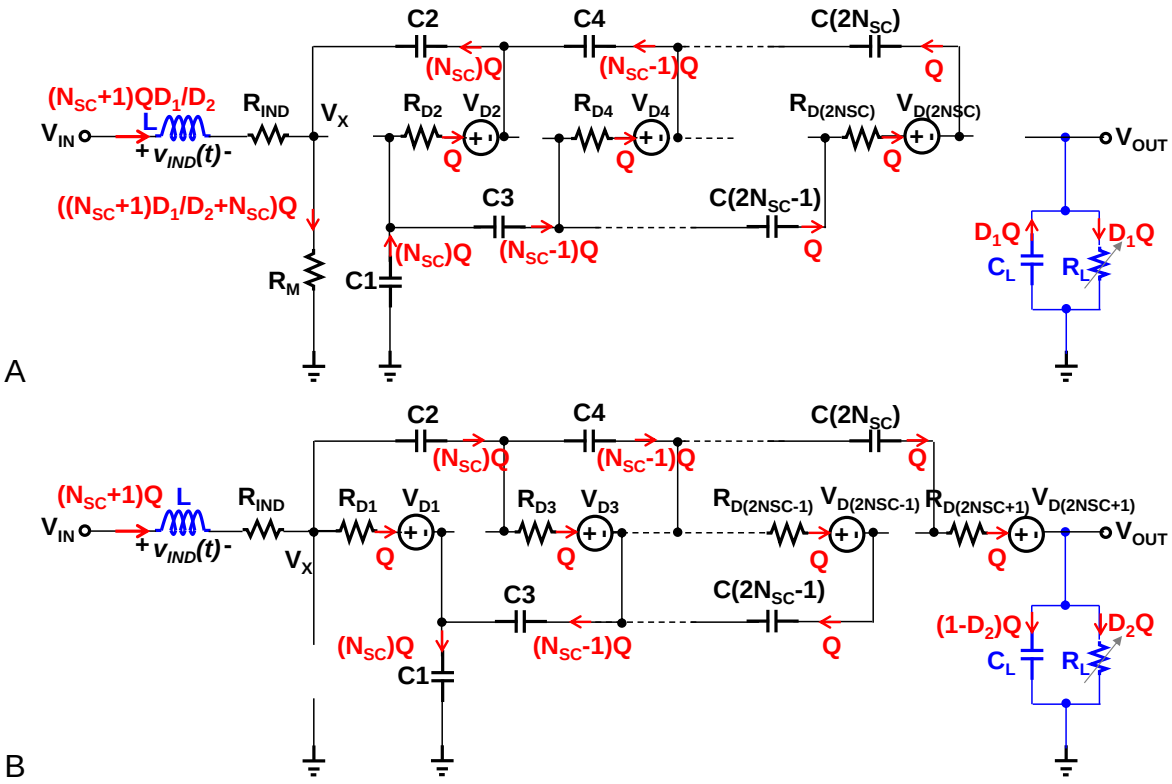


Figure 5-5. Charge flows in the hybrid SI/SC converter. A) Subinterval I, B) Subinterval II.

When analyzing the conduction loss for the generalized hybrid converter, charge vectors can be employed for simplifying equations, as used for SC converter in [66][73]. Following the same analysis procedure, charge flows through each element in subintervals I and II are illustrated in Figure 5-5 for the hybrid SI-SC converter. Charge and duty cycle vectors $\boldsymbol{a_r}$ and $\boldsymbol{d_r}$ for the resistive loss elements can be defined. A charge vector $\boldsymbol{a_c}$ is also defined for the flying and holding capacitors C1, C2, …, C($2N_{SC}$) as with [66][73]. Table 5-1 lists the elements of the defined vectors.

Table 5-1. Defined charge and duty cycle vector for the hybrid SI-SC step-up converter

	R_{IND}	R_M	R_{D1}	R_{D2}	R_{D3}	…	$R_{D(2NSC)}$	$R_{D(2NSC+1)}$
a_{ri}	$(N_{SC}+1)\bullet(D_1+D_2)/D_2$	$(N_{SC}+1)D_1/D_2+N_{SC}$	1	1	1	…	1	1
d_{ri}	D_1+D_2	D_1	D_2	D_1	D_2	…	D_1	D_2
	C1	C2	…	…	…	…	$C(2N_{SC}-1)$	$C(2N_{SC})$
a_{ci}	N_{SC}	N_{SC}	…	…	…	…	1	1

As analyzed for SC converters in [66], the equivalent output resistance R_O is estimated separately at low and high switching limits. The output resistance at the slow and fast switching limits is given by

$$R_{OSSL} = \sum_i \frac{{a_{ci}}^2}{C_i f_s} \tag{5-6a}$$

and

$$R_{OFSL} = \sum_i \frac{{a_{ri}}^2 R_i}{d_{ri}} \tag{5-6b}$$

respectively. R_O is then approximated as

$$R_O = \sqrt{{R_{OSSL}}^2 + {R_{OFSL}}^2} \tag{5-6c}$$

The equivalent output voltage drop V_{DE} for the hybrid SI/SC converter is given by

$$V_{DE} = (2N_{SC}+1)V_D \tag{5-7}$$

The hybrid SI/SC converter's inductor current ripple results in an output-unrelated AC conduction loss, which can be approximated by

$$P_{C\langle AC\rangle} = \frac{\Delta I_{IND}^2}{12}\left(R_{IND}(D_1 + D_2) + R_M D_1 + \frac{1}{\left(N_{SC}+1\right)^2} \sum_{i=1,3,\ldots,(2N_{SC}+1)} R_{Di} D_2 \right) \tag{5-8a}$$

Here the peak-to-peak inductor current ripple ΔI_{IND} is

$$\Delta I_{IND} = \frac{V_{IN} - I_{IND}(R_{IND} + R_M)}{L} D_1 T_S \tag{5-8b}$$

where the averaged inductor current is $I_{IND}=(N_{SC}+1)\cdot I_{OUT}/D_2$.

The equivalent resistance R_{SWI} represents the output-unrelated losses and includes the inductor ripple AC conduction loss $P_{A<AC>}$ and the gate-drive losses due to C_{GS}. Switching loss due to C_{SW} (i.e. the switched parasitic capacitances in the diodes and at the drain of the switch) contributes to both the output-unrelated and output-related loss terms, but not necessarily equally if analyzing carefully. For simplicity (and supported by simulation results), we assume equal contributions (0.5) to each. Different distribution values (i.e. 0.8) might be used for different other topologies to achieve better estimate since switching loss might affect input and output differently.

The voltage swings of the parasitic capacitances represented by C_{SW} are approximately $V_{IN}(D_1+D_2)/D_2$, thus R_{SWI} can be expressed as

$$R_{SWI} = \frac{{V_{IN}}^2}{\frac{\mathrm{FOM}}{R_N} V_{DD} f_S + P_{C\langle AC\rangle} + 0.5 \cdot C_{SW}\left(\frac{V_{IN}(D_1+D_2)}{D_2}\right)^2 f_S} \tag{5-9a}$$

where

$$C_{SW} = \left(\sum_i \frac{1}{2\pi f_T R_{Di}} + \frac{\mathrm{FOM}}{V_{DD} R_M (1+n)} \gamma \right) \tag{5-9b}$$

Here n=V_{DS}/V_{GS} and V_{DS} and V_{GS} are drain-to-source and gate-to-source voltage of the NMOS switch.

Table 5-2. Summary of steady state model equations for the hybrid SI-SC step-up converter

V_{OUT}	$\left(N \cdot V_{IN} - V_{DE}\right)\dfrac{(R_L \parallel R_{SWO})}{R_O + (R_L \parallel R_{SWO})}$
η	$\dfrac{\dfrac{V_{OUT}{}^2}{R_L}}{\dfrac{V_{IN}{}^2}{R_{SWI}} + NV_{IN}\dfrac{NV_{IN} - V_{DE}}{R_O + (R_L \parallel R_{SWO})}}$
	Hybrid SI-SC with N_{SC} SC ladder
D_2	$D_2 = \begin{cases} 1 - D_1 & \text{CCM} \\ \dfrac{B_m + \sqrt{B_m{}^2 + 4D_1{}^2 / K_m}}{2D_1 / K_m} & \text{DCM} \end{cases}$
N	$\left(N_{SC} + 1\right)\dfrac{D_1 + D_2}{D_2}$
R_O	$\sqrt{\left(\sum_i \dfrac{a_{ci}{}^2}{C_i f_s}\right)^2 + \left(\sum_i \dfrac{a_{ri}{}^2 R_i}{d_{ri}}\right)^2}$
V_{DE}	$(2N_{SC} + 1)V_D$
R_{SWI}	$\dfrac{V_{IN}{}^2}{\dfrac{\text{FOM}}{R_M}V_{DD} f_S + P_{C\langle AC\rangle} + 0.5 \cdot C_{SW}\left(\dfrac{V_{IN}(D_1 + D_2)}{D_2}\right)^2 f_S}$
$P_{C<AC>}$	$\dfrac{\Delta I_{IND}{}^2}{12}\left(R_{IND}(D_1 + D_2) + R_M D_1 + \dfrac{1}{\left(N_{SC} + 1\right)^2}\sum_{i=1,3,\ldots,2N_{SC}+1} R_{Di} D_2\right)$
R_{SWO}	$\dfrac{\left(N_{SC} + 1\right)^2}{0.5 C_{SW} f_S}$
C_{SW}	$\left(\sum_i \dfrac{1}{2\pi f_T R_{Di}} + \dfrac{\text{FOM}}{V_{DD} R_M \left(1 + n\right)}\gamma\right)$

And the equivalent resistance for the output-related loss RSWO can be written as

$$R_{SWO} = \frac{\left(N_{SC} + 1\right)^2}{0.5 \cdot C_{SW} f_s} \tag{5-10}$$

Table 5-2 summarizes the model parameters and equations for the generalized hybrid SI/SC step-up converter.

5.3 Model Validation

Table 5-3. Important device parameters used in SPICE simulation for SI converter (N_{SC}=0)

	Inductor		Switch ($n=V_{DS}/V_{GS}$=5)			Diode		
Topology	L	R_{IND} @50MHz	R_M	C_{GS}	C_{DS}	R_D	V_D	C_D
N_{SC}=0	820nH	9.28Ω	8.5Ω	1.8pF	1.7pF	45.5 Ω	0.24V	1.5pF

Table 5-4. Important device parameters used in SPICE simulation for hybrid SI-SC converter (N_{SC}=1)

	Inductor		Switch			Diode (1x)		
Topology	L	R_{IND} @50MHz	R_M	C_{GS}	C_{DS}	R_D	V_D	C_D
N_{SC}=1	820nH	9.28Ω	2.16Ω	0.3pF	5pF	15.6Ω	0.5	3.2pF
Diode/Cap	D1	D2	C1	C2				
Size	1x	1x	17pF	17pF				

Table 5-5. Important device parameters used in SPICE simulation for hybrid SI-SC converter (N_{SC}=4)

	Inductor		Switch			Diode (1x)			
Topology	L	R_{IND} @50MHz	R_M	C_{GS}	C_{DS}	R_D	V_D	C_D	
N_{SC}=4	390nH	7.75Ω	8.5Ω	1.8pF	1.7pF	2k Ω	0.24V	100fF	
Diode	D1	D2	D3	D4	D5	D6	D7	D8	D9
Size	10x	5x	10x	5x	10x	5x	8x	4x	6x
Cap	C1	C2	C3	C4	C5	C6	C7	C8	
Size	180pF	180pF	180pF	160pF	160pF	140pF	140pF	120pF	

The accuracy of the proposed circuit model is verified against SPICE using the simplified device model shown in Figure 5-4. Table 5-3-5 list the corresponding simulation parameters of three specific hybrid converter examples (N_{SC}=0, 1 and 4) employed in this section. These device parameters are employed based on power devices implemented in a 1.2V CMOS process. The dc-dc converters' efficiency and output voltage (V_{OUT}) were simulated against load resistance (R_L) and switching frequency (f_S) and across duty cycles D_1=0.2 and 0.8, without restrictions on DCM or

CCM operation. For these simulations, R_L was varied from 10Ω to 100kΩ and the switching frequency from 1MHz to 400MHz.

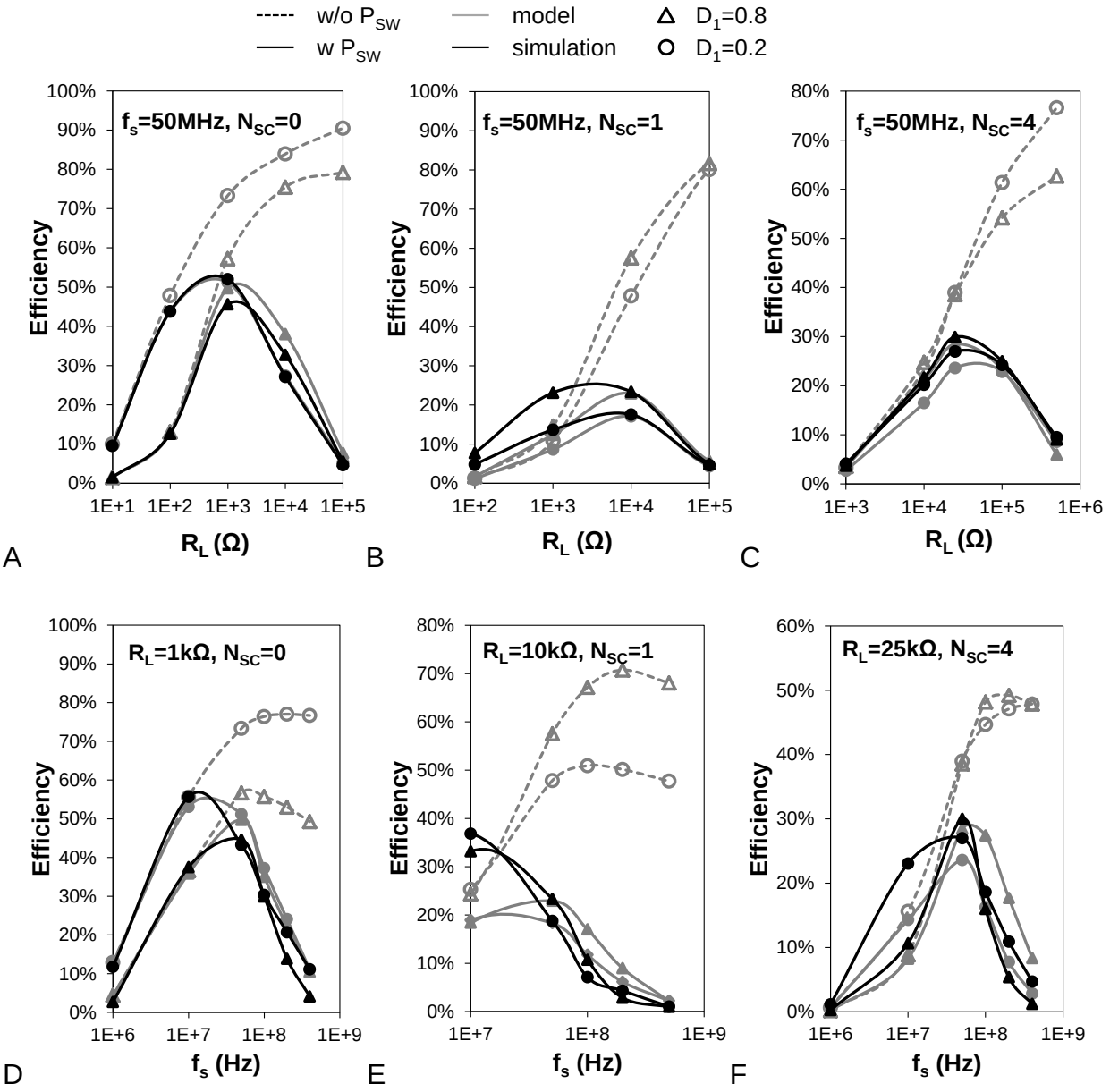


Figure 5-6. Power efficiency obtained from model and SPICE simulation for the three hybrid SI/SC converters. A) N_{SC}=0 and f_S=50MHz, B) N_{SC}=1 and f_S=50MHz, C) N_{SC}=4 and f_S=50MHz, D) N_{SC}=0 and R_L=1kΩ, E) N_{SC}=1 and R_L=10kΩ, F) N_{SC}=4 and R_L=25kΩ.

The efficiency vs R_L and f_S for the switched inductor topology (N_{SC}=0) shown in Figure 5-6a and 6d is in good agreement with SPICE with an average model error of

<20%. For the SI-SC topologies (N_{SC}=1 and 4), the average model error is <35%, which is primarily due to: (a), current nonlinearity in the SC stages that is not captured by the equivalent output resistance approximation in Eq. 6; (b), slow turning on/off transitions resulted from large switching loss and their effects on effective duty cycle and conduction loss calculation. The model exhibits improved accuracy for larger R_L or f_S values mainly due to small current nonlinearity in these conditions. As one would expect, efficiency degrades as R_L is increased for fixed f_S (Figure 5-6a-c) and/or as f_S is increased for fixed R_L (Figure 5-6d-f). To highlight the importance of switching losses, also included in Figure 5-6 are the model results when these losses are neglected altogether, showing a noticeable drop in power efficiency at lighter loads and higher switching frequencies. Importantly, the model predicts desirable operating switching frequency range for optimal efficiency. Moreover, the proposed model does not make any assumptions of DCM or CCM operation. Conventional models [66][73][74], which only employ R_{SWI} to incorporate the effect of the switching loss, are less accurate especially in DCM.

As with the power efficiency, plots of output voltage vs R_L and f_S for the three simulated converters are also shown Figure 5-7. In simulations, maximum output voltages are ~7V, ~11V, and ~35V for the three converters respectively at 50MHz. Average model error is <20% for the switched inductor topology (N_{SC}=0), <30% for the hybrid SI/SC topologies (N_{SC}=1, 4). Dashed lines of analysis results without including switching loss are also shown to demonstrate the effects of switching loss on output voltage. Conventional models [66][73][74] which only employ R_{SWI} to incorporate the effect of the switching loss result in huge model error especially in deep DCM.

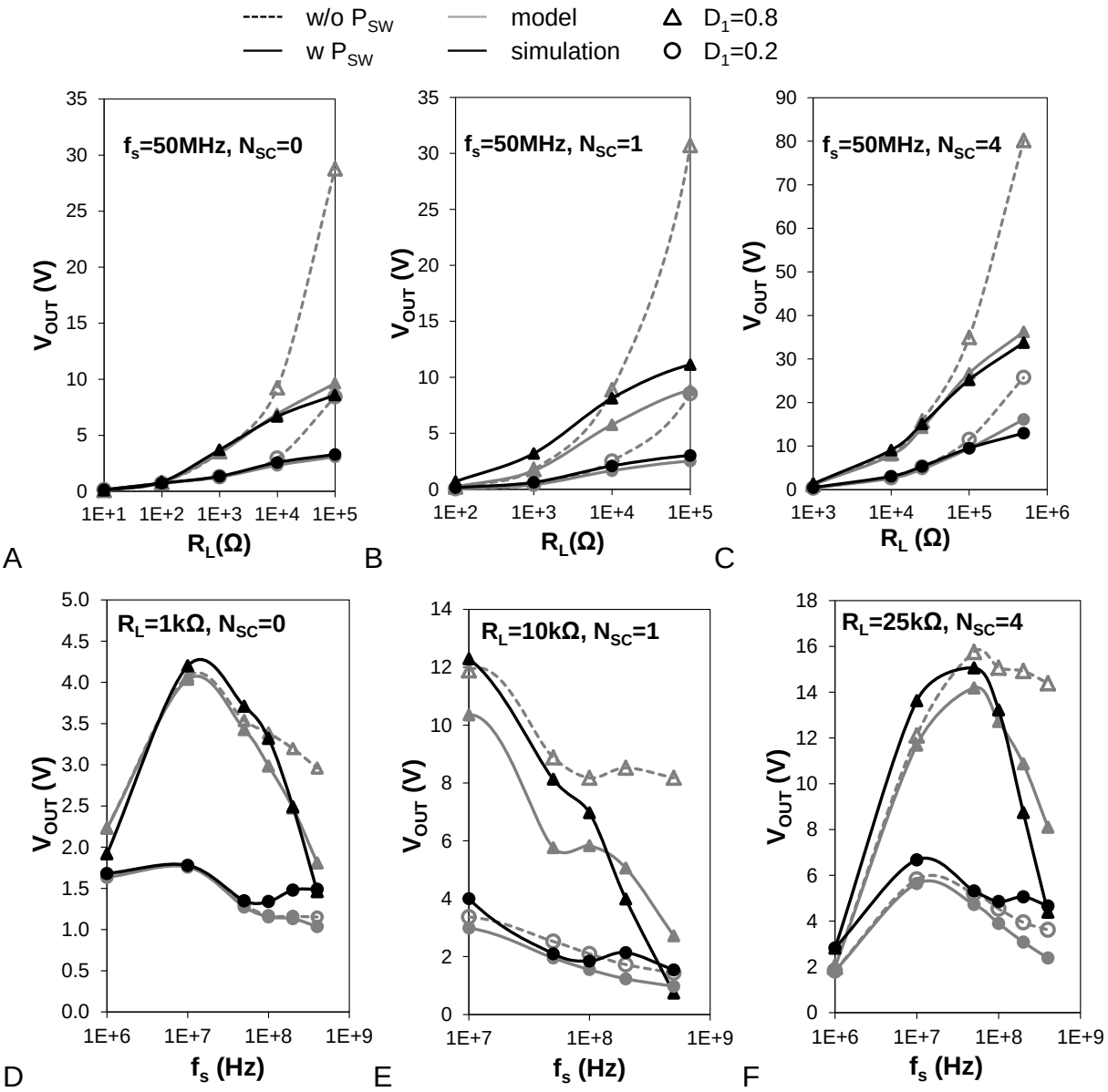


Figure 5-7. Output voltage obtained from model and SPICE simulation for the three hybrid SI/SC converters. A) N_{SC}=0 and f_S=50MHz, B) N_{SC}=1 and f_S=50MHz, C) N_{SC}=4 and f_S=50MHz, D) N_{SC}=0 and R_L=1kΩ, E) N_{SC}=1 and R_L=10kΩ, F) N_{SC}=4 and R_L=25kΩ.

Moreover, the plots in Figure 5-7 show increased model error at large R_L for fixed f_S (Figure 5-7a, 7b, 7c) or at large f_S for fixed R_L (Figure 5-7d, 7e, 7f) for all three converters. The reason is because switching loss becomes dominating at large R_L or at large f_S, resulting in slow switching transition and inaccurate calculation of duty cycle D_2 in eq. 5. Switching behavior becomes extremely complicated especially when both

inductor and capacitor are present and may also involve energy oscillating. Referring to Figure 5-6, power efficiency drops quickly at these regions and designers should avoid operating converters near these regions for performance consideration.

5.4 Experimental Results

To provide more proof for the proposed analysis model as well as to demonstrate ultra-miniature high voltage powering system, three hybrid SI-SC converters with respective N_{SC}=0, 1, and 4 have been fabricated in a 130nm 1.2V CMOS process. Since the baseline CMOS process only provides 1.2V thin oxide and 3.3V I/O transistors, in order to create large output voltages, some custom high voltage tolerant devices such as stacked NMOS switch and schottky barrier diodes were developed and utilized in the three hybrid converters. Device testing kits including two types of stacked NMOS switch and four types of schottky barrier diodes were fabricated without using any extra masking and process steps. And measurement results have shown that breakdown voltage of these customized devices could be extended to ~10V which is 3x larger than the operating voltage of the standard 3.3V devices [39].

For stacked NMOS switch, the first composite structure is stacking a 3.3V thick-ox transistor on top of a 1.2V thin-ox transistor, and the second one is stacking two 3.3V thick-ox transistors while using a low-threshold footer device. These two composite structures were chosen since they have good tradeoff between large block voltage and low on-resistance while they are driven by 1.2V switching clocks. Gate bias of the top transistor in each composite structure was selected as 2.5V and 3V respectively for life time requirement of the footer transistor considering time dependent dielectric breakdown (TDDT) [34]. Measurement shows that specific on-resistance of these two composite structures are 1.9e-5 $\Omega\cdot cm^2$ and 1.5e-4 $\Omega\cdot cm^2$ respectively. Switching gate

charges which are useful for switching loss estimate were approximated through SPICE simulation when assuming 6V (n=6/1.2=5) block voltage from the top drain to the bottom source. Thus from these estimated switching gate charges, FOMs of the two stacked NMOS switches are then calculated as 48 mΩ·nC and 345 mΩ·nC (for V_D=6V).

Table 5-6. Characteristic summary of stacked NMOS switches

	$A \cdot R_{ON}$ (Ω·cm2)	FOM (mΩ·nC)
Stacked-Switch w/ thin-ox transistor	1.9E-5	48
Stacked-Switch w/ thick-ox LVT transistor	1.5E-4	345

Table 5-7. Characteristic summary of schottky barrier diodes

	V_D (mV)	$A \cdot R_D$ (Ω·cm2)	f_T (GHz)
n-type SBD w/o guard ring	380	3.2e-5	26
p-type SBD w/o guard ring	270	5.2e-5	15
n-type SBD w/ guard ring	495	5.1e-5	12
p-type SBD w/ guard ring	460	6.7e-5	8

For schottky barrier diodes, testing structures of n- and p-type with and without p+/n+ guard rings were implemented by selectively blocking the n+/p+ implants in desired diffusion areas or by directly contacting the N-/P-well with metallization [39][76]. On-state current density was measured and their specific on-resistance ($A \cdot R_D$) and turn-on voltage (V_D) were extracted using first-order piecewise linear model. To evaluate their switching behavior, cutoff frequency was also measured using network analyzer from which their switching loss could be modeled and estimated. Table 5-6 and Table 5-7 summarize electric characteristics of implemented custom high voltage devices.

Schematics of the three hybrid SI-SC converters with respective N_{SC}=0, 1, and 4 are illustrated in Figure 5-8. The first two converters in Figure 5-8a (N_{SC}=0) and 8b (N_{SC}=1) use the same stacked NMOS switch (with thin-ox footer transistor) but different n-type schottky barrier diodes. The diode in Figure 5-8a has guard rings for less reverse

leakage current, while the second diode in Figure 5-8b does not have guard rings for low on-resistance and low turning-on voltage. The second converter also has three 17pF onchip capacitors for voltage doubling. Among them, the third capacitor C3 can be lumped with the external load capacitor C_L, thus it is not included in analysis model. All onchip capacitors were implemented using Metal-insulator-Metal (MIM) with capacitance density of ~1fF/μm^2. Die photo of the first two hybrid converters in Figure 5-8a and 8b is shown in Figure 5-9a, in which the first one takes ~500x380μm^2 and the second one takes ~500x400μm^2. The high voltage devices (i.e. NMOS switch and Schottky diodes) occupy ~43% of the total area in both designs.

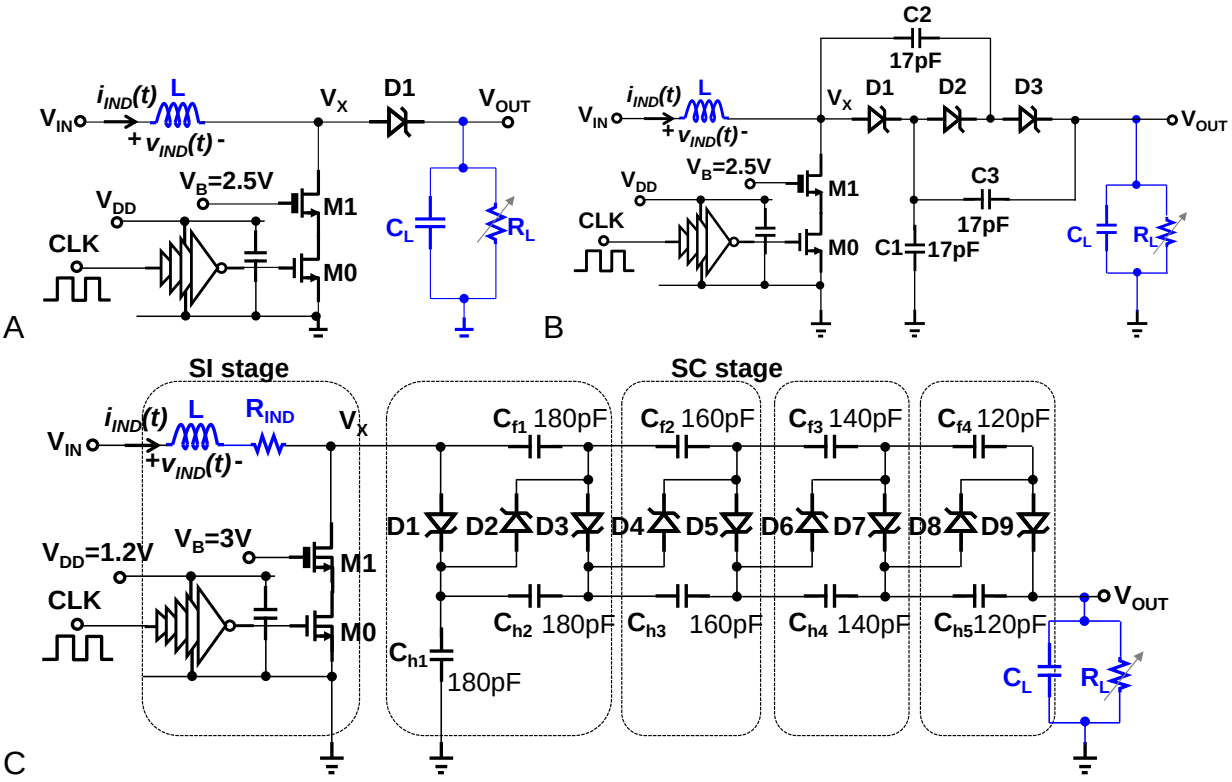


Figure 5-8. Schematics of three fabricated hybrid SI-SC converters. A) N_{SC}=0 (SI boost), B) N_{SC}=1, C) N_{SC}=4.

Schematic of the third hybrid SI-SC converter with N_{SC}=4 is shown in Figure 5-8c. It employs the second stacked NMOS switch which uses both thick oxide devices but

the footer transistor has low threshold voltage to reduce on-resistance. The SC ladder multiplier utilizes p-type schottky barrier diodes for even less on-resistance and the capacitors are all onchip MIM caps. One important thing to mention here is that as the number of the SC stage increases, though voltage stress on each device is small, large output voltage may cause some parasitic junctions to break down. To avoid junction breakdown, post-process step was implemented to create isolation trenches between each SC islands as outlined with dashed lines in Figure 5-8c. Since the cost of the post process step is low, this could be a potential low cost approach for generating very large voltages for autonomous microsystems. Die photo of the converter after post processing is shown in Figure 5-9c, where the SI stage is 1.2mm*1mm and the SC stage is 1.2mm*2.4mm with isolation trenches shown between SC islands. Isolation trenches were done by using dicing saw with width of ~35μm. The bottom of the die was attached to a pyrex wafer for electrical insulation.

To verify the analysis model presented in section II, the three hybrid SI-SC step-up converters were open-loop tested using external drive clocks with constant duty cycle of D=0.8 and input voltage of 1.2V. Figure 5-10, 11, and 12 plot their measured output voltages and efficiencies alongside their respective analysis model results for comparison. As shown in Figure 5-10 and 11, the first two converters were evaluated over a variety of loads at 25MHz and 50MHz respectively when coilcraft chip inductors of 390nH with quality factor Q=22 at 50MHz and of 820nH with Q=18 at 25MHz were employed. While in Figure 5-12, the third hybrid converter was measured using chip inductors of 390nH, 1μH, and 2.7μH at 25MHz, 12.5MHz, and 6.25MHz respectively. Inductor quality factors Q are estimated from datasheet as 10, 20, and 25 at their

respective switching frequency. Different inductor values and switching frequencies picked for each topology in measurements were to maximize output voltage while keeping power efficiency as high as possible.

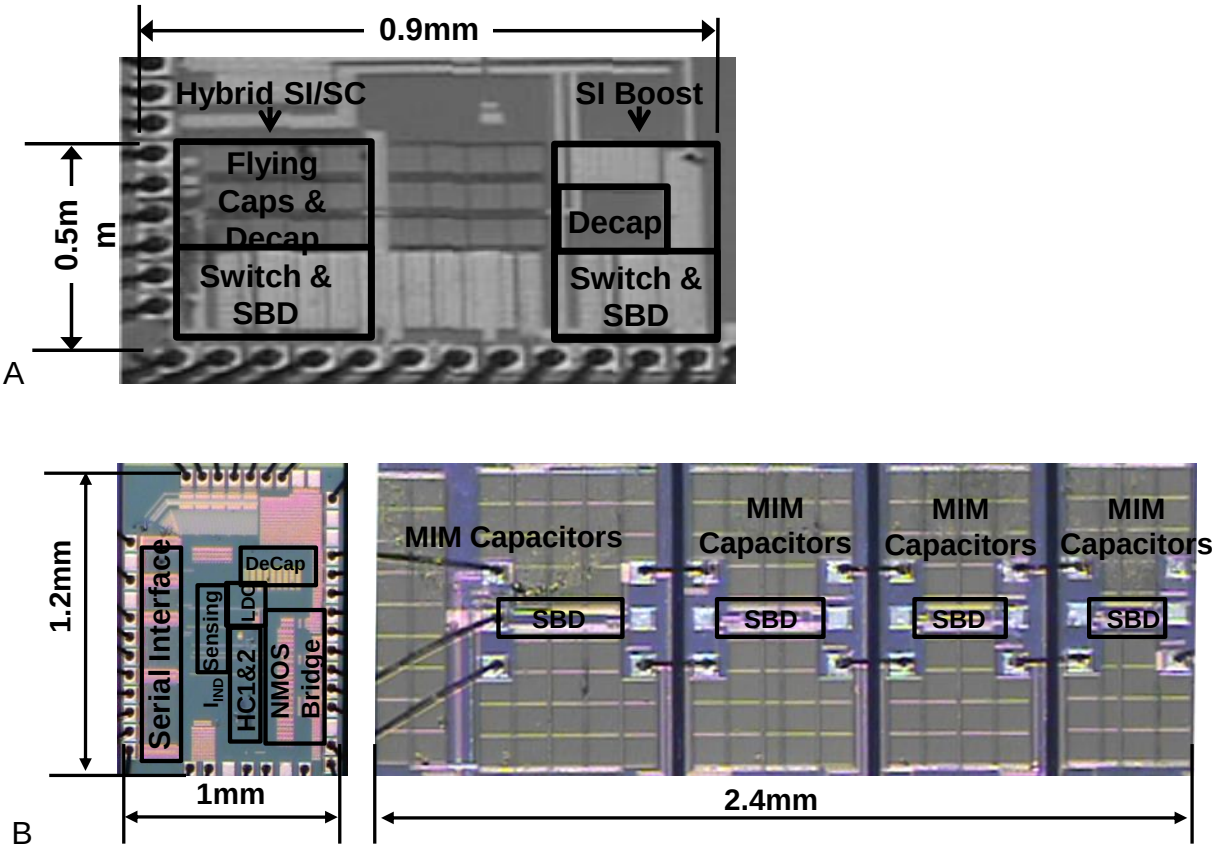


Figure 5-9. Die photos of three hybrid converters. A) SI (N_{SC}=0) and hybrid SI-SC (N_{SC}=1), B) hybrid SI-SC (N_{SC}=4).

In Figure 5-10, the first hybrid SI-SC converter with N_{SC}=0 (also called SI converter) achieves a peak output voltage of ~6V at 3.5kΩ and peak efficiency of ~61% at ~800Ω when switching at 50MHz with an inductor of 390nH in measurement. Similar output voltage and a slightly higher peak efficiency of ~69% at 1.2kΩ are obtained for a switching frequency of 25MHz with an 820nH inductor. In Figure 5-11, maximum output voltage of the second converter is ~10V at 15kΩ, which is ~1.7x larger than that of the first hybrid converter. Measurement shows output voltage of the second hybrid

converter could not go higher than 10V. The reason for that is because NWELL-PSUB junction breaks down at ~10V. Thus by using post-processing, as shown in Figure 5-12, the third hybrid converter with four-stage SC ladder (N_{SC}=4) achieves a maximum output voltage of ~30V in measurement, which is 3x larger than that of the second converter. Maximum power efficiency of the second and third hybrid converters in measurement is similar, ~40% as shown in Figure 5-11 and 12.

Analysis model results after accounting for conduction and switching loss based on electric characteristics of utilized inductors and those custom high voltage devices in Table 5-6 and 5-7 were plotted as gray lines in Figure 5-10, 11, and 12. For output voltage, these plots show that modeling error increases with load resistance. Possible reasons include: firstly, as voltage increases, reverse leakage current of power devices increases, which has not been included in the model presented in section II; secondly, as load resistance increases, each hybrid converter intends to move from CCM where conduction loss dominates to DCM where switching loss dominates. The calculation equation of duty cycle D_2 in Table 5-2 only accounts resistive elements and becomes less accurate as load resistance increases.

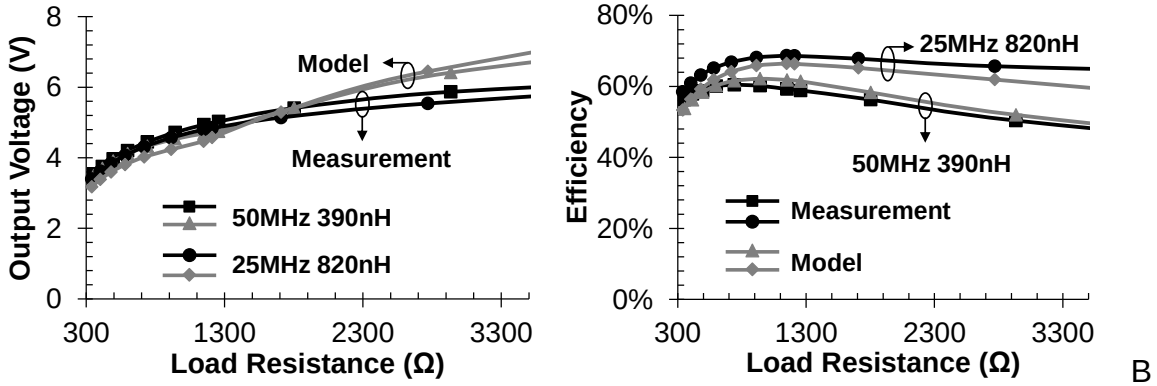


Figure 5-10. Measurement and model results of the first hybrid converter (N_{SC}=0) with V_{IN}=1.2V and D_1=0.8. A) Output voltage, B) Efficiency.

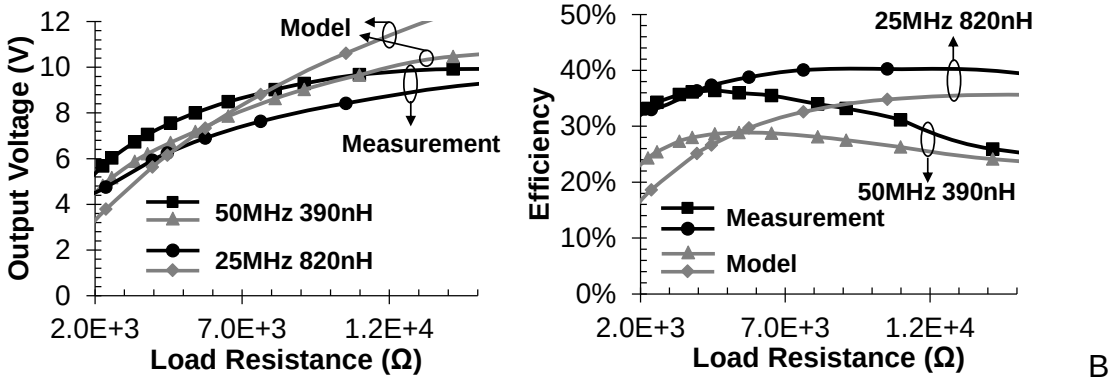


Figure 5-11. Measurement and model results of the second hybrid converter (N_{SC}=1) with V_{IN}=1.2V and D_1=0.8. A) Output voltage, B) Efficiency.

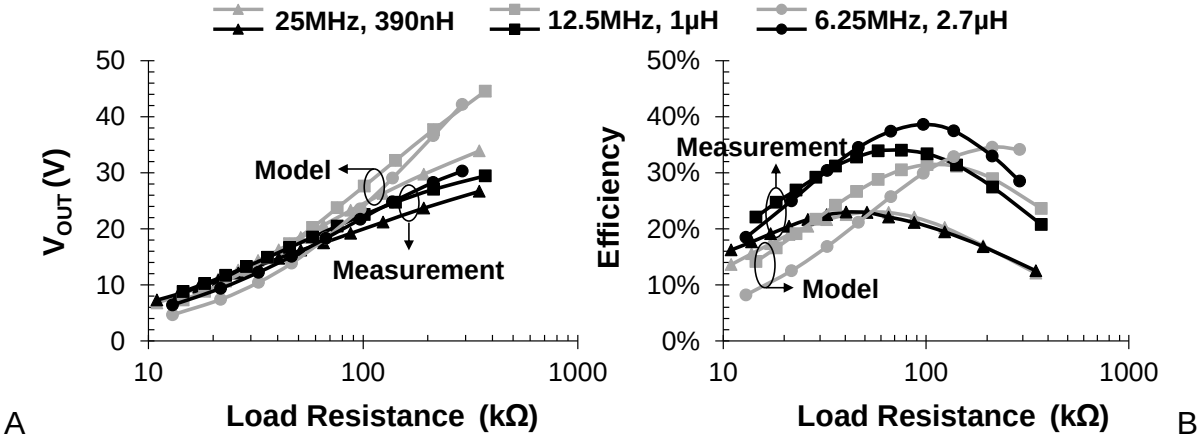


Figure 5-12. Measurement and model results for the third hybrid converter (N_{SC}=4) with V_{IN}=1.2V and D_1=0.8. A) Output voltage, B) Power efficiency.

For power efficiency, comparison between measurement and analysis model results show that modeling error is relatively large when load resistance is small (large output current). Possible explanation for this behavior is that when load current is large, capacitor voltage varies significantly causing charging and discharging current highly nonlinear. Thus the equation for approximating output resistance (R_O) using its slow switching limit and fast switching limit in Table 5-2 becomes less accurate and induces large modeling error at low load resistance condition. However, considering the entire load resistance range, average modeling percent error between analysis model and

measurement results is reasonable, which is ~20%, ~30%, and 35% for the first (N_{SC}=0), second (N_{SC}=1), and third (N_{SC}=4) hybrid SI-SC step-up converter respectively.

5.5 Modeling and Analysis Conclusions

This chapter presents a generalized hybrid SI-SC step up DC-DC converter that is good at generating large voltage conversion ratio for driving high voltage actuators in autonomous microsystems. To accurately analyze its performance, a modified circuit model is proposed by accounting for all important non-ideal conduction and switching losses. Different from other approaches, ours divides dynamic switching loss into output-unrelated and output-related contributions and utilizes two additional resistive loads to separately model them. All these model parameters including equivalent output resistance are then derived using a theoretic network methodology based on charge multiplier vectors. SPICE simulation and experimental results of three specific hybrid SI-SC converter examples are provided for comparison with the proposed analysis model. Good agreement on output voltage and power efficiency is demonstrated. Therefore the proposed circuit model could be used to guide circuit designers to analyze and optimize the performance of hybrid SI-SC converters when designing a suitable high voltage powering unit in autonomous microsystems.

CHAPTER 6
MINIATURE HIGH VOLTAGE HYBRID STEP-UP POWER CONVERTER FOR SMART PIEZOELECTRIC MICROSYSTEMS

6.1 Introduction of High Voltage Converters in Microsystems

Bug-sized robotic platforms that crawl, jump, flap or fly [2][77] have been actively pursuing miniature high voltage power converters for driving actuators (i.e. piezoelectric) to realize locomotion. For example, a power survey on tiny platforms that are under development in MAST [3] has been illustrated in Figure 6-1, from which we could see most actuators require driving voltage >10V. To address these design concerns, power converters not only need to have large voltage conversion ratio, but also need to be highly efficient and ultra-compact, which at small scales posts a remarkably daunting task. Additionally, to meet the stringent mass and volume requirements, the necessary digital motion control and communication system should be integrated on the same die with the power conversion blocks. To date, little work has been introduced that combines the functionality of these blocks in a highly integrated form using a standard fine-line CMOS process. This chapter is aimed to fill this gap by presenting a hysteretic-controlled hybrid SI-SC step-up converter in a 130nm CMOS process for creating large driving voltages and using it with a TI commercial DSP to create a smart piezoelectric micro-flapper for demonstration.

Traditionally, high voltage power converters in micro-robots are usually realized by using either a large number of discrete components [9] or a bulky transformer [10], resulting in large system volume and low power density. P. Basset, et al. demonstrated a miniature 10kHz 100V Cockcroft-Walton step-up converter with digital control circuitry integrated in a 100V CMOS technology with total area of 5mm x 3mm for actuators [11]. However, the relatively low cutoff frequency of the high voltage process restricts

achievable switching frequency employed for the step-up converter, thereby causing big passives, large area and low efficiency. K. Ishida, et al. presented a 20-30MHz 1.8V-to-20V switched inductor (SI) boost converter using a 0.18μm CMOS and 20V NAND flash process [78], resulting in a much smaller footprint. But the utilization of an extra high voltage process to implement power switches and rectifiers for handling large voltage stress intrinsically imposed by the SI boost topology causes this solution expensive. M. Innocent, et al. [79] and R. Pelliconi, et al. [52] reported fully integrated 50-100MHz 10-15V high voltage generators in 0.18μm CMOS technologies by using switched-capacitor (SC) topologies which are superior in distributing large voltage stress across switches and diodes comparing to the SI boost, thereby allowing their monolithic integration in low voltage processes. The main drawback for SC converters is that efficiency drops significantly at heavy loads or non-integral conversion ratios causing line/load regulation poor. Moreover, SC converters suffer from large input current ripple, demanding big decoupling capacitors at the input. The above drawbacks of SC converters could be mitigated by using different techniques such as quasi-SC [80] or hybrid topology [39]. The hybrid SI-SC topology reported in [39] combines the benefits of both SI and SC converters, keeping reduced voltage stress across devices, thereby allowing exploration of fine feature size, large transistor density, and high switching frequency of advanced CMOS technologies to realize ultraminiaturized onchip high voltage step-up converters. E. Stelz, et al. [9] also present that the hybrid topology is one of the best solutions for powering high voltage actuators.

This chapter utilizes the hybrid SI-SC topology and customized high voltage tolerant devices in a 1.2V standard CMOS process to generate large driving voltages up

to 35V from a 3V input with minimal post-process steps and external components as well as demonstrates a smart piezoelectric flapper using the implemented hybrid step-up converter with a TI commercial DSP. The structure of this chapter is as follows: Section II presents the converter schematics and discusses a design methodology for optimizing area and power efficiency. Section III then introduces a high-frequency hysteretic controller and a serial-parallel interface for programming and communicating to the hybrid converter with minimal external wires. Section IV provides experimental results of the stand-alone hybrid step-up converter and section V describes the details of the demo, a smart piezoelectric flapper and its testing results.

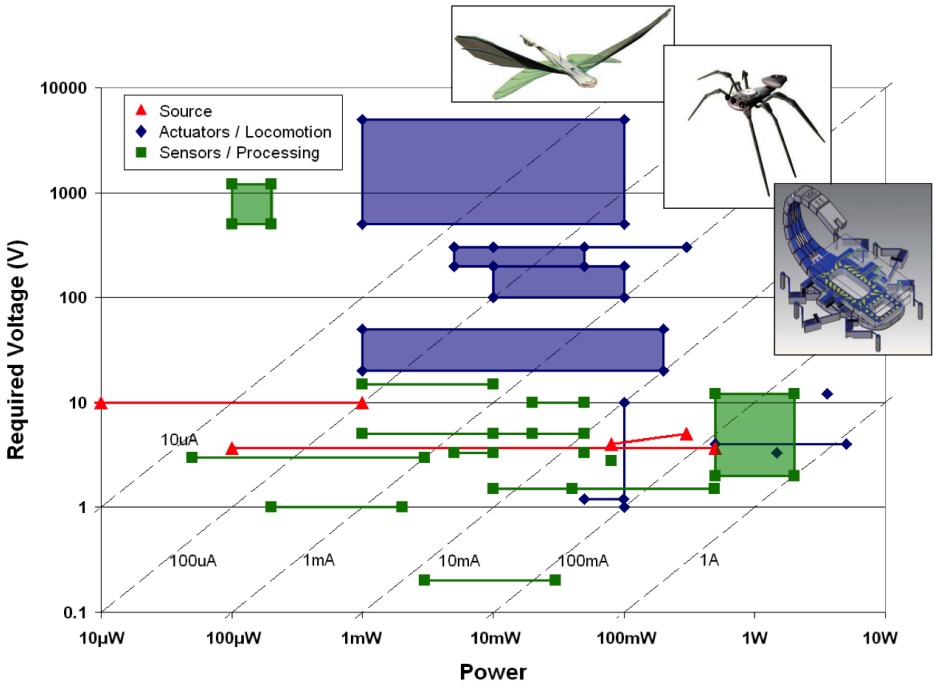


Figure 6-1. Power requirements for various autonomous microsystems.

6.2 High Voltage Hybrid SI-SC Step-Up Converter

Implementation of a hybrid SI-SC step-up converter in an advanced CMOS process is challenging for reliability reasons due to large voltage stress. The potential strategy for enabling voltages beyond the maximum voltage rating of a CMOS process

consists of distributing the output voltage of the step-up converter across multiple of its constituent devices so that the blocking voltage seen by any single device never exceeds its safe operating limit. Thus power transistor trains [39][45] especially low side NMOS are good solutions to realize high voltage tolerant power switches in a low voltage CMOS process without using extra process steps as well as to keep the fabrication cost low. For high side PMOS switch, however, power transistor trains require complicated floating driving circuitry. Thus in this chapter schottky barrier diodes are chosen over PMOS as high side switches since they have low voltage drop and fast transition time and could also genuinely block any reverse current flow which is very common when the converter works in discontinuous conduction mode for large conversion ratio situations.

Figure 6-2 illustrates the implementation details of the high voltage hybrid SI-SC step-up converter using the two specialized high voltage tolerant devices fabricated in a standard 130nm CMOS process. The low side stacked NMOS switch is made with a 3.3V 70Å thick-oxide nMOS stacked on a low-V_T thick-oxide nMOS device. A 1.2V switching clock is selected to drive the bottom device while the top transistor is biased at a fixed gate voltage. In this way, switching loss is reduced and conductivity is kept high. Measurement results show that its specific on-conductance is 1.5E-4 Ω/cm^2 with breakdown >10V. Moreover, with the aid of SPICE simulation, gate charge of the stacked NMOS switch is estimated from which its FOM (figure of merit) is calculated as 345 mΩ•nC [46]. For high side rectifiers, p-type schottky diodes are used which are fabricated in isolated p-wells (enclosed in deep n-well) by selectively blocking p+ implants in desired diffusion areas [39]. Measured forward turn-on voltage,

conductance, and cutoff frequency of the SBD are 280 mV, 5.2E-5 Ω/cm^2, and 15GHz respectively.

The hybrid SI-SC converter is composed of a SI stage and a 4-stage SC ladder multiplier. As with the SI boost converter, the SI stage creates a large amplitude square wave at node V_X. Assuming the driving clock has a duty of D, the generated wave amplitude is $V_{IN}/(1-D)$. This large amplitude square wave is then multiplied and rectified four times by the SC ladder thus ideally creating an output voltage up to $5V_{IN}/(1-D)$. Here the ladder multiplier topology is chosen over Dickson charge pump [81] and other SC architectures [66] since large voltage stress is equally distributed across each diode and capacitor which makes it more suitable for integration in low cost low voltage CMOS technology. In the SC ladder multiplier, all capacitors are implemented using onchip MIM capacitors with total capacitance of 1.4nF and density of 1fF/um^2. Each MIM capacitor has a breakdown voltage >15V.

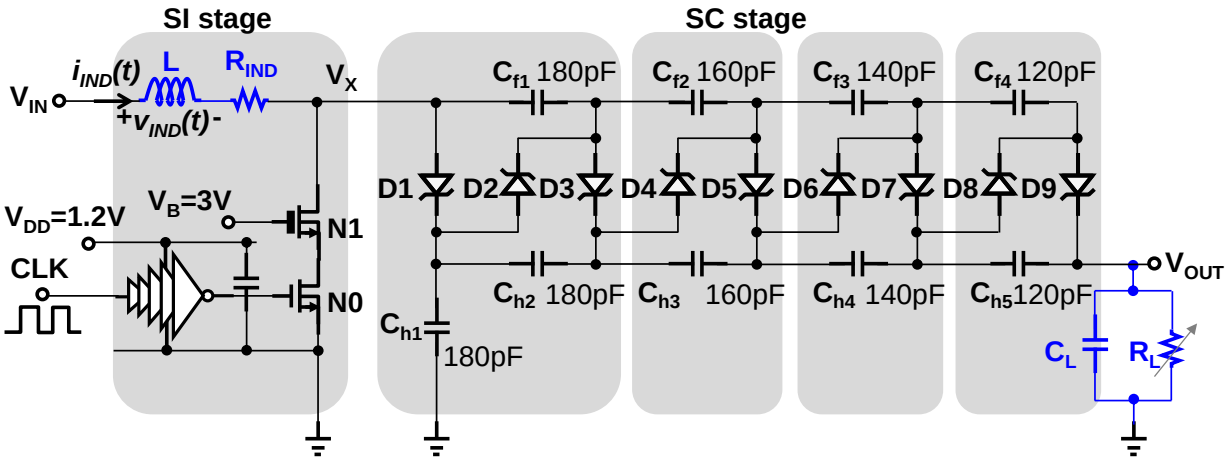


Figure 6-2. Implementation detail of the high voltage hybrid SI-SC step up converter.

6.2.1 Optimal Design Procedure

To help analyze the performance of the hybrid SI-SC step up converter, a DC circuit model using an ideal DC transformer to represent power conversion [66] as

shown in Figure 6-3 could be used. In this DC circuit model, conduction and switching loss is lumped and modeled using output and input impedance R_O and R_I respectively. Additionally, since diodes are used in the hybrid topology, power loss related to their turn on voltages is modeled using a lump voltage source V_{DE} as shown in Figure 6-3. Thus, from the DC circuit model, the performance of the hybrid converter could be represented using the following two equations:

$$V_{OUT} = \left(N \cdot V_{IN} - V_{DE}\right)\frac{R_L}{R_O + R_L} \tag{6-1a}$$

$$\eta = \frac{\frac{V_{OUT}{}^2}{R_L}}{\frac{V_{IN}{}^2}{R_I} + NV_{IN}\frac{NV_{IN} - V_{DE}}{R_O + R_L}} \tag{6-1b}$$

where N is ideal voltage conversion ratio, η is power efficiency, and R_L is load resistance.

Regarding the circuit parameters in Figure 6-3 for the hybrid SI-SC step up converter, a theoretic network methodology based on charge multiplier vectors [66] can be employed. By analyzing charge flow in the two switching phases in Figure 6-4a and 4b when the stacked NMOS is turned on and off, a charge vector a_r and duty cycle vector d_r for all switches and the inductor, and a charge vector a_c for all capacitors could be defined to represent output-normalized charge flowing through each device over one switching period. The defined vector values are listed in Table I. Here D_1 and D_2 are duty cycles when the stacked NMOS is on and off respectively. In continuous conduction mode, D_2=1-D_1. And V_D is the turn on voltage of the diodes. Additionally, the charge flow through C_{h5} is negligible when output capacitor C_L is large enough thus C_{h5} is not modeled in later analysis.

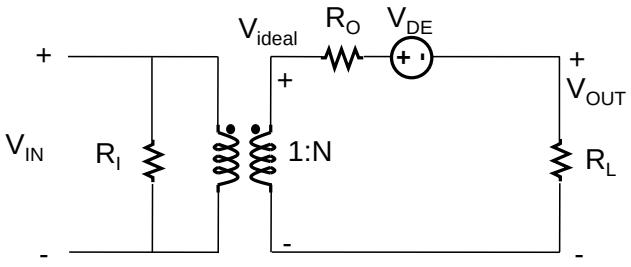


Figure 6-3. A DC circuit model for performance analysis.

Table 6-1. Defined charge and duty cycle vector for the hybrid SI-SC step-up converter

R_i	L	NMOS	D1	D2	D3	D4	D5	D6	D7	D8	D9
a_{ri}	$5D_1/D_2+5$	$5D_1/D_2+4$	1	1	1	1	1	1	1	1	1
d_{ri}	D_1+D_2	D_1	D_2	D_1	D_2	D_1	D_2	D_1	D_2	D_1	D_2
C_i	C_{h1}	C_{f1}	C_{h2}	C_{f2}	C_{h3}	C_{f3}	C_{h4}	C_{f4}	C_{h5}		
a_{ci}	4	4	3	3	2	2	1	1	-		

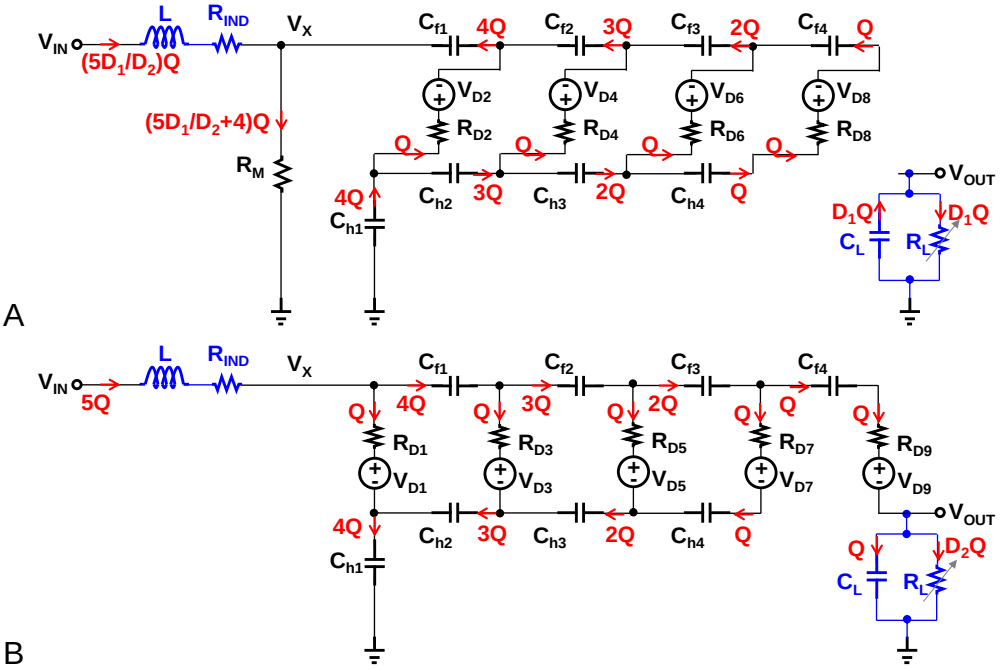


Figure 6-4. Charge flow analysis of the hybrid SI-SC step up converter in the two switching phases. A) When the stacked NMOS is on, B) When the stacked NMOS is off.

As analyzed for SC converters in [66], the equivalent output resistance R_O is estimated separately at low and high switching limits. Assuming the switching frequency

is f_s, the output resistance at the slow and fast switching limits (SSL and FSL) is given by

$$R_{OSSL} = \sum_i \frac{a_{ci}^{\ 2}}{C_i f_s} \tag{6-2a}$$

and

$$R_{OFSL} = \sum_i \frac{a_{ri}^{\ 2} R_i}{d_{ri}} \tag{6-2b}$$

respectively. R_O is then approximated as

$$R_O = \sqrt{R_{OSSL}^{\ 2} + R_{OFSL}^{\ 2}} \tag{6-2c}$$

The equivalent output voltage drop V_{DE} for the hybrid SI/SC converter is given by

$$V_{DE} = 9V_D \tag{6-3}$$

To optimally design the hybrid SI-SC step up converter for target specs on V_{OUT}, P_{OUT}, and η, the following procedure illustrated in Figure 6-5 could be employed.

Firstly, from target output power and efficiency, total allowed power loss can be calculated as $P_{loss}=P_{OUT}(1- \eta)/ \eta$. Since the total power loss is comprised of switching loss P_{SW} and conduction loss P_{cond}, a parameter α could be defined to represent the ratio of conduction loss to total loss. Thus $P_{cond}=P_{loss}*\alpha$, and $P_{SW}=P_{loss}*(1-\alpha)$. Here optimal value α=0.5 is usually used since in this condition the switching loss and conduction loss are balanced. Secondly, the conduction loss of the hybrid converter can be derived by using the circuit model in Figure 6-3, from which we have the equation $P_{cond}=V_{DE}*I_{OUT}+I_{OUT}^{2}*R_O$. Since conduction loss has already been known from efficiency, output impedance R_O is then calculated. After R_O is known, based on the DC circuit model in Figure 6-3, ideal voltage conversion ratio N is then obtained as

$N=(V_{OUT}+V_{DE}+I_{OUT}*R_O)/V_{IN}$. Assuming the hybrid converter is in continuous conduction mode, duty cycle of the switching clock is then calculated as $D_1=1-5/N$. For a selected switching frequency f_s and a selected inductor ripple ratio $\gamma=\Delta I_{IND}/I_{IND}$, inductor value could be obtained, which is $L=V_{IN}/\Delta I_{IND} *D_1T_s$. Here ΔI_{IND} is the peak to peak inductor current ripple, and I_{IND} is the average value. Their ratio γ is usually selected as 0.3 [82] for small inductor and little ac current loss. After L is known, its equivalent serial resistance could then be calculated as $R_{IND}=2\pi f_sL/Q$ where Q is the quality factor of the inductor L at frequency f_s.

Thirdly, as shown in equation (6-2), the output impedance is estimated using its slow and fast switching limit which represents capacitive loss at low frequency and resistive loss at high frequency respectively. Another parameter β could be utilized to split the conduction loss to $R_{OSSL}=R_O*\sqrt{\beta}$ and $R_{OFSL}=R_O*\sqrt{(1-\beta)}$. Optimal value of β is usually suggested as 0.5 [66]. When R_{OSSL} and R_{OFSL} are known, Lagrange optimization could be used to obtain the optimal size of each capacitor and switch by minimizing their total area [73]. Optimization results are then obtained as follows:

$$R_i = \frac{1}{\left(a_{ri}/\sqrt{d_{ri}}\right)\sum_j\left(a_{rj}/\sqrt{d_{rj}}\right)}\left(R_{OFSL}-\left(\frac{5}{1-D_1}\right)^2 R_{IND}\right) \tag{6-4a}$$

$$C_i = \frac{a_{ci}\sum_j a_{cj}}{R_{OSSL}f_s} \tag{6-4b}$$

where a_{ri}, a_{rj}, d_{ri}, d_{rj}, a_{ci}, and a_{cj} are the ith or j^{th} element of the vectors defined in table I.

After on-resistance of each switch and capacitance of each capacitor are obtained, SPICE simulation could be used to check the output voltage, output power, and

efficiency of the designed hybrid converter. If simulation results are off target, parameters such as α, β, γ, and f_S could be tweaked to optimize the converter design again following the procedure in Figure 6-5 until the simulation results are on target.

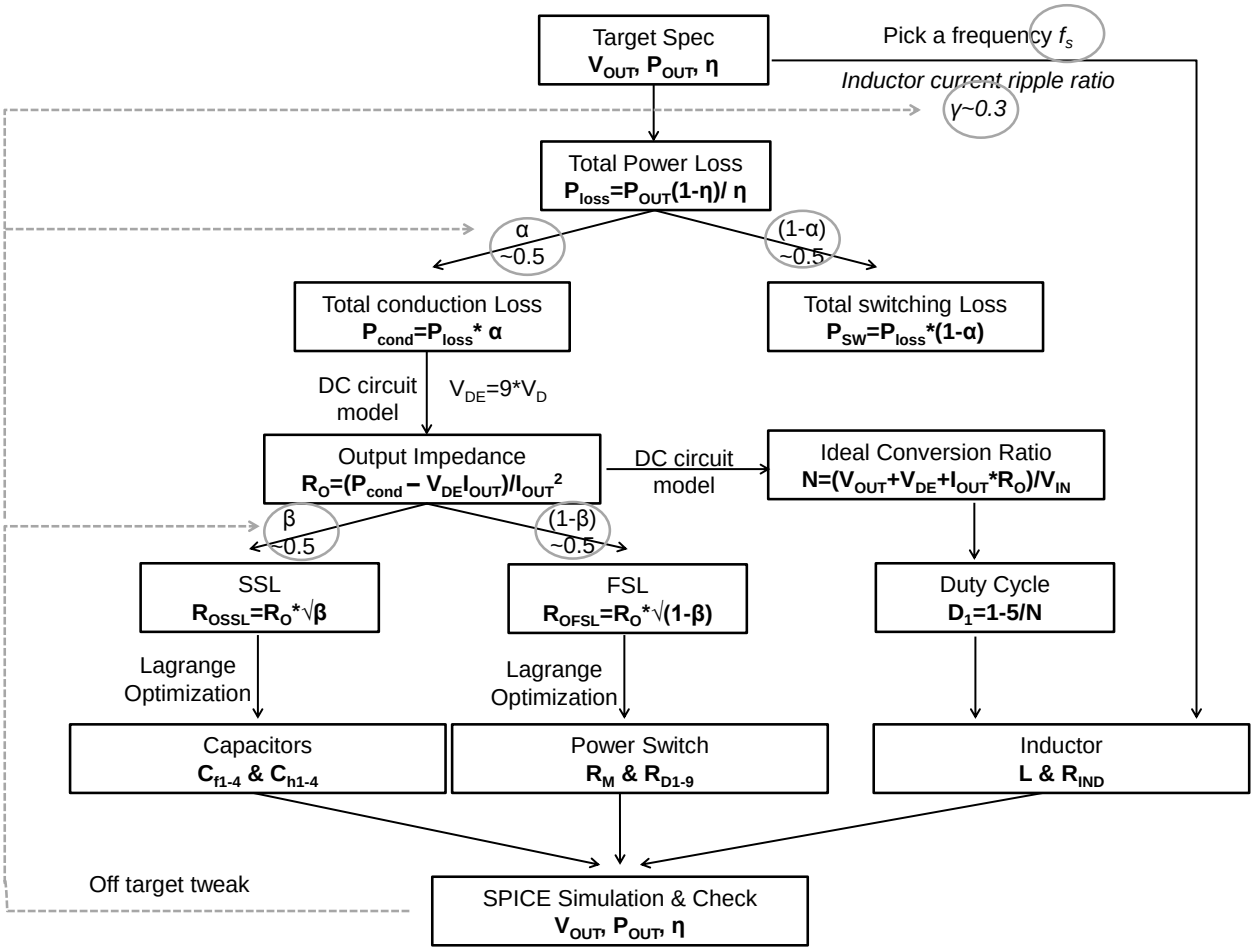


Figure 6-5. Optimal design procedure for the hybrid SI-SC step up converter.

6.3 Hysteretic Controller

The hybrid SI-SC step up converter could be regulated the same as the SI boost converter by controlling the duty cycle of its driving clock. Thus conventional voltage mode or current mode PWM control schemes [24] could be used. However, small signal analysis shows that the hybrid SI-SC converter, if operating in CCM, exhibits two poles and one right half plane (RHP) zero in its loop-gain transfer function. Appendix B and C show some analysis details. Stability frequency compensation has to compromise the

loop bandwidth to mitigate the influence of the RHP zero, thus resulting in slow transient response [83]. To overcome the drawback above, hysteretic control scheme could be employed, which as a nonlinear control method is advantageous in avoiding frequency compensation and achieving large bandwidth and fast transient response.

Hysteretic control has been widely used in switching buck converters [6][7]. However, most hysteretic controllers designed for buck converters could not be directly used for boost converters due to their very different loop characteristics. In buck converters, inductor current ripple is in phase with output voltage ripple, while in boost converters, the two ripples are out of phase. To resolve this difficulty, several hysteretic approaches which adopt extra control variables have been proposed [84][85] and demonstrated good transient response. However, adopted extra control variables introduce extra design complexity. In this chapter, a hysteretic controller that doesn't use any extra control variable is presented and designed for the hybrid SI-SC step-up converter. Compared to other approaches, the hysteretic controller is easier and simpler to design since no extra control variable is used. The switching on-time of the controller is fixed during transient response. Though it is not optimal, the constant on-time could keep inductor energy always under control so that no unpredicted large voltage stress during transient response will be seen on the specialized stacked NMOS switch to ensure lifetime requirement in real applications.

Details of the designed hysteretic controller with the SI stage of the hybrid converter are illustrated in Figure 6-6a. The hysteretic controller has two comparator loops, one for output voltage and one for inductor current. The first comparator loop consists of the resistor voltage divider R_{f1}, R_{f2} and the hysteretic comparator HC1. R_{f1},

R_{f2} sense the output and send the divided-down voltage V_{FB} to HC1. HC1 compares V_{FB} to V_{REF} and asserts signal EN whenever V_{FB} is smaller. The asserted signal EN then keeps the hybrid SI-SC converter constantly pumping energy to the output until HC1 de-asserts it. The second comparator loop includes the lossless inductor current sensing network R_1, C_1, R_2, C_2 and hysteretic comparator HC2 to regulate inductor current. As shown in Figure 6-6a, R_1, C_1, as a pseudo-integrator, sense the inductor current I_{IND} and create a voltage in proportion to I_{IND} with inverted polarity, which is then coupled to sense node V_S through high-pass filter C_2, R_2. R_2C_2 is ~$100 \cdot R_1C_1$. V_{BL} and V_{BH} are bias voltages conditioned through a start-up circuit with V_{BL} setting the center of HC2 hysteretic window V_H. V_{BH} is set slightly higher than the hysteretic window of HC2 to make sure the low side NMOS will be always turned on whenever signal EN is asserted.

To better illustrate the working principle of the hysteretic controller, sample waveforms during start up and in steady state are shown in Figure 6-6b. When the hybrid converter is initially turned on, V_{FB} is below V_{REF} and EN is high. To avoid large inrush inductor current, V_{BL} is initially set higher than V_{BH} so that I_{IND} remains zero until the start-up sequence ends with V_{BH} crossing the top of the hysteretic window of HC2. The conditioning circuit for this purpose is shown in Figure 6-7a which generates the rising V_{BH} and the falling V_{BL} during start up. V_{BHDC} and V_{BLDC} are bias voltages that V_{BH} and V_{BL} will settle at after start up. Then sensing voltage V_S inversely changes with I_{IND} until V_S hits the limits of the hysteretic window. CKS toggles and keeps the hybrid converter continuously pumping energy to output until V_{OUT} reaches the target. During this process, the slope of V_S and hysteretic window V_H of HC2 together determine the on-time of the driving clock which is expressed as $t_{on}=V_H/V_{IN}*R_1C_1$. Since V_{IN}, V_H, R_1, C_1

are fixed, t_{on} is nearly constant. After EN is low, the controller stays idle and V_S drifts to V_{BH} until V_{OUT} hits the lower hysteretic window of HC1 and asserts EN. Moreover, to improve the testing capability of the controller, a MUX is added to allow for bypassing with external clock CLK_E. A serial interface is also included to digitally program C_1, R_2, and hysteretic windows of HC1 and HC2 for flexibility.

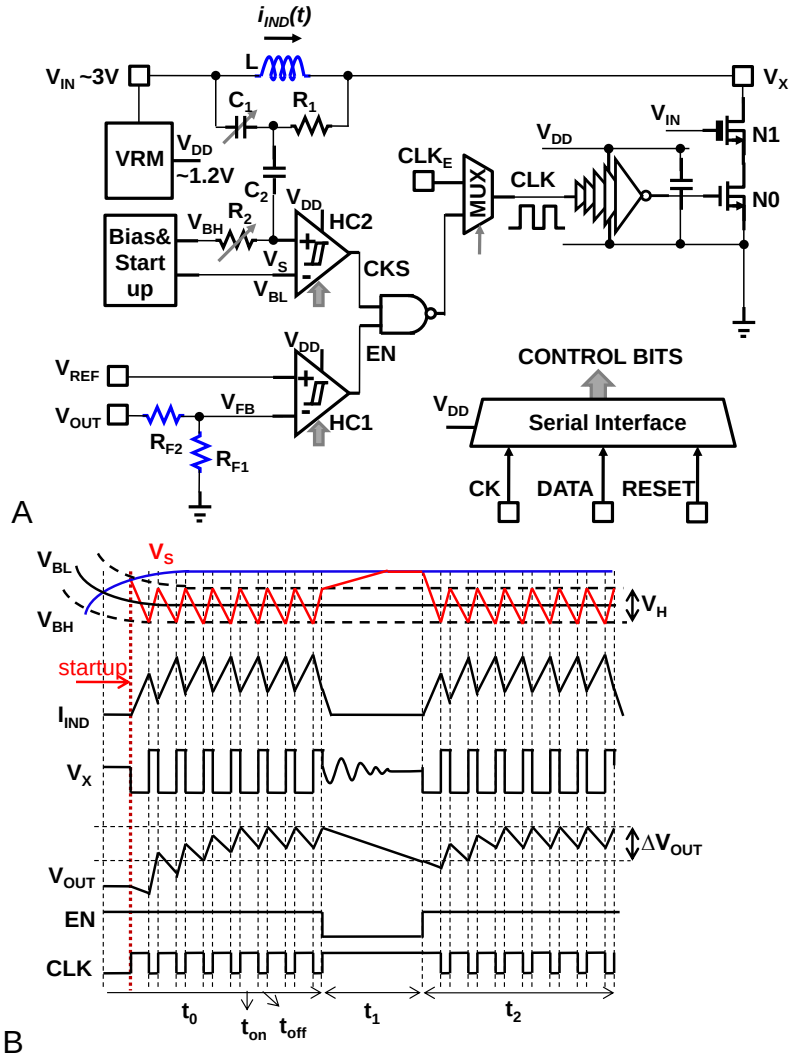


Figure 6-6. Hysteretic controller designed for the hybrid SI-SC step up converter and its sample waveforms. A) Block diagram of the hysteretic controller, B) sample waveforms.

Figure 6-7b shows the design of the hysteretic comparator shared by HC1 and HC2. It consists of a pre-amplification stage, a cross-gate decision stage with

hysteresis, and an output stage, all realized using 1.2V high speed devices. The preamplifier uses both NMOS and PMOS input pairs to achieve rail-to-rail input voltage range. In the decision stage, NMOS pairs M1/M3 and M2/M4 use cross-gate connection to realize positive feedback and hysteresis. By adjusting the size ratio of these pairs, hysteresis window V_H could be programmed and five digital bits are employed for this purpose. DC simulation shows the maximum hysteresis window is ~100mV and the program step is ~3mV. Quiescent current of the comparator is ~350 µA and transient simulation shows the delay is ~1ns.

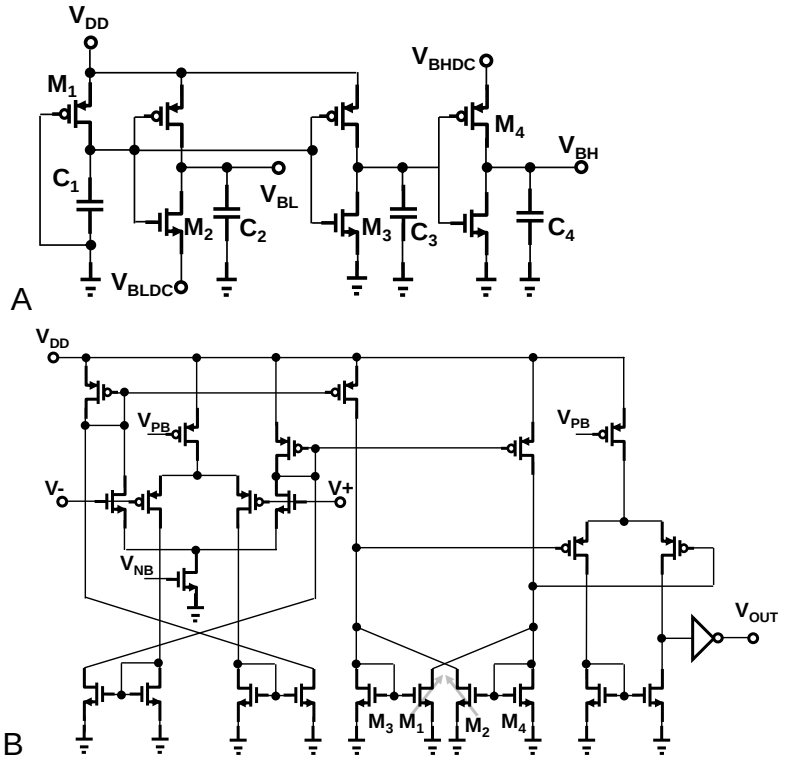


Figure 6-7. Conditioning circuit for V_{BL} and V_{BH} and hysteretic comparator with programmable window. A) Conditioning circuit, B) Hysteretic comparator.

An onchip voltage regulator is also included in this controller design to generate an internal 1.2V supply from the 3V input for powering the two comparators and control logics. Figure 6-8 shows its schematic [86], which is composed of a high-slew-rate error amplifier and a pass PMOS. The pass PMOS is a thick oxide transistor with a size of

20µm/0.34µm. The error amplifier employs two common gate differential input pairs M1/M2 and M3/M4 with bias currents (I_{bias}) set as 5µA. Two 4x current mirrors then sum the input differential current at the output as a push-pull stage. Since the slew rate is not limited by the bias current, very fast slew rate is achieved with low quiescent current. Simulation shows the error amplifier has a total quiescent current of ~50µA. And loop bandwidth of the regulator is ~20MHz and phase margin is 45 degree.

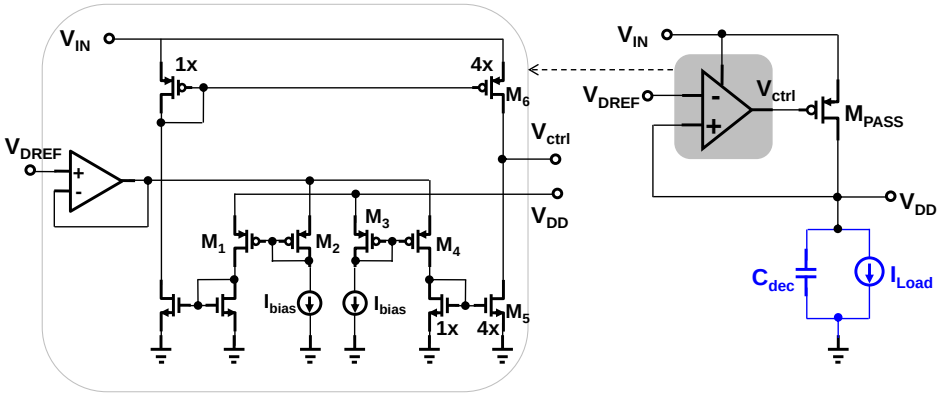


Figure 6-8. Onchip linear regulator to generate internal power supply for the controller.

6.4 Experimental Results

The hysteretic controlled hybrid SI-SC step up converter was fabricated in a standard 1.2V 130nm CMOS process as two chips. As shown in Figure 6-9, the first chip integrates the hysteretic controller and the stacked NMOS switch together with a size of 1.2mm x 1mm, and the second one contains the 4-stage SC multiplier with a size of 1.2mm x 2.4mm. Measurement shows that parasitic substrate junction in the SC multiplier has a breakdown voltage of ~10V. To generate output greater than 10V, a post process step was employed to create three substrate isolation trenches inside the SC multiplier. Four isolated islands were then formed inside the second chip and wire bonding was used to connect them. After the post process step, both chips were mounted onto a testing board directly without using any packages to minimize footprint.

Wire bonding was used again to connect the I/O pads of the silicon dies to the PCB board. Other discrete components such as inductor, feedback resistors, and decoupling capacitors are also mounted onto the same board using solder paste as shown in Figure 6-9.

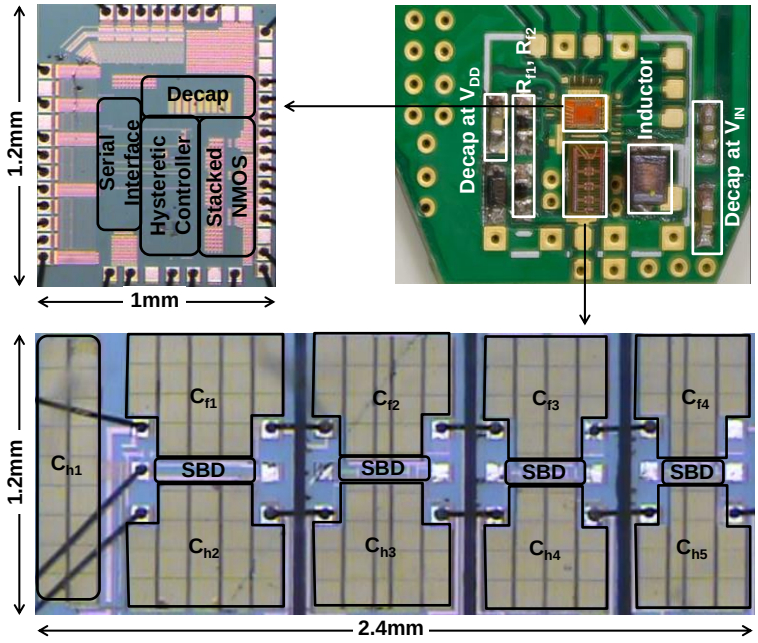


Figure 6-9. Testing board for the hybrid SI-SC step up converter and zoomed-in die photos of the hysteretic controller with stacked NMOS switch and the SC multiplier.

The hybrid SI-SC step up converter was firstly evaluated with the hysteretic controller bypassed. External switching clocks of 50MHz, 25MHz, and 12.5MHz with duty cycle of D=0.5 were explicitly selected to drive the hybrid converter with V_{IN}=3V when three chip inductors L=390nH, 1µH, 2.7µH were consecutively employed. These testing parameter combinations were chosen for achieving maximal output voltage for the hybrid converter. Measured output voltage and power efficiency are plotted in Figure 6-10. As shown in Figure 6-10a, when load resistance increases from 10kΩ to 500kΩ, the hybrid converter achieves a maximal output voltage of ~35V for all testing cases. In Figure 6-10b, the peak power efficiency for L=390nH and f_S=50MHz is the lowest,

~33%, while for L=2.7μH and f_S=12.5MHz, the peak efficiency is ~45%. Though the efficiency difference is ~12%, the latter inductor is 7x larger. Considering the tradeoff between inductor size and power efficiency, L=1μH and f_S=25MHz is the best.

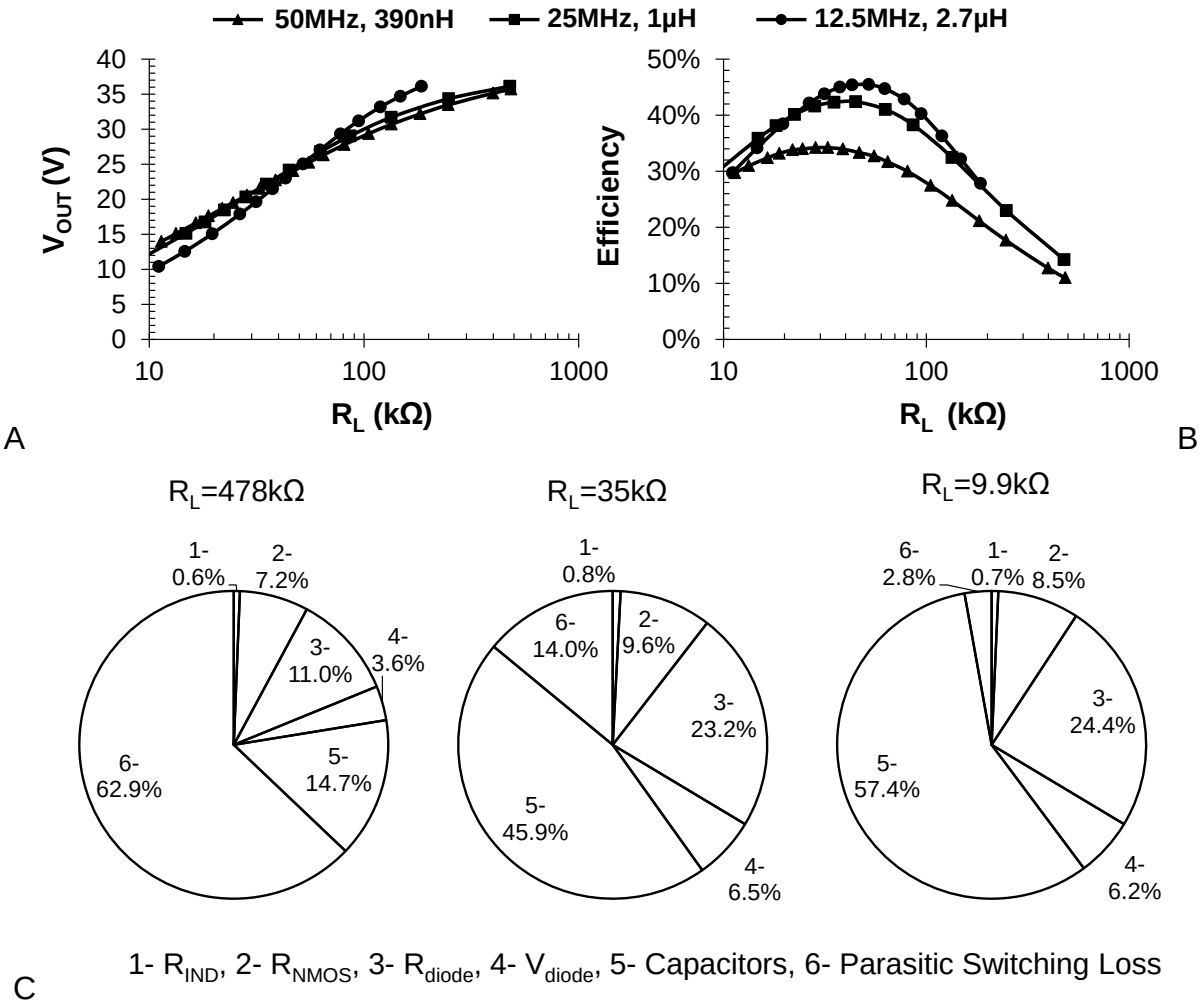
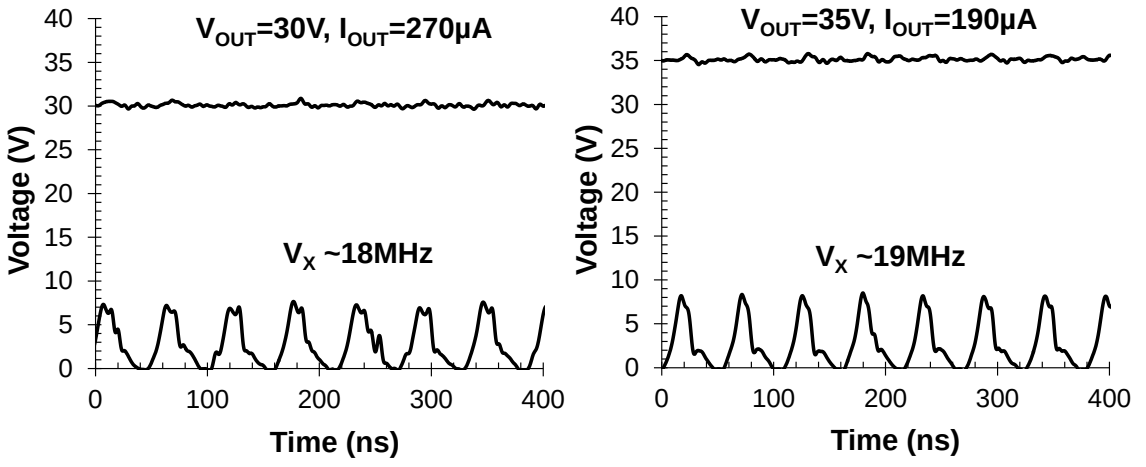


Figure 6-10. Open loop measurement results with D=0.5 and V_{IN}=3V and power loss distribution when f_S=25MHz and L=1μH. A) Measured output voltage, B) Power efficiency, C) Power loss distribution.

To better understand the performance of the hybrid converter, a power loss distribution for the testing case with L=1μH and f_S=25MHz was done and illustrated in Figure 6-10c. The total power loss are broken down through simulation and analysis as six parts including inductor resistive loss, NMOS on-resistance loss, diode on-resistance loss, diode turn-on voltage loss, charging and discharging loss of capacitors in SC

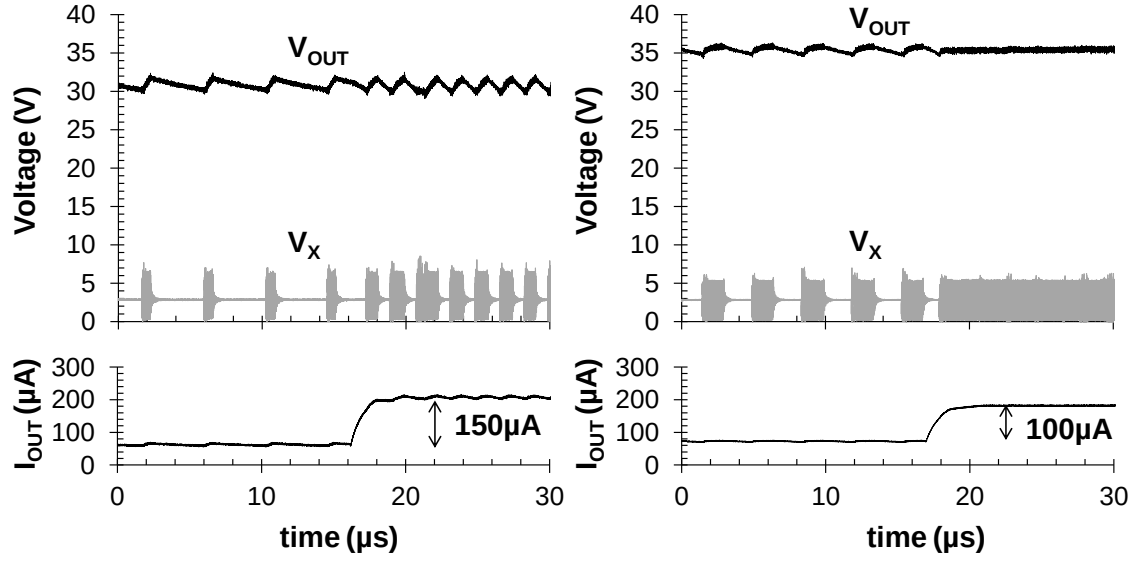
multiplier, and parasitic capacitive switching loss. When load resistance R_L=478kΩ, the hybrid converter achieves the maximal output voltage, but 62.9% of total power loss is due to parasitic switching loss. When R_L=35kΩ, the hybrid converter has the best power efficiency of 43% with an output voltage of 24V. In this condition, 45.9% of total power loss is due to charging and discharging loss of capacitors in SC multiplier. From these pie charts, we could see that, in order to improve power efficiency at large output voltages, utilizing lower switching frequency or larger capacitors in SC multiplier could be used. However, low switching frequency requires large inductor value and large capacitors will consume too much silicon dies. Therefore, later measurements will continue using the testing setup with L=1µH and f_s~25MHz.

Close loop testing results of the hybrid step up converter with its hysteretic controller enabled are plotted in Figure 6-11-13. All results were obtained with L=1µH and V_{IN}=3V. Shown in Figure 6-11 are measured timing waveforms of the output and the switching voltage at node V_X which connects the SI stage and the SC multiplier as shown in Figure 6-2. Figure 6-11a shows when output is 30V with a maximal load current of 270µA, peak voltage at V_X is ~7V and the close loop switching frequency is ~18MHz. When the output increases to 35V, maximal output current decreases to 190 µA. And measured timing waveforms in Figure 6-11b show that peak voltage at V_X increases to ~8V with a switching frequency of ~19MHz. Moreover, analysis and measurement show that peak voltage at node V_X should be kept no greater than ~8.5V to avoid time dependent dielectric breakdown and hot carrier effects on those specialized high voltage tolerant devices. When peak voltage at V_X is >8.5V, device life time might be reduced, or permanent damage may be observed.



A B

Figure 6-11. Measured close loop timing waveforms when the hybrid SI-SC converter is tested with L=1µH and V_{IN}=3V. A) V_{OUT}=30V and I_{OUT}=270µA, B) V_{OUT}=35V and I_{OUT}=190µA.



A B

Figure 6-12. Measured timing waveforms of the hybrid step up converter for positive load transient response with L=1µH and V_{IN}=3V. A) V_{OUT}=30V, B) V_{OUT}=35V.

Shown in Figure 6-12 are measured timing waveforms of the hybrid step up converter when positive 50% load step occurs for 30V and 35V outputs. These waveforms demonstrate that the hysteretic controller is stable and could respond to load step immediately by pumping more energy to the output to keep V_{OUT} of the hybrid converter within spec. Transient response for negative 50% load step was also captured but not plotted here since the response is slow due to the hybrid converter could not

sink current from the output. Moreover, Figure 6-13 plots the output waveform of the hybrid step up converter with a modulated reference when a pseudo piezo actuator load of 1MΩ and 100pF is used. For a step reference, the hybrid converter reaches 15V output at 0.9µs and 35V at 15µs. For a sine or triangular reference, the output follows V_{REF} to generate 500Hz sineish and triangular waves. Figure 6-13 demonstrates that the hybrid converter successfully generates 35V 500Hz driving voltage for the pseudo piezo actuator.

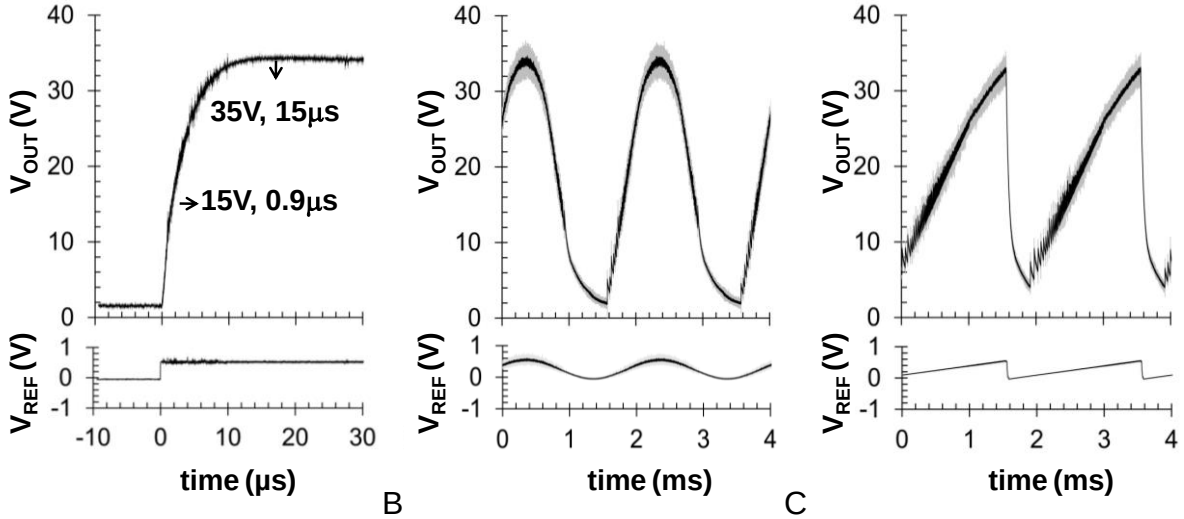


Figure 6-13. Measured timing waveforms with a pseudo piezo load of 1MΩ and 100pF when the reference is modulated. A) Step, B) 500Hz sine, C) 500Hz triangular wave.

6.5 Preliminary Demo of a Smart Piezoelectric Microsystem

The miniature high voltage hybrid power converter was employed with a commercial microprocessor (TI MSP430L092) to form a smart piezoelectric microsystem as a preliminary demo for driving a resonant piezoelectric fan (#RFN1-005). Figure 6-14a shows a picture of the demo which consists of a laptop, a custom power supply board, a TI microprocessor, a high voltage hybrid step up converter, and a resonant piezo fan. The laptop provides both power and communication signals via a USB interface to the whole microsystem. Since the USB voltage is 5V, a custom power

supply board was designed using commercial voltage regulators to generate 3V and 1.2V supplies for powering the hybrid step up converter and the microprocessor respectively. The low voltage microprocessor then generates specific configuring sequences (CLK, DAT) and a voltage reference (VREF) to control and program the high voltage hybrid step up converter for creating large driving signals for the resonant piezo fan. Appendix D shows the code that could be loaded in IAR software to generate the required sequences (CLK, DAT, VREF). Here TI MSP430L092 was selected since it uses a supply of 1.2V and could be potentially integrated with the hybrid power converter on the same die using the standard 1.2V CMOS process. Moreover, the hybrid power converter and the piezo fan were mounted together inside a black box for easy measurement and protection from hazardous damage. In the end of the piezo fan, a custom wing was also attached for visual demonstration and its resonant frequency was measured as ~25Hz.

The high voltage hybrid power converter and the microprocessor were programmed to generate 35V 25Hz driving signals. After the microsystem was enabled, real time displacement of the custom wing was measured using a laser displacement sensor and the testing results are plotted in Figure 6-14b. It shows that peak output voltage of the hybrid power converter is ~35V and the piezo fan resonates at 25Hz with a maximum displacement of 1.5mm. One more thing to be mentioned here is that the output voltage waveform has a very slow falling slope since the hybrid step up converter could not sink current for its load. Therefore, when a high frequency actuator with a large load capacitance is needed to be driven, a DC-AC inverter has to be inserted between the hybrid step up converter and the actuator to generate accurate AC driving

waveforms [87]. The preliminary demo shown in this section is only applicable to low frequency actuators due to the slow falling slope.

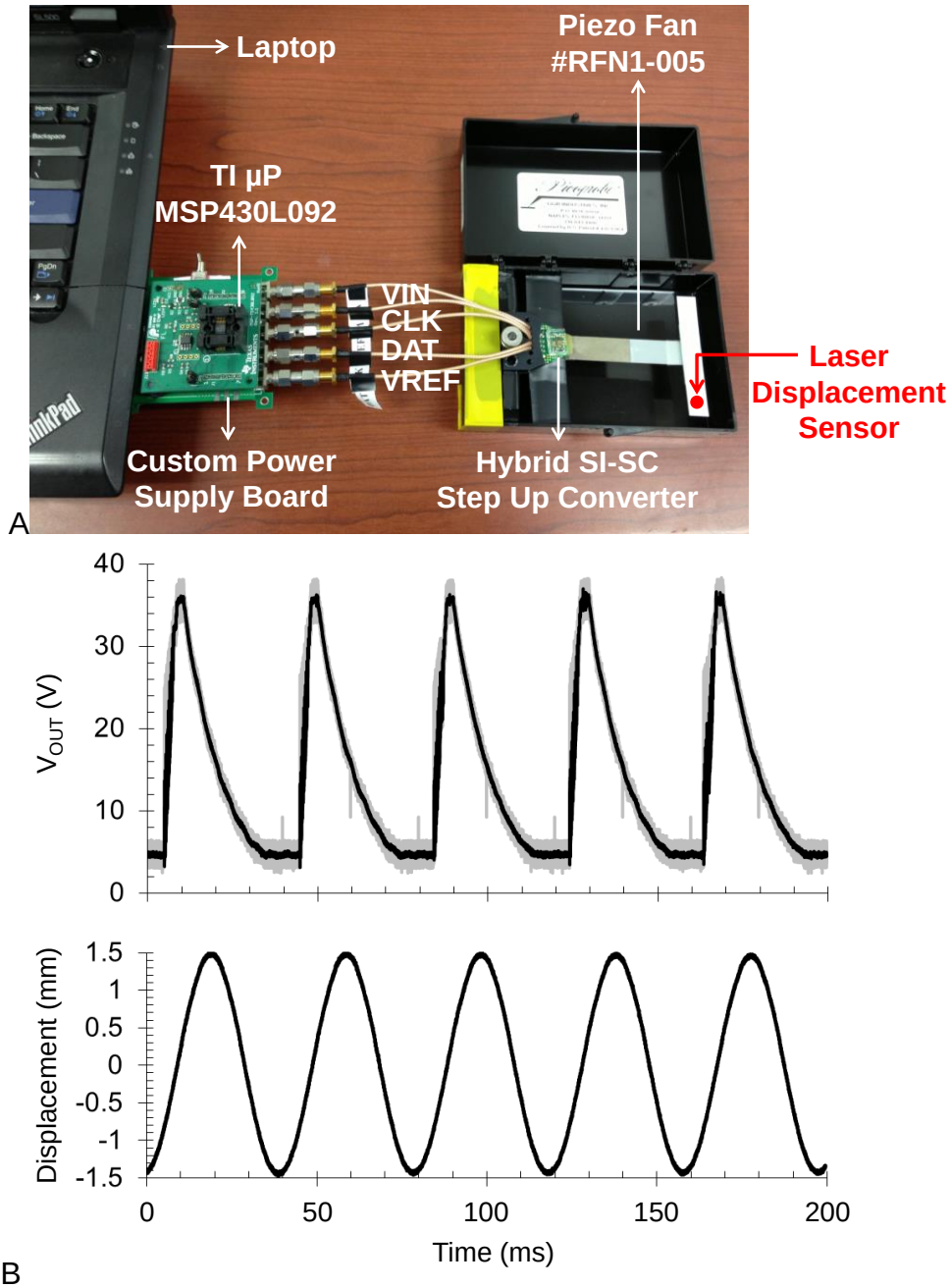


Figure 6-14. A smart piezoelectric microsystem using the hybrid SI-SC step up converter and a commercial MSP and measurement results. A) Microsystem photo, B) Measurement results.

CHAPTER 7
CONCLUSIONS AND FUTURE WORKS

7.1 Research Summary and Contributions

The focus of this dissertation is on highly-integrated switching mode step-up DC-DC converters in advanced CMOS processes for portable devices and microsystem applications. These applications have strict design requirements, such as large voltage conversion ratio, miniaturized footprint, light weight, and high power density. Utilizing the fine feature size in advanced CMOS processes, step up voltage converters could be miniaturized. Additionally, advanced CMOS processes allow integrating those step-up voltage converters with digital signal processing and RF communication circuits on a single die, thus enabling an extremely small electronic solution for portable or microsystem applications.

Implementing step up voltage converters in advanced CMOS processes introduces design challenges on device reliability and system performance, which are investigated in different chapters through this dissertation. Device reliability issue is dealt with by developing specialized device structures in chapter 3 and utilizing hybrid topology techniques in chapter 4. The first contribution is that three high voltage tolerant power devices, namely schottky barrier diodes (SBD), stacked NMOS switches, and extended-drain MOS devices are developed in a standard 1.2V 130nm CMOS process without adding any masking steps. These specialized devices extend the maximum block voltage to be 2-3X larger than the standard thick-oxide devices in the process.

The second contribution is that this dissertation evaluates two 50-100MHz hybrid step-up converter topologies, namely hybrid switched inductor (SI) switched capacitor

(SC) and hybrid SI-flyback converter, in the standard 1.2V 130nm CMOS process. These two hybrid topologies are able to distribute large voltage stress across many of constituent devices to mitigate the device reliability concern. Experimental results show that by using specialized high voltage tolerant devices and a 24nH commercial air-core inductor (Q=30@100MHz), the SI-SC converter achieves a maximum output of 10V from 1.2V input and a maximum efficiency of 42% at 1.9mA of load current for a 7V output. The hybrid SI-flyback converter was tested at 100MHz with a commercial transformer (25nH/200nH). It achieves a peak efficiency of 57% for a 4.3mA load current and 7V output. Moreover, a micro-fabrication technique is also demonstrated to further reduce the sizes of passive components. Custom high-inductance-density air-core inductors and transformers were fabricated and employed with these two hybrid converters in measurements. Experimental results show that compared to commercial counterparts, the micro-fabricated components achieve comparable performance with much smaller footprints.

To deal with the performance concern of step up voltage converters, a general circuit model is proposed in chapter 5 for performance analysis of hybrid SI-SC step up converters, which is the third contribution of this dissertation. The proposed circuit model uses a theoretic network methodology to evaluate the output impedance and account for various sources of switching loss prevalent at high operating frequencies and in on-chip implementations. Unlike previous approaches, this approach divides dynamic switching loss into output-unrelated (i.e. gate-drive loss) and output-related (i.e. capacitive loss of diodes). It then uses two equivalent input and output resistive loads to model them separately. Comparisons with SPICE simulations and experimental

results demonstrate that for the three specific hybrid converters examined in chapter 5, the proposed approach is accurate for evaluating the power efficiency and the output regulation as a function of load.

A complete hybrid SI-SC step up converter with a hysteretic controller and an internal voltage regulator is demonstrated in a 1.2V CMOS process with minimal post-process steps. An optimal design procedure based on theoretic network analysis is also presented to minimize design cost. Experimental results show that the fabricated hybrid converter generates output voltage up to 35V from a 3V input. Moreover, the hybrid converter is employed with a commercial microprocessor to form a preliminary demo as a smart piezoelectric microsystem which successfully drives a 25Hz piezo fan.

7.2 Future Works

This dissertation has explored some high frequency (10-100MHz) step-up voltage converters in a standard 1.2V 130nm CMOS process. Maximum output voltages of 10V and 35V have been demonstrated with commercial and micro-fabricated passives without and with extra post-process steps.

A potential research direction is using the hybrid SI-SC converter to achieve an even larger output voltage with better performance for autonomous microsystems. The hybrid SI-SC converter is one of the best solutions since device voltage stress is equally distributed and the output voltage can be increased without adding more voltage stress on power devices. One possible direction is using a SOI process which eliminates the N-well-to-substrate junction. Another possible direction is using microfabrication techniques to isolate the high voltage N-wells. Possible techniques include back-side etching to remove the substrate in selected regions. With all these techniques, >35V

output voltages or even higher can be achieved in the standard 1.2V CMOS process for driving piezoelectric actuators.

APPENDIX A
D_2 DERIVATION FOR SI AND HYBRID SI-SC CONVERTER IN DCM

A.1 Derivation of D_2 for SI Step-Up Converter in DCM

For a non-ideal SI step-up converter, when calculating the current and voltage across the inductor, the on-resistances of the switch and diode have to be considered. With the aid of the current and voltage waveforms depicted in Figure A-1, the peak-to-peak inductor current ripple ΔI_{IND} can be derived as follows.

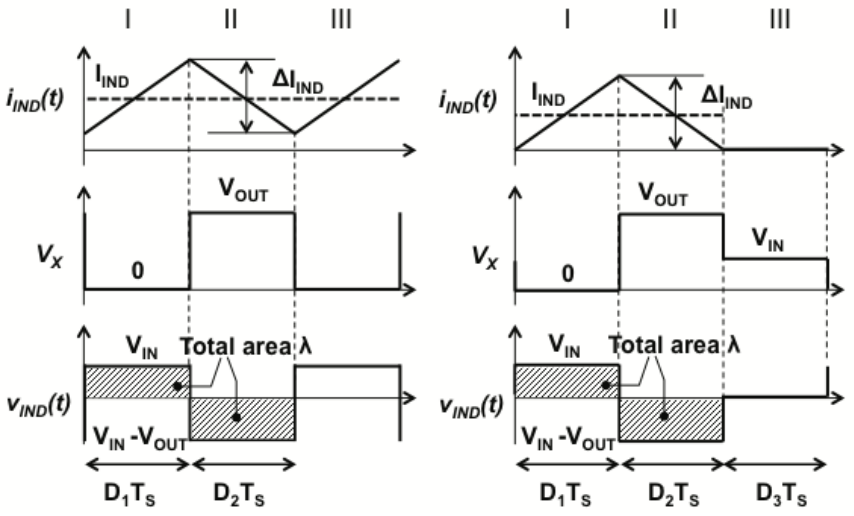


Figure A-1. Representative waveforms of the SI step-up converter. A) CCM, B) DCM.

In subinterval I,

$$\Delta I_{IND} = \frac{V_{IN} - 0.5\Delta I_{IND}\left(R_{IND} + R_N\right)}{L} D_1 T_S \tag{A-1}$$

and in subinterval II,

$$\Delta I_{IND} = \frac{V_{OUT} + V_{D1} + 0.5\Delta I_{IND}\left(R_{IND} + R_{D1}\right) - V_{IN}}{L} D_2 T_S \tag{A-2}$$

The total charge supplied to the load during one period Q is given by

$$Q = \frac{1}{2}\Delta I_{IND} D_2 T_S \tag{A-3}$$

and the output voltage V_{OUT} is

$$V_{OUT} = \frac{Q}{T_S} R_L \tag{A-4}$$

To solve for D_2, we first substitute (A-3) into (A-4) and the resulting V_{OUT} expression is substituted back into (A-2). Then we solve for ΔI_{IND} in (A-1) and substitute into (A-2) to obtain

$$\frac{D_1}{K}(D_2)^2 - D_2 B - D_1 = 0 \tag{A-5}$$

Solving (A-5) for D_2 yields

$$D_2 = \frac{B + \sqrt{B^2 + 4D_1^2 / K}}{2D_1 / K} \tag{A-6}$$

where

$$B = \left(1 - \frac{V_{D1}}{V_{IN}}\right)\left(1 + \frac{(R_{IND} + R_N)DT_S}{2L}\right) - \frac{(R_{IND} + R_{D1})DT_S}{2L} \tag{A-7}$$

and

$$K = \frac{2L}{R_L T_S} \tag{A-8}$$

In DCM, $D_2 \leq (1\text{-}D_1)$ and $K \leq D_1(1\text{-}D_1)^2$.

A.2 Derivation of D_2 for Hybrid SI-SC Converter (N_{SC}-Stage)

The SI/SC converter can be viewed as a SI converter cascaded with a SC converter, as shown in Figure A-2. The effective load of the SI stage is R_L+R_{OSC}, where R_{OSC} is the equivalent output resistance of the SC stage. Applying the same derivation procedure as in Appendix A1 to the hybrid SI/SC step-up converter, D_2 in DCM can be expressed as

$$D_2 = \frac{B_m + \sqrt{B_m{}^2 + 4D_1^2 / K_m}}{2D_1 / K_m} \tag{A-9}$$

where

$$B_m = \left(1 - \frac{V_{DE}}{N_{SC} V_{IN}}\right)\left(1 + \frac{(R_{IND} + R_N) D T_S}{2L}\right) - \frac{R_{IND} D T_S}{2L} \tag{A-10}$$

and

$$K_m = \frac{2L N_{SC}^{\ 2}}{(R_L + R_{OSC}) T_S} \tag{A-11}$$

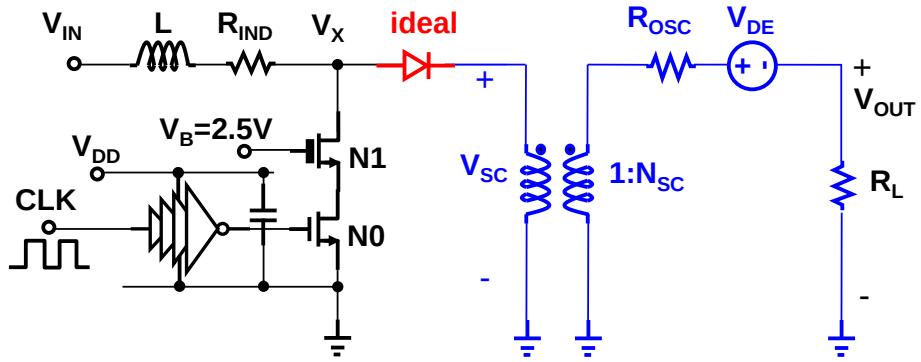


Figure A-2. Simplified circuit model for the hybrid SI/SC step-up converter.

APPENDIX B
SMALL SIGNAL AC ANALYSIS FOR SI BOOST IN CCM

The configuration of a SI boost under investigation is shown in Figure B-1. To apply state-space averaging to this topology, only parasitic resistances are considered. Derived results based on the above assumption will apply when the converter is highly efficient where capacitive switching losses are insignificant.

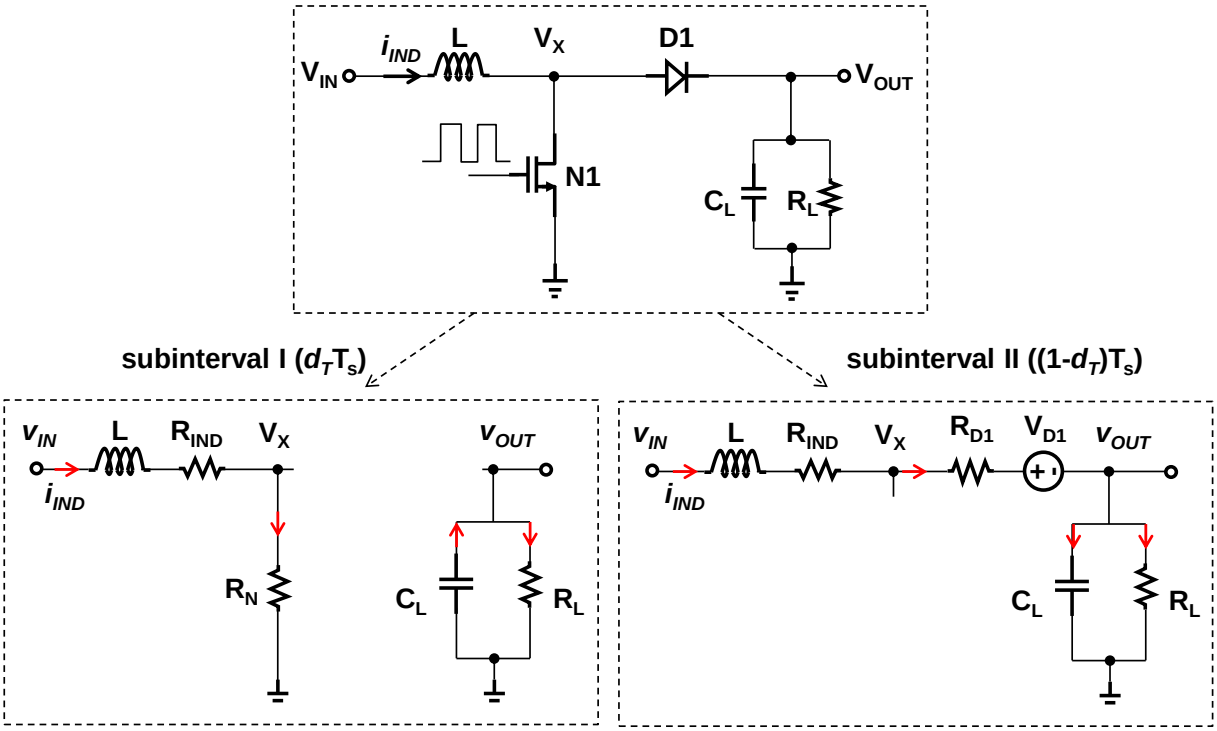


Figure B-1. The configuration of a SI boost converter and equivalent circuits in subinterval I and II when operating in CCM.

In subinterval I ($0 \le t \le d_T T_s$),

$$L\frac{di_{IND}}{dt} = v_{IN} - i_{IND}\left(R_{IND} + R_N\right) \tag{C-1}$$

$$C_L\frac{dv_{OUT}}{dt} = -\frac{v_{OUT}}{R_L} \tag{C-2}$$

In subinterval II ($d_T T_s \le t \le T_s$),

$$L\frac{di_{IND}}{dt} = v_{IN} - v_{OUT} - V_D - i_{IND}\left(R_{IND} + R_D\right) \tag{C-3}$$

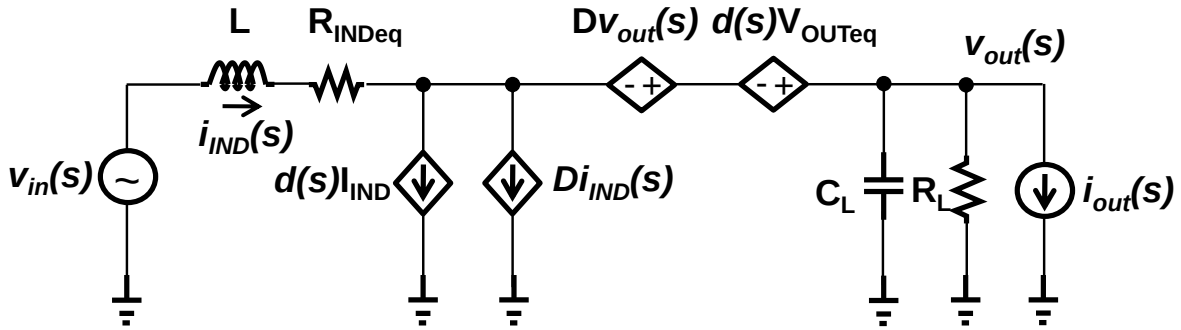
$$C_L \frac{dv_{OUT}}{dt} = i_{IND} - \frac{v_{OUT}}{R_L} \tag{C-4}$$

Through state-space averaging, we have equations

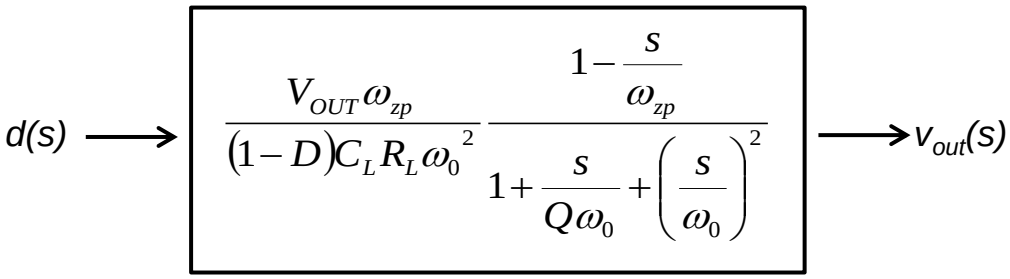
$$L\frac{di_{IND}}{dt} = d_T\left(v_{IN} - i_{IND}\left(R_{IND} + R_N\right)\right) + \left(1-d_T\right)\left(v_{IN} - v_{OUT} - V_D - i_{IND}\left(R_{IND} + R_D\right)\right)$$

$$= v_{IN} - \left(1-d_T\right)\left(v_{OUT} + V_D\right) - i_{IND}\left(R_{IND} + d_T R_N + \left(1-d_T\right)R_D\right) \tag{C-5}$$

$$C_L \frac{dv_{OUT}}{dt} = -d_T \frac{v_{OUT}}{R_L} + \left(1-d_T\right)\left(i_{IND} - \frac{v_{OUT}}{R_L}\right) = -\frac{v_{OUT}}{R_L} + \left(1-d_T\right)i_{IND} \tag{C-6}$$



A



B

Figure B-2. Small signal circuit model and duty-to-output transfer function for the SI boost in CCM. A) Small signal circuit model, B) duty-to-output transfer function.

Assuming small low-frequency perturbations as

$$v_{IN} = V_{IN} + v_{in}$$

$$v_{OUT} = V_{OUT} + v_{out}$$

$$i_{IND} = I_{IND} + i_{ind}$$

$$d_T = D + d$$

and ignoring higher-order terms, DC and low-frequency AC equations can be obtained.

$$\begin{cases} 0 = V_{IN} - (1-D)(V_{OUT} + V_D) - I_{IND} R_{INDeq} \\ 0 = -\dfrac{V_{OUT}}{R_L} + (1-D) I_{IND} \end{cases} \tag{C-7}$$

$$\begin{cases} L \dfrac{di_{ind}}{dt} = v_{in} - (1-D) v_{out} + dV_{OUTeq} - i_{ind} R_{INDeq} \\ C_L \dfrac{dv_{out}}{dt} = -\dfrac{v_{out}}{R_L} + (1-D) i_{ind} - dI_{IND} \end{cases} \tag{C-8}$$

where $R_{INDeq}=R_{IND}+D\cdot R_N+(1-D)\cdot R_D$, $V_{OUTeq}=V_{OUT}+V_D-I_{IND}(R_N-R_D)$.

From C-8, a small signal circuit model for the SI boost converter in CCM is derived and illustrated in Figure B-2. From the derived small signal circuit model, duty-to-output transfer function T_p can be derived which is also shown in Figure B-2.

$$T_p = \frac{V_{OUT}\omega_{zp}}{(1-D) C_L R_L \omega_0^{\,2}} \frac{1 - \dfrac{s}{\omega_{zp}}}{1 + \dfrac{s}{Q\omega_0} + \left(\dfrac{s}{\omega_0}\right)^2} \tag{C-9}$$

The right-half-plane zero is

$$\omega_{zp} = \frac{\dfrac{V_{OUTeq}}{V_{OUT}} R_L (1-D)^2 - R_{INDeq}}{L} \approx \frac{R_L (1-D)^2 - R_{INDeq}}{L} \tag{C-10}$$

The corner frequency is

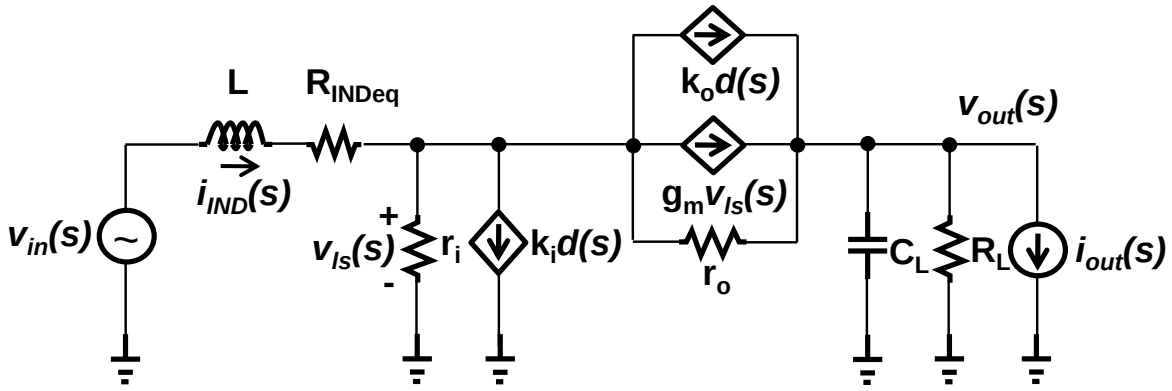
$$\omega_0 = \sqrt{\frac{R_{INDeq} + R_L (1-D)^2}{C_L R_L L}} \tag{C-11}$$

The quality factor is

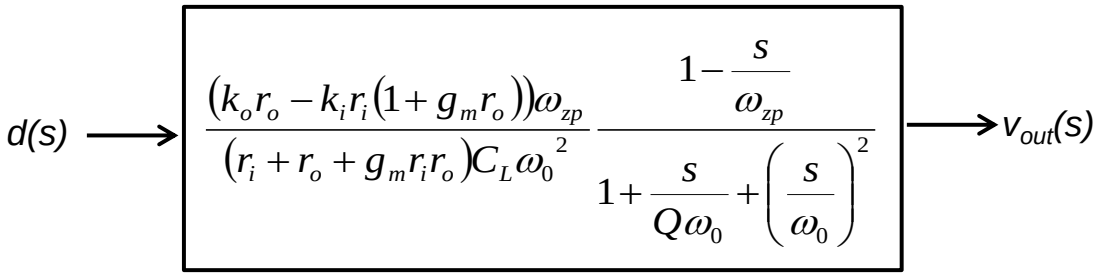
$$Q = \frac{\sqrt{\left(R_{INDeq} + R_L (1-D)^2\right) C_L R_L L}}{L + C_L R_L R_{INDeq}} \tag{C-12}$$

APPENDIX C
SMALL SIGNAL AC ANALYSIS FOR SI BOOST IN DCM

Averaged switch model in DCM has been derived and described clearly in [x]. Here the derived model is applied to the SI boost, resulting in a small-signal circuit model as shown in Figure C-1.



A



B

Figure C-1. Derived small-signal circuit model and duty-to-output transfer function for the SI boost in DCM. A) Small signal circuit model, B) Duty-to-output transfer function.

Parameters used in Figure C-1 are detailed as follows.

$$R_{INDeq} = \frac{4\mu}{3D}\left(\mu R_N + R_{IND} + R_D\frac{\mu-1}{\mu}\right) \quad \text{(in DCM)} \tag{D-1}$$

$$r_i = \frac{2 f_s L}{D^2} \tag{D-2}$$

$$k_i = \frac{D\left(V_{IN} - R_{INDeq} I_{IND}\right)}{f_s L} \tag{D-3}$$

$$g_m = \frac{D^2\left(V_{IN} - R_{INDeq} I_{IND}\right)}{f_s L\left(V_{OUT} - V_{IN} + R_{INDeq} I_{IND} - V_D(1-\mu)\right)} \tag{D-4}$$

$$k_o = \frac{D\left(V_{IN} - R_{INDeq} I_{IND}\right)^2}{f_s L\left(V_{OUT} - V_{IN} + R_{INDeq} I_{IND} - V_D\left(1-\mu\right)\right)} \tag{D-5}$$

$$r_o = \frac{2 f_s L\left(V_{OUT} - V_{IN} + R_{INDeq} I_{IND} - V_D\left(1-\mu\right)\right)^2}{D\left(V_{IN} - R_{INDeq} I_{IND}\right)^2} \tag{D-6}$$

$$\mu = \frac{D}{D + D_2} = 1 - \frac{1}{2}\frac{V_{IN}}{V_{OUT} + V_D}\left(1 - \sqrt{1 - \frac{4R_{INDeq}}{R_L}\frac{V_{OUT}\left(V_{OUT} + V_D\right)}{{V_{IN}}^2}}\right) \tag{D-7}$$

Figure C-1b shows the duty-to-output transfer function, which includes a possible RHP zero and two poles.

$$T_p = \frac{\left(k_o r_o - k_i r_i\left(1 + g_m r_o\right)\right)\omega_{zp}}{\left(r_i + r_o + g_m r_i r_o\right) C_L {\omega_0}^2} \frac{1 - \dfrac{s}{\omega_{zp}}}{1 + \dfrac{s}{Q\omega_0} + \left(\dfrac{s}{\omega_0}\right)^2} \tag{D-10}$$

$$\omega_{zp} = \frac{k_o r_o\left(R_{INDeq} + r_i\right) - k_i R_{INDeq} r_i\left(1 + g_m r_o\right)}{L\left(k_i r_i\left(1 + g_m r_o\right) - k_o r_o\right)} \tag{D-11}$$

$$\omega_0 = \sqrt{\frac{R_L\left(R_{INDeq} + r_i\right) + R_{INDeq}\left(r_i + r_o + g_m r_i r_o\right) + r_i r_o}{L C_L R_L\left(r_i + r_o + g_m r_i r_o\right)}} \tag{D-12}$$

$$Q = \frac{1}{2\xi} \tag{D-13}$$

$$\xi = \frac{L\left(R_L + r_i + r_o + g_m r_i r_o\right) + C_L R_L\left(r_i r_o + R_{INDeq}\left(r_i + r_o + g_m r_i r_o\right)\right)}{2\sqrt{L C_L R_L\left(r_i + r_o + g_m r_i r_o\right)\left(R_L\left(R_{INDeq} + r_i\right) + R_{INDeq}\left(r_i + r_o + g_m r_i r_o\right) + r_i r_o\right)}} \tag{D-14}$$

APPENDIX D
MSP430L092 CODE FOR SMART PIEZO MICROSYSTEM DEMO

```
//*****************************************************************************
// Code for utilizing the MSP430L092 microprocessor to generate the digital
// sequences of (CLK, DAT) for controlling the hysteretic hybrid SI-SC converter
// Built with IAR Version 5.10.4
// Note: Load this code in IAR and click “RUN” to talk to the microprocessor
//*****************************************************************************
#include "msp430l092.h"
//int Output;
//unsigned int out1, out2;
int DACup;
int i, j;
int loop;
//data pattern for SCBoost Controller
unsigned char CLKcell=0xC3; //[11000011]
unsigned char DATHeader=0xF0; //[11110000]
unsigned char DATEnder=0x0F; //[00001111]
//Q[32:29]=0,Q[28:25]=0,Q[24:21]=0,Q[20:17]=[0001],
//Q[16:13]=[1111],Q[12:9]=[0000],Q[8:5]=[1010],Q[4:1]=[0011],
unsigned long DATcell=0xC50F8000;
void main(void)
{
  WDTCTL = WDTPW + WDTHOLD;                 // Stop watchdog timer
```

```
        // Set P1.0, P1.1 output
        P1DIR |= BIT0 + BIT1;

        //Setup of the A-POOL module for DAC output
        APCNF = DBON+CONVON+APREFON;                    // Configure A-POOL
elements
        APCTL |= ODEN+OSEL;                             // A-POOL Comparator/Saturation
Based Stop Enable and Running
        APINT=0;
        /************************/
        /* Setup CCS            */
        /************************/
        CCSCTL0 = CCSKEY;                   // Unlock CCS
        while (SFRIFG1 & OFIFG)             // Oscillator Flag(s)?
        {
          CCSCTL7 = 0;                      // Clear HF & LF OSC fault flags
          SFRIFG1 = 0;                     // Clear OFIFG
        }
        CCSCTL4 = SELA_0 + SELM_0 + SELS_0;    // Select HFCLK/DCO as the
source for ACLK, MCLK, and SMCLK
        CCSCTL5 = DIVA_0 + DIVM_0 + DIVS_0;     // Set the Dividers for ACLK to 1,
MCLK to 1, and SMCLK to 1
        CCSCTL0_H |= 0xFF;                  // Lock CCS
```

```
        /* Lock by writing to upper byte */
        // Setup of TimerA0 Capture Compare Register 0
         TA0CCTL0 = CCIE;                          // TA0CCRO Interupt Enable
         TA0CCR0 = 1;
        // Setup of TimerA0 Control Register
         TA0CTL = TASSEL_2 + MC_1 + TACLR;              // SMCLK, Up Mode
         __bis_SR_register(LPM0_bits + GIE);            // Enter LPM0 w/ interrupts
enabled
        while (loop < 1000)
        {
          //loop++;
          if(APINT<0x01) DACup=1;
          else{
            if(APINT>0xFE) DACup=0;
          }
          //header
          for(i=1;i<9;i++){
            if(DACup){
              if(APINT<0xFF){
                APINT=APINT+0x1E;
              }
              else APINT=0xFF;
            }
```

```
  else{
     if(APINT>0x00){
     APINT=APINT-0x1E;
    }
    else APINT=0x00;
  }
  if(BIT0 & CLKcell){
    P1OUT |= BIT0;   //set
    CLKcell = (CLKcell >> 1) | (CLKcell << 7);
  }
  else{
    P1OUT &= ~BIT0; //reset
    CLKcell = (CLKcell >> 1) | (CLKcell << 7);
  }
  if(BIT0 & DATHeader){
    P1OUT |= BIT1;   //set
    DATHeader = (DATHeader >> 1) | (DATHeader << 7);
  }
  else{
    P1OUT &= ~BIT1; //reset
    DATHeader = (DATHeader >> 1) | (DATHeader << 7);
  }
}
```

```
//data pattern
for(j=1;j<33;j++){
  for(i=1;i<9;i++){
    if(BIT0 & CLKcell){
      P1OUT |= BIT0;   //set
      CLKcell = (CLKcell >> 1) | (CLKcell << 7);
    }
    else{
      P1OUT &= ~BIT0; //reset
      CLKcell = (CLKcell >> 1) | (CLKcell << 7);
    }
    //
    if(BIT0 & DATcell){
      P1OUT |= BIT1;   //set
    }
    else{
      P1OUT &= ~BIT1; //reset
    }
  }
  DATcell = (DATcell >> 1) | (DATcell << 31);
}
//ender
for(i=1;i<9;i++){
```

```
      if(BIT0 & CLKcell){
        P1OUT |= BIT0;   //set
        CLKcell = (CLKcell >> 1) | (CLKcell << 7);
      }
      else{
        P1OUT &= ~BIT0; //reset
        CLKcell = (CLKcell >> 1) | (CLKcell << 7);
      }
      //
      if(BIT0 & DATEnder){
        P1OUT |= BIT1;   //set
        DATEnder = (DATEnder >> 1) | (DATEnder << 7);
      }
      else{
        P1OUT &= ~BIT1; //reset
        DATEnder = (DATEnder >> 1) | (DATEnder << 7);
      }
    }
  }
}
#pragma vector=TIMER0_A0_VECTOR
__interrupt void Timer_A (void)
{
```

```
  if(APINT < 0x01)
    DACup = 1;
  else {
    if (APINT > 0xFE)
    DACup = 0;
  }
  if(DACup){
    while(APINT < 0xEF)
      APINT=APINT+0x10;
    APINT = 0xFF;
  }
  else{
    while(APINT > 0x10)
      APINT=APINT-0x10;
    APINT = 0x00;
  }
  TA0R = 0x0000; //???
  for(loop=0;loop<500;loop++){}
}
```

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