ULTRA LOW POWER PASSIVE TRANSPONDERS FOR BIOMEDICAL MICROSYSTEMS

By

CHUN-MING TANG

A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA
2013

To my family

ACKNOWLEDGMENTS

I would like to first thank my advisor Dr. Rizwan Bashirullah for giving me this great opportunity to work toward a Ph.D.degree under his supervision. His constant guidance and encouragement provided me a clear path for my study, and I have truly enjoyed working with him over these years of acquiring knowledge. I would also like to thank Dr. John Harris, Dr. Jenshan Lin, and Dr. Christopher Batich for their valuable time and for being on my Ph.D. committee.

I feel very fortunate to have worked together with all my colleagues, especially Zhiming Xiao, Qiuzhong Wu, Chris Dougherty, Walker Turner, Jikai Chen, Lin Xue, and Edgar Garay of the ICR group. The helpful discussion, suggestion, and friendship I have shared with my all my colleagues have improved the quality of my work, and without them I would not have been able to complete this project.

Finally, I would like to acknowledge the love and continuous encouragement I have received from my parents Ms Mei-Hsin Fan and Mr. Kuo-Chu Tang and my wife Dr. Qing Yang.

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

Abstract of Dissertation Presented to the Graduate School
of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Doctor of Philosophy

ULTRA LOW POWER PASSIVE TRANSPONDERS FOR BIOMEDICAL MICROSYSTEMS

By

Chun-Ming Tang

August 2013

Chair: Rizwan Bashirullah
Major: Electrical and Computer Engineering

This dissertation examines several aspects of designing high-efficiency and low-power building blocks for passive microsystems used in biomedical applications.

To reduce losses in the power conversion in voltage multiplier, the architecture implements several types of Schottky diodes on standard CMOS processes. The Schottky diode provides a lower turn-on voltage, which minimizes the losses associated with the forward biased voltage drop. Utilizing the diode's measured I-V characteristics, this dissertation proposes a new RF-DC voltage multiplier design procedure. This design method provides an overview of the voltage multiplier's design parameters, including the diode sizing, number of stages, the RF-DC voltage multiplier's input impedance, matching between antennas, and power conversion efficiency.

A new calibration-free low-power clock generator is also presented. This clock generation scheme provides a clock frequency that is more stable against process, temperature, and voltage variations. This allows more reliable data decoding and encoding. Additionally, this dissertation also proposes a dual power supply RF-DC power management unit to minimize the clock generator's power consumption and to improve the overall DC-DC voltage conversion efficiency.

A novel passive transponder architecture is proposed, which minimizes overall chip area. All building blocks in the proposed transponder are designed to be operated from an AC power supply. With this architecture, the AC power supply not only powers the transponder but also provides a clock signal for the chip. This allows the architecture to eliminate area-consuming building blocks, such as an RF-DC multiplier, a decoupling capacitor, a voltage regulator, and a power-on-reset circuit.

Finally, a battery-assisted transponder is presented. The transponder can use take the DC voltage at the input to improve the sensitivity. A radio transmitter is used in this proposed transponder to improve the communication range. The transponder can also operate by harvesting energy from electromagnetic wave if the DC voltage is not available at the input. The proposed transponder has both advantages of the active and passive transponder architectures.

CHAPTER 1
INTRODUCTION

1.1 Motivation

Advances in microelectronics have allowed wireless systems to perform complicated tasks while minimizing power consumption. To date, researches have explored using wireless microsystems mainly in healthcare and biomedical applications. Applications have included implantable devices, medication compliance improvement, neuromuscular stimulation, and biological signal monitoring [1, 2, 3, 4, 5, 6]. Devices for these uses must meet strict technical parameters, such as requirements on physical size, power consumption, heat generation, and operational lifetime. Because of these constraints, microsystems for biomedical applications must have low power consumption, high power conversion efficiency, long life span, and they must be small. Figure 1-1 shows an example of a wireless microsystem for neurosignal measurement. The device is powered by an inductive link. The recorded data from the electrode array is amplified by a low noise amplifier, digitized by an Analog-to-Digital converter, and transmitted via a transmitter through the antenna to the external reader.

Wireless microsystems usually share many basic components and features. The basic components include a high efficiency external reader, an antenna (coil), a communication module, a power management module, a digital control unit, an analog frontend, and a sensor interface. Wireless transponders are classified into two categories depending on the power source they use: active and passive. An active transponder incorporates a battery into the microsystem, which provides the power necessary to perform the communication function to the reader and for the analog and digital blocks. A passive transponder harvests energy from the carrier transmitted from the reader, which means it doesn't require a battery. Consequently, a completely passive microsystem has several advantages over active ones. For example, a passive microsystem is

simpler to fabricate and package because it doesn't need a battery. The size of an active transponder is constrained due to the inclusion of a battery into the microsystem because the size of the battery has not been miniaturized to the micro-scale. Moreover, passive microsystems provide a less invasive alternative for wireless implant devices, and thus reduce the risk of infection. All things considered, passive microsystems are more cost effective overall and more suitable for biomedical applications. However, passive microsystems do suffer from several fundamental performance issues, including low power conversion efficiency in the energy harvest circuit and clock drifting of the on-chip clock generator due to process, voltage, and temperature variations (PVT).

The power efficiency of a passive microsystem is crucial [7]. Consider powering a passive implantable device intended for chronic recording. If the device's power consumption is high it not only increases the tissue temperature but also requires a denser electromagnetic field through the tissues for power up. To avoid damage due to heat and electromagnetics, the device needs a passive microsystem with high power efficiency. To achieve this, the energy harvester must provide high power conversion efficiency, and the power consumption of building blocks in the microsystem must be minimized.

To provide reliable communication between the reader and the passive transponder, the transponder's clock generator must be stable. For instance, the EPC class-1 generation-2 RFID protocol requires the frequency drift and short-term frequency variation to be less +/- 2.5% during backscattering [8]. However, the on-chip generator suffers process, voltage, and temperature (PVT) variations that can result in frequency variation as large as +/- 20% [9, 10]. A higher clock frequency lowers the bit error rate, but this results in increased power consumption.

The challenges to clock generator design are how to achieve low power consumption and free of trimming process to tune the target frequency to reduce the cost.

1.2 Research Goals

For certain biomedical applications passive microsystems have several advantages over active approaches. This research focuses on passive microsystems. The first research goal is to provide a power efficient RF frontend for the passive microsystem that minimizes the system size for biomedical applications. Figure 1-2 shows the wireless passive microsystem's functional block diagram. The passive microsystem's sensitivity is determined by the power consumption of the analog and digital blocks divided by the rectifier's power conversion efficiency. To achieve high power conversion efficiency, the optimization procedure of the RF-DC multiplier for a given power load needs to be developed. The voltage regulator that follows after the RF-DC multiplier must also be efficient. To minimize the losses associated with the rectifying diode in the RF-DC multiplier, different diode structures that can be implemented in a standard CMOS process will be investigated.

The second goal of this research is to provide a stable clock signal on the transponder while minimizing power consumption. Different commonly used clock generators for passive microsystems are surveyed. A clock generator architecture that can use a wirelessly received reference clock is investigated.

The third goal of this research is to minimize the size of the passive microsystem. The advantages of a small passive transponder chip are low cost and small form package.

1.3 Thesis Organization

In Chapter 2, we review passive transponders used for biomedical applications and study the basics of building blocks. Next we investigate communication channels, including free space

and in-body. After this, we present various powering strategies: far filed powering, inductive coupling, capacitor coupling, and galvanic coupling. Finally, we examine the uplink and downlink communications between reader and tag. We compare the active transmission and backscattering modulation for uplink communication. For downlink, we review other modulation methods.

Chapter 3 discusses the design methodology for the diode-based RF-DC voltage multiplier and describes key specifications for the passive microsystem. For a given loading specification, the proposed design procedure can provide the required diode and capacitor size while achieving high power conversion efficiency. Chapter 3 also presents the implementation of Schottky diodes in a standard CMOS process. Several types of Schottky diodes are designed, fabricated, and measured. We then measure and compare the performances of RF-DC voltage multipliers with different rectifying diodes.

Chapter 4 presents a scheme to efficiently generate dual regulated supply voltages from a single RF-DC converter block, supporting a low voltage for the digital processing at V_{REGL}~260 mV and a higher voltage for the analog circuits at V_{REGH}~725 mV. We also demonstrate a ~200 nW on-chip clock generator, which is based on a digital phase locked-loop (DPLL) operating in the subthreshold region. This clock synchronizes communication functions between the reader and the passive transponder.

Chapter 5 describes a novel passive transponder architecture that minimizes the chip area. We propose and implement a supply modulated passive microsystem for medication compliance. The input AC signal powers the proposed chip directly, thus avoiding the need for area consuming blocks such as a RF-DC multiplier, a decoupling capacitor, power-on reset circuitry, and voltage regulator. The system uses a low frequency carrier (125 kHz) as the power supply

and system clock, and it transmits data through a high frequency carrier (915 MHz) when the chip's supply voltage level reaches a certain level. The novel building blocks for this transponder, such as the AC logic, the voltage divider, and the low power UHF oscillator, are designed and measured.

Chapter 6 presents a new transponder architecture. The proposed chip can provide AC/DC or DC/DC conversion in the energy harvester. It can use a coil to receive data and system clock, and uses DC voltage to power the chip at the input to improve the chip's sensitivity. It also can harvest energy from the electromagnetic waves. The chip's measured results are shown in chapter to demonstrate the idea.

Chapter 7 summarizes this work and lists the future work necessary to complete this dissertation.

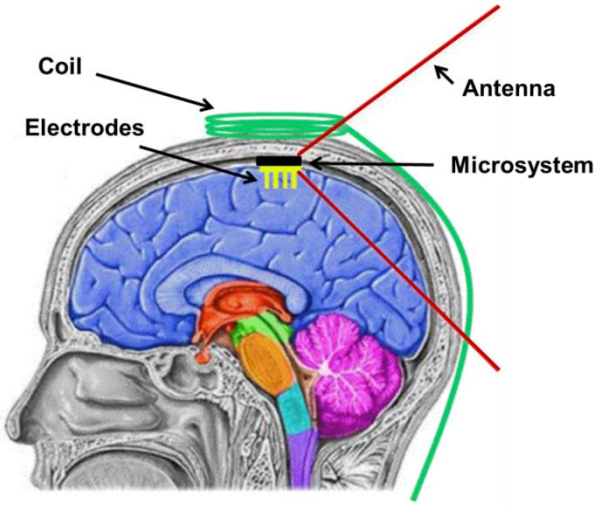


Figure 1-1. A wireless passive microsystem for neurosignal measurement.

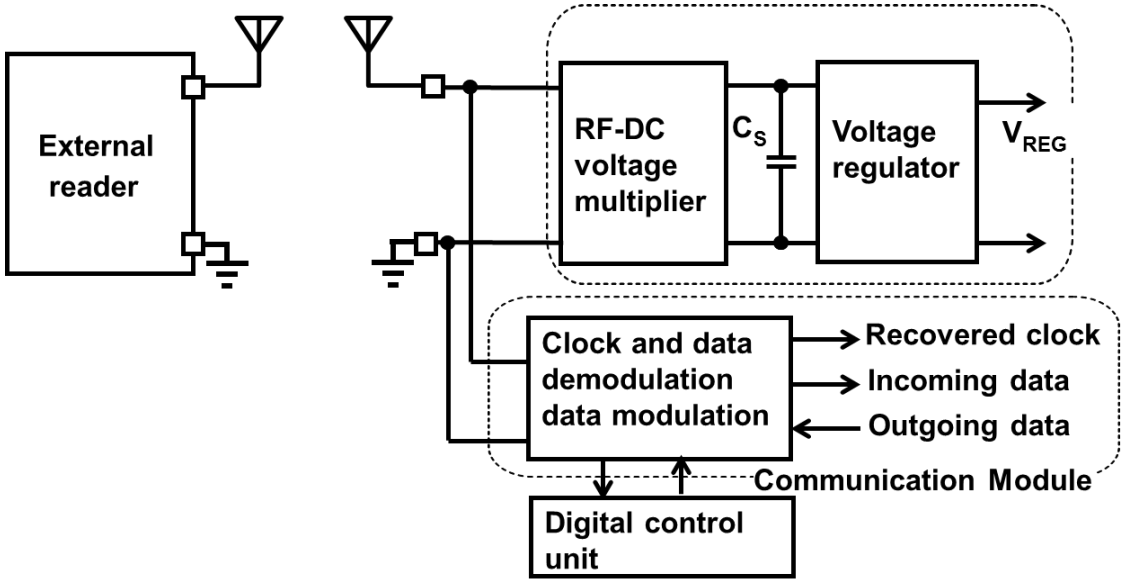


Figure 1-2. Functional block diagram of a wireless passive microsystem.

CHAPTER 2
OVERVIEW OF PASSIVE TRANSPONDERS FOR BIOMEDICAL APPLICATIONS

Passive wireless transponders provide more advantages than active transponders in biomedical applications. In this chapter, we review the published passive transponders that are used in various biomedical applications. Here we discuss several widely used powering methods of powering passive transponders: near-field inductive coupling, far-field electromagnetic coupling, capacitive coupling, and galvanic coupling. We also review the most widely adopted communications schemes used in passive transponders. These modulation methods provide different characteristics for powering and power consumption of the demodulator and modulator. Finally, safety must also be considered for passive transponder used in biomedical applications. This chapter presents two exposure limitations from IEEE standards.

2.1 Biomedical Applications

Passive transponders have found a broad range of uses in biomedical applications, including neural signal recording [11], tear glucose measurement [12], body temperature monitoring [13], and retinal prosthetic devices [14, 15]. Different applications employ different powering and communication methods depending on the where the transponder is located and the channel's characteristics.

2.2 Passive Transponder Building Blocks for Biomedical Applications

The building blocks of the passive transponder for biomedical applications include an energy harvester, voltage regulator, voltage limiter, demodulator, clock generator, modulator, analog-to-digital converter, sensor interface, and antenna.

To obtain the power necessary to operate the transponder, the energy harvester converters the external AC carrier to DC voltage on a capacitor. Several factors determine the amount of

power the transponder receives: the amount of power transmitted from the reader, the channel loss, the transponder antenna gain, the matching between antenna and transponder, and the energy harvester's power conversion efficiency. In near-field coupling, a diode-bridge rectifier is widely used due to the large power transfer it provides. In far-field coupling the received signal amplitude is usually smaller than near-field coupling. When the input signal amplitude is close to the diode device's turn-on voltage, a diode-bridge rectifier encounters high voltage conversion loss that causes the transponder to have very low sensitivity. To avoid this, a RF-DC multiplier is widely employed in far-field passive transponders.

At the output of the energy harvester, output load and input power level affect the output voltage ripple. Although the decoupling capacitor's size can be increased to reduce the output voltage ripple, this increases chip area and cost. Moreover, building blocks, such as a clock generator, sensor analog frontend, and ADC, are required precise supply voltage to maintain operation. To meet this requirement, we incorporate the voltage reference and voltage regulator into the passive transponder design. A linear series regulator can provide several advantages over the switching mode voltage regulator, such as lower noise, a small area, and high speed. The linear series regulator is widely used in passive transponders [16, 17].

The demodulator and modulator are used to communicate between the reader and transponder. Their functions include data decoding, data encoding, calibration, and synchronization. Their power consumption and circuit complexity depend on the modulation scheme. The on-off keying enables the use of a simple demodulator and modulator design, an approach that is widely used in passive wireless transponders [18].

The clock generator provides the clock for the baseband unit, data decoding, and encoding function for downlink and uplink. The clock generator's power consumption is a crucial issue.

An LC tank oscillator provides an accurate clock and less sensitivity to PVT variations, but it requires a larger area. For applications that require a small area and low power consumption, both the current starved ring oscillator and the relaxation oscillator are widely used. However, these types of oscillators are prone to PVT variations.

The sensor analog frontend provides the input signal conditioning. The building block depends on the type of sensor and application. A low noise amplifier is a typical choice for neural signal recording applications. There is a tradeoff between noise performance and power consumption. To achieve low power while providing required noise performance in the amplifier, several techniques have been explored [19, 20, 21], including time-multiplexing, bias current reuse, and supply current modulation.

For biomedical applications, the ADC is essential. It converts the input signal to digital format for the modulator. In passive transponders, which ADC architecture to use is usually limited by the stringent power budget. Because of this, successive approximation register (SAR) ADCs are widely used for biomedical applications [22, 23]. Pipeline converters may be required for some high-speed biomedical systems.

As for the antenna, it converts captured electromagnetic waves to AC voltage for the energy harvester and converts AC signals to electromagnetic waves for the external reader. The dimensions of the antenna impose a challenge on the passive transponder design. If the antenna is electrically small, it's very inefficient, however its maximum size is limited by the operating carrier frequency, the size of the implant site, and impedance matching.

2.3 Powering Strategies

Passive microsystems harvest power from electromagnetic waves transmitted by the reader. Two widely used powering approaches are near-field inductive coupling and far-field

electromagnetic coupling. If the antenna size is compatible with the wavelength (UHF/Microwave RFID), the boundary between near field and far field is given by $r = 2D^2/\lambda$ where D is the maximum antenna size and r is the wavelength. However, for electrically small antennas (LF/HF RFID and biomedical applications), the boundary between near field and far field is defined as $\lambda/2\pi$, where λ is the carrier's wavelength [24, 25]. The near-field frequency usually ranges from one hundred kHz to ten Mhz. Near-field coupling is less susceptible to absorption by human body tissue than the far-field coupling. As a result, near-field coupling is widely used in wireless implant. Far-field coupling is used more often with ultra-high frequencies (UHF) and microwave frequencies, such as ISM 900 MHz and 2.4 GHz bands.

Nevertheless, studies of bioelectricity show useful alternatives to both near-field magnetic coupling and far-field RF powering as a means of energizing a passive device inside the body (Galvani, Volta, Faraday, etc.).

The human body supports current flow via the intra-cellular and cellular membranes, and the resulting impedance between two points in the body is a complex function of frequency, tissue type, organs, geometry, and distance. A significant amount of literature studies and assesses bioelectricity and equivalent tissue models [26, 27, 28]. Gabriel [29] gives a very thorough review of tissue permittivity and conductivity. While these models and studies provide excellent explanations of the pathways electrical current takes through the human body, the most relevant information for establishing the human body as a direct transmission channel between two or more devices within or on the body is the frequency dependent signal attenuation characteristics among these nodes. These characteristics, in turn, depend both on the method of coupling the signals into the body and the human body channel characteristics.

The remainder of this section presents and studies the various powering strategies.

2.3.1 Near-Field Inductive Link

The near-field link can be modeled using two closely spaced inductively coupled coils. The primary coil is in the external reader and the secondary coil is in the implant device. Usually the two are several millimeters to tens of millimeters apart. In this approach, normally both sides of the coil are tuned to the same resonant frequency to maximize the power transmission efficiency.

To maximize the power conversion efficiency from the DC power supply to magnetic fields, designers often use the Class-E power amplifier to drive the reader coil. If the magnetic field on the primary coil (L_1) induces an AC voltage on the secondary coil (L_2), then the AC voltage can be rectified and regulated to supply the implanted device. Assume the coils are parallel and center aligned. The induced AC voltage is determined by the coils' coupling coefficient (k), where is k is $0 < k < 1$ and dimensionless. k can be defined by

$$k = \frac{M}{\sqrt{L_1 \cdot L_2}} \tag{2-1}$$

where M is the mutual inductance.

Figure 2-1 shows a simplified schematic of an inductive link and the equivalent RLC network. The resistor R_1 is the combination of the effective series resistor (ESR) of $L_1$and the output resistor of the power amplifier. The resistor R_2 is the effective series resistor (ESR) of L_2. RL represents the loading effect from the rectifier, the LDO, and the output load. The capacitors C1 and C2 are used to resonate the primary and secondary coil at frequency f_0. The frequency f0 is given by

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_1}} = \frac{1}{2\pi\sqrt{L_2 C_2}} \tag{2-2}$$

The entire system efficiency can be presented as in an equivalent RLC circuit. The entire inductive link efficiency η_{IND} is given by

$$\eta_{IND} = \eta_{PA} \cdot \eta_{T\cdot} \cdot \eta_R \cdot \eta_{RECTIFIER} \cdot \eta_{LDO} \tag{2-3}$$

where η_{PA} is the power amplifier power deliver efficiency, η_T is the primary coil power conversion efficiency, η_R is the secondary coil power conversion efficiency, $\eta_{RECTIFIER}$ is the rectifier power conversion efficiency, and η_{LDO} is the LDO power conversion efficiency.

The efficiency of the secondary coil η_R is given by

$$\eta_R = \frac{Q_2{}^2 R_2}{Q_2{}^2 R_2 + R_L} = \frac{Q_2}{Q_2 + Q_L} \tag{2-4}$$

where $Q_2=\omega_0 L_2/R_2$ is the quality factor of the unloaded secondary coil and $Q_L=\omega_0 L_2 C_2$.

Next we find the primary coil power conversion efficiency. We can convert the weak coupling between the primary and secondary coil as an ideal transformer and two inductors L_{T1} and L_{T2} [30]. L_{T1} and L_{T2} can be expressed as $L_1(1-k^2)$ and L_1k^2, respectively. Then reflecting the R and C into the ideal transformer, the C_{REFL} and R_{REFL} are expressed as $C_{REFL}=(C_2/k^2)(L_2/L_1)$ and $R_{REFL}=(k^2L_1/ L_2)(R_L//Q_2{}^2R_2)$. L_{T2} and C_{REFL} are resonated, and then the equivalent circuit can be simplified to

Figure 2-1(D). The primary coil power conversion efficiency η_T is given by

$$\eta_T = \frac{R_{REFL}}{R_{REFL} + R_1} = \frac{k^2 Q_1 Q_2}{1 + k^2 Q_1 Q_2 + \frac{Q_2}{Q_L}} \tag{2-5}$$

where $Q_1= \omega_0 L_1/R_1$.-

If a full-bridge diode rectifier is used as the rectifier, the $\eta_{RECTIFIER}$ is given by

$$\eta_{RECTIFIER} \cong \frac{V_{RECT}}{V_{RECT} + 2V_{DIODE}} \tag{2-6}$$

where V_{RECT} is the rectifier output voltage and V_{DIODE} is the diode voltage drop.

The LDO power conversion efficiency η_{LDO} is given by

$$\eta_{LDO} \cong \frac{V_{REG}}{V_{RECT}} \tag{2-7}$$

As a result, the efficiency of the inductive power link η_{IND} is presented as a simple form by given the required load of the implanted device. To improve the overall frequency, equation 2-3 and 2-4 should be maximized. If Q_L increases, η_T decreases and η_R increases. By differentiating equation 2-4 and 2-5, there is an existing optimum Q_L, which maximizes the overall efficiency. From equation 2-6 to 2-7, to maximize the overall efficiency, the diode drop voltage V_{DIODE} should be minimized and the dropout voltage in the LDO should be reduced.

2.3.2 Far-Field Wireless Power Link

Far-field powering occurs at high frequencies. The path loss in the air is inversely proportional to the distance between the transponder and the reader. Because of this, at high frequencies, the system can have small antenna size and long communication link (several meters). However, unlike near-field coupling, far-field coupling usually generates less than a couple hundred millivolts. A RF-DC multiplier is usually used to generate the DC voltage required for the IC.

The communication distance is determined by the maximum power transmitted from the reader, the antenna radiation resistance, input matching, and tag sensitivity. The incident power captured by the antenna is given by [31, 32, 33]

$$P_{TAG} = P_{READER} G_{READER} G_{TAG} \left(\frac{\lambda}{4\pi r} \right)^2 \tag{2-8}$$

where P_{READER} is the amount of power the reader delivers to the antenna, G_{READER} is the gain of the reader, r is the distance, and λ is wavelength of the carrier. Figure 2-2 shows a simplified schematic of far-field powering and the equivalent circuit of the antenna and the RF-DC

multiplier. If the antenna and RF-DC multiplier are conjugate matched, the input power available for the RF-DC multiplier is $P_{TAG}/2$.

The efficiency of the RF-DC multiplier can expressed as

$$\eta_{RF-DC} = \frac{P_{OUT}}{P_{TAG}/2} \tag{2-9}$$

where P_{OUT} is the DC output load power of the RF-DC multiplier. By given P_{OUT}, P_{READER}, G_{READER}, and G_{TAG} from equation 2-7 and 2-8 the higher RF-DC efficiency and conjugate matching can increase the communication distance.

If the required input voltage for the RF-DC multiplier based on a given load is V_{IN}, then we can derive the distance at which the transponder can be powered. The induced open circuit voltage on the antenna is given by

$$v_A = 2\sqrt{2R_A P_{TAG}} \tag{2-10}$$

where R_A is radiation resistance. If the input of the RF-DC multiplier can be modeled as resistor R_{IN}, this condition assumes the reactance components are cancelled by matching. V_{IN} is expressed as

$$v_{IN} = 2\sqrt{2R_A P_{TAG}}\,\frac{R_{IN}}{R_{IN}+R_A} \tag{2-11}$$

From equation 2-10 and 2-11, we see that a high radiation resistance of the antenna is favored. If we want maximum power delivery, R_{IN} must equal R_A.

To conclude, the communication distance of a far-field passive transponder can be increased by a lower output power P_{OUT}, a conjugate matching network, a high radiation resistance of the tag antenna, and high input impedance of the RF-DC multiplier.

2.3.3 Capacitive Coupling

Figure 2-3 shows a simplified schematic of the capacitive body transmissions methods. Capacitively coupled body transmission systems exploit the capacitive coupling between the body and its environment to establish signal pathways between a source and a detector in close proximity to the body [34]. The transmitter and receiver, each with two electrodes, are coupled via electric field lines generated by the transmitter and terminating at the receiver. Transmission predominantly uses the surface of the body as the propagation medium. Return pathways are established by the second electrode of each unit and the surrounding environment (or ground). Since the field lines generated by the transmitter electrode escape through the body to ground and are partially cancelled by the localized return pathways and stray fields, only a small portion of the fields couple to the receiver. In addition, since the return pathways via ground play an integral role in the overall transmission system, the signals detected at the receiver depend not only on the human body but also on its surrounding environment, which is subject to changing conditions.

2.3.4 Galvanic Coupling

An alternative to capacitive coupling is to directly couple signals into the body using a galvanic method, as shown in Figure 2-4 [35, 36]. Similar to the capacitive approach, galvanic transmission relies on a transmitter and receiver, each with two electrodes, coupled via transmission of alternating currents through the body and/or over the body surface using electrodes in direct contact with the skin. Current flow, generated by a differential alternating voltage across the transmitter electrodes, is primarily between these electrodes. A portion of the current, however, reaches the receiver to create a detectable differential voltage across the receiver electrodes. This method of transmission depends primarily on the human body channel

instead of the surrounding environment (ground) or air to couple the transmitter and receiver via electrical conduction supported by ionic fluids within the body.

2.4 Communications

The downlink communication uses data modulation schemes into the carrier. Three modulation schemes are widely used, ASK, FSK, and PSK. The uplink communication between the reader and the tag is based two methods: one is backscattering and the other is to use different frequency carrier transmitting the data. This section discusses the communication between the reader and tag.

2.4.1 Backscattering

Backscattering switches the state of the matching between the antenna and the tag to communicate with the reader. The tag and antenna are designed to be conjugate matched to deliver maximum power. During matched condition, there is no power being reflected. On the other hand, if there is a switch shorted the antenna to ground. The power is reflected, and part of power is reflected to the reader antenna. This backscattering method has very low power consumption in the modulator because it reflects power back and can use a low frequency clock generator to modulate the switch [37]. The backscattering method's main disadvantage is its limited range. The reflected signal experiences the same path loss as incoming signal. As a consequence, the communication range is not just determined by the tag's sensitivity but also by the reader receiver sensitivity. The clock frequency is a tradeoff between power and the channel receiver selectivity. Figure 2-5 shows a simplified block diagram of a backscattering system.

2.4.2 Active Transmitting

This active transmitting architecture uses a higher frequency oscillator and transmitter to deliver signal out of the tag. The modulator employs a simple modulation scheme (OOK) to

directly modulate the oscillator and minimize power consumption. In this case, the oscillator turns on or off based on the baseband data. The uplink frequency can be different from the downlink carrier frequency. The advantage of this approach is that it has a longer range than the backscattering approach since the uplink signal only encounter one-way path loss. However, it has higher power consumption because the high frequency oscillator resides in the tag. One way to reduce the average power consumption is to send the output signal at very short time and then to accumulate energy on a large capacitor. Figure 2-6 shows a simplified block diagram of an active transmitting system.

2.4.3 Signaling

This section reviews the modulation schemes for passive transponder systems. Complex modulation schemes, such as quadrature phase-shift keying (QPSK), minimum shift keying (MSK), and Gaussian MSK (GMSK) [38] are widely used in RF communication to improve the bit error rate and data rate. However, the strict power restrictions on passive transponders prevents compatibility with complex modulation schemes.

2.4.3.1. Amplitude shift keying (ASK)

The ASK method modulates the carrier's amplitude with the digital date stream. The symbol of an ASK digital bit stream can be expressed as

$$S(t) = A(t)\cos(\omega_C t) \tag{2-12}$$

where A(t) is the carrier amplitude and the ω_C is the carrier frequency. The modulation index M in given by

$$m = \frac{A_1 - A_0}{A_1} \tag{2-13}$$

where A_1 is the amplitude when the data is 1 and A_0 is the amplitude when the data is 0. If M is equal to 1, then the modulation is on-off keying. Figure 2-7 shows the waveform of ASK modulation. Figure 2-8 shows the constellation diagram of OOK.

The OOK method is most widely used modulation scheme in passive transponders due to the simple modulator and demodulator and its low power consumption.

2.4.3.2. Frequency shift keying (FSK)

The FSK method modulates the amplitude of the carrier with the digital date stream. The symbol of an FSK digital bit stream can be expressed as

$$S(t) = A\cos[(\omega_C + \omega)t] \tag{2-14}$$

where A is the carrier amplitude and the ω_C is the carrier frequency. The ω is 0 when the data is 0, and ω is a constant frequency when the data is 1. Figure 2-9 shows the waveform of FSK modulation. Figure 2-10 shows the constellation diagram of FSK. FSK less popular than the OOK scheme because it requires a more complicated modulator and demodulator. This increases the power consumption of the passive transponder. FSK, however, provides continuous power to the tag unlike OOK, which provides power only when the data symbol is 1.

2.4.3.3. Phase shift keying (PSK)

The PSK method modulates the amplitude of the carrier with the digital date stream. The symbol of an FSK digital bit stream can be expressed as

$$S(t) = A\cos(\omega_C t + \phi) \tag{2-15}$$

where A is the carrier amplitude and the ω_C is the carrier frequency. The ϕ is 0 when the data is 0, and ϕ is a constant phase when the data is 1. Figure 2-11 shows the waveform of PSK modulation. Figure 2-12 shows the constellation diagram of PSK. PSK is less popular than the OOK scheme because, like FSK, PSK requires a more complicated modulator and demodulator.

This increases the power consumption of the passive transponder. Also like FSK, PSK provides continuous power to the tag unlike OOK, which provides power only when the data symbol is 1.

2.4.3.4. OOK with pulse-width modulation (PWM)

This modulation scheme uses different duty cycles, on time and off time, to encode data. A non-coherent demodulation scheme can be implemented to further lower the power consumption in the modulator. OOK-PWM, unlike regular OOK, can encode the clock information into the carrier. A simple clock and data recovery circuit can exact the clock and data for the passive transponder. However, this scheme also suffers from non-continuous power transfer. Figure 2-13 shows the OOK-PWM waveform.

2.4.3.5. OOK with pulse-interval encoding (PIE)

OOK-PIE is similar to PWM. The modulation uses the same off time but different on time to encode the data 0 and data 1. This modulation scheme is widely used in the EPC protocol. This scheme also suffers from non-continuous power transfer. Figure 2-14 shows the OOK-PIE waveform.

2.4.3.6. OOK with pulse-position modulation (PPM)

This modulation scheme uses a short pulse with different locations to encode data. Adding in PPM provides a better continuous power delivery, which is beneficial to the passive transponder. Figure 2-15 shows the OOK-PPM waveform.

2.5 Regulation

In this section, we discuss some power regulations and frequency bands for biomedical applications.

2.5.1 ISM Bands

The communication for the tag and the reader usually use ISM (industrial, scientific, and medical) bands. The widely used ISM bands are 13.553–13.57 MHz, 902–928 MHz, 2.4–2.485 GHz, and 5.725–5.850 GHz [39].

2.5.2 Power Regulation

In order not interfere with other communication protocols, Part 15 of the FCC Rules regulate the maximum power that can be transmitted by the reader. There are three limits:

Maximum transmitter output is 1 W (30 dBm).

Maximum EIRP is 4 W (36 dBm), i.e. for every dB of antenna gain above 6dBi, transmitter output must be reduced by 1 dBm; per this rule, a 24 dBi antenna limits the output power to 12 dBm which is 16mW. For fixed point to point operation in ISM2.4, peak output need only be reduced by 1 dBm for every 3 dBi of antenna gain above 6, i.e. per this rule, a 24 dBi antenna may be fed by 24 dBm or 250 mW.

In ISM5.8, The gain can apply all the antenna gain with no reduction in output power.

Electromagnetic fields generated by the telemetry system can lead to heat generation in body tissue and cause damage. Hence, there is a limit on the maximum power a human body can be exposed to. One well-known and widely used IEEE standard fixes the level of human exposure to radio frequency electromagnetic fields as safe from 3 kHz to 300 GHz. For frequencies between 100 kHz and 3 GHz, frequencies widely used in passive transponders, basic restrictions (BRs) are expressed in terms of specific absorption rate (SAR).

The SAR is primarily determined by the E-field and is related it to by

$$SAR = \frac{\sigma \cdot E^2}{2\rho} \tag{2-16}$$

where σ is conductivity of the tissue(S/m), ρ is the mass density of the tissue (Kg/m^3), and E is the rms electric field strength (V/m) in tissue [40].

In situations where calculating the SAR is difficult, the maximum permissible exposures (MPE_S) are provided in the IEEE standards.

Two issues need to be addressed. First, sometimes even when the SAR limited is met, the MPEs can still be exceeded. Second, in some environments when the body is close to an RF source, the MPEs may not ensure the SARs limits are complied with. Both standards are required to ensure safety.

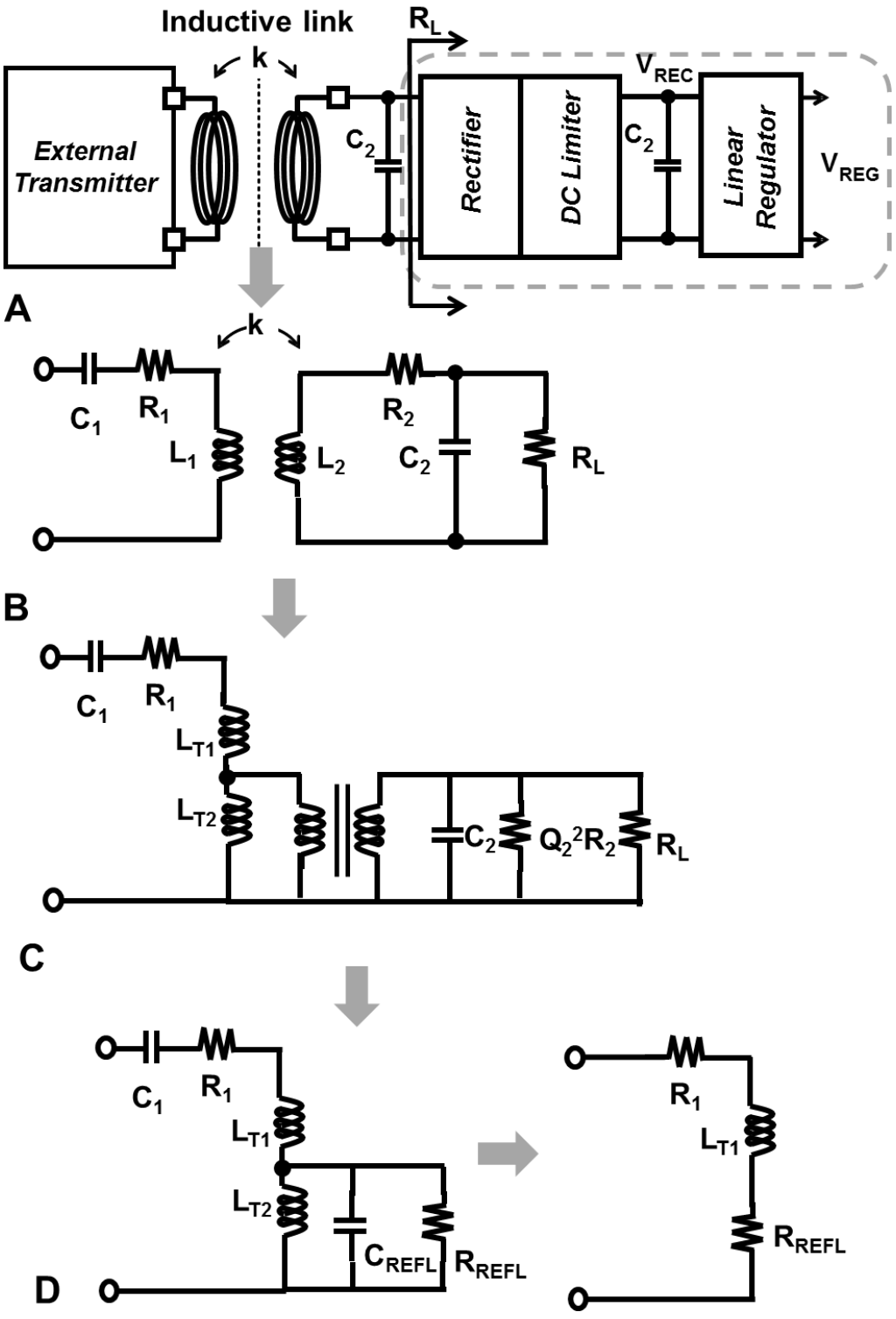


Figure 2-1. Simplified schematic of an inductive link and equivalent circuit.

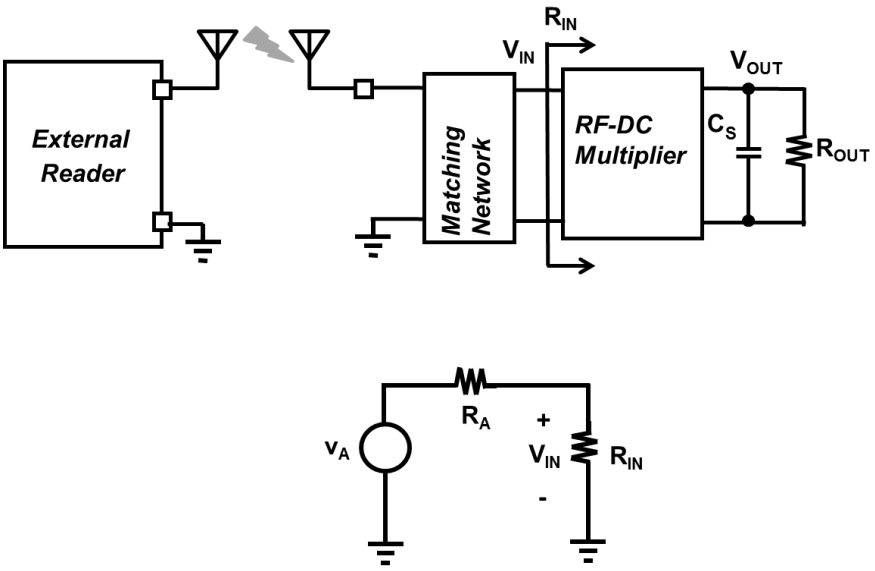


Figure 2-2. Simplified schematic of far-field powering link and equivalent circuit.

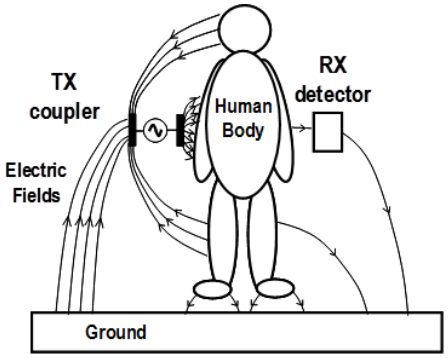


Figure 2-3. Body transmission systems for external devices using capacitive coupling.

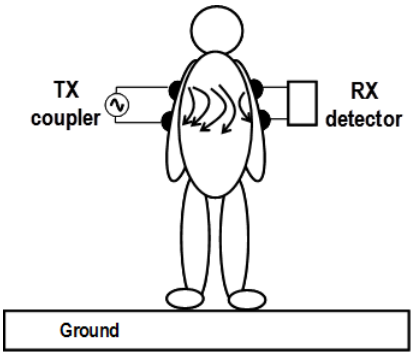


Figure 2-4. Body transmission systems for external devices using galvanic coupling.

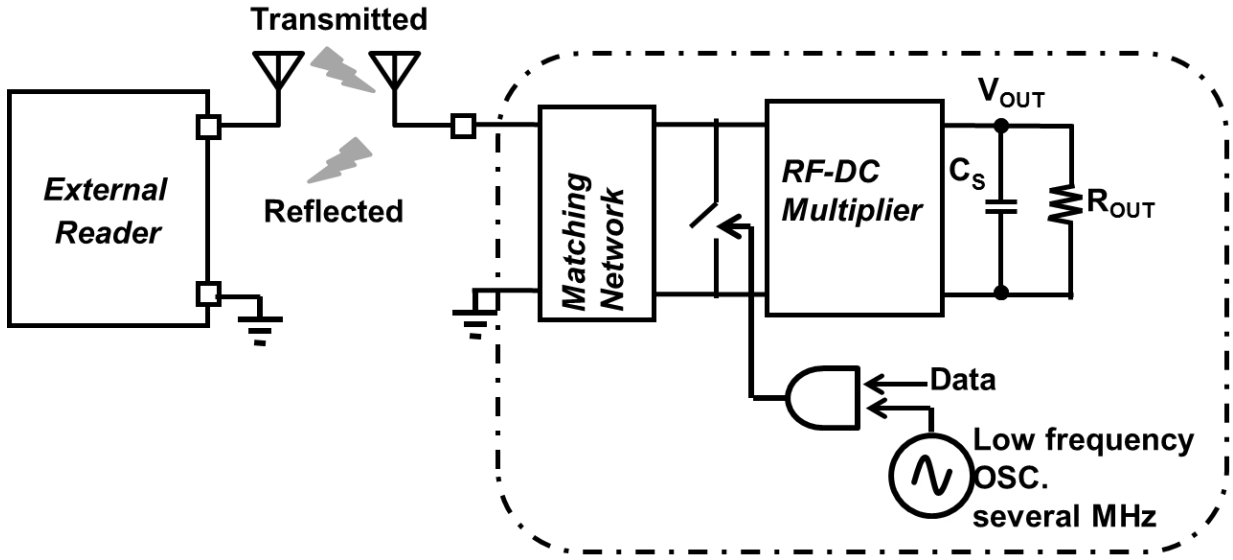


Figure 2-5. A simplified block diagram of a backscattering system.

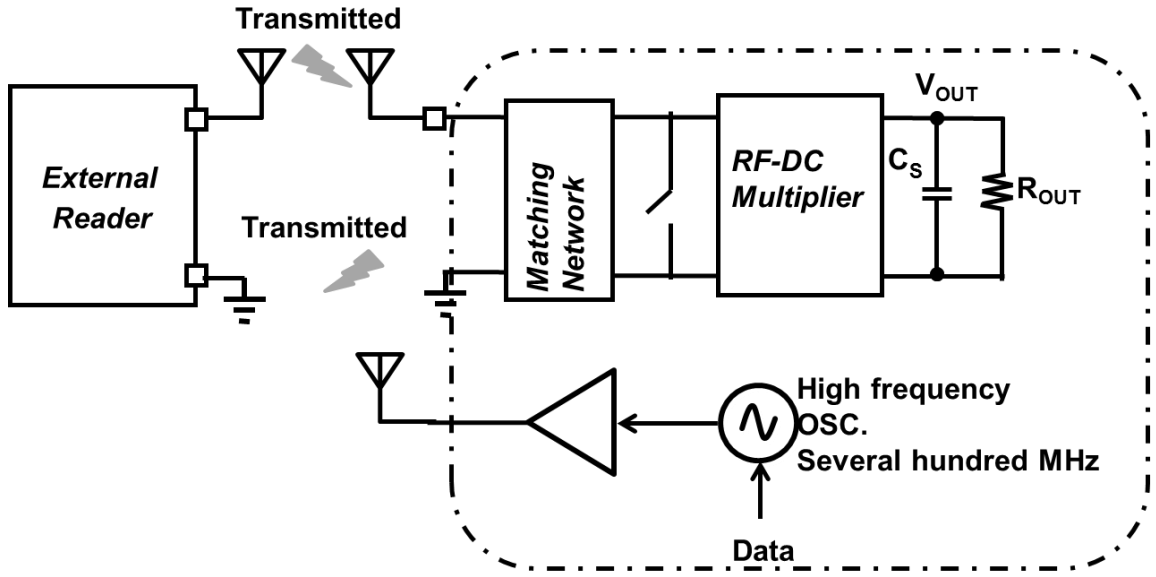


Figure 2-6. A simplified block diagram of an active transmitting system.

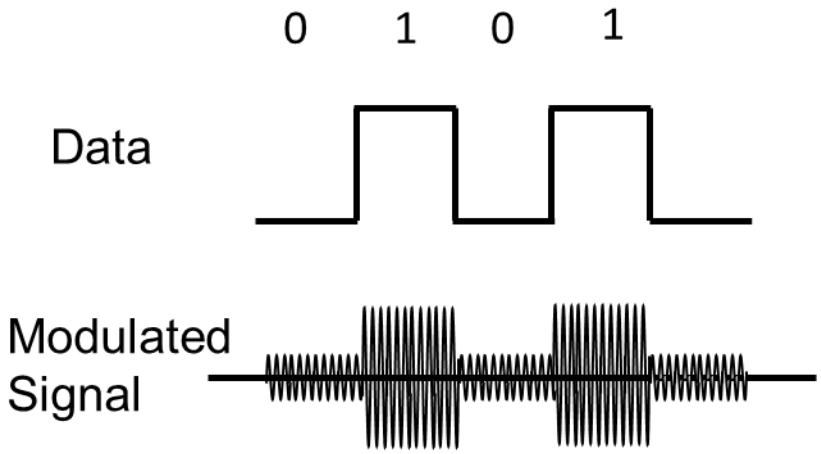


Figure 2-7. The waveform of ASK modulation.

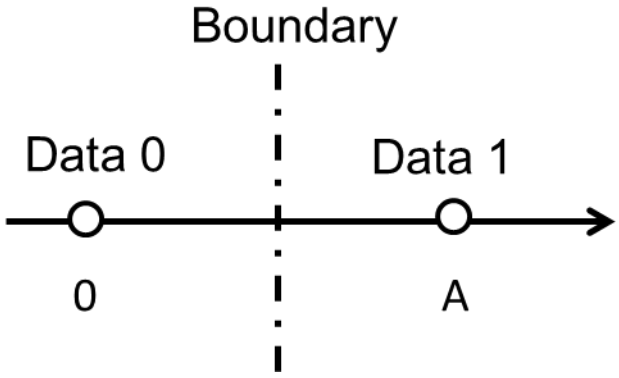


Figure 2-8. The constellation diagram of OOK modulation.

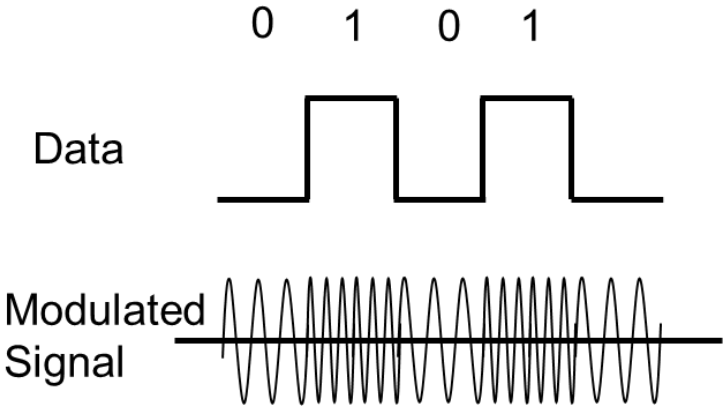


Figure 2-9. The waveform of FSK modulation.

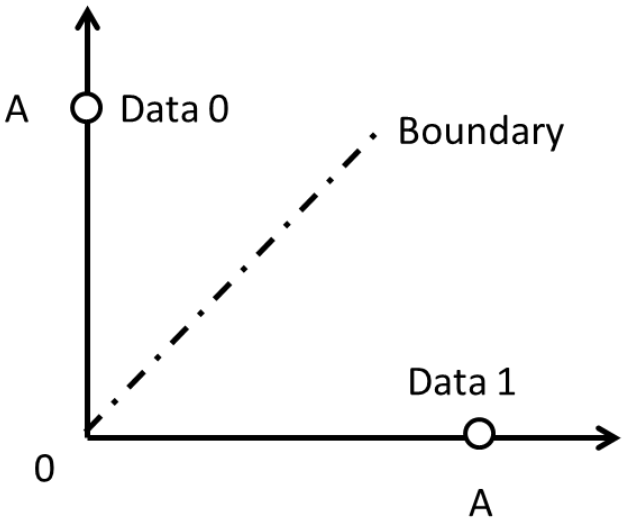


Figure 2-10. The constellation diagram of FSK modulation.

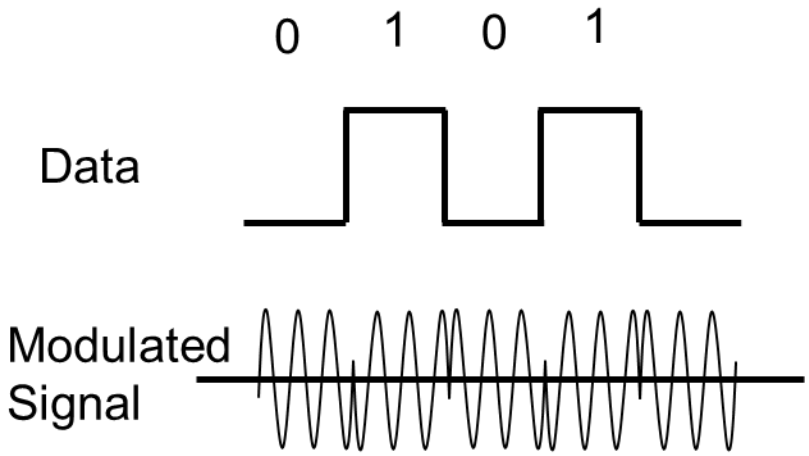


Figure 2-11. The waveform of PSK modulation.

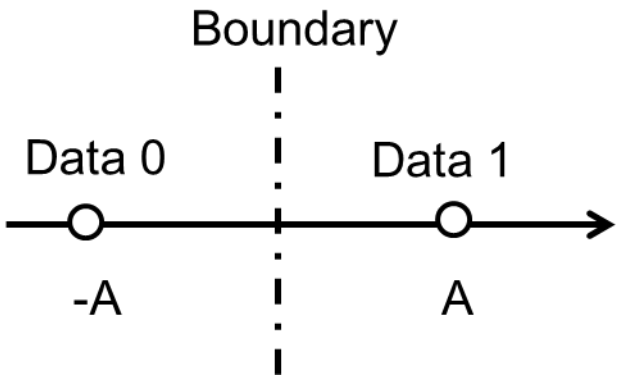


Figure 2-12. The constellation diagram of PSK modulation.

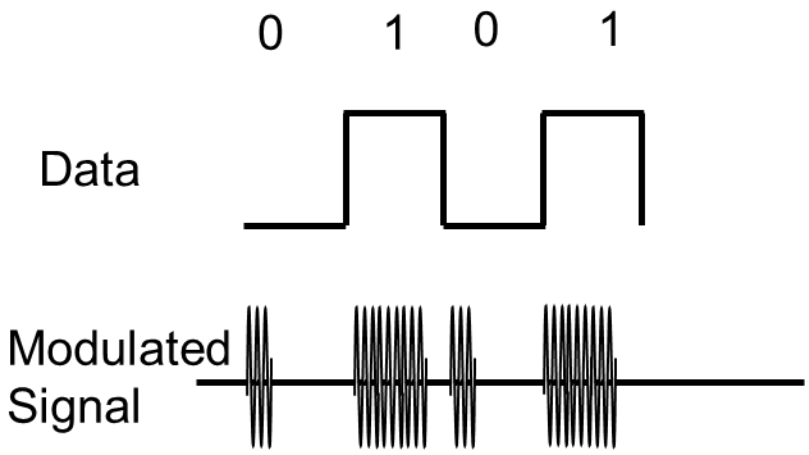


Figure 2-13. The waveform of OOK-PWM modulation.

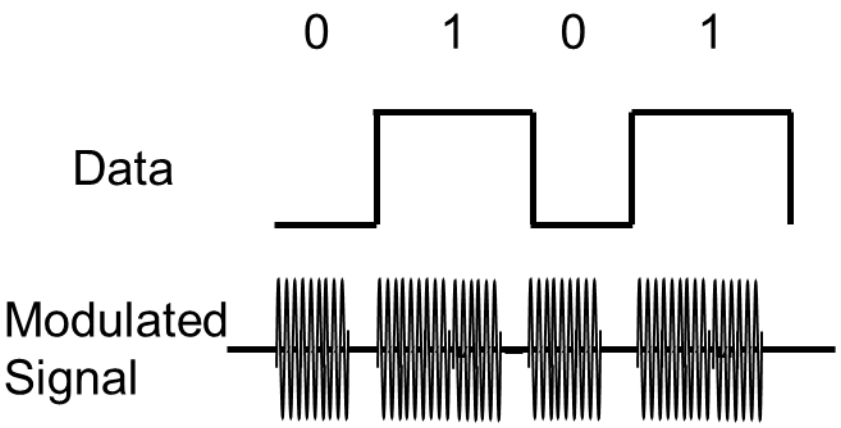


Figure 2-14. The waveform of OOK-PIE modulation.

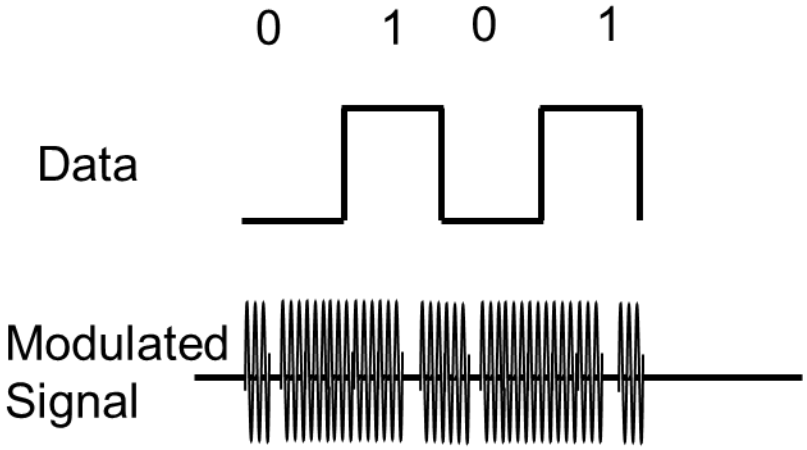


Figure 2-15. The waveform of OOK-PPM modulation.

Table 2-1. Maximum permissible exposure

		General public SAR (W/Kg)	In controlled environments SAR (W/Kg)
Whole body exposure	Whole body average	0.08	0.4
Localized exposure	Localized (peak spatial-average)	2	10
Localized exposure	Extremitiesa and pinnae	4	20

[a] The extremities are the arms and legs distal from the elbows and knees.

Table 2-2. MPE for the general public for different frequiencies

Frequency Range (MHz)	RMS electric field strength (E) (V/m)	RMS magnetic field strength (H) (A/m)
0.1-1.34	614	16.3/f
1.34-3	823.8/f	16.3/f
3-30	823.8/f	16.3/f
30-100	27.5	158.3/f
100-400	27.5	0.0729

CHAPTER 3
POWERING CIRCUTIS

3.1 Motivation

Low power biomedical implant microsystems such as those used in drug delivery, glucose sensing, neural recording, and in stimulation devices are often powered using close-proximity low frequency inductive links or far-field powering [41, 42, 43]. Wireless sensors can be divided into three categories: active, semi-passive, and passive sensors. Active and semi-passive sensors are powered by a battery, which increases the cost and size of sensors. Implantable biomedical sensors are usually constrained limited in their size and cost. Moreover, batteries must be replaced after a certain time and so aren't suitable for implant devices. Passive sensors are more attractive for these applications since they can operate without a battery. Instead, the DC power required to operate the passive sensor is generated by an integrated rectifier, which converts the incident RF signal to DC supply.

Most power interfaces for integrated biomedical implants operating in the μW to mW range employ RF-DC converters based on p-n junction diodes and diode connected MOS transistors. Schottky barrier diodes offer an alternative to the p+-n-well junction diodes or diode-connected PMOS devices fabricated in a standard n-well CMOS process. These Schottky devices exhibit higher operating frequencies and lower forward voltage drop and have been extensively used in microwave applications for rectification/detection and voltage multipliers for RFID systems [44, 45]. Unlike the standard p-n junction based diodes, the Schottky barrier diode is a majority carrier device, meaning it doesn't suffer from minority carrier storage effects and can therefore be switched faster. The fabrication of these diodes in a standard foundry CMOS process is of interest as it allows monolithic integration with both analog and digital processing circuits.

In this chapter, we discuss the implementation of a Schottky diode based RF-DC multiplier for a wirelessly powered analog frontend.

3.2 Rectifier Circuits

The rectifier circuit converts AC signal from transformer or power source into pulsating DC voltage. This circuit is generally classified into two types:

Half wave rectifier: This circuit type is simply implemented by a diode, as shown in Figure 3-1(A). The diode allows one direction current to flow into the capacitor while blocking the other direction current flow.

Full wave rectifier: This circuit type requires at least two diodes to perform full wave rectification, as shown in Figure 3-1(B). The full wave rectifier manipulates the incoming AC signal so that both halves are used to generate the output current flow in one direction.

The full wave rectifier is more efficient than the half wave rectifier, because the half wave rectifier uses only half of the incoming ac cycle and wastes all of the energy available in the other half. Rectifier circuits are widely used in inductive coupled circuits for wireless implants, because the magnetic field penetrates the biological tissue very well. However, the coupling distance is short (~ 10-50cm) because the magnetic field strength is attenuated third power of distance in near-field. The implant device operates by capturing AC signal from the external transmitter, which is amplified using a passive resonant tank and converted into useful DC power using an AC-DC converter or rectifier. For a fixed reading distance, the efficiency of this converter is crucial in determining the overall system efficiency and power requirements.

As shown in Figure 3-2, these wireless powering interfaces share a common framework that consists of a high-efficiency external transmitter, a wireless link, and a full wave bridge rectifier, which is often followed by a linear regulator and DC voltage limiter to ensure stable supply

voltage and over-voltage protection for the downstream on-chip electronics in the presence of amplitude variations due to coil or antenna misalignments.

3.3 Diode Devices

Diode devices are used to rectify the voltage in the voltage multiplier. Ideally, when the diode is forward biased, the current flows from anode to cathode. When the diode is negative biased, it blocks the current flowing back. As the RF-DC converter uses diodes, the voltage drop across them induces loss. Moreover, the rectifying devices have parasitic capacitances to the substrate, and those capacitances cause power loss, especially at high frequencies. The rectifying devices can be implemented by different types of diodes in a CMOS process. This section introduces and compares three commonly used rectify diodes.

3.3.1 P-N Diodes

A p-n diode can be fabricated by doping opposite impurities to form the p and n region of the diode. The p-n junction diode is widely used in rectifier design and is available in most CMOS processes without extra masks. However the p-n junction diode is known as a minority carrier device since the current conduction is controlled by the diffusion of minority carriers (i.e. electrons in the p region and holes in the n region) in a p-n junction diode. Therefore the p-n diode exhibits slow switching speed.

3.3.2 Diode-Connected MOS

Another widely used method in CMOS is to connect the gate and drain of the MOS transistor and use it as a diode. There is one drawback to the diode-connected NMOS, which is that it suffers body effect when the RF-DC multiplier has multiple stages. This problem can be resolved by using PMOS. However, the choice to use NMOS or PMOS depends on the process.

For instance, the NMOS transistor suffers body effect, but the threshold voltage can still be smaller than the PMOS transistor.

3.3.3 Schottky Diode

Schottky contact barrier diodes are used to implement a rectifier, as Schottky devices exhibit higher cutoff frequencies and lower forward voltage drop than p-n junction based diodes. Unlike standard p-n junction based diodes, the Schottky barrier diode is a majority carrier device, meaning it avoids the minority carrier storage effects and can therefore be switched faster. By selectively blocking the n+/p+ implants in desired diffusion areas or by directly contacting the n-well/p-well with metallization, integrated Schottky barrier diodes can be fabricated in a standard CMOS process [46, 47]. Fabricating the Schottky contact does not require any process enhancements and can be designed entirely with available process layers.

A Schottky diode can be designed with a p-n junction guard ring that terminates the perimeter with a diffused p+ region. Figure 3-3 shows the two types of Schottky diode layouts and cross sections. The guard ring reduces the reverse leakage current due to sharp electrode edge effects [48]. Using a guard ring can increase the reverse breakdown voltage and reduce the reverse leakage current. However, guard rings also reduce the forward current due to the alleviated edge effect. Depending on an application's requirements, thinking of these design features as tradeoffs can help determine whether a guard ring is appropriate when designing Schottky diodes. For example, a DC/DC boost converter requires a diode featuring a low forward voltage drop but a large reverse breakdown voltage. In this case a Schottky diode with a guard ring structure would be preferable. In a UHF RFID application, the RF-DC multiplier in the transponder uses Schottky diodes without guard ring structures, because the input amplitude is

limited and the multiplier favors less parasitic capacitance to minimize the power lost to the substrate.

3.4 RF-DC Voltage Multiplier

For those biomedical applications that require longer operation ranges (> 1m), ultra-high-frequency (UHF) transponders are preferable with far-field region. The one-stage rectifier for the UHF transponder is not usually used because the input amplitude coupling from the antenna is very small. Unlike the inductive coupled transponder, which can provide induced amplitudes of several volts, the amplitudes induced in input of the UHF transponder is usually less 200 mV. The RF-DC multiplier is required to provide sufficient DC voltage for the UHF transponder.

3.4.1 Basic Operations

Figure 3-4 shows a basic one-stage voltage doubler, which consists of two diodes and two capacitors. When the voltage drop across the diode is larger than the diode's threshold voltage, it conducts current that charges the capacitor. One stage of the voltage doubler consists of a clamping circuit and a rectifying circuit. The clamping circuit is used to build DC voltage across the coupling capacitor when the input signal is in the negative cycle. In the positive cycle, the voltage amplitude at the clamping circuit's output becomes the sum of the input amplitude and the DC voltage generated across the coupling capacitor. At the same time, the rectifying circuit is on and passing current to charge the storage capacitor. Ideally the output DC voltage amplitude of a one-stage rectifier is two times the peak amplitude of the input signal, but the voltage is usually lower than that due to the device's nonzero turn-on voltage and reverse leakage current and due to capacitor parasitics. If there is no loading in the output, the maximum output DC voltage for one-stage voltage doubler is approximately

$$V_{OUT} = 2 \times (V_{IN} - V_D) \tag{3-1}$$

The RF-DC multiplier cascades multiple one-stage voltage doublers to generate higher output voltage while reducing the required input amplitude, which improves the passive transponder sensitivity. This is a key building block in the passive transponder. The major challenge is to increase the efficiency while providing the minimum DC voltage and current to operate the integrated circuit on the transponder. Figure 3-5 shows a schematic of a three-stage full-wave RF-DC converter. The full-wave rectifier uses both the positive and negative cycles of the differential signal, thereby decreasing the minimum required input power to generate a certain DC output level. To decrease the power loss to the substrate, a metal-to-metal flux capacitor is utilized. Rectifier design is of significant importance to low input sensitivity. To minimize the output voltage ripple, the capacitor in last stage is sized large enough so that the time constant is much larger than the input signal period.

3.4.2 Analysis and Design Procedure

The RF-DC multiplier is similar to the AC-DC charge pump proposed by Dickson in 1976. The output voltage of the Dickson's AC-DC charge pump is given by [49]

$$V_{OUT} = N \cdot (V_{IN} \cdot (\frac{C_C}{C_C + C_P}) - V_D) - \frac{I_L \cdot N}{C_C \cdot f} \tag{3-2}$$

where N is number of diodes, V_{IN} is the amplitude of input voltage, C_C is the coupling capacitor, C_P is the sum of the diodes' parasitic capacitances, I_L is the load current, and f is the input frequency. Equation 3-2 considers the voltage drop of each diode is constant that is true when the input voltage is much larger than the turn-on voltage or threshold voltage of the diodes. Moreover, the reverse current and the substrate power loss are ignored in equation 3-2. The input amplitude is usually smaller than the turn-on voltage for the RF-DC multiplier for a UHF transponder. As a result, equation 3-2 is less accurate. This section develops a new design procedure for RF-DC multipliers.

To achieve a higher voltage conversion efficiency, equation 3-2 indicates that we should select a coupling capacitor (C_C) that is larger than the parasitic capacitor (C_P). As a result, in the high frequency analysis, the coupling capacitors are considered short circuits. Therefore, the diodes are arranged in parallel or anti-parallel to the input of the RF-DC converter. On the other hand, the diodes are in series with the output because the coupling capacitors are open circuits in DC analysis. Assuming the input signal is sinusoidal. Given the required output DC voltage (V_{OUT}), the voltage (v_D) across each diode in a full wave RF-DC multiplier is given by [50, 51]

$$v_D = \pm v_{IN} \sin(2\pi ft) - \frac{V_{OUT}}{4N} \tag{3-3}$$

Figure 3-6 shows the analysis of N-stage RF-DC multiplier. Using the given output voltage doesn't give enough information to design the RF-DC multiplier because the multiplier's output is a resistive load. So to complete the design, we must also specify the load current. As we can see when the multiplier reaches steady state, the total charge generated from a diode in one clock period cycle equals the total charge delivered to the load in one clock cycle. That behavior is given by

$$\int_o^T I_D(v_D)dt = I_{OUT}T \tag{3-4}$$

The diode current is expressed in

$$I_D = A \cdot J_S \left(e^{\frac{nV_D}{V_T}} - 1 \right) \tag{3-5}$$

where A is the diode device's area, J_S is the saturation current density, and V_T is the thermal voltage. Equation 3-4 is valid for a pn or Schottky diode. If we use a diode-connected MOS, then equation 3-4 needs to be modified. By combining equation 3-3, 3-4, and 3-5, equation 3-4 can be expressed as

$$\int_0^T A \cdot J_S \left(e^{\frac{n.v_D}{V_T}} - 1 \right) dt = I_{OUT} T \tag{3-6}$$

From equation 3-2, vd is a function of the input amplitude, number of stages, and output voltage. Moreover, the current is a function of vd and the area of the diode. Therefore, to meet the load constraints, V_{OUT} and I_{OUT}, the three design variables are diode area A, number of stages N, and input voltage amplitude V_{IN}. We seek to derive an expression relating the minimum input amplitude as a function of these three design variables. Figure 3-7 illustrates the charge conservation for a one-stage voltage doubler. The analysis considers two current components: the forward current and the reverse current.

To accurately present the diode's current and voltage in different regions, we can use the measured or simulated I-V characteristics of the diode to replace the left side term in the integral in equation 3-6. Then we can develop a MATLAB code to do a numerical iteration to find the required number of stages and diode area for a given load. As shown in equation 3-3, the voltage drop of the diode is a function of the number of stages and the input amplitude. The frequency and output voltage are already specified. The process sweeps the two variables, input amplitude and number of stages, to find the current associated with the voltage drop across the diode from the measured I-V data. The derived current needs to satisfy the charge conservation as shown in equation 3-6. In this way we can find the required area for each diode. However, the results can give several solutions that satisfy the load requirement. To find the minimum transponder sensitivity, we need to consider the input matching in the interface, so the input impedance of the multiplier is derived in the design procedure.

The RF-DC multiplier's input impedance consists of resistive and capacitive components. The power PD consumption on each diode can be presented as equation 3-7, and the total input

power, which is equal to total power consumption on the diodes and load in one period, can be presented as equation 3-8. The factor 4 in equation 3-8 is for the full-wave rectifier. Therefore, we can find the chip input resistance R_{IN} as shown in equation 3-9.

$$P_D = \int_0^T I_D \cdot V_D dt \tag{3-7}$$

$$P_{IN} = 4 \cdot N \cdot P_D + I_{OUT} \cdot V_{OUT} \tag{3-8}$$

$$R_{IN} = \frac{V_{IN}^2}{2P_{IN}} \tag{3-9}$$

The input capacitance consists of parasitic capacitance (C_P) associated with the coupling capacitor and the capacitance (C_D) associated with the depletion region.

$$C_D = \int_0^T C_D(vd)dt \tag{3-10}$$

The total capacitance of the multiplier is given by

$$C_{IN} = 4 \cdot N \cdot (C_D + C_P) \tag{3-11}$$

and the input impedance is given by

$$Z_{IN} = R_{IN} - j\frac{1}{\omega C_{IN}} \tag{3-12}$$

Therefore, the induced input voltage can expressed as

$$V_{IN} = 2 \times V_{ANT} \times \left| \frac{Z_{IN}}{Z_{ANT} + Z_{IN}} \right| \tag{3-13}$$

where V_{ANT} is the open circuit voltage in the antenna, Z_{ANT} is the antenna's impedance, and Z_{IN} is the multiplier's input impedance.

The voltage multiplier power conversion efficiency is defined as

$$\eta = \frac{I_{OUT} \cdot V_{OUT}}{P_{IN}} \tag{3-14}$$

A design example of a full-wave RF-DC multiplier for 915 MHz ISM band with a given output load voltage V_{OUT} = 1V and I_{OUT} = 2 µA. This example uses an antenna impedance of 50 Ohm, and a P-type Schottky diode. Figure 3-8 shows the measured I-V of the P-Schottky diode with area 7.2 μm^2. The proposed design procedure can be applied to any diode device with the measured or simulated I-V data. Figure 3-9 demonstrates the required diode area, number of stages, efficiency, and power the antenna receives. The red line represents the input voltage amplitude V_{IN} for 70mV. Each blue line represents V_{IN} when increased by 10mV. The result shows a minimum sensitivity of 27.1 µW for 14 stages of multipliers to meet the required output specification.

Figure 3-10 presents another design example. With the same load power 2 µW and a load voltage of 0.5 V, the load current is 4 µA. As in the example in Figure 3-9, the input amplitude starts from 70 mV and increases by 10mV. Although the output load power is the same in both examples, the required diode area, minimum sensitivity, and efficiency are different. The design where V_{OUT}= 1 Volt and I_{OUT} = 2 µA is more sensitive than the design where V_{OUT}= 0.5 Volt and I_{OUT}= 4 µA. This is because a larger diode area is required to deliver the load current. Moreover, the first case shows a better power conversion efficiency.

3.5 Antenna Consideration

A wireless passive transponder uses an antenna to receiver power and converter to AC voltage to RF-DC multiplier. The antenna impedance consists of a resistive component and a reactance component. Since the input impedance of the RF-DC multiplier is usually capacitive, it's preferable that the antenna's reactance be inductive to cancel the capacitive load. The resistive component consists of a radiation resistor and a loss resistor. The radiation resistance is modeled the radiation behavior in the antenna. When electrons are accelerated in the antenna, the

electrons generate electromagnetic fields radiating outward. The electromagnetic waves take energy from the electrons. The loss of energy is analogous to ohmic resistance. When the antenna is used to capture power, the higher radiation resistance gives a larger induced open circuit voltage, which is more desirable. The loss resistance presents the power loss as heat in the antenna. Therefore, the efficiency of the antenna is given by

$$\eta_{ANT} = \frac{R_r}{R_r + R_l} \tag{3-15}$$

where R_r is the radiation resistance and R_l is the loss resistance.

3.6 Transponder Sensitivity

As shown in the design example, the RF-DC multiplier requires a minimum input power to operate the IC by a given load power. The minimum input power is defined as the chip sensitivity. Since the transponder consists of an antenna and chip, the transponder sensitivity depends on the antenna's radiation resistance, the input match, and the chip sensitivity. Therefore, the transponder's sensitivity is given by

$$P_{ANT} = \frac{P_{IN,MIN}}{(1 - \left(\left| \frac{Z_{ANT} - Z_{IN}}{Z_{ANT} + Z_{IN}} \right| \right)^2)} \tag{3-16}$$

3.7 Experiments

Here, we present the measured results of the Schottky diode and multiplier.

3.7.1 Schottky Diodes

To evaluate the I-V characteristics of the Schottky diode, several diodes of different cross sections were laid out in a 0.6μm n-well and a 130nm twin-well standard CMOS process. The AMI 0.6μm n-well CMOS process is a titanium polycide process, so the silicon surface doesn't have a silicide compound. The Schottky diode's effective area is the VIA metal contact area. In

the UMC 130nm, this process is silicide process. On top of the silicon, there is silicide compound layer, and this layer forms the Schottky barrier contact with the lightly doped silicon. The effective area of Schottky diode is the lightly doped area. Diodes are fabricated with small Schottky contact areas [52] as this yields a higher cutoff frequency, and multiple cells are placed in parallel to improve the current handling capability.

The measured forward current and reverse current density-voltage (J-V) curves for the Schottky barrier diodes in AMI C5 process are shown in Figure 3-11. Two shapes of Schottky diodes are fabricated to explore the performance. The first one is laid out by following the design rule, so the standard sized contacts form the Schottky diode. The second one provided by the foundry is laid out with design rule violation. As shown in Figure 3-12, the second one's contact is laid out in a rectangle shape. When the effective Schottky contact area is the same, the first case consumes more area. However, the first shows better forward current density and small reverse current leakage.

The parameters of the fabricated Schottky diode can be extracted from the measured J-V characteristics. The barrier height is computed using the Richardson-Dushman equation for the thermionic current [53],

$$\phi_B = V_T \cdot \ln(\frac{A^* T^2}{J_{S0}}) \tag{3-17}$$

and the ideality factor is calculated with

$$n = \frac{\Delta V_B}{V_T \ln(\Delta J_S)} \tag{3-18}$$

In equation 3-17 ϕ_B is the barrier height, V_T is the thermal voltage, A* is the effective Richardson constant, J_{SO} is the zero bias current density, and T is the absolute temperature. In equation 3-18 n is the ideality factor, and ΔV_B and ΔJ_S are the measured differences in forward

bias voltage and current density. From euqation 3-17 and 3-18, the calculated barrier height is 0.72 eV for Vendor design rule and 0.64ev for the Standard design rule. The ideality factor is 1.12 for Vendor design rule and 1.08 for the Standard design rule. Table 3-1 summaries the calculated Schottky diode parameters from the measured J-V characteristics.

Due to the availability of the triple-well process on a UMC 130nm CMOS process, we implement 4 types of Schottky diodes: P-type Schottky diode without guard ring, P-type Schottky diode with guard ring, N-type Schottky diode without guard ring, and N-type Schottky diode with guard ring. Figure 3-11 shows the layout and measured J-V characteristics of the 4 types of Schottky diodes. The Schottky diode effective area is the area of the active region on the lightly doped area. From the measured results, the Schottky diodes with guard rings have better reverse breakdown voltage performances for both types of diodes. Table 3-2 summaries the calculated Schottky diode parameters from the measured J-V characteristics.

3.7.2 HF Voltage Multiplier

To evaluate the performance of different Schottky diodes, four three-stage full-wave LF multipliers are fabricated, each of which is implemented in a UMC 130nm CMOS process using one of the four Schottky diodes. The area of the Schottky diode is 144 μm2 and the coupling capacitor is 3.5 pF. Figure 3-13 shows the die photo of the multiplier. Given input power -5 dBm and load 1 MΩ, Figure 3-14 shows the measured multiplier output voltage vs. frequency. The rectifier with the P-type Schottky diode without guard ring provides the highest voltage output, because it has the largest forward current density of these four Schottky diodes.

3.7.3 RF-DC Multiplier

In this section, a RF-DC half-wave multiplier chip is designed. It provides a 1 Volt DC output voltage at 217 kΩ resistive load, and the source resistance is 50 Ω. Figure 3-15 presents

the optimized results, and the RF-DC multiplier uses 16 stages. A test chip was designed and manufactured in a 130 nm CMOS process with the low V_T diode connected MOS to evaluate the design procedure for UHF RFID applications. Figure 3-16 shows the micrograph of the half-wave multiplier. The overall test chip size is 1610 µm x 520 µm, while the area of the RF-DC multiplier is 1610 µm x 520 µm. The half-wave RF-DC converter consists of 16 stages of voltage doublers. The aspect ratio of the low V_T diode connected MOS is 60 µm/0.12 µm and the coupling capacitor is 2.714 pF. Although the design results show that 47 µm/0.12 µm for a 16-stage RF-DC multiplier, the Spectre simulation shows 60 µm/0.12 µm can meet the output requirements. This design procedure provides design tradeoffs among diode size, the number of stages, input power, and conversion efficiency based on diode's IV characteristics, but the final design still needs to be simulated with CAD tools.

The chip is directly measured by a probe with a single-tone continuous-wave (CW) 50-Ω source at 915 MHz, and there is no any matching network between the chip and RF signal generator. Figure 3-17 shows both the simulated and measured results for the rectifier output voltage vs. input power at 915 MHz. Figure 3-18 shows the measured input impedance vs. different input power at 915 MHz with an output load of 217 kΩ. Figure 3-19 presents the measured input impedance vs. different frequency at -10 dBm input power with an output load of 217 kΩ.

To provide maximum power transfer, the input impedance needs to be transformed to match the source impedance of 50 Ω. Figure 3-20 shows the measured input impedance vs. frequency. In Figure 3-21, the matching network design starts from the load impedance 33 - j73 and is in series with an 8 nH inductor that models the bonding wire. We use an L-matching network to bring the load impedance to 50 Ω. The L-matching network is a 10 nH shunt inductor and then a

33 pF series capacitor. Figure 3-22 shows the test board with the RF-DC multiplier chip and input matching network. After the matching network, the measured input impedance is 48.2 + j5.8, which is close to the source impedance as shown in Figure 3-23. Figure 3-24 presents the input impedance vs. input power both with and without the matching network at -10 dBm input power and 217 kΩ load resistance.

From Figure 3-25, the output voltage of RF-DC multiplier is increased using the input matching network. To reach the output voltage 1.1 volt at 217 kΩ load, the sensitivity improves from -11.02 dBm to -12.65 dBm. The measured power conversion efficiency for 1.1 Volt at 217 kΩ load is 10.3% with the matching network and 9.03% for without it.

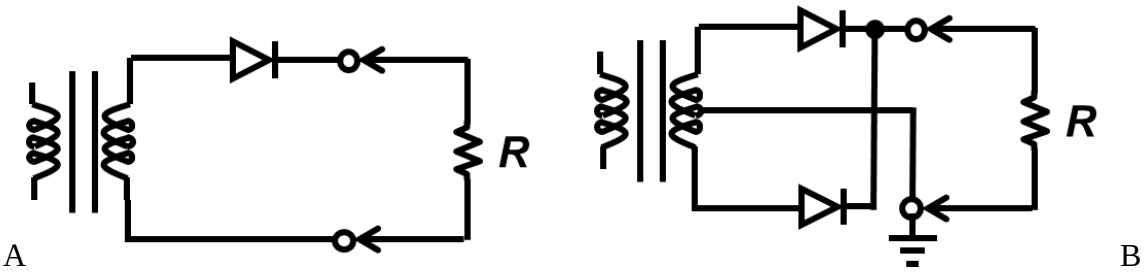


Figure 3-1. Rectifier circuits. A) Half wave rectifier. B) Full wave rectifier.

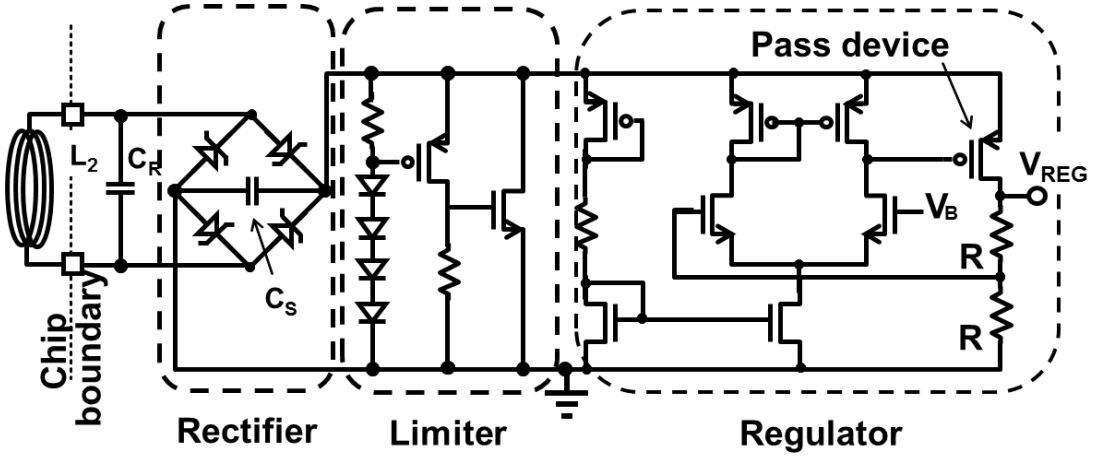
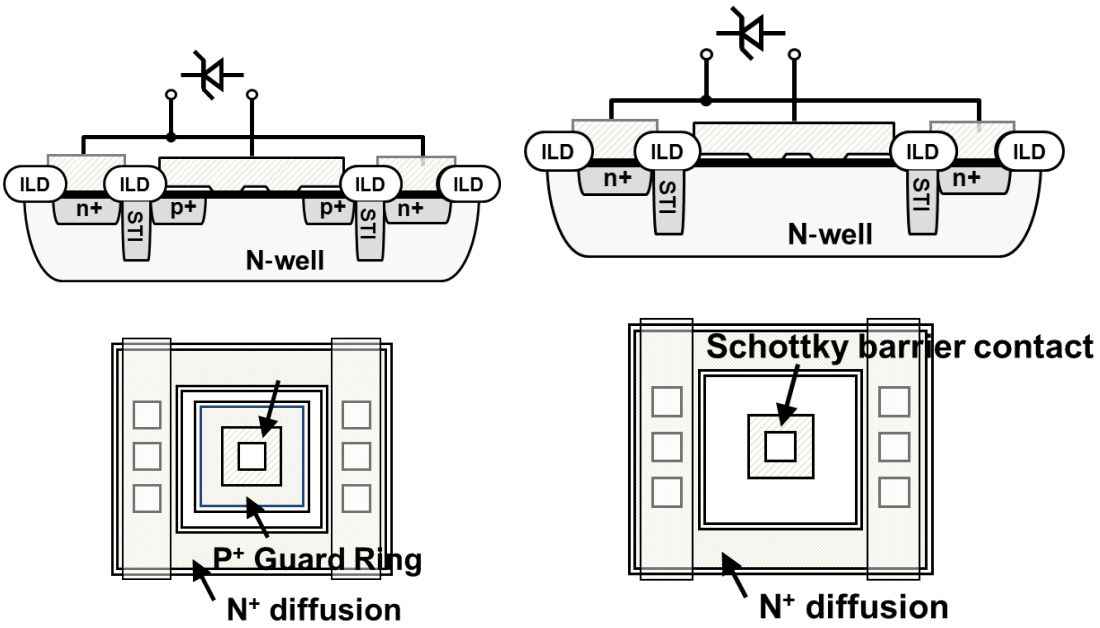


Figure 3-2. Block diagram of a typical wireless power interface frontend for biomedical implants.



A B

Figure 3-3. Cross section and layout of A) n-type Schottky diode with guard ring. B) n-type Schottky diode without guard ring.

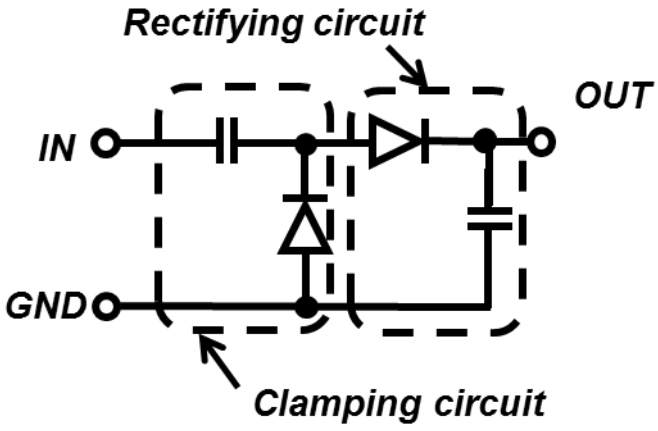


Figure 3-4. One-stage voltage doubler.

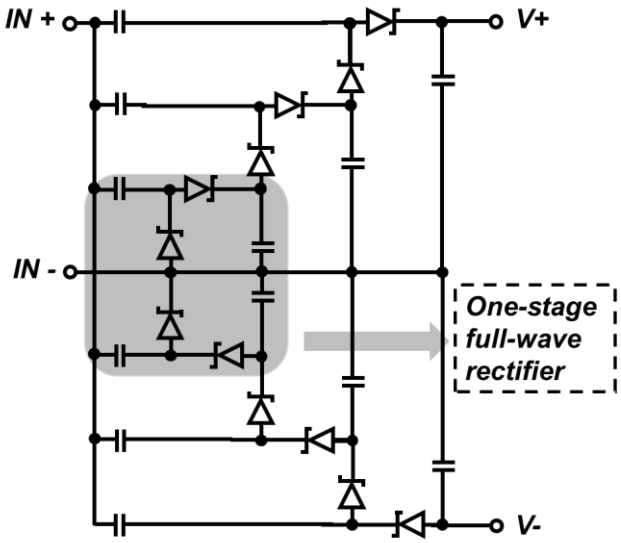


Figure 3-5. The schematic of three-stage full-wave RF-DC converter.

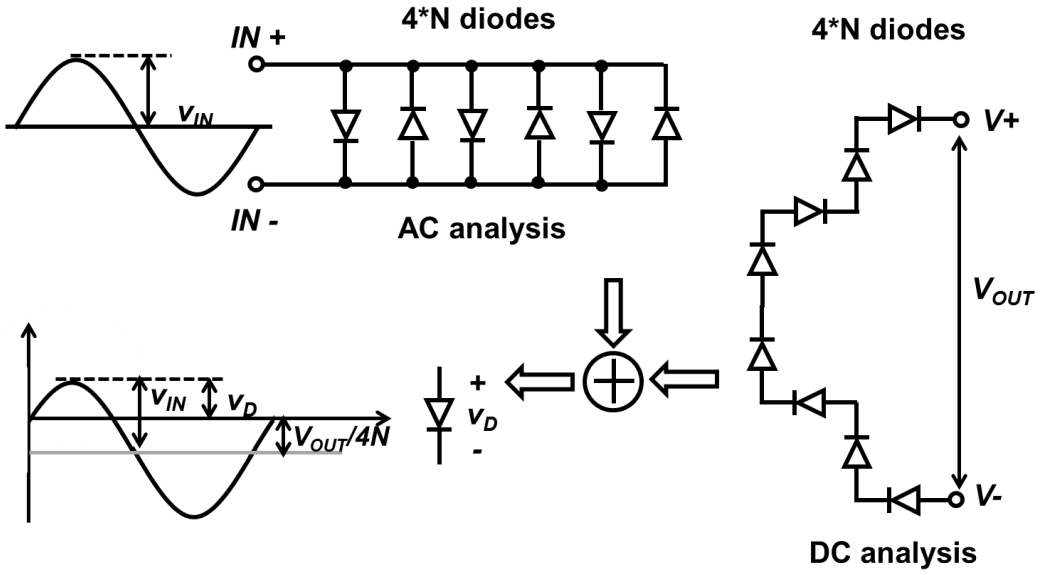


Figure 3-6. The analysis of N-stage RF-DC multiplier.

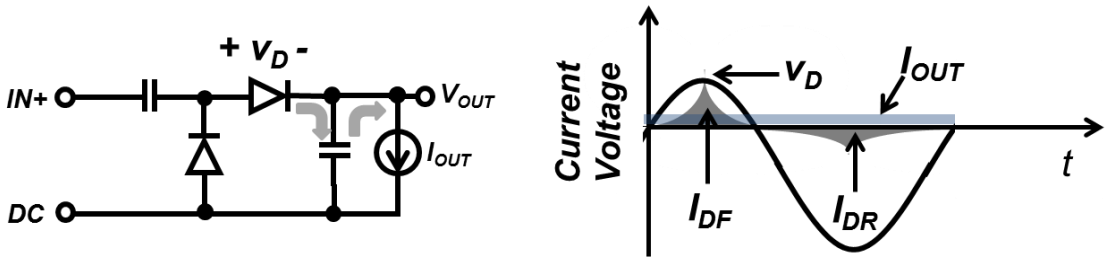


Figure 3-7. Charge conservation in steady state.

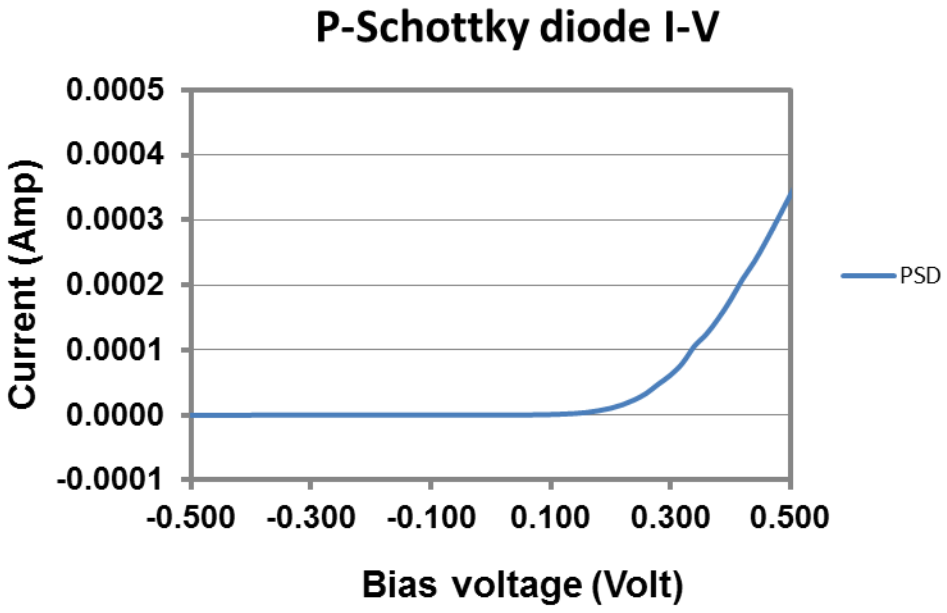


Figure 3-8. Measured I-V of P-type Schottky diode.

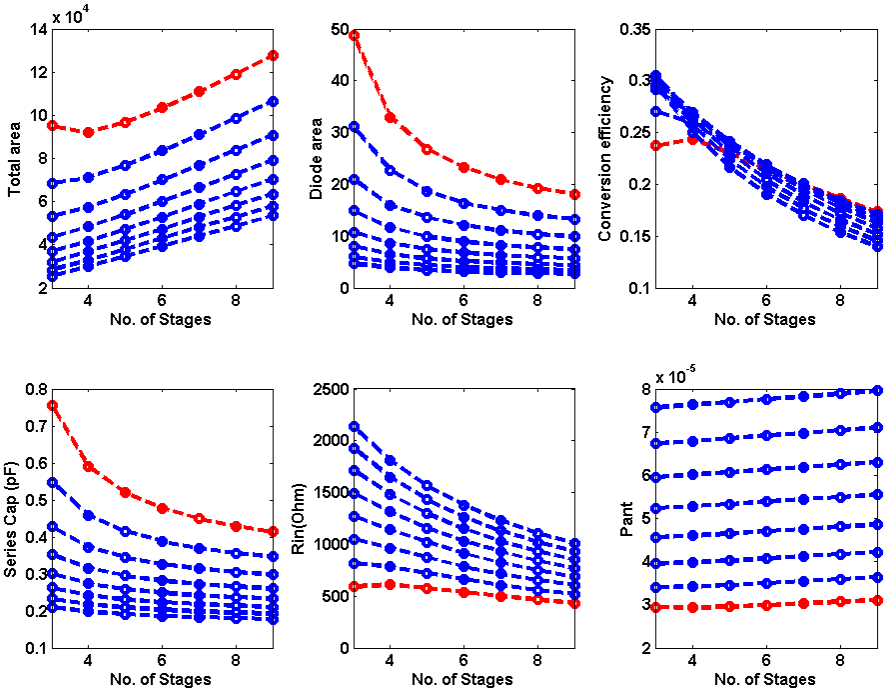


Figure 3-9. RF-DC multiplier design for V_{OUT} =1 V and I_{OUT}=2 µA.

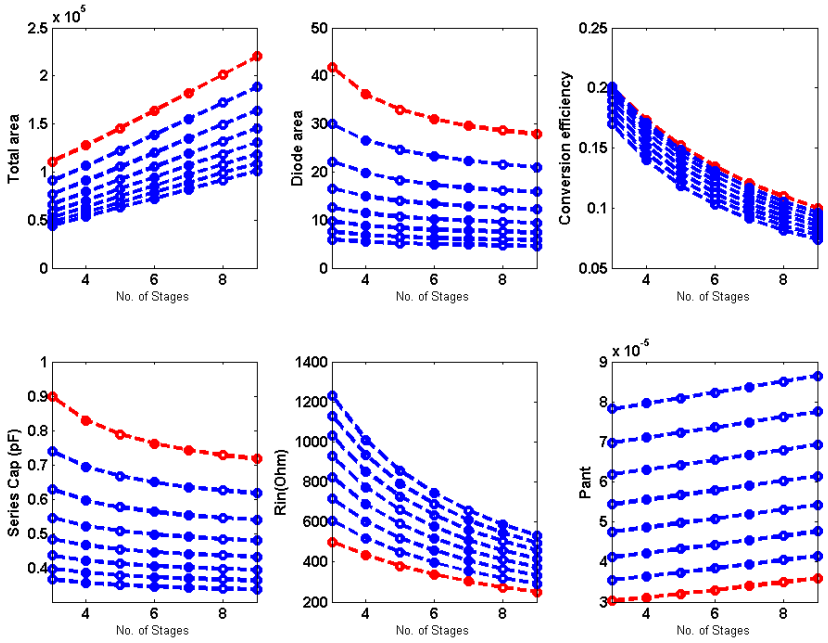


Figure 3-10. RF-DC multiplier design for V_{OUT} =0.5 V and I_{OUT}=4 µA.

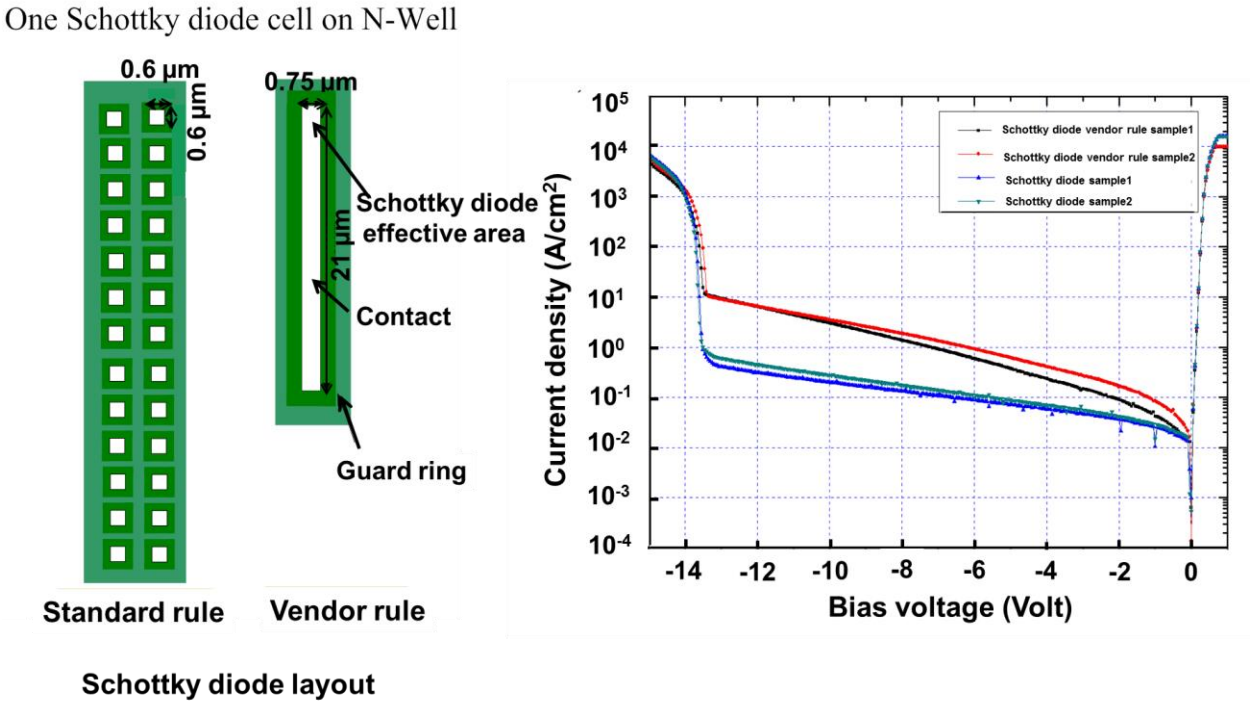


Figure 3-11. Schottky diode layout and measured Schottky diode current density vs. bias voltage in AMI 0.6 µm CMOS process.

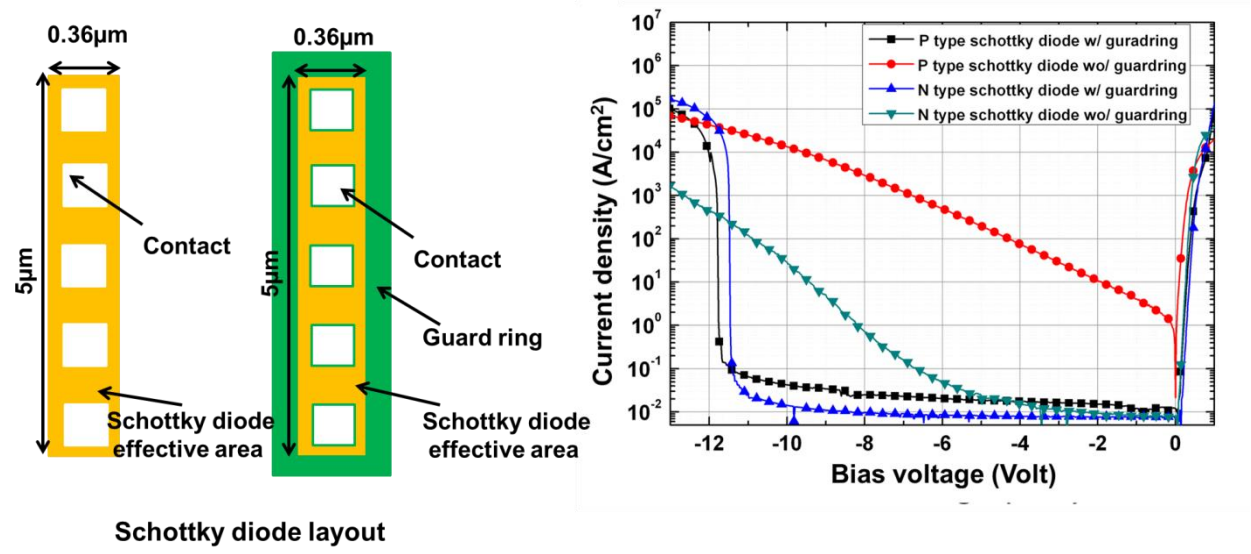


Figure 3-12. Schottky diode layout and measured Schottky diode current density vs. bias voltage in UMC 130 nm CMOS process.

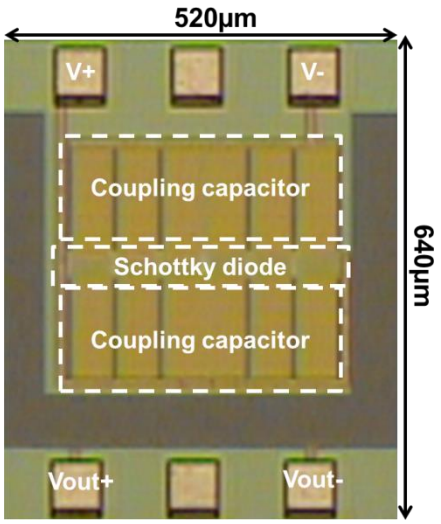


Figure 3-13. Die photo of the three-stage full-wave HF voltage multiplier.

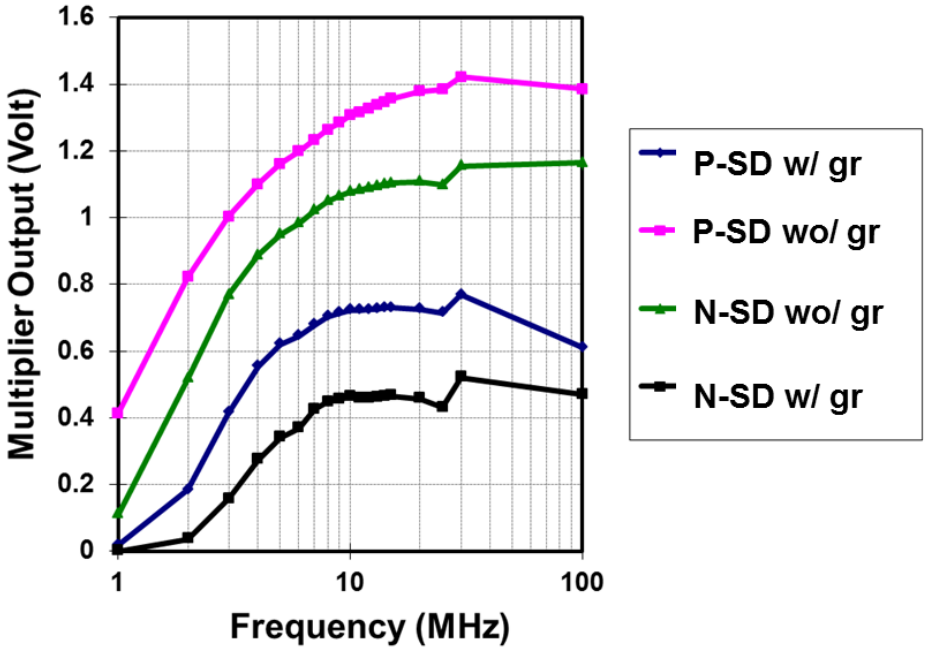


Figure 3-14. The measured multiplier output voltage vs. frequency.

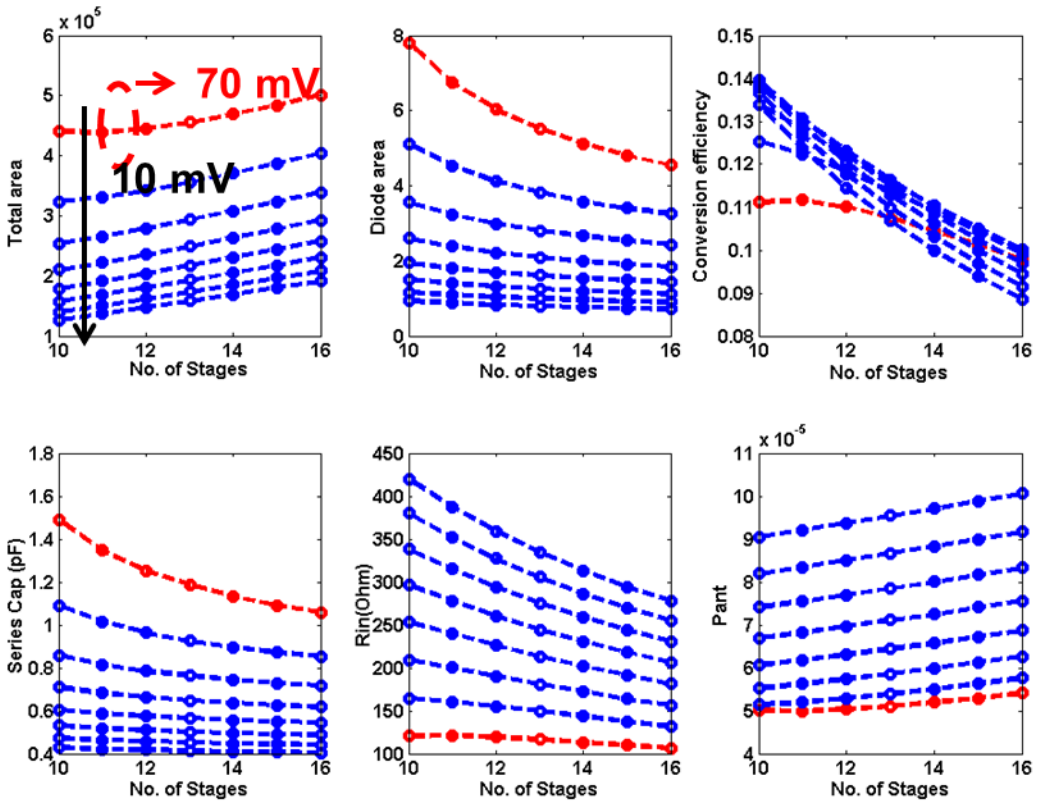


Figure 3-15. RF-DC multiplier design for V_{OUT} = 1 V and RLOAD = 217 kΩ.

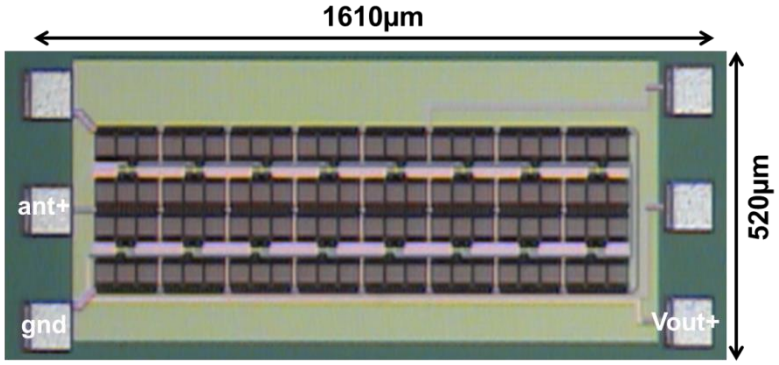


Figure 3-16. Die photo of the 16-stage half-wave RF-DC multiplier.

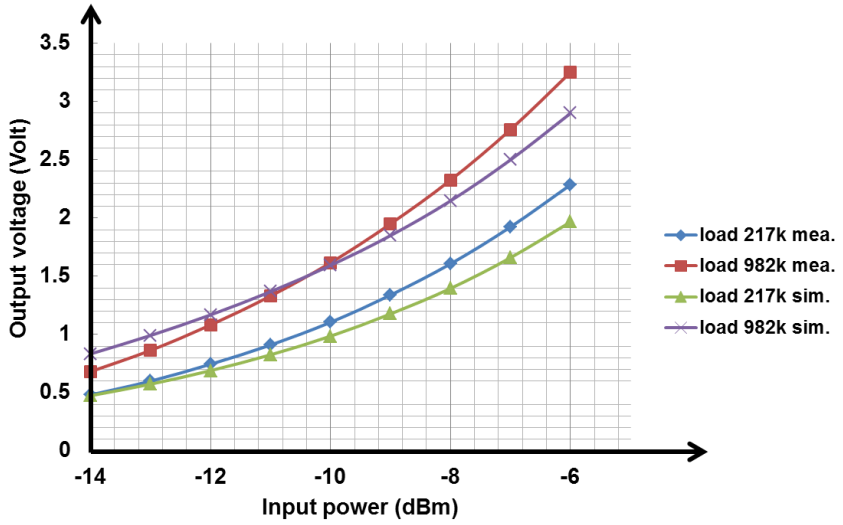


Figure 3-17. The measured and simulated multiplier output voltage vs. input power.

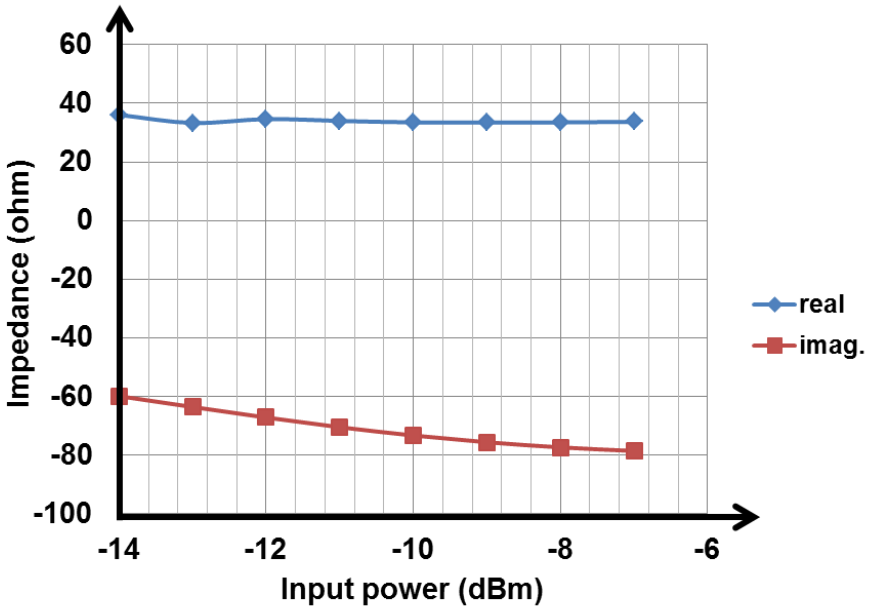


Figure 3-18 Input impedance vs. input power.

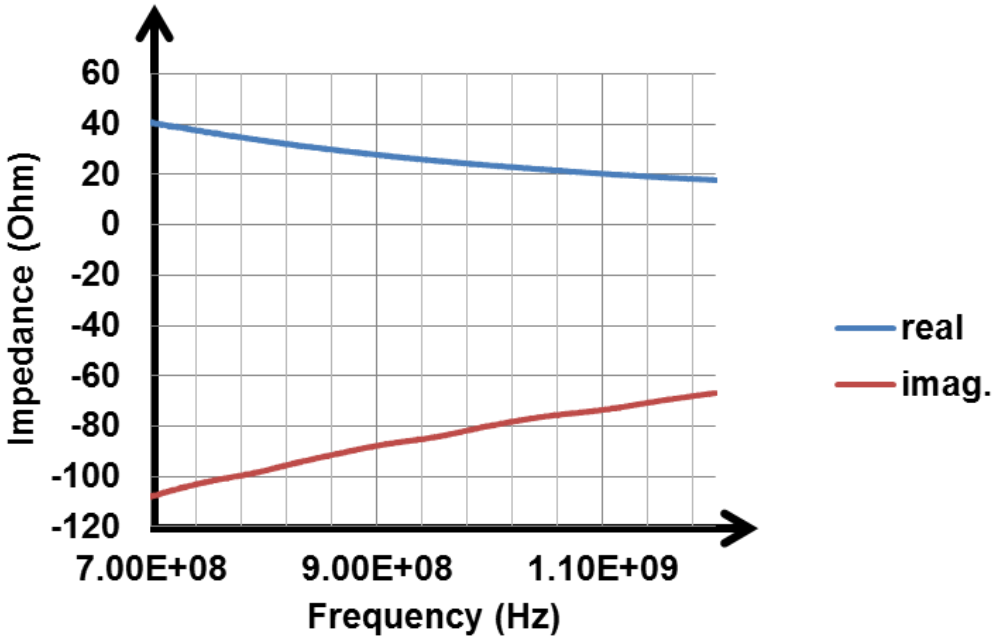


Figure 3-19. Input impedance vs. input frequency.

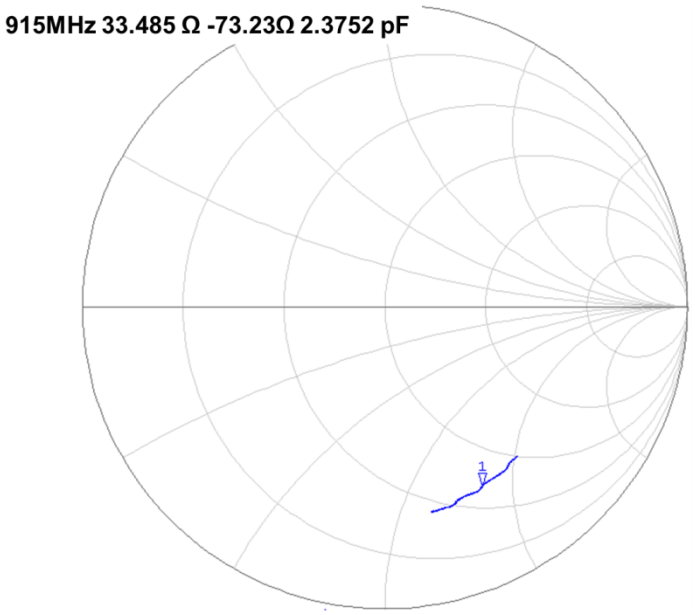


Figure 3-20. Input impedance vs. input frequency on Smith chart.

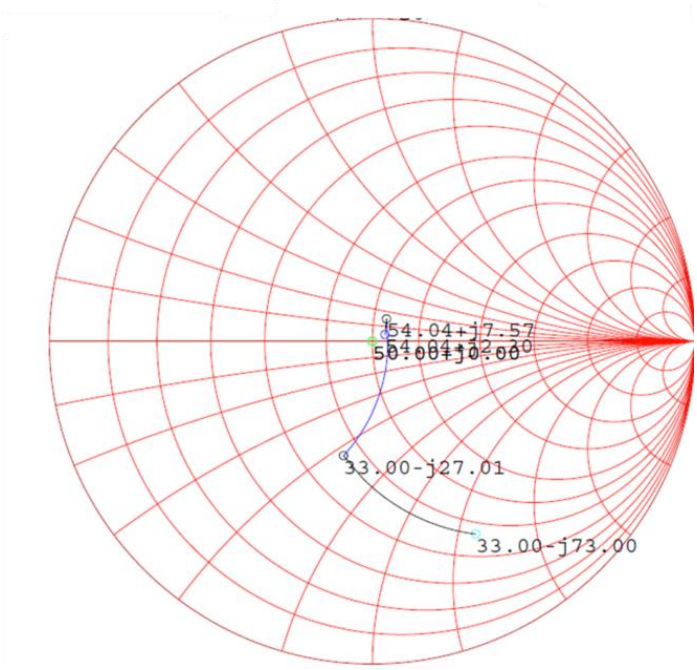


Figure 3-21. Matching network design.

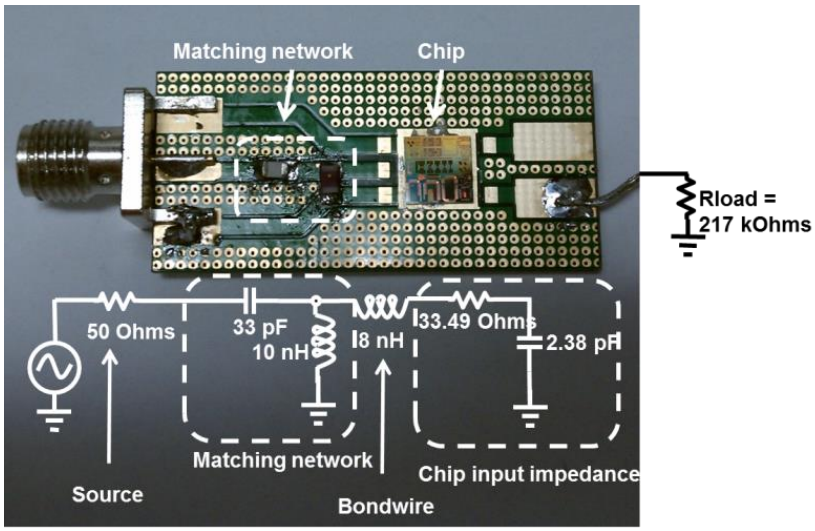


Figure 3-22. The RF-DC multiplier with input matching network.

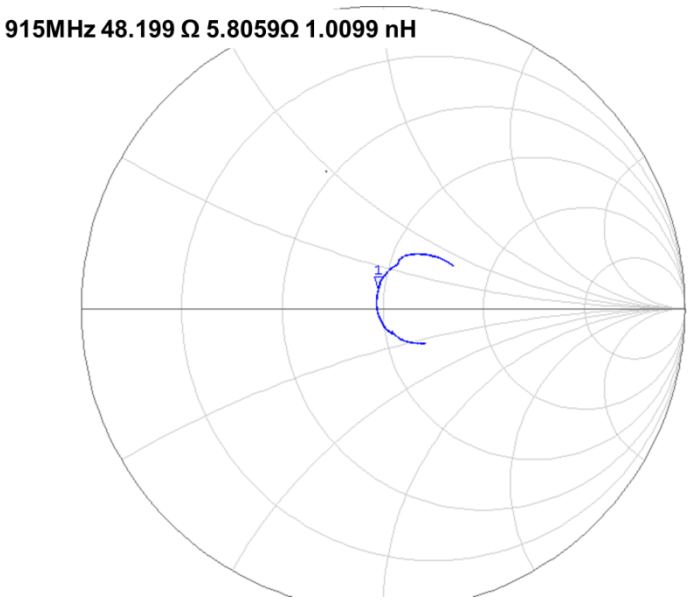


Figure 3-23. Input impedance vs. input frequency with input matching network on Smith chart.

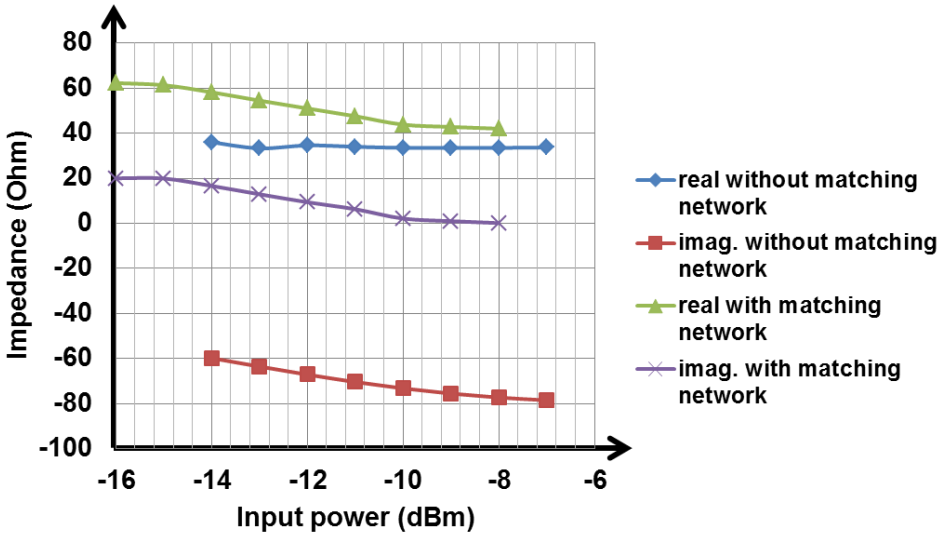


Figure 3-24. Input impedance vs. input power for -10 dBm input power at 217 kΩ.

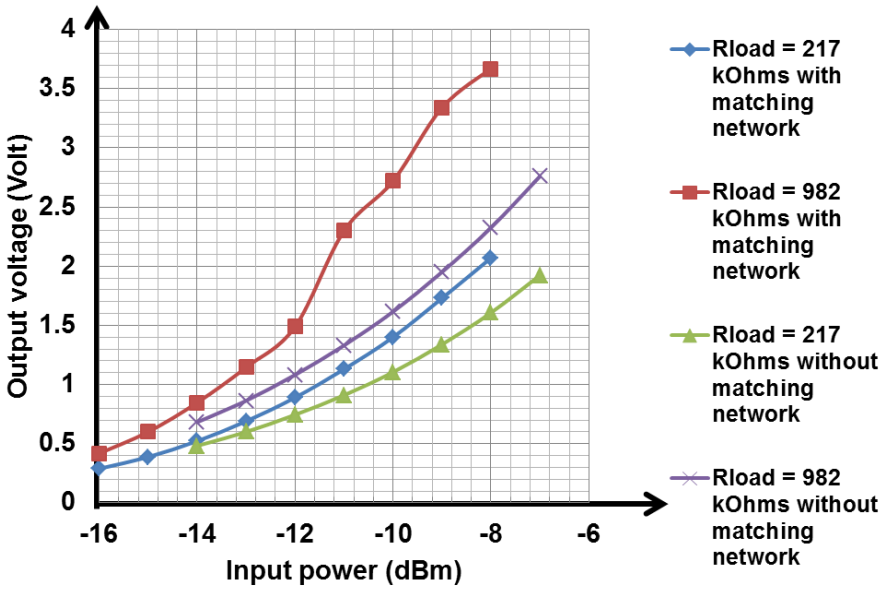


Figure 3-25. The measured multiplier output voltage vs. input power.

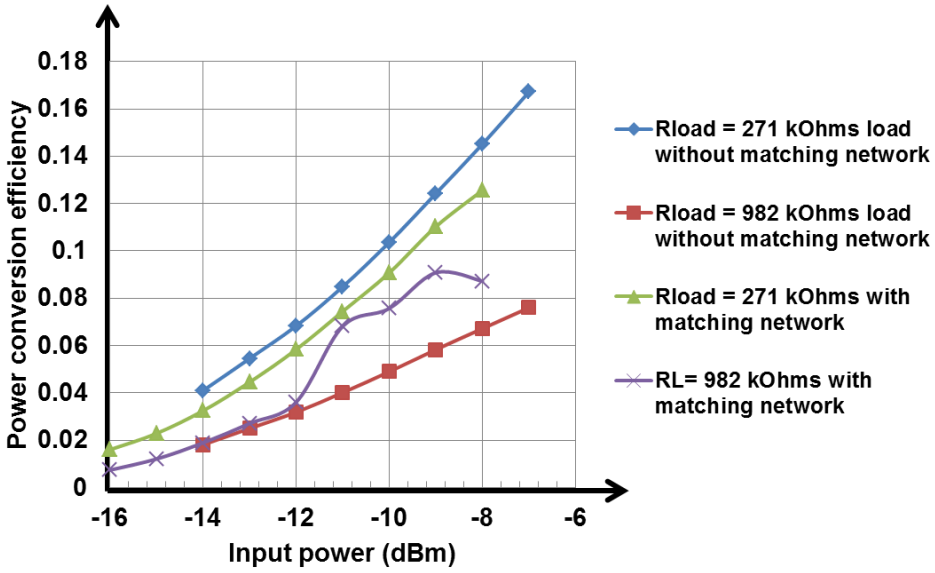


Figure 3-26. The measured multiplier output power conversion efficiency vs. input power.

Table 3-1. Summary of measured Schottky diode performance in AMI C5 process

	Schottky diode Vendor rule design rule	Schottky diode Standard design rule
Ideality factor	1.12	1.08
Zero bias current (A/cm^2)	0.000136	0.000987
Barrier height (eV)	0.72	0.64
Reverse breakdown (V)	-13.5	-13.4
Reverse leakage current @1V (A/cm^2)	12.05	13.6

Table 3-2. Summary of measured Schottky diode performance in UMC 130 nm CMOS process

	P-Schottky diode without guardring	N-Schottky diode without guardring	P-Schottky diode with guardring	N-Schottky diode without guardring
Ideality factor	1.54	1.4	1.24	1.04
Zero bias current (A/cm^2)	0.0215	0.0082	0.0095	0.0066
Barrier height (eV)	0.52	0.54	0.536	0.546
Reverse breakdown (V)	-0.5	-5.2	-11.7	-11.5
Reverse leakage current @1V (A/cm^2)	4.11	0.0083	0.0023	0.0077

CHAPTER 4
A 0.3-V, 200-NW DIGITAL PHASE-LOCKED LOOP AND A DUAL-SUPPLY OUTPUT RF-DC VOLTAGE MULTIPLIER FOR UHF PASSIVE TRANSPONDERS

4.1 Motivation

Passive RF transponders have been used in a variety of ways in many applications, for instance biosignal recording and wireless sensor nodes. A clock generator is required in the passive transponder to decode the downlink data, modulate the baseband data, and clock analog and digital building blocks.

The major challenges are the frequency stability and power consumption. The clock frequency drifts with process, voltage, and temperature (PVT) variation, which results in synchronization failure between the tag and the reader. Thus, the reader is unable to recover the backscattered data and the tag itself cannot decode tag parameter instructions. Published solutions to deal with this variation include temperature compensation, injection locking, post-fabrication trimming, and preamble training. [54] uses an injection lock divider, which derives the tag's clock from the high frequency carrier (950 MHz); however, the power consumption of this clock generator is 7 μW, which is unsuitable for passive transponder applications. In [55], the proposed solution uses a VCO accompanied by a digital calibration circuit, which together consume nearly 31 μW. The calibration scheme employs a counter on the transponder to count a series of pulses from the reader. Each pulse has enough long time period than the on-chip oscillator output clock period. The on-chip clock counts each pulse and then adjusts the current of the current starved oscillator to change the frequency. However, over time the transponder's clock frequency may drift from the calibrated point. It requires recalibration, which is inefficient. A training process (12.5 μs delimiter) was proposed after calibration in [56], however, like other approaches the clock frequency is prone to environmental variation. Several RFID protocols, such as EPC Gen2, use a higher clock frequency to resolve the timing difference between data-0

and data-1 without calibration or compensation processes. The EPC Gen2 protocol uses a reader-to-tag calibration symbol (RTcal) as a reference for the signal processor to differentiate between data-0 and data-1. To successfully decode the downlink data, the required clock frequency to resolve RTcal /2 is 1.28MHz. This protocol provides a calibration free solution, but the required high frequency is proportional to the data rate, so this protocol consumes more power and reduces the tag's sensitivity in high data rate applications. In [57], the proposed FLL continuously calibrates the clock generator frequency with EPC Gen2 standard by counting Tari to counter the clock frequency drift. However, during the PW period in Tari symbols, there is no power available to the transponder. The width of PW is 0.5 Tari for data-0 and is normally around 0.25 Tari for data-1. This puts stringent power constraints on the transponder. As a consequence, for power stringent applications, the approaches presented above are unsuitable.

We propose a ~200 nW on-chip clock generator based on a digital phase locked-loop (DPLL) operating in the subthreshold region. The reference clock is extracted from the small duty cycle on-off keying (OOK) RF carrier, and therefore the available power to the transponder is more continuous. This clock also synchronizes communication functions between the reader and the passive transponder.

To further minimize the clock generator power consumption, we propose a new power management strategy to maximize efficiency. To improve the RF-DC conversion efficiency, the RF-DC multiplier can use Schottky diode or low-VT MOS. In addition, the efficiency of the DC-DC converter after the RF-DC multiplier must be high. As the complexity of RFID systems increases with the addition of digital processing and supplementary analog blocks, the power constraints for each subsystem become more stringent. In a bio-signal application, the analog modules require a higher voltage to operate. On the other hand, digital modules can use

subthreshold logic to operate at lower voltages to reduce power consumption. There are two traditional ways to simultaneously deliver these separate output voltages. One option is to use a charge pump circuit that boosts the low output voltage from an RF-DC multiplier to a higher voltage for the analog block with the digital blocks directly using the low voltage. Alternatively, an RF-DC multiplier can generate the high voltage level for the analog supply, which is then stepped down to the lower voltage using a buck converter. However, both methods degrade the overall RF-DC conversion efficiency. Thus, it is desirable to use a single RF-DC converter efficiently deliver multiple supply voltages so as to independently optimize the power consumption of the digital and analog supply modules.

In this chapter, we propose a power management block that efficiently generates dual regulated supply voltages from a single RF-DC converter block, supporting low voltage digital processing blocks at V_{REGL}~290mV and analog circuits at V_{REGH}~760 mV.

4.2 System Architecture

Figure 4-1 shows a block level drawing of the proposed transponder architecture, including the proposed power management unit (PMU) with dual regulated supply, a power level detector, an envelope detector with embedded modulator charge injection and clock feed-through cancelling switch and filter, the subthreshold clock multiplier unit (DPLL), and a backscattering modulator with on-chip PRBS.

The DC power supplies are generated by rectification and boosting of the RF carrier through a diode-multiplier with corresponding storage capacitors. The design uses linear regulators and a DC voltage limiter to provide stable DC voltages to the analog and digital blocks with protection from system over-voltage damage. The proposed transponder employs the DPLL as the on-chip clock generator. The reference clock for the DPLL is derived from a low-

frequency amplitude modulated signal (5-20 kHz) embedded in the RF carrier, which the reader continuously sends. The power detector block continuously monitors the voltage level across each storage capacitor. Once this voltage reaches a pre-programmed threshold, both the DPLL and backscattering modulator are enabled, allowing for data communication between the transponder and the reader. By enabling the backscattering switch only after receiving sufficient power, we can ensure the DPLL output frequency operates within the designated range (385 kHz-1.54 MHz). This minimizes power supply activation and system start-up times while also eliminating the possibility of system failure when the backscattered signal is at a similar frequency to that of the modulated reference. Under these conditions, the system may never capture enough energy to be properly powered. During backscattering, the PRBS data modulates the DPLL output clock. If no measures are taken, this modulation will pass through the envelope detector and change the reference frequency of the PLL causing it to lose its lock. This is highly undesirable, and to address this issue, we use a sense amplifier flip-flop (SAFF) to store the state of the envelope detector output each time the backscattering switch closes. Thus, when the modulator output is high or the antenna port is shorted, the SAFF holds the previous value, keeping the received DPLL reference clock (CKRX) stable. Figure 4-2 shows the proposed block diagram of the demodulator and the timing waveform of operation.

4.3 Circuit Implementation

4.3.1 Sub-Threshold Digital PLL

There are several reasons to use a D-PLL over its analog counterpart. For low input frequencies, the time constant or the RC product of the filter should be high, thus an analog filter will occupy a large chip area. Also analog charge pump based PLLs are more power hungry since they require complex current generation and voltage-to-current conversion circuitry.

Besides allowing for power saving techniques, such as voltage scaling, digital circuits are inherently more immune to noise.

Most high-performance DPLLs incorporate time-digital-converter (TDC) that works as the loop's PFD. A high-resolution TDC generates the digital codes proportional to the phase error between the divided-down clock and reference clock. Unlike the bang-bang phase and frequency detector (BB-PFD), the TDC in the loop can better linearize the PFD response. However, the TDC consumes more power and chip area. Therefore, to minimize the power consumption is to use a binary phase and frequency detector (BB-PFD) where the phase/frequency difference is a single bit signal.

Figure 4-29 (A) shows the functional block diagram of the sub-threshold D-PLL operated from a 260 mV supply. A BB-PFD compares the divided down clock from the digitally controlled oscillator (DCO) and the extracted reference clock from the envelope detector to generate a single bit early/late signal. A digital loop filter with programmable proportional (KP) and integral (KI) path gains is updated every reference clock cycle, producing a 10-bit output based on the early/late signal. Out of these 10 bits, the 3 least significant bits are used by a sigma-delta sampled at 1/M of the output clock frequency to produce a bit-stream, which, along with the remaining 7 bits from the loop filter output, form an 8-bit control word for the DCO.

Figure 4-3 (A) can be analyzed as a second order system, where KP and KI control the damping factor and loop bandwidth. The system needs a high damping factor and a high loop bandwidth to mitigate the effect of noise at the output. This is even more crucial for ring oscillator based PLLs since they are susceptible to noise when operated at low voltages. Increasing the value of KP also increases the damping factor, but an increase in KI can make the system oscillatory since KI affects the loop bandwidth as well as the damping factor. Thus by

choosing a high KP / KI ratio the system can be made more stable. However, a higher KP will increase the jitter in the DPLL, because the control words change (2Kp+1) when the BB-PFD toggles.

A DCO topology with tunable coarse and fine delay stages, shown in Figure 4-3 (B), was chosen over a relaxation oscillator topology for all digital operation at very low supply voltages. The coarse tuning stage is implemented as a 32-to-1 delay select path architecture with tristate buffers acting as selection switches. We use the five most significant bits of the control word for tuning the coarse delay stage through a 5-to-32 bit decoder (COARSE[31:0]). The fine tuning stage has tristate buffers connected in parallel with the inverters and is activated by an 8-bit thermometric control word (FINE[7:0]), which is based on the remaining 3 bits of the control word. Overall, by compressing 3 bits of the loop filter output by a sigma-delta we achieve an increased dithering resolution. Also as shown in Figure 4-1, the output of the envelope detector and input reference clock to the DPLL is sampled by a SAFF using the DPLL output clock frequency to eliminate glitches that can result when the back-scattering switch is enabled. Although this increases the jitter, it ensures the input clock frequency is stable. This architecture meets the tunable frequency range requirements while operating in sub-threshold region at very low power levels. All modules, except for the PFD and DCO, were synthesized using custom low power standard cells with P/N ratio of one.

4.3.2 RF-DC Power Management Unit

Figure 4-4 illustrates the conventional and proposed RF-DC PMU architectures for delivering dual-V_{DD} for digital and analog modules. In the conventional topology, the regulated voltage for the digital blocks is generated by stepping down the 1V supply, which wastes the power used in the RF-DC multiplication process only to regulate back down with a large

dropout. In the proposed approach, the voltage conversion efficiency can be improved because the regulated voltage is obtained from an earlier stage of the RF-DC converter, thus requiring only a few tens of mVs of dropout voltage. However, if the error amplifier and bias circuitry were to be connected to this voltage, the function of these blocks would be compromised and the necessary drop out voltage of the regulator would increase. To alleviate this problem, the two error amplifiers, which consume minuscule current, are connected to a higher power supply. The error amplifier of the analog block regulator is powered by the 16th stage output of the RF-DC converter while the error amplifier of the digital block takes its power from the LDO analog supply output. Thus, the supply-sensitive delay cells of the subthreshold DPLL benefit from the improvement in ripple rejection; only the pass transistor—at the output stage, where any error is reduced by the loop gain—is powered by an unregulated supply. By using this proposed arrangement in the RF-DC voltage generation block, the efficiency of the linear voltage regulator improves from 22.5% to 71.2%. Moreover, the power required from the RF-DC converter falls from 925nW to 365nW. In such a configuration, power efficiency of PMU, and thus RFID activation range, can be maximized.

Figure 4-5 shows the functional schematic implementing the RF-DC voltage generation block. The RF-DC converter is composed of sixteen stages. The diodes in the multiplier are implemented with low-V_T NMOS devices, minimizing forward-voltage drop. The flying capacitors are metal-metal (MIM) capacitors to reduce substrate loss. The schematic of the voltage reference and LDO_L block, excluding the start-up circuit, is shown in Figure 4-6. The error amplifier for LDO_L is a PMOS differential amplifier with active NMOS load, and the error amplifier for LDO_H is a NMOS differential amplifier with active PMOS load. This accommodates the different input common mode voltage requirements of each block. The

current and voltage reference circuits are composed of bootstrap current mirror and weighted ΔV_{GS} voltage references [58]. The power consumption of the voltage reference and the LDO_L are 105 nW and 75 nW, respectively. M_3 and M_4 are biased in the subthreshold region. In order to minimize the sensitivity of the bias-current-to-power supply variation, M_1 and M_2 are sized with large lengths and operate in strong inversion, for improved matching by minimizing channel length modulation in the PMOS current mirror. The minimum voltages required for each of the outputs of the diode multiplier can be defined in terms of the voltage headroom requirements of the various blocks. For instance, V_{DDL} is determined by the minimum voltage of the pass transistor in LDO_L, and V_{DDM} and V_{DDH} are imposed by the error amplifier of LDO_L and reference circuit respectively. Thus, the minimum voltages V_{DDL}, V_{DDM} and V_{DDH} required from the RF-DC converter are given by

$$V_{DDL}(\mathrm{Min}) = V_{REGL} + V_{DSN,SAT} \cong 330\mathrm{mV} \tag{4-1}$$

$$V_{DDM}(\mathrm{Min}) = V_{REGH} + V_{DSP,SAT} \cong 790\mathrm{mV} \tag{4-2}$$

$$V_{DDH}(\mathrm{Min}) = V_{GS,P7} + V_{GS,P5} + V_{GS,N3} + V_{GS,N2} \cong 1160\,\mathrm{mV} \tag{4-3}$$

Based on the required voltages, the RF-DC converter is designed to meet three different output voltages at maxi-mum conversion efficiency. The multiplier is tapped at stages five, fourteen, and sixteen, providing DC voltages of ~330, 800, and 1160 mV respectively. These voltages are stored on three separate MOS capacitors. The first stage is regulated down to 290 mV and functions as the digital supply (V_{REGL}), and the second is regulated down to 725 mV (V_{REGH}) to power the analog blocks.

4.3.3 Demodulator

The proposed architecture uses a DPLL as the on-chip clock generator. DPLL requires a reference clock, and the most common implementation is to use a crystal oscillator. However,

the crystal oscillator is usually bulky in size and power hungry, which is unsuitable for this application. In the proposed chip, the reference clock is extracted from the modulated transmitted signal from the external reader. ASK modulation is used in this application, since FSK modulation requires a mixer and high frequency local oscillator, which are power hungry blocks.

The proposed ASK demodulator, as shown in Figure 4-7, consists of a three-stage RF-DC converter, DC voltage limiter, low-pass filter, and positive edge-trigger register. The three-stage RF-DC converter extracts the envelope signal with an addition of RC load. When the input signal amplitude drops, the resistor provides a discharge path. The time constant $\tau = RC$ is selected much faster than the data rate, so the envelope at the output can follow the incident signal's change of amplitude. A DC limiter is added in the output of the RF-DC converter to prevent the input common mode voltage of the data slicer from exceeding the range. The low-pass filter corner frequency is set at 200 kHz to accommodate input clock frequencies from 5~20 kHz while filtering out the high frequency carrier and backscattering signals.

Figure 4-8 shows the proposed data slicer, which extracts the reference clock for the DPLL. The objective is to use a higher frequency clock and DCO output to sample the low frequency extracted envelope signal and then digitize it to the CMOS logic level. To minimize power consumption, the data slicer employs a preamp followed by a sense amplifier flip-flop [59]. In this configuration, the preamp provides a small enough gain to resolve the voltage difference between the envelope voltage and filtered voltage. The SAFF then uses positive feedback amplified to the CMOS logic level. The preamplifier provides 12.5 dB gain while consuming 110 nA DC current. The SAFF uses a cross-coupled inverter pair. The inverter pair swings to its stable state based on the value of the input. When the DCO output is low, PMOS transistors

precharge the output node of the latch to high. In this way the NAND flip-flop is able to hold the previous output state.

4.4 Experimental Results

This chip was fabricated in a UMC 0.13 μm CMOS process. The chip micrograph is shown in Figure 4-9. The chip's area is 2.12 mm^2 and the DPLL's is 0.017 mm^2.

We tested the DPLL alone to evaluate the jitter performance with battery supply. The reference clock for the DPLL is fed from a signal generator. Figure 4-10 presents the measured jitter performance, which shows the deterministic jitter in this DPLL design when the DPLL is locked. This is due to the nature of the BB-PFD DPLL. Moreover, the deterministic jitter is dependent on the delay of delay cell in DCO. The measured jitter of the free-running VCO with battery supply is shown in Figure 4-11. The chip is fed with 915 MHz signal, powered by the RF-DC converter, and the reference clock is extracted from the OOK signal. Figure 4-12 presents the measured jitter performance while Figure 4-13 shows the measured phase noise. There are several spurs in the measurement due to the reference clock coupling and mismatches in the loop filter. This increases the phase noise significantly.

The table summarizes the proposed DPLL performance and compares it with other low power PLL designs. The FOM [60] is used to evaluate the overall performance. A lower number indicates a superior PLL design.

$$\mathrm{FOM} = \left[\frac{\mathrm{area}(\mathrm{mm}^2)}{\left(\frac{\mathrm{tech}}{0.13}\right)^2}\right]\left[\frac{\mathrm{mW}}{\mathrm{MHz}}\right]^{1.5}\left[\mathrm{jitter}_{\mathrm{rms}} \cdot \sqrt{\mathrm{mW}}\right] \tag{4-4}$$

Although the proposed DPLL has the highest FOM, the DPLL has smallest area and lowest power consumption in the Table 4-1.

Measurements were set up using an arbitrary waveform generator (AWG) to generate a low frequency that was feed into RF signal generator set at 915 MHz. A folded dipole antenna connects to the output of the RF signal generator. The fabricated chip is tested on PCB with a folded dipole antenna connected to its input. Figure 4-14 shows the wirelessly measured DPLL timing waveforms. The reference clock is extracted from a 915 MHz RF carrier input that is ASK modulated with a 20 kHz signal. The waveforms show the extracted envelope (V_{ENV}) properly phased aligned and locked with the sampled input reference ($CK_{TX}/64$) and the PLL output clock frequency (CK_{TX}) of ~1.28MHz (M*N=64). In Figure 4-15, the backscattered modulation sidebands for wireless reader-tag operation were measured at 915.64, 915.96, and 916.28 MHz with corresponding reference clock frequencies of 10, 15, and 20 kHz (PLL multiplier set to 64).

Figure 4-16 shows the measured unregulated output, V_{DDH}, and the regulated V_{REGH} and V_{REGL} voltages of the PMU versus input power. Once the RF input power reaches -12 dBm, the regulated output voltages remain constant with a line regulation of 2.07 mV/V at 1 uA load for V_{REGL} and 3.7 mV/V at 3 uA load for V_{REGH}.

Table 4-2 shows a performance summary, and Table 4-3 compares the DPLL's performance with relevant published works. The RF transponder shows a measured sensitivity of -12 dBm, and the DPLL dissipates ~200 nW from a 260 mV supply at 1.54 MHz.

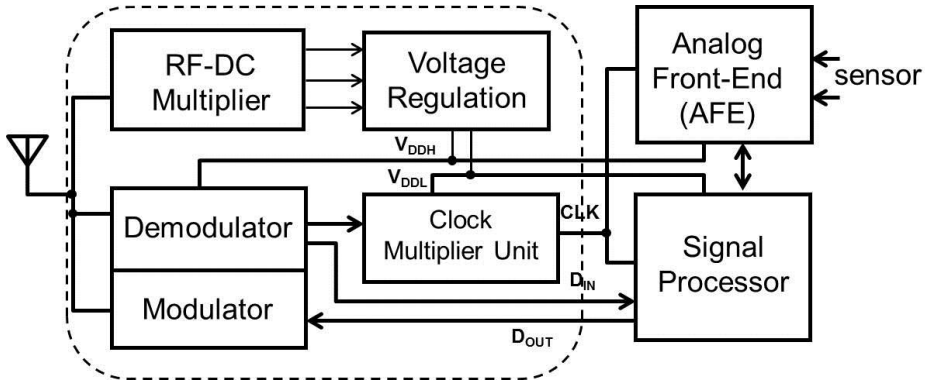


Figure 4-1. Functional block diagram of RFID transponder.

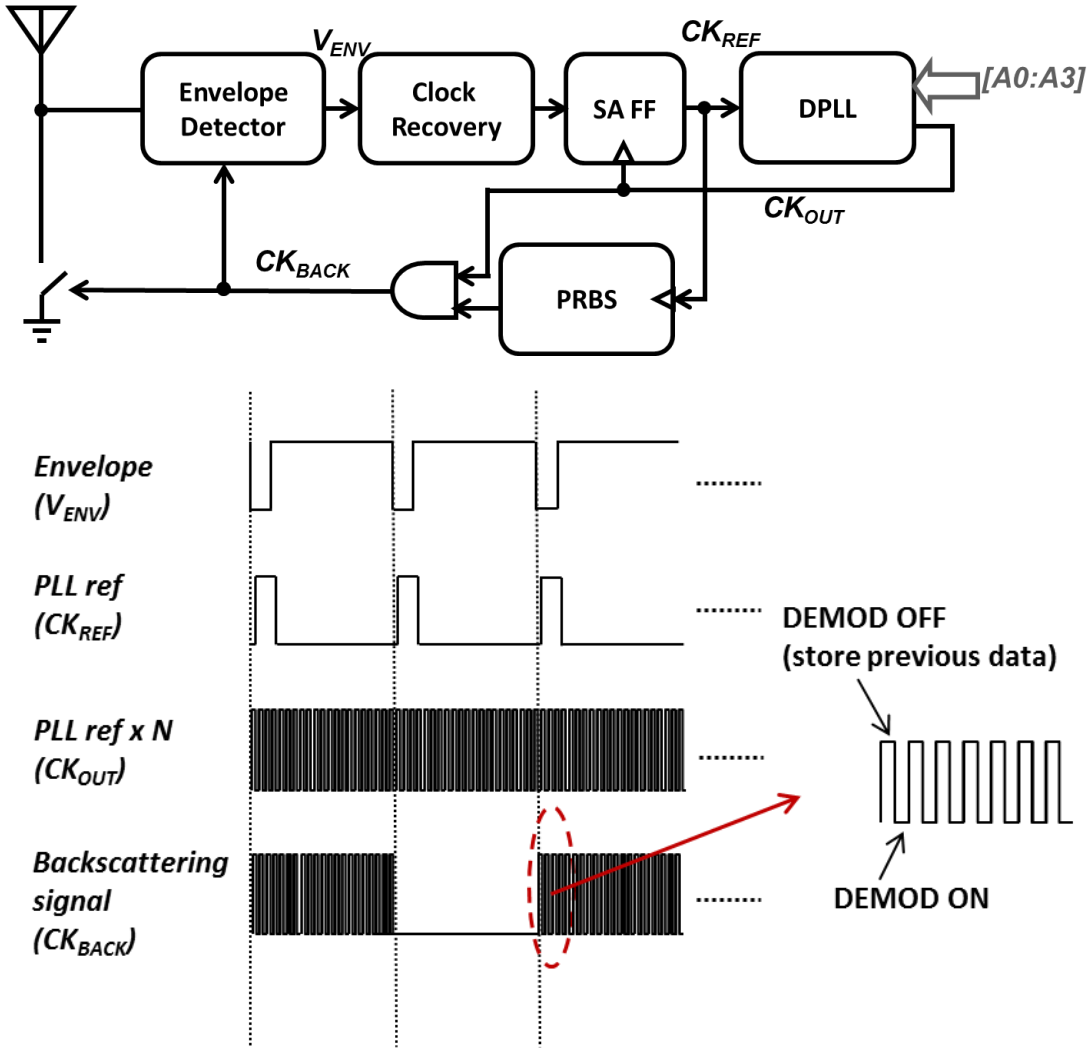


Figure 4-2. Simplified block diagram of the demodulator and the timing waveform of operation.

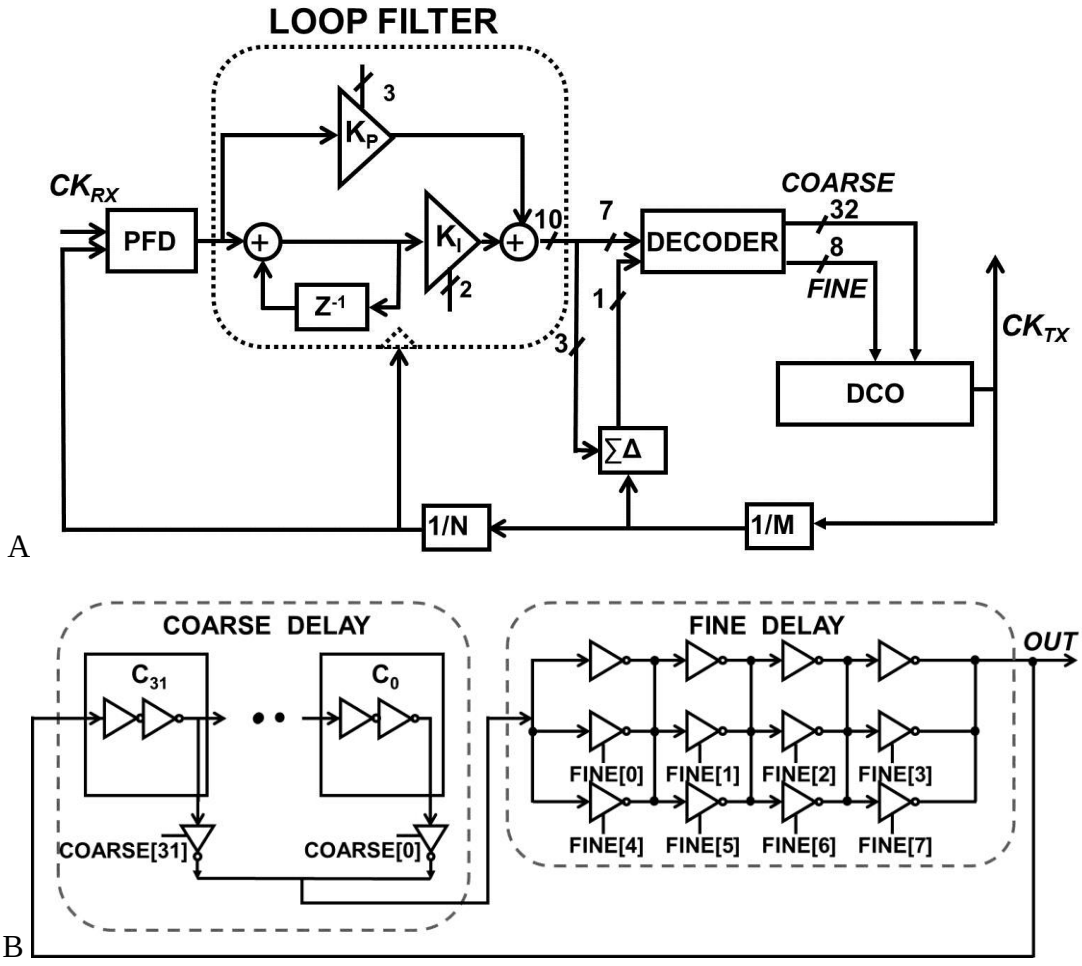


Figure 4-3. Functional block diagram. A) D-PLL, B) DCO.

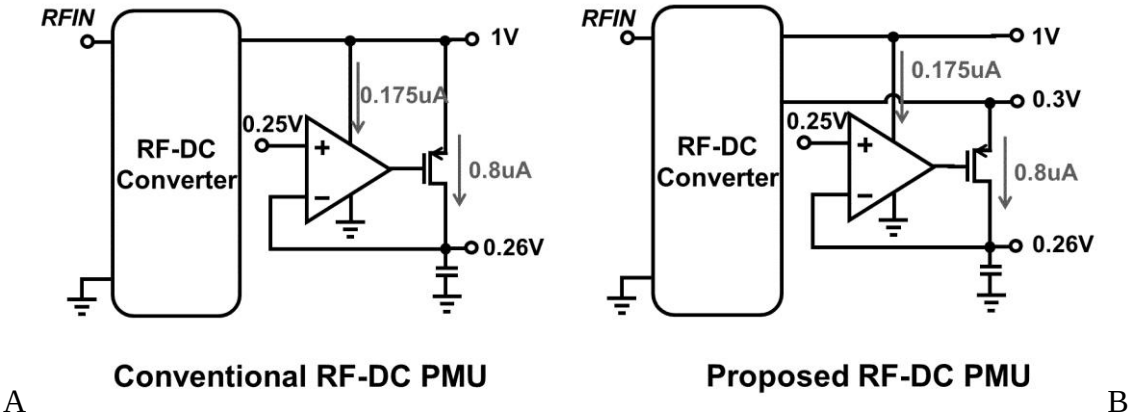


Figure 4-4. Power management unit. A) conventional, B) proposed.

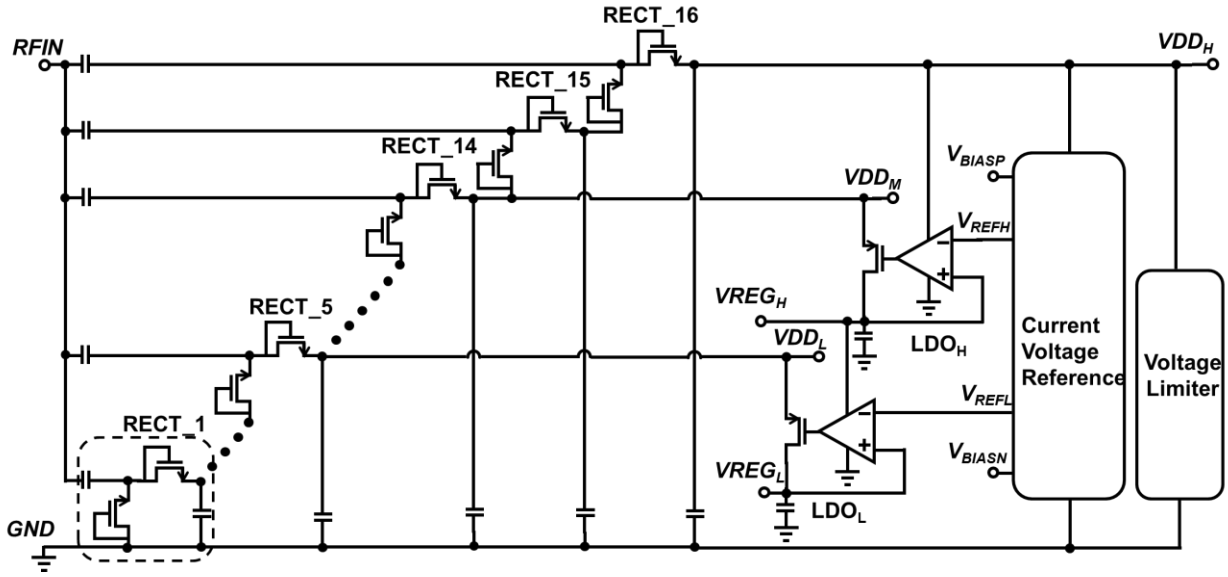


Figure 4-5. Functional schematic of the proposed RF-DC power management unit.

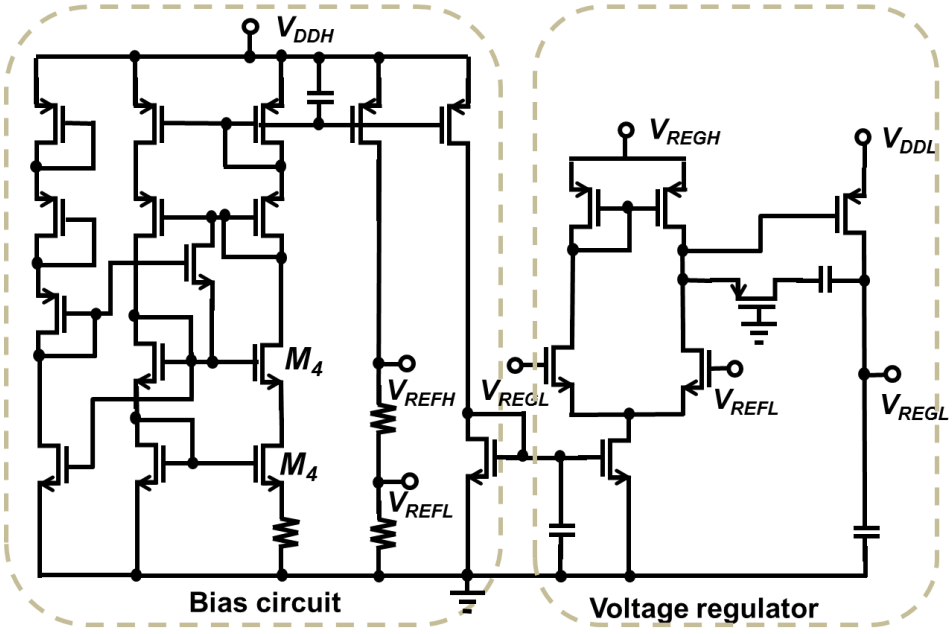


Figure 4-6. Functional schematic of the voltage reference and voltage regulator L_{DOL}.

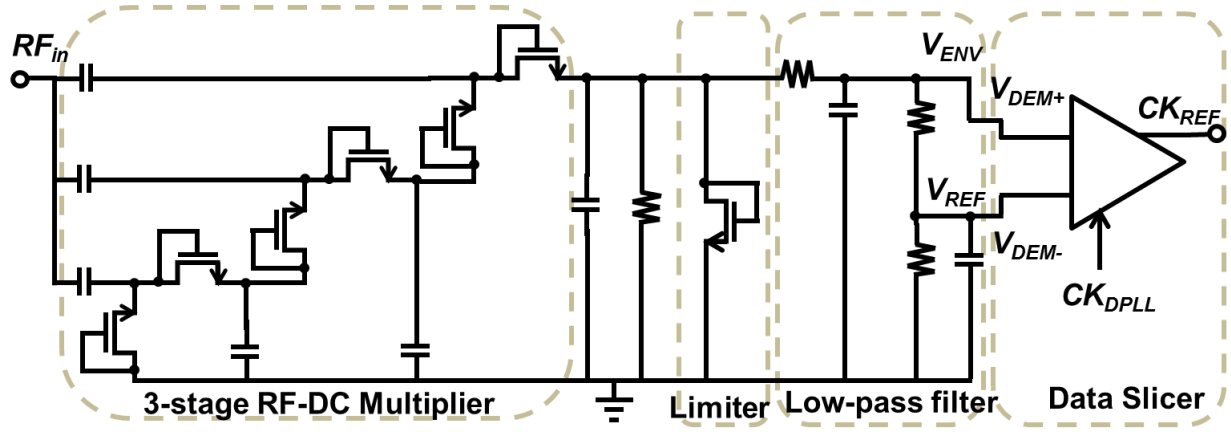


Figure 4-7. Functional schematic of the ASK demodulator.

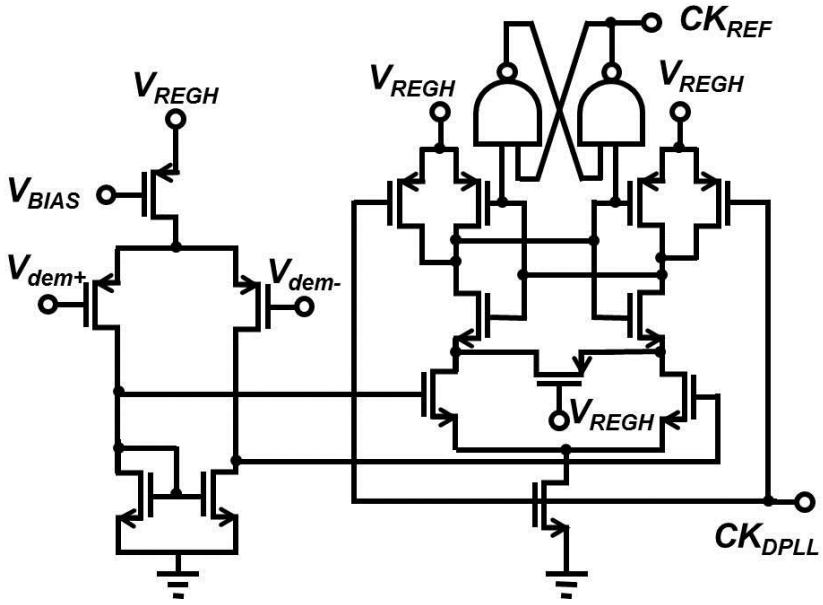


Figure 4-8. Functional schematic of the proposed data slicer.

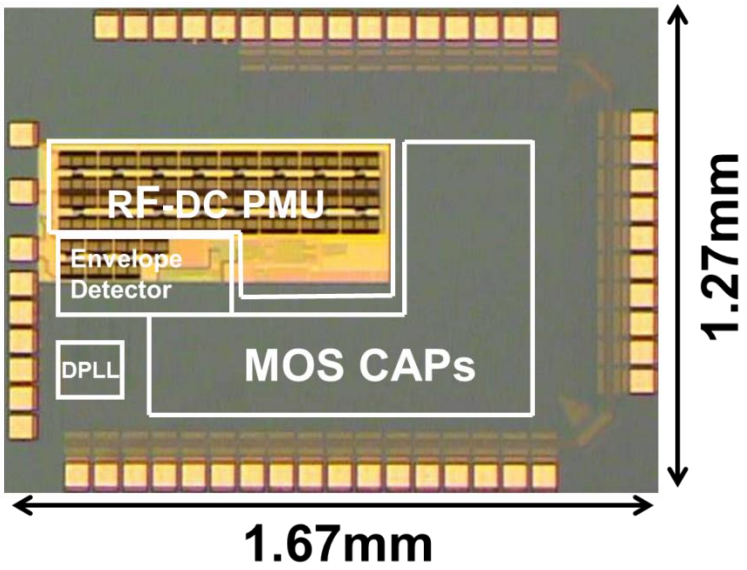


Figure 4-9. Die photo of the proposed RFID transponder.

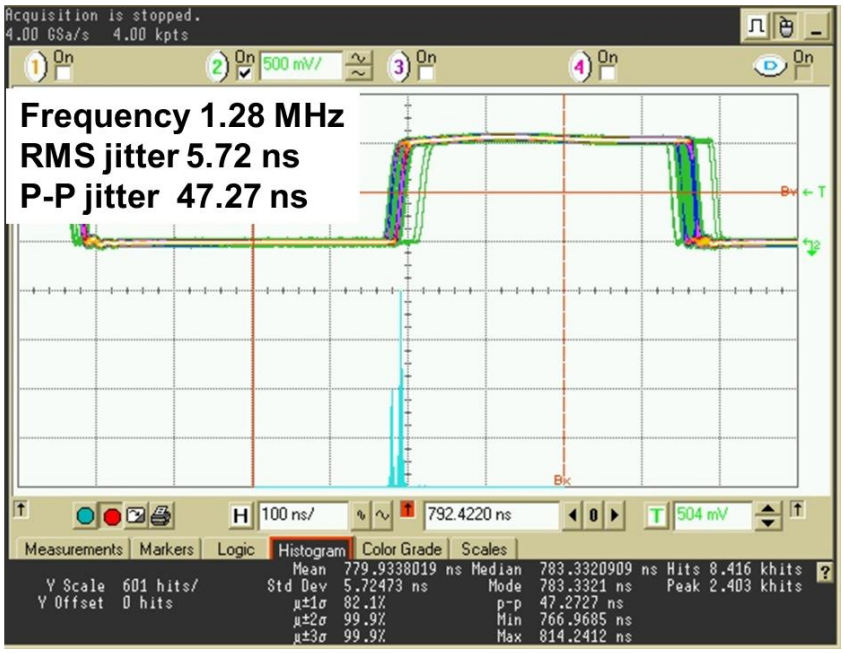


Figure 4-10. The measured jitter performance with battery supply.

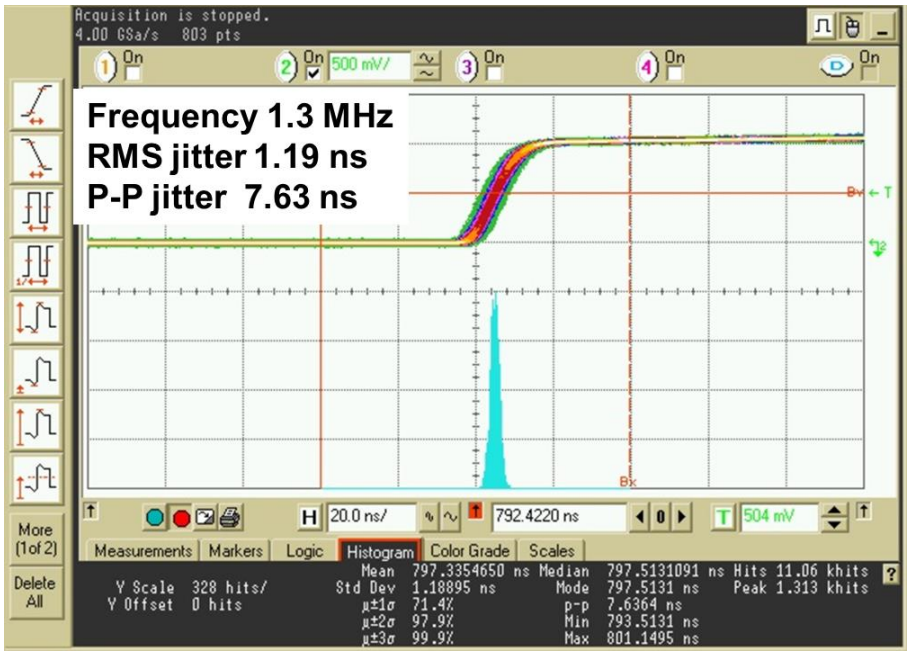


Figure 4-11. The measured jitter performance of free running DCO with battery supply.

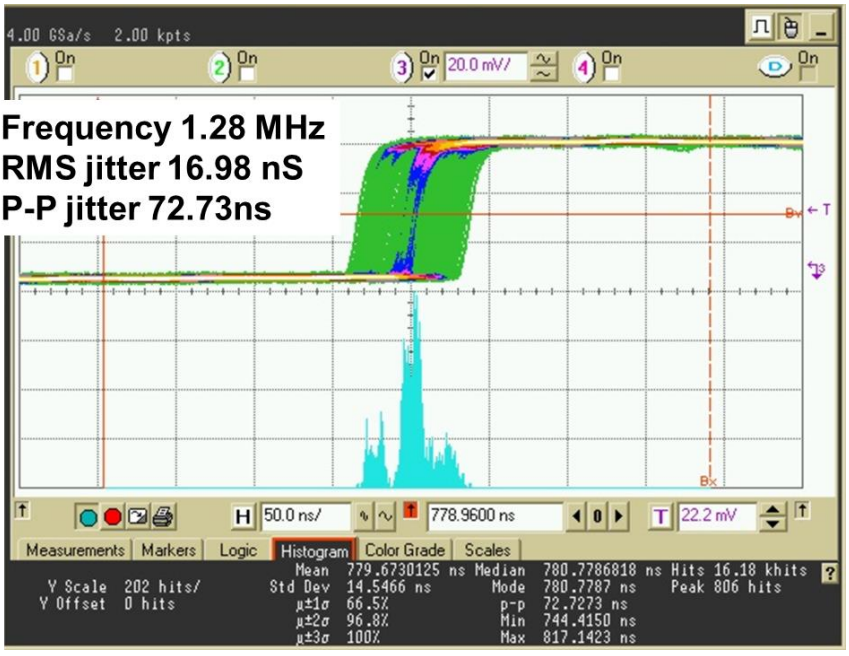


Figure 4-12. The measured jitter performance with RF source powered.

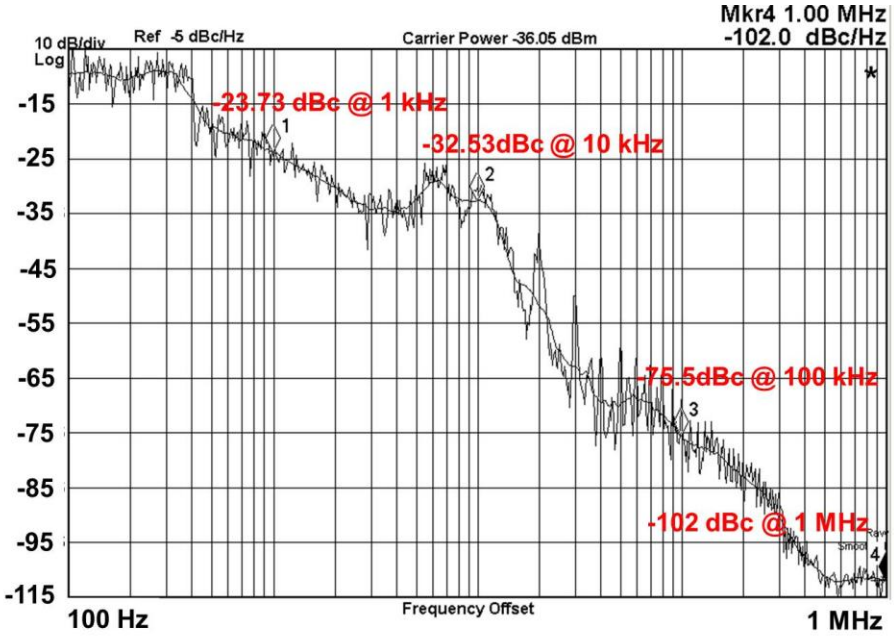


Figure 4-13. The measured phase noise of the DPLL with RF source powered.

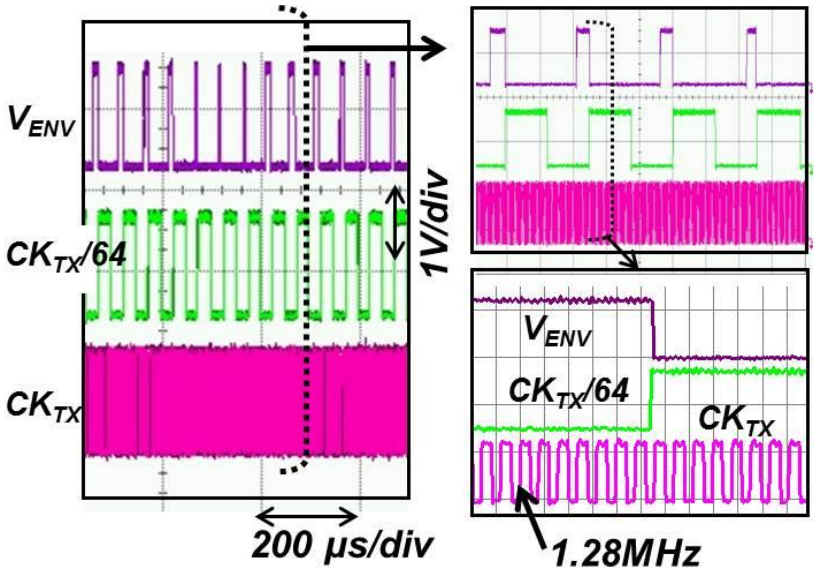


Figure 4-14. Measured recovered clock and DPLL output.

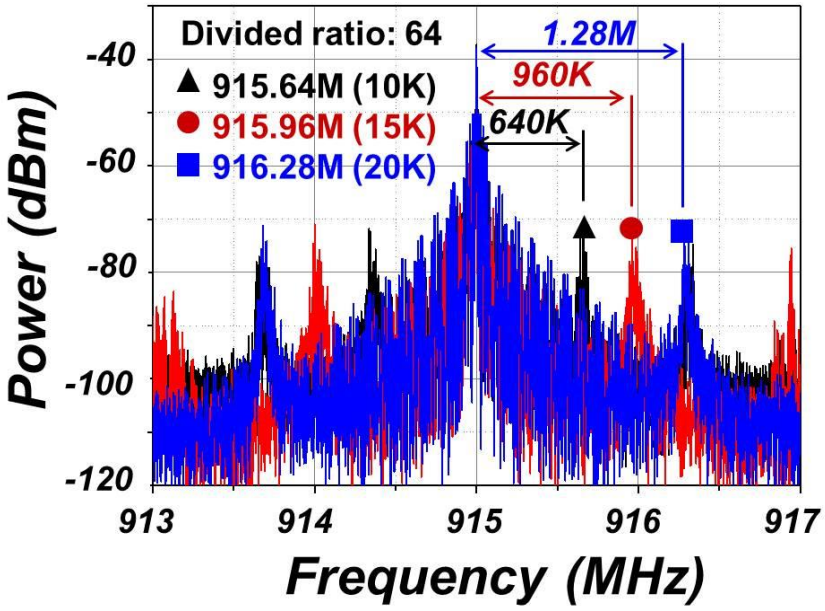


Figure 4-15. Measured backscattering modulated sideband spectrum for M*N = 64.

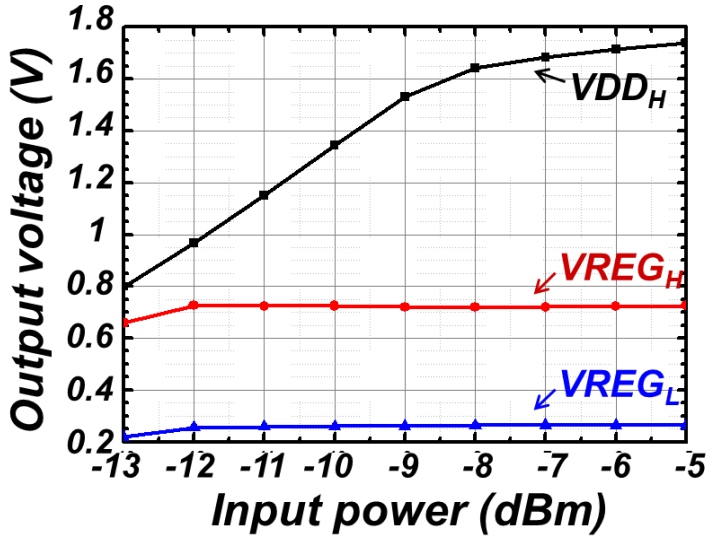


Figure 4-16. The measured unregulated output, VDD_H, and regulated $VREG_H$ and $VREG_L$ voltages of the PMU versus input power.

Table 4-1. PLL performance comparison

	[61]	[62]	[63]	[64]	This work
Technology	90 nm	130 nm	90 nm	130 nm	130 nm
Power consumption (mW)	10	1.25	0.4	0.44	0.000181
Power supply (Volt)	0.6-1.2	0.5	0.5	0.5	0.29
Output frequency (MHz)	5000	550	400	400-433	1.28
Area ($mm^{\wedge 2}$)	0.1	0.04	0.074	0.736	0.0107
RMS jitter (ps)	0.62	8.01	9.62	5.5	16980
P-P jitter (ps)	N/A	56.36	77.78	49.1	72730
Phase noise @1MHz offset (dBc/Hz)	-115	-95	-87	-91.5	-102
Jitter/cycle (%)	0.31	0.44	0.38	0.24	2.18
FOM	0.0754	0.3718	0.1927	0.0338	1

Table 4-2. Chip performance summary

Overview	
Technology	0.13 μm CMOS
Tag sensitivity	-12 dBm
Modulation method	ASK
RF-DC PMU efficiency	12.54%
RF-DC output power	6.96 μW
RF-DC output voltages	260 mV/725 Mv
Backscattering frequency	384 kHz – 1.54 MHz
Chip area	2.12 mm^2

Table 4-3. On-chip clock performance comparison

	[65]	[57]	This work
Circuit topology	Relaxation OSC.	FLL	D-PLL
Power consumption (nW)	302	1800	200
Power supply (Volt)	0.8	1	0.26
Output frequency (MHz)	1.52	2.56	0.384-1.54
Frequency deviation of fosc	<2% (over supply)	+1.2/-3.2	+1.5/-1.5%
Active area (mm^2)	0.134	N/A	0.017

CHAPTER 5
A SUPPLY MODULATED TRANSPONDER

5.1 Motivation

Medication non-compliance costs a large amount of money in developing drugs during clinical trials and results in high patient fatality. Currently, the most reliable method to improve medication compliance is direct observation therapy, which requires patients report to the health provider after they take medicine. However, this method becomes unrealistic when attempted on a large scale. This chapter presents a novel method and device that can be used to improve the medication compliance. The proposed method uses the RFID technology, which attaches a tiny transponder to a bio-compatible antenna printed on a small substrate. Once the patient swallows the transponder and the device reaches the stomach, it activates and begins transmitting UHF signal to an external reader, which confirms that the transponder has been taken into the GI tract. The transponder can be programmed with a set of ID numbers, each of which represents a specific medicine. By reading out the transmitted IDs from the patients or subjects automatically, this method achieves low-cost and reliable direct observation therapy for validating medication compliance.

In this proposed method, the size of transponder is a critical factor. A large chip area has the potential to cause damage to the GI tract, so it is crucial to minimize the size of tagging device in whenever possible. This chapter proposes a new transponder architecture that achieves a smaller chip area than a conventional transponder by removing the AC-DC converter, DC voltage conditioning blocks, and low frequency clock generator.

5.2 System Architecture

A passive transponder uses an antenna to interact with electromagnetic waves sent from an interrogator. It converts the waves to AC voltage across the AC-DC converter input. Then the

AC-DC multiplier converters the AC voltage to DC voltage on a storage capacitor and provides the DC power to the tag's circuit blocks. In this way it avoids the problems associated with using a battery. When the transponder is activated, it can communicate data to the reader. Figure 5-1 presents the building blocks diagram of the conventional passive transponder. A passive transponder chip consists of an AC-DC multiplier, on-chip storage capacitor, demodulator, clock generator, power-on reset circuit, and digital baseband circuit. The AC-DC multiplier consists of diodes and capacitors, the sizes of which are determined mainly by the input signal frequency and the load current requirement and output DC voltage. The AC-DC multiplier and demodulator consume a large percent of the chip area, especially when the carrier frequency is low like in HF or LF bands. Moreover, minimizing the rectifier output voltage ripple requires an on-chip storage capacitor with a large value, which consumes a lot of chip area. The rectifier output voltage also must be regulated in order to provide a stable DC voltage for the analog building blocks, and hence a series voltage regulator is normally required. To ensure that the digital logic starts at a known state when power is first applied, the transponder employs a power-on reset block.

Minimizing the chip area in RFID chip can be challenging. To do so, the transponder architecture must eliminate the RF-DC conversion block and the on-chip storage capacitor since their areas are larger than the other building blocks in RFID. This chapter proposes a novel passive transponder architecture that can operate directly from an AC power supply. All building blocks in the proposed transponder are designed to be operated at AC power supply voltage. In addition, the AC power supply voltage not only powers the transponder but also clocks the digital blocks in the chip. In this way, we can also remove the low frequency clock generation block from the proposed transponder. When the amplitude of the AC supply voltage reaches the designated voltage level, the transponder sends an 8-bit OOK modulated signal at 902 MHz ISM

band to the reader, as shown in Figure 5-2. The input voltage clamp block provides two functions. First, the clamper can limit the input voltage to protect the building blocks from over voltage damage. Second, the voltage clamper provides trapezoid-like supply voltage profile that minimizes the variation in the transponder's supply voltage. This transponder, shown in Figure 5-3, consists of the input voltage clamping circuit, frequency divider, decoder, ROM and modulator.

5.3 Circuit Implementation

In this section, the circuit building blocks in the proposed AC supply modulated transponder are presented including the basic AC logic circuit, frequency divider, 915 MHz oscillator and transmitter. The AC logic circuit is used in all digital blocks to perform the function from an AC supply voltage.

5.3.1 AC Logic Circuit

Figure 5-4 illustrates the AC inverter schematic [66] [67]. The AC inverter consists of two identical inverters and two transmission gates. The power and ground nodes of the two inverters are connected in opposite directions from each other. For instance, the sources of the upper inverter's PMOS and NMOS connect to V+ and V- , respectively. On the bottom path, the sources of the PMOS and NMOS connected to V- and V+, respectively. When the supply voltage V+ is larger than V-, the upper path is active and the bottom path is off. The bottom inverter is active only when V- is larger than V+. In this way, the two paths can process the signal during both positive and negative supply voltage.

5.3.2 Frequency Divider

Complicated digital logic cells can be implemented using the idea of a basic AC logic inverter. The AC supply Reset-Set register is shown in Figure 5-5. The AC supply voltage is also

the clock frequency for the frequency divider. The frequency divider is built by cascading AC supply RS registers.

The design challenge for this RS register comes when the supply voltages (V+ and V-) are close to zero. Here, the charge needs to be large enough to maintain the corresponding state on the output of the previous stage. When the supply voltage is close to zero, the transmission gate and the inverter form a discharge path from the output node to the power supply as shown in Figure 5-6. Otherwise this register doesn't hold the state, the function of frequency division fails. This problem becomes worse when the clock frequency is low, because the charge can be completely discharged in a short time. To resolve this problem, a capacitor can be added to the inverter's output node to increase the discharge time. In this design, the capacitor size is 75 fF for a minimum 100 kHz clock frequency. Figure 5-7 shows the simulation results of the frequency divider with and without the additional capacitor. In (A), the voltage of Q is discharged to zero. (B) shows the state of Q is held. (C) and (D) illustrate the frequency divider's function with and without the additional capacitor.

5.3.3 Oscillator Design

The transponder uses the ISM 900 MHz frequency band as the uplink frequency. The transponder operates from an AC power supply. This requirement makes the oscillator's oscillating frequency less sensitive to power supply voltage variation. Using a cross-coupled LC oscillator makes the frequency less sensitive to supply voltage variation, but it requires passive elements like inductor and capacitor. Also, compared to a ring oscillator, the cross-coupled LC oscillator consumes more area and power. This proposed transponder uses the cross-coupled ring oscillator with a constant biasing technique to minimize the frequency's sensitivity to power supply variation.

Figure 5-8 shows the schematic of the proposed oscillator. The oscillator consists of three differential delay cells and a bias voltage generator. The delay cells employ NMOS transistors to achieve high speed operation and use PMOS transistors as current sources. The oscillator uses a bias circuit to control the gate-to-source voltage of the PMOS in the delay cell reduce the bias current's less sensitivity to supply voltage variation. When the supply voltage increases, the ring oscillator frequency increases due to more bias current being injected into the delay cell. To offset the bias current's positive supply voltage coefficient, the PMOS's gate source voltage needs to remain constant. This minimizes the current variation with supply voltage. Figure 5-9 presents the simulation results of the oscillator frequency at AC supply voltage. The gate-to-source voltage of the PMOS in the delay cell ranges from 301 mV to 303 mV. The voltage variation results in oscillation frequency changes from 902 to 916 MHz, which still remains in the ISM 900 MHz band.

5.3.4 Transmitter

Figure 5-10 shows the schematic of the transmitter. The transmitter consists of a differential-to-single converter and a class-D power amplifier. This transponder uses a class-D amplifier because of its potentially high power conversion efficiency and its small chip area size. The class-D power amplifier is a switching amplifier, so the switch is either fully on or fully off. The power loss, therefore, can be significantly reduced, which leads to higher power efficiency. The class-D amplifier design uses two static switches, which can be implemented as an inverter, to generate square wave. Following the inverter, a series-tuned filter passes the fundamental frequency to the load. The parasitic capacitor from the inverter and inductive antenna can be used as the amplifier's LC filter.

Figure 5-10 shows the schematic of the class-D power amplifier, which consists of inverters and a series-tuned filter. In reality, the switches have parasitic capacitors and finite turn-on resistors, so the design procedure needs to consider the power loss from these. The output power of the transmitter is expressed in equation 5-1

$$P_{OUT} = \frac{2}{\pi^2}\left(\frac{V_{DD}}{R_{ANT} + R_{ON}}\right)^2 \cdot R_{ANT} \tag{5-1}$$

where V_{DD} is the transmitter's supply voltage (which equals V+ - V-), R_{ANT} is the load resistance, and R_{ON} is the inverter's on resistor. Given the required output power and specified V_{DD}, from equation 5-1 the necessary load resistance can be found in equation 5-2 [68].

$$R_{ANT} = \frac{V_{DD}^2}{\pi^2 P_{OUT}} - R_{ON} + \sqrt{\frac{V_{DD}^2}{\pi^2 P_{OUT}}\left(\frac{V_{DD}^2}{\pi^2 P_{OUT}} - 2R_{ON}\right)} \tag{5-2}$$

The design procedure is to find the aspect ratio of the inverter size that maximizes the power conversion efficiency. The required antenna resistance can then be found in equation 5-2. Figure 5-11 presents the design procedure for this transmitter. In (A), the aspect ratio of NMOS is found to be 175. As a result, the required antenna resistance can be determined as shown in (B).

From Figure 5-11, the aspect ratio of the NMOS in the class-D power amplifier can be found 175. For the inverter, we use a minimum gate length 0.12 μm and the corresponding width 21 μm. Given the driver size, the class-D amplifier's parasitic capacitance can be found from simulation. The value of capacitor is 0.275 pF, which means the antenna has to have 114 nH in order to resonate at 915 MHz at the output. The corresponding antenna resistance can be determined from (B). As a result, the antenna requires 240 Ω of resistance. The required resistor

and inductor values are the antenna impedance needed to be met to achieve the highest power conversion efficiency.

5.4 Antenna Design

To implement the inductive antenna, a loop antenna is employed. Loop antennas are usually classified as either electrically large or electrically small based on the circumference of the loop. If the circumference is less than or equal to $\lambda/10$ the antenna is considered electrically small antenna. λ is the wavelength of the output frequency. The coil and antenna were fabricated on a Pyrex wafer with a 1 μm thick electroplating cooper layer. The copper layer was coated with a gold layer to facilitate the wire-bonding process. Figure 5-12 shows the 3-D drawing of the proposed tagging system for medication compliance. The size of the substrate is 11 mm*4.5 mm, which fits into a standard OOO capsule. Figure 5-13 shows the 3D plot of the antenna structure. The simulated impedance of the antenna is shown in Figure 5-15. The impedance is 15.6 + 696i at 920 MHz and the inductance is 120 nH. Figure 5-15 presents the simulated radiation patterns of the antenna.

5.5 Experimental Results

This chip was fabricated in a 130 nm 1P8M CMOS process from UMC. A chip microphotograph is shown in Figure 5-16. The total chip area is 380 μm×340 μm. The electrical performance of the chip was measured by housing the chip on a glass slide and testing it on a probe station. The input signal was fed by a custom designed low frequency balun to generate 125 kHz differential input signal. Figure 5-17 shows the measurement setup for the proposed transponder. The signal generator outputs a 125 kHz AC voltage to the Balun to generate a differential signal across the input of the transponder. The MXA analyzer captures the burst signal from the transponder's output. Figure 5-18 shows the measured waveform on an

oscilloscope. The input signal amplitude is 1 Volt from the signal generator output, and the differential input signal amplitude is limiting around 200 mV by using the input clamp circuit. The output signal of the transponder shows an 8-bit data pattern with 15 mV peak amplitude on a 50 Ω load. At 0.4 Volt DC voltage, the measured power consumption is 245 µA without the input clamp circuit and 843 µA with it. The output waveform is measured by a signal analyzer, as shown in Figure 5-19. The output signal level is -68 dBV, which is equal to -48.89 dBm on 50 Ω. Table 5-1 summarizes the performance of the proposed supply modulated tag.

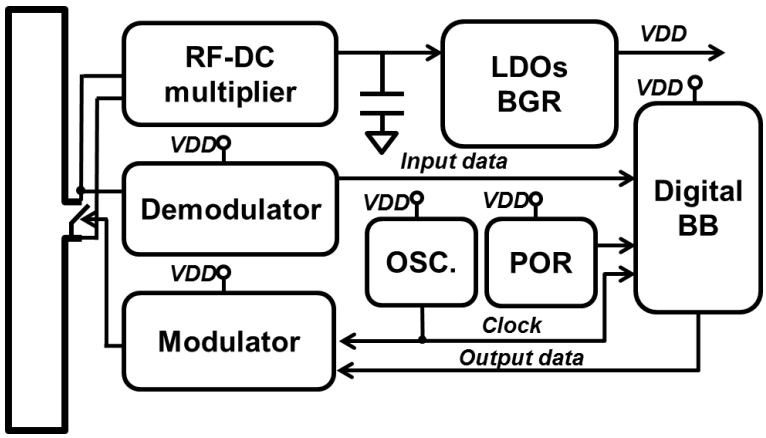


Figure 5-1. Conventional passive transponder building blocks diagram.

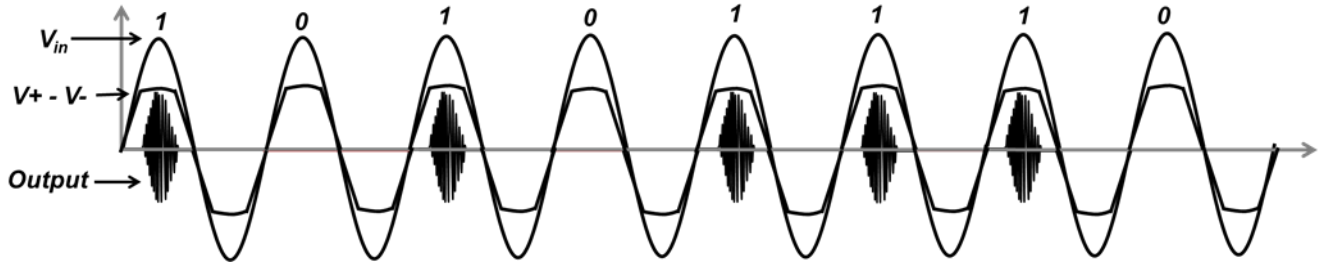


Figure 5-2. Proposed supply modulated transponder input and output waveform.

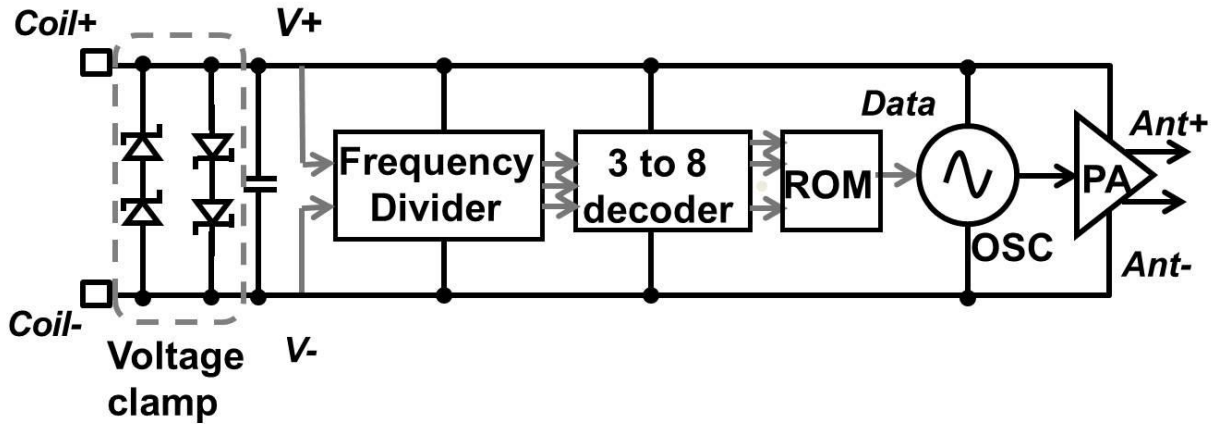


Figure 5-3. Proposed AC supply modulated transponder building block diagram.

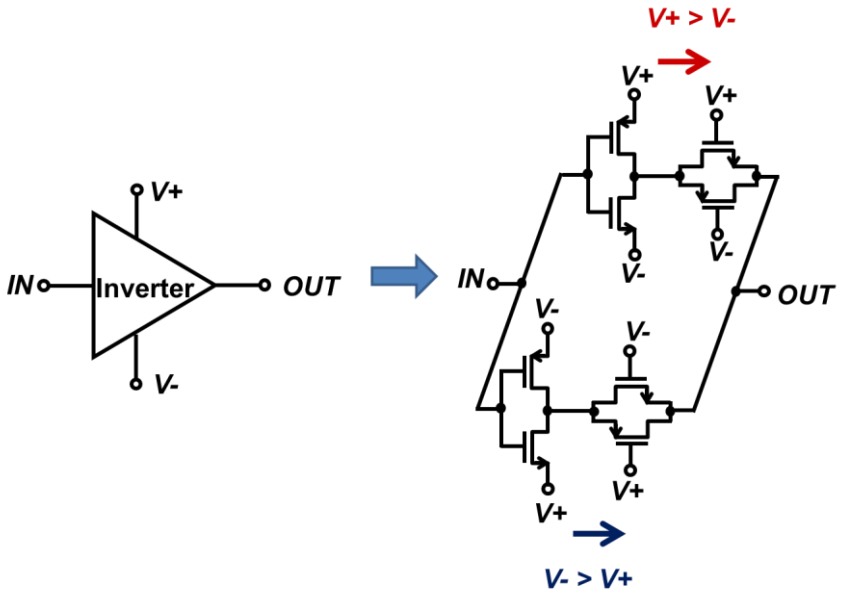


Figure 5-4. Schematic of AC inverter.

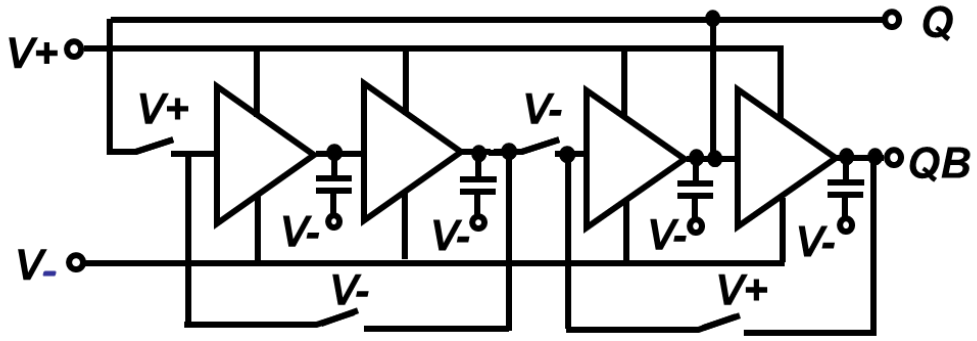


Figure 5-5. The schematic of the AC supply RS register.

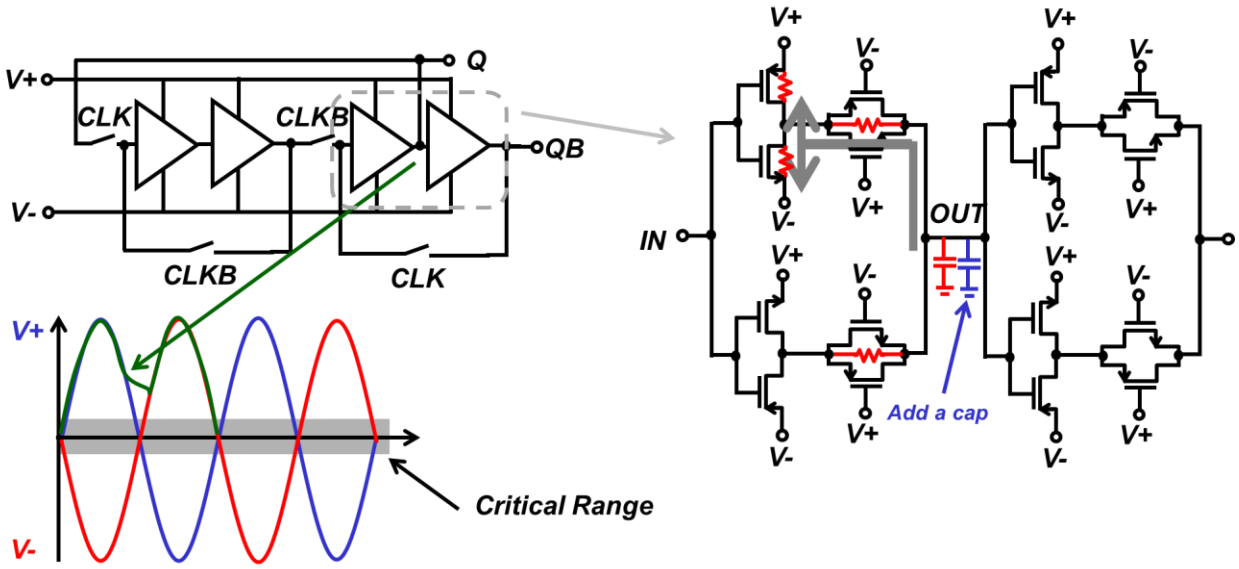


Figure 5-6. AC supply RS register design.

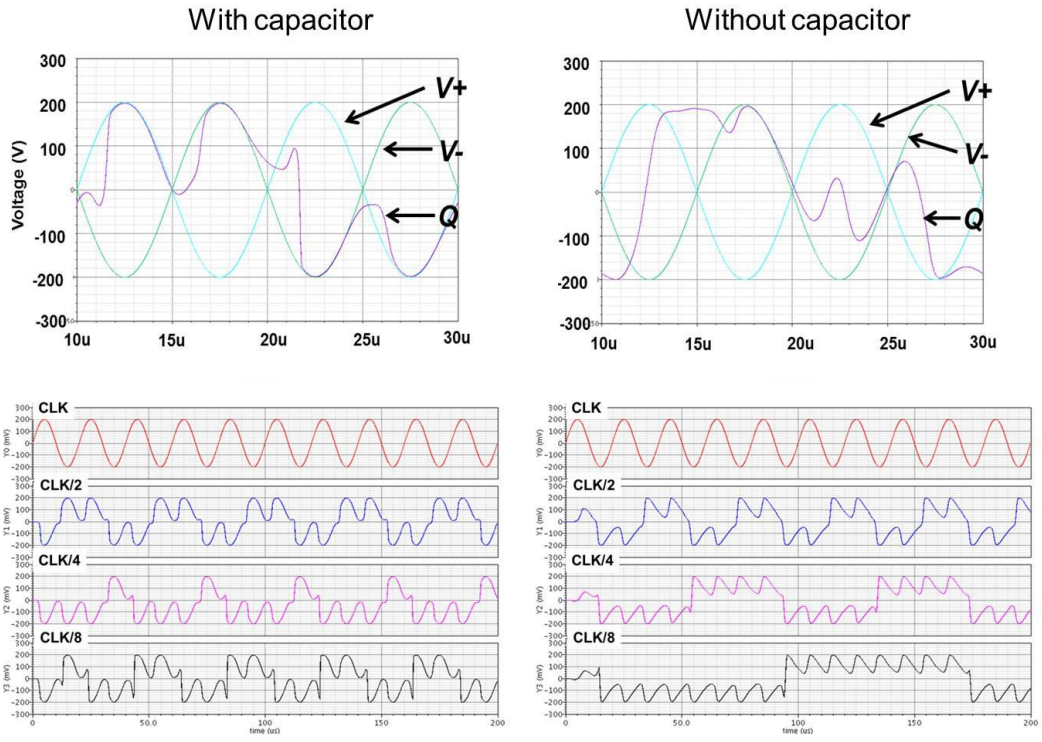


Figure 5-7. Simulated results of the AC supply RS register.

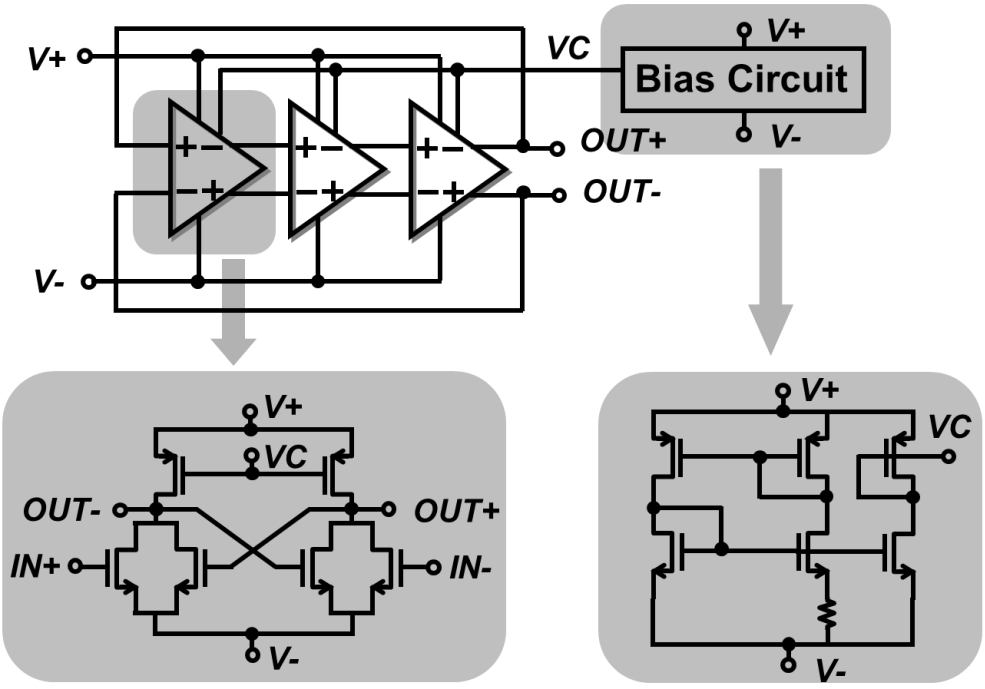


Figure 5-8. Schematic of NMOS transistor cross-coupled ring oscillator.

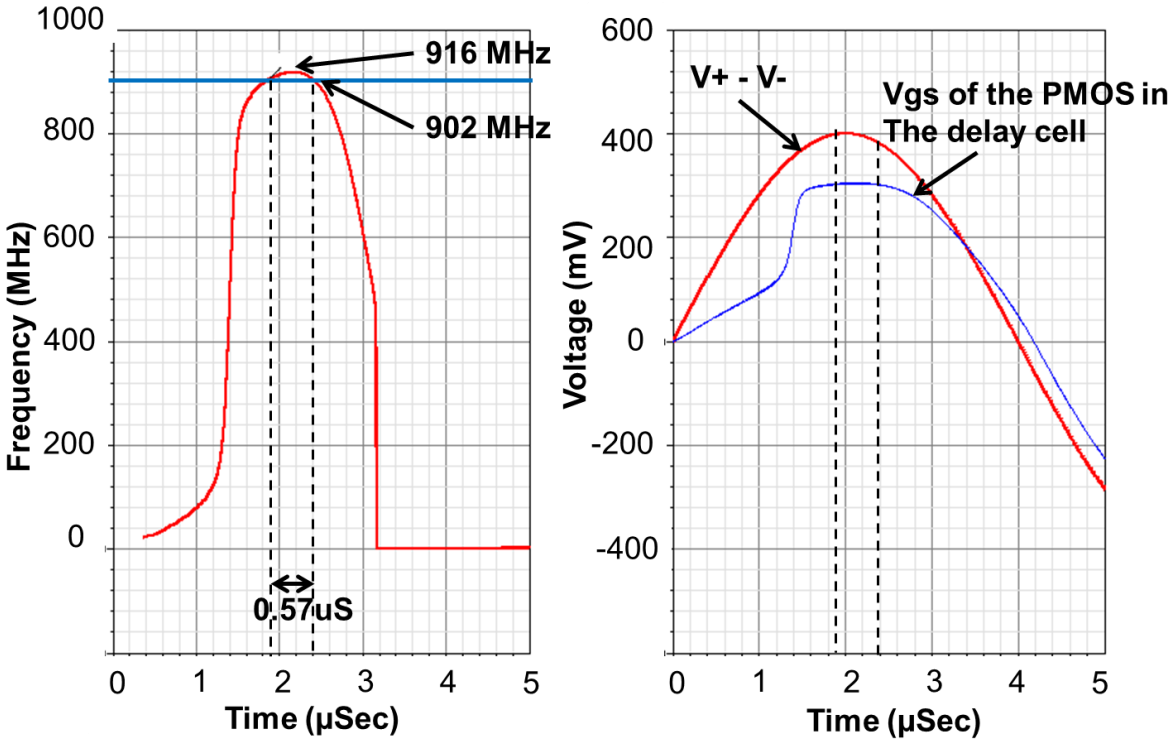


Figure 5-9. Simulation results of the oscillator frequency with AC supply voltage.

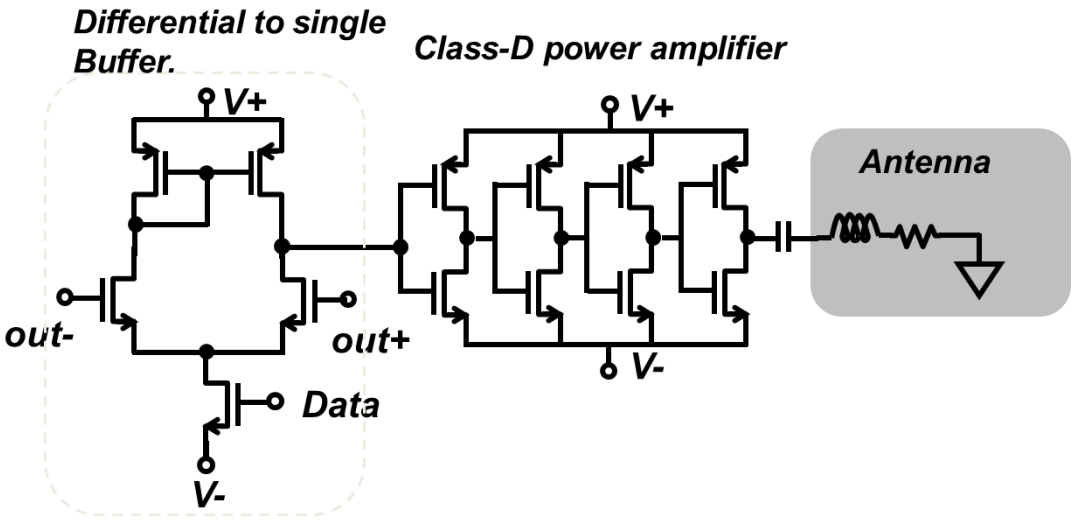
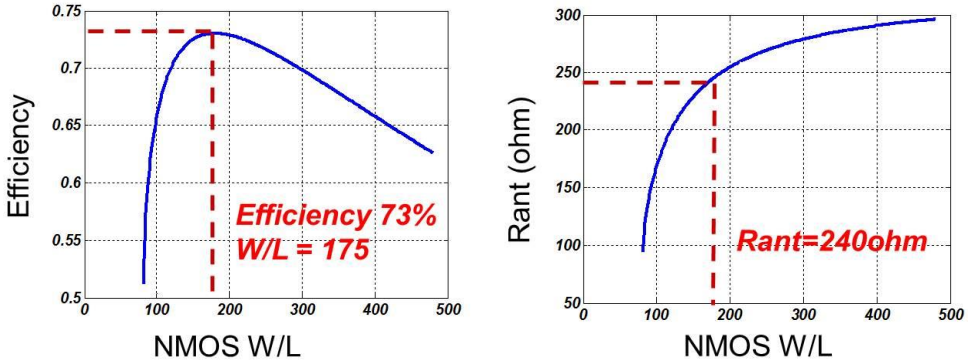


Figure 5-10. Schematic of class-D power amplifier.



A B

Figure 5-11. Class-D power amplifier sizing: A) Inverter size vs. conversion efficiency, B) The corresponding antenna resistance by given aspect ratio of Inverter size.

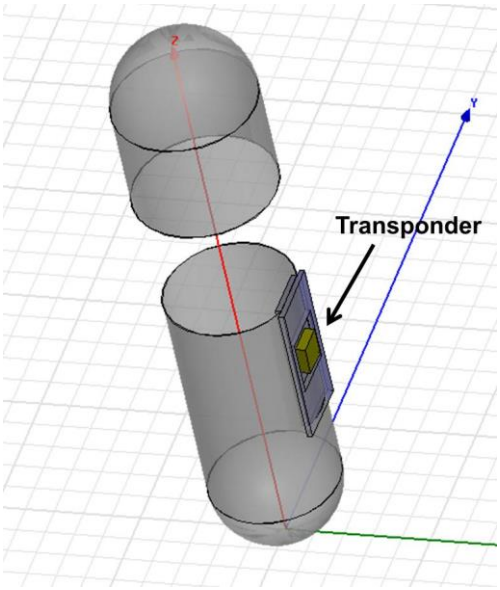


Figure 5-12. The 3-D drawing of the proposed supply modulated tag.

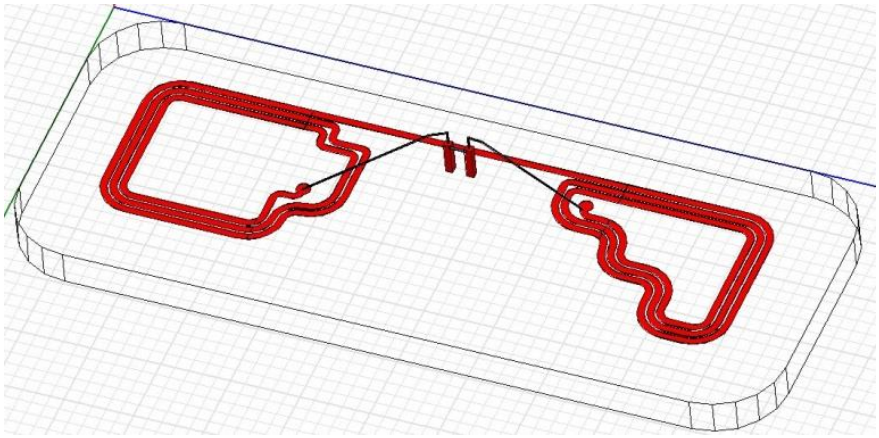


Figure 5-13. The 3-D plot of the antenna on the Pyrex substrate.

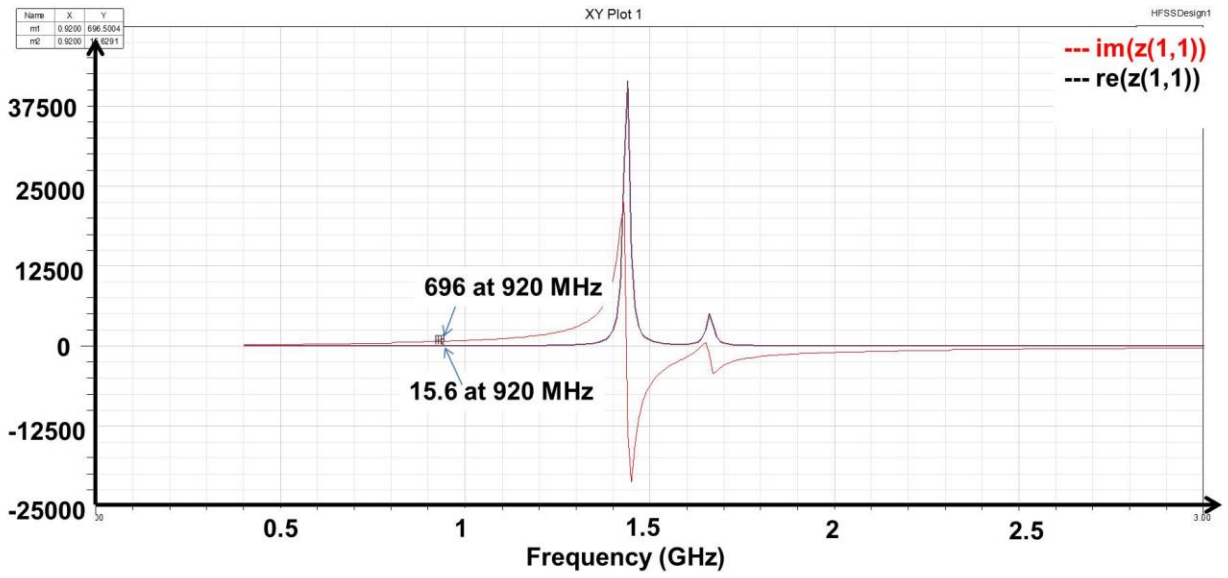


Figure 5-14. Simulated antenna impedance.

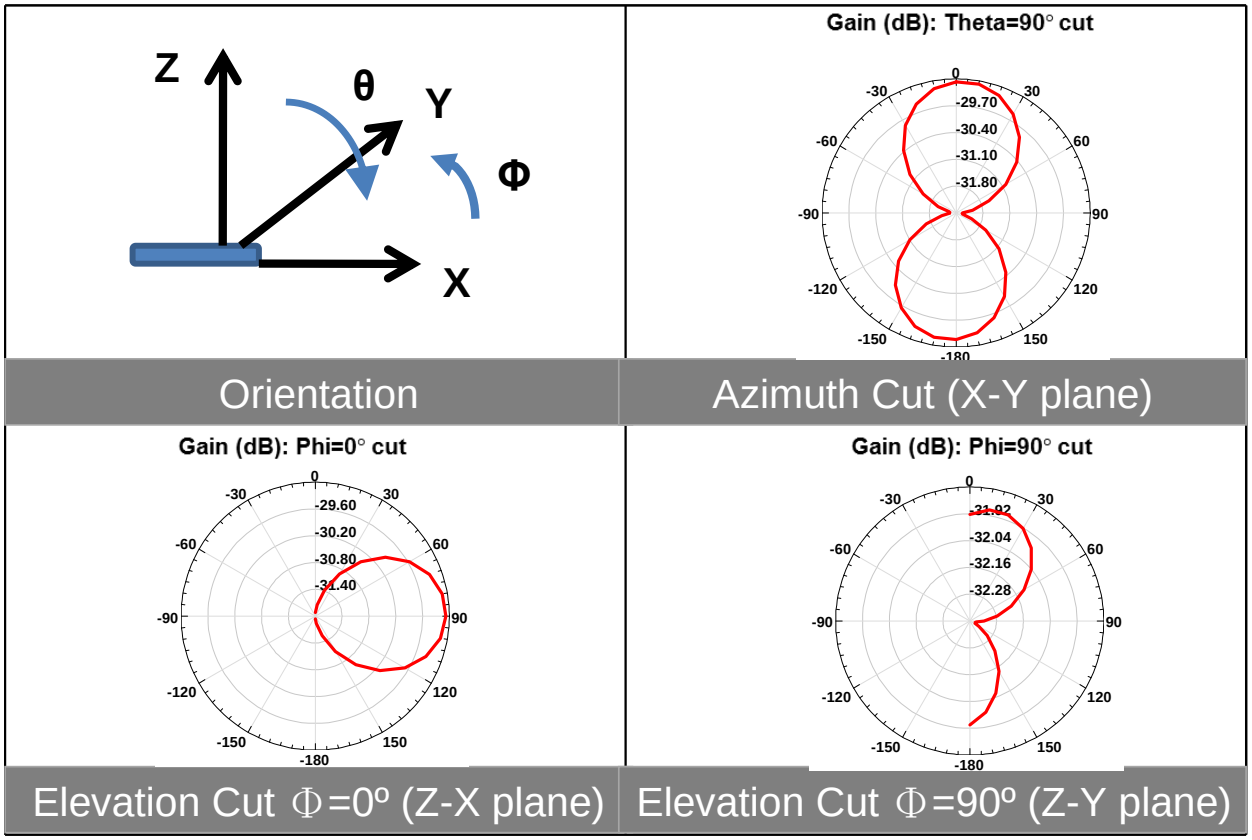


Figure 5-15. The simulated antenna radiation pattern.

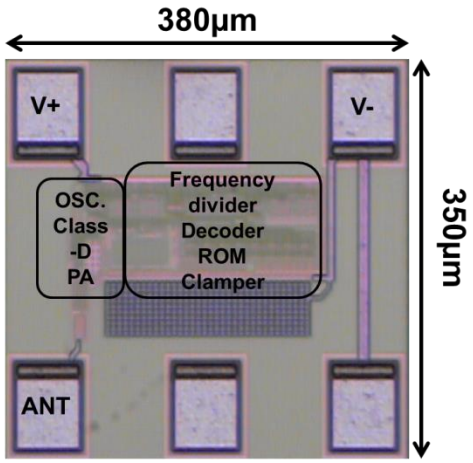


Figure 5-16. Chip microphotograph of the supply modulated transponder.

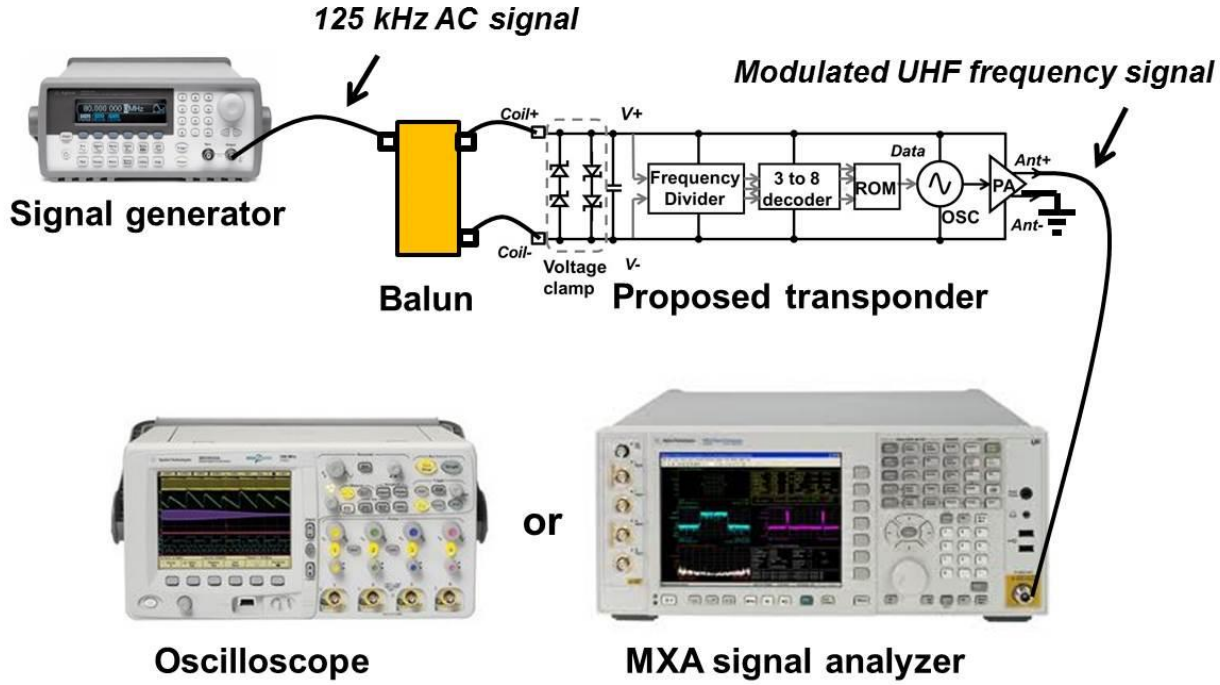


Figure 5-17. The measurement setup for the proposed transponder.

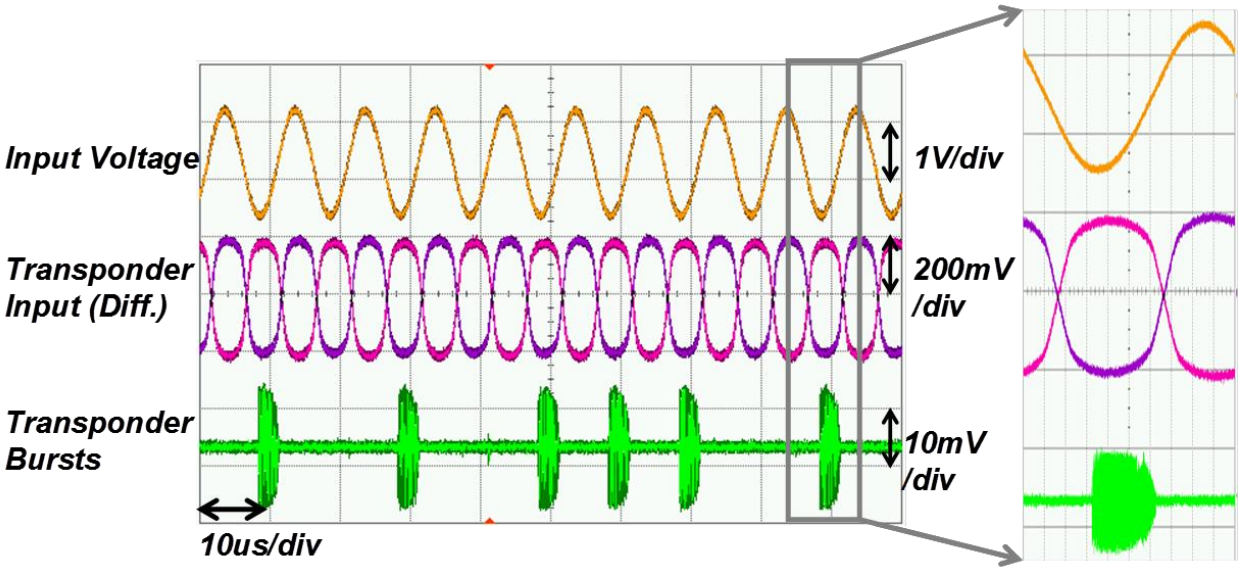


Figure 5-18. Measured time domain waveforms on an oscilloscope.

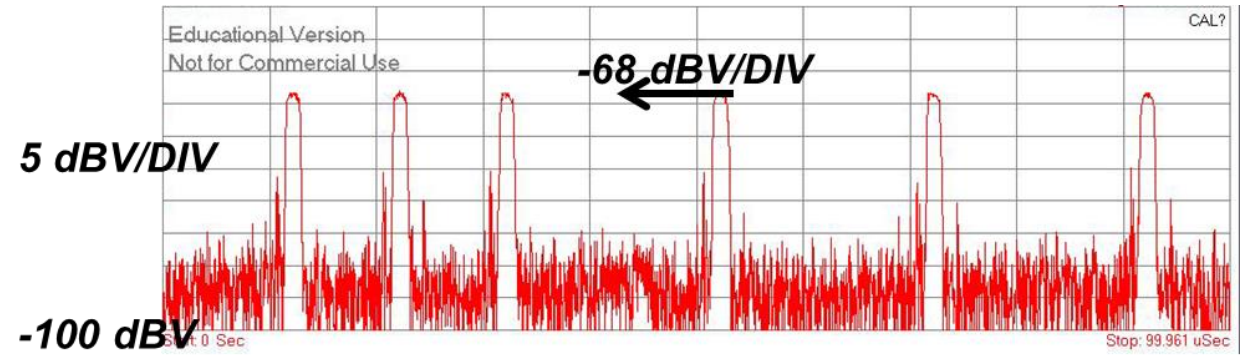


Figure 5-19. Measured output signal using signal analyzer.

Table 5-1. Summary of supply modulated transponder performance.

	This work
Technology	130 nm CMOS technology
Supply voltage (V)	0.4
Down/Uplink frequency	125 kHz/915 MHz
Input power (µW)	338.4
Output power (dBm)	-48.89
Chip area (mm^2)	0.1292

CHAPTER 6
A BATTERY ASSISTED TRANSPONDER

6.1 Motivation

There is an increasing demand for ultra-low power transceiver for biomedical applications. For those applications that don't require high data rate transmission, a RFID transponder is a good candidate for ultra-low power applications. There are three types of transponders: active transponders, semi-passive transponders and passive transponders. The passive tag has no battery to power the circuitry in the tag and has no radio transmitter. Passive tags depend on rectification of the received power from the reader to power the circuitry in the tag, and they modulate the impedance between the antenna and the chip to send information back to reader. Because of this last feature, the communication range is normally less than in active transponders. However, passive transponder can be smaller than the active ones and require minimum maintenance of the tag, which is far more preferable for biomedical applications.

This chapter presents a new transponder architecture. It can use a coil to receive data and system clock, and uses a DC voltage at the input to power the chip. In this way, the transponder doesn't need to harvest energy from the electromagnetic waves. The transponder sensitivity can be improved. The transponder can also use a coil to harvest the energy from electromagnetic wave to power the chip. This proposed transponder has advantages of both the active and passive transponder approaches. With the battery assisting and radio transmitter, the communication range is improved.

This transponder find an application as applied in the medicine electronic identification and in medication compliance. The proposed transponder can be attached to a standard-sized capsule. When the capsule requires to be programmed ID, the transponder can be activated and written in the air through inductive coupling. When used in the body for improving medication compliance,

the excellent sensitivity of the transponder's battery-assisted mode helps deal with the high loss that occurs in human body.

6.2 System Architecture

Figure 6-1 shows the functional block diagram of the proposed transponder, which consists of an AC/DC-DC converter, a receiver module, a storage capacitor, digital logics, and a transmitter module. The downlink frequency is 13.65 MHz, and the uplink frequency 915 MHz. Both frequencies are located in the ISM bands.

The energy harvester in the proposed transponder can take either AC or DC input voltage and output DC voltage. An energy detector is used to monitor the DC voltage across the storage cap, and it actives the transmitter when the voltage level reaches the designed value. The receiver module can decode the data and provide system clock for the baseband circuit in the transponder. A 256-bit pseudo-random binary sequence (PRBS) generator is built in for test purpose. The transmitter consists of an LC tank oscillator and a class-D amplifier to provide excellent output power efficiency.

6.3 Circuit Implementation

6.3.1 AC/DC-DC Converter

The challenge associated with the proposed transponder is that the energy harvested needs to be able to work under both AC and DC voltage. In order to work for DC voltage input, another signal path for DC voltage input can be added to the AC-DC voltage multiplier as shown in Figure 6-2. During AC voltage input, the diode in the DC path functions as a half wave multiplier. On the other hand, the multiple-stage AC-DC voltage converter multiplies the input signal amplitude to a higher DC voltage level at the output. In this mode, the diode in the DC

path presents an energy loss for the conversion process, because the output voltage of the converter imposes a large reverse voltage across the diode.

There are tradeoffs in the AC/DC-DC converter between the input sensitivity for AC signal input and voltage conversion efficiency for DC input. In the DC input, the voltage drop is not constant when the forward current is small. Especially in the passive transponder applications, the load current is usually less than a micro ampere. In the DC input, the larger diode size is better. However, in the AC input the larger diode size introduce a larger reverse leakage current, because the reverse leakage current is proportional to the diode size.

The converter consists of five stages of voltage doublers and a diode for the DC input path. Low-Vt diode connected MOS transistors are used to implement the rectifying device in the converter, and metal-to-metal capacitors are chosen for the coupling capacitors. The voltage detector continuously monitors the supply voltage and sets the transponder in standby or the enabled mode. In standby mode, the system waits and dissipates very little power. When the voltage across the capacitor exceeds 0.85 V, then it enters the enabled mode.

6.3.2 Receiver Circuit

The receiver consists of an envelope detector, a clock recovery circuit, and a 256-bit pseudo-random binary sequence (PRBS) generator, as shown in Figure 6-3. In this chip, a one-stage voltage doubler and two non-inverting buffers with different bandwidths are used to extract the envelope from the downlink signal. When the transponder operates in inductive coupling mode, the envelope detector's output is initially high. Once the modulated signal comes in, the logic level of the output flips. After the modulated signal, the output logic level flips again. However, when the transponder operates in DC input (battery assisting mode) the output of the envelope detector is low. As a result, the clock recovery is designed to generate two pulses

whenever the envelope signal toggles so that the initial state of envelope detector does not cause clock signal recovery error. Figure 6-4 shows the proposed timing diagram of the received signal and recovered signal.

6.3.3 Transmitter

The transmitter consists of an LC oscillator and a class-D power amplifier, as shown in Figure 6-5. Compared to the ring oscillator, the LC tank oscillator is less sensitive to power supply voltage variation. The design uses an LC tank oscillator to generate an ISM band 915 MHz signal output due to the higher quality factor of the LC tank oscillator and the lower sensitivity to supply voltage variation. When the transmitter is enabled, the oscillator and the power amplifier draw a large current from the storage capacitor, which causes the power supply to vary. If a ring oscillator is used, the oscillating frequency varies enough to possibly cause the output frequency to move out of the ISM band, which degrades the class-D power amplifier power conversion efficiency. Hence the LC tank oscillator's characteristic of being less sensitive to supply voltage variation is crucial for this proposed transponder. Although the area of the LC tank oscillator is larger than the ring oscillator, the LC tank oscillator provides stable frequency vs. supply voltage.

The oscillator is activated only when the output voltage is at least 0.85 V and the clock and data are high.

6.4 Experimental Results

This chip is measured on a test board to verify its electrical characteristics. The chip was fabricated in a UMC 0.13 μm CMOS process, and the chip micrograph is shown in Figure 6-6, with the area of the chip measuring 0.9375 mm^2. Figure 6-7 shows the measurement setup for the proposed transponder. The transponder's input is fed OOK modulated 13.65 MHz carrier with a

DC voltage through a bias tee. The transponder's output is measured by an Agilent MXA signal analyzer or an oscilloscope. Figure 6-8 shows the measured input power vs. output voltage of the proposed AC/DC-DC converter for 210 kΩ load at 13.65 MHz carrier frequency. Figure 6-9 shows the AC/DC-DC converter's measured reverse leakage vs. its output voltage. Most of the leakage comes from the reverse leakage of the diode in the DC path. Testing of the voltage level detector is shown in Figure 6-10. The top trace is the output of the AC/DC-DC converter taken through on-chip wafer probing while the bottom trace shows the output signal of the transponder output. An additional zoom-in window of the converter's output shows the power level detector's hysteresis window is from 500~840 mV.

Measurements of the function of the proposed transponder communication are shown in the following figures. Tests were performed using an arbitrary waveform generator (AWG) for the clock and routing the 1 kHz clock to the modulation input of the signal generator set at 13.65 MHz. Figure 6-11 shows the input signal and the resulting clock and data. The top trace shows the modulated input waveform using 1% pulse width amplitude modulation. The second trace is the envelope output, and the third trace is the output data pattern of the PRBS. The bottom trace is the 915 MHz output of the transmitter on 50 Ω load. Figure 6-12 shows the same output waveforms except here using battery power instead of inductive coupling. The top trace shows the output of AC/DC-DC converter. Both cases were tested under the chip's minimum sensitivity at 1 kHz clock rate. Figure 6-13 shows the measured burst using a mixed-signal analyzer. The measured voltage level is -52 dBV, which equals -38.99 dBm for 50 Ω load. The number of burst pulses during data-1 also depends on the DC voltage level across the storage capacitor. Figure 6-14 shows the number of pulses versus the input DC voltage during battery assisting mode.

The minimum sensitivity is -6.4 dBm for inductive couple powering. The minimum required battery voltage is 840 mV for battery assisting mode and -39 dBm for the input modulated signal. If the chip input power is more than the minimum sensitivity in inductive coupling mode or if the battery voltage is higher than the minimum voltage required, the chip is able to transmit more than one burst in one clock cycle. Table 6-1 summarizes the performance of the proposed tag.

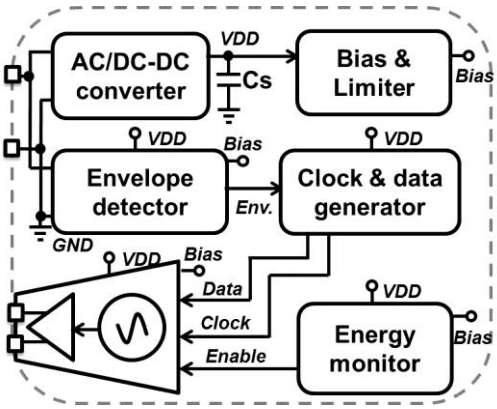


Figure 6-1. Functional block diagram of the proposed transponder.

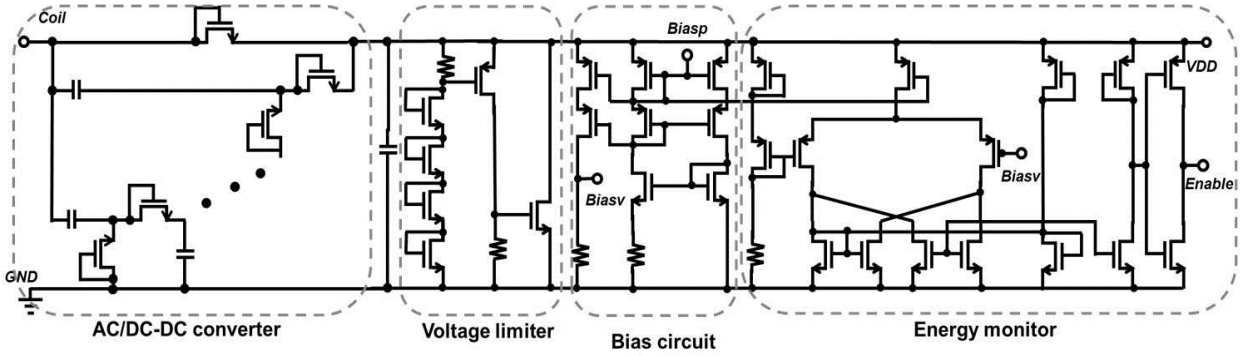


Figure 6-2. Schematic of the proposed ac/dc-dc converter and voltage level detector.

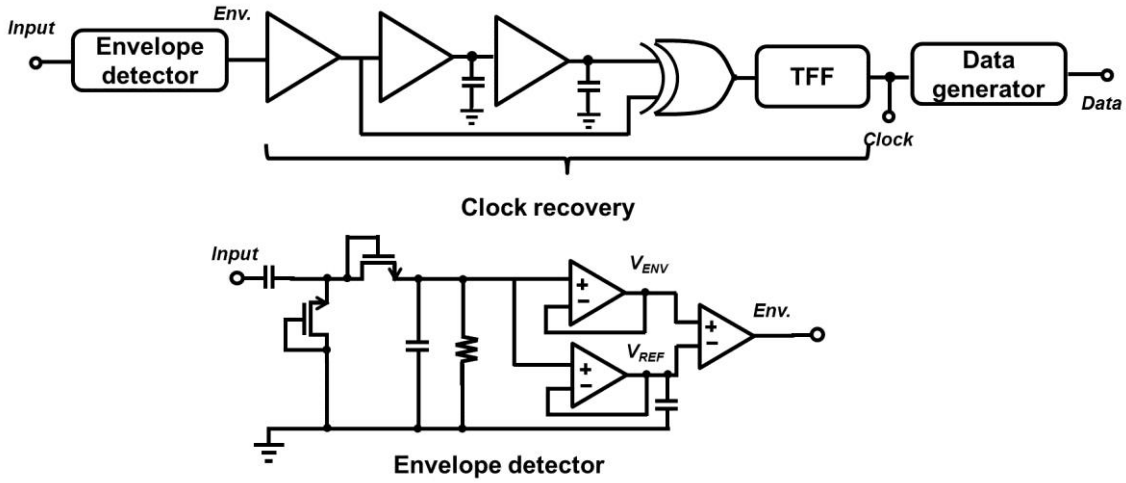


Figure 6-3. Schematic of the receiver circuit.

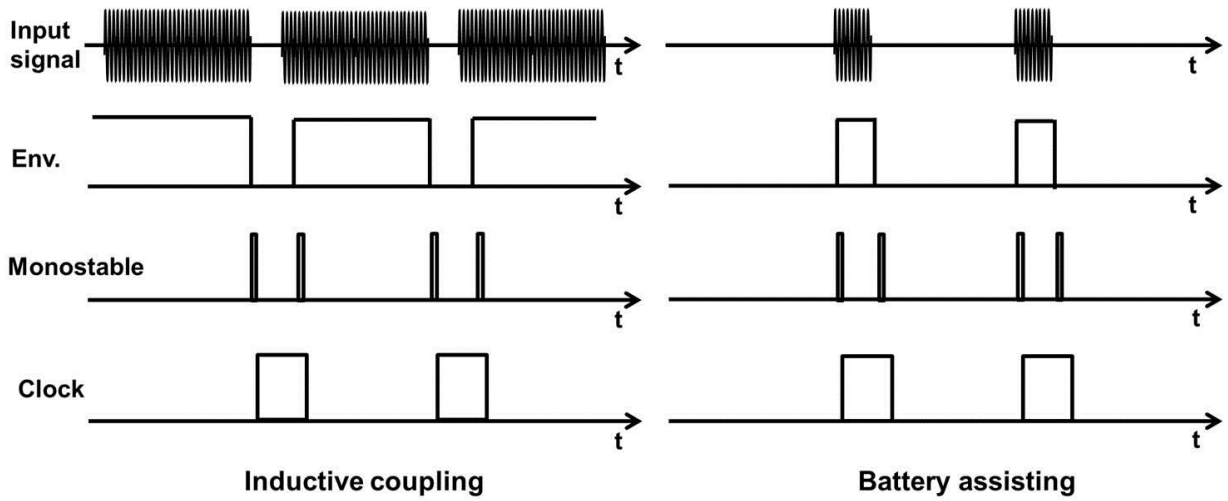


Figure 6-4. Timing diagram of the input signal and recovered clock from the clock recovery block in two modes.

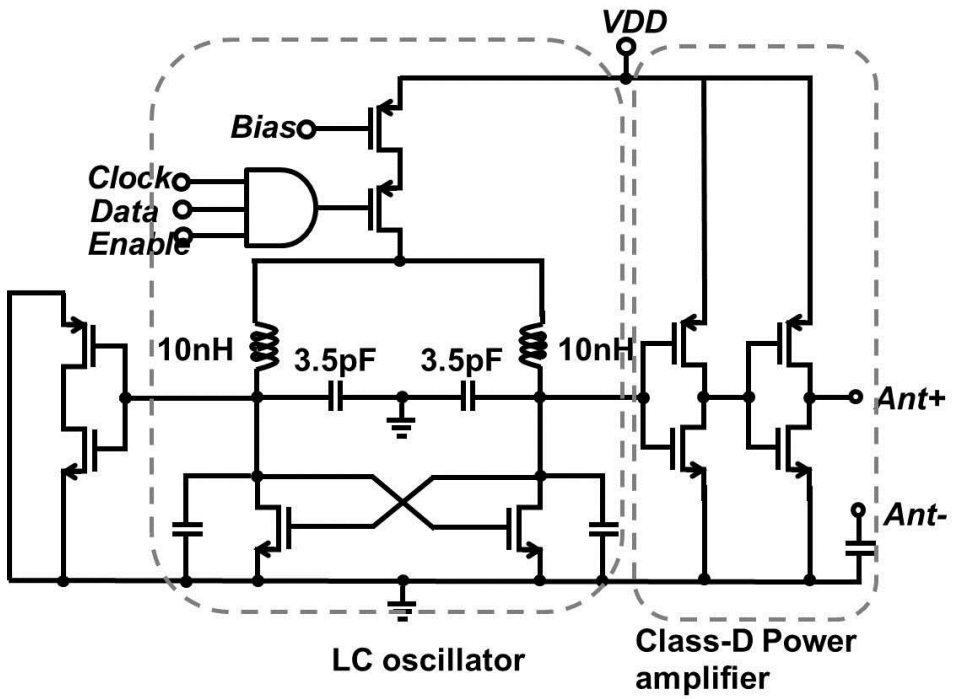


Figure 6-5. Schematic of the transmitter.

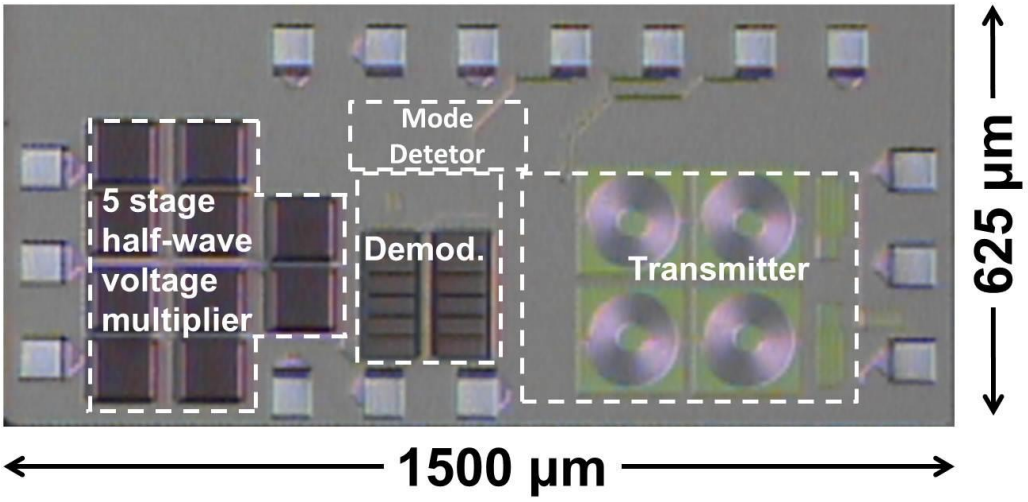


Figure 6-6. The photograph of the proposed transponder.

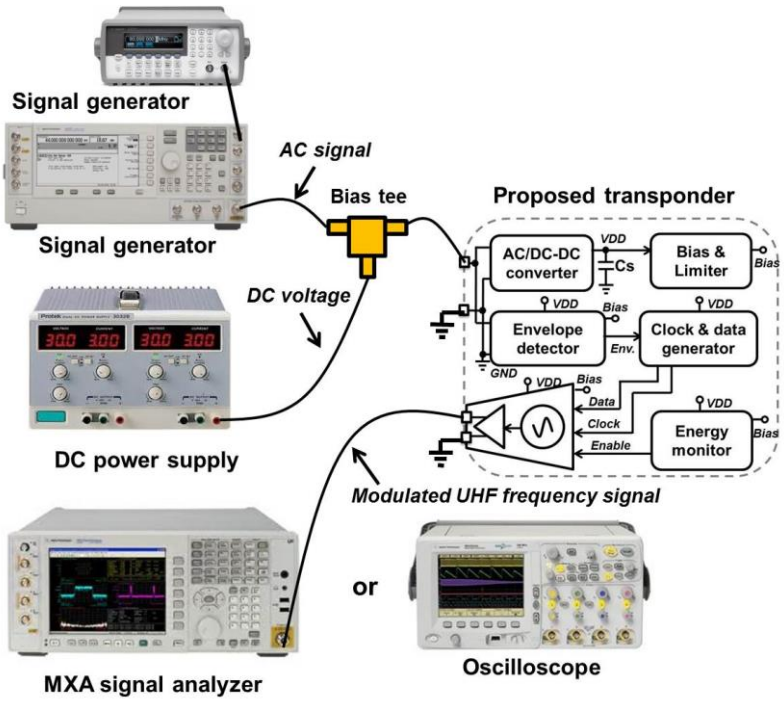


Figure 6-7. The measurement setup for the proposed transponder.

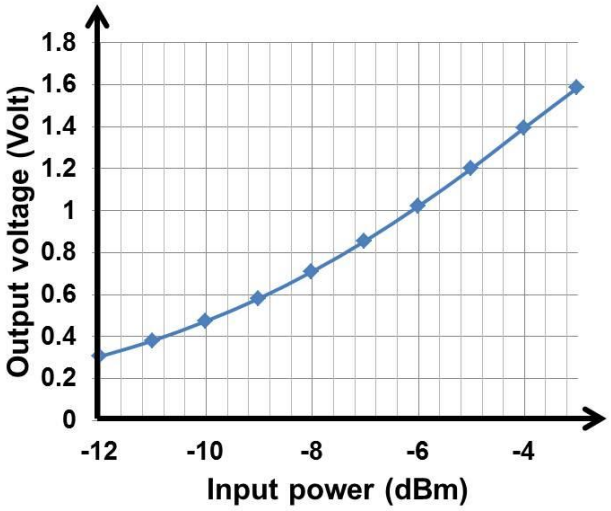


Figure 6-8. Measured input power vs. output voltage of the proposed AC/DC-DC converter.

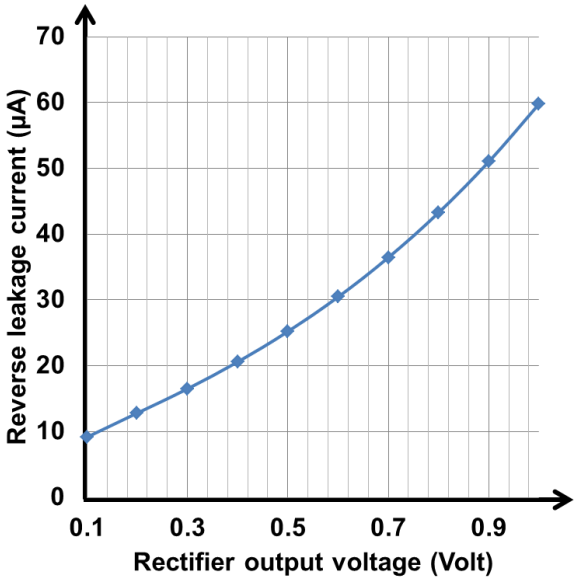


Figure 6-9. Measured reverse leakage current vs. output voltage of the proposed AC/DC-DC converter.

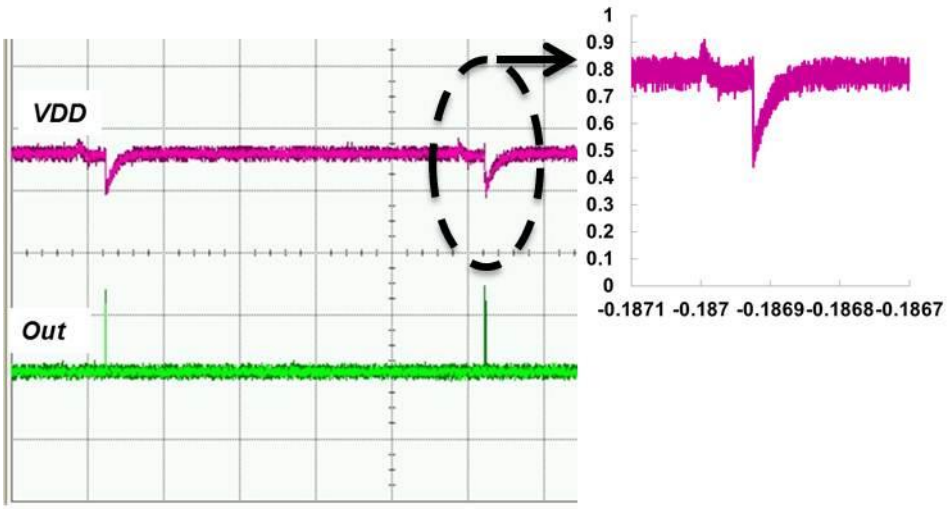


Figure 6-10. Measured timing waveforms of the output voltage of the converter and transponder.

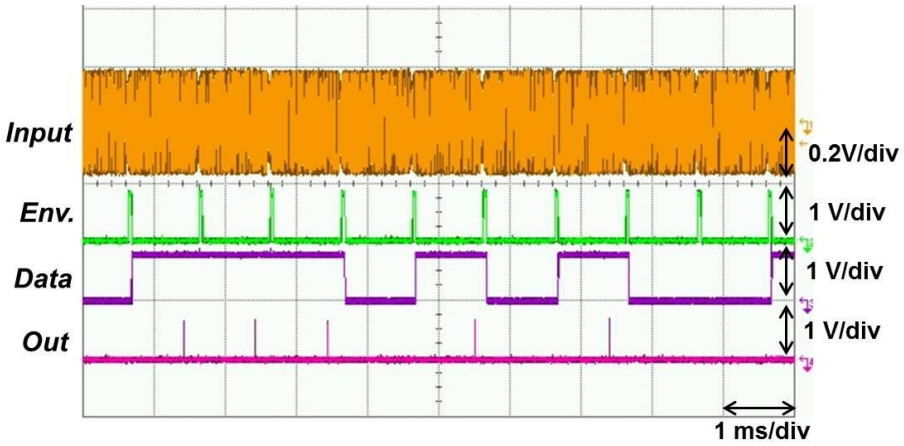


Figure 6-11. Measured input signal, envelope output, output data pattern and transponder output using inductive couple powering.

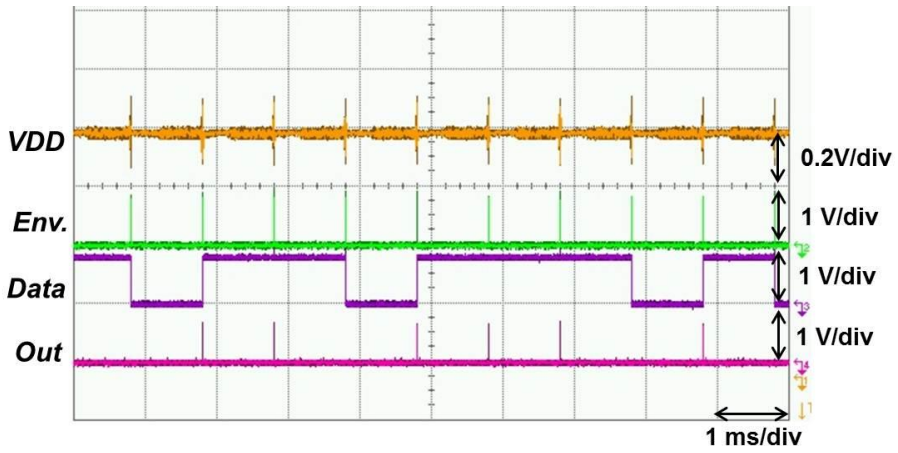


Figure 6-12. Measured input signal, envelope output, output data pattern and transponder output using battery powering.

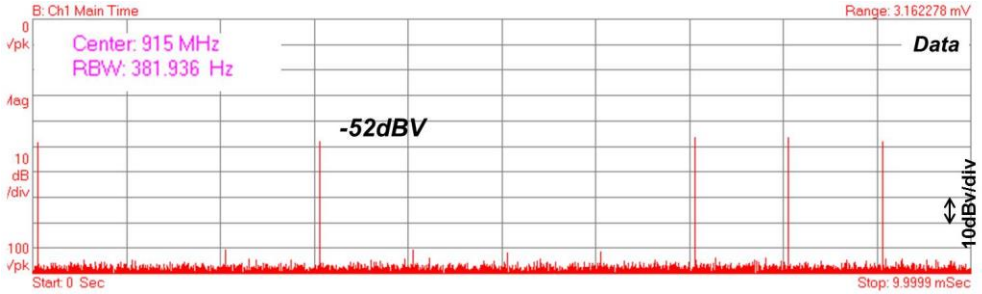


Figure 6-13. Measured output signal using signal analyzer.

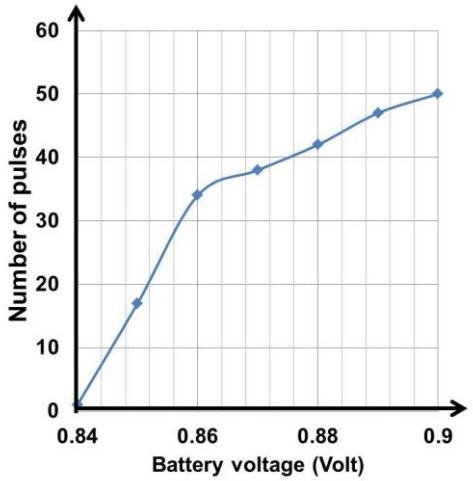


Figure 6-14. Measured number of output pulses vs. battery voltage.

Table 6-1. Summary of the proposed transponder performance.

	This work
Technology	130 nm CMOS technology
Power scheme:	
Near-field	13.56 MHz carrier
Battery assisted	Built-in battery
Sensitivity:	
Near-field coupling	-6.4 dBm
Battery assisted	-39 dBm
Data transmission MOD.	OOK
Die area	625×1500 μm^2

CHAPTER 7
CONCLUSION

7.1 Summary

This dissertation presents the challenges and benefits of using passive microsystems for biomedical applications. To maximize the power conversion efficiency, the energy harvester design is crucial. In chapter 3, we present an RF-DC multiplier design method that utilizes the I-V curve from the simulation or measurement. This method can quickly show the diode size, the required number of stages for the multiplier, and the minimum sensitivity to deliver the output load specifications. The rectifying diode's voltage loss is also very important to the multiplier design. The Schottky diode provides lower turn-on voltage, which minimizes the loss associated with the voltage drop. We designed and implemented several types of Schottky diodes in a standard CMOS process. The HF multipliers are designed to evaluate the performance of the implemented Schottky diodes. A UHF RF-DC multiplier is implemented by using the proposed method, and the simulation results and measured results are presented and discussed.

In order to provide reliable communication between the reader and transponder, the on-chip clock needs to be stable. Moreover, the clock generator consumes most of the power for the passive microsystem. In chapter 4, we present a new architecture of clock generator that uses DPLL. A new calibration-free-low-power clock generator is presented. A 200 nW DPLL is designed and implemented in a CMOS 130 nm process, and this DPLL is used as a clock generator for the passive transponder. Generating the clock in this way provides a stable clock frequency against process, temperature, and voltage variations, allowing reliable data decoding and encoding.

Chapter 5 presents a transponder that operates under AC input without any AC-DC conversion block and DC voltage conditioning block. Because the AC-DC and DC signal

conditioning blocks consume a large area, by using the proposed architecture, the chip area can be decreased. Moreover this proposed chip uses the input AC signal as the clock signal for system clock, thus a clock generator is not required for this transponder. In this chip, all the digital circuits are implemented using the AC logic. The advantages of this chip are the low cost and small die size. The die size of this proposed chip including pads is 0.1292 mm^2. The uplink and downlink frequencies are 125 kHz and 915 MHz, respectively.

Finally the chapter 6 presents a transponder that can be wirelessly programmed and used for medicine ID and can also be employed in medication compliance. The prototype of the transponder has advantages of both passive and active transponders. While this invention is extremely useful for applications that require a chip inside human body, the human body introduces higher loss than in air. The chip utilizes 13.56 MHz for the input carrier frequency and the 915 MHz for the output carrier frequency. The high output frequency can help minimize the antenna size. The transponder has -6.4 dBm sensitivity for near-field coupling and -39 dBm for the battery assisting mode, respectively. Since the chip burst rate depends on the voltage on the converter output, the number of output pulses is proportional to the input power or DC voltage of the chemical battery. Because of this unique characteristic of the transponder, the voltage information of the input power level or the DC voltage level of the battery can be wirelessly acquired.

7.2 Future Work

This dissertation presents several novel architectures of the transponder and shows their applications in the biomedical field. While developing and researching the RFID architecture and circuit blocks, several interested topics were discovered which are suitable for future research in

this field. Moreover, RFID transponders are widely used and in the future will be used in biomedical applications. The following is a list of topics for future research.

1. On-chip antenna research
2. Ultra-power circuit block and architecture research
3. Bio-compatible material for chemical battery
4. Transponder design on the organic semiconductor
5. High efficiency antenna design in electrical small antenna
6. RFID technology combines with analog frontend for biomedical applications

LIST OF REFERENCES

[1] M. Ghovanloo and K. Najafi, "A wide-band frequency-shift keying wireless link for inductively powered biomedical implants," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 51, no. 12, pp. 2374-2383, Dec. 2004.

[2] T. Akin, K. Najafi and R. M. Bradely, "A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode," IEEE J. Solid-State Circuits, vol. 33, no. 1, pp. 109-118, Jan. 1998.

[3] Y. Hang, C. M. Tang and R. Bashirullah, "An asymmetric RF tagging IC for ingestible medication compliance capsules," in IEEE Radio Frequency Integrated Circuits (RFIC) Symp., Boston, June 2009.

[4] D. Yeager, F. Zhang, A. Zarrasvand, T. Daniel, N. T. George and B. P. Otis, "A 9 uA, addressable gen2 sensor tag for biosignal acquisition," IEEE J. Solid-State Circuits, vol. 45, no. 10, pp. 2198-2209, Oct. 2010.

[5] B. Ziaie, M. D. Nardin, R. Coghlan and K. Najafi, "A single-channel implantable microstimulator for functional neuromuscular stimulation," IEEE Trans. Biomedical Engineering,, vol. 44, no. 10, pp. 909-920, 1997.

[6] G. Wang, W. Liu, M. Sivaprakasam and G. A. Kendir, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," IEEE Trans. Circuits and Systems I: Regular Papers, vol. 52, no. 10, pp. 2109-2117, 2005.

[7] M. Ghovanloo and S. Atluri, "A wide-band power-efficient inductive wireless link for implantable microelectronic devices using multiple carriers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 10, pp. 2211-2221, 2007.

[8] EPC radio-frequency identity protocols class-1 generation-2 UHF RFID protocol for communicaions at 860MHz - 960MHz,version 1.0.9, EPCglobal Inc., 2005.

[9] F. Cilek, K. Seemann, G. Holweg and R. Weigel, "Impact of the local oscillator on baseband processing in RFID transponder," in Int. Symp. Signals Systems Electron, Aug. 2007.

[10] V. Pillai, H. Heinrich, D. Dieska, P. V. Nikitin, R. Martinez and K. V. S. Rao, "An ultra-low-power long range battery/passive RFID tag for UHF and microwave bands with a current consumption of 700 nA at 1.5 V," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 7, pp. 1500-1512, 1500–1512.

[11] Z. Xiao, C.-M. Tang, C. Dougherty and R. Bashirullah, "A 20uW neural recording tag with supply-current-modulated AFE in 0.13um CMOS," in IEEE ISSCC Dig.Tech. Papers, 2010.

[12] Y.-T. Liao, H. Yao, A. Lingley, B. Parviz and B. P. Otis, "A 3-uW CMOS glucose sensor for wireless contact-lens tear glucose monitoring," IEEE J. Solid-State Circuits, vol. 45, no. 10, pp. 2198-2209, Jan. 2012.

[13] A. Vaz, A. Ubarretxena, I. Zalbide, D. Pardo, H. Solar, A. García-Alonso and R. Berenguer, "Full passive UHF tag with a temperature sensor suitable for human body temperature monitoring," IEEE Trans. Circuits and Systems II: Express Papers, vol. 57, no. 2, pp. 95-99, Feb. 2010.

[14] R. Bashirullah, L. Wentai, J. Ying, A. Kendir, M. Sivaprakasam, W. Guoxing and B. Pundi, "A smart bi-directional telemetry unit for retinal prosthetic device," in IEEE International Symposium on Circuit and System, 2003.

[15] W. Liu, K. Vichienchom, M. Clements, S. DeMarco, C. Hughs, E. McGucken, M. Humayun, E. Juan, J. Weiland and R. Greenber, "A neuron-stimulus chip with telemetry unit for retinal prosthetic device," IEEE J. Solid-State Circuits, vol. 35, no. 10, pp. 1487-1497, Oct. 2000.

[16] G. K. Balachandran and R. E. Barnett, "A 110 nA voltage regulator system with dynamic bandwidth boosting for RFID systems," IEEE J. Solid-State Circuits, vol. 41, no. 9, pp. 2019-2028, 2006.

[17] G. De Vita and G. Iannaccone, "Ultra-low-power series voltage regulator for passive RFID transponders with subthreshold logic," IEEE Electronics Letters, vol. 42, no. 23, pp. 1350-1351, 2006.

[18] D. M. Dobkin, The RF in RFID: Passive UHF RFID in Practice, Newnes, 2007.

[19] R. R. Harrisonan and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," Solid-State Circuits, IEEE Journal of, vol. 38, no. 6, pp. 958-965, Jun. 2003..

[20] Z. Xiao, T. Chun-Ming, C.-C. Peng and R. Bashirullah, "A 190µW–915MHz active neural transponder with 4-channel time multiplexed AFE," in IEEE Symposium on VLSI Circuits, 2009.

[21] S. Rai, J. Holleman, J. N. Pandey, F. Zhang and B. Otis, "A 500µW neural tag with 2µVrms AFE and frequency-multiplying MICS/ISM FSK transmitter," in IEEE ISSCC Dig.Tech. Papers, 2009.

[22] A. P. Chandrakasan, N. Verma and D. C. Daly, "Ultralowpower electronics for biomedical applications," Annual Review of Biomedical Engineering, vol. 10, pp. 247-274, 2008.

[23] X. Zou, W.-S. Liew, L. Yao and Y. Lian, "A 1V 22µW 32-channel implantable EEG recording IC," in IEEE ISSCC Dig.Tech. Papers, 2010.

[24] C. A. Balanis, Antenna theory: analysis and design, John Wiley & Sons, 1997.

[25] S. L. a. P. Combes, "On radiating-zone boundaries of shor, lambda/2, and lambda dipoles," IEEE Antennas and Propagation Magazine, vol. 46, no. 5, pp. 53-64, 2004.

[26] H. P. Shawn, "Electrical properties of tissue and cell suspensions," Advances in Biological and Medical Physics, vol. 5, pp. 147-209, 1957.

[27] K. R. Foster and H. P. Schwan, "Dielectric properties of tissues and biological materials: A critical review," Critical reviews in biomedical Engineering, vol. 1, pp. 25-104, 1989.

[28] D. C. Barber and B. H. Brown, "Applied potential tomography," Journal of Physics E: Scientific Instruments, vol. 17, pp. 723-733, 1984.

[29] S. Gabriel, R. W. Lau and C. Gabriel, "The dielectric properties of biological tissues: II. Measurements in the frequency range 10 Hz to 20 GHz," Phys. Med. Biology, vol. 41, pp. 2251-2269, 1996.

[30] R. Harrison, "Designing Efficient Inductive Power Links for Implantable Devices," in IEEE International Symposium on Circuit and System, 2007.

[31] Friis, "A note on a simple transmission formula," Pro. IRE, vol. 34, pp. 254-256, 1946.

[32] J. D. Kraus and D. A. Fleisch, Electromagnetics, McGraw-Hill, 1999.

[33] D.M.Pozar, Microwave Engineering, Wiley, 1998.

[34] M. S. Wegmuller, "Intra-body communication for biomedical sensor networks," PhD dissertation, ETH No.17323, 2007.

[35] T. G. Zimmerman, "Personal area network (PAN)," Master thesis, Massachusetts Institute of Technology, 1995.

[36] K. Hachisuka, A. Nakata, T. Takeda, Y. Terauchi, K. Shiba, K. Sasaki, H. Hosaka, and K. Itao, "Development and performance analysis of an intra-body communication device," in International Conference on Transducers, Solid-State Sensors, Actuators and Microsystems, 2003.

[37] J. R. Tuttle, "Traditional and emerging technologies and applications in the radio frequency identification (RFID) industry," in IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 1997.

[38] J. Proakis, Digital Communications, McGraw-Hill, 2000.

[39] K. Finkenzeller, RFID handbook, 2nd ed., Wiley, 2003.

[40] IEEE C95.1-2005, IEEE Standard for Safety Levels with Respect to Human Exposure to Radio Frequency Electromagnetic Fields, 3 kHz to 300 GHz, New York: The Institute of Electrical and Electronics Engineers Inc., 2006.

[41] W. H. Ko, S. P. Liang and C. D. Fung, "Design of radio-frequency powered coils for implant instruments," Med. Biol. Eng. Comput-15, pp. 634-640, 1977.

[42] K. D. Wise, D. J. Anderson, J. F. Hetke, D. P. Kipke and K. Najafi, "Wireless Implantable Microsystems: High-Density Electronic Interfaces to the Nervous System," IEEE Proceedings, vol. 92, no. 1, pp. 76-97, 2004.

[43] M. Nagata, A. Saraswat, H. Nakahara, H. Yumoto, D.M. Skinlo, K. Takeya and H. Tsukamoto, "Miniature pin-type lithium batteries for medical applications," J. of Power Sources, vol. 146, no. 1, pp. 762-765, 2005.

[44] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power," IEEE J. Solid-State Circuits, vol. 38, no. 10, pp. 1602-1609, 2003.

[45] R. Barnett, G. Balachandran, S. Lazar, B. Kramer, G. Konnail, S. Rajasekhar, and V. Drobny, "A passive UHF RFID transponder for EPC Gen 2 with -14dBm sensitivity in 0.13um CMOS," in IEEE ISSCC Dig.Tech. Papers, 2007.

[46] V. Milanovic; M. Gaitan; J. C. Marshall and M. E. Zaghloul, "CMOS foundry implementation of Schottky diodes for RF detection," , IEEE Trans. Electron Devices, vol. 43, no. 12, pp. 2210-2214, 1996.

[47] S. Sankaran and K. K. O, "Schottky barrier diodes for millimeter wave detection in a foundry CMOS process," IEEE Electron Device Letters, vol. 26, no. 7, pp. 492-494, 2005.

[48] S. I. Cha, Y. H. Cho, Y. I. Choi and S. K. Chung, "Novel Schottky didoe with selfaligned guard ring," Electronics Letters, vol. 28, no. 13, pp. 1221-1223, 1992.

[49] J. F. Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits," IEEE J. Solid-State Circuits, Vols. SC-11, no. 3, pp. 374-378, 1976.

[50] J-P Curty, N. Joehl, C. Dehollain, and M. Declercq, "Remotely powered addressable UHF RFID integrated system," IEEE J. Solid-State Circuits, vol. 40, no. 11, pp. 2193-2202, 2005.

[51] G. De Vita and G. Iannaccone, "Design criteria for the RF section of UHF and microwave passive RFID transponders," IEEE Trans. Microwave Theory and Techniques, vol. 53, no. 9, pp. 2978-2990, 2005.

[52] S. Sankaran and K. K. O., "Schottky diode with cutoff frequency of 400 GHz fabricated in 0.18 μm CMOS," Electronics Letters, vol. 41, no. 8, pp. 506-508, 2005.

[53] M. Shur, Physics of Semiconductor Devices, Prentice-Hall, 1990.

[54] L. K. L. a. H. C. Luong, "A 7-uW clock generator in 0.18-um CMOS for passive UHF RFID EPC G2 tags," in Europe Solid-State Circuit Conference, Sep. 2007.

[55] J-W. Lee and B. Lee, "A Long-Range UHF-Band Passive RFID Tag IC Based on High-Q Design Approach," IEEE Trans. Industrial Electronics, vol. 56, no. 7, pp. 2308-2316, 2009.

[56] V. Najafi, M. Jenabi, S. Mohammadi, A. Fotowat-Ahmady, and M. B. Marvasti, "A dual mode EPC gen 2 UHF RFID transponder in 0.18µm CMOS," in Proc. IEEE Int. Conf. Electron. Circuits and Systems, Aug. 2008.

[57] C. F. Chan, K. P. Pun, K. N. Leung, J. Guo and L. K. L. a. C. S. Chiu, "A Low-Power Continuously-Calibrated Clock Recovery Circuit for UHF RFID EPC Class-1 Generation-2 Transponders," IEEE J. Solid-State Circuits, vol. 45, no. 3, pp. 587-599, Mar. 2010.

[58] K. N. L. a. P. K. T. Mok, "A CMOS voltage reference based on weighted ΔVGS for CMOS low-dropout linear regulators," Solid-State Circuits, IEEE Journal of, vol. 38, no. 1, pp. 146-150, Jan. 2003.

[59] J. M. Rabaey and A. C. a. B. N. , Digital Integrated Circuits (2nd Edition), 2003.

[60] W. H. Chen; W. F. Loke and B. jung, "A 0.5-V, 440-µW Frequency Synthesizer for Implantable Medical Devices," Solid-State Circuits, IEEE Journal of, vol. 47, no. 8, pp. 1896-1907, 2012.

[61] P. Raha, "A 0.6–4.2 V low-power configurable PLL architecture for 6 GHz-300MHz applications in a 90 nmCMOS process," in Proc. Symp. VLSI Circuits, Jun. 2004.

[62] Y. L. Lo ; W. B. Yang and K. H. Cheng , "Designing ultra-lowvoltage PLL using a bulk-driven technique," in Proc. European Solid-State Circuits Conf., Sep. 2009.

[63] K. H. Cheng, "A 0.5-V 0.4–2.24-GHz inductorless phase-locked loop in a system-on-chip," IEEE Transactions on Circuits and Systems I: Regular Papers , vol. 58, no. 5, p. 849–859, May 2011.

[64] W. H. Chen; W. F. Loke and B. jung, "A 0.5-V, 440-µW Frequency Synthesizer for Implantable Medical Devices," IEEE J. Solid-State Circuits, vol. 47, no. 8, pp. 1896-1907, 2012.

[65] R. Barnett and J. Liu, "A 0.8V 1.52MHz MSVC Relaxation Oscillator with Inverted Mirror Feedback Reference for UHF RFID," in IEEE Custom Integrated Circuits Conference, 2006.

[66] S. Briole, C. Pacha, K. Goser, A. Kaiser, R. Thewes, and W. Weber, "AC-Only RF ID Tags for Barcode Replacement," in IEEE ISSCC Dig.Tech. Papers, 2004.

[67] Y. Ye and K. Roy, "QSERL: Quasi-Static Energy Recovery Logic," IEEE J. Solid-State Circuits, vol. 36, no. 2, pp. 239-248, 2001.

[68] M. K. Kazimierczuk, RF Power Amplifiers, Wiley, 2008.

BIOGRAPHICAL SKETCH

Chun-Ming Tang was born in Taipei, Taiwan. He received his bachelor's degree from the National Central University, Chung-Li, Taiwan, in 2000, and his master's degree in electronics from National Tsing-Hua University, Hsin-Chu, Taiwan, in 2002. From 2002 to 2005, he was an analog IC design engineer with FrontAnD technology in Hsin-Chu, Taiwan, where he worked on limiting amplifiers and laser diode drivers for optical fiber communication applications. Since 2006, he has been working as a research assistant at the Integrated Circuits Research (ICR) Lab under the guidance of Dr. Rizwan Bashirullah. His research interests include low power and energy harvesting circuits for wireless sensors and RFID applications. Since 2013, he has been part of the circuit design division of the image sensor group at OmniVision, working on various low power circuits for CMOS image sensors.