INVESTIGATION OF STRESS EFFECTS ON FERROELECTRIC CAPACITORS FOR PERFORMANCE ENHANCEMENT OF FERROELECTRIC RANDOM ACCESS MEMORY

By

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2012

To my mother, father, and three beautiful sisters: Janeth, Jessica, and Janel

ACKNOWLEDGMENTS

First and foremost, I would like to thank my advisor, Dr. Toshikazu Nishida, for giving me the opportunity to work on a Ph.D. and pursue my research interests under his guidance at the University of Florida. His constant support, encouragement, and teachings have been instrumental in making me not only a better researcher but also a better person. I would also like to thank my Ph.D. committee members Dr. Scott Thompson, Dr. Jing Guo, Dr. Jacob Jones, and Dr. John Rodriguez.

I would like to give a special thanks to our collaborators at Texas Instruments Incorporated, especially Dr. John Rodriguez. He has supported this project from the beginning and was very instrumental in making this work a reality. His technical expertise and our weekly discussions with him have been significant to the progress that has been made to date. He has also been very supportive and helpful in my professional development as a researcher and engineer. I also owe a very deep thanks to Dr. Srikanth Krishnan and Dr. Ted Moise, without whom this project would not have been possible. The constant support and resources they have provided to the project have been important to its progression. Thank you also to Dr. Scott Summerfelt and Dr. Kezhakkedah Udayakumar for their suggestions, feedback, and interest in this work.

Finally, I would like to thank my research colleagues and fellow students for their support and help with experiments, technical discussions, social gatherings, and for providing a pleasant and joyful working environment every day: Dr. Hyunwoo Park, Dr. Min Chu, Dr. Andrew Koehler, Dr. Erin Patrick, Dr. Robert Dieme, Mehmet Baykan, Ashish Kumar, Amit Gupta, Shancy Augustine, Viswanath Sankar, and Peng Zhao. I would especially like to thank Srivatsan Parthasarathy for his help in writing the software code for automating the measurement and test set-up and for his interest in the project.

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August 2012

Chair: Toshikazu Nishida
Major: Electrical and Computer Engineering

Ferroelectric Random Access Memory (FRAM) has emerged as a viable nonvolatile memory in recent years due to its low power, fast read/write times, and high cycling endurance. Future technology scaling can lead to increased storage density and reduced costs which can in turn enable new markets and applications. However, further scaling of FRAM remains a challenge. Ferroelectric capacitors lose their polarization as their thickness decreases due to a decrease in tetragonality and asymmetry in the crystal lattice arising from electrostatics at the film and electrode interface. The stress effects also become more pronounced as the film thickness decreases. With a smaller film thickness the mismatch strain imposed by the underlying substrate becomes more significant.

While temperature and bias have been traditionally used to pole ferroelectric capacitors, mechanical stress has also been shown to change the switching behavior. This work experimentally investigated the combined effects of stress, temperature, and bias on the ferroelectric properties of lead zirconate titanate (PZT) thin-film capacitors for the purposes of FRAM enhancement. An optimal combination of these three

variables may enhance the performance of FRAM devices and enable scaling to future technology nodes.

A mechanical compressive stress was applied to 70nm PZT thin film ferroelectric capacitors embedded in a 130-nm CMOS technology process. Stress effects were characterized at room temperature, at elevated temperature, and as a combination of stress, temperature, and electric field. An increase of 3.37% per -100MPa at room temperature was observed. This increase was attributed to the reorientation of domains from in-plane polarization to out-of-plane polarization. In contrast, polarization enhancement of up to 585% was observed when the ferroelectric capacitors were annealed at elevated temperature while under a uniaxial compressive stress. This large increase was attributed to the activation and switching of previously pinned domains due to annealing at a temperature approaching the Curie point while under compressive stress.

Electrically poling the ferroelectric capacitors while under a compressive stress and elevated temperature was also found to permanently increase the switching polarization. A permanent increase in the switching polarization of up to 15% was observed when a bipolar pulse was continually applied while the sample was under a compressive stress of -148MPa at 205°C. Stress and electric field were also applied as the sample cooled down to room temperature. An energy-based switching model is presented to explain these results. In this model a critical energy, supplied in the form electrical and mechanical energy, is required to reorient 90° domains. Application of temperature eliminates or decreases defects in the film which enables previously pinned domains to participate in the polarization switching process.

CHAPTER 1
INTRODUCTION

1.1 Motivation

As the market for low-power, high-performance, and portable electronic devices continues to grow, there is an increasing demand for a non-volatile memory technology that can meet all of these requirements. Ferroelectrics are materials that show a spontaneous polarization when no external electric field is applied. Ferroelectric random access memory (FRAM) based on metal-organic chemical vapor deposition (MOCVD) technology has emerged over the past decade as a viable non-volatile memory technology for applications requiring low power consumption, fast read/write times, and high cycling endurance [1], [2]. Due to simultaneous features of low power, fast speed, and high endurance, FRAM technology has been proposed as a possible solution to the long-sought universal memory [3]. However, further scaling of FRAM is required to realize its potential as a non-volatile memory technology.

While currently manufactured at the 130-nm node [4] , further scaling of FRAM to 90-nm technology and beyond can increase storage density and reduce production costs [5], enabling new market applications. Technology scaling requires a decrease in the thickness of the ferroelectric thin-film layer which may result in overall reduced polarization [6], [7]. The industry consensus is that new structures and/or materials may be needed to scale FRAM to the 90-nm technology node and beyond [3], [5], [8–11].

Figure 1-1 shows a projection of FRAM technology through the year 2014 [5] by Fujitsu, a leading manufacturer of FRAM. As seen in the figure, Fujitsu expects a three-dimensional (3D) trench capacitor structure at the 90-nm node in contrast to the current stacked planar structure being used. Beyond that, they predict that ferroelectric field-

effect transistors (FeFET) will be required in order to allow for FRAM technology scaling.

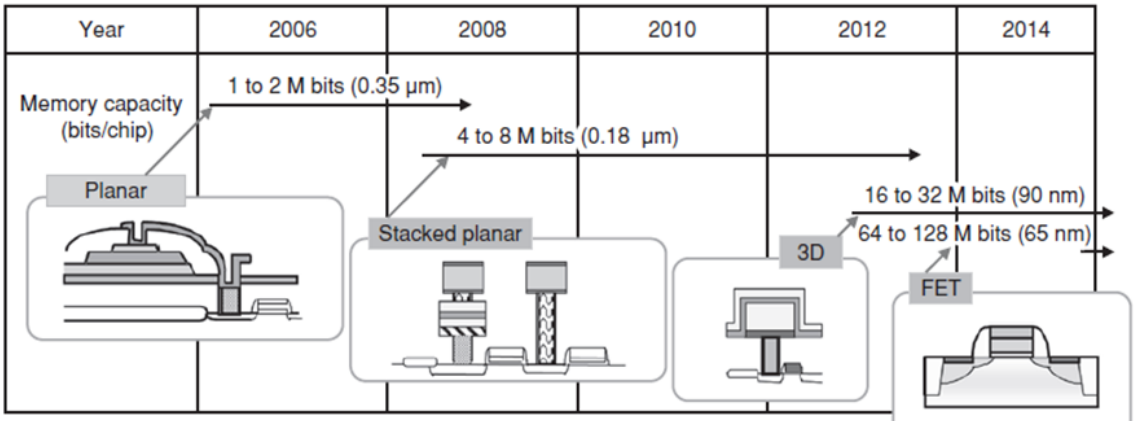

Figure 1-1. Fujitsu FRAM technology scaling roadmap. [Reprinted with permission from V. Kondo and V. Singh, "New ferroelectric material for embedded FRAM LSIs," *Fujitsu Sci. Tech. J.*, vol. 507, no. 4, pp. 502-507, Oct. 2007.]

Table 1-1 shows key embedded FRAM design features by Texas Instruments [12], another leading manufacturer of FRAM products. While these features have already been implemented into their current 130-nm FRAM products [1], [4], projections are shown for both the 90-nm and 65-nm technology nodes. According to their roadmap, Texas Instruments expects the use of a 3-D capacitor structure beyond the 65-nm node. As can be seen in Table 1-1, a decrease in supply voltage, capacitor area, cell area, and bitline capacitance is expected with technology scaling which will lead to a decrease in switched polarization (P_{sw}).

In addition, as the ferroelectric thin-film thickness decreases, the induced stress in the film becomes more prominent. Depending on the type and amount of stress induced, the ferroelectric properties may be enhanced or degraded. It is therefore

important to understand the underlying physics of stress effects on the properties of ferroelectric thin films.

Table 1-1. Texas Instruments key embedded FRAM design features.

Logic Node (nm)	130	90	~65
Metal half-pitch (nm)	175	135	90
Supply Voltage (V)	1.5	1.2	90
Cell Type	2d	2d	2d
Mask Adder	2	2	2
Cell Area (µm2)	0.71	0.35	0.24
Capacitor Area-Si	0.36	0.18	0.13
Bitline Capacitance (fF)	240	180	120

 [Adapted with permission from K. Udayakumar *et al.*, "Bit distribution and reliability of high density 1.5 V Ferroelectric Random Access Memory embedded with 130 nm, 5lm copper complementary metal oxide semiconductor logic," *Jpn. J. Appl. Phys.*, vol. 45, no. 4B, p. 3202, Apr. 2006.]

According to industry projection [3], [5], [8–11] it is clear that a change in the structure and/or materials of FRAM is necessary to scale the technology. However, these changes can lead to increased costs and development times. The ideal solution would be to extend the current FRAM stacked planar technology as much as possible while reducing the cell area to allow for scaling. Stress engineering can be a possible solution for extending the planar structure to 90-nm technology and beyond. Hence, it is important to understand stress effects on the properties of ferroelectric thin films and their reliability as the film thickness decreases with technology scaling.

FRAM signal margin, a key metric in reliable memory operation, is directly related to the amount of switched polarization (P_{sw}) in a ferroelectric capacitor. In addition to composition and structural details in an as-fabricated capacitor, P_{sw} can be modified through various external means. Conventionally, ferroelectric materials have been poled by applying an electrical bias at elevated temperature as a means of increasing P_{sw}. Mechanical stress has also been shown to modify the polarization in ferroelectric

materials [13–23]. Depending on the type of mechanical stress applied, the ferroelectric properties may be enhanced or degraded.

Preliminary data has shown an enhancement in switched polarization with applied compressive stress at room temperature, consistent with what has been reported in the literature [13], [18], [20], [24]. However, the polarization enhancement by stress alone may not be sufficient to successfully enhance the ferroelectric properties and thus allow current FRAM technology to scale. The combined application of stress, temperature, and bias has the potential to enable scaling of FRAM technology by maintaining and/or improving performance of ferroelectric devices at the 130-nm node and beyond.

1.2 Objectives and Organization

It is the aim of this work to experimentally investigate the combined effects of stress, temperature, and bias on the properties of MOCVD PZT ferroelectric thin-film capacitors. A better understanding of the underlying physics of these effects may be used to advantageously enhance FRAM performance. The knowledge gained can be used to potentially exploit the effects of stress, temperature, and bias to enhance the ferroelectric properties and enable scaling of FRAM technology using the current stacked planar structure.

To date no work has been done to comprehensively investigate the combined effects of stress, temperature, and electric bias on advanced FRAM technology, to the best knowledge of the author. The main goal of this work was to experimentally investigate the effects of stress, temperature, and electric bias on the ferroelectric properties of embedded MOCVD PZT thin-film ferroelectric capacitors. This was accomplished in three different phases: (1) stress effects at room temperature, (2)

stress effects at elevated temperatures, and (3) the combined effects of stress, elevated temperature, and electric bias.

The main contribution of the present work is the experimental verification that mechanical stress, temperature, and electric bias can all be used to enhance the switching polarization in ferroelectric capacitors. As FRAM technology scales, these effects can be exploited to maintain the required FRAM signal margin. Switching polarization was permanently enhanced on fully processed PZT thin film capacitors by applying a combination of stress, elevated temperature, and electric field. Another contribution is an improved understanding of the underlying physics of the stress effects on ferroelectric capacitors. Furthermore, the knowledge obtained from this work can be used to develop strategies that exploit effects of stress, temperature, and bias on ferroelectric thin films for enhancement of FRAM performance. This, in turn, can enable the scaling of FRAM technology using the current stacked capacitor planar structure. In addition, the knowledge and understanding gained from this work can be used in the development of future ferroelectric-based devices. It is important to note that the potential application for ferroelectric thin films extends beyond memory devices. While the focus of this work is on ferroelectric thin films for FRAM applications, the understanding of the underlying physics gained can contribute to the future development of ferroelectric thin films for nanoscale applications.

Chapter 2 gives an overview of ferroelectric thin films and devices. After an overview of ferroelectric materials, the applications of ferroelectric thin films are discussed. A brief background on ferroelectric memories is then given. Next, the physics of ferroelectric thin films are described including domain structure, formation,

and switching properties. The effects of stress on ferroelectric thin films are also presented and discussed. The chapter ends with a description of the basic operation and memory structure of current FRAM devices.

Chapter 3 describes the experimental set-up and characterization of ferroelectric capacitors. This includes wafer bending, hysteresis measurement, pulse testing, and reliability testing. The experimental set-up used for this work is explained in detail at the end of the chapter.

Chapter 4 describes the effects of a uniaxial compressive stress at room temperature on PZT thin film capacitors. An introduction, background, and experimental details are first described. A change in P_r of 3.37% per -100MPa was observed, with a similar trend for P_{sw}. Compressive stress did not appear to accelerate cycling fatigue mechanisms. These changes are attributed to an increase in the lattice tetragonality and reorientation of 90° domains, both effects due to compressive stress. The results are consistent with previously published data. Differences in the magnitude of the polarization changes are attributed to residual stresses, processing and structural differences in the ferroelectric capacitors.

The effects of stress at elevated temperature are presented in Chapter 5. An introduction is given that describes the motivation for the work and outlines the components of the chapter. Since one goal is the enhancement of polarization, the maximum polarization in PZT thin films and effects of temperature is discussed. This is followed by a description of the experimental details and methods used to modify the ferroelectric structure. A novel quartz apparatus was used to apply stress at elevated temperatures. Temperatures up to 430°C were applied to the ferroelectric capacitors

while under stress. An increase of over 550% in P_r observed for the smallest capacitor area. Similar results were also observed at 370°C. It is believed that application of elevated temperature activates previously inactive domains. As the capacitor is cooled to room temperature while under a compressive stress, the domains will preferentially orient to the out-of-plane direction, leading to the large polarization that was observed. Subsequent cycling endurance tests showed that the enhanced P_r remained stable at room temperature.

Chapter 6 describes the combined effects of stress, temperature, and electric field on the properties of thin film PZT ferroelectric capacitors. The motivation for this work is to permanently enhance the polarization using a lower temperature, since applying high temperature to the devices may damage surrounding circuitry. A brief background on the efforts to pole ferroelectric materials and capacitors using a combination of electric field, stress, and temperature is given. Stress assisted electrical poling at room temperature showed enhanced P_{sw} of 2-4% when compared to electrical poling with no externally applied stress. The switching polarization was permanently enhanced up to 15% when a ferroelectric capacitor was electrically poled at -150MPa and 205°C. An energy based model is then given to describe the results. In this model a critical energy is required to reorient in-plane domains to the out-of-plane direction. The addition of stress into the poling process increases the energy and thus there is more 90° domain reorientation. Application of temperature in addition to stress will eliminate or decrease defects in the film, activating domains that were previously pinned and not contributing to the switching polarization process.

Finally, Chapter 7 summarizes the entire work that was presented and recommendations for future work are also described. Reliability testing under compressive stress at room and elevated temperatures are recommended. Experiments are suggested to further investigate the effects of stress, temperature, and electric field on ferroelectric properties. X-ray diffraction experiments and quantitative modeling are also recommended for validating the results.

CHAPTER 2
FERROELECTRIC THIN FILMS, DEVICES, AND STRESS EFFECTS

This chapter provides an overview of ferroelectric thin films and their applications. Ferroelectric materials are first defined and described. The physics of ferroelectric thin films is then presented. Domain structure and formation, the switching properties, and size effects are all considered. The effects of stress on ferroelectric thin films are also discussed. Finally, a general introduction to FRAM operation is given.

2.1 Ferroelectric Materials

Ferroelectric materials are dielectric crystals which exhibit a spontaneous polarization [25]. This spontaneous polarization is possible due to asymmetry in the crystal structure. Ferroelectrics have a distorted perovskite structure with the general chemical formula of ABO_3 where A and B are both metals. Figure 2-1 shows the lattice structure for a tetragonal PZT. Here, the Pb ions are located at the corners of the crystal and the O_2 ions are on the center faces. The single Zr/Ti ion is located in the center of the lattice. Its displacement along the polar (or *c*) axis relative to the oxygen ions is what makes spontaneous polarization possible. Spontaneous polarization is related to the surface charge density by [25]

$$P_s = \sigma \tag{2-1}$$

where P_s is the spontaneous polarization and σ is the surface charge density which have units of C/cm^2. These surface charges are typically compensated by defect charges [25].

A consequence of P_s is the hysteretic behavior of ferroelectric materials. Application of an electric field reorients the polarization in a ferroelectric by moving the Zr/Ti ion along the polar axis. This is demonstrated in Figure 2-2 which shows a typical hysteresis

loop. The hysteresis loop shows the polarization as a function of applied electric field. The dotted line in the figure corresponds to the case where the ferroelectric material is a single domain structure whereas the solid line represents the polydomain case.

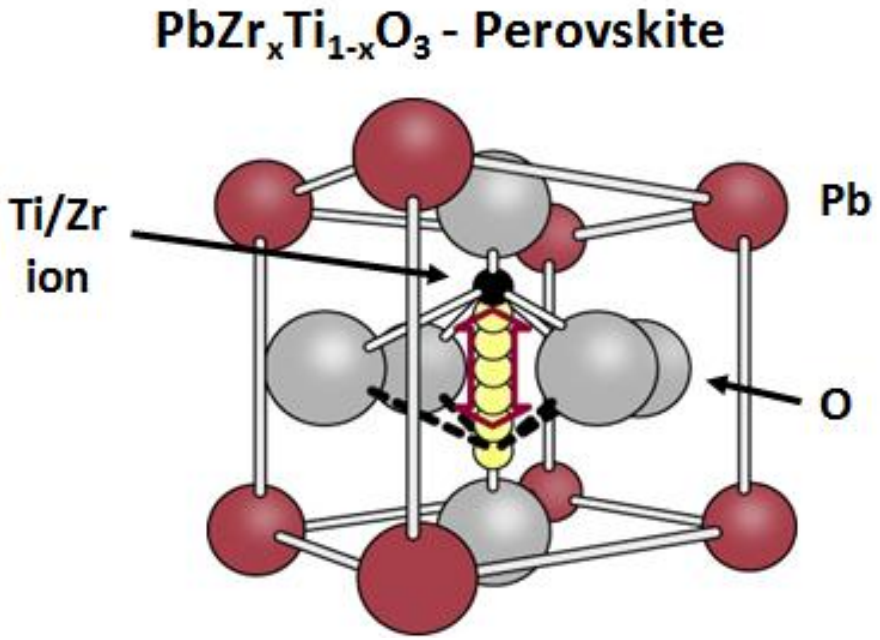

Figure 2-1. PZT perovskite structure showing asymmetry along the c-axis and spontaneous polarization. [Reprinted with permission from Texas Instruments, Inc.]

In the case of a single domain P_r and P_s are both the same value. Also, there is an abrupt switch between P_s+ and P_s- states as opposed to the polydomain case. This is due to a combination of the dielectric ionic and electronic polarization and the spontaneous polarization [25]. Initially, in a polydomain structure, there is a statistical distribution of many domains. As the polydomain material is poled, not all of the domains are polarized in the same direction due to space charges, elastic stress, and other defects in the crystal. These effects become more significant as the thin-film thickness is decreased.

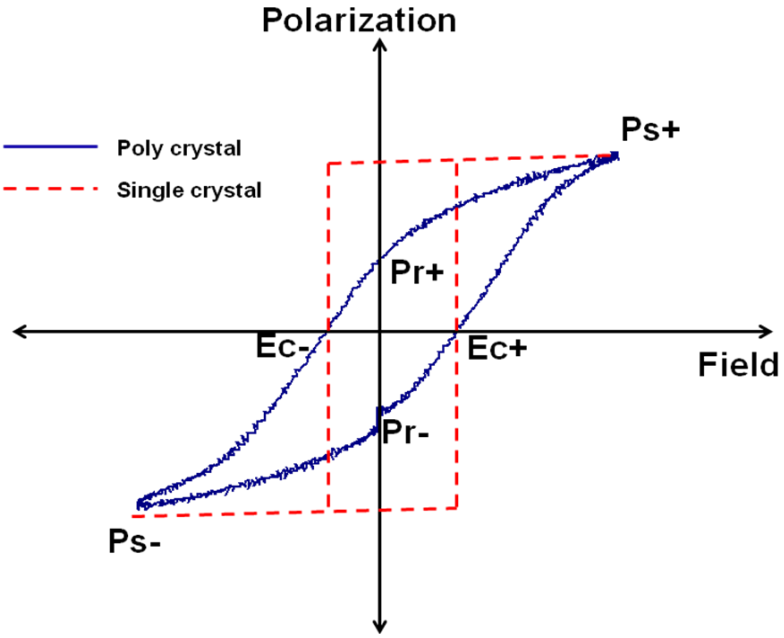

Figure 2-2. Hysteresis loop characteristics for single- and poly-domain ferroelectric films. From the hysteresis loop, it is possible to extract the remanent polarization, the coercive field, and the saturation polarization.

The hysteresis loop in a ferroelectric material originates from irreversible polarization processes. There are two mechanisms for these irreversible processes. The first is due to lattice defects which prevent a domain wall from returning to its initial state after the electric field is removed (known as pinning) [26]. Defect dipoles and free charges can also interact with the domain wall and prevent it from returning to its initial state. The second is due to the growth and nucleation of domains that do not disappear after the electric field has been removed. Details on domain structure, formation, and switching properties are presented in the section 2-5: Physics of Ferroelectric Thin Films.

The switching polarization in a ferroelectric is strongly temperature dependent. As the temperature is increased and the material approaches its Curie temperature, the center Ti/Zr ion moves toward the center of the crystal and polarization is lost. The

Curie temperature, T_c, or Curie point refers to the temperature at which the film undergoes a transition from the ferroelectric to the paraelectric phase as the temperature is increased. This temperature is associated with a change in the permittivity, ε, and can be described by the following relation known as the Curie-Weiss Law [25]

$$\varepsilon = \frac{C}{T - \Theta} \tag{2-2}$$

where C is the Curie constant, T is the temperature and Θ is the Curie-Weiss temperature. In the case of a continuous transition, T_c is equal to Θ, however the transition is often discontinuous.

The recent interest in ferroelectric thin films is due to their potential application in electronic and nanoscale devices. While bulk ferroelectric materials have been conventionally considered as dielectrics, the physics of ferroelectrics are such that , as films become thinner, ferroelectric thin films may be treated as large band gap semiconductors [27].

There are about 600 ferro- and anti-ferroelectric materials [25], [28], [29]. Anti-ferroelectric materials are similar to ferroelectric materials but with adjacent dipoles oriented in opposite (antiparallel) directions. Table 2-1 shows a selection of some of the most common ferroelectric materials that have been studied along with their chemical formula and Curie temperature (T_c) [25]. The preferred materials for ferroelectric memory applications are lead zirconate titanate (PZT), barium titanate ($BaTiO_3$), and strontium bismuth tantalite ($SrBi_2Ta_2O_9$). PZT is the ferroelectric used in most commercial FRAM products. This is mainly due to its large remanent polarization and present ability to easily integrate into existing CMOS processes. For many years PZT

was thought to be incompatible with standard CMOS processes. However, the development of barrier metals and back-end process techniques has allowed successful integration [1], [4], [30]. Compared to other ferroelectric materials, PZT has a high remanent polarization, low coercive field, and a low Curie temperature that is compatible with silicon manufacturing processes. The focus of this work will be on thin-film PZT ferroelectric capacitors.

Table 2-1. List of selected ferroelectric materials.

Material	Chemical Formula	T_c (ºC)
Barium titanate	$BaTiO_3$	120
Lead titanate	$PbTiO_3$	~490
PZT	$Pb(ZrTi)O_3$	~370
Lithium niobate	$LiNbO_3$	1210
Strontium bismuth tantalite	$SrBi_2Ta_2O_9$	570
Yttrium manganate	$YMnO_3$	~640
Potassium dihydrogen phosphate	KH_2PO_4	-150
Ammonium fluoberyllate	$(NH_4)BeF_4$	-98
Rochelle salt	$KNaC_4H_4O_6{\cdot}4H_2O$	-18; 24
Triglycine sulfate	$(NH_4CH_2COOH)_3{\cdot}H_2SO_4$	49
Trisarconsine calcium chloride	$(CH_3NHCH_2COOH)_3{\cdot}CaCl_2$	-146
Sodium nitrite	$NaNO_2$	164
Lead germinate	$Pb_5Ge_3O_{11}$	180
Germanium tellurium	GeTe	400

 [Adapted from R. Waser, Ed., *Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices*, 2nd ed. Weinheim: WILEY-VCH, 2005, p. 995.]

The temperature dependence of the material properties of PZT as a function of material composition are illustrated in Figure 2-3, which shows the phase diagram for PZT [31]. Above the Curie point, the material is cubic and in the paraelectric state. Below T_c, the material becomes ferroelectric and can be in one of several phases depending on the temperature as well as the composition of Zr and Ti in the PZT film. In the tetragonal state, the film is oriented in the <001> direction along the c-axis. In the rhombohedral state, the crystal is oriented in the <111> direction. This is also known as the r-phase. The tetragonal structure is most widely used in PZT thin-film FRAM devices due to its preferred polarization and switching properties.

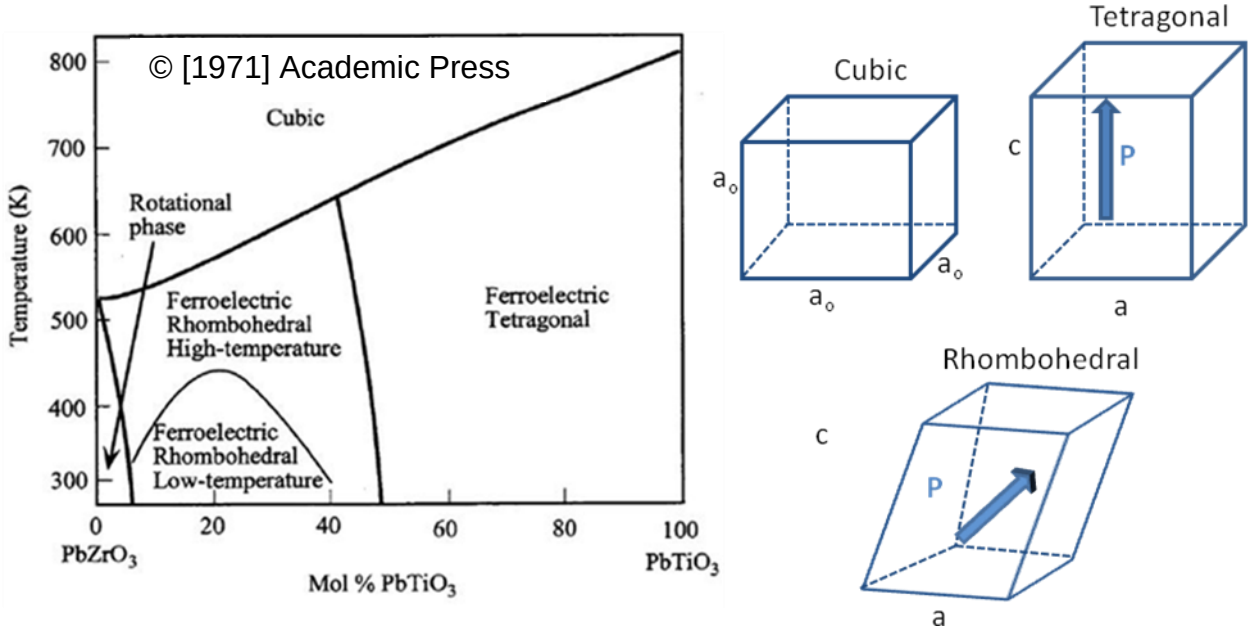

Figure 2-3. Phase diagram of PZT. [Adapted with permission from B. Jaffe, W. Cook, and H. Jaffe, *Piezoelectric Ceramics*. London: Academic Press, 1971.]

Tetragonality refers to the distortion in the crystal lattice between the *c* and *a* lattice constants, as illustrated in Figure 2-4. An increase in the c/a ratio also increases the remanent and spontaneous polarization.

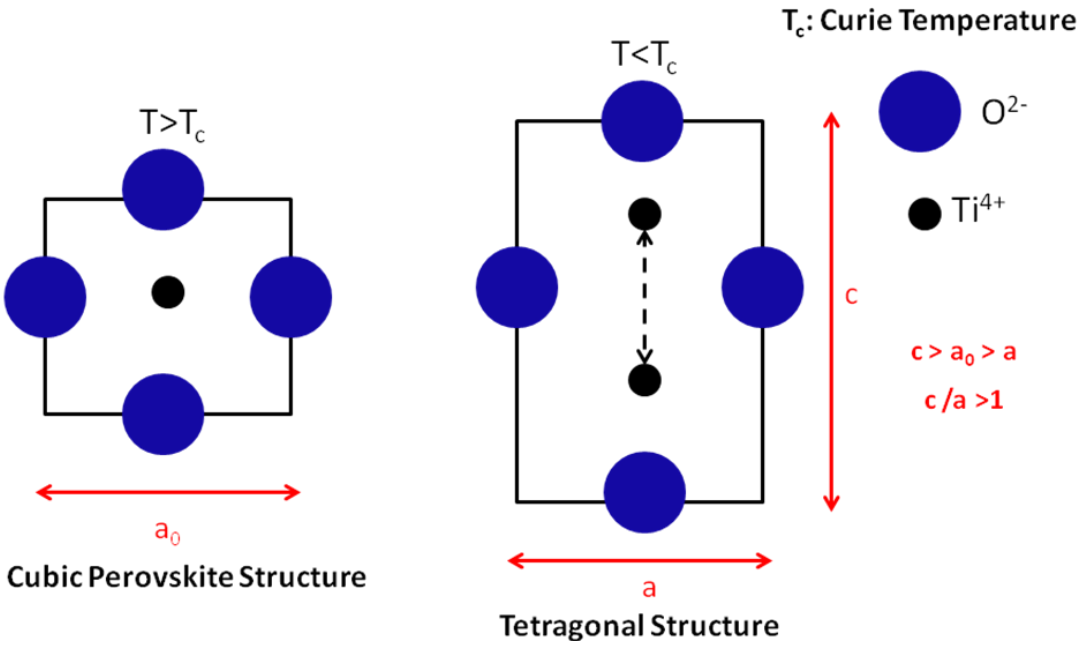

Figure 2-4. Tetragonality in the cubic and ferroelectric structure of PZT. Ratio of c/a determines the level of tetragonality.

2.2 Applications of Ferroelectric Thin Films

Ferroelectric materials can be used in a wide array of applications due to their unique properties such as a large piezoelectric effect, pyroelectric effect, and large dielectric constant [27], [32]. The piezoelectric effect is a linear change in the polarization with a small applied stress [25]. It can also refer to a linear change in the strain with an applied electric field. The pyroelectric effects is a change in polarization due change in temperature [25]. They have been used extensively in sensors, actuators, and transducers. They can also be used as the dielectric material in dynamic random access memory (DRAM). Recently, there has been intense focus and interest on ferroelectric thin films for non-volatile memory applications.

Ferroelectric thin films are desirable for non-volatile memory due to their remanent polarization (P_r) properties. As discussed previously, non-cubic forms of PZT posses an ability to retain a polarization when no voltage is applied to the film. In addition, they

can be polarized in two different states which can correspond to the logic “0” and “1” states in a memory device. In FRAM, a ferroelectric capacitor is used as the storage component. A ferroelectric thin-film is sandwiched between two metal electrodes and connected to transistors as part of a memory circuit. The polarization (and thus memory state) can be switched by applying a voltage across the ferroelectric capacitor.

Aside from its potential application for high-density memory [8], [27], [32], the FeFET has also been proposed as a possible candidate to replace the standard MOSFET in a CMOS integrated circuit (IC) [33–36]. An FeFET is similar to a MOSFET except that the gate oxide layer is replaced by a ferroelectric material. This is due to its potential to achieve a subthreshold slope lower than that of the silicon MOSFET, which has a theoretical limit of 60mV/decade. It is important to note that the potential application for ferroelectric thin films extends beyond memory devices. While the focus of this work is on ferroelectric thin films for FRAM applications, the understanding of the underlying physics gained can also contribute to the future development of ferroelectric thin films for micro- and nanoscale devices, sensors, and actu.

2.3 Ferroelectric Memories

The application of ferroelectric materials for memory was first suggested in the 1950’s. Dudley Allen Buck first proposed the concept of a ferroelectric memory in his 1952 master’s thesis from MIT titled “Ferroelectrics for Digital Information Storage and Switching” [37]. The idea was to capitalize on the switching characteristics of ferroelectrics for memory storage. Then in 1957 at Bell Laboratories, Ian Ross filed a patent which first mentioned the idea for a FeFET [38]. Merz [39–41] and Fatuzzo [42] experimentally investigated the switching effects in $BaTiO_3$, the most promising ferroelectric material at that time. Merz discovered that new domains are formed in a

ferroelectric material when an opposite electric field is applied. Ishibashi later presented a theoretical framework for the switching behavior of ferroelectrics in 1971 [43]. Development continued through the 1970s by several leading semiconductor companies but was soon abandoned due to the difficulty of integrating ferroelectric materials into standard silicon manufacturing processes. Research on ferroelectrics was mainly of academic interest during this time.

A resurgence in FRAM industrial research occurred in the 1980s due to developments in thin-film technology which allowed fabrication of thin films at temperatures compatible with silicon processes [44]. Demonstration of the first FRAM device integrated with CMOS was in 1987 [45]. This ferroelectric memory consisted of only 256 bits; however the cell size and minimum feature size decreased rapidly thereafter. In 1991, NASA did work on improving non-destructive read-out methods [46]. Mass production of FRAM products started in 1992 [47]. In 2002, Texas Instruments developed a 4Mb FRAM device embedded on 130-nm logic technology [1]. This was followed by demonstration of an embedded 8Mb, 130-nm technology FRAM in 2007 [4].

2.4 Physics of Ferroelectric Thin Films

2.4.1 Domain Structure and Formation

A domain is a region in the ferroelectric material in which the spontaneous polarization is uniformly oriented in the same direction. For a PZT tetragonal film, the Ti ion is displaced into one of the six possible crystallographic directions. Thus, for this structure there are six possible domain types as illustrated in Figure 2-5. The domains are referenced to the x, y, z coordinates in a cubic crystal lattice. Domains can be oriented along the positive and negative directions of the z-axis, which corresponds to

the c-axis of a tetragonal structure. In a similar fashion, they can be oriented along the positive or negative directions of the x and y axes. Orientation along the x and y axes corresponds to a-type domains in a tetragonal structure.

The boundary between two neighboring domains is referred to as a domain wall. Domain walls are described by the angle between the neighboring domains. Thus, in PZT tetragonal films there exists two types of domain walls, 180° and 90°, as illustrated in Figure 2-6.

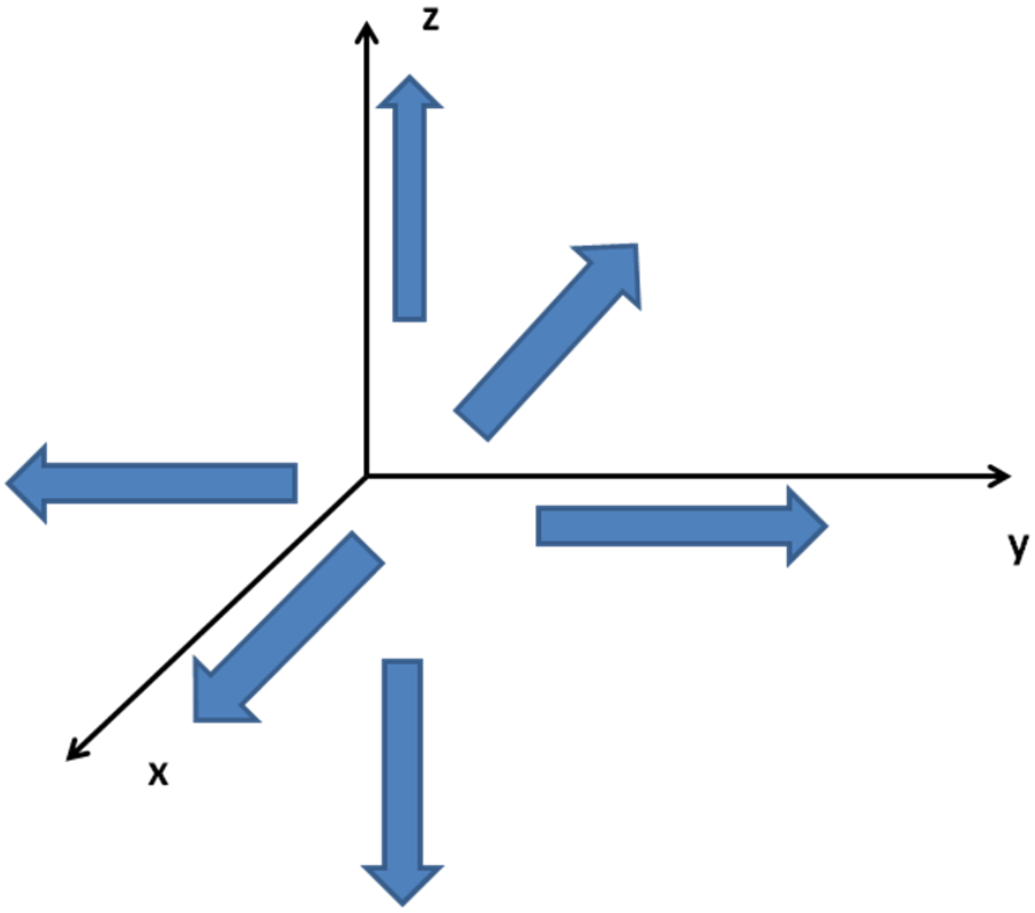

Figure 2-5. Six different types of domains in PZT tetragonal thin films. Domain orientation is referenced to the x, y, z coordinate system of a crystal lattice.

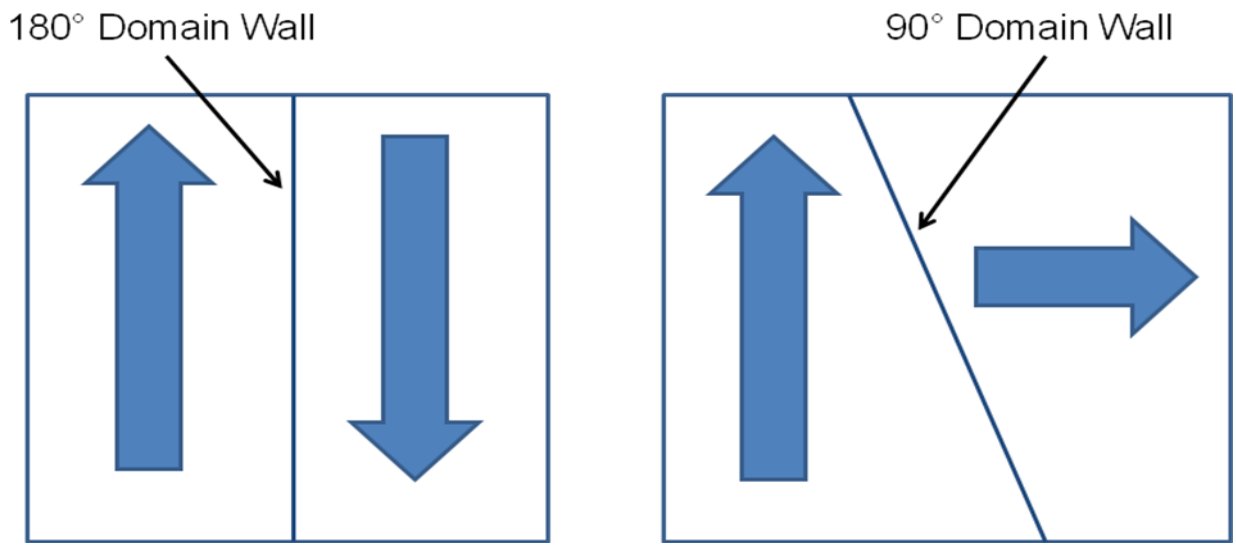

Figure 2-6. Example of 180° and 90° domain walls present in PZT tetragonal thin films.

For a fully charge-compensated ferroelectric single crystal, the ground state is a single domain state [25]. Fully charge-compensated refers to a single crystal with its associated free energy minimized. However, in most cases the film will not be fully compensated and the domain formation process will be driven by electrical and mechanical conditions. For example, the polarization in an uncompensated material will lead to a depolarizing electric field [48]. In order to minimize the energy associated with the depolarizing field, additional domains will be formed. A stress will affect the equilibrium domain structure and can lead to additional domain structures [25]. However, it should be noted that creation of additional domains will lead to an increase in the free energy. Therefore, in an effort to minimize this increase in the free energy, this domain creation process will continue until a balance in the energy is reached.

In ferroelectric thin films, the process of domain formation is driven by the clamped conditions of the substrate. As the thin-film is grown on the substrate, the film will be oriented in the direction that best matches the substrate. Upon cooling from high

temperature, the film will be in either a compressive or tensile state due to the lattice mismatch between the thin-film and substrate. This stress will in turn deform the crystal lattice and cause a misfit strain in the thin-film.

The type and amount of strain present in the thin-film will influence both the phase-transition temperature and orientation, as shown in Figure 2-7 for single-domain epitaxial lead titanate after Pertsev *et al.* [49]. Pertsev *et al.* developed a phenomenological theory for both $BaTiO_3$ and $PbTiO_3$ [49]. They concluded that the transition from paraelectric to ferroelectric phase is of second order and that there exists three different ferroelectric phases at equilibrium for $PbTiO_3$ as a function of misfit strain: c-phase, r-phase, and aa-phase. In the c-phase, the polarization is oriented along the (001) direction (or along the c-axis) of the tetragonal structure. In the r-phase, the polarization is in the (110) direction, and in the aa-phase polarization is along the (111) direction. As can be seen in the figure, a negative or compressive strain will favor the formation of a c-type domain. This behavior is also similar for poly-crystalline PZT thin films [25].

Most real ferroelectric thin films have a polydomain structure. Figure 2-8 shows possible domain structures of a PZT thin-film in the poled and unpoled state after Waser [25]. 180° and 90° domain walls are clearly visible in the (001) and (100) oriented cases. For materials with (111) orientation (r-phase), poling of the film will lead to a single r-phase domain state according to [25]. A compressive stress in the (001) oriented PZT thin film will lead to PZT oriented in predominantly in the (001) direction (c-phase). Upon electrically poling in the (001) direction, the number of 180° domain walls reduces and gradually disappear with enough electric field. However, 90° domains are

still present after poling the device. A tensile stress in the film will lead to a (100) oriented PZT thin-film (aa-phase). Poling the device has a similar effect to the (001) case, but the a-type domains are still preferred.

2.4.2 Switching Properties

The switching properties of ferroelectric materials were first studied by Walter Merz [39–41] in the 1950's. Merz experimentally observed the switching behavior of $BaTiO_3$, the most popular ferroelectric material during that period. He concluded that many new domains are formed in this material in response to an opposite electric field instead of continued growth of the already present domains [41].

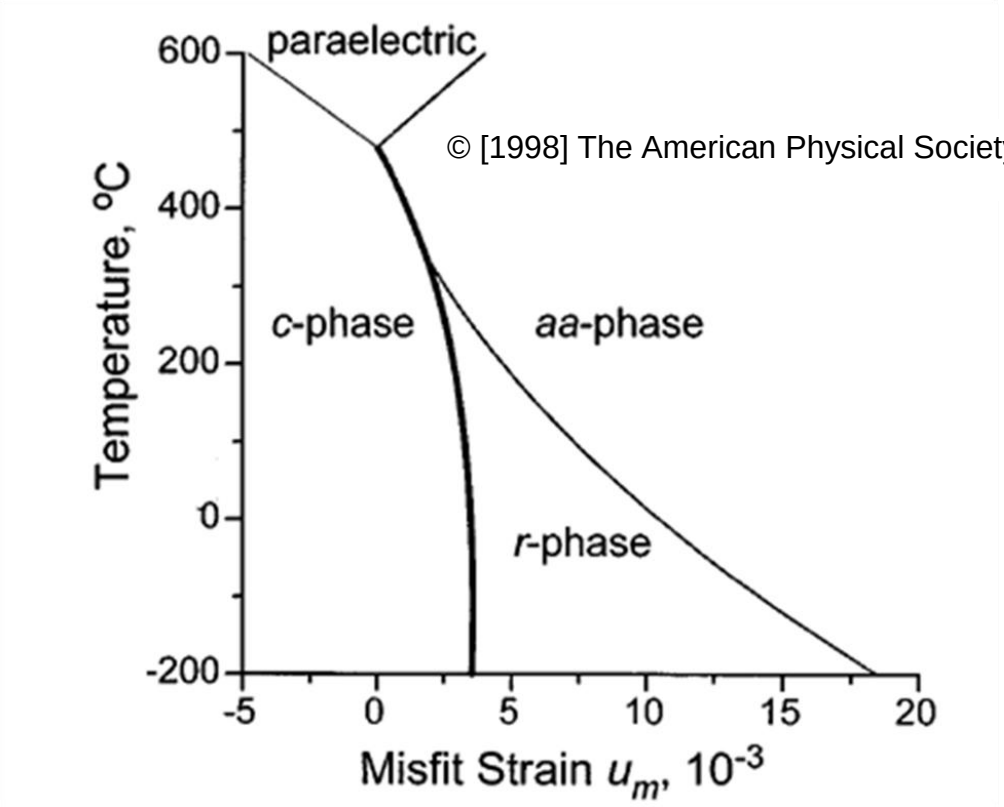

Figure 2-7. Phase diagram of single domain lead titanate. [Reprinted with permission from N. A. Pertsev, A. G. Zembilgotov, and A. K. Tagantsev, "Effect of mechanical boundary conditions on phase diagrams of epitaxial ferroelectric thin films," *Phys. Rev. Lett.*, vol. 80, no. 9, pp. 1988-1991, Mar. 1998.]

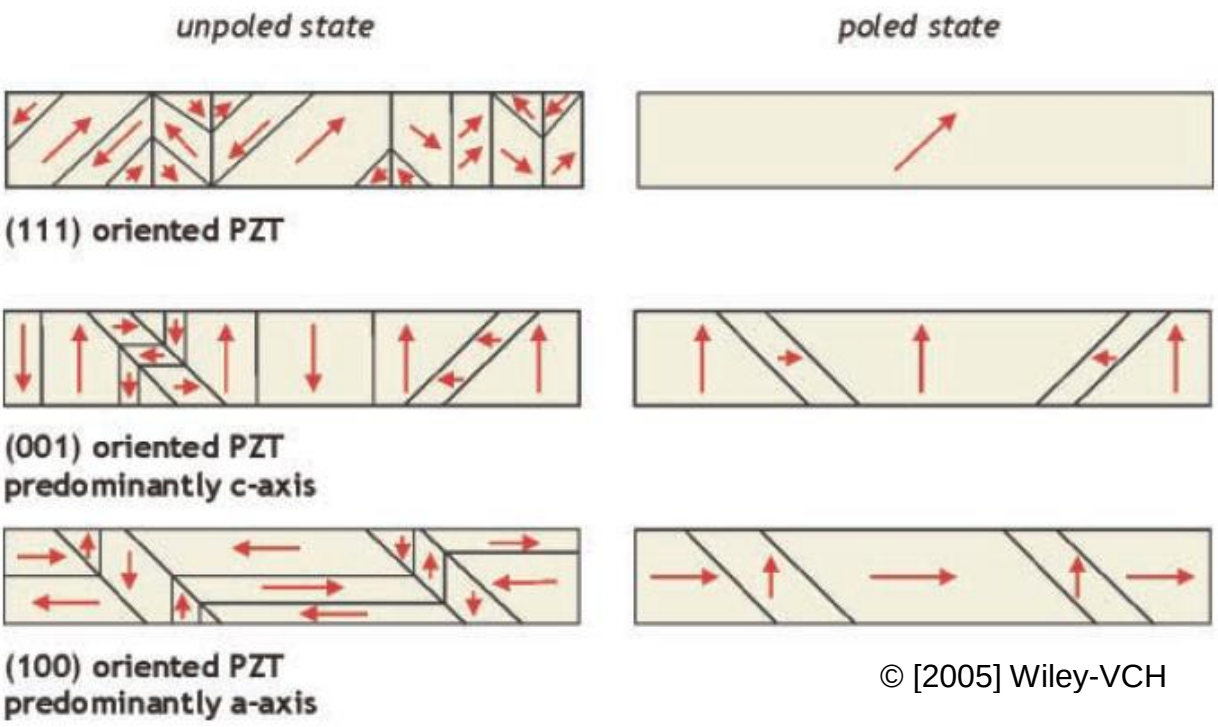

Figure 2-8. Domain structure of tetragonal PZT with different orientations for unpoled and poled states. [Reprinted with permission from R. Waser, Ed., *Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices*, 2nd ed. Weinheim: WILEY-VCH, 2005, p. 995.]

Merz proposed that ferroelectric domains switch in two stages: (1) nucleation of new domains when the electric field is switched and (2) forward growth of these new domains, known as domain wall motion [41]. The resulting maximum displacement current, i_{max}, and switching time, t_s, are described as [41], [42]

$$i_{\max} = i_o \exp(-\alpha / E) \tag{2-3}$$

$$t_s = t_o \exp(-\alpha / E) \tag{2-4}$$

where i_o and t_o are constants, α is the activation field (also a constant), and E is the applied electric field. The above equations are only valid when there is a constant electric field.

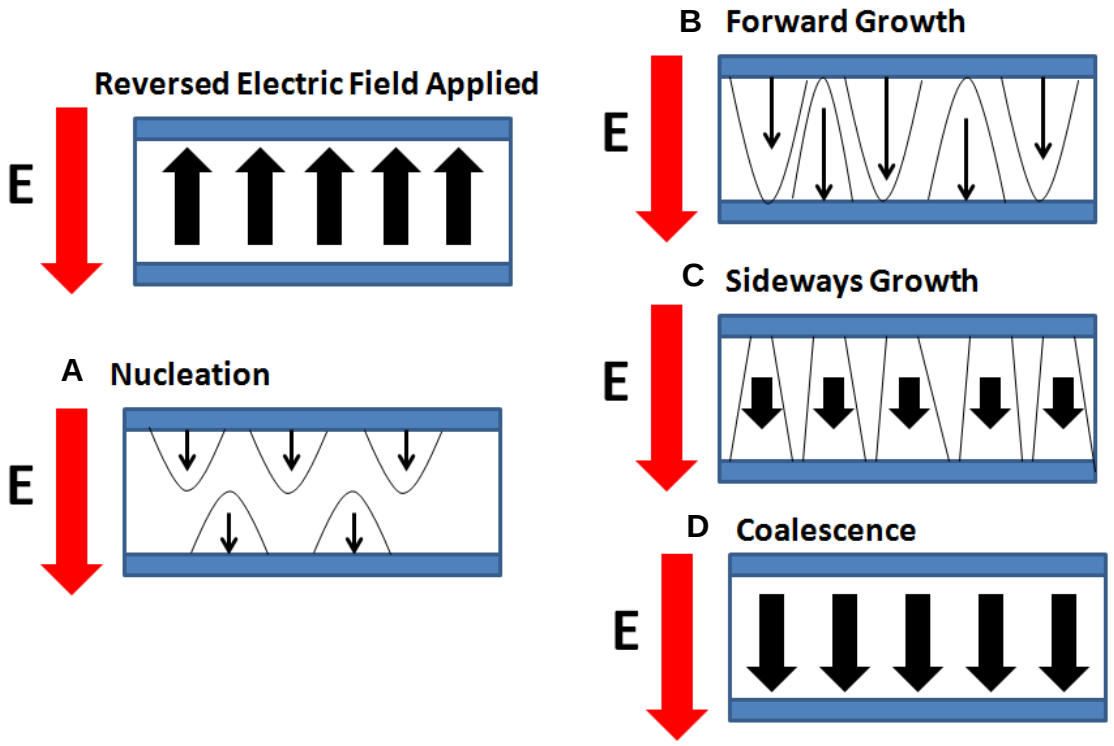

Figure 2-9. The four phases of ferroelectric thin-film domain switching: A) nucleation, B) forward growth, C) sideways growth, and D) coalescence. [Adapted with permission from M. Dawber and J. F. Scott, "Physics of thin-film ferroelectric oxides," *Rev. Mod. Phys.*, vol. 77, no. 4, pp. 1083-1130, Oct. 2005.]

Ennio Fatuzzo later suggested that ferroelectric domain switching actually occurs in four stages [42]. In addition to the mechanisms proposed by Merz, there was also a sideways growth of the domains and a final coalescence stage [42]. Figure 2-9 illustrates how switching progresses in a ferroelectric thin-film [27]. Initially, a reversed electric field is applied to the film. Switching then progresses as follows: (A) There is then a nucleation of opposite domains at the electrodes. (B) The nucleated domains grow forward until reaching the opposite electrode. (C) After forward growth, there is sideways growth of the domains, or domain wall motion. (D) The domain reversal process is complete after the domains have coalesced. Sideways domain growth is

usually slower than the first two stages in perovskite oxides. Depending on the material, (A), (B), or (C) can be the limiting parameter.

The switching time depends on many factors such as domain structure, domain nucleation, and domain wall motion [50]. Ishibashi developed a theoretical model based on the probability of nucleation and growth that describes the switching in ferroelectric materials [43], [51–54]. The model is based on Kolmogorov-Avrami [55–57] growth kinetics and has become the standard model in recent years to describe switching processes in ferroelectric materials. It is commonly referred to as the Kolmogorov-Avrami-Ishibashi (KAI) model or the Ishibashi-Orihara. According to the model, the volume fraction of domains is expressed as [52]

$$q(t) = 1 - \exp\left[-\int_0^t C(t,t')n(t')dt' \right] , \quad (2\text{-}5)$$

where C(t,t') is the volume of domains at time t, grown at time t' and n(t') is the number of nuclei per unit volume nucleated at t'.

Two assumptions are made in the Ishibashi-Orihara model: (1) the domain wall velocity is a function of the electric field and not the domain radius, and (2) nucleation is deterministic (inhomogenous). Implementing these two assumptions, the volume of domains and number of nuclei per unit volume can be represented as [52]

$$C(t,t') = C_d\left[\int_{t'}^{t} v(t'')dt'' \right]^d , \quad (2\text{-}6)$$

and

$$n(t)dt = n_E(E)dE , \quad (2\text{-}7)$$

where C_d is a constant, d is the growth dimensionality, v is domain velocity, and E is the applied electric field.

Substituting Eqs. 2-6 into Eq. 2-7 yields [52]

$$q(E) = 1 - \exp\left[-\int_0^E C_d \left(\int_{E'}^{E} v(E'') \left. \frac{dt}{dE} \right|_{E=E''} dE'' \right)^d n_E(E') dE' \right] \quad .(2\text{-}8)$$

The fraction of switched charge as a function of electric field, E, and frequency, f, can then be expressed as [52]

$$q(E) = 1 - \exp\left[- f^{-d} \phi(E) \right] \quad (2\text{-}9)$$

where φ(E) depends on the waveform of the applied field. While this model has been used to fit data well to PZT thin films [27], Lohse *et al.*, observed that it deviates over larger frequency ranges and does not adequately describe switching behavior in polycrystalline thin films [32], [58].

An alternative model was developed by Tagantsev *et al.* [59], which is nucleation-limited rather than domain wall-limited and is referred to as the nucleation limited model, or NLS. In this model, the ferroelectric thin-film is treated as a collection of many independent microscopic regions each having its own polarization switching process. As a result, the nucleation of new domains will be the limiting parameter. This model is also voltage dependent in contrast to the KAI model. At low voltages, the switching process is very slow and increases as the voltage increases. Experimental data matched the NLS model very well as can be seen in Figure 2-10 after [32]. The data from 150nm IrO_x/PZT/Pt ferroelectric capacitors over several voltages was fit to the NLS model. The NLS model is valid over a wide range of applied voltages and switching times [59]. It should be noted, however, that the model fails for thin films at low

temperatures (below -50°C). In this temperature regime, the thin-film shows single-crystal behavior and can be modeled by KAI switching kinetics [60].

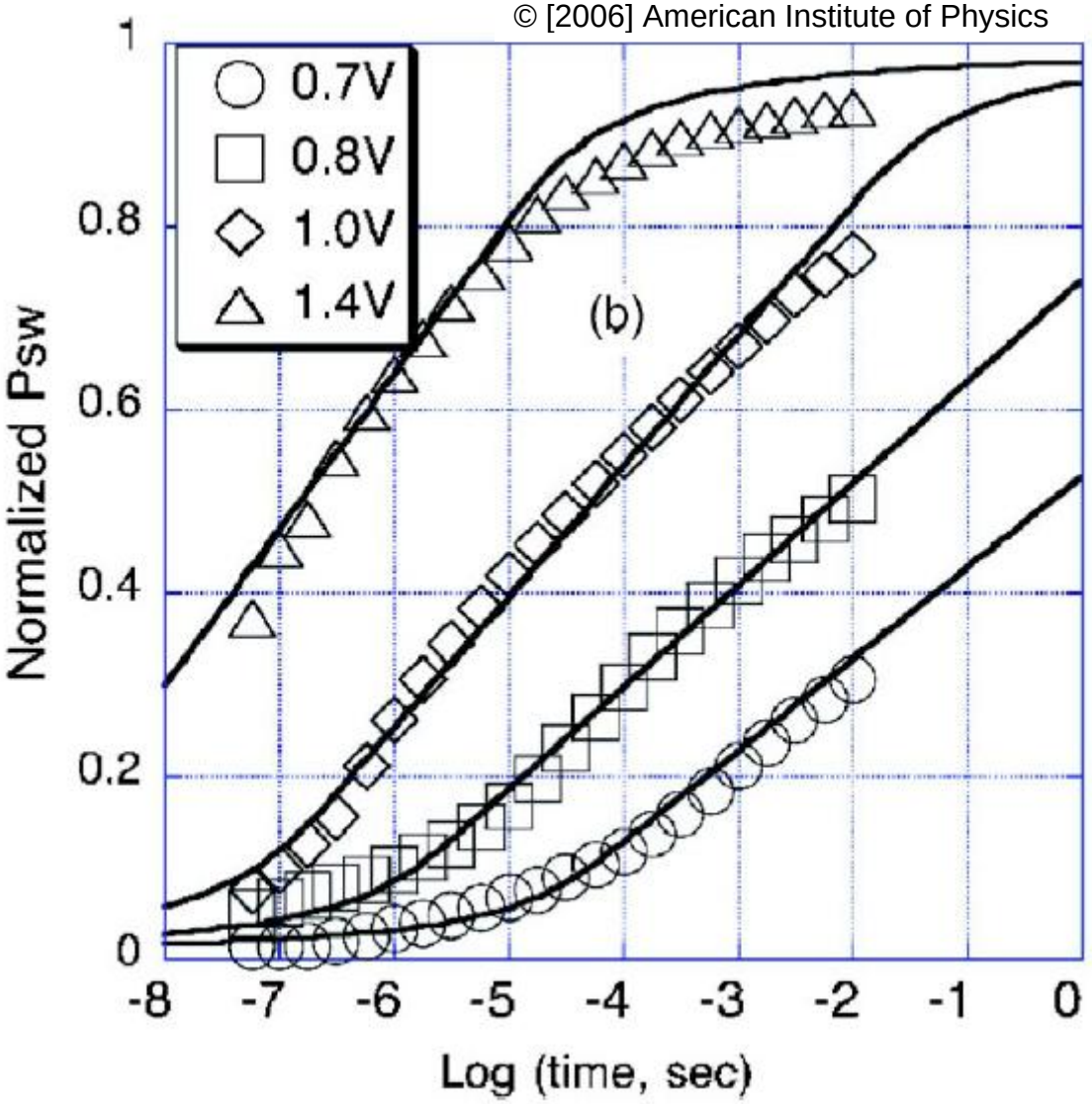

Figure 2-10. Experimental fitting of data to NLS model at different voltages and switching times for 150nm ferroelectric capacitors with IrO_x/PZT/Pt stack. [Reprinted with permission from N. Setter *et al*., "Ferroelectric thin films: Review of materials, properties, and applications," *J. of App. Phys.*, vol. 100, no. 5, p. 051606, Sept. 2006.]

2.4.3 Size Effects

As the thickness of ferroelectric thin films decreases, they begin to lose their polarization. This is due to the depolarization fields at the electrode-film interfaces.

Spontaneous polarization will induce a depolarization field at the electrode-film interface in order to compensate the charges present [61]. This depolarizing field can be expressed as [61]

$$E_{Depolarization} = \frac{P}{\varepsilon_o \varepsilon_{Ferro}} \tag{2-10}$$

where P is the polarization, ε_o is the permittivity of free space and ε_{Ferro} is the permittivity of the ferroelectric film. As the thickness of the ferroelectric film decreases, these depolarizing fields can penetrate deeper into the film and remove the spontaneous polarization. At a certain thickness, the thin-film will lose its ferroelectric properties. The minimum thickness limit for ferroelectricity in a ferroelectric thin-film capacitor is estimated to be about 4nm [62], [63].

The effects of lateral scaling were found to be minimal for the switching polarization [64]. Prasertchoung tested ferroelectric capacitors with sizes ranging from 40000μm^2 to 0.19 μm^2 and observed that the switching polarization remained constant at approximately 30μC/cm^2 [64]. The theoretical minimum volume for ferroelectricity was estimated to be approximately 1000nm^3 as calculated by Li *et al* [64], [65].

2.5 Stress Effects in Ferroelectric Thin Films

The effects of stress on the polarization properties in PZT ferroelectric thin films have been studied extensively [13–23], [66]. Tuttle *et al.*, first investigated the effect of stress and orientation in ferroelectric thin films deposited on different structures [13]. They fabricated thin films with PZT compositions of 60/40, 40/60, and 20/80 Ti/Zr ratios [13]. They postulated that the type of stress present in the film as it is cooled through its Curie point determines the polarization. A compressive stress on a highly (001)

oriented film was found to enhance the polarization while a tensile stress reduced it. Their results were later confirmed by various groups [14], [15], [17–23].

Spierings *et al.* investigated the effects of stress induced by annealing treatments during processing [13]. Annealing of the top electrode had a significant effect on the polarization properties of the ferroelectric thin-film. The film is under a tensile stress after depositing on the bottom electrode and annealing. It is reported that since the film is in a tensile state, as it cools down through the Curie point most of the domains will be oriented parallel to the plane of the film as this is the lowest energy state. Upon deposition and annealing of the top electrode, the thin-film is in a compressive stress state and the switching polarization is enhanced as a result. The minimum energy state is changed as a result of the film being under compression as it is cooled through the Curie point and the domains become perpendicular to the plane of the film. Kobayashi *et al.* also observed that the ferroelectric properties are degraded due to the tensile stress present in the film when it is annealed [17]. In their case, the tensile stress was induced by thermal strain of the Al/TiN/Ti interconnect layer since its coefficient of thermal expansion is much larger than that of PZT. Both of these results are very similar to what was reported by Tuttle *et al.* in [13].

Shepard *et al.* [15] and Kelman *et al.* [19] investigated the effects of biaxial stress on polarization by applying an external mechanical stress. In [15], a compressive biaxial stress enhanced the polarization while a tensile biaxial stress degraded the polarization. There were no significant changes in the coercive voltage. A model for these results was not reported in this work. Kelman *et al.* applied external biaxial tensile stress using a bending rig consisting of two concentric knife edge rings with different

radii [19]. They reported a decrease in P_r and P_s of ~13%. This result is attributed to 90° domain wall motion that accommodates the strain induced in the film. Details of this model will be explained later in this section.

Application of an external uniaxial stress via four-point bending was reported in [18], [22]. The results are consistent with what has been previously reported: uniaxial tensile stress degraded the ferroelectric properties while a uniaxial compressive stress enhanced the ferroelectric properties. Kumazawa *et al.* also tested the cycling endurance as a function of stress [18]. They observed that a tensile stress reduced cycling endurance while a compressive stress delayed the degradation due to voltage cycling when compared to a device with no stress applied. Zhu *et al.* reported the change in polarization as a function of uniaxial tensile stress [22]. They compared their results to ferroelectric bulk ceramics and found that the rate of polarization decrease is 30x less in thin films. They also estimated the critical stress in their ferroelectric thin films to be about 2.3GPa and attribute these results to the thin-film being clamped to the substrate [22].

Permanently enhancing ferroelectric properties using compressive stress has been previously proposed [20], [21]. Lee *et al.* deposited a polycrystalline PZT film on a bent substrate [20]. The substrate was bent using a specially designed substrate holder. After deposition, the film was annealed and immediately removed from the holder and allowed to cool. A remanent polarization enhancement of 35% was reported using this process. Rodel *et al.* suggested permanently enhancing the polarization by poling the ferroelectric using stress and electric bias [21]. A DC bias was applied to a PZT ferroelectric while the sample was under a compressive stress. They observed

that when the ferroelectric is under a mechanical load, the electric bias required to pole the material is reduced [21]. The combined mechanical stress and electric field work needed to induce 90° switching is described as [21], [67]

$$W_M + W_E \geq 2P^0 E_0 \left[\frac{J}{cm^3}\right], \tag{2-11}$$

where W_M and W_E are the work done by a mechanical load and the work done by an electric field, respectively. $2P_0$ is the change of spontaneous polarization during switching and E_0 is the critical field needed for switching.

As the thickness in ferroelectric films becomes smaller, the effects of stress are more pronounced. A compressive stress applied to a ferroelectric thin-film will induce 90° switching of the domains. As was presented by Pertsev *et al.* [49] for a single domain structure and later by Koukhar *et al.* [68] for polydomain films, a highly compressed structure below the Curie point will lead to a ferroelectric thin-film with mostly c-type domains while a structure with a large tensile strain will lead to a film with predominately a-type domains. As can be seen in Figure 2-11 at relatively low levels of strain, there will be a combination of both c-type and a-type domains. As a compressive stress is applied to the thin-film, the volume fraction of c-type domains increases. This increase in c-type domains will in turn lead to an increase in the polarization of the film. Alternatively, a tensile stress will increase the volume fraction of a-type domains and reduce the polarization along the polar axis. This model is consistent with the results reported above.

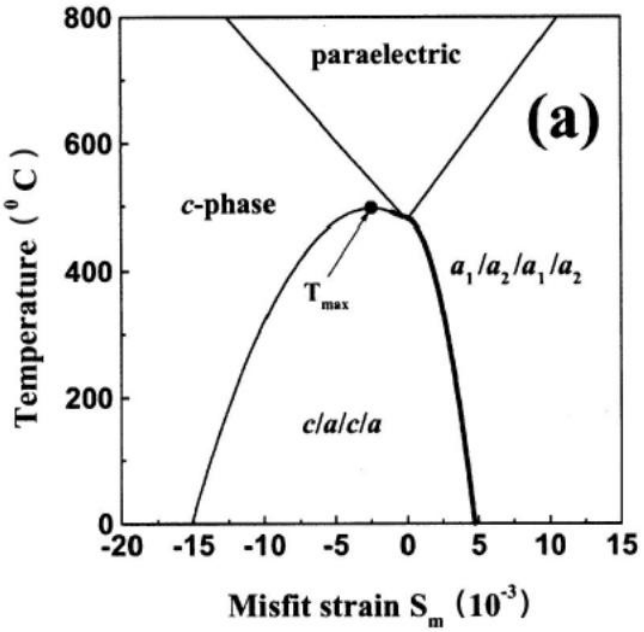

Figure 2-11. Phase diagram for polydomain $PbTiO_3$ as calculated. [Adapted with permission from V. Koukhar, N. Pertsev, and R. Waser, "Thermodynamic theory of epitaxial ferroelectric thin films with dense domain structures," *Phys. Rev. B*, vol. 64, no. 21, pp. 1-15, Nov. 2001.]

The model presented by Kelman *et al.*, suggests that 90° domain wall motion occurs in response to a biaxial tensile stress rather than an elastic distortion of the crystal lattice [19]. This model relies on calculating the number of a-type and c-type domains in the film. In an unstrained sample, the total size can be calculated as [19]

$$L^0 = A_C^0 a_0 + A_a^0 c_0^* \tag{2-12}$$

where A^0_C and A^0_a are the surface area fractions of c-type and a-type domains, respectively, a_0 is the effective lattice parameter of a-type domains, and c^*_0 is the effective lattice parameter of c-type domains. Assuming that all of the imposed strain in the film is accommodated, then the relative change in the area fraction of each type of domain can be calculated as [19]

$$(1+\varepsilon)L^0 = A_C^{'} a_0 + A_a^{'} c_0^* \tag{2-13}$$

where A'_c and A'_a are the area fractions of c-type and a-type domains in the strained sample, respectively, and ε is the strain in the film. Having calculated the new fraction of a-type and c-type domains in the strained sample, the change in remanent polarization can then be calculated as follows [19]

$$\frac{P - P_0}{P_0} = \frac{A_c^{'} - A_c^0}{A_c^0} \quad . \tag{2-13}$$

Since it was assumed that the domain structure was the same throughout the thickness of the film, the area fractions of the domains are the same as the volume fractions of a-type and c-type domains and can be calculated by integrating the intensity of two peaks observed from x-ray diffraction (XRD) scans [19].

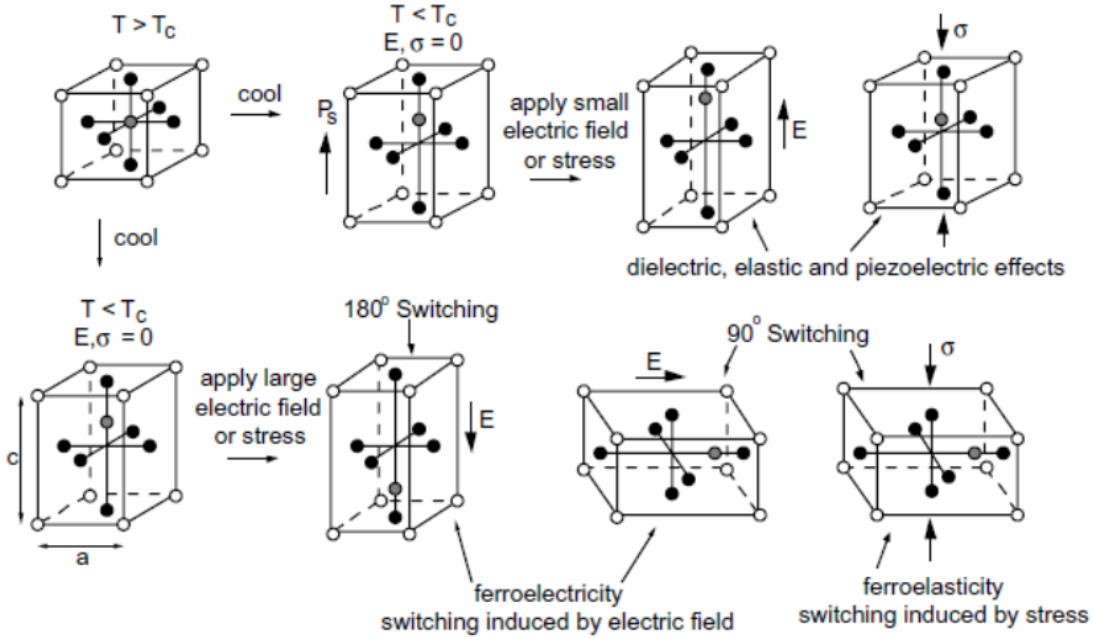

Figure 2-12. Effects of stress and electric field on a PZT tetragonal crystal cell. An electric field can cause 180° and 90° switching while a stress will only induce 90° switching. [Reprinted with permission from C. M. Landis, "Non-linear constitutive modeling of ferroelectrics," *Current Opinion in Solid State and Materials Science*, vol. 8, no. 1, pp. 59-69, 2004.]

Figure 2-12, after Landis *et al.* [69], summarizes the effects of stress and electric field in a ferroelectric crystal lattice cell. The structure is initially in its cubic structure above the Curie point and no ferroelectricity exists. As the sample is cooled below the Curie point, it goes from the paraelectric to the ferroelectric state, and a spontaneous polarization occurs due to asymmetry in the lattice. The response to a small electric field or stress will move the Zr/Ti along the polar axis, increasing or decreasing the asymmetry in crystal. This will in turn increase or decrease the polarization. However, if the amount of electric field or stress is small, does not move the Zr/Ti ion into one of the other allowed crystallographic directions. In response to a large enough electric field, the Zr/Ti ion will switch either 180° or 90° into one of the other allowed crystallographic directions depending on the direction of the applied electric field. An electric field parallel and in the opposite direction to the polar axis will cause 180° switching, while an electric field in the direction perpendicular to the polar axis will cause 90° switching. In response to an applied stress, only 90° switching will occur in the lattice. A free energy model will be used to describe these stress effects.

2.6 FRAM Structure and Operation

Ferroelectric Random Access Memory (FRAM) is a non-volatile memory that has gained attention in recent years due to its low power, fast read and write times, and high cycling endurance. Table 2-1 compares FRAM to the mainstream nonvolatile memories EEPROM and Flash after [70]. According to the table, while its Read access-time is on the same scale as EEPROM and Flash, the write access-time for FRAM is considerably faster at 100ns. The energy consumed per 32b write is also significantly less for FRAM at 1nJ. When compared to Flash and EEPROM, the limitation for FRAM seems to be its ability to scale to smaller dimensions.

Table 2-2. Comparison of FRAM features to other nonvolatile memories.

Nonvolatile Memory	EEProm	Flash Memory	FeRAM
Area per cell (norm.)	2	1	5
Read access-time	50 ns	50 ns	100 ns
Write (prog.) access-time	10 µs	1 µs	100 ns
Energy per 32 b write	1 µJ	2 µJ	1 nJ
Energy per 32 b read	150 pJ	150pJ	1nJ

In FRAM technology, a ferroelectric capacitor is used to digitally store information. A negative P_r in the ferroelectric capacitor corresponds to logic "1" while a positive P_r corresponds to the logic "0" state. To switch the ferroelectric capacitor, an electric field of opposite polarization is applied. The ferroelectric capacitor is typically fabricated after the front end-of-line (FEOL) process of a conventional CMOS process technology. Ferroelectric capacitors in an FRAM cell are written and read by applying voltage pulses.

FRAM has two typical cell structures: 1T1C and 2T2C, as shown in Figure 2-13 after [70]. In a 1T1C cell, the ferroelectric capacitor is connected to one transistor. The sense amplifier will compare the state in the ferroelectric capacitor to a reference cell and determine the logic level in the cell. The 2T2C cell contains the 1T1C structure plus its complement in the same cell. The sense amplifier will simply compare the polarization across both ferroelectric capacitors and from this margin determine the logic level in the memory cell.

The 1T1C cell allows for a higher bit density since it is half the size of a 2T2C cell. However, this comes at the expense of increased fatigue in the reference cell, since all the memory cells in a 1T1C structure use the same reference cell. Therefore, the 2T2C

cell will have longer cycle endurance since each memory cell will have its own reference, but this comes at the cost of larger area. Due to its higher storage density, the 1T1C cell is the more commonly used structure.

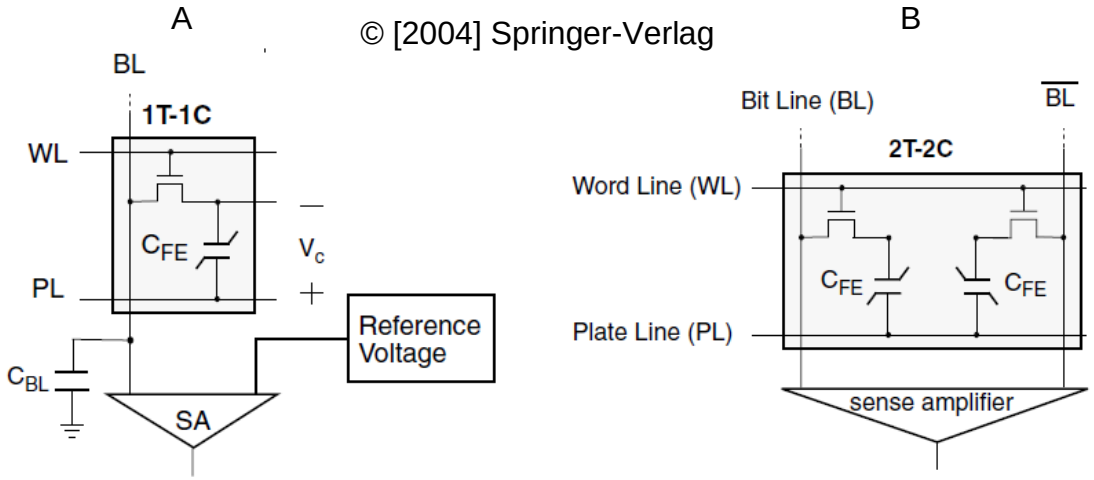

Figure 2-13. FRAM cells with A) 1T1C structure and B) 2T2C structure. [Reprinted with permission from A. Sheikholeslami, "Operation Principle and Circuit Design Issues," in *Ferroelectric Random Access Memories: Topics in Applied Physics*, vol. 164, H. Ishiwara, M. Okuyama, and Y. Arimoto, Eds. Berlin Hidelberg: Springer-Verlag, 2004, pp. 149-164.]

To write to a 1T1C cell, the bitline (BL) is either raised high to VDD (for logic "1") or it is kept low at 0V (for logic "0"). The wordline (WL) is then driven high so that either VDD or 0V volts appears across the capacitor. The plateline (PL) is then pulsed to VDD. The wordline and bitline remain high until the plateline pulse is removed. This ensures that the capacitor will be in either the positive ("0") or negative ("1") remanent polarization state.

During a read operation, WL, PL, and BL are first set low to 0V. Then the wordline is driven high followed shortly by the plateline being driven high. This will divide the plateline voltage between the ferroelectric capacitance, C_{Ferro}, and the bitline capacitance, C_{BL}. C_{Ferro} will vary depending on the state of the capacitor and as a result

so will the bitline voltage read at the sense amplifier. Comparing this bitline voltage to the reference determines the state of the memory cell. More details on the read operation can be found in [70].

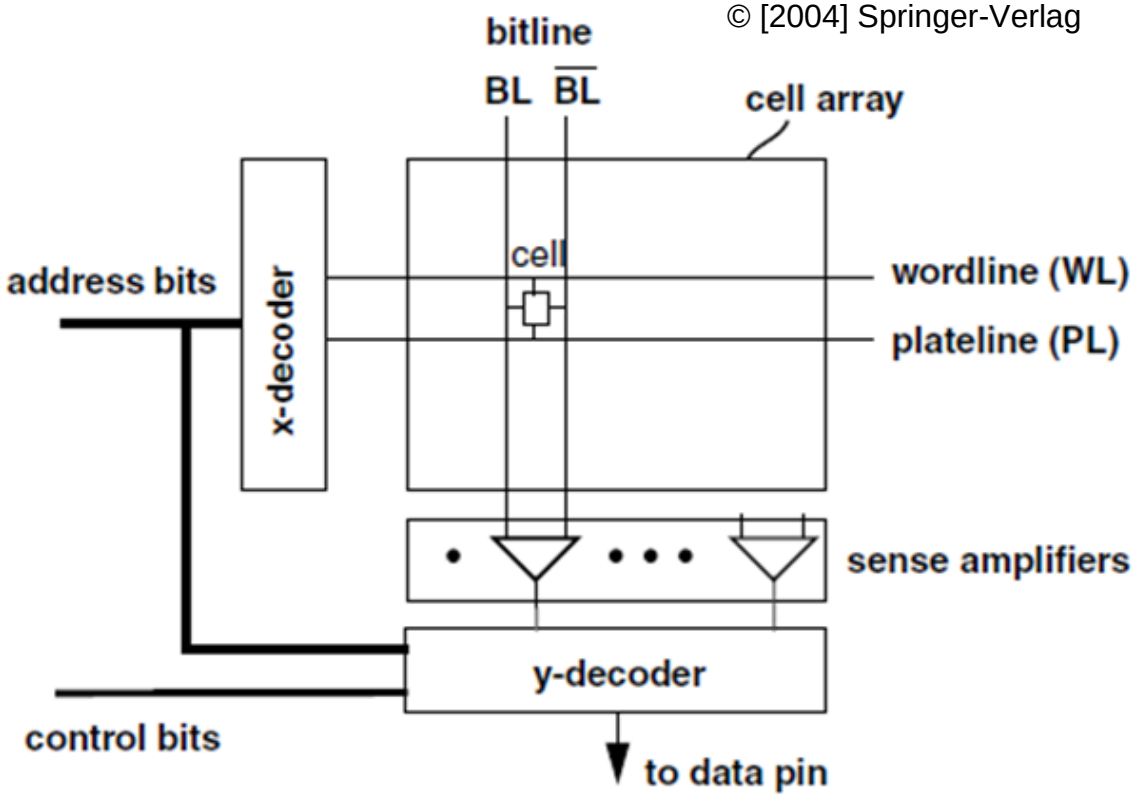

Figure 2-14. Basic FRAM circuit architecture. [Reprinted with permission from A. Sheikholeslami, "Operation Principle and Circuit Design Issues," in *Ferroelectric Random Access Memories: Topics in Applied Physics*, vol. 164, H. Ishiwara, M. Okuyama, and Y. Arimoto, Eds. Berlin Hidelberg: Springer-Verlag, 2004, pp. 149-164.]

Figure 2-14 shows a typical FRAM circuit architecture. It is very similar to other circuit architectures for SRAM, DRAM, EEPROM, and Flash, except that FRAM includes the plateline. The address bits are used to access the rows in the array via the wordline and plateline. The control bits are used to select the column in the array via the bitline. It should be noted that FRAM has a destructive read. That is, after a cell has been read, it needs to be re-written into its original state.

CHAPTER 3
EXPERIMENT SET-UP AND DEVICE CHARACTERIZATION

The experiment set-up and device characterization technique used in this work are presented in this chapter. First, a description of wafer bending is given. The advantage of wafer bending to vary stress for stress effect studies is discussed. Four-point bending, three-point bending, and the methods for calculating stress are described. Next, device characterization techniques including hysteresis measurement, the PUND test, leakage current, and cycling endurance are reviewed. Finally, the experiment set-up is described in detail.

3.1 Wafer Bending

3.1.1 Four-Point Bending

Four-point bending [71] has been previously used to study the effects of stress on Si CMOS devices [72–76]. When compared to process-induced stress the advantage of wafer bending is that the amount and type of applied stress can be systematically varied on the same wafer sample and devices. Wafer bending also allows for repeated cycling of the stress as the bending is elastic for silicon wafers. It will be used similarly in this work to study the effects of stress on integrated ferroelectric capacitors. Figure 3-1 illustrates how four-point bending is used to apply stress to the devices. The FRAM device wafer is cleaved into long, narrow strips with the desired device under test (DUT) located in the center of the top surface of the cleaved wafer sample. The sample is then placed between two pairs of point forces: two on the bottom surface of the wafer and two on the top surface of the wafer as shown in Figure 3-1. The wafer is bent as the force is applied with the top surface being under a tensile stress and the bottom surface being under a compressive stress. In the configuration shown in Figure 3-1, the

top surface is under a tensile stress. In order to apply a compressive stress to the top surface of the sample, the positions of the top and bottom point forces are reversed.

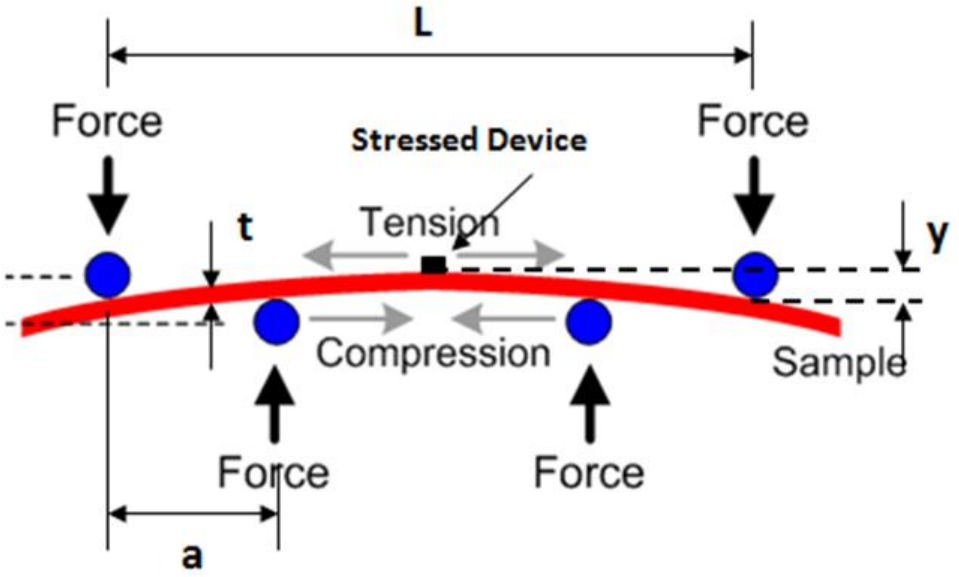

Figure 3-1. Schematic of four-point bending applied to a wafer sample. In this configuration, tensile stress is applied to the top surface and compressive stress is applied on the bottom surface.

Following analysis from Timoshenko [71], the following relation for stress is obtained

$$\sigma = \frac{Eyt}{2a\left(\frac{L}{2} - \frac{2a}{3}\right)}, \tag{3-1}$$

where E is the elastic modulus of the material being bent, y is the maximum deflection of the sample, t is the thickness of the sample, and σ represents the stress. L is the distance between the two outermost point forces, and a is the distance between the outer- and inner-most point forces. The maximum stress occurs between the two inner-most forces and is approximately constant in this region [71]. While the elastic modulus

and thickness of the sample are fixed, the amount of applied stress can be controlled and varied by adjusting *y*, *L*, and *a*.

To apply mechanical uniaxial stress, the sample is placed inside a four-point bending apparatus [73], [74], [76], as shown in Figure 3-2 . This apparatus is used to apply stress in the range of 0 to ~200MPa. 200MPa is approximately the stress at which the cleaved sample fractures using this apparatus. Mechanical stress is applied via four metal rods, which approximate the point forces. As the top plate is lowered, the rods apply a force to the sample, causing the wafer sample to bend. The amount of mechanical stress applied is controlled using two micrometers on the top plate of the stress apparatus. An opening in the top plate allows the DUT to be probed for device characterization while it is under mechanical stress.

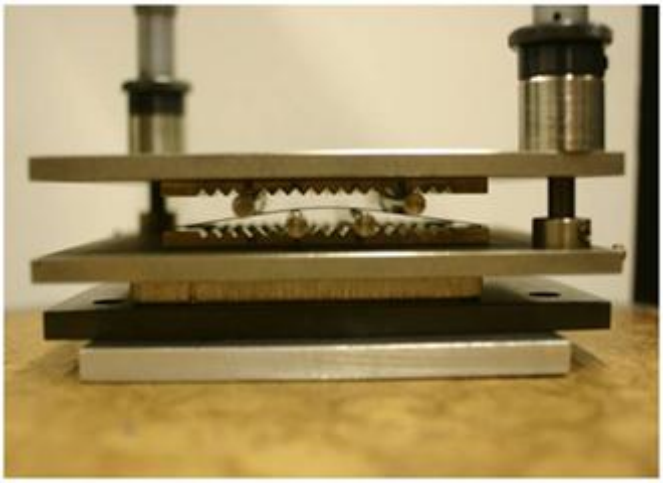

Figure 3-2. Photograph of four-point bending apparatus used for applying uniaxial stress up to 150MPa. Tensile and compressive stress can be applied to the top surface of the wafer sample, depending on the position of the metal rods.

The maximum stress with two micrometers is limited by the difficulty of achieving parallel plates. A four-point flexure-based apparatus, shown in Figure 3-3, is used to apply high stress to the devices [72], [75]. The flexures ensure parallel plates independent of applied stress. Uniaxial mechanical stresses up to 1GPa have been

applied using this apparatus [75]. In this apparatus, eight flexure beams are used to apply an upwards force to the bottom rods which then bends the sample and places the top surface of the sample under a tensile or compressive stress depending on the placement of the rods (as previously described). Previous work shows that there is a 5% error margin between the calculated stress using Eq. 3-1 and the actual measured stress using a strain gauge [75].

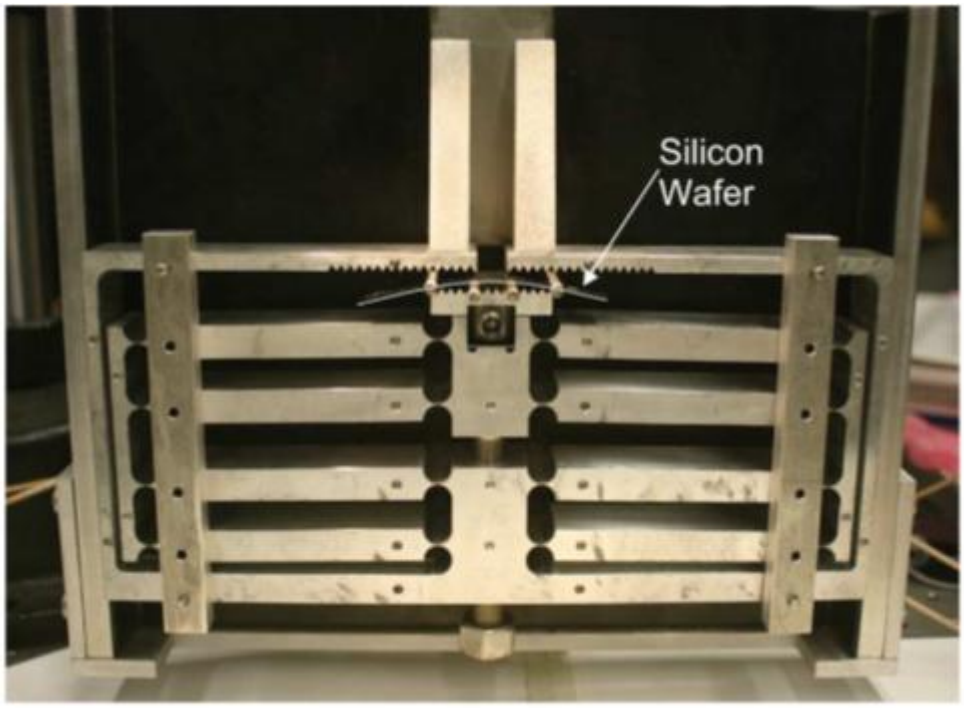

Figure 3-3. Flexure-based four-point bending apparatus used for applying high stress to the wafer sample. [Reprinted from S. Suthram, J. Ziegert, T. Nishida, and S. Thompson, “Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (~ 1.5 GPa) channel stress,” *IEEE Electron Device Lett.*, vol. 28, no. 1, pp. 58–61, Jan. 2007.]

Biaxial stress is applied by placing the sample between two concentric rings as shown schematically in Figure 3-4. In this case, the wafer sample containing the DUTs is square-shaped and must be larger than the area of the larger ring. The DUTs are in the center of the wafer sample to achieve maximum uniform stress. To apply biaxial

tensile stress to the top surface, the larger ring is placed on top of the sample, and the smaller ring is placed on the bottom. A force is then applied between the top and bottom rings. To apply compressive stress to the top surface, the positions of the rings are reversed. In the configuration in Figure 3-4, the sample will be under a compressive stress. Figure 3-5 shows the apparatus for applying biaxial stress to the FRAM devices. It works in a similar fashion to the uniaxial stress apparatus. Two micrometers on the top plate are used to lower the top plate and move it closer to the bottom plate. This causes the concentric rings to apply a biaxial stress to the sample. The stress is maximum and approximately uniform in the area on the wafer sample encompassed by the smaller ring.

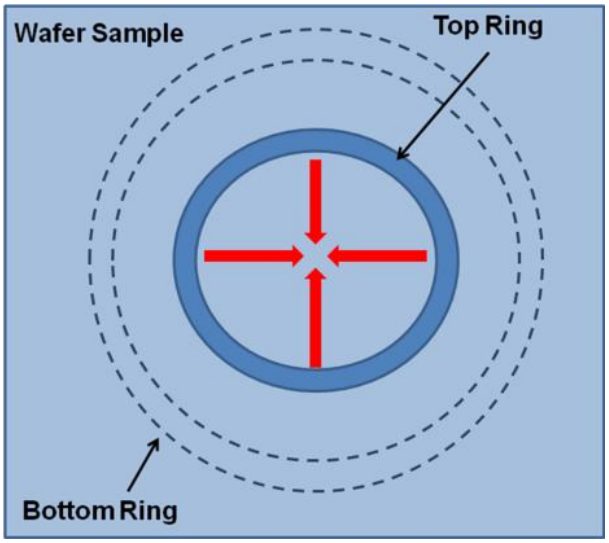

Figure 3-4. Schematic of biaxial bending a wafer sample. In this configuration the sample is under a biaxial compressive stress.

The applied stress is measured and calibrated by placing a strain gauge on the top surface of the wafer. Previous work by Chu, *et al.* has shown a good agreement between the stress calculated by Eq. 3-1 and the actual stress measured with a strain gauge [73]. The error margin was within 5%. Finite element analysis has been used to validate the stress measurements on this biaxial stress apparatus [77].

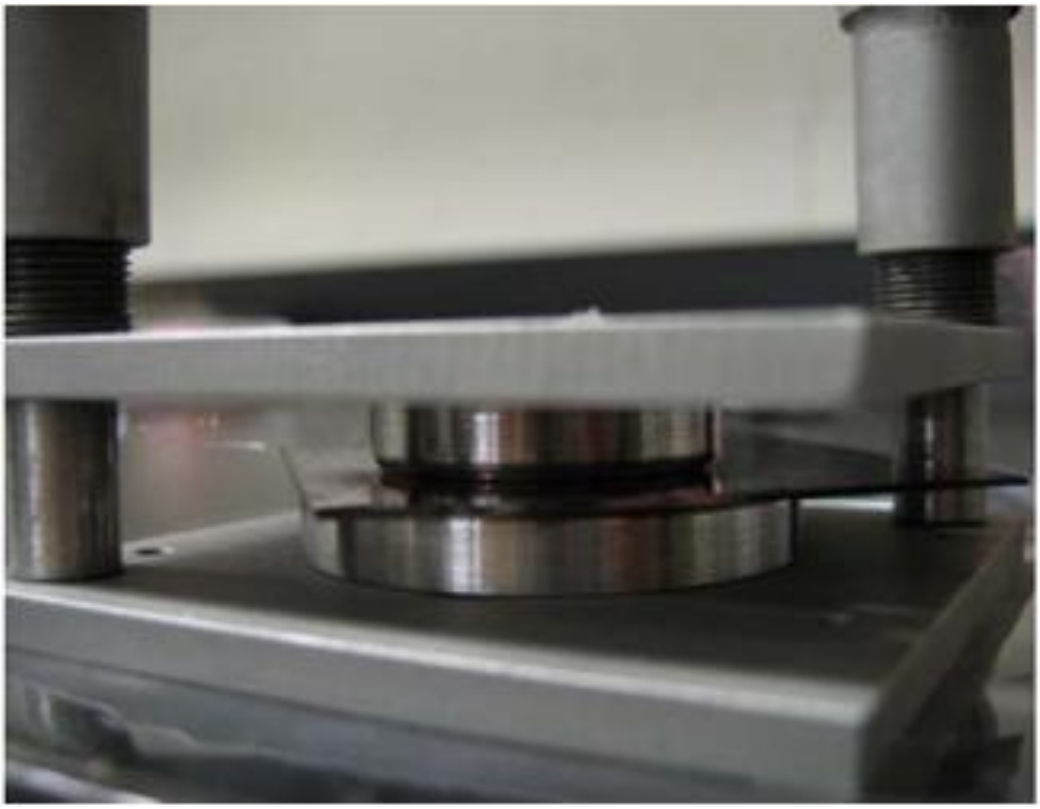

Figure 3-5. Bending apparatus used for applying biaxial stress to wafer sample. Concentric rings are used for applying either compressive or biaxial stress, depending on their position.

3.1.2 Three-Point Bending

A special quartz bending apparatus, shown in Figure 3-6, is used to apply stress to the wafer sample at elevated temperature [78–80]. This bending apparatus is based on three-point bending and was designed and fabricated to be used at high temperatures. The sample is placed in the apparatus so that each end is under the counter-force points. Then, from beneath the bottom surface of the sample, a threaded graphite screw is used to apply an upwards force on to the wafer. The wafer will be bent with a curvature gradient along the length of the sample. The top surface of the wafer will be under uniaxial tensile stress while the bottom surface will be under a uniaxial compressive stress. The area of the wafer under the screw has the highest stress and the stress gradually reduces along the length of the sample towards the counter-force

points. Therefore, the devices used in the experiments are located approximately in the center of the wafer.

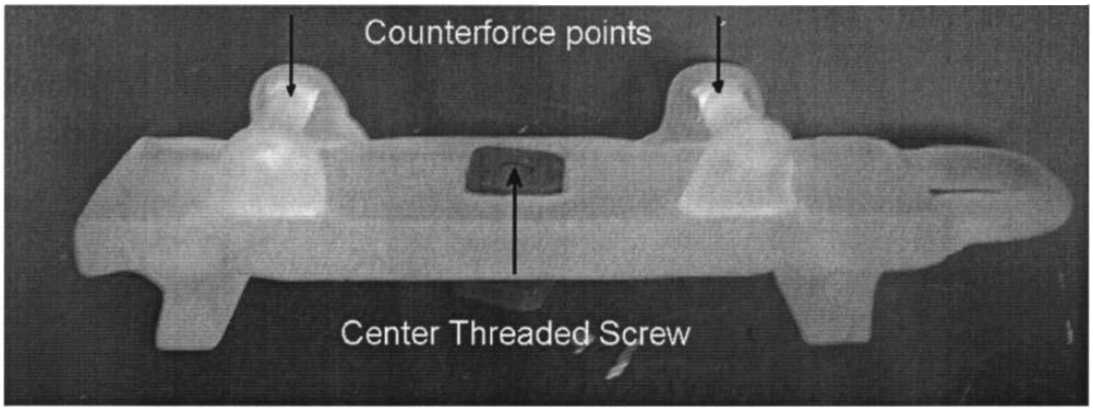

Figure 3-6. Novel three-point bending apparatus used for bending the wafer at high temperatures. [Reprinted from C. R. Olson, E. Kuryliw, B. E. Jones, and K. S. Jones, "Effect of stress on the evolution of mask-edge defects in ion-implanted silicon," *J. Vac. Sci. Technol. B: Microelectronics and Nanometer Structures*, vol. 24, no. 1, p. 446, Jan.-Feb. 2006.]

Measurement of the stress along the curved surface of the wafer is done using a Philtec laser displacement system [79], [80]. A schematic illustrating how the stress is measured is shown in Figure 3-7. A laser sensor is attached to a vertical stage. The bent sample is placed underneath this sensor on a horizontal stage. The sample is then moved back and forth horizontally so that the laser sensor can scan the entire bent surface. As the laser is scanned across the surface of the bent wafer, the displacement of the laser tip from the surface, y, is plotted as a function of the lateral displacement along the length of the wafer, x. Once the wafer surface has been mapped out and the values of y and x recorded, the radius of curvature, r, can be calculated as follows

$$\frac{1}{r} = \frac{\frac{d^2 y}{dx^2}}{\left[1 + \left(\frac{dy}{dx}\right)^2\right]^{3/2}} \tag{3-2}$$

The stress can then be calculated from the radius of curvature from the following relation [78]

$$\sigma = \frac{E \times c}{r} \tag{3-3}$$

where *E* is the elastic modulus of the material and *c* is the half thickness of the wafer.

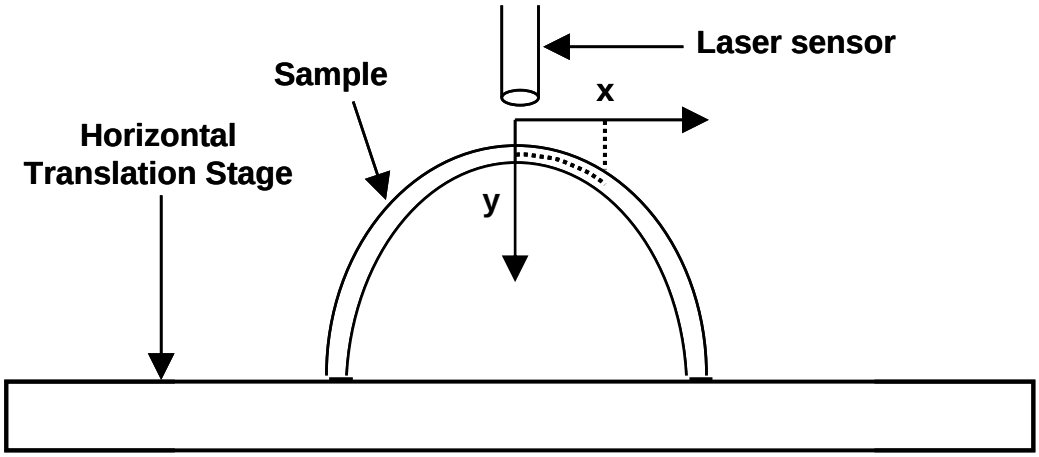

Figure 3-7. Schematic of laser displacement system used for optically measuring the radius of curvature of a bent sample. [Reprinted with permission from the University of Florida.]

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3.2 Hysteresis Measurement

There are two common methods to characterize a ferroelectric capacitor: (1) a hysteresis measurement, and (2) a pulse-switching measurement. This section describes the hysteresis measurement, and the pulse-switching method is described in the subsequent section.

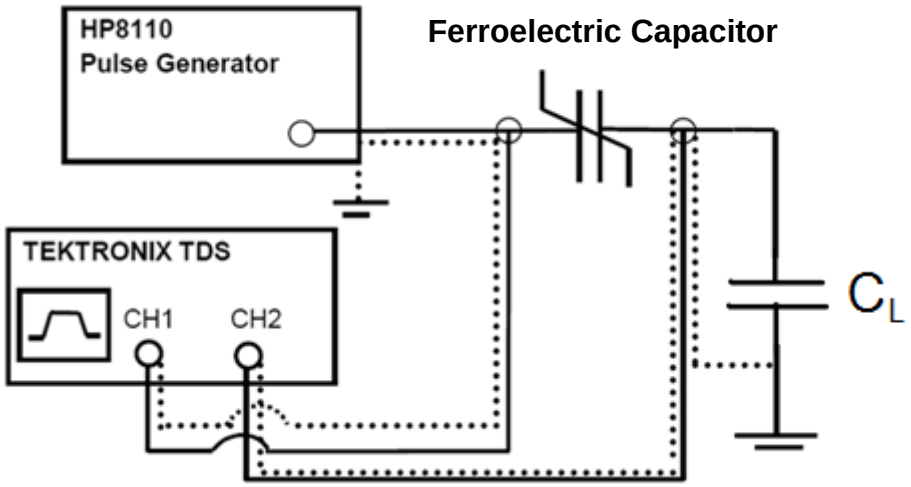


Figure 3-8. Sawyer-Tower circuit used for measuring the hysteresis loop on a ferroelectric capacitor. A pulse generator and oscilloscope are used in the circuit.

The standard measurement for characterizing ferroelectric capacitors has traditionally been the hysteresis loop measurement. The hysteresis loop was previously described in Chapter 2. It represents the polarization of the ferroelectric capacitor as a function of applied electric field. The hysteresis loop for a non-linear capacitor can be measured using a Sawyer-Tower circuit [81] as shown in Figure 3-8. The ferroelectric capacitor is connected in series with a linear load capacitor (C_L). The load capacitance should be chosen to be much larger than the ferroelectric capacitor so that the voltage drop across the C_L is negligible. A function generator is used to apply a low-frequency (50-1000Hz) voltage waveform to the top electrode of the ferroelectric capacitor. As seen in the figure, an oscilloscope is used to measure the applied and load voltages. Figure 3-9 is a sample plot of the typical applied and load voltage waveforms in a Sawyer-Tower circuit for a hysteresis measurement as a function of time. The applied waveform to the circuit is typically a triangular wave that is applied to the top electrode of the ferroelectric capacitor, causing a shared switching charge to appear on both the

ferroelectric and linear capacitor. This switching charge is obtained by measuring the voltage across the load capacitor and multiplying it by the load capacitance.

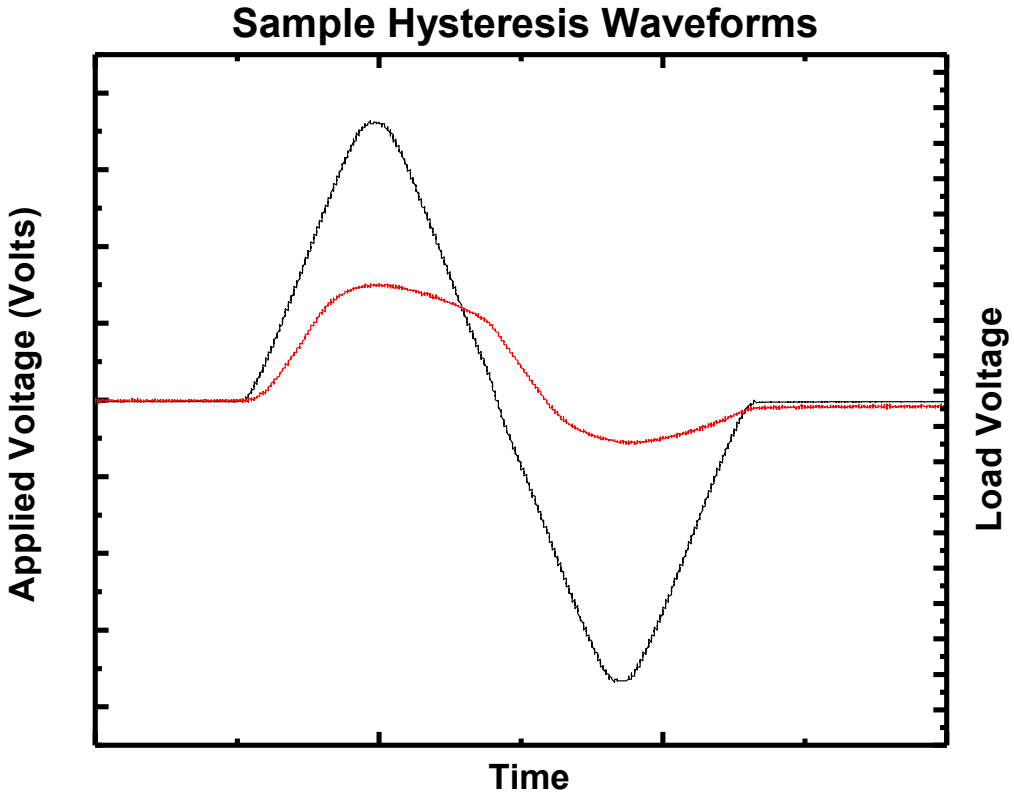


Figure 3-9. Sample applied and load voltage waveforms in a Sawyer-Tower circuit for hysteresis measurement as a function of time.

Polarization is a function of the applied voltage and is calculated as follows

$$P(V_A) = \frac{C_L \times V_L(V_A)}{A_{Ferro}}, \qquad (3\text{-}4)$$

where C_L is the load capacitance, V_L is the voltage measured across the load capacitor , and A_{Ferro} is the area of the ferroelectric capacitor. V_A refers to the applied voltage from the function generator. One then obtains the hysteresis loop of the ferroelectric capacitor by plotting the polarization, $P(V_A)$, as a function of V_A, as shown in Figure 3-10. From the hysteresis loop, it is possible to extract the saturation polarization, P_s, the

remanent polarization, P_r, and the coercive voltage, V_c. P_s is the polarization at which the hysteresis loop saturates. The absolute value of P_{s+} and P_{s-} are typically the same. For a hysteresis loop with a sharp transition, V_c is the voltage at which all the domains approximately switch. However, for a hysteresis loop with a smooth transition, as is the case with most poly-domain ferroelectric thin films, there is a range of voltages at which the domains switch gradually. There are two components to the coercive voltage: V_{c+} and V_{c-}, corresponding to the positive and negative coercive voltages, respectively. The remanent polarization is the polarization present in the capacitor when no external voltage is applied. There are two remanent polarization states: a positive remanent polarization, P_{r+}, and a negative remanent polarization, P_{r-}. P_{r+} and P_{r-} correspond to the "0" and "1" states, respectively, in a binary logic memory. It is this remanent polarization property that makes ferroelectrics suitable for non-volatile memories. P_r is the average of the absolute values of P_{r+} and P_{r-}, or

$$P_r = \frac{\left|P_{r^+}\right| + \left|P_{r^-}\right|}{2} \quad . \qquad \text{(Eq. 3-5)}$$

The switching polarization, P_{sw}, is simply the difference in the positive and negative polarization or

$$P_{sw} = 2P_r = P_{r^+} - P_{r^-} \quad , \qquad \text{(Eq. 3-6)}$$

While the hysteresis loop is a simple and useful measurement for gaining a fundamental insight on ferroelectric capacitors, it is not ideal for memory applications. Application of an AC signal can quickly degrade the ferroelectric properties as a low frequency wave is constantly being applied. This can also induce significant leakage current. This leakage current will in turn distort the hysteresis measurement. Another disadvantage

of the hysteresis measurement is that it typically requires a signal in the low frequency range (50-1000Hz), while ferroelectric memories operate in the hundreds of MHz range.

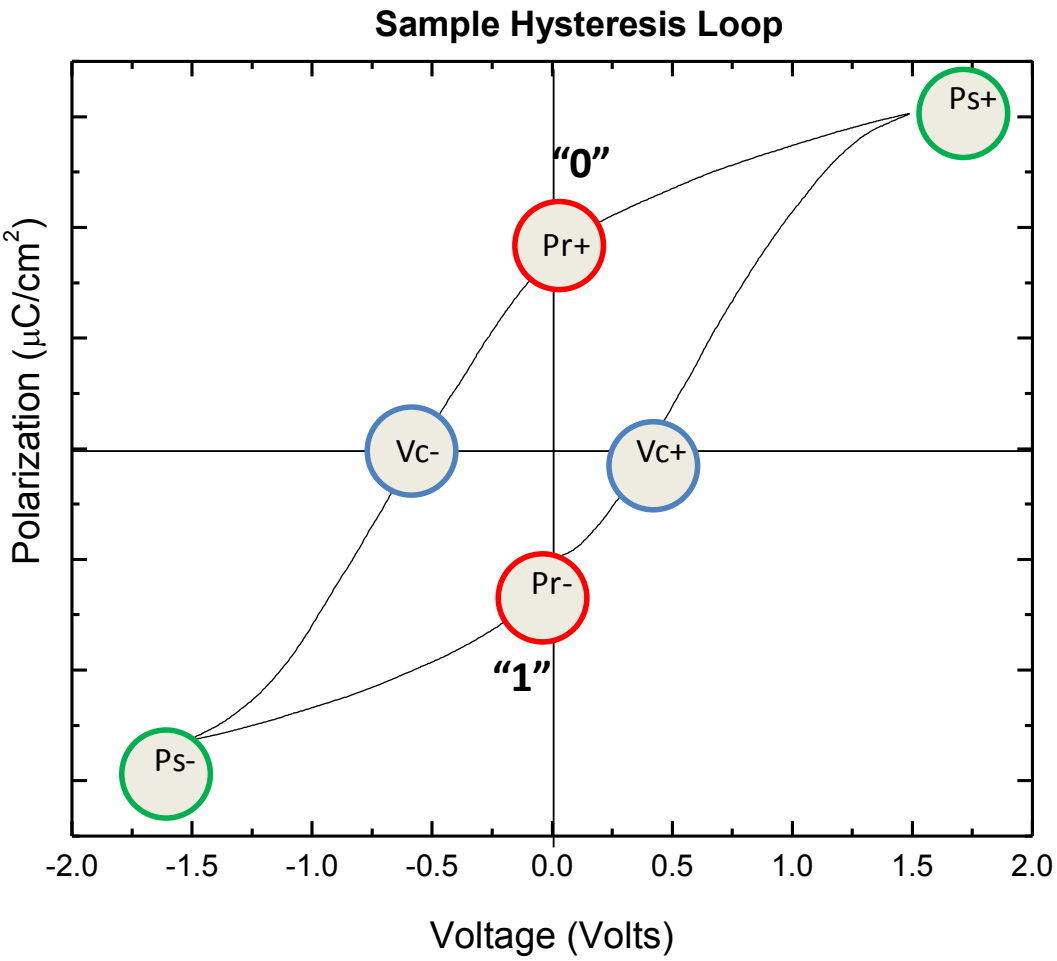


Figure 3-10. Sample hysteresis loop of a PZT thin-film ferroelectric capacitor. The P_r+ state is equivalent to a logic "0", while the P_r- state is equivalent to a logic "1".

3.3 PUND Testing

Pulse testing has become the preferred method to characterize the properties of a ferroelectric capacitor for FRAM. This is mainly due to the fact that it most closely resembles non-volatile memory circuit operation where high speed pulses are applied to write and read the memory cells. It also minimizes leakage current and other

degradation effects that may be induced during the traditional hysteresis measurement. Pulse testing is also useful for measuring the displacement current.

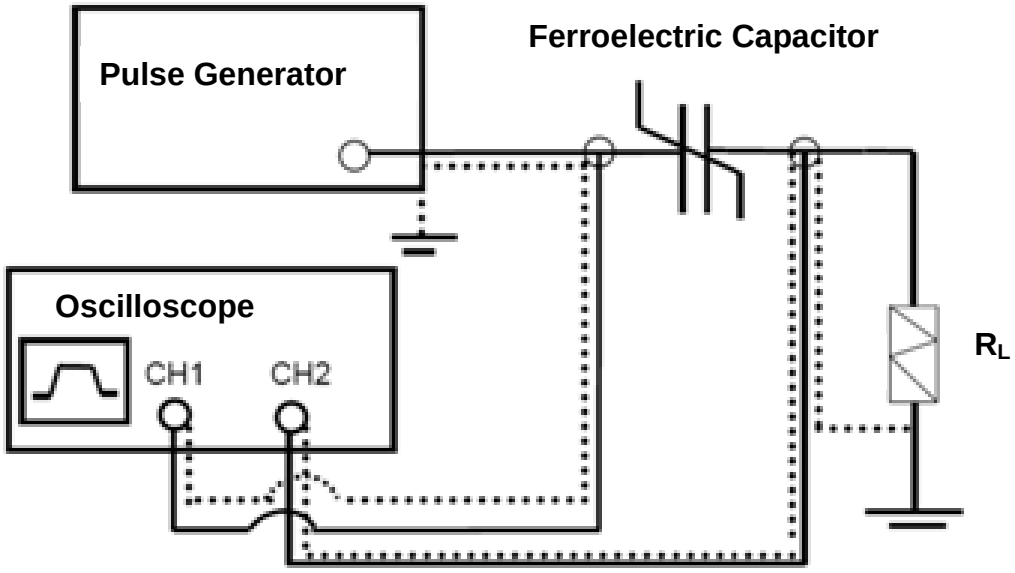


Figure 3-11. Modified Sawyer-Tower circuit for pulse testing on a ferroelectric capacitor. The load capacitor is replaced by a shunt resistor.

In pulse testing, write/read pulses are applied to the ferroelectric capacitor to switch and/or determine the polarization state of the capacitor. Pulse testing is done using a modified Sawyer-Tower circuit, as shown in Figure 3-11. In this circuit, the load capacitor is replaced with a load resistor, R_L, also known as a shunt resistor (consequently, another term for pulse testing is “shunt method”). Using a function (or pulse) generator, a pulse or a series of pulses is applied to the ferroelectric capacitor. The load voltage across the shunt resistor is measured with an oscilloscope. The load voltage is divided by the shunt resistance to obtain the load current. This load current is then integrated over time to obtain the polarization.

According to standardized ferroelectric capacitor testing [82], pulse switching should be done using the PUND method. PUND is an acronym for “Positive Up

Negative Down". The PUND method is used to extract the switched polarization of a ferroelectric capacitor. A sample PUND waveform and the responding measured load voltage from the shunt resistor are shown in Figure 3-12. Before applying a PUND waveform, a negative voltage pulse is usually applied in order to set the polarization of the ferroelectric capacitor. This is known as the "set pulse". Then the PUND waveform is applied by sending two consecutive positive pulses immediately followed by two consecutive negative pulses, as shown in Figure 3-12.

During the "P" pulse, the capacitor is switched from the negative polarization (set-pulse) state to the positive polarization state. Due to this switching, there will be a large displacement current across the shunt capacitor. This displacement current is represented in Figure 3-12 as the load voltage response to the "P" pulse. A sharp spike in the load current can be seen. The P-term is thus referred to as the switching pulse. On the falling edge of the "P" pulse, there is a small negative load voltage response. This is due to backswitching of some domains that takes place after the electric field is removed. After the "P" pulse, the "U" pulse is applied. There is also a load voltage response during the "U" pulse; however it is much smaller than the "P-term" response, since the capacitor was already in the positive polarization state. Therefore, the load response for the "U-term" is referred to as the non-switching current. Again, as the "U" pulse is removed, there is a negative load voltage response which is due to backswitching of some domains.

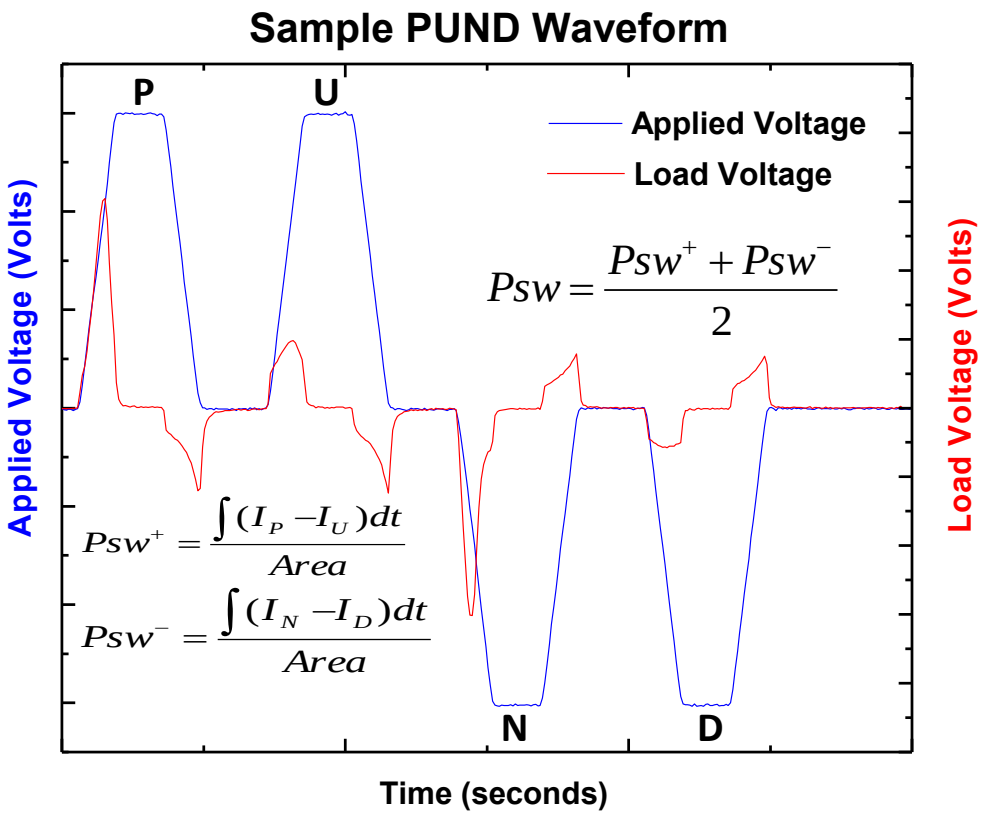


Figure 3-12. Sample applied and load voltage waveforms from a PUND test. Switching polarization is calculated by integrating the area under the load voltage.

The load responses to the “N” and “D” pulses are similar to the “P” and “U” terms, respectively except that the load voltage responses are reversed as can be seen in the figure. The purpose of applying both positive and negative switching and non-switching pulses is that there may be some asymmetry in the ferroelectric capacitors due to asymmetry in the top and bottom electrodes. The positive and negative switching polarization are calculated by subtracting the switching and non-switching currents and integrating this current over time as follows,

$$Psw^+ = \frac{\int (I_P - I_U)dt}{Area} \qquad \text{(Eq. 3-7)}$$

$$Psw^{-} = \frac{\int (I_N - I_D)dt}{Area} \quad , \qquad \text{(Eq. 3-8)}$$

where I_P, I_U, I_N, and I_D are the current responses for the P-, U-, N-, and D-terms, respectively, and *Area* is the area of the ferroelectric capacitor. To obtain the load currents, the corresponding load voltage is divided by the shunt resistance. The switching polarization is then taken as the average magnitude of P_{sw+} and P_{sw-},

$$P_{sw} = \frac{\left|P_{sw^{+}}\right| + \left|P_{sw^{-}}\right|}{2} \quad . \qquad \text{(Eq. 3-9)}$$

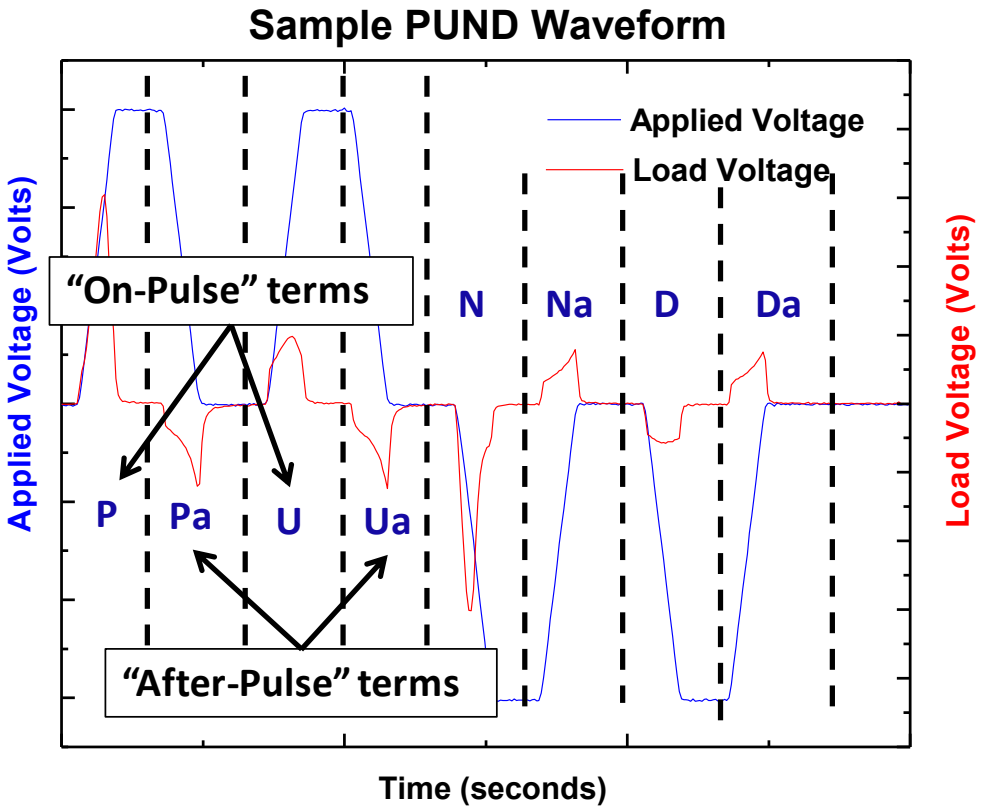


Figure 3-13. Sample PUND waveforms which show how the "On-Pulse" and "After-Pulse" terms are determined.

Figure 3-13 defines the different terms of the PUND waveforms and indicates the times over which the switching and non-switching currents are integrated to obtain the polarization values [82], [83]. There are both “On-pulse” and “After-pulse” terms in the PUND waveforms. “On-pulse” terms are the part of the positive load voltages corresponding to the P-, U-, N-, and D-terms. The “After-pulse” terms contain the backswitching elements of the load voltage. While the “After-pulse” terms are sometimes used to calculate the switching and non-switching polarization, in this study the switching and non-switching polarizations will be calculated using the “On-pulse” terms since the difference is negligible between both methods. For “On-pulse” testing, the current is integrated over the first part of the pulse only, and the “After-pulse” terms are not used in the calculation.

Figure 3-14 illustrates how the PUND waveform switches the ferroelectric capacitor and traverses along the hysteresis loop. Assuming the capacitor is initially set in the negative polarization state, the polarization is at P_{r-} on the hysteresis loop. When the P-pulse is applied, the capacitor switches into the positive polarization state and reaches P_{s+} at the top of the pulse. As the P-pulse is removed, the polarization reduces from P_{s+} and settles into P_{r+} on the hysteresis loop, corresponding to the Pa term. Next, the positive U-pulse is applied. Since the capacitor is already in the positive polarization state the polarization only goes from P_{r+} to P_{s+}. The difference between P_{r+} and P_{s+} is the positive non-switched polarization. After the U pulse is removed, the polarization once again reduces from P_{s+} to P_{r+}, this time representing the Ua term. During the N pulse, the polarization is switched from P_{r+} to P_{s-} at the top of the N pulse, and reduces to P_{r-} after the N pulse is removed (Na). There is then a negative non-switching

polarization from P_{r-} to P_{s-} in response to the D-pulse. Finally, the Da-pulse corresponds to the reduction in polarization from P_{s-} to P_{r-} after the D pulse has been removed.

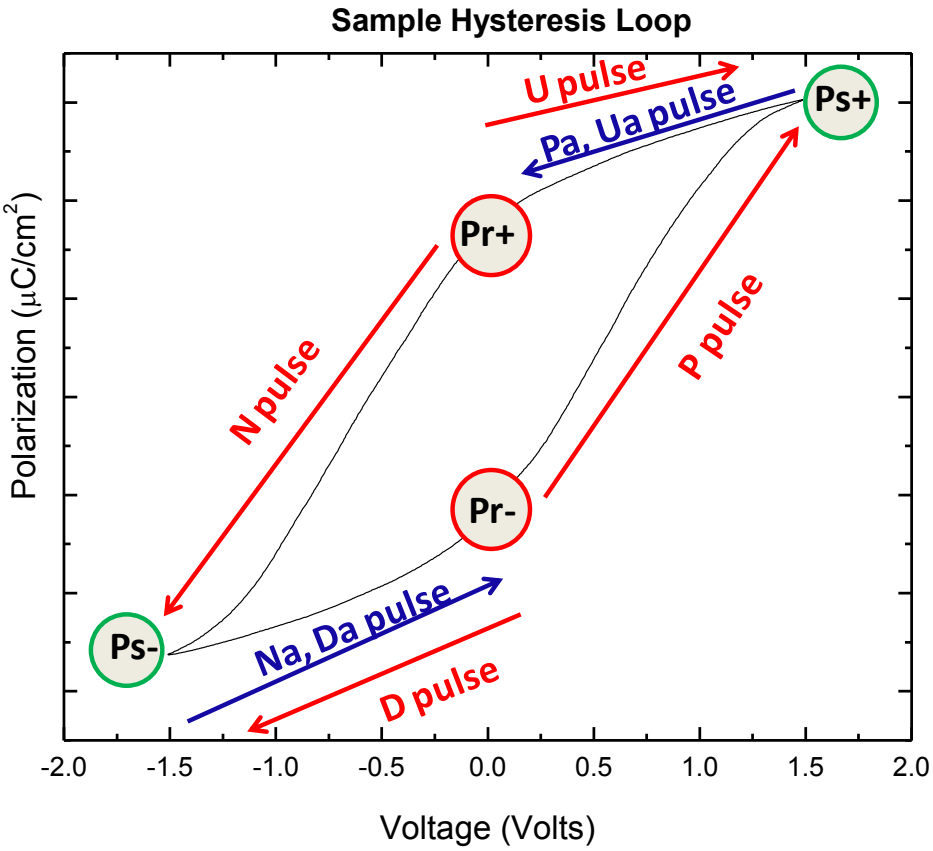


Figure 3-14. Sample hysteresis loop showing the correlation between the hysteresis loop and PUND terms.

The PUND method is commonly used to observe the behavior of the switched polarization as a function of pulse voltage amplitude. In this case, PUND waveforms are swept from low to high voltage on the ferroelectric capacitor and plotted as a function of the applied pulse voltage. Figure 3-15 shows a sample plot of typical PUND curves. Here, the positive and negative switching polarization values are plotted as a function of applied pulse voltage. It can be seen that the polarization begins to saturate

as the voltage is increased. PUND curves are useful for determining the intrinsic behavior of ferroelectric capacitors.

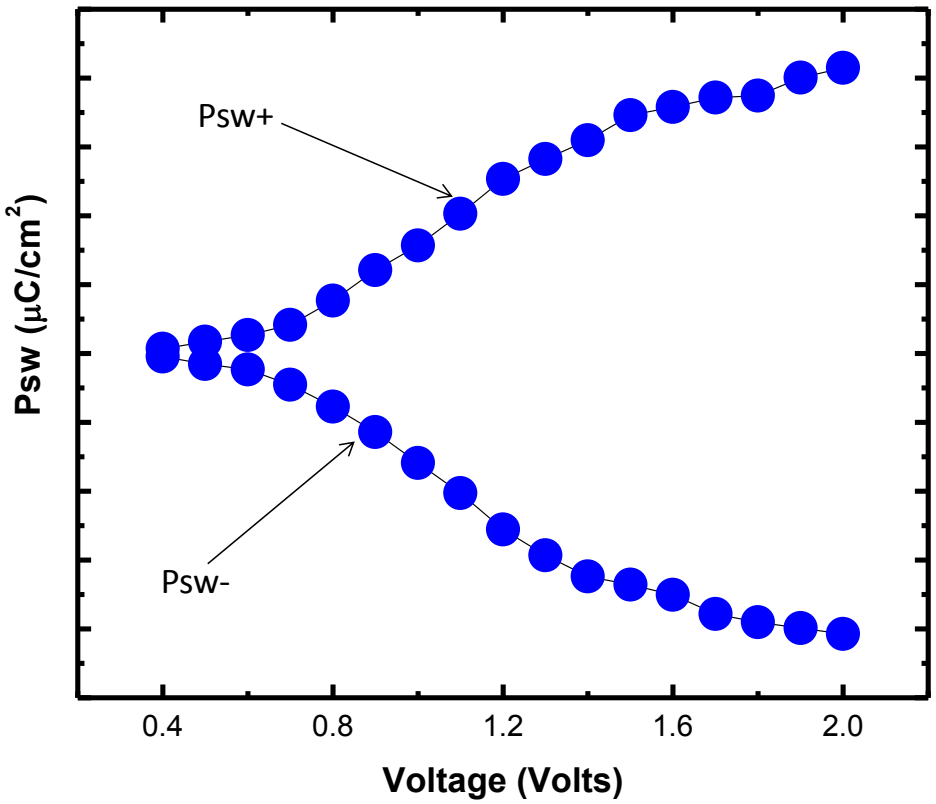


Figure 3-15. Sample PUND curve. A PUND waveform is swept across different voltages and the calculated positive and negative switching polarization is then plotted as a function of voltage.

3.4 Leakage Current

Measurement of leakage current is another important characterization tool for ferroelectric capacitors, especially since ferroelectrics are used as the dielectric layer in FRAM. It is important that there is no significant leakage current in the device as a result of a high electric field during hysteresis and PUND measurements. Leakage current in the capacitor should be monitored along with polarization and switching measurements, especially in the case of the hysteresis measurement during which an

AC signal is applied to the capacitor. Leakage current is also useful for monitoring the electrical breakdown in the device.

Leakage current is caused by carrier conduction in the ferroelectric as a result of a high electric field and temperature. A charge in a ferroelectric capacitor will eventually leak through the dielectric when it is under a high electric field. Leakage current is monitored by incrementally increasing the voltage across the capacitor at a given temperature and measuring the current across the ferroelectric capacitor at each voltage increment. The current or current density is then plotted as a function of applied voltage. It is important that enough time is allowed at each measurement step so that the current being measured is the steady-state leakage current and not the relaxation current. It is recommended that there be about a 1 second interval between each voltage increment [83].

Figure 3-16 shows a sample plot of the leakage current measured across a stand-alone 120μm x 120μm capacitor after Rodriguez *et al.* [83]. In this figure, a voltage is swept across the capacitor from negative polarity to positive polarity, then again from positive polarity to negative polarity, in 100mV increments. Peaks are observed at +/- 0.5V which correspond to the maximum polarization switching displacement currents.

3.5 Cycling Endurance

Cycling endurance is a very important reliability component for ferroelectric memory applications. A memory must be able to switch states reliably at different environmental conditions throughout the lifetime of the device. A standard metric for FRAM reliability is reliable device operation for 10 years at 85ºC. Therefore, it is important to study how the effects of stress, temperature, and bias affect the reliability properties of FRAM.

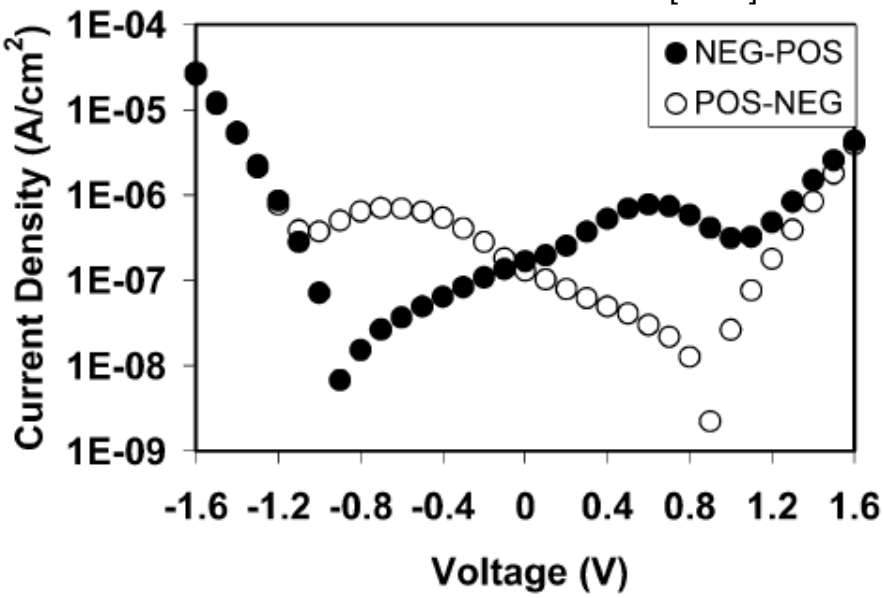


Figure 3-16. Sample plot of leakage current in a ferroelectric capacitor. [Reprinted with permission from J. A. Rodriguez *et al*., "Reliability properties of low-voltage ferroelectric capacitors and memory arrays," *IEEE Trans. Dev. Mat. Rel.*, vol. 4, no. 3, pp. 436-449, Sep. 2004.]

Cycling endurance refers to the amount of switchable polarization that is lost due to read/write cycling during normal device operation. It is also commonly referred to as cycling fatigue. This reduction in switching polarization will affect the FRAM signal margin and may lead to memory malfunction. In FRAM, this becomes a further challenge as it requires an additional rewrite after a read due to destructive reading. A typical FRAM product may require 10^{12} to 10^{14} cycles throughout its lifetime [83]. Ferroelectric fatigue in PZT-based capacitors is believed to be caused by a buildup of space charges at the electrode-ferroelectric thin-film interface [84], [85].

To characterize the cycling endurance, the ferroelectric capacitor is constantly cycled with a bipolar voltage square pulse for a large amount of cycles. Throughout the cycling, a hysteresis and/or PUND test is conducted to monitor the switching polarization as a function of cycling. Accelerated testing can be done by increasing the

cycling voltage, temperature, and by making the voltage cycling pulses shorter. Figure 3-17 shows a sample plot of switched polarization as a function of bipolar voltage pulse cycling after Rodriguez *et al.* [83]. Here both P_{sw+} and P_{sw-} are plotted. Cycling was done at 1.5V and the switching polarization was measured at 1.2V. It can be seen that switched polarization for this device is maintained after $3x10^{11}$ cycles.

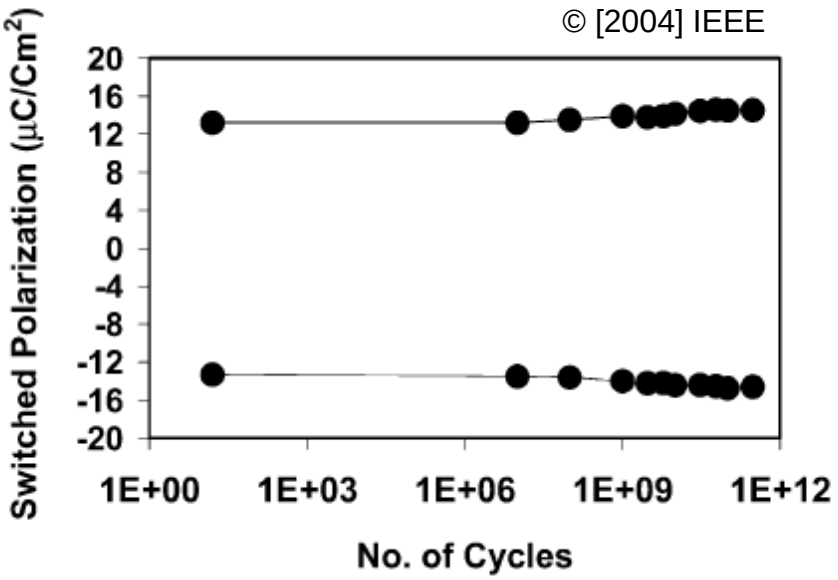


Figure 3-17. Sample plot of the cycling endurance of a ferroelectric capacitor, [Reprinted with permission from J. A. Rodriguez *et al*., "Reliability properties of low-voltage ferroelectric capacitors and memory arrays," *IEEE Trans. Dev. Mat. Rel.*, vol. 4, no. 3, pp. 436-449, Sep. 2004.]

3.6 Experiment Set-up

The experiment set-up for electrical testing is represented in Figure 3-18. A computer is connected to a function generator and oscilloscope via GPIB to control the instruments. An Agilent 33120A arbitrary waveform function generator is used for supplying voltage pulses (PUND measurements, pre-cycling, and cycling endurance) and triangular voltage waves (for hysteresis measurement). Arbitrary pulse waveforms are created using Agilent's Waveform Editor Software and then downloaded onto the

function generator via GPIB. A Tektronix TDS 5104B oscilloscope is used to measure the applied and load voltage pulses.

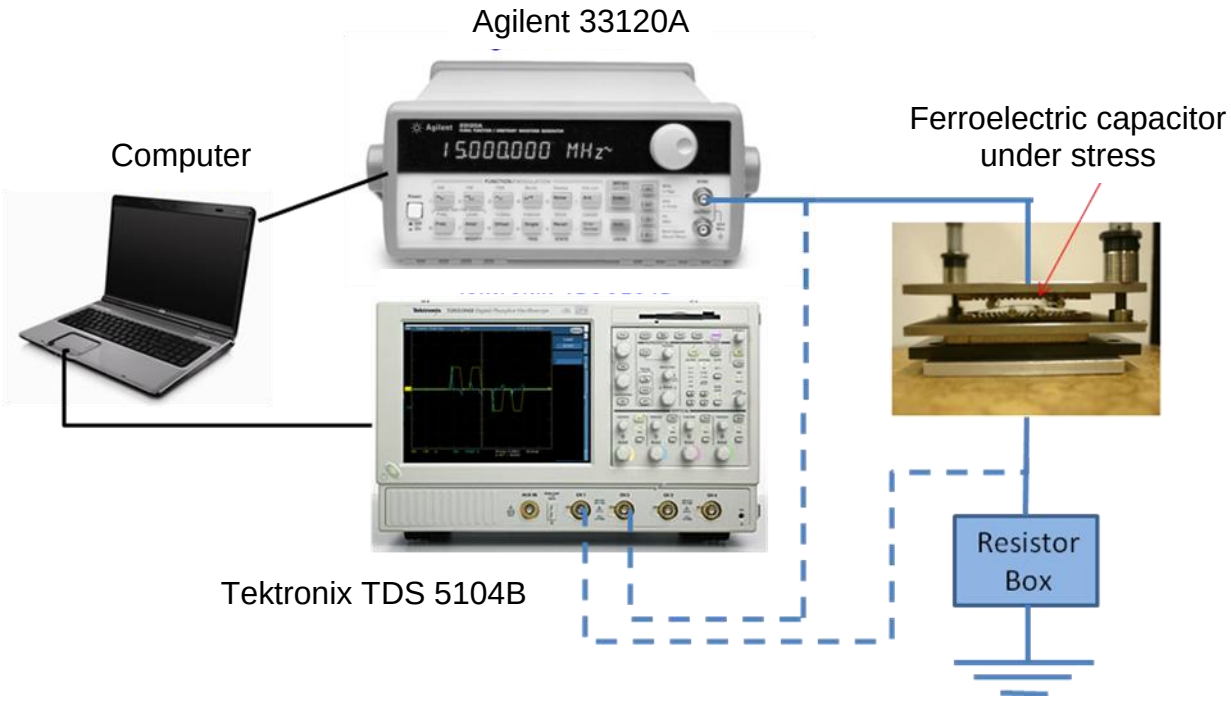


Figure 3-18. Experiment set-up for characterizing ferroelectric capacitors as a function of stress that is used in this investigation. Measurements are automated using GBIP code and MATLAB.

While under stress, the devices on the wafer are probed using two probe tips, each attached to a micromanipulator inside a Faraday cage as shown in Figure 3-19. As can be seen in the figure, an opening on the top plate of the bending apparatus enables probing of the wafer sample while it is under stress. One probe tip, connected to the Agilent 33120A, contacts the top electrode pad of the ferroelectric capacitor. The other probe tip, connected to the resistor box, contacts the bottom electrode pad. The resistor box is used to switch the connection between a linear load capacitor for a hysteresis measurement and shunt resistor for a pulse measurement. The top and

bottom electrodes are also each connected to a different channel on the oscilloscope in order to monitor and record the data.

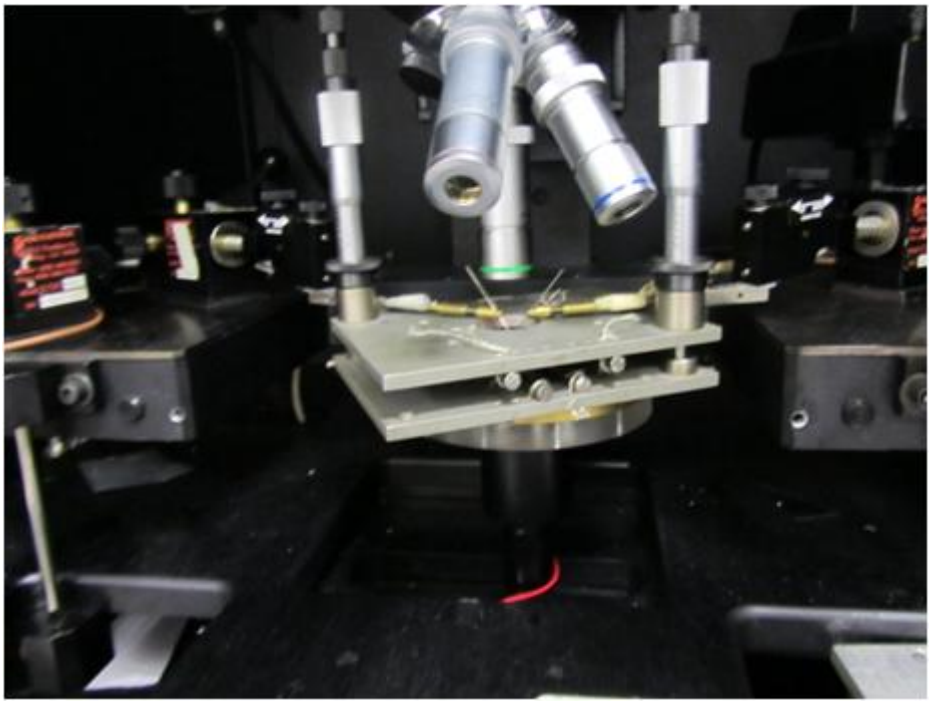


Figure 3-19. Photograph of four-point bending apparatus inside probe station. With the opening on the top plate, it is possible to probe the wafer sample in the apparatus.

The measurements are automated using GPIB code. A custom program was developed in MATLAB called “Ferroelectric Electrical and Reliability Measurement Interface”, or FERMI. The graphical user interface for FERMI is shown in Figure 3-20. Using FERMI, one can choose the type of measurement to be done. The sample name is input into the GUI along with the type and magnitude of stress applied (if any). The user also inputs the ferroelectric capacitor area, load capacitance, and shunt resistance. Finally, the parameters of the waveform are entered such as voltage, frequency, and number of bursts. For pulse measurements, the frequency can be used to vary the pulse width and rise/fall times. The pulse waveforms are fixed so that the rise and fall times are 1/3 of the pulse width as is the recommended test procedure [82], [83].

After the parameters have been entered and the instruments initialized, a button is clicked on the GUI to start and/or stop the measurement. If, for example, the number of bursts is set to 16, then the program will send 16 identical waveforms and record the load voltage responses for each of those waveforms. The data is then averaged out. A plot of the hysteresis or PUND waveforms is shown on the GUI. There are also two tables. One table shows the extracted hysteresis parameters: P_{r+}, P_{r-}, P_r, V_{c+}, V_{c-}, P_{max} (equivalent to $|P_{s+,-}|$), and the stress magnitude. The parameters for the previous measurement on the device are also shown for comparison to the current measurement. The other table shows the following extracted PUND parameters: P-pulse polarization, U-pulse polarization, N-pulse polarization and D-pulse polarization. The table also shows the calculated values for P_{sw} and the stress magnitude. As the measurements are on-going, there is also a graph on the GUI that plots the P_{sw} or P_r vs. stress, depending on the current measurement being conducted. After the measurement is complete, the user can choose to save the data by clicking on the "Save Data" button in the upper right portion of the GUI. There are four files saved with each measurement: (1) a .png file which is a plot of the hysteresis or PUND waveforms, (2) a .txt data file containing the averaged values for Ch1 (applied voltage) and Ch2 (load voltage), (3) a .txt data file containing all of the Ch1 raw data and (4) a .txt data file containing all the Ch2 raw data.

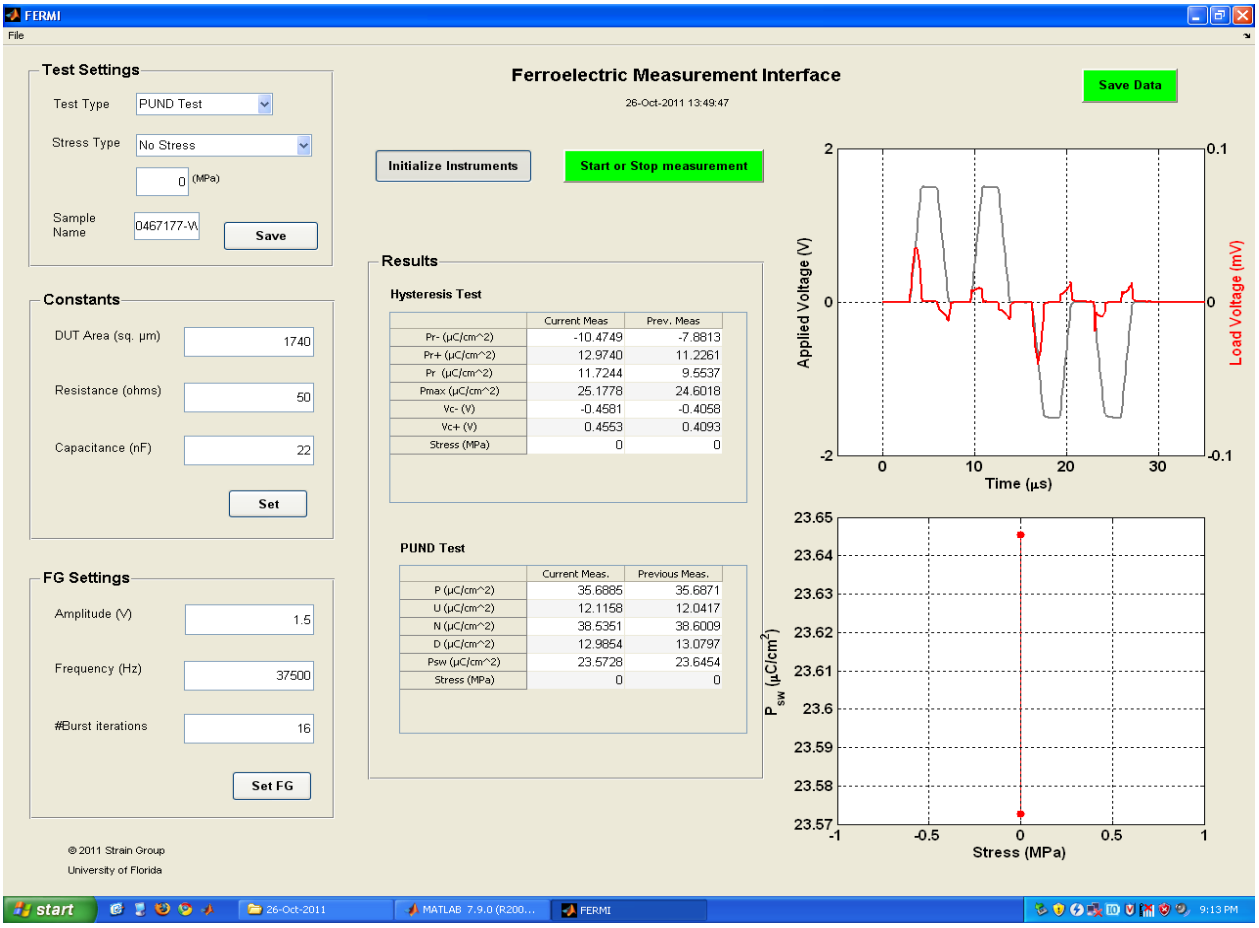


Figure 3-20. Screen capture of the Ferroelectric Electrical and Reliability Measurement Interface (FERMI) graphical user interface (GUI) that is used for automating the measurements and analyzing the data in this study.

While it is currently programmed for hysteresis and PUND measurements, FERMI is currently being modified to include cycling endurance and PUND sweeps as part of the testing procedure for ferroelectric capacitors.

Leakage current measurements are conducted using a Keithley 4200 Semiconductor Characterization System (SCS). Two SMUs from the Keithley 4200 SCS are used for leakage current measurements: one connected to the top electrode of the ferroelectric capacitor and the other connected to the bottom electrode. A voltage sweep is then applied directly to one electrode of the capacitor while the other electrode

is grounded or kept at zero volts. The corresponding current across the capacitor is recorded and plotted as a function of applied voltage.

3.7 Summary

The characterization methods and experiment-setup were presented in this chapter. Wafer bending, used to apply stress to the wafer samples, was introduced. This included four-point bending, three-point bending, and biaxial bending. Methods for calculating and measuring the mechanical stress on the sample were also described. The hysteresis measurement and PUND testing were explained in some detail as well as characterization of leakage current and cycling endurance. Finally, the experimental set-up used for applying stress and automating the measurements was described.

CHAPTER 4
STRESS EFFECTS ON CMOS-INTEGRATED PZT THIN-FILM FERROELECTRIC CAPACITORS AT ROOM TEMPERATURE

Ferroelectric random access memory (FRAM) embedded in a standard CMOS process technology has emerged in recent years as a competitive non-volatile memory, particularly for applications requiring low-power, fast read and write times, and a high cycling endurance [1], [2], [4]. Further scaling of the technology beyond the 130-nm technology node can increase the memory storage density and/or reduce manufacturing costs [5], leading to potential new markets and applications. However, geometric scaling down of ferroelectric thin films will lead to decreased polarization [65], [86–92], and, consequently, a decrease in the FRAM signal margin. It is expected that alternate structures or new materials will be required to scale FRAM to the 90-nm node and beyond [3], [5], [8–11]. These changes can lead to increased manufacturing costs and a large development lag time. Stress engineering may be a possible solution to enable scaling of the current FRAM structure and materials in the short-term. Since the effects of stress on ferroelectric properties also become more significant in ferroelectric thin films as the technology is scaled, it is important to study and understand the physics of stress effects in ferroelectric thin films.

The work described in this chapter investigated the effects of externally applied uniaxial stress on the ferroelectric properties of CMOS-embedded ferroelectric thin films at room temperature. Ferroelectric properties such as polarization and coercive voltage were measured as a function of the applied stress.

The chapter is organized as follows: Previous efforts to apply stress to ferroelectric thin films are first described. This is followed by a description of the experimental details and procedure. The key results are then reported and analyzed,

followed by a discussion of the results. Final conclusions and a summary are then presented at the end of the chapter.

4.1 Background

The effects of stress on ferroelectric thin films have been studied for various conditions due to the relationship between electric field and strain in ferroelectric materials. Tuttle *et al.* [13] were the first to isolate the effects of stress on PZT thin-film ferroelectric capacitors. Compressive stress was induced by depositing a PZT film directly onto an MgO substrate. They observed that compressive stress enhanced the polarization while tensile stress decreased it. They hypothesized that the type of stress present in the thin-film as it is cooled through its Curie temperature controls the orientation and ferroelectric properties present in the film. Thus, for a compressive stress the majority of domains will orient out of the plane of the film while for a tensile stress a majority of the domains will be oriented in the plane of the film. Other researchers have observed similar results as [13] by studying the effects of thermally-induced stress on PZT ferroelectric capacitors [14], [15], [17], [66]. They applied various annealing treatments to the capacitor stack and were able to vary the stress due to thermal lattice mismatch. The results confirmed the hypothesis by Tuttle *et al.*

Stress effects have also been investigated by applying an external mechanical stress [18–20], [22], [23]. Kumazawa *et al.* [18] observed an increase in remanent polarization (3.4%/100MPa) with uniaxial compressive stress and the opposite trend with uniaxial tensile stress (0.6%/100MPa). Their results showed virtually no change in the spontaneous polarization with compressive stress and a change of 0.8%/100MPa with tensile stress. The external stress was applied by bending the sample and probing the top electrode while the sample is under stress. The polarization was then measured

as a function of applied stress. Details of the bending rig were not given but it was assumed to be one-point bending due to the variance in their results (i.e., sample is clamped at one end and bent by applying a force to the other end). They also studied the effects of stress on cycling endurance.

While the work by Kumazawa *et al.* showed similar trends as previous work, the results are unreliable due to the large variance in their results from sample-to-sample. Also, the change in remanent polarization due to compressive stress should equally track changes due to tensile stress. They did not observe a change in the spontaneous polarization which was inconsistent with previous work and attributed this to the difference in switching mechanisms of uniaxial biaxial stress. In addition, they calculated the stress in the thin-film by making several assumptions and did not directly measure the stress/strain in the film. For example, they make the assumption that the stress is uniform throughout the surface of the sample when it is known that the stress will vary throughout the surface on a sample bent by clamping at one end.

Kelman *et al.* [19] studied the effects of external biaxial tensile stress using concentric rings of different diameter. They observed a decrease of 13% in both the spontaneous and remanent polarization at a biaxial stress of 130MPa. The change in polarization was attributed to 90° domain wall motion due to tensile stress. The thickness of their films varied from 70nm to 400nm, and the stress was calculated by monitoring measuring the deflection of the bent wafer sample.

Lee *et al.* [20] enhanced the polarization of PZT films by inducing a permanent compressive stress. They were able to accomplish this by sputtering the film on a bent substrate and immediately removing the sample from the substrate holder after

annealing. A compressive stress of 150MPa was then permanently induced in the PZT thin-film [20]. This corresponded to an increase of 35% and 24% in the remanent and saturation polarizations, respectively [20].

Zhu *et al.* studied the stress effects using both a four-point bending rig [22] and hydrostatic stress [23]. In the former, uniaxial tensile stress up to 150MPa was applied to PZTN (Niobium-doped PZT) thin film capacitors with a thickness of 130nm. With tensile stress, the polarization decreased at a rate of -0.002μC/cm^2 per MPa [22]. In Ref. [23], a 130 nm PZT thin-film capacitor sample was placed inside a poly (tetrafluoroethylene) (PTFE) tube with pressure fluid surrounding the sample. A piston on the pressure cell is pushed down, compressing the PTFE tube and applying an isotropic hydrostatic stress. The polarization was monitored as a function of this applied stress. To compare their results, the stress was converted into an equivalent out-of-plane stress. Their results were consistent with previous work. They also studied the effects of tensile stress on leakage current and observed an increase in leakage current with increasing tensile stress. They attributed the change in polarization to lattice distortion and not domain wall motion since they claim that 90° domain wall motion is impeded due to the clamping of the thin-film on the substrate [23].

In contrast to previous work, the work presented in this chapter focuses on the effects of uniaxial compressive stress on ferroelectric properties and cycling endurance of thin-film PZT capacitors embedded in a CMOS technology.

4.2 Experiment Details

4.2.1 FRAM Process and Device Characteristics

The embedded ferroelectric memory capacitors used in this investigation were fabricated on a standard fully-integrated 130-nm CMOS process [1], [4], designed for a

nominal voltage of 1.5V. It includes 5 layer metal Cu/fused silicon glass (FSG) interconnects, and 70nm thick PZT. Additional process details are shown in Table 4-1 after Moise *et al.* [1]. Figure 4-1 shows a cross section SEM image of the FRAM array. Only two additional masks are required to integrate the ferroelectric capacitors. The ferroelectric module is "sandwiched" between the front-end-of-line (FEOL) and back-end-of-line (BEOL) standard CMOS process. The capacitor gate stack is TiAlN/Ir/PZT/IrO_x/Ir. PZT thin-film is deposited onto an iridium (Ir) electrode via metal organic chemical vapor deposition (MOCVD). The Zr/Ti concentration in the PZT film is 25/75.

Table 4-1. Process and device characteristics of the ferroelectric devices.

Process Features	
Logic	130nm
Interconnect	5LM Cu/FSG
MET 1 Pitch	0.35µm
Nominal Voltage	1.5V
Plug	W
Capacitor	TiAlN/Ir/PZT/IrOx/Ir
Ferroelectric	MOCVD $Pb_{1.0}Zr_{0.25}Ti_{0.75}O_3$
Capacitor Height	250nm
PZT Thickness	70nm
Stack Etch	1 Mask
FRAM VIA	W
FRAM ILD	SiO_2
Mask Adder	2 Masks
FRAM Cap Size (designed)	$0.44\mu m^2$
FRAM Cell Size	$0.71\mu m^2$
SRAM Cell Size	$1.95\mu m^2$

Table 4-2 contains the film thickness and capacitor areas of the various test structures used in this study. PZT ferroelectric capacitors with thicknesses of 70nm were studied. Each device under test (DUT) consisted of an array of capacitors,

ranging from 1 up to 1740 ferroelectric capacitors connected in parallel in the same array. Individual capacitor areas ranged from 1μm^2 to 3600μm^2 while the total capacitor area ranged from 1740μm^2 to 3600μm^2. The nominal voltage was 1.5V.

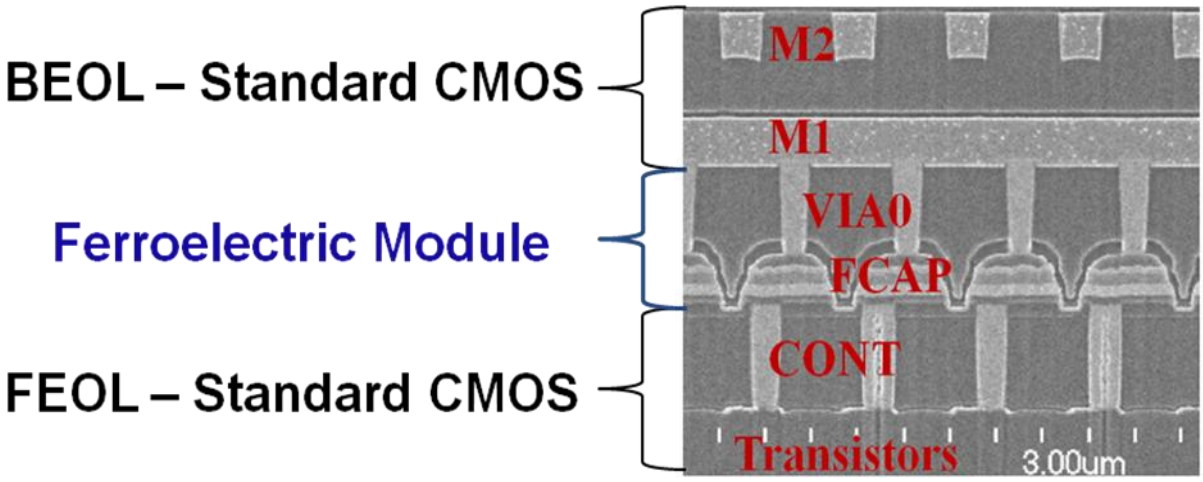


Figure 4-1. Cross section SEM image of FRAM array. [Adapted with permission from T. S. Moise et al., "Demonstration of a 4 Mb, high density ferroelectric memory embedded within a 130 nm, 5 LM Cu/FSG logic process," in *IEEE Int. Electron Devices Meeting*, San Francisco, CA, 2002, pp. 535-538.]

Table 4-2. Thickness and area details for the ferroelectric capacitors used in this study.

PZT Thickness (nm)	Individual Cap Area (μm^2)	# Capacitors in Array	Total Cap Area (μm^2)	Nom. Voltage (V)
70	3600	1	3600	1.5
70	100	18	1800	1.5
70	1	1740	1740	1.5

4.2.2 Experiment Procedure

The hysteresis measurement and PUND test [82] was conducted as a function of stress. Figure 4-2 shows the testing procedure that was used to study the effects of stress. A four-point bending apparatus was used to apply uniaxial stresses up to 240MPa to the devices. Initially, before any stress is applied, a "wake-up" cycling (or "pre-cycling") treatment is applied to each DUT. During this process at least 200,000

continuous bipolar cycles with peak voltage of +/- 1.5V are applied to the DUT. This ensures that previously inactive domains will become activated due to the constant cycling (this process is similar to electrically poling a virgin device). After enough cycling, the switching polarization will begin to saturate and any changes in the polarization observed will be solely due to stress and not electric field cycling.

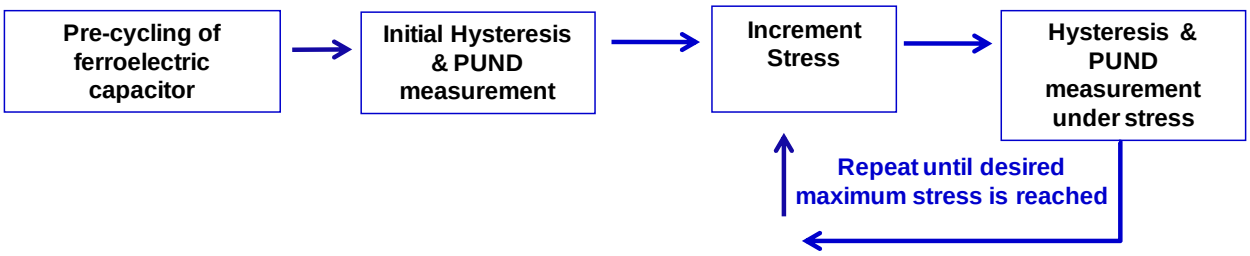


Figure 4-2. Experimental test procedure for characterizing ferroelectric capacitors as a function of stress at room temperature

A Sawyer–Tower circuit is used for the hysteresis measurement while a modified Sawyer-Tower configuration was used for the PUND test [81], [82]. Figure 3-16 showed a diagram of the test set-up which was discussed in more detail in Chapter 3. An Agilent 33120A Arbitrary Waveform Generator is used to supply the voltage pulses and a Tektronix TDS 5104B oscilloscope is used to measure the load voltages, either on the linear capacitor or the shunt resistor, depending on the measurement type.

For the hysteresis measurements, a triangular waveform is applied at a frequency of 1 kHz, with peak voltages of +/-1.5V. The capacitance of the linear capacitor was 22nF. For the PUND measurement, the pulse width is 3μs with a rise/fall time of 1μs. The frequency of the PUND waveform is 37.5 kHz. The delay between pulses is approximately 2μs. The pulse voltage was 1.5V (unless otherwise noted), and the shunt resistance was 50Ω.

FERMI was used to automate the measurements and collect and analyze the data (FERMI was discussed in more detail in Chapter 3). The hysteresis parameters or P_r, P_s, and V_c are extracted and the switched polarization is calculated from the PUND measurement.

4.3 Results and Analysis

To illustrate the overall effects of mechanical stress on the polarization properties, Figure 4-3 shows the hysteresis loop of a 3600μm^2 ferroelectric capacitor at 0MPa and 224MPa of applied uniaxial compressive stress. The polarization in the figure is normalized to the zero stress remanent polarization. Clear increases in the saturation and remanent polarization are observed while there is no change in the coercive voltage. P_r increased by 9.6% at -240MPa, while P_{max} increased by 6.3%. Both P_{r+} and P_{r-} contributed to the increase in P_r. This result was consistent for all DUTs tested in this study, which also included array DUTs with individual capacitor areas of 100μm^2 and 1μm^2.

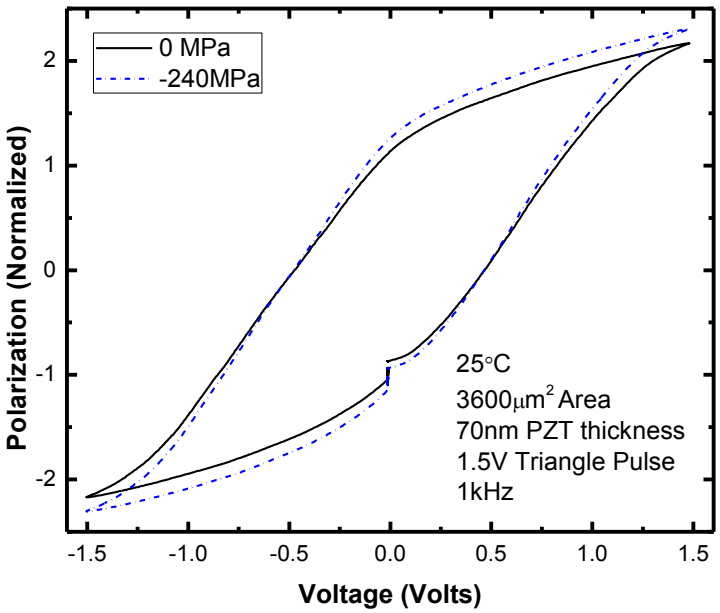


Figure 4-3. Comparison of a hysteresis loop at 0MPa and -240MPa of applied compressive stress for a 3600μm^2, 70nm thick PZT ferroelectric capacitor.

Figure 4-4 plots the percent change in remanent polarization, ΔP_r, as a function of the mechanically applied compressive stress. Data is shown for DUTs of three different individual capacitor areas: 3600μm^2, 100μm^2, and 1μm^2. A clear increase in P_r with applied stress is observed. The capacitor area does not appear to have a significant influence on ΔP_r, meaning that stress-induced polarization enhancement scales with area. The data shows a linear trend, with a maximum ΔP_r of almost 8% at 224MPa. This leads to a rate of change of P_r of 3.37%/100MPa. Also plotted in Figure 4-4 is the expected change in P_r from the lattice distortion model (LD). The LD model, and its discrepancy when compared to our data, will be discussed later in this section.

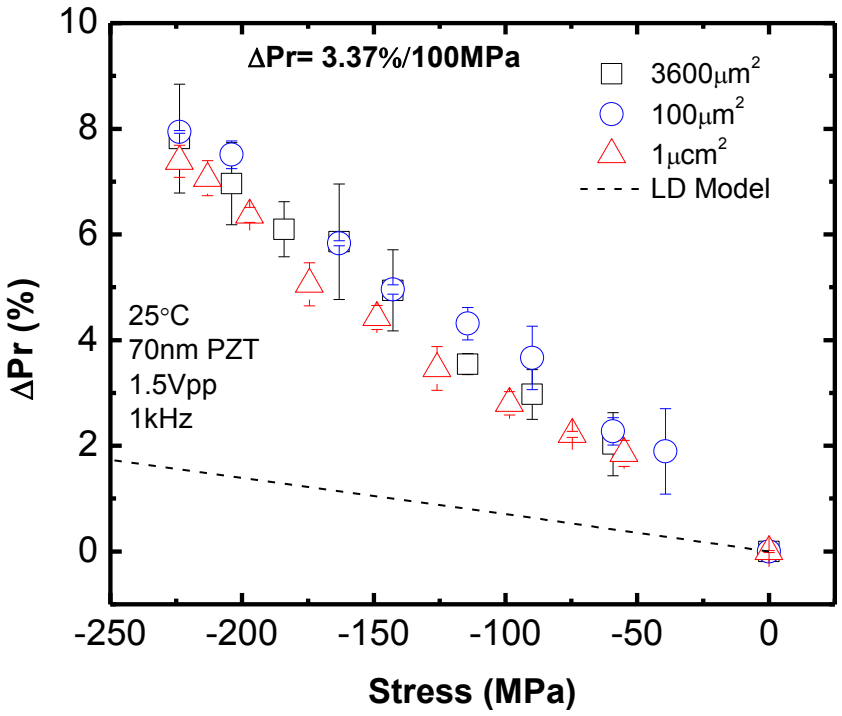


Figure 4-4. Change in remanent polarization (ΔP_r) as a function of applied compressive stress for ferroelectric capacitors of different areas. Expected ΔP_r based on lattice distortion (LD) model is also plotted.

In a similar fashion, the percent change in the maximum polarization, ΔP_{max}, is plotted as a function of stress in Figure 4-5. P_{max} may also be referred to as the saturation polarization (P_{sat}). Similar trends are observed as with ΔP_r. ΔP_{max} increased linearly with increasing uniaxial compressive stress. However, at 2.68%/MPa, the rate of change for ΔP_{max} is lower than for ΔP_r. This result is significant as it indicates that there is less domain relaxation with an applied compressive stress when the applied voltage during the hysteresis measurement is removed. Thus the polarization loss due to domain relaxation and backswitching is decreased with an applied compressive stress.

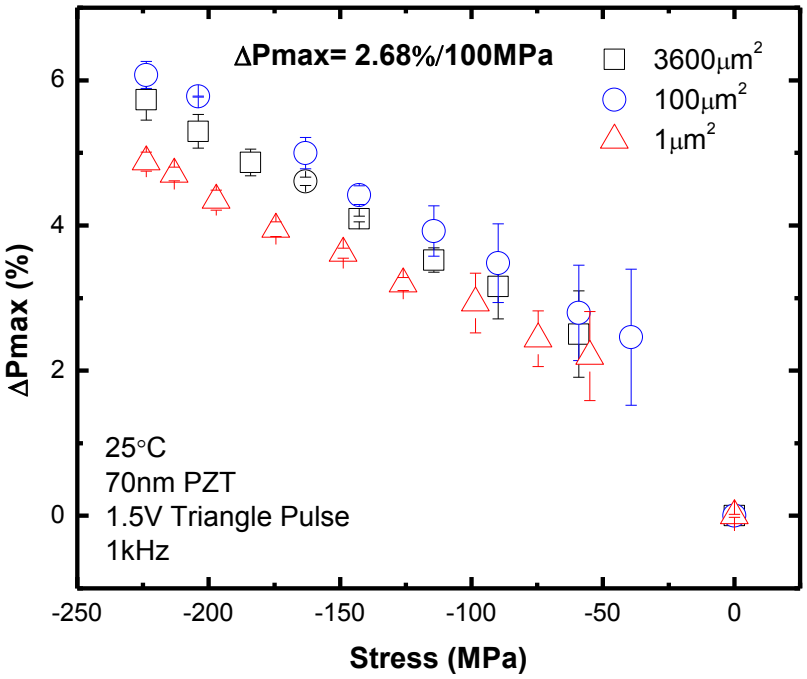


Figure 4-5. Change in maximum polarization (ΔP_{max}) as a function of mechanically applied compressive stress for ferroelectric capacitors of different areas.

As aforementioned, there did not appear to be any significant change in the coercive voltage with applied compressive stress. This is illustrated in Figure 4-6, where the change in coercive voltage, ΔV_c, is plotted as a function of applied uniaxial

compressive stress for DUTs with three different individual capacitor areas. There is no discernible trend with stress and any fluctuation is within the error margin of the measurement. This result is consistent with previously published data where a stress was applied in the plane of the film [15], [19], [22]. It may be noted that Zhu *et al.*, observed a significant change in V_c with applied stress [23]. However, in this work a hydrostatic stress up to 1.5GPa was applied. In addition, when the hydrostatic stress was converted into an effective out-of-plane stress, a maximum effective out-of-plane stress of approximately 600MPa was applied. In their earlier work, Zhu *et al* applied an in-plane tensile stress up to 150MPa and did not observe a significant change in the coercive voltage [22]. Therefore it may be possible that while no change in V_c is observed at in-plane the stress levels studied in this work (≤ 240MPa), a large enough out-of-plane stress may cause significant change in the coercive voltages.

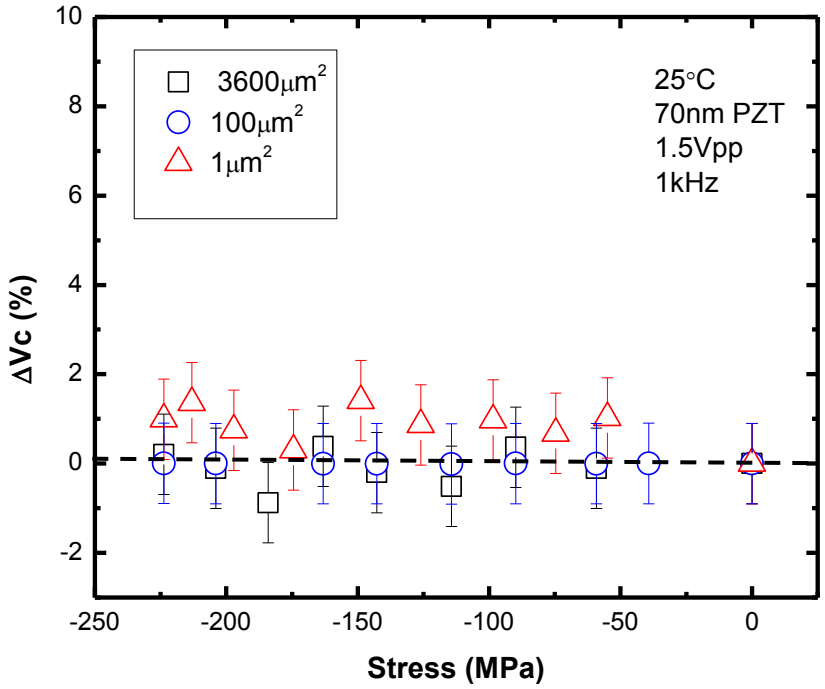


Figure 4-6. Change in coercive voltage (ΔV_c) as a function of mechanically applied compressive stress for ferroelectric capacitors of different areas.

The switching polarization extracted from a PUND measurement was also measured as a function of applied uniaxial compressive stress. P_{sw} calculated from PUND should correlate to $2P_r$ extracted from the hysteresis loop measurement ($2P_r$ is also essentially P_{sw}). The two values should be similar, although there will be some variance due to the measurement error and higher frequency of the PUND waveform compared to the triangle waveform. Therefore, performing a PUND measurement in addition to hysteresis can serve to better validate the results.

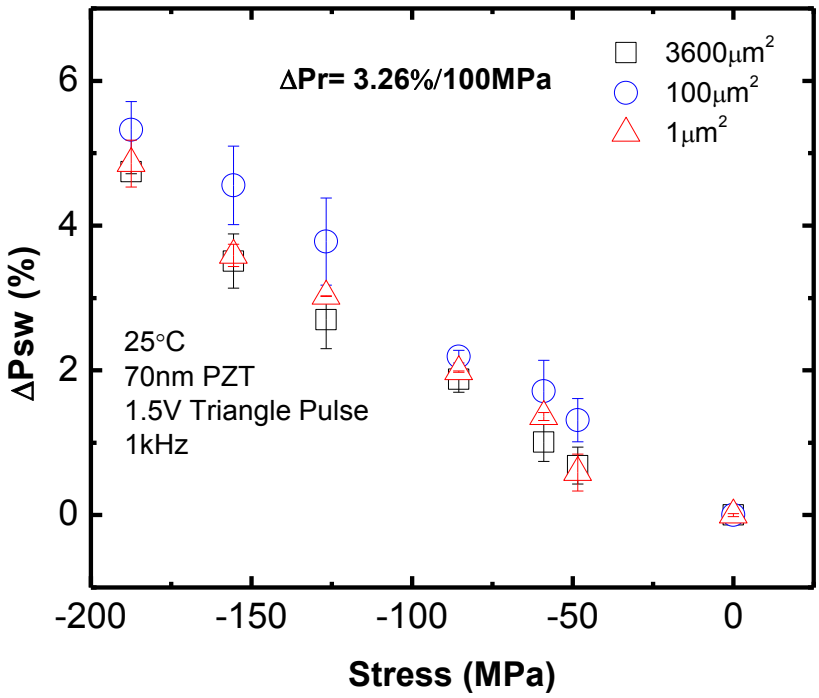


Figure 4-7. Change in switching polarization (ΔP_{sw}) as a function of mechanically applied compressive stress for ferroelectric capacitors of different areas.

The switching polarization calculated from a PUND measurement, ΔP_{sw}, as a function of applied compressive stress is plotted in Figure 4-7 for three different individual capacitor areas. For these devices, the maximum applied compressive stress was almost -190MPa. The same trend is observed as for ΔP_r, that is, an increase in

ΔP_{sw} with increasing compressive stress. When fitted to a linear trend, the rate of change of P_{sw} is 3.26%/100MPa which, as expected, is very similar to that for ΔP_r (3.37%/100MPa). In terms of practicality, PUND measurements are more useful for calculating switching polarization as it more closely resembles the pulse that is used in a memory device. In addition, pulse testing minimizes leakage current that is commonly observed when doing hysteresis measurements in capacitors with small dimensions, which are used in memory devices.

The effect of stress on the cycling endurance of thin-film ferroelectric capacitors was also characterized. Cycling endurance is a key component of memory reliability and characterizes the device's ability to retain data over a large number of applied cycles. It simulates continuous write and read commands of a memory device. Therefore it is important to study how stress affects the reliability properties of a device.

Figure 4-8 compares the cycling endurance of two identical DUTs. One DUT was cycled with no external stress applied (0MPa) and the other was cycled at a compressive stress of -150MPa. The DUTs were 3600μm^2 and up to 3x10^{10} cycles were applied. A larger pulse voltage (1.8V) and frequency (1.2MHz) were used for cycling fatigue than is typically used for characterizing P_{sw} in order to induce degradation in the device. The switching polarization was measured after various cycling intervals. The normalized P_{sw} is plotted as a function of cycles. The values were normalized to the switching polarization at 0MPa of applied stress. P_{sw} is initially larger for the sample under compressive stress. After cycling is completed, there does not appear to be a significant difference in the P_{sw} degradation for the stressed sample when compared to the un-stressed sample. This indicates that compressive stress

does not appear to accelerate the degradation mechanisms. These results are consistent with previous work reported by Kumazawa *et al* [18].

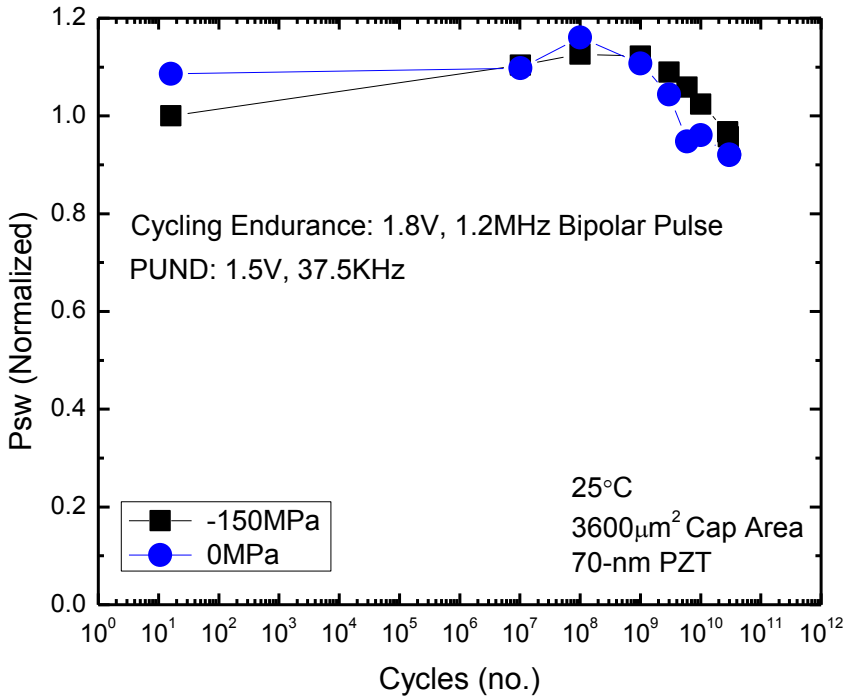


Figure 4-8. Effects of uniaxial compressive stress on cycling endurance of ferroelectric thin-film capacitors.

4.4 Physics and Discussion

The effects of stress on ferroelectric materials at the microscopic level are illustrated in Figure 4-9. For a single crystal lattice in a tetragonal structure, an applied mechanical stress, which is above the coercive stress, will switch the Zr/Ti ion into a lattice direction which is perpendicular to the direction of the applied stress [67], [93]. Coercive stress is the stress required for 90° domain reorientation. The reason for this is that the energy equilibrium of the system is disturbed upon the application of an external stimulus, which in this case is stress. The energy landscape is changed, and in an effort to minimize the internal energy of the system, the central ion will settle into a

new minimum energy. Unlike the application of an electric field, a stress will only cause 90º switching. Thus, the ion will switch into one of the four possible neighboring directions.

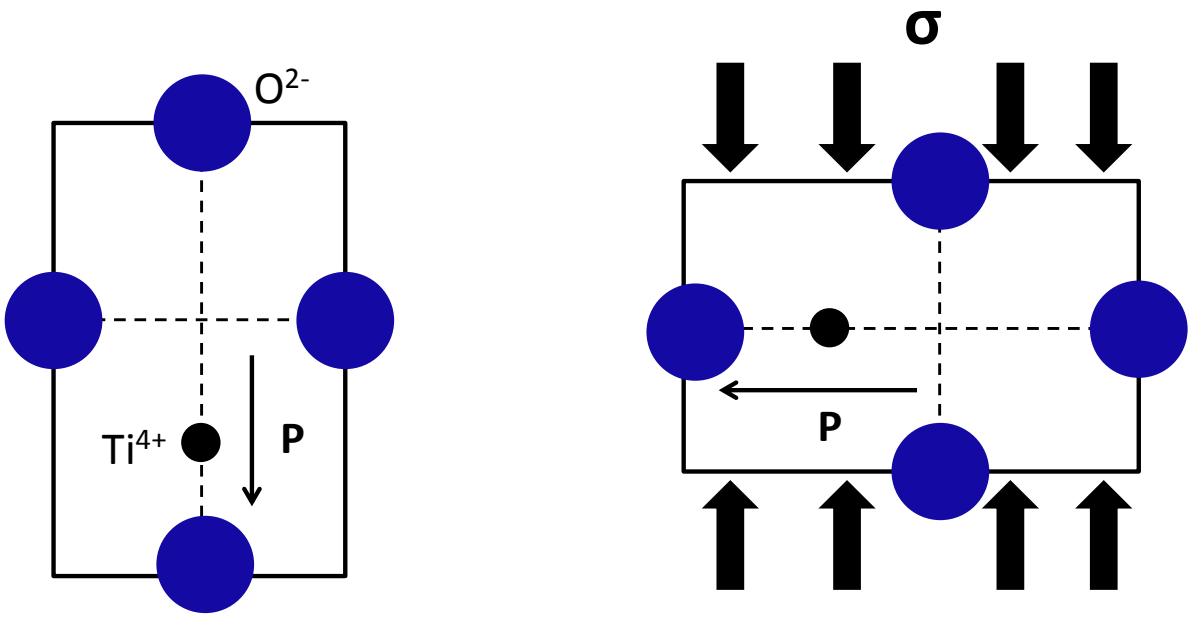


Figure 4-9. 90° switching at the lattice level induced by a compressive stress.

The change in energy with stress is illustrated in Figure 4-10 for an *a*-type domain. Initially, the energetically favored P_{90} state (90° domain) is preferred, as shown in Figure 4-10A. An applied in-plane compressive stress will introduce additional energy into the system (this energy can also be in the form of an electric field, or a combination of electric field and stress). In order to minimize this energy, the barrier required for switching into P_+ or P_- from the P_{90} state will be lowered, as shown in Figure 4-10B. If enough energy is introduced, the P_{90} minima is eventually eliminated and the Gibbs energy landscape changes into what is shown in Figure 4-10C [94]. The central ion will settle into either P_+ or P_-. To switch from one state into another, a certain energy magnitude is required to move the ion over the P_s barrier.

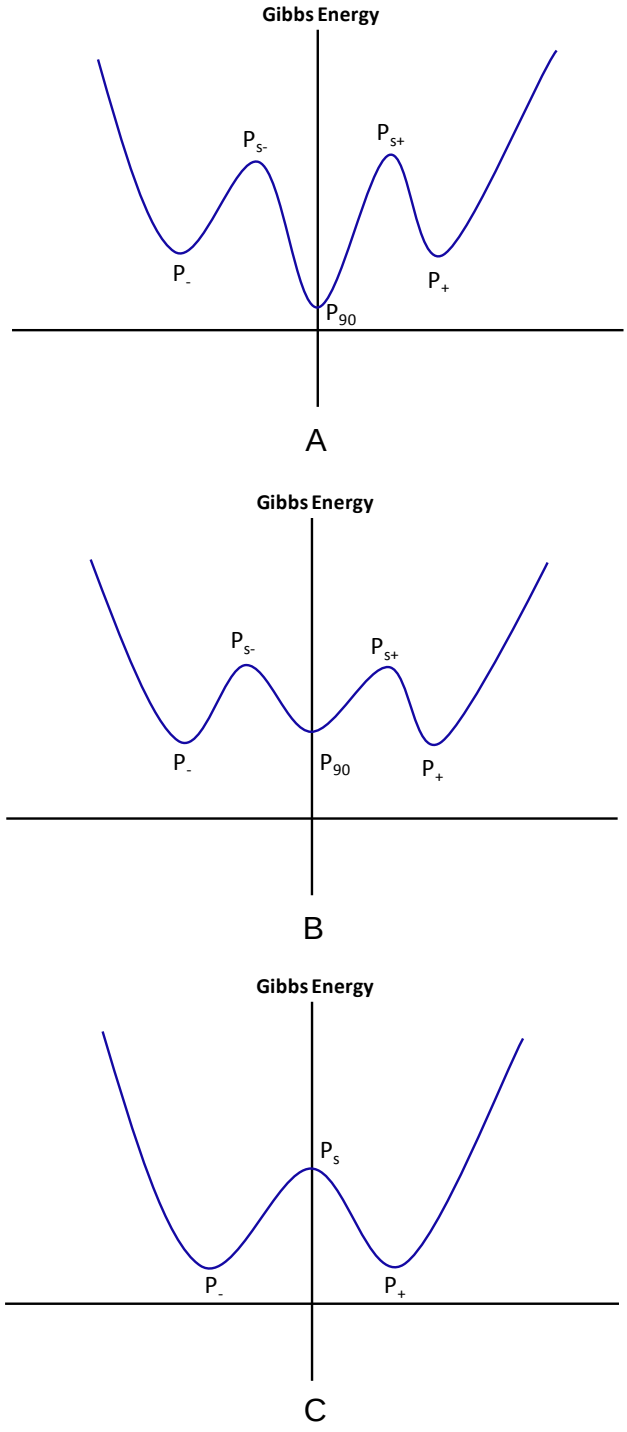


Figure 4-10. Gibbs free energy of an in-plane tetragonal ferroelectric single crystal at A) equilibrium (no stress or electric field applied), B) upon application of external energy due to compressive stress, and C) after enough energy has been introduced to eliminate P_{90} minima. [Adapted with permission from B. L. Ball, R. C. Smith, S.-J. Kim, and S. Seelecke, "A stress-dependent hysteresis model for ferroelectric materials," *Journal of Intelligent Material Systems and Structures*, vol. 18, no. 1, pp. 69-88, Jan. 2007.]

Quantitatively, minimizing the energy can be expressed as [93]

$$\frac{\partial G}{\partial P} = 0 \,, \tag{4-1}$$

where *G* is the Gibbs free energy and *P* is the polarization. The Gibbs free energy is defined as [93]

$$G(E,P,\sigma) = \hat{\psi}(P,\sigma) - EP - \sigma\varepsilon \,, \tag{4-2}$$

where *E* is the applied electric field, σ is the applied stress, ε is the strain, and ψ is the elastic free energy as derived in Ref. [93]. The electric field required to eliminate the P_{90} minima (E_c^{90}) as a function of stress, also derived in Ref. [93], can be defined as

$$E_c^{90}(\sigma) = -(\sigma)\frac{a + 2qP_{90}}{Y} - \frac{2q^2P_{90}^3 + 3aqP_{90}^2 + (a^2 - \eta^2 Y)P_{90}}{Y} \,, \tag{4-3}$$

where *Y* is the Young's Modulus, *a* is the piezoelectric coefficient, *q* is the electrostrictive coefficient, and η is a coefficient used in Ref. [93]. Stress-induced 90° switching will occur when the applied stress is greater than the coercive stress, $\sigma > \sigma_c$. A more detailed quantitative analysis of the stress effects can be found in Ref. [93].

The effects of stress at the macroscopic level are illustrated in Figure 4-11. The figure shows 90° domain wall mobility due to an applied stress. When a compressive stress is applied, domains oriented in the plane of the film will re-orient to the out-of-plane direction, increasing the volume fraction of *c*-type domains and enhancing the net polarization as a result. A tensile stress will have the opposite effect (decrease in the ratio of *c*-type to *a*-type domains). It should be noted that domain wall mobility is more limited in thin films than in bulk ferroelectric materials. This is due to increased defects, non-homogeneous regions (in the case of polycrystalline material), and clamping effects due to substrate-induced strain, all of which can cause domain pinning [32], [49], [95].

Another mechanism for the change in polarization due to stress is lattice distortion. During lattice distortion, the ratio of the *c* lattice parameter to the *a* lattice parameter in a tetragonal structure is altered but the Zr/Ti ion does not switch. This is related to the spontaneous polarization, P_s, as follows [96], [97]

$$c/a - 1 = QP_s^2, \tag{4-4}$$

where *Q* is the electrostrictive constant of the ferroelectric film.

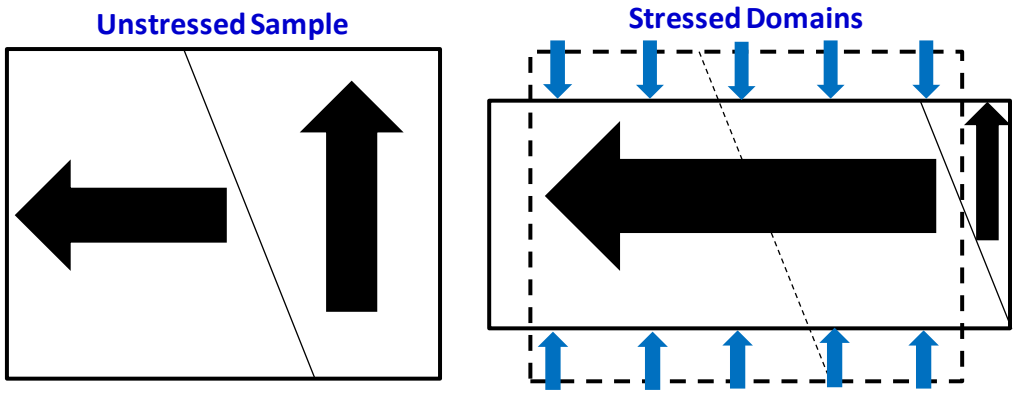


Figure 4-11. 90° domain wall mobility due to an applied compressive stress.

The results obtained in this work are consistent with similar work that has been reported in the literature. Namely, a mechanical compressive stress applied in the plane of the PZT thin-film will increase the polarization properties (larger P_r, P_{max}, and P_{sw}). The uniqueness of this work is that the effects of stress on PZT thin film capacitors embedded in a standard CMOS technology process were investigated at room temperature. In addition, this study focused specifically on compressive stress for the purposes of enhancing polarization whereas previous similar studies have focused on uniaxial tensile stress [19], [22], [23].

Kumazawa *et al.,* reported a mean P_r change of 3.4% per 100MPa [18], compared to the 3.37% per 100MPa observed in this work. However, Kumazawa and workers did not observe a significant change in the saturation polarization (it is assumed that the spontaneous polarization reported in their work refers to the saturation polarization) [18].

When compared to the work of Zhu *et al.*[22], the present work shows a larger rate of increase of the polarization with applied mechanical stress. Zhu and co-authors reported a polarization change of -.0023μC/cm^2 per MPa and a critical stress of 7.8GPa [22]. Critical stress refers to the extrapolated stress at which the thin film loses its ferroelectricity (this will be a positive or tensile stress). In this work, the extracted rate of change is -0.0062μC/cm^2 per MPa and extrapolated critical stress of 2.9GPa. A similar observation is made when comparing the obtained results in this work with those from the work of Zhu *et al.,* in 2009. In order to properly compare our results obtained from a uniaxial in-plane stress to those from Ref. [23] using hydrostatic stress, the in-plane stress was converted into an effective out-of-plane stress as was done in Ref. [23]. After conversion to an effective out-of-plane stress Zhu and co-workers report a P_r change of -0.013μC/cm^2 per MPa and a critical stress of 1.4GPa. This compares to -0.021μC/cm^2 and 860MPa for the P_r change and critical stress, respectively, obtained in the present work.

Proposed mechanisms for the change in polarization with applied mechanical stress include lattice distortion and 90° domain wall movement. Zhu *et al.,* claim that the change in polarization with an applied stress in their work is only to lattice distortion and not 90º domain wall motion (or ferroelastic switching, as is referred to in Ref. [23]).

They made this conclusion by comparing the results for their thin films (130nm) with available data for a 600nm film and a bulk material and attributed the high residual stress and clamping effect in the film for inhibiting ferroelastic switching [23]. To determine if the stress effects observed in this work were due only to lattice distortion, the out-of-plane polarization (or remanent polarization) was calculated using the lattice distortion model developed in Ref. [98] and compared to the experimental results. The out-of-plane polarization can be calculated as a function of stress using the following relation based on the Landau-Ginzburg-Devonshire free energy expansion [98]

$$P_3(\sigma) = \sqrt{-\frac{\alpha_{11}}{3\alpha_{111}} + \frac{\sqrt{\alpha_{11}^2 - 3\alpha_1\alpha_{111} + 6Q_{12}\alpha_{111}\sigma}}{3\alpha_{111}}}\,, \qquad (4\text{-}5)$$

where α_1, α_{11}, and α_{111} are the dielectric stiffness coefficients, Q_{12} is the electrostriction constant, and σ is the stress. The dielectric stiffness coefficients and electrostriction constant depend on the composition of the ferroelectric film and were calculated using equations from Refs. [99], [100].

The P_r calculated from the Lattice Distortion (LD) model is plotted along with the experimental data in Figure 4-4. The LD model significantly underestimates the observed change in P_r with stress. The large discrepancy between the experimental results and the model indicates that the stress-induced polarization enhancement observed in this work is not solely due to lattice distortion but is also due to ferroelastic switching, or 90° domain wall motion.

Kelman *et al.,* reported on a similar experiment where a biaxial tensile stress was applied to ferroelectric thin film capacitors [19]. They observed a linear decrease in the polarization with applied tensile stress. P_r decreased up to 13% at 130MPa [19]. The

experimental results were compared to two models: the LD model from Ref. [98], where polarization change is due to only distortion of the lattice and a domain wall motion model [19]. Their data fit the domain wall motion model well and, similar to the present work, there was a large discrepancy between their experimental results and the LD model. Thus, they concluded that the change in polarization in their films was due to both lattice distortion and domain wall motion.

The polarization can be calculated from the domain wall motion model reported in Ref. [19] using the following equation

$$\frac{P - P_0}{P_0} = \frac{A_c^{'} - A_c^0}{A_c^0}, \tag{4-6}$$

where P is the polarization at a certain stress, P_0 is the initial polarization when no stress is applied, A'_c is the area fraction of c-type domains at a certain stress level, and A^0_c is the area fraction of *c*-type domains before application of stress.

Knowledge of the initial domain volume fraction and lattice parameters at nzero externally applied stress is required for this model. Kelman *et al.,* performed an XRD analysis on their un-stressed sample to determine these values. They then assumed that 90° domain wall motion accommodates all of the imposed strain. By measuring the strain with a strain gage, they were then able to approximate the volume fraction of *a*-type and *c*-type domains at different stress levels. While the data in Ref. [19] fit the domain wall motion model well, it should be noted that there was a large variance in the calculation of the unstressed volume fraction of *c*-type domains.

An improved method to quantify these results would employ an *in situ* XRD scan and analysis as mechanical stress is being applied to the sample. With this method the volume fraction of domains at each stress level can then be directly calculated, rather

than estimated, and will reduce the uncertainty of the calculation. The challenge in comparing our results to the 90° domain wall motion is that it is very difficult to detect PZT in the thin films used in this study due to their integration into a CMOS process. The PZT films are surrounded by many different structures. All of the different metal layers in the stack can make it difficult to accurately detect PZT. Also, the total PZT volume in device is very small compared to the entire volume of the sample.

Initial results from XRD experiments conducted on the CMOS-embedded PZT thin-film devices in a standard university-level laboratory were inconclusive. It was therefore determined that a high energy X-ray beam was needed. Subsequent experiments were conducted at the Advanced Photon Source at Argonne National Labs. Preliminary results are shown in Figure 4-12. The figure plots the intensity of refracted X-rays as a function of lattice spacing at different angles of reflection. The peaks indicate that PZT was strongly detected in the {110} and {001} orientations. Future experiments and plans for performing in-situ XRD analysis are addressed in Chapter 7.

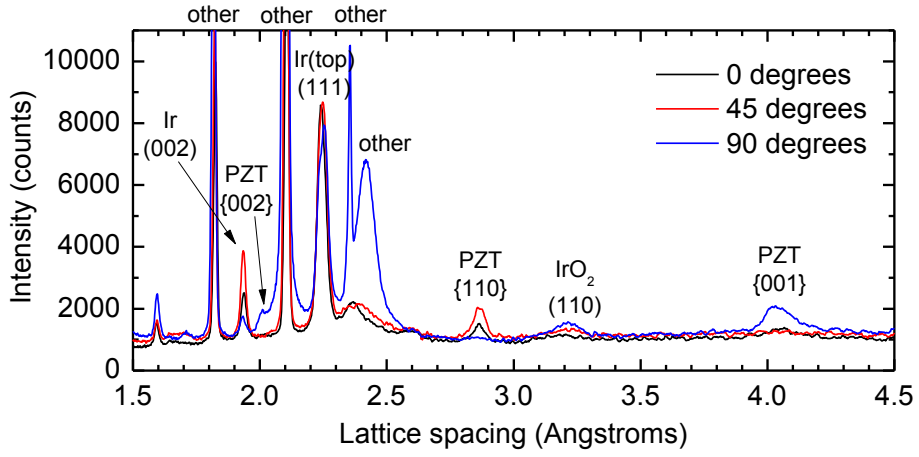


Figure 4-12. XRD patterns of PZT thin-film capacitors embedded in a 130-nm CMOS process technology.

4.5 Summary and Conclusions

To the best knowledge of the author, this is the first work to investigate the effects of a mechanically applied stress on PZT thin film ferroelectric capacitors embedded in a standard CMOS technology. Uniaxial mechanical compressive stress up to -240MPa was applied using a four-point bending flexure-based apparatus and the ferroelectric properties were characterized as a function of stress. An increase in the remanent polarization of 3.37% per 100MPa was observed for ferroelectric capacitors of different areas. Increases in the maximum polarization and switching polarization (calculated from the PUND test) were also observed with compressive stress while there was no significant change in the coercive voltage. The effect of stress on the cycling endurance of the capacitors was also characterized. Stress did not appear to accelerate degradation due to cycling fatigue. The observed trends on PZT thin film ferroelectric capacitors embedded in a 130-nm CMOS technology were similar to previously reported results on non-integrated thin film and bulk PZT; however there was some discrepancy in the magnitude of the change. This discrepancy can be due to differences in the fabrication, thickness, and residual stress of the different devices that were tested.

Energy based models were discussed to explain the physics of the observed results. The enhanced polarization is attributed to increased volume fraction of *c*-type domains when stress is applied and an increase in the ratio of the *c* lattice parameter to the *a* lattice parameter. At the microscopic level this can be explained by minimization of the Gibbs free energy and a reduction in the energy barrier required to switch an in-plane domain to an out-of-plane domain. Macroscopically, this leads to increased 90º domain wall motion.

The stress effects observed in this work are attributed to both lattice distortion and 90° domain wall motion. In order to quantify stress-induced domain wall motion, an XRD analysis of the embedded PZT films is required. Initial results indicate that PZT can be detected in our devices using high energy X-rays. Future experiments will be designed to quantify domain volume fraction *in situ* as a function of stress using XRD.

CHAPTER 5
STRESS EFFECTS ON CMOS-INTEGRATED PZT THIN-FILM FERROELECTRIC CAPACITORS AT ELEVATED TEMPERATURE

Traditionally, temperature and electric field have been used to pole and/or switch ferroelectric materials[101–112]. It has also been shown that stress can influence the behavior of ferroelectric materials [13–15], [18], [19], [22–24], [66], [67], [113], [114]. As was described in Chapter 4, the switching and remanent polarization can be significantly enhanced with the right amount and type of stress. The results presented showed an increase in P_r of 3.37% per -100MPa with applied uniaxial compressive stress. According to previous literature, the maximum P_r possible in PZT thin films is approximately 75μC/cm^2 [88–90], [97], [115]. According to Baerwald, the upper limit of the polarization of a tetragonal ceramic is 0.831*P*, where *P* is the polarization of a single domain[116]. The maximum polarization of PZT will depend on the Zr/Ti ratio. For bulk $PbTiO_3$ (100% Ti), the maximum spontaneous polarization has been theoretically calculated to be 75μC/cm^2 by Haun *et al* [117].

Assuming the linear dependence shown in the results from Chapter 4 continues at high stress levels, and assuming 100% domain orientation (i.e. no domain pinning), it will take a stress of almost 10GPa to reach the maximum polarization in our ferroelectric capacitors at room temperature. Inducing this level of stress on a 130-nm CMOS technology integrated wafer for strain engineering purposes will be virtually impossible. Therefore, other methods are needed to maximize the total possible polarization in PZT thin films in order to scale the current stacked planar FRAM structure to future technology nodes.

The work presented in this chapter investigated the effects of applying stress at elevated temperature in CMOS-embedded PZT thin film ferroelectric capacitors. The

objective was to determine if temperature can be used in addition to stress to enhance the polarization to even higher levels than was observed with stress at room temperature. The thermal energy introduced by an elevated temperature may help to reorient previously inactive domains and decrease the necessary stress required to enhance the remanent polarization to levels approaching 75μC/cm^2.

A brief background on the effects of temperature on ferroelectric thin films and the maximum polarization possible in these materials is first given. This is followed by the experimental details and methods used in the study. The results are then reported and analyzed, followed by a discussion of the results and physics. The chapter ends with a summary and conclusions from the work presented.

5.1 Background

A polycrystalline ferroelectric material in its virgin state is composed of many randomly oriented domains. For a tetragonal structure, there exist two types of domains: *c*-type, which are polarized out of the plane of the film, and *a*-type, which are polarized in the plane of the film. While initially randomly oriented, upon the application of an electric field most of the domains will attempt to re-orient in a polarization direction closest to the direction of the applied field. Under a (001) electric field some *c*-type domains reorient 180° and some *a*-type domains will reorient 90° relative to their initial polarization directions. However, not all of the domains are able to reorient upon application of an electric field, even if enough energy is supplied, and thus the maximum possible polarization is not achieved. This is due to the structure of the material, lattice defects, intrinsic effects, etc. In bulk materials, it is typically assumed that most, if not all, 180° domains can switch upon application of an electric field but not many of the 90° domains reorient. For example, if there is 100% switching of 180° domains but no

switching of 90° domains, then only 28% of the total crystal polarization will be obtained, according to Berlincourt and Krueger [109]. Mechanical stress has been used as a means to aid in the switching of 90° domains [21], [101], [102], [113], [118–121]; however, as was shown in Chapter 4, polarization changes due to stress are incremental.

Domain reorientation becomes more difficult in thin films, mainly due to increased 90° domain pinning caused by substrate clamping, stress effects, surface effects and other intrinsic effects [88–91], [97], [122]. There may also be reduced tetragonality in ultra-thin films [88–90], [97]. However, a maximum remanent or spontaneous polarization of 75μC/cm^2 has been experimentally shown in PZT thin films down to 15nm by careful engineering of the bottom electrode materials [88], [89], which is in agreement with the theoretically calculated maximum polarization from Haun *et al*[115]. While the proof of concept has been shown, engineering ferroelectric thin films with 100% c-type domain orientation for maximum polarization is difficult to implement on a large-scale manufacturing platform due to process integration issues. Therefore, alternate methods should be investigated to maximize polarization in thin films and enable scaling of the technology.

Elevated temperature has been previously used in conjunction with stress to advantageously control domain growth and orientation[13], [15], [20], [24], [66], [113], [123]. However, in these previous works the temperature was applied mostly during device processing and fabrication. Tuttle *et al.,* first theorized in 1992 that the type of stress present in ferroelectric thin films as the sample is cooled through the Curie point to room temperature strongly influences the domain orientation [13]. This work was

further extended and validated by Brennecka *et al* [24]. Similar to Ref. [13], they showed that the stress state as the sample is cooled through the Curie temperature can be used to control 90° domain structures. In a patent filed in 2000, Hendrix and co-workers proposed that the properties of a ferroelectric film can be controlled by applying a force to the substrate during the deposition process of the material or during the cooling of the material from an elevated temperature as a result of the deposition process [123]. Similar work was done by Lee *et al* [20], [113]. They applied a stress to the substrate of the film during the annealing process. Annealing is a heat treatment step during fabrication that follows thin film deposition. After annealing, there was a residual compressive stress in the film which enhanced the remanent polarization up to 35% and the saturation polarization up to 24% [20]. Spierings *et al.*[66], and Shepard *et al.*[15], observed that both the annealing temperature and electrode materials influence the stress induced in the films. This, in turn, will either enhance or degrade the polarization depending on the type of induced stress.

Previous literature indicates that annealing ferroelectric thin films at temperatures approaching the Curie point and subsequently cooling while under stress can significantly enhance the polarization in these films. The uniqueness of the work presented in this chapter is that both external mechanical stress and high temperature approaching the Curie point were applied after the device has been processed.

5.2 Experiment Details

5.2.1 FRAM Process and Device Characteristics

The embedded ferroelectric memory capacitors used in this investigation were fabricated on a standard fully-integrated 130-nm CMOS process [1], [4], designed for a nominal voltage of 1.5V. It includes 5 layer metal Cu/FSG interconnects, and 70nm

thick PZT. Additional process details were shown in Table 4-1 in Chapter 4 after Moise *et al* [1]. Figure 4-1 showed a cross section SEM image of the FRAM array. Only two additional masks are required to integrate the ferroelectric capacitors. The ferroelectric module is "sandwiched" between the front end-of-line (FEOL) and back end-of-line (BEOL) standard CMOS process. The capacitor gate stack is TiAlN/Ir/PZT/IrO_x/Ir. PZT thin-film is deposited onto an iridium (Ir) electrode via metal organic chemical vapor deposition (MOCVD). The Zr/Ti concentration in the PZT film is 25/75.

Table 4-2 lists the film thickness and capacitor areas of the various test structures used in this study. PZT ferroelectric capacitors with a thickness of 70nm were studied. Each device under test (DUT) consisted of an array of capacitors, ranging from 1 up to 1740 ferroelectric capacitors in the same array. Individual capacitor areas ranged from 1μm^2 to 3600μm^2 while the total capacitor area ranged from 1740μm^2 to 3600μm^2.

5.2.2 Experiment Procedure

The typical experiment procedure used for applying stress at elevated temperature is shown in Figure 5-1. The devices were first characterized with hysteresis and PUND measurements at room temperature and no externally applied stress. This initial characterization included "wakeup" cycling of the capacitors. An external uniaxial compressive stress of -150MPa was then applied using a novel quartz 3-point bending apparatus, shown in Figure 3-6. This bending apparatus was specifically designed for applying stress at high temperature [78].

After externally applying stress, the sample was placed in a tube furnace that was previously set to the desired temperature, which was at or slightly below the Curie temperature of the PZT films. After the sample reached the set temperature, it was annealed for approximately 2 minutes. The at-stress sample was then removed from

the tube furnace and allowed to cool to room temperature. Once at room temperature, the sample was removed from the quartz stress apparatus, and its ferroelectric properties were characterized with hysteresis and PUND measurements.

A schematic of this experiment set-up is shown in Figure 5-2. A thermocouple is used to monitor the temperature on the bent wafer sample. The stress is measured using a general purpose strain gage from OMEGA engineering (Part no. SG-2/350-LY11) as was described in Chapter 4 [124]. The total anneal time, including the time for the sample to reach the desired temperature and time to cool to room temperature, was approximately 10 minutes.

Some of the DUTs tested in this study were characterized only after the sample was annealed at stress and elevated temperature (no initial characterization). This was done to determine what effect, if any, electrical cycling had on the devices before the stress and temperature treatment.

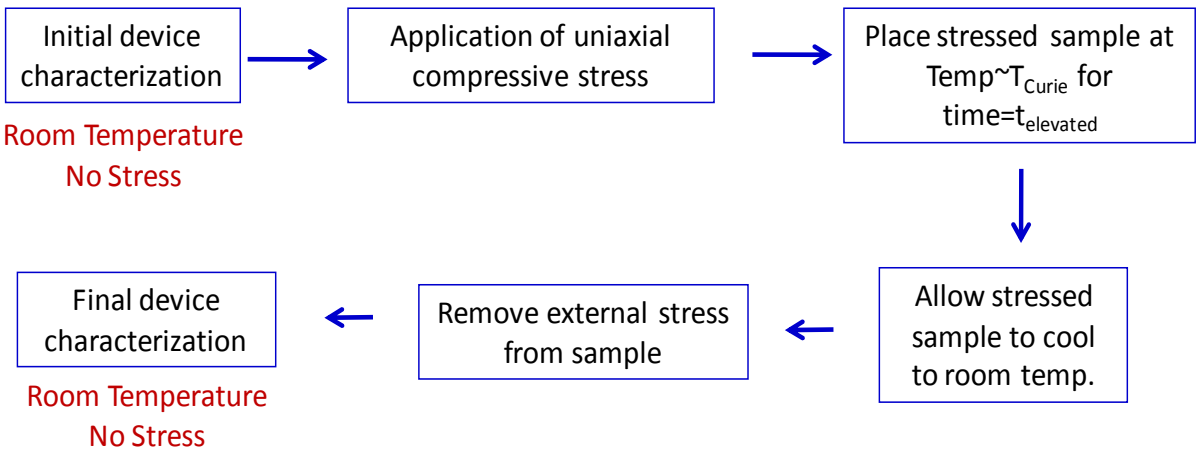


Figure 5-1. Typical experiment procedure used for applying a uniaxial compressive stress at elevated temperature to the PZT thin film capacitors.

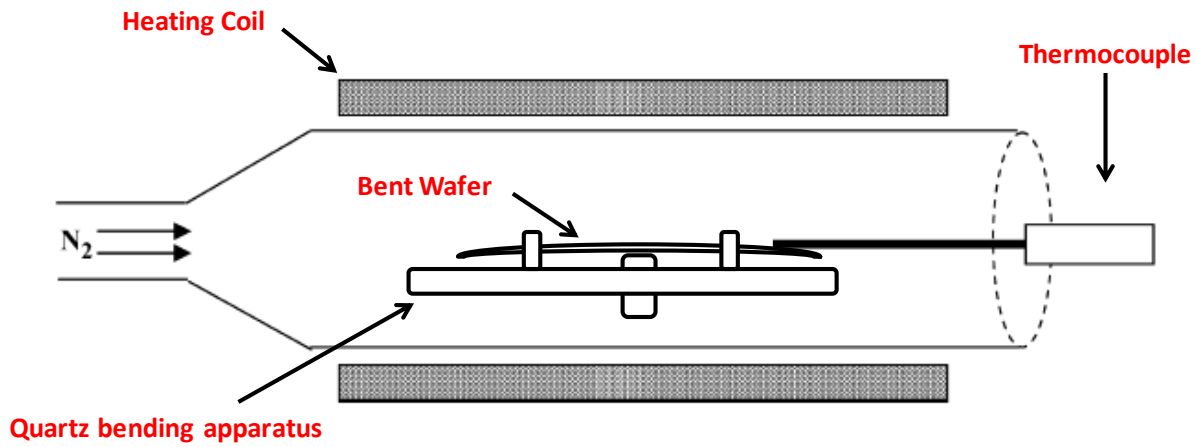
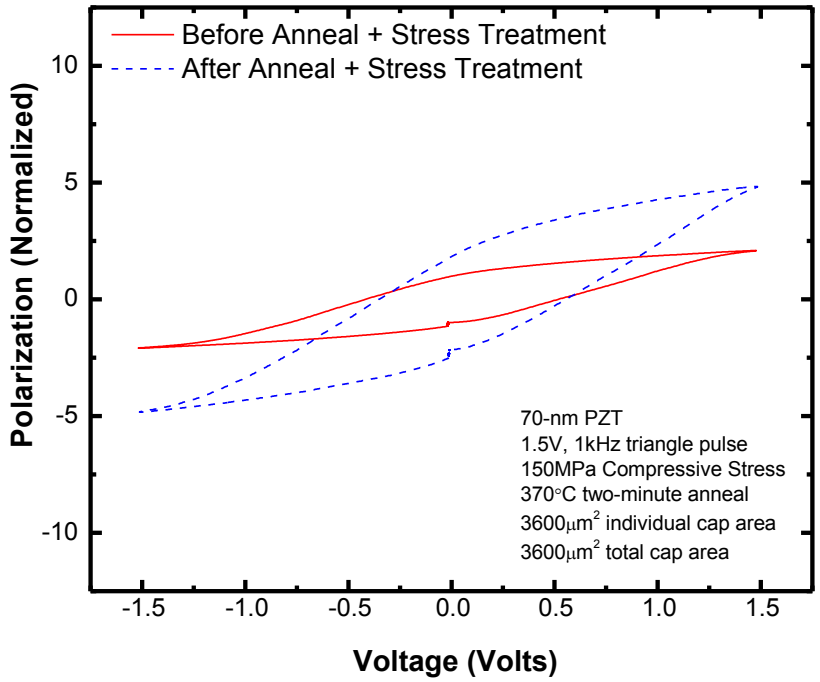


Figure 5-2. Schematic of experiment set-up used for applying stress at elevated temperature to PZT thin film capacitors. [Reprinted with permission from the University of Florida.]

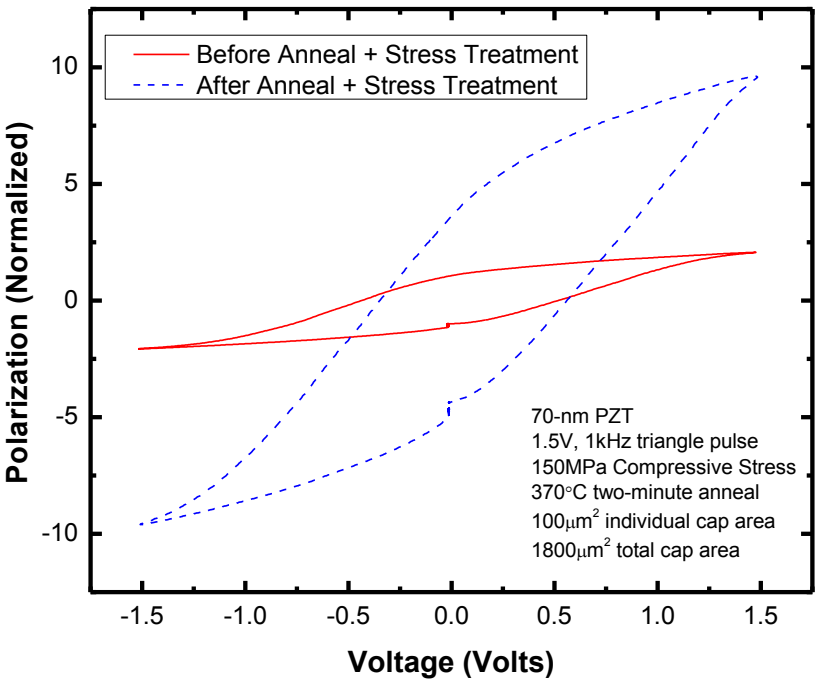
5.3 Results and Analysis

The normalized hysteresis loops before and after the stress and temperature treatment is shown for two different DUTs in Figure 5-3. Figure 5-3A shows the data for a 3600μm^2 capacitor. The anneal temperature was 370°C, which is lower than the Curie temperature of 430°C for these PZT films. An increase in P_r of 100% was observed after the treatment with negligible change in the coercive voltages. Similar changes were observed in P_{sw} calculated from PUND measurements.

A larger increase in polarization was observed for the 100μm^2 DUT, as shown in Figure 5-3B. P_r increased by 285% and any changes in the coercive voltages were negligible. This DUT was also annealed at 370°C. A similar set of DUTs was also annealed at 430°C and similar results were observed. However, these DUTs shorted shortly after the post-treatment characterization. It is possible that the high temperature in addition to the electric field affected the metal via oxidation or diffusion which led to excessive leakage current and electrical shorting the devices.



A



B

Figure 5-3. Hysteresis loops measured before and after applying a uniaxial compressive stress and annealing at 370°C for capacitors with individual area of A) 3600μm^2 and B) 100μm^2.

The results from the PUND characterization are shown in Figure 5-4. The normalized P_{sw} is plotted after the stress and high temperature anneal treatment for the two DUTs from Figure 5-3 as a function of pulse voltage, which ranged from 0.4V to 1.9V. For reference, the normalized P_{sw} is also plotted for a virgin 100μm^2 ferroelectric capacitor that did not undergo the stress and high temperature treatment. In all cases P_{sw} starts to saturate after 1.2V. For the 3600μm^2 capacitor, the P_{sw} increased by 137% at 1.5V and 149% at 1.8V when compared to the virgin capacitor. For the 100μm^2 capacitor, P_{sw} increased by approximately 400% at both 1.5V and 1.8V. These results are consistent with the polarization changes observed in the hysteresis measurement.

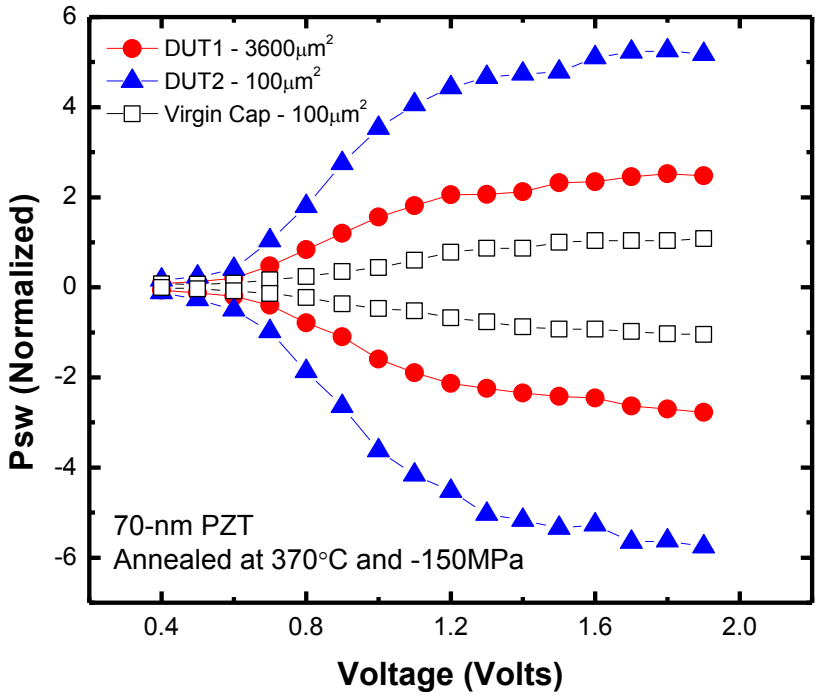


Figure 5-4. Normalized P_{sw} as a function of pulse voltage after stress and temperature anneal treatment. Data is presented for the polarization enhanced capacitors and a reference capacitor.

In order to determine if the result is repeatable and reliable, the cycling endurance of the DUTs was measured. Figure 5-5 plots the normalized P_{sw} as a function of bipolar

cycling for the polarization-enhanced 3600μm^2 ferroelectric capacitor. As can be seen, the enhanced polarization remained stable and no significant degradation was observed after cycling for 5.6x10^8 bipolar cycles. During cycling, the bipolar pulse voltage was +/- 1.5V with a frequency of 1.2MHz. PUND tests at different voltage levels before and after the cycling endurance test confirmed that there was no degradation in P_{sw}.

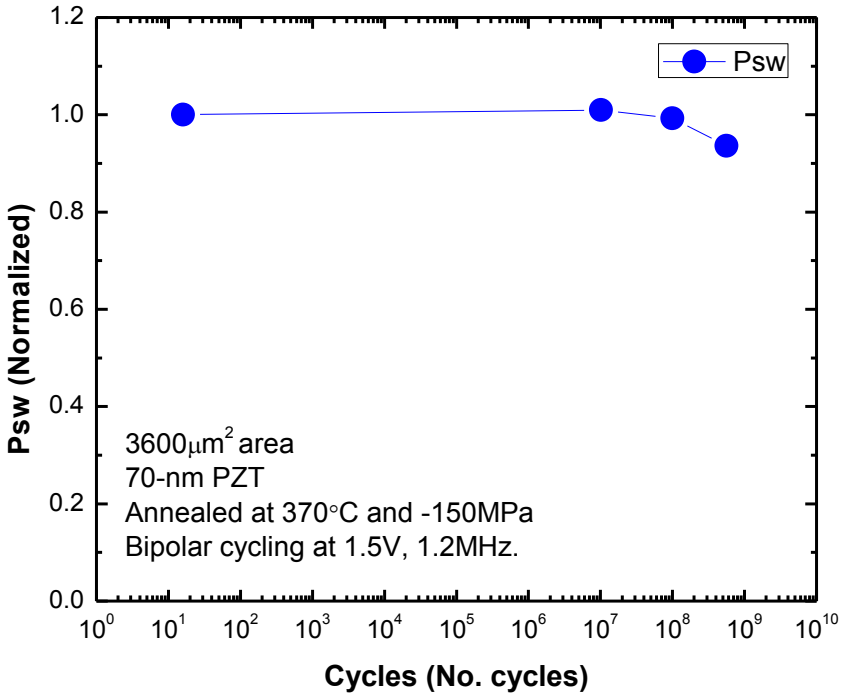


Figure 5-5. Normalized P_{sw} as a function of continuous bipolar cycling for the 3600μm^2 polarization enhanced capacitor.

The largest increase in polarization was observed in the smaller capacitors. Figure 5-6 plots the normalized hysteresis loop of a 1μm^2 ferroelectric capacitor after undergoing the stress and high temperature treatment. This particular DUT was also annealed at 370°C. An increase of over 550% in P_r was measured after the stress and temperature anneal treatment

This initial hysteresis loop is shown in Figure 5-6. However, the large increase in polarization appeared upon subsequent electrical cycling of the device as can be seen in the figure. This result indicates that applying stress at elevated temperature and then allowing the sample to cool to room temperature may activate previously inactive domains, and additional energy, in the form of electric field may required to induce this large polarization. Thus, the application of an electric field, in addition to applied stress and elevated temperature, is significant for enhancing the polarization via domain reorientation.

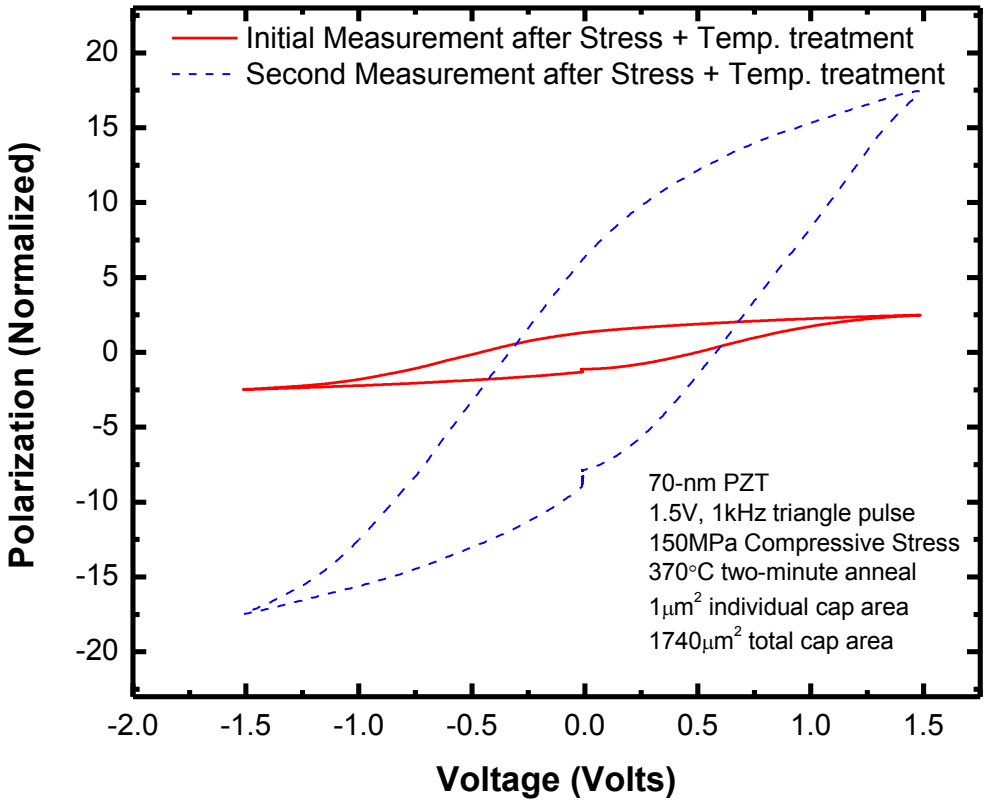


Figure 5-6. Hysteresis loop of a 1μm^2 ferroelectric capacitor showing enhanced polarization after applying stress at elevated temperature. The plot illustrates the polarization enhancement upon subsequent characterization.

The remanent polarization for the 1μm^2 capacitor from Figure 5-6 after the treatment was measured to be 75.89μC/cm^2, very similar to the experimentally and theoretically reported maximum polarization of 75μC/cm^2 [88], [90], [97], [115] . This result may indicate that the ferroelectric capacitors in this study are approaching single domain behavior. An explanation of the physics and proposed model are presented in the following section.

It should be noted that this experiment was subsequently performed on even smaller capacitors (0.4μm^2) that are actually used in FRAM circuits. Similar trends were observed as with the larger capacitors, however they did show higher leakage current levels.

5.4 Discussion

Leakage current levels of the polarization-enhanced capacitors were measured to confirm that the observed increase in polarization was not due to increased leakage current. No significant change in the leakage current was observed. The measurement polarization values also remained stable after repeated testing at room temperature. The devices were also measured on different set-ups to rule out measurement error. The result was also repeated on several wafer samples indicating that the result was not a coincidence.

The observed phenomena from this study seem to indicate that the ferroelectric capacitors approached single domain behavior after a high temperature anneal while under compressive stress. The results are consistent with the transformation stress concept proposed by Tuttle and co-authors [13], which states that the domain orientation of the film can be controlled by applying a certain stress as the film is cooled through the Curie point. In this study, the large change in polarization was observed

only when the anneal temperature was at or slightly below the Curie temperature, T_c, for the PZT composition in these films, which is 430°C for bulk PZT [48], [99]. However, as indicated by Rodriguez *et al.,* T_c in the thin films used in this study may be somewhat below 400°C [83]. It may also be possible that the applied stress in this work shifted the Curie temperature [125]. No polarization enhancement was observed when the experiment was conducted at anneal temperatures below 350°C. These factors can be used to further validate the transformation stress concept proposed by Tuttle *et al.*

A qualitative model is proposed to explain the observed results. To help illustrate this model at the microscopic level, consider the schematic shown in Figure 5-7. Before applying any thermal or mechanical stimuli each lattice in the thin film can be polarized in one of the 6 possible crystal orientations of a tetragonal structure. As an example, consider the four different lattice orientations for a PZT tetragonal shown in Figure 5-7. For simplicity, assume that these are all neighboring lattices in a PZT thin film. At a temperature well below the Curie temperature, a dipole will be present in each lattice. As the temperature is increased, the asymmetry in the crystal will decrease as the Zr/Ti ion will move toward the center of the crystal, decreasing the tetragonality of the crystal. This will decrease the dipole created by the displacement of the Zr/Ti ion relative to the O^2 ions. Once the Curie temperature is reached, each lattice will become cubic and lose its tetragonality, as shown in Figure 5-7A. There will be no dipole and no net polarization as a result. However, as the sample is cooled from T_c, it will once again become tetragonal and regain its ferroelectricity.

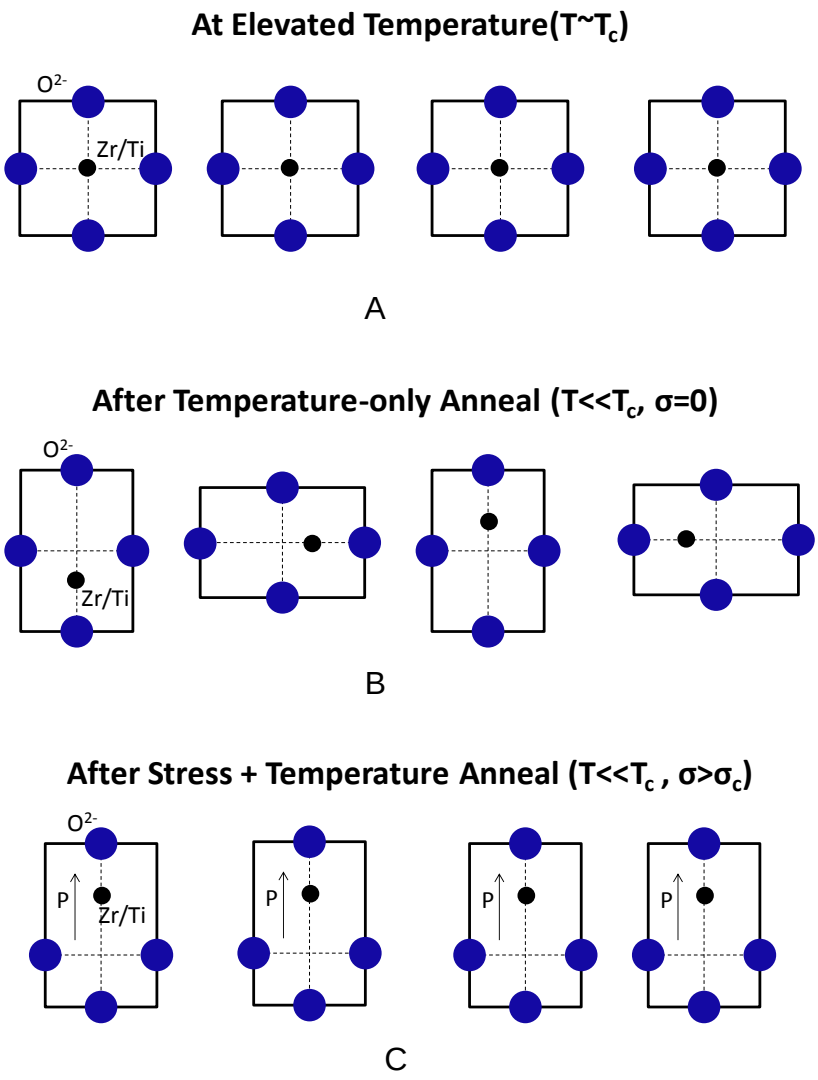


Figure 5-7. Hypothetical example of four different crystal lattice polarizations A) at the Curie temperature, T_c, B) after cooling down from T_c with no external stress, and C) after cooling down from T_c while under a compressive stress (proposed model).

Once the ambient temperature is well below T_c (for example, room temperature), each lattice will once again be oriented in one of the allowable crystal directions. In the absence of an external stimulus this orientation will be random. The ion will settle into the more energetically favored state. This is illustrated in Figure 5-7B, where the film is cooled down from the Curie temperature under no external stress (or electric field).

With no external influence, there will be six energetically equal states for the ion and so it will randomly settle into one of these states.

However, if the film is under a compressive stress as the sample is cooled from the Curie temperature, there will be a preferred orientation state as the compressive stress will alter the energy landscape and force the central ion into an energetically preferred state. This is shown in Figure 5-7C where all four lattices are polarized along the same crystal direction due to the influence of the compressive stress. This will increase the local polarization in the film. Macroscopically, this will lead to an increase in domain size.

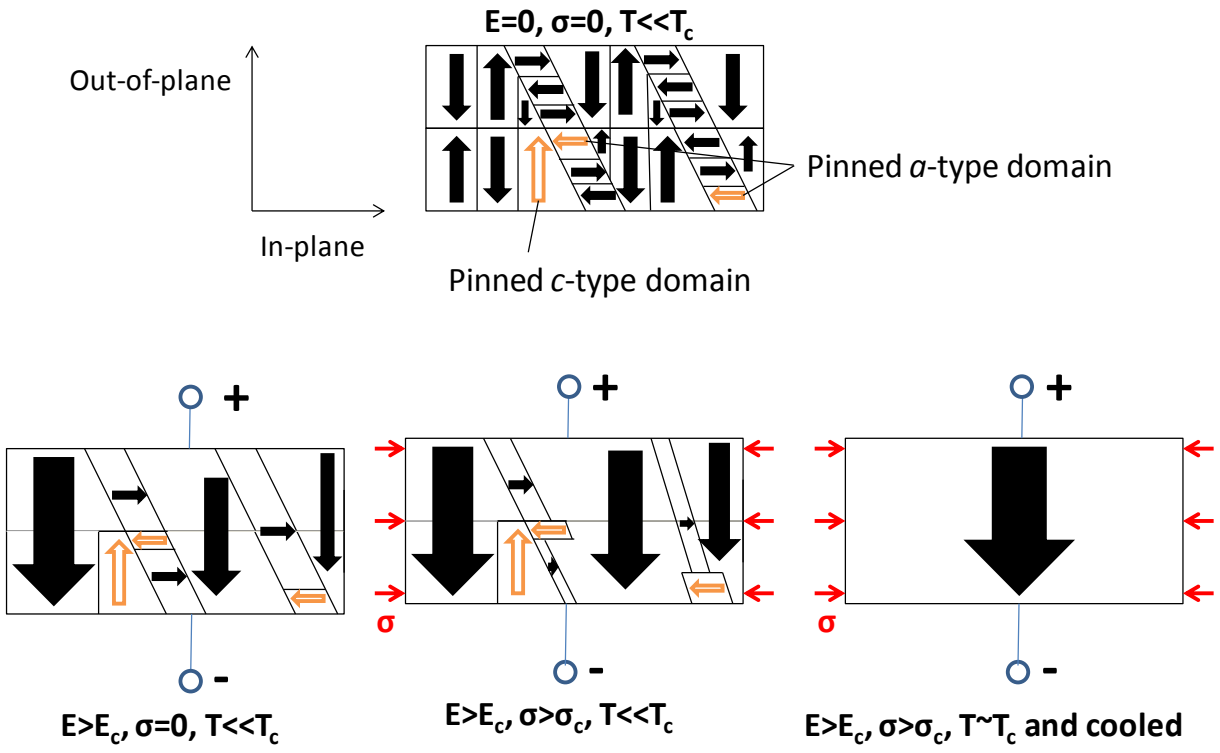


Figure 5-8. Qualitative model of the proposed macroscopic effects of annealing a ferroelectric film at T=~T_c while under a uniaxial compressive stress.

Figure 5-8 illustrates the proposed model at the macroscopic level. Initially, under no external stimuli and at a temperature well below T_c, a ferroelectric tetragonal thin film will contain many randomly oriented domains resulting in 180° and 90° domain walls. Some of those domains will be pinned, as indicated in the figure. For simplicity, assume that an electric field will not cause 90°domain wall mobility. The net polarization in this structure will initially be zero due to the randomly polarized domains. Upon the application of an electric field above the coercive field most of the 180° domain walls will be eliminated, as shown in the figure, and a net polarization will be present. However, the pinned domains will remain pinned and not reorient or switch under the influence of the electric field. Application of a compressive stress perpendicular to the electric field will cause 90° domain wall mobility, reducing the volume fraction of *a*-type domains and increasing the volume fraction of *c*-type domains. This will cause a larger polarization in the film compared to applying only an electric field. However, some 90° domains and all of the pinned domains will still remain in the film, so the total polarization possible is not being utilized.

Upon application of a high temperature, the model proposes that previously pinned domains become unpinned and the mobility of 90° domain walls increases. This is due to redistribution of defects and oxygen vacancies present in the thin film. Thus, previously inactive domains become active and can participate in the polarization switching process. As the film is cooled from high temperature, these newly active domains will orient preferentially due to the presence of a compressive stress. This will result in an enhanced polarization in the film.

Annealing the film to a high temperature approaching the Curie point and then allowing it to cool essentially “freezes in” the domain structure present as the temperature is reduced. Since the sample is under a compressive stress the domains will orient preferentially rather than randomly. A similar model has been used to explain the enhanced polarization of PZT thin films that were electrically poled at elevated temperature [111]. In this case the film was under the influence of an electric field rather than a compressive stress as the film was cooled down. The redistribution of defects can be observed by a shift in the hysteresis loop along the voltage axis. The charged defects were redistributed preferentially along the film-electrode interface due to the elevated temperature, which increased the mobility of the defects and oxygen vacancies as well [111], [126]. This effect was observed in DUTs that did not produce a large polarization increase.

While the experimental findings can be qualitatively explained, a quantitative validation of the observed results is recommended. X-ray diffraction experiments can be used to validate the proposed model. Development of a thermodynamic model is also recommended as future work.

5.5 Summary and Conclusions

The effects of compressive stress at elevated temperature on CMOS-embedded PZT thin film capacitors were experimentally investigated. The ferroelectric capacitors were annealed at temperatures approaching the Curie temperature and allowed to cool while under an applied uniaxial compressive stress. Increases over 100% and 200% in the remanent polarization were observed for individual capacitor areas of 3600μm^2 and 100μm^2, respectively. An increase in the remanent polarization over 550% was observed for an individual capacitor area of 1μm^2. The change in polarization was

stable and remained through subsequent testing and continuous bipolar cycling. Switching polarization calculated using the PUND method as a function of pulse voltage showed similar increases in the polarization. The leakage current levels were not significantly changed as a function of this stress and temperature treatment although electrical shorts were observed in some devices.

These observed results are consistent with a previously proposed model by Tuttle *et al.*[13], where the stress of the film as it is cooled through the Curie point determines the orientation of the domains. These results indicate that the ferroelectric capacitors may be approaching single domain behavior. A qualitative model was proposed to describe the observed phenomena. It is theorized that annealing the sample at a temperature at or near the Curie point of the film activates previously dormant domains. As the sample is cooled, the compressive stress will preferentially orient these domains In the *c*-direction, resulting in the large polarization increase. X-ray diffraction experiments and quantitative modeling is recommended for further validation of the observed results.

CHAPTER 6
COMBINED EFFECTS OF STRESS, TEMPERATURE, AND ELECTRIC FIELD ON CMOS-INTEGRATED PZT THIN-FILM FERROELECTRIC CAPACITORS

The effects of mechanical stress at room temperature and at elevated temperature were experimentally investigated and reported in the previous chapters. While applying uniaxial compressive stress at room temperature showed incremental increases in remanent and switching polarization (3.37% and 3.24% per 100MPa, respectively), application of stress while cooling the sample from a temperature at or near the Curie point induced remanent polarization changes well over 100%. However, inducing this level of polarization enhancement required annealing the sample at a temperature at or slowly below the Curie temperature. Applying these temperature levels to a ferroelectric capacitor embedded within a CMOS process may damage some of the surrounding structures. The ferroelectric capacitors may also short at these high temperatures, as was observed in some experiments. From a manufacturing point of view it may be impractical to apply this temperature level as part of a standard CMOS process.

Electric field and temperature have been traditionally used to pole ferroelectric materials. Recently, a mechanical stress has also been used to assist the electrical poling of bulk ferroelectric materials. However, work on stress-assisted poling has been limited in thin films. In addition, to the best knowledge of the author, the combined effects of the three factors of mechanical stress, temperature, and electric field have not been investigated in ferroelectric thin film capacitors. This work investigated the effects of mechanical stress and electric field on the poling of ferroelectric thin film capacitors as well is the combined effects of mechanical stress, temperature, and electric field.

Further scaling of current FRAM technology can increase the storage density and reduce manufacturing costs, which can lead to new markets and applications.

However, geometric scaling will cause ferroelectric capacitors to decrease their polarization. This in turn will degrade the FRAM signal margin. As a result, alternate methods to scale the technology to future technology nodes are needed. Electrically poling thin film ferroelectric capacitors using mechanical stress and/or elevated temperature and electric field can be used as a means to feasibly and effectively enhance the polarization.

A brief background on the poling of ferroelectric materials is first given. This includes electrically poling with a mechanical stress and electrically poling at an elevated temperature. The experimental details and methods used to electrically pole ferroelectric thin film capacitors at stress and elevated temperature are then described. This is followed by a reporting of the results and analysis. A discussion of the physics and explanation of the observed results is then presented. Finally, the chapter ends by summarizing present work and offering key conclusions.

6.1 Background

Electric field and temperature have been traditionally used as a means of enhancing the polarization in ferroelectric materials [48], [103], [104], [106], [108–112]. When an electric field is applied to an un-poled ferroelectric material, the domains will attempt to reorient into an allowable polarization state that is closest to the direction of the electric field. Both 180° and 90° domain reorientations can occur in tetragonal PZT [109]. This causes an increase in the volume fraction of *c*-type domains in the material and an increase in the polarization as a result.

An interesting result on repeated poling was observed by Kohli *et al* [111]. They poled ferroelectric thin films by applying an AC and DC electric field at room temperature and by applying a DC field at high temperature. It was found that applying

a high DC field at room temperature did not induce 90° domain switching, while application of consecutive bipolar pulses for an extended period of time did significantly decrease the volume fraction of 90° domains in thin films. They concluded that pulse poling repeatedly forces a domain wall to move by redistribution of the defects, and therefore domains may become unpinned [111]. Similar observations were made by Khalack and Lotev [127]. Kohli and co-authors also observed that a high DC field at elevated temperature had similar results to bipolar pulse poling at room temperature [111]. This was also attributed to the re-arranging of defects at high temperature. They theorize that upon cooling the domain pattern "freezes in", whether this pattern is random or preferentially oriented due to the applied electric field. The temperature range for this effect to take place was reported as 100-200°C [111].

Kamel and de With also explored temperature as a means of releasing pinned domain walls in PZT ceramics [108]. Samples were poled at 70°C, 90°C, and 100°C. The electric field was held constant as the temperature was removed and the sample was allowed to cool back down to room temperature. They also observed enhanced polarization using this poling procedure and concluded that domain walls become unpinned in a ferroelectric material after quenching from a high temperature while under the application of an electric field. This was attributed to the decrease of defects in the material at high temperature. With reduced defects, the domains can then be easily reoriented if an external field is applied [108].

Kholkin *et al.* [110], studied the effects of poling at elevated temperature on PZT thin films with similar results as Ref. [106] and [109]. The films were electrically poled at temperatures up to 150°C. They attributed their observed results to the buildup of an

electric field at high temperature, caused by trapping of electronic charge carriers at defect sites near the interface of the film and electrode [110], [126]. These traps stabilize the polarization achieved at high temperatures.

A recent effort was reported by Noda *et al.* where an electric field was applied during an anneal of the film as part of the fabrication process [103]. They observed a domain orientation in the (001) direction of 75.6% using their electric field annealing (EFA) method compared to a 19.8% (001) domain orientation when an electric field is not used during annealing of the thin films. They attributed this to an intrinsic epitaxial growth from original (001) oriented grains in the seed layer of the PZT film [103].

A mechanical stress has also been used to assist in electrical poling of ferroelectric materials. Berlincourt and Krueger were the first to show that application of a compressive stress to PZT ceramics reorients 90° domains, causing a change in the polarization compared to when the materials are only poled with an electric field [109].

Granzow *et al* [21], [118–121]., have recently studied the effects of mechanical stress during poling of PZT ceramics. They reported that application of compressive stress will cause 90° domain switching away from the direction of the applied stress. Thus, applying a stress parallel to the poling direction will decrease the polarization while applying a compressive stress perpendicular to the poling direction will increase the polarization. Similar experiments and observations where made by Suchanicz *et al* [101], [102]. Energy based models are used to explain these effects and will be discussed later in the chapter.

Previous work has shown that both temperature and stress can have a significant influence on the poling properties of PZT ferroelectric materials. While mechanical

stress has been used to assist in the poling process of PZT ceramics, similar work has been very limited in PZT thin films. This work experimentally investigated the stress effects in CMOS-embedded PZT thin films during electrical poling processes. In addition, methods have been proposed for enhancing the polarization of PZT thin films by poling the capacitors at elevated temperature [106]. However, no work has been reported on the combined effects of mechanical stress, temperature, and electric field on PZT thin films up until now. These combined effects were also investigated in this work. Experiment details, results, and a discussion of the physics are reported in the remainder of this chapter.

6.2 Experiment Details

6.2.1 Stress-Assisted Poling

The capacitors tested in this study were metal-ferroelectric-metal capacitors with 70nm thick PZT thin films. The individual capacitor area was 0.4μm^2 with a total capacitor area of 1581 μm^2, thus the DUT is an array of 4,942 capacitors. These devices were fabricated on a standard 130-nm CMOS technology process. More details on the process technology and device structure can be found in Ref.[1], [4].

The procedure for poling and characterizing the devices was as follows: The wafer sample was placed in the 4-point bending flexure apparatus and the desired stress was applied to the sample. Devices were poled at uniaxial compressive stresses of 0MPa, -75MPa, -120MPa, and -152MPa. Once under stress, the devices were electrically poled. The poling was done with bipolar triangular pulses at a frequency of 100kHz. At each stress level, different devices were poled at bipolar peak amplitudes of +/-1.26V, +/- 1.5V, +/-1.8V, and +/-2.1V. It should be noted that these capacitors are rated to operate at 1.5V. The devices were electrically poled at the desired stress for a

duration of 10 minutes. After poling, the sample was characterized while under stress. The switching polarization was extracted using the PUND method. The sample was then removed from the flexure apparatus and characterized again at no externally applied mechanical stress. The samples were then re-poled under the same conditions at no applied stress and a second characterization was done after this second re-poling.

6.2.2 Stress and Temperature Assisted Poling

The capacitors tested in this study were metal-ferroelectric-metal capacitors with 70nm thick PZT thin films. The capacitor area was 3600μm^2. These devices were fabricated on a standard 130-nm CMOS technology process. More details on the process technology and device structure can be found in Ref.[1], [4].

For this experiment, the wafer sample was first placed in the four-point bending flexure apparatus. A uniaxial compressive stress of -148MPa was then applied to the sample. Once at the stress, a bipolar electric pulse of +/-1.5V at 100kHz was continuously applied. A temperature of 205°C was then applied to the sample using a heat gun. Once the temperature stabilized, it was left for 10 minutes. The temperature was then removed, and the sample was allowed to cool to room temperature while still under the influence of an applied electric field and -148MPa uniaxial compressive stress. At 40°C, the electric field was removed and the sample was characterized while still at -148MPa. The sample was then removed from the flexure apparatus and once again characterized at room temperature and 0MPa of externally applied stress. The temperature was monitored using a surface-mount resistance temperature detector (RTD) from OMEGA Engineering (model no. SA1-RTD) [124]. The RTD was mounted on the center of the bottom surface of the sample.

In both sets of experiments described above, the applied stress was measured using a uniaxial strain gage mounted to the surface of the wafer sample. The strain gage was an OMEGA transducer quality strain gage (model no. SGT-1/350-TY11)[124]. The stress is measured by monitoring the change in resistance as a function of stress. Dividing this change in resistance by the gage factor of the strain gage (1.99) gives the strain, and, using the Young's Modulus of silicon, the stress can then be calculated. The Young's Modulus of the silicon wafer substrate used in these devices (<110> (100) orientation) is 169GPa [128].

6.3 Results and Analysis

6.3.1 Stress-Assisted Poling

The effects of electric field only as a function of bipolar pulse voltage poling are shown in Figure 6-1. The capacitors were poled at room temperature and no external mechanical stress was applied. It is evident that an electric field by itself has a strong influence on the remanent polarization. As can be observed from the error bars, the uncertainty in the measurement is larger at the lower pulse voltage (+/-1.26V). This supports the model that a given threshold energy is required to switch a majority of the domains in the film from Hwang and co-workers [67] . A +/-1.26V voltage pulse alone does not contain enough energy to surpass this threshold energy. Below this threshold energy only the tail of the distribution of domains is expected to switch.

The effects of mechanical stress on the poling process are illustrated in Figure 6-2. The normalized P_{sw} as a function of bipolar pulse poling voltage is shown at different applied mechanical stresses. P_{sw} was measured while the sample was at the indicated stress level. It is observed that an applied compressive stress during electrical poling of the devices at room temperature incrementally enhances the polarization.

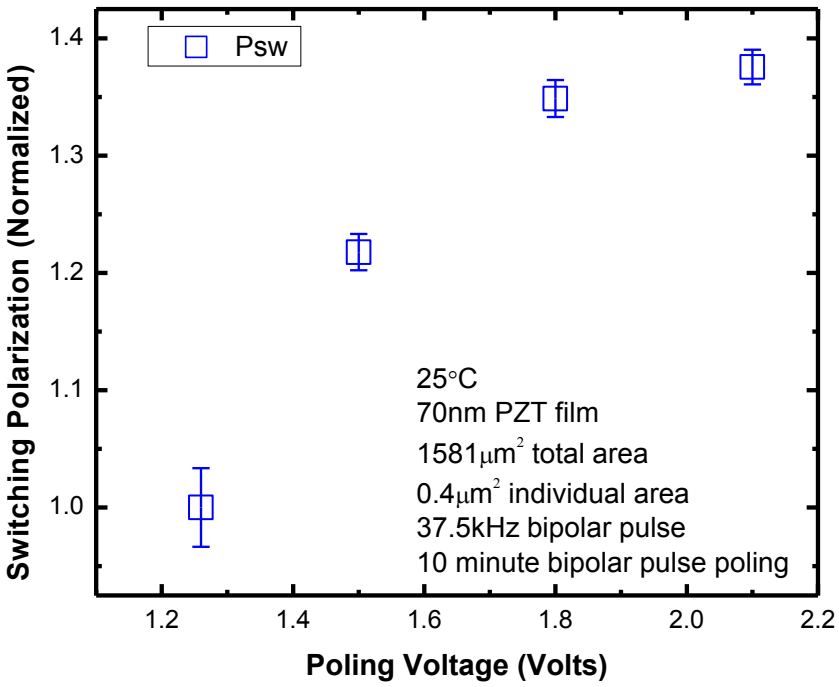


Figure 6-1. Switching polarization in PZT thin film capacitors as a function of bipolar pulse poling voltage at room temperature and no externally applied stress.

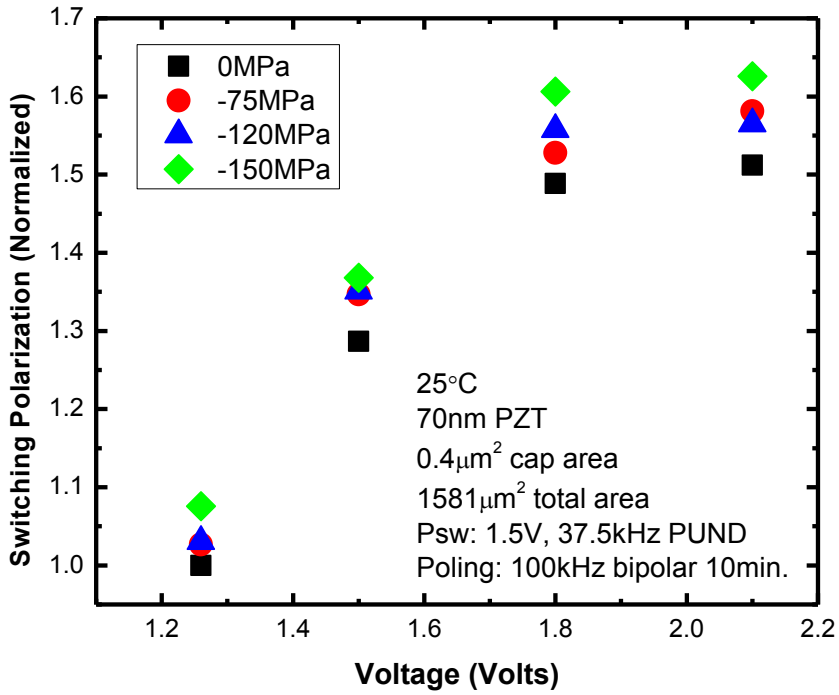


Figure 6-2. Switching polarization in PZT thin film capacitors as a function of bipolar pulse poling voltage at various levels of applied compressive stress.

The increase in P_{sw} is smaller at the lower poling voltages (1.2V and 1.5V). This may be due to the total energy being below the critical energy required to switch active domains at these electric field and stress levels. Below the critical energy, there will be a distribution of domains which are switched at different energies. Up to an 8% change in P_{sw} was observed when applying a -152MPa compressive stress during the poling process at 1.8V. It can also be observed that P_{sw} appears to saturate after 1.8V. This may be an indication that the required threshold energy has been reached, at which point a majority of the switchable active domains have been reoriented in the direction of the electric field.

An interesting result can be seen in Figure 6-3 in the effect of removing the stress and repoling. The figure plots three switching polarization versus poling voltage curves: (1) P_{sw} at -152MPa after the initial poling, (2) P_{sw} after the stress was removed, and (3) P_{sw} after the sample was re-poled at 0MPa. After the stress is removed, P_{sw} appears to relax to the levels observed when the sample is poled with only a bipolar electric field (no externally applied mechanical stress). However, a portion of the switching polarization was regained after the sample was re-poled. A similar result was observed in [120]. In order to confirm that the increase in P_{sw} due to re-poling was only due to stress, DUTs that were initially poled at 0MPa were re-poled again at 0MPa. These results are shown in Figure 6-4. There was no change in the switching polarization of these DUTs after the second re-poling. These results support the notion that stress can be used to permanently enhance P_{sw} and that poling with stress may unpin some domains which subsequently switch with a second poling step.

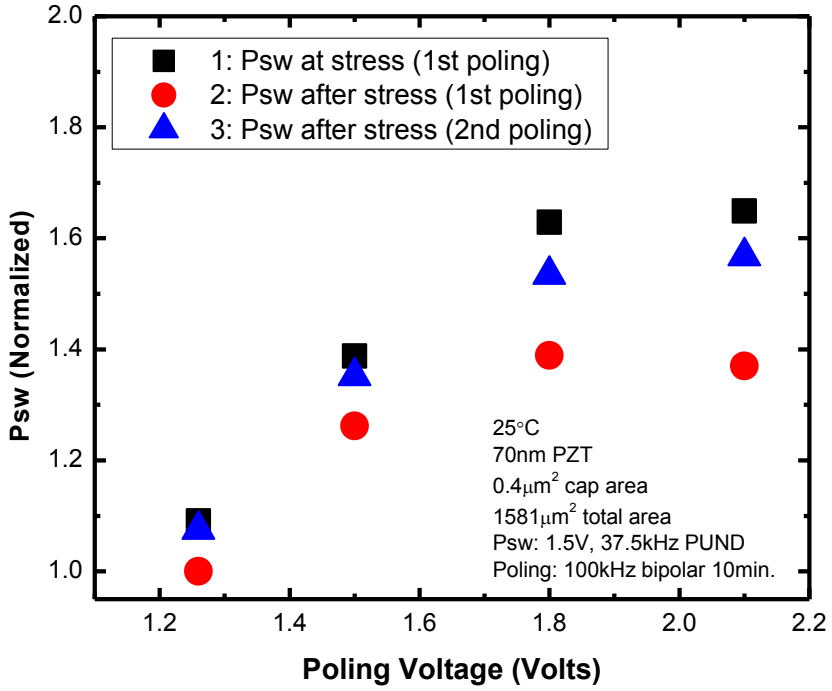


Figure 6-3. Normalized switching polarization after electrically poling device at -152MPa.

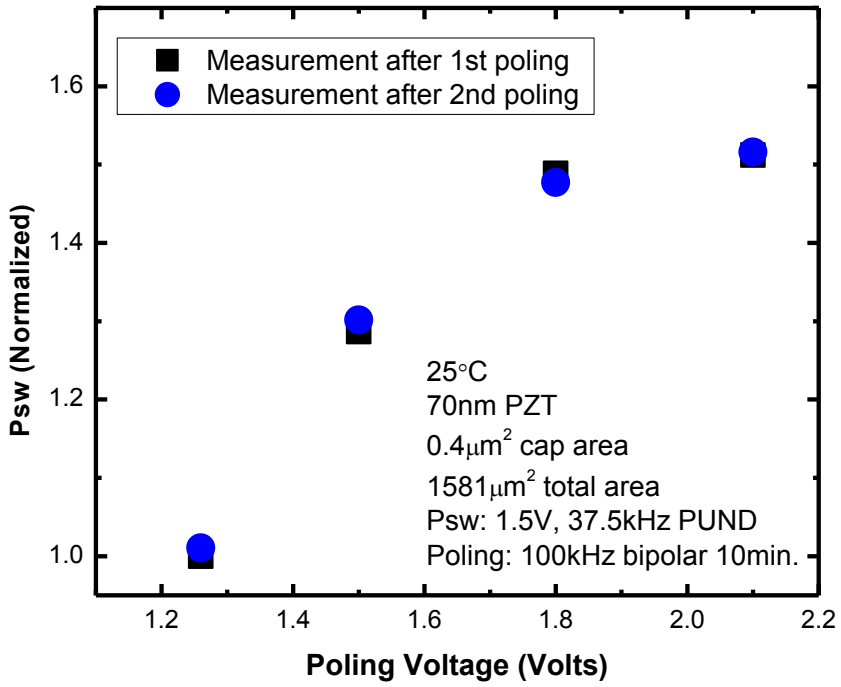


Figure 6-4. Normalized switching polarization after re-poling devices that were initially poled at 0MPa at room temperature.

Figure 6-5 shows the change in switching polarization after the second re-poling for DUTs initially poled at 0MPa and -152MPa. An applied compressive stress permanently enhanced the switching polarization for all poling voltages. An increase in P_{sw} of 2-4% was observed, well beyond the uncertainty in the measurement which was calculated to be less than 1%.

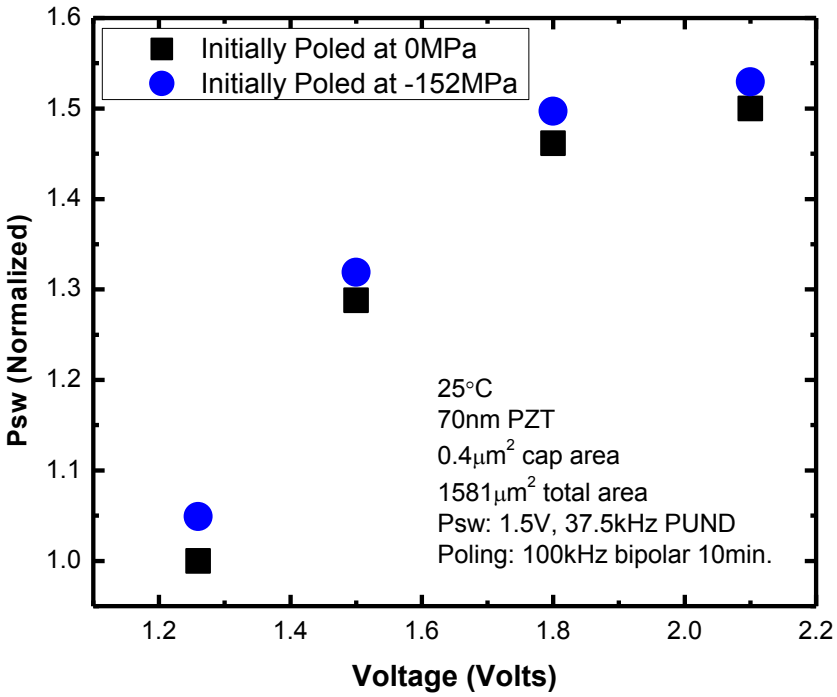


Figure 6-5. Normalized switching polarization after re-poling devices that were initially poled at -152MPa and 0MPa.

6.3.2 Stress and Temperature Assisted Poling

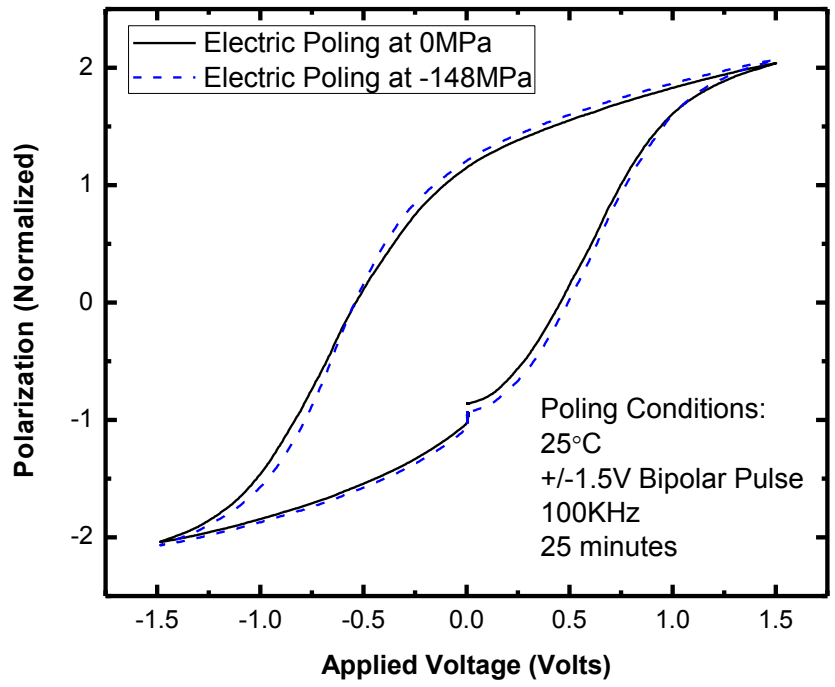
The effects of adding temperature in addition to mechanical stress to the electrical poling process can be observed in Figure 6-6. Figure 6-6A compares the hysteresis loop of two similar DUTs. One DUT was electrically poled with a bipolar pulse voltage only while the other DUT was poled with both an electric bipolar pulse voltage and an applied compressive stress of -148MPa. Both DUTs were poled at room temperature.

It can be seen that poling while at a compressive stress of -148MPa increased the remanent polarization by 4.7%.

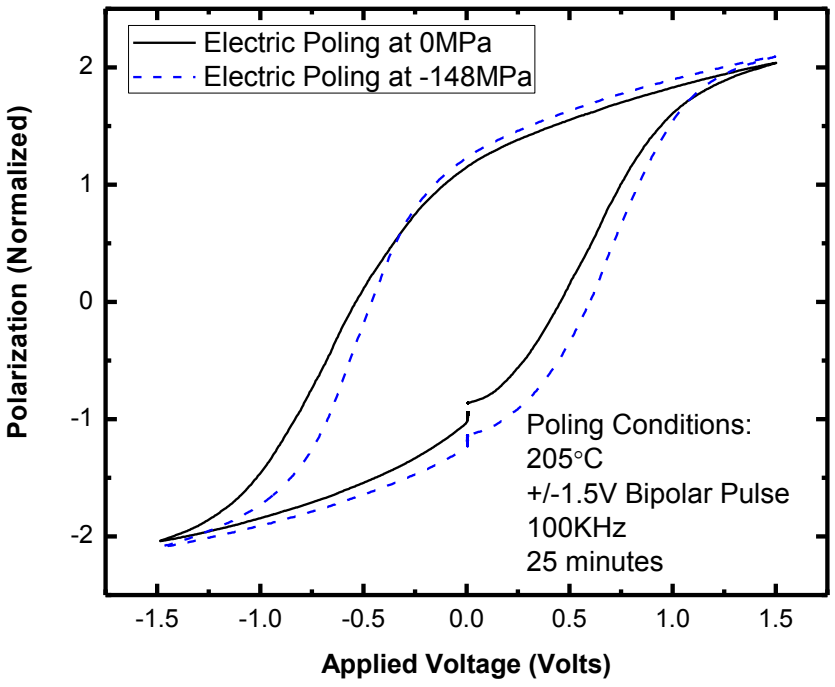
In contrast, when a DUT is electrically poled with both an applied compressive stress and elevated temperature (205°C) a 13.6% change in the remanent polarization was observed. This result can is shown in Figure 6-6B. A shift in the hysteresis loop along the voltage axis can also be observed in Figure 6-6B. This voltage shift is a result of poling at elevated temperature [110], [111], [126]. An elevated temperature may cause a redistribution or decrease of defects and oxygen vacancies in the ferroelectric thin film [110], [111], [126]. These defects will “freeze-in” upon cooling to room temperature [111]. This voltage shift may induce imprint in the ferroelectric capacitor, causing the capacitor to prefer one polarization state over the other [83], [111].

6.4 Discussion

The results indicate that stress and temperature can be used to assist in the electrically poling of ferroelectric capacitors. A mechanical compressive stress enhances the switching polarization when compared to electric field-only poling. Combining stress and elevated temperature during the poling process enhances the switching polarization even further. In our devices, electrically poling using a bipolar pulse voltage was found to enhance the polarization at room temperature, while electric poling with a 1.5V DC voltage under similar conditions showed negligible change in the switching polarization. This result is consistent with what has been reported in Ref. [111].



A



B

Figure 6-6. Mechanical stress effects on the bipolar voltage pulse poling of ferroelectric thin film capacitors at A) room temperature and B) 205°C.

An energy-based model, first suggested by Hwang and co-workers [67], is used to explain the observed behavior. In this model a critical energy is required to switch both 180° and 90° domains. This energy can be introduced by an electric field or mechanical stress, or both. It can be generally described as

$$W_M + W_E \geq W_S \,, \tag{6-1}$$

where W_M is the mechanical work done on the system, W_E is the electrical energy work done, and W_S is the energy required to switch the domains.

The electrical work can be defined as

$$W_E = \int E \cdot dD \,, \tag{6-2}$$

where E is the electric field and D is the electric displacement. The work required for 180° domain switching is given by [67]

$$W_E = 2P^0 E_0 \,, \tag{6-3}$$

where P^0 and E_0 represent the spontaneous polarization and coercive electric field, respectively. Thus, the requirement for 180° switching of a given domain or grain, i, becomes [67]

$$E_i \Delta P_i \geq 2P^0 E_0 \,. \tag{6-4}$$

A similar approach is used to derive the mechanical work needed to induce 90° domain switching at the lattice level. The general equation for mechanical work is

$$W_M = \int \sigma \cdot d\varepsilon \,, \tag{6-5}$$

with σ and ε referring to the stress and strain, respectively. Similar to 180° switching, the mechanical work required for 90° switching is [67]

$$W_M = 2P^0 E_0 \,. \tag{6-6}$$

The mechanical energy required for 90° switching at the grain lattice level then becomes [67]

$$\sigma_{ij}\Delta\varepsilon_{ij} \geq 2P^0E_0, \tag{6-7}$$

where σ_{ij} is the applied stress on the grain or domain and $\Delta\varepsilon_{ij}$ is the change in the strain of this grain due to the applied stress.

Combining Eqs. 6-4 and 6-7, the total energy required to induce 90° and 180° domain switching for a given domain can be represented as [67]

$$E_i\Delta P_i + \sigma_{ij}\Delta\varepsilon_{ij} \geq 2P^0E_0. \tag{6-8}$$

Using the above equations and Preisach modeling methods, Hwang *et al.,* calculated the energy of each grain and then averaged the energy over the entire sample to simulate the macroscopic polarization in the film as a function of applied stress and electric field [67]. Their simulated results fit their experiment results quite well [67], [114].

One drawback of the model developed by Hwang *et al.* is that they assumed that the same energy is required to switch both 180° and 90° domains. This assumption was proven to be incorrect by Granzow and co-authors [118]. They experimentally observed that the order in which stress and electric field are applied during the poling process influences the degree of polarization enhancement. Applying an electric field first and then applying a compressive stress was found to enhance the polarization more than applying the stress first followed by the electric field [21], [118].

A two-step switching model was then proposed to explain these results [129], [130] . In this model, a different energy is required to switch 180° and 90° domains. The energy required for 90° switching remains the same as in the model above.

However, 180° switching takes place in two successive 90° switching steps. Eq. 6-8 becomes [130]

$$E_i \Delta P_i + \sigma_{ij} \Delta \varepsilon_{ij} \geq E_{90}, \tag{6-9}$$

where E_{90} is the required energy for 90° switching. Any excess energy from the first switching step is stored as a potential energy and released during the second energy step. Thus, all switching takes place in 90° switching steps.

If electric field is applied initially, enough energy will be supplied to switch 180° domains and some 90° domains. Any 90° domains not switched initially will be switched upon the application of the mechanical stress. If a mechanical stress is first applied, 90° domains will switch. However, in the absence of an electric field, they will switch randomly into one of the four allowable neighboring polarization states. In the case that a domain is initially polarized in the direction of the electric field, application of a compressive stress may cause 90° switching of this domain. The subsequent application of an electric field will not contain enough energy to switch this domain back to its original polarization state.

The results observed in this work validate this energy-based model. As previously mentioned, at low poling voltages, there is a large spread in P_{sw} for different capacitors due to a large distribution of domains below the macroscopic critical energy. The fact that there is a small change in the P_{sw} at poling voltages of 1.8V and 2.1V indicates that the critical energy has been surpassed at 1.8V and most of the available active domains have been switched.

A similar model is used to qualitatively describe the combined effects of stress, temperature and electric field as was described in Chapter 5 to describe the effects of

stress at elevated temperature. When ferroelectric thin film capacitors are electrically poled at an applied compressive stress, enough energy is supplied to switch more 90° domains than if the capacitors are only poled using an electric field. However, there will still be 90° domains that do not switch because of domain pinning. As has been previously discussed, increasing the ambient temperature of a ferroelectric thin film may decrease or redistribute defects and oxygen vacancies in the film. This will increase the mobility of 90° domain walls by releasing previously pinned domains and thus allow them to participate in the switching polarization. As the film is quenched from high temperature, the domain pattern that is present will “freeze in”. Since the ferroelectric film is under the influence of both an electric field and compressive stress, the domains will be preferentially oriented as the film is cooled to room temperature. If no external stimuli are present during the quenching of the film, the domains will randomly orient and there will be no net polarization when the film reaches room temperature. Similar models have been proposed by Kohli [111] and Kamel [108]. They theorize that the presence of an electric field as the film is quenched will preferentially orient all the active domains in the film, including previously pinned domains that were un-pinned by the temperature anneal. However, in their work there was no compressive stress applied. The uniqueness of this work is that a compressive stress was applied during this poling process, which increased the supplied energy into the system and as a result the reorientation of 90° domains was also increased.

As part of this study, a similar experiment was conducted at a lower compressive stress of -96MPa. At this stress level, there was no observed permanent change in the switching polarization, even after the second re-poling of the capacitors. In comparison,

the capacitors that were electrically poled at -152MPa of applied stress once temperature was introduced into the poling process did not need to be re-poled at room temperature and 0MPa of external stress in order to induce a permanent increase in the polarization. These observations further validate the model of a critical energy needed for domain switching.

6.5 Summary and Conclusions

The effects of mechanical stress and electric field and combined effects of mechanical stress, electric field, and elevated temperature on CMOS-embedded PZT thin film capacitors were investigated. The results showed that applying a stress during the electrical poling of the ferroelectric thin films enhanced the switching polarization. Applying a compressive stress of -148MPa at room temperature during poling increased the remanent polarization by 4.7%. However, when elevated temperature was introduced into the poling process, the remanent polarization increased by 13.6%.

Energy based models were presented to qualitatively describe the observed results. A two-step switching model was used to describe the effects of an applied mechanical stress during the electrical poling process of the ferroelectric capacitors. This increased the energy in the system during the poling process resulting in an increased reorientation of 90° domains. Increasing the temperature during the poling process increases the mobility of 90° domain walls by releasing previously pinned domains. These newly activated domains are then available to contribute to the overall switching polarization. As the film is quenched from high temperature, the domain pattern that is present at this elevated temperature will “freeze in”. Since an electric field and mechanical stress are applied as the film is cooled to room temperature, the available domains will be preferentially reoriented.

Methods for enhancing the polarization of ferroelectric thin films are needed in order to successfully scale current FRAM technology to future technology nodes. This work showed that electric field, temperature, and mechanical stress can be used to enhance the switching and remanent polarization in ferroelectric thin films. While Chapter 5 showed that a significant increase in polarization can be induced when applying a stress and high temperature anneal treatment, the temperature applied in that work approached the Curie temperature of the material. These levels of temperature can electrically short the ferroelectric capacitors and may be difficult to implement into a standard manufacturing process.

Including an electric field into this poling process can decrease the temperature required to significantly enhance the polarization. While the polarization enhancement levels in this study were modest compared to those reported in Chapter 5, further experimentation is recommended. A temperature of 205°C and -148MPa of compressive stress were applied to the polarization-enhanced capacitors. Modest increases in the temperature and applied stress may induce an even larger change in polarization, especially when one considers that a critical energy is needed to switch all of the domains. Stress, temperature, and electric field may all be combined to supply this critical energy.

Development of a quantitative model is also recommended to further validate the observed results. In addition, XRD experiments may be used to confirm the model of increased 90° domain reorientation.

CHAPTER 7
SUMMARY AND FUTURE WORK

The results obtained from this work show that an applied mechanical stress, in combination with temperature and/or electric field, can be used to permanently and significantly enhance the switching polarization in ferroelectric thin film capacitors. Thus, it may be feasible to engineer methods to induce a polarization enhancement for the purposes of increasing FRAM signal margin that will enable scaling of FRAM to future technology nodes. Future work is recommended to study the effects of stress on reliability and to develop models for simulating the combined effects of stress, temperature, and electric field on ferroelectric thin films. X-ray diffraction studies on the ferroelectric thin films as a function of applied mechanical stress are also recommended in order to validate the proposed models.

To the best knowledge of the author, this is the first work to investigate the effects of a mechanically applied stress on PZT thin film ferroelectric capacitors embedded in a standard CMOS technology. Uniaxial mechanical compressive stress up to -240MPa was applied at room temperature using a four-point bending flexure-based apparatus and the ferroelectric properties were characterized as a function of stress. An increase in the remanent polarization of 3.37% per 100MPa was observed for ferroelectric capacitors of different areas. Increases in the maximum polarization and switching polarization (calculated from the PUND test) were also observed with compressive stress, while there was no significant change in the coercive voltage. The effect of stress on the cycling endurance of the capacitors was also characterized. Stress did not appear to accelerate degradation due to cycling fatigue.

Energy based models were given to explain the physics of the observed results. The enhanced polarization is due to increased volume fraction of *c*-type domains when stress is applied and an increase in the ratio of the *c* lattice parameter to the *a* lattice parameter. At the microscopic level, this can be explained by minimization of the Gibbs free energy and a reduction in the energy barrier required to switch an in-plane domain to an out-of-plane domain. Macroscopically, this leads to increased 90º domain wall motion.

Chapter 5 presented the effects of compressive stress at elevated temperature on CMOS-embedded PZT thin film capacitors. The ferroelectric capacitors were annealed at temperatures approaching the Curie temperature and allowed to cool while under an applied uniaxial compressive stress. Increases over 100% and 200% in the remanent polarization were observed for individual capacitor areas of 3600μm^2 and 100μm^2, respectively. An increase in the remanent polarization over 550% was observed for an individual capacitor area of 1μm^2. The change in polarization remained stable and was maintained through subsequent testing and continuous bipolar cycling. Switching polarization calculated using the PUND method as a function of pulse voltage showed similar increases in the polarization. The leakage current levels were not significantly changed as a function of this stress and temperature treatment.

A qualitative model was proposed to describe the observed phenomena which extends a previously proposed model by Tuttle *et al.*[13], where the stress of the film as it is cooled through the Curie point determines the orientation of the domains. They indicate that the ferroelectric capacitors may be approaching single domain behavior. It is theorized that annealing the sample to a temperature at or near the Curie point of the

film activates previously dormant domains. As the sample is cooled, the compressive stress will preferentially orient these domains along the direction of an applied electric field, resulting in the large polarization increase.

Finally, the effects of mechanical stress and electric field and combined effects of mechanical stress, electric field, and elevated temperature on CMOS-embedded PZT thin film capacitors were studied. The results showed that applying a stress during the electrical poling of the ferroelectric thin films enhanced the switching polarization. Applying a compressive stress of -148MPa at room temperature during poling increased the remanent polarization by 4.7%. However, when elevated temperature was introduced into the poling process the remanent polarization was further enhanced. A temperature of 205°C and -148MPa of compressive stress were applied during the poling of the ferroelectric capacitor, resulting in a 13.6% increase in remanent polarization. Modest increases in the temperature and applied stress may induce an even larger change in polarization, especially when one considers that a critical energy is needed to switch all of the domains. Stress, temperature, and electric field may all be combined to supply this critical energy

Energy based models were presented to qualitatively describe the observed results. A two-step switching model was used to describe the effects of an applied mechanical stress during the electrical poling process of the ferroelectric capacitors. This increased the energy in the system during the poling process resulting in an increased reorientation of 90° domains. Increasing the temperature during the poling process increases the mobility of 90° domain walls by releasing previously pinned domains. These newly activated domains are then available to contribute to the overall

switching polarization. As the film is quenched from high temperature, the domain pattern that is present at this elevated temperature will “freeze in”. Since an electric field and mechanical stress are applied as the film is cooled to room temperature, the available domains will preferentially reorient.

Overall this work comprehensively demonstrated that stress engineering may be potentially used in various forms to enhance the switching polarization in thin film ferroelectric capacitors. This work showed that electric field, temperature, and mechanical stress can be used to enhance the switching and remanent polarization in ferroelectric thin films. Enhancing the switching polarization will also enhance the signal margin in FRAM devices and can enable scaling of the technology to future technological nodes. Combining stress with electric field and temperature will further enhance the polarization properties of ferroelectric thin film capacitors.

As future work, further experimentation is recommended to study the combined effects of stress, temperature, and electric field on the polarization of ferroelectric capacitors. The switching polarization should be characterized at various temperatures and compressive stress levels. The reliability properties of these effects on ferroelectric capacitors should also be studied. Reliability is a very important metric in memory technology. If these methods are to be considered for commercial FRAM devices, then it is important to confirm that there is a minimal trade-off in the reliability properties.

Development of quantitative models is also recommended. This includes constitutive modeling of the combined electrical, mechanical, and thermal effects. While current models have been developed for bulk PZT, models are needed to accurately describe the behavior of PZT thin film capacitors. These models can then be used to

accurately simulate the combined effects of stress, temperature, and electric field. Successful simulations can then be used to develop methods for efficiently and practically inducing an enhancement in the polarization properties of ferroelectric devices at a large scale manufacturing level.

Finally, XRD studies are recommended. The stress effects observed in this work were attributed to lattice distortion, 90° domain wall motion, reorientation of in-plane domains to out-of-plane domains, and nearly 100% *c*-axis domain orientation. In order to quantify these effects an XRD analysis of the embedded PZT films is required. Initial results indicate that PZT can be detected in our devices using high energy X-rays. Future experiments will be designed to quantify domain volume fraction *in situ* as a function of stress using XRD.

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BIOGRAPHICAL SKETCH

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