ADVANCED DEVICE RELIABILITY STUDY OF GAN HEMTS USING LOW FREQUENCY NOISE SPECTROSCOPY

By

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Dedicated to my parents

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AlGaN/GaN HEMTs have entered commercial production from 2005 and have demonstrated excellent performance levels for high power RF applications like cellular 3G and WiMax base transceiver stations (BTS). To realize the full potential of this material technology it is imperative to gain a deeper understanding of the failure mechanisms which are not fully understood yet. This work uses low frequency noise as a defect spectroscopic tool and microwave noise spectroscopy for studying hot-carrier effects.

A baseline is established by identifying key noise sources in the AlGaN/GaN HEMT gate stack and channel region. The channel is found to be stable showing only interface defect related 1/f type noise. The gate stack shows vulnerability with the presence of mobile point defect centers and the existence of dislocations very close to the gate metal.

The role of the inverse-piezoelectric effect as a failure mechanism is explored by systematic gate step stress. New permanent defect centers are generated right under the gate metal contact along with the activation of mobile point defects. The channel is

found be to immune to the stress. The role of impurity diffusion as a precursor to catastrophic degradation is also pointed out.

Key bias points are identified which result in permanent trap creation at the AlGaN/GaN channel interface. The role of hot-carriers as a failure mechanism is discussed by measuring electron temperature profiles in the channel. Finally degradation of the gate stack under RF overdrive stress is studied and the activation energy and the trap location of a point defect center in the AlGaN barrier is extracted.

CHAPTER 1
GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS

Introduction

High electron mobility transistors (HEMT) based on the III-Nitride AlGaN/GaN heterostructure have shown immense potential. The wide-bandgap (3.4 eV) and high saturation velocity (~ 3×10^7cm/sec) of gallium nitride makes it useful for both high power and high frequency applications. A performance metric often used to compare RF power transistor potential of various material technologies is the Johnson Figure of Merit (JFoM). It is the product of the critical breakdown electric field and the carrier saturation velocity. Among the existing semiconductor technologies GaN shows the highest JFoM of ~ 50THz.V which is 2× higher than 4H-SiC, 10× higher than InP, 20× higher than GaAs and 100× higher than Silicon [1]. In real world scenarios these devices demonstrate good performance initially but start to degrade as soon as they are operated for prolonged duration. In fact, in many cases these devices degrade in a very short period of time. This device technology is fairly new and processes are still not mature leading to low yields and pre-mature breakdown. In spite of this it is important to thoroughly investigate the mechanisms which cause degradation and affect not only short term but long term reliability as well. The motivation thus, becomes to understand failure mechanisms and the physics of device degradation in these III-Nitride HEMTs which can be used to optimize device structure and develop processes to unleash the full potential of this technology.

In solid state devices the primary cause of degradation is always in some way linked to generation and/or migration of defects in critical locations inside the device. Common MOSFET failure mechanisms like hot carrier injection (HCI), gate oxide

breakdown (GOB), and negative bias temperature instability (NBTI) are typically associated with defect generation which changes threshold voltage, transconductance, series resistance etc. Defects can be characterized by techniques such as Pulsed I-V, Charge-pumping and DLTS. Most of these methods require special test structures. For instance capacitances of the order of a few picoFarads are needed for an accurate capacitance based DLTS measurement. Large gate leakage currents can reduce the accuracy of impedance based measurements like charge pumping. Most realistic devices have low gate capacitance due to small feature sizes and relatively high gate leakage currents. Low frequency noise (LFN) measurements can be performed on fully processed advanced sub-micron devices. Unlike other techniques low frequency noise measurements are the most benign way of performing defect spectroscopy. Defects which actually affect charge transport in the device show up in the noise spectra. More precisely defects which are located within a few kTs around the Fermi level participate in noise generating process. Traps which are far above the Fermi level are nearly empty and the ones located far below the Fermi level are almost filled. Defect energies and their physical locations can be determined by scanning the Fermi level through the bandgap by changing the gate bias, drain bias and/or temperature. This enables, a component defect level analysis by looking at noise from each of part of the system like interconnects, contacts, channel or the gate stack. Low frequency noise is therefore a powerful defect spectroscopy tool for semiconductor devices particularly suitable for reliability studies. A brief introduction to the theory of noise in electron devices is presented next.

Noise Mechanisms in Devices

Electrical noise in semiconductor devices and materials has many physical origins. It is a steady-state spontaneous fluctuation in either the electric current or voltage in the time domain measured at the contacts of a device. According to Ramo's theorem the instantaneous current measured at the contact is given by the following relation,

$$I(t) = \frac{q}{L}\sum_{k=1}^{N(t)} v_k(t) \quad (1\text{-}1)$$

Where N(t) is the number of carriers, $v_k(t)$ the instant carrier velocity, and L the contact spacing. In the frequency domain these fluctuations show up in the low and high frequency regimes depending on the type of mechanism. The fluctuations in the high frequency regime viz. shot noise and thermal noise are typically associated with instantaneous velocity fluctuation of charge carriers and exhibit flat spectra. These noise sources are fundamentally linked to the kinetics of the electron gas. Typically the short-circuit thermal current noise spectral density is given by,

$$S_{\Delta I}(f) = 4k_B T_N Re(Y) \quad (1\text{-}2)$$

Where Re(Y) is the real part of the small signal AC admittance of the device, k_B is the Boltzmann constant and T_N is the noise temperature. At low biases the carriers are in thermal equilibrium with the lattice since the dominant scattering mechanism is nearly elastic with longitudinal acoustic (LA) phonons. Enough scattering events randomize the electron momentum or the electron velocity giving rise to velocity fluctuation noise. In this case T_N equals the lattice temperature (T_L) which is typically the ambient temperature of the measurement environment. However, when higher electric fields are applied the carriers gain kinetic energy and are not in thermal equilibrium with the lattice. In polar semiconductors like the GaN the dominant scattering mechanism at high

fields is the polar optical phonon (POP) scattering. Hence the electrons loose energy by emitting longitudinal optical (LO) phonons and in the process exchange both momentum and energy. When there are large numbers of carriers and electric fields are uniform in the device the electron momentum distribution function is fairly uniform and can be approximated by a Boltzmann function with an effective spread given by the electron temperature (T_E). In this case T_N equals the hot-electron temperature (T_E). Thus, by measuring high frequency noise temperatures in the device one can determine the nature of these hot-electron processes quantified by the electron temperature profiles.

In the low frequency part of the spectra the carrier number fluctuation dominates. This component is very sensitive to the microscopic environment that the charge carriers “see” during transport. There are three types of noise which form the low frequency spectra.

Generation-Recombination (GR) noise is a fluctuation in the conductance due to trapping and de-trapping of free carriers (electron or hole) between the continuum states and discrete local levels. A single trap level leads to a Lorentzian noise spectrum which has a characteristic frequency equal to the reciprocal effective trapping time constant. GR noise underlies one of the well-known methods of performing defect spectroscopy in modern devices [2], [3].

Random telegraph switching (RTS) noise is a discrete two level switching of the conductance in the time-domain. It is generally a single electron event often found in modern nano-devices with a small number of free carriers. It is again a powerful spectroscopic tool since it provides information of both capture and emission time constants associated with the trap [4], [5].

1/f noise is the most ubiquitous of noise sources but one of the least understood physically. Two competing models are used to explain the mechanism. The number fluctuation (Δn) model proposed by McWhorter proposes that elastic tunneling of channel carriers into the oxide layer at the Fermi level in the channel of a MOS structure produces an exponential distribution of time-constants. This leads to 1/f noise in the channel conductance. On the other hand Hooge's model is based on mobility fluctuations ($\Delta\mu$). The random acoustic scattering events are said to produce this noise. Presently the most accepted model for MOS structures is the so-called correlated number-mobility fluctuation [6]. Although there is no consensus on the mechanism, there is strong evidence of the process dependence of 1/f noise [7]. The Hooge value is an excellent figure of merit for the crystallographic quality of the bulk material or inverted channel region. It has been known to have a strong correlation with the quality of the SiO_2/Si interface [8].

Organization

This work is a comprehensive account of five investigations performed in a systematic way to unravel the gate stack and channel reliability by a combination of different DC and RF stresses. Chapter 2 shows the novel low frequency noise setup that we developed to perform simultaneous defect spectroscopy of the gate stack and the channel region. It is used to demonstrate the instability that exists in the gate stack due to mobile point defect centers right under the gate metal. The channel is found to be stable with only $1/f^{\gamma}$ type interface defect noise dominating. In Chapter 3 the gate stack is probed in more detail. Inverse-Piezo electric stress is invoked by a step stress experiment. Transient and permanent effects are separated. Transient effects are due

to trapping and de-trapping of carriers in the existing trap states in the AlGaN barrier. New defect centers are created under the gate metal along with the activation of mobile point defect centers. The channel was found to be immune to the whole stress regime. Very early stages of the gate stack degradation are well captured which point to defect creation and migration as a precursor to catastrophic gate breakdown. In Chapter 4 the attention is turned to the channel region by applying a combination of gate and drain voltages to probe hot-carrier and self-heating effects. Key regions in the bias range are identified where permanent degradation occurs in the channel due to an increase of AlGaN/GaN interface defect density. In Chapter 5 microwave electron temperature spectroscopy is used to understand the kinetics of the hot-carrier effects which cause this degradation in the channel. From the electron energies it is found that hot-carriers are fairly well confined in the AlGaN/GaN interface and are responsible for creating new interface defects. In Chapter 6 large signal RF reliability of GaN HEMTs is discussed by applying RF overdrive stress. New defect centers are created in the gate stack at higher compression levels. Finally the activation energy and the physical location of an unstable point defect center is extracted.

CHAPTER 2
NOISE SOURCES IN UNSTRESSED GAN HEMTS

Motivation

A large part of the current research effort in AlGaN/GaN HEMT reliability is concentrated on the poor gate contact and associated high leakage currents leading to problems such as drain current collapse, virtual gate effect etc [9]. The gate leakage current has been shown to significantly enhance the drain noise in the AlGaN/GaN transistors and therefore, defect spectroscopy using drain noise alone becomes difficult [10]. As a result an independent study of gate and drain noise simultaneously is required which to the author's knowledge has not been performed till date. This chapter demonstrates a comprehensive experimental setup developed to perform these simultaneous measurements on drain and gate noise as a function of respective bias (Figure 2-1). The results of these measurements are used to identify individual noise sources in the vertical and lateral regions of gate stack and channel, respectively.

Devices under Study

In reliability studies it is often important to differentiate between process induced defects from stress induced defects which are typically generated during device operation. If we think in terms of the reliability bathub curve the early "infant mortality" failure of the devices can be reduced by a more mature device process which gives high yielding devices. Therefore, this study is mainly focused on industrial grade fully processed advanced AlGaN/GaN HEMTs grown on Silicon substrate. The device under study (Figure 2-2) consisted of an 800 nm GaN buffer layer grown on a high resistivity Si substrate by metal organic chemical vapor deposition (MOCVD). A transition layer of AlN is employed for stress mitigation. The buffer is semi-insulating with the Fermi level

in GaN at around E_C-0.5eV. On top of this buffer an 18 nm of unintentionally doped (UID) $Al_{0.26}Ga_{0.74}N$ barrier layer is grown by MOCVD and finally capped by 1.5 nm of GaN. All the layers are undoped. A Schottky gate contact of 0.65 μm length is formed by depositing Ni/Au followed by a rapid thermal anneal (RTA). Ohmic contacts are created for drain and source regions by depositing Ti/Al followed by RTA. A SiN passivation is made by PECVD. The transistor has a gate width of 200 μm with 10 fingers corresponding to a gate periphery of 2 mm.

The setup for measuring the voltage drain noise uses a low noise voltage pre-amplifier (SRS560) connected at the drain terminal and a drain bias resistor at least 10 times higher than the small signal channel resistance. The gate noise setup required a different approach due to high leakage currents. Direct voltage amplification couldn't be done with a gate bias resistor. The gate current noise gets reflected to the drain noise via a voltage drop across the gate bias resistor and is subsequently enhanced by transconductance in the linear regime. Therefore, an ultra-low noise op-amp AD797 was used to create an AC short circuit at the gate terminal and to convert gate current to voltage which in turn was amplified by a low noise voltage amplifier. Both these signals were simultaneously measured using the 2-channel Agilent 35670A spectrum analyzer as shown in Figure 2-1. It should be mentioned here that the main idea behind this approach is to create an AC short-circuit at the gate terminal thus, preventing any circuit induced fluctuation to show in the drain noise. Interestingly most AlGaN/GaN HEMTs currently suffer from the problem of high gate leakage current and therefore, even a single channel drain noise measurement will show noise features of gate current if the gate is not properly AC shorted. A time domain noise measurement of both the

channels or a spectral correlation measurement can determine if this problem exists. Time domain random telegraph switching (RTS) noise was measured using an Agilent U2542A data acquisition unit sampled at 2 μs. DC characterization was performed by a HP4145B parameter analyser and was limited to gate and drain I-V, and transconductance measurements. A C-V characterization using HP 4275A was also performed for the gate to source-drain diode to extract various device parameters of interest.

DC Characterization

The effective mobility of the channel was extracted from a combination of DC transconductance and CV profiling measurements. The mobility of the FET in the linear regime was deduced using,

$$\mu_N = \frac{L_G}{q n_S W_G R_{CH}} \tag{2-1}$$

Where, L_G, W_G are gate length and periphery respectively and R_{CH} is the channel resistance. Sheet carrier densities were extracted from the C-V characterization of the reverse bias gate to source-drain diode at 100 kHz using,

$$n_S(V_G) = \frac{1}{q}\int_{V_P<V_T}^{V_G} C dV_G \tag{2-2}$$

Where V_P is taken below the threshold voltage. The calculated mobility values were between 180 – 415 $cm^2/V\text{-}s$ for sheet concentrations of 10^{11} to 10^{12} cm^{-2} and agreed well with results from other groups [11]. It was found that the field effect mobility was a function of sheet carrier density which is also reported extensively [12]. Here, the effect of source and drain access series resistance was neglected which needs to be taken into account to accurately extract the channel mobility.

Drain Current Noise

The device under test was biased in a common-source configuration at a constant low drain to source voltage of 80 mV. Drain current noise measurement is conducted by sweeping the gate voltage from -1.32 V to -1.0 V at a constant V_{DS} = 80mV. The gate sweep was always over threshold voltage $V_T \approx$ -1.38 V. The FET was kept in the linear regime and the resulting noise spectra were measured for the frequency range of 1 Hz to 51.2 kHz at 300K. The noise spectra were of the $1/f^{\gamma}$ type with the exponent γ ~ 0.9-0.85 varying inversely with the gate overdrive voltage shown in inset of Figure 2-2. No distinct generation-recombination (GR) noise components could be seen. In the triode region, the channel consists of a gated part and un-gated part of source, drain access regions. If the noises originating from these regions are assumed to be uncorrelated then the short circuited drain noise is,

$$\frac{S_{ID}}{I_D^2} = \frac{S_{RCH}}{R_{CH}^2}\left(\frac{R_{CH}^2}{\left(R_S + R_D + R_{CH}\right)^2}\right) + \frac{S_{RD}}{R_D^2}\left(\frac{R_D^2}{\left(R_S + R_D + R_{CH}\right)^2}\right) + \frac{S_{RS}}{R_S^2}\left(\frac{R_S^2}{\left(R_S + R_D + R_{CH}\right)^2}\right) \quad (2\text{-}3)$$

Where S_{RCH}, S_{RS} and S_{RD} represent the uncorrelated resistance noise of the channel, source and drain access regions respectively. Only the channel noise is dependent on the gate bias and this feature is exploited to determine which term dominates in Eq. (2-3).

Figure 2-3 shows a plot of normalized drain current versus gate overdrive voltage (V_G-V_T). Two distinct regions of $S_{ID} \propto V_G^{-1}$ and V_G^{-3} dependence are observed in low and high gate voltage respectively. This is a clear indicator that only the gated part of the channel noise is the dominant source [13]. Having determined the noise source, a Hooge parameter was calculated using the classical phenomenological equation,

$$S_{ID}(f) = \frac{q\mu_n \alpha_H I_D V_D}{L_G^2 \, f} \tag{2-4}$$

As seen in Figure 2-4 the Hooge parameter associated with the gated part of the channel varies from ≈ 10^{-3} to 10^{-4} and shows an inverse dependence with the sheet carrier concentration. These values indicate that the noise from the access regions is still lower indicating the maturing of ohmic contact technology in nitride based materials. Also the temporal stability of the noise indicates a good quality of AlGaN/GaN interface. The inverse dependence of α_H with the sheet carrier concentration has been attributed to number fluctuations of carriers by thermally-assisted tunneling in and out of the GaN donor states [11]. A temperature based measurement was not performed which is essential to verify this claim. Also, the effect of series resistance needs to be decoupled in the analysis. The frequency exponent $\gamma \propto 1/V_G$ dependence (see inset of Figure 2-2) is another indication of a number fluctuation phenomena. Band-bending changes the trap distribution at the Fermi level thereby altering the dynamics of carrier trapping and de-trapping process [14].

Gate Current Noise

Gate current noise is measured simultaneously with the drain noise as a function of gate overdrive voltage at constant V_{DS} of 80 mV. Therefore, the inverted channel exists for the complete gate bias range of V_G from -1.3 V to -1.0 V. In the DC case the gate metal semiconductor junction is reverse biased and vertical tunneling of electrons, Figure 2-5, is expected to be the dominant current leakage mechanism in this regime [15]. Considering this, the electron transport is predominantly from gate to the channel region, and therefore the low frequency noise of the leakage current is directly probing the metal semiconductor contact quality and space-charge region traps in the AlGaN

barrier layer. If it's assumed that the noise sources in the device are uncorrelated, the compact noise model of the device can be constructed as shown in Figure 2-5. The gate current flows from drain to gate through the channel therefore, the short circuit current fluctuation measured at the gate terminal is,

$$\frac{S_{IG}}{I_G^2} = \frac{S_{rg}}{R_G^2}\left(\frac{R_G^2}{\left(R_G + R_D + R_{CH}\right)^2}\right) + \frac{S_{RCH}}{R_{CH}^2}\left(\frac{R_{CH}^2}{\left(R_G + R_D + R_{CH}\right)^2}\right) + \frac{S_{RD}}{R_D^2}\left(\frac{R_D^2}{\left(R_G + R_D + R_{CH}\right)^2}\right) \quad (2\text{-}5)$$

Where, S_{rg}, S_{RCH} and S_{RD} represent the noise of gate, channel and drain regions respectively. Channel and drain resistances $R_{CH} \approx 18.5\ \Omega$, $R_D \approx 2.5\ \Omega$ at gate bias $V_G \approx -1.3$V were determined from the differential transconductance characteristics of the FET. Differential gate resistance $R_G \approx 6.6\ M\Omega$ at $V_G \approx -1.3$V and $V_{DS} = 80$ mV was determined from the reverse gate to source I-V characteristics. Since $R_G >> (R_{CH} + R_D)$ Eq. (2-5) reduces to

$$\frac{S_{IG}}{I_G^2} \approx \frac{S_{rg}}{R_G^2} \quad (2\text{-}6)$$

This indicates that the gate noise originates mainly from the gate stack region and channel noise is negligible.

1/f$^{\gamma}$ Noise

Gate current noise power spectra of the same device under identical bias conditions but carried out at different time instances are shown in Figure 2-6. In each case the spectrum has the form of 1/f$^{\gamma}$ noise with a visible Lorentzian noise component on top of it. No high frequency roll-off of noise was observed at any of the gate voltage in the measured frequency range of 1Hz to 51.2 kHz. As an indicator, the measured noise is at least 3 orders of magnitude higher than the shot noise ($2qI_G$) at 51.2 kHz,

and therefore doesn't show up at high frequencies. Oftentimes RTS noise was also observed in the time domain which manifested as a Lorentzian component in the frequency domain. The nature of the Lorentzian noise component is discussed in the next section. The $1/f^{\gamma}$ noise component of S_{IG} is extracted from the spectrum and plotted as function of gate direct current (I_G). A dependence of S_{IG} proportional to square of I_G is seen in Figure 2-7. This $S_{IG} \propto I_G^2$ dependence is typical of a trap density fluctuation in the space charge region of the Schottky junction [16]. This $1/f^{\gamma}$ noise component was found to be temporally stable and reproducible. Therefore it may be argued that the gate Schottky contact is of high quality and does not degrade at least under normal bias conditions $V_{DS} < 0.1$ V and $V_T < V_G < 0$. Also, since the absolute magnitude of the $1/f^{\gamma}$ noise component remained the same the interface defect density does not change.

RTS Noise

As mentioned previously a non-repeatable Lorentzian component was observed in the gate noise spectra when measured at different time instants under identical biasing conditions. Inset in Figure 2-6 (c) and (d) show the measured RTS noise in the time domain. The corner frequencies and respective time constants are different for both RTS. It was observed that repeating the same measurement at different time instances led to a change in the Lorentzian characteristic frequency (f_C) and magnitude. It "appeared" and "disappeared" randomly in the low and high frequency region of the spectra and no specific trend in the frequency drift could be observed. On the contrary, the background $1/f^{\gamma}$ noise in all those measurements remained stable and showed the same I_G dependence. This non-repeatable Lorentzian and a repeatable $1/f^{\gamma}$ noise showed up in all the measurements. It is concluded that the gate fluctuation is actually a

sum of uncorrelated 1/f and RTS noise sources. RTS noise in my measurements mainly consisted of discrete two level fluctuations. These fluctuating current states are a direct indicator of a single electron trapping and de-trapping at a point defect center. The time an electron spends at the defect site determines the high and low current times. The dynamics of the process is governed by the principle of detailed balance but since it's a statistical process it shows a Poisson distribution given by this relation,

$$t_{high/low} \sim exp\left(-\frac{t}{\tau_{high/low}}\right) \tag{2-7}$$

It was found that the measured high and low current times exhibited these Poisson distribution confirming that electron trapping and de-trapping at point defect centers in the gate stack was responsible for the observed RTS noise. RTS noise is also observed in confined Si MOSFET channels when the defect is located at a strategic location inside the device whereby it can modulate the complete channel current for instance in the SiO_2 oxide region near the source side where electron injection takes place. Even a small change in the local potential due to electron trapping at that location can significantly affect the channel current. In our device the gate leakage current shows large relative two level fluctuations. If the gate leakage current was due to a homogenous electron injection across the whole gate area ($N_{fingers} \times W_G \times L_G$) then it is very unlikely that a single electron would modulate the whole DC gate leakage current. This indicates that the DC gate leakage current mechanism in our device is physically localized whereby a single electron trapping and de-trapping can electrostatically modulate the whole leakage current if it is located very close to the leakage pathway. The other interesting result is that these RTS high and low current states show a different mean time constant when the same measurement is performed on different

days. However during the noise measurements which typically last for an hour the time constants are stable and do not change showing only gate bias dependence. This indicates that the defect center responsible for trapping and de-trapping a single electron is unstable and exhibits defect migration at room temperature in the time frame of a few days. It is known that even in an unbiased device high electrical fields of the order of a few MV/cm are present in the AlGaN/GaN heterostructure due to spontaneous and piezoelectric polarization which are not present in silicon MOSFETs [17]. These electric fields are further enhanced by the applied gate bias during device operation. Also it is known that the AlGaN barrier is mechanically strained on top of GaN buffer and exhibits inverse piezo-electric properties [18].

Therefore, it can be easily proposed that an unstable defect center in AlGaN barrier layer can migrate under the influence of these factors or by a complex interplay of them like electric field induced mechanical strain. On one of the days the defect can be physically very close to the localized region of DC gate current and it captures and emits an electron from the gate metal thereby modulating the complete current pathway and shows up as a RTS noise as seen in Figure 2-7 (c) and (d). On other days it can be physically away from the localized regions of DC gate current and when it captures and emits an electron it does not modulate the complete current pathway thereby showing only Lorentzian in the frequency domain as seen in Figure 2-7 (a) and (b) due to weaker electrostatic coupling with the gate leakage current. It is widely reported that the dominant gate leakage mechanism in these devices is via dislocation spots [19],[20],[21],[22], often a defect center located close to these dislocations will enable electron trapping and de-trapping which will modulate the current and create large

relative RTS noise. In all other cases it will lead to a Lorentzian component in the noise spectra. It was observed that most times the RTS noise showed a relative large fluctuation of $\Delta I_G/I_G$ between 20% to 40%. If it is assumed that the defect center responsible for modulating the dislocation current “blocks” the complete electron leakage pathway in that region, then a crude estimate of dislocation density can be extracted from the relative amplitude of the RTS noise. In this case, a dislocation density of less than 10^6 cm^{-2} is deduced which is being reported in current state-of-the-art AlGaN/GaN HEMT devices [23].

In summary, the gate noise analysis points to two key effects that are observed in the gate stack. There are localized regions of gate leakage current in the device possibly linked to threading dislocations and extended defects under the gate stack. Also there are unstable point defect centers under the gate stack which show room temperature defect migration in the time frame of a few days. In the next chapter I study the effect of systematic reverse gate voltage step-stress which stresses the gate stack with high electric fields and mechanical strain via the inverse-piezo electric effect.

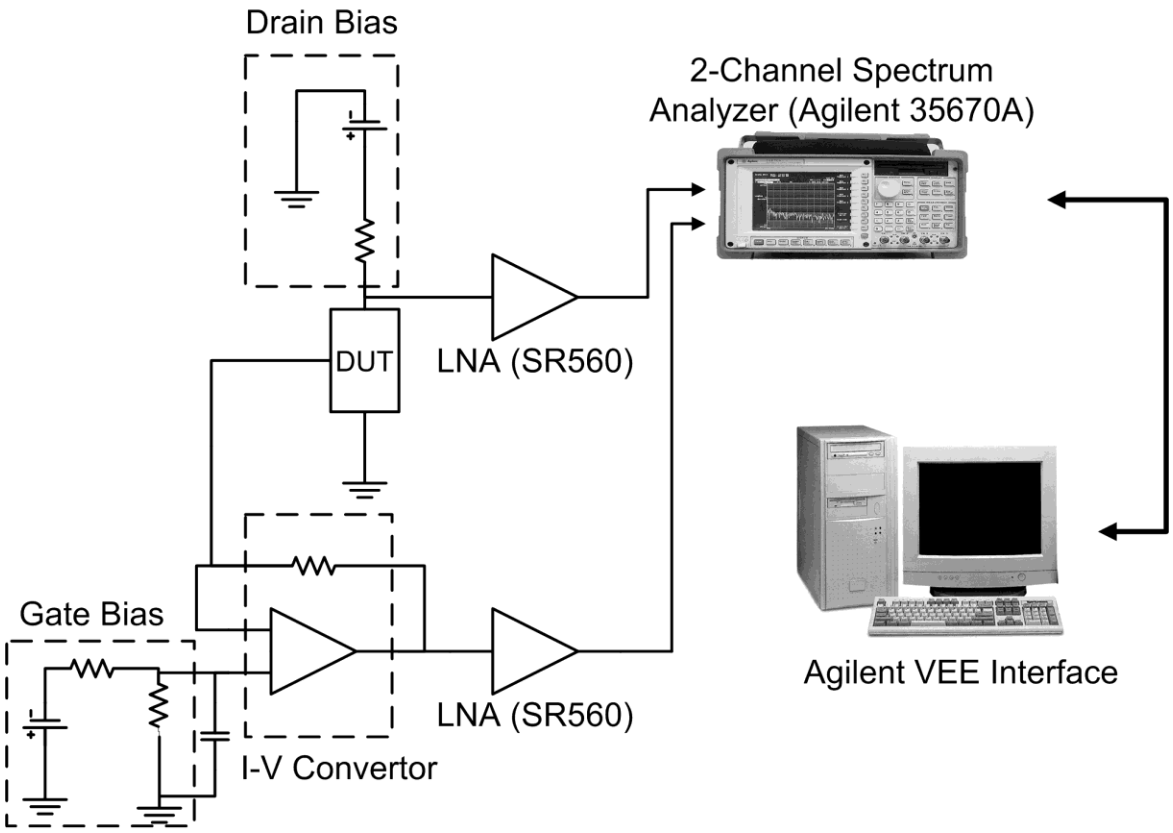

Figure 2-1. Experimental setup for low frequency noise characterization. An ultra-low noise Op-Amp (AD797) is employed as an I-V converter for gate current noise. Two SRS560 low noise voltage amplifiers are used to amplify gate and drain noise.

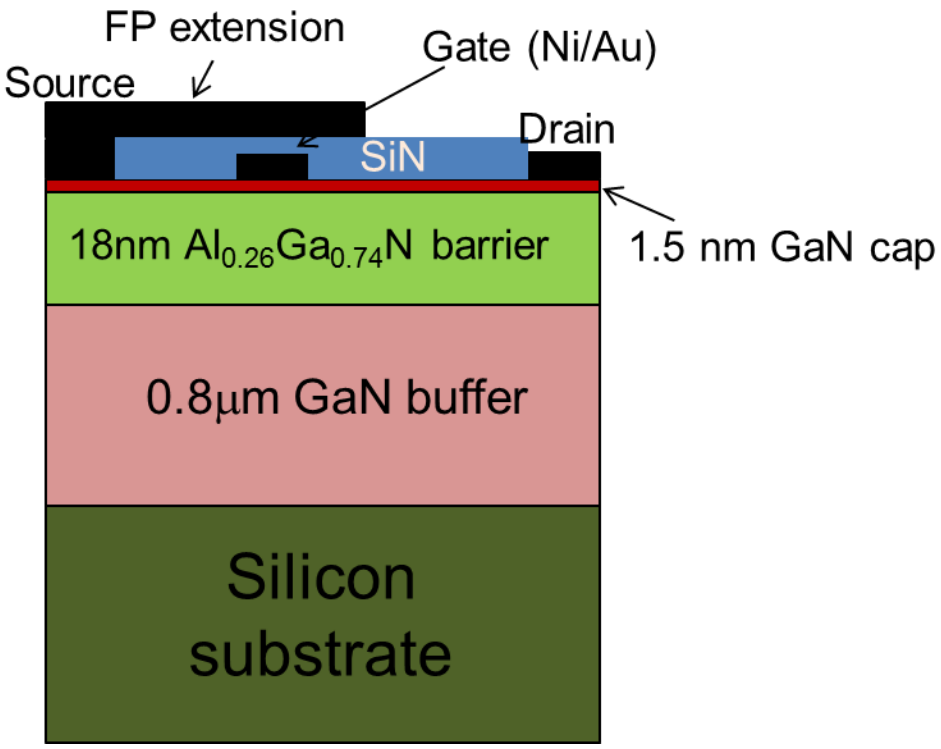

Figure 2-2. Device cross-section of GaN HEMTs used in this study.

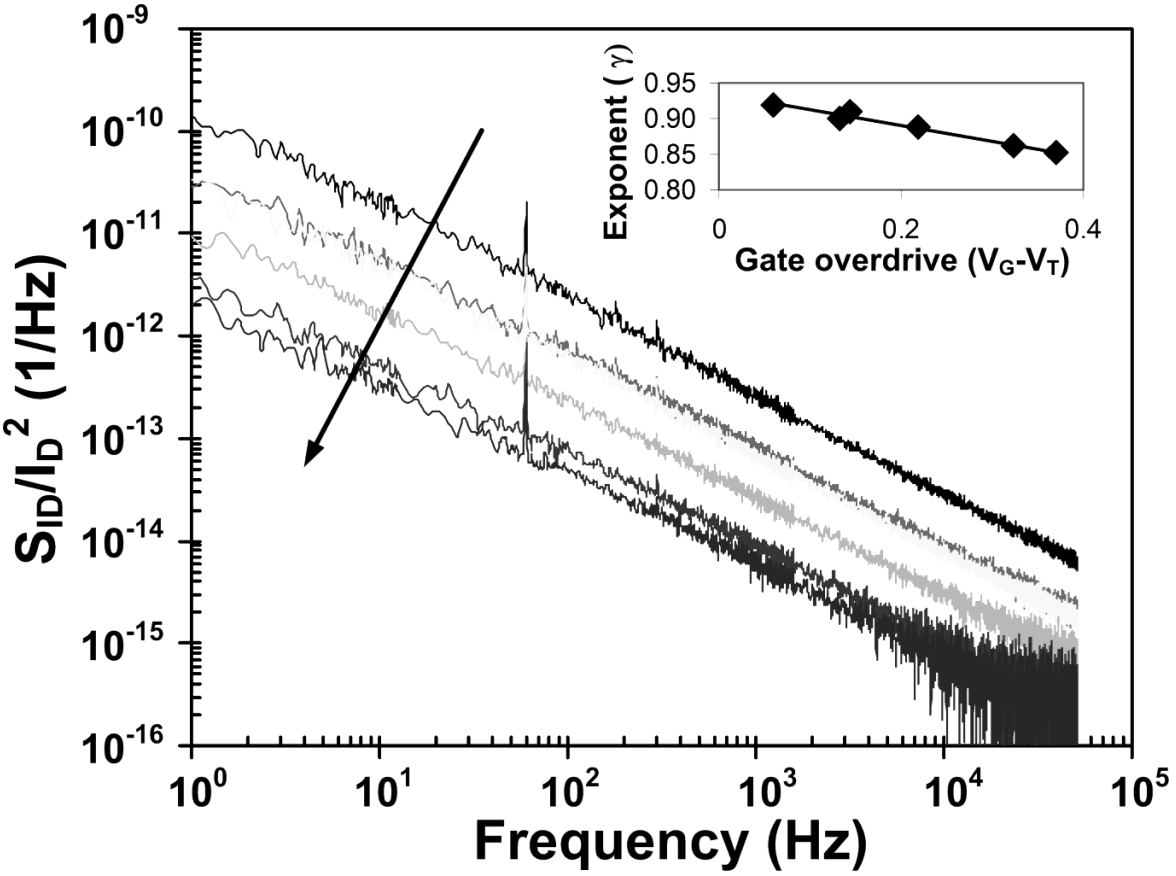

Figure 2-3. Normalized drain current noise (S_{ID}/I_D^2) as a function of increasing (indicated by arrow) gate bias (V_G) of -1.32V to -1.01V at V_{DS} = 80 mV. Frequency exponent (γ) of the $1/f^{\gamma}$ noise varies from 0.9 to 0.85 as a function of increasing gate bias. Inset shows the measured frequency exponent γ as a function of gate overdrive voltage (V_G-V_T). The solid line is a theoretical best fit.

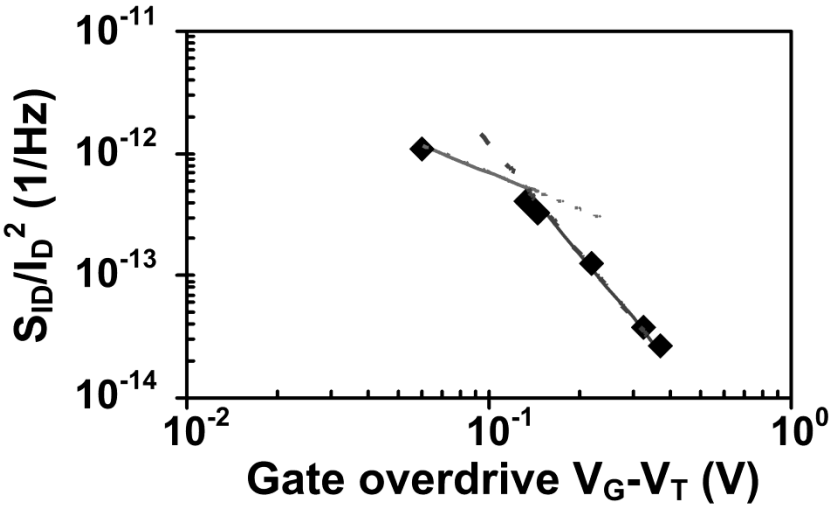

Figure 2-4. Normalized drain current noise (S_{ID}/I_D^2) at 200 Hz as a function of gate overdrive voltage V_G-V_T. Solid lines are V_G^{-1} and V_G^{-3} fits on the measured data points for $0 < V_{G\text{-}overdrive} < 0.1$ and $V_{G\text{-}overdrive} > 0.1$ respectively.

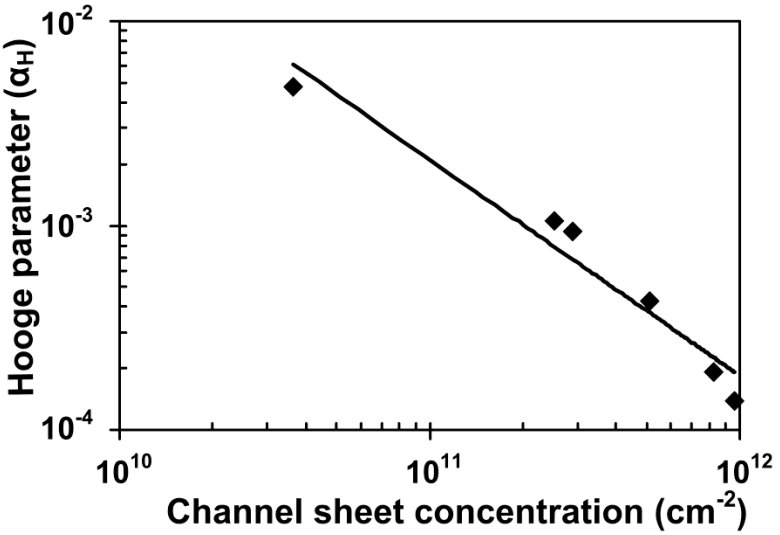

Figure 2-5. Dependence of the Hooge parameter α_H on the sheet carrier concentration n_s (cm^{-2}). Solid line is a theoretical best fit for the measured data points; it shows $1/n_s$ dependence.

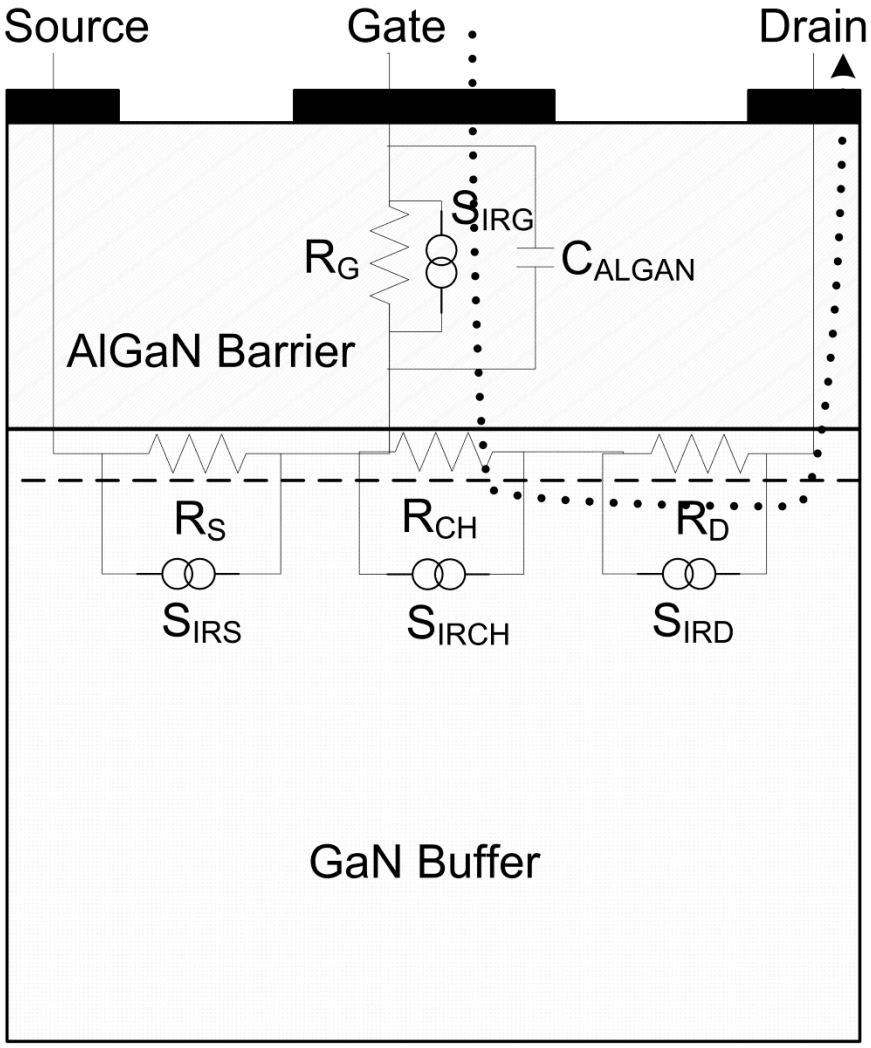

Figure 2-6. Compact model of noise sources in the channel (S_{IRS}, S_{IRCH}, S_{IRD}) and gate region (S_{IRG}) of the device. The dashed line indicates the channel region at the AlGaN/GaN interface. The dotted line indicates the electron current leakage path for strong inversion and low drain bias.

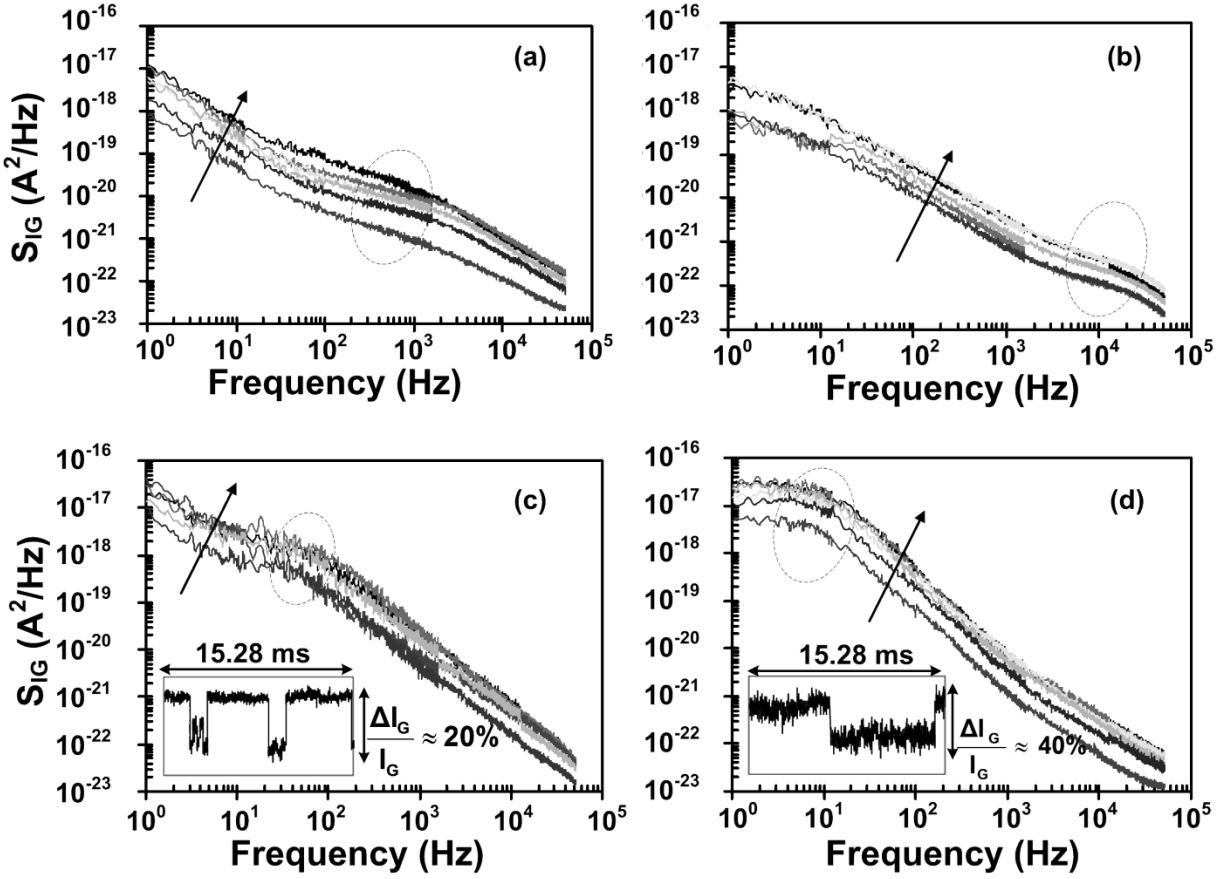

Figure 2-7. Gate current noise spectra as a function of decreasing (indicated by arrow) gate bias (V_G) of -1.01V to -1.32V and V_{DS} = 80 mV measured at four different time instances. A Lorentzian noise component without a time RTS noise is seen in (a) and (b). The insets in (c) and (d) show the corresponding RTS noise. The characteristic frequencies of all Lorentzians are different.

CHAPTER 3
HIGH GATE ELECTRIC FIELD STRESS EXPERIMENT

Motivation

Many prominent degradation mechanisms have been identified in GaN HEMTs by various groups which cause temporary and permanent changes in the electronic and material structure of the device [24–26]. Figure 3-1 shows a classification of these mechanisms in these devices as a function of physical effect. Except polarization most of these effects have been well studied in other III-V HEMTs and are relevant for nitride transistors as well. Lattice mismatch induced strain in the AlGaN barrier via inverse-piezoelectric effect has been identified as one of key cause of degradation at high electric fields under the gate stack [18]. RF devices experience high gate reverse bias during normal operations which cause large vertical fields below the gate. Therefore, it's important to probe this effect in more detail.

Low frequency noise is known to be an extremely sensitive tool for studying reliability and changes in electronic structure due to degradation [27], [28]. A few reliability studies have been performed in these devices using drain current noise to understand changes in the channel region [29–32]. Most of these groups have concluded that off-state stress doesn't seem to cause major changes in drain noise. This work on the other hand reveals that interesting things are happening right below the gate stack which doesn't seem to be affecting the channel and thereby drain noise. To gain a detailed understanding, a simultaneous measurement of gate and drain current noise is necessary to isolate degradation in the gate stack and/or the heterostructure interface [33]. This work demonstrates the results of DC and low frequency noise characterization of gate and drain currents in AlGaN/GaN HEMTs

which were stressed to high reverse gate biases with source and drain connected to ground. Noise and IV measurements were performed during and after stress in both frequency and time domain. Temporary and permanent changes in the electronic structure of the device are delineated and physical locations of degradation are identified.

Device Description and Experimental Details

The devices under test are the same used in the previous study. The devices are fully packaged to avoid any ambient optical instability to affect electrical measurements.

A fully automated characterization suite is developed for performing stress, DC and noise measurements. A semiconductor parameter analyzer HP4145B is configured for performing both electrical stress and IV measurements. Figure 3-2 shows the stress protocol and time instances when a measurement is performed. The gate is stressed by applying a stepped reverse bias from -5 to -20V with -5V increment for 10 minutes each. After each cycle, stress is stopped and DC transconductance, drain and gate current noise are measured. Both drain and gate DC currents are measured at low V_{DS} of 80 mV. Low frequency noise of gate and drain currents is measured at a constant V_{DS} and V_{GS} of 80 mV and -1.23 V, respectively, using a setup which was demonstrated in the last chapter. As will be shown later, threshold voltage itself changed during stress and the chosen value of gate voltage for measuring noise was found to be appropriate for keeping the device in strong inversion. It should be mentioned here that DC and noise measurements were carried out also several weeks after the stress was applied which was useful for isolating transient trapping and de-trapping effects from permanent changes in the device electrical properties.

Stress Characterization Results

DC Characterization

The focus of this work was to understand changes in the low frequency noise characteristics of the device which undergoes systematically applied electrical stress. Therefore, the DC parameters which were monitored during the stress were mainly chosen for convenience to extract the relevant noise parameters. The noise measurements were conducted at low drain current and voltage levels which were significantly smaller than the stress conditions making the measurements electrically benign so as not to alter the device characteristics. The inset in Figure 3-3 (a) shows the measured drain current transfer characteristics before and after stress respectively. A large positive shift can be seen in the threshold voltage which forces a drift in the transfer characteristics. The peak value of the transconductance (gm) was found to be constant with an overall positive voltage shift before and after stress indicating that no major changes took place in the channel region. As mentioned earlier DC characterization was also carried out several weeks after the stress was removed to isolate transient trapping de-trapping effects. Figure 3-3 (a) and (b) show the changes in the threshold voltage of the device during and after stress respectively. It can be clearly seen that a large positive V_T shift is induced during stress changing it from -1.36 V to -1.17 V in a span of 40 minutes. This recovers back to pre-stress levels several days later. In subsequent sections it will be seen that drain current noise also changes in accordance with this large V_T shift due to a change in sheet carrier concentration in the channel. Gate leakage current was also measured simultaneously with drain current in the transfer characteristics. Figure 3-4 shows the evolution of gate leakage current

during stress. It shows a constant decline and exhibits large relative fluctuations contributing to large gate current noise in the frequency domain.

Drain Current Noise Characterization

Drain current noise is very sensitive to the defect states affecting charge transport in the channel and access regions making it an excellent indicator of the channel quality. Normalized drain current noise was measured as a function of gate bias to identify the dominant noise sources from different parts of the channel. It was found that the gated part of the channel was the main source of drain current noise as found previously in unstressed devices. A DC gate voltage of -1.23 V was chosen for noise measurement since both channel noise and resistance dominate in that region. Figure 3-5 shows the drain current noise before and after stress at the same DC bias level. An increase by a factor of 4 is visible in the spectra. It was observed that this increase was temporary and the noise recovered completely to its pre-stress levels a few weeks later. A Hooge equation of the normalized drain current noise can be written as,

$$\frac{S_{I_D}}{I_D^2} \cong \frac{S_{R_{CH}}}{R_{CH}^2} = \frac{\alpha_{CH}}{A_{CH} N_{CH} f} \tag{3-1}$$

Where, S_{RCH}, R_{CH} and A_{CH} represent the resistance noise, resistance of the gated part of the channel and area of the channel respectively. In the triode region at low drain voltages, the sheet carrier concentration in the channel (N_{CH}) is directly proportional to the gate overdrive voltage given by,

$$N_{CH} = \frac{1}{q} C_{AlGaN} (V_{GS} - V_T) \tag{3-2}$$

Where C_{AlGaN} is the capacitance per unit area of the AlGaN layer. Assuming α_H remains the same and noise is measured at a constant V_{GS}. A change of V_T of around

0.2 V causes a change of the channel carriers which in turn changes S_{ID}/I_D^2 by a factor of around 4. This explains the noted shift in the drain current noise both during and after stress. Therefore, it can be concluded that the channel is immune to any degradation due to high gate reverse biases.

Gate Current Noise Characterization

Figure 3-6 shows the pre and post stress normalized gate current power spectra. An increase by a factor of 10 is seen in the spectra. On the other hand the DC gate leakage current measured at V_{GS} = -1.23 V increased only by a factor of 2. Initially it seemed that this was analogous to the drain noise increase which would recover once the stress was removed. It was found that this increase was permanent and no recovery could be obtained even several weeks later. Furthermore, it showed a temporal instability with Lorentzians shifting positions in the frequency domain. Two level switching was also observed in the time domain with varying characteristic times. This phenomenon was observed in a previous work and was linked to an electrical activation of mobile defect centers. In order to get a better understanding of these changes a low temperature noise measurement was performed to reduce the temporal instability of the Lorentzians. The device was cooled to 77K and noise was measured. Interestingly, in the triode region at V_{DS} = 80 mV a $1/f^{\gamma}$-type spectra was obtained but when the device was biased in saturation at V_{DS} = 2 V a large Lorentzian emerged in the gate noise spectra (Figure 3-7). This same behavior was seen when the source and drain were swapped.

Discussion

In this part a critical analysis of the physical origins of the results is performed. The results suggest that two dominant mechanisms are at play. First are the transient effects

due to existing defects which affect DC device characteristics and drain current noise. Second are the permanent changes in the material structure which changes the gate current noise in a significant way. Earlier it was shown that threshold voltage shifted positively during stress and later recovered to pre-stress levels. The threshold voltage is typically determined by the gate metal-semiconductor barrier height, band-discontinuity at AlGaN/GaN interface, polarization charges and fixed defect states in the barrier [34]. It was found that forward biasing of the gate to source-drain diode led to a faster recovery of threshold voltage to pre-stress levels. Studies performed on similar devices (GaN-on-Si) by other groups have shown that threshold voltage also recovers by optical excitation via UV light illumination with a frequency comparable to the band-gap of the barrier [35]. The band discontinuity and polarization charges would be invariant to both optical excitation and forward biasing of the gate-to-channel diode. Furthermore, a change in these parameters during stress would be permanent in nature and would be irreversible unlike what was observed. Therefore, it can be assumed that threshold voltage shift is due to the charging and discharging of fixed defect states in the AlGaN barrier. An effective estimate of the trap density can be made if it's assumed that a fixed sheet charge is located in the AlGaN barrier near the channel,

$$\Delta V_T \cong \frac{Q_F}{C_I} = \frac{qN_T d_{AlGaN}}{\varepsilon_{AlGaN}} \tag{3-3}$$

A positive shift of 0.2 V corresponds to an effective trap density (N_T) of 5 x 10^{11} cm^{-2}. This value is smaller than the typical polarization charges at the interfaces [36]. It has been shown that in AlGaN/GaN HEMTs at high reverse gate voltages ($V_{GS} << V_T$) the electrons predominantly tunnel from the gate edges [36]. Some of these electrons

can get trapped in the existing defect states in the AlGaN layer which will cause an increase of the threshold voltage. This is shown in process P2 in Figure 3-8. This event will also lead to a change in the potential profile in the AlGaN barrier. Charged defect states decrease the band bending which in turn increases the barrier-width as seen by the tunneling electrons from the gate metal. The tunneling probability of electrons will thereby decrease resulting in reduced gate leakage current. Both these effects were visible in the measurement results. When the stress is removed the trapped electrons beneath the gate slowly de-trap which leads to a recovery of the threshold voltage. Shown in process P1 in Figure 3-8. Gate current noise results demonstrated that a permanent change took place in the environment seen by the electrons tunneling from gate to semiconductor. In a previous work it was noted that $1/f^{\gamma}$ component of the spectra is due to the trap state fluctuation at the metal semiconductor Schottky interface [33]. Since it increased by a factor of 10 it can be concluded that near interface defect density increased at the metal semiconductor junction and additional trap states were created. Low temperature measurements pointed out that when the device was biased at V_{DS} = 2V where the DC drain current was saturated, the gate noise increased dramatically. The same measurement was performed when source and drain terminals were swapped and a similar increase was observed. In the former experiment the vertical fields at the gate drain edge become larger than fields at the center. In the latter case, the vertical fields at the gate source edge become larger than fields at the center. This leads to an increase in tunneling probability at the edges and more electrons at the Fermi level of the metal can access the trap states in the AlGaN leading to discrete switching noise. It is proposed that during stress new trap states were generated in the

AlGaN barrier beneath both the gate edges which are most probably located above the metal Fermi level. Although it has been shown that inverse-piezoelectric breakdown not only degrades the AlGaN barrier but also the channel region in the GaN buffer [18]. The results presented in this work do show degradation of the AlGaN barrier but not the channel. This could be due to relatively low stress voltages used in this work and/or a smearing down of peak electric field due to source field plate. Also the degradation is below the onset of the “critical voltage” for major breakdown. This demonstrates that low frequency noise is an insightful tool to predict early degradation at relatively low stress levels which eventually leads to large performance degradation at higher voltages. This large degradation not only affects noise but also change the DC characteristics drastically.

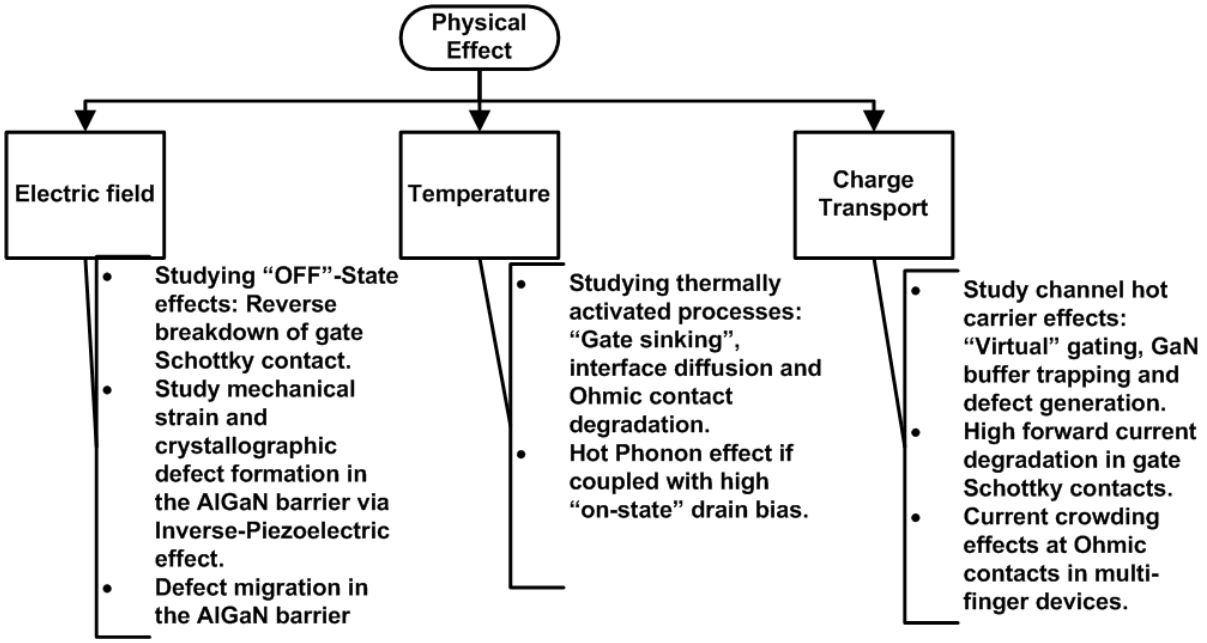

Figure 3-1. Illustration of prominent failure mechanisms in AlGaN/GaN HEMTs as a function of physical effects. This work limits its study to the electric field driven effects particularly in the "OFF"-state.

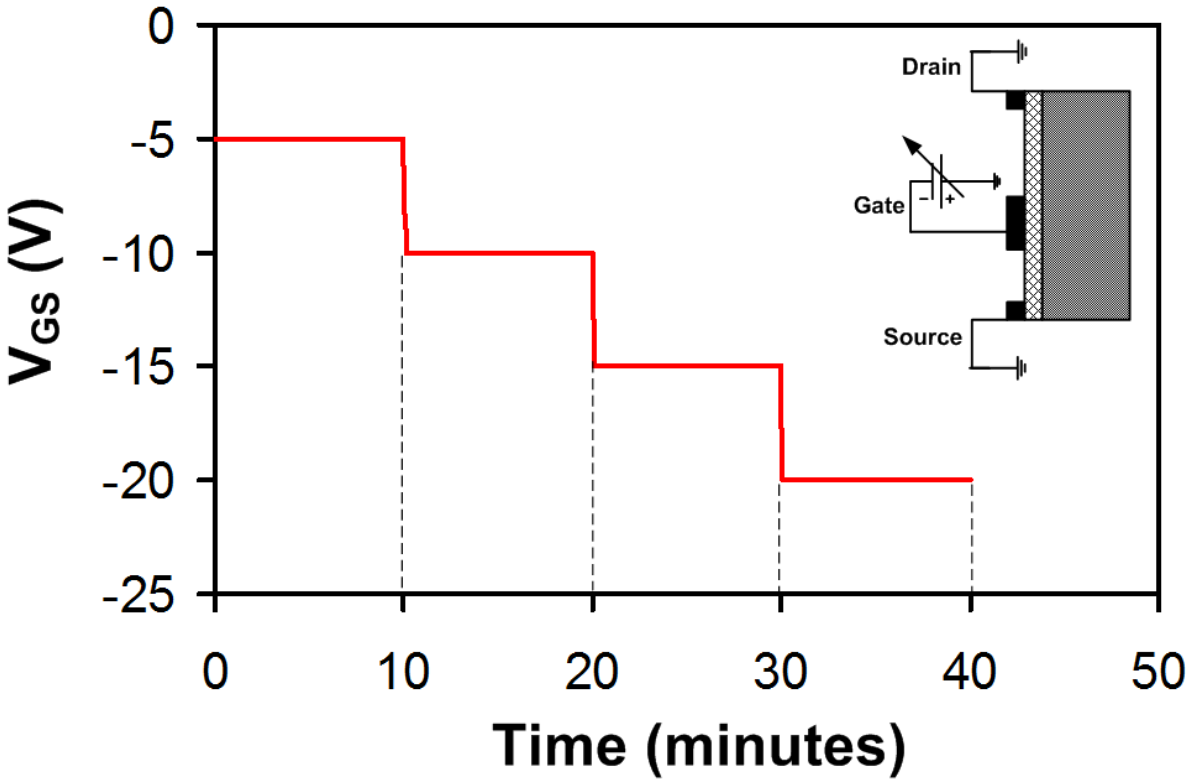

Figure 3-2. Reverse gate voltage step stress protocol. The solid line indicates the step-voltage stress from -5V to -20V applied to the gate terminal where source and drain are connected to ground (Biasing shown in the inset). The measurements are performed at the end of the 10 min stress period (indicated by dashed line) by measuring I_{DS}, I_{GS} v/s V_{GS}, drain current noise and gate current noise.

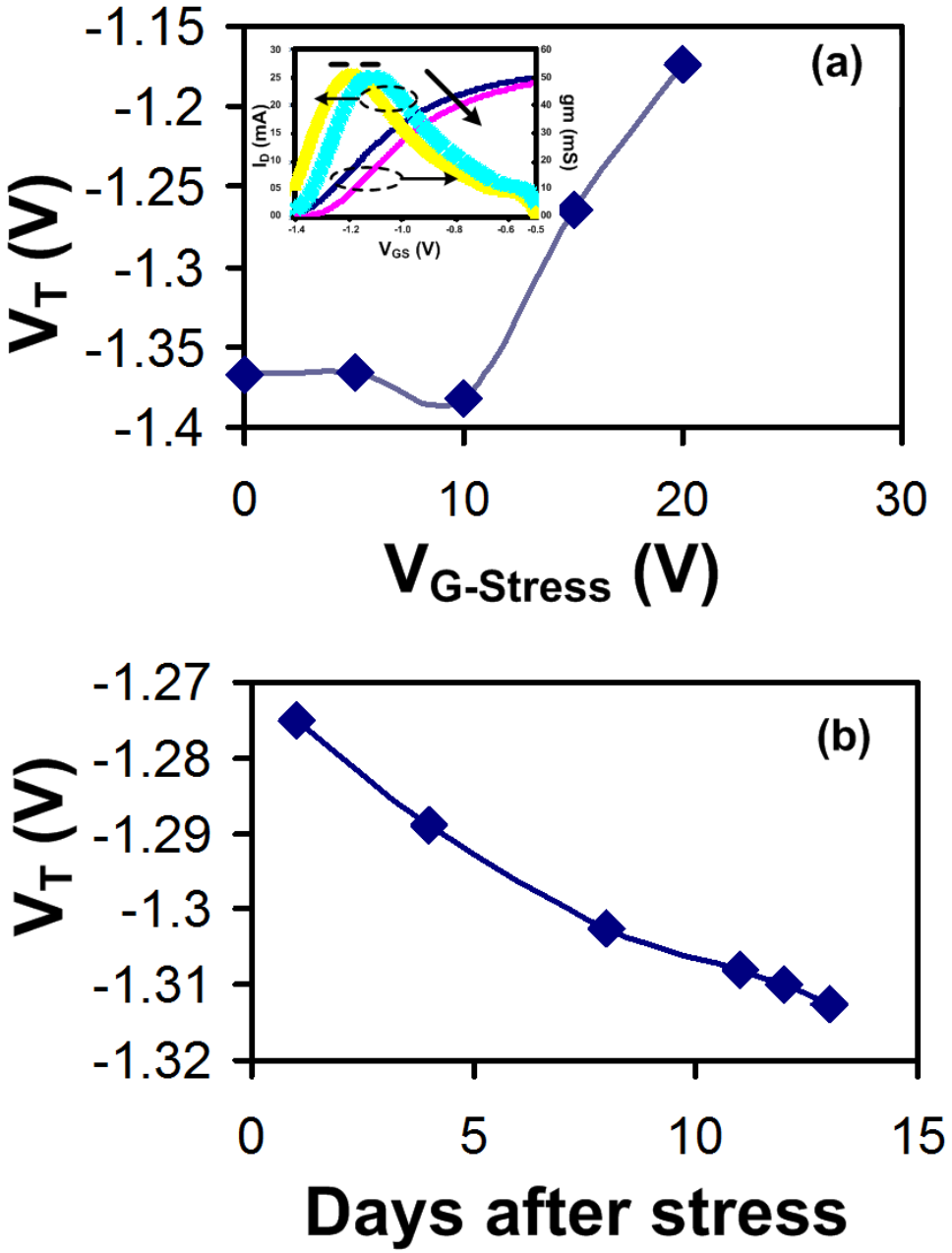

Figure 3-3. Threshold voltage changes during and after stress. Top figure (a) shows the increase of threshold voltage during stress. The inset in (a) depicts the pre and post stress drain current transfer (I_{DS}-V_{GS}) characteristics at V_{DS}=80 mV. The slow threshold voltage recovery is shown in bottom figure (b).

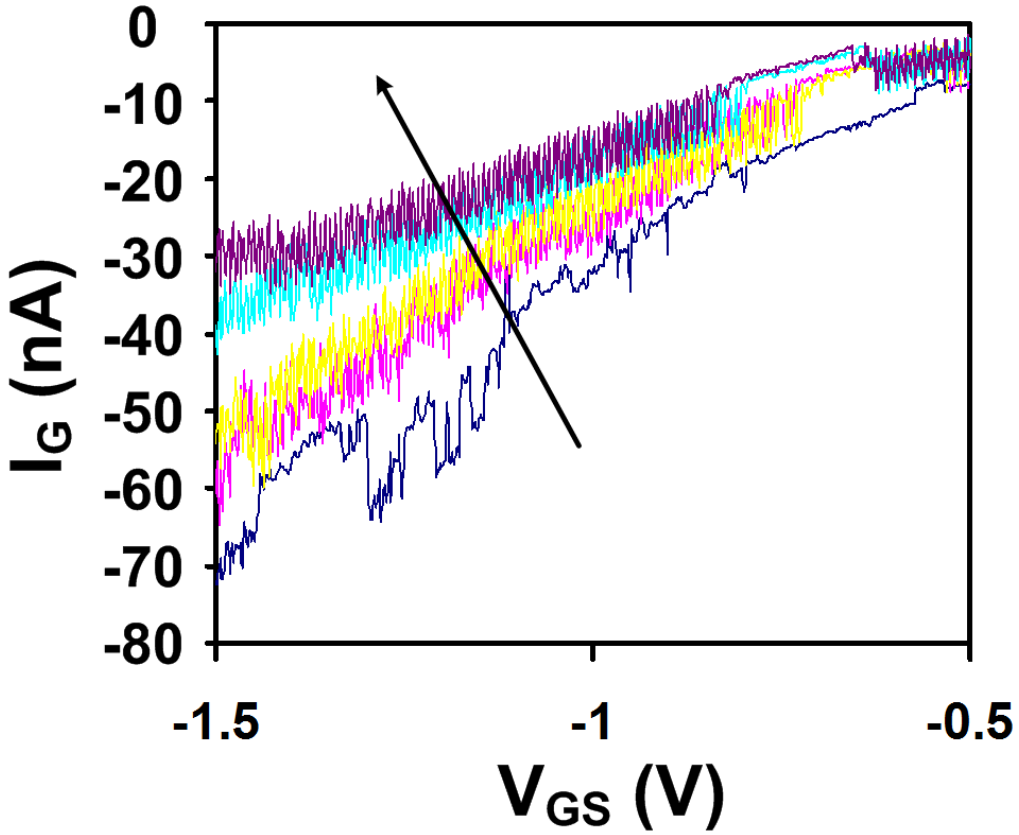

Figure 3-4. The evolution of the gate leakage current measured at V_{DS} = 80 mV during stress is shown at each stress-step. An overall decrease is seen (indicated by the arrow) as stress is increased.

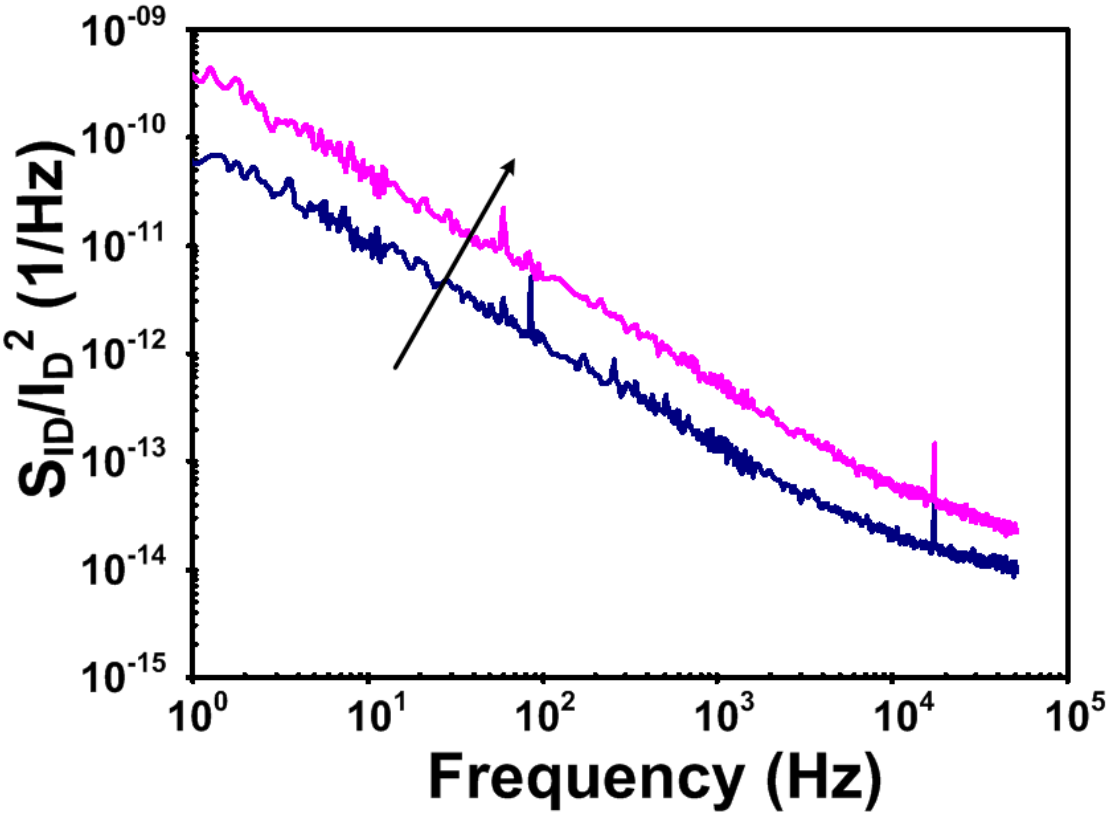

Figure 3-5. Normalized drain current spectra (S_{ID}/I_D^2) for pre and post stress cases. An increase by a factor of 4 is seen indicated by the arrow. This increase was found to temporary and it fully recovered to its pre-stress levels a few weeks later as the DC threshold voltage recovered.

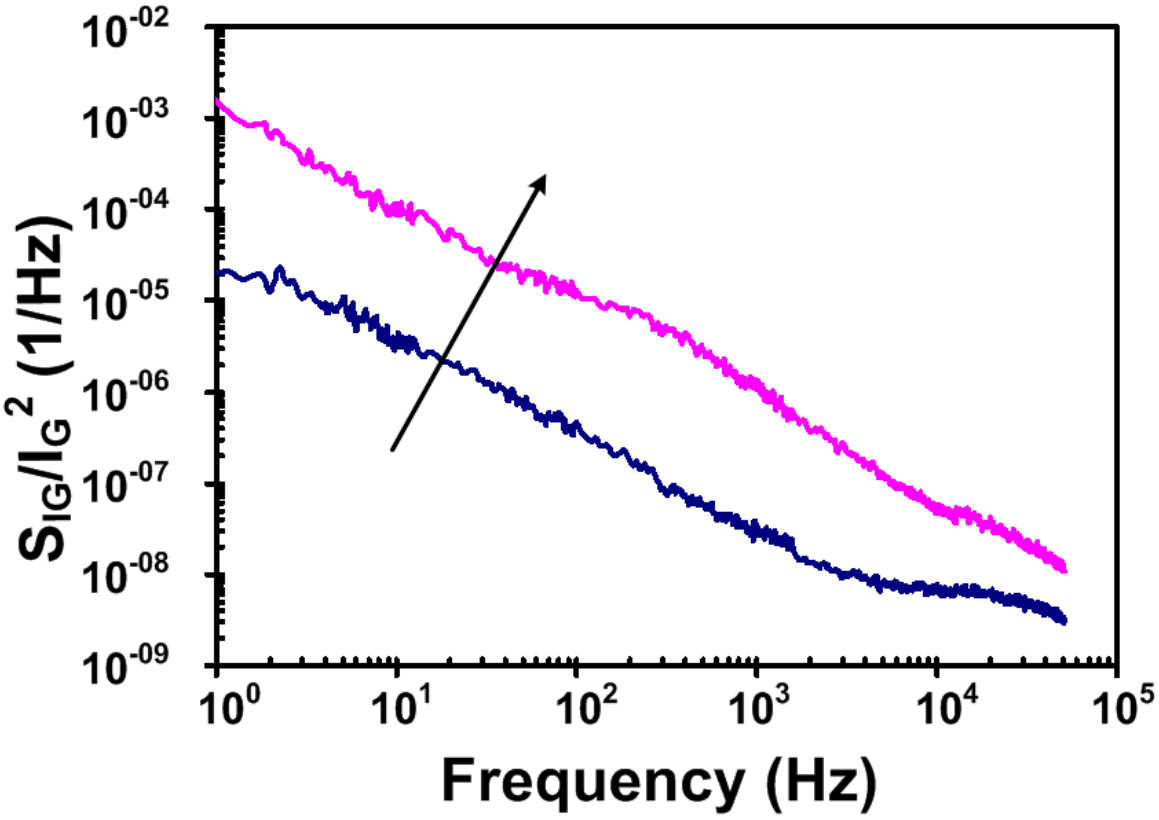

Figure 3-6. Normalized gate current noise (S_{IG}/I_G^2) for pre and post stress cases. An increase by a factor of 10 can be seen (indicated by the arrow). This shift was found to be permanent and did not recover.

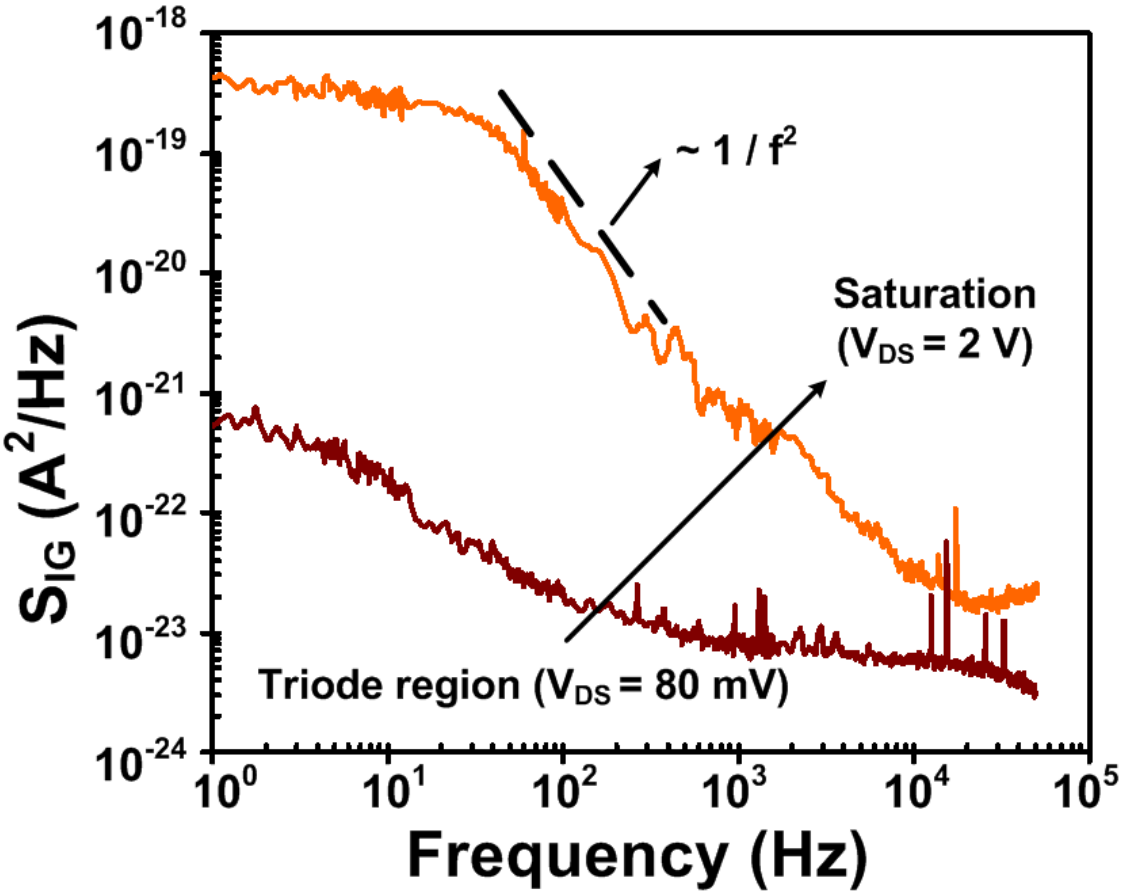

Figure 3-7. Gate current noise (S_{IG}) measured at 77 K for two DC biasing in triode region and saturation. A drastic increase of noise is seen in saturation with a distinct Lorentzian at a corner frequency of 30 Hz.

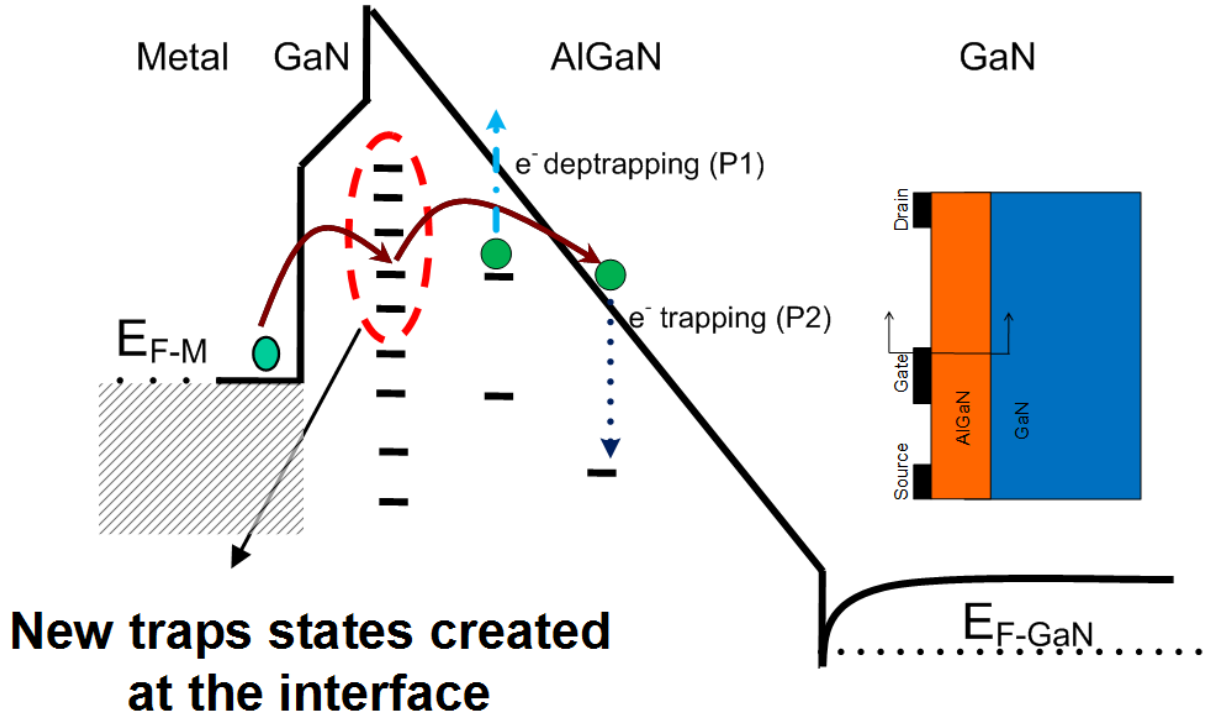

Figure 3-8. Conduction band diagram of the cross-section at the gate-drain edge (shown in the device structure on the right). Electrons tunneling in and out (shown in solid arrows) contribute to the increased DC gate leakage current and gate current noise. New trap states are created (indicated by dashed circle) in the AlGaN barrier which are above the metal Fermi level (E_{F-M}). P1 (dash-dot arrow) shows the de-trapping of electrons from the existing traps which contribute to recovery of threshold voltage after stress. P2 (dotted arrow) shows the trapping of electrons which tunnel from the gate terminal during stress. They lead to an increase of the threshold voltage.

CHAPTER 4
HIGH CHANNEL ELECTRIC FIELD STRESS EXPERIMENT

Motivation

In the previous chapter it was reported that the channel is stable and does not degrade under high gate electric field stress. Now, the focus is on the channel.A set of different stress conditions were applied to the device to isolate physical mechanisms viz. hot carrier injection (HCI), inverse piezo-electric effect, self-heating effect and a combination of self-heating and HCI. The focus of this study has been limited to only short term stresses. In each case the noise was measured before and after stress respectively. A low bias (V_{DS}=80 mV) transconductance measurement was also performed during and after stress.

Experimental Setup and Results

Experimental Setup and Stress Methodology

The devices used for this study have the same structure as the ones that were used in previous experiments. An experimental setup was developed to perform automated electrical stressing, DC I-V characterization and drain and gate current LFN characterization (see Figure 4-1) using the Agilent VEE instrument control program. An Agilent E5252A is used to switch between a high power power supply unit (PSU) and a parameter analyser. For DC characterisation, transconductance I_D-V_{GS} and I_G-V_{GS} were monitored. This was measured in the triode region at a low V_{DS}=80 mV. LFN measurements were also performed in the triode regime of the HEMT via a 2-channel Agilent 35670A. The noise measurement setup is same as shown in chapter 2. The DC bias voltages were chosen in such a way that during noise measurements low currents

(I_D<25 mA) and low voltages (V_{DS}=80 mV) are present in the device. Thus, the measurements were from a stress point of view electrically benign and non-destructive.

Four different types of stress conditions were applied to the devices which are mapped to the typical I_D-V_{DS} load line DC biasing shown in Figure 4-2. The four points invoke a combination of physical failure mechanisms like high self-heating (P_D=$I_D V_{DS}$), hot-carrier injection (E_{CH}~V_{DS}) and inverse-piezoelectric effect. The four points can be expressed as four quadrants starting anti-clockwise from the top right.

Quadrant I: V_{DS} = 20 V at V_{GS} = -1.7 V, I_{DS} = 0.115 A/mm for 5 minutes. The device is stressed at constant voltage and channel current is monitored during stress.

Quadrant II: V_{DS} = 2 V at V_{GS} = 2 V, I_{DS} = 0.2875A/mm for 30 minutes. Again, constant voltage is applied.

Quadrant III: V_{DS} = 0 V at V_{GS} = 0 to -20V (-5 V increment), 10 minutes each step. Here, the constant voltage is stepped after 10 minutes of stressing.

Quadrant IV: V_{DS} = 10 to 30 V (5 V increment) at V_{GS} = -4 V. The channel current (I_{DS}) at 30V stress was ~ 15 µA/mm.. Here again, constant voltage is stepped after 20 minutes of stress.

Figure 4-2 shows also the key changes in LFN in either drain or gate currents for each quadrant. Also shown is the corresponding change in the transconductance of the device in the triode region.

Results and Discussion

The results indicate that there are two mechanisms at play. One is a transient effect like a threshold voltage shift due to electron trapping at deep levels in the AlGaN barrier layer during stress and de-trapping subsequently. Second is a permanent change due to trap creation and/or migration which may lead to effects like permanent

degradation of the low-field mobility and gate leakage currents. To isolate these phenomena, noise and DC measurements were carried up to several weeks after the stress procedures outlined above.

Quadrant I test conditions were equivalent to a high self heating and hot carrier injection environment for the device. It was observed that the drain current noise drastically degraded after the stress by almost one order of magnitude. This also resulted in a factor of two reduction in peak transconductance in the linear region. Both these changes were found to be permanent and did not show any recovery. It is interesting to point out here that right after stress, there was a positive shift in the threshold voltage of the device which later recovered to the pre-stress level. Therefore, this V_T shift was found to be a transient effect due to electron trapping and subsequently detrapping in existing trap states in the AlGaN barrier layer. By measuring channel noise as a function of gate bias it was determined that this degradation occurred in the gated part of the channel (Figure 4-3). A Hooge parameter was calculated using the classical phenomenological equation,

$$\alpha_H = fN\left(\frac{S_{I_D}^2}{I_D^2}\right) \tag{4-1}$$

Here, I_D is the DC drain current at a gate bias of -1.3 V where the noise measurement is also performed. It is important to point out here that the DC channel current also decreased after stress. This effect is instrinsically cancelled out since the Hooge parameter is dependent on the drain current normalized channel noise spectral density ($S_{I_D}^2/I_D^2$) and therefore, it is an indicator of the AlGaN/GaN channel interface trap density. The number of electrons in the channel (N) was determined by measuring the C-V characteristics of the gate-to-source/drain diode. A Hooge parameter $\alpha_H = 1.5 \times 10^{-}$

^{2} is calculated which is higher than the pre-stress α_H of ~ 10^{-3} indicating a 15× increase of trap density at the AlGaN/GaN interface. The gate current noise did not show any major changes in this regime. It is interesting to observe that such a large degradation can occur at such short duration. Most HCI related degradation mechanisms in these devices have shown relatively long time rates viz. few hours [37]. Therefore, hot-carriers alone cannot lead to this large degradation. The role of localized temperature increase leading to defect diffusion cannot be ruled out. More insights into these mechanisms are probed in the next chapter.

Quadrant II test conditions were predominantly self-heating effects and the drain noise characteristics showed a slight decrease due to the threshold voltage decrease. This later recovered to pre-stress levels when the threshold voltage recovered. It was concluded that no permanent degradation took place during this condition. The channel temperature is fairly uniform in this regime thus; most of the heat is spread out uniformly in the channel. It is therefore, not surprising that self-heating alone does not cause any degradation.

Quadrant III is a situation where only the gate stack was stressed since the source and drain are grounded. This is the same experiment that was performed in chapter 3.

The final quadrant (IV) stresses the device in the hot-carrier regime without self-heating. Threshold voltage shifts occurred during stress but no net shift occurred after stress. Both drain and gate noise characteristics did not show any post-stress change. Again no permanent degradation occurred in this regime. It seems that not enough hot-carriers were generated in the channel to cause changes.

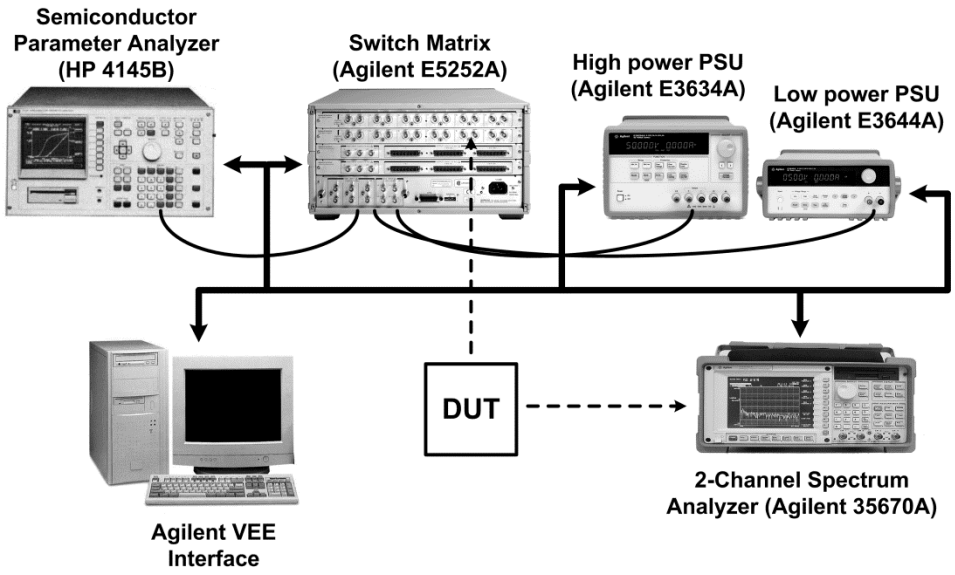

Figure 4-1. Experimental setup for performing electrical stress and LFN characterization. The thick solid black lines show the GPIB connection to the computer. Thin solid lines show the electrical connections between instruments. Dashed arrow lines show the device connection to either noise setup (Agilent 35670A) or stress/I-V setup via a switch matrix (Agilent E5252A).

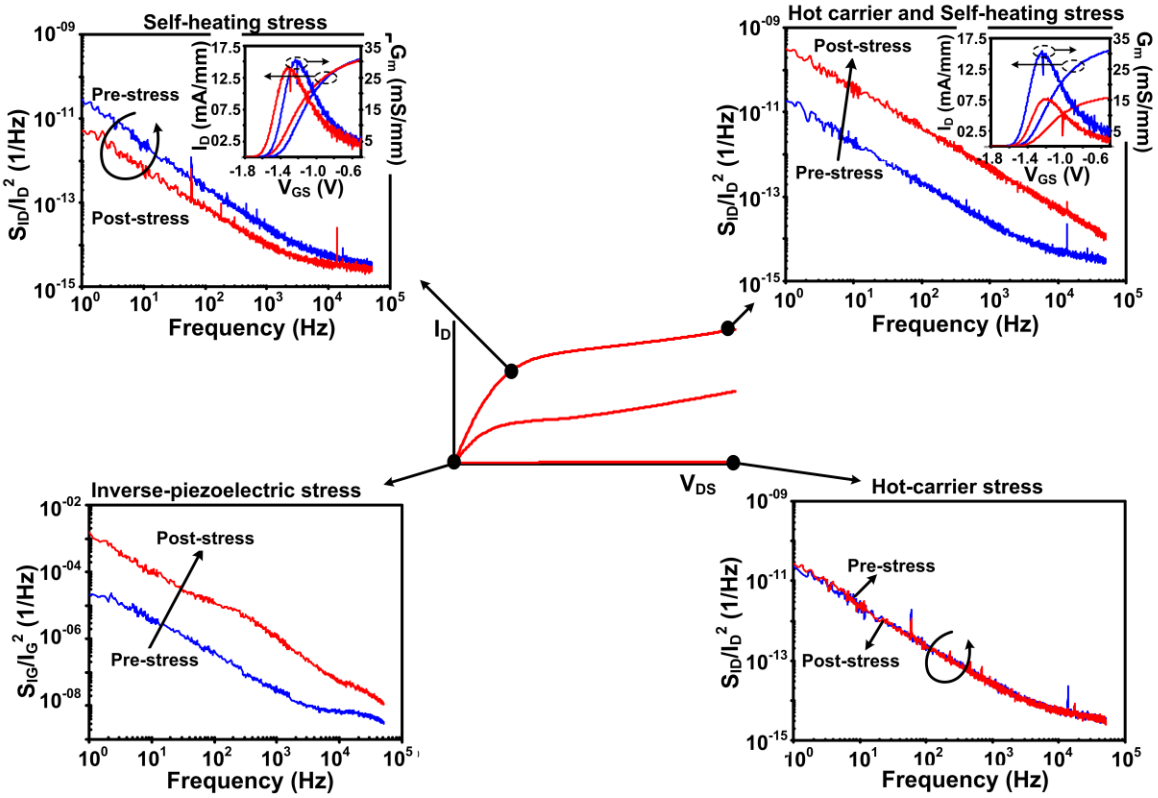

Figure 4-2. Summary map of stress effects. Quadrants I, II and IV show pre- and post-stress normalized drain noise spectra (S_{ID}/I_D^2) in blue and red lines respectively. The insets in quadrant I and II are the transconductance and I_D-V_G in the linear region for pre- and post-stress (blue and red lines respectively). Quadrant III shows normalized gate noise spectra (S_{IG}/I_G^2) before and after stress.

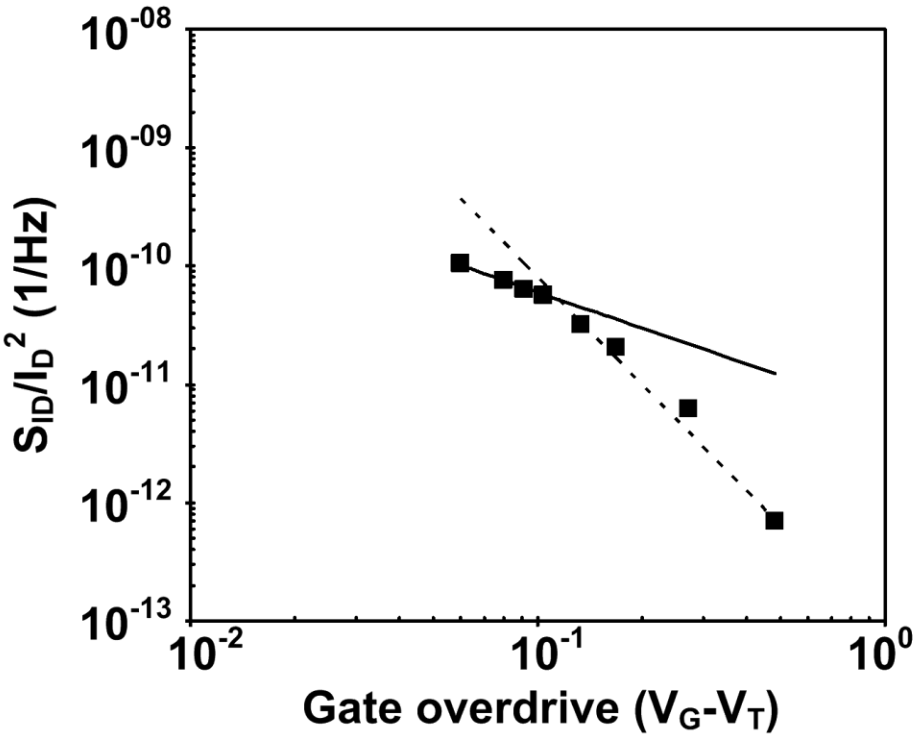

Figure 4-3. Normalized drain current noise as a function of gate overdrive voltage. Square dots are the measured values. Solid and dashed lines are the V_G^{-1} and V_G^{-3} fits respectively. This dependence is a clear indicator of noise originating from the gated channel [33].

CHAPTER 5
HOT-CARRIER EFFECTS AND NOISE TEMPERATURE SPECTROSCOPY

Motivation

Earlier it was found that in the channel region, the combined effect of self-heating and hot-carrier stress creates a permanent increase of the defect density at the AlGaN/GaN interface. Also it has been recently pointed out that this regime of operation becomes important at higher RF power levels for a device biased in the power amplifier mode [38]. High frequency noise measurements are known to give physical insights into hot-carrier and self-heating effects [39], [40] but very few studies have been performed on gated devices under realistic bias conditions. This chapter shows the results of using both low frequency and high frequency noise as a spectroscopic tool to study device degradation and failure mechanisms at typical bias regimes in actual devices.

Experimental Details

Figure 5-1 shows the experimental setup to measure the high frequency device noise which is based on the circulator method developed by Gasquet [41]. The noise was measured at 2.20 GHz beyond the spectral range where the 1/f-like noise observed at low frequencies has a contribution. The device is biased at a typical class AB mode of operation with the gate voltage greater than the threshold voltage to induce a channel at a constant drain bias. The measurements were not performed under pulsed condition thereby allowing the lattice temperature to reach steady state at each bias. The gate terminal was AC-open circuited with the help of a tuner to minimize the impact of both induced gate noise and thermal noise associated with gate resistance on the channel noise. It was found that at high drain biases the drain noise mainly stemmed from the channel electrons since the transconductance of the device was relatively constant

while the measured device noise temperature increased with bias. The low frequency noise was measured by the same setup shown in chapter 2.

Results and Discussion

Figure 5-2 shows the effect of various bias points of the I_D-V_{DS} load line on degradation in the channel and the gate stack. This work concentrates on the channel region and two important failure mechanisms based on self-heating and hot-carrier are explored in more detail. The methodology that is adopted here is to systematically probe each region of the load line by increasing gate and drain bias. Increasing the gate bias at a constant drain voltage will increase only the self-heating effect by allowing more carriers in the channel thereby changing the lattice temperature via increased phonon scattering. On the other hand, increasing the drain bias at a constant gate voltage will increase the channel electric-field and result in an increased electron temperature. Figure 5-3 shows the measured noise temperature of the channel at 2.20 GHz for three different gate biases as a function of drain voltage ranging from the triode to the saturation regime. Although a precise quantitative relation between the channel electron temperature and the measured noise temperature is lacking at this time, qualitative trends can be readily seen in the measurements. Figure 5-4 shows the effects of self-heating and channel voltage on the measured noise temperature in the saturation regime of device operation. The effect of power dissipation was measured by keeping the drain voltage constant at 22V and changing the gate bias from -1.2 V to -1.0 V which resulted in a drain current change from 50 mA to 100 mA. To observe the effect of drain voltage on device noise temperature the drain voltage was varied between 10 and 22V at a constant gate bias of -1.1V. The noise temperature shows a strong correlation to the channel electric field as opposed to the power dissipation. For an increase of 100% in

the drain voltage at V_{GS}= -1.1 V, the noise temperature increases by ~ 70% indicating that it is correlated to the hot electron temperature of the channel. On the other hand, a similar increase in the power dissipation ($P_D=I_D \times V_D$) in the channel raises the noise temperature by only ~ 20%.

Now that a correlation between noise temperature and channel hot-electron temperature has been established one can understand the physical mechanisms at play which cause the dramatic degradation of LFN characteristics at high drain current and voltage as shown in Figure 5-2. At high drain voltage and low channel current it was observed that no permanent degradation occurs in the channel region. Noise temperature measured in this regime pointed out that hot-carriers do indeed exist and show a correlation to the channel electric field. Thus, it can be concluded that hot-carriers alone don't seem to be causing this degradation. On the other hand when high drain bias and currents exist in the channel, the LFN shows a permanent degradation. The Hooge parameter increased 15 times from its pre-stress value. In this regime, the Joule heating in the channel is significantly higher. Therefore, it can be inferred that the observed degradation in the LFN characteristics at high drain bias and current is linked more closely to the self-heating effect which enhances the rate of degradation at the interface than the hot-electron effect alone. This has also been pointed out by other groups [9]. These results point to the role of thermally activated degradation processes in the high power regime.

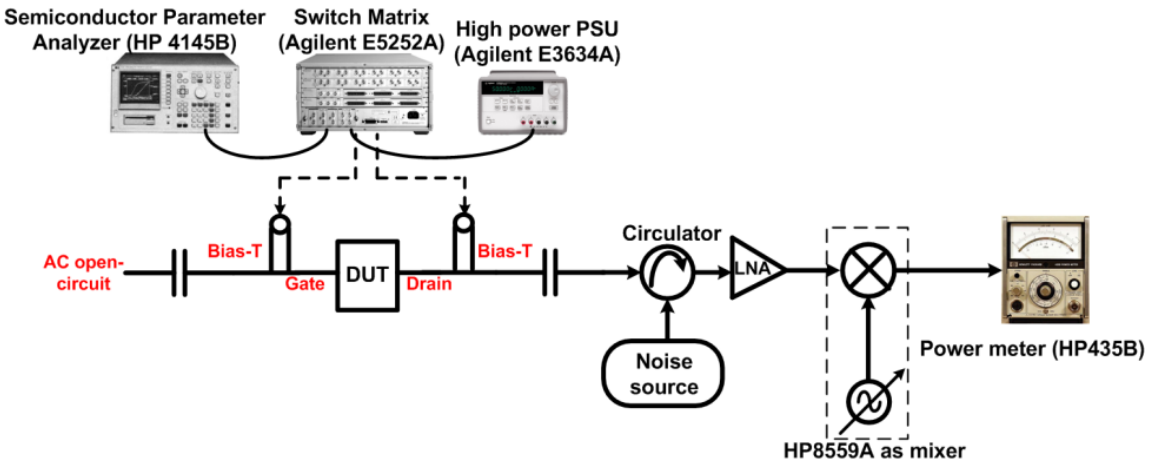

Figure 5-1. Device noise temperature measurement system. DC bias is applied via a parameter analyser and a high power PSU. The gate is kept AC open with the help of a tuner. The drain noise at 2.20 GHz is measured as a function of drain bias at three different gate biases.

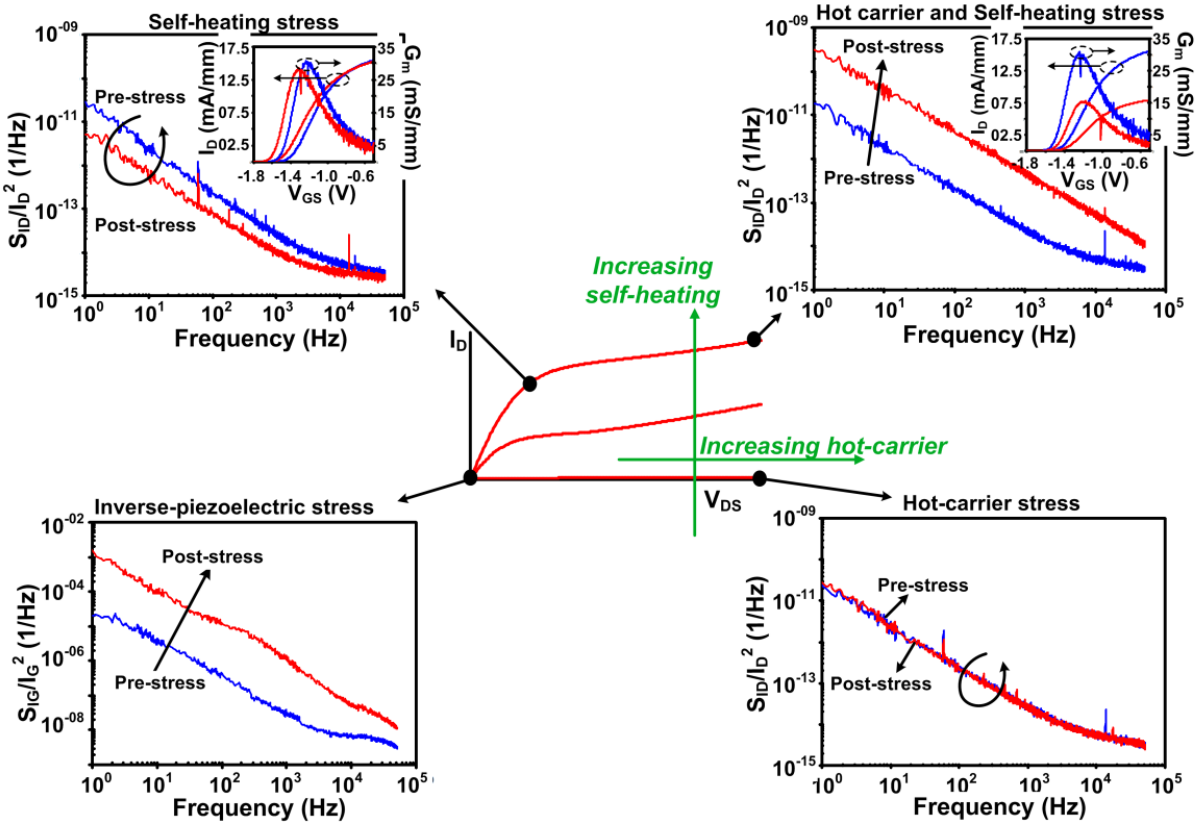

Figure 5-2. I_D-V_{DS} map showing the effect of hot-carrier and self-heating. The measured low frequency noise characteristics are shown for pre and post stressed GaN HEMTs at different stress bias points [42]. The channel is stressed with hot carrier and self-heating stress by varying drain or gate bias, respectively, keeping the other variable constant.

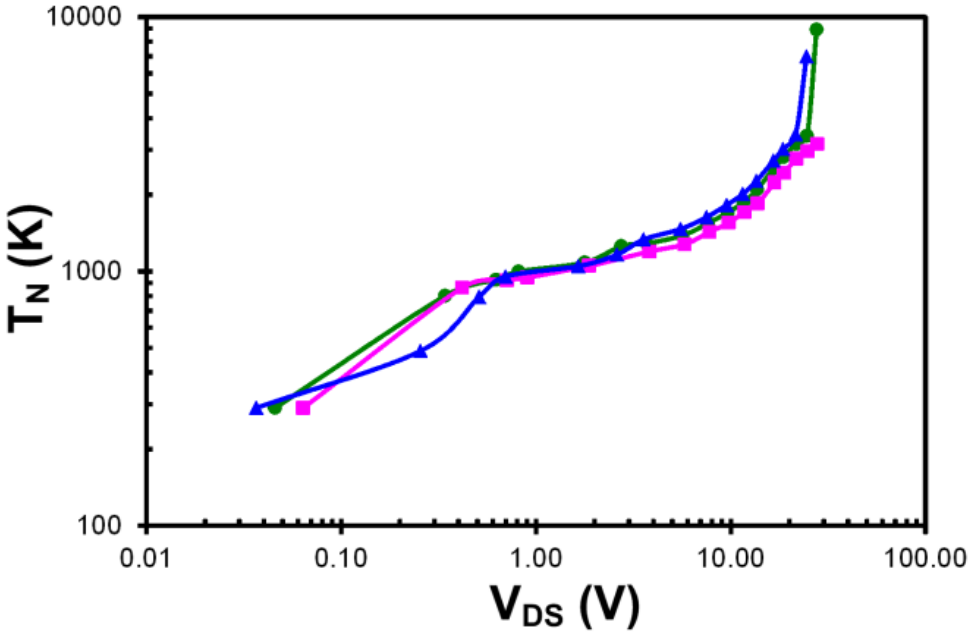

Figure 5-3. The channel noise temperature measured at 2.20 GHz as a function of drain voltage is shown for three different gate biases. Squares (■) are measured at V_{GS}=-1.2V. Circles (●) are measured at V_{GS} = -1.1V and triangles (▲) are measured at V_{GS} = -1.0V.

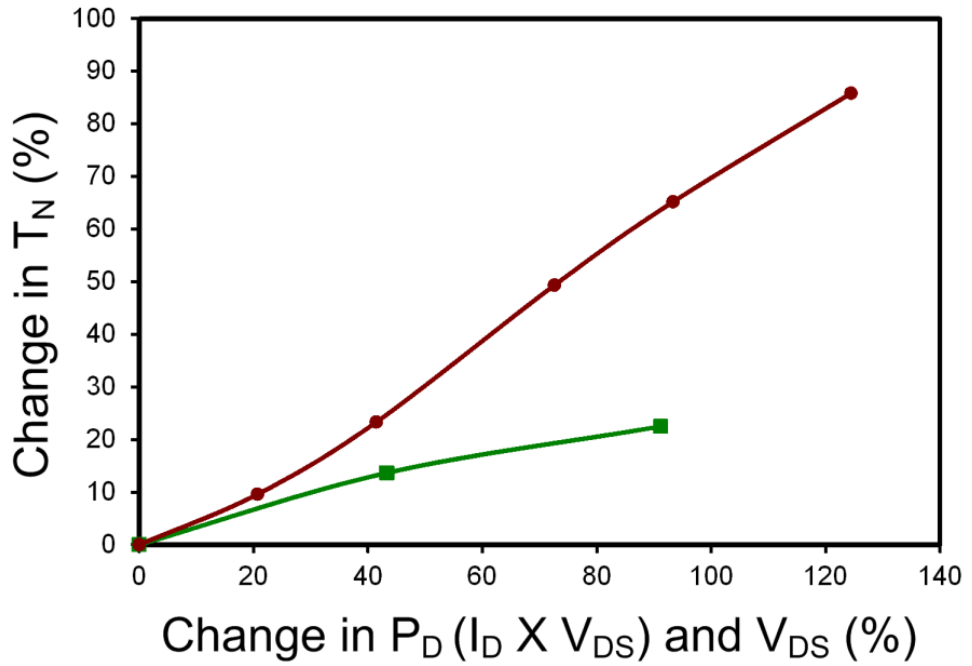

Figure 5-4. The relative sensitivities of device noise temperature to a change in power dissipation (squares) and drain voltage (circles) are shown. The channel noise temperature is more strongly correlated to the drain voltage than to power dissipation.

CHAPTER 6
RF RELIABILITY OF GAN HEMTS

Motivation

As device designs are optimized for achieving higher RF power levels there is an increased need to assess their long-term reliability in actual operating conditions. DC stress tests are typically performed to determine RF reliability but this approach has its own challenges. For instance some of the failure mechanisms which are active under DC stress may not be the same under RF operation [38]. But the relative simplicity of the tests renders them useful. A better experiment is the RF operating life time test which is performed to extrapolate RF reliability of the device. But high temperatures used in the stress accelerate thermally activated processes more than the electric field driven processes [43]. In this regards one practical test than can be performed readily and mimics RF failure mechanisms more closely is the RF overdrive stress. Power amplifiers are typically biased for higher gain saturation to optimize both efficiency and output power [44]. Also, since these devices are biased at the edge of gain compression levels, a slight change (transient or permanent) in the device characteristics can lead to impedance mismatch and thus, drive the device into higher gain compression levels or generate spurious device oscillations. This type of stress not only enables a study of RF failure mechanisms but can also give insights into the limits of the device to withstand high RF power levels [45]. This work uses low frequency noise measurements as a reliability characterization tool to systematically probe microscopic degradation in the electronic structure of the gate stack and the channel region under high RF overdrive condition. Although similar studies have been done on GaAs devices, very few studies exist on GaN HEMTs [46], [47], [38].

Experimental Details

Experimental Setup and Stress Methodology

A semi-automated experimental setup is developed to perform RF stressing, DC characterization and low frequency noise (LFN) measurements (Figure 6-1). A circulator is utilized on the RF generator side to measure reflected power from the gate terminal. It gives the ability to monitor changes in the power gain of the device during stress due to variation in the input impedance due to possible trapping or self-heating effects. An Agilent 35670A spectrum analyzer is used to simultaneously measure gate and drain current LFN. The details of the noise setup are in chapter 2. The complete setup is computer controlled via Agilent VEE. The device was biased in a class AB mode of operation at V_{DS} = 28 V and I_{DQ} = 25 mA/mm. The static DC power dissipation in the device was significant, with package temperatures reaching 65 °C during operation. A channel temperature of 100 °C was determined based on a thermal resistance of 23 °C/W which is a reasonable approximation for this device. The device test fixture was kept at the ambient temperature of 25 °C throughout the stress duration. RF power gain of the device was characterized before stress to determine the 3 dB and 8 dB gain compression points (Figure 6-2). A small signal linear gain of 13 dB was measured at 3 GHz. At 3 dB compression the input power is around 6 dBm and at 8 dB compression the input power is around 18 dBm. The source and load impedances were initially tuned for maximum gain in the linear regime and then kept fixed for the duration of the stress. RF stress at 3 dB and 8 dB gain compression at 3 GHz was applied for 60 minutes (Figure 6-3). The device was left to stabilize for few minutes to reach thermal quasi-equilibrium then the input RF power (P_{IN}), output RF power (P_{OUT}) and quiescent drain

current (I_{DQ}) were monitored as a function of time. Before stress application, a complete set of DC and LFN characteristics of the gate and channel were measured. It is important to point out here that RF stress with no gain compression was also performed and it was found that no degradation of the output RF power (P_{OUT}) occurred. The DC characteristics V_T, g_m and gate leakage current did not change. Gate and channel noise characteristics were also unchanged. Only higher levels of gain compressions resulted in degradation of device characteristics.

After stress, DC characteristics like threshold voltage, gate leakage current, transconductance and Gate and Drain current LFN were measured repeatedly for several weeks to differentiate between temporary and permanent effects.

Experimental Results

Figure 6-3 shows the change of RF output power during stress of 1 hour for 3 dB and 8 dB compression. Despite that these are very short-term stresses they result in significant reduction in power levels. Therefore, a systematic study of degradation can give new insights into these failure mechanisms. A significant (~ 1.5 dB) power loss takes places in the first 10 minutes of stress for high gain compression of 8 dB and thereafter the power remains relatively steady. On the other hand a 3 dB gain compression stress causes much less degradation which almost recovers to pre-stress levels in 60 minutes. It should be mentioned here that the measured RF power gain followed similar trends since the input power did not change much during stress. Figure 6-4 shows the DC I-V characteristics of the gate before and after stress. DC gate leakage current degraded significantly after stress. In the reverse bias the gate leakage current increased 10 times for 8 dB compression and 2.5 times for 3 dB compression RF stress. Figure 6-5 shows the transconductance of the device before and after 8 dB

compression stress. The peak transconductance does not change. However, there is a negative threshold voltage shift which was found to be permanent. After 3 dB compression stress the channel characteristics (not shown here) remained the same without a change in peak transconductance and threshold voltage.

The microscopic origin of the degradation was studied via gate and channel current LFN measurements. Figure 6-6 shows the evolution of the relative channel noise before and after 8 dB compression stress. The quantitative decrease of the noise agrees well with the threshold voltage shift. For the 3 dB compression stress (not shown here) the relative channel noise magnitude remains the same. The Hooge parameter (α_H) was found to be ~ 10^{-3} for both stress conditions. This is also a common value for unstressed GaN HEMTs [48]. Figure 6-7 shows the relative gate noise characteristics of the device after 3 dB compression stress. It can be seen that post 3 dB compression stress the gate 1/f noise increases slightly but also induces temporally unstable Lorentzians indicated in the figure by the dashed ellipsoids. These Lorentzians sometimes also manifested as random telegraph switching (RTS) noise in the time domain. RTS noise is a powerful tool to study single defects [5], [49].

During one of the measurements a stable RTS was found which lasted for several hours before it disappeared. RTS noise measurements were performed as a function of gate voltage to extract mean up and down time constants from the Poissonian statistics given by,

$$t_{up/down} \sim exp\left(-\frac{t}{\tau_{up/down}}\right) \quad (6\text{-}1)$$

Where $\tau_{up/down}$ is the mean up/down time constant. Figure 6-8 shows the extracted up and down time constants as a function of gate voltage. It can be seen that one of

these time constants labelled as the capture time is exponentially dependent on the gate voltage whereas the other time constant is not. The details of the mechanism are explained in the next section where the trap characteristics are determined by analyzing this data. Figure 6-9 shows the gate noise characteristics before and after 8 dB compression stress. It can be observed that the 1/f noise increases drastically after stress. Furthermore, no distinct Lorentzian components are visible in the spectra after 8 dB compression stress unlike the 3 dB compression stress which resulted in temporally unstable Lorentzians.

Discussion and Model

Channel Noise Analysis

It is clear from the channel noise characteristics that microscopic degradation does not occur in the channel region of the device. After the 3 dB compression stress there is no net change in the relative channel noise characteristics and its $1/f^{\gamma}$-type characteristic is intact. However, for 8 dB compression stress a net decrease of channel noise occurs which was found to be permanent. This was explained by the threshold voltage shift which became more negative after stress as pointed out earlier. The Hooge parameter (α_H) remained unchanged after both stresses confirming the immunity of channel region to the applied RF stress at the microscopic level.

Gate Noise Analysis

Gate leakage current, gate noise and relative gate noise increased after 8 dB compression stress. 1/f noise is typically linked to interface trap states close to the gate metal/semiconductor interface [46], [42]. A permanent increase of 1/f noise indicates that trap density near this interface increased and new defect states were generated during stress. The exact mechanism of DC gate leakage current in GaN HEMTs is still

unclear. There is however a consensus that trap states in the AlGaN barrier are responsible for high leakage currents [15], [50]. Therefore, one can conclude that the trap density indeed increased at the interface which explains the gate noise increase. One more interesting aspect of the study was the activation of temporally unstable Lorentzians which gave RTS noise in the time domain after 3 dB compression stress (Figure 6-8). It is known that a 2-level switching RTS is a single electron event with a single defect participating in the process [5].The large observed relative gate current fluctuations point to a localized nature of gate leakage current. So instead of all the 10 fingers equally participating in the DC gate leakage current only 1 or 2 fingers participate. Furthermore, one can extract the physical location of this defect along the gate-to-channel direction by studying its gate bias dependence. For a single defect the principle of detailed balance requires,

$$\frac{\overline{\tau_C}}{\overline{\tau_E}} = g\ exp\left(\frac{E_T - E_F}{k_B T}\right) \quad (6\text{-}2)$$

Where E_T is the trap energy level, E_F is the Fermi energy level, k_B is the Boltzmann constant, g is the trap degeneracy and T is the temperature. Figure 6-10 shows the 1-D energy conduction band diagram along gate-to-GaN buffer simulated using a self-consistent Poisson-Schrodinger solver [51]. Analytically E_T-E_F can be evaluated from the band-diagram,

$$E_T - E_F = q\Phi_B + x_1(k_1 V_G + E_{PGaN}) + \Delta E_C - x_T(k_2 V_G + E_{PAlGaN}) - (E_C - E_T) \quad (6\text{-}3)$$

Where φ_B is the metal/semiconductor Schottky barrier height, k_1V_G is the electric field component in the GaN capping layer resulting from applying V_G, E_{PGaN} is the electric field in the GaN capping layer due to spontaneous polarization, ΔE_C is the conduction band discontinuity between GaN capping and AlGaN barrier, x_T is the

distance of the trap location along the gate-to-GaN buffer direction from the GaN capping/AlGaN barrier interface, k_2V_G is the electric field component in the AlGaN barrier layer resulting from applying V_G and E_{PAlGaN} is the electric field in the AlGaN barrier layer due to net spontaneous and piezoelectric polarization. Assuming g = 1 and differentiating eq. 3 with respect to the gate voltage,

$$\frac{\partial(E_T-E_F)}{\partial V_G} = k_B T \frac{\partial ln\left(\frac{\overline{\tau_C}}{\overline{\tau_E}}\right)}{\partial V_G} = k_1 x_1 - x_T k_2 \cong -x_T k_2 \qquad (6\text{-}4)$$

Is the slope which gives the location of the defect (x_T) and the intercept of Eq. (6-3) gives the energy of the defect (E_C-E_T) if the values of k_1, k_2, φ_B, ΔE_C, E_{PGaN}, E_{PAlGaN} are known. Figure 6-11 shows the measured RTS data and simulated τ_C/τ_E from the band-diagram.

An excellent agreement between the measured and simulated values is obtained for a trap located 4.5 nm from the metal/semiconductor interface and 0.9 eV below the conduction band-edge of the AlGaN barrier. The experimentally measured RTS time constants were the mean values of more than hundred up and down current transitions, therefore, for uncertainty analysis they can be neglected. The energy band parameters and polarization coefficients of nitride materials exhibit very less uncertianity as seen in the literature. Therefore, the trap location (x_T) is accurate. The main source of uncertainity in Eq. (6-3) is the Schottky barrier height (φ_B). Here we assume a Schottky barrier height (φ_B) of 0.8 eV. If the uncertainty in the barrier height is taken into account then the extracted trap activation energy (E_C-E_T) becomes 0.9 ± 0.2 eV. This value agrees very well with what is reported in the literature as dislocation/extended defects related complexes or point defects loosely bound to dislocations [52–55]. It has been postulated in the literature that point defects aggregate around dislocations which act as

stepping stones for defect-assisted tunnelling [15]. Also these defects are located close to the Fermi level making them accessible from the gate terminal. It can be argued that the overall increase of the trap density in the gate stack observed at high RF stress (8 dB compression) is a result of an overall increase of these individual point defects.

Failure Mechanism

The device experiences elevated temperatures due to static and dynamic current in the channel. It has been shown in the literature that thermo-elastic stress counteracts the effect of inverse-piezo electric stress thereby increasing the robustness of the gate stack at higher temperatures [56].

This brings attention to a failure mechanism which is particularly relevant for high RF overdrive conditions. During large RF positive voltage swings on the gate, high forward currents flow through the gate Schottky junction. Figure 6-12 shows the simulated 1D conduction band-diagram at a positive gate voltage of 2V along the gate to GaN buffer layer direction without solving the transport equations. It's clear from the diagram that most of the potential drop takes place very near to the metal/semiconductor interface and GaN capping layer due to large opposite built-in piezoelectric polarization electric field in the AlGaN barrier. Thus, carriers which are injected from the 2DEG channel dissipate most of their energy into the gate metal/semiconductor junction and GaN capping layer thereby the probability of degradation increases in this region. This agrees well with the gate noise characteristics which confirmed degradation right under the gate metal. To further corroborate this, the authors performed a forward gate DC voltage stress. Figure 6-13 shows the results of DC forward voltage stress on the gate diode characteristics with source and drain grounded. It can be seen that gate leakage current degrades irreversibly after V_G=1V

DC stress. The threshold voltage (not shown here) also shifted towards more negative values. These two effects are well correlated to the DC degradation effects observed after the 8dB compression RF stress. Furthermore, noise measurements were also carried out on DC stressed devices which agreed well with results from RF stress. Thus, confirming the role of forward gate bias as a primary failure mechanism in this study.

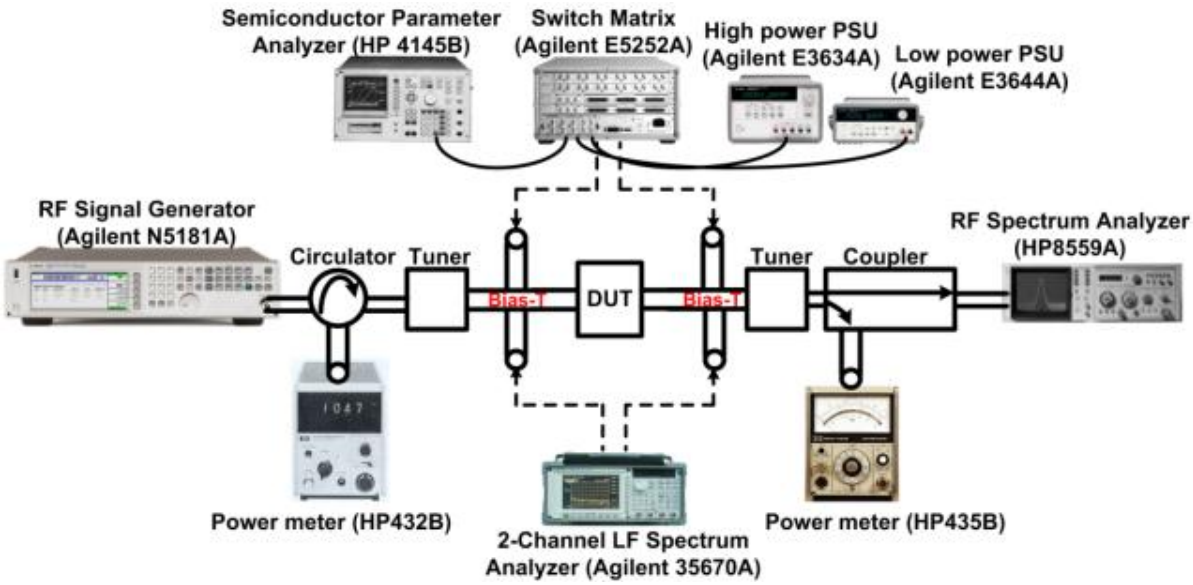

Figure 6-1. Experimental setup to perform DC characterization, RF stress and LFN measurements.

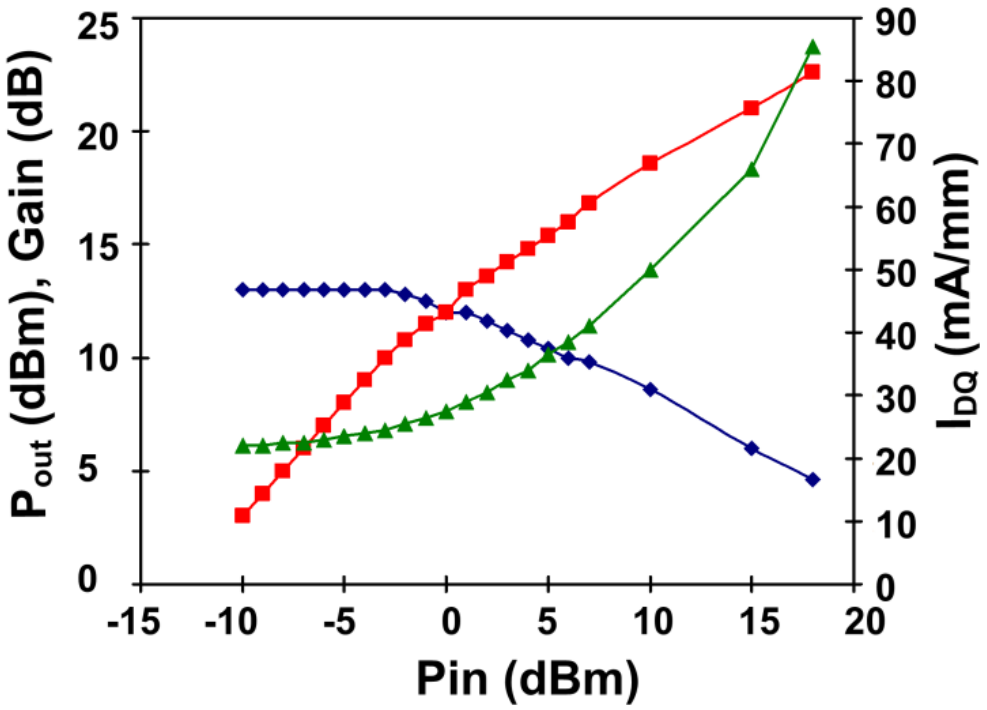

Figure 6-2. RF power measurement at 3 GHz. Power gain (diamond) and output power (squares) on the left axis. DC quiescent current (triangles) is shown on the right axis. The 3 dB and 8 dB gain compression occurs at an input power of 6 dBm and 18 dBm respectively.

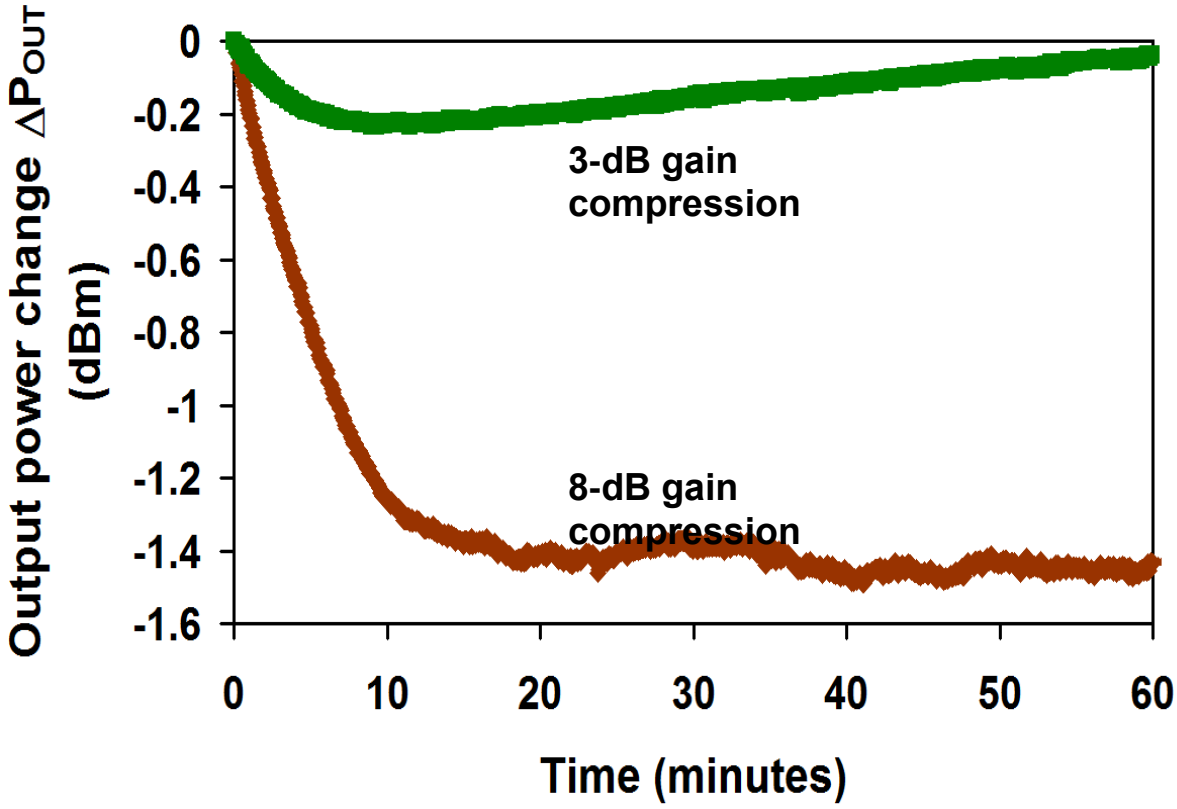

Figure 6-3. Degradation of RF output power for 3 dB (green) and 8 dB (brown) gain compression is shown.

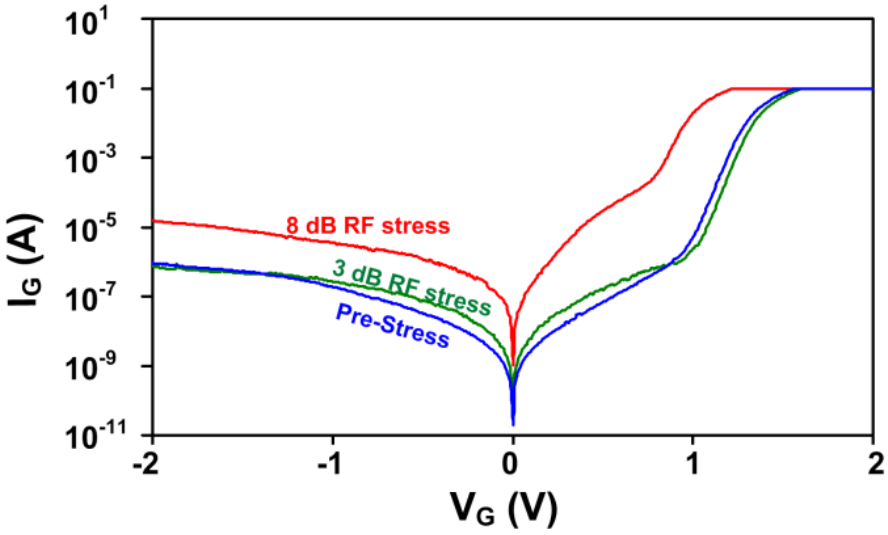

Figure 6-4. DC gate I-V for V_{DS}=0 are shown for pre-stress (blue), post 3 dB compression stress (green) and post 8 dB compression stress (red).

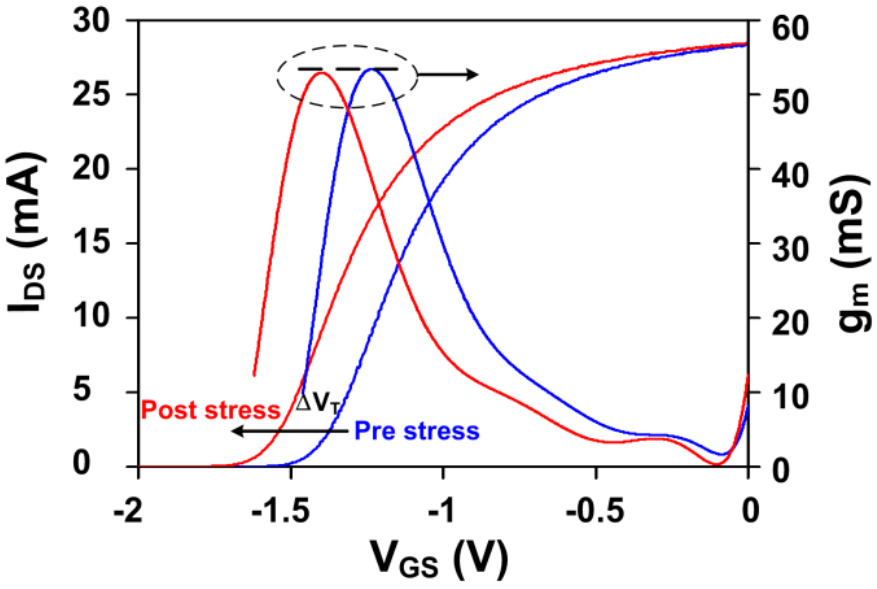

Figure 6-5. DC I_D-V_{GS} for V_{DS}=80 mV is shown for pre and post 8 dB compression stress.

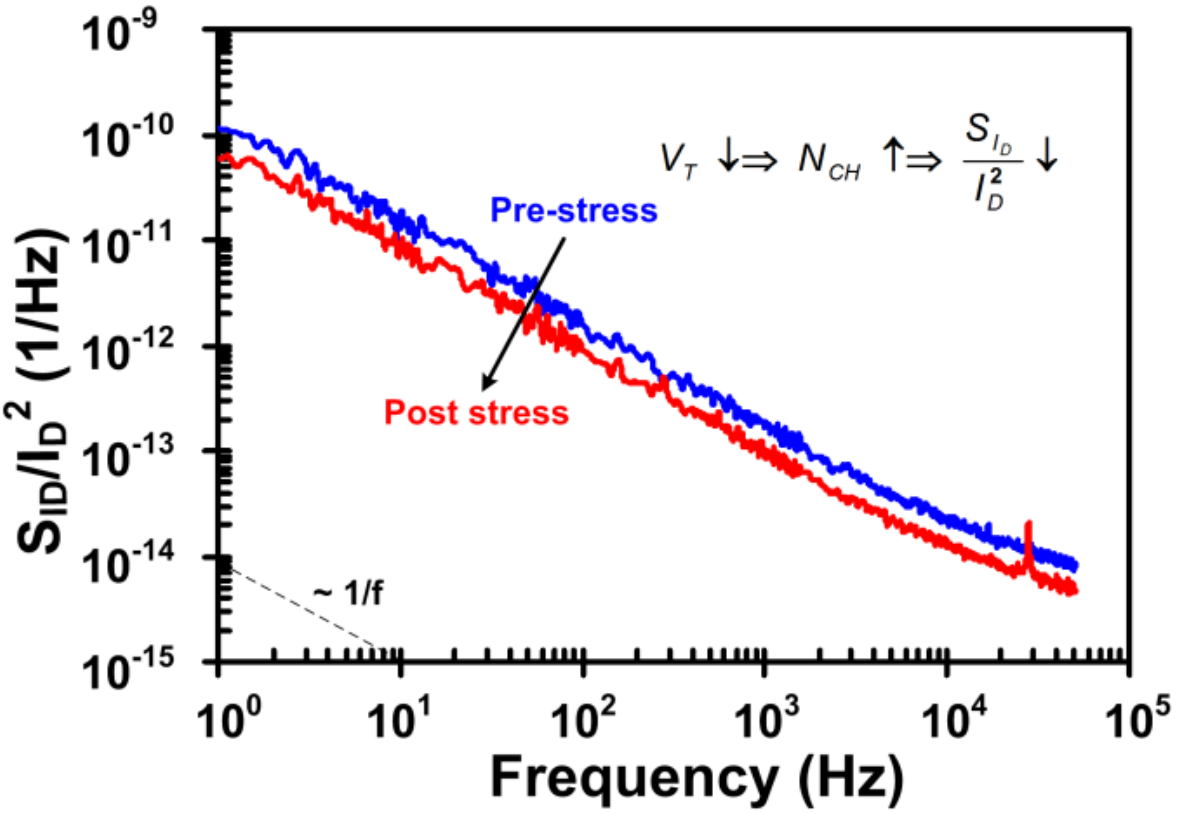

Figure 6-6. Relative channel current noise before stress (blue) and after 8 dB compression stress (red).

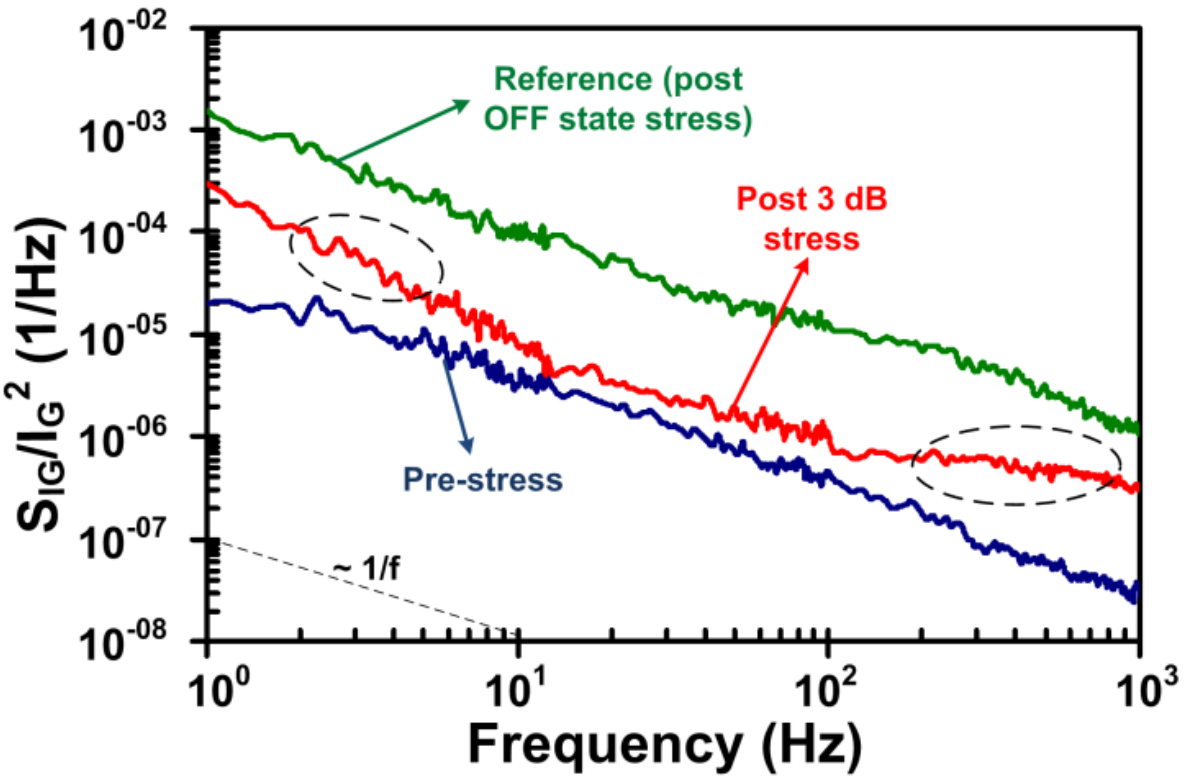

Figure 6-7. Relative gate current noise before RF stress (blue), after 3 dB RF stress (red). Noise after DC inverse-piezo electric stress (OFF state) is shown in green. More details of that work can be found in a previous work [47].

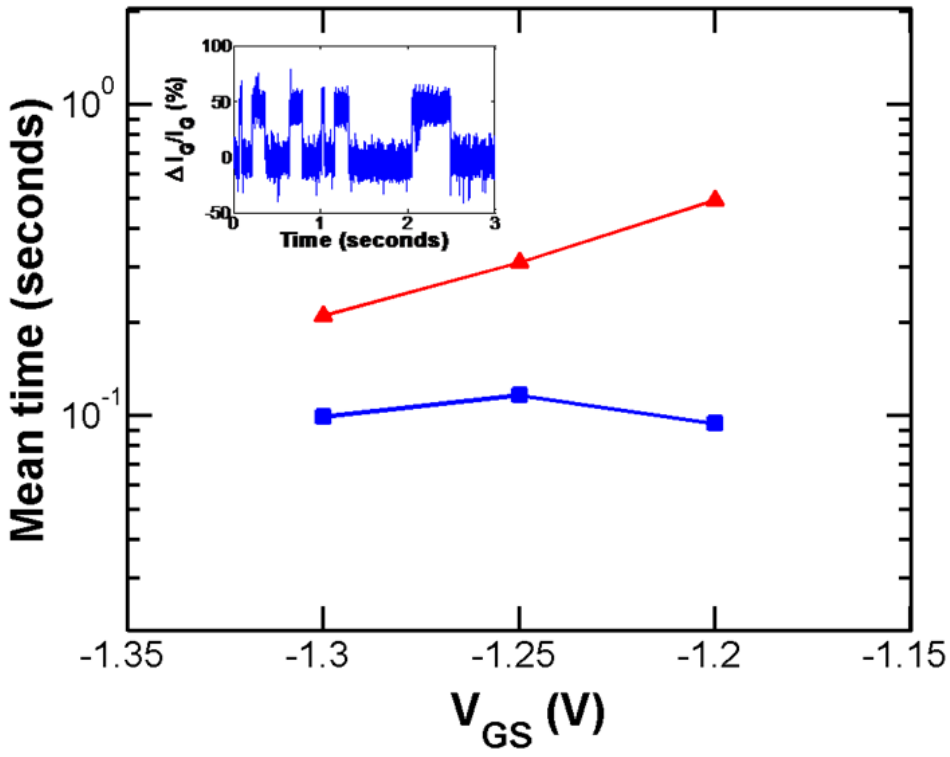

Figure 6-8. Mean capture (triangle) and emission times (square) determined from RTS noise data as a function of gate voltage (above threshold voltage). Inset shows the relative gate current fluctuation in the time domain.

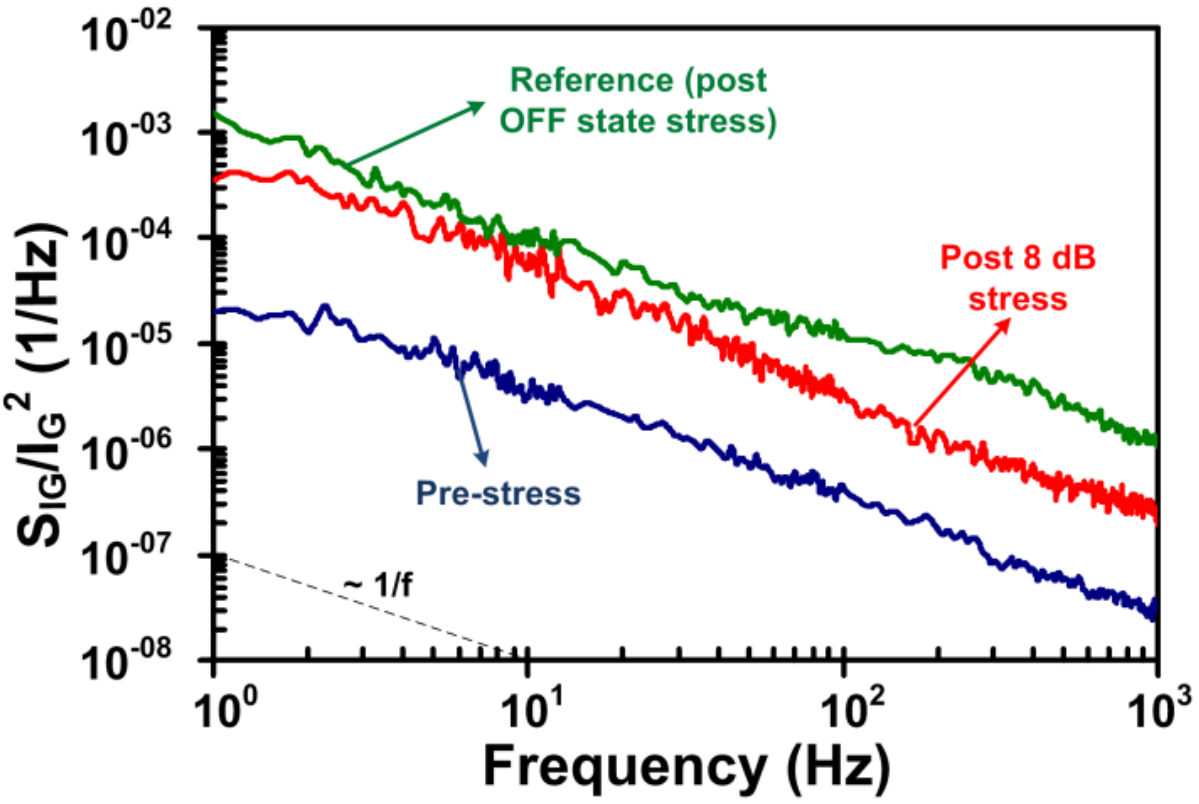

Figure 6-9. Relative gate current noise before stress (blue) after 8-dB RF stress (red). Noise after inverse-piezo electric stress (OFF state) is shown in green. More details of that work can be found in a previous work [47].

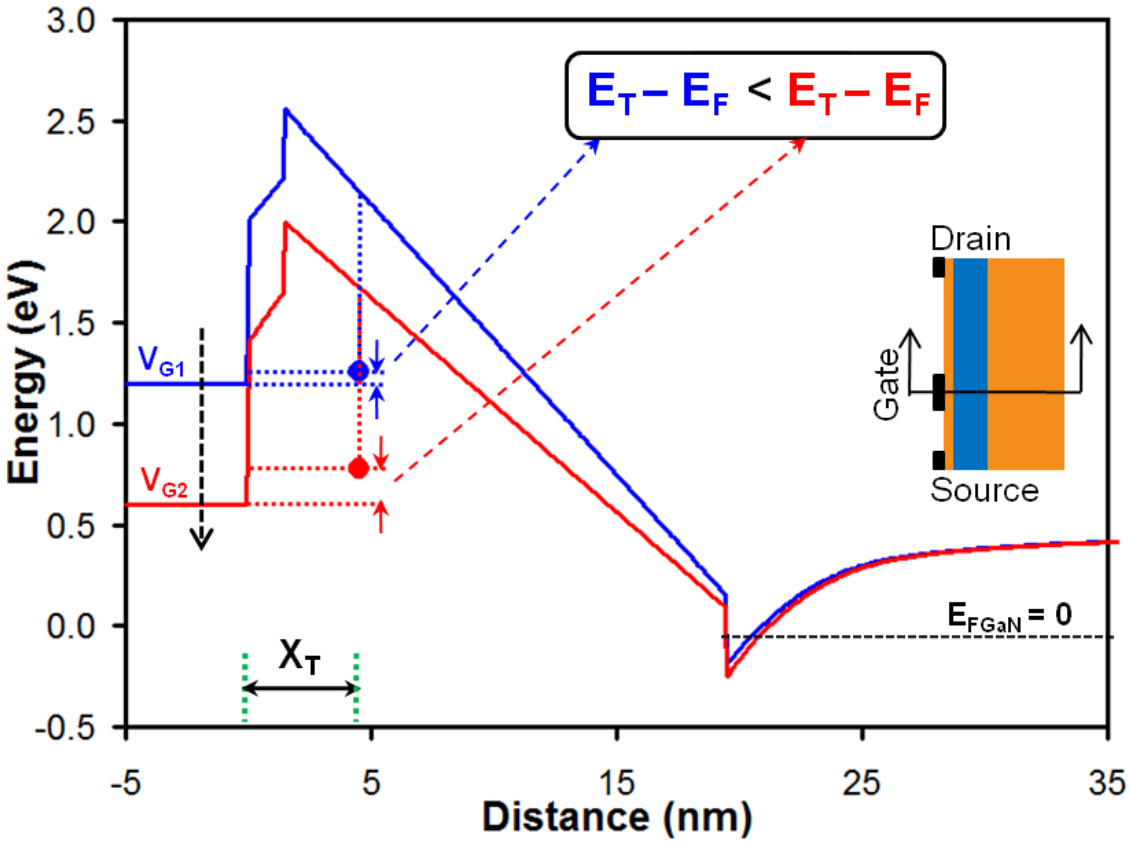

Figure 6-10. Conduction band-diagram under the gate for two increasing (black dashed arrow) gate voltages V_{G1} and V_{G2} (above the threshold voltage).

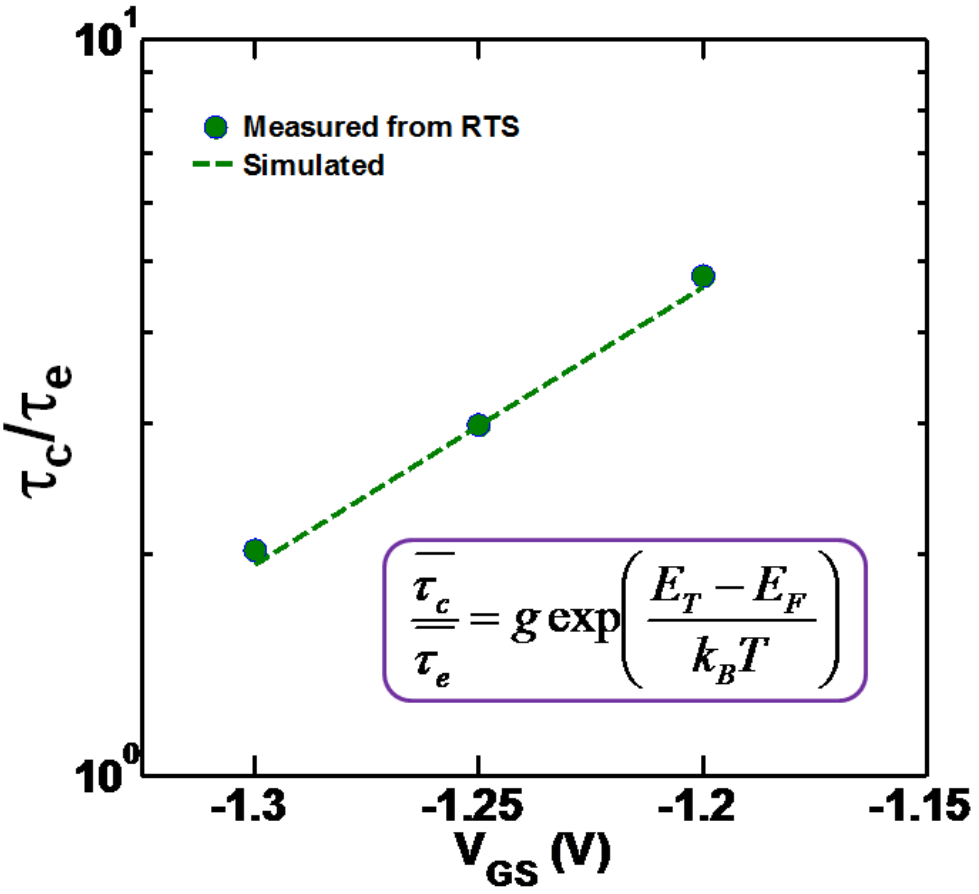

Figure 6-11. The ratio of mean time switching constants (dots) is plotted as a function of gate voltage. The dashed line shows the simulated value of this ratio equation relation (6-2) and (6-3).

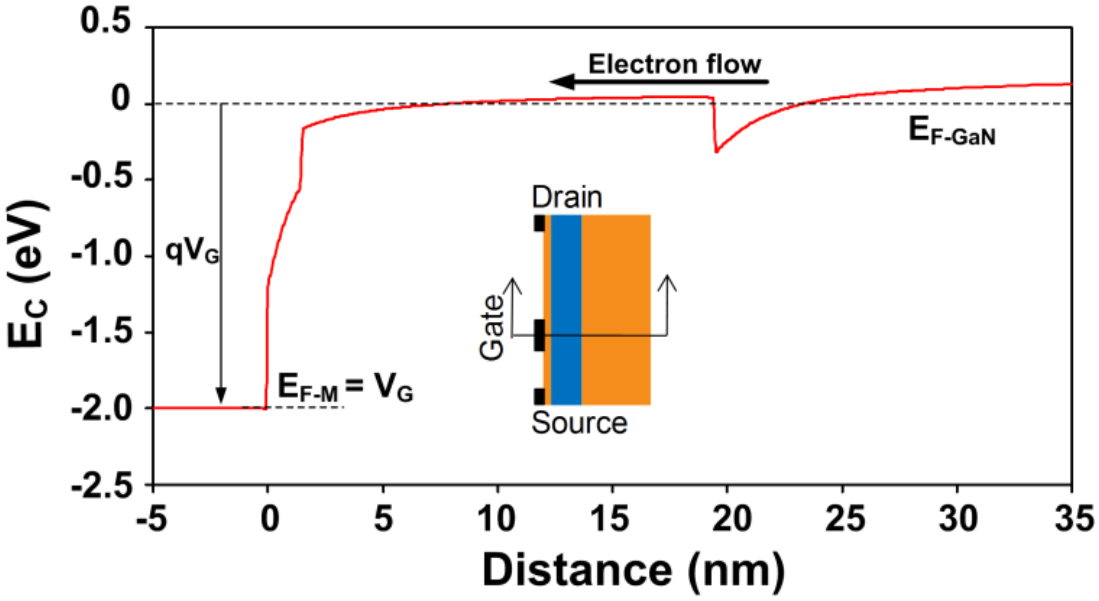

Figure 6-12. Conduction band-diagram under the gate for V_{GS} = 2 V. Most of the voltage drop occurs very near to the gate metal/GaN capping semiconductor interface and GaN capping layer. The dashed line shows the Fermi level in the GaN channel layer. The arrow shows the direction of electron motion for forward gate current.

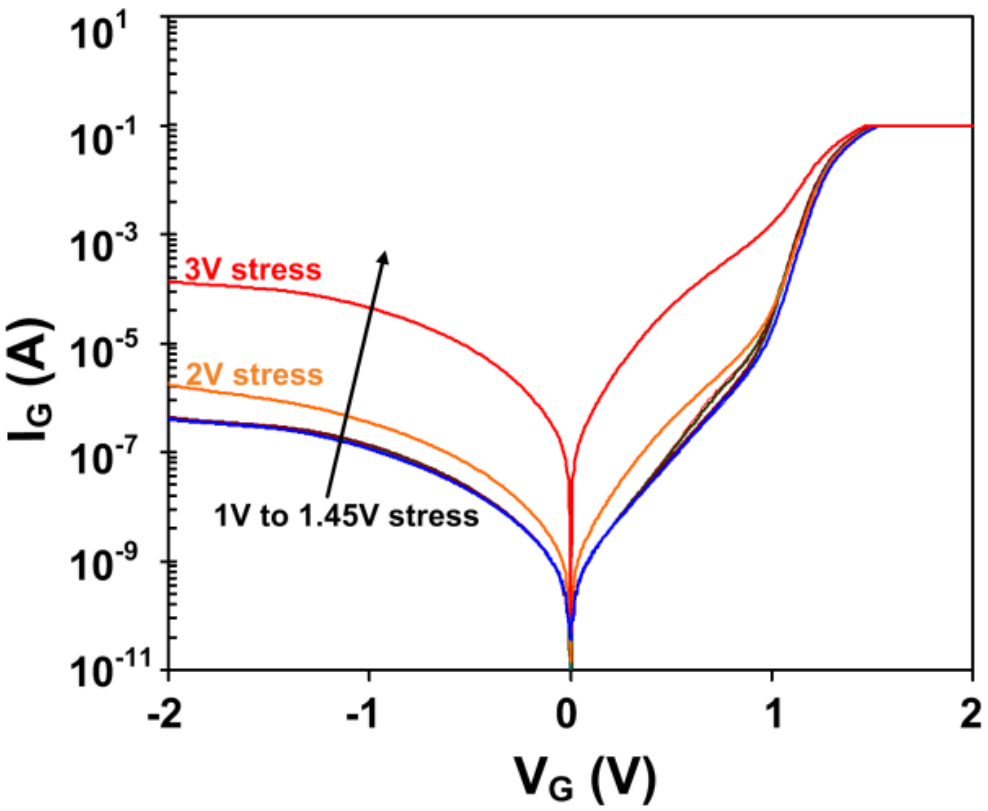

Figure 6-13. Gate diode I-V characteristics for increasing (arrow direction) forward DC gate voltage stress from 1V to 3V of 5 minutes each.

CHAPTER 7
CONCLUSIONS

Summary of Results

The objective of this study was to understand the nature of defects which negatively impact the reliability of GaN HEMTs using low frequency noise measurements. A defect map of location, density and activation energy of defects is a powerful instrument for increasing device reliability via device geometry and material choice optimization.

In chapter 2 fundamental noise sources are identified in AlGaN/GaN HEMTs. It is found that there is an extremely weak correlation between gate and drain current noise. Drain current mainly stems from the gated channel region and shows a stable $1/f^{\gamma}$ noise without distinct GR noise components. A low value of Hooge parameter 10^{-4} is determined for it. On the other hand, gate current noise also exhibits a $1/f^{\gamma}$ noise with $S_{IG} \propto I_G^2$ dependence but shows in addition distinct Lorentzian components. Often these Lorentzians are so dominant that they show up as RTS noise in the time domain. These Lorentzians are found to be temporally unstable and their noise sources migrate under device operation whereas the background $1/f^{\gamma}$ noise is stable. It is proposed that the Schottky contact is of high quality and does not degrade under device operation but factors like high electric fields, low defect migration barriers, high mechanical strain via inverse piezo-electric effect in the AlGaN/GaN system create a possibility whereby, defect centers in AlGaN barrier evolve spatially or change their energy locations. The exact nature of this migration needs to be explored further possibly by studying low frequency noise under systematically applied electrical stress to the gate stack. This

makes the study of low frequency noise an extremely sensitive tool to study device reliability under realistic bias conditions.

In chapter 3 the gate is stressed by applying reverse bias voltage. Temporary and permanent degradation of device characteristics were identified in stressed AlGaN/GaN HEMTs. It was found that existing traps in the AlGaN barrier layer contribute to the threshold voltage instability and change the drain current noise. The DC and channel noise characteristics of the device fully recovered after several days indicating that no microscopic degradation occurred in the channel region of the device. On the other hand gate current noise showed a permanent change which does not recover once the stress is removed. It was proposed that new defect states were created at gate edges via inverse-piezoelectric effect below the so called “critical voltage” [18]. The activation of mobile defects pointed to a defect movement or diffusion related mechanism at these early stages of degradation.

In chapter 4 the failure mechanisms in the channel were probed in more detail. It was found that hot carrier injection combined with self -heating was a dominant cause of degradation in the channel for ON-state stress conditions by increasing the trap density at the AlGaN/GaN interface. In chapter 5 the kinetics of the hot-carriers in GaN HEMTs was studied in detail by performing microwave noise spectroscopy. It was found that hot-electrons which exist in the channel are confined at the AlGaN/GaN interface but have enough energies to generate new interface defects responsible for the observed degradation in ON-state stress.

In chapter 6 the effect of short term high power RF stress on AlGaN/GaN HEMTs is characterized. It was found that degradation occurs right under the gate in the gate

metal-semiconductor interface and GaN capping layer without affecting the channel. Gate noise measurements pointed out that an increase of the trap density near the metal-semiconductor interface occurred after high gain compression RF stress. A point defect located at 4.5 nm under the gate and activation energy (E_C-E_T) of 0.9 ± 0.2 eV was extracted from gate RTS noise measurements. These defects have been often reported to be related to the core of the dislocations or point defects loosely bound to dislocations [52–55]. These unstable point defects were activated after low RF power stress. The role of forward gate biasing as a failure mechanism was discussed. This also points out that when the reliability of the gate stack at high RF compression levels is considered a simpler gate forward biased DC stress test can replace the high gain compression RF stress measurement

Future Work

The majority of my research was concentrated on short-term reliability studies since most of the devices did not survive long enough under applied stresses. However, it would be useful to study lower stress levels but applied for long durations to understand the role of time.

The inverse-piezo electric stress in our study used voltages which did not exceed the so-called “Critical Voltage” [18]. It would be beneficial to study the effect of full breakdown of the gate stack over critical voltage. That would give insights into the nature of the breakdown pathway and the nature of defects responsible for that. It is similar to a study of Soft and Hard Breakdown of oxides in silicon MOSFETs.

It would be valuable to develop a more quantitative estimation of interface defects both at the gate metal semiconductor interface and AlGaN/GaN channel interface which can be used as an input parameter for reliability simulations and lifetime estimations.

Finally, this work should be expanded to study more devices to improve the statistical significance of the results. This would also enable a better correlation of the results to material characterization techniques to study defects such as the transmission electron microscopy.

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BIOGRAPHICAL SKETCH

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