

SENSING AND CONTROL ELECTRONICS DESIGN FOR
CAPACITIVE CMOS-MEMS INERTIAL SENSORS

By

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To my parents;
and to my wife, Hanyao.

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The deep reactive-ion-etching CMOS-MEMS techniques provide a low-cost, small-size, and high-performance inertial sensing solution. However, the design of the read-out electronics for the CMOS-MEMS inertial sensors, including accelerometers and gyroscopes, is challenging because of their low mechanical sensitivity and small capacitance. In this thesis work, new low-power low-noise circuits architectures for CMOS-MEMS inertial sensors are proposed and are verified experimentally.

For accelerometers, an improved dual-chopper amplifier (DCA), which modulates/demodulates the signal from MEMS structures twice at high frequency and intermediate frequency and have the overall gain distributed properly in two amplification stages, is applied to realize low noise and low power consumption simultaneously. A three-axis accelerometer has been fabricated with the DCA-based electronics and has achieved $40\mu\text{g}/\sqrt{\text{Hz}}$ for lateral axis, and $130\mu\text{g}/\sqrt{\text{Hz}}$ for vertical axis, respectively, and 1mW/axis power consumption.

For gyroscopes, a novel differential difference amplifier (DDA) is developed as the front end of Coriolis signal detection. This DDA has advantages of high gain, low temperature coefficient, good linearity, and low noise. The DDA achieves a 24dB gain

and 0.01%/°C temperature coefficient. A transimpedance amplifier (TIA) with a tunable gain is employed as the front-end amplifier in the primary mode. A self-oscillation loop with automatic gain control (AGC) has also been implemented. A lateral-axis gyroscope and a vertical-axis gyroscope have been integrated with the control and sensing electronics on a standard CMOS chip. The two systems achieve the sensitivities of 1.3 mV/°/s for the lateral axis and 1.2 mV/°/s for the vertical axis, with the noise floors of 0.046 °/s/√Hz and 0.050 °/s/√Hz, respectively.

A 5-axis inertial measurement unit has been fabricated, containing a three-axis accelerometer, a lateral-axis gyroscope, and a vertical-axis gyroscope. The accelerometer uses symmetrical structures and vertical springs for z axis for higher sensitivity and less cross-axis coupling. The accelerometer achieves 50 μg/√Hz for lateral axis and 80 μg/√Hz for vertical axis, respectively.

In order to improve the performance of the gyroscopes, a six-stage Dickson charge pump is developed to achieve as high as 32V voltage on chip, to increase the mechanical sensitivity. A fully-integrated ripple-free peak detector is developed for fast peak tracking in the AGC loop of the drive mode. A method of quadrature error compensation is proposed and analyzed.

This circuit designs presented in this work are designed for but not limited to CMOS-MEMS inertial sensors. The method of balancing the low noise and low power consumption, the analysis of the system dynamics, and the concept of high gain front-end amplifiers for ultra-small capacitors are also useful for other capacitive MEMS inertial sensors.

CHAPTER 1 INTRODUCTION

1.1 Background and Motivation

Since the transistor was invented in 1947, the world has witnessed the revolution leaded by the rapid development of microelectronics. The similarly significant progress in microelectronics manufacturing technology extends the scope beyond the pure electronics and makes possible the development of the structures in micrometer and with mechanical functions, the so-called micro-electro-mechanical systems (MEMS). The MEMS devices are able to work as the sensors of acceleration, rotation, light, pressure and so on, or as the actuators to drive the movement in micrometer range, or as the carrier of chemical reactions. In short, the appearance of MEMS extends the way much how microelectronics interface with the real world.

The first MEMS device is traced back to the resonant gate transistor published by Nathanson in 1965 [1] and this area had made significant progress in the last two decades. The MEMS are forming a fast-growing market. Some MEMS devices have been commercialized successfully, such as inkjet nozzles [2], micro-mirrors [3], and pressure sensors [4], and currently inertial sensors stars in the market show [5-10].

Inertial sensors, which comprise accelerometers and gyroscopes, are used to measure the linear acceleration and the rotation rate of an object with respect to an inertial frame [5]. The classical market for MEMS inertial sensors is for automotive applications, in which MEMS accelerometers are employed as crash sensors [11-13], and gyroscopes are used for electronic stability control (ESC) and roll-over detection [14-17]. The market of consumer electronics, however, has grown rapidly in recent years. The ADXL 330 accelerometers from Analog Devices were applied in Nintendo's

Wii[®] game console in 2006 and marked the startup of a booming consumer market [18]. In 2008, the IDG 600 gyroscopes from Invensense were added into the same system [10] and made the area even hotter. Currently, three-axis accelerometers and gyroscopes have been standard features of many popular mobile electronics devices, the most well-known of which is the iPhone[®] from Apple [19, 20]. The share of consumer electronics are predicted to grow more rapidly than any other area and to dominate the market volume of MEMS accelerometers and gyroscopes by 2013, which is projected by the Yole Development to be \$3 billion by then [21]. The consumer electronics market is sensitive to unit cost, and power consumption is another important factor for portable devices. Therefore, the development of the MEMS inertial sensors with low cost, low power consumption and medium accuracy [22, 23] is highly demanded.

There has been a variety of sensing mechanisms reported for accelerometers. The piezoresistive sensing has simpler structure and fabrication process, but the performance is inferior due to the intrinsic thermal noise from the resistors and the large temperature dependence [24-26]. The tunneling current sensing achieves sub- μg noise floor [27-31]. However, those devices require an extremely small gap between the tip and the electrode (<10 Angstrom), which makes the fabrication very expensive. Moreover, the operation of the tunneling accelerometer needs a high voltage (tens of hundred volts), which limits the applications, and the noise floor of the low voltage device does not have significant advantage over the capacitive sensing [32]. The thermal accelerometers can avoid using movable proof mass to achieve high reliability [7, 33, 34], but the noise floor is relatively high, in the order of mg. The resonant

accelerometer has a quasi-digital output, which has better immunity to noise, so it can achieve high resolution [35-38]. But its major drawback is the narrow bandwidth (less than a few hertz).

Most published and commercialized gyroscopes are based on the vibratory concept [5], and the reported sensing mechanisms include capacitive [17, 23, 39-42], piezoelectric [43, 44] and magnetic detection [45]. Among the published MEMS inertial sensors technologies, capacitive sensing has the advantages of high sensitivity, low noise, low temperature dependence, good linearity, low power dissipation and low structure complexity [5], so it dominates the market and is the approach of this work as well.

The CMOS-MEMS technologies, which are also called single-chip or monolithic solutions in contrast to two-chip solutions, integrate the MEMS microstructures and the electronics on a single chip. Compared to its counterpart with two separate chips for the mechanical and the electronic parts, the CMOS-MEMS technologies entitle reduced die size and parasitic parameters caused by the interconnections between the two parts. The cost for packaging and testing will be lower as well. Therefore, the CMOS-MEMS technologies have the potential to be the ideal solution for low-cost and small-size inertial sensors. The design of the electronics for CMOS-MEMS inertial sensors, however, is more challenging. Due to the limits by fabrication processes, the mechanical sensitivity and the sensing capacitance of CMOS-MEMS sensors are much smaller than those in two-chip solutions, so the noise from the electronics will degrade the noise performance of the whole system more significantly. The research of low-

power low-noise electronics for the capacitive CMOS-MEMS inertial sensors will have noticeable benefits on the commercial applications of the technologies.

The technologies of CMOS-MEMS inertial sensors can be further developed to build the inertial measurement unit (IMU), which contains accelerometers and gyroscopes for all three axes to track an object's inertial movements. The conventional way of building an IMU is to mount multiple single-axis devices orthogonally [46]. In this way, the device at each single axis can be optimized, but the unit is bulky and the assembling cost is high. UC Irvine [47] reported an IMU based on the folded-MEMS technology that shrinks the size, but the assembling cost is still too high. An IMU that integrates all the devices on a single chip with CMOS-MEMS technologies is of great interests and the research on the electronics for all the MEMS devices at all axes is critical for this goal.

1.2 Objectives and Contributions

The objectives of this work are to develop low-power and low-noise interface circuits for CMOS-MEMS accelerometers and gyroscopes of all three axes, and to integrate multiple MEMS devices and corresponding electronics on a single standard CMOS chip with the bulk post-CMOS technology developed in University of Florida.

The work in this dissertation focuses on two aspects: one is the sensing electronics for CMOS-MEMS accelerometers. The research focused on the open-loop signal detection with low power and low noise realized simultaneously, while the force feedback is out of the scope of the work. Based on the detailed analysis of the noise and the power consumption of the interface circuitry, an improved dual-chopper amplifier (DCA) with open-loop front-end amplifier is proposed, implemented and verified. In order to reduce the gain drifting with temperature, the front-end amplifier is

improved by replacing the NMOS load with PMOS, and a bandgap circuit is designed to provide stable voltage reference. The DCA has been implemented with two prototype three-axis accelerometers with the bulk CMOS-MEMS technology and characterized with extensive experiments.

The second area that weighs more is the development of the sensing and the control electronics for MEMS gyroscopes. This work focuses on the electronics for the gyroscopes working in atmosphere. Higher performance is achievable with vacuum packaging or mode matching, but they will either increase the cost or reduce the sensor bandwidth, so they are out of interest of this work. The fundamental theories of gyroscopes, including the Coriolis force, the excitation of the drive mode and the non-idealities are studied at first. The electronics design covers two modes: the drive mode and the sense mode. In the sense mode, a novel differential difference amplifier (DDA) is used as the front-end amplifier for the first time to realize low noise, high gain, high linearity and low temperature coefficient. In the drive mode, the sensor is driven at its resonant frequency by a self-oscillation loop. A transimpedance amplifier (TIA) with tunable gate voltage is designed as the front-end amplifier that picks up the signal from the sensor and generates proper phase change, and an intermediate low-offset amplifier and an output stage with large linear range follow the TIA to amplify the signal and to feed it back to the sensor to excite the oscillation. An automatic gain control (AGC) loop is applied to control the amplitude of the driving signal, and a switched-capacitor fast-settling and no-ripple peak detector is designed for tracking the amplitude fast. All the electronics mentioned above and the other supporting electronics have

been implemented with an x/y axis and a z-axis CMOS-MEMS gyroscope on standard CMOS chip and have been verified experimentally.

In order for better performance, a 6-stage Dickson charge pump is designed to generate high on-chip voltage. It has been implemented independently and characterized experimentally. A dynamic quadrature error cancellation loop is proposed and is verified with Matlab Simulink.

1.3 Organizations of the Dissertation

This dissertation mainly discusses the sense and control electronics for the CMOS-MEMS inertial sensors, including accelerometers and gyroscopes. The technologies for sensor design are included as well. This work is divided into eight chapters.

Chapter 1 introduces the background and the motivations of this work. The objectives and the contributions of the author are stated in this chapter. The organizations of this dissertation is provided at the end of this chapter.

Chapter 2 introduces the background knowledge of the capacitive MEMS inertial sensors, which is necessary for the rest of the thesis. Then the operations and the non-idealities existing in the practical designs are discussed in details. The manufacturing technologies of the MEMS inertial sensors are summarized at the end of this chapter.

Chapter 3 focuses on the CMOS-MEMS technologies. The development of the CMOS-MEMS technologies are reviewed first, and then the bulk post-CMOS technology used for this work is introduced. All the fabricated MEMS devices in this work are shown in the end of this chapter.

Chapter 4 summarizes the front-ends for capacitive sensors and discusses the issues of noise, power, and bandwidth that need to be considered during design. The system designs for MEMS gyroscopes from other groups are introduced as well.

Chapter 5 discusses the improved low-power and low noise electronics for accelerometers. The trade-offs between the noise and the power are discussed first and then a method of achieving low power and low noise simultaneously is proposed. The improvements on the first amplification stage for lower temperature coefficient are introduced. The details of the circuit implementation are provided with details, followed by the experimental characterizations of the circuits and the system.

Chapter 6 focuses on the circuitry for gyroscopes. A novel differential difference amplifier is proposed for high gain, low noise and low temperature dependence at the beginning of this chapter. Then the system-level design and the transistor-level implementations are provided with details. The circuitry is characterized firstly by itself and then together with the sensors, and the results of both steps are included in this chapter.

Chapter 7 describes the improvements made on the current gyroscope system. The design of a Dickson charge pump for high on-chip voltage is introduced and the testing results are provided. Then a fully-integrated ripple-free peak detector is discussed. A loop for automatic quadrature error compensation is analyzed and verified with Matlab in the end of this chapter. Chapter 8 concludes the work of this thesis and suggests the work in the future.

CHAPTER 2 MEMS INERTIAL SENSORS

In this chapter, the fundamental theories of both accelerometers and gyroscopes will be discussed. Then the micromachining process of CMOS-MEMS inertial sensors will be reviewed, with the details of the bulk CMOS-MEMS process developed in University of Florida described in details.

2.1 Capacitive MEMS Accelerometers

A capacitive MEMS accelerometer can be modeled simply as a block with certain mass called proof mass, whose movements are restrained to an anchor through a spring. The movements of the proof mass are damped if it is not packaged in vacuum. A lumped mechanical model is shown in Figure 2-1(a). The governing equation of the system is

$$m \frac{d^2x}{dt^2} + b \frac{dx}{dt} + kx = ma_{ext} \quad (2-1)$$

where m is the mass, k is the spring constant, and b is the spring constant. x and a_{ext} represent the displacement and the acceleration of the proof mass, respectively.

And the transfer function is derived as

$$H(s) = \frac{X(s)}{A(s)} = \frac{1}{s^2 + \frac{b}{m}s + \frac{k}{m}} = \frac{1}{s^2 + \frac{\omega}{Q}s + \omega_n^2} \quad (2-2)$$

$$\omega_n = \frac{k}{m},$$

And

$$Q = \frac{\omega_n m}{b}$$

where ω_n is the natural resonant frequency and Q defines the quality factor of the mechanical structure. For the ease of analysis, the variables in mechanical domain can be converted to electrical domain, based on the conjugate rules that converts k , m , b , a , and F , to $1/C$, L , R , I , and V , respectively. Therefore, the dynamics of the mechanical system can be analyzed as electrical circuits, which is more intuitive. The equivalent electrical model of the accelerometer shown in Figure 2-1(a) is schemed in Figure 2-1(b).

For the accelerometers working in the flat band whose frequency is below the resonant frequency, (2-2) can be simplified as

$$H(s) = \frac{1}{\omega_n^2} = \frac{m}{k} \quad (2-3)$$

In time domain, the mechanical sensitivity is defined as

$$s_{a-m} = \frac{x}{a_{ext}} = \frac{m}{k}$$

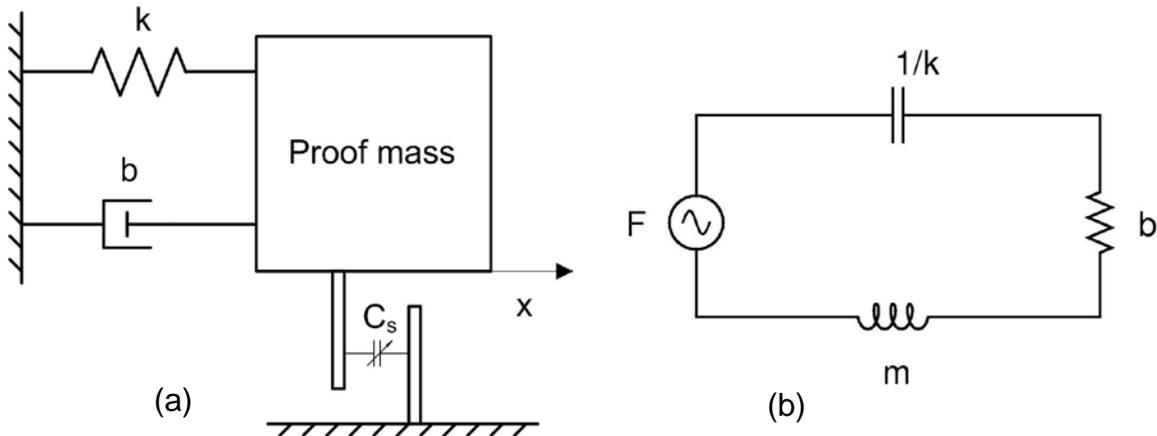


Figure 2-1. The lump mechanical model and the equivalent circuits of MEMS accelerometers; (a) mechanical model; (b) equivalent circuit model.

It is interesting to notice that the mechanical sensitivity is inversely proportional to the square root of the resonant frequency, which implies a trade-off between the sensitivity and the bandwidth.

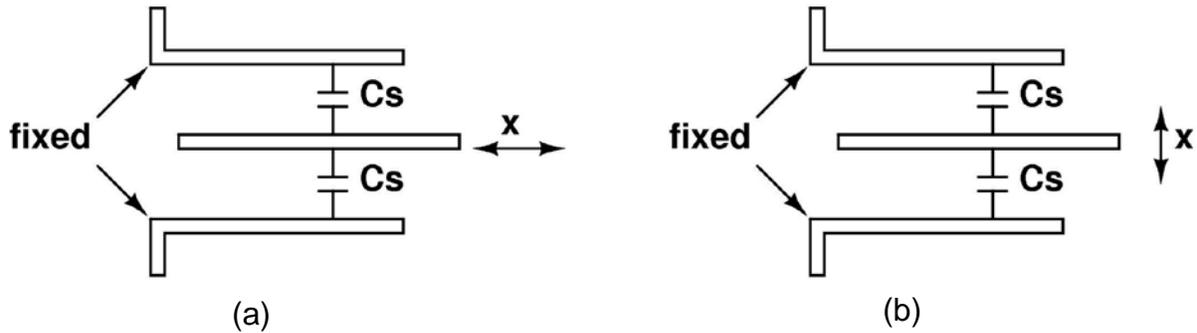


Figure 2-2. Capacitance variation caused by acceleration; (a) variable overlap; (b) variable gap.

The capacitance between two plates is

$$C = \frac{\epsilon A}{g} \quad (2-4)$$

where ϵ is the permittivity of the dielectric material, A is the overlap area, and g is the gap between two plates. Since the capacitance change caused by proof mass movements is very small compared to the initial value, the capacitance change can be linearized as

$$\Delta C = \frac{dC}{dx} \cdot \Delta x \quad (2-5)$$

Although (2-5) has different mathematical format for variable-gap and variable-overlap cases, it can be proved that the results after proper approximation are uniform, written as

$$\Delta C = \frac{\Delta x}{x_0} \cdot C \quad (2-6)$$

In (2-6), x_0 is the initial length of overlap for variable-overlap accelerometers, and is the initial gap for variable-gap ones, and Δx is the movement in the dedicated directions, which is linearly proportional to its acceleration. Therefore, the acceleration signal is transduced to capacitance variations that can be picked up by analog circuits.

2.2 Vibratory Gyroscopes

MEMS gyroscopes detect the capacitive change caused by the Coriolis force, which will be discussed in details in the following section, and the conversion from acceleration to capacitance variation is similar with that of accelerometers. In this section, the Coriolis effect is introduced first, and then the operation and the non-idealities of vibratory gyroscopes will be discussed.

2.2.1 Coriolis Effect

The Coriolis effect is the fundamental basis of the MEMS vibratory gyroscopes, and needs to be addressed before the other contents.

As shown in Figure 2-3, a rotating frame of reference is defined with the axes of x' , y' , and z' . For the ease of understanding, the frame is subject to a counter-clockwise rotation along z' , whose angular rate is Ω . A subject in the frame has the velocity \vec{v} referred to the ground, which satisfies

$$\vec{v} = \vec{v}' + \vec{\Omega} \times \vec{r}' \quad (2-7)$$

where \vec{v}' is the local velocity referred to the frame, and \vec{r}' is the vector pointing from the rotation center to the subject. For the purpose of discussion in general cases, all the velocities appearing in the following analysis are vectors. By differentiating (2-7) with time, the acceleration is expressed as

$$\vec{a} = \vec{a}' + 2(\vec{\Omega} \times \vec{v}') + \vec{\Omega} \times (\vec{\Omega} \times \vec{r}') \quad (2-8)$$

Taking the linear acceleration of the frame into consideration, a generalized equation is written as

$$\sum \vec{F} = m\vec{a}' + 2m(\vec{\Omega} \times \vec{v}') + m\vec{\Omega} \times (\vec{\Omega} \times \vec{r}') + m\vec{a}_{frame} + m\vec{a}_{frame} \times \vec{r}' \quad (2-9)$$

$\sum \vec{F}$ in (2-9) is the total force applied to the subject. The term $2m \times (\vec{\Omega} \times \vec{v}')$ is called Coriolis force, which is perpendicular to both the rotation axis and the vector of local velocity, and the term $m\vec{\Omega} \times (\vec{\Omega} \times \vec{r}')$ is called Centrifugal force. The other two forces, $m\vec{a}_{frame}$ and $m\vec{a}_{frame} \times \vec{r}'$, are because of the linear acceleration of the frame. Although the last three terms may contribute significant error to a gyroscope in practical cases, the Coriolis force should be focused on at the beginning of analysis. In a simplified case with zero linear acceleration of the inertial frame, the total external force is zero, so (2-9) can be reduced to

$$m\vec{a}' = -2m(\vec{\Omega} \times \vec{v}') \quad (2-10)$$

So there is a local acceleration referred to the frame mainly caused by the Coriolis force, and that acceleration can be detected by an accelerometer whose sensitive direction aligns to the Coriolis acceleration, with the mechanism mentioned in the previous section. According to (2-10), certain velocity is necessary to generate the Coriolis acceleration, and for vibratory gyroscopes, the velocity is generated by driving the proof mass periodically with electrostatic force, as discussed in the next section.

2.2.2 Operation of Gyroscopes

The gyroscope can be modeled as a system with 2-degree-of-freedom system (2 DOF), as shown in Figure 2-4. In the drive mode, the center proof mass is driven by electrostatic force to move up and down along with the frame, whose movements is

restrained by the rollers within the vertical direction. When the gyroscope is subject to rotation in the direction perpendicular to the paper in the sense mode, the induced Coriolis acceleration is in the horizontal direction, which causes the center proof mass to move horizontally relative to the frame and makes the sensing capacitance vary. The dynamics of the sense mode is similar with that of accelerometers as introduced in the previous section. Generally, a gyroscope is modeled as an actuator in the drive mode and an accelerometer in the sense mode.

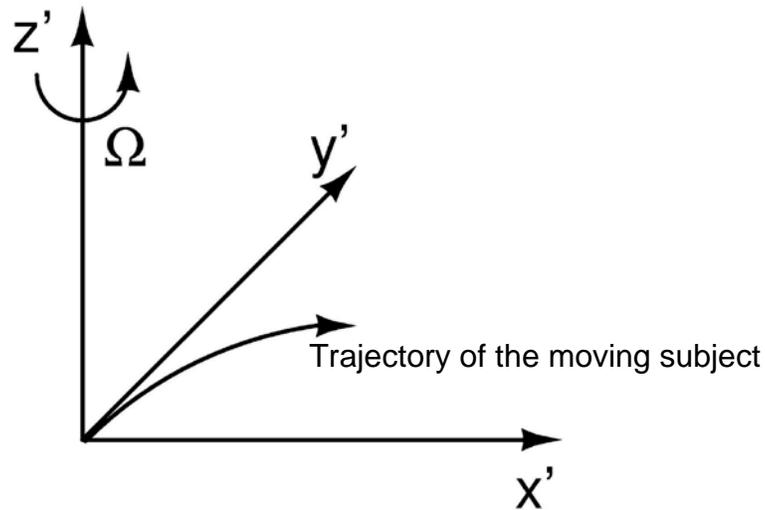


Figure 2-3. Trajectory of the moving subject in a rotating frame.

Similar to the accelerometers, the governing equations on the two directions are written as

$$m_d \frac{d^2 x}{dt^2} + b_d \frac{dx}{dt} + k_d x = F_d \quad (2-11)$$

$$m_s \frac{d^2 y}{dt^2} + b_s \frac{dy}{dt} + k_s y = 2m_s \Omega \frac{dx}{dt} \quad (2-12)$$

The subscriptions d and s represent the drive mode and the sense mode, respectively. In order to simplify the analysis, the net force in the drive mode, F_d , comes

from the electrostatic force applied externally, and the net force in the sense mode is only the Coriolis force.

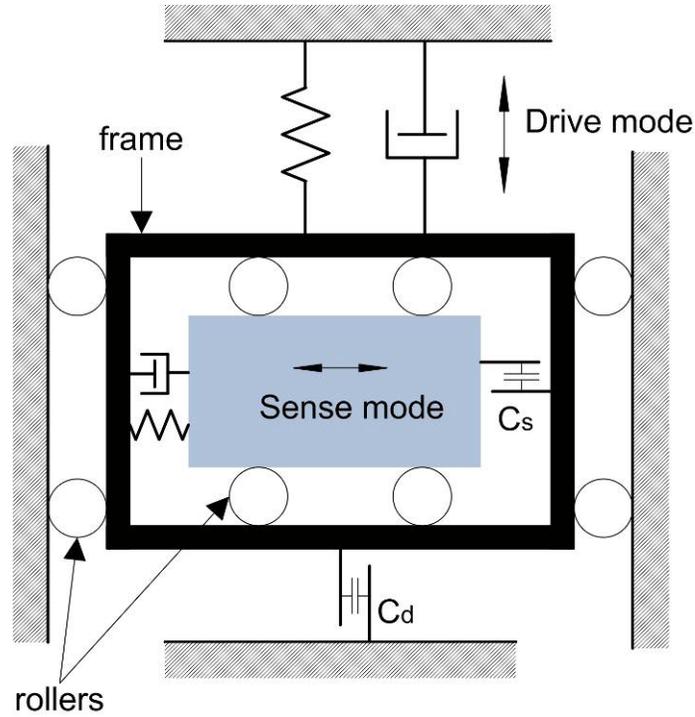


Figure 2-4. Simplified mechanical model of a capacitive MEMS gyroscope.

The driving force is assumed sinusoidal as

$$F_d(t) = F_d \sin(\omega t)$$

By solving (2-11), we get the function of the movements in driving mode.

$$x(t) = \frac{F_d}{k_d \sqrt{\left(1 - \left(\frac{\omega}{\omega_d}\right)^2\right)^2 + \left(\frac{\omega}{Q_d \omega_d}\right)^2}} \sin(\omega t - \phi_d) \quad (2-13)$$

and

$$\phi_d = \arctan \frac{\omega / \omega_d}{Q_d [1 - (\omega / \omega_d)^2]} \quad (2-14)$$

The function of the movements in sense mode can be obtained by solving (2-12) and substituting (2-13) into the result, as shown in (2-15) and (2-16).

$$y(t) = \frac{2F_d m_s \omega \Omega}{k_d k_s} \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_d}\right)^2\right)^2 + \left(\frac{\omega}{Q_d \omega_d}\right)^2}} \cdot \frac{\sin(\omega t - \phi_d - \phi_{ds})}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_s}\right)^2\right)^2 + \left(\frac{\omega}{Q_s \omega_s}\right)^2}} \quad (2-15)$$

and

$$\phi_{ds} = \phi_s - \phi_d = \arctan \frac{\omega / \omega_s}{Q_s [1 - (\omega / \omega_s)^2]} - \arctan \frac{\omega / \omega_d}{Q_d [1 - (\omega / \omega_d)^2]} \quad (2-16)$$

In equations (2-13) to (2-16), people should be noticed that

$$Q_i = \frac{m_i \omega_i}{b_i} \quad \text{and} \quad \omega_i = \sqrt{\frac{k_i}{m_i}}, \quad i=d,s.$$

The mechanical sensitivity of a gyroscope is defined as:

$$\begin{aligned} S_{g_m} &= \frac{|Y|}{\Omega} \\ &= \frac{2F_d m_s \omega}{k_d k_s} \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_d}\right)^2\right)^2 + \left(\frac{\omega}{Q_d \omega_d}\right)^2}} \cdot \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_s}\right)^2\right)^2 + \left(\frac{\omega}{Q_s \omega_s}\right)^2}} \end{aligned} \quad (2-17)$$

Figure 2-5 plots the normalized mechanical sensitivity of gyroscopes versus frequency, with a typical set of parameters. The resonant frequency of the drive mode and the sense mode is 5 kHz and 6 kHz, respectively. The quality factor, Q_d , is equal to 200, while Q_s is equal to 5. It can be observed from the figure that the maximum mechanical sensitivity is achieved at the resonant frequency of the drive mode. This conclusion consists with the general understanding of the second-order system that has high Q. Therefore, a gyroscope should be excited to resonate in the drive mode for optimal sensitivity, where the displacement lags the driving force by 90° , and then (2-16) becomes

$$\phi_{ds} = \phi_s - \phi_d = \arctan \frac{\omega / \omega_s}{Q_s [1 - (\omega / \omega_s)^2]} - 90^\circ \quad (2-18)$$

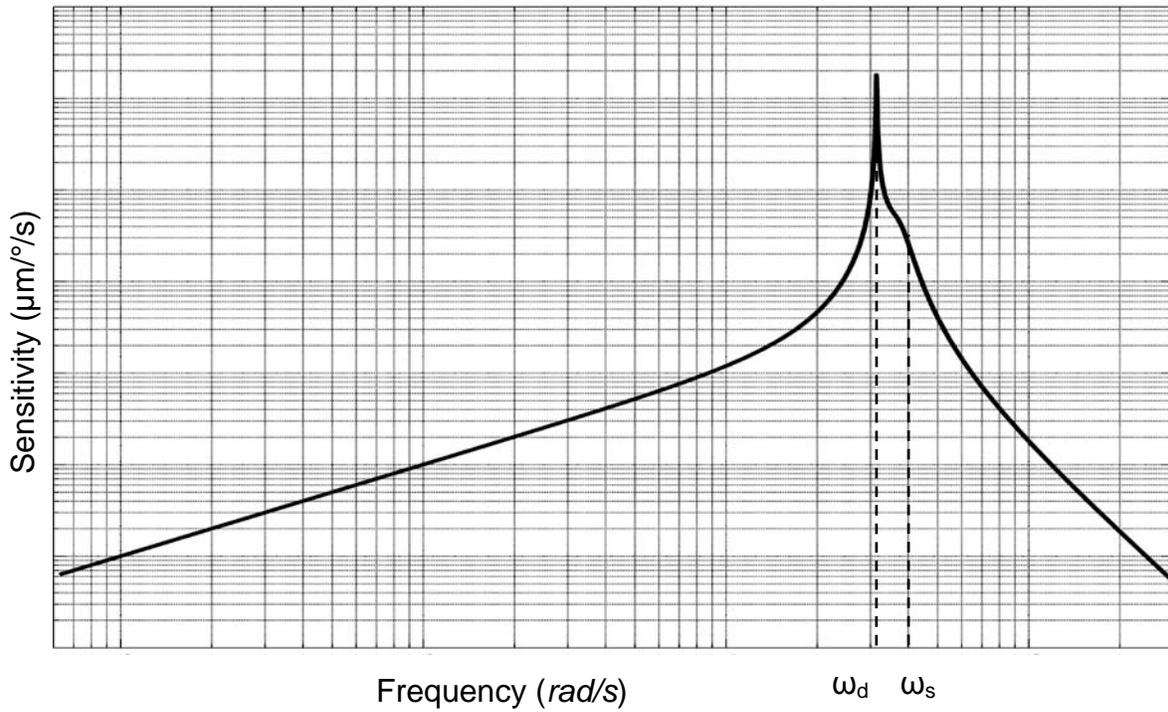


Figure 2-5. Bode diagram of the mechanical sensitivity of gyroscopes.

For gyroscopes with $\omega_s > \omega_d$, which is the case of the design in this work, $\phi_d = 90^\circ$ and $\phi_{ds} = -90^\circ$, so the Coriolis acceleration is in phase with the driving force. So the amplitude of the displacement in drive mode is

$$|X| = \frac{F_d Q_d}{k_d} \quad (2-19)$$

The thermo-mechanical noise of the gyroscope in terms of Coriolis acceleration is then written as

$$a_{\text{Coriolis}_n} = \frac{\sqrt{4k_B T b_s}}{m} \quad (2-20)$$

where k_B is the Boltzmann constant, T is the absolute temperature, and b_s is the damping coefficient of the sense mode.

2.2.3 Electrostatic Force

The drive mode of MEMS capacitive gyroscopes is excited by electrostatic force between comb fingers or electrodes. Figure 2-6(a) shows a capacitor composed of two electrode plates, of which the area and the gap are A and g , respectively. The voltage applied on each of the two plates is V_{dc} and V_{ac} , where V_{dc} is a fixed dc bias, and V_{ac} varies with time. The potential energy stored in the capacitor is

$$E = \frac{1}{2} \cdot \frac{\epsilon A}{g} \cdot (V_{ac} - V_{dc})^2 \quad (2-21)$$

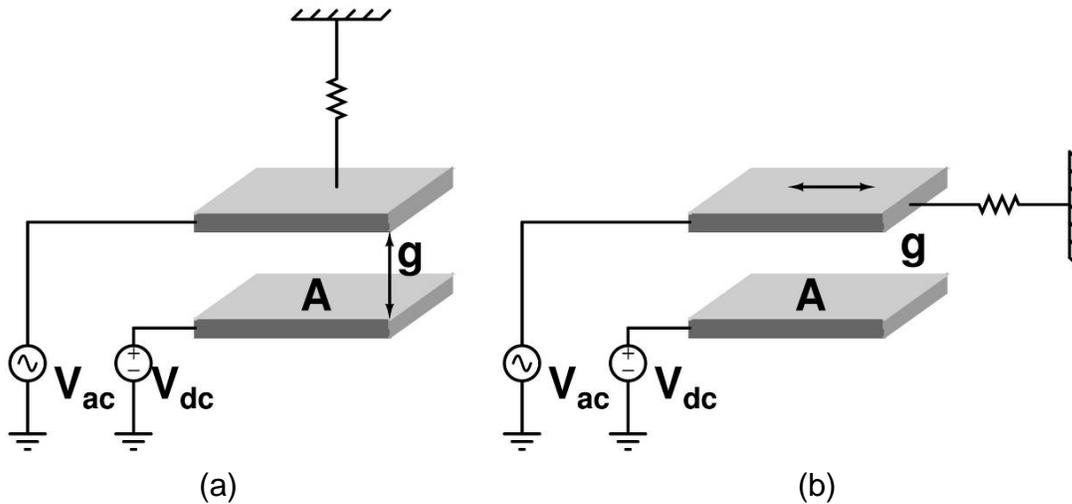


Figure 2-6. Electrostatic force between two electrodes; (a) gap-changing force; (b) area-changing force.

The electrostatic force between electrodes appears attractive and tends to change either the gap or the overlap area of the capacitor, depending on the restraining conditions. And its value is derived as

$$F_e = -\frac{\partial E}{\partial g} = \frac{1}{2} \cdot \frac{\epsilon A}{g^2} \cdot (V_{ac} - V_{dc})^2 \quad (2-22)$$

for gap-changing case, and

$$F_e = -\frac{\partial E}{\partial l} = -\frac{1}{2} \cdot \frac{\epsilon d}{g} \cdot (V_{ac} - V_{dc})^2 \quad (2-23)$$

for area-changing case.

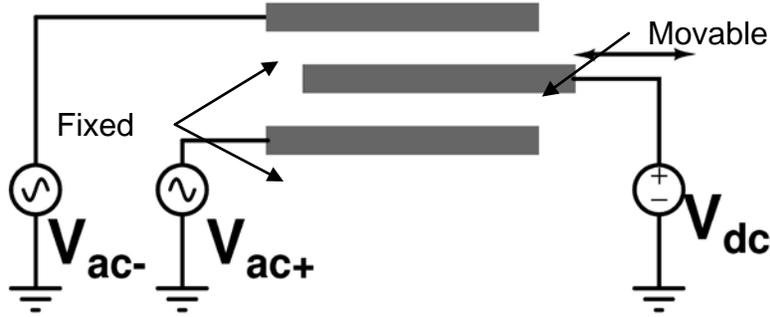


Figure 2-7. Differential driving with electrostatic force.

Considering the MEMS structure design in this work, the area-changing case will be taken as example for detailed analysis in the following sections, and the results of gap-changing case will be provided without derivation as well. The result in (2-22) and (2-23) contains higher order harmonics of V_{ac} , which introduces nonlinearities and thus is undesirable. Differential driving is used to cancel the harmonics, whose diagram is schemed in Figure 2-7. Two out-of-phase ac signals, V_{ac+} and V_{ac-} , are applied at the differential driving electrodes at the fixed plates, so the net electrostatic force that the movable part suffers is

$$F_{net} = F_{e+} - F_{e-} = -2 \frac{\epsilon d}{g} \cdot V_{ac} V_{dc} \quad (2-24)$$

Similarly, the net force for the gap-changing case is

$$F_{net} = F_{e+} - F_{e-} = 2 \frac{\epsilon A}{g^2} \cdot V_{ac} V_{dc} \quad (2-25)$$

It can be observed from (2-24) and (2-25) that in both area-changing and gap-changing cases the driving force is proportional to the product of ac and dc signals.

Compared to the gap-changing case, however, the area-changing electrostatic force has better linearity, because the scale factor is not affected by the movements of the electrodes. Therefore, the design in this work uses electrostatic force to change the overlap area. Recalled from (2-15), the mechanical sensitivity of a MEMS gyroscope is linearly proportional to the driving force, so high amplitude of ac or dc signal is desirable. High-voltage dc can be generated with charge pump, which will be discussed in details in Chapter 6, but high ac amplitude requires MOS devices working under high power supply voltage, which are not provided by all foundries.

2.2.4 Quadrature Error and Direct Coupling

The discussions in the previous sections are based on ideal gyroscopes. In realistic devices, however, various non-idealities exist and affect the devices' performance, either slightly or seriously. Some non-idealities have so significant impacts on the devices that they cannot be regarded negligible. The most important two out of them are so-called "quadrature" error and direct coupling, as will be covered by this section.

The first non-ideality to discuss is the quadrature error. Due to defects and/or variations from fabrication process, such imperfections as asymmetry and anisoelasticity are generated, which cause the movement of the proof mass to deviate from the ideal direction of the drive mode. Consequently, cross-coupled motions can be observed in other directions. For example, the proof mass is driven in the x direction, but movement may be observed in y- and z-axis, of which y-axis is the one for Coriolis signal in the previous analysis. Since the cross-coupled movement in other axis is in phase with that in the main axis, according to (2-14) and (2-18), it lags either the driving signal or the Coriolis signal by 90° and is commonly called "quadrature" error. The

amplitude of the displacement in the drive mode is usually 2 to 3 orders higher than that induced by Coriolis force, so even small ratio of the drive-mode movements coupled to the sense mode is strong enough to overwhelm the rotation signal. The quadrature error has the potential risk to saturate the interfacing amplifier and to limit the dynamic range of the system significantly, if it is not dealt with properly. Due to the exact 90° phase difference, the quadrature error can be eliminated by the synchronous demodulation, which demodulates the output signal with a clock that is in phase with the Coriolis signal.

Another error source is the movement direct coupled from the drive mode to the sense mode. In the previous analysis, the proof mass is driven in the sense mode along x axis, and the movements in other directions are restrained by rollers, which do not exist in real devices. Instead, the off-axis movements are restrained by the beams that have certain spring constant k_x , k_y , and k_z in the three axes, respectively, out of which k_y and k_z are much higher than k_x , but not infinity. So the resonant frequencies of y and z axes are much higher than that of the drive mode. According to (2-14), the phase delay of the off-axis movements compared to the driving signal is close to zero, which means the movements leaked to the sense mode due to finite off-axis spring constant is in phase with the Coriolis signal and is not able to be removed by synchronous modulation. Figure 2-8 shows the phase relations among important variables.

Based on the discussion, there will be signal in the sense mode even if there is no rotation happening, due to the non-idealities, so the output signal of the sense mode is always a mixture of the real Coriolis signal and the couplings. The output signal at zero rotary rate, which is called zero rate output (ZRO), measures the extent how the

vibration in drive mode is coupled to the sense mode. The ZRO can be reduced in several ways, including demodulating the output sense-mode signal synchronously, and using electrodes in the sense mode to apply an electrostatic force that counters the quadrature error.

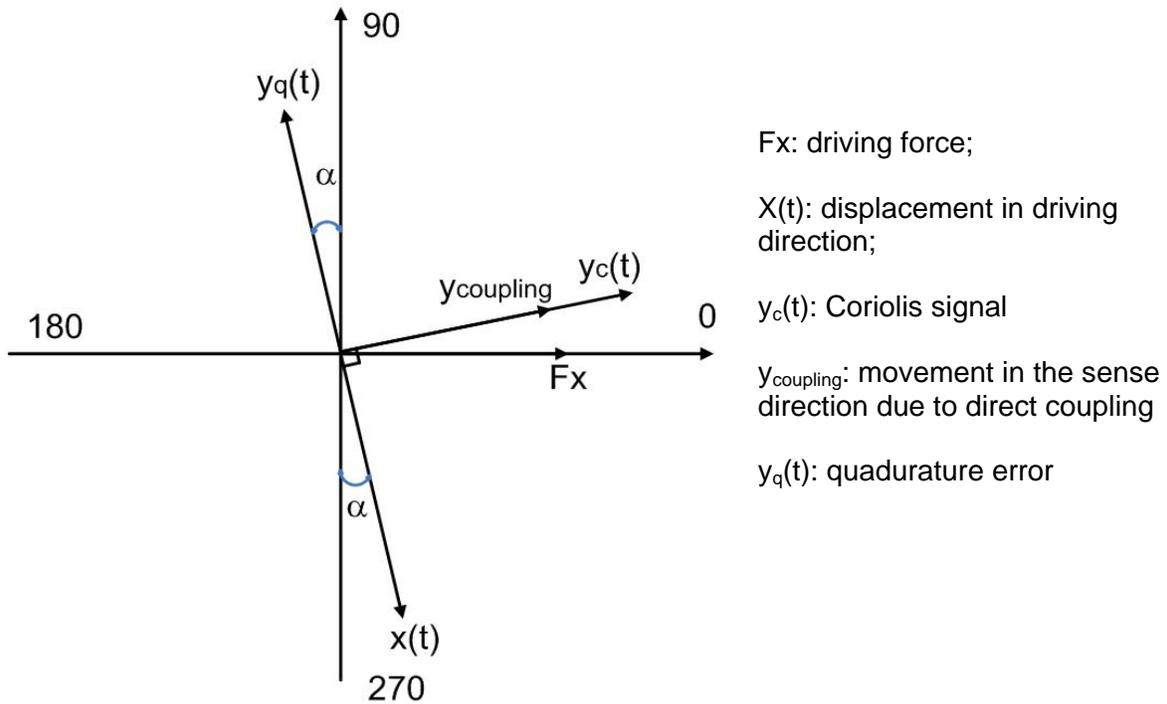


Figure 2-8. Phase relationship of the important vectors of gyroscopes.

2.2.5 Excitation of the Primary Mode

The resonator of the gyroscope in the primary mode should be driven at the resonant frequency to achieve best sensitivity. The simplest way of doing so is scanning the frequency of an ac signal to find the resonant frequency. However, from (2-13), the bandwidth of the transfer function around the resonant frequency is derived as

$$BW_d = \frac{\omega_d}{Q_d} \tag{2-26}$$

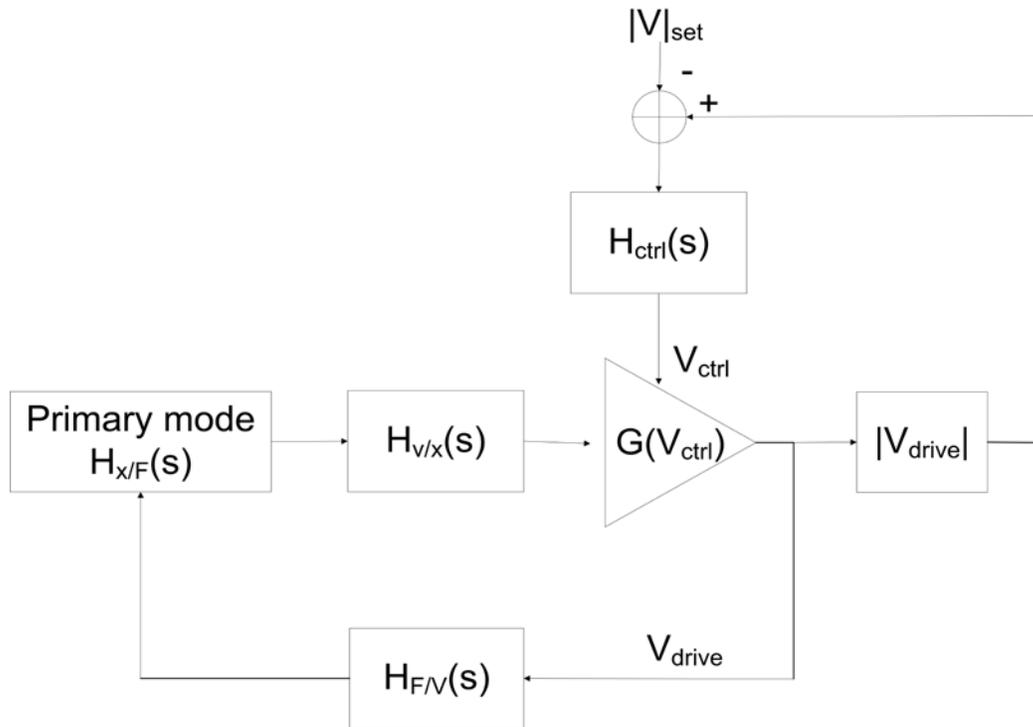


Figure 2-9. Block diagram of the excitation loop for the primary resonator.

A rough estimation of the bandwidth can be made by substituting typical values such as $\omega_d=10\text{ kHz}$, and $Q_d=200$ for the gyroscopes working in atmosphere, as it results in a 50 Hz bandwidth, which means 25 Hz drift will cut the oscillation amplitude by 3dB. The quality factor can be even more than 10,000 for those with vacuum packaging, in which case the bandwidth is as narrow as 1 Hz. So even a small drift in frequency will cause a significant drop on resonance amplitude. Due to the imperfections of the fabrication, the resonant frequency of gyroscopes spreads, which means the open-loop driving signal needs a fine tuning in frequency for each single device. Therefore, the open-loop excitation is not suitable for the batch-fabricated gyroscopes. Furthermore, the resonant frequency drifts during operations along with the environmental

parameters, such as temperature and air pressure, *etc*, which requires the excitation circuits to be able to track the frequency drift in real-time.

Since the gyroscope in the primary mode is a band pass filter by itself with high quality factor, A better solution is to build up a closed-loop oscillator with the primary-mode resonator as the loop filter, as shown in Figure 2-9, where $H_{x/F, V/x, Fx/V\dots}$ represent the transfer functions and the subscription x, V, and F represent the displacement, voltage and the force, respectively. The conditions for oscillation are

$$|H_{F/V}(s)H_{x/F}(s)H_{V/x}(s)G|=1 \quad (2-27)$$

and

$$\angle H_{F/V}(s)H_{x/F}(s)H_{V/x}(s)G = 0 \quad (2-28)$$

According to (2-14), (2-24), and (2-25), $\angle H_{x/F} = -90^\circ$ and $\angle H_{F/V} = 0^\circ$ at the natural resonant frequency, so the phase of the term $H_{V/x}(s)G$, which comes from the electronics, should be 90° leading to satisfy these conditions. The loop gain is set at 2~3 at the beginning for starting up the oscillation and it will settle down to unity in steady state. The closed-loop excitation has the advantage of better stability than the open-loop solution. If the phase of the electronics is not exactly 90° , which is usually the case, the oscillation frequency will drift to satisfy (2-28). Assume the phase of the electronics is $90^\circ + \varphi'$, the phase delay of the displacement over the driving signal is then $90^\circ + \varphi'$. According to (2-14), the corresponding frequency is

$$\omega_d' = \omega_d \left(1 - \frac{1}{2Q_d \tan(90^\circ + \varphi)}\right) \quad (2-29)$$

The transfer function of the displacement over the driving force is then

$$H_{x/F}(\omega_d') = H_{x/F}(\omega_d) \cdot \frac{1}{\sqrt{1 + (1/\tan(90^\circ + \varphi))^2}} \quad (2-30)$$

In order to have the magnitude of the transfer function from driving force to displacement cut no more than 3dB, up to extra 45° phase change is allowed, regardless of the quality factor. It is a very loose requirement on the analog electronics compared with that implied from the frequency point of view mentioned in this section, which varies from less than 1 Hz to tens of Hz. For a proper CMOS design, 5° extra phase change is a reasonable estimation for the electronics for the primary mode, in which case the magnitude of the transfer function drops by approximately 0.4%, or 0.03 dB. Since the initial set of the loop gain is 2~3, the gain requirements of (2-27) can still be satisfied. Eventually the system will find a frequency that satisfies both (2-27) and (2-28) and oscillate at that frequency.

2.3 Manufacturing Technologies

Many technologies for MEMS inertial sensors fabrication have been reported in literatures. In terms of how the mechanical structures are formed, these technologies can be broadly divided into two groups: the bulk micromachining technologies, which form the microstructures by selectively etching bulk materials, and the surface micromachining technologies, which form the microstructure by growing and etching different kinds of films on top of the supporting substrates. The border between these two groups is not precise, and technologies can be probably found to fit into both of the two groups or neither of them. However, for the purpose of briefly introducing the manufacturing technologies, this division is sufficient.

The manufacturing technologies can also be divided into two-chip solutions and single-chip monolithic solutions in terms of how the MEMS microstructures are

implemented with the circuitry. This division is more accurate because a monolithic solution integrates both parts on a single die, whereas a two-chip solution has two separate chips for the mechanical part and the electronic part, and the two chips are combined using external connections. The technologies of single-chip solutions are also referred as CMOS-MEMS technologies.

In this section, the surface and bulk micromachining technologies will be reviewed briefly. The CMOS-MEMS technologies, as the technical approach of this work, will be introduced in details in Chapter 3.

2.3.1 Surface Micromachining

In surface micromachining technologies, the mechanical structures are formed by etching the films grown on top of the substrate [48-52]. The most commonly used material for device layer is polysilicon, and the accelerometers with thin polysilicon film as the surface layer have been commercialized for more than 10 years [11]. Other structural materials include various metals and amorphous silicon nitride, such as the surface micromachining technologies developed by Carnegie Mellon University, which uses the metal layer existing in CMOS chips as the structure layer [53, 54], as well as the mask for etching.

The main drawback of the thin-film technologies is the small device thickness, which limits the available capacitance and proof mass and leads to high thermal-mechanical noise. And the residual stress existing in the structure layer can cause serious curling, which limits the size of the proof mass and degrades the performance more. The typical noise floor for the MEMS accelerometers fabricated with thin-film polysilicon is hundreds of $\mu g/\sqrt{\text{Hz}}$.

In order for larger masses, a so-called epi-poly technology is used to grow thick polysilicon layer on SiO₂ film on a silicon substrate. Bosch and STMicroelectronics have achieved more than 10 μ m thick polysilicon in their commercial gyroscope products.

2.3.2 Bulk Micromachining

In bulk micromachining process, the microstructure is formed by etching the single-crystal silicon of the substrate. The usage of the bulk material increases the device thickness and avoids the stress existing in the surface micromachining technologies, so the devices with large size and weight can be realized [55-58].

Most reported high-performance accelerometers and gyroscopes are fabricated with the bulk micromachining technology [58-60]. Many of them use multi-wafer bonding or silicon-on-insulator (SOI) technology to form the proof with desired large thickness [59, 61-63]. Some special techniques such as wafer dissolving, double-side process and thick EPI-SOI wafer are also utilized in the bulk process [60, 64, 65]. Although high performance is achieved, those processes complicate the fabrication and increase the cost.

The devices mentioned above are all for two-chip solutions, but the bulk micromachining can also be applied on single-chip solutions. The bulk CMOS-MEMS technology developed by Qu [58, 66] at University of Florida uses the substrate of CMOS chips as the bulk material. It inherits the advantage of process simplicity from the thin-film CMOS-MEMS technology developed by Carnegie Mellon University, and increases the proof mass with the single-crystal silicon underneath the metal films. The reported accelerometer fabricated with this process achieves a 12 μ g/ $\sqrt{\text{Hz}}$ noise floor.

The Invensense Inc. has invented a so-called Nasiri process, which use the wafer level bonding to reduce the package cost. In this process, the wafer for devices is firstly

processed and bonded to the wafer for CMOS circuits, and then the last etching step is executed to release the devices.

CHAPTER 3 CMOS-MEMS TECHNOLOGIES

In this chapter, various CMOS-MEMS technologies are introduced, followed by the detailed description of the manufacturing process for the sensors in this dissertation. The fabricated accelerometers and gyroscopes that work with the electronics in this work will be shown at the end of this chapter.

3.1 CMOS-MEMS Technologies

The MEMS inertial sensors and CMOS electronics can be implemented on a single chip or on two chips. In two-chip solutions, there are two separate chips for MEMS structures and application-specified integrated circuits (ASIC). The MEMS chip sits either beside or on the top of the ASIC chip, and the two chips are combined using, for example, bonding wires. The ASIC can be fabricated with standard foundry technologies, and the mechanical and the electronic part can be optimized separately for better performance and higher yield. However, the large parasitic parameters introduced by the interconnection between the two parts degrade the signal-to-noise ratio (*SNR*). The increased size for allowing two chips and extra cost for packaging and testing also need to be considered.

The CMOS-MEMS process refers to the technologies that integrate MEMS structures and CMOS circuitry on a single chip, in comparison to the two-chip solutions mentioned above. In terms of the procedure of CMOS and MEMS fabrication, the CMOS-MEMS technologies can be categorized as pre-CMOS, inter-CMOS, and post-CMOS technology [67].

3.1.1 Pre-CMOS and Inter-CMOS Technology

Sandia National Laboratory developed a pre-CMOS technology, called “micromechanics-first” process, which fabricates micromechanical structures in a trench etched on the surface of the wafer before CMOS process [68]. The micromechanical structures are sealed by a nitride membrane during the CMOS process. Post-CMOS process is still needed to expose and release the structures. The pre-CMOS technology requires customized CMOS process, which limits its applications.

One typical example of the intermediate-CMOS technology is the iMEMS[®] process developed by Analog Devices, Inc. (ADI) [69-71], originally dedicated for the fabrication of accelerometers and gyroscopes. It is customized based on their BiCMOS technology. LPCVD poly silicon deposition and annealing are inserted in the CMOS process steps to form the micromechanical structures. The feasibility of ADI's intermediate-CMOS technology has been proved by their products on market, but there are several drawbacks remaining. First, similar as the pre-CMOS technology, the inter-CMOS technology requires customized CMOS process, which means higher price than the standard process. Second, high-temperature annealing is required during the CMOS process, in order to reduce the residual stress of the mechanical structures, and it is potentially harmful to the formed CMOS layers. Third, the contamination during the switch between MEMS and CMOS processes would possibly be a serious problem.

3.1.2 Post-CMOS MEMS Technology

Post-CMOS MEMS technology has the potential to overcome the drawbacks of pre-CMOS and intermediate-CMOS technologies. Since the micromechanical structures are fabricated after the CMOS process is finished, it is possible to use standard CMOS

process, instead of expensive customized CMOS technology, to fabricate the electronics, as long as it is compatible with the micromachining process.

The post-CMOS micromachining can be categorized into two classes, thin-film technology and bulk technology, depending on what layer is used to form the micromechanical layer.

The thin film technology uses thin films, either from add-on layers or from CMOS chips, as the structure layers. The structure layers can be metal, dielectric, or other semiconductor materials, as long as they have the desired mechanical properties. The modularly integrated MEMS technology (MOD-MEMS) developed at UC-Berkeley can use either polysilicon or poly-SiGe as the structure materials. However, when polysilicon is used as the structure material, the aluminum interconnection of CMOS chips must be replaced with tungsten to sustain the high temperature for polysilicon annealing, and an extra TiN_4 barrier layer is required to prevent the reaction between silicon and tungsten, both of which are non-standard CMOS process [49, 72]. Texas Instruments uses a sputtered metal layer for the structures of digital micromirrors and deep-UV hardened photoresist as the sacrificial layer [73]. Other materials such as electroplated copper have also been reported as the structural materials for MEMS accelerometers [74].

The thin-film structure can also be formed by micromachining the CMOS surface layers. A high-Q RF MEMS filter was reported by IBM with the inter-metal dielectric layer as the structure layer [57]. A 256-pixel thermal image array and a CO gas sensor with dielectric layer as the structure material were reported by a research group at ETH in Switzerland [75, 76]. These technologies are all based on wet etching steps, which

imply challenge on the protection of the CMOS circuitry during etching and complicate the whole process.

Carnegie Mellon University developed a technology that involves dry etch steps to avoid the problems caused by wet etch [53, 77]. The micromechanical structure in this approach is predefined with metal layers on CMOS chips, which work as masks in the post-CMOS etching, therefore no lithography is needed and the process is simplified. Moreover, the multiple metal layers (normally 4~6 layers depending on technologies) provide high flexibility of the wiring and reduce the parasitics.

The main drawbacks of the thin-film technologies when they are applied to inertial sensor fabrication are: first, due to the small thickness of the device layer, the sensing capacitance is small; second, the thin-film structures suffer from serious residual stress [78], which limits the device size and complicates the process. Therefore, the performance of thin-film devices is limited.

Unlike the thin-film technology, the bulk micromachining process uses the substrate as the device layer. Carnegie Mellon University developed a DRIE bulk micromachining process based on their thin-film technology, and it has shown great advantages on the fabrication of large devices [77]. A large flat micromirror was obtained with the help of the bulk silicon underneath the mirror surface [79]. This process, however, has severe problems of undercut during the isotropic etching.

Qu of University of Florida developed a new DRIE bulk micromachining process to overcome the undercut problems. A three-axis accelerometer has been reported [58, 66]. The existence of the bulk silicon prevents the curling of the structure due to stress and increase the sensing capacitance and sensitivity as well.

3.2 Bulk Post-CMOS Process in This Work

The bulk micromachining post-CMOS process was reported for the first time to fabricate a three-axis accelerometer [58, 66]. Recently the process has been improved for the fabrication of gyroscopes to improve the yield [80]. The improved process flow is illustrated in Figure 3-1, of which each step is explained as the following.

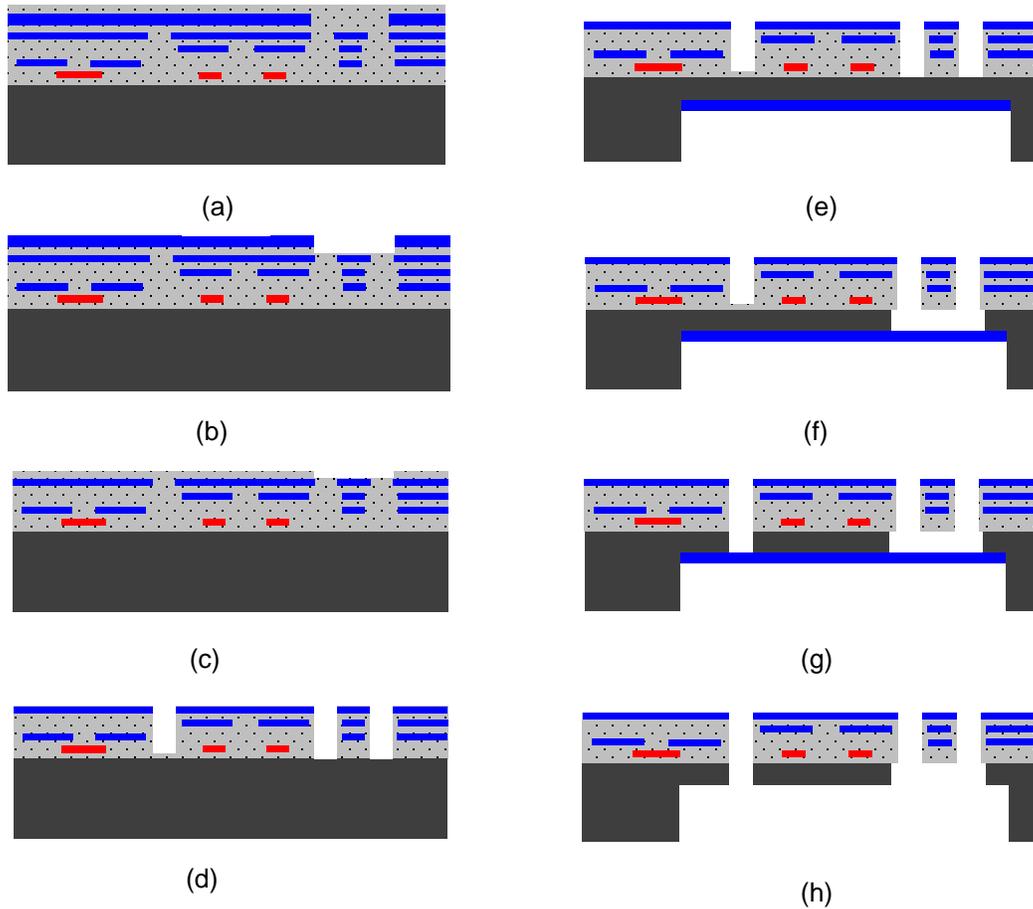


Figure 3-1. Process flow of the bulk micromachining post-CMOS process.

The process is started with a fresh standard CMOS die from the foundry. Firstly, a silicon dioxide (SiO_2) etching is performed to remove the top glass layer of the foundry CMOS chip (a, b). Protected by the Metal4 layer, most of the device area is not etched in this step except the isolation region of the comb fingers. The etching is controlled

precisely and is stopped at about 0.1-0.3 μm above the Metal3 layer which defines the structure. Then a wet Al etching removes the Metal4 layer and the Metal3 layer is protected by the SiO_2 on top of it (c). Since the SiO_2 in the isolation region is thinner than other regions, the silicon in the isolation region is exposed through a following anisotropic SiO_2 etching (d) while the silicon in other regions is still covered by a SiO_2 layer. Then, a backside silicon deep-reactive-ion etch (Si DRIE) forms a cavity with the remaining bulk silicon at the desired structural thickness ($\sim 40\mu\text{m}$). After that, a 0.2 μm -thick Al is sputtered on the backside (e). An isotropic Si etching forms the insulated structures (f), followed by another SiO_2 etching plus a deep Si etching to define the springs, comb fingers and other mechanical structures (g). In this step, the Al layer deposited in (e) forms a thermal path that eliminates the over-heating problem that causes the quick over-etch of the silicon underneath the isolated comb fingers. Furthermore, this Al layer also significantly reduces the DRIE footing effect and helps produce finer microstructures. Finally, an Aluminum dry etch step on the backside releases the microstructures (h).

One advantage of the process is the low cost, as the surface micromachining technology, because no masks are used during the processing. The metal layers on standard CMOS chips are used as the pre-deposited etching mask to define the sensor structures. Since the interconnection is realized with the metal layers, the noise from the wiring is expected low. The process in this work is based on the TSMC 0.35 μm 2P4M technology. Metal1 and Metal2 are for wiring, Metal3 defines the structure, and Metal4 helps to define the isolation regions on comb fingers to make the voltage on each finger can be defined individually.

The bulk micromachining technology enables the usage of the bulk silicon of the chip as the device layer, which increase the proof mass effectively. The thickness of the silicon is 30~50 μm , controlled by the etching time of the DRIE. The old process uses the photoresist as the thermal path, which tends to be carbonized during the DRIE processing and becomes hard to be removed by ashing. The aluminum layer is expected to have good thermal conductivity and is easy to remove. The CMOS-MEMS gyroscope mentioned in this work is fabricated with the improved process successfully. The extent of improvement of the new process over the old one still needs more investigation.

3.3 Fabricated Devices

Figure 3-2 shows a three-axis accelerometer fabricated with the bulk post-CMOS technologies. The CMOS circuits and the microstructure patterns are fabricated with the standard TSMC 0.35 μm technology. The interface circuits are covered by the metal3 layer, so they are invisible in the figure. The details of the comb fingers and the isolation region on the fingers are shown on the right side. The comb fingers are flat due to the single-crystal silicon underneath the metal films, and the silicon in the isolation area has been etched away to keep the fingers isolated from the proof mass electrically. The x/y axis detection is realized with the capacitive change caused by the in-plane movements of the proof mass, while the z axis detection is realized with the out-of-plane movements of an imbalanced proof mass anchored with torsional beams. The proof mass for the z-axis accelerometer is isolated with that for x/y-axis to reduce the cross axis couplings. The details of the three-axis accelerometer are summarized in Table 3-1.

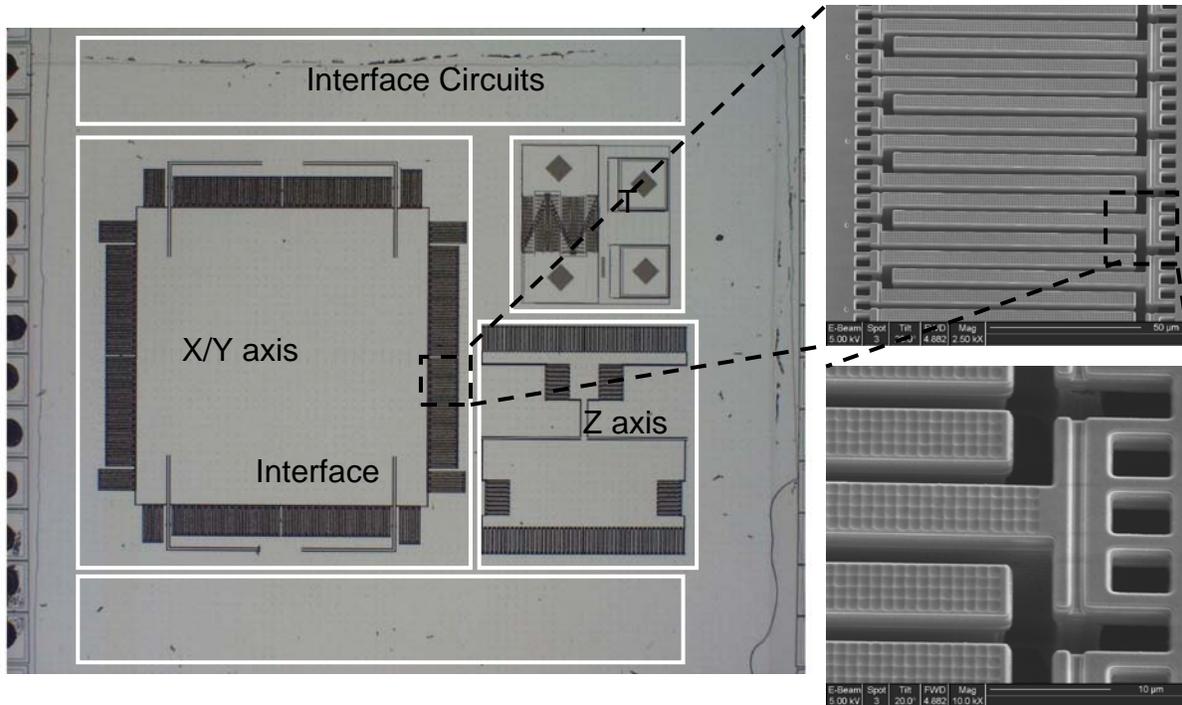


Figure 3-2. SEM photos of the three-axis accelerometer with separate proof mass.

Table 3-1. Summary of the mechanical structures design of the accelerometer.

Parameters	Values	
	x-y axis	z-axis
Overall size	1290 μm ×1330 μm	780 μm ×720 μm
Structure thickness	50 μm	50 μm
Proof mass	200 μg	29.5 μg
Springs (L_{sp} × W_{sp})	320 μm ×6 μm	720 μm ×5 μm
Sensing fingers (L_s × W_s)	85 μm ×4.8 μm	85 μm ×4.8 μm
Finger gap	3 μm	3 μm
Sensing capacitance	400 fF	86 fF
Mechanical sensitivity	10 nm/g	1.6 nm/g
Thermo-mechanical noise	7.5 $\mu\text{g}/\sqrt{\text{Hz}}$	34 $\mu\text{g}/\sqrt{\text{Hz}}$

A 5-axis IMU that comprises of a three-axis accelerometer, an x/y-axis gyroscope, and a z-axis gyroscope is then fabricated with the same micromachining process on a $5 \times 5 \text{mm}^2$ standard CMOS chip with Vanguard $0.35 \mu\text{m}$ technology. Figure 3-3(a) compares the chip with a US dime, and Figure 3-3(b) shows the microscopic picture of an released IMU. All the CMOS circuits are integrated with the MEMS structures and are protected by the metal3 layer during the post-CMOS processing.

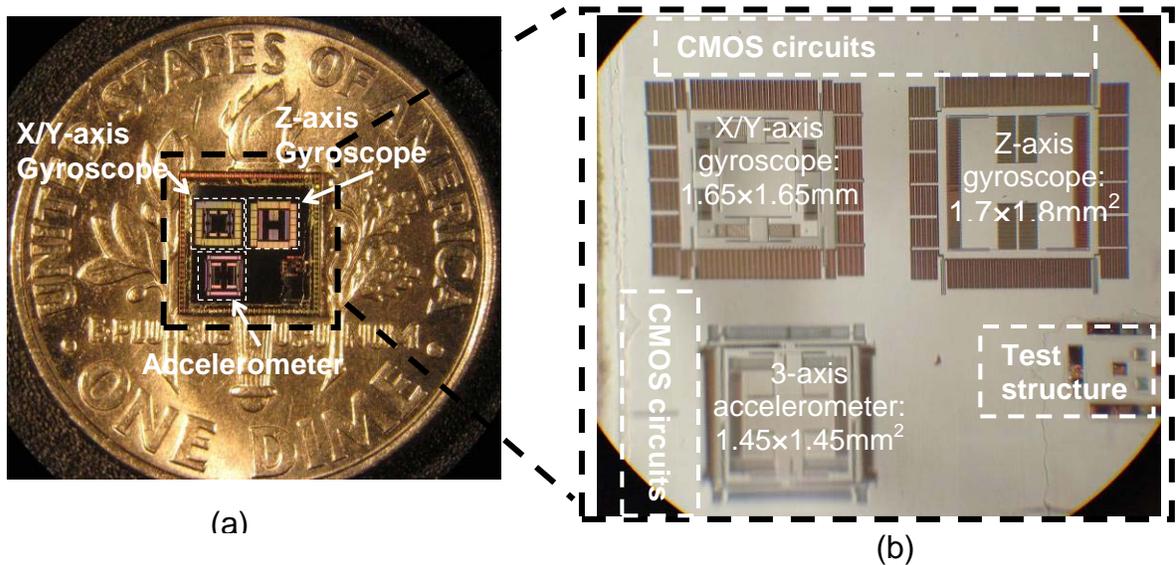


Figure 3-3. Photos of a fabricated 5-axis IMU chip. (a) the IMU chip compared with a US dime; (b) image under microscope.

Figure 3-4 shows the SEM photo of the three-axis accelerometer of the IMU. The sensor designs for the lateral axis are the same as the one mentioned above, but there are some improvements made on the z axis. The proof mass for the z axis is of symmetrical geometry and it is anchored with two vertical springs evenly. The symmetrical design eliminates the serious coupling from the y axis existing in the previous design. The z-axis accelerometer shares the proof mass with the x/y axis in order to save area on the chip.

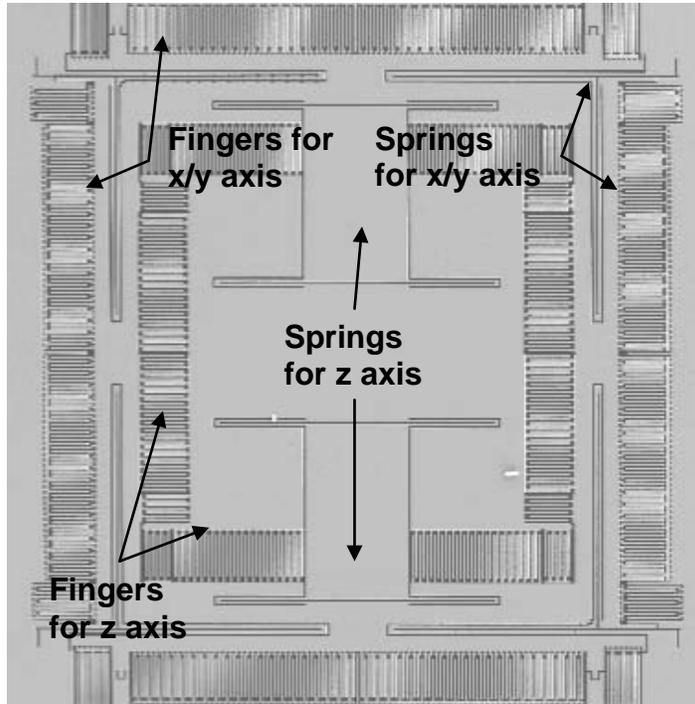


Figure 3-4. SEM photo of the improved three-axis accelerometer.

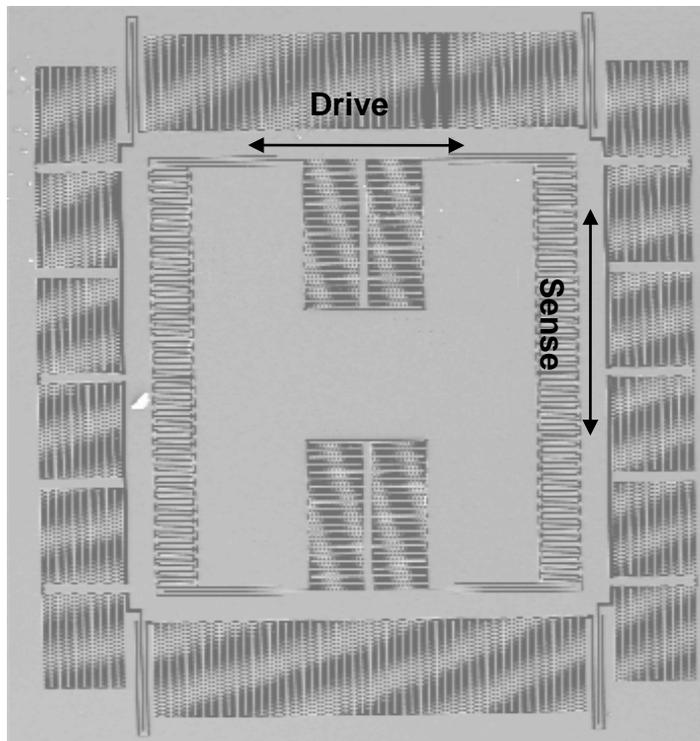


Figure 3-5. SEM photo of the z-axis gyroscope.

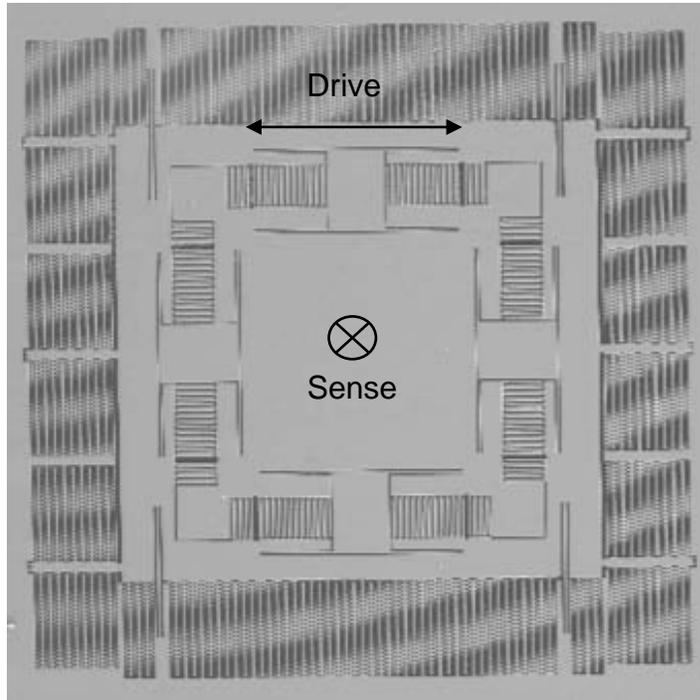


Figure 3-6. SEM photo of the x/y-axis gyroscope.

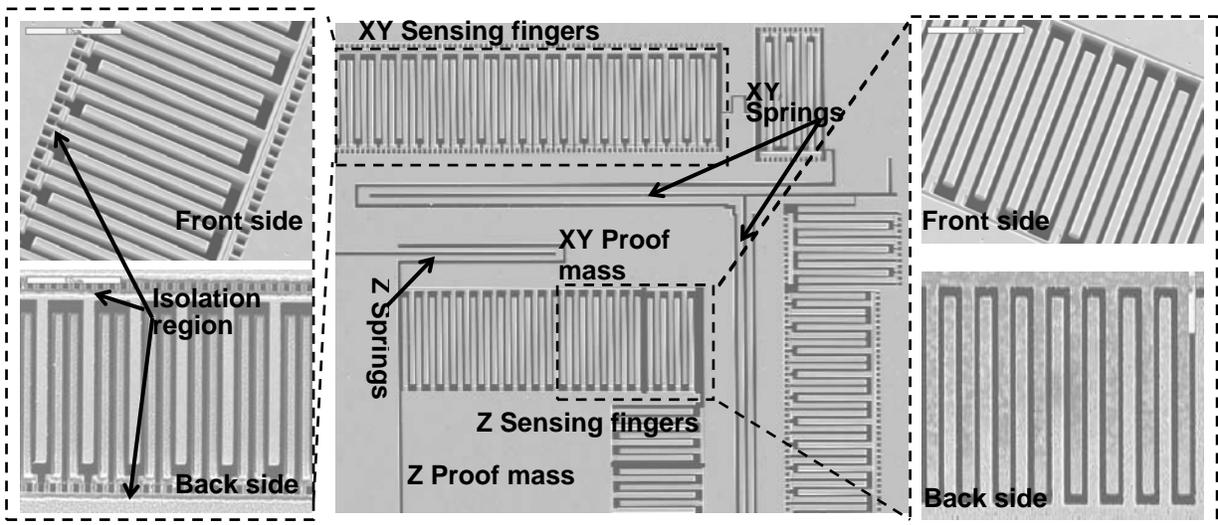


Figure 3-7. SEM images of a quarter of the 3-axis accelerometer with the details of the X/Y sensing fingers and the Z sensing fingers.

The SEM photo of the z-axis gyroscope is shown in Figure 3-5. The proof mass is driven in the horizontal direction and the Coriolis acceleration occurs in the vertical direction, so all the movements are in-plane.

The SEM photo of the x/y axis gyroscope is shown in Figure 3-6. The proof mass is driven horizontally to move in plane, while the Coriolis acceleration occurs out of plane.

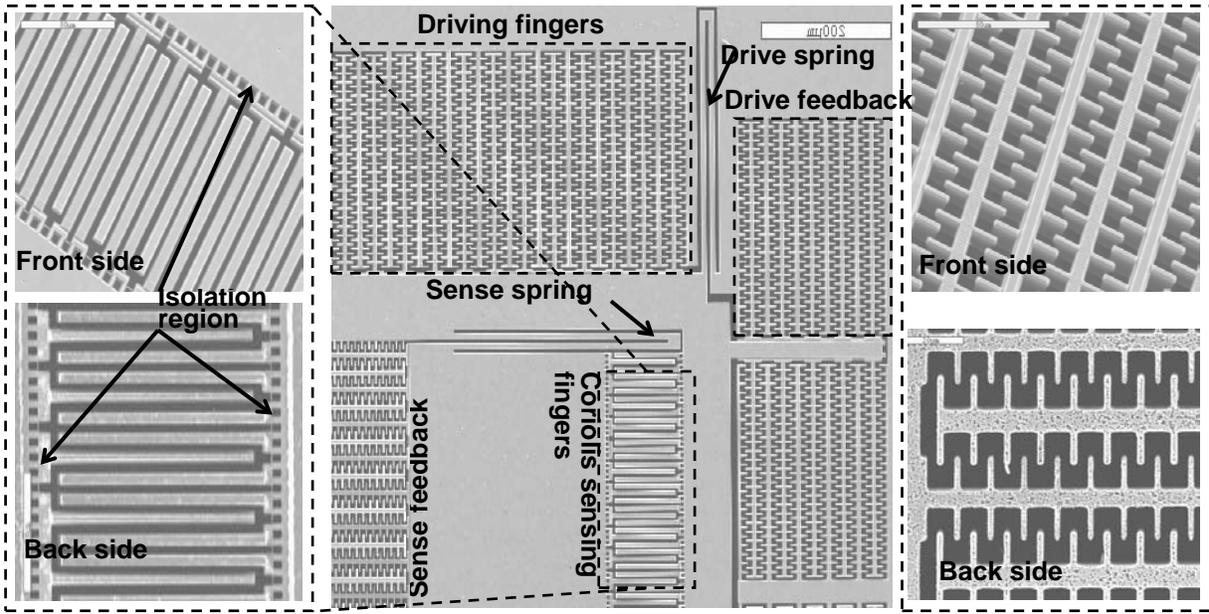


Figure 3-8. SEM images of a quarter of the z-axis gyroscope with the details of the sensing fingers and the driving fingers.

The released comb fingers and their functions are shown in Figure 3-9, Figure 3-8, and Figure 3-9. In order to show more details within one figure, only a quarter of each device is shown. It should be noticed that the Coriolis sensing fingers for in-plane detection have the isolation regions at their roots, such as the fingers of the x/y accelerometers and the sensing fingers of the z-axis gyroscope, while those for out-of-plane detection, such as the fingers of the z-axis accelerometer and the x/y-axis gyroscope, do not. The SEM photos indicate that all the mechanical structures have been released completely and the isolation regions have been formed successfully. Therefore, the feasibility of the bulk post-CMOS process is verified.

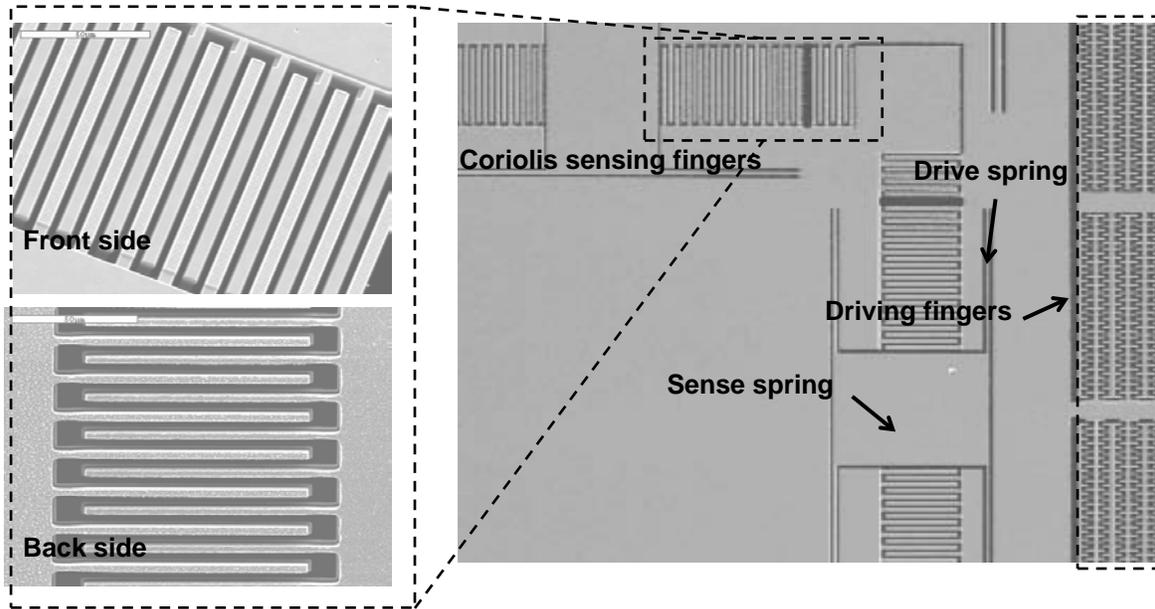


Figure 3-9. SEM images of a quarter of the x/y-axis with the details of the sensing fingers.

CHAPTER 4 READ-OUT CIRCUITRY AND SYSTEMS FOR CAPACITIVE MEMS SENSORS

The target signal of the capacitive inertial sensors (acceleration and rotation rate) is converted to the capacitance change. The read-out circuitry works to convert the capacitance change to the electric signals that can be further processed with other electronics module like amplifiers, filters, data converters, etc. The electric signals can be voltage, current, or frequency. The capacitance change is typically converted to voltage. Basically there are two fundamental front ends for the conversion, the discrete-time front ends and the continuous-time counterpart. Both two types will be discussed in details in this chapter. The capacitance-to-frequency (C/f) conversion is also possible, in which case, the capacitance change modulates the fundamental frequency of the signal. It can be implemented as a resonator with its frequency dependent on the sensing capacitance. The discussion of the C/f converter is beyond the scope of this work so no more details will be introduced.

Due to the complexity of the electronics for gyroscope, the system designs of other groups will be particularly introduced after the discussions on the front ends. The technologies of their sensors will be introduced as well to make the information complete.

4.1 Front Ends for MEMS Inertial Sensors

4.1.1 Discrete-Time Front Ends

The typical implementations of discrete-time front ends for capacitive sensors use the switched-capacitor (SC) architecture [51, 55, 60, 81-83]. The switched-capacitor front-end takes the samples from the sensors at periodical time and output it for further processing. A typical SC voltage amplifier is schemed in Figure 4-1. When Φ_1 is high,

the voltage signal from the source is sampled to the capacitor C_1 , while the feedback capacitor C_2 is discharged. When ϕ_2 is high, C_1 is discharged and its stored charge is transferred to C_2 , so the voltage signal sampled at the dropping edge of ϕ_1 is transferred to the load capacitance with the gain of $(-C_1/C_2)$. Regarding the capacitive inertial sensor, C_1 is replaced with C_s , the sensing capacitor of the sensor, whose value is variable depending on the external mechanical signal. The input voltage source becomes an ac or dc reference voltage, V_{ref} . The output signal is then written as

$$v_{out} = \frac{\Delta C_s}{C_2} \cdot V_{ref}$$

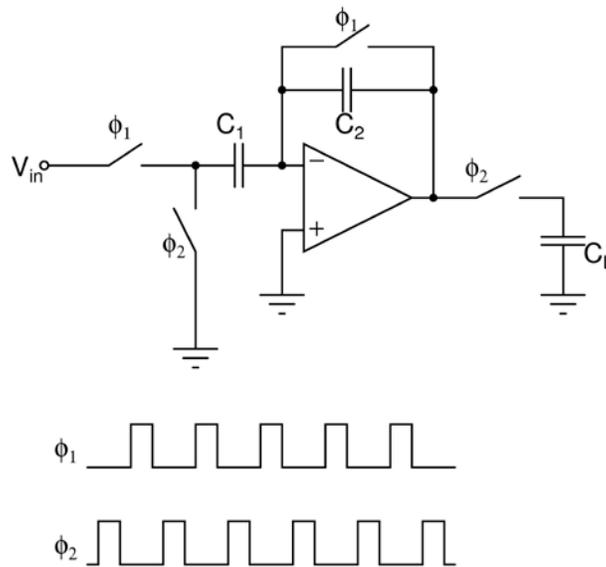


Figure 4-1. Schematic of an SC voltage amplifier

The SC front end provides a stable virtual ground, so the output signal is immune to the parasitic capacitance. Furthermore, the SC circuit can be easily integrated with the $\Sigma\Delta$ module to provide a digital output.

The noise of the SC front ends contains two major parts. One of them is due to the switching behavior. The switch made of a MOS transistor can be modeled as a resistor

when it is at “on” state, and its thermal noise is sampled at the moment when the switch is turned off. The power of the noise is proportional to the value of $k_B T / C_s$, where k_B is the Boltzmann constant, T is the absolute temperature, and C_s is the sensing capacitance of the sensor. The capacitance of the MEMS inertial sensor is usually in the order of pF ($10^{-12} F$) or sub pF , and the calculated sampling noise is in the order of tens of μV ($10^{-6} V$), which is a significant noise source.

The other major noise contributor is the noise from the amplifier in the feedback loop, which comprises of thermal noise and flicker noise. The total noise from the amplifiers is lumped to the input node and the output noise is derived in (4-1). The flicker noise is also called $1/f$ noise, whose power spectral density is inversely proportional to frequency. At the resonant frequency of an inertial sensor, the flicker noise is usually the dominant component. The effects of the flicker noise can be reduced by increasing the sampling frequency, but a larger bandwidth is required to keep the loop gain large enough, which usually means higher power dissipation.

$$\frac{v_{n,out,amp}}{C_2} = \frac{C_s + C_p}{C_2} \cdot v_{n,m,amp} \quad (4-1)$$

Another issue coming with the increased bandwidth is called noise folding, which is illustrated in Figure 4-2. According to the sampling theorem, the sampled signal in the frequency domain is

$$X_s(\omega) = \frac{1}{T} \sum_{n=-\infty}^{+\infty} X_s(\omega - n\omega_s) \quad (4-2)$$

T_s and ω_s represent the sampling period and the sampling frequency, respectively. It can be observed that the noise at the frequencies of the higher order harmonics of the sampling signals will be folded back to the base band and be added into the total noise.

The equation assumes an infinite bandwidth, which is not true in the real case. So the number of the harmonics, n , is determined by the bandwidth of the amplifier in the feedback loop. In SC circuits, the bandwidth of the amplifier is usually several times larger than that of the signal to ensure that the circuit behaves properly. Assuming the bandwidth of the amplifier is BW , and

$$BW = Nf_s \quad (4-3)$$

The spectrum of the signal and the noise will be

$$\begin{aligned} v_s(f) &= \frac{1}{T_s} \sum_{n=-N}^{+N} v_0(f - nf_s) \\ &= \frac{1}{T_s} v_0(f) \end{aligned} \quad , \quad -\frac{f_s}{2} < f < \frac{f_s}{2} \quad (4-4)$$

and

$$n_s(f) = \frac{1}{T_s} \sum_{n=-N}^{+N} n_0(f - nf_s) \quad (4-5)$$

The power of the signal and the noise is

$$S_s(f) = \frac{1}{T_s^2} S_0 \quad (4-6)$$

and

$$N_s = \frac{1}{T_s^2} NN_0 \quad (4-7)$$

So the signal-to-noise ratio after sampling is reduced by a factor of N :

$$\frac{S_s}{N_s} = \frac{1}{N} \cdot \frac{S_0}{N_0} \quad (4-8)$$

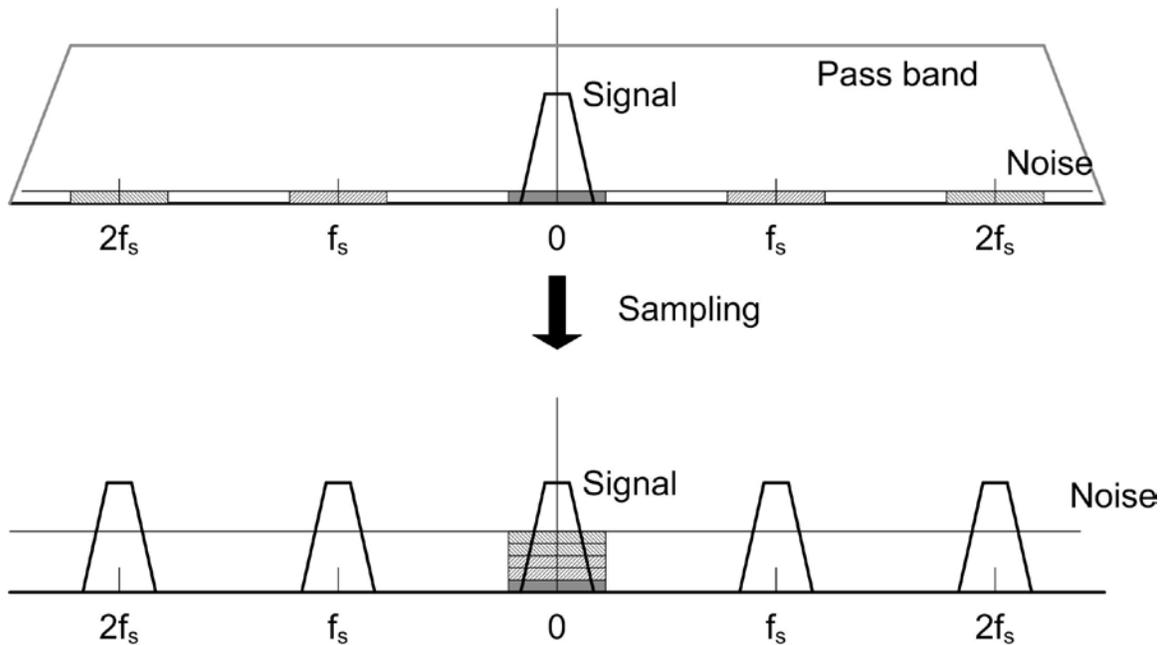


Figure 4-2. Illustration of noise folding.

The correlate-double-sampling (CDS) is applied on the SC front-ends to reduce the flicker noise and sampling noise [84, 85], as shown in Figure 4-3. It requires that the sampling frequency much higher than the resonant frequency of the sensors, which implies higher power dissipation. The noise folding still exists in the SC front-ends with CDS as well.

4.1.2 Continuous-Time Front Ends

Unlike the switched-capacitor circuitry, the continuous-time front-ends pick up and amplify the signal from the sensing capacitors continuously. The continuous-time front-ends are typically implemented as either open-loop voltage amplifiers or transimpedance amplifiers.

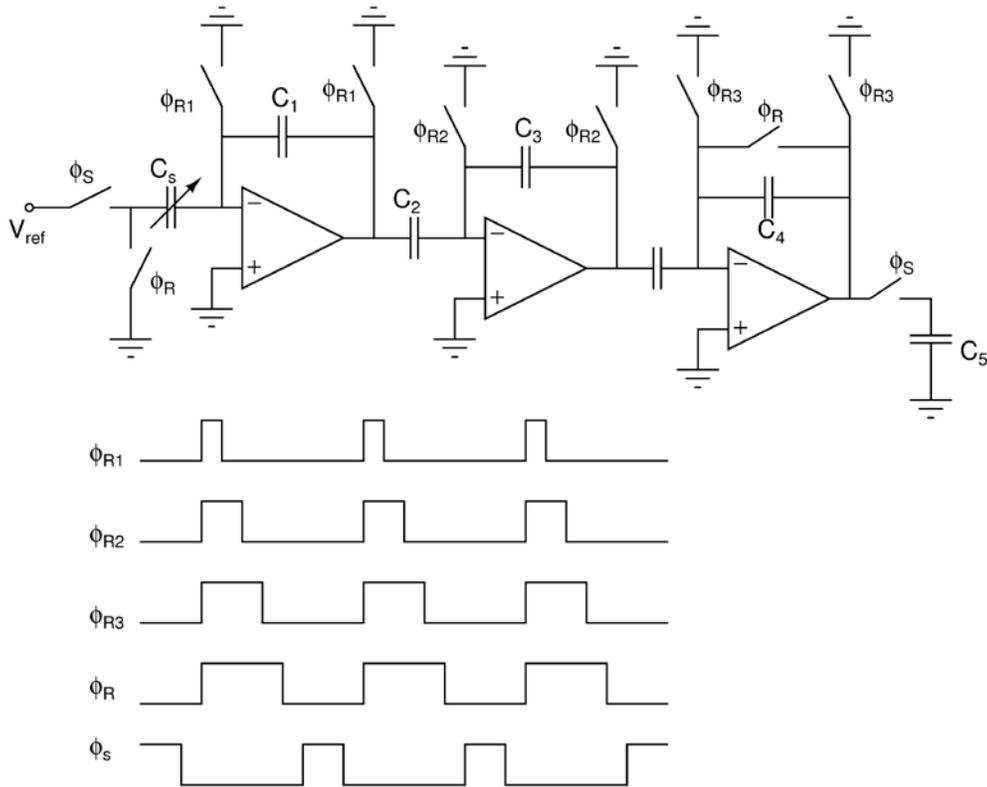


Figure 4-3. Schematic of an SC circuits with CDS.

4.1.2.1 Closed-loop amplifiers

A typical transimpedance (TIA) amplifier is schemed in Figure 4-4 [48, 86, 87]. R_f and C_f represent the resistive and capacitive feedback impedance, respectively, and C_p represent the parasitic capacitance. The equivalent impedance is

$$Z_e(j\omega) = \frac{R_f}{1 + j\omega C_f R_f} \quad (4-9)$$

Assuming the ideal amplifier, the output signal can be derived easily as:

$$V_{out}(j\omega) = \frac{j\omega \Delta C(j\omega) R_f}{1 + j\omega C_f R_f} V_m \quad (4-10)$$

Because of the virtual ground provided by the feedback loop, the output signal is immune to C_p , and this is an important advantage of the transimpedance amplifier.

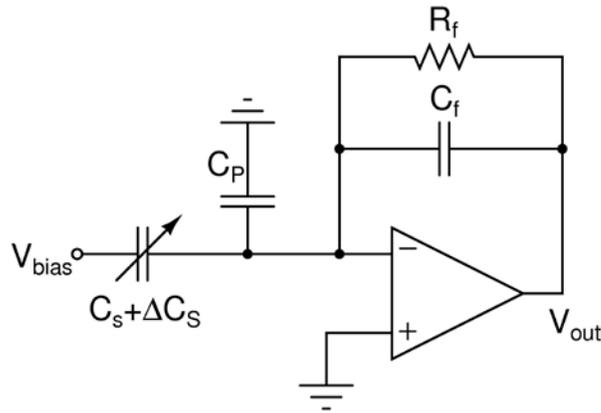


Figure 4-4. Interface of a Transimpedance amplifier to a sensor.

The behavior of the transimpedance depends on the selection of the parameters.

If

$$C_f R_f \gg \frac{1}{\omega},$$

where ω is the operating frequency of the input signal, then (4-10) reduces to

$$V_{out}(j\omega) = \frac{\Delta C(j\omega)}{C_f} V_m \quad (4-11)$$

The output signal is proportional to the ratio of the sensing capacitance change over the feedback capacitance, but independent on its frequency. The configuration with large RC constant has a high-pass behavior, so the dc offset of the amplifier will not affect the output signal. The transimpedance amplifier in this configuration is also called transcapacitance amplifier (TCA). The gain of the TCA is frequency-independent, and the output signal is in phase with the capacitance change.

If

$$C_f R_f \ll \frac{1}{\omega},$$

(4-10) becomes

$$V_{out}(j\omega) = j\omega\Delta C(j\omega)R_f V_m \quad (4-12)$$

The amplifier shows a frequency-dependent gain, and the output signal has a 90° phase leading the capacitance change. The phase shifting property is useful in the excitation loop of the primary resonator, because it can compensate the 90° lagging of the transducer at the resonant frequency for a 0° phase delay resonator loop.

For a transimpedance amplifier, both the resistor and the capacitor are necessary. The resistor provides a dc path for the feedback path to avoid the saturation due to dc offset of the amplifier, while the capacitor helps to stabilize the loop.

The output noise of a TIA is written as

$$\overline{v_{n,out}^2} = \frac{j\omega(C_s + C_p)R_f}{1 + j\omega C_f R_f} \cdot \overline{v_{n,in,amp}^2} + 4kTR_f \quad (4-13)$$

The two terms describe the noise from the amplifier and that from the feedback resistor. On one hand, the input-referred noise of the amplifier is amplified by a factor, which is called noise gain, to the output; on the other hand, the feedback resistor adds more noise. The noise from the resistor might be significant, depending on the parameters choice. A trade-off arises between the noise and the gain of the TIA. From (4-11) and (4-12), the gain of the TIA is expected to be properly high, so that the signal-to-noise ratio will not be degraded much by the noise from the following stages. In the TCA, configuration, high gain requires small C_f , and in order to satisfy the condition that $R_f C_f \gg 1/\omega$, the resistance needs to be very high, in the order of hundreds of MΩ to GΩ. The gain of the TRA is determined by R_f , although $R_f C_f \ll 1/\omega$, the required R_f is still in the order of 10 MΩ to get proper gain, and the value of C_f should be very small, which is

hard to realize with the typical Poly-insulator-poly (PIP) on-chip capacitors. The large feedback resistance adds so much noise to the amplifier that can be the dominant noise source.

The operation at a modulated high frequency helps to relax the requirement on the passive devices to reduce the noise. However, high frequency implies at the same time larger bandwidth and larger power dissipation to ensure the phase shift within a certain range. The details of frequency are discussed in 4.1.2.3.

4.1.2.2 Open-loop amplifiers

Unlike the TIA whose gain is set by the component parameters in the feedback loop, the gain of the open-loop amplifier is set by the parameters of the amplifier itself [52, 88-90]. The simplest case of an open-loop amplifier is the common-source configuration of a single transistor. Figure 4-5 illustrates the interface between the detection capacitor and the open-loop amplifier. The output signal is then

$$v_s = \frac{\Delta C_s}{2C_s + C_p + C_{gs} + (1 + g_m R_{load})C_{gd}} \cdot V_m \quad (4-14)$$

C_s is the sensing capacitance, C_p is the parasitic capacitance from wiring, C_{gs} is the gate-to-source capacitance and C_{gd} is the gate-to-drain capacitance of the input MOS transistors, and V_m is the amplitude of the modulation signal that is applied to the sensing capacitors. A gain factor of $(1 + g_m R_{load})$ is put in front of C_{gd} , with the miller effects taken into consideration.

The unity-gain buffer [91, 92] is categorized into the open-loop amplifiers in this work, although its gain is set by the feedback loop with zero impedance. The sensor is not connected to the virtual ground of the unity-gain buffer, so the output signal still

suffers from the parasitic capacitance, which is fundamentally different from the TIA mentioned in the previous sections.

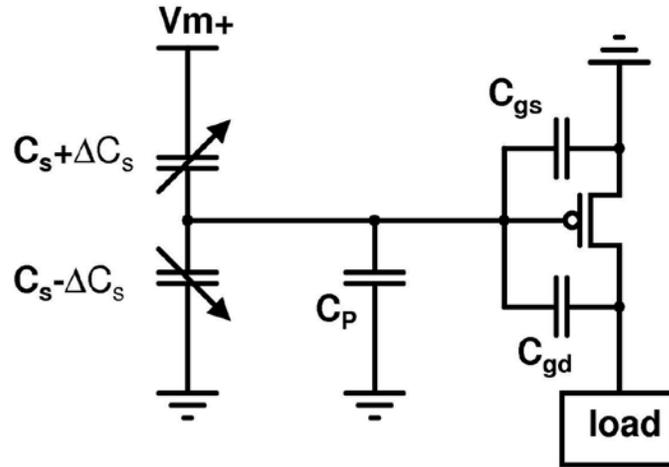


Figure 4-5. Interface of an open-loop amplifier to a sensor.

The output noise of the open-loop architecture is

$$\overline{v_{n,out}^2} = G^2 \overline{v_{n,in,amp}^2} \quad (4-15)$$

4.1.2.3 Noise, bandwidth and power

There are two major types of noise existing in the CMOS analog circuits, the thermal noise and the flicker noise. The thermal noise is also called white noise because its spectrum is uniformly distributed at all frequency. The thermal noise of a MOS transistor in saturation region is

$$\overline{v_{n,thermal}^2} = \frac{4kT}{g_m} \quad (4-16)$$

$$g_m = \sqrt{2\mu_{eff}C_{ox}(W/L)I_D} \quad (4-17)$$

g_m is the transconductance of the transistor, μ_{eff} is the effective mobility of the carriers, C_{ox} is the gate capacitance density, (W/L) is size of the transistor, and I_D is the dc bias current. The flicker noise is also called pink noise, whose equation is

$$\overline{v_{n, flicker}^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \quad (4-18)$$

The flicker noise is a frequency dependent noise, which is more significant at low frequency and decays as the frequency increases. The comparison of the two noise sources with respect to the frequency is shown in Figure 4-6. At the frequency of the MEMS inertial sensors, usually in the order of kHz, the flicker noise dominates in the total noise. So the idea comes up to modulate the capacitance change information to a carrier signal at higher frequency to reduce the noise level.

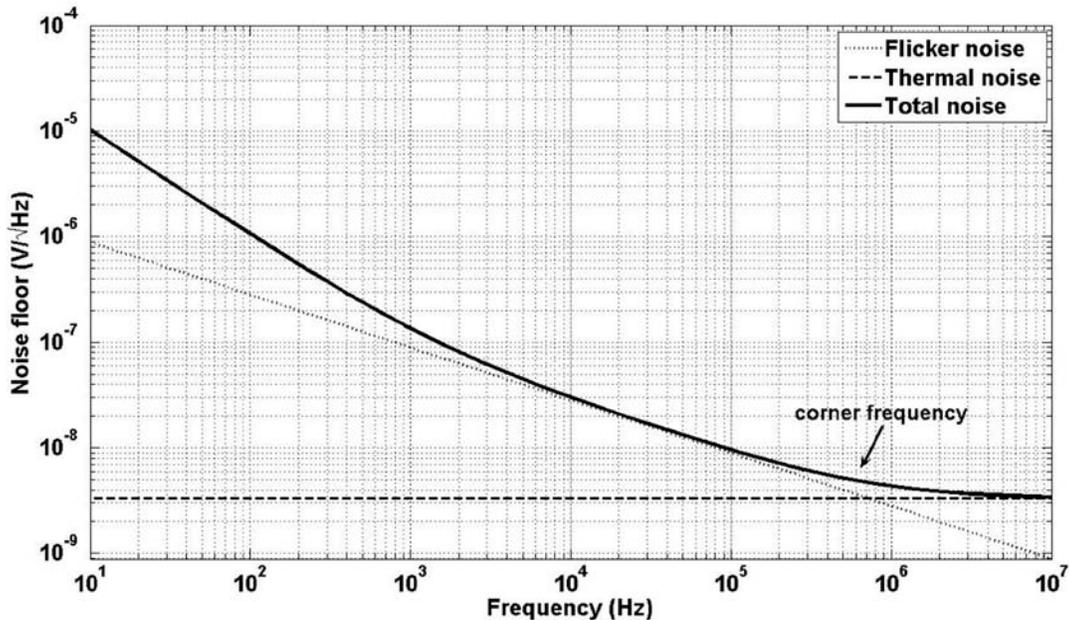


Figure 4-6. Flicker noise and thermal noise vs. frequency.

The continuous-time front-ends can work either at the baseband frequency or at a higher carrier frequency, as shown in Figure 4-7.

The output signals of the TIA and the open-loop amplifiers are

$$v_{out}(j\omega) = \frac{j\omega\Delta C_s(j\omega)R_f}{1 + j\omega C_f R_f} V_m \quad (4-19)$$

and

$$v_{out}(j\omega) = \frac{\Delta C_s(j\omega)G}{2C_s + C_p + C_{gs} + (1 + g_m R_{load})C_{gd}} \cdot V_m \quad (4-20)$$

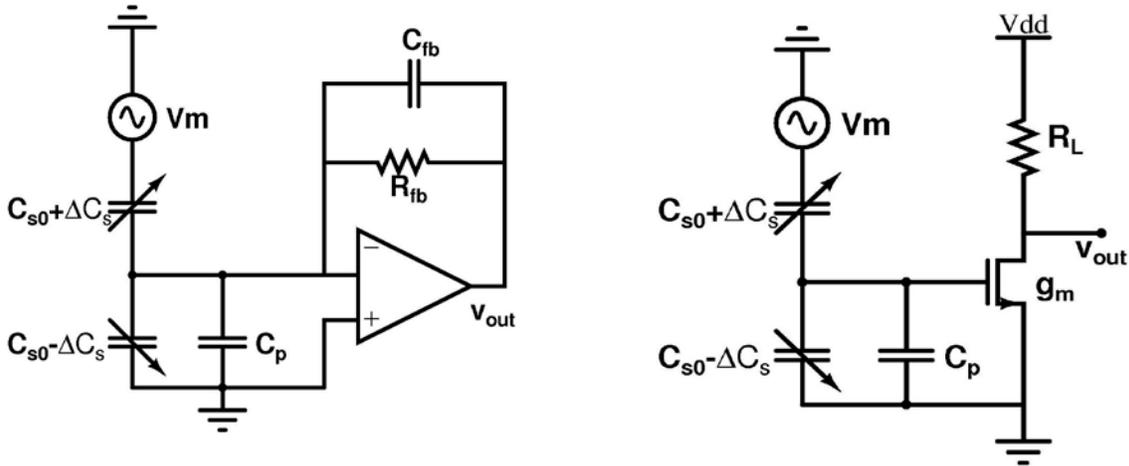


Figure 4-7. TIA and open-loop amplifier working at carrier frequency.

The equations have the same expression as those previously listed, but V_m in (4-19) and (4-20) means an ac modulation signal with the frequency of f_m . It should be noted that the ΔC in (4-10) and (4-14) represent only the capacitance change due to the external mechanical signal, while the capacitance mismatch during fabrication does not affect the output signal. In (4-19) and (4-20), however, the capacitance mismatch is also modulated to the carrier frequency and is included in the term ΔC . The capacitance change of the capacitive sensors is usually small, so the signal due to the mismatch can easily overwhelm the desired signal and saturate the circuits, if the gain is high.

The equations (4-10) and (4-14) assume an infinite bandwidth of the amplifier for the simplicity of the analysis, which is not true in the real cases. A more realistic analysis can be done, assuming that the core amplifiers are well compensated with the dominant pole at ω_{p1} . The spectrum of the output signals of the open-loop amplifier and the TIA are

$$\begin{aligned} v_{out}(j\omega) &= \frac{\Delta C_s(j\omega)G_{open}}{2C_s + C_p + C_{gs} + (1 + g_m R_{load})C_{gd}} \cdot \frac{1}{1 + j(\omega / \omega_{p1})} V_m \\ &= v_{out_ideal}(j\omega) \cdot \frac{1}{1 + j(\omega / \omega_{p1})} \end{aligned} \quad (4-21)$$

and

$$\begin{aligned} v_{out}(j\omega) &= \frac{j\omega\Delta C_s(j\omega)R_f}{1 + j\omega C_f R_f} \cdot \frac{1}{1 + \frac{(1 + j\omega R_f(C_f + C_s))(1 + j(\omega / \omega_{p1}))}{G_{open}(1 + j\omega R_f C_f)}} V_m \\ &\approx v_{out_ideal}(j\omega) \cdot \frac{1}{1 + j(G_{cl}\omega / G_{open} \cdot \omega_{p1})} \end{aligned} \quad (4-22)$$

$$G_{cl} = \frac{C_f + C_s}{C_f} \text{ for transcapacitance amplifier, and}$$

$$G_{cl} = 1 + j\omega R_f C_f \text{ for transresistance amplifier.}$$

where G_{open} is the open-loop gain, and G_{cl} is the close-loop gain of the TIA.

The finite bandwidth of the core amplifier leads to an extra phase shift φ . For open-loop configurations,

$$\varphi = \tan^{-1}\left(\frac{\omega}{\omega_{p1}}\right) \quad (4-23)$$

and for the TIA,

$$\varphi = \tan^{-1}\left(\frac{G_{cl}\omega}{G\omega_{p1}}\right) \quad (4-24)$$

The gain bandwidth product GBW is derived as

$$\begin{aligned}
 GBW &= \frac{G_{eff} \omega}{\tan \varphi} = \frac{g_m}{C_L} \\
 &= \frac{\sqrt{2\mu_{eff} C_{ox} (W/L) I_D}}{C_L}
 \end{aligned} \tag{4-25}$$

G_{eff} is the effective gain of the front-ends, which is equal to G_{open} in open-loop architectures and G_{cl} in closed-loop architectures. So a universal equation is derived to relate the phase delay of both configurations to the power dissipation. In short words, less phase delay means more power.

The requirement of the phase delay of the sensed signal is strict for MEMS gyroscopes, because the excessive phase delay in the excitation loop cause the primary resonator to resonate not at the natural frequency with degraded amplitude, and that in the sense path leads to serious zero-rate output (ZRO). Some accelerometers, especially those on portable devices, have stringy requirement on power dissipation but less on the phase delay, so the phase delay can be properly large for the optimization of power.

Another important issue is the optimization of the front-ends for best performance on noise. By looking at (4-16) and (4-18), both the flicker noise and the thermal noise are related to the transistor sizes, and generally the larger size means lower noise. However, larger transistor size brings more parasitic capacitance, which degrades the desired signal in the open-loop configuration. So there should be an optimal size for the best SNR, which satisfies

$$\frac{\partial SNR}{\partial W} = 0 \tag{4-26}$$

Only the width of the transistor is considered in this equation, because the length is usually the available minimum size after considering such factors as the dc offset, and the layout issue, to reduce the power consumption.

4.2 State-of-the-Art Works

Almost all the published MEMS gyroscopes are based on the vibratory concept. This section will review the available literatures about the MEMS gyroscopes with their readout-out electronics. There are a large amount of publications talking about the MEMS structures only, but they are beyond the scope of this work. The research on gyroscopes is currently a hot topic, and there are many new publications coming up every year. Due to the system complexity, the previous works of the gyroscope will be reviewed by the institutes for better understanding.

The Berkeley Sensors and Actuators Center (BSAC) at the University of California, Berkeley has the traditional to use the digital force feedback to construct an electromechanical sigma-delta loop. The architecture was firstly implemented with accelerometers and was published in 1992 [49-51, 93]. The first published gyroscope systems are the works of Clark and Junear from the year 1996 [94, 95]. The primary resonator is excited with a loop implemented with a transresistance amplifier and an automatic gain control (AGC) loop that controls the exciting signal at the certain amplitude. The Coriolis signal is modulated to a higher carrier frequency and sensed by a charge sensitive amplifier (CSA). The demodulation signal is provided by a phase lock loop (PLL). In the work of Seshia in 2002 [38], the angular rate is resolved by measuring the frequency drift of the third resonator, whose resonant frequency is affected by the compressive stress caused by the Coriolid force. Jiang in 2000/2002 [39, 96], and Petkov in 2004 [97, 98] used SC circuits as the front ends of the sense mode, and

Coriolis detection is based on the higher-order electromechanical $\Sigma\Delta$ loop. All these works are based on surface micromachining technology.

Analog Devices Inc. (ADI) published parts of their design of the ADXRS150 gyroscope in 2002 [48]. The MEMS device and the circuitry are integrated on a single chip. The primary resonance loop contains a transresistance amplifier and a comparator, while the Coriolis signal is sensed by a transcapacitance amplifier and then demodulated by the signal from the primary resonator. The gain accuracy is improved by the open-loop temperature compensation, in which the gain of the Coriolis signal is tuned according to the temperature from a Proportional-to-Absolute-Temperature (PTAT) sensor. The structure is fabricated with a 3- μm BiCMOS process with 4- μm poly silicon structural layer.

Robert Bosch GmbH, Germany, is another main manufacturer of MEMS gyroscopes. All the three generations of their sensors, DRS-MM1, DRS-MM2, and DRS-MM3 have been published. The first one, DRS-MM1 from the year 1997 [14], is fabricated using combined bulk and surface micromachining of silicon substrate with 12- μm -thick polysilicon layer (epi-poly). The last two sensors, DRS-MM2 in 1999 [99] and DRS-MM3 in 2005 [17], are both based on surface micromachining technology. In the latest version of DRS-MM3, the drive mode is excited with a PLL, and the amplitude of the drive signal is controlled by an AGC. The force feedback is established in the detection loop for a close-loop control and there is temperature compensation to improve the gain accuracy.

Carnegie Mellon University has developed a post-CMOS process that does not require etching masks. The process uses the metal layer on standard CMOS chips as

the mask to define the structures and to make the interconnections, so it is also a surface micromachining technology. There are several gyroscopes reported by Xie [100] and Luo [101], which are all single-chip solutions. The read-out circuit is realized with unity-gain buffer, and the details of the electronics are reported in [102].

Georgia Institute of Technology has a gyroscope fabricated by micromachining an SOI substrate, whose device layer is 40 μm to 50 μm [103], and an electronic system is reported by Sharma [86]. The signals of both the drive mode and sense mode are read out by transimpedance amplifiers. The amplitude of the drive signal is controlled by an AGC. The rotary rate is obtained by demodulating the sense-mode signal with a clock from a PLL and filtering the signal with the off-chip low-pass filter.

Helsinki University of Technology has reported a gyroscope system with the device from VTI Technologies [104]. The device has two orthogonal torsional springs so that there is no mechanical coupling between the two modes. The device is fabricated with the bulk micromachining technology and the structure wafer is sandwiched into two wafers with electrodes. The system is a two-chip solution, the front-end amplifiers in both the drive mode and sense mode are realized with transcapacitance amplifiers. The system introduces the discrete signal processing (DSP) to work with the analog front end to realize the control and sense function.

ST Microelectronics performs well in the consumer electronics market, and their devices are all manufactured by thick polysilicon with the epi-poly technology. In the recently reported gyroscope system, time division is used to read out the Coriolis signal from three axes with only one channel. The Quadrature error is compensated before it is fed into the main SC charge amplifier [105].

The Invensense Inc. has invented a so-called Nasiri process, which use the wafer-level bonding to reduce the packaging cost. The device wafer is firstly processed and bonded to the circuit wafer, then the last etching step is executed and the device is released. The details of their gyroscopes have not been published yet.

4.3 Summaries

The SC and closed-loop front ends have been widely used, for their robustness and the immunity to parasitic capacitance, which is the shortcoming of the open-loop architectures. So they are very suitable for the two-chip approach, which suffers from large parasitic parameters. The main advantage of the open-loop front ends over the other architecture is their low noise floor. In CMOS-MEMS technologies, the parasitic parameters are much smaller than the two-chip solutions, while the sensing capacitance is relatively small, so noise from the electronics is the major issue. Therefore, the open-loop architecture is a better solution for CMOS-MEMS inertial sensors. The simple open-loop amplifier suffers from worse linearity and power supply reject ratio, and the gain set by resistive load is sensitive to temperature. These issues will be solved by the design discussed in the next two chapters.

Particularly for MEMS gyroscopes, because of the complexity of the system, the system design is very important too. For the drive mode, most of the published works use continuous-time electromechanical self-oscillation loop with certain mechanisms for automatic gain control. Those methods ensure the stable oscillation and the good linearity. In the sense mode, SC, TIA, unity-gain buffer, and open-loop amplifiers are all reported as the front ends. A very important matter is the precise phase control, which eliminates the effects of quadrature error and increases the dynamic range of the system. The DSPs or computer control add more freedom of the system and improve

the performance, but for the CMOS-MEMS sensors, the analog solutions are sufficient for the development and verification purpose.

CHAPTER 5 IMPROVED DUAL-CHOPPER AMPLIFIER FOR CMOS-MEMS ACCELEROMETERS

In this chapter, the details of the dual-chopper amplifier for CMOS-MEMS will be discussed in details. The idea of the DCA has been reported by Fang [88, 106], and there is some improvements in this work for better performance. This chapter will start from the lumped model of an accelerometer and go through the whole design and optimization procedures to the experimental results.

5.1 Dual-Chopper Amplifier

5.1.1 Noise Model and Optimization

Figure 5-1 shows the equivalent model of the capacitive sensing front-end circuit. For the sake of analysis simplicity, only half of the common-source differential pair is schemed, and the input PMOS transistor is shown as a small-signal model. M_{bias} , a MOS-bipolar pseudo-resistor, is connected to the gate of the input transistor to provide the proper DC bias while maintaining large AC impedance [107]. The electrical signal at the gate of the input transistor is governed by the following equation:

$$v_s = \frac{\Delta C_s}{2C_s + C_p + C_{gs} + (1 + g_m R_{load})C_{gd}} \cdot V_m \quad (5-1)$$

where C_s is the sensing capacitance, C_p is the parasitic capacitance from wiring, C_{gs} is the gate-to-source capacitance and C_{gd} is the gate-to-drain capacitance of the input MOS transistors, and V_m is the amplitude of the modulation signal that is applied to the sensing capacitors. A gain factor of $(1+g_m R_{load})$ is put in front of C_{gd} in (5-1), with the miller effects taken into consideration. Figure 5-1 also lumps various noise sources existing in the front end of the interface circuits and model them in voltage or current, whichever is more convenient for analysis.

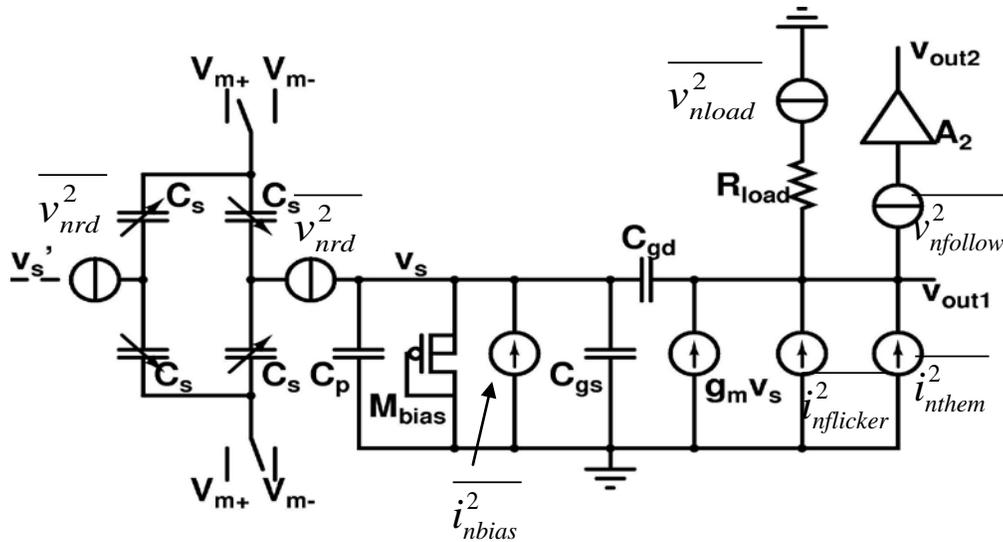


Figure 5-1. Universal model of the noise of front-end amplifier.

In Figure 5-1, $\overline{i_{n\text{flicker}}^2}$ and $\overline{i_{n\text{them}}^2}$ represent the flicker noise and the thermal noise from the input MOSFET. $\overline{i_{n\text{bias}}^2}$ is the shot noise of the pseudo-resistor for DC bias, $\overline{v_{nrd}^2}$ is the residue noise injected to the sense node from the reference voltage sources for the modulation signals and the corresponding switches, $\overline{v_{nload}^2}$ is the noise from the resistive load of the front-end amplifier, and $\overline{v_{nfollow}^2}$ in series with the next amplifier stage lumps the noise from the following stages. In a properly designed amplifier, $\overline{v_{nfollow}^2}$ and $\overline{v_{nload}^2}$ are both negligible since these noises are reduced by a factor of the gain of the first stage when referred to the input node. The MOS-bipolar device M_{bias} can work as either a subthreshold PMOS or a diode-connected *pn*p transistor, depending on the polarity of v_s . $\overline{i_{n\text{bias}}^2}$ is a shot noise, and it is negligible compared with other noise sources since the DC leakage current is small during operation. The residue noises from the voltage references and the corresponding switches for generating the modulation signals may

be injected into the sensing node. However, for full-bridge sensing capacitors, the residue noises are injected equally to v_s and v_s' , which are two input nodes of a fully differential amplifier, so that they are canceled by each other.

Wu *et al* reported a detailed noise analysis [52]. Generally, at low frequency, the flicker noise dominates, while the thermal noise takes it over in high frequency (usually above hundreds of kHz) and limits the noise floor eventually. In this design, the modulation frequency is chosen higher than the corner frequency, so only the thermal noise needs to be considered and it can be written as

$$\overline{v_n^2} = \frac{8kT}{3\sqrt{2\mu_{eff}C_{ox}(W/L)I_{ds}}} \Delta f \quad (5-2)$$

where k is the Boltzmann constant, T is the absolute temperature, μ_{eff} is the carrier mobility of the input transistors, C_{ox} is the gate capacitance density, W and L are the width and length of the input transistor, and I_{ds} is the drain-to-source current of the input transistor. It can be observed from (5-2) that a higher W/L ratio of the input transistors means lower noise level. The length can take the minimum value, but the width cannot be arbitrarily large because the acceleration signal v_s in (5-1) will be attenuated as the gate capacitance increases when the gate width increases. Therefore, there is an optimal width to obtain the maximum signal-to-noise ratio (SNR), which can be derived by letting

$$\frac{\partial}{\partial W} \left(\frac{\sqrt{\overline{v_n^2}}}{v_s} \right) = 0 \quad (5-3)$$

Plugging (5-2) into (5-3), we can obtain the optimal transistor width which satisfies the following equation:

$$C_{gs} + (1 + G_1)C_{gd} = \eta(2C_s + C_p) \quad (5-4)$$

where C_{gs} , C_{gd} , and C_p are the gate-to-source, gate-to-drain capacitance of the input transistors and the parasitic capacitance of the metal stray for interconnection, respectively, G_1 is the gain of the amplifier stage, and η is 1/3 for ideal long-channel transistors and needs fine tuning during simulation. More details about the derivation can be found in [52].

5.1.2 Trade-Offs between Noise and Power

The governing equation of a simple open-loop amplifier is given by

$$\begin{aligned} GBW &= G_{dc} \cdot f_{3dB} = g_m / C_{load} \\ &= \sqrt{2\mu_{eff} C_{ox} (W/L) I_{ds}} / C_{load} \end{aligned} \quad (5-5)$$

where GBW represents the product of the dc gain and the bandwidth of the amplifier, G_{dc} is the DC gain of the amplifier, f_{3dB} is its open-loop bandwidth, g_m is the transconductance of the input transistors, C_{load} is the load capacitance, and μ_{eff} , C_{ox} , W and L are the carrier mobility, the gate capacitance density, and the size of the input transistor, respectively. The DC bias current is then derived from (5-5),

$$I_{ds} = (G_{dc} \cdot f_{3dB} \cdot C_{load})^2 / 2\mu_{eff} C_{ox} (W/L) \quad (5-6)$$

This is the minimum bias current to meet the gain-bandwidth requirement. So the power consumption of an amplifier can be written as

$$\begin{aligned} P &= \alpha V_{dd} I_{ds} = \alpha V_{dd} (G_{dc} \cdot f_{3dB} \cdot C_{load})^2 / 2\mu_{eff} C_{ox} (W/L) \\ &= K G_{dc}^2 f_{3dB}^2 C_{load}^2 / (W/L) \\ &= K \cdot GBW^2 C_{load}^2 (W/L) \end{aligned} \quad (5-7)$$

where α is a constant representing the ratio of the total current to the current given in (5.7), which is the current in a single branch of the differential pair. Open-loop amplifiers and telescopic amplifiers, for instance, have $\alpha=2$, while folded-cascode

amplifiers have $\alpha > 2$, since the current drawn in the current mirrors need to be taken into consideration. Despite of the variation of α of different architectures, $2 \leq \alpha \leq 3$ is a good assumption in practical design, since the input differential pair usually consumes most of the power. V_{dd} represents the power supply, and G_{dc} is the DC gain of the amplifier. K is a constant defined to lump all constants appearing in (4.7). In real designs, the value of K depends on the architecture of the amplifier, and it will make the following analysis very tedious. For the sake of easier understanding, K is assumed identical for both open-loop and closed-loop amplifiers in the following analysis.

It has been mentioned in the previous section that the modulation frequency is above the corner frequency of the thermal and flicker noise, which is normally hundreds of kHz, to get rid of the flicker noise. So the operation frequency of the interface stage is much higher than the base band frequency of the acceleration signal. The single-stage amplifier working at a single high modulation frequency is shown in Figure 5-2(a), whose power is rewritten as

$$P_{1_stage} = KG^2 f_H^2 C_H^2 / (W_H / L_H) \quad (5-8)$$

The equation is rewritten directly from (5.7) with proper subscription. Typically, f_{3dB} is designed to be close to f_H . Thus the power consumption of the amplifier is directly proportional to the square of GBW .

Since the power of an amplifier is proportional to the quadratic value of its gain, it is beneficial to split a high overall gain to two stages, as shown in Figure 5-2(b).

Assuming the gains of the two stages are G_1 and G_2 , respectively, the power of this single-chopper dual-stage architecture is given by

$$P_{2_stage} = K[(G_1^2 + G_2^2) f_H^2 C_H^2 / (W_H / L_H)] \quad (5-9)$$

where the two stages are assumed to have the same load and transistor size.

Comparing the power consumption of these two architectures by considering the same overall gain, i.e., $G_1 \cdot G_2 = G^2$, we have

$$\frac{P_{2_stage}}{P_{1_stage}} = \frac{G_1^2 + G_2^2}{G^2} \geq \frac{2}{G} \quad (5-10)$$

The two-stage amplifier achieves its minimum power consumption when the overall gain is equally split into the two stages, i.e., $G_1 = G_2 = \sqrt{G}$, and the power in this case is reduced by a factor of $G/2$ compared to the single-stage architecture. The required overall gain of MEMS accelerometers is usually larger than 100, so the two-stage architecture has significant advantage in terms of power over the single-stage amplifier for interfacing with MEMS accelerometers.

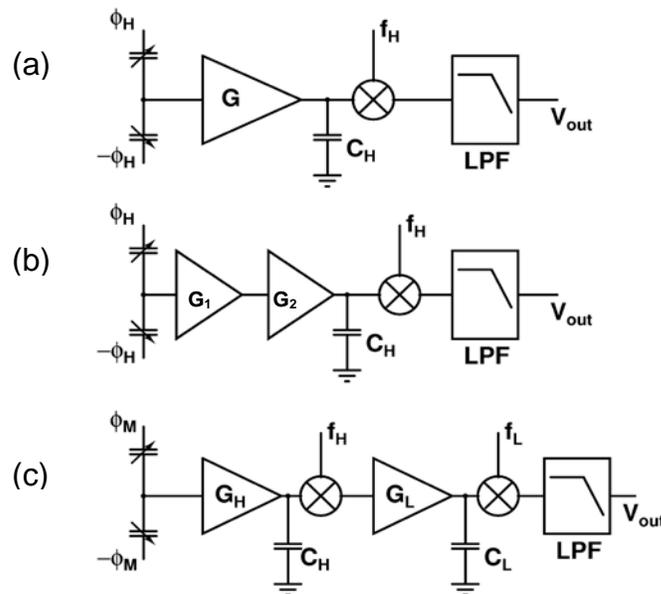


Figure 5-2. Comparisons of different architectures: (a) single-chopper single-stage, (b) single-chopper dual-stage and (c) dual-chopper dual-stage amplifiers.

The amplifier working at high frequency has low noise floor due to the flicker noise reduction. In a well-designed two-stage amplifier, the noise from the first stage

dominates. Thus, it may be unnecessary to have the second stage still working at the same high frequency. That is the basic idea of the dual-chopper amplifier (DCA), in which the overall gain is split into two stages and, at the same time, the two stages operate at different modulation frequencies, i.e., two chopping clocks [88]. As shown in Figure 5-2(c), the first stage operates at the high chopping frequency and a moderate gain while the second stage operates at the low chopping frequency with a larger gain. Thus the power of the DCA is written as:

$$P_{DCA} = K \left[G_H^2 f_H^2 C_H^2 / (W_H / L_H) + G_L^2 f_L^2 C_L^2 / (W_L / L_L) \right] \quad (5-11)$$

where G_H and G_L are the gains of the two stages, W_L and L_L are the width and the length of the input transistors of the second stage, and C_L is the load capacitance of the second stage. In this DCA design, the high modulation frequency f_H is chosen at 1MHz, higher than the noise corner frequency to minimize the flicker noise. Further increase on the modulation frequency may not have significant merit of noise reduction, but it has the cost of more power consumption. The low modulation frequency f_L is much lower than f_H to avoid aliasing. In this DCA design, f_L is chosen to be 20kHz.

According to (5-2), (5-5) and (5-9), high G_H means high gain bandwidth of the first stage, and thus leads to low input noise, but the cost is significantly high power consumption. So there is a trade-off between the noise and power. The criterion of optimization is to obtain the minimum value of the product of the total power and total input-referred noise by choosing a proper G_H . It can be derived as

$$\frac{\partial}{\partial G_H} (\overline{v_n^2} P) = 0 \quad (5-12)$$

By substituting (5-2), (5-5) and (5.11) into (5-12), the optimized gain of the first stage for the 2-stage dual-chopper architecture is

$$G_{H_opt} = \sqrt{\frac{3f_L C_L (W_H / L_H)^{1/2}}{f_H C_H (W_L / L_L)^{1/2}}} \cdot \sqrt{G} \quad (5-13)$$

where G is the overall gain. This result is based on the assumption that the noise from the second stage is comparable to that from the first stage when referred to the input node, which is usually the case. The power of the DCA after optimization of the high frequency gain is then

$$\begin{aligned} P_{DCA_optimal} &= (10/3)K[Gf_H f_L C_H C_L / (W_H / L_H)] \\ &= (5/3)(f_L / f_H)P_{2-stage} \\ &= (10/3G)(f_L / f_H)P_{1-stage} \end{aligned} \quad (5-14)$$

So the power consumption of the DCA is further reduced by a factor of $(3f_H/5f_L)$, compared with the two-stage architecture working at a single high frequency. It is a significant reduction considering $f_H \gg f_L$.

For the CMOS-MEMS accelerometer reported in this paper, based on (5-13), after taking some practical factors into consideration and setting $G=200$, $f_H=1\text{MHz}$, $f_L=20\text{kHz}$, $C_L=4C_H$, and $(W_H/L_H)/(W_L/L_L)=5$, the optimized high-frequency gain, G_H , is about 10.

5.1.3 System Design

The architecture and the operational principle of the dual-chopper amplifier (DCA) are shown in Figure 5-3. The sensed signal is amplified by two amplification stages and chopped by two fundamental clocks Φ_H and Φ_L to demodulate the signal back to the base band. The clock frequencies are f_H and f_L , respectively, and $f_H \gg f_L$. A similar nest-chopper architecture has been reported in [108] to reduce noise and DC offset. The modulation signals applied on the sensing capacitors are generated by chopping two DC references, and the switching signal Φ_M comes from XOR operation of two clocks, Φ_H and Φ_L , as shown in Figure 5-3(b). The employed CMOS-MEMS processing gives

the possibility to make two electrically-isolated pairs of sensing capacitors for the fully differential amplifier, so that the noise from the modulation signal injects into the two input node equally and cancel each other. There are no switches between the sensing capacitors and the input transistors of the front-end amplifier. This arrangement makes the kT/C noise from switches and the residual spikes during switching, which is an important noise source as mentioned in [108], to the common mode, so they do not play a significant role in this fully differential amplifier.

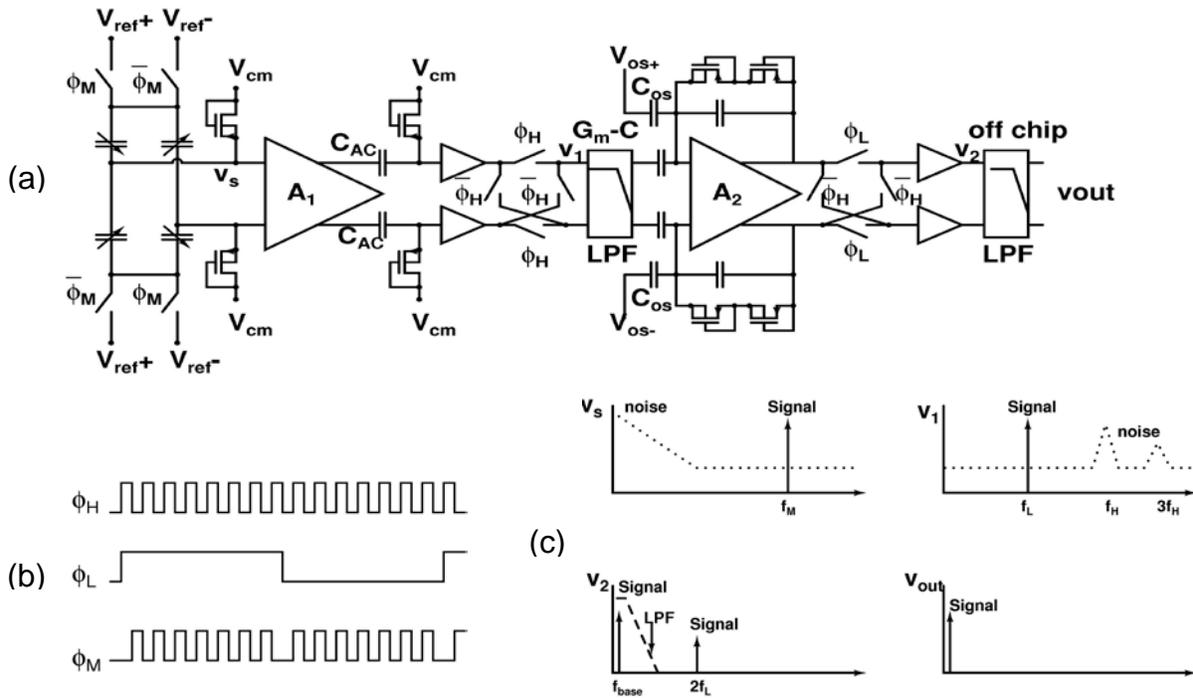


Figure 5-3. The architecture and operation of the DCA system. (a) System architecture. (b) Clock signals in DCA. (c) Operation in frequency domain.

The first stage A_1 is an open-loop amplifier with a gain of about 10. The open-loop architecture is believed to have better noise performance because it suffers less from noise folding compared with transimpedance amplifiers and capacitive feedback amplifiers. Following A_1 are an AC coupling circuitry and buffers that remove the DC

offset from A_1 . The capacitor C_{ac} and the MOS-bipolar device work as a high-pass filter whose cutoff frequency is set at 2 kHz. The value of C_{ac} is 4pF, which is realized with an on-chip poly-insulator-poly capacitor. Then the signal is demodulated by f_H for the first time to move the signal to the f_L band. Followed is a G_m -C low-pass filter with a cut-off frequency of 200 kHz, which filters the high-frequency harmonics and high frequency noises to reduce the noise folding in the next demodulation. Then the signal is amplified by the second amplification stage A_2 , which is a capacitive-feedback amplifier based on an OTA.

Two MOS-bipolar pseudo-resistors, similar to the ones discussed in 5.1.1, are in series to provide high feedback impedance. Compared with the open-loop amplifier A_1 , this closed-loop amplifier A_2 can provide a larger signal swing with good linearity and increase the dynamic range of the system. Since the operating frequency of A_2 is low, a relatively high gain can be allowed in A_2 without adding too much power consumption. The offset tuning signals, V_{os+} and V_{os-} , have the same frequency as Φ_L , and they are used to remove the offset due to the sensing capacitance mismatch. The signal amplified by A_2 is then demodulated by Φ_L , and the buffered output is fed into an off-chip low-pass filter to obtain the baseband signal.

Figure 5-3(c) shows the operation in frequency domain. The acceleration signal is modulated to the high modulation frequency, f_H , so the signal is moved away from the large flicker noise frequency range. Flicker noise dominates in the signal's baseband. After the high frequency chopping, the flicker noise is moved to odd harmonics of f_H , and then filtered by the G_m -C filter. The signal after A_2 is chopped with Φ_L to demodulate the signal back to the baseband. Of course there is some power loss at

higher harmonics of f_L during this procedure. Finally the off-chip low-pass filter removes all out-of-band signals and obtains the acceleration signal at the base band.

5.1.4 Temperature Dependence Reduction

Another important consideration is the dependence of the performance on temperature variation. The output signal is written as

$$v_o = G_H G_L v_s = \frac{\Delta C_s}{2C_s + C_p} \cdot V_m \cdot G_H \cdot G_L \quad (5-15)$$

So the temperature coefficient can be expressed as

$$\alpha = \frac{\partial v_o}{v_o \partial T} = \frac{1}{V_m} \frac{\partial V_m}{\partial T} + \frac{1}{G_H} \frac{\partial G_H}{\partial T} + \frac{1}{G_L} \frac{\partial G_L}{\partial T} \quad (5-16)$$

There are mainly three sources of the temperature dependence: the amplitude variation of the modulation signal applied to the sensing capacitors and the gain variations of the two amplification stages. The modulation signal is generated by chopping two DC reference voltages, so ideally the reference should be temperature insensitive. It is not a problem if the DC reference comes from a regulated power supply, but in that case the output signal will be sensitive to the fluctuation of the power line. In this design, a band-gap voltage reference is applied to generate the temperature independent reference voltage. The second stage is based on capacitive feedback, so the effect of temperature is negligible.

Since the first stage of the DCA is an open-loop amplifier without feedback to clamp the gain, A_1 is the major source of the temperature dependence. The first version of the DCA reported in [88] is affected much by temperature variation. The solution of the problem will be discussed in 5.1.5.

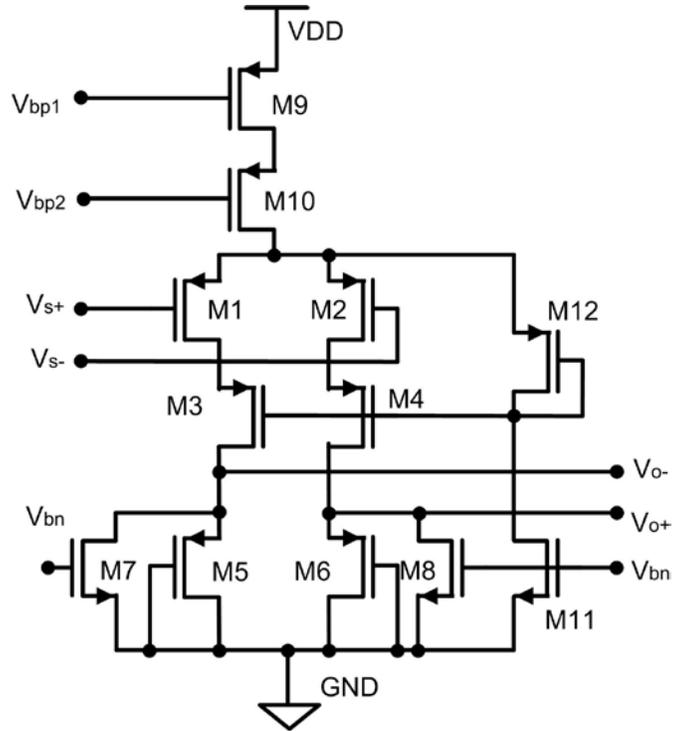


Figure 5-4. The schematic of A_1 with PMOS load.

5.1.5 Circuits Implementation

The schematic of the first stage A_1 is shown in Figure 5-4. M_3 and M_4 are cascaded with the input transistors to have good linearity. M_7 and M_8 draw the DC current from the load branch to increase the impedance of the diode-connected load transistors to ensure a proper gain. In the early version, the load resistors are realized with two diode-connected NMOS transistors, and the gain of this stage is

$$G_H = g_{m1} / g_{m5} = \sqrt{2I_1\beta_1} / \sqrt{2I_5\beta_5} = \sqrt{\mu_1 / \mu_5} \cdot K \quad (5-17)$$

where g_{m1} and g_{m5} are the transconductances of M_1 and M_5 , I_1 and I_5 are their static currents, μ_1 and μ_5 are their carrier mobilities, $\beta = \mu_{\text{eff}} C_{\text{ox}} (W/L)$, and K is a constant related to transistor sizes. If M_1 , M_2 and M_5 , M_6 are of different types, their carrier

mobility mismatch will lead to a significant temperature dependence of G_H , which is the case of the first version of the DCA design [88].

In this DCA design, M_5 and M_6 have been changed from NMOS to PMOS, as shown in Figure 5-4. In this case the input and load transistors are of the same type, so the temperature dependences of the input and load transistors will cancel each other, making G_H in (5-17) less sensitive to temperature variation.

The second amplifier stage is a closed-loop capacitive-feedback amplifier based on an operational transconductance amplifier (OTA), whose schematic is plotted in Figure 5-5. It is implemented with a fully differential folded-cascode architecture which has two transistors M_7 and M_8 working in the triode region to control the common-mode voltage level of the output signal. The input differential pair uses long-channel large-width PMOS transistors to reduce the flicker-noise corner frequency to around 20 kHz. The open-loop gain is designed to be 80 dB with the unity-gain frequency at 20 MHz in order to maintain a good virtual ground at the input node.

The low-pass G_m -C filter is schematically shown in Figure 5-6. Source degeneration is applied to the input transistors for better linearity. Two diode-connected transistors with very long channel length work as the load resistors to provide properly high resistance to achieve a cut-off frequency of 200 kHz. That cut-off frequency is low enough to attenuate the high frequency noise after the first modulation and to keep the phase lagging introduced by this stage acceptable. The capacitor required in this application is 6 pF, which can be realized by on-chip poly capacitors.

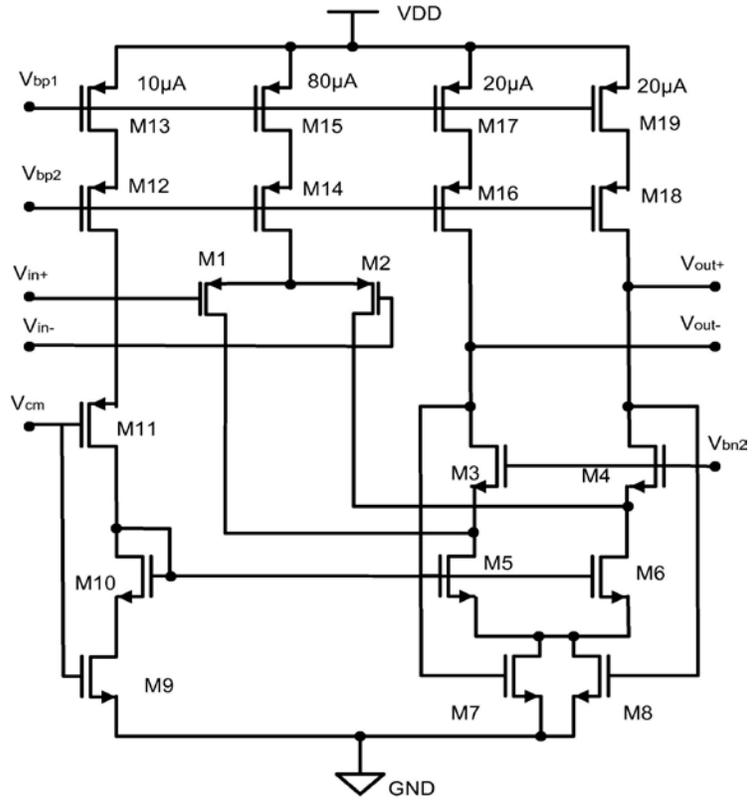


Figure 5-5. Schematic of the OTA of the second amplification stage.

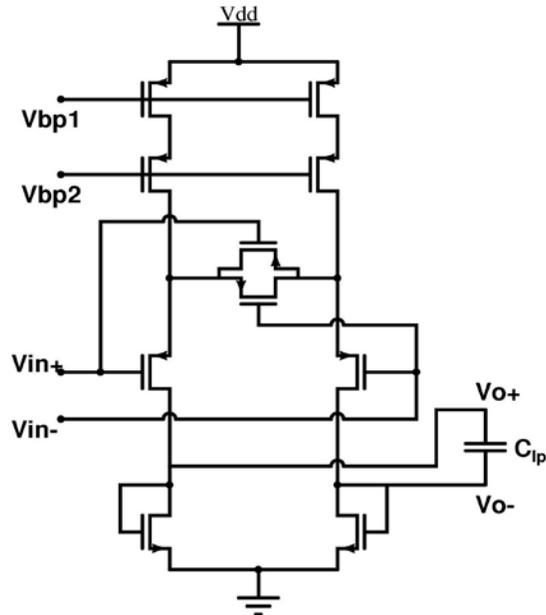


Figure 5-6. Schematic of the low-pass G_m-C filter.

5.2 Experimental Results

There are two batches of accelerometer designs included in this work. The earlier version has separate proof mass for the lateral-axis and z-axis detection for reducing the cross-axis couplings. The lateral-axis direction is based on the in-plane movements of the proof mass that change the gaps of the sensing capacitors, while the vertical-axis detection is realized by the torsion of an imbalanced proof mass, as discussed in [109, 110]. The SEM photos of the whole chip and the details of the comb fingers with isolation regions have been shown in Figure 3-2, and the details of the device parameters have been listed in Table 3-1.

The interface circuitry has been fabricated together with a CMOS-MEMS 3-axis accelerometer using TSMC 0.35 μm 2P4M technology, followed by a post-CMOS micromachining processing. The circuitry is not visible in Figure 3-2, because it is covered by a whole piece of Metal3 layer to avoid any circuit detriment during the micromachining processing.

The acceleration measurements are made on a LDS V-408 shaker that can generate a single-tone sinusoidal acceleration. A SR 560 low-noise amplifier with high input impedance and tunable filter is used to pick up the output signal, minimize the loading effect of other testing equipment and provide a proper low-pass filtering. The cutoff frequency is 10 kHz. A PCB Piezotronics 356A16 reference accelerometer, whose sensitivity is 100mV/g, is mounted on the shaker to monitor the acceleration. The experiment setups are shown in Figure 5-7.

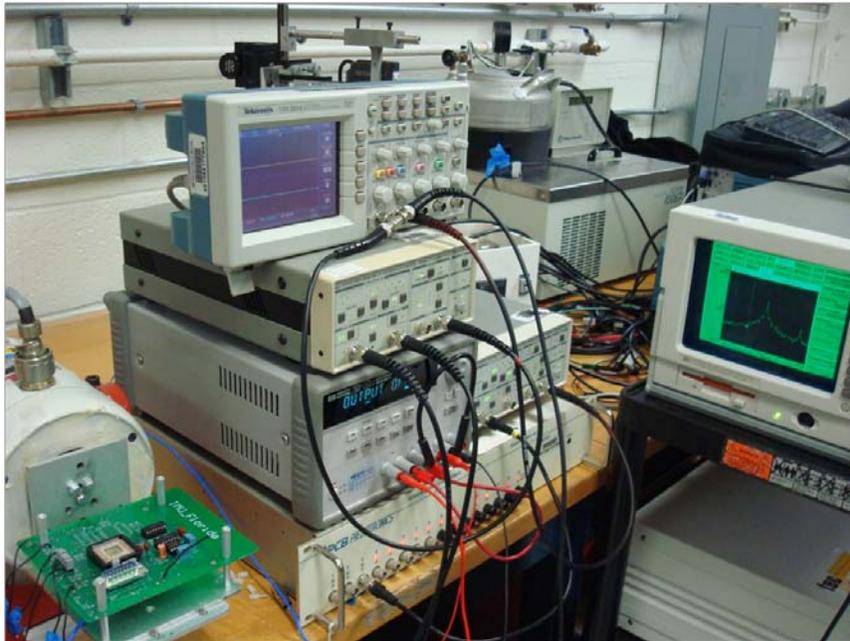


Figure 5-7. Experiment setups for the accelerometer testing.

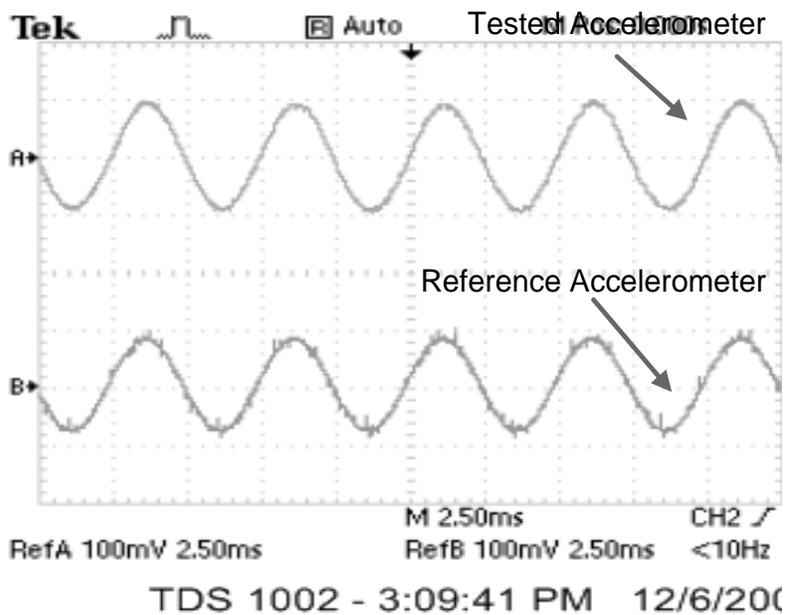


Figure 5-8. The waveforms of the tested accelerometer and the reference to a 200 Hz 0.4g oscillation.

Figure 5-8 shows the output signal of the tested accelerometer in response to a 200 Hz 0.4g oscillation in the lateral direction, compared to the signal from the reference

accelerometer. It indicates that the MEMS device and the interface circuitry both function correctly to track the acceleration signals.

Figure 5-9 plots the dynamic responses of the three axes to 100Hz sinusoidal accelerations. The measured sensitivity of X, Y and Z axis are 144mV/g, 139mV/g, and 23.3mV/g, respectively, as shown in Figure 5-9. The linear ranges of the lateral axes are both ± 11.5 g, and that of the z axis is as high as ± 29 g due to its smaller sensitivity.

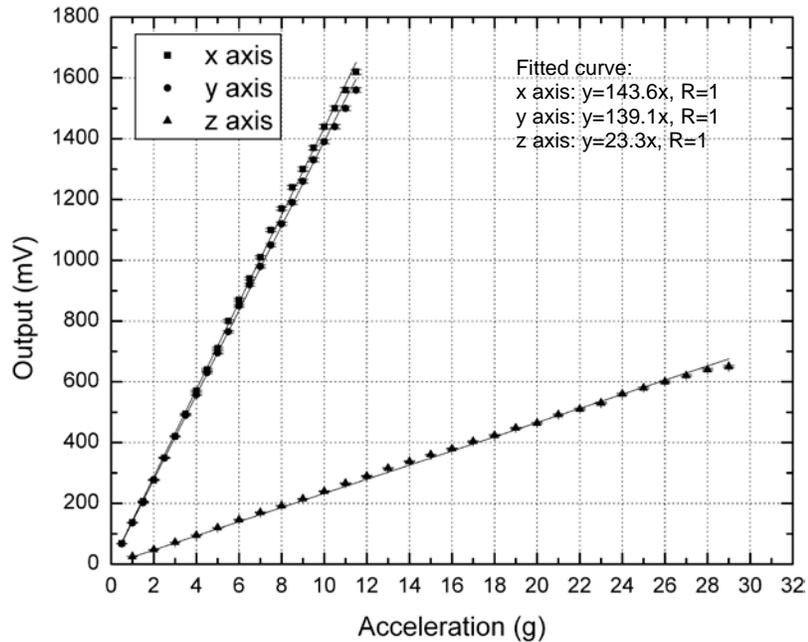


Figure 5-9. Dynamic response of the three-axis accelerometer to 100Hz acceleration.

The spectra of the output signal of the the x-axis and z-axis in response to a 100Hz-acceleration are shown in Figure 5-10. The spectrum of the y-axis is not shown because it looks the same as that of x-axis. The noise floors of X, Y and Z axis are $40 \mu\text{g}/\sqrt{\text{Hz}}$, $40 \mu\text{g}/\sqrt{\text{Hz}}$, and $130 \mu\text{g}/\sqrt{\text{Hz}}$, respectively.

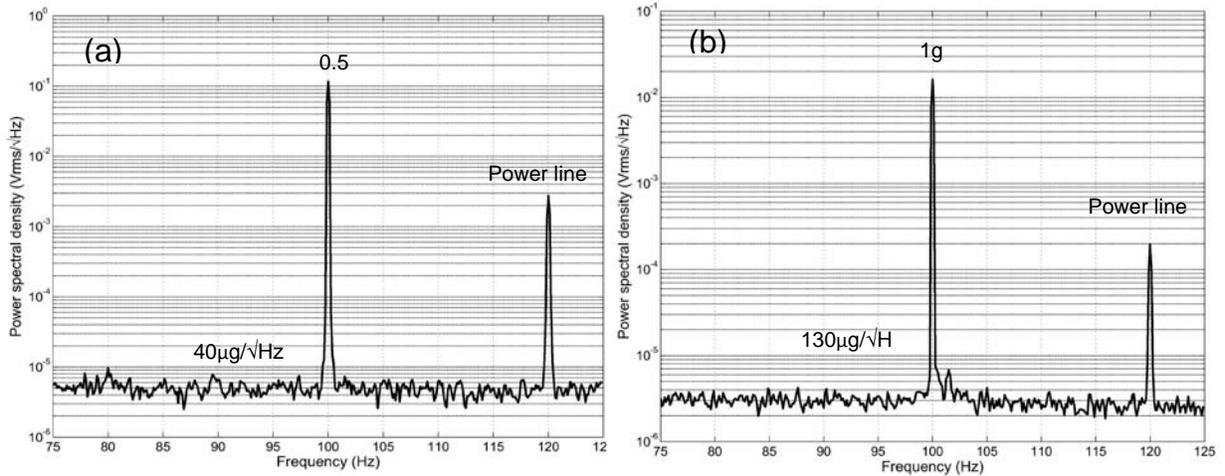


Figure 5-10. Spectra of the accelerometer in response to a 100-Hz acceleration: (a) x axis; and (b) z axis.

The cross talks between the three axes are measured by monitoring the outputs of other two axes when the device is excited in a certain axis. The results are shown in .

The Z-axis accelerometer is based on imbalanced torsional force in y axis, so it is sensitive to the acceleration in y axis especially when the spring constant is lower than the designed value due to processing imperfections. It can be further reduced by better process control. The characteristics of the 3-axis accelerometer are summarized in Table 5-2.

The latest version of the three-axis accelerometer is part of the five-axis IMU. The sensor design is improved by using vertical springs and symmetrical proof mass, instead of torsional beams and imbalanced proof mass, to achieve better sensitivity and linearity. The proof mass of the z-axis accelerometer is shared with the x/y-axis devices to save area. The SEM photos of this three-axis accelerometer have been shown in Figure 3-4.

Table 5-1. Cross-axis couplings of the three-axis accelerometer.

		Affected directions		
		X	Y	Z
Moving	X		1.7%	2.5%
directions	Y	0.5%		4.7%
	Z	1.8%	2.3%	

Table 5-2. Performance summary of the three-axis accelerometer.

Axis	X	Y	Z
Sensitivity	144 <i>mV/g</i>	139 <i>mV/g</i>	23.3 <i>mV/g</i>
Noise floor	40 $\mu\text{g}/\sqrt{\text{Hz}}$	40 $\mu\text{g}/\sqrt{\text{Hz}}$	130 $\mu\text{g}/\sqrt{\text{Hz}}$
Linear range	$\pm 11.5 \text{ g}$	$\pm 11.5 \text{ g}$	$\pm 29 \text{ g}$
Modulation frequency	1 <i>MHz</i>	1 <i>MHz</i>	1 <i>MHz</i>
Power (3.3 V)	1 <i>mW</i>	1 <i>mW</i>	1 <i>mW</i>

The experimental results of the dynamic testing of the new three-axis accelerometer are plotted in Figure 5-11. The accelerometer achieves the sensitivities of 191 *mV/g* for the x/y-axis and 129 *mV/g* for the z-axis, respectively, with the dynamic range of $\pm 5\text{g}$ for all axes. The sensitivity of the z-axis accelerometer is increased by almost 4 times and is comparable with the lateral axes, while the gain from circuitry keeps the same. It helps to make the sensitivities of all three axes well balanced with no need of power consumption for providing extra gain.

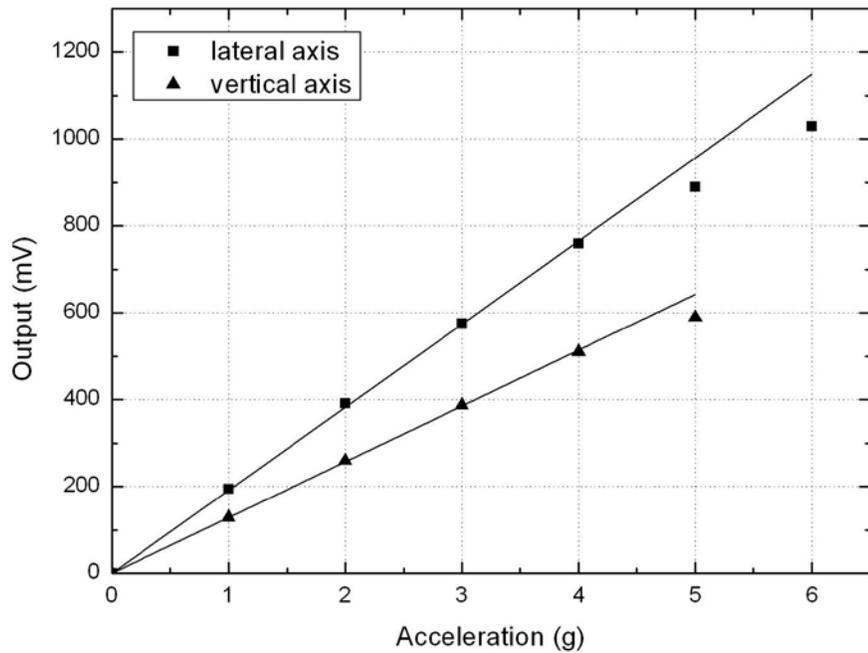


Figure 5-11. Dynamic response of the three-axis accelerometer with improved z-axis design.

Table 5-3. Performance summary of the accelerometer of the latest version.

Axis	X/Y	Z
Sensitivity	191 mV/g	129 mV/g
Noise	50 $\mu\text{g}/\sqrt{\text{Hz}}$	80 $\mu\text{g}/\sqrt{\text{Hz}}$
Linear range (5% THD)	± 5 g	± 5 g
Modulation frequency	1 MHz	1 MHz
Resonant frequency	1.2 kHz	750 Hz
Cross-axis coupling	1.6% (from z)	1.4% (from X/Y)
Power consumption	1 mW	1 mW

The performance of the accelerometer is summarized in Table 4-3. Due the symmetrical proof mass for z axis, the cross axis coupling from the lateral axis to the vertical axis has been reduced from 4.7% of the previous version to 1.4%. The accelerometer achieves the noise floors of $50 \mu\text{g}/\sqrt{\text{Hz}}$ for the x/y-axis and $80 \mu\text{g}/\sqrt{\text{Hz}}$ for the z-axis, respectively, and the noise consumption is $1 \text{ mW}/\text{axis}$. So low noise and low power is achieved simultaneously.

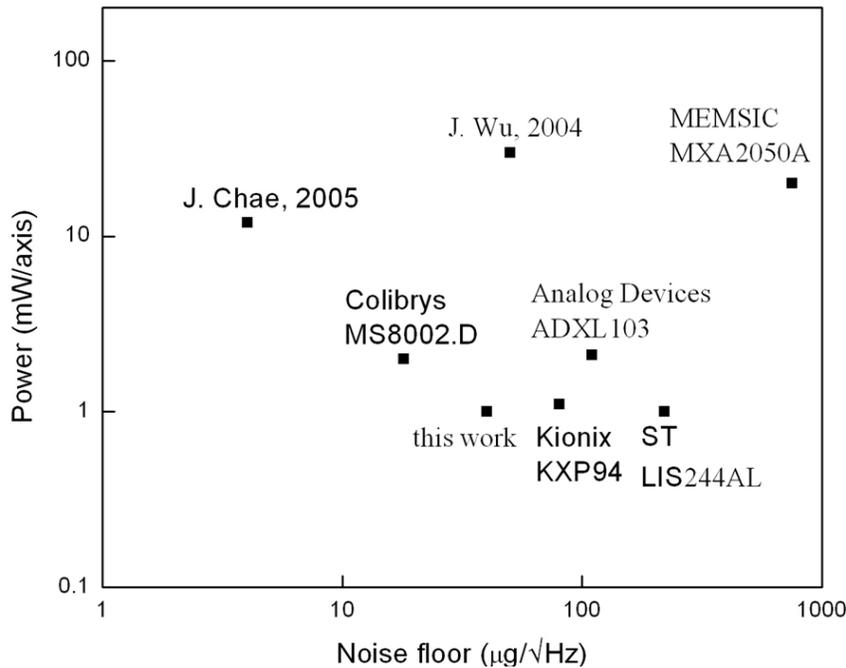


Figure 5-12. Comparisons of this work to other works in terms of noise and power.

5.3 Discussions

Figure 5-12 compares the noise and power consumption of this work with the previous work from other groups [52, 60] and some commercially available accelerometers [6-8, 111, 112]. Chae *et al* reported a $4 \mu\text{g}/\sqrt{\text{Hz}}$ resolution, but the device size is $7 \times 9 \text{ mm}^2$ and the power consumption is over 12 mW per axis. Colibrys achieves $18 \mu\text{g}/\sqrt{\text{Hz}}$ at 2 mW, but the package size is $14.2 \times 14.2 \text{ mm}^2$. The $45 \mu\text{g}/\sqrt{\text{Hz}}$

resolution at only a 1mW power consumption and a $3\times 3\text{mm}^2$ die size (CMOS circuitry included) makes this work a very good balance between the noise, power and size.

CHAPTER 6 ELECTRONICS DESIGN FOR CMOS-MEMS GYROSCOPES

This chapter will discuss the system-level design for CMOS-MEMS gyroscopes. The operation of a gyroscope system includes both the primary mode, which is also called drive mode, and the secondary mode, which is also called sense mode. A novel differential difference front-end amplifier for the sense mode with high gain and low temperature dependence is discussed first. Then the system-level design for both modes is shown, followed by the transistor-level implementation and the experimental results.

6.1 Front-End Differential Difference Amplifier

6.1.1 Design Trade-Offs

The Coriolis acceleration is much smaller than the linear acceleration detected by accelerometers. Assuming a gyroscope with the primary-mode resonant frequency of 5 kHz and the oscillation amplitude of 2 μm , which are both of typical value, then the peak velocity of the proof mass in the primary mode is 6.28×10^{-2} m/s, according to the equation:

$$v = dx / dt$$

Thus the peak Coriolis acceleration corresponding to a 1°/s rotation is approximately 100 μg . Due to the limit of processing, both the sensing capacitance and the mechanical sensitivity of CMOS-MEMS gyroscopes are relatively low compared to the hybrid solutions, which makes the signal detection even more challenging. So the architecture of the front end is very important for the sensor's performance. The front-end circuitry for the drive-mode displacement has much looser requirement on the noise performance than that for the Coriolis signal, because the displacement in the primary

mode is 2 to 3 orders larger than that induced by Coriolis acceleration. So in this section, the discussion will focus on the front-end amplifier for the Coriolis signal detection.

The interface between a capacitive sensor and various front-end architectures is described with a universal model, as shown in Figure 6-1. The front end A_1 has the gain of G_1 , and the following stages are represented by A_2 . The Coriolis signal is modeled as a voltage source v_s , which satisfies

$$v_s = (\Delta C_s / C_{s0}) \cdot V_p \quad (6-1)$$

where V_p is the reference voltage, and C_{s0} and ΔC_s are the sensing capacitance and its change due to Coriolis acceleration, respectively.

The input-referred noise from the front end is $\overline{v_{n1}}$, and the noise from the following stages is lumped as $\overline{v_{n2}}$. The signal-to-noise ratio (SNR) is then written as:

$$SNR = \frac{v_s^2}{v_{n1}^2 + v_{n2}^2 / G_1^2} \quad (6-2)$$

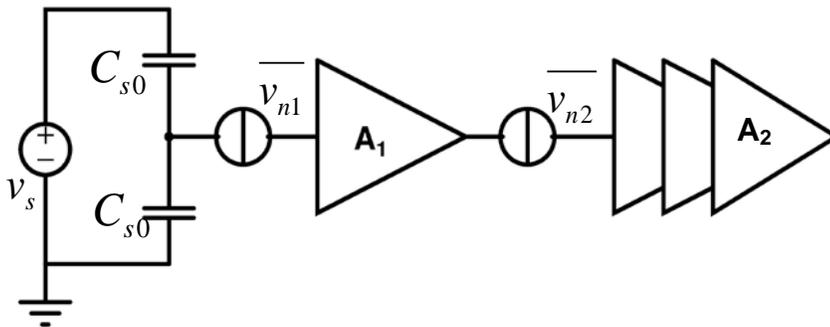


Figure 6-1. The model of the front-end amplifiers with lumped following stages.

According to (6-2), the gain of the front end must be high enough, or the signal-to-noise ratio (SNR) will be degraded significantly as the signal passes the following

stages. It is not a serious issue for the two-chip solutions, because the sensing capacitance of the sensors is relatively large in those cases. For CMOS-MEMS inertial sensors, however, it becomes challenging because the sensing capacitance is small and any circuit that has its gain dependent on the sensing capacitance will have the gain much lower than the two-chip solutions. The currently available architectures are analyzed in the following paragraphs.

The commonly used front-end architectures and their gain are shown in Figure 6-2. The open-loop amplifiers and TIAs are able to achieve high gain. However, since their gains are determined by the resistive load or the feedback resistors, which are temperature-sensitive, they suffer from large temperature dependence. In the open-loop architecture, the gain-to-drain capacitance of the input transistors contributes more to the parasitic capacitance as the gain is increased, because of the miller effect, so the signal is attenuated. The miller effect can be reduced by adding cascode transistors to the load, as shown in Figure 5-4, with the cost of limited signal swing. Another drawback of the open-loop amplifier is the low power-supply reject ratio (PSRR). Even though the fully differential configuration is theoretically immune to the noise from power supply, the power supply affects the output if there is any mismatch in the circuits. The transfer function of the TIA requires high resistance and very low capacitance as the feedback impedance, which are both hard to implement. The high resistance can be realized with long transistors, but the costs are smaller linear range and more complicated circuits.

Switched-capacitor (SC) amplifiers and CSAs provide low-impedance interface to the sensor, and they are insensitive to parasitic capacitance. They are also much less sensitive to temperature variation as well. However, the gains of both SC amplifiers and

CSAs are set by the ratio of the sensing capacitance over the feedback capacitance. The sensing capacitance of CMOS-MEMS gyroscopes is small, typically in the order of 100 fF, which is comparable or even smaller than the available on-chip capacitance, so their gains are small. Therefore, more following amplification stages are needed to achieve the required gain, which may increase the circuit complexity and/or power consumption. In addition, the discrete-time SC circuits are immune to the leakage current from the sensor, but they suffer from noise folding during sampling, which degrades the signal-to-noise ratio (SNR). Moreover, there exists another issue. The impedance of the resistive feedback in the CSA is required to be much larger than that of the capacitive feedback, which is in the order of $10^{10} \Omega$ for dc detection, in order to meet the transfer function characteristics and to reduce its noise contribution. The large resistance can be implemented with a transistor working in linear region [16, 18], but it requires extra bias circuits and fine tuning, and the signal swing is relatively small. Switching techniques can provide large equivalent resistance [16], but significant kT/C noise will be added into the front-end amplifier. The requirement can be mitigated by increasing the feedback capacitance or using ac detection, but increasing the feedback capacitance will reduce the gain and the SNR. Using ac detection can lower the electronic noise and mitigate the stringent requirement on the passive components, but the added modulation/demodulation complicates the circuits, and the power consumption is increased much due to the increased gain-bandwidth product. Furthermore, unlike the dc detection, any static mismatch of the sensing capacitance will be detected by the ac detection, whose amplitude may be significant compared with the capacitance change caused by the Coriolis force.

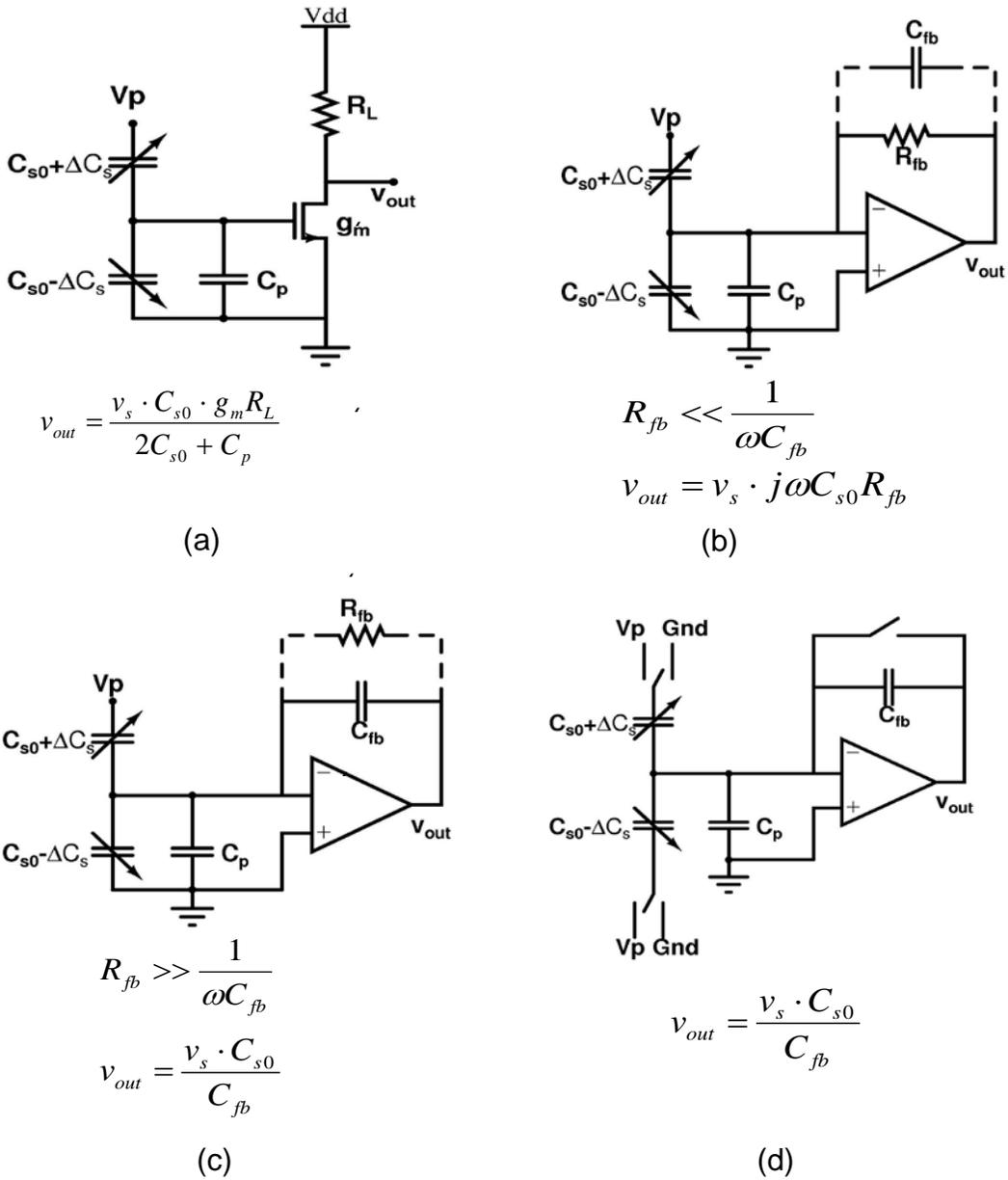


Figure 6-2. Comparisons of the available architectures: (a) open-loop amplifier; (b) TIA; (c) CSA; and (d) SC circuits. v_s is given in (6-1).

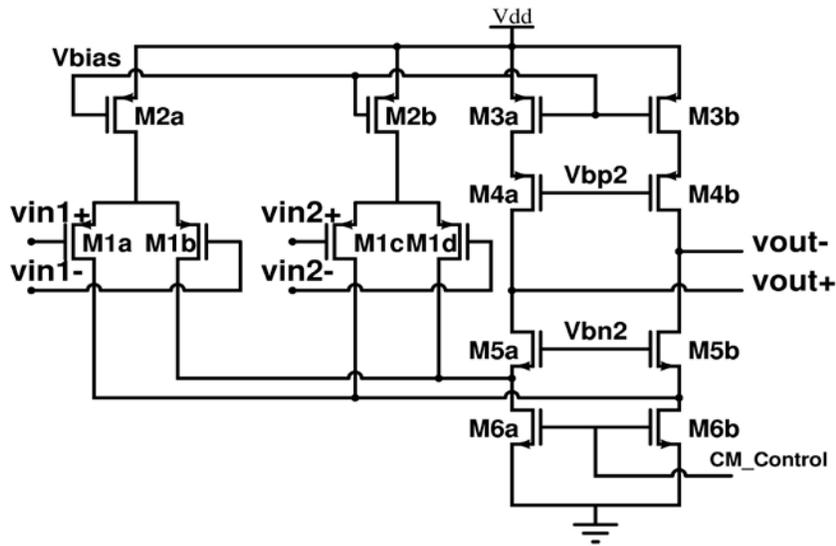
6.1.2 Differential Difference Amplifier

In order to accommodate CMOS-MEMS gyroscopes working at atmosphere, a differential difference amplifier (DDA) is designed and is analyzed in the following sections, which allows continuous-time dc detection so that the immunity to capacitance

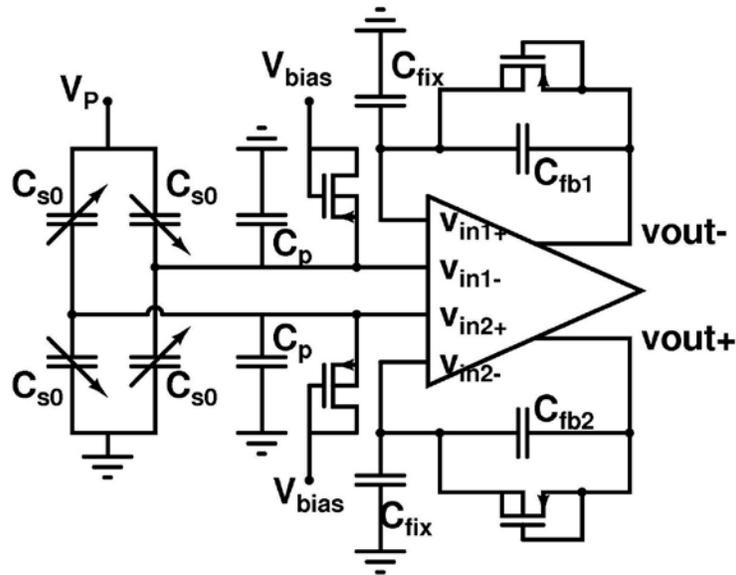
mismatch and low power consumption can be achieved without sacrificing noise performance.

Differential difference amplifiers (DDAs) have two pairs of differential inputs and one pair of differential outputs, and they are commonly used in instrumentation amplifiers, voltage-controlled current sources, comparators, *etc.* [22]. A DDA is schemed in Figure 6-3(a), and its connection to the sensing capacitances of the gyroscope is shown in Figure 6-3(b). The input nodes are biased with a MOS-bipolar pseudo resistor [23], which is implemented with a PMOS transistor with its gate and drain connected to the DC bias voltage and its bulk and source connected to the sensing nodes and the input nodes of the pre-amplifier. An AC impedance up to $10^{11} \Omega$ can be realized with this pseudo resistor, which is at least 10 times higher than the impedance of the capacitances of the sensing capacitor and the input transistors to avoid significant signal attenuation. The time constant of the input RC network is controlled within 0.1s. With the input signal applied between one pair of inputs and with feedback applied differentially between the other pair of inputs, the DDA is the fully differential equivalent of a single-ended non-inverting amplifier. Because of the high-impedance input, C_{s0} is no longer important to the front-end gain, but the gain can be set by a capacitive ratio. PMOS transistors are used as the input pairs for their lower flicker noise than NMOS. Transistors M_{1a} , M_{1b} , M_{1c} , and M_{1d} compose two differential input pairs, corresponding to v_{in1+} , v_{in1-} , v_{in2+} , and v_{in2-} , respectively. The drains of M_{1a} and M_{1c} , and M_{1b} and M_{1d} are respectively shorted and fed to the low impedance nodes of the cascaded NMOS pairs M_{5a} and M_{5b} . The DDA satisfies the following equation:

$$v_{out+} - v_{out-} = (g_{m1}v_{in1+} + g_{m2}v_{in2+} - g_{m3}v_{in1-} - g_{m4}v_{in2-}) \cdot R_{out} \quad (6-3)$$



(a)



(b)

Figure 6-3. The schematic of the DDA and its interface to the sensing capacitors. (a) Schematic of the DDA; and (b) the interface with the sensing capacitors.

where $g_{m1,2,3}$ represent the transconductance of the four input transistors and R_{out} represents the output impedance of the amplifier. In this design all the input transistors are of the same size, so (6-3) can be reduced to

$$v_{out+} - v_{out-} = (v_{in1+} + v_{in2+} - v_{in1-} - v_{in2-}) \cdot g_m R_{out} \quad (6-4)$$

A capacitive negative feedback loop is formed once v_{in1+} and v_{out-} are connected through a feedback capacitor C_{fb1} , and v_{in2-} , v_{out+} , and C_{fb2} form another capacitive negative feedback loop. A MOS-bipolar pseudo resistor is in parallel with each C_{fb} to provide the DC path with large AC impedance. C_{fix} is connected to the feedback capacitance and the analog ground to define the gain of the DDA. Due to the high loop gain of the negative feedback loop, there exists the following equations:

$$v_{in1+} - v_{in2-} = v_{in1-} - v_{in2+} \quad (6-5)$$

The output of the DDA is then determined by the non-inverting feedback, as shown in (6-6).

$$v_{out-} = (1 + C_{fix} / C_{fb}) v_{in1+} \quad (6-6)$$

Combining (6-5) and (6-6) leads to

$$v_{out+} - v_{out-} = (1 + C_{fix} / C_{fb}) \cdot (v_{in2+} - v_{in1-}) \quad (6-7)$$

The two inner input nodes, v_{in1-} and v_{in2+} , are connected to the Coriolis sensing capacitances, and another two MOS-bipolar pseudo resistors are used to provide the proper DC bias at the sensing input nodes. Considering the parasitic capacitance C_p due to the gate-to-source capacitance of the input transistors and the stray capacitance from the interconnections, the differential input signal can be written as:

$$v_{in1-} - v_{in2+} = \frac{2\Delta C_s}{2C_{s0} + C_p} \cdot V_P \quad (6-8)$$

where C_{s0} is the Coriolis sensing capacitance, C_p is the parasitic capacitance from the interconnection and the input transistors, ΔC_s is the change of C_s due to the Coriolis

acceleration, and V_P is the polar voltage applied on C_s . By substituting (6-5) and (6-8) into (6-6), the output of the DDA can thus be derived as

$$\begin{aligned} v_{out+} - v_{out-} &= \frac{2\Delta C_s \cdot (C_{fix} + C_{fb})}{(2C_{s0} + C_p) \cdot C_{fb}} \cdot V_P \\ &= \frac{2v_s C_{s0} (C_{fix} + C_{fb})}{(2C_{s0} + C_p) \cdot C_{fb}} \end{aligned} \quad (6-9)$$

Compared with the TCA whose output is $\Delta C_s V_p / C_{fb}$, the gain is boosted by a factor of $2(C_{fix} + C_{fb}) / (2C_{s0} + C_p)$. It is a significant factor, considering the value of C_s and C_p are in the order of 100fF and C_{fix} and C_{fb} is on-chip poly-poly capacitors that can easily achieve the capacitance of several pF. To make the comparison more straightforward, a term of equivalent feedback capacitance (EFC) is defined as

$$EFC = (2C_{s0} + C_p) C_{fb} / 2(C_{fix} + C_{fb}) \quad (6-10)$$

It represents the required feedback capacitance in the TCA to achieve the same gain as that by the DDA. In this design, C_{fix} and C_{fb} are 1.5 pF and 90 fF, respectively, and $(2C_{s0} + C_p)$ is approximately equal to 150 fF, so the equivalent TCA capacitance is 4 fF. Furthermore, since the gain of the DDA is based on the capacitance ratio, it is inherently independent on temperature. Therefore, the boosted gain and low temperature dependence are realized simultaneously with the DDA.

6.1.3 Noise Analysis

At the resonant frequency of the CMOS-MEMS gyroscope, the flicker noise is the dominant noise source, whose power density for a MOS transistor can be approximately given by (6-11).

$$\overline{v_{nif}^2} = \frac{K_f}{C_{ox} WL} \cdot \Delta f \quad (6-11)$$

where K_f is a constant, C_{ox} is the gate capacitance density of the MOS transistors, and W and L are the width and length of the transistors, respectively. It is revealed by (6-11) that larger transistor size reduces the flicker noise. However, like the case of open-loop amplifiers, the gate capacitance contributes to the parasitic parameters as well, which will degrade the Coriolis signal. According to (6-9) and (6-11), there should be an optimal transistor size for the best SNR . The optimal width can be derived by letting

$$\frac{\partial SNR}{\partial W} = 0 \quad (6-12)$$

By solving (6-12), we can obtain that the optimal transistor size satisfies the following equation

$$\begin{aligned} C_{gs} &= \frac{2}{3} C_{ox} WL \\ &= 2C_{s0} + C_p' \end{aligned} \quad (6-13)$$

where C_{gs} is the gate-to-source capacitance of the input transistor, and C_p' is the parasitic capacitance other than C_{gs} , which can be caused by the interconnection between the front end and the sensor.

In order to evaluate the noise performance of the DDA, the optimized SNR of DDA is plotted with respect to the sensing capacitance and is compared with other architectures in Figure 6-4. In order to simplify the analysis, it is assumed that $v_{n1}=v_{n2}$, and $C_f=2 \text{ pF}$, which are the typical values from literatures [16, 24]. The transistor sizes of all architectures are optimized for the best noise performance.

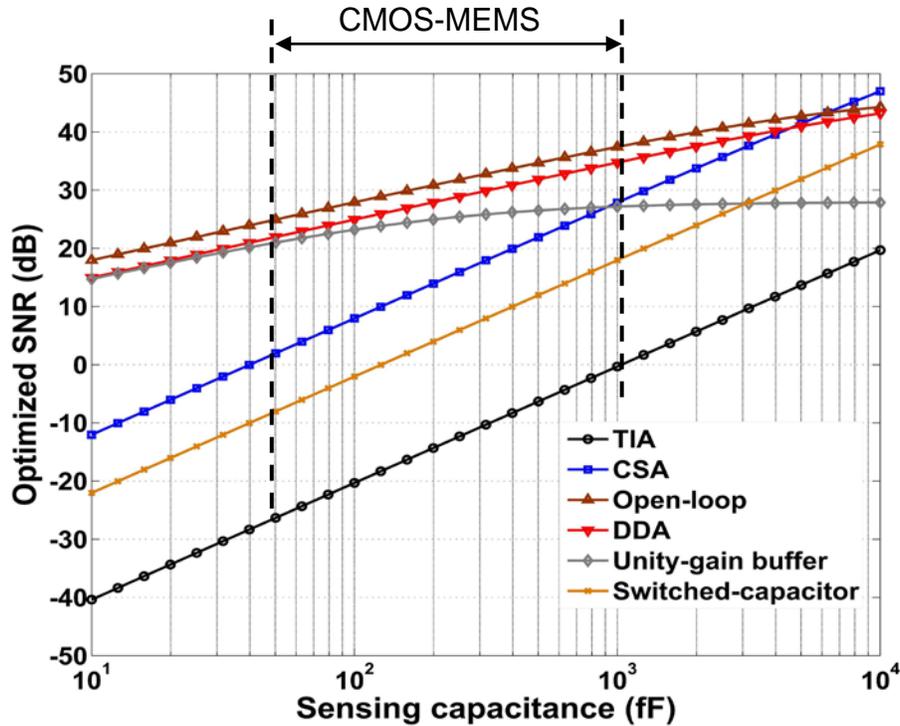


Figure 6-4. The optimized *SNR* of DDA, compared to TIA, CSA, open-loop amplifier, unity-gain buffer, and SC circuits.

6.1.4 Considerations of Quadrature Error and Leakage

The quadrature error, which comes from the cross-axis coupling from the drive mode to the sense mode, is an important issue that needs to be addressed. The quadrature error signal has a 90° phase difference relative to the Coriolis signal, so it can be removed by synchronous demodulation with the driving signal as the demodulation signal. However, the amplitude of the drive mode oscillation is in the order of μm while the Coriolis motion amplitude is only in the order of sub- nm . Thus, even with a 0.1% cross-axis coupling, the induced quadrature signal may overwhelm the Coriolis signal, which results in dynamic range deduction, or in the extreme case of a high-gain system as discussed in this paper, the saturation of the interface circuits. Mechanical decoupling is often incorporated in the sensor structural design to minimize the cross-

axis coupling [25, 26]. In this design, the overdrive voltage of the input transistors of DDA is chosen conservatively large (~ 100 mV) to tolerate the quadrature error and to improve the linearity as well.

Leakage current is another issue that needs to be addressed for the circuits with high input impedance. The CMOS-MEMS process allows fully-differential configuration of the sensing capacitance, as shown in Figure 6-3(b), and V_{bias} is chosen as $1/2$ of V_p for a balanced bias to reduce the leakage current. Due to the capacitive feedback of the DDA, any DC offset caused by leakage current will retain at the output without any amplification and it will not be taken by the following gain stages based on capacitive feedback. Therefore, the drift caused by the leakage will be small.

6.2 System-Level Design

The system for the gyroscope comprised of two subdivisions: the self-oscillation loop for the drive mode and the read-out and processing circuitry for the sense mode. The system works in continuous-time to avoid the noise folding existing in the discrete-time sampling. The block diagram of the system is schemed in Figure 6-5.

In the self-oscillation loop, a transresistance amplifier (TRA) is employed as the front end to detect the drive-mode displacements of the proof mass. There are two reasons for doing so. Firstly, the transresistance amplifier and the sensing capacitance of the sensor comprise a differentiator, which generates 90° phase change to the incoming signal, so the extra phase delay caused by the mechanical structure at the resonant frequency is compensated and the requirements on phase is satisfied to start an oscillation . Secondly, the impedance of the transresistance can be tuned by its gate voltage, in order to achieve a controllable gain of this stage. The TRA is implemented with the fully-differential configuration to reject the common-mode noise. The signal out

of the TRA is further amplified with two more amplification stages before being fed back to the driving electrodes of the sensor to close the loop. Since the CMOS-MEMS gyroscopes are designed to work in atmosphere, the quality factor of the mechanical structure is limited by the damping of air at around 100. Therefore, the amplitude of the drive signal is expected as large as possible for better sensitivity. In order to handle the driving signal with large amplitude, rail-to-rail output is desired on the amplifier that interfaces with the driving electrodes directly. The amplitude of the driving signal is controlled by an automatic gain control (AGC) loop, in which the signal amplitude obtained by an off-chip RMS-DC converter is compared with the reference voltage, and the difference filtered by the loop filter is used to control the gate voltage of the TRA.

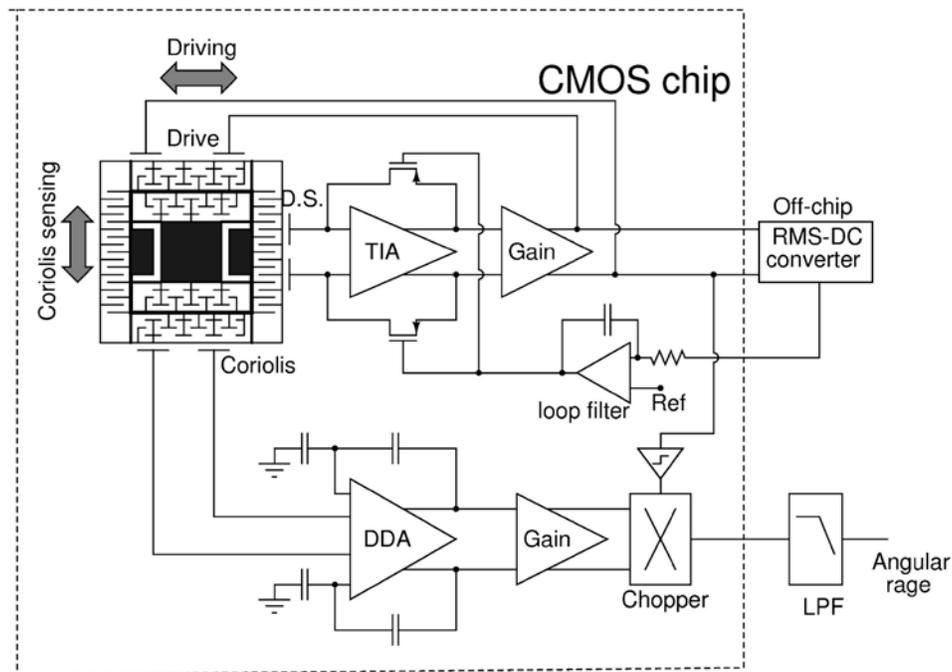


Figure 6-5. System design of the electronics for MEMS gyroscopes.

The Coriolis signal is sensed and amplified with open-loop architecture. The “open-loop” here means that the signal is amplified directly for the next processing

without force feedback to the electrodes. The front-end for the sense mode is a differential difference amplifier (DDA) that combines the advantages of the low noise of the open-loop amplifier and the temperature-dependent gain of the transcapacitance amplifier, and the details will be discussed in the following sections. The signal from the front-end is amplified by a capacitive-feedback amplifier to the desired level.

The information of the rotary rate is modulated to the frequency of the primary resonator, so a chopper demodulator and a low-pass filter are placed to get the signal of the rotation. Since the velocity of the primary resonator is in phase with the driving signal, so does the Coriolis signal. The driving signal is used as the demodulation clock to phase out the quadrature error to get the rotation rate.

The phase issue inside the loop is the most important factor for the system-level design. The driving signal is assumed as

$$V_d = V_0 \sin(\omega t)$$

and the phase delay of the electronics in the drive mode and in the sense mode is φ_d and φ_s , respectively. The Coriolis signal is then

$$V_{coriolis} = K_c \sin(\omega t - \varphi_d - \varphi_s) \quad (6-14)$$

and the quadrature error is

$$V_{quadrature} = K_q \cos(\omega t - \varphi_d - \varphi_s) \quad (6-15)$$

where K_c and K_q are the constants representing the scale factor of the sense mode.

Since the sense mode signal is demodulated with the drive signal. The Coriolis signal and the quadrature signal after demodulation are

$$\begin{aligned} V'_{coriolis} &= K_c V_0 \sin(\omega t - \varphi_d - \varphi_s) \sin(\omega t) \\ &= \frac{1}{2} K_c V_0 (\cos(\varphi_d + \varphi_s) + \cos(2\omega t - \varphi_d - \varphi_s)) \end{aligned} \quad (6-16)$$

and

$$\begin{aligned} V'_{quadrature} &= K_q V_0 \cos(\omega t - \varphi_d - \varphi_s) \sin(\omega t) \\ &= \frac{1}{2} K_c V_0 (\sin(\varphi_d + \varphi_s) + \sin(2\omega t - \varphi_d - \varphi_s)) \end{aligned} \quad (6-17)$$

respectively.

After the low-pass filter, the rotation rate and the zero-rate output due to the quadrature error are

$$V_{rot} = \frac{1}{2} K_c V_0 \cos(\varphi_d + \varphi_s) \quad (6-18)$$

and

$$V_{zro} = \frac{1}{2} K_c V_0 \sin(\varphi_d + \varphi_s) \quad (6-19)$$

respectively.

Due to the phase delay of the electronics, the quadrature error is leaked into the signal rotation rate. And because the coupled movement is much larger than that due to the Coriolis acceleration in amplitude, the significant zero-rate-output will limit the dynamic range of the system, or even more seriously, saturate the amplifier and prevent the system from functioning properly. In this work, the total phase delay of both the drive mode and the sense mode is controlled within 1°.

6.3 Circuits Implementation

In this section, the details of the implementation of the circuitry for both the drive mode and sense mode are discussed. The details of the DDA are not included in this section because they have been discussed in 6.1. The issues considered during the design process are also described.

6.3.1 Driving Circuits

6.3.1.1 Front-end amplifier

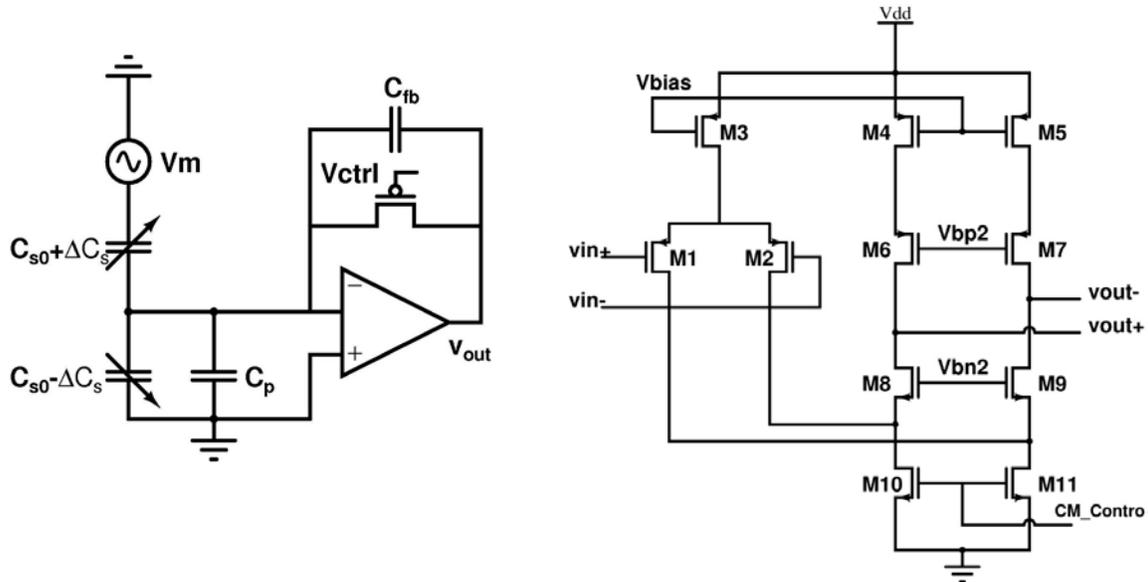


Figure 6-6. The TRA design and the interface to the sensor; (a) the configuration, (b) the schematic of the core amplifier.

The first stage of driving circuits is important, because it not only connects to the sensing capacitor, but works as both VGA and differentiator. A_1 is an operational transconductance amplifier (OTA) based on the folded-cascode topology. The simplified schematic of the core amplifier is shown in Figure 6-6, where the circuits for bias and common mode feedback are not shown. In the following paragraphs, design considerations that determine the circuit parameters will be discussed in details.

Recalled from (4-25)

$$GBW = \frac{G_{eff} \omega}{\tan \phi}$$

In our application, the resonant frequency of the gyroscope is 5-10 kHz. To make the phase delay after amplification within 0.3° , GBW needs to be at least 1.8 MHz, assuming $\omega = 10$ kHz and $G_{eff} = 1$.

With regards to the amplifier, the gain-bandwidth satisfies the following equation,

$$GBW = g_m R_{out} \cdot \frac{1}{R_{out} C_L} = \frac{g_{m1}}{C_L} \quad (6-20)$$

where g_{m1} is defined as the transconductance of input differential pair, while C_L as the load capacitance. And the DC gain is

$$G_{open} = g_{m1} \cdot R_{out} = g_{m1} \cdot (g_{m7} r_{ds7} r_{ds5} // g_{m9} r_{ds9} r_{ds11}) \quad (6-21)$$

$$r_o = \frac{1}{\lambda I_D} \quad (6-22)$$

$$g_m = \frac{2I_D}{v_{od}} = \frac{2I_D}{V_{gs} - V_T} \quad (6-23)$$

From (6-21) and (6-23)

$$G_{open} = \frac{2I_{D1}}{\lambda^2 I_{D7} V_{od1} V_{od7}} \quad (6-24)$$

The size of the input differential pair is calculated based on (6-25).

$$W / L = \frac{I_D}{\mu_{eff} C_{ox} (V_{gs} - V_T)^2} \quad (6-25)$$

(6-25) determines the ratio, but not the actual size of the input differential pairs.

DC offset is another issue that has to be considered, which comes from the parameter mismatch of the transistors. Although A_1 is a transimpedance amplifier that amplifies AC signals only, the input referred DC offset is still passed to output, which will affect the next stage. So the length of input transistors is set to be $2 \mu m$, instead of minimum length. The same measure applies on the current mirrors such as M_4 , M_5 , M_{10} and M_{11} . As regard the other transistors, since it will not introduce DC offset and large transistor size will decrease the frequency of non-dominant pole and do harms to stability, their length is the minimum value.

6.3.1.2 Low-offset amplifier

The second amplifier stage, A_2 , whose schematic is drawn in Figure 6-7, works to amplify the signal to the medium level and cancel the DC offset. The gain of this stage is determined by the ratio of resistors, namely, R_o/R_i . The input transistors work as voltage followers to pass the input AC signal across R_i and convert differential voltage to current difference. The current difference of M_{2b} and M_{2c} is mirrored to the load resistor R_o and converted back to voltage. The key parameter of this stage is the DC current of each branch. There is a tradeoff between power consumption and chip area, since the amplitude of output signal is

$$v_{out} = i_{out} R_{load} \quad (6-26)$$

So less power consumption means larger resistor, and then larger area. One drawback of huge load resistance is that the device mismatch may result in significant dc offset at the output nodes, so that the automatic offset cancellation technology has been applied.

To eliminate the effects of dc offset, an auxiliary amplifier with ultra-low gain-bandwidth and a replica of A_2 are added in, as shown in Figure 6-7(b) and (c). The replica of the main amplifier does not have the output stage.

The auxiliary amplifier and the replica amplifier contribute to make a negative feedback with A_2 , in which the gain is derived as

$$G(s) = \frac{G_2(s)}{1 + G_{aux}(s)G_{replica}(s)} \quad (6-27)$$

where G_2 , G_{aux} , and $G_{replica}$ are the open-loop gain of A_2 , the auxiliary amplifier and the replica amplifier, respectively. The goal of the design is reducing the DC gain as much as possible while keep the AC gain, therefore, the gain-bandwidth of the auxiliary

amplifier is very narrow. In this case, it can be observed that $G \approx 0$ at DC and $G \approx G_2$ at high frequency. The gain-bandwidth of the auxiliary amplifier is designed to be around 50 Hz.

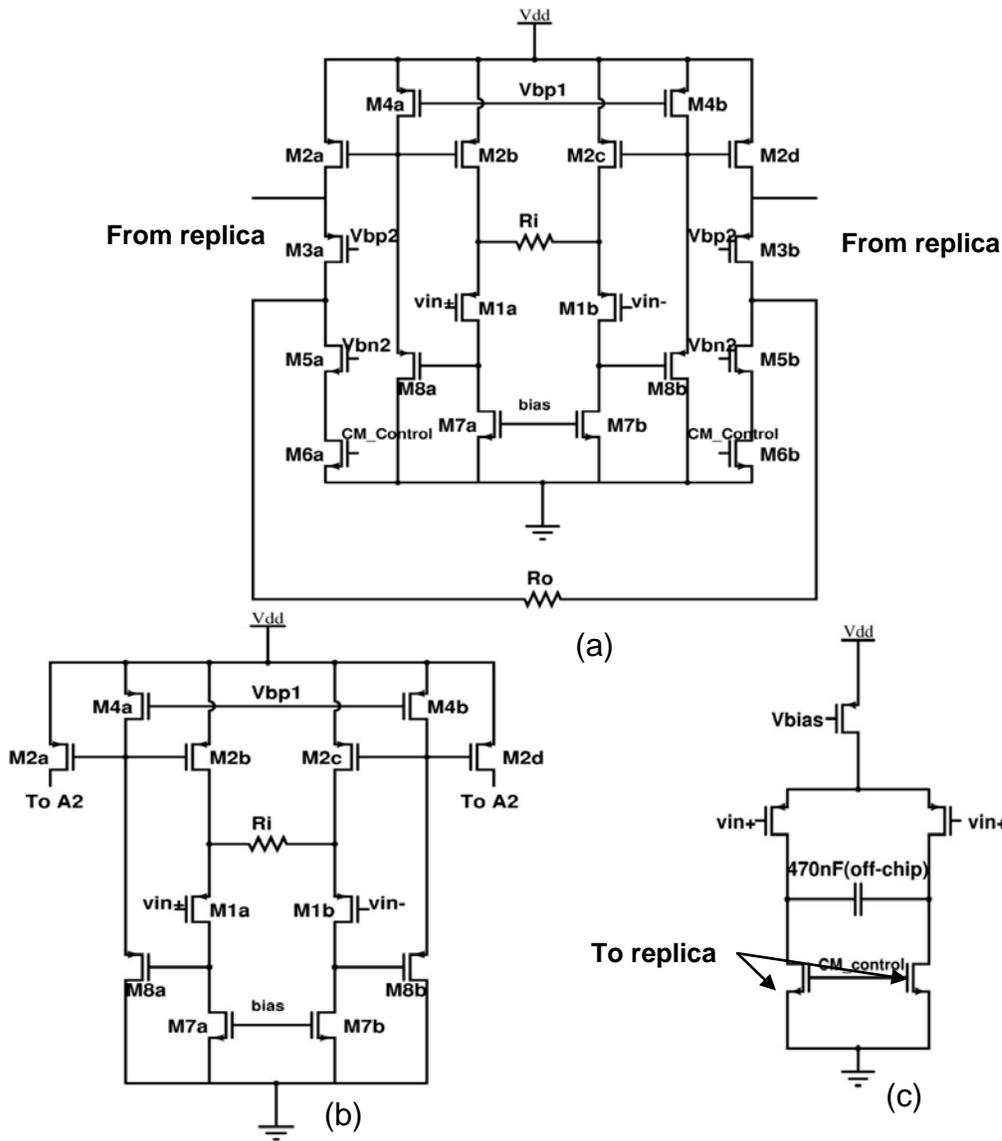


Figure 6-7. Low-offset amplifier of the second amplification stage of the driving circuits; (a) The core amplifier, (b) the replica amplifier, and (c) the auxiliary amplifier.

6.3.1.3 Driving stage

The third stage amplifies the signal to expected amplitude, 2 V in our case, and drives the electrodes of sensor. In this work, it is realized with a two-stage op-amp with

non-inverting configurations based on resistive feedback to get high input impedance. The configuration of the driving stage and the schematic of the core amplifier are drawn in Figure 6-8.

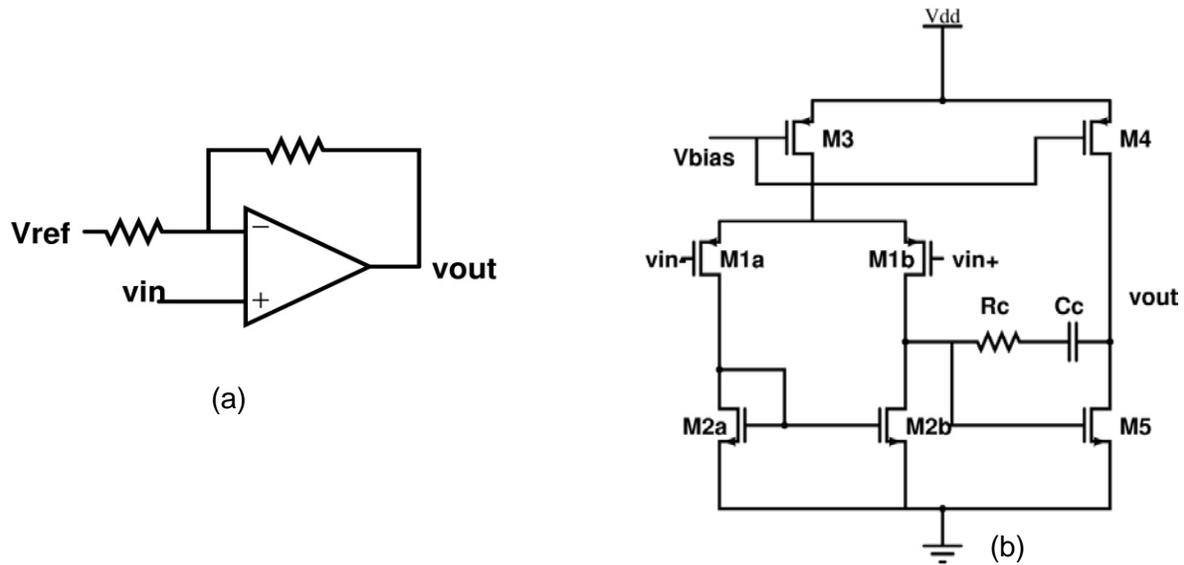


Figure 6-8. Schematic of the third stage of the driving circuits; (a) non-inverting configuration, (b) schematic of the core amplifier.

6.3.2 Other Coriolis Sensing Circuits

The circuits for the detection of the Coriolis signal comprise of two stages of amplifiers, of which the first stage is a low-noise low temperature-dependence DDA as discussed at the beginning of this chapter, and the second stage is an OTA with capacitive feedback to set its gain, with diode-connected PMOS as the DC path. The advantages of the capacitive feedback are the low noise and the low DC offset, compared to the resistive feedback. The configuration and the schematic of the core amplifier are shown in Figure 6-9. The core amplifier of this stage is a fully differential OTA with folded-cascode architecture with common-mode feedback to maintain the DC level.

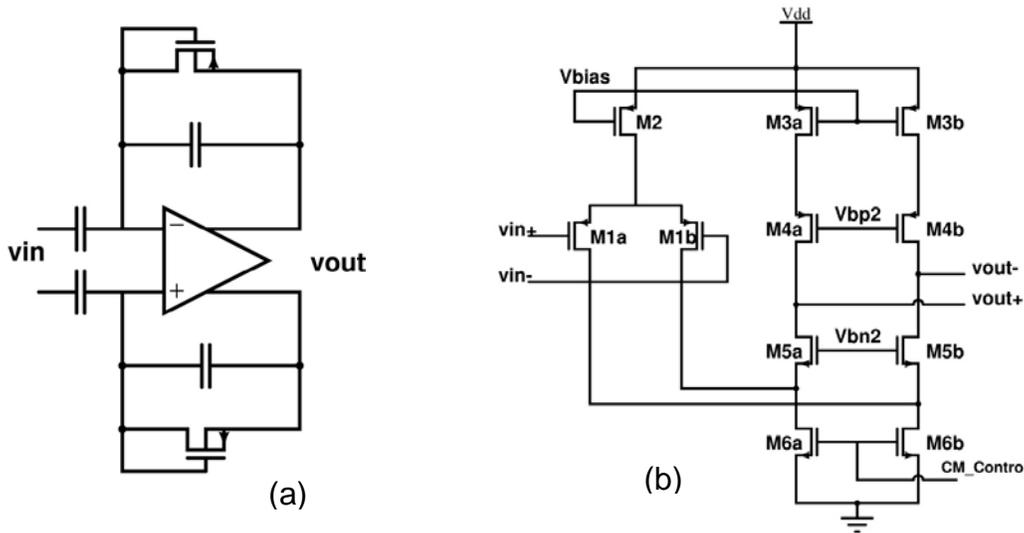


Figure 6-9. Schematic of the second stage of the sensing circuits; (a) configuration of the capacitive feedback; (b) schematic of the core amplifier.

6.3.3 Layout

The chip is fabricated with the Vanguard 0.35 μm 2P4M technology. The layout of the whole chip is shown in Figure 6-10. The die size is $5 \times 5 \text{ mm}^2$, and it contains three devices, a three-axis accelerometer, a z-axis gyroscope, and an x/y-axis gyroscope. The accelerometer is the improved versions mentioned in Chapter 3, with good sensitivity and linearity in the z axis. The electronics sit beside the devices and are covered all over by metal3 layer to be protected in the post-CMOS micromachining process. The big pieces of metal3 layer are slotted properly, with 30 μm interval, to reduce the stress during the CMOS processing. A replica of the interface circuits is implemented with for self-test purpose.

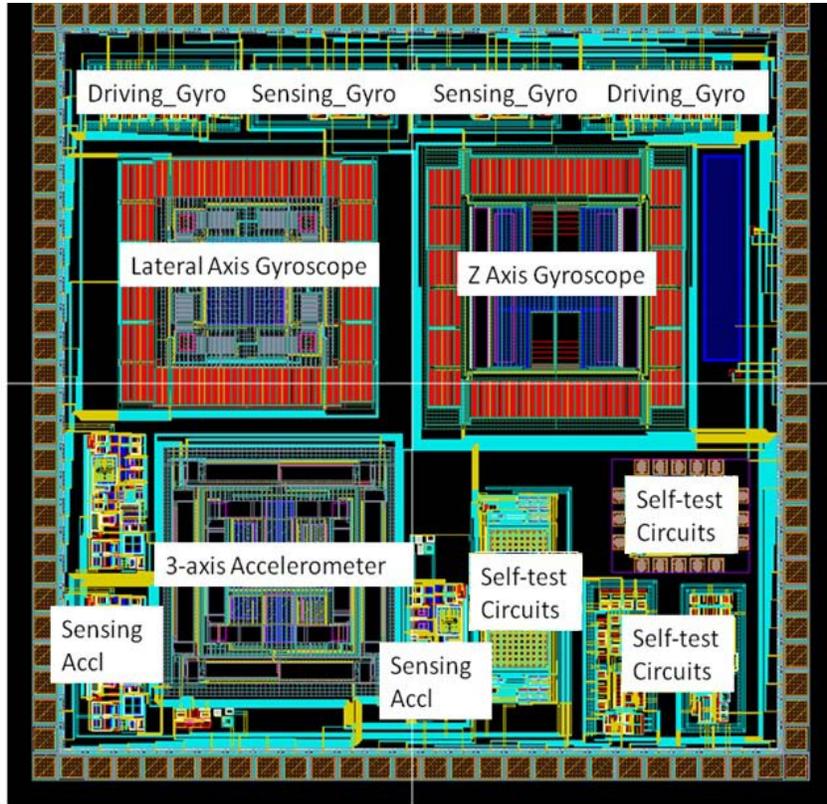


Figure 6-10. Layout of the whole IMU chip.

6.4 Experimental Results

The experimental results of the CMOS-MEMS gyroscope systems will be discussed in this section. The experiments include two parts: the characterizations of the circuits without the MEMS sensors and the testing of the whole system. In this chapter, details of the testing of the circuits and the preliminary results of the system will be discussed.

6.4.1 Coriolis Sensing Circuits

The sensing circuit was tested on bread-board, and the testing environment is schemed in Figure 6-11. Due to the high gain of the Coriolis sensing circuits, it is hard to generate an input signal with sufficient small amplitude directly with function generators. In order to get a small-amplitude differential signal, two in-phase AC signals with

identical DC level of 2.5V, are generated by function generator, so the actual differential signal can be tuned, by 0.1mV resolution, through sweeping the amplitude of one channel while keeping the other channel fixed. Table 6-1 and Table 6-2 list the equipments for testing and the experiment conditions.

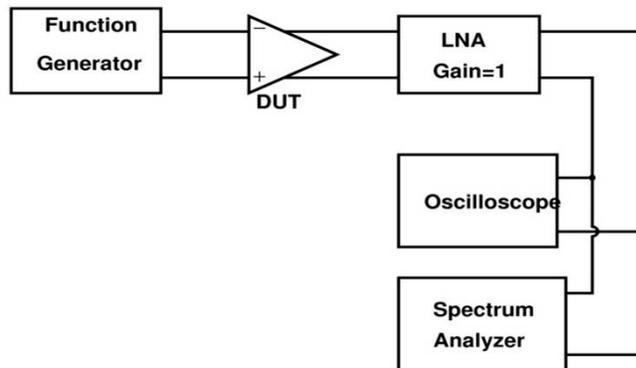


Figure 6-11. Testing setup for the Coriolis signal sensing circuits.

To determine the gain of the circuits, the amplitude of the input signal one channel is fixed at 30 mV and the other channel has amplitude swept from 26.5mV to 34 mV, both at frequency of 10 kHz. The 30 mV ac signal simulates the possible quadrature error and directly coupling, so the performance of the circuits with the presence of large couplings is verified as well with this method. The differential signal is swept then from -3.5mV to 4mV, to remove the possible drifting from the function generator, and the amplitude of the output signal is regarded “negative” in the curve. The results are plotted in Figure 6-12, compared with an ideal linear curve fitted from experimental data, which shows the gain of the sensing circuit is 415, with maximum nonlinearity of 5%. The signal swing is $2.76 V_{p-p}$.

Table 6-1. List of equipments used for the testing of the sensing circuits.

Equipment	Application
HP E3631A	DC power supply
Tektronix AFG3102	Dual-channel function generator
Tektronix TDS 2014	Oscilloscope
SRS SR560	Low noise amplifier
Keithley 225	DC Current source
HP 8561E	Spectrum Analyzer
SRS SR780	Network signal analyzer

Table 6-2. Experimental conditions for the sensing circuits.

Power supply	5V
Bias current	20 μ A
Common mode voltage	2.5V
Amplitude of AC signal from channel 1	30mV
Amplitude of AC signal from channel 2	variable

The transfer function of the whole Coriolis sensing circuits is measured with the SRS 780 signal analyzer, and the phase response is shown in Figure 6-13. It can be observed that the phase delay of the whole sensing circuits is 0.98° at 10 *kHz*, so less than 1° phase delay is achieved at the operating frequencies of the MEMS gyroscopes in this design, which are 2.1 *kHz* for the z axis and 4.2 *kHz*, respectively.

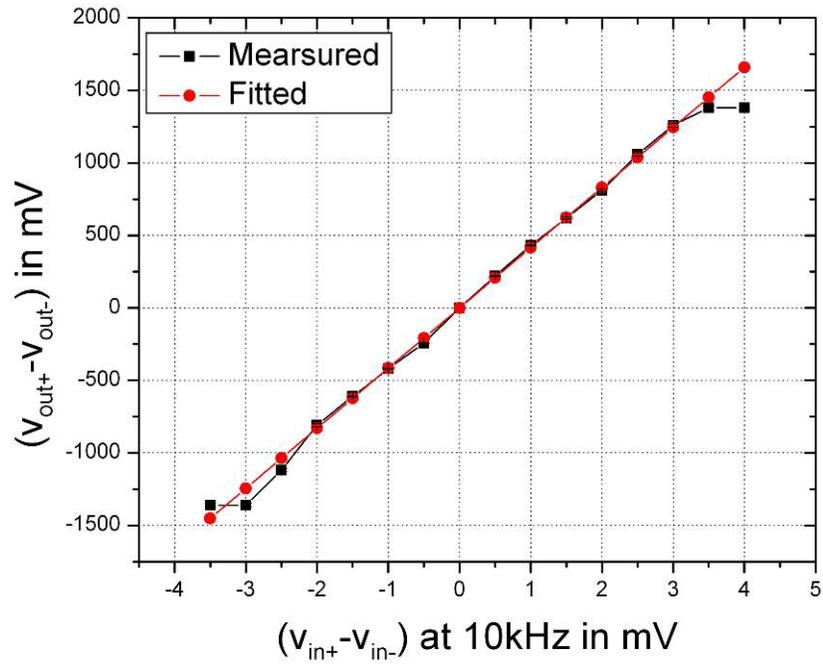


Figure 6-12. Output signal of the sensing circuits vs. input signal in amplitude.

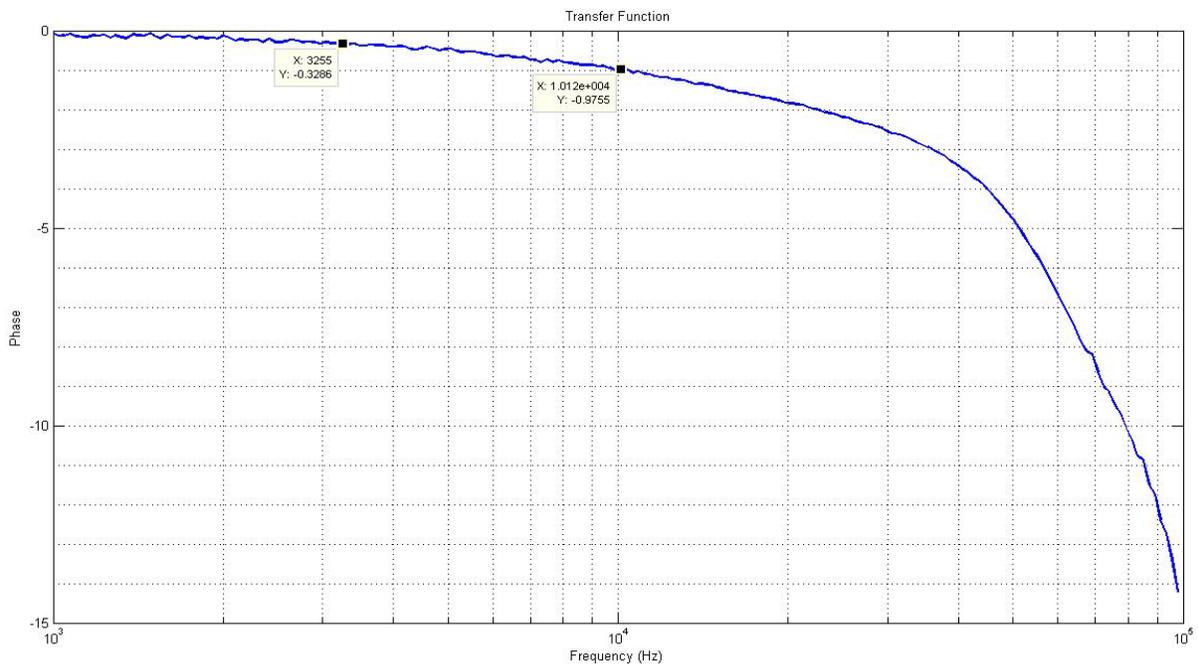


Figure 6-13. Transfer function (phase) of the sensing circuits at 1 kHz-100 kHz.

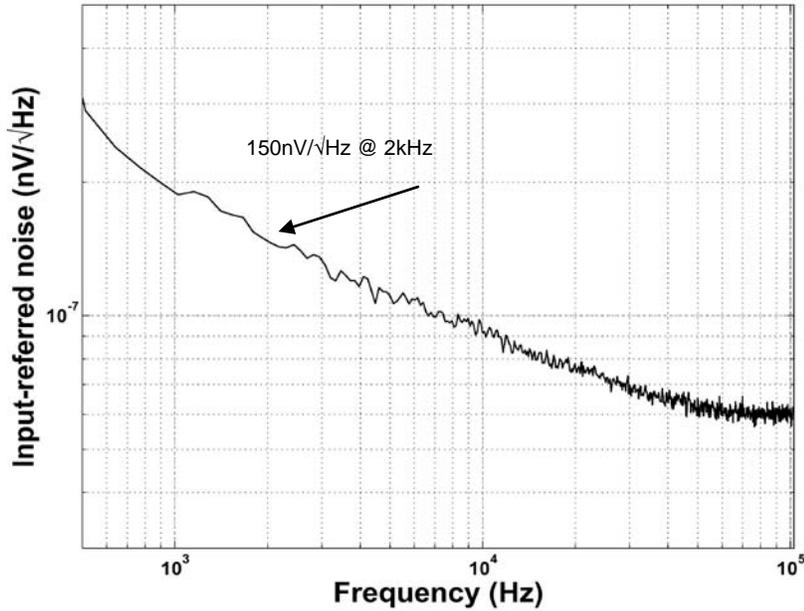


Figure 6-14. Noise spectrum of the sensing circuits.

The input-referred spectrum is plotted in Figure 6-14. The spectrum shows a frequency dependence, which means the main noise source is the flicker noise, and the noise floor at 2 kHz is 150 nV/\sqrt{Hz} . The dynamic range of the sensing circuits can be calculated as (6-28) shows, assuming 10 Hz bandwidth.

$$DR = \frac{MaximumOutput}{NoiseFloor \times BandWidth} = 82dB \quad (6-28)$$

The gain drifting with temperature is measured from 24°C to 104°C. The gain varies from 400 to 396 when temperature is increased from 24°C to 104°C, so the temperature sensitivity is 125ppm/°C. The Coriolis sensing circuit gives good stability over temperature variation, since feedback is applied to both stages, which means the gain of the circuits is set by capacitance ratio, instead of transistor parameters. And the performance of the sensing circuit is summarized in Table 6-3.

Table 6-3. Performance summary of the sensing circuits for gyroscopes.

Item	Value
Gain	415
Maximum Nonlinearity	5%
Signal Swing	2.76V (peak to peak)
Dynamic Range	82 dB
Offset	20 mV
Input referred noise	150 nV/ $\sqrt{\text{Hz}}$ (@2.0 kHz)
Flicker Noise Corner Frequency	74 kHz
Gain drifting	125 ppm/ $^{\circ}\text{C}$

6.4.2 Driving Circuits

The block of driving circuit has three functions: amplification, phase shifting, and automatic gain control. The realization of automatic gain control needs a peak detector, a variable-gain amplifier, and a loop filter. The first stage of the driving circuit is a transimpedance amplifier that works to convert the current signal from capacitor to voltage while keeping the voltage at the sensing node at virtual ground. After conversion, the output signal has 90° phase shift with respect to the input signal. And also, the voltage on gate controls the impedance of the feedback transistor, which determines the gain that stage.

The testing setup for characterization of the first stage of driving circuit is drawn in Figure 6-15. Two 4 pF capacitors are put in the place of the capacitance of the sensor. The gain of the stage is $G=\omega RC$, where $C=4 \text{ pF}$, and $\omega=2\pi\times 10 \text{ kHz}$. The impedance of the transistor can be calculated from the gain. An optional T-network can boost the

transimpedance by a factor of $(1+R_2/R_1)$, where R_1 is a 100 k Ω on-chip resistor and R_2 is external. During testing, R_2 is not connected into the configuration. Figure 6-16 plots the relationship between the impedance and control voltage applied on gate. It can be observed that the impedance is increased by a factor of 4, from 1.8 M Ω to 6.9 M Ω , when control voltage tuned from 0 to 1.3 V.

Figure 6-17 plots the curve of peak-to-peak amplitude of differential output signal of the TRA in response to input signal. The amplifier shows better linearity when the output amplitude is less than 1 V, which corresponds to ± 0.25 V fluctuation of the drain-to-source voltage of each transimpedance transistor. It is normal because the impedance is realized with a long transistor in linear range, which works as a resistor when its drain-to-source voltage is small and has more significant nonlinearity as that voltage gets larger. Since the gain of the following two stages is more than 10, thus the amplitude of the output is less than 0.5 V at steady state after the oscillation has been excited. It can be observed that the TRA stage has good linearity in this range.

Figure 6-18 plots the curve to show the amplitude of the output of the whole driving circuits in response to the input. The signal swing of the output differential signal is up to 4.6V, with the maximum nonlinearity of 5%, so the large signal swing is achieved with the two-stage op amp and non-inverting resistive configuration. The low-offset intermediate amplifier functions properly to prevent the driving stage from being saturated by the offset of the previous stage.

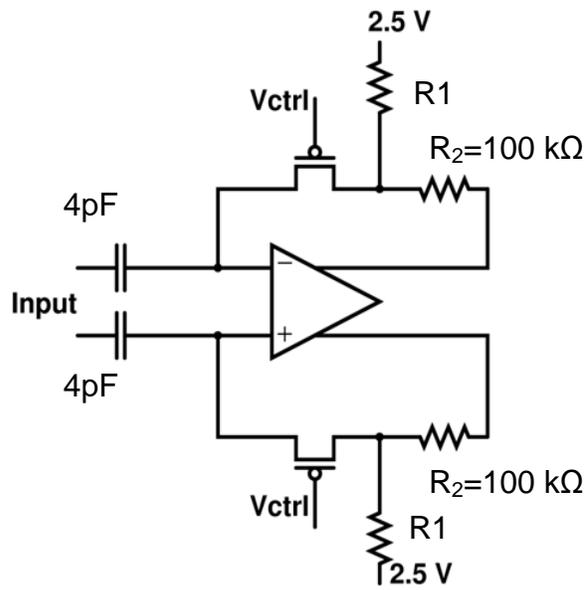


Figure 6-15. Testing setup for the TRA.

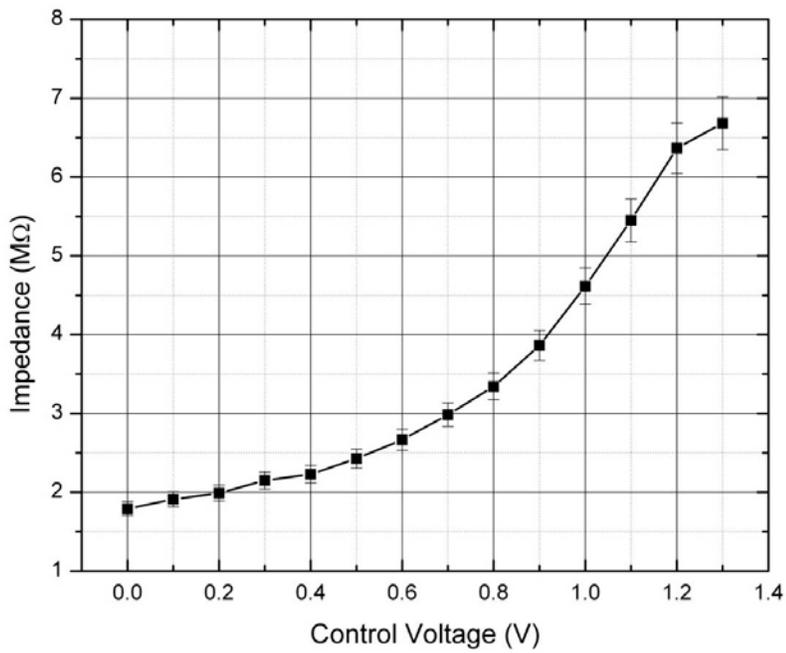


Figure 6-16. The transresistance of the TRA vs. the gate voltage.

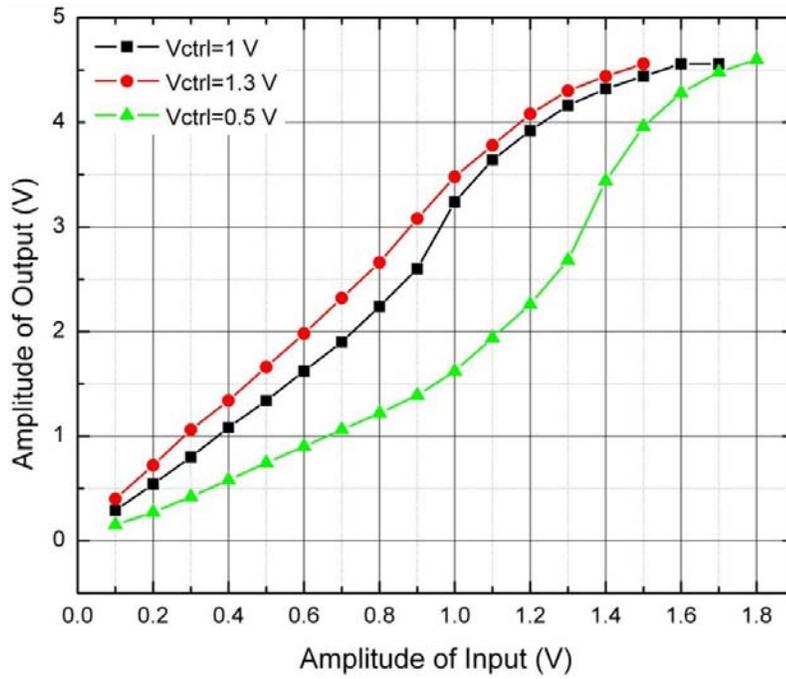


Figure 6-17. Differential output of the TRA vs. input in terms of peak-to-peak amplitude.

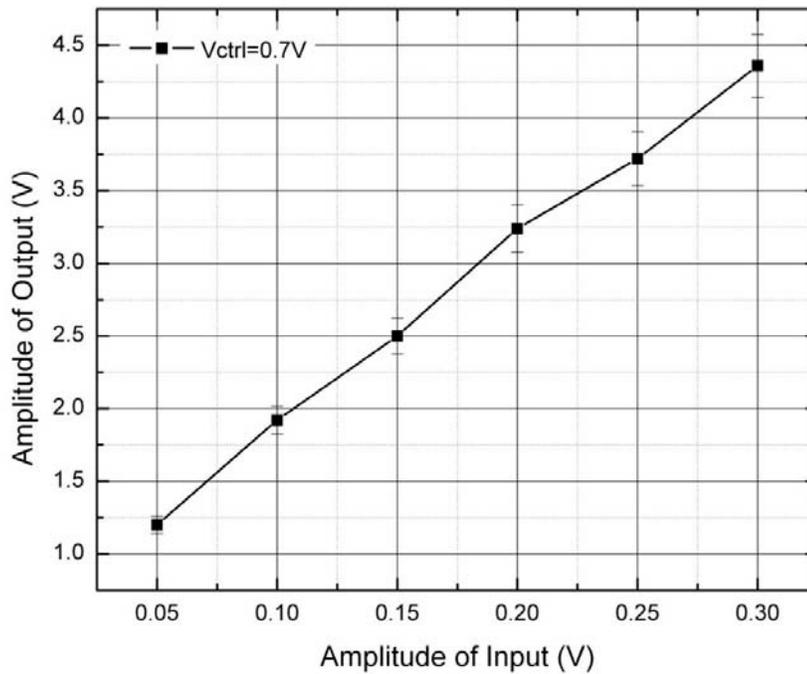


Figure 6-18. Output of the whole driving circuits vs. the input in amplitude.

The influence of temperature is characterized through gain drifting of the whole driving circuit with respect to temperature variation, as shown in Figure 6-19. As temperature is increased from 24°C to 104°C, the overall gain decreased from 8.08 to 7.04, a 12.9% change. The temperature dependence is because of the gain set by feedback resistance in TRA. In the driving circuits, the drifting is not a big issue, because the AGC can tune the gain to achieve certain amplitude automatically.

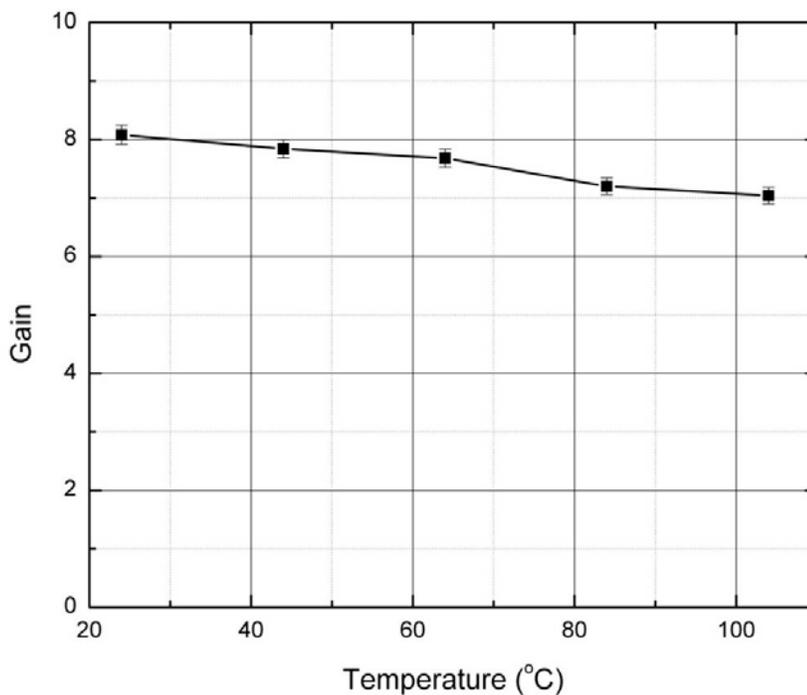


Figure 6-19. Overall gain of the driving amplifiers vs. temperature.

The performance of the TIA based circuits in the drive mode is summarized in Table 6-4. 1.8-6.9 $M\Omega$ tunable impedance is achieved. The gain of the whole circuits is sensitive to temperature due to the transimpedance realized with MOS transistors, but the drifting can be compensated by the automatic gain control so it will not generate any drifting on the oscillation amplitude in the drive mode.

Table 6-4. Performance summary of the driving circuits for gyroscopes.

Item	Value
Tunable Impedance	1.8-6.9 $M\Omega$
Maximum Nonlinearity	5%
Phase shift (10 kHz)	88.6°
Signal swing	4.6 V (peak to peak)
Gain drifting	1600 ppm/°C

6.4.3 System Characterization

The electronics have been integrated with the MEMS gyroscopes on a 5x5 mm² chip with the Vanguard 0.35 μm technology. The released z-axis and x/y-axis gyroscopes have been shown in Figure 3-5 and Figure 3-6.

The system of the z-axis gyroscope with all the electronics is characterized first. Figure 6-20 shows the waveform of the driving signal after the self-oscillation loop is closed. It can be observed that a stable oscillation is started up successfully within 120 ms. The functionality of the electronics for the drive mode is verified. Since the on-chip high voltage is unavailable, the amplitude of the driving signal should be as large as possible to increase the sensitivity of the system. Therefore, the control voltage is raised to make the driving signal saturated for the largest amplitude.

The chip with released devices is mounted on a pendulum for the dynamic response testing, and a reference accelerometer is mounted as a reference for calculating the rotation rate, as shown in Figure 6-21. Figure 6-22 shows the spectrum of the z-axis gyroscope under an 8 °/s rotation, so the sensitivity is estimated as 1.2 mV/°/s, and the noise floor is 0.050 °/s/ $\sqrt{\text{Hz}}$.

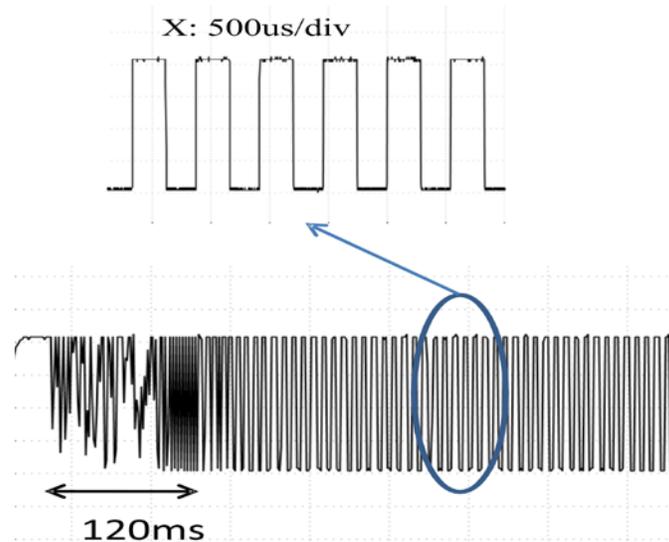


Figure 6-20. Waveform of the start-up of the self-oscillation.

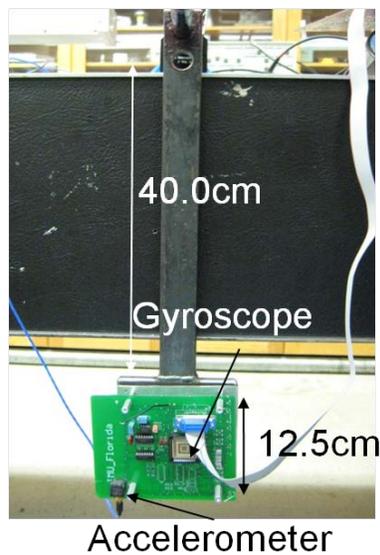


Figure 6-21. The setup of the pendulum for the dynamic testing of the z-axis gyroscope.

Figure 6-23 compares the base-band rotation signal out of the z-axis gyroscope and the radius acceleration signal measured by the reference accelerometer. The frequency of the signal from the gyroscope is half of that of the accelerometer as expected, because the radius acceleration does not tell the rotary direction while the rotation rate does. Therefore, the signal detected by the gyroscope is the real Coriolis

signal instead of interference from the linear acceleration, and the functionality of the system is verified.

Similarly, the functionality of the x/y-axis gyroscope has been verified. The spectrum of the output signal of its sensing circuits in response to an 8 °/s rotation is shown in Figure 6-24. Its sensitivity is estimated as 1.3 mV/°/s, and the noise floor is 0.046 °/s/√Hz. The performance of the DDA-based electronics and that of the two gyroscope systems are summarized in Table 6-5 and Table 6-6.

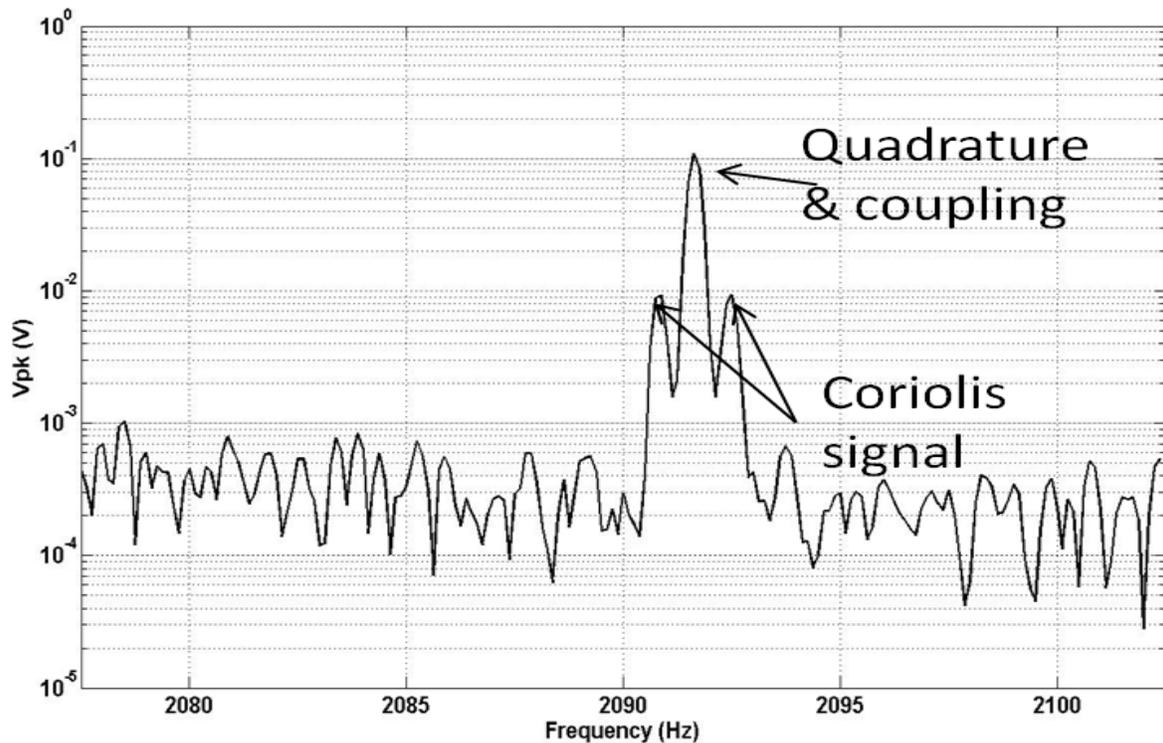


Figure 6-22. Spectrum of the output of Z-axis under 8°/s rotation.

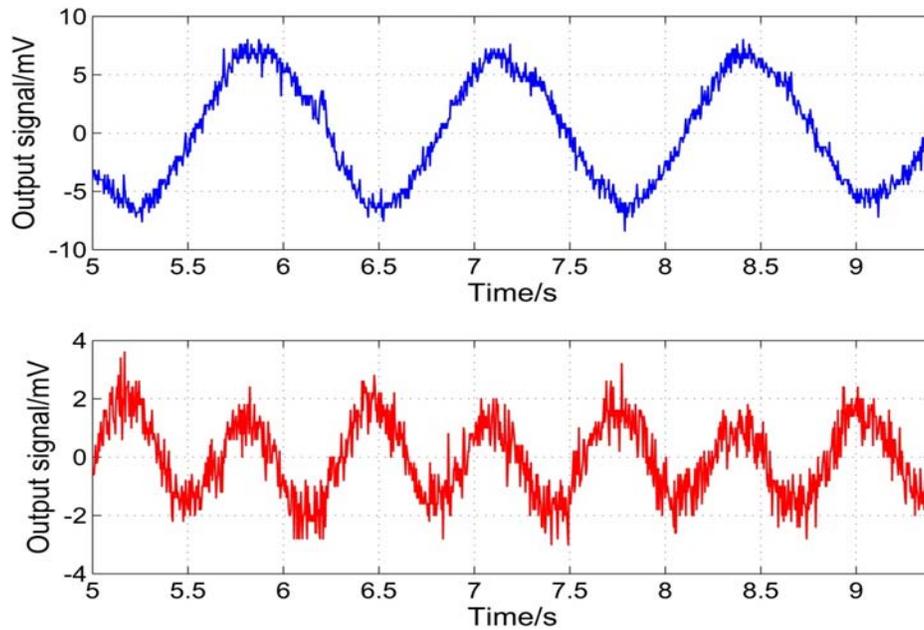


Figure 6-23. Output of the rotation rate of a pendulum compared with a reference accelerometer.

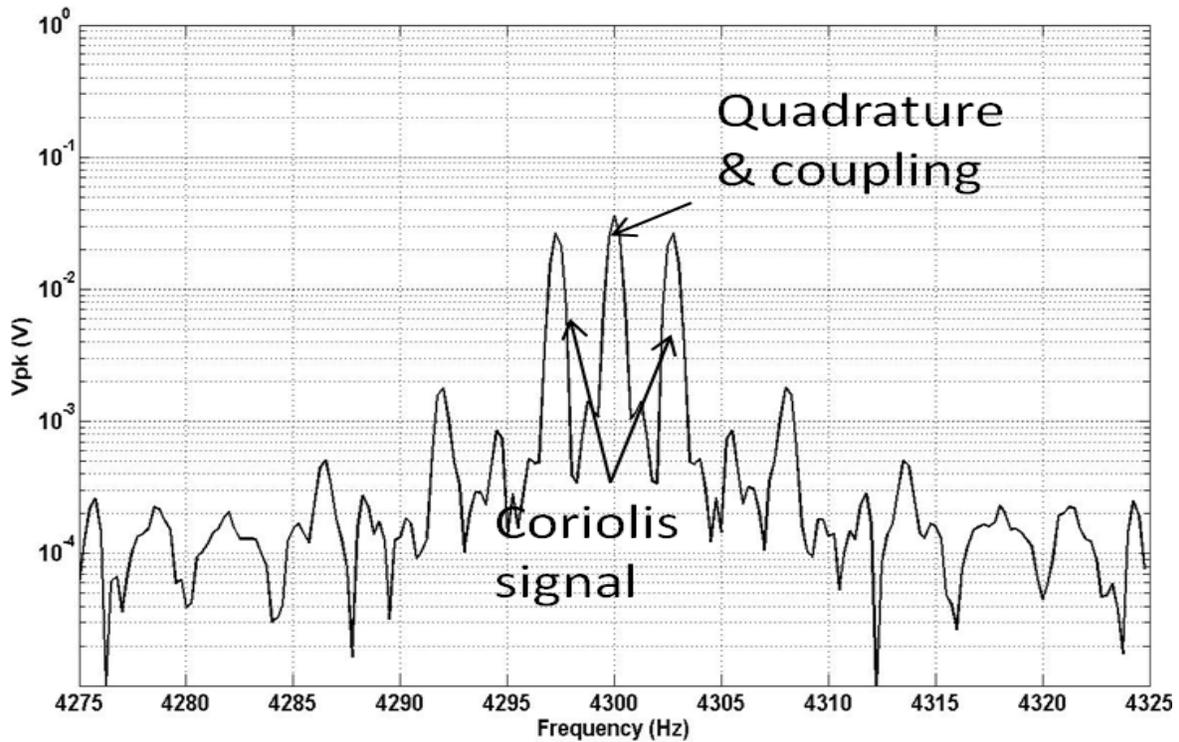


Figure 6-24. Spectrum of the output of X/Y-axis under $8^\circ/s$ rotation.

Table 6-5. Performance summary of the DDA-based electronics for gyroscopes.

Circuits	
Gain	24 dB (DDA) 52 dB (overall)
Sensitivity drift	0.01%/°C
Power	5V, 750 μ W (DDA), 4.25 mW (overall)
Noise (input)	150 nV/ \sqrt Hz @ 2 kHz
Dynamic range	83 dB (10Hz Bandwidth)
Equivalent TCA capacitance	4 fF

Table 6-6. Performance of the z-axis and the x/y axis gyroscopes.

Gyroscope	z axis	x/y axis
Noise floor	0.050°/s/ \sqrt Hz	0.046°/s/ \sqrt Hz
Sensitivity	1.2mV/°/s	1.3mV/°/s
Drive mode	4.2 kHz	2.1 kHz
Sense mode	5.12 kHz	3.05 kHz

6.5 Discussions

Figure 6-25 compares the power and the noise floor in terms of zF/\sqrt Hz, which represents the resolution of capacitive change, with other works that have this parameter available [40, 48, 86]. Finer capacitive resolution means lower noise floor when the sensors have the same mechanical sensitivities. It can be found from the figure that this work achieves the finest capacitive resolution with the lowest power

consumption. That means the DDA-based sensing electronics achieves low power and low noise simultaneously.

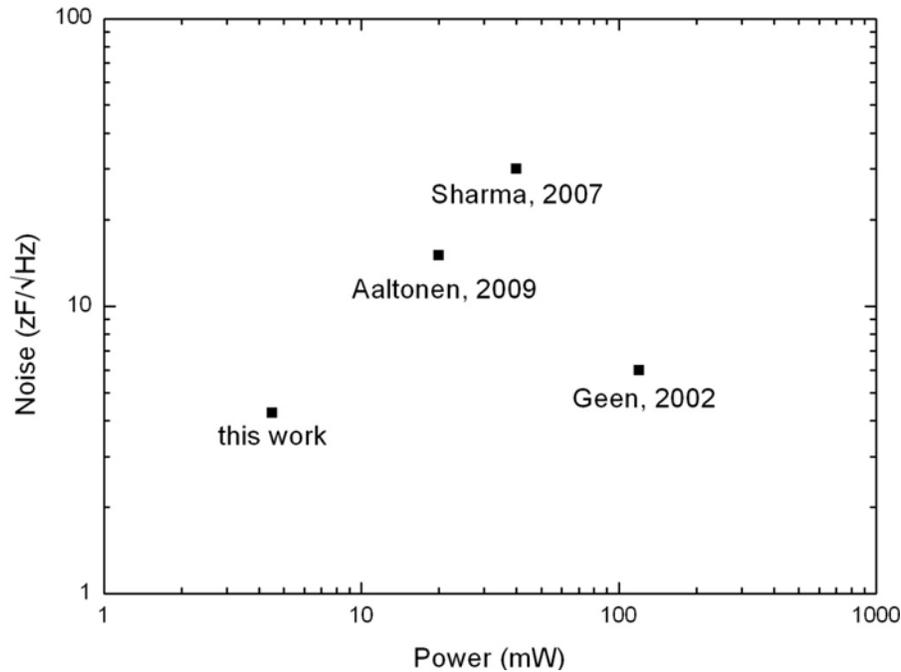


Figure 6-25. Comparisons of the power and noise in terms of zF/\sqrt{Hz} .

However, when the noise floor is represented in terms of $\%s/\sqrt{Hz}$ [40, 48, 113, 114], which measures the resolution for the real mechanical signals, this work still achieves low power consumption, but the noise floor is relatively high, as shown in Figure 6-26. That is because the mechanical sensitivity of the sensor in this work is low, so the same mechanical rotation induces less capacitive change in this work than other sensors. Those sensors with vacuum packaging are not counted into the comparisons due to their inherently high sensitivity and low bandwidth. The most important reason of this phenomenon is the lack of on-chip high voltage, so the amplitude of the movements in the drive mode is relatively low. Due to the ESD diodes on the IO pads, the high

voltage cannot be applied externally. With 15 V on-chip voltage, less than $0.01 \text{ }^\circ/\text{s}/\sqrt{\text{Hz}}$ noise floor is achievable, and the design of the charge pump is discussed in Chapter 7.

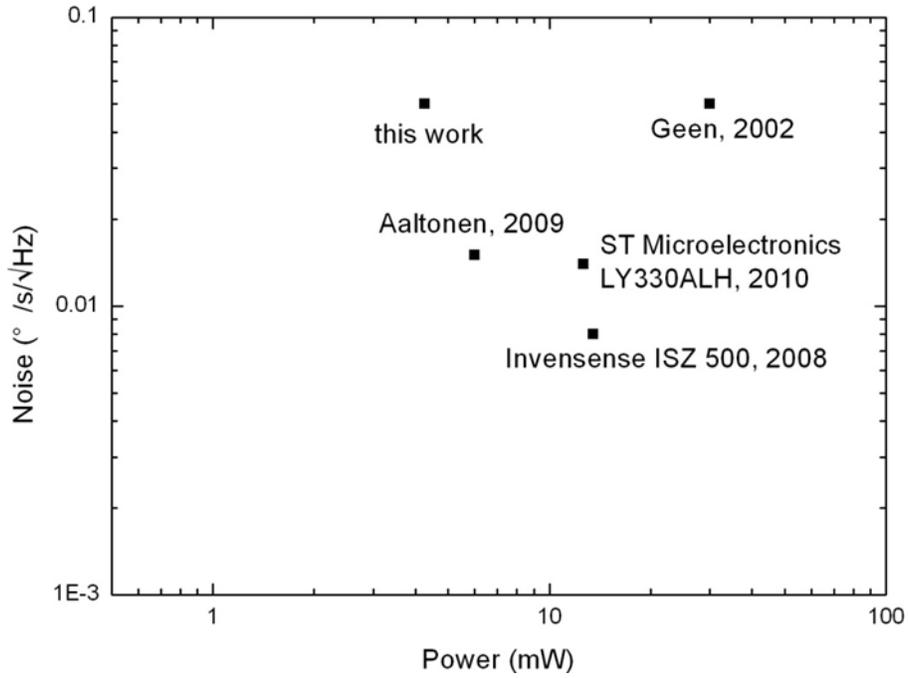


Figure 6-26. Comparisons of power and noise floor in $^\circ/\text{s}/\sqrt{\text{Hz}}$.

CHAPTER 7 IMPROVEMENTS ON THE GYROSCOPE SYSTEM

In this chapter, the improvements made on the current gyroscope system are introduced, which include both circuitry implementation and system-level improvements. Specifically, a charge pump is designed for high voltage generation, a ripple-free fast settling peak detector is designed for better integration capabilities, and a quadrature error cancellation loop is proposed, the first two of which have been verified by experimentally, while the third of which has been verified with simulation.

7.1 High On-Chip Voltage Generation

It is discussed in Chapter 2 that high on-chip voltage is desired, because it can increase the mechanical sensitivity and the strength of the signal fed into the interface circuits. The high voltage can be generated with charge pumps, which pump the charge from low voltage to high level through a cascade of diodes by switching capacitors between the diodes. In this design, A Dickson charge pump is chosen for the high voltage generation for its advantage of good compatibility with the standard CMOS technologies. In this section, the operations of the Dickson charge pump is introduced, and the implementation and the experimental results are shown to verify the design.

7.1.1 Dickson Charge Pump

A typical Dickson charge pump is shown in Figure 7-1. ϕ and $\bar{\phi}$ are out-of-phase signals that drive the charge-storage capacitors, and C_{1-n} represents capacitors that store charge. To simplify the analysis, only D_{1-4} will be considered in the following discussion. When ϕ is high and $\bar{\phi}$ is low, D_2 and D_4 are forward-biased, while D_1 and D_3 are reverse-biased, so current flows from C_1 and C_3 through D_2 and D_4 to charge C_2 and the load, respectively. When ϕ is low and $\bar{\phi}$ is high, D_2 and D_4 are reverse-biased,

while D_1 and D_3 are forward-biased, allowing current flowing through D_1 and D_3 to recharge C_1 and C_3 , which will be discharged in the next cycle. Alternate switching pumps charges continuously from input to output, and after n stages, the voltage increases by

$$\Delta V = V_\phi - V_d \tag{7-1}$$

where V_ϕ and V_d are the amplitude of the driving signal and the drop voltage of the diodes, respectively. Considering the parasitic capacitance from the diodes, however, (7-1) becomes

$$\Delta V = \frac{C}{C + C_s} V_\phi - V_d \tag{7-2}$$

Assuming a purely capacitive load with $R_L = \infty$, one can calculate the output voltage of an N -stage Dickson charge pump as

$$V_{out} = V_{in} + N \left(\frac{C}{C + C_s} \cdot V_\phi - V_d \right) - V_d \tag{7-3}$$

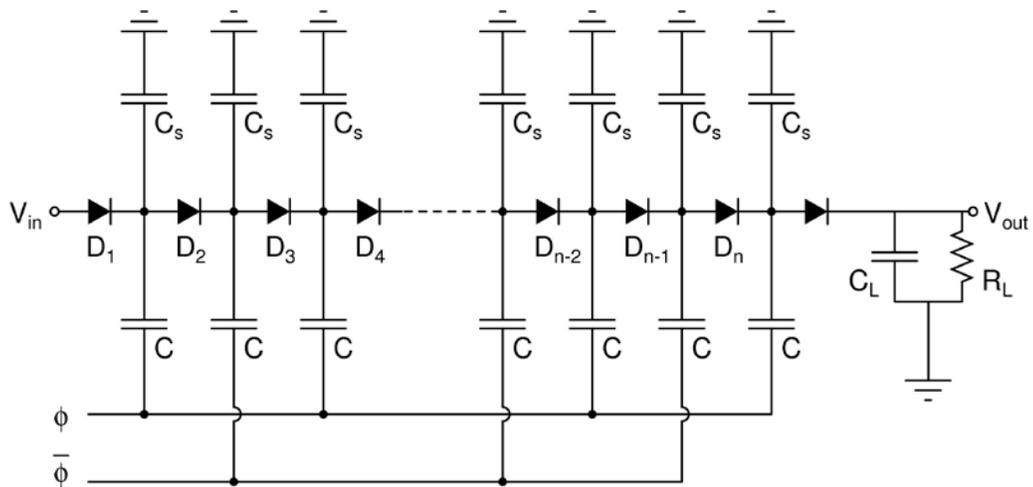


Figure 7-1. Schematic of the Dickson charge pump.

If $R_L \neq \infty$, the loading effect must be taken into consideration, and the output voltage is

$$\begin{aligned}
 V_{out}' &= V_{in} + N \left(\frac{C}{C + C_s} \cdot V_{\phi} - V_d - \frac{I_{out}}{(C + C_s) \cdot f_{\phi}} \right) - V_d \\
 &= V_{out} - \frac{I_{out}}{(C + C_s) \cdot f_{\phi}}
 \end{aligned}
 \tag{7-4}$$

where I_{out} is the current delivered to the load, and f_{ϕ} is the frequency of the driving clocks. The equivalent output resistance is defined as R_s , and the output voltage of the Thevenin network is

$$V_{out}' = V_{out} - I_{out} R_s
 \tag{7-5}$$

Therefore, comparing (7-4) and (7-5) gives the output resistance as

$$R_s = \frac{1}{(C + C_s) \cdot f_{\phi}}
 \tag{7-6}$$

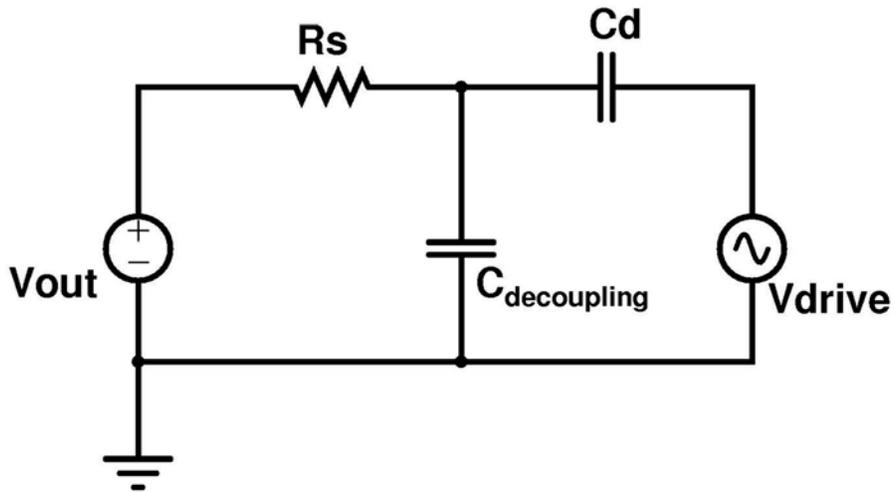


Figure 7-2. Simplified model of the interface between the charge pump and the sensor.

Figure 7-2 simply models the interface of the charge pump to the comb fingers of the sensor, where the charge pump is represented with a Thevenin network and the total capacitance of all the driving comb fingers is lumped into C_d . In order to keep good

linearity, V_I should be virtual ground and the fluctuations due to coupling from the driving circuits should be as small as possible. A 1 nF capacitor $C_{decoupling}$ is put in parallel with the load to reduce ac fluctuations. It is calculated from the model that

$$V_I = \frac{R_s}{R_s + 1/j\omega C_d} V_d \quad (7-7)$$

In this design, the total capacitance of all driving fingers is approximately 500 fF , and the driving-mode resonant frequency is around 2 kHz . In order to make V_I no more than 0.1% of V_d , which is 5 V in this design, R_s should be less than $150\text{ k}\Omega$. The total capacitance of each stage is around 2.5 pF , so the clock frequency of the driving signal should be more than 2.5 MHz .

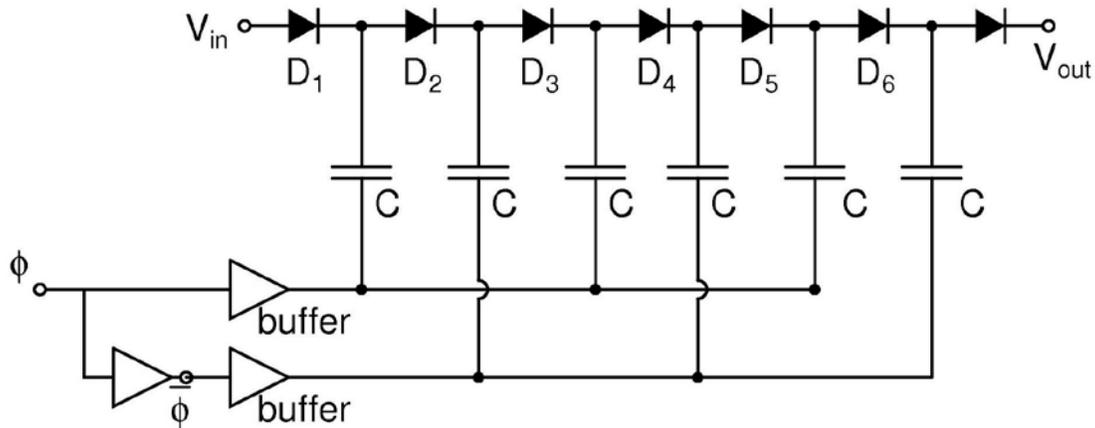


Figure 7-3. The schematic of the Dickson charge pump.

7.1.2 Circuit Implementation

The schematic of the 6-stage Dickson charge pump in this design is illustrated in Figure 7-3. Schottky diodes are used for their low drop-off voltage and fast response. The on-chip capacitors are realized with poly-insulator-poly (PIP) capacitors, and the

capacitance value of each capacitor is 2 pF . The charge pump is implemented with AMI $0.5 \text{ }\mu\text{m}$ technology and the layout is shown in Figure 7-4.

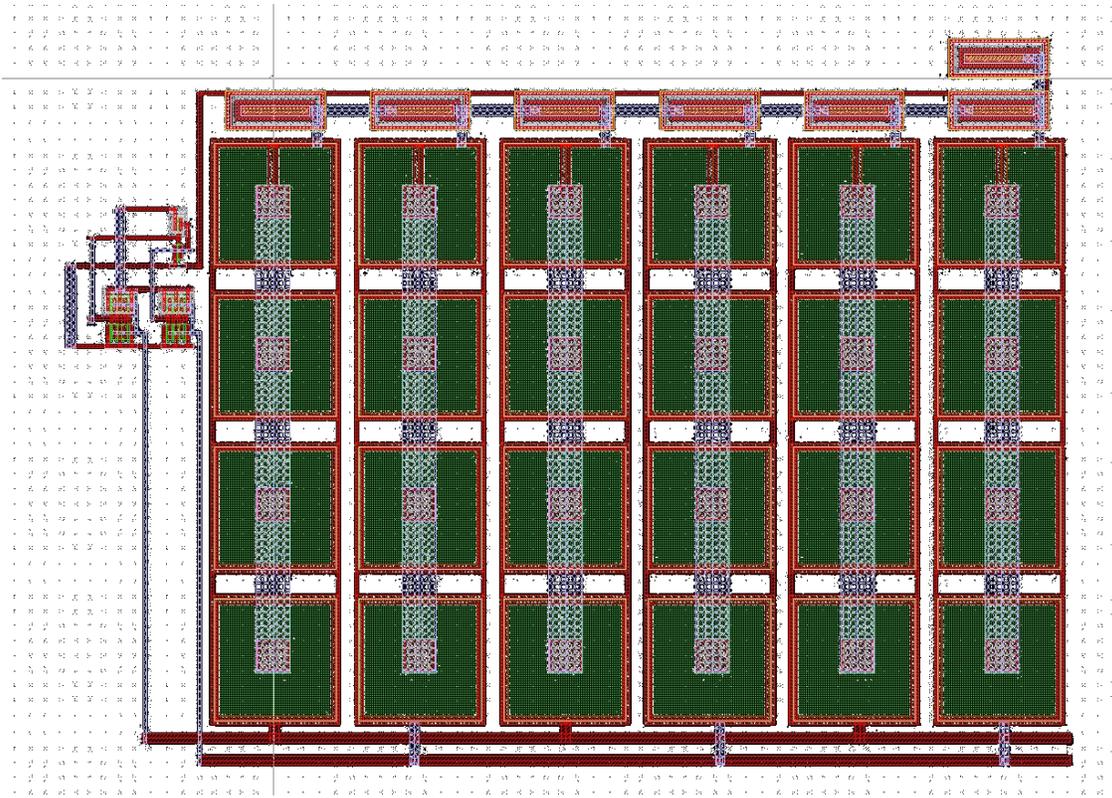


Figure 7-4. Layout of the 6-stage charge pump.

7.1.3 Experimental Results

For performance comparison, a 4-stage charge pump with the same capacitors is fabricated as well. Figure 7-5 shows how the output voltage is affected by the clock frequency, with the load of $100 \text{ k}\Omega$, $1 \text{ M}\Omega$, and $10 \text{ M}\Omega$, respectively. As predicted by (7-9), the output voltage increases at higher clock frequency or with lighter load. It can be observed that a dc level as high as 32 V is generated by the 6-stage charge pump at 10 MHz clock frequency, when the load is $10 \text{ M}\Omega$. The worst case happens when the load resistance is $100 \text{ k}\Omega$, which represents serious leakage of the sensor capacitor, and the maximum output is 14 V , which is still sufficient to start up the self-oscillation.

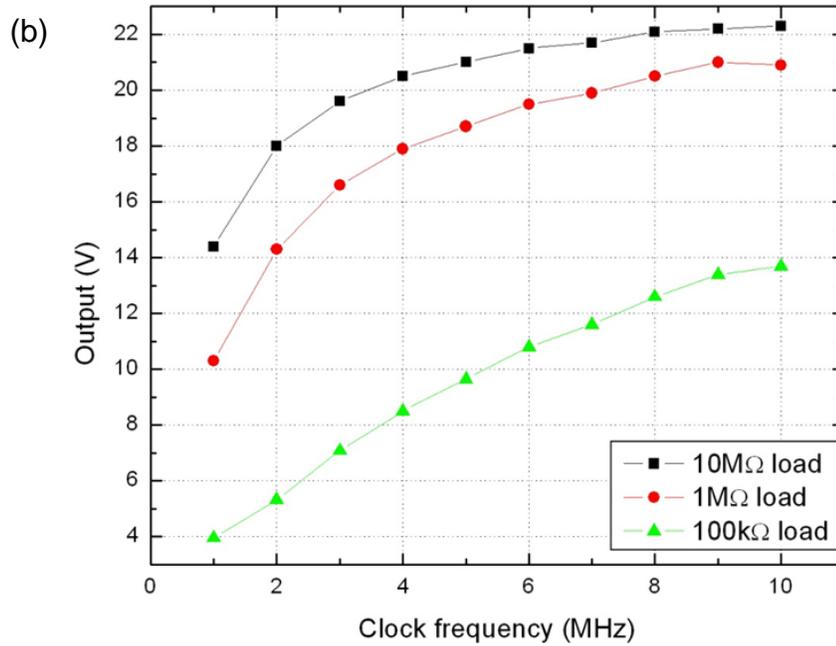
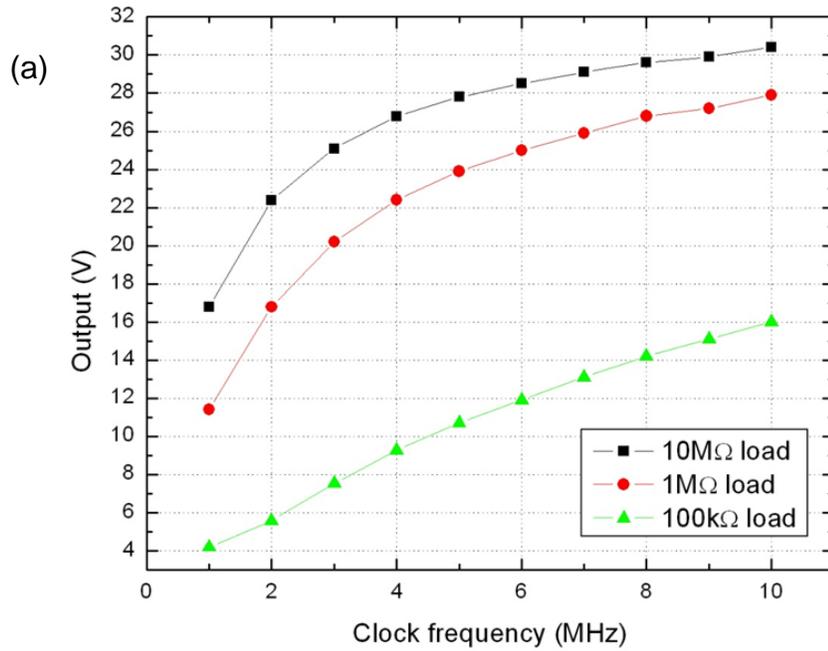


Figure 7-5. Output voltage of different charge pump designs vs. clock frequency: (a) 6-stage charge pump; (b) 4-stage charge pump.

7.2 Fast-Settling Ripple-Free Peak Detector

7.2.1 Circuits Implementation

Envelope detector is the key component in the AGC loop. The traditional RC envelope detector suffers from a trade-off between tracking speed and ripple amplitude, i.e., fast envelope tracking will lead to large output ripples. In addition, large filtering capacitors are needed in such low-frequency applications as MEMS gyroscopes, which are hard to be integrated. In this work, a new switched-capacitor based envelope detector is designed to realize accurate and fast tracking for various input signals in the audio frequency range, such as speech signals and driving signals for MEMS gyroscopes.

Figure 7-6(a) shows the architecture of the proposed envelope detector, where “+” and “-” are used in the subscription to identify differential signal pairs or device pairs with similar functions. Two complimentary channels work in sequence for the input signal, V_{in+} and its inverted signal, V_{in-} , respectively, in order to obtain the continuous envelope signal. In each channel, A_1 , M_1 , and C_1 compose a peak detector, followed by a switched-capacitor (SC) amplifier composed of A_2 , C_1 , and C_2 . The peak voltage of each cycle of the input signal is captured by the peak detector and is stored in C_1 . Then the peak voltage is transferred to the output through C_2 of the SC amplifier A_2 . The clock signals are configured such that the peak value is isolated from the previous peak detecting stage as C_1 is discharged to the analog ground for each cycle. Since the output is not affected by the charging/discharging of C_1 , the ripples due to this process are minimized. Also the capacitance of C_1 can be small for fast settling. Compared with a conventional diode-based peak detector that draws the charging current from the amplifier and through a diode, this detector draws current directly from the power source

while the amplifier just provides a control signal. So, the slew rate is much higher, depending on the size of M_1 .

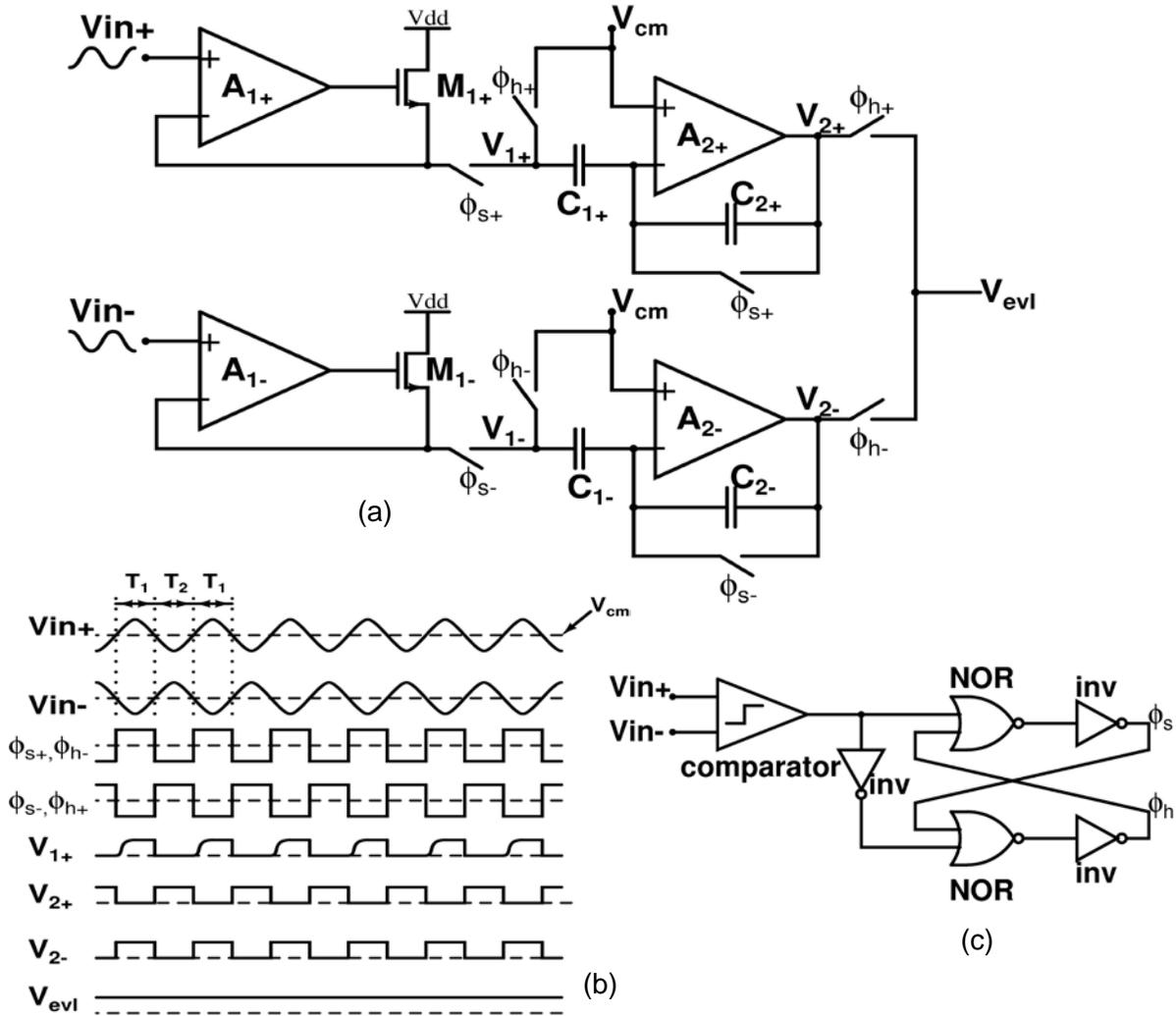


Figure 7-6. (a) Architecture of the switched-capacitor envelope detector; (b) clock signals and the voltage at critical nodes; (c) circuits for generating the non-overlap control signals.

The waveforms of the control signals and the voltages at critical nodes are illustrated in Figure 7-6(b). The control signals, ϕ_s and ϕ_h , are the buffered outputs of the comparison result of the input signal pair, as shown in Figure 7-6(c). ϕ_s and ϕ_h are

non-overlapping to reduce the glitches when the multiplexer is switched. To simplify the analysis, V_{in+} is taken as the example to explain the operation.

During the sampling phase, T_1 , ϕ_{s+} is high and ϕ_{h+} is low, so V_{1+} follows the ascending input signal and keeps the peak value after the input begins to descend because M_1 only allows a current injected from the power supply to charge C_1 . The sampling phase will last until the input signal goes negative to minimize the error due to the phase misalignment of the sampling clocks. V_{2+} is set to the analog ground during this phase.

During the holding phase, T_2 , ϕ_{s+} goes low and ϕ_{h+} goes high, and the peak voltage previously stored in C_1 is transferred to C_2 with the gain of (C_1/C_2) , and then a multiplexer is used to output the envelope signal. At the same time, the voltage across C_1 is reset to zero, ready for the sampling of the next cycle. During T_2 , the channel of V_{in-} does the sampling and has the peak value ready for output. The two channels work in consequence to ensure that the envelop signal is detected continuously. Since the output envelope signal is isolated from the previous stage, theoretically there are no ripples due to the charging/discharging of C_1 . Therefore, C_1 and C_2 can be small for fast settling. Furthermore, the envelope detector can be fully-integrated because large filtering capacitors are not needed even for low-frequency applications.

7.2.2 Experimental Results

Figure 7-7 plots the output signal of the peak detector in response to an amplitude-modulated testing signal, whose fundamental frequency is 1 kHz and whose modulation signal is a 100Hz square wave, showing its ability to track abrupt amplitude change. The peak and valley amplitudes of the testing signal are 700mV and 7mV, respectively. The minimum amplitude is not zero because the envelope detector needs a non-zero

input to generate the control signal. It can be observed that the peak changing of the burst signal is tracked without any ripples due to the charging/discharging of the capacitor as conventional envelope detectors have. The tracking delay contains two parts. The first part is 1/4 of the modulation signal period because the detector needs a complete half cycle to finish the sampling and holding, while the second delay is due to the transition from the previous state to the analog ground, which is approximately 1 μ s.

The peak detector functions well in the frequency below 10 kHz, and the maximum fundamental frequency that can be tracked by this envelope detector is limited majorly by the gain-bandwidth product and the slew rate of the amplifiers. The signals with frequency higher than 10 kHz may result in glitches at the output due to the insufficient response speed of the amplifiers.

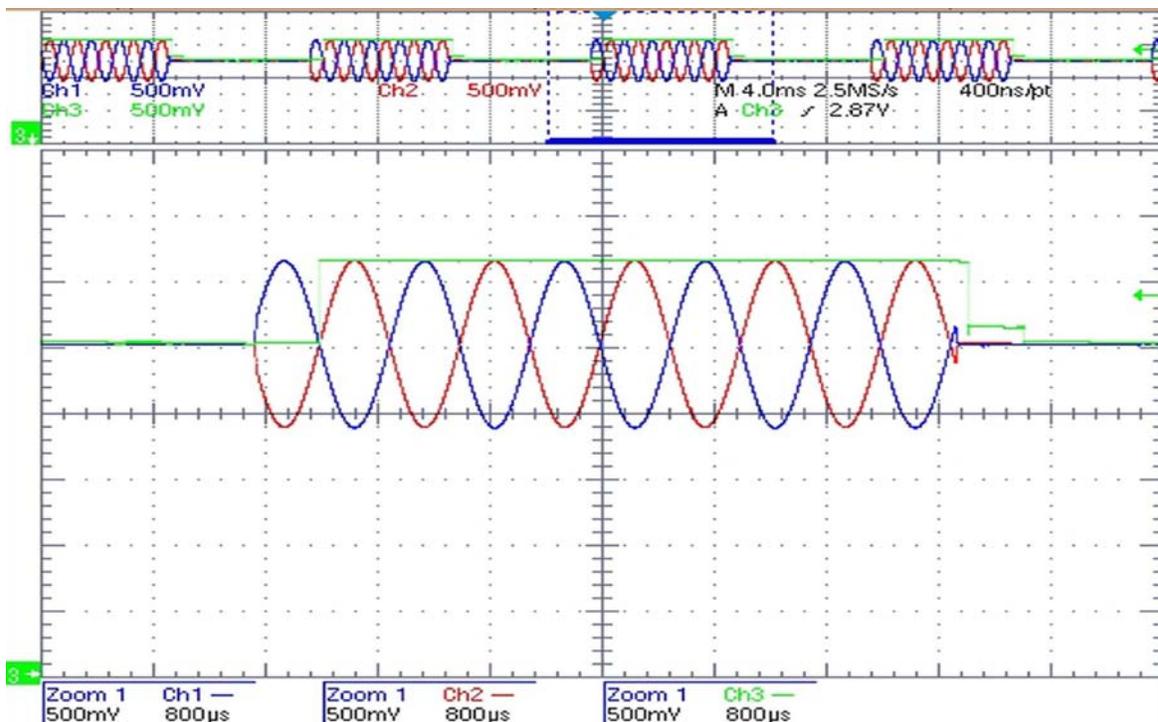


Figure 7-7. Response of the envelope detector to an AM signal.

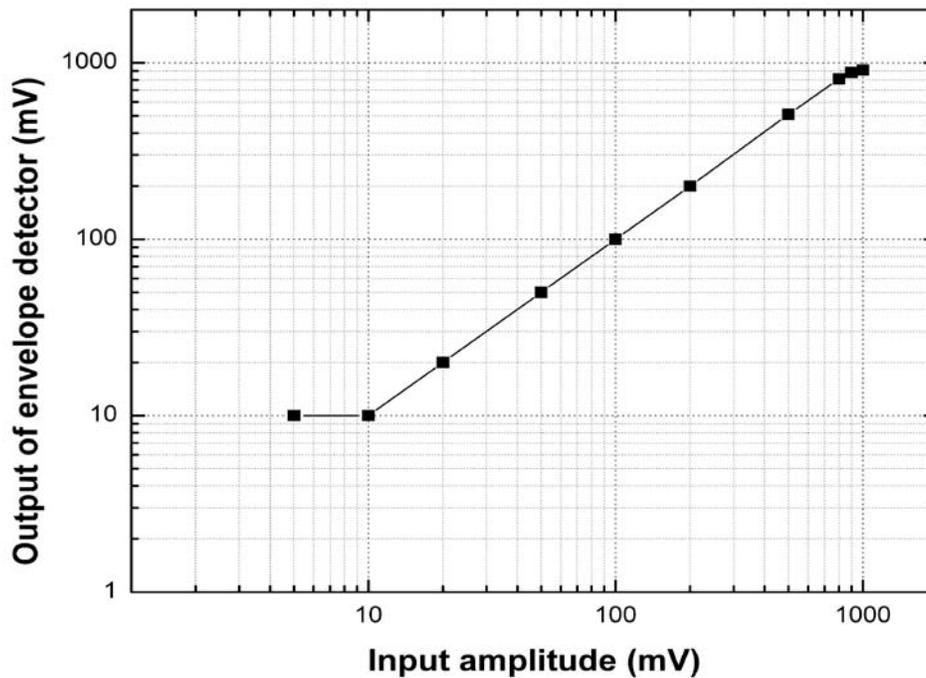


Figure 7-8. Dynamic range of the peak detector.

The measurement result of the dynamic range is shown in Figure 7-8, where the peak detector shows less than 2% nonlinearity when the input amplitude changes from 10 mV to 900 mV, which indicates a 39 dB dynamic range.

7.3 Quadrature Error Compensation

As discussed in Chapter 3, the quadrature error is orthogonal to the driving signal in phase and ideally is eliminated after the synchronous demodulation. However, due to the an extra delay existing in the driving loop, the resonant frequency in the primary mode drifts off the natural frequency, so the contribution of the quadrature error to the zero-rate-output (ZRO) will be nonzero after filtering. Furthermore, the risk exists that the quadrature error affects the dynamic range and the linearity of the interface circuitry severely or even saturates it, because the amplitude of the coupled movement is usually much larger than the Coriolis signal. Therefore, it will be very beneficial to the

performance of the system if the quadrature error can be cancelled automatically by an electrostatic force that counters the quadrature error. Figure 7-9 shows a proposed block diagram to cancel the quadrature error automatically. Extra comb fingers are used to actuate the proof mass in the sense mode, which makes the gyroscope an actuator, more than a pure accelerometer, in the sense mode. The amplitude of the quadrature error is obtained by demodulating the mixture of the Coriolis signal and all coupled errors from the sense mode with a clock orthogonal to the driving signal. The amplitude information is then used to control the polarity and the amplitude of the signal feedback to actuate the sense mode. Since the quadrature error is cancelled mechanically, the requirements on the dynamic range of the sensing circuits are mitigated.

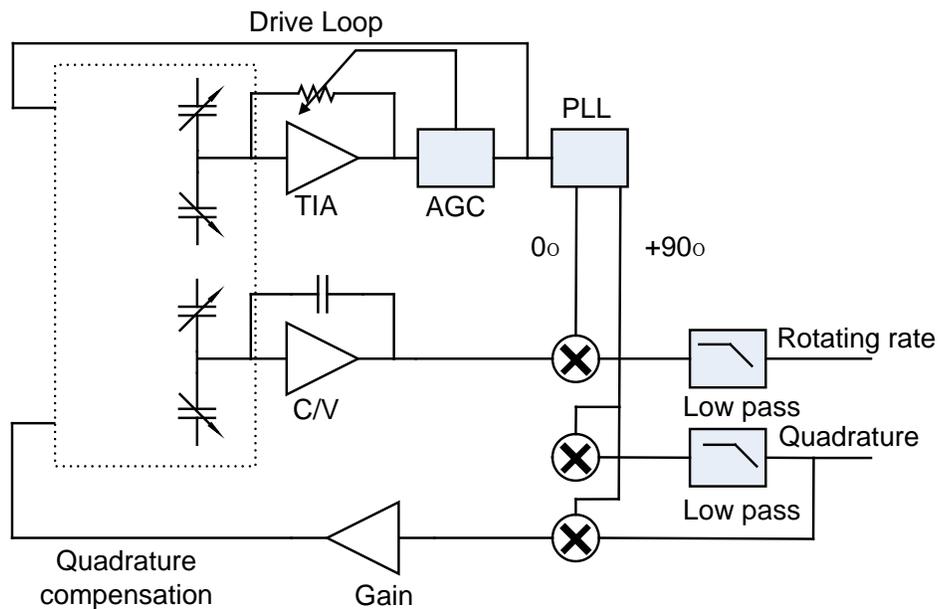


Figure 7-9. Block diagram of automatic quadrature error compensation.

The force feedback loop is modeled mathematically in the block diagram shown in Figure 7-10: The sense mode is modeled as a second-order system, and the signal out of the sensor, which contains both the Coriolis signal and the quadrature error, is

synchronously demodulated by the clock in phase with the quadrature error, in order to eliminate the effects of the Coriolis signal. Then the dc component after a low-pass filter is modulated by the same clock and is amplified with certain gain as the driving signal that actuates the proof mass to cancel the quadrature error.

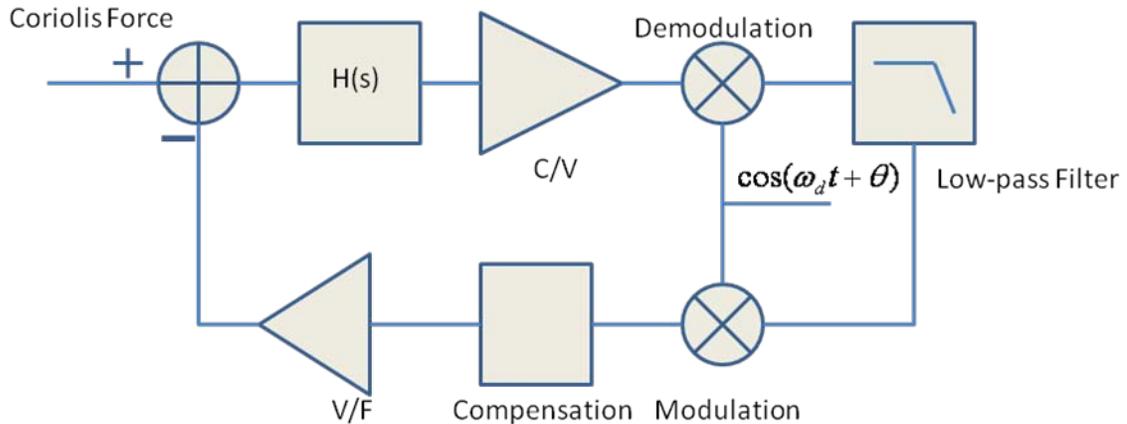


Figure 7-10. Block Diagram of Loop for Quadrature Compensation.

The transfer function of each block is listed as following:

Sensor:

$$H_s(j\omega) = \frac{1}{k_s \sqrt{\left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right]^2 + \left(\frac{\omega}{Q \cdot \omega_0}\right)^2}} \cdot e^{-j\theta},$$

$$\text{where } \theta = \tan^{-1}\left(\frac{\frac{\omega}{\omega_0}}{Q \cdot \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right]}\right) \quad (7-8)$$

Mixer:

$$h_m(t) = \cos(\omega_d t) \quad (7-9)$$

where ω_d is the self-oscillation frequency of the drive mode. So the transfer function in the frequency domain is:

$$H_m(j\omega) = \pi(\delta(\omega - \omega_d) + \delta(\omega + \omega_d)) \quad (7-10)$$

Low-pass filter (1st order):

$$H_{LP}(j\omega) = \frac{1}{1 + j\omega/\omega_p} \quad (7-11)$$

So that the transfer function of the whole loop is then

$$\begin{aligned} H_{loop}(j\omega) &= H_s(j\omega) \otimes H_m(j\omega) \cdot H_{LP}(j\omega) \otimes H_m(j\omega)G \\ &= \pi(H_s(j(\omega - \omega_d)) + H_s(j(\omega + \omega_d))) \cdot H_{LP}(j\omega) \otimes H_m(j\omega) \\ &= \pi^2 G(H_s(j\omega)H_{LP}(j(\omega - \omega_d)) + H_s(j\omega)H_{LP}(j(\omega + \omega_d))) \\ &\quad + \pi^2 G(H_s(j(\omega - 2\omega_d))H_{LP}(j(\omega - \omega_d)) + H_s(j(\omega + 2\omega_d))H_{LP}(j(\omega + \omega_d))) \end{aligned} \quad (7-12)$$

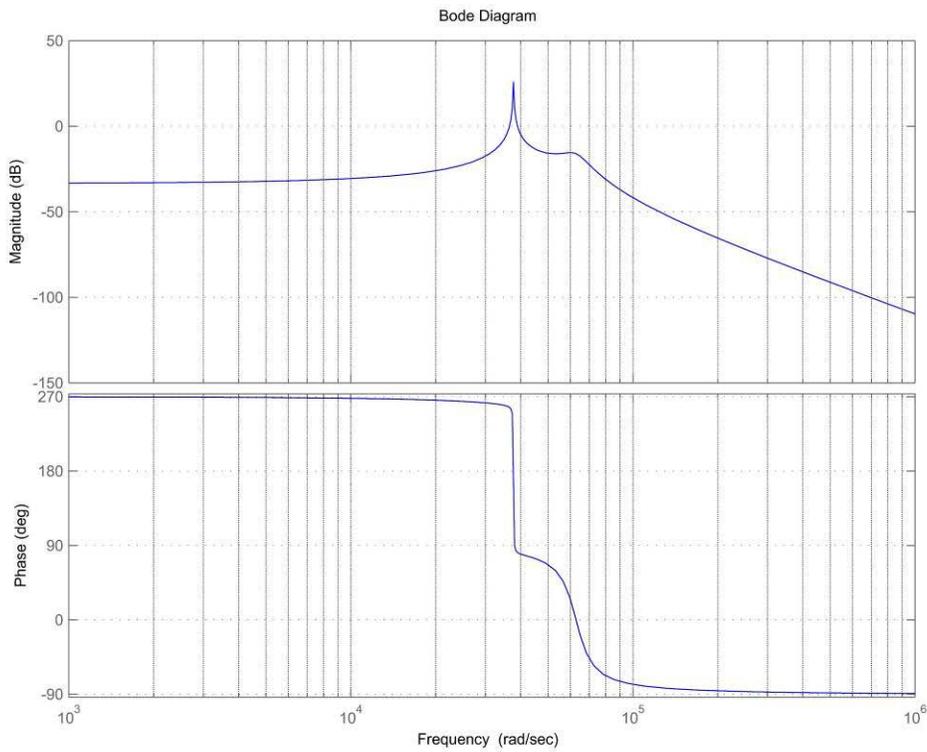


Figure 7-11. Bode diagram of the quadrature compensation loop.

The Bode diagram of the loop looks as drawn in Figure 7-11. Approximately 6 kHz resonant frequency in the driving mode and 10 kHz in the sensing mode are assumed

to plot the diagram. The quality factor of the sense mode is set to 5, and the bandwidth of the low-pass loop filter is 10 Hz. All of the above value is typical for MEMS gyroscopes. Due to the demodulation/modulation process, the pass band of the low-pass loop filter is moved higher to the oscillation frequency of the drive mode as band-pass for the whole loop.

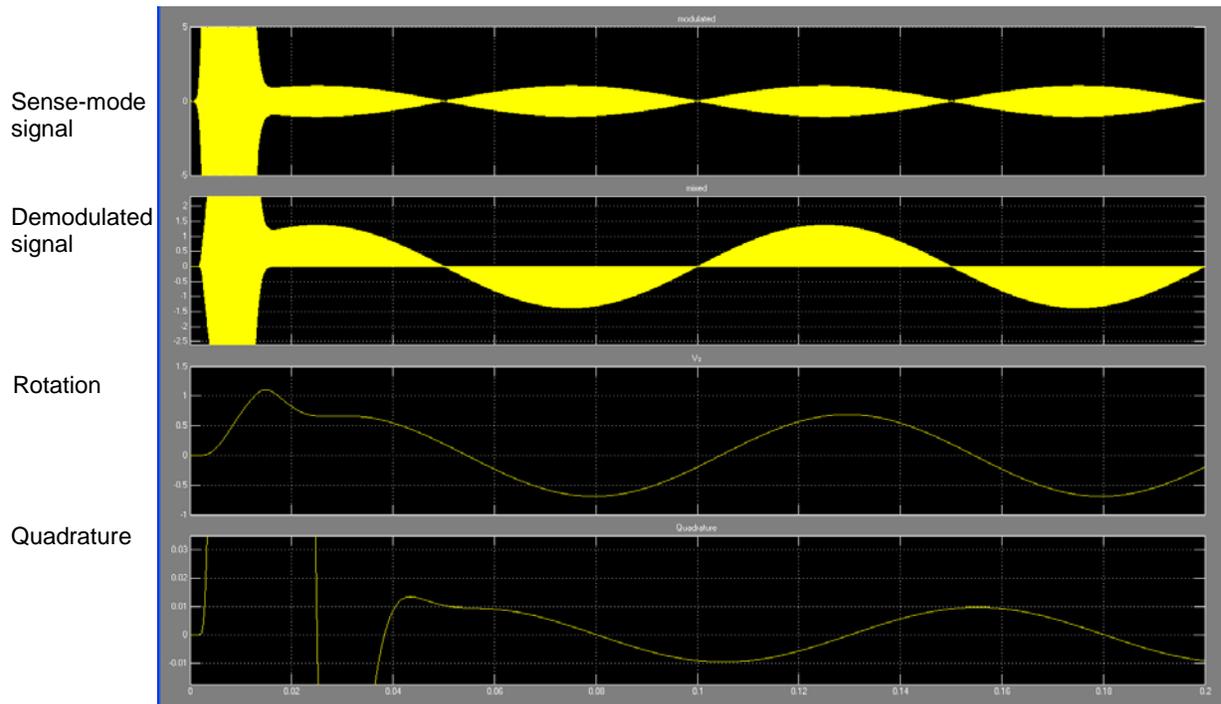
The trade-offs arise among the loop gain, the bandwidth and the stability of the loop. Higher-frequency pole of the loop filter means faster responding speed to quadrature error change and smaller passive components value. Higher loop gain reduces the quadrature error better as well. However, the phase of the loop may drop to zero before the loop gain drops to unity, if the bandwidth of the loop filter is too high or the loop gain is too high. So the gain bandwidth product of the loop should be chosen carefully to avoid instability. Considering the fact that the oscillation in the drive mode is very stable due to the automatic gain control loop, high loop bandwidth is not necessary. Therefore, high dc loop gain and low bandwidth of the loop filter are the best combination in the quadrature cancellation loop. Since the quadrature error is a pure dc signal after the synchronous demodulation and the low-pass filter, an integrator is used as the loop filter, which reduces the pole frequency to zero.

A Matlab Simulink model is built to verify the concept and the simulation results with and without the quadrature error cancellation loop are compared in Figure 7-12(a) and (b). Figure 7-12(a) shows the simulation results of a system with an integrator as low pass filter, and the counterpart without the compensation loop is shown in Figure 7-12(b). It is observed that dc component of the quadrature error after demodulation and low-pass filter has been reduced from 4V to less than 0.1V, when the gyroscope is

subject to 200°/s rotation. The comparison of these two figures indicates that the compensation loop reduces the quadrature error significantly.



(a)



(b)

Figure 7-12. Simulink simulation results of the gyroscope system: (a) without quadrature error cancellation; and (b) with quadrature error cancellation loop.

CHAPTER 8 CONCLUSIONS AND FUTURE WORKS

In this thesis, techniques are demonstrated for the sensing and control electronics design for monolithic CMOS-MEMS inertial sensors, with the focus on low power and low noise. A monolithic inertial measurement unit composed with a three-axis accelerometer, a lateral-axis gyroscope, and a vertical-axis gyroscope has been developed with TSMC/Vanguard 0.35 μm technology, and the electronics has been integrated with the MEMS devices on a single chip and has been characterized.

An improved dual-chopper amplifier is developed for the three-axis accelerometers to achieve low noise and low power consumption. The improvement to the front-end amplifier reduces the temperature coefficient of its gain by replacing the NMOS load with the PMOS counterpart. A three-axis accelerometer with DCA achieves the noise floor of 40 $\mu\text{g}/\sqrt{\text{Hz}}$, 40 $\mu\text{g}/\sqrt{\text{Hz}}$, and 130 $\mu\text{g}/\sqrt{\text{Hz}}$, respectively, with the power consumption of 1mW/axis.

A novel three-axis accelerometer has been demonstrated being integrated with CMOS electronics base on the DCA as a part of the 5-axis inertial measurement unit. The vertical springs for the z axis reduce the cross coupling from the lateral axes. The device achieves the noise floor of 50 $\mu\text{g}/\sqrt{\text{Hz}}$ for x/y axis, and 80 $\mu\text{g}/\sqrt{\text{Hz}}$ for z axis.

A novel differential difference amplifier has been demonstrated in this dissertation as the front-end amplifier for CMOS-MEMS gyroscopes, which have when ultra-small sensing capacitance and ultra-low mechanical sensitivity, in order to realize high gain, low temperature dependence, and low noise. The gain set by the extra capacitive feedback is independent on the sensing capacitance of the device. The advantage of SNR over most of other architectures has been proved theoretically. A 24dB gain is

achieved with the DDA, with the temperature dependence as low as 0.01%/°C. The Coriolis sensing circuit with the DDA as the front end achieves 150nV/√Hz input-referred noise floor.

The control electronics of the primary mode of the CMOS-MEMS gyroscopes have been demonstrated. The transimpedance amplifier with tunable gate voltage converts the displacements of the primary mode to voltage signal with 90° phase leading to compensate the phase change from the driving signal to the displacement, and it ensures that the proof mass oscillate at the natural resonant frequency. 1.8~6.9 MΩ transimpedance is achieved with a long transistor, and the T-network provides another degree of freedom to adjust the impedance. A novel low-ripple fast-settling peak detector has been demonstrated to track the amplitude of the driving signal fast without glitches. 1 μs response time is achieved for the input signals with their frequency up to 10 kHz.

One X/Y-axis gyroscope and one z-axis gyroscope have been demonstrated to be integrated with the electronics on the single standard CMOS chip. The two systems show the sensitivities and noise floors of 1.2mV/°/s and 0.050°/s/√Hz for z-axis, and 1.3mV/°/s and 0.046°/s/√Hz, respectively. The performance of the gyroscope is downgraded by the lack of high on-chip voltage, which limits the oscillation amplitude and the mechanical sensitivity. With the charge pump added in, a noise floor of 0.005°/s/√Hz is achievable.

A prototype Dickson charge pump has been developed with AMI 0.5μm technology to provide high on-chip voltage. 32V high voltage is generated to 10 MΩ load, with 6-stage charge pump and 10 MHz clock frequency. The charge pump has

been proved to be able to provide higher voltage than 14V in the worst case, when the load is increased to 100k Ω due to serious leakage of the capacitors, which is still high enough to start up the oscillation.

The dynamics of the gyroscope is studied theoretically and a method of cancelling the quadrature error is demonstrated in this dissertation. The trade-off between quadrature error reduction and system stability is analyzed theoretically.

One of the suggested works in the future is the study on the system level. The work in this dissertation focuses on low power and low noise of the front-end circuitry and the function of the whole system. A detailed research on the noise related to other parts, including power supply, modulation signal, and the architecture of the system, *etc*, will be beneficial on the performance optimization of the system.

Another suggested work is the implementation of the quadrature error cancellation loop for MEMS gyroscopes. With the quadrature error reduced automatically, the dynamic range of the system can be improved significantly. A phase lock loop (PLL) is suggested being added in to generate the quadrature clock. The loop dynamics needs to be understood thoroughly to reduce the quadrature error while keeping the system stable.

The last but not least, the long-term testing is necessary to investigate the bias stability of the system. Since the gyroscope works in air, the resonant frequency can shift due to the environment variation, such as temperature, pressure, *etc*. The purpose of the long-term testing is to investigate the ability of the control electronics to track the resonant frequency change and to maintain the resonance.

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