CHARACTERIZATION AND RELIABILITY OF ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS

By

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To my loving husband, Kenneth

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Compound semiconductor devices, particularly those based on GaN, have found significant use in military and civilian systems for both microwave and optoelectronic applications. Future uses in ultra-high power radar systems will require the use of GaN transistors operated at very high voltages, currents and temperatures. GaN-based high electron mobility transistors (HEMTs) have proven power handling capability that overshadows all other wide band gap semiconductor devices for high frequency and high-power applications. Little conclusive research has been reported in order to determine the dominating degradation mechanisms of the devices that result in failure under standard operating conditions in the field. Therefore, it is imperative that further reliability testing be carried out to determine the failure mechanisms present in GaN HEMTs in order to improve device performance, and thus further the ability for future technologies to be developed.

In order to obtain a better understanding of the true reliability of AlGaN/GaN HEMTs and determine the MTTF under standard operating conditions, it is crucial to investigate the interaction effects between thermal and electrical degradation. This research spans device characterization, device reliability, and device simulation in order

to obtain an all-encompassing picture of the device physics. Initially, finite element thermal simulations were performed to investigate the effect of device design on self-heating under high power operation. This was then followed by a study of reliability of HEMTs and other tests structures during high power dc operation. Test structures without Schottky contacts showed high stability as compared to HEMTs, indicating that degradation of the gate is the reason for permanent device degradation.

High reverse bias of the gate has been shown to induce the inverse piezoelectric effect, resulting in a sharp increase in gate leakage current due to crack formation. The introduction of elevated temperatures during high reverse gate bias indicated that device failure is due to the breakdown of an unintentional gate oxide. RF stress of AlGaN/GaN HEMTs showed comparable critical voltage breakdown regime as that of similar devices stressed under dc conditions. Though RF device characteristics showed stability up to a drain bias of 20 V, Schottky diode characteristics degraded substantially at all voltages investigated. Results from both dc and RF stress conditions, under several bias regimes, confirm that the primary root for stress induced degradation was due to the Schottky contact.

CHAPTER 1
INTRODUCTION

Motivation

Compound semiconductor devices, particularly those based on GaN, have found significant use in military and civilian systems for both microwave and optoelectronic applications [1-9]. Future uses in ultra-high power radar systems will require the use of GaN transistors operated at very high voltages, currents and temperatures. GaN-based high electron mobility transistors (HEMTs) have proven power handling capability that overshadows all other wide band gap semiconductor devices for high frequency and high-power applications. The unprecedented performance of GaN HEMTs is due to the high breakdown field because of the larger band gap, high electron saturation and overshoot velocities as well as a high electron sheet density [10-13]. Due to the fact that GaN can be grown on silicon carbide with little lattice mismatch, the exceptional thermal conductivity of SiC can be taken advantage of for improved thermal management of the devices as opposed to those grown on Si or sapphire [14]. Though an extremely attractive candidate to replace the present day leading materials for power applications, there is still significant uncertainty with respect to the reliability of GaN HEMTs while under high power operation.

Numerous accelerated stress tests have already been performed on AlGaN/GaN HEMTs, with a mean time to failure (MTTF) often exceeding 10^6 hours at 200°C [14-17]. However, the main focus of previous research to determine MTTF has employed the use of temperature-accelerated tests. Little conclusive research has been reported in order to determine the dominating degradation mechanisms of the devices that result in failure under standard operating conditions in the field. Therefore, it is imperative that

further reliability testing be carried out to determine the failure mechanisms present in GaN HEMTs in order to improve device performance, and thus further the ability for future technologies to be developed.

Objectives of Research

The purpose of this research is to understand the driving degradation mechanisms in AlGaN/GaN HEMTs under electrical and thermal stress conditions. Under certain stress conditions, thermally driven degradation mechanisms can mask other mechanisms. In order to obtain a better understanding of the true reliability of AlGaN/GaN HEMTs and determine the MTTF under standard operating conditions, it is crucial to isolate these degradation mechanisms. The interaction effects between thermal and electrical degradation will then be investigated. This research spans device characterization, device reliability, and device simulation in order to obtain an all-encompassing picture of the device physics.

Dissertation Outline

The main focus of this work is to ascertain the degradation mechanisms limiting lifetime and performance for GaN based HEMTs. The properties of GaN and the background of previously determined degradation mechanisms are reviewed in Chapter 2. Thermal effects on AlGaN/GaN HEMTs will be covered in Chapters 3 through 5, with the effect of device design on self-heating is presented in Chapter 3. Chapter 4 shows the experimental results of high power dc operation on self-heating and degradation. Chapter 5 presents the interacting effects of temperature on high electric field stress for AlGaN/GaN HEMTs with unintentional gate oxides. The effect of bias and gate length under RF operation is discussed in Chapter 6.

CHAPTER 2
BACKGROUND

Properties of GaN and AlN

Though the first reported GaN light emitting diode (LED) was fabricated by Pankove et al. in 1971 [18], the first n-GaN/AlGaN transistor was not demonstrated until 1993 [19]. The delay was due in large part to the inability to develop high quality heteroepitaxial films resulting from lattice mismatched substrates. The incorporation of AlN and GaN nucleation layers produced epitaxial films with lower defect densities and better surface morphology. The need for increased speed in computation, high power communications spanning from RF to millimeter wave, and space borne applications such as satellite links, has transcended the capability of Si based devices as well as many compound semiconductor devices, such as GaAs and InP. Though GaN based devices are relatively new, there are numerous material properties that have made GaN an attractive material choice for high power, high temperature applications, including a large band gap (3.4 eV), large breakdown fields (~$5x10^6$ V cm^{-1}), great electron transport properties (electron mobility in excess of 2000 cm^2 V^{-1} s^{-1}), peak electron velocity close to 3 x 10^7 cm s^{-1}, and high thermal stability shown in Table 2-1 [10-13, 20].

Gallium Nitride can be grown with either a wurtzite or zinc blende structure, though wurtzite is typically the preferred crystal structure for semiconductor electronics. GaN, grown in the c-direction, can be either terminated with Ga or N. The direction of the spontaneous polarization is dependent upon termination (Figure 2-1).

Device Physics

Ohmic Contacts

In order to supply current with minimal voltage drop to a device, metal-semiconductor contacts that do not limit current flow are necessary. These contacts are ohmic contacts, due to the fact that their current-voltage response obeys Ohm's Law (Figure 2-2). An ohmic contact has small junction resistance with respect to the resistance of the device. The most important characteristic that limits performance of ohmic contacts is the specific contact resistance, ρ_C.

$$\rho_C \equiv \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0}, \tag{2-1}$$

where $\partial J/\partial V$ is the rate of change of current density with voltage through the interface of a contact. As the specific contact resistance increases, the localized heating at the contact increases due to increased dissipated power, which can significantly diminish device performance.

Fabricating high quality ohmic contacts to wide band gap semiconductors can be particularly difficult since there are few metals that have a low enough work function to generate a low barrier at the interface. In order to attain low specific contact resistance, one can either highly dope the contact region (typically through ion implantation) or employ the use of a thin layer of a small band gap material. For high doping levels, tunneling is dominated by thermionic field emission (TFE) and

$$\rho_C = \exp\left(\frac{2\sqrt{\varepsilon_s m^* \phi_B}}{\hbar\sqrt{N_D}}\right), \tag{2-2}$$

where m^* is the effective mass, φ_B is the barrier height, $\hbar$ is plank's constant, and N_D is the doping concentration (n-type). The specific contact resistance for low to moderate doping levels can be expressed by

$$\rho_C = \frac{k}{A^{**}Tq}\exp\left(\frac{q\phi_B}{kT}\right), \quad (2\text{-}3)$$

where k is Boltzmann's constant, A^{**} is Richardson's constant, T is temperature, and q is the electronic charge. The specific contact resistance is a function of the doping concentration and barrier height for both TFE and field emission (FE) mechanisms, with thermionic emission (TE) and TFE being much more dependent on temperature.

Schottky Contacts

Metal-semiconductor junctions can form rectifying, or Schottky, contacts in which no current flows until a certain voltage is achieved. Once this voltage is reached under forward bias, conduction occurs, whereas current flow only occurs at breakdown under reverse bias. This rectifying junction is possible when the work function of the metal ($q\phi_m$) is larger than the semiconductor ($q\phi_n$, for n-type). As the most energetic electrons tunnel through the barrier to the metal contact to attain lower empty energy levels, they leave behind positive space charge in a "depletion region" of width, W_D. This ultimately results in a built-in potential (V_0) and electric field (E_0) at the interface between the metal and the semiconductor, with the depletion width

$$W_D = \sqrt{\frac{2\varepsilon_s}{qN_D}\left(V_0 - V - \frac{kT}{q}\right)}, \quad (2\text{-}4)$$

where ε_s is the permittivity of the semiconductor and V is the applied voltage. The barrier that forms at the interface of the metal and the semiconductor, the Schottky barrier height, can be expressed as (for a n-type semiconductor),

$$q\phi_B = q(\phi_n - \chi), \quad (2\text{-}5)$$

where $q\chi$ is the electron affinity.

Experimental determination of the work function for metals is extremely sensitive and can be affected by surface contamination, interface layers, and image-force

lowering, causing it to deviate from the ideal condition. When a metal is deposited on a semiconductor, it can be assumed that there will be interface states that form. The interface states are an intrinsic property of the semiconductor and are independent of the type of metal contact. It can also be assumed that there will be a thin interfacial layer that will form. If the processing is done correctly (i.e. the surface is properly cleaned prior to metal deposition), then this interfacial layer should only be a few angstroms thick, thus allowing electrons to easily tunnel through the barrier. For all semiconductors, a general model for the Schottky barrier height can be expressed as

$$q\phi_B = q(SX_m + \phi_0), \tag{2-6}$$

where the interface index is $S = \frac{d\phi_{Bn0}}{dX_M}$, X_M is the electronegativity of the metal, and ϕ_0 is the contribution of surface states from the semiconductor. For ionic semiconductors, such as GaN, S approaches 1 and thus this class of semiconductors exhibit a strong dependence of barrier height on the metal. This is due to the Pauling electronegativity difference between the cation and the anion of the semiconductor, which is 1.4 for GaN.

There are three categories in which current tunneling can take place: thermionic emission (TE), field emission (FE) and thermionic-field emission (TFE) which falls in between TE and FE (Figure 2-3). Neglecting series and shunt resistance, the thermionic Schottky barrier height is expressed by

$$J = J_s\left[\exp\left(\frac{qV}{kT}\right) - 1\right] = A^{**}T^2\exp\left(-\frac{q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{2-7}$$

where J_s is the saturation current density. The barrier height, in an actual device, is dependent on the bias voltage can be more accurately described by

$$J = A^{**}T^2\exp\left(-\frac{q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{2-8}$$

where n is the ideality factor. Since a Schottky contact is likely to be non-uniform, the ideality factor incorporates all of the unknown effects that make the contact deviate from the ideal case. For example, if the barrier height has non-uniformity over the entire contact area, this will lead to n > 1.

Spontaneous and Piezoelectric Polarization

High electron mobility transistors are possible in III-V nitrides because of the spontaneous polarization and piezoelectric polarization that are present. Spontaneous polarization is an intrinsic property that is due to the nature of the bonds in the material. The non-symmetric formation of negative charges from the electrons with respect to the positive nucleus results in an ionic nature in which spontaneous polarization occurs. Most semiconductors do not show this because the cubic crystal structure and sp^3 hybridization results in a balance of bonds and charges. Due to the non-symmetric wurtzite structure, the spontaneous polarization is along the [0001] axis. The spontaneous polarization in AlGaN is dependent upon the Al content and can be calculated by:

$$P^{sp}_{Al_xGa_{1-x}N}(x) = [-0.090x - 0.034(1-x) + 0.019x(1-x)]\ cm^{-2} \quad (2\text{-}9)$$

Strained heterostructures in materials with no inversion symmetry can also give rise to piezoelectric polarization. For AlGaN/GaN heterostructures, this is due to the large lattice mismatch between AlGaN and GaN. The piezoelectric polarization in strained AlGaN on GaN can be calculated by:

$$P^{pz}_{Al_xGa_{1-x}N}(x) = [-0.0525x - 0.0282x(1-x)]\ cm^{-2} \quad (2\text{-}10)$$

Due to the large piezoelectric response in AlGaN with high Al fractions, it is more accurate to derive the electrical and mechanical components using electromechanical

coupling from the Legendre transform to obtain the total internal energy density per unit volume from the electric enthalpy H,

$$H = U - \boldsymbol{E} * \boldsymbol{D}, \tag{2-11}$$

where **E** and **D** are the electric field and electric displacement, respectively [21]. U is the total internal energy, including both strain and electrostatic energy, in which

$$U = \frac{1}{2} c_{ijkl} S_{ij} S_{kl} - \frac{1}{2} \varepsilon_{ij} E_i E_j, \tag{2-12}$$

where C_{ijkl} is the fourth-ranked elastic stiffness tensor, **S** is the strain tensor, ε_{ij} is the electric permittivity tensor [21]. Spontaneous polarization for piezoelectric materials for electric displacement is given by

$$D_i = e_{ijk} S_{jk} + \varepsilon_{ij} E_j + D_{0i}, \tag{2-13}$$

where e_{ijk} is the piezoelectric coefficient tensor and D_{0i} is the effect of the spontaneous polarization [21-24]. Additionally, the temperature dependence on D_{0i} results in a pyroelectric behavior. Due to the sixfold rotational symmetry of wurtzite materials, D_{0i} exists only along the [0001] direction [22-24]. Substituting into 2-11 results in the electric enthalpy for the system

$$H = \frac{1}{2} c_{ijkl} S_{ij} S_{kl} - e_{ijk} E_i S_{jk} - \frac{1}{2} \varepsilon_{ij} E_i E_j - E_i D_{0i}. \tag{2-14}$$

Piezoelectric semiconductors present an interesting material system for study. The movement of charges can interact with mechanical fields within the material, which results in the acoustoelectric effect. Applying a dc electric field to the semiconductor can actually amplify this traveling acoustic wave [21]. This effect has been exploited in semiconductors for a range of devices, such as interdigital transducers.

Gauss's law, conservation of charge, and the equations of motion for small signals provides the equations that govern the basic behavior of piezoelectric semiconductors,

$$D_{i,i} = qn, \tag{2-15}$$

$$q\dot{n} + J_{i,i} = 0, \tag{2-16}$$

$$T_{ji,j} = \rho\ddot{u}_{\iota}. \tag{2-17}$$

where J is the steady state current and can be expressed by,

$$\bar{J}_i = q\bar{n}\mu_{ij}\bar{E}_j \tag{2-18}$$

and where q is the carrier charge, n is the carrier density, T is the stress tensor, ρ is the mass density, and u is the mechanical displacement [21]. The response of the semiconductor to external forces can be described by:

$$T_{ij} = c_{ijkl}S_{kl} - e_{kij}E_k, \tag{2-19}$$

$$D_i = e_{ijk}S_{jk} + \varepsilon_{ij}E_j, \tag{2-20}$$

$$J_i = q\bar{n}\mu_{ij}\varphi_{ij} + qn\mu_{ij}\bar{E}_j - qd_{ij}n_j, \tag{2-21}$$

where d_{ij} is the carrier diffusion constant. Equations 2-17 to 2-19 can be rewritten in terms of electric potential (φ), carrier density, and mechanical displacement [21].

$$c_{ijkl}u_{k,lj} + e_{kij}\varphi_{kj} + f_i = \rho\ddot{u}_{\iota} \tag{2-22}$$

$$e_{ikl}u_{k,li} - \varepsilon_{kij}\varphi_{ij} = qn \tag{2-23}$$

$$\dot{n} - \bar{n}\mu_{ij}\varphi_{ij} + \mu_{ij}\bar{E}_j n_i - d_{ij}n_{ij} = 0 \tag{2-24}$$

High Electron Mobility Transistors

The addition of the spontaneous polarization in III-V nitrides, which is not present in other III-V materials, such as GaAs and InP, allows for much larger 2DEG formation (up to ten times larger than GaAs) without additional doping, Figure 2-4 [25]. A

heterojunction of III-V nitrides, such as AlGaN and GaN, will have a net fixed polar charge at the interface due to the two materials having different polarization values. This results in a net electric field induced at the surface of the heterojunction. A relatively thin $Al_xGa_{1-x}N$ layer, typically less than 40 nm with an Al content of x < 0.4, grown on top of a thick GaN buffer layer will be under tensile stress and thus result in the formation of the 2DEG at the interface. The ability to create a high density 2DEG without doping results in higher mobility since there is no scattering of electrons on dopants. The carrier density is a function of Al content in AlGaN as well as the applied gate voltage (V_{GS}) and can be expressed by:

$$n_s(x) = \frac{\sigma_{\frac{AlGaN}{GaN}}(x)}{q} - \frac{\epsilon_0 E_F}{q^2}\left[\frac{\epsilon_{AlGaN}(x)}{t_{AlGaN}} + \frac{\epsilon_{GaN}}{t_{GaN}}\right] -$$

$$\frac{\epsilon_0 \epsilon_{AlGaN}(x)}{q^2 t_{AlGaN}}[q(\phi_{AlGaN}(x) - V_{GS}) + \Delta(x) - \Delta E^c_{AlGaN}(x)] \quad (2\text{-}25)$$

GaN Degradation Mechanisms

Hot-carriers and Trap Generation

Permanent device degradation after high V_{DG} stress under on-state conditions has been attributed to the presence of hot electrons. In GaAs- based devices, hot electrons generate holes which are accumulated by the gate and result in a negative shift in V_T [14, 26]. Typically, I_G is used to derive the field-acceleration laws for failure. Impact ionization, however, is negligible in GaN HEMTs. This is due to the fact that tunneling injection dominates gate current, preventing gate current from being used as an indicator for hot electron degradation [14]. However, these hot electrons likely lead to trap generation at the AlGaN/GaN interface and/or at the passivation GaN cap interface. As in GaAs and InP based HEMTs, traps lead to an increase in the depletion region

between the gate and the drain, ultimately resulting in an increase in drain resistance and subsequently a decrease in I_{DSS}. Comparatively, under off-state conditions the degradation is greatly reduced due to the reduction of electrons present in the channel. Sozza et al. showed that GaN/AlGaN/GaN HEMTs that underwent a 3000 hour on-state stress resulted in an increase in surface traps with an activation energy of about 0.55 eV [14, 27]. On the other hand, devices stressed under off-state conditions saw a very small increase in traps.

Meneghesso et al. have employed the use of electroluminescence (EL) to study the effect of hot-carriers and its dependence on stress conditions [14]. Uniform EL emission was observed along the channel for devices stressed at V_{GS} = 0 V and V_{DS} = 20 V, which is due to hot electrons. However, there is no presence of hot spots or current crowding. On the other hand, under OFF state conditions with V_{GS} = -6 V and V_{DS} = 20 V (resulting in a V_{GD} = -26 V), the EL emission from the channel is not uniform. These hot spots may be due to injection of electrons from the gate into the channel. Due to the high bias conditions, the electrons acquire enough energy to give rise to photon emission.

Contact Degradation

Contact degradation and gate sinking are significant degradation mechanisms at elevated temperatures in GaAs and InP based HEMTs. This has not yet proven to be a significant issue with AlGaN/GaN HEMTs at temperatures below 400°C for Pt/Au Schottky contacts and Ti/Al/Pt/Au annealed ohmic contacts [14]. An increase in Schottky barrier height was observed for Ni/Au Schottky contacts after dc stress at elevated junction temperatures (200°C) [14, 15]. This was due to a consumption of an interfacial layer between the Schottky contact and the AlGaN layer. Though the

resulting positive shift in the Schottky barrier height, and thus the pinch-off voltage, is ideal, the subsequent change in I_{DSS} is not favorable. Unstressed devices were subjected to an anneal after the Schottky contact was deposited in order to decrease the interfacial layer between the gate and semiconductor. Devices that underwent the gate anneal showed 50% less degradation during a 24 hours stress test as opposed to devices that did not receive a gate anneal [14]. Thermal storage tests up to 2000 hours on Ti/Al/Ni/Au ohmic contacts at and above 290°C showed an increase in contact resistance as well as surface roughness due to growth of Au-rich grains that ultimately led to cracks in passivation [28]. The two primary degradation mechanisms were determined to be Au inter-diffusion within the metal layers and Ga out-diffusion from the semiconductor into the metallic compounds. Similar degradation was observed after dc stress tests that resulted in junction temperatures equivalent to the thermal storage tests. Due to the high power capability of AlGaN/GaN HEMTs, proper temperature management is crucial in order to optimize device performance under high current and high voltage operation. Self heating of devices can ultimately result in poor device performance through contact degradation. As shown above, reliability of contacts is highly dependent upon both metal schemes as well as processing during fabrication.

Inverse Piezoelectric Effect

Several research groups have shown that high reverse bias on the gate results in a defect generated path of gate current leakage [29-33]. It has been determined that this defect formation mechanism is a result of the inverse piezoelectric effect. Due to the fact that GaN and AlGaN are intrinsically piezoelectric materials, the presence of high electric fields will result in an increase in stress within the GaN and AlGaN layers. AlGaN is lattice mismatched to GaN, resulting in significant tensile strain, even in the

absence of an electric field. If under electric stress the elastic energy within the AlGaN/GaN layers surpasses a critical value, the strained layer will relax through crystallographic defect formation. It is possible that the defects could be electrically active and result in device degradation [30].

J. Joh et al. have established that I_D and I_G degradation under high reverse gate bias occurs at a critical voltage, typically above 20 V on V_{DG} [31]. This is also correlated with a sharp rise in both source and drain resistance as well as a positive shift in V_T. However, the critical voltage for devices can deviate substantially within one wafer, though adjoining devices appear to exhibit similar performance. This broad distribution of critical voltage, ranging from V_{DG} of ~15 V to ~30 V, has been attributed to slow changes within the substrate or epilayer growth over the wafer [28, 31]. As mentioned above, hot electrons are generated exponentially as the field increases and only linearly with current [30, 34]. Though stress experiments in the high power state have shown that increasing $I_{Dstress}$ does not significantly accelerate degradation, it was found that the critical voltage for reverse bias stress in which I_{Goff} dramatically increases is dependent upon the $I_{Dstress}$, as V_{crit} increases with increasing $I_{Dstress}$ [30]. It is evident from this result that hot electrons are not the driving degradation mechanism for this stress condition. In order to verify the inverse piezoelectric effect, TEM cross sections were studied by Chowdhury et al. after stressing with V_{DS} = 40 V and I_{D0} = 250 mA/mm at various base-plate temperatures, which corresponded to a junction temperature of 250 °C, 285 °C, and 320 °C based on device modeling [29]. Unstressed devices showed no evidence of pits or cracks near the edge of the Schottky contact. However, all stressed devices showed evidence of pit-like defects on the drain side of the gate. The depth of the pit

was about 10nm, and remained within the AlGaN layer. Crack-like defects were observed in a few of the stressed devices, and appeared to originate at the bottom of the pit defect, extending to the heterointerface of the AlGaN/GaN layer and occasionally into the GaN buffer. As the junction temperature increased, the time after which the crack appeared decreased, developing within 6 hours at a temperature of 320°C. Gate metal was also observed to diffuse ~2nm into the defect crack. The formation of the crack was hypothesized by Chowdhury et al. to originate in the deepest points in the defect pit and spread along the gate width, thus explaining the presence of cracks in very shallow defect pits [29].

Del Alamo et al. have postulated that the inverse piezoelectric effect is solely an electric field driven degradation mechanism due to the fact that it is the induced mechanical stress that results in the relaxation of the AlGaN layer [30]. It has also been hypothesized by the del Alamo group that current should not drive this mechanism, except for indirect self heating that would accelerate degradation of the device. Device design that affects the profile of the electric field on the drain side of the gate will also, in turn, impact the critical voltage [30].

Sarua et al. have investigated the effect of piezoelectric strain in AlGaN/GaN FETs under bias with micro-raman spectroscopy [33]. Devices implemented 30 nm of $Al_{0.25}Ga_{0.75}N$ on 1.2 µm of undoped, insulating GaN on insulating 4H-SiC with 2x50 µm (source-drain gap = 4.8 µm, gate length = 1.2 µm). It was confirmed with 2D finite element simulations that a pinched-off device at V_{DS} = 20 V results in a peak electric field on the drain side of the gate within the AlGaN layer. However, the z component of the electric field extended down into the GaN layer [33]. Fe doping of the GaN buffer

layer is often used in order to improve the control of short-channel effects in HFETs [35]. It was later shown by Sarua et al. that Fe doped GaN, which raises the acceptor concentration and decreases the depletion width in the GaN buffer, confines the z component of the electric field to the AlGaN/GaN interface [36]. Self-heating will occur under high power stress conditions, which results in a compressive thermal strain/stress. It is possible that due to the mitigation of the piezoelectric stress by the thermal stress, slower device degradation was seen in devices stressed under the high power state as opposed to off-state condition. This is in contrast to the hypothesis of del Alamo et al. that higher temperatures will result in an acceleration of device degradation.

Other issues can lead to additional compressive and tensile strains on the underlying epitaxial layers, including SiN passivation, which is used extensively to minimize surface traps on the AlGaN surface. Mastro et al. reported the simulated effects of non-uniform strain due to SiN passivation [37]. Typically, SiN has a relatively small magnitude of stress as compared to the tensile strain present in the AlGaN layer due to lattice mismatch. The strain in SiN is highly dependent on processing conditions, i.e. thickness, frequency of the plasma during PECVD, pressure, and temperature. When deposited on the device, variations and discontinuities can increase the stress fields. For instance, the opening at the edge of the gate metal will result in a force on the AlGaN which will be perpendicular to the gate edge and parallel to the surface of the AlGaN [37]. It was predicted by Mastro et al. that as the gate length decreases, the magnitude of the strain fields increases. This effect on gate length is of great importance due to the desire to continuously scale down the dimensions of the devices.

Characterization Techniques

Electrical Measurements

Transfer length method

As described above, an extremely important parameter to optimize for device performance is specific contact resistance. It is also imperative to monitor specific contact resistance in order to understand device behavior throughout electrical and thermal stress. The transfer length method is employed here in order to determine contact resistance.

The transfer length method is preferred for the studies to be performed due to the fact that it does not require the bulk resistivity of the semiconductor or the sheet resistance (R_{sh}) to be known prior to measurement, both of which can change during stress. For this method, numerous identical ohmic contacts are made to the semiconductor with increasing spaces, d, between the contacts. A bias is applied to the contacts in order to induce a current, which is subjected to ρ_c and R_{sh}. Below the contact, a potential distribution occurs as due to ρ_c and R_{sh}.

$$V(x) = \frac{I\sqrt{R_{sh}\rho_c}}{Z}\frac{\cosh\left[\frac{L-x}{L_T}\right]}{\sinh\left(\frac{L}{L_T}\right)}, \tag{2-26}$$

where L is the contact length, Z is the contact width, L_T is the transfer length, and I is the current flowing into the ohmic contact. The transfer length,

$$L_T = \sqrt{\rho_c / R_{SH}}, \tag{2-27}$$

is the distance over which the majority of the current transfers from the semiconductor to the metal contact. The total resistance measured between the ohmic contacts is then plotted against the spacing of the contacts. From this graph, one can extract several

parameters about the material and the contacts. The slope of the plot, $\Delta(R_T)/\Delta(d)$, is the sheet resistance divided by the contact width, R_{SH}/Z. The point at which the slope intercepts at $d = 0$ is $R_T = 2R_C$, the contact resistance. The transfer length, L_T, is determined at the intercept when $R_T = 0$, given by $-d = 2L_T$ [38]. Figure 2-5 shows a graphical representation of this method.

Schottky diode characteristics

The barrier height of a Schottky contact can be determined by current-voltage methods. The method used here to calculate the barrier height (ϕ_B) is from extrapolating the semilog of current (I_S) versus voltage (V_{GS}),

$$\phi_B = \frac{kT}{q} \ln \left(\frac{AA^* T^2}{I_s}\right). \quad (2\text{-}28)$$

The barrier height is determined at zero bias. At high biases, the current will deviate from linear due to series resistance. The ideality factor, n, can be defined by

$$\frac{1}{n} = 1 - \frac{\partial \phi_B}{\partial V} \quad (2\text{-}29)$$

Thermionic-field emission, interfacial layers and interfacial damage can cause the ideality factor to deviate from 1 [38].

Scanning Electron Microscopy

In order to obtain high magnification and resolution of samples, it can be beneficial to use scanning electron microscopy (SEM). Due to the fact that the electron wavelengths are much smaller than photon wavelengths, it is possible to achieve larger magnifications. An SEM produces an image by scanning the sample with a focused electron beam. This incident electron beam results in either secondary or backscattered electrons. These electrons that are emitted from the sample are attracted and collected by a detector, which then converts it into an image. The incident electron beam is

formed from electrons that are emitted from an electron gun. These electrons pass through numerous magnetic lenses which focus the electron beam. The energy of the electrons can range from 10-30 keV, though insulating materials may require much lower energies down to several hundred eV. This broad range of energies is necessary in order to prevent charge accumulation of insulating materials, which in turn will result in a distortion of the image [38].

Photoluminescence

Photoluminescence (PL) characterization is performed by irradiating the sample with a light source with a wavelength that is larger than the band gap of the material under study. The incident light generates electron-hole pairs, which then recombine and emit photons with various energies dependent up on the process of recombination. For PL, these processes can range from intraband transition, free exciton, neutral donor and exciton, ionized donor bound exciton, neutral acceptor bound exciton, donor-acceptor pair, Auger transition, phonon emission, etc. Emission of photons, observed as luminescence, occurs during these processes except for non-radiative recombination sites [39].

Cathodoluminescence

Cathodoluminescence (CL) is a technique that employs the use of an electron beam incident on a sample that results in light emission. It is particularly useful for III-V materials due to their high radiative recombination rate. CL data is acquired by typically cooling the sample and collecting the light that is emitted [38]. The emission of light is due to the impinging electron beam exciting an electron into the conduction band, leaving behind a hole in the valence band. When the electron and hole recombine either across the band gap or between the band edge and a deep level, a photon is emitted.

The recombination sites can be from direct band-to-band, dopant-to-band, donor-acceptor, or from defect transitions in the material. Radiative recombination sites in III-V materials are typically extremely high, particularly in GaN, due to high defect densities [40]. An advantage of CL over PL is the ability to vary the penetration depth of the incident electrons by varying the electron energy. The excitation depth of the electrons can be determined using the Everhart and Hoff model in which the electron energy loss per unit is:

$$\frac{\partial E}{\partial s} = -(2\pi N_A e^4)\left(\frac{Z\rho}{A}\right)\left(\frac{1}{E}\right)\ln\left(\frac{aE}{I}\right) \quad (2\text{-}30)$$

where N_A is Avagadro's number, Z is the atomic number, ρ is the density, A is the atomic weight, a=1.166, E is the beam energy, and I is the mean excitation energy. The electrons can reach a maximum range of:

$$R_B = \int_0^{\xi(E_B)} \frac{\xi}{\ln(\xi)}\partial(\xi) \quad (2\text{-}31)$$

where ξ =aE/I.

The CL images and spectra taken in this study are taken by an FEI NanoSEM 430 with a Gatan MonoCL4 attachment by Oxford Instruments, using a 1200 lines/mm grating. All spectra were taken at room temperature.

Electroluminescence

Electroluminescence (EL) is a technique similar to PL and CL in that photon emission is used for characterization of radiative recombination in order to determine trap formation and defect sites. However unlike PL and CL, there is not an incident electron or photon beam that creates electron-hole pairs for recombination. EL is possible when electrical contacts are made to a semiconductor material and a bias is applied. The electrical bias results in electron-hole pair formation, which can in turn lead

to photon emission. This is particularly useful for III-V materials in order to determine regions of a device that have high densities of radiative recombination sites within the active region.

Transmission Electron Microscopy

Transmission electron microscopy (TEM) is similar to SEM in that electrons emitted from an electron gun are accelerated to high voltage (100-400 kV), with a series of lenses collimating and focusing the electron beam. The resolution of a TEM is extremely high, typically ~ 0.08 nm. However, the sample for TEM must be transparent to electrons, from tens to hundreds of nm thick. This sample is placed on a small copper grid. As the electrons pass through the sample, they are scattered and form a diffraction pattern on the back focal plane as well as an image. There are three types of images that can be formed, bright-field, dark-field and high resolution. Bright-field images are formed only with the transmitted electrons. The electrons that are diffracted form the dark-field images. Dark-field images can provide a great deal of information about the materials in the sample, as it is highly dependent on the atomic number of the atoms. Atoms with high atomic numbers scatter much more than atoms with small atomic numbers, often resulting in the transmitted electrons not reaching the screen and thus the material appearing dark on the image.

Table 2-1. Comparison of material properties for multiple semiconductors.

Material Properties	**Si**	**GaAs**	**4H-SiC**	**GaN**
Band gap (eV)	1.12	1.42	3.25	3.40
Breakdown field (MV/cm)	0.25	0.4	3.0	5.0
Thermal Conductivity (W/cmK)	1.5	0.5	4.9	1.3
Dielectric constant	11.8	12.8	9.7	9.0
Electron mobility (cm^2/Vs	1350	6000	800	2000
Maximum velocity (10^7 cm/s)	1.0	2.0	2.0	3.0

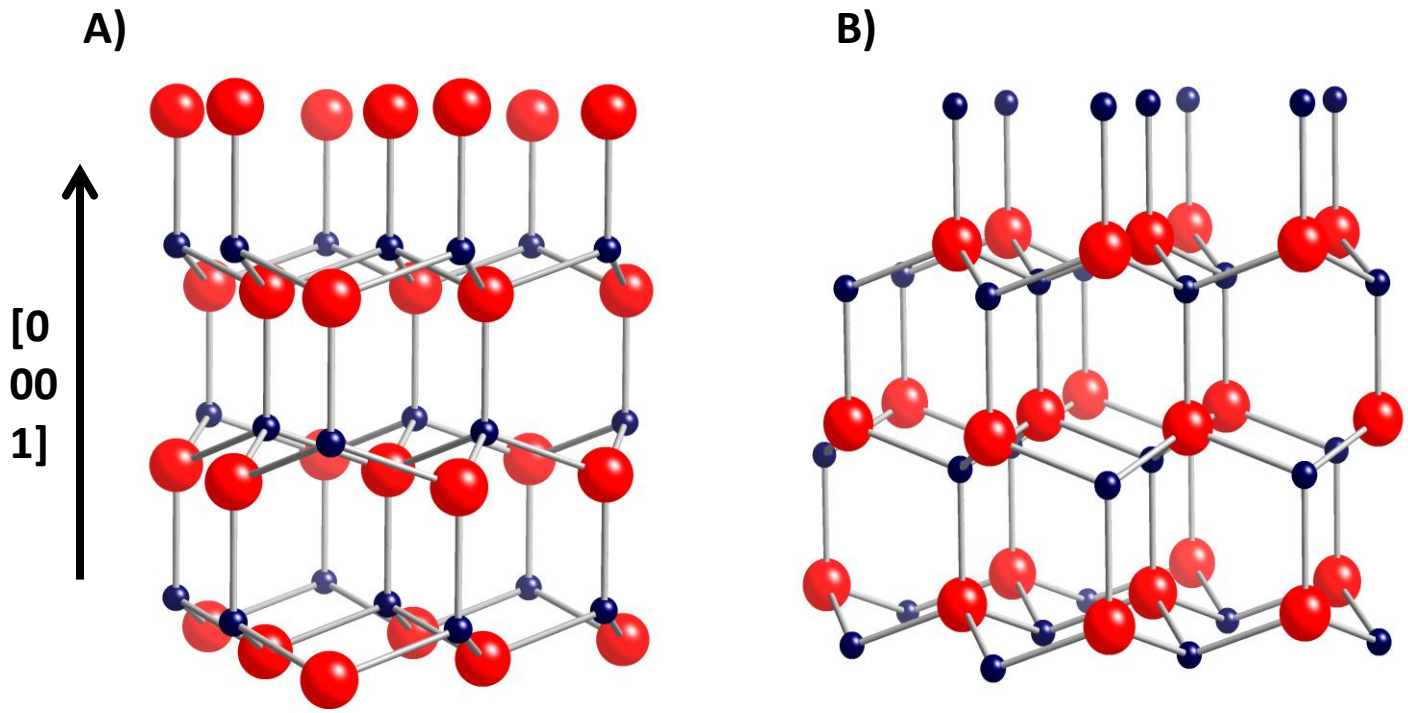

Figure 2-1. Schematic showing the wurtzite structure of GaN. A) Ga terminating and B) N terminating faces which result in opposite polarity. The dipole is induced from the N to the Ga atom. As shown, the [0001] is not equivalent to the [000-1] direction.

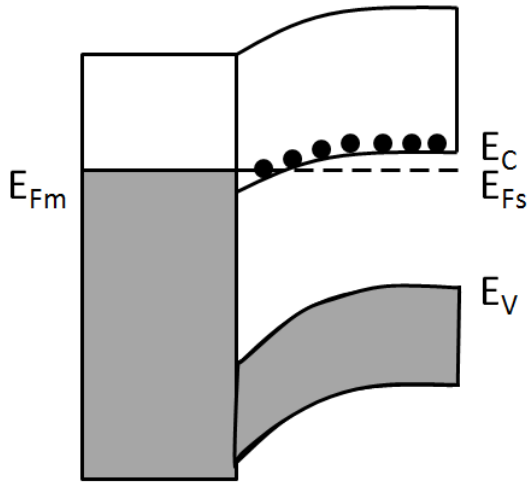

Figure 2-2. Band diagram of an ohmic metal-semiconductor contact with the metal having a smaller work function than the n-type semiconductor.

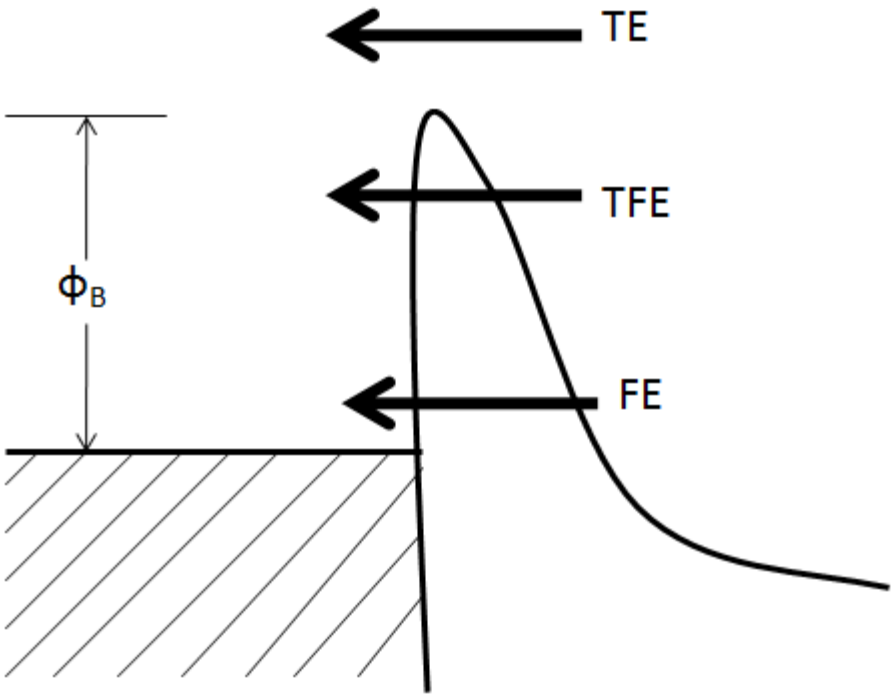

Figure 2-3. Energy- band diagram depicting electron tunneling mechanisms for metal-semiconductor contacts under forward bias. FE = field emission, TFE = thermionic-field emission, TE = thermionic emission.

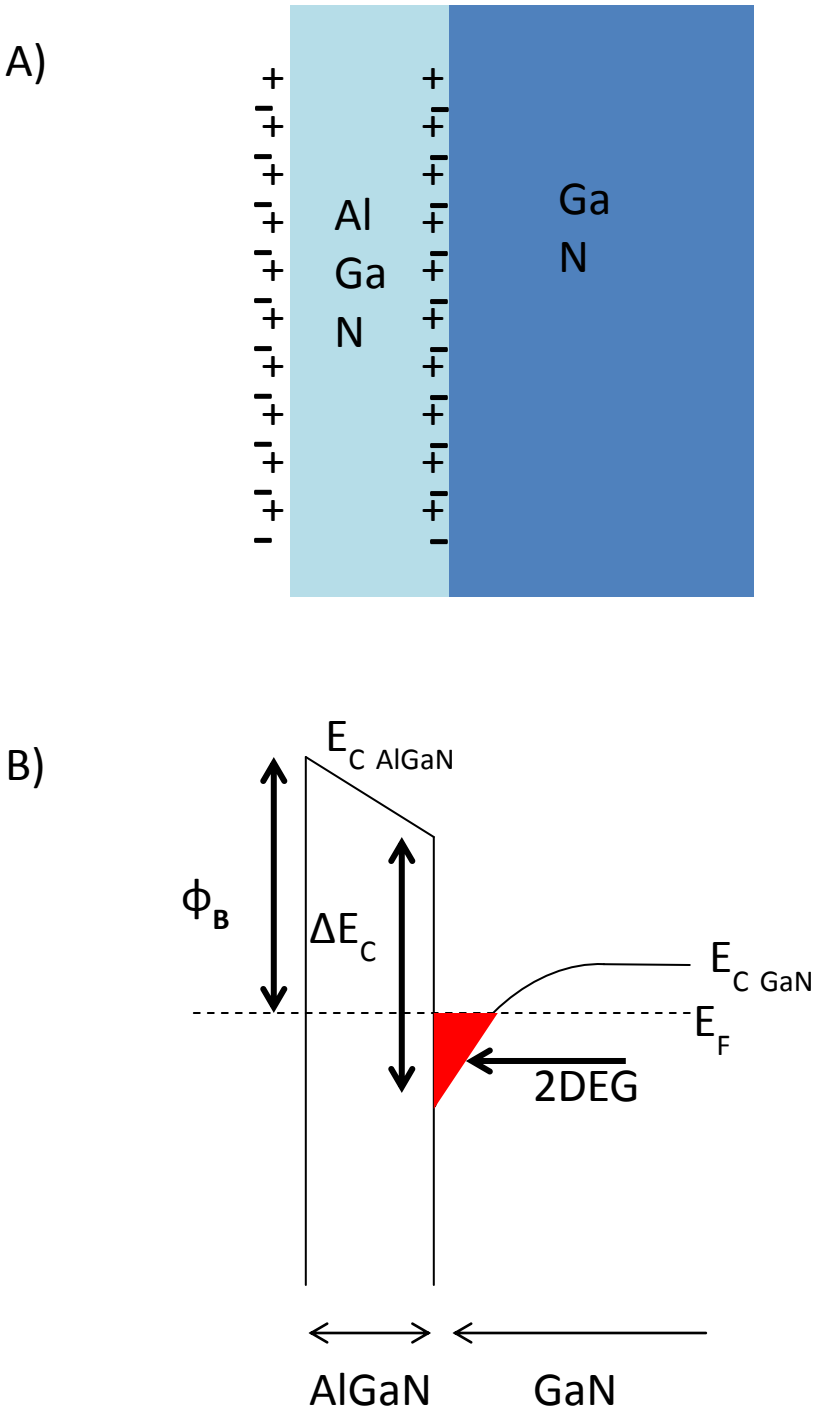

Figure 2-4. Formation of two dimensional electron gas due to spontaneous and piezoelectric polarization. (A) Schematic indicating charges induced at surface and interfaces of tensile AlGaN layer grown on top of GaN. (B) Band diagram of AlGaN/GaN heterostructure with 2DEG induced in GaN (shown in red).

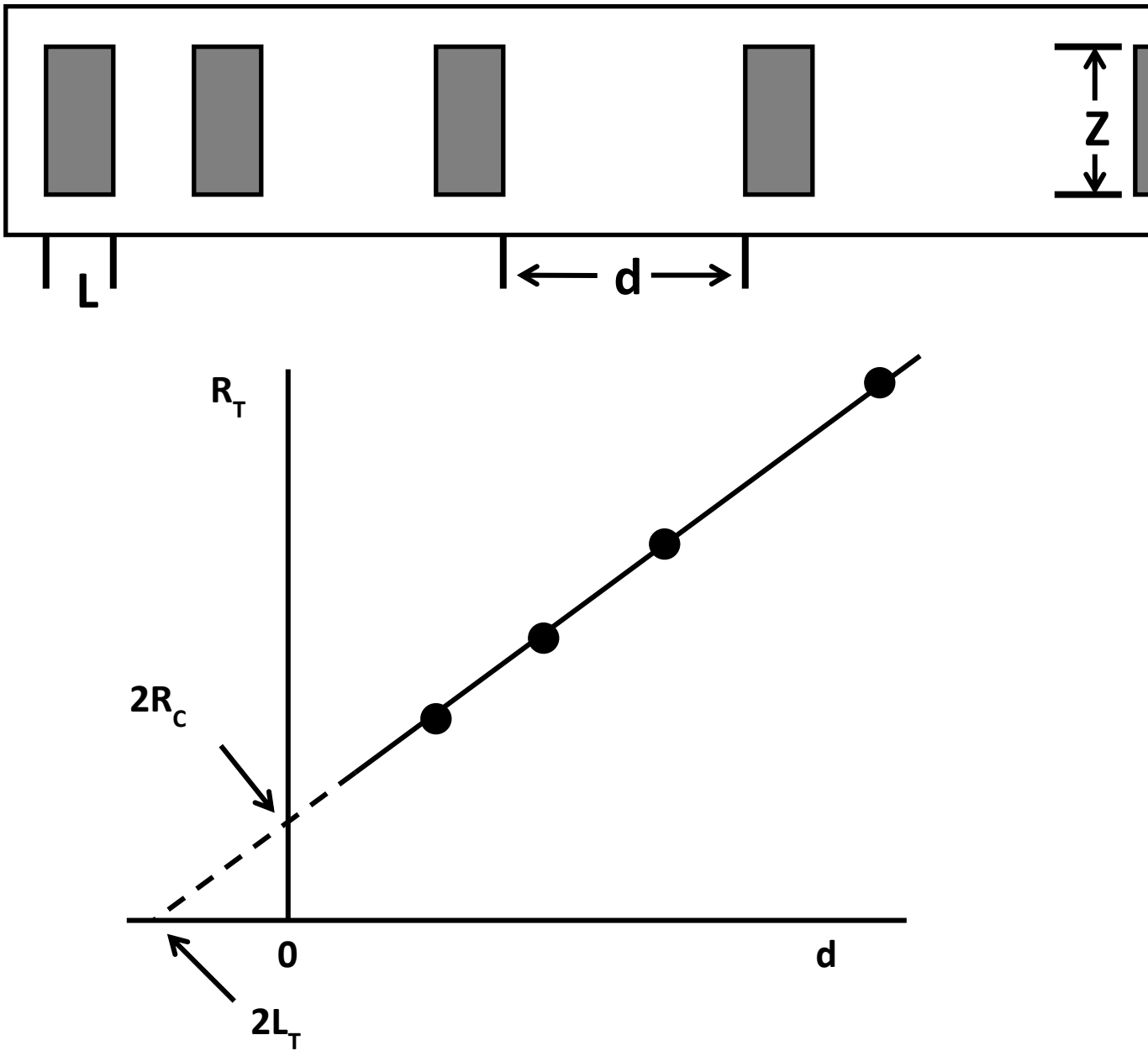

Figure 2-5. The transfer length method test structure. Schematic of TLM (top) and total resistance plotted as a function of the distance between the contact spacing (bottom). The slope of the line provides the sheet resistance divided by Z.

CHAPTER 3
DEVICE DESIGN ON SELF HEATING

Motivation

Due to their much larger band gap and breakdown fields, GaN devices have shown greater power densities than silicon, GaAs and InP devices[1] [10, 41]. Operating under high power conditions can result in significant self-heating within the device [10, 41-45]. Heating can in turn negatively affect the current output, due to a reduction in the 2DEG mobility and saturation carrier velocity [44, 45]. This makes thermal management a critical factor in the design of GaN transistors and their corresponding circuits. Operating at elevated channel temperatures can also decrease the reliability of devices, reducing the mean time to failure [46]. Therefore it is imperative that device design and packaging be optimized to properly manage channel temperatures and extend device lifetime.

Numerous experimental techniques have been utilized to measure temperature within the channel, including micro-Raman [47-51], scanning thermal microscope [52], and photocurrent measurements [53]. Resolution limitations for these techniques, as well as the presence of the gate metal and field plates, can hinder measurements where the temperature reaches a maximum in the channel [54]. For this reason, finite element simulations at dissipated power densities up to 5 $W.mm^{-1}$ have been carried out in order to investigate the effect of device design on the maximum channel temperature of AlGaN/GaN high electron mobility transistors (HEMTs) [55-57]. While focusing solely on thermal simulations does limit any electrical feedback typically gained from electro-

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thermal simulations, this simplified modeling technique provides valuable information on the nature of heat flow within the structure under investigation.

Experimental

Figure 3-1 shows a schematic of the device used for simulation. The substrate thickness is set at 250 µm for all three substrates investigated, unless otherwise noted: sapphire, Si, and SiC. Due to the negligible change in thermal conductivity between AlGaN and GaN and to decrease computation time, the structure was simplified to a GaN layer 2.27 µm thick. Including the effect of thermal boundary resistance (TBR) has been shown to increase the accuracy of thermal simulations [58, 59]. However, due to the fact that the resistance between the GaN and SiC interface (thermal boundary resistance, or TBR) varies substantially depending on growth conditions, as much as a factor of two reported from vendors, the effect of temperature due to TBR was not included in this study. A double gate structure is employed with a gate width of 150 µm, a gate length of 1 µm, and gate-to-gate spacing of 40 µm. Gold contacts 0.3 µm thick were placed on top of the GaN layer. Unless otherwise noted, the substrate and buffer area are 100 x100 μm^2.

The steady state condition was investigated, with

$$-k\left(\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}\right)=P_D, \tag{3-1}$$

where *k* is the thermal conductivity (W/m-K), T is the temperature (K), and P_D is the source of power. The active region was set with a constant heat flux,

$$q = P_D/(WLD), \tag{3-2}$$

where W=150 µm, L=1 µm, and D=0.02 µm. All sides were set for free convection, except for the base, which is set to 300 K by assuming a perfect heat sink. The initial

temperature of the system was set to 300 K. Due to the strong temperate dependence of thermal conductivity of some of the materials under investigation, temperature dependent thermal conductivities are used for all materials in the simulation, as shown in Table 3-1.

Results and Discussion

Effect of Substrate Material

Due to the high thermal conductivity and small lattice mismatch, SiC is becoming an extremely attractive candidate for replacing Si and sapphire as a substrate [45]. However, the high cost of SiC has prevented its exclusive use as a substrate, particularly for lower cost applications. Nonetheless, proper thermal management for all three substrates is required for optimal device operation. The substrate dependence on the increase in temperature was investigated as the dissipated power is increased up to 5 W/mm. As expected due to the large difference in thermal conductivity, Figure 3-2 shows the sharp rise in channel temperature for the sapphire substrate, displaying a second order polynomial increase. This increase in temperature is clearly prohibitive at high power densities. Kuball et al. reported a linear increase in maximum channel temperature as a function of dissipated power [47]. However, the results reported here show the trend becomes polynomial at much higher dissipated power. Both Si and SiC exhibit a linear increase in channel temperature up to 10 W/mm (not shown), with the latter being a much more effective heat sink because of the higher thermal conductivity (Table 3-1). Both experimental and simulated results in literature investigating the effect of channel temperature on substrates have reported this general trend, in which SiC has shown to be the superior choice for substrate material due its higher thermal conductivity [42, 44, 47, 50, 53, 54, 57, 60].

Effect of Die Size and Device Location

As the demand for higher packing densities and thus smaller electronics increases, there is a necessity for chips to occupy an increasingly smaller landscape. While the chip area decreases, however, the ability for the substrate to conduct heat away from active region diminishes. This, in turn, can ultimately result in an increase in the maximum channel temperature. Therefore, it is important to know the critical minimum die size before an increase in temperature occurs. 5 W/mm was applied to two gates on SiC, Si and sapphire substrates. The distance, d, from the gate was decreased from 500 µm to 25 µm (Figure 3-1). As can be seen in Figure 3-3, the minimum area is largely dependent on the substrate material. For the SiC substrate, maximum channel temperature increased as d decreased below 150 µm. The critical distance for a Si substrate is 200 µm. The sapphire substrate had the largest critical distance of 300 µm.

Though the substrate material will have a significant impact on the minimum size of the die required for optimal thermal dissipation, the location of the device on the die will also affect channel temperature. Even if the total area of the die meets the requirement stated above for proper thermal management, thermal dissipation can be hampered if the device is placed within close proximity to the edge of the die. This is due to the restricted thermal dissipation by conduction through the substrate and an increase in free convection which is not as efficient.

Effect of Device Design

The effect the number of gates has on the maximum temperature on sapphire, Si, and SiC substrates was then investigated. As was expected, the sapphire substrate resulted in a much larger increase in temperature as the number of gates increased.

Nonetheless, all three substrates exhibited a logarithmic increase in temperature (Figure 3-4). Two dimensional simulations are typically used in order to reduce computation time. However, a substantial difference in maximum channel temperature was observed between 2D and 3D finite element simulations. This effect was reported by Bertoluzza *et al*. with respect to increasing gate widths [54]. As can be seen in Figure 3-5 and 3-6, the discrepancy between 2D and 3D simulations becomes increasingly large as the number of gates present on SiC increases. The divergence in maximum channel temperature between 2D and 3D simulations is believed to arise due to the inability to incorporate the effect of heat dissipation at the ends of the gate in 2D. As shown in Figure 3-7, there is substantial dissipation of heat that occurs along the y-axis that would not be taken into account in 2D simulations, resulting in higher maximum channel temperatures in 2D simulations. 3D simulations can provide a much more accurate model of temperature distribution in the device, resulting in the ability to enhance device design and thermal management.

Additionally, there is a thermal gradient present between individual gate fingers (Figure 3-6 a and b) and along the width of the gate fingers (Figure 3-7). This trend is consistent with previous reports in literature, with up to a 30 °C maximum channel temperature difference between individual gates reported in six finger devices [47, 54]. Non-uniform temperature distributions within a single device, if significant, can lead to preferential degradation for thermally active degradation mechanisms [54, 57].

Summary

The maximum channel temperature in AlGaN/ GaN HEMTs increases when the die size is reduced below a critical distance, d, from the gate finger. This distance is significantly dependent on the substrate material, with the largest critical distance of

300μm for the sapphire substrate. Deviation of temperature between individual gate fingers and along the width of the gates was observed, especially as the number of gate fingers increased. A substantial variation in peak temperatures between 2D and 3D simulations was also observed, indicating the need for three dimensional analysis for accurate reliability and MTTF predictions.

Table 3-1. Thermal conductivity of materials used in simulations [54]

Material	Thermal Conductivity ($Wm^{-1}K^{-1}$)
GaN	$160(300/T)^{1.4}$
SiC	$400(300/T)$
Si	$148(\ 300/T)^{1.3}$
Sapphire	$35(\ 300/T)$

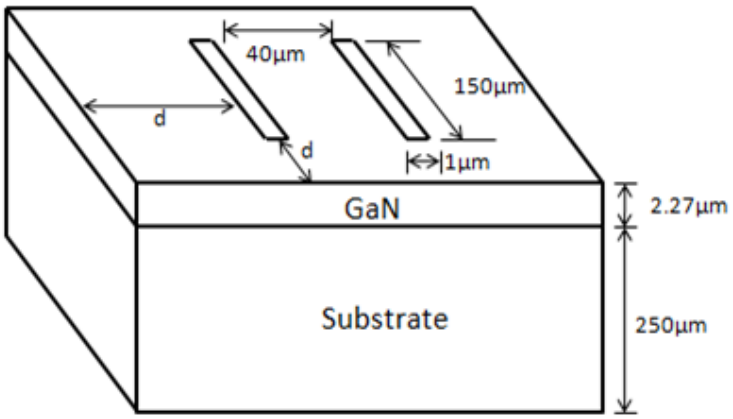


Figure 3-1. Schematic of 2-finger HEMT device used in thermal simulation with SiC, Si and sapphire substrates.

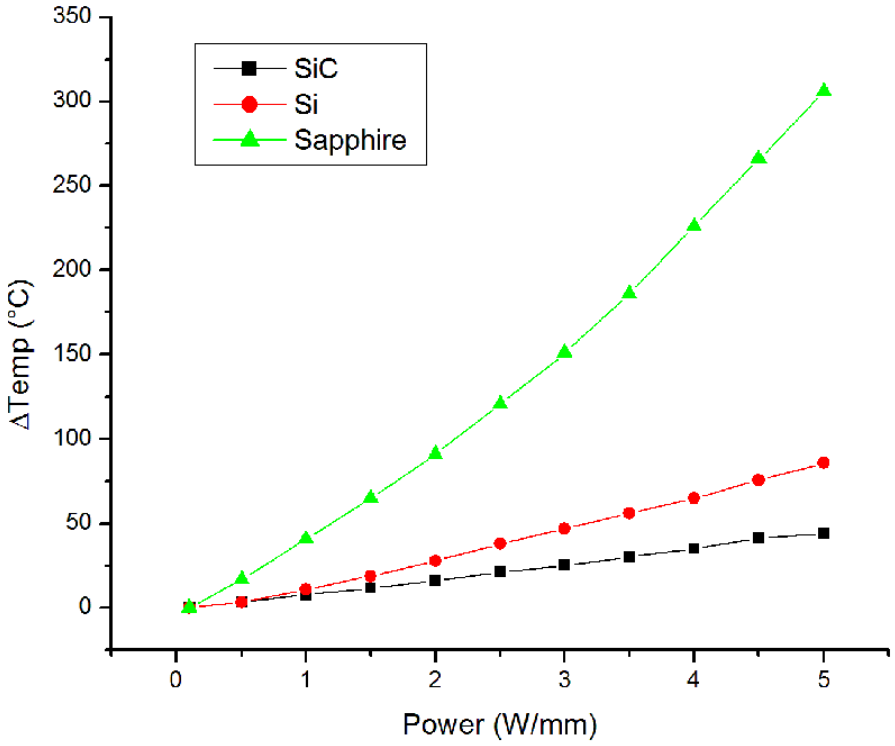


Figure 3-2. Increase in temperature as a function of dissipated power for SiC, Si and sapphire substrates for 2-finger HEMTs.

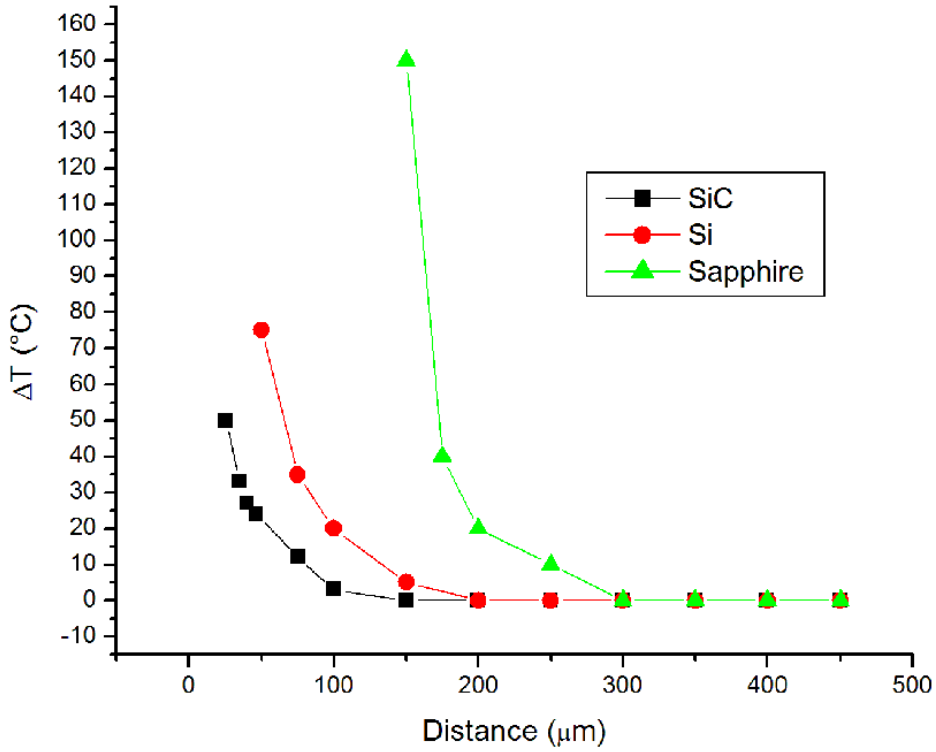


Figure 3-3. Maximum channel temperature as the distance, d, from the gate finger is increased for various substrates.

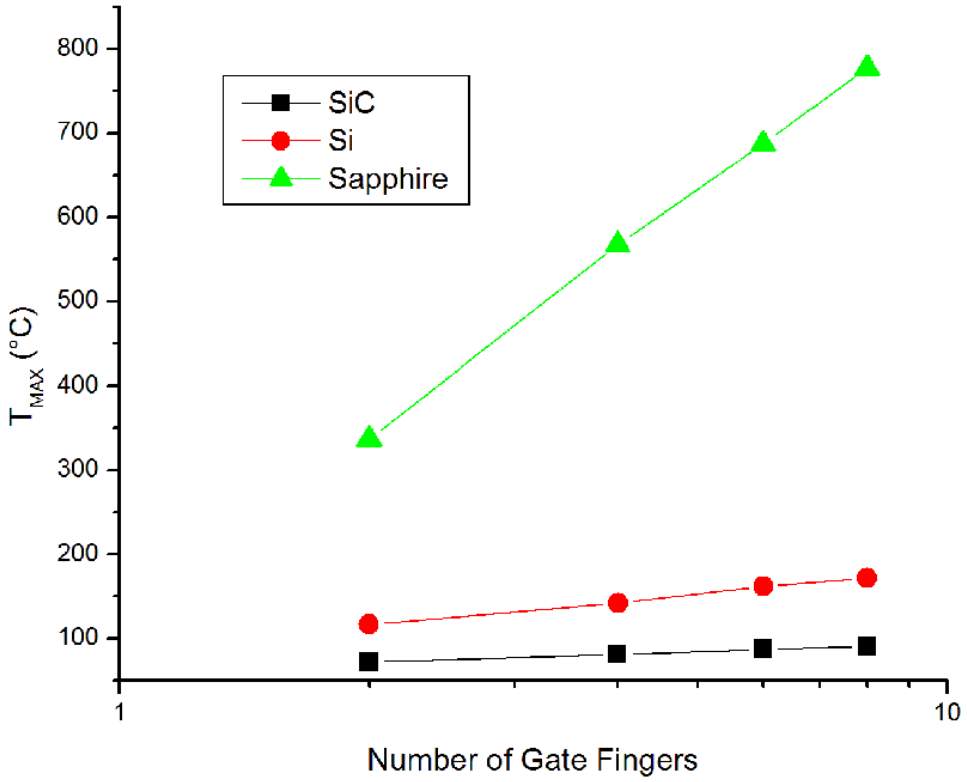


Figure 3-4. Maximum channel temperature as the number of gate fingers increases for various substrates. Device dimensions were set to L_G=1 µm, W_G=150 µm, and spacing between each gate finger of 40 µm.

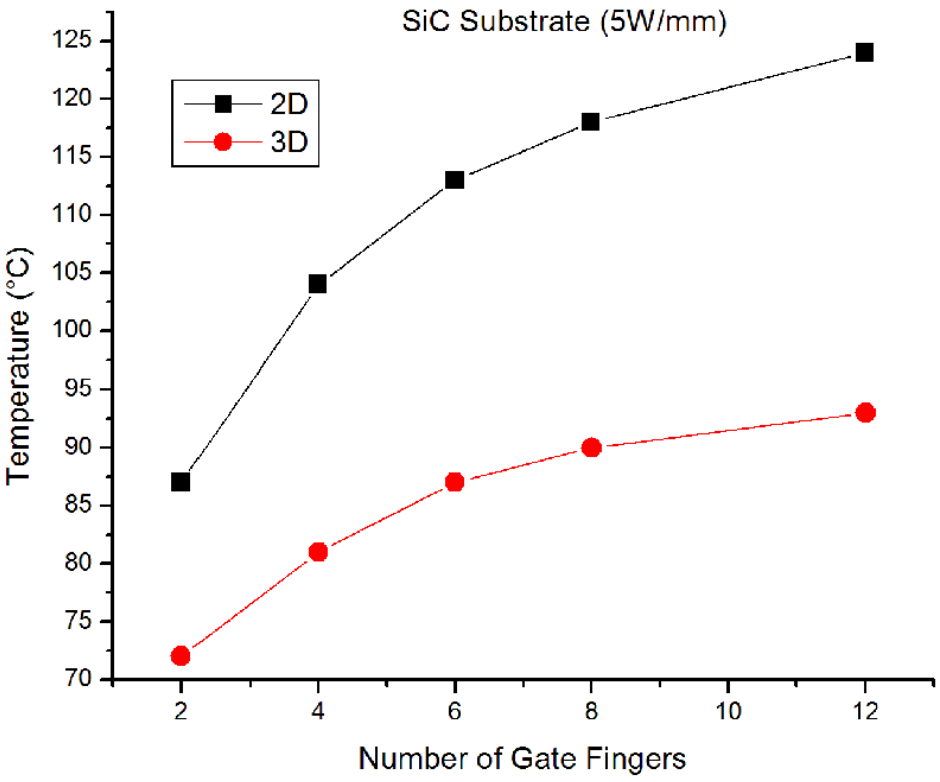


Figure 3-5. Increase in channel temperature for increasing number of gate fingers for both 2D and 3D simulations. Two finger HEMT with 5 W/mm dissipated power on SiC substrate.

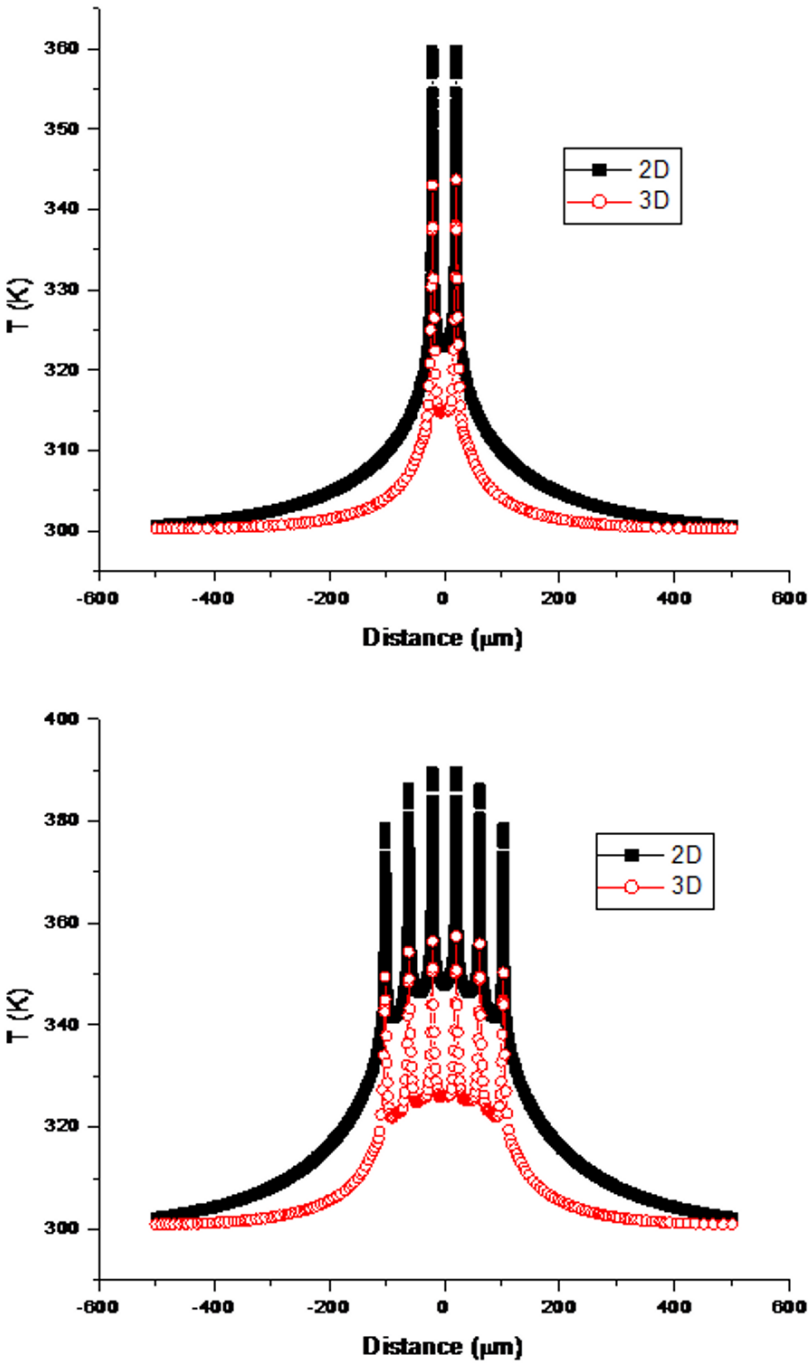


Figure 3-6. Distribution of temperature along x-axis of Figure 1 for (a) 2-finger HEMT and (b) 6-finger HEMT for 2D and 3D simulations on SiC substrate with 5 W/mm dissipated power.

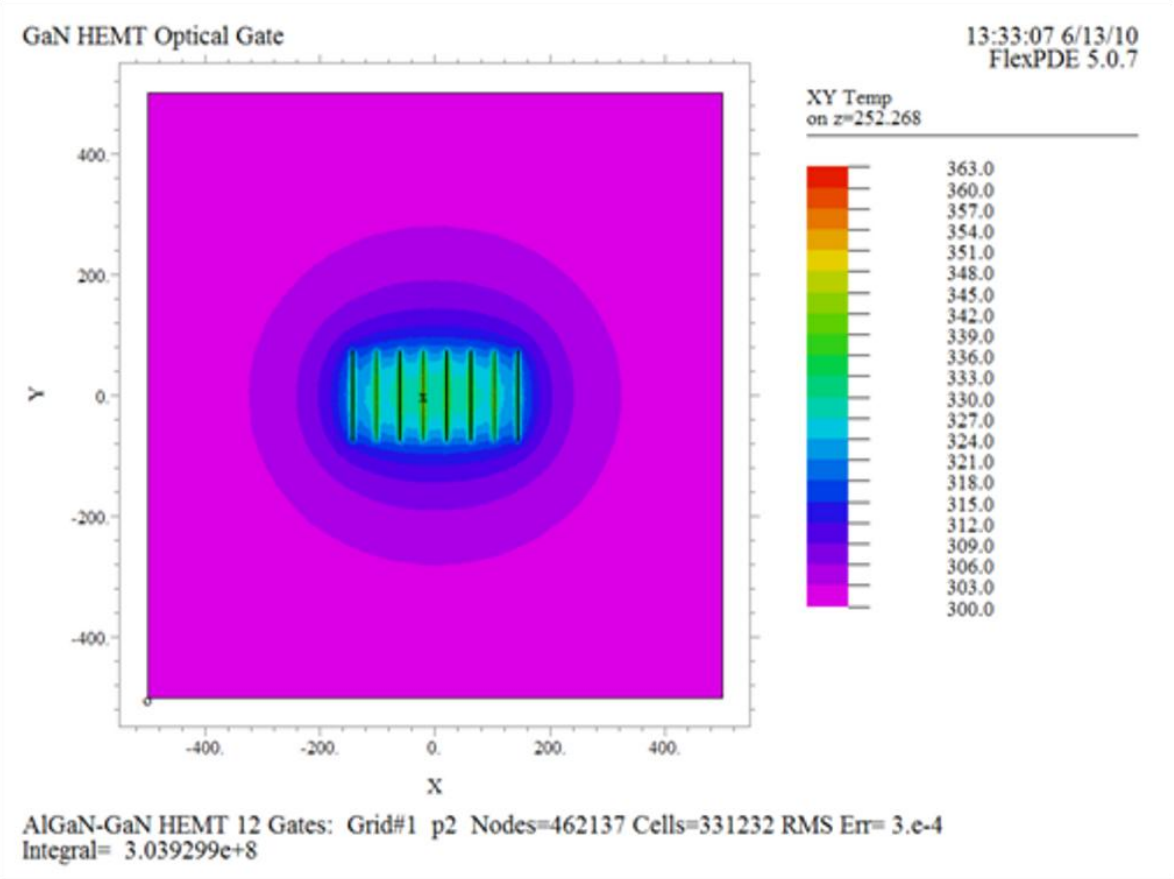


Figure 3-7 Temperature distribution of 8-finger HEMT on SiC substrate with 5 W/mm dissipated power. Temperature scale is in Kelvin.

CHAPTER 4
HIGH POWER STRESS

Background

GaN-based High Electron Mobility Transistors (HEMTs) have shown exceptional promise for use in both commercial and military systems for microwave and optoelectronic applications[1]. Ultra-high power radar systems will require the use of GaN transistors to be operated at very high voltages, currents and temperatures. Though GaN HEMTs are emerging in the commercial market, there is still concern with respect to their electrical reliability and the driving mechanisms for degradation [14, 15, 27, 30, 61-64]. Numerous degradation mechanisms have been reported, ranging from hot-electron induced degradation to field-driven mechanisms [28, 29, 31, 32, 65-67]. High power operation of GaN HEMTs can also result in substantial self-heating, which will reduce the 2DEG mobility and saturation carrier velocity [42, 44-46].

This chapter reports on the degradation of AlGaN/GaN HEMTs due to on-state (high power) conditions. The devices under test have a gate length ranging from submicron (0.1-0.17μm) to 1μm. To isolate the effect of the gate, a transmission line method structure was also stressed under the on-state condition.

Experimental

For high power stress, both the source and gate were held at ground while the drain bias was stepped up in 1 V increments at 30 minute intervals. HEMTs with a gate length of 0.17 μm were stressed with the baseplate temperature ranging from 60°C to

[1] Reprinted from Microelectronics Reliability, E.A. Douglas, C.Y. Chang, D.J. Cheney, B.P. Gila, C.F. Lo, Liu Lu, R. Holzworth, P. Whiting, K. Jones, G.D. Via, Jinhyung Kim, Soohwan Jang, Fan Ren, S.J. Pearton, , AlGaN/GaN High Electron Mobility Transistor degradation under on- and off-state stress, Vol 51, Issue 2, Pages No. 207-211 (2010), with permission from Elsevier.

100°C. To examine the effect of the gate, a single TLM segment with a 5 µm ohmic to ohmic spacing and 90 µm width was stressed under the same conditions as the 0.17 µm gate length HEMT.

Results and Discussion

HEMT Degradation

HEMTs with a gate length of 0.17 µm were step-stressed with a drain bias of 1 V to 25 V. As evident in Figure 4-1, an increase in baseplate temperature of 40 °C results in ~15% decrease in I_{DSS} during the stress test. Upon closer inspection of the drain current (Figure 4-2), the output current is constant for the duration of each step until a critical voltage is applied, at which point the degradation becomes permanent in nature and the output current decays under constant drain bias. This permanent degradation occurs when 10 V and 13 V is applied on the drain for a baseplate temperature of 100 °C and 60 °C, respectively. The channel temperature at the onset of degradation for both baseplate temperatures is 195 °C, as determined by three dimensional finite element thermal simulations. The maximum temperature in the channel during the stress test was 240 °C for both baseplate temperatures. These results indicate that degradation is due to a temperature activated mechanism. A positive shift in V_T of about 0.5 V was observed at 60 °C and an increase in V_T of about 0.7 V at 100 °C. Both baseplate temperatures resulted in ~90 % decrease in drain current. The majority of this decrease in drain current can be attributed to an increase in drain resistance, Figure 4-3, with the largest increase of about 20 Ω after stressing at 100 °C. Additionally, gate current characteristics after stress show about a two orders of magnitude increase in gate leakage current for a baseplate temperature of 60 °C, and about three orders of magnitude increase at 100 °C (Figure 4-4).

HEMT vs TLM Degradation

In order to eliminate the effect of the gate on the device, Transmission Line Method (TLM) patterns with a 5 μm spacing were stressed under the same conditions. Though the drain current for the HEMT devices exhibited substantial degradation at a lower current density, the TLM patterns exhibited excellent stability regardless of the baseplate temperature, with negligible increase in total resistance (Figure 4-5). In addition, the sheet resistance was found to be independent of temperature (Figure 4-6), further establishing that the ohmic contacts and underlying epitaxial layers are not the source of degradation in the HEMTs. Devices with 0.17 μm gate length exhibited the onset of degradation at lower voltages with an increase in baseplate temperature. Thermal simulations, however, showed that permanent degradation occurred at the same channel temperature.

Both gate and drain current-voltage characteristics reveal significant degradation, while the TLM structure displays remarkable stability under the same stress conditions and higher current density. These results confirm that the Schottky contact is the source of degradation for the HEMT. Reaction of the gate with the underlying epitaxial layers and subsequent gate metal sinking would result in a decrease in distance between the metal-semiconductor interface and the channel. This sinking would in turn increase the depletion region and account for the decrease in drain current, increase in V_T, and an increase in gate leakage current seen in the HEMTs. Additionally, damage due to hot electrons would create a significant amount of traps within the channel close to the drain contact, which can explain the increase in the observed drain resistance.

Gateless, HEMT, and TLM Breakdown

The effect of device design and stress temperature was investigated on 0.17 µm gate length HEMTs (4 x 150 µm channel area), 5 µm spacing TLM structures (5 x 90 µm channel area), and gateless HEMT structures (4 x 150 µm channel area). All three structures were step stressed to catastrophic failure in 1V increments for 30 min each step at baseplate temperatures ranging from 60 to 130 °C. As can be seen in Figure 4-7, once the baseplate temperature is increased above 100 °C, the breakdown decreases from a bias of 21 V to 19 V. Comparison of the breakdown voltage for all three structures stressed at a temperature of 100 °C is shown in Figure 4-8. As the overall current density increases, the breakdown voltage decreases significantly, from over 40 V to close to 21 V. However, 3D finite element thermal simulations indicate that the maximum channel temperatures present in the devices at breakdown are significantly different. Gateless HEMT structures, with the highest current show the maximum channel temperature of about 310 °C, which is above the known thermal stability for Ti/Al/Ni/Au ohmic contacts [28]. Conversely, the TLM and 0.17 µm gate length HEMT show breakdown voltages of 28 V and 42 V with corresponding maximum channel temperatures of about 160 °C and 110 °C, respectively. These results indicate that catastrophic failure of the devices under high power conditions is not governed by temperature alone.

Summary

The effect of on-state, high power, step stress was investigated on several device structures, including 0.17 µm gate length HEMTs, gateless HEMT structures, and TLM structures with 5 µm spacing. Permanent degradation was observed in the 0.17 µm

gate length HEMTs at relatively low drain bias voltages. However, temperature dependent stress tests revealed that permanent degradation was dependent on channel temperatures reaching 195 °C. Conversely, TLM structures, in which there is no Schottky contact, exhibited exceptional stability up to 25 V bias even though current densities, thus channel temperatures, reached much higher values. Therefore, the Schottky contact is the likely cause for permanent degradation. Breakdown voltages for all three structures indicated that catastrophic failure was not due to channel temperatures, as peak channel temperatures varied significantly (110 °C to 310 °C) at breakdown. There are likely multiple degradation drivers present under these stress conditions, and future tests will be required to isolate the effect of current, voltage and temperature under high power conditions.

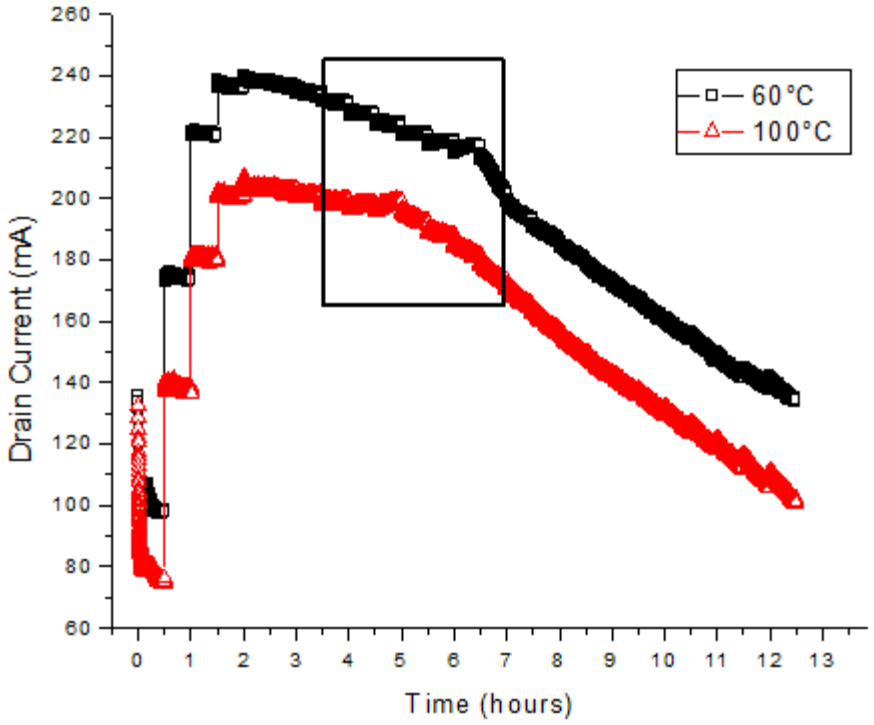


Figure 4-1. Drain current of 0.17 µm gate length HEMTs during step stress with baseplate temperatures of 60°C and 100°C.

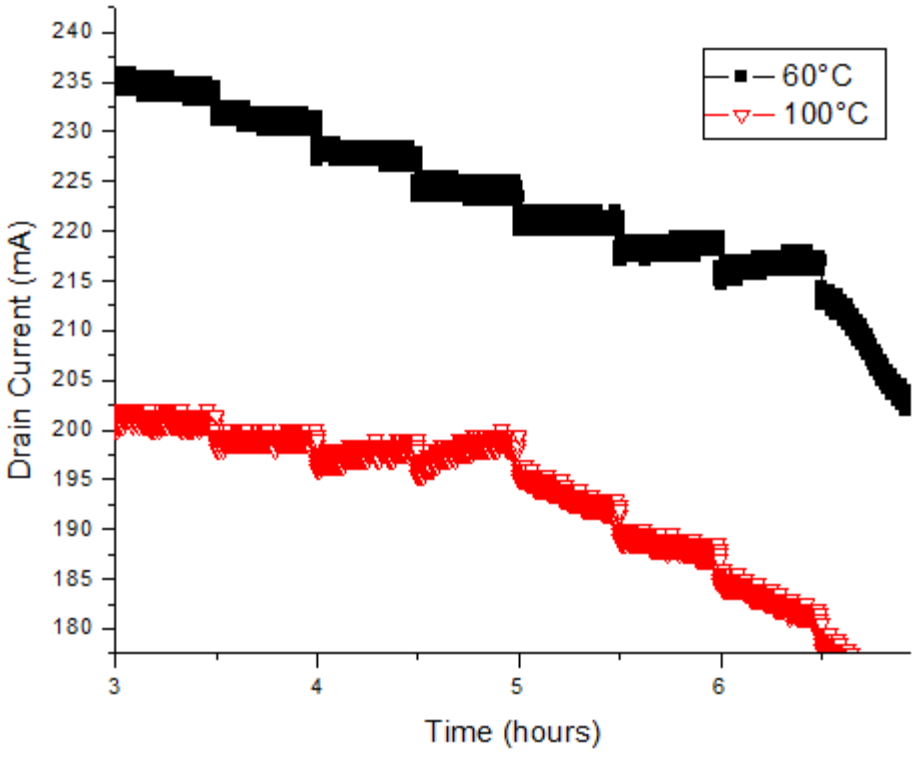


Figure 4-2. Drain current of 0.17 µm gate length HEMTs during step stress with baseplate temperatures of 60°C and 100°C. (Inset of Figure 4-1)

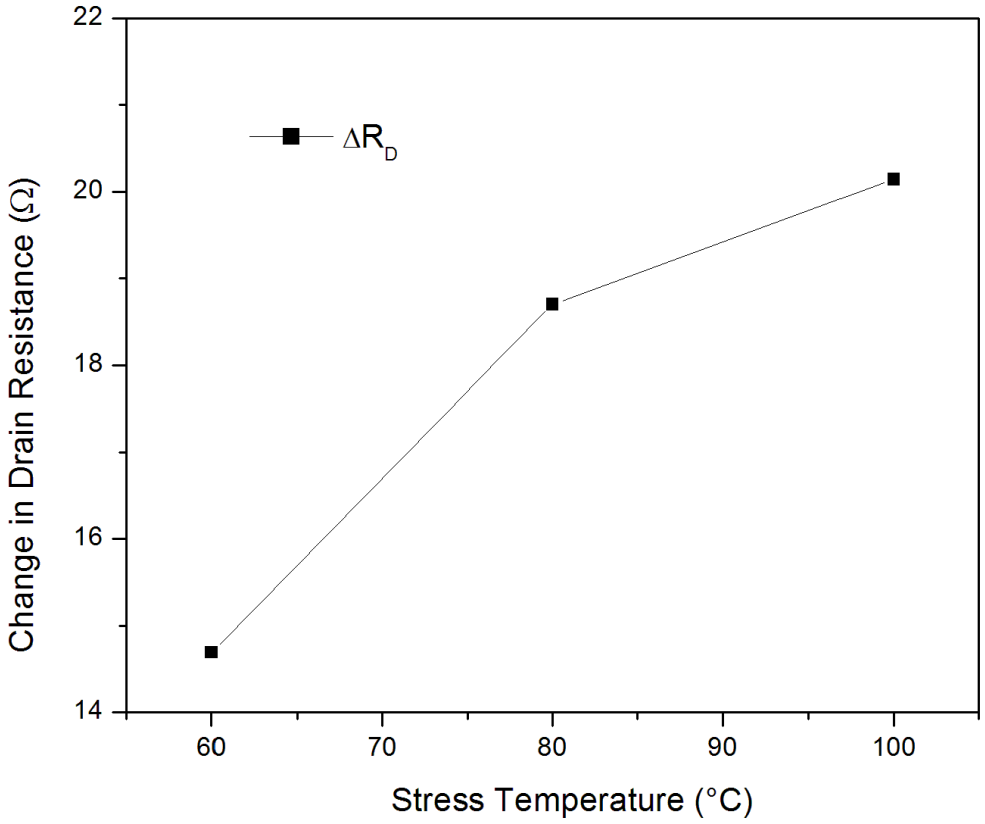


Figure 4-3. Increase in drain resistance (Ω) after step stress up to V_{DS} = 25 V of 0.17 µm gate length HEMTs with baseplate temperatures of 60, 80 and 100°C.

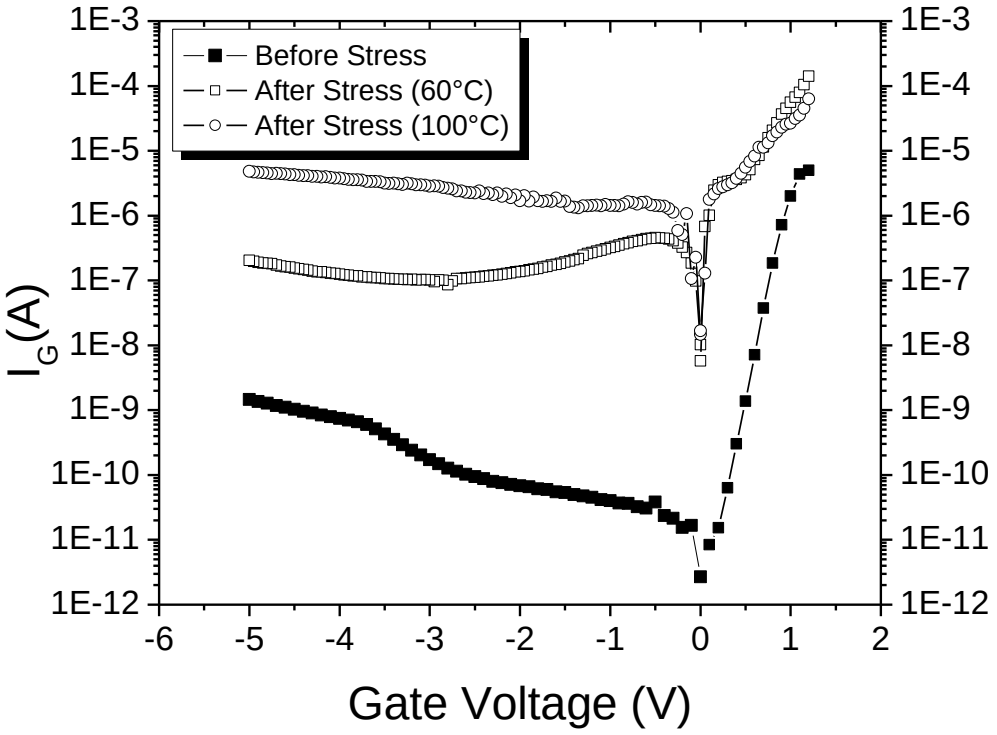


Figure 4-4. Gate current of 0.17 µm gate length HEMT before and after on-state step stress with a baseplate temperature of 60°C and 100°C.

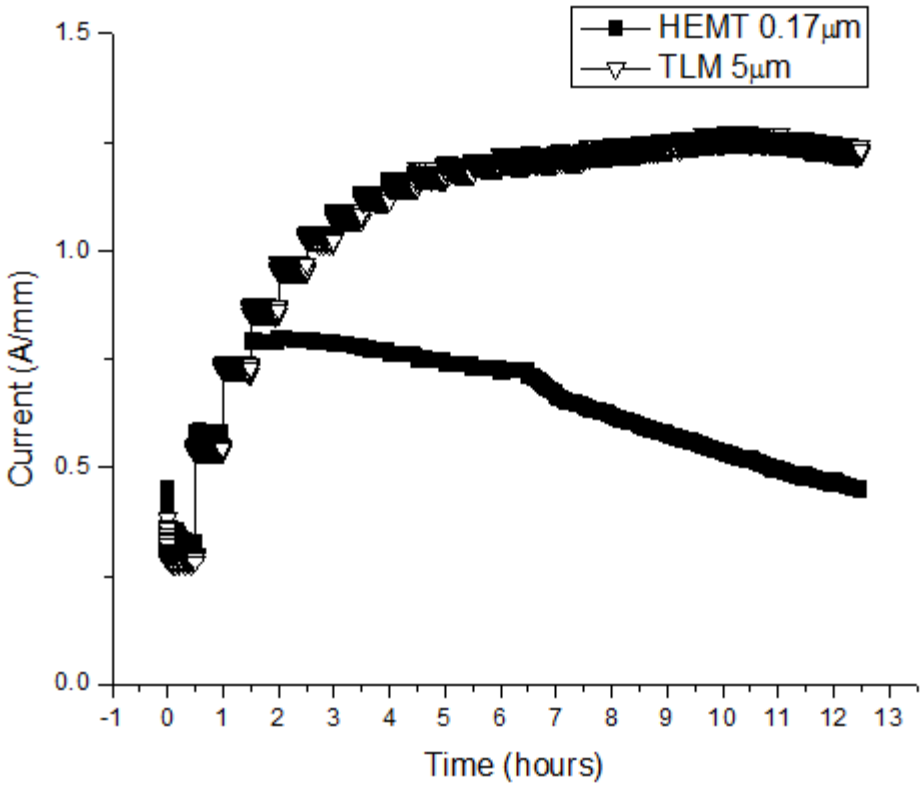


Figure 4-5. Comparison of current (A/mm) of 0.17 μm gate length HEMT and TLM with 5 μm spacing.

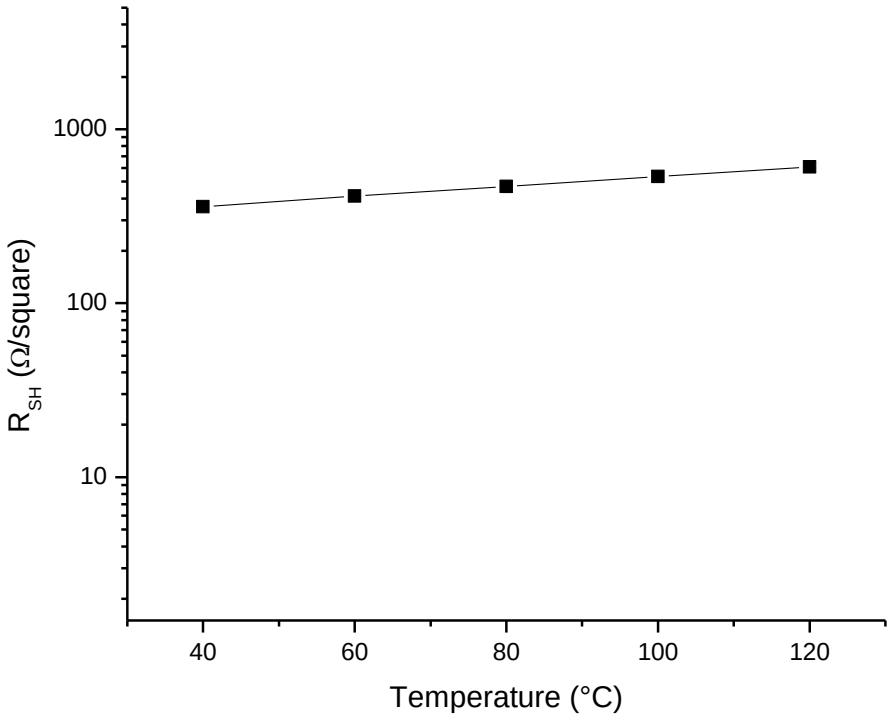


Figure 4-6. Temperature dependence of sheet resistance.

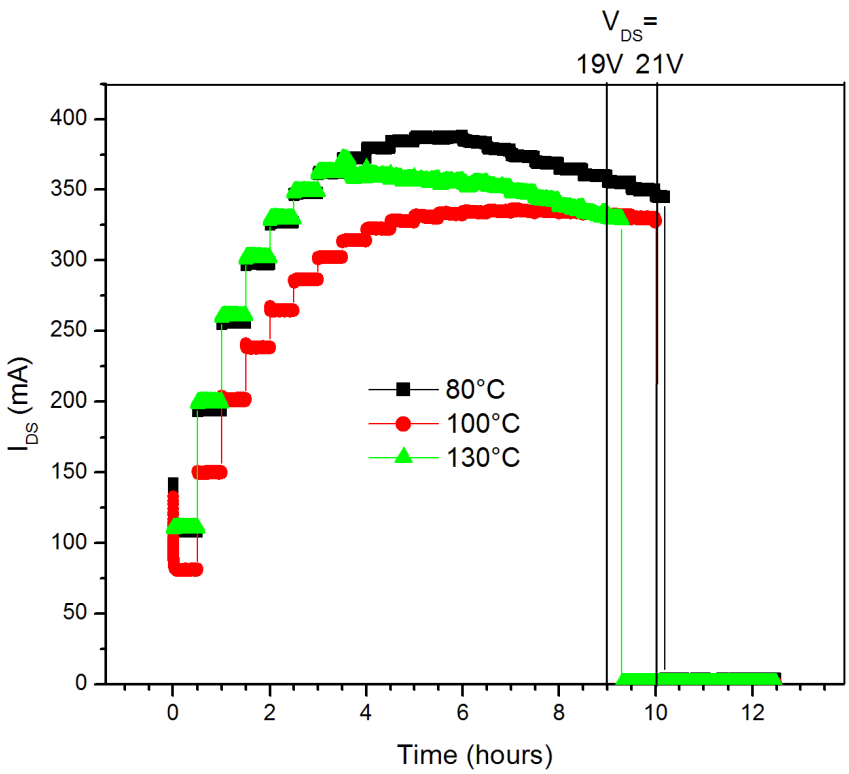


Figure 4-7. Effect of baseplate temperature on breakdown of gateless HEMT structures.

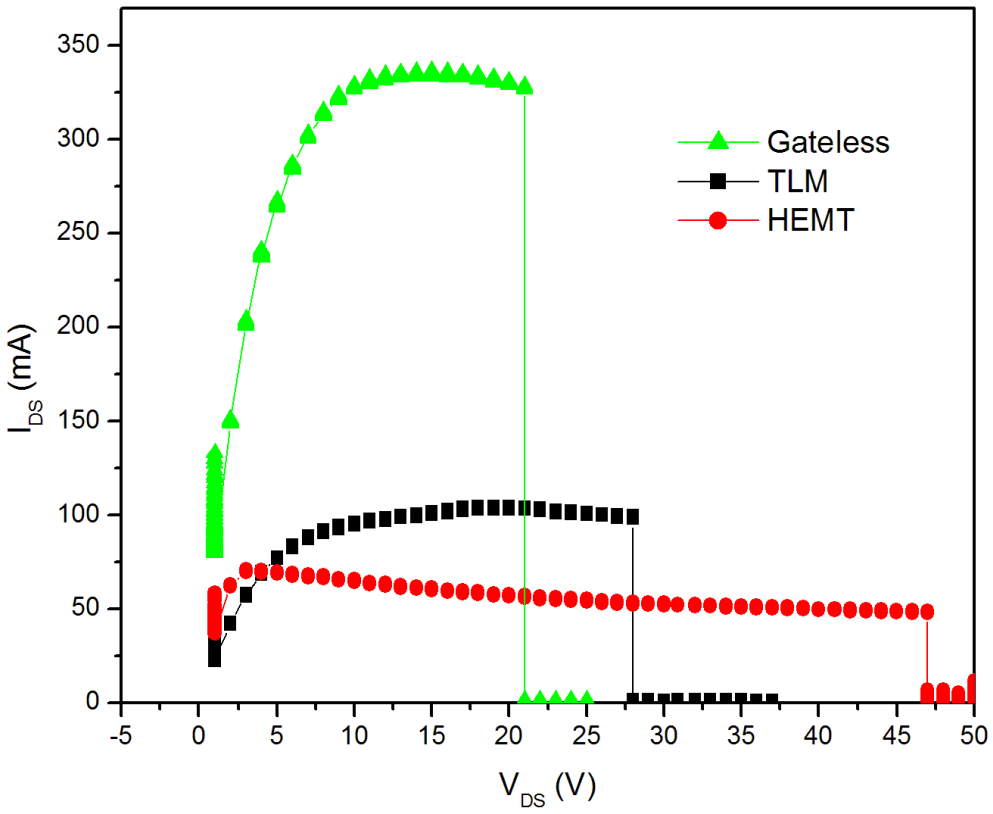


Figure 4-8. Drain current as voltage is step stressed until catastrophic failure is achieved for 0.17 µm gate length HEMT, gateless HEMT structure, and TLM structure. Baseplate temperature set to 100°C for all three structures.

CHAPTER 5
TEMPERATURE DEPENDENT OFF-STATE STRESS

Motivation

AlGaN/GaN High Electron Mobility Transistors (HEMTs) have attracted interest due to their high performance capabilities[1]. For this technology to become a key component for high frequency and high power applications, there is a need to understand the degradation mechanisms that affect the long-term reliability. Employment of GaN HEMTs for applications such as high power radar systems will require devices to be driven into saturation while being subjected to large-signal RF, resulting in devices experiencing high electric fields and high current densities. For example, Campbell and Dumpka have reported upwards of 40 W of off-state power for single pole double throw GaN on SiC switches with a gate bias of -37 V for source-to-drain spacing of 4 μm, similar to the devices studied here [68]. A dc gate bias step stress permits one to isolate the effect of high electric field on the Schottky contact, which has been investigated in detail by several groups [14, 29-31, 69-78]. However, there has been no study on the interacting effects of temperature and high reverse dc gate bias on the Schottky contact to the authors' knowledge.

During a high reverse gate bias step stress, gate leakage current in AlGaN/GaN HEMTs is seen to steadily increase, until critical voltage (V_{CRI}) is reached [30, 31, 69, 70, 75, 76]. At this point, the gate leakage current sharply increases about 1-2 orders of magnitude. This sharp rise in current has been attributed to the inverse piezoelectric

[1] Reprinted from Microelectronics Reliability, E.A. Douglas, C.Y. Chang, B.P. Gila, M.R. Holzworth, K.S. Jones, L. Liu, Jinhyung Kim, Soohwan Jang, G.D. Via, F. Ren, S.J. Pearton, Investigation of the effect of temperature during off-state degradation of AlGaN/GaN high electron mobility transistors, (2011), with permission from Elsevier.

effect [30, 75, 76]. As the electric field increases, the tensile stress in the AlGaN layer increases. Added on top of the intrinsic tensile strain, it is believed that at the critical voltage, crystallographic defects form from the excessive mechanical strain, creating both electron traps and increasing electron tunneling through the defect states [14, 17, 29, 30, 72, 76, 78-80]. Though the devices in this study exhibit electrical characteristics during and after performing the gate step stress that are similar to previously reported results, the formation of cracks at the gate edge have not been observed in the studies presented here [69, 70]. In order to further investigate and understand the degradation mechanisms causing the increase in gate leakage current under high reverse gate bias, this chapter reports on the temperature dependence of critical voltage.

Experimental

AlGaN/GaN HEMTs were fabricated on 6H SiC semi-insulating substrate, beginning with a 2.25 µm Fe-doped GaN buffer layer grown on top of an AlN nucleation layer (Figure 5-1A). This was followed by 15 nm of $Al_{0.28}Ga_{0.72}N$, capped with 3 nm of unintentionally doped GaN. On- wafer Hall measurements showed a sheet carrier concentration, sheet resistance, and mobility of 1.06 x 10^{13} cm^{-2}, 310 Ohms/square, and 1900 cm^2/V.s, respectively. An inductively coupled plasma mesa etch of ~1000 Å was performed to isolate neighboring devices. Ti/Al/Ni/Au Ohmic metallization was annealed at 850 °C for 30 sec for source/drain contacts. The HEMTs employed a Ni/Au double gate design with a gate width of 150 µm, source-to-gate and gate-to-drain distances of 2 µm and were passivated with SiN_x deposited by plasma enhanced chemical vapor deposition (Figure 5-1B).

Over twenty identical neighboring HEMTs from a single wafer with a gate length of 0.14 µm were stepped stressed with a HP 4156C semiconductor parameter analyzer from -10 V to -42 V in 1 V increments for 60 sec each step in the dark at different temperatures ranging from 24 °C to 150 °C. The temperature of the devices was regulated by a heated chuck, with at least two devices stressed at each temperature. Pre-stress electrical characteristics were taken at ambient temperature in order to verify that the selected devices exhibited similar performance. The gate current (I_G), gate-to-drain leakage current (I_{GD}), and gate-to-source leakage current (I_{GS}) were monitored during the stressing. Additionally, gate current in the off-state, I_{GOFF}, was measured after each step with a bias of V_{DS} = 0.2 V and V_{GS} = -5 V. Drain and gate current-voltage sweeps were measured pre- and post-stress at room temperature. The device was heated to the desired stress temperature before the step-stress was performed, with gate leakage current, drain and gate I-Vs, and extrinsic transconductance being measured at elevated temperatures after each step of the stress test. Both source and drain were held at ground in order to symmetrically stress the gate contact. Furthermore, numerical device simulations (ATLAS/Blaze) were carried out to determine the maximum electric field present in the GaN cap layer at the edge of the gate contact (both source and drain side since the device is symmetrically stressed) when critical voltage is reached.

Results and Discussion

Effect of Temperature on Critical Voltage

For all devices, gate leakage current steadily increases as the step-stress is carried out until the critical voltage (V_{CRI}) is reached, upon which permanent degradation occurs and I_G abruptly increases about an order of magnitude. At room

temperature, the HEMTs show a considerable increase (four to five orders of magnitude) in gate leakage current after step-stressing to -42 V (Figure 5-2). However, the total gate current increase is less significant after stress at increased temperature (Figure 5-3). The increase in I_G after high reverse gate bias has been previously reported and correlated to an increase in drain and source resistance as well as a decrease in saturated drain current, which was also observed in our devices (Figure 5-4) [29, 30, 72, 75, 76].

The critical voltage of our devices at 24 °C is -30 V. As the temperature of the devices is increased to 150° C, the critical voltage is observed to linearly decrease (Figure 5-5). Error bars shown in Figure 5-5 indicate the small variations in critical voltage observed across the region of wafer in which the devices were located, likely due to slight variations in epitaxial layers [67] . Due to the fact that V_{CRI} occurs at lower voltages as the temperature increases, the maximum electric field present at the edge of the gate at V_{CRI} also decreases. ATLAS/Blaze electrical simulations indicate that the peak electric field decreases from 3.3 MV/cm at a critical voltage of -28 V with a stress temperature of 28 °C to 2.6 MV/cm at a critical voltage of -18 V at 150 °C (Figure 5-6). The gate leakage current measured during the step stress of four different devices stressed at four different temperatures ranging from 24 °C to 150 °C (Figure 5-7) further illustrate the negative temperature dependence. Previous reports in the literature attribute the sharp rise in I_G at the critical voltage and resulting permanent I_G degradation to the inverse piezoelectric effect [30, 31, 69, 72, 75, 76, 78, 81]. However, this result reveals that the breakdown which results in a sharp increase in gate leakage

current does not occur at the same electric field, and therefore does not occur at the same piezoelectric induced stress.

Upon closer examination, one can see that the gate leakage current is independent of critical voltage, (Figure 5-8). In addition, a linear fit of gate current indicates that there is no change in I_G as a function of stress temperature (Figure 5-9) either at the critical voltage or just above critical voltage (V_{CRI} – 1 V). Error bars in Figure 5-8 and 5-9 were calculated based on the variations of current measured during the step stress and variations across the region of the wafer in which the devices were located. Devices stressed at room temperature have been reported to display a significant dependence on gate voltage / electric field [17, 29-31, 69, 72, 75, 76, 78, 81]. Ni/Au metallization schemes for Schottky contacts on GaN have been determined to be thermally unstable above 400 °C, with numerous nickel nitrides reported being formed at temperatures as low as 200 °C [82-84]. Additionally, thermal instability of Ni/Au based ohmic contacts have been reported due to Ga out-diffusion and Au inter-diffusion at elevated temperatures [28]. The voltage at which gate leakage current sharply increases (i.e. critical voltage) exhibits a negative temperature dependence with an activation energy of 41.6 meV. The abrupt and permanent gate degradation at elevated temperatures was observed to occur at similar gate leakage currents regardless of critical voltage and stress temperature (~10^{-7} A). Gate leakage currents immediately after critical voltage was reached also displayed similar values at all stress temperatures (~10^{-6} A), indicating similar leakage paths for all stress temperatures.

Interfacial Layer Breakdown

Pitting and crack formation at the edges of the gate contact have been reported after high reverse gate bias step stress of similar devices [29-31, 75, 76]. However, pitting and cracks do not typically develop in our devices after gate step stress, though the degradation and electrical signatures are similar to those reported in literature [30, 75, 76]. Figure 5-10 shows the gate leakage current of a typical device during a 60 sec step when critical voltage was reached. The sharp increase in gate leakage current does not occur immediately, but displays a time dependence and occurs anywhere from 20 to 40 sec after bias is applied. Cross sectional transmission electron microscopy (TEM) of an unstressed device shows an interfacial layer present between the Ni/Au Schottky contact and the GaN cap layer (Figure 5-11 A). X-ray energy dispersive spectroscopy (EDS), not shown, indicates that this interface is an oxide layer ~ 15 Å thick, though this layer is too thin for accurate resolution of the oxide species. Oxygen has been shown to be a shallow donor in GaN, with the most favorable defect formation of oxygen substituting for N (O_N). Experimental results have indicated a very low activation energy associated with O_N, ~ 34 meV [85-87]. Additionally, GaN easily forms a native oxide, particularly at elevated temperatures [26]. The unintentional oxide interfacial layer present in these devices is due to processing, from not completely removing the native oxide before depositing Ni for the Schottky contact. Holzworth et al. performed laser assisted atom probe tomography on the Ni / AlGaN interface of an AlGaN/GaN HEMT and also observed an oxide interfacial layer, indicating that the presence of an oxide interfacial layer is not unique to the devices in this study [88].

TDDB

Time dependent dielectric breakdown (TDDB) is typically observed when the applied electric field, less than the breakdown electric field, is held for a sufficient amount of time. When an electric field is applied to a dielectric, a net electric dipole moment is induced and results in a total dipole moment in the dielectric, or polarization **P**. The polarization can be expressed as

$$\boldsymbol{P} = \chi \epsilon_0 \boldsymbol{E}_{OX}, \tag{5-1}$$

where χ is the electric susceptibility, $\epsilon_0$the permittivity of free space (5.52 x 10^{-3} e/V Å), and E_{ox} is the electric field on the dielectric.

$$E_{ox} = V_{ox}/t_{ox}, \tag{5-2}$$

where V_{ox} is the voltage drop across the dielectric and t_{ox} is the thickness of the dielectric layer. The local electric field (E_{loc}) experienced by each dielectric molecule is expressed by

$$\boldsymbol{E}_{loc} = \boldsymbol{E}_{ox} + L(\boldsymbol{P}/\epsilon_0) \tag{5-3}$$

where *L* is the Lorentz factor. At breakdown, the resulting current density flowing through the dielectric results in a “localized meltdown,” with the breaking of bonds between atoms as the degradation mechanism for TDDB [89-91]. Following the thermochemical electric field model for TDDB in thin SiO_2 films, one can calculate the ionic displacement due to applied electric field [89, 90]. Thermal oxidation of GaN has shown the formation of β-Ga_2O_3, a stable polymorph with a monoclinic structure, and can be assumed to be one possible oxide formed at the interface between the Ni-based Schottky contact and the GaN cap layer for our devices [92-95]. One can calculate the total molecular polarizability from the Clausius-Mossoti relation given by,

$$\alpha^t = \frac{3(\epsilon_r - 1)\epsilon_0}{(\epsilon_r + 2)N_V} \quad (5\text{-}4)$$

where ϵ_r is the relative dielectric constant for Ga_2O_3 (14.2) and N_V is the number of molecules per unit volume (2.07 x 10^{22} cm^{-3}) giving a molecular polarizability for Ga_2O_3 of 5.96 x 10^{-17} e cm^2/V. The total molecular polarizability is comprised of the ionic and electronic component, in which $\alpha^t = \alpha^i + \alpha^e$. The ionic bond displacement (Figure 5-12) can then, in turn, be calculated by the ionic component of the induced molecular dipole moment Δp^i, where

$$\Delta p^i = \alpha^i E_{loc} = 0.4\alpha^t(\frac{\chi+3}{3})E_{ox}. \quad (5\text{-}5)$$

The bond strength of a Ga-O bond is much higher than that of a Ga-Ga or O-O counterpart. This is due in part to the ionic nature of the bond and can be quite significant. The total single bond energy between two atoms, A and B, is due to the molecular covalent single bond ($U_{A-B}^{(e)}$) and the ionic contribution ($U_{A-B}^{(i)}$), in which

$$U_{A-B}^{(t)} = U_{A-B}^{(e)} + U_{A-B}^{(i)}. \quad (5\text{-}6)$$

While the covalent single bond energy between two atoms can be determined by

$$U_{A-B}^{(e)} = \sqrt{U_{A-A} * U_{B-B}}, \quad (5\text{-}7)$$

the total bond energy can increase substantially if there is a large electronegativity between the two atoms. This is especially true in a Ga-O bond, where the electronegativity difference is 1.7. The ionic contribution can be determined by

$$U_{A-B}^{(i)} = 1.3(\chi_A - \chi_B)^2. \quad (5\text{-}8)$$

where χ_A and χ_B are the Pauling electronegativities. The total energy for a Ga-O bond is 6.16, with ~60% ionic contribution. This leads to an extremely polar bond, which would thus be exceptionally susceptible to bond distortion under an electric field. During bond

formation, the effective net charge (Z^*e) that would be transferred can be determined from the contribution of the ionic bond

$$U_{O-Ga}^{(i)} = \frac{-(Z^*e)^2}{4\pi\epsilon_0 r}. \quad (5\text{-}9)$$

The ionic bond displacement (Δx) can be determined from the induced molecular dipole moment:

$$\Delta p^{(i)} = 2(Z^*e)(\Delta x)\cos\left(\theta/_2\right) \quad (5\text{-}10)$$

Given a very conservative electric field of 2 MV/cm, which is lower than minimum electric field simulated at critical voltage for a stress temperature of 150 °C, this results in a ~ 10% increase of the Ga-O bond length. A substantial distortion of the ionic bond can result in significant anharmonic coupling to the lattice, increasing the ability for the strained bond to interact with thermal phonons [89, 90]. An increase in the stress temperature can provide enough energy to cause the strained ionic bonds to break and lead to breakdown in the dielectric, which contributes to the negative temperature dependence observed for the critical voltage. Once breakdown in the dielectric occurs, a leakage path for electrons can form.

Lo et al. reported on the stability of Ni on GaN investigated by x-ray photoelectron spectroscopy [77]. After an anneal at 300 °C, they observed a decrease in the O-Ga bonding and an increase in O-Ni bonding through a shift in the Ni 2p and O 1s peak. This indicates that at elevated temperatures Ni will strip oxygen from the native oxide on GaN to create a layer of NiO. It is likely that if oxygen becomes disassociated from Ga during electrical stress because of field induced bond breakage, oxygen will diffuse to form NiO, even at temperatures of 150 °C and lower. Both the intrinsic and piezoelectric induced strain in the GaN cap and AlGaN layer enhance diffusion.

Additionally the thermal expansion coefficients of GaN and Ni are considerably different, 5.59×10^{-6} K^{-1} and 14.17×10^{6} K^{-1}, respectively, resulting in an increase of strain at the interface and further aiding diffusion as the stress temperature increases [96, 97]. The breakdown of the interfacial oxide layer due to electric field induced bond breakage, enhanced by thermal and strain effects, results in the consumption of oxide observed from cross sectional TEM after off-state stress, (Figure 5-11 B), as well as the observed negative temperature dependence on breakdown. A comparison of Ni based and Pt based Schottky contacts during high reverse gate bias step stress on AlGaN/GaN HEMTs was reported by Lo et al. They showed that Pt based Schottky contacts resulted in enhanced stability with no observed breakdown up to -100 V gate step stress, whereas Ni based Schottky contacts showed typical critical voltage breakdown at -55 V [77]. This further reveals that the breakdown occurring at V_{CRI} is dependent upon the reactivity of the gate metal, particularly in the presence of disassociated oxygen.

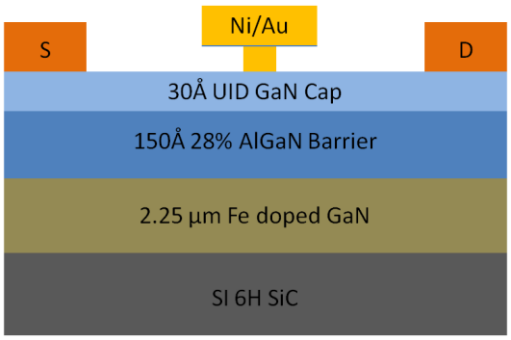
In order to further investigate the role of time dependent breakdown, additional step-stress tests were performed with varying the length of time at each voltage step. The time steps ranged from 10 sec to 1000 sec while increasing the gate voltage in 1 V steps. It was observed that as the time steps increased, the time that elapses before gate leakage current abruptly jumps also increased (Figure 5-13). Furthermore, at 1000 sec time intervals, gate leakage current is observed to steadily increase from ~750 sec to 800 sec before the characteristic sharp breakdown. It is interesting to note that after breakdown, a transient is still present in the current. This indicates that there is a clear presence of electron traps refilling even after breakdown. Figure 5-14 shows that there is a clear linear dependence of the time to breakdown versus the time interval per step.

It is also worth noting that the presence of multiple breakdowns can be observed in some instances in which the time step is long enough (Figure 5-15). Additionally, significant fluctuations in the gate leakage current are occasionally observed prior to breakdown. It is likely that these fluctuations are due to an increase in electron trap formation prior to breakdown with the large electric field causing electron trapping and de-trapping to occur rapidly.

Summary

High reverse gate bias step-stress from -10 V to -42 V was performed on AlGaN/GaN HEMTs and resulted in a large increase in gate leakage current, with a sharp one order of magnitude increase in current at the critical voltage. The critical voltage of 0.14 μm gate length devices at room temperature was observed to be -30 V. Over 20 devices were step-stressed at temperatures ranging from 25 °C to 150 °C, exhibiting an activation energy of about 42 meV for the critical voltage. As the stress temperature of the devices increased, the critical voltage was found to decrease linearly. This is due to the breakdown of the unintentional interfacial oxide layer from electric field induced bond breakage resulting in the consumption of the oxide interface between the Ni/Au Schottky contact and the GaN cap. Disassociation of oxygen from Ga under high electric fields results in diffusion of oxygen to form NiO_X, likely enhanced by thermal and strain effects. Gate leakage current at V_{CRI} was similar (~10^{-7} A) regardless of stress temperature, indicating similar leakage paths for all stress temperatures. Increasing the time interval at each voltage step indicated a linear time dependence with time to breakdown. Future studies will investigate the effect of steady state TDDB voltage on AlGaN/GaN HEMTs with unintentional oxides.

A)



B)

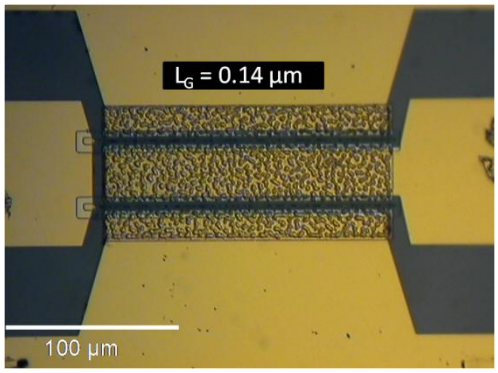


Figure 5-1. AlGaN/GaN HEMT used in temperature dependent study. (A) Cross-section diagram of AlGaN/GaN HEMT. (B) Optical microscope image of device with gate length (L_G) of 0.14 µm.

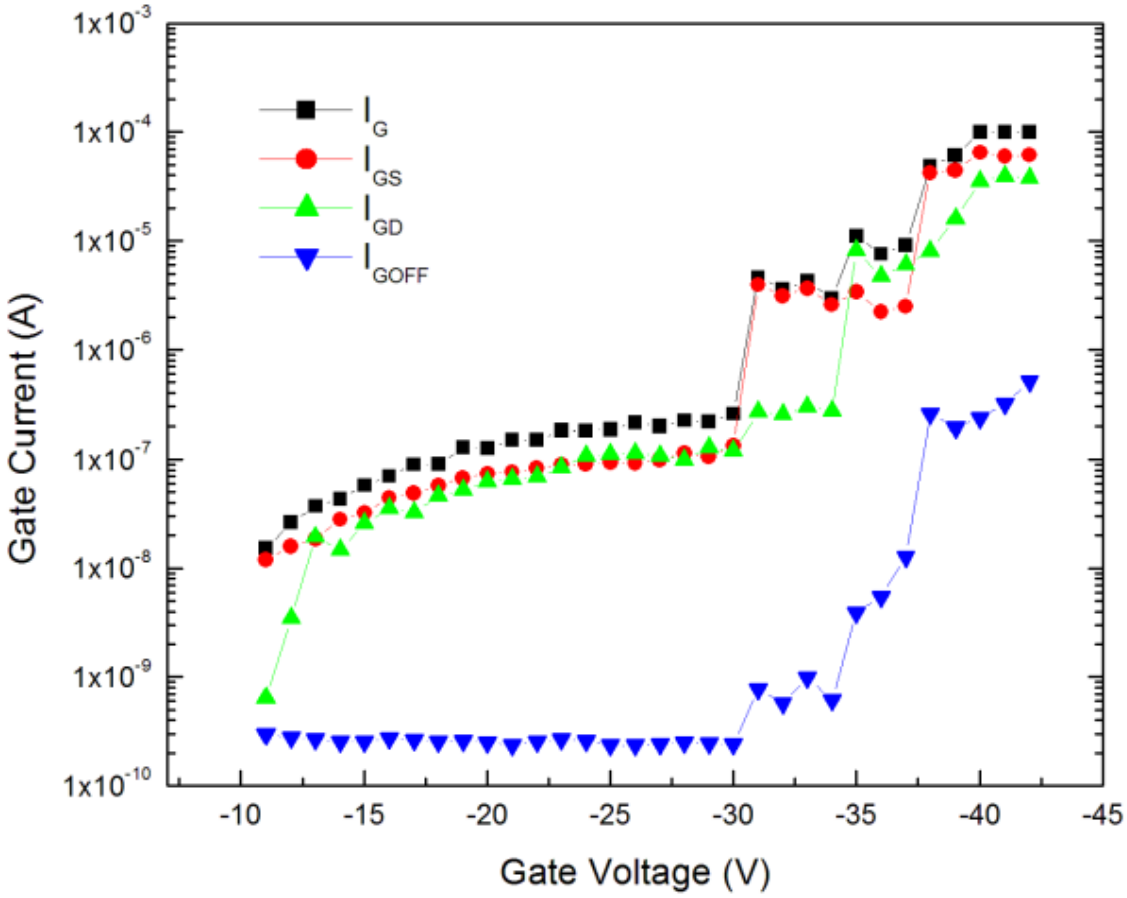
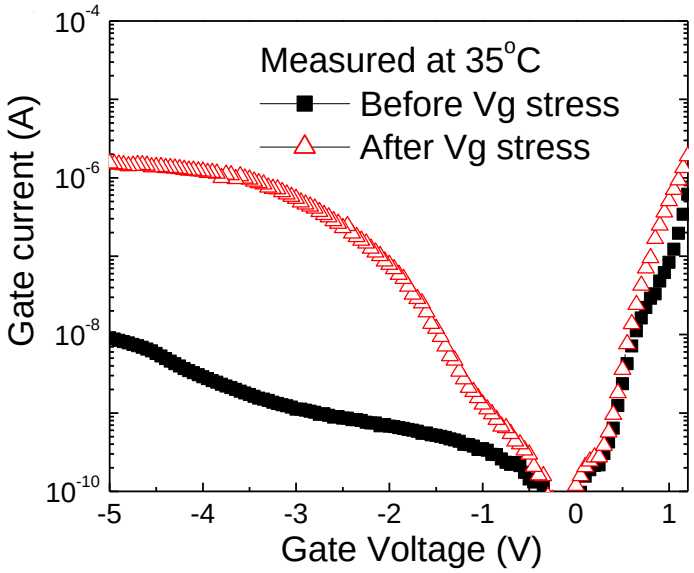
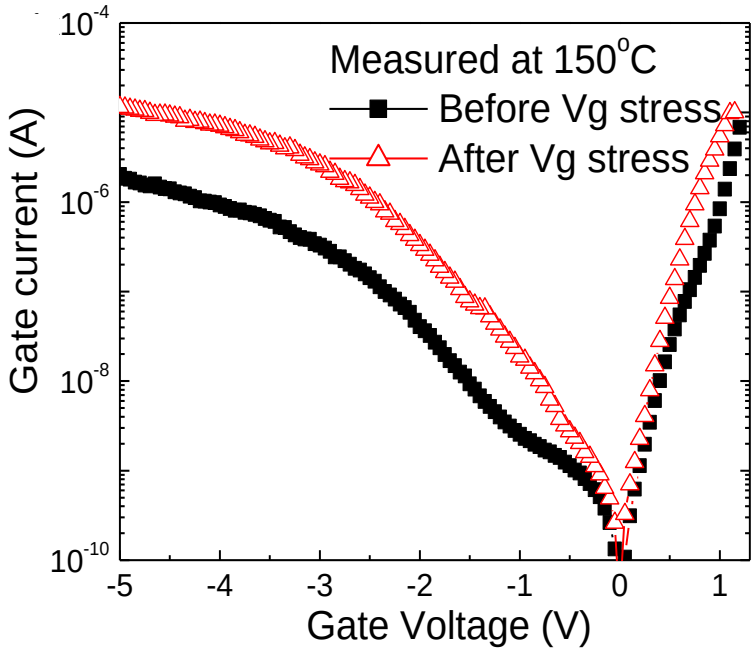


Figure 5-2. Gate current of typical device during off-state step stress at room temperature.



(A)



(B)

Figure 5-3. Gate current-voltage characteristics of 0.14 µm gate length HEMT before and after step-stressing. Baseplate temperatures of (A) 35 °C and (B) 150 °C.

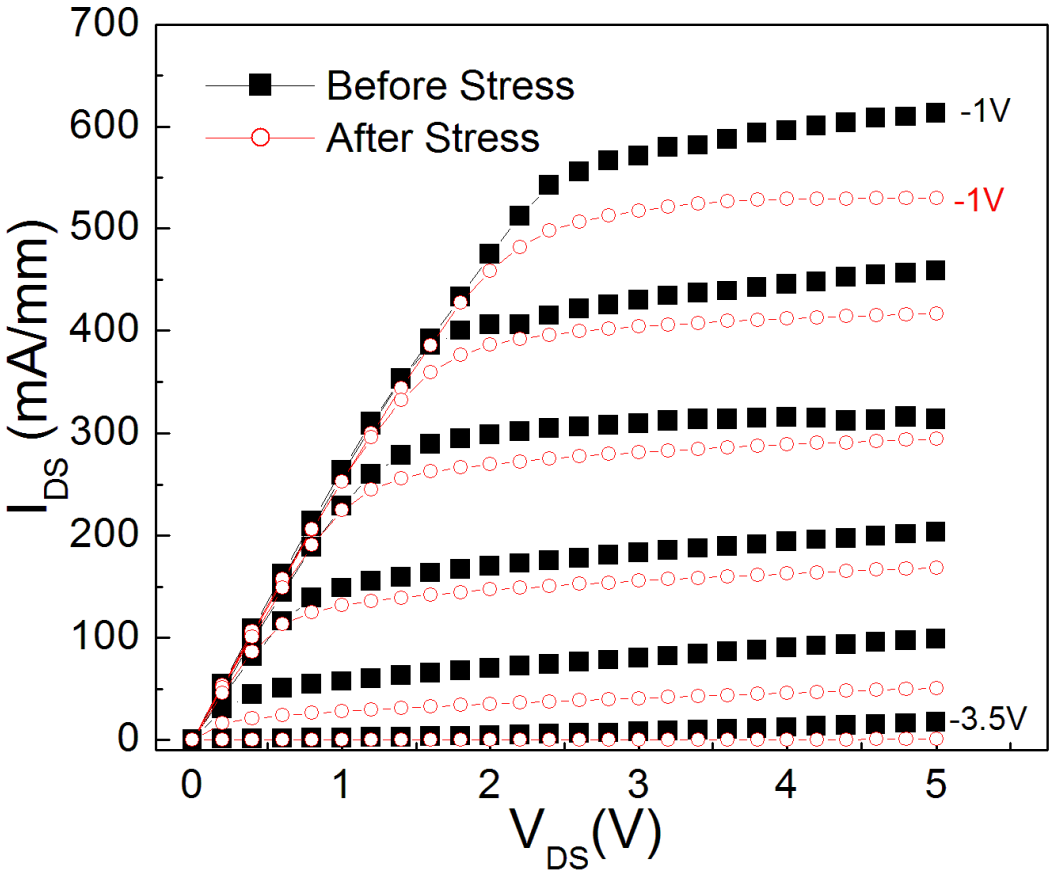


Figure 5-4. Drain current-voltage characteristics of a typical device before and after off-state stress test at 24°C.

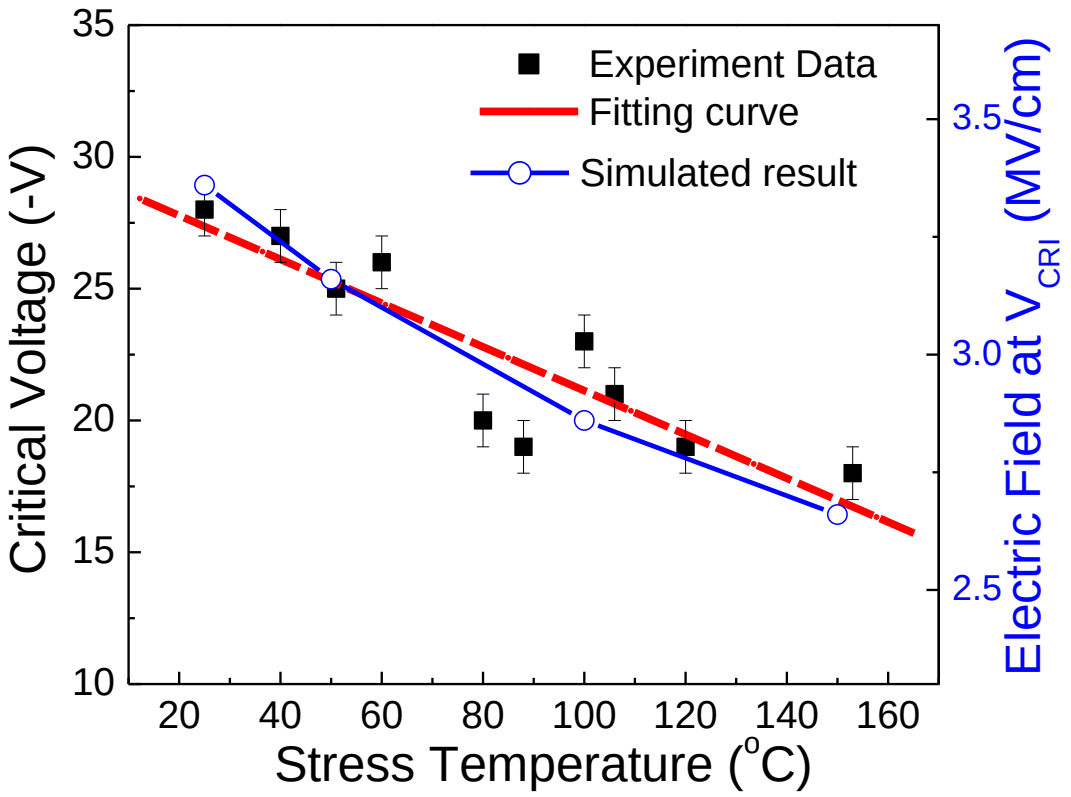


Figure 5-5. Critical voltage vs stress temperature of 0.14 µm gate length HEMT. Maximum electric field at the edge of the Schottky contact vs stress temperature when critical voltage occurs as determined by ATLAS/Blaze 2D simulations.

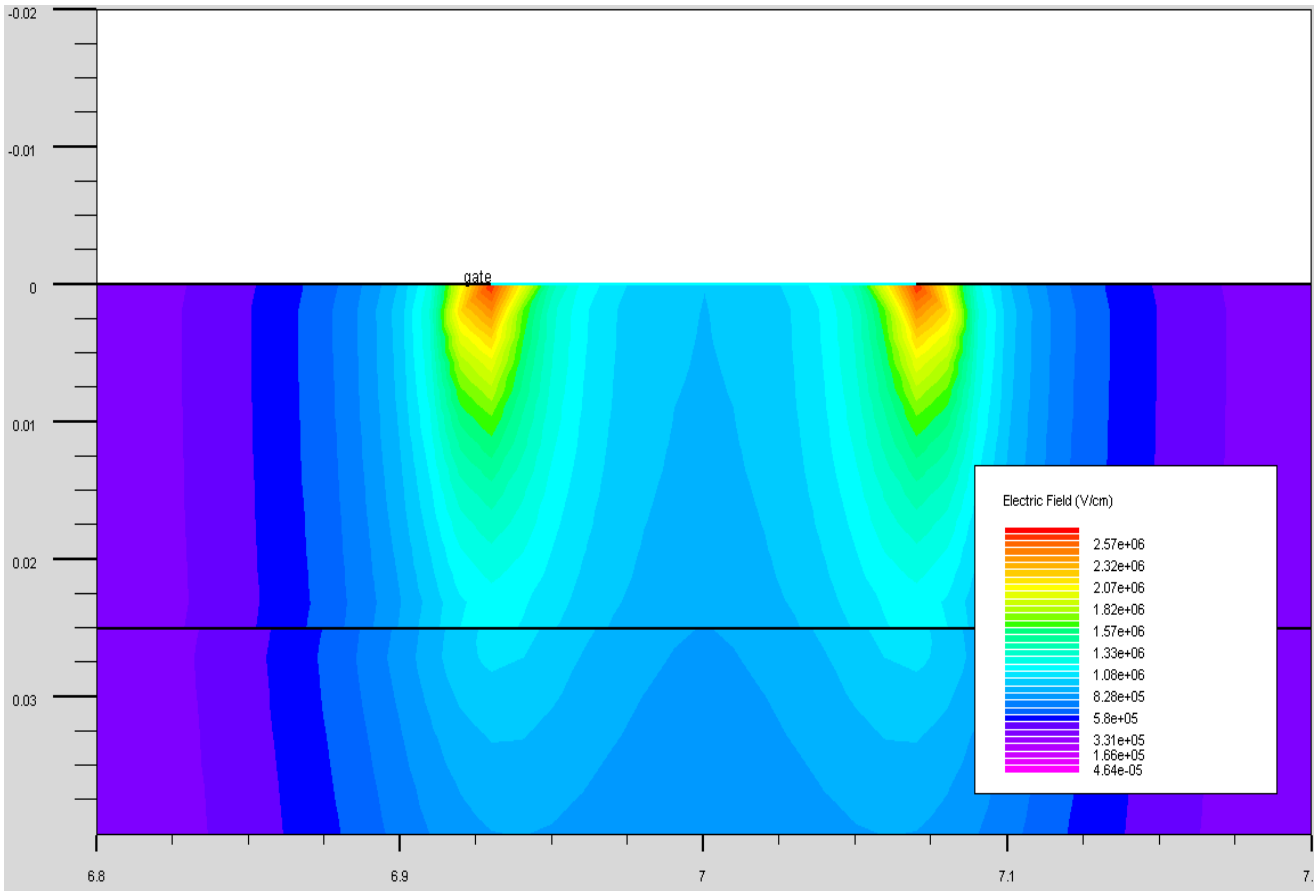


Figure 5-6. ALTAS/Blaze 2D simulation of electric field distribution in AlGaN/GaN HEMTs at -21V and 423 K.

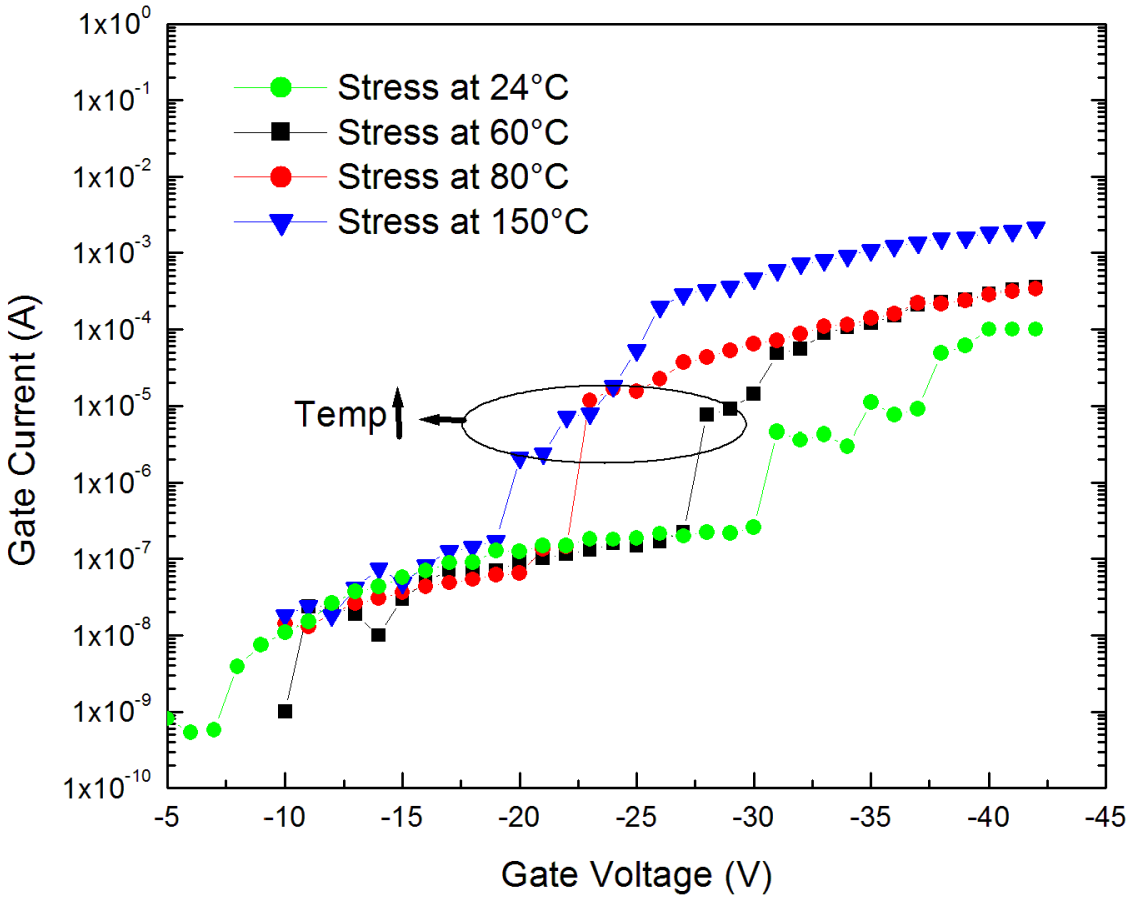


Figure 5-7. Gate current of four AlGaN/GaN HEMTs step stressed from -10V to -42V at 24°C, 60°C, 80°C, and 150°C.

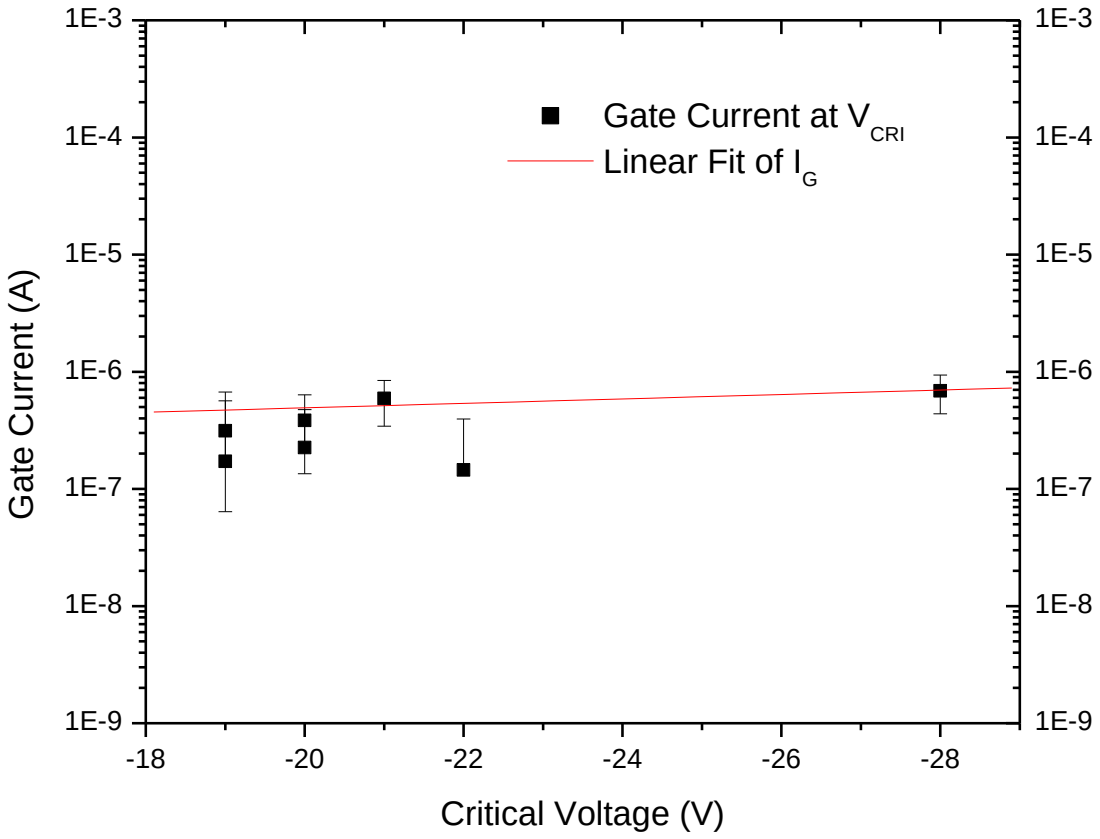


Figure 5-8. Gate current dependence on critical voltage of AlGaN/GaN HEMTs measured at V_{CRI}.

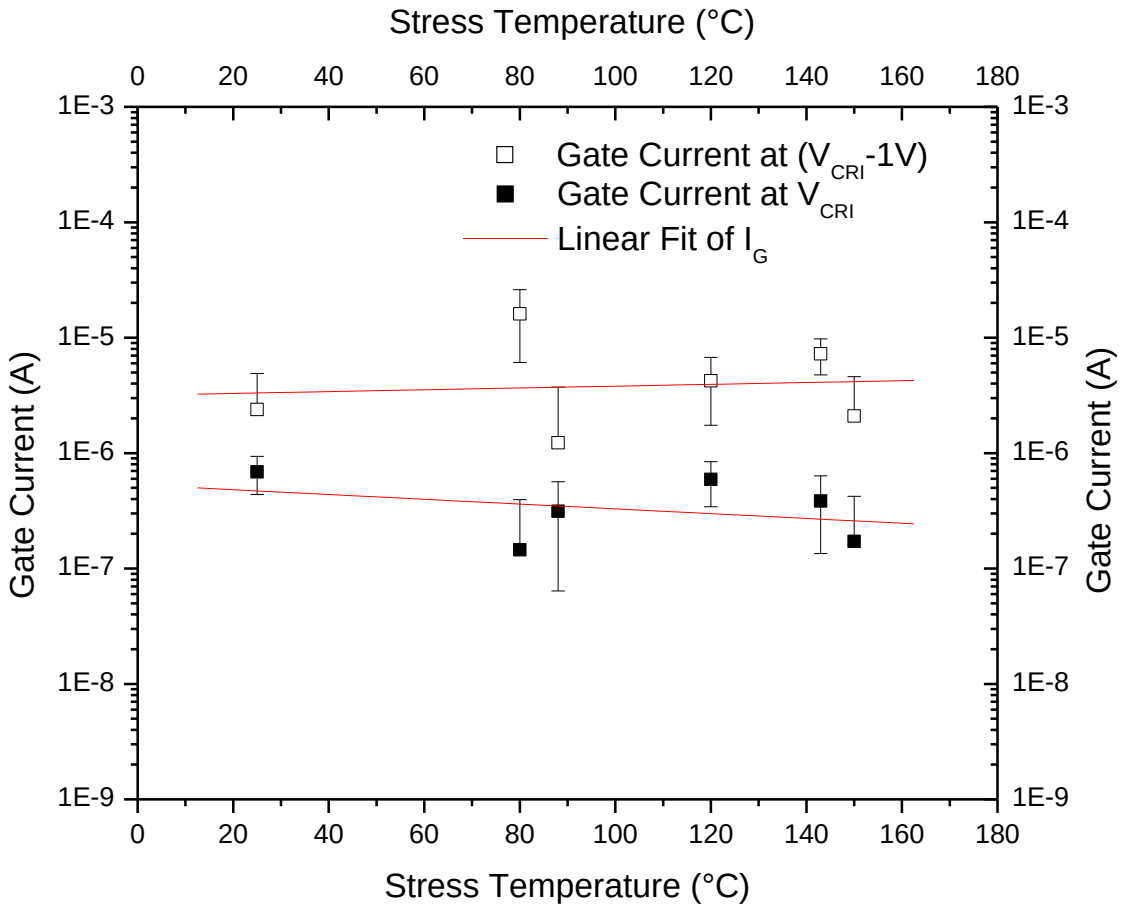


Figure 5-9. Gate current dependence on stress temperature of AlGaN/GaN HEMTs measured at V_{CRI} and after V_{CRI} (V_{CRI} – 1 V).

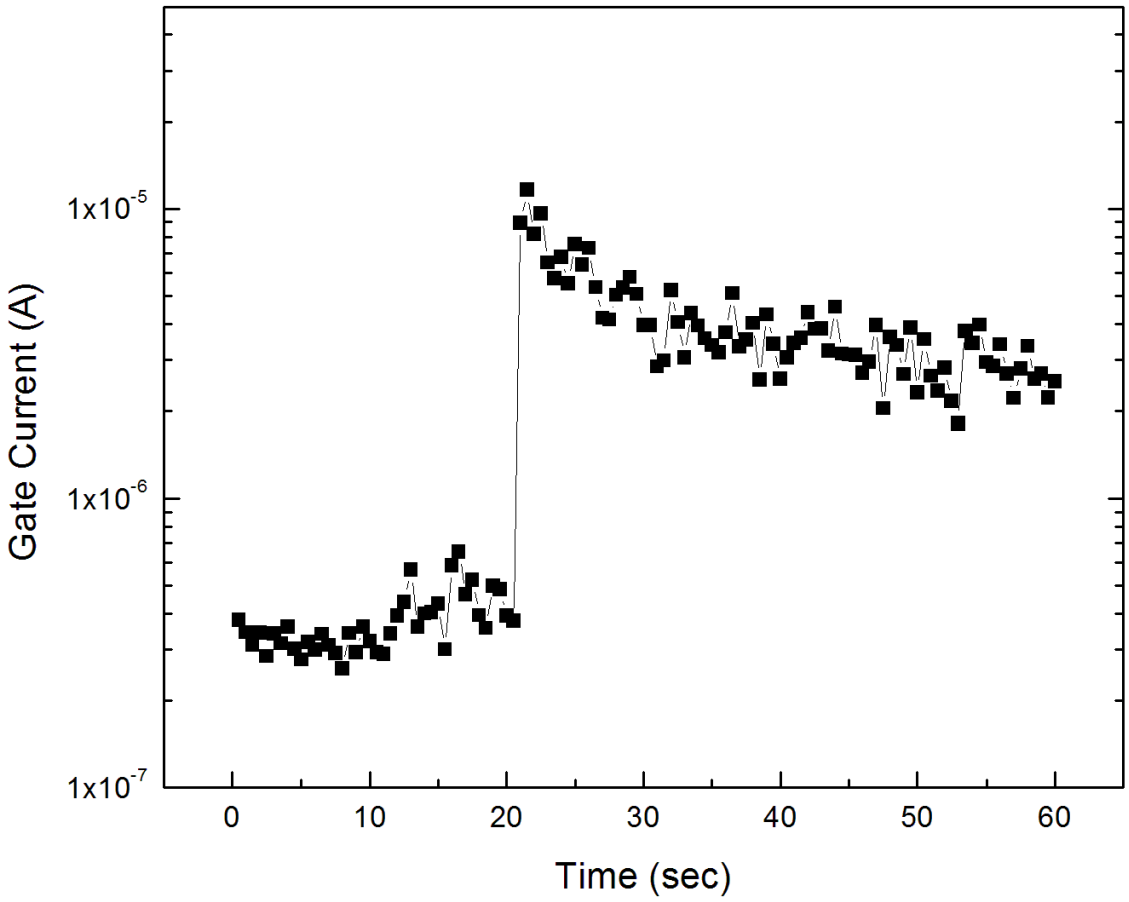


Figure 5-10. Gate leakage current during step stress at 24°C when V_{CRI} occurs (V_{DS} = 0V, V_{GS} = -30 V).

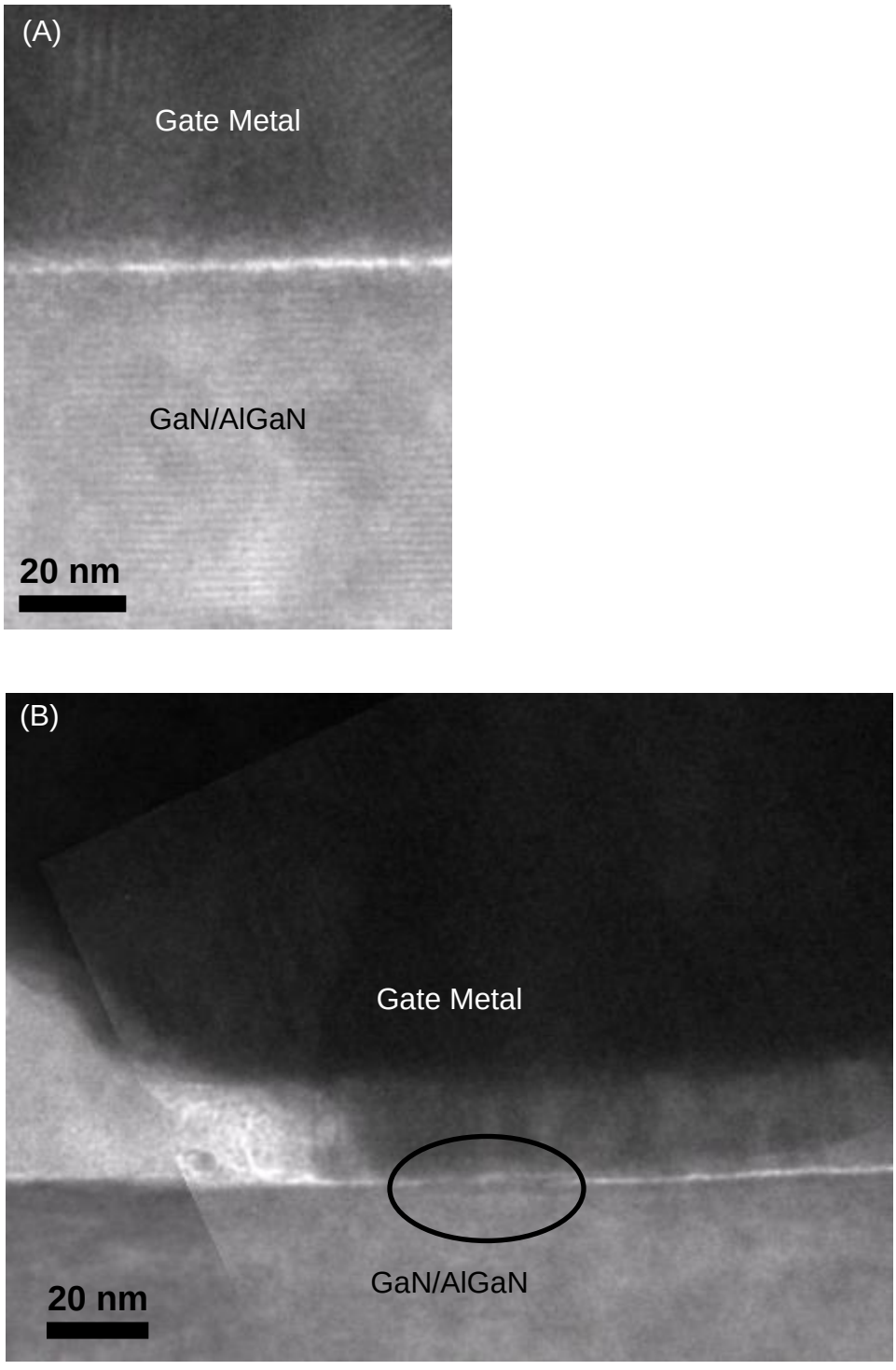


Figure 5-11. Cross-sectional transmission electron microscopy images. TEM image of an (A) unstressed device with interfacial layer present, and (B) device step-stressed to V_{GS} = -42 V at 150°C. Circled region shows oxide consumption due to stress.

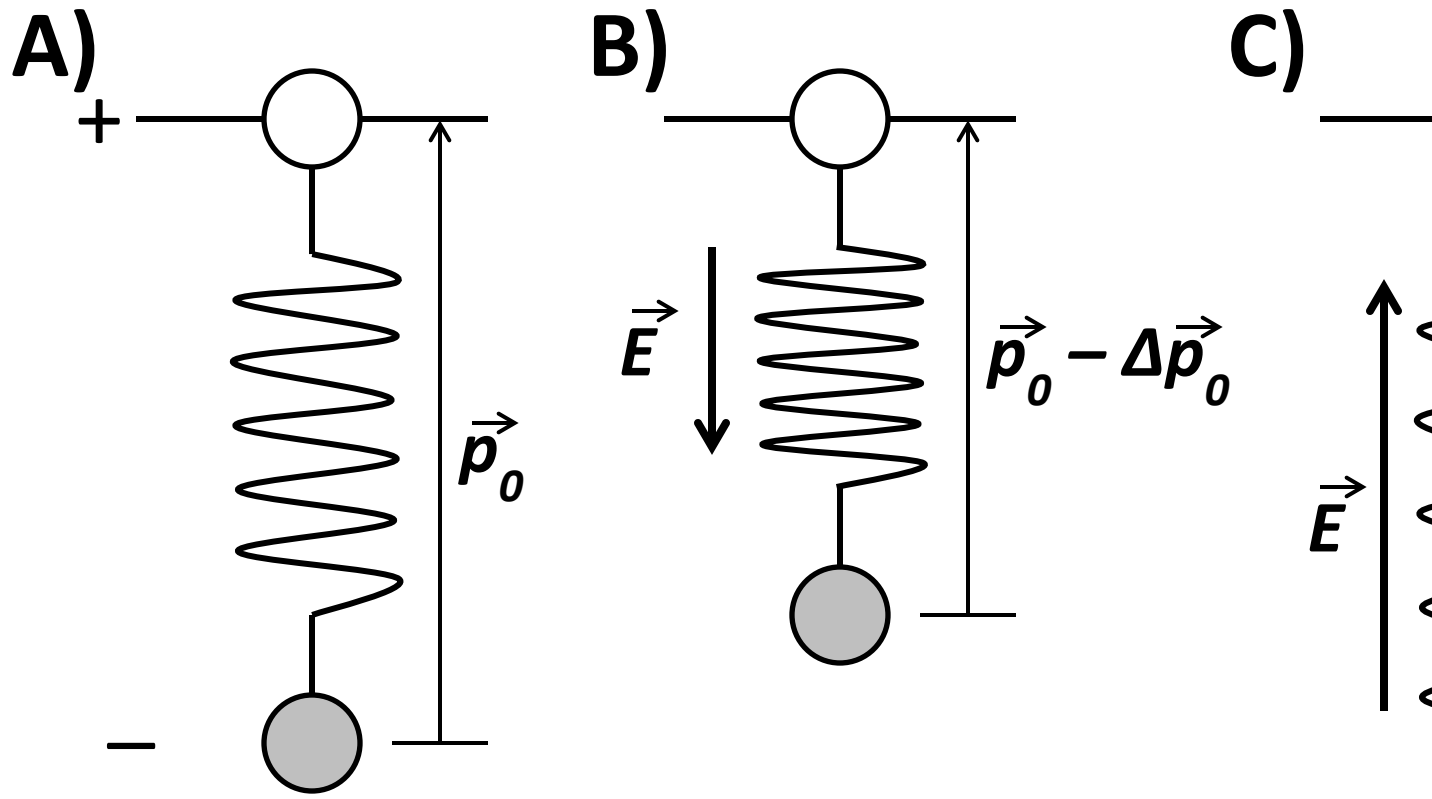


Figure 5-12. The effect of electric field on an intrinsic dipole moment in a dielectric. A) Intrinsic dipole moment with no electric field present B) Effect of dipole moment when subject to an anti-parallel electric field. This results in a compression of the bond length. C) Applied electric field is parallel to dipole moment and results in the extension of the ionic bond.

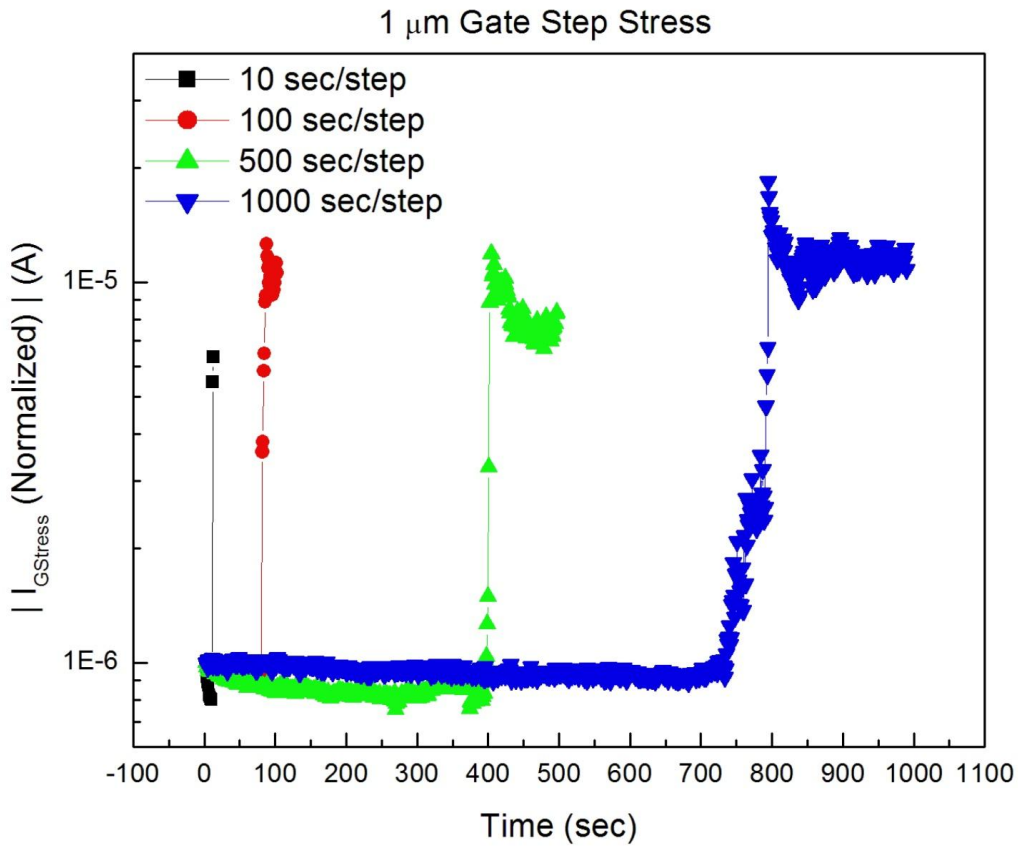


Figure 5-13. Gate current during gate step-stress of 1 μm gate length AlGaN/GaN HEMTs at varying time intervals of 10 sec/step to 1000 sec/step. Figure shows gate current during voltage step at which breakdown occurs. Additionally, transients in the current are present after breakdown.

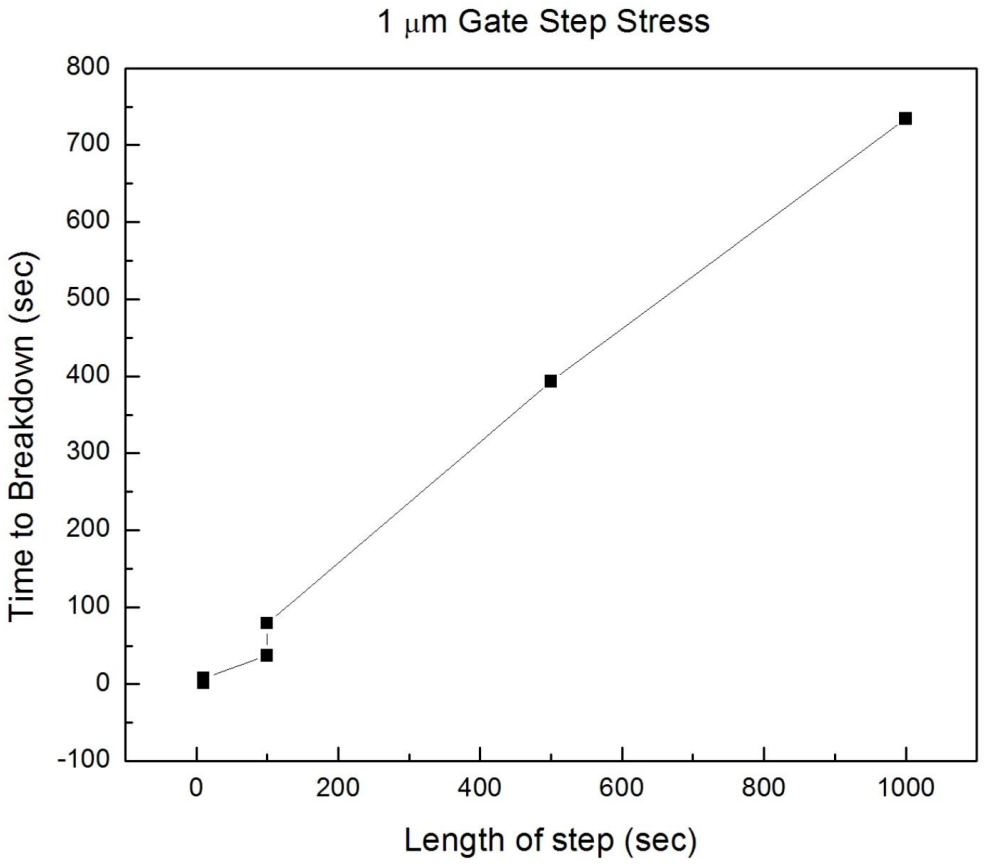


Figure 5-14. Plot showing the time it takes for breakdown to occur during high reverse gate bias step stress with increasing the length of time per step.

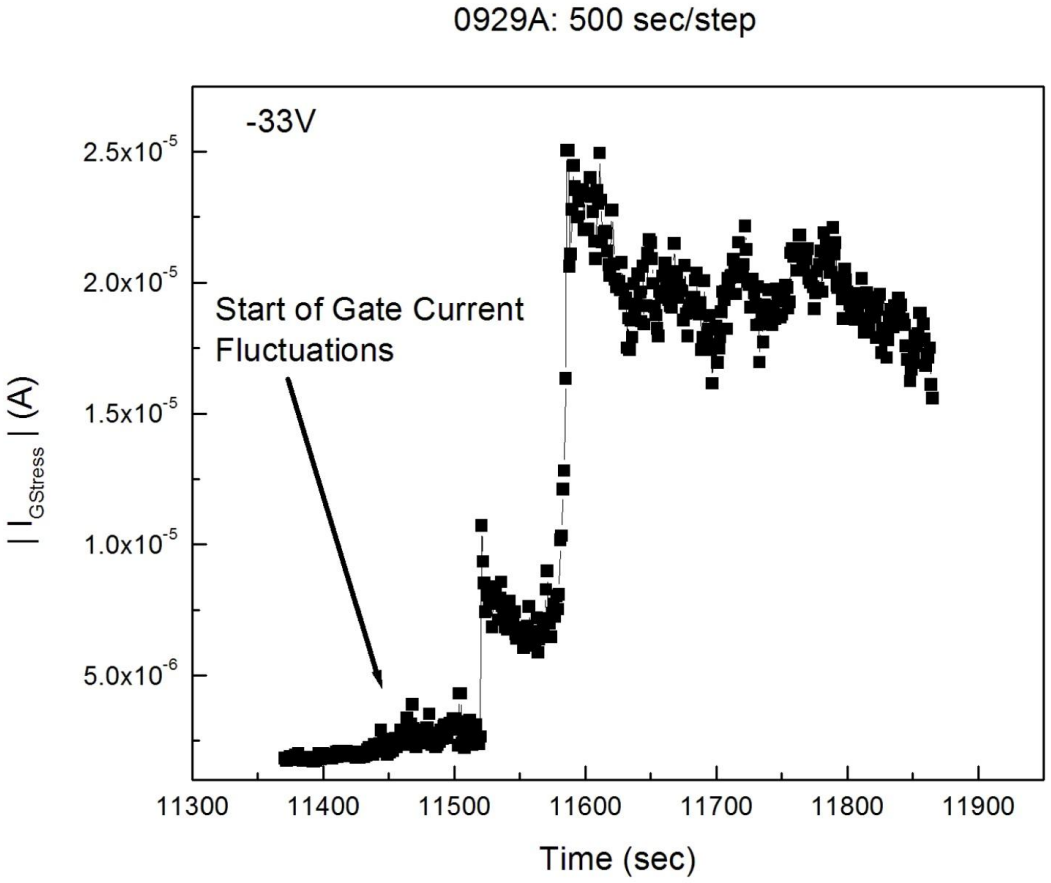


Figure 5-15. Gate current during a single step of high reverse gate bias step-stress (V_{GS} = -33 V) with two clear breakdowns present during the single step. Significant fluctuations in gate current occur prior to the first breakdown, indicating substantial electron trapping and detrapping.

CHAPTER 6
DEGRADATION DUE TO X-BAND OPERATION

Motivation

Reliability and degradation mechanisms of GaN HEMTs under RF operation at room temperature is still of concern and critical importance [32, 71, 98]. High voltage operation can lead to substantial electric fields present in the device, with several research groups reporting permanent degradation in device characteristics due to the inverse piezoelectric effect under dc bias conditions [29, 69, 70, 72, 73, 75, 99]. Additionally, in order to push AlGaN/GaN HEMT applications into higher frequency regimes, even into W-band operation, the gate length must be scaled below 0.2 µm [100]. While the DC and thermal stability of such short gate lengths have been reported, there is still need for extensive investigation of the reliability of the Schottky contacts under RF operation [14, 15, 82, 83]. In this chapter, the effect of drain bias on device degradation under RF operation for 0.125 µm gate length AlGaN/GaN HEMTs on SiC is investigated.

Experimental

Devices with a 0.125 µm gate length were biased under Class AB conditions with a quiescent drain current (I_{DQ}) of 200 mA/mm at drain bias (V_{DS}) of 10 V, 20 V, and 25 V. RF stress up to 350 hours was performed with an AccelRF stress system at 10 GHz, driven into 3dB compression and a baseplate temperature of 30°C. Output power (P_{OUT}), drain current (I_{DS}), gate current (I_{GS}), gain, and power added efficiency (PAE) were monitored throughout the life test.

Results and Discussion

Electrical Stress

As can be seen in Figure 6-1, both P_{OUT} and I_{DS} showed little to no degradation for drain bias of 10V and 20V. However, rapid permanent degradation is present at a drain bias of 25V. A small recovery in both P_{OUT} and I_{DS} is present after pausing at ~25 hours to obtain mid-stress device characteristics, yet, degradation continues at the same rate under RF drive.

Investigation of the degradation mechanisms for AlGaN/GaN HEMTs under high dc bias have shown the onset of rapid, permanent degradation of device characteristics once a critical voltage is reached. This degradation has been attributed to the inverse piezoelectric effect with an increase in source and drain resistance, a small decrease in saturated drain current, a decrease in Schottky barrier height, and a sharp increase in I_{GS} observed [30, 69, 70, 73, 75, 76]. Devices stressed under high dc bias from the same wafer described above with 0.125 µm gate length showed a critical voltage of 22 V [69, 70]. Operating at a drain bias of 25 V, therefore, is above the threshold necessary for the onset of degradation for these particular devices and is consistent with the observed critical voltage during dc stress. RF drive under high voltage and power conditions results in significant changes in the electric field due to an increase in voltage swing available on the loadline. With a load impedance (R_L) of 50 Ω, I_{DQ} of 200 mA/mm and quiescent drain voltage (V_{DQ}) of 25V, one can calculate the maximum drain current and drain voltage seen by the device on the RF load line, 1.87 A/mm and 28V, respectively, from [101]

$$I_{DMAX} = \mathrm{I_{DQ}} + \mathrm{V_{DQ}}/\mathrm{R_L} \tag{6-1}$$

$$V_{DMAX} = V_{DQ} + I_{DQ} * R_L \quad (6\text{-}2)$$

High bias conditions can also lead to an increase in device temperature and limit performance. As the drain bias increased from 20 V to 25 V, PAE increased and led to similar dissipated power at the start of the stress test (3.5 W/mm and 3.77 W/mm, respectively), resulting in similar channel temperatures [88, 102, 103].

Small degradation in saturated drain current (I_{DSS}), less than 10%, occurred for all three drain bias conditions after stress (Figure 6-2) and is consistent with prior reports on RF reliability [15, 98]. For the lowest drain bias of 10 V, a small increase (~3%) in PAE and I_{DS} (~1 mA) was observed during RF stressing for 350 hours, and may indicate that device burn-in is necessary in order to stabilize and improve RF device performance at lower bias conditions. Similarly, minimal degradation in PAE, P_{OUT}, gain, and transconductance occurred for a drain bias of 20 V. An increase in threshold voltage (V_{TH}) was observed for all stress conditions (Figure 6-3), with the largest ΔV_{TH} of 0.37 V at a drain bias of 25 V. Trap formation below the gate or in the channel region results in a decrease in transconductance, which is observed after stress, and would produce a shift in threshold voltage. Trap formation due to defect creation, consistent with the inverse piezoelectric effect, would also result in an increase in gate leakage current through enhanced trap-assisted tunneling [14]. Additionally, the Schottky barrier height reduced from 673 mV to 602 mV after stress at V_{DS} = 25 V.

High dc bias stress of these devices, as well as others, have shown a consumption of the oxide layer present between the Ni/Au Schottky contact and underlying semiconductor layer, and has been correlated to an increase in threshold voltage, decrease in I_{DSS}, and a decrease in Schottky barrier height, all of which was

observed after RF stress [14, 69, 70]. Future studies investigating the role of oxygen during electrical stress are needed to fully understand the stability of the Schottky contact. Although the stress at a drain bias of 25 V was performed for the shortest duration, only ~85 hours, gate leakage current shows the largest increase with almost a three order of magnitude rise in current. Even though device characteristics for drain bias at or below 20 V do not show significant RF degradation (Figure 6-4), the gate current-voltage sweeps with V_{DS} = 0 V (Figure 6-5) indicate that the Schottky contact suffered considerable degradation, with almost a 2 order of magnitude increase in gate leakage current. A rapid increase in gate leakage current observed during high dc bias stress tests indicates the onset of permanent degradation. However, the increase in gate leakage current prior to rapid degradation during RF stress suggests that reliability of devices under dc operation does not fully transcend to RF operation.

Electroluminescence and Photoluminescence

An activation energy of 0.45 eV was obtained for devices stressed with a drain bias of 25 V. Electroluminescence imaging was performed using a deep-depletion CCD camera with a 50X magnification and 5 s integration time to examine the devices before and after stressing. Devices for both stressed and unstressed conditions were forward biased at V_{DS} = 5 V and the gate was modulated so that drain current reached 50 mA. Reverse bias conditions were set to V_{DS} = 0 V and V_{GS} = -10 V. Photoluminescence was performed with a Horiba Micro-Raman utilizing a 325 nm He-Cd laser.

Prior to stress, devices exhibited uniform EL emission under forward bias. However, points of gate leakage appeared with gate bias of -10 V. After RF stress, gate leakage paths were not present on the same channel as present prior to stress (Figure 6-6). It appears from EL emission that degradation due to RF stress may be localized

along the channel, from post-stress EL emission of device under forward bias (Figure 6-6). One device, which met all pre-stress electrical requirements (gate leakage current, V_{TH}, $g_{m\,max}$, I_{DSS}, PAE, P_{OUT}) exhibited non-uniform EL emission under forward bias and no EL emission under reverse gate bias up to V_{GS} of -10 V (Figure 6-7). When stressed at V_{DS} = 25 V under 3.7 dB compression and a baseplate temperature of 100 °C, this device reached failure (drop in P_{OUT} by 1 dB) within 5 minutes of stress. Devices stressed under identical conditions but with uniform EL emission prior to stress did not reach failure for at least 50 minutes.

PL was performed post-stress on the atypical device in which a region of the (top) channel showed no EL emission (Figure 6-7, circled). PL spectra was taken along the entire channel, initially in 25 µm step sizes (Figure 6-8). PL spectra was then obtained in 6 µm step sizes for the region of interest. PL obtained along the channel length showed similar intensity, until spectra was acquired within the region circled (~75 µm) in Figure 6-7. This region resulted in a significant decrease in PL intensity of the GaN band edge emission. No defect peaks were present in any of the spectra taken. This sharp decrease in intensity after stress in the region of interest indicates that there is an increase in non-radiative trap formation.

Cathodoluminescence

CL spectra performed on the atypical device indicated a difference between the “defective” region (no EL emission and a decrease in PL, circled region in Figure 6-7) and a “stressed” region (uniform EL emission). By varying the electron beam energy, it is possible to perform a depth analysis in the channel by CL. Approximating Equation 2-

31, one can determine the penetration depth based upon the density of the material under study (6.1 g/cm^3 for GaN) and the electron beam energy (E) by

$$R_B(\mu m) = \left(\frac{0.052}{\rho}\right) * E^{1.75} \quad (6\text{-}3)$$

where R_B is the penetration depth [104]. By varying the electron beam energy from 2.5 kV to 30 kV, it allows one to investigate defects ranging from 40 nm to 3.3 µm deep in the device.

By first analyzing an unstressed device, it is possible to establish a baseline of defects present in the "as-grown" material as a function of depth. In Figure 6-9A, one can see that the GaN near-band-edge (NBE) at 3.4 eV and blue emission (BL) peak at ~2.9 eV increase until an electron beam energy E_B of 10 kV (~480 nm) for an unstressed device. The BL peak has been attributed to O_{Ga} defect, N vacancies, or from Fe-doping of the buffer layer [105-107]. With a penetration depth of 480 nm, these defects should be well beyond the active region of the device. The yellow emission (YL) peak at 2.2 eV becomes predominant at 20 kV (~1.6 µm) indicating that this defect peak is due to traps and defects deep within the GaN buffer layer (Figure 6-9A). The YL peak has been mainly attributed to V_{Ga} defects or the V_{Ga} - O_N complex [40, 104, 108, 109].

After subjecting the device to RF stress of 10 GHz under Class AB conditions until failure (P_{OUT} drops by 1 dB), the CL intensity at 5 kV (~140 nm) of BL peak is similar to that of the unstressed peak though the GaN NBE and BL peak ratio dramatically increases (Table 6-1). Though the overall ratio for the GaN NBE to the YL peak decreases in the stressed device, the total CL intensity for both peaks increases significantly with the GaN NBE emission peaking at 20 kV (1.6 µm). This increase in YL peak at lower voltages after stress indicates that more of these defects, likely V_{Ga} are

now closer to the active region of the device then before stress and could be the reason for failure in the device. BL peak intensity is fairly similar to pre-stress levels. CL images taken in panchromatic mode of an unstressed device and a RF stressed device show an increase in threading dislocations after stress with a beam energy of 20 kV (1.6 μm) (Figure 6-10).

GaN NBE maximum peak intensity is reached in an unstressed device at 30 kV (~3.3 μm), for a stressed device at 20 kV (~1.6μm), and 10 kV (~480 nm) for the defective region of the stressed device. The BL maximum peak intensity for all three cases is 20 kV (Figure 6-9C). Perhaps most telling is that both the GaN NBE emission and the YL peak are larger in the “defective” region as opposed to pre-stress emission as well as “stressed” regions of the channel (Figure 6-11). The stressed region actually showed a slightly lower YL maximum at 30 kV compared to the unstressed channel. However, the defective region has a YL peak at 30 kV that is 3 times larger than the unstressed YL peak and 4 times larger than the stressed YL peak. Even at lower energies, such as 5 kV (~140 nm) the YL peak in the defective region is 5 times larger. The large disparity between the YL peak in the defective region of the channel and the rest of the channel indicates that a greater number of Ga vacancies are present in this region at all penetration depths. The localized formation of defects is likely the cause for premature failure in the device. CL spectra of the defective region was not performed prior to stress, so it is not possible to differentiate if the defects were present prior to electrical stress or if their formation occurred during stress.

Effect of Gate Length

As the gate length of the devices decreases below 0.2 μm, the stability of the Schottky contact becomes increasingly important. The decreasing interaction area for

submicron gate lengths can cause early failure as the voltage and current applied to the gate does not scale accordingly with the gate dimensions. To this end, the stability of the Schottky contact as a function of gate length is investigated.

Three gate lengths were examined, 0.125 µm, 0.14 µm and 1µm. The devices were stressed on a Focus Microwave Load-Pull system at 10 GHz, Class AB conditions, with a quiescent drain current of 200 mA/mm, and up to 3.9 dB compression. The input power was 13.8 dBm, which correlated to about 75% of maximum power, and a drain bias of 20 V. During the stress, the following parameters were monitored: V_{DS}, V_{GS}, I_{DS}, I_{GS}, P_{IN}, P_{OUT}, gain, collector efficiency, & PAE.

Overall, all three gate lengths showed excellent stability in dc device characteristics, with less than 5% change in threshold voltage, maximum transconductance, and saturated drain current for up to 75 hours of stress (Figure 6-12). These results indicate that there is minimal trap formation and channel damage due to RF stress. Gate leakage current showed significant increase for the submicron gate length, almost two orders of magnitude, after stress (noise is due to limit of resolution in nA range) (Figure 6-13). Conversely, there was no increase in gate leakage current, either forward or reverse for the micron gate length. Additionally, RF device characteristics showed a strong dependence on gate length. Submicron gate lengths exhibited similar degradation in terms of PAE, gain, and output power. Submicron gate lengths showed upwards of 80 % degradation for all three RF parameters, whereas the 1 µm gate length displayed less than 20 % degradation (Figure 6-14).

These results indicated that under Class AB conditions for X-band operation with the current technology, larger gate lengths will be necessary in order to obtain excellent

long term stability. The degradation of sub-micron gate lengths is primarily due to degradation of the Schottky contact, which is evident in the I_{GS} vs. V_{GS} curves.

Summary

In summary, sub-micron gate length AlGaN/GaN HEMTs show excellent reliability up to a drain bias of 20 V under 3dB compression, however the Schottky contact properties show substantial degradation in terms of threshold voltage shift, gate leakage current, and Schottky barrier height increase. This indicates the gate contact is the cause for device failure under long-term lifetests. Additionally, RF stressing at a drain bias of 25 V is above the threshold necessary for the onset of degradation and resulted in rapid, permanent degradation in P_{OUT} and $I_{DS.}$ EL and PL indicate an increase in non-radiative trap formation after RF stress.

Under 3.9 dB compression, 75% maximum output power, and a drain bias of 20 V, AlGaN/GaN HEMT degradation exhibited a strong dependence on gate length. Devices with a large gate length, 1 µm, showed the greatest stability with no observed degradation in both dc and RF device characteristics. Sub-micron gate length devices, however, demonstrated degradation that was due to Schottky contact failure, with an observed two order of magnitude increase in gate leakage current and a decrease in PAE, gain, and output power. Greater stability of the Schottky contact will be necessary in order to improve device reliability and performance for sub-micron gate devices.

Additionally, EL and PL have shown to be a useful tool in order to localize regions of interest that can then be further analyzed with CL both before and after stress. CL indicates that an increase V_{Ga} occurs after RF stress. Additionally, these defects are at shallower levels than before stress and are likely causing traps which leads to enhanced device degradation. Further studies are needed in order to investigate the

origin of the defects in order to determine if the localized increase in Ga vacancies is due to growth/process or due to electrical stress. The concentration of defects, not observed in devices that exhibited typical failure rates, likely resulted in early failure. Further analysis of the defective region by means of transmission electron microscopy is also needed to further understand the degradation mechanism.

Table 6-1. Peak intensity of cathodoluminescence spectra at various beam energies for yellow, blue and near band edge emission. Peak intensities for A) unstressed channel, B) stressed channel, and C) defective region of stressed channel.

A)

Unstressed						
Beam Energy (eV)	GaN	BL	YL	GaN/BL	GaN/YL	BL/YL
2.5	43.0	15.0	15.0	2.9	2.9	1.0
5.0	5094.0	62.5	28.5	81.5	178.7	2.2
10.0	24148.5	192.5	92.5	125.4	261.1	2.1
20.0	19653.5	234.5	398.0	83.8	49.4	0.6
30.0	36059.5	184.0	4143.0	196.0	8.7	0.0

B)

Stressed						
Beam Energy (eV)	GaN	BL	YL	GaN/BL	GaN/YL	BL/YL
2.5	170.0	10.0	24.0	17.0	7.1	0.4
5.0	14192.5	33.0	88.0	430.1	161.3	0.4
10.0	14251.0	135.0	73.0	105.6	195.2	1.8
20.0	43246.5	215.5	1519.5	200.7	28.5	0.1
30.0	21457.5	200.0	3190.5	107.3	6.7	0.1

C)

Defective						
Beam Energy (eV)	GaN	BL	YL	GaN/BL	GaN/YL	BL/YL
2.5	168.0	12.0	23.5	14.0	7.1	0.5
5.0	24080.0	35.0	144.5	688.0	166.6	0.2
10.0	75143.0	132.0	539.5	569.3	139.3	0.2
20.0	67862.0	281.5	7733.0	241.1	8.8	0.0
30.0	24731.0	159.5	12768.0	155.1	1.9	0.0

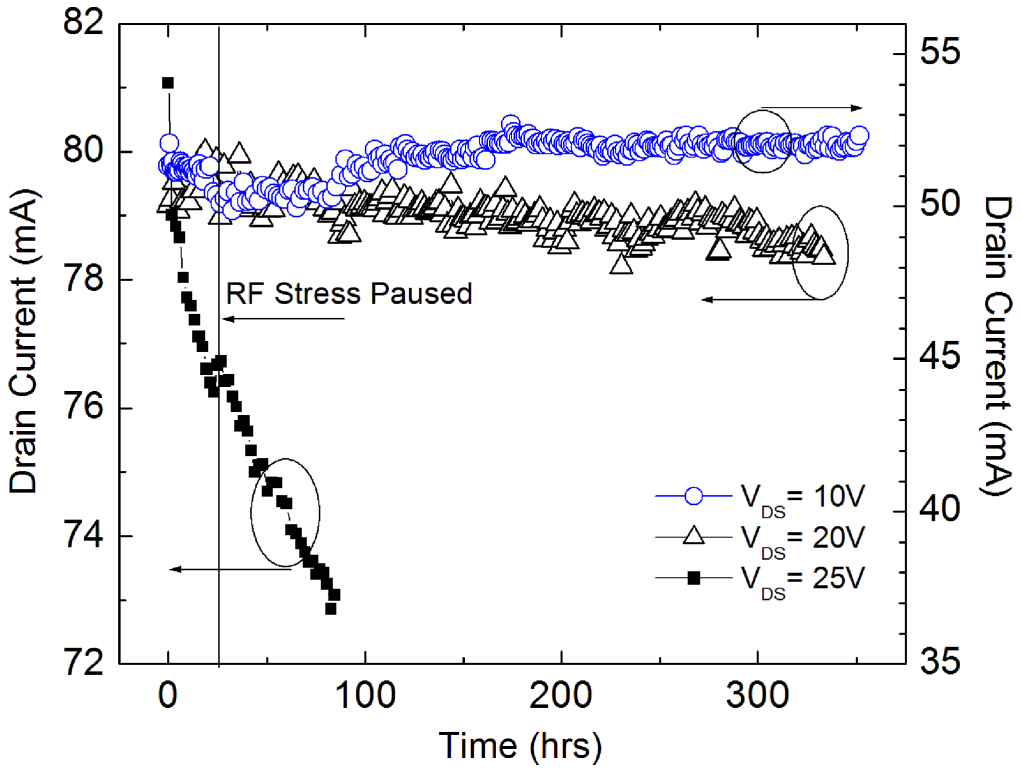


Figure 6-1. Drain current during RF stress at 10 GHz under 3 dB compression of 0.125 µm gate length AlGaN/GaN HEMT.

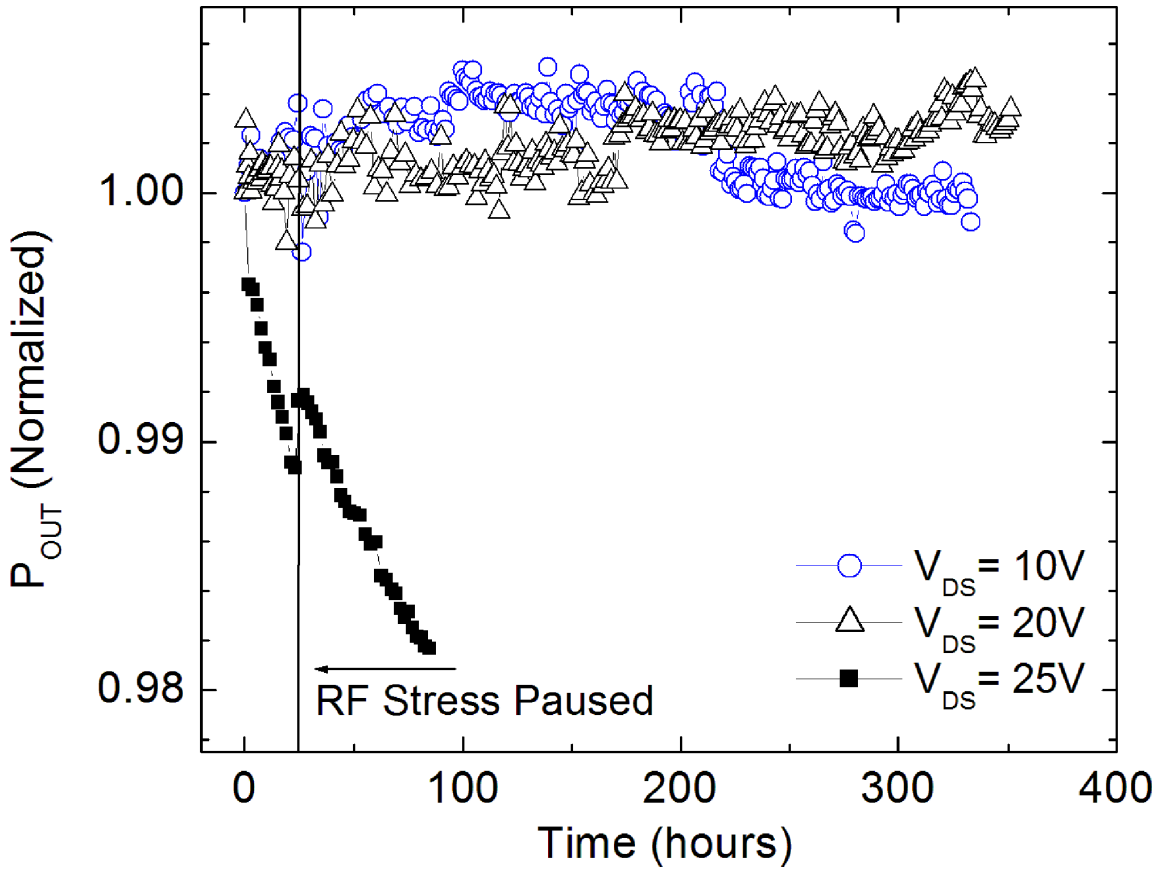


Figure 6-2. Output power during RF stress at 10 GHz under 3 dB compression of 0.125 µm gate length AlGaN/GaN HEMT.

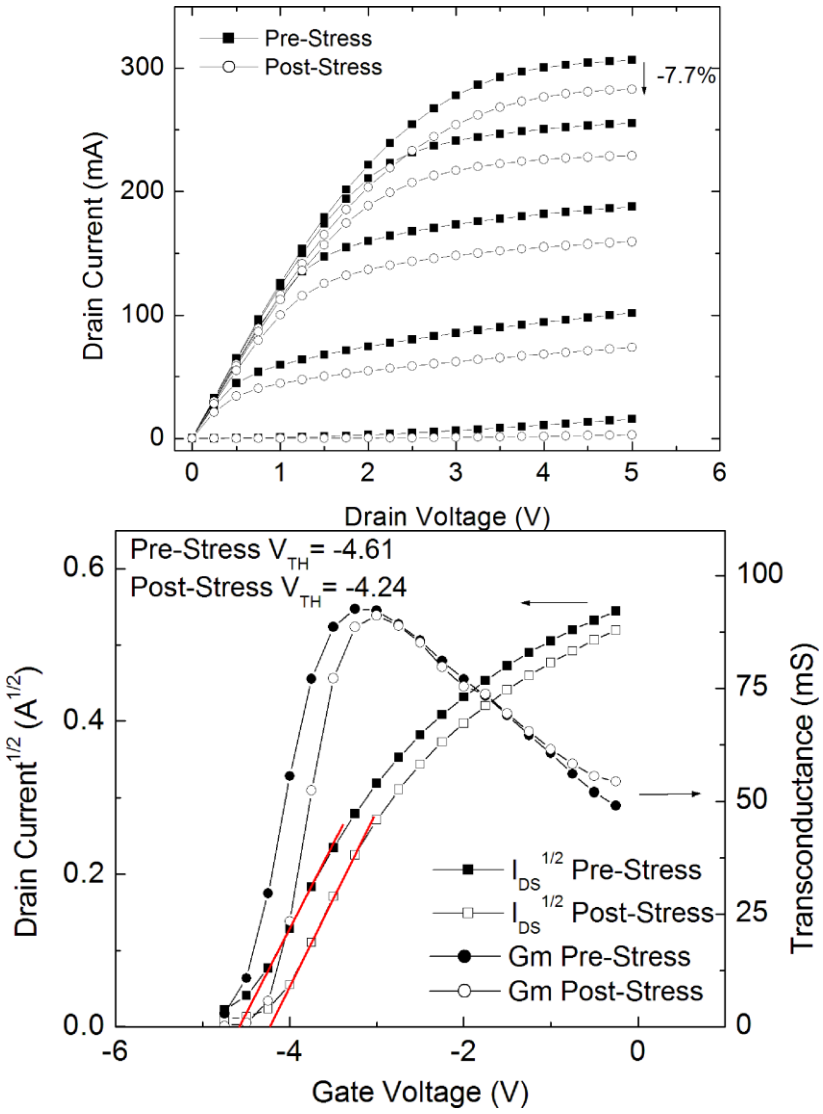


Figure 6-3. Effect of RF stress on dc device characteristics. (A) Typical drain current-voltage and (B) transconductance characteristics before and after RF stress at drain bias of 25 V.

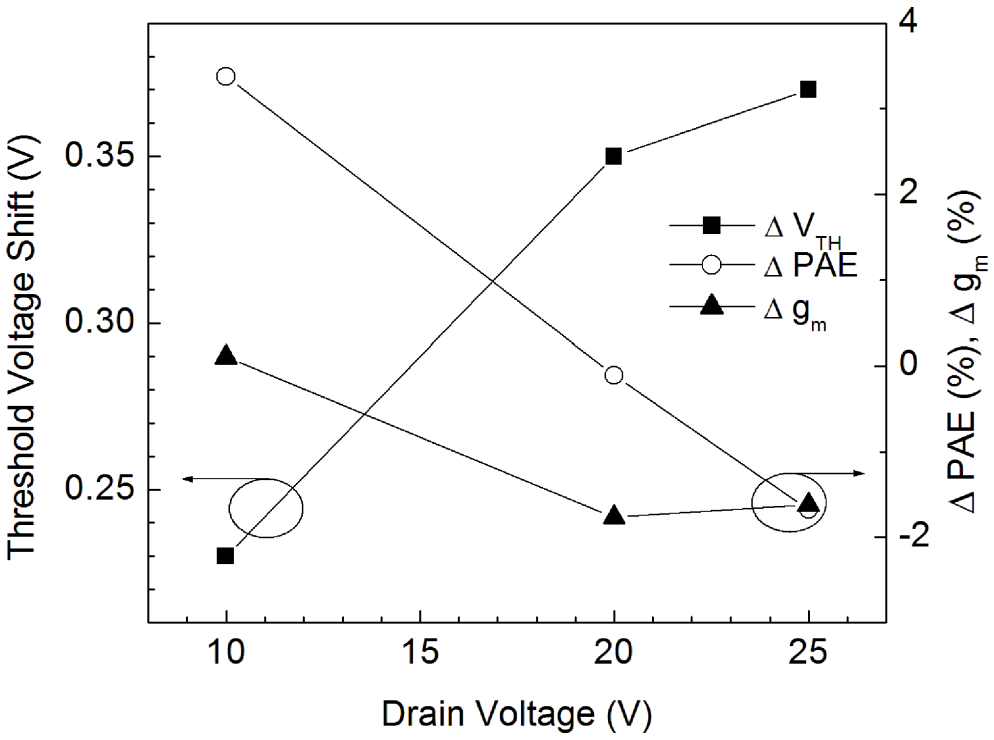


Figure 6-4. Change in device characteristics vs. drain bias of 10, 20 and 25 V after 10 GHz RF stress.

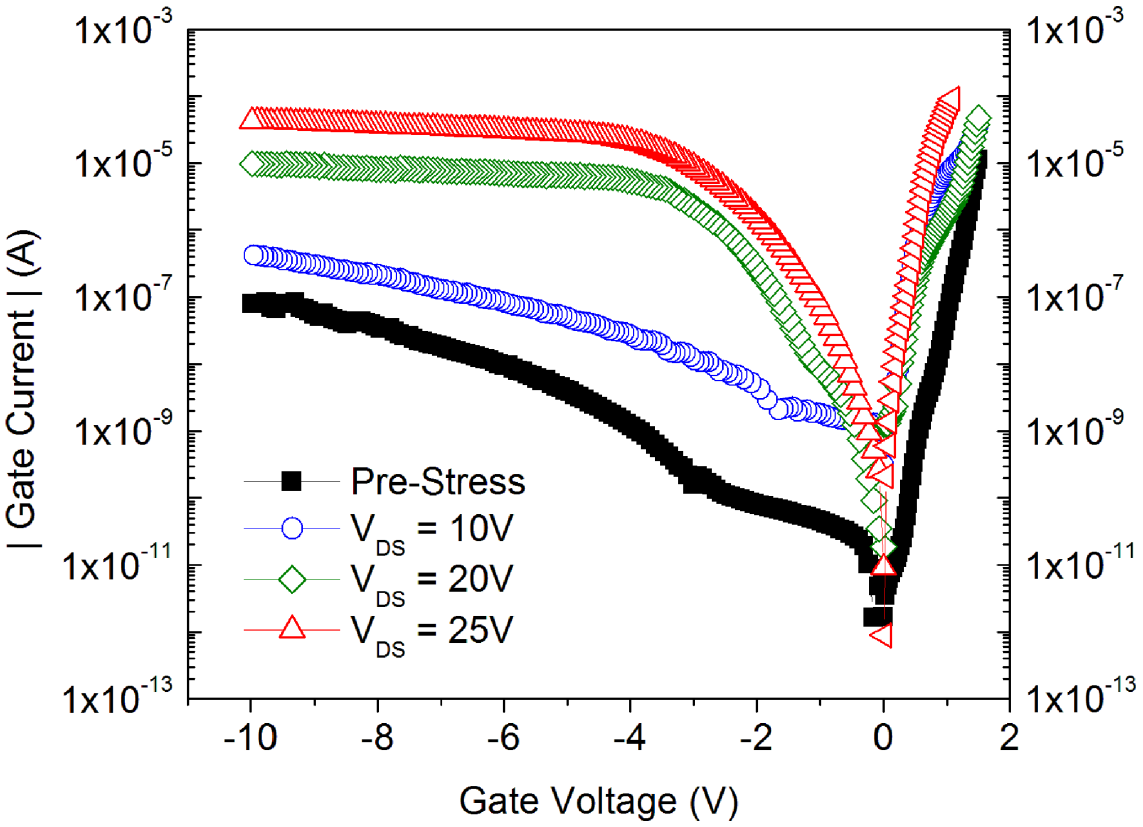


Figure 6-5. Gate current – voltage curves before and after RF stress at V_{DS} = 10, 20 and 25V.

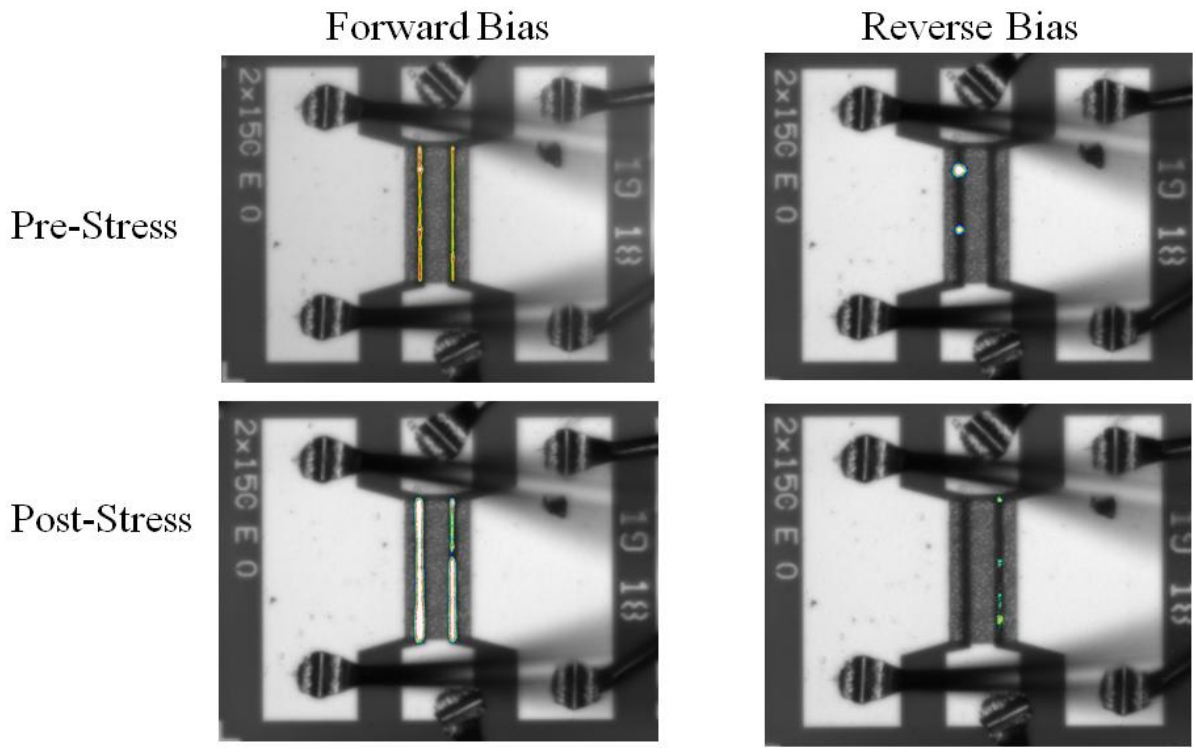


Figure 6-6. Electroluminescence of HEMTs pre and post RF stress at a drain bias of 20 V. EL emission was observed for both a forward bias of V_{DS} = 5 V and gate bias modulated in order to obtain a drain current of 50 mA. Reverse bias conditions were set to V_{DS} = 0 V and V_{GS} = -10 V.

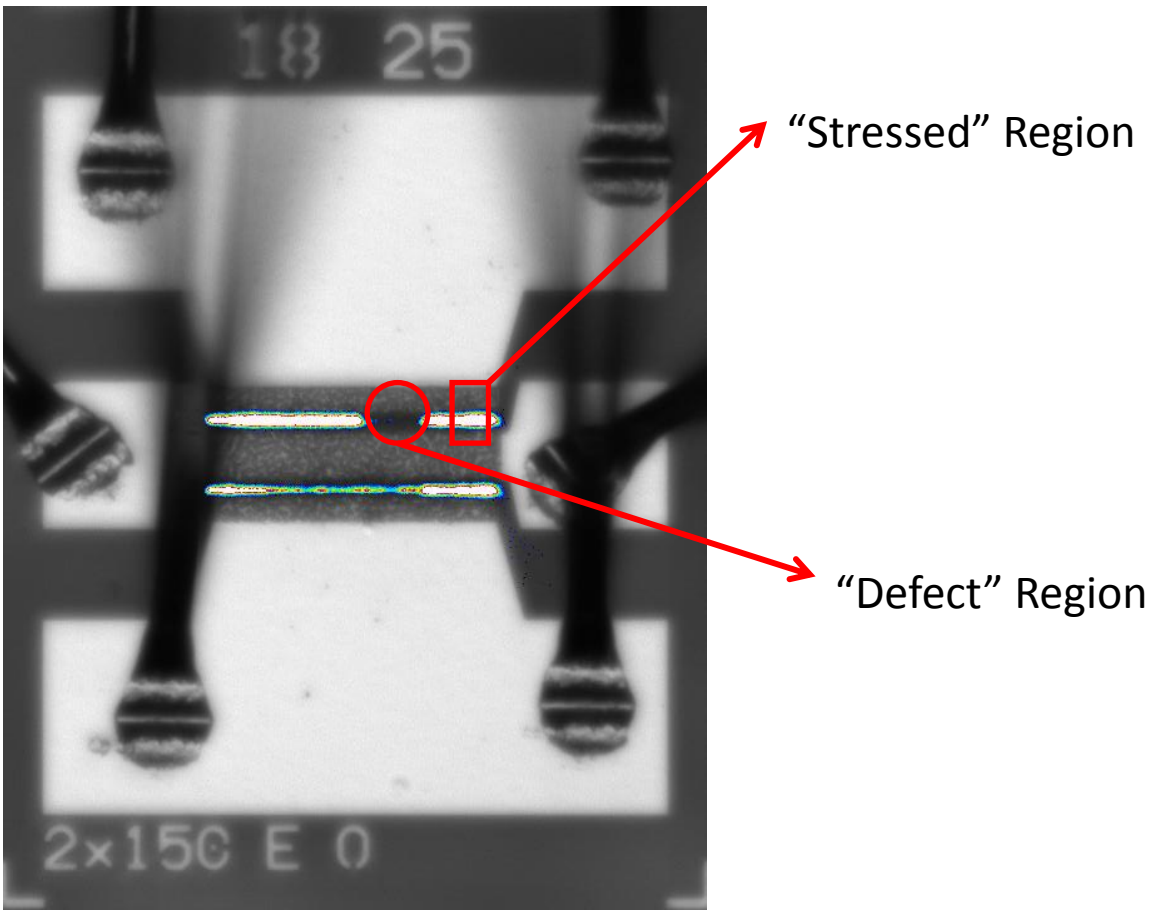


Figure 6-7. Electroluminescence of AlGaN/GaN HEMT after stress at V_{DS} = 25 V and Class AB operation. Circled region indicates area of channel that has an increase in non-radiative trap formation after stress. Uniform EL emission during forward bias was not observed prior to stress. Photoluminescence and cathodoluminescence spectra taken at the region in the square (labeled “stressed”) and the region in the circle (labeled “Defect”).

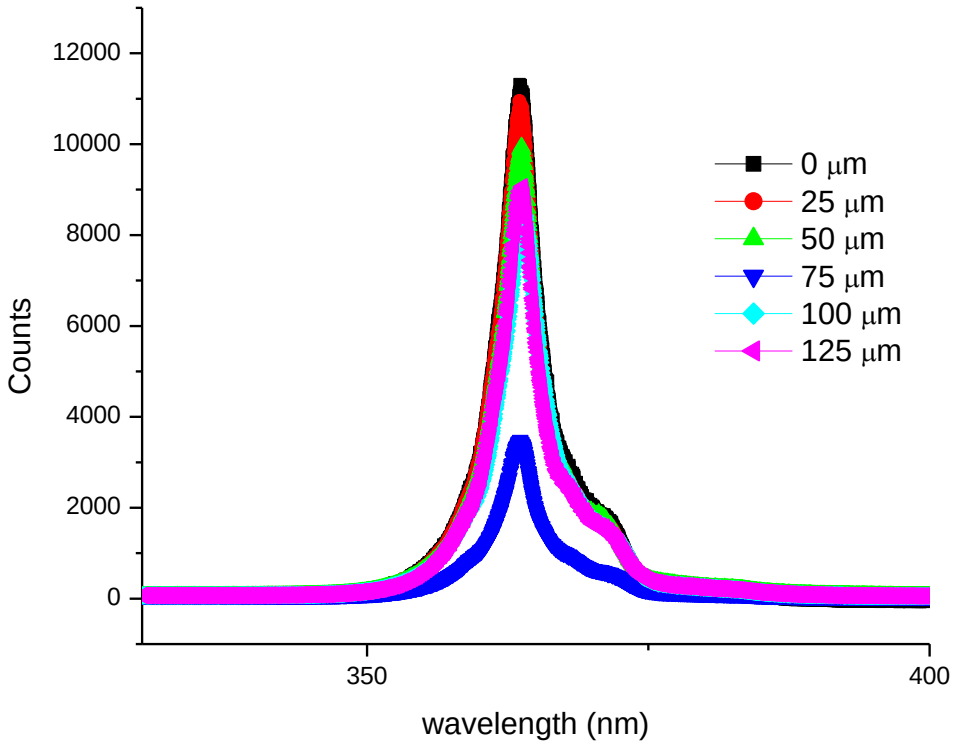


Figure 6-8. Photoluminescence spectra taken from device with non-uniform EL emission after RF stress. Sharp decrease in GaN band edge emission at 75 μm along channel indicative of increase of non-radiative trap formation due to electrical stress.

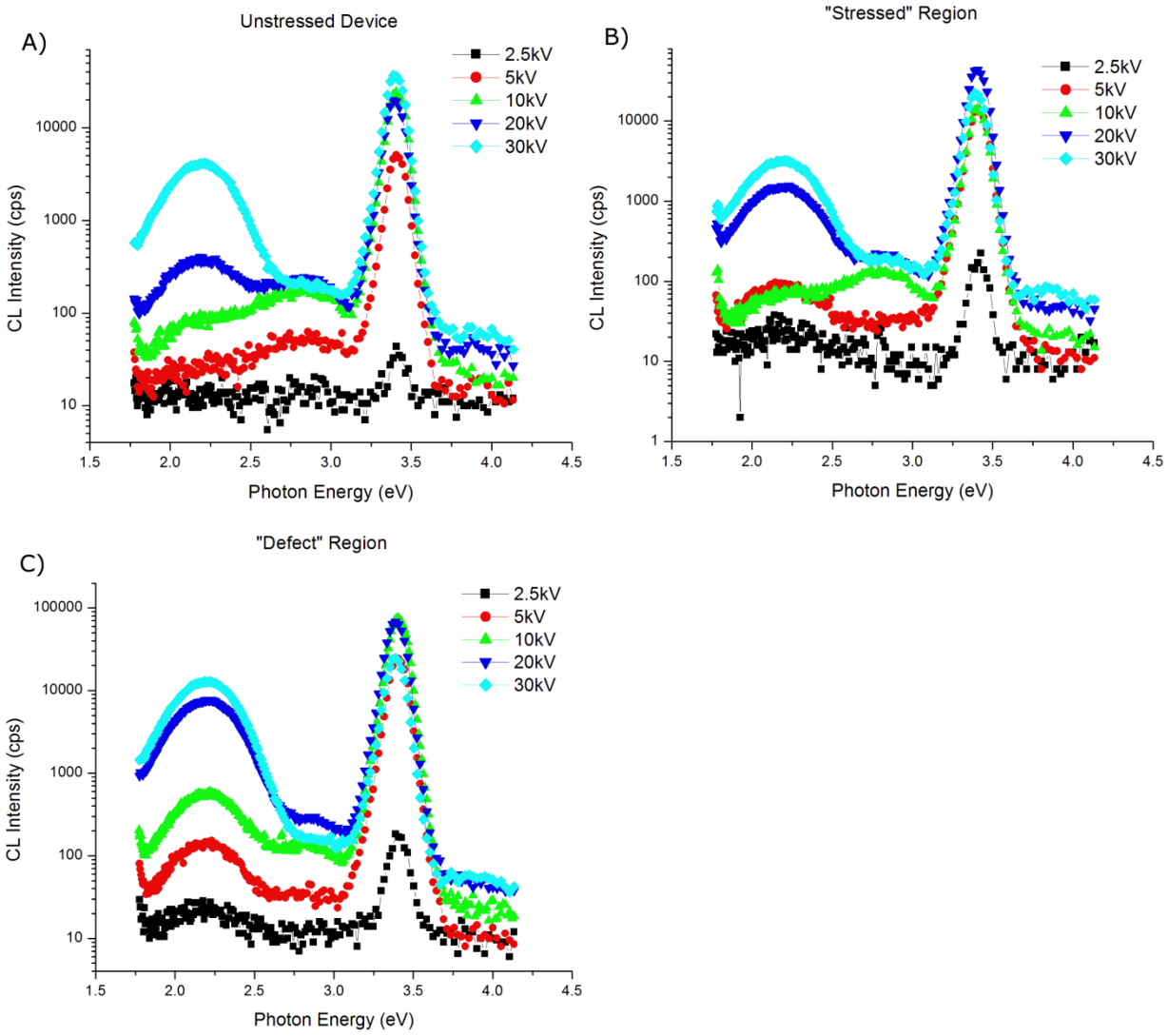


Figure 6-9. Cathodoluminescence spectra taken with electron beam energy ranging from 2.5 kV to 30 kV. Spectra from A) channel before RF stress, B) channel after RF stress at 10 GHz, and C) defective region of channel after 10 GHz RF stress.

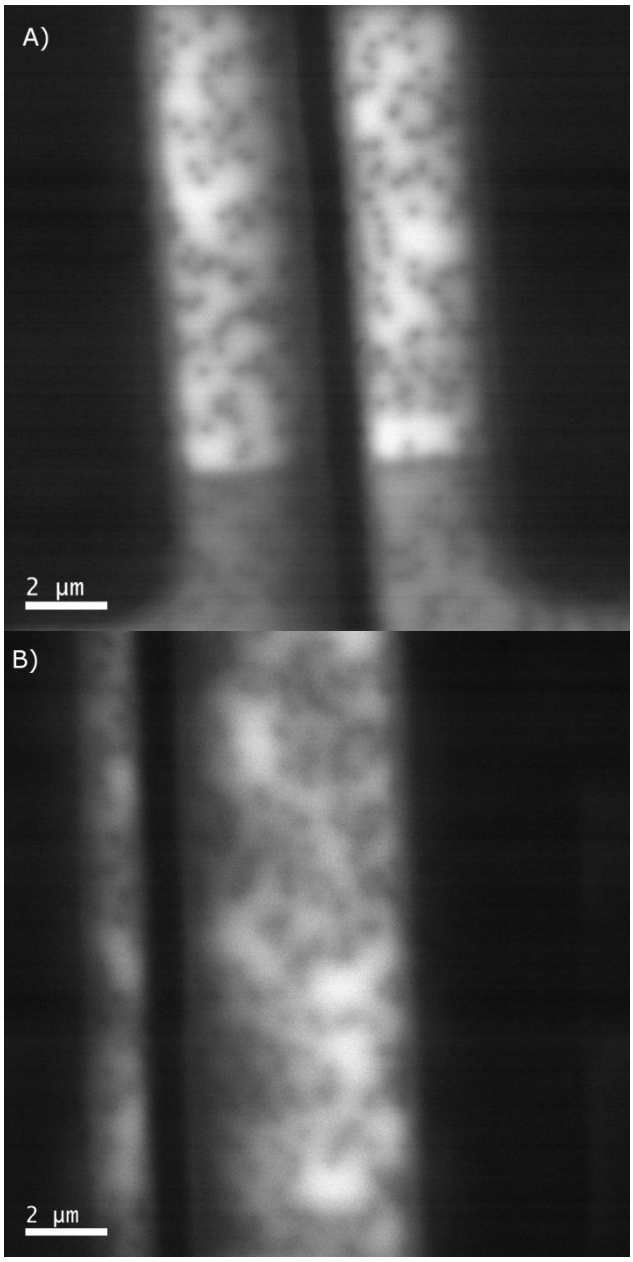


Figure 6-10. Cathodoluminescence image taken in panchromatic mode with electron beam energy at 18 kV. Channel before RF stress (A), channel after RF stress at 10 GHz (B). An increase in defect density is apparent after RF stress.

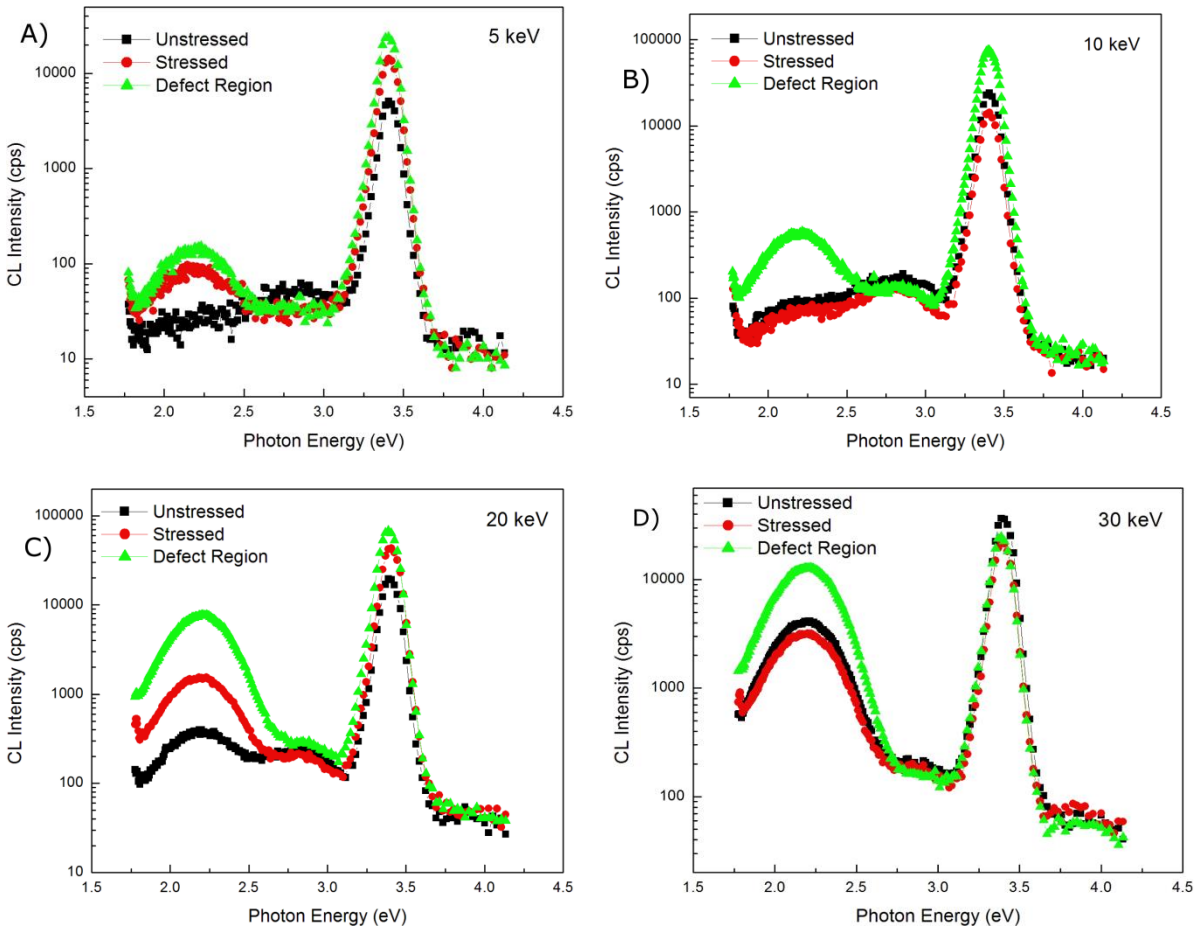


Figure 6-11. CL spectra taken from unstressed channel, RF “stressed” channel, and “defective” region of RF stressed channel of an AlGaN/GaN HEMT. Voltage ranging from (A) 5 keV, (B) 10 keV, (C) 20 keV, and (D) 30 keV.

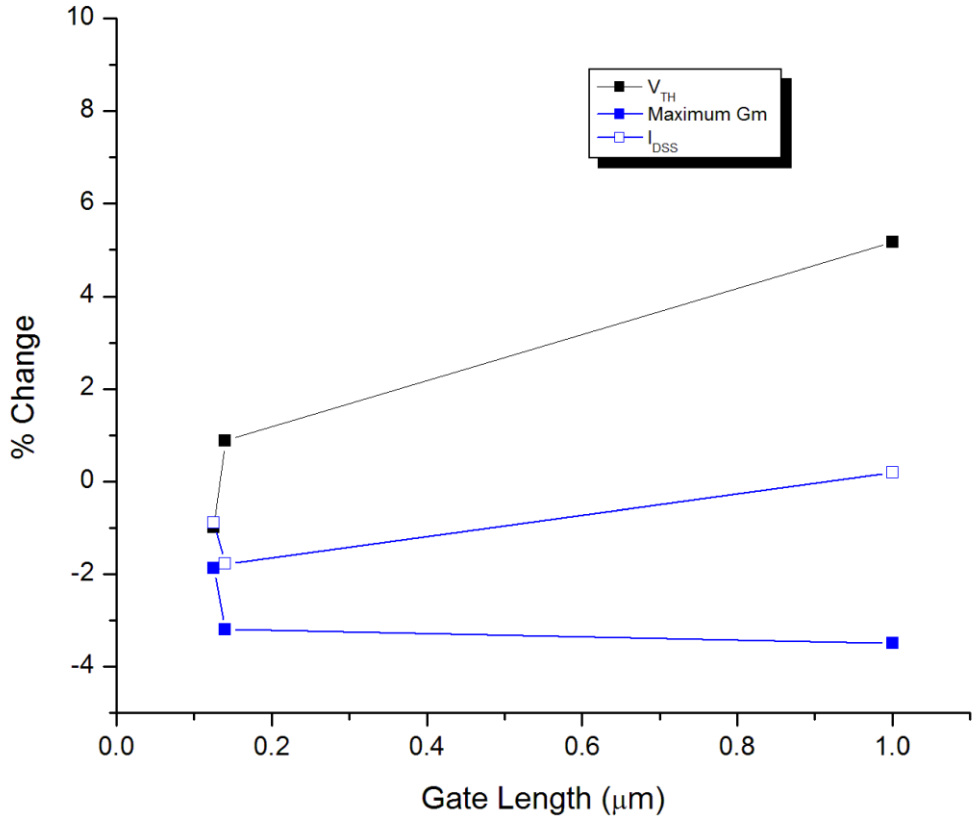


Figure 6-12. Shift in threshold voltage, maximum transconductance, and saturated drain current as a function of gate length. Three gate lengths investigated: 0.125 µm, 0.14 µm and 1µm.

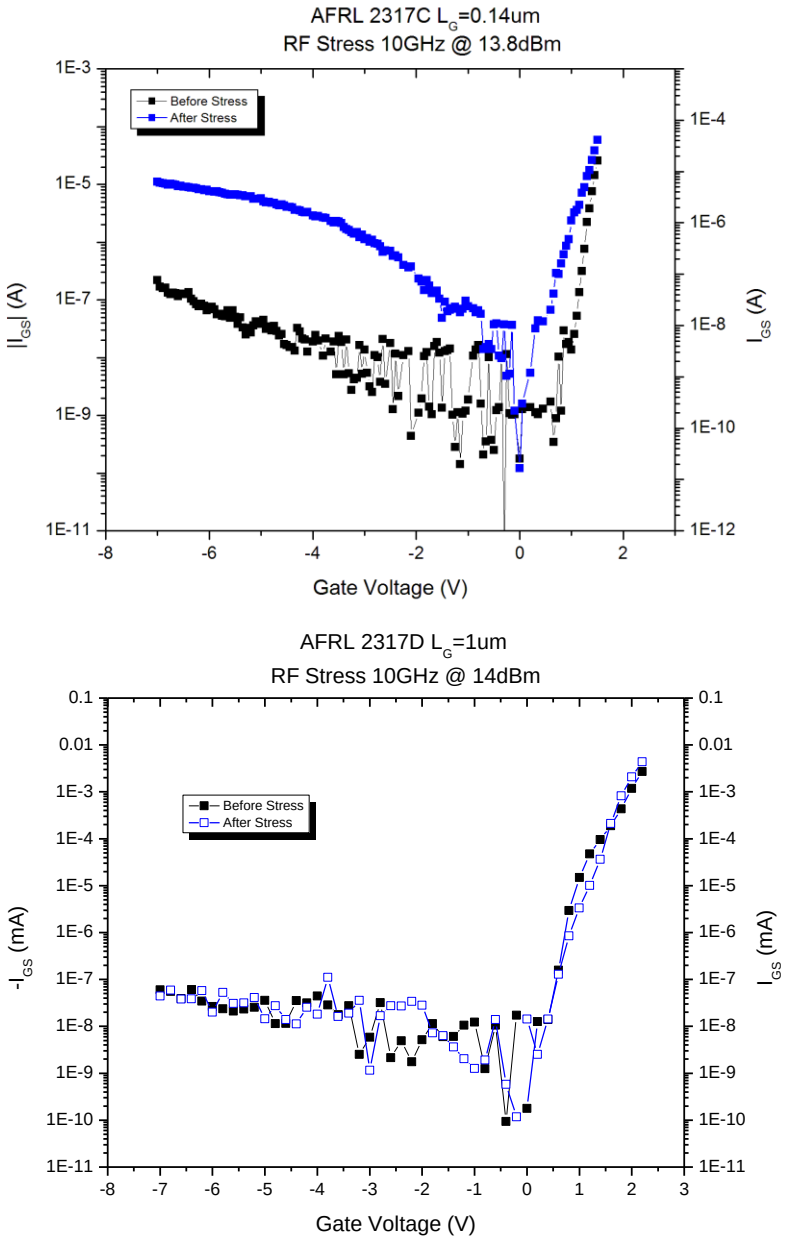


Figure 6-13. Effect of 10 GHz RF stress at V_{DS} = 20 V, I_{DQ} = 200mA/mm on gate leakage current. (TOP) Gate leakage current before and after RF stress on 0.14 µm gate length AlGaN/GaN HEMT. (BOTTOM) Gate leakage current before and after RF stress on 1 µm gate length device.

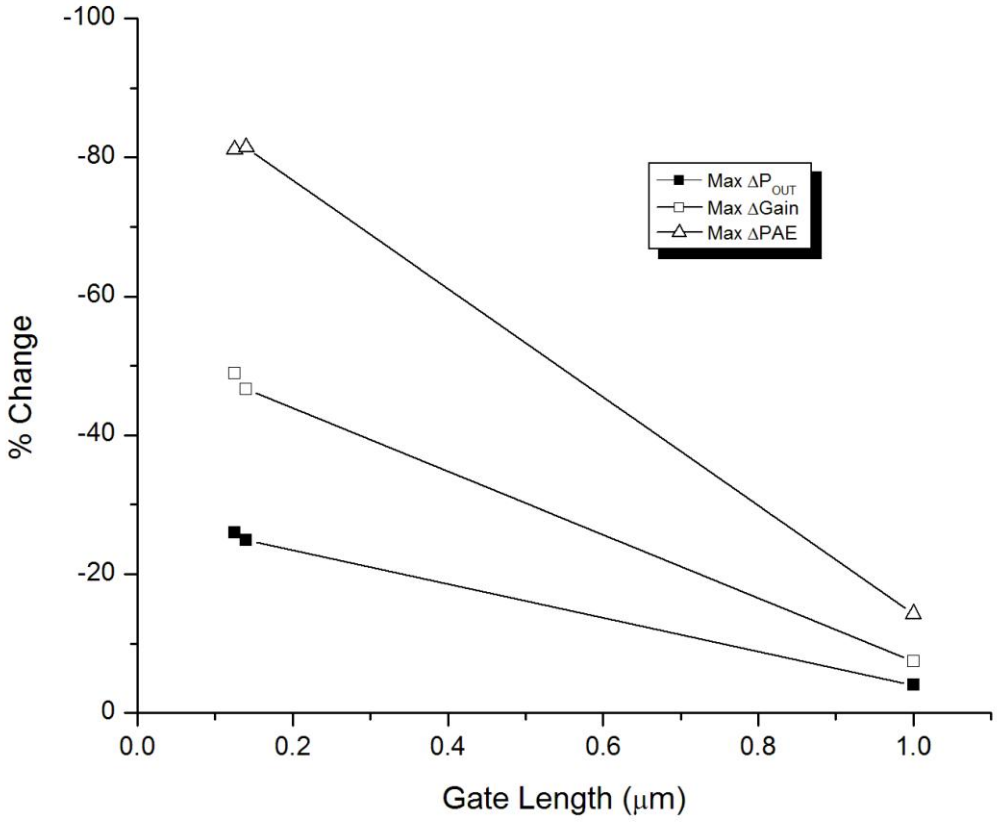


Figure 6-14. Effect of RF device characteristics (ouput power, gain, and power added efficiency) from 10 GHz stress for up to 75 hours. Sub-micron gate lengths exhibit the largest (and similar) degradation .

CHAPTER 7
CONCLUSION

GaN based HEMTs are being inserted into numerous applications ranging from communication base stations to satellites. Though an extremely attractive candidate to replace the present day leading materials for power applications, there is still significant uncertainty with respect to the reliability of GaN HEMTs. The purpose of this research was to understand the driving degradation mechanisms in AlGaN/GaN HEMTs under electrical and thermal stress conditions for both dc and RF operation.

The effect of device design on self-heating was investigated for high power applications. The maximum channel temperature in AlGaN/ GaN HEMTs was shown to increase when the die size is reduced below a critical distance, d, from the gate finger. This distance is significantly dependent on the substrate material, with the largest critical distance of 300μm for the sapphire substrate. Deviation of temperature between individual gate fingers and along the width of the gates was observed, especially as the number of gate fingers increased. A substantial variation in peak temperatures between 2D and 3D simulations was also observed, indicating the need for three dimensional analysis for accurate reliability and MTTF predictions.

The effect of on-state, high power, step stress was investigated on several device structures, including 0.17 μm gate length HEMTs, gateless HEMT structures, and TLM structures with 5 μm spacing. Permanent degradation was observed in the 0.17 μm gate length HEMTs at relatively low drain bias voltages. However, temperature dependent stress tests revealed that permanent degradation was dependent on channel temperatures reaching 195 °C. Conversely, TLM structures, in which there is no Schottky contact, exhibited exceptional stability up to 25 V bias even though current

densities, thus channel temperatures, reached much higher values. Therefore, the Schottky contact is the likely cause for permanent degradation. Breakdown voltages for all three structures indicated that catastrophic failure was not due to channel temperatures, as peak channel temperatures varied significantly (110 °C to 310 °C) at breakdown. There are likely multiple degradation drivers present under these stress conditions, and future tests will be required to isolate the effect of current, voltage and temperature under high power conditions.

High reverse gate bias step-stress from -10 V to -42 V was performed on AlGaN/GaN HEMTs and resulted in a large increase in gate leakage current, with a sharp one order of magnitude increase in current at the critical voltage. The critical voltage of 0.14 µm gate length devices at room temperature was observed to be -30 V. Over 20 devices were step-stressed at temperatures ranging from 25 °C to 150 °C, exhibiting an activation energy of about 42 meV for the critical voltage. As the stress temperature of the devices increased, the critical voltage was found to decrease linearly. This is due to the breakdown of the interfacial oxide layer from electric field induced bond breakage resulting in the consumption of the oxide interface between the Ni/Au Schottky contact and the GaN cap. Disassociation of oxygen from Ga under high electric fields results in diffusion of oxygen to form NiO_x, likely enhanced by thermal and strain effects. Gate leakage current at V_{CRI} was similar (~10^{-7} A) regardless of stress temperature, indicating similar leakage paths for all stress temperatures. Increasing the time interval at each voltage step indicated a linear time dependence with time to breakdown. Future studies will investigate the effect of steady state TDDB voltage on the breakdown AlGaN/GaN HEMTs with unintentional interfacial oxides.

Sub-micron gate length AlGaN/GaN HEMTs were stressed under Class AB RF conditions with drain bias of 10, 20 and 25 V. AlGaN/GaN HEMTs show excellent reliability up to a drain bias of 20 V, however the Schottky contact properties show substantial degradation in terms of threshold voltage shift, gate leakage current, and Schottky barrier height increase. This indicates the gate contact is the cause for device failure under long-term lifetests. Additionally, RF stressing at a drain bias of 25 V is above the threshold necessary for the onset of degradation and resulted in rapid, permanent degradation in P_{OUT} and $I_{DS.}$. Devices with a large gate length, 1 µm, showed the greatest stability with no observed degradation in both dc and RF device characteristics. Sub-micron gate length devices, however, demonstrated degradation that was due to Schottky contact failure, with an observed two order of magnitude increase in gate leakage current and a decrease in PAE, gain, and output power. EL and PL were shown to be a useful tool in order to localize regions of interest that can then be further analyzed with CL both before and after stress. CL indicates that an increase V_{Ga} occurs after RF stress. Additionally, these defects are at shallower levels than before stress and are likely causing traps which leads to enhanced device degradation. The concentration of defects, not observed in devices that exhibited typical failure rates, likely resulted in early failure.

In all, electrical stress under both dc and RF operation indicated that degradation of the Schottky contact was the first occurrence of degradation. In certain instances, such as when operating below V_{CRI} threshold while under RF operation, the devices exhibited excellent stability for almost all RF and dc device characteristics except for those relating to Schottky contact characteristics. Degradation of the Schottky contact

has been shown to be a precursor to device failure. It has also been determined that process induced interfacial oxides between the Schottky contact and GaN cap results in a time dependent dielectric breakdown of the gate contact under high reverse gate bias. Either improvement of processing during device fabrication or the use of a less reactive gate metal, besides Ni, will likely enhance device performance.

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BIOGRAPHICAL SKETCH

Erica Douglas was born in Hollywood, Florida in 1985. She was raised in Lake Placid, Florida and graduated from Lake Placid High School in 2004. Erica earned a Bachelor of Science in Physics in 2008 from the University of Florida. While pursuing her undergraduate degree, she was part of Professor Yasu Takano's research group investigating anti-ferromagnetic triangularly frustrated materials. She also was an Engineering Technician and Engineering Lead at Applied Plasmonics (now Advanced Plasmonics).

In August of 2008 she joined Professor Stephen Pearton's research group while pursuing a Ph.D. from the Materials Science and Engineering Department at the University of Florida. Her work focused on GaN device reliability as well as transparent oxide semiconductor device fabrication. She worked as a Physicist for the U. S. Army Research Laboratory in Adelphi, MD during the summer of 2009 and 2010 in the Flexible Display Group fabricating and optimizing organic light emitting diodes and organic thin film transistors. During the summer of 2011, Erica interned at Sandia National Laboratory in Albuquerque, NM working under the mentorship of Dr. Randy J. Shul.