IMPACT OF UNIAXIAL STRESS ON SILICON DIODES AND METAL-OXIDE - SEMICONDUCTOR-FIELD-EFFECT-TRANSISTORS UNDER RADIATION

By

HYUNWOO PARK

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To my family

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TABLE OF CONTENTS

page

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

COTs	Commercial off-the-shelf
DRAM	Dynamic random access memory
DSETs	Digital single event transients
EDS	Energy-dispersive X-ray spectroscopy
FLOODS	Florida object oriented device simulator
FLOOPS	Florida object oriented process simulator
MOSFET	Metal oxide semiconductor field effect transistor
SEB	Single event burnout
SEEs	Single event effects
SEFI	Single event functional interrupt
SEGR	Single event gate rupture
SELU	Single event latch up
SETs	Single event transients
SEUs	Single event upsets
SRAM	Static random access memory
TEM	Transmission electron microscopy
TID	Total ionizing dose

Abstract of Dissertation Presented to the Graduate School
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By

Hyunwoo Park

December 2011

Chair: Scott E. Thompson
Cochair: Toshikazu Nishida
Major: Electrical and Computer Engineering

Uniaxial strained-silicon (Si) has emerged as a leading technique for enhancing transistor performance for sub-100 nm logic technology for use in commercial and consumer electronics. Traditionally, semiconductor chips for military and space applications are fabricated using expensive radiation hardened technology. There is significant interest in the radiation research community towards integrating commercial CMOS technology for use in radiation environments to reduce costs. Although radiation effects in deep-submicron MOSFETs have been studied extensively in recent years, the effects of mechanical stress on transients in advanced MOSFETs have not been understood fully. Since strained-Si technology is widely adopted to increase carrier mobility in the channel in commercial off-the-shelf (COTs) chips, it is important to understand the trade-offs between chip performance and radiation effects in strained-Si devices. This work investigates the effect of uniaixial stress on Si diodes and MOSFETs under radiation through controlled stress experiments and device simulation.

X-ray-induced charge trapping and mobility degradation are investigated on uniaxially stressed HfO_2-based nMOSFETs. Uniaxial tensile and compressive stress in

nMOSFETs decreases the amount of net positive charge trapping and reduces the threshold voltage shift. Our experimental results suggest that changes in bond lengths and angles in HfO_2 and/or SiO_x as function of mechanical stress can reduce trap activation energy in gate dielectrics. Drive current (electron mobility) degradation in nMOSFETs is characterized and explained after irradiating devices under stress.

Laser-induced current transients in uniaxially stressed silicon (Si) N+/P and P+/N diodes are studied. They are good representation of source and drain regions of MOSFETs. Uniaxial stress alters the shape of the current transient in diodes resulting from strain induced changes in carrier mobility. The Florida Object Oriented Device Simulator (FLOODS) is used to model and explain the mechanism of current transients in unstressed and stressed diodes. The correlation between the external mechanical stress results on large diodes and deep sub-micron MOSFETs (both n-type and p-type) with process induced stress is also investigated and explained.

CHAPTER 1
INTRODUCTION AND BACKGROUND

1.1 Motivation

Continued scaling of silicon (Si) MOSFETs has enabled manufacturing cost reduction and performance improvement in the semiconductor industry for the last thirty years [1, 2]. In 1965 Gordon Moore predicted that “the number of transistors incorporated in a chip will approximately double every 24 months” [3-6]. For a number of years, simple geometrical scaling was sufficient to keep Moore’s law alive. However, as device dimensions reached deep sub-micron levels, the presence of severe short channel effects and high leakage current levels [7-10] meant that the conventional constant-field based scaling alone was not enough to meet the goals set in the International Technology Roadmap for Semiconductors (ITRS) [11].In the last decade, a number of technological innovations at the device, circuit and architecture levels have been necessary to maintain Moore’s law [12, 13]. Amongst these innovations, uniaxial strained Si technology has emerged as one of the most important techniques at the device level to improve performance [2, 14-18]. Intentional uniaxial mechanical stress using SiN capping layer or SiGe epitaxial growth applied to the channel of MOSFETs increases their drive currents [17-19]. Since the uniaxial strained Si engineering is a very cost effective technique, it is widely used in logic transistors today [16-18]. Figure 1-1 shows transmission electron microscopy (TEM) micrographs of Intel’s 90, 65, 45, and 32 nm n- and pMOSFETs that incorporate uniaxial stress [15, 16, 20-24].

Radiation-hardened device technology for space and military electronics market has been strongly influenced by commercial CMOS technology [25, 26]. Since the cost of making radiation hardened devices is becoming very expensive, there is an ongoing

research effort towards the feasibility of using commercial off-the-shelf (COTs) chips to reduce costs. However, to date, there has been no systematic study on the radiation hardness of strain-engineered advanced MOSFETs. In this work, we investigate the reliability of strained devices in radiation environment towards understanding the benefits of using strained devices for space and nuclear applications (Figure 1-2).

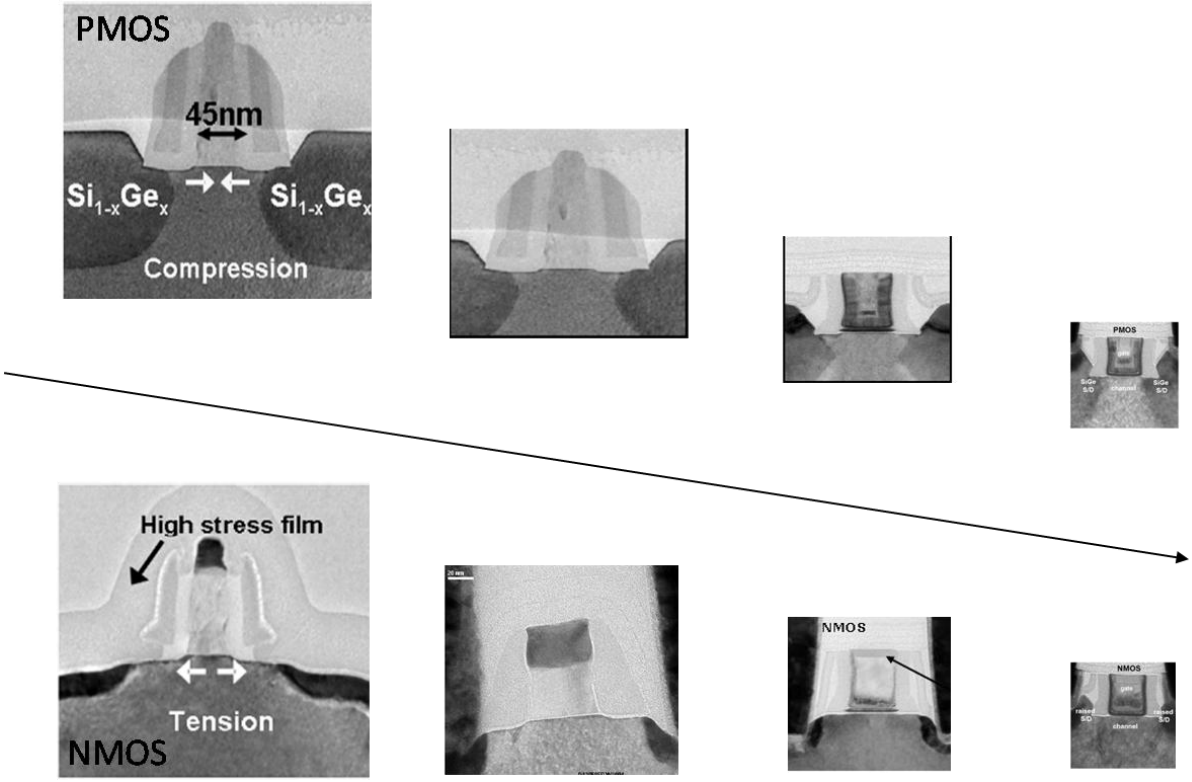


Figure 1-1. Uniaxial stress in Si MOSFETs beyond 90 nm logic technology. Transistors using 90,65,45,and 32 nm technology are shown [Reprinted, with permission, from [S. E. Thompson et al., "A logic nanotechnology featuring strained-silicon", IEEE Electron Dev. Lett., vol. 25, p. 191, Figure 1, Apr. 2004.], [P. Bai, et al., "A 65nm logic technology featuring 35nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and 0.57 μm^2 SRAM cell", in IEDM Tech. Dig., p. 658, Figure 1 and 2, Dec.2004], [K. Mistry, et al., "A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging", in IEDM Tech. Dig., p. 248, Figure 6, Dec. 2007], [C. Auth, et al., "45nm High-k + metal gate strain-enhanced transistors", in VLSI tehnology Tech. Dig., p.129, Figure2, Dec. 2008], [P. Packan, et al.,"High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors", in IEDM Tech. Dig., p. 28.4.2, Figure 5, Dec. 2009]]

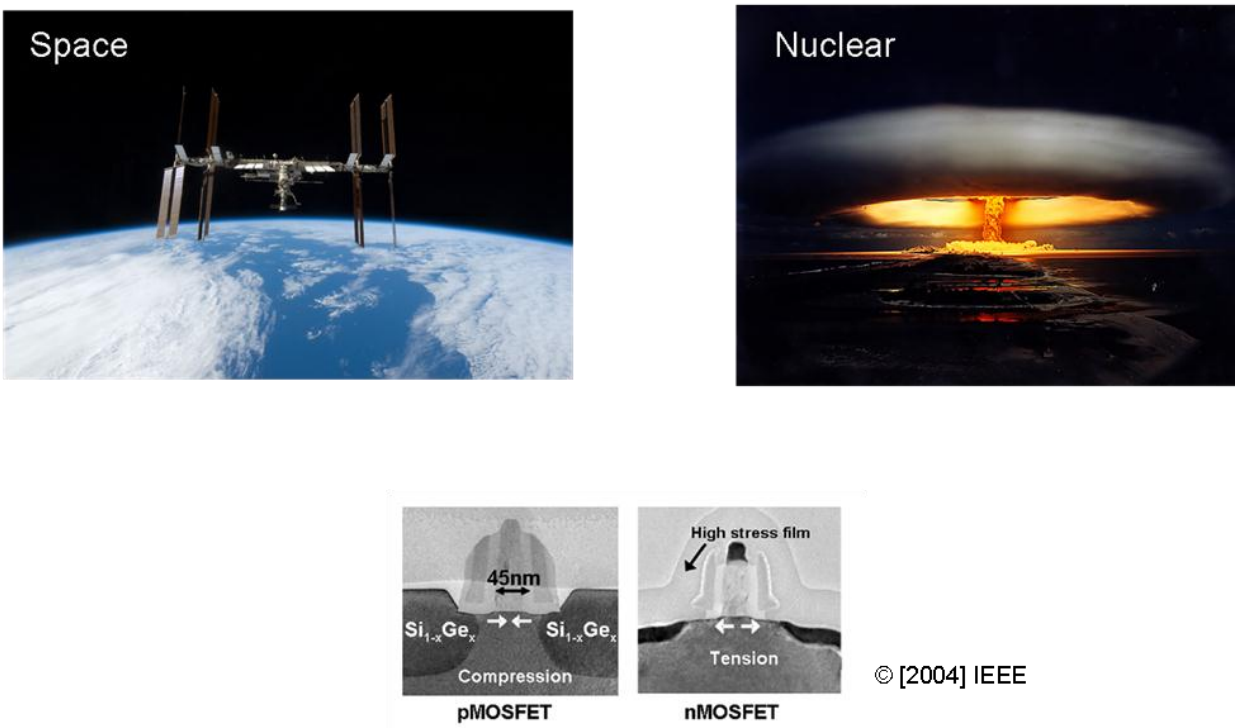


Figure 1-2. Strained Si MOSFETs in the radiation environment. [Reprinted, with permission, from S. E. Thompson et al., “A logic nanotechnology featuring strained-silicon”, IEEE Electron Dev. Lett., vol. 25, p. 191, Figure 1, Apr. 2004.]

1.2 Overview of Strained Silicon Technology

Mechanical stress in the transistor channel enhances the drive current in MOSFETs through an increases in carrier mobility for both electrons and holes. These enhancements are attributed to a decrease in carrier effective mass or scattering due to stress altered Si band structure [2, 16-18, 27-29].

Biaxial stress was the first technique to be investigated for enhancing carrier mobility. High amounts of biaxial stress can be introduced by growing a thin Si layer on relaxed silicon-germanium (SiGe) substrate [30-32]. However, due to the presence of a large number of defects at high stress levels [33] , large threshold voltage shift [34, 35], and very small hole mobility enhancements observed [17], biaxial stress started losing its appeal. In addition, integration difficulties associated with introducing tensile and

compressive stress for n- and pMOSFETs simultaneously makes biaxial stress less attractive for very large scale integration [12].

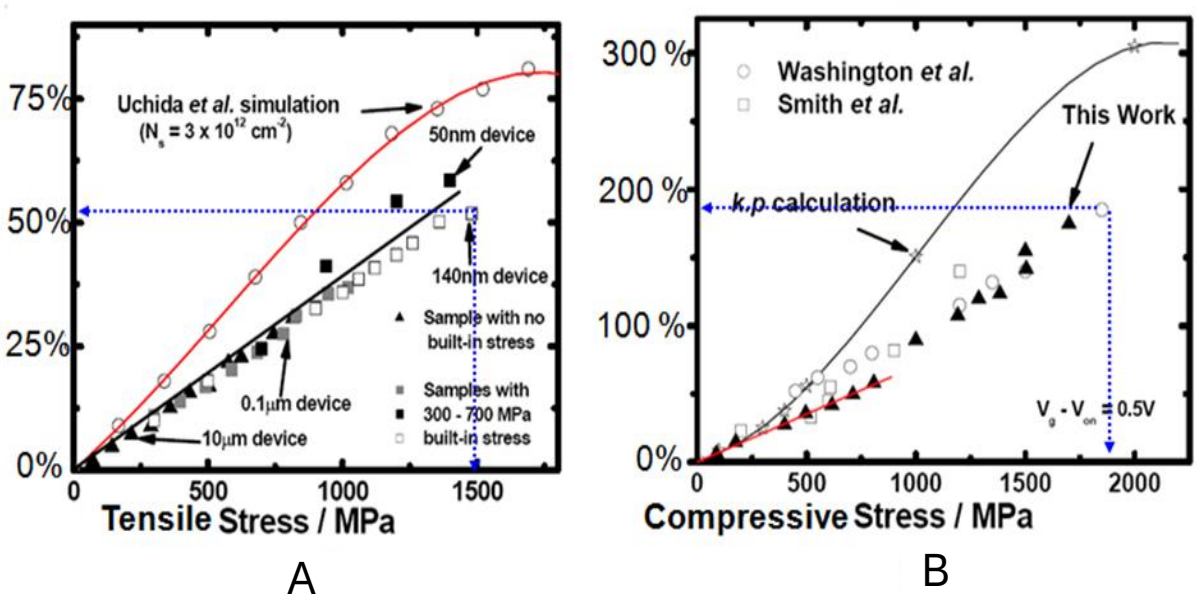


Figure 1-3. Uniaxial stress effect on electron and hole mobility. A) Electron and B) hole mobility enhancement in uniaxial stress.[Reprinted, with permission, from S. Suthram, et al., "Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (similar to 1.5 GPa) channel stress," IEEE Elec. Dev. Lett., vol. 28, p. 60, Figure 3, Jan. 2007](b) [Reprinted, with permission, from S. Suthram, "Study of the Piezoresistive Properties of Si, Ge, and GaAs MOSFETs Using a Novel Flexure Based Wafer Bending Setup, PhD Gainesville: University of Florida, p. 49, Figure 3-6, 2008]

Compared to biaxial stress, uniaxial compressive stress produces a large hole mobility enhancement [17, 19] and introduces minimal threshold voltage shifts [34, 35]. It also decreases gate tunneling current [36, 37]. Electron mobility enhancement in nMOSFETs up to ~ 50% (for 1.5 GPa uniaxial stress) and hole mobility enhancement in pMOSFETs up to ~200% (for ~2GPa uniaxial stress) have been reported, as shown in Figure 1-3 [38]. Uniaxial tensile stress on n-MOSFETs and uniaxial compressive stress on p-MOSFETs can be concurrently applied on the same wafer without incurring much additional process complexity [17, 39-42]. This was the primary reason as to why

uniaxial stress engineering was adopted by the industry as a performance booster starting from the 90-nm node.

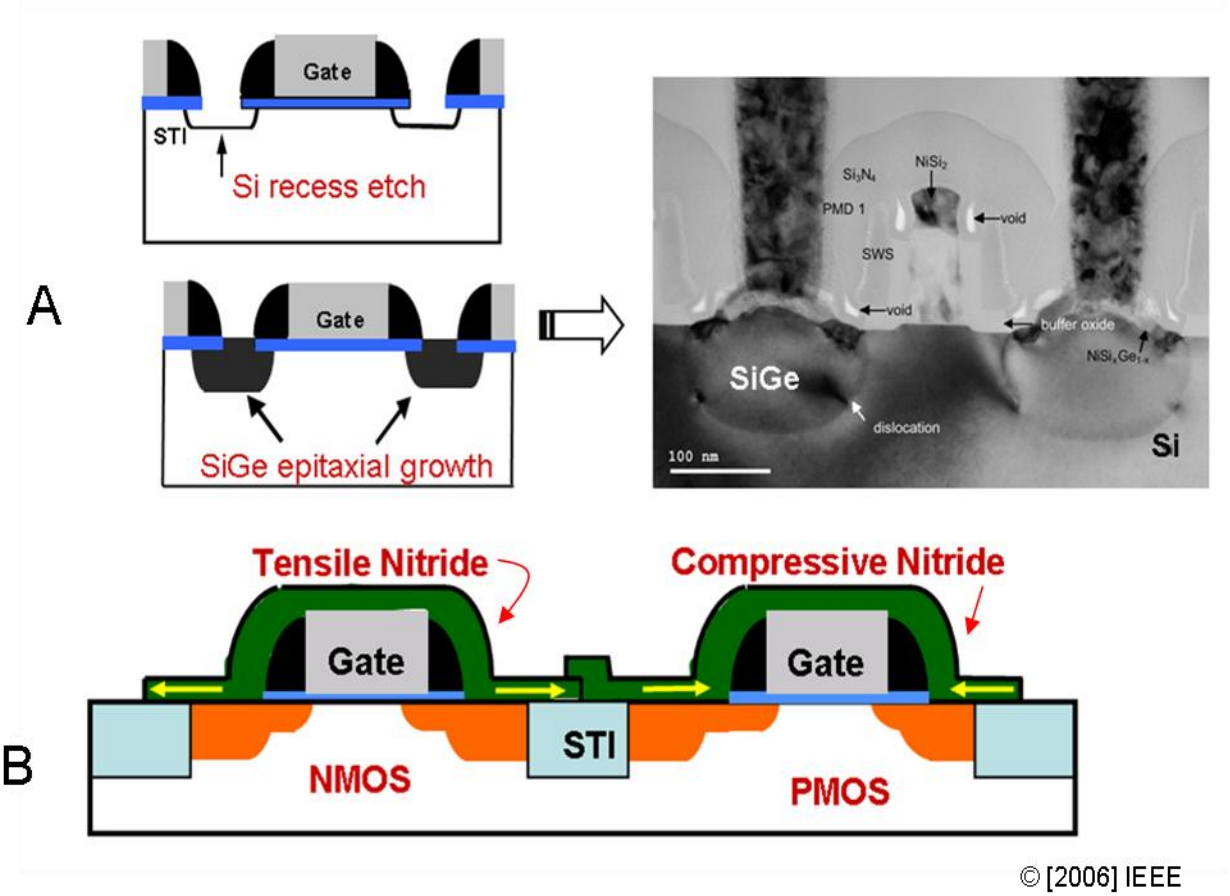


Figure 1-4. Process-induced uniaxial stress. A) SiGe epitaxial growth in pMOSFETs B) SiN capping layer in n- and pMOSFETs [Reprinted, with permission, from S. E. Thompson, et al., "Uniaxial-process-induced strained-Si: Extending the CMOS roadmap," IEEE Trans. Electron Dev., vol. 53, p. 1018, Figure 13, May 2006.]

There are two ways to apply uniaxial stress to devices. The first technique is SiGe epitaxial growth in source/drain regions to create compressive stress in pMOSFETs [15, 16, 39], as shown in Figure 1-4 (a). It was successfully implemented in 90 nm technology node by Intel in 2002 at first [15]. Dual stress liner technique using compressive and tensile Silicon Nitride (SiN) can be implemented in n- and pMOSFETs, respectively [39], as shown in Figure 1-4 (b).

1.3 Overview of Radiation Effects

Radiation effects in MOS devices are generally categorized into total ionizing dose (TID) effects and single event effects (SEEs) [43-47]. TID effects in MOSFETs are due to radiation induced trapped charges in gate oxide and shallow trench isolation (STI). Trapped charges shift threshold voltage, decrease carrier mobility, and degrade the dielectric [26, 43, 45, 48-50]. Figure 1-5 shows how radiation introduces charges in the devices which are trapped in the gate oxide. 1-1000 keV energy range electrons or protons create electron-hole pairs in gate oxide [45, 51]. In the presence of applied bias, electrons are swept out of gate oxide. However, relatively immobile holes are trapped inside the gate oxide and it results in a negative threshold voltage shift. The radiation also generates traps near the Si/SiO_2 interface. In thick STI (~400 nm), a large number of electrons and holes can build up and increase the off-state leakage [43, 52].

To maintain the same applied electric field, the thickness of gate oxide is reduced in scaled devices as the supply voltage is lowered. Due to the reduction in the insulator volume where charge trapping could occur, scaled MOSFETs have a smaller threshold voltage shift [48, 49]. However, the high gate leakage current in a very thin SiO_2 increases the off state power and impacts the reliability issues of devices. High-k dielectrics have emerged as a solution [21, 23, 53] to combat the leakage and reliability issues within the last 5 years. While the performance and reliability of high-k dielectrics have been investigated extensively for over a decade [47, 54-60] for commercial MOSFET applications, the effect of radiation damages in high-k dielectrics has been done only recently [47, 61-64]. The effects of uniaxial stress on radiation induced charge trapping and mobility degradation in high-k based MOSFETs have not been understood fully to this date.

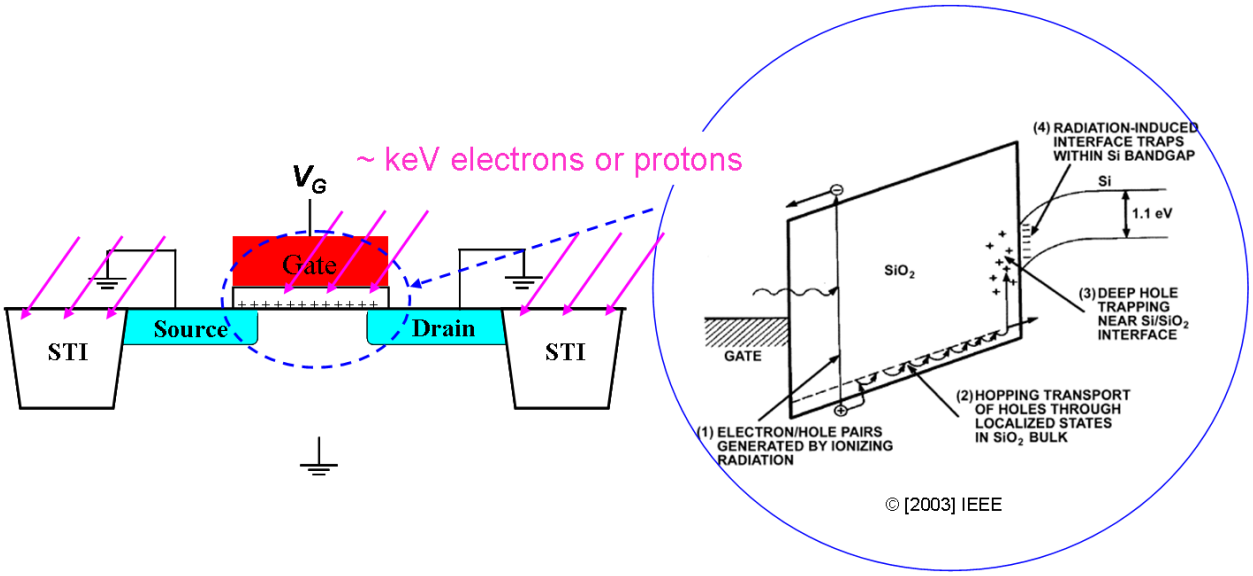


Figure 1-5. Total inonizing dose effects in MOSFETs. [Reprinted, with permission, from [T. R. Oldham et al., Total ionizing dose effects in MOS oxides and devices, IEEE Trans. Nucl. Sci., vol. 50, p 484, Figure 2, Jun. 2003.]

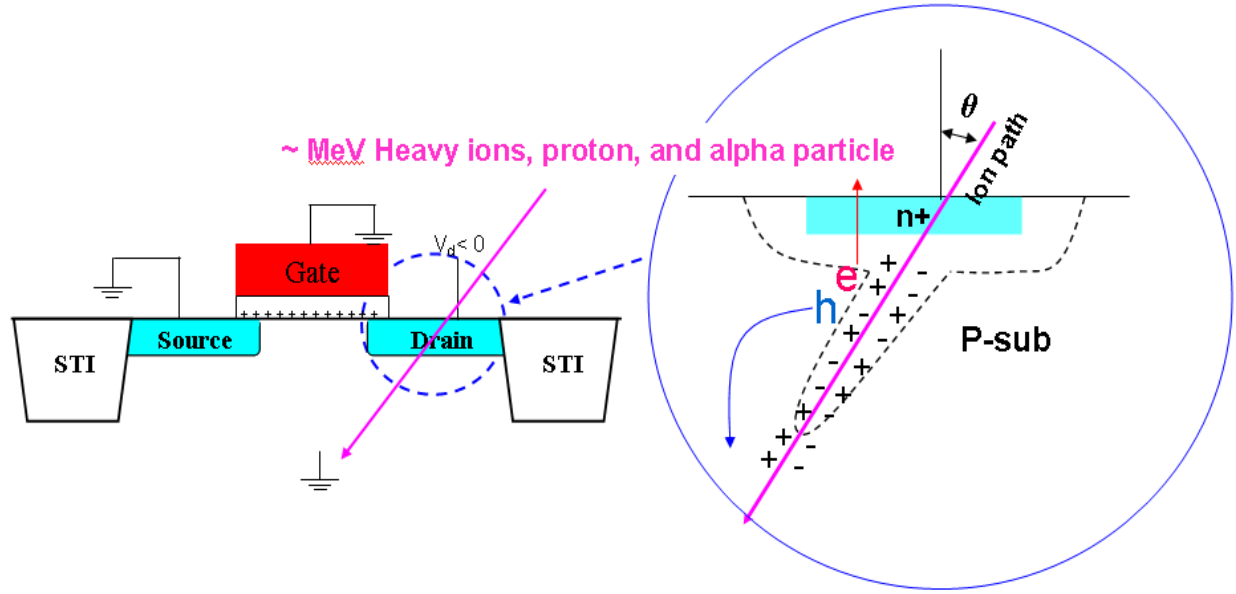


Figure 1-6. Single Event Effects in MOSFETs.

SEEs in MOSFETs are voltage or current transients in sensitive nodes (such as the MOSFETs' source and drain regions) caused by 1-1000 MeV high energy particles such as protons, neutrons, heavy ions, and alpha particles, as shown in Figure 1-6 [25, 44]. SEEs are divided into soft (nondestructive) and hard (destructive) errors. The

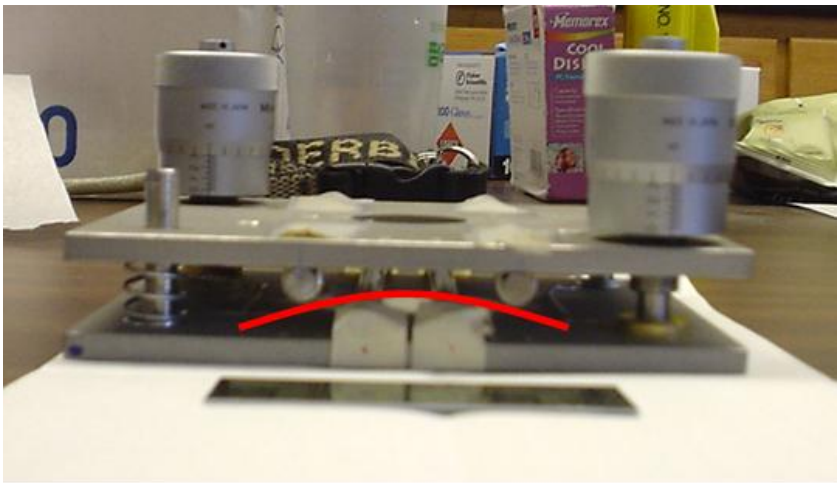
common physics in both types of SEEs is the presence of a transient pulse caused by drift and diffusion of a large number of electrons or holes due to the high energy particles [25, 44, 46]. For examples, the transients can cause single event upsets (SEU) [25, 65], which manifests as inversion of the bits stored in memory devices such as dynamic random access memory (DRAM) and static random access memory (SRAM). Digital single event transients (DSETs) are those transients propagating through combinational logic circuits and are stored into memory components [44, 66]. Other soft errors are single event functional interrupt (SEFI) and single event latch up (SELU) [44, 46]. While soft errors cause temporarily data loss, hard errors like single event gate rupture (SEGR) and single event burnout (SEB) [44, 46] lead to permanent data breakdown.

1.4 Mechanical Stress Bending Setup

Controlled external mechanical stress is applied via a four-point bending setup [67, 68], as shown in Figure 1-7. The amount of applied uniaxial stress can be obtained using [69]

$$\sigma = E \cdot \varepsilon = E \cdot \frac{t \cdot d}{2a\left(\frac{L}{2} - \frac{2a}{3}\right)} \tag{1-1}$$

where σ is the applied stress, *E* is the Young's modulus of Si along the stress direction, ***ε*** is strain, *t* is the thickness of the wafer, *d* is vertical displacement between the upper and lower plates of a four point bending setup, *a* is the distance between the inner and outer rods, and *L* is the distance between the two outer rods, as shown in Figure 1-8. Previous work by Chu et al. [70] shows the calculated stress is in good agreement with a measurement using a strain gage with less than 5% error.



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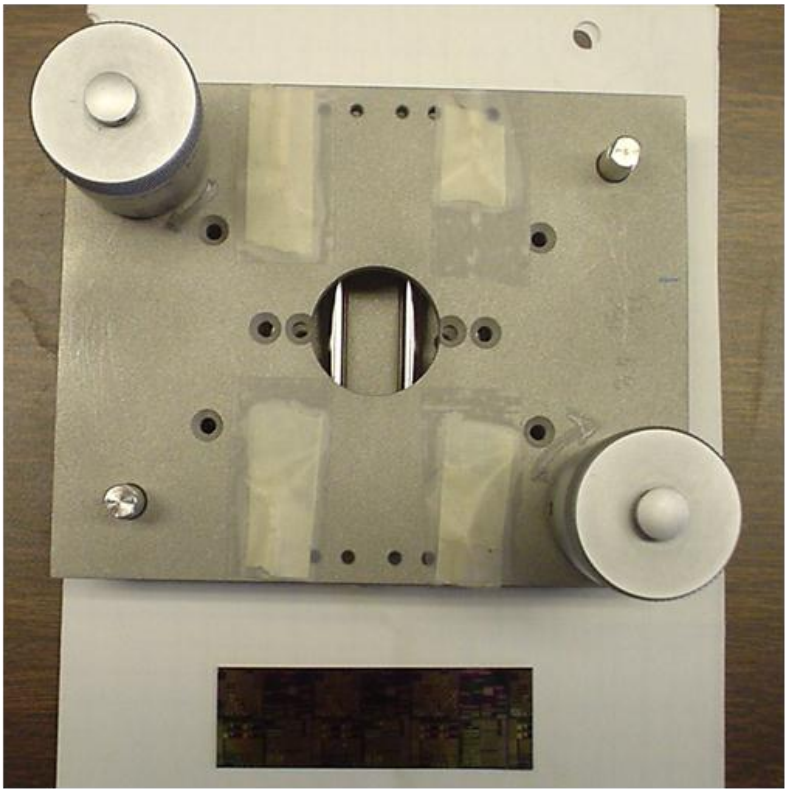

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Figure 1-7. Four point mechanical bending setup A) cross section B) top view.

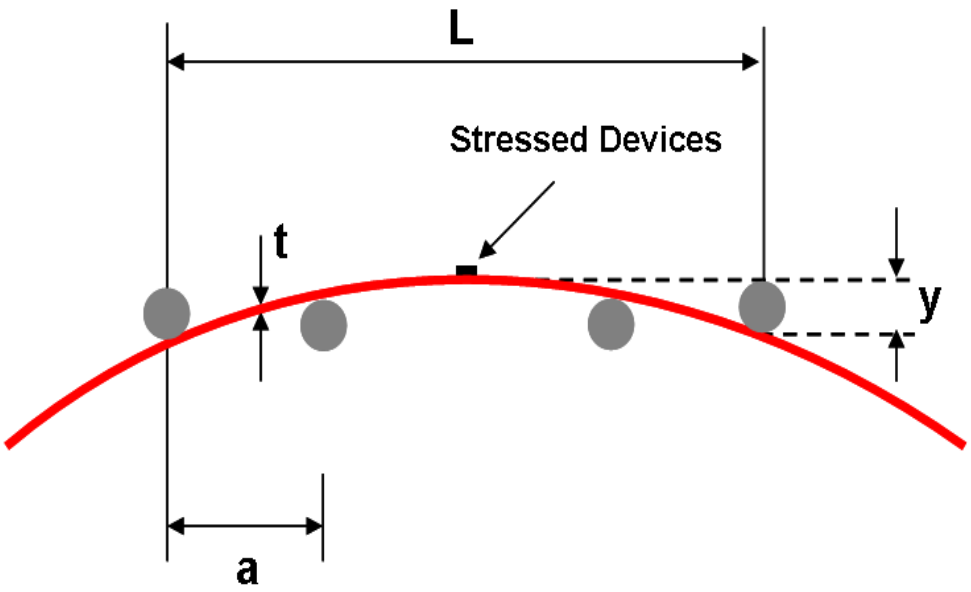


Figure 1-8. Schematic of uniaxially stressed wafer via mechanical bending set up. Uniaxial tensile stress is applied to a wafer.

1.5 Objectives and Organization

The main goal of this study is to understand how mechanical stress affects the reliability of semiconductor devices in the radiation environment in view of total ionizing effects (radiation induced trapped charges, mobility degradation) and single event effect (voltage or current transients).

In Chapter 2, radiation induced threshold voltage shift and electron mobility degradation in strained metal gate high-k nMOSFETs are measured quantitatively and a qualitative physics based model based is presented.

Chapter 3 investigates experimentally and theoretically how uniaxial stress changes the laser induced current transients in uniaxially stressed N+/P Si diodes. The effects of mobility enhancement/degradation under mechanical stress on peak current of current transients and collected charges in the diodes are presented in detail.

Based on the method developed in Chapter 3 for analyzing transients, laser induced current transients in P+/N diodes as a function of uniaxial stress are studied in

Chapter 4 experimentally and theoretically. The difference between laser induced current transients in uniaxially stressed P+/N diode and alpha particle induced current transients in STI induced stressed pMOSFETs are discussed.

Chapter 5 summarizes this study and suggests the future work.

CHAPTER 2
TOTAL IONIZING DOSE EFFECTS ON STRAINED HFO_2-BASED NMOSFETS

2.1 Introduction

Uniaxial strained-silicon (Si) [14, 15] and high-k gate dielectric [71] are key technologies used to enhance transistor performance for sub 100-nm logic technology nodes. Uniaxial strain improves device characteristics such as mobility [17, 19], gate tunneling current [36, 37, 72, 73], with minimal threshold voltage shifts [34, 35]. High-k gate dielectrics are being implemented to reduce transistor gate leakage current in the 45 nm CMOS technology node [23]. Hafnium-based dielectrics, in the form of silicates and nitrided silicates, with a relative dielectric constant of ~15 to 26, have emerged as the materials of choice for high-k gate dielectrics.

Although radiation damage of HfO_2-based MOS devices has been studied in recent years [61, 63], the effects of uniaxial mechanical stress on the ionizing radiation response of HfO_2-based MOS devices have not been reported. Hole trapping is observed to be dominant in HfO_2 [61, 63] dielectric layers, similar to SiO_2 [26]. The effects of mechanical stress on the ionizing radiation response of SiO_2-based MOS devices have been reported [74, 75], but the mechanical stress (≤ 4 MPa) produced in these studies by changing the gate electrode thickness is much smaller than that used in strained-Si technology (~ 2 GPa) [76, 77].

In high-k transistors, remote Coulomb scattering (RCS) is one of the main factors limiting the mobility [71, 78]. In commercial devices, most of the RCS effect comes from fixed charges generated by the fabrication process [78]. The effects of radiation induced

charges on RCS would likely be similar to what is seen in commercial devices. Owing to the ubiquitous use of high-k based strained-Si technology in the future, it is important to address the radiation response of these devices as a function of stress. In this work, we investigate the effects of uniaxial stress on the radiation-induced threshold voltage shifts and mobility degradation in HfO_2-based nMOSFETs using controlled external mechanical stress.

2.2 Experimental Setup

Radiation-induced threshold voltage shifts and mobility degradation in mechanically stressed HfO_2-based nMOSFET are extracted from drain current-gate voltage (I_D-V_{GS}) characteristics. The samples used in this study are TiN/HfO_2 gate stack nMOSFETs on Si (001) wafers and <110> channel direction. The high-k gate dielectric is 7.5 nm in physical thickness. The thickness of the SiO_x interlayer is 1 nm. The effective oxide thickness (EOT) of these transistors is 2.3 nm. The size (W/L) of the transistors used in this investigation is 10 µm/3 µm. Strain in the devices is produced by applying uniaxial mechanical stress using a four point bending setup [35], as shown in Figure 2-1. The devices are irradiated in an ARACOR 10-keV X-ray irradiation system under different values of stress (100 MPa and 200 MPa tensile, no stress, and 200 MPa compressive), at –2 V gate bias, with the source, drain, and body grounded [61]. Samples are irradiated to a cumulative dose of 5 Mrad(SiO_2) at a dose rate of 31.5 krad(SiO_2)/min; the experimental matrix is shown in Table 2-1. Post irradiation I_D-V_{GS} curves are measured using an Agilent 4156 semiconductor parameter analyzer.

Threshold voltage shifts (ΔV_T) are monitored as a function of radiation dose for different applied uniaxial mechanical stresses. Threshold voltages are extracted using a

constant-current (CC) method [79]. Pre- and post-irradiation subthreshold behavior is also studied. –2 V gate bias stress experiments without irradiation are performed

Table 2-1. TID experimental matrix

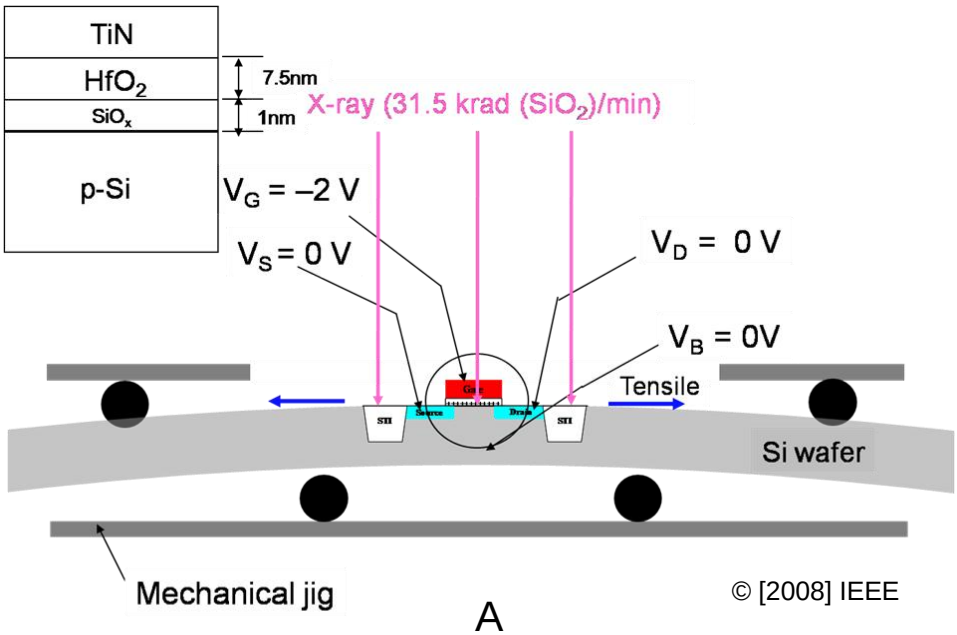
	Compressive 200 MPa	No Stress 0MPa	Tensile 100MPa	Tensile 200MPa
Pre-rad (0Mrad)	✓	✓	✓	✓
0.5 Mrad	✓	✓	✓	✓
1 Mrad	✓	✓	✓	✓
5 Mrad	✓	✓	✓	✓

to separate the contributions of bias-induced charge trapping/creation [80] in these gate dielectrics from the radiation-induced shifts. The extracted electron mobility from current voltage equation at low drain voltage (V_{DS} = *0.1 V*) is expressed as [1]

$$\mu_e = \frac{I_D L_g}{W C_{ox}(V_{GS} - V_T)V_{DS}} \tag{2-1}$$

where is I_D is the current of nMOSFETs, V_{GS} is the applied voltage between gate and source, L_g is the channel length, W is the channel width, C_{ox} is the gate oxide capacitance per unit area, and V_T is the threshold voltage.

Threshold voltage instability is one of the main issues in high-k devices [81-83]. In this work, threshold voltage shifts are measured after being stabilized by sweeping the I_D-V_{GS} curves before and after irradiation. For the samples used in this investigation, the threshold voltage shift stabilizes generally after the second I_D-V_{GS} curve after irradiation or bias stress. The stabilization occurs because charges in shallow hole trap sites of SiO_x or HfO_2 may detrap, or holes in deeper trap sites near the interface may recombine with injected electrons during the first I_D-V_{GS} sweep under a given irradiation or bias condition. Previous work by Dixit et al. [61] focused on the threshold voltage shift of the



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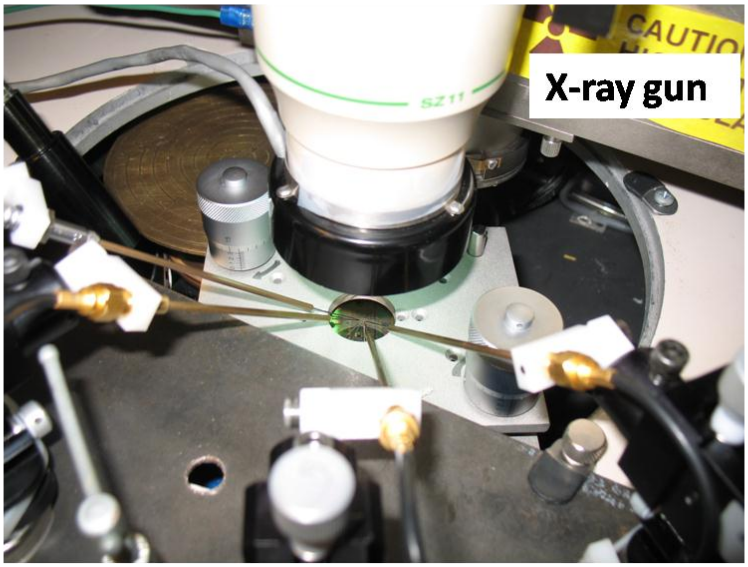

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Figure 2-1. Experiment set up for TID measurements. A) schematic (not to scale) B) picture for measuring total ionizing dose (TID) effects under mechanically strained nMOSFET and cross section of gate stack of high-k nMOSFET. (a) [Reprinted, with permission, from H. Park, et al., Total Ionizing Dose Effects on Strained HfO2-Based nMOSFETs, IEEE Trans. Nucl. Sci., vol. 55, pp. 2982, Figure 1, Dec. 2008]

first I-V curve, which includes the effects of these transient shifts. This work focuses instead on the changes in radiation-induced charge trapping under uniaxial mechanical stress after the threshold voltage stabilizes.

2.3 Results and Discussion

Hole trapping in the gate oxide is the dominant radiation-induced charge for these devices under the irradiation conditions, as seen by the decrease in the threshold voltage as shown in Figure 2-2. This agrees with previous results on HfO_2-based nMOSFETs in [61]. Threshold voltage shifts (ΔV_T) can be caused by interface trapped charge (ΔQ_{it}) and oxide trapped charges (ΔQ_{ot}) [84]. Since there is no significant change observed in the subthreshold slope in Figure 2-2, the threshold voltage shifts are caused mainly by an increase in ΔQ_{ot} [61]. Transistors irradiated under mechanical stress conditions (compressive (200 MPa), no stress, and tensile (200 MPa)) are also dominated by positive charge trapping.

2.3.1 Radiation Induced Threshold Voltage Shifts under Uniaxial Stress

The effect of applied mechanical stress on charge trapping is characterized by monitoring threshold voltage shifts at each given radiation dose. The tensile stress effect is shown in Figure 2-3. Increasing tensile stress results in less threshold voltage shift at each dose level than that measured for devices irradiated with no stress applied. Smaller threshold-voltage shifts are observed after applying only bias for a total time of 2.5 h, which is equivalent to the time required for 5 Mrad(SiO_2) irradiation. Tensile stress also reduces the threshold voltage shift resulting only from the bias. The data points are the average threshold voltage shifts at each radiation dose or bias time. The error bars in the data points represent the standard deviation in the data at each dose and stress

level. Figure 2-4 shows a similar trend for the threshold voltage shifts under 200 MPa ofcompressive stress.

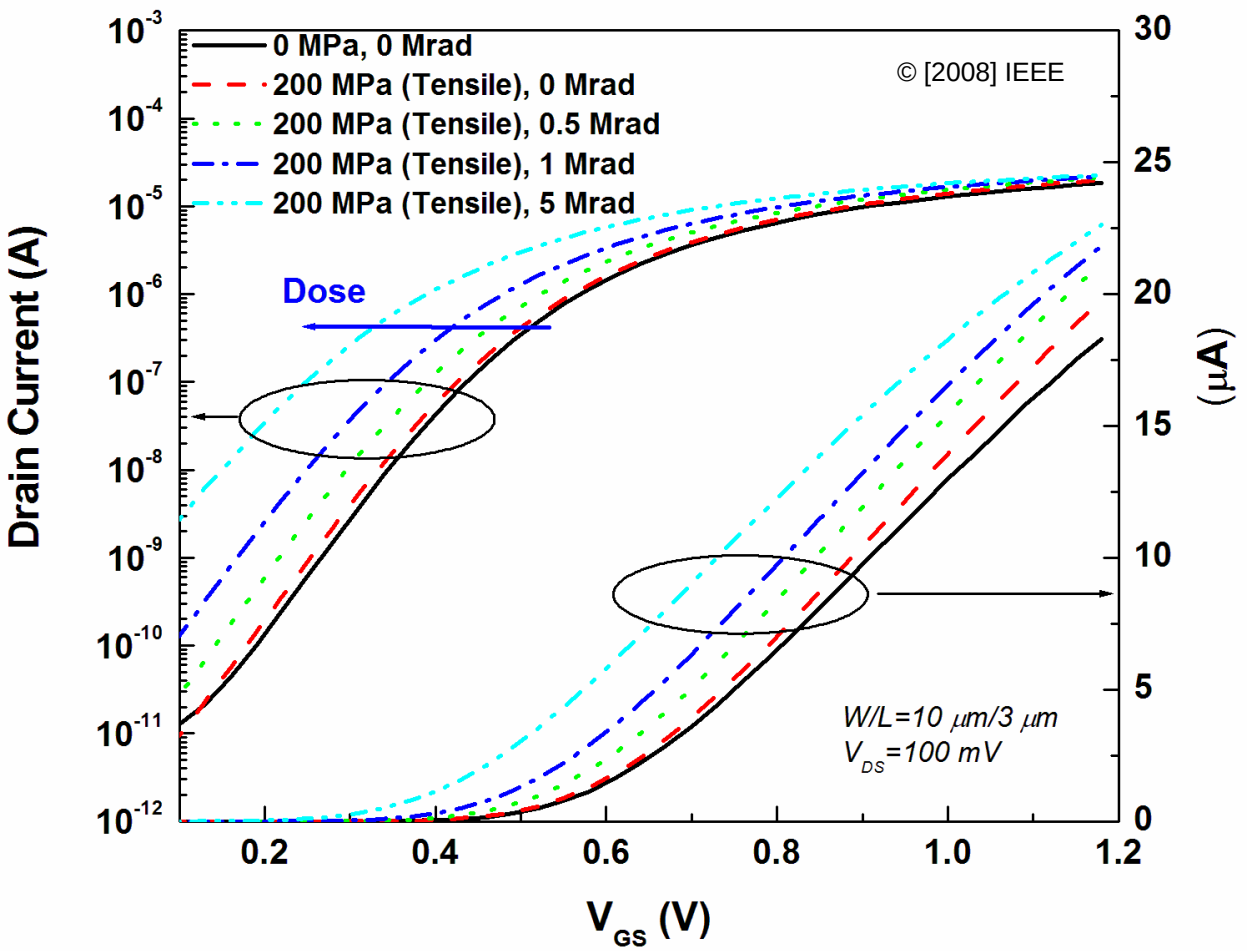


Figure 2-2. Semilog and linear plot of the I_D-V_{GS} characteristics as a function of the accumulated x-ray dose under tensile stress of 200 MPa. [Reprinted, with permission, from H. Park, et al., Total Ionizing Dose Effects on Strained HfO2-Based nMOSFETs, IEEE Trans. Nucl. Sci., vol. 55, pp. 2983, Figure 2, Dec. 2008]

In contrast to the reported stress dependence of the SiO_2 nMOSFET threshold voltage shift under irradiation [74], both applied tensile and compressive uniaxial stress reduce the threshold voltage shifts in devices with HfO2 and SiOx dielectrics in Figure 2-5 that were either irradiated under bias, or subjected only to bias stress without irradiation, for comparison.

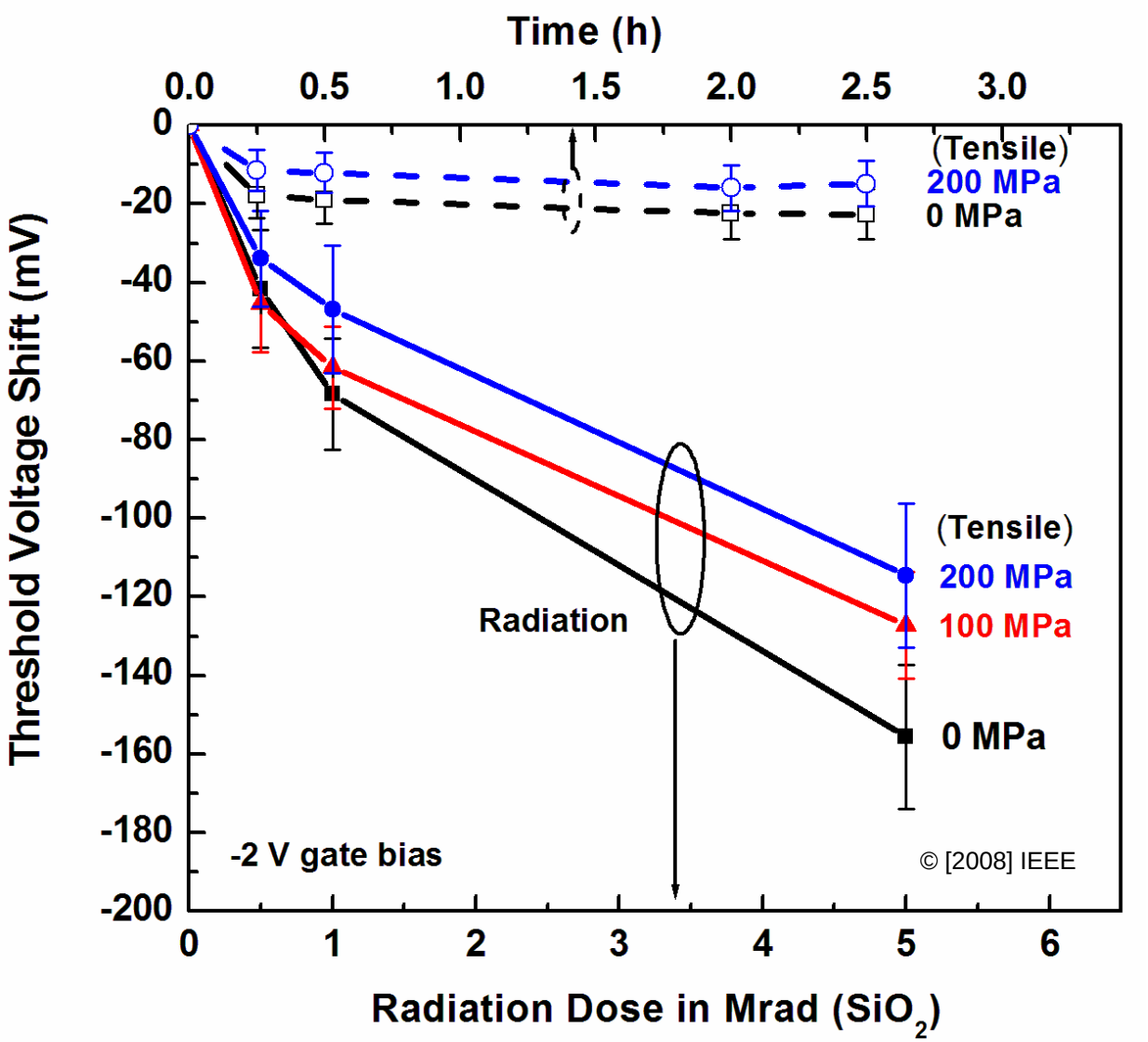


Figure 2-3. Threshold voltage shifts (ΔV_T) observed with and without tensile stress and radiation at -2V gate bias. [Reprinted, with permission, from H. Park, et al., Total Ionizing Dose Effects on Strained HfO2-Based nMOSFETs, IEEE Trans. Nucl. Sci., vol. 55, pp. 2983, Figure 3, Dec. 2008]

A possible explanation of these results is that compressive and tensile uniaxial mechanical stress both lower the hole trap energy level in HfO_2 and/or SiO_x, reducing hole trapped charges. In recent work, trap-assisted gate tunneling current in high-k MOS capacitors increased under both compressive and tensile stress as shown in Figue 2-6 [85], suggesting that the hole trap energy distribution may be shifted to lower

average values by uniaxial mechanical stress. Uniaxial mechanical stress may change the trap energy levels by changing bond lengths and angles in HfO_2 and SiO_x [86, 87].

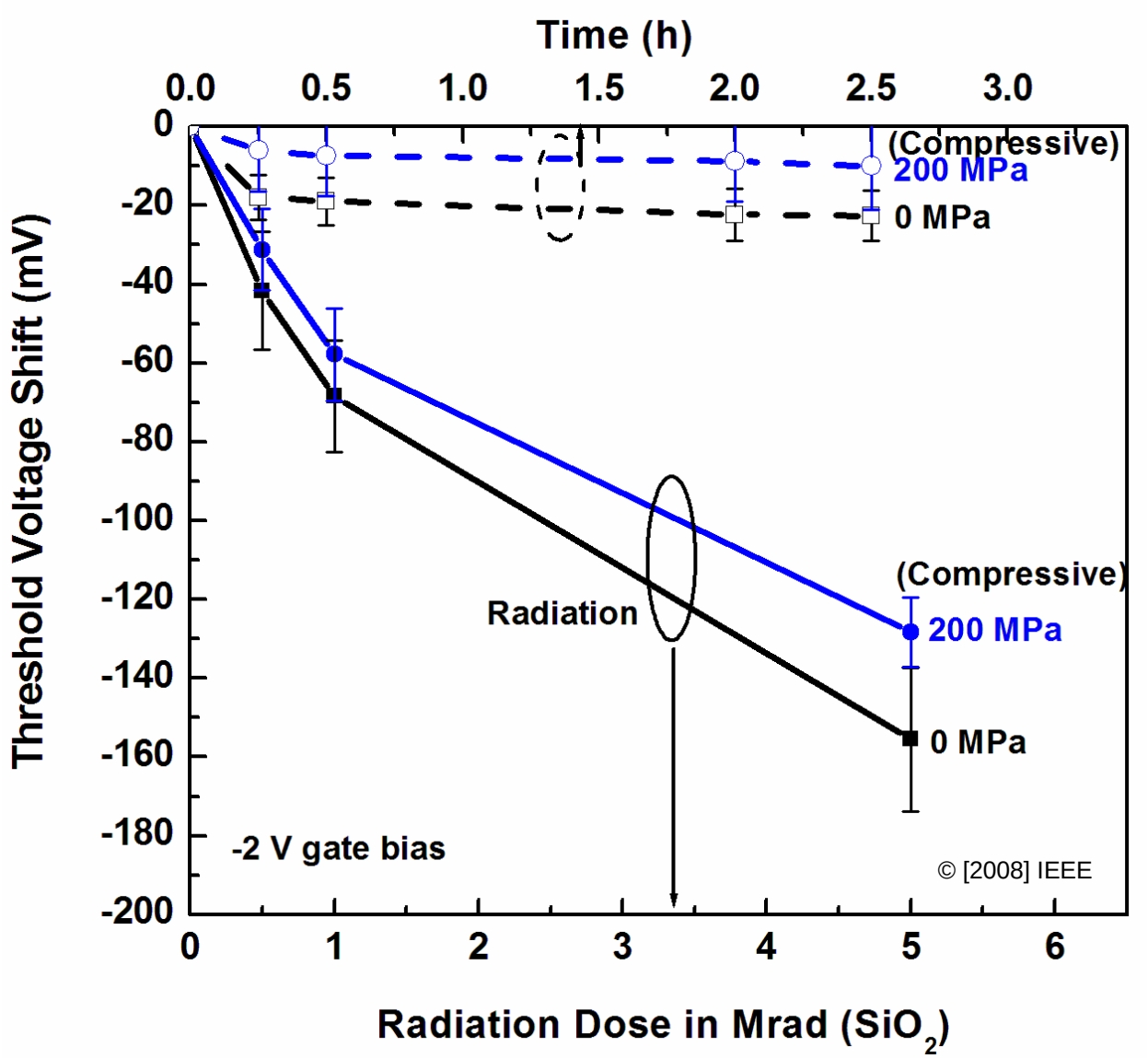


Figure 2-4. Threshold voltage shifts (ΔV_T) observed with and without tensile stress and radiation at -2V gate bias. [Reprinted, with permission, from H. Park, et al., Total Ionizing Dose Effects on Strained HfO_2-Based nMOSFETs, IEEE Trans. Nucl. Sci., vol. 55, pp.2983, Figure 4, Dec. 2008]

This is consistent with previous works on the oxygen vacancy defect that show that the trap microstructure and energy levels can be changed by stretching the Si-Si bonds and/or changing the bond angles [88-91]. The assumption that mechanical stress can

change the trap energy level (or trap activation energy) is also supported by a band diagram showing the relationship between trap activation energy and mechanical stress by Choi et al. [57], as shown in Figure 2-7.

We can consider two possible reasons why lowering hole trap energy levels will reduce charge trapping in HfO_2 and/or SiO_x. First, uniaxial mechanical stress may enhance the detrapping of holes in shallow trap sites, or the neutralization in deep trap sites by electron injection, as illustrated in Figure 2-8(a). This reduction in hole trap energy increases the probability that these defects can emit a trapped hole or capture an electron to compensate a nearby trapped hole. Trapped holes in deep trap sites can be neutralized by capturing electrons [89, 90].

Second, the effective hole mobility in the gate dielectrics along the <001> direction under uniaxial mechanical stress may be increased by reducing the average trap energy level. Hole transport in thin (~10 nm) high-k oxides is expected to be consistent with a multiple trapping model [49, 92, 93]. Holes move in oxides by trapping and detrapping from trap sites [49] as shown in Figure 2-8 (b). Reduced trap energy levels can increase the effective hole mobility, which is proportional to exp ($-E_a/kT$)[92]. E_a is the hole trap activation energy, k is the Boltzman constant, and T is temperature. Hence, strain-induced lowering of hole trap energy levels may reduce charge trapping in HfO_2 and SiO_x.

2.3.2 Radiation Induced Mobility Degradation under Uniaxial Stress

Electron mobility is shown as a function of gate over-drive voltage ($V_{GS}-V_T$) in Figure 2-9. 200 MPa of tensile stress enhances the electron mobility at all gate biases. Electron mobility degradation for devices irradiated to 5 Mrad(SiO_2) under 200 MPa of tensile stress is ~ 1% at $V_{GS}-V_T$ = 0.55 V, compared to the pre-irradiation 200 MPa

case, but the electron mobility is still higher than the unstressed case. Figure 2-10 shows the electron mobility enhancement as a function of stress before and after 5 Mrad(SiO_2) irradiation. The mobility enhancement compared to unstressed devices is positive after a total dose of 5 Mrad(SiO_2) at all tensile stress levels above 70 MPa , indicating the potential benefit of strained Si for producing radiation-hard nMOSFET devices.

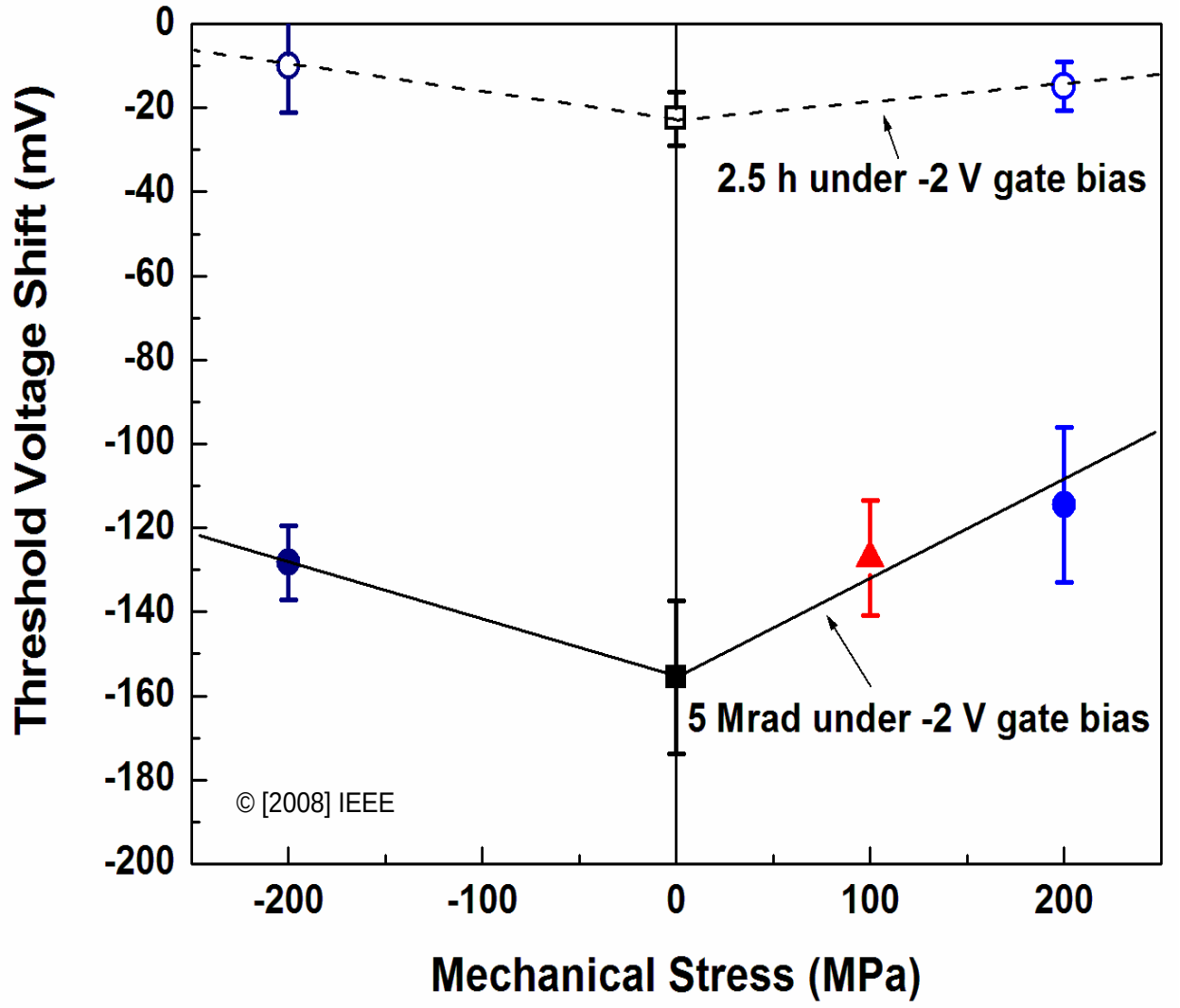
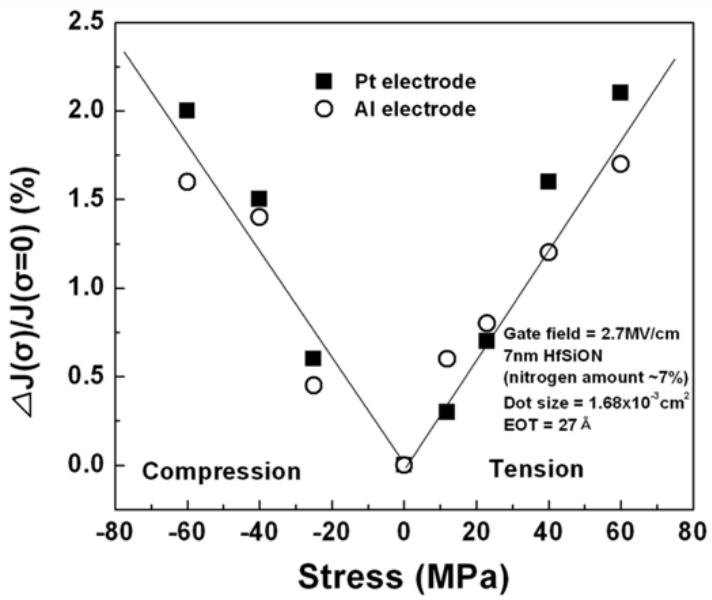


Figure 2-5. Threshold voltage shifts (ΔV_T) vs. mechanical stress after 5Mrad (SiO_2) and 2.5 h under -2 V gate bias. [Reprinted, with permission, from H. Park, et al., Total Ionizing Dose Effects on Strained HfO2-Based nMOSFETs, IEEE Trans. Nucl. Sci., vol. 55, pp.2984, Figure 5, December, 2008]



Figue 2-6. Gate leakage change in Si high-k MOS capacitor (7nm HfSiON dielectric) as a function of uniaxial stress. [Reprinted, with permission, from S. Y. Son, et al., "Strained induced changes in gate leakage current and dielectric constant nitrided Hf-silicate dielectric silicon MOS capacitors," Appl. Phys. Lett., vol. 93, p. 153505, Figure 3, Oct., 2008]

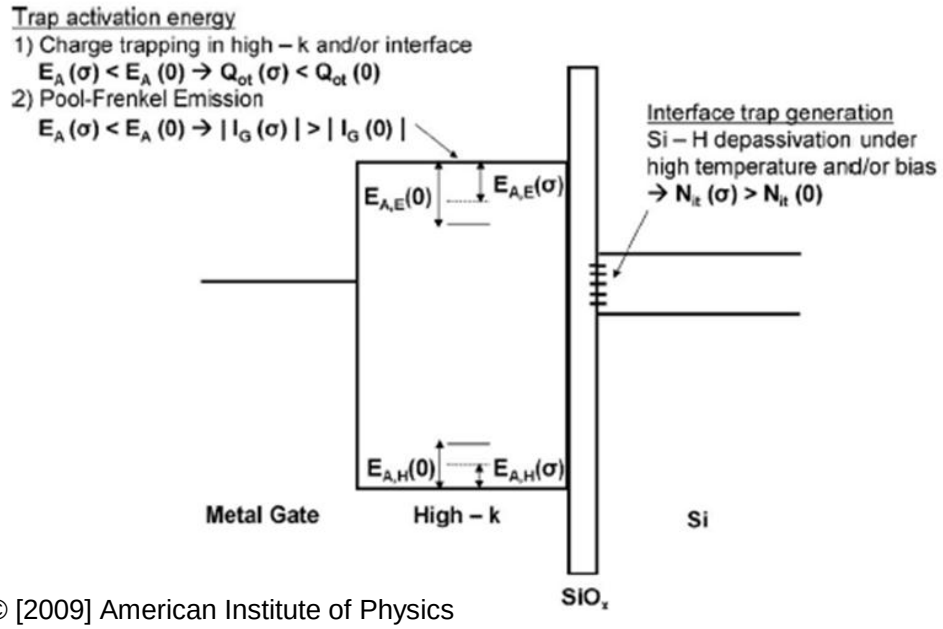


Figure 2-7. A band diagram of Si high-k MOS capacitor showing trap activation energy reduction as a function of uniaxial stress. [Reprinted, with permission, from Y. S. Choi, et al., "Reliability of HfSiON gate dielectric silicon MOS devices under [110] mechanical stress: Time dependent dielectric breakdown," J. Appl. Phys., vol. 105, p. 044503, Figure 7, Feb., 2009.]

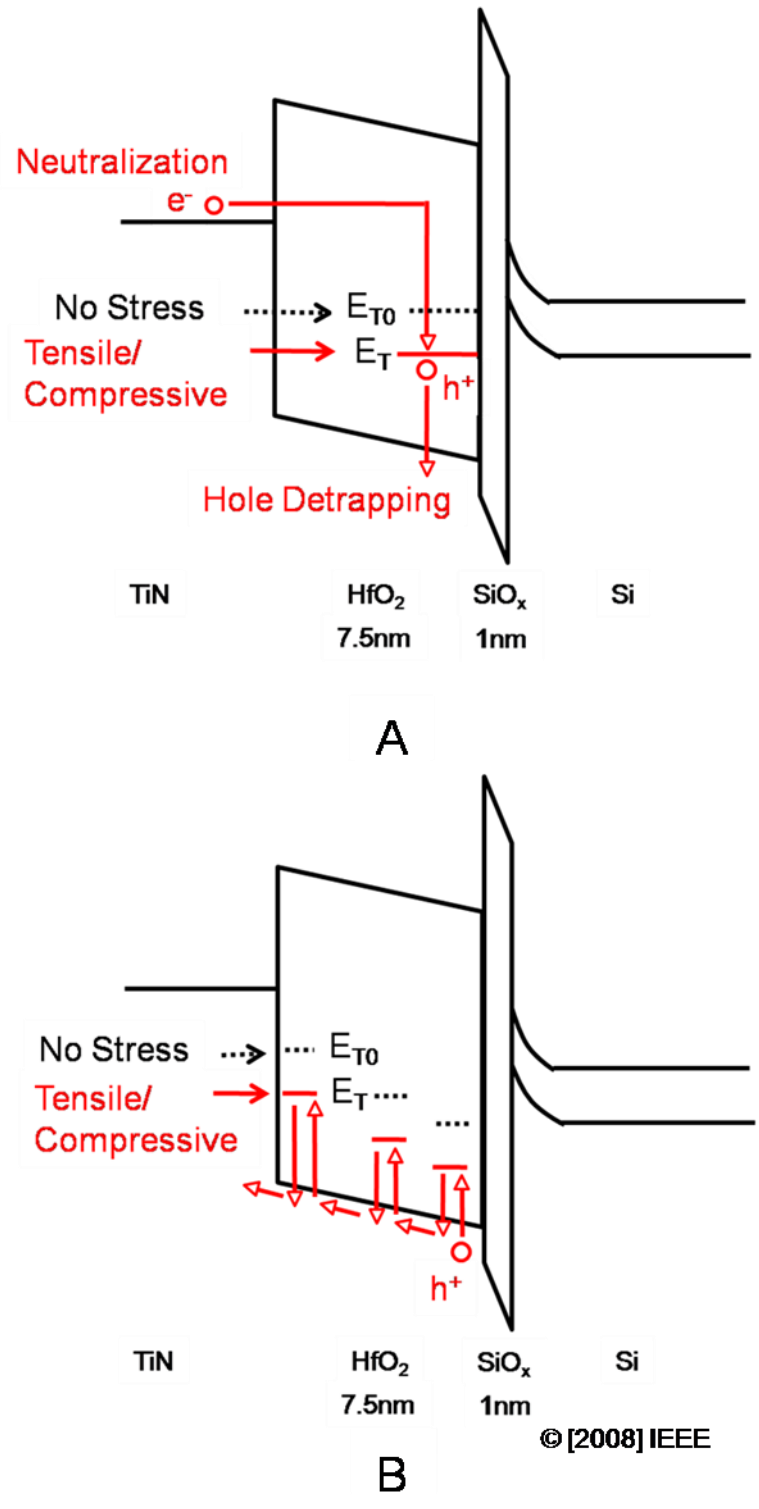


Figure 2-8. Radiation-induced charge trapping model under uniaxial stress A) Charge detrapping/neutralization model B) multiple trapping-detrapping hole transport model [49, 92]. [Reprinted, with permission, from H. Park, et al., Total Ionizing Dose Effects on Strained HfO2-Based nMOSFETs, IEEE Trans. Nucl. Sci., vol. 55, pp. 2984, Figure 6, Dec. 2008]

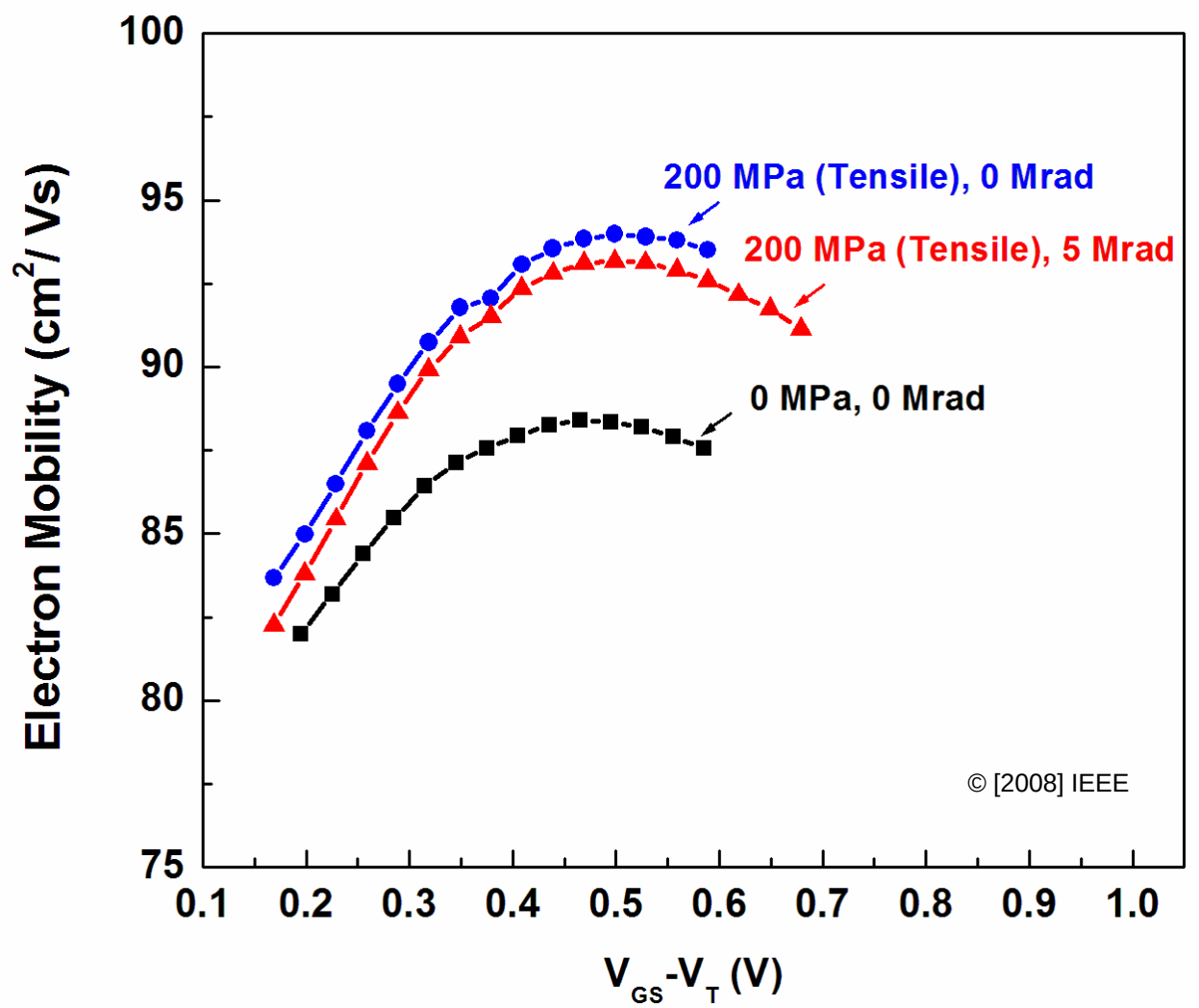


Figure 2-9. Electron mobility vs. gate over-drive voltage (V_{GS}-V_T) with and without uniaxial tensile stress (200 MPa) and radiation (5 Mrad) [Reprinted, with permission, from H. Park, et al., Total Ionizing Dose Effects on Strained HfO2-Based nMOSFETs, IEEE Trans. Nucl. Sci., vol. 55, pp. 2984, Figure 7, Dec. 2008]

2.4 Conclusion

Positive charge trapping is the dominant radiation-induced degradation mechanism in both unstressed and mechanically stressed HfO_2-based nMOSFETs. Uniaxial tensile and compressive stress in nMOSFETs decreases the amount of net positive charge trapping and reduces the threshold voltage shift. This is attributed to enhanced detrapping of holes or compensating electron trapping in HfO_2 and/or SiO_x,

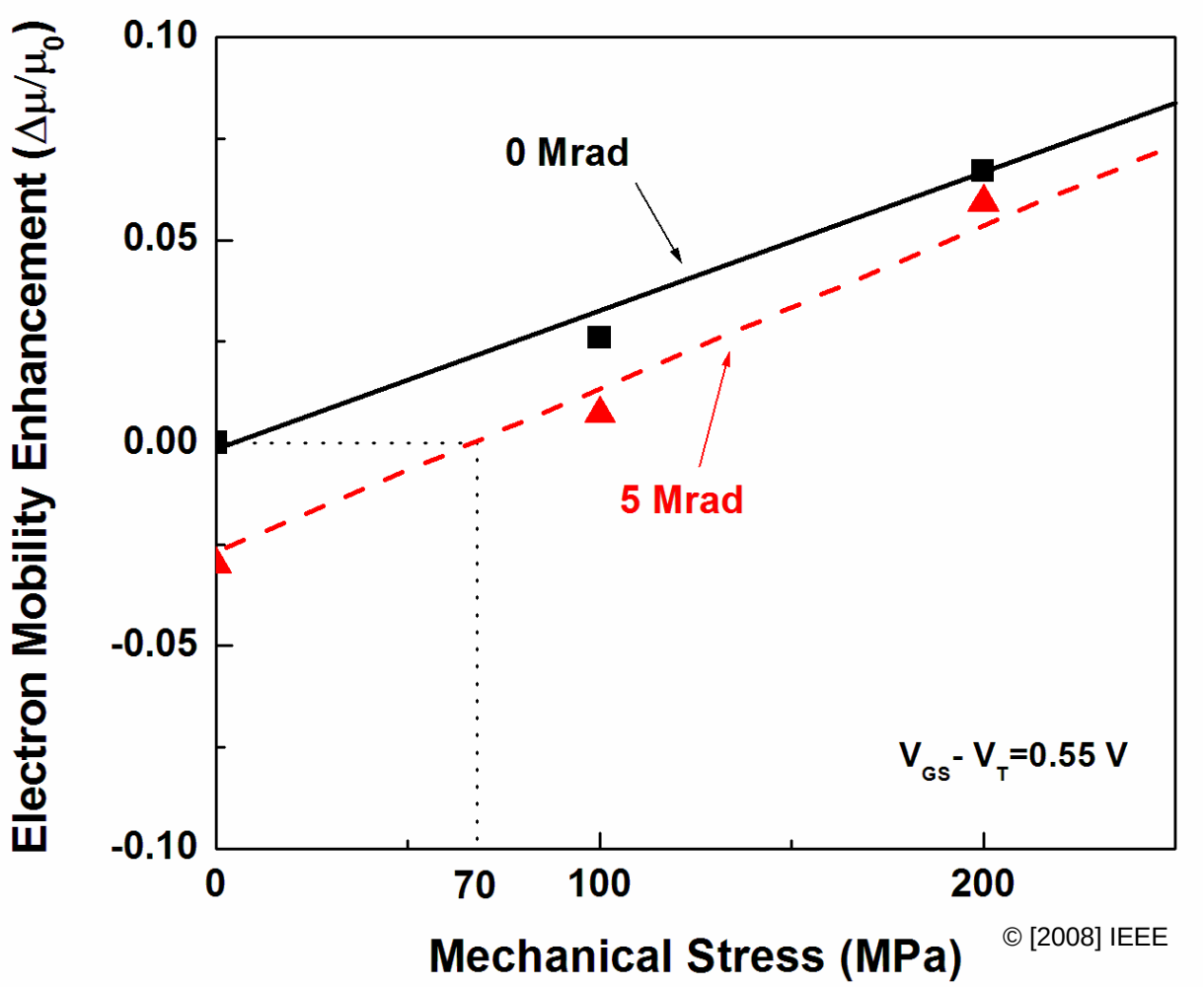


Figure 2-10. Electron mobility enhancement vs. mechanical stress before and after 5 Mrad (SiO_2) irradiation. [Reprinted, with permission, from [H. Park, et al., Total Ionizing Dose Effects on Strained HfO2-Based nMOSFETs, IEEE Trans. Nucl. Sci., vol. 55, pp. 2984, Figure 8, Dec. 2008]

and/or increasing effective hole mobility in the gate dielectric. Electron mobility enhancement with stress is retained in 5 Mrad(SiO_2) irradiated devices above approximately 70 MPa of tensile stress. Uniaxial strain engineering for drive current (mobility) enhancement has the potential to increase radiation hardness in these advanced HfO_2-based MOSFETs.

CHAPTER 3
LASER-INDUCED CURRENT TRANSIENTS IN STRAINED-SI N+/P DIODES

3.1 Introduction

Single event transients (SETs) and single event upsets (SEUs) are related to collection of radiation-generated charge at sensitive circuit nodes [25]. SETs and SEUs in unstressed deep-submicron MOSFETs have been studied extensively in recent years [25, 44, 66, 94-96]. Although strained-Si technology is widely adopted, the effects of mechanical stress on current transients generated by laser or ion strikes at the source/drain regions of uniaxially stressed devices have not been reported. It is important to understand how mechanical stress affects these transient pulses since the transport of the radiation-generated carriers in the substrate is affected by stress.

Laser-induced current transients on a uniaxially stressed Si N+/P junction diode are reported in this chapter. An N+/P diode is a good representation of the source/drain junctions that are responsible for charge collection in n-channel MOSFETs. P-channel MOSFETs are also important for considering SETs and SEUs. However, stress-induced electron mobility enhancement is easier to understand than that of holes [17, 18, 97, 98], so N+/P diodes are used in this chapter.

The shapes of current transients and the amount of collected charges are measured as a function of stress, because both of them are crucial in predicting SETs and SEUs in circuits [25]. Controlled external mechanical stress is applied via a four-point bending setup [35] while the samples are irradiated using a picosecond pulsed

laser [99, 100]. The characterization system is based on the direct measurement of the current transients [101, 102]. The FLOODS simulation tool [103] is used to investigate the mechanisms responsible for the differences in charge collection between stressed and unstressed devices. Additionally, the simulations provide insight into the effects of high mechanical stress (~1 GPa) on laser-induced current transients, above the maximum stress that could be applied using the four-point bending setup (240 MPa on these samples).

3.2 Experimental Setup

The laser-induced current transients in mechanically-stressed Si N+/P diodes are captured using a high-speed measurement system with an integrated four-point bending setup, as shown in Figure 3-1 and 3-2. The samples used in this study are N+/P diodes fabricated on (001) Si wafers using a standard 130-nm CMOS technology. The active area of the diodes is 50 µm × 100 µm. Nickel silicide (NiSi), silicon oxide (SiO_x), and copper (Cu) patterns are present on top of the diodes as shown in Figure 3-3 using transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS).The thickness of the NiSi, SiO_x, and Cu patterns is ~20 nm, 720 nm, and 280 nm, respectively. The doping densities of the n^+, p-well, and p-substrate are ~10^{20}, ~10^{18}, and ~10^{16} cm^{-3}, respectively [104]. The shallow trench isolation (STI) in these devices is an additional source of mechanical stress. However, STI-induced stress in the center of the large diodes is negligible [105]. Uniaxial mechanical stress along the <110> direction is applied using a four-point bending setup [35].

A cavity-dumped dye laser with a wavelength of 590 nm, a pulse energy of 218 pJ, and a pulse width of 1 ps is used to inject electron-hole pairs in the diode. The laser direction is normally incident to the diode surface with a spot size of 6.3 µm full-width-

half-maximum diameter. The peak carrier concentration produced by the laser is ~1.6 × 10^{19} cm^{-3}. The pulse laser energy reaching the diode active area is smaller than the value measured at the surface of the structure due to the optical properties of the layers on top of the diode [99, 106].

The transient measurement system uses a Tektronix TDS8200 digital sampling oscilloscope with 80E03 sampling module (20 GHz bandwidth) and is connected to the device using a bias tee (10 kHz to 40 GHz) and a ground-signal-ground (GSG) probe tip (DC to 40 GHz).

Current transients on the N+/P diode are measured under different values of stress (160 MPa and 240 MPa tensile, no stress, and 160 MPa compressive) with a 5 V reverse bias.

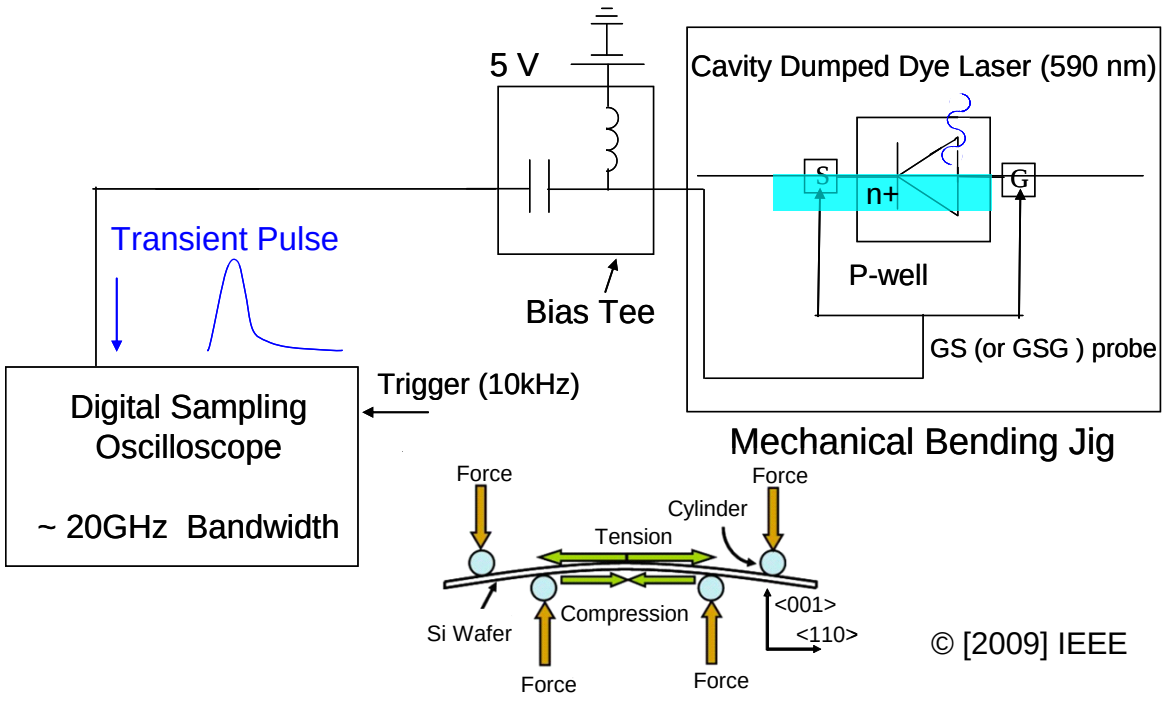


Figure 3-1. Schematic of Laser-induced current transient measurement system using a four- point bending setup. [Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes, IEEE Transaction on Nuclear Science, , IEEE Trans. Nucl. Sci., vol. 56, pp. 3203, Figure 1, Dec. 2009]

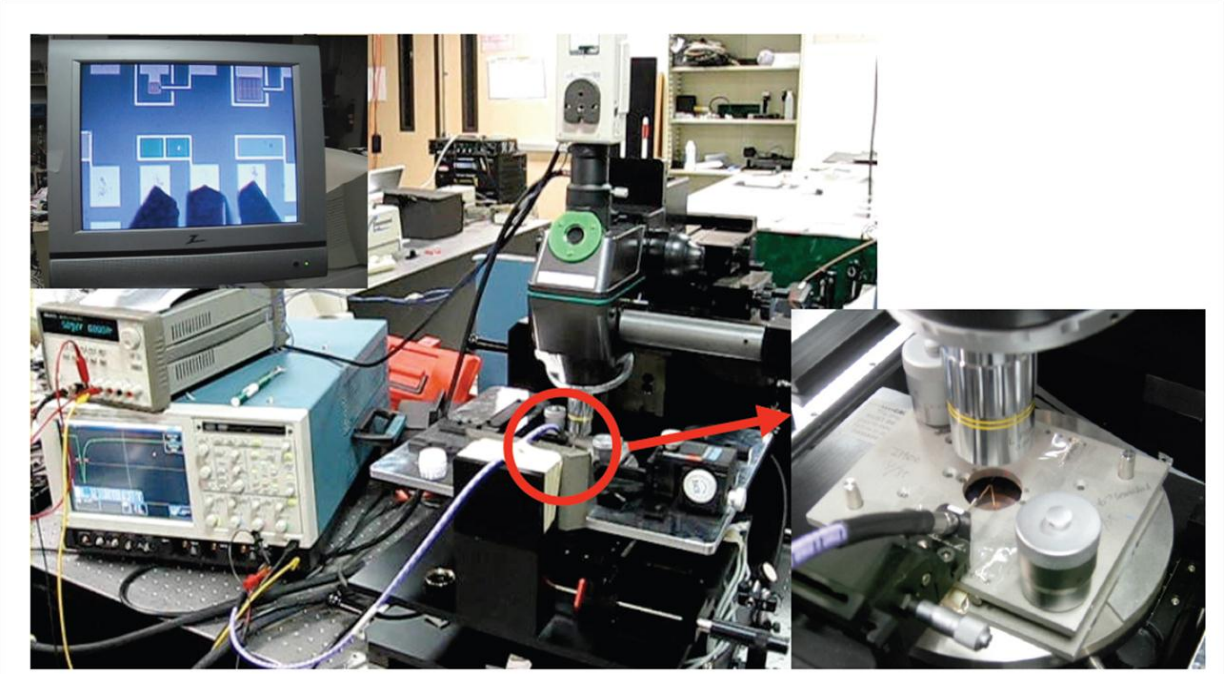
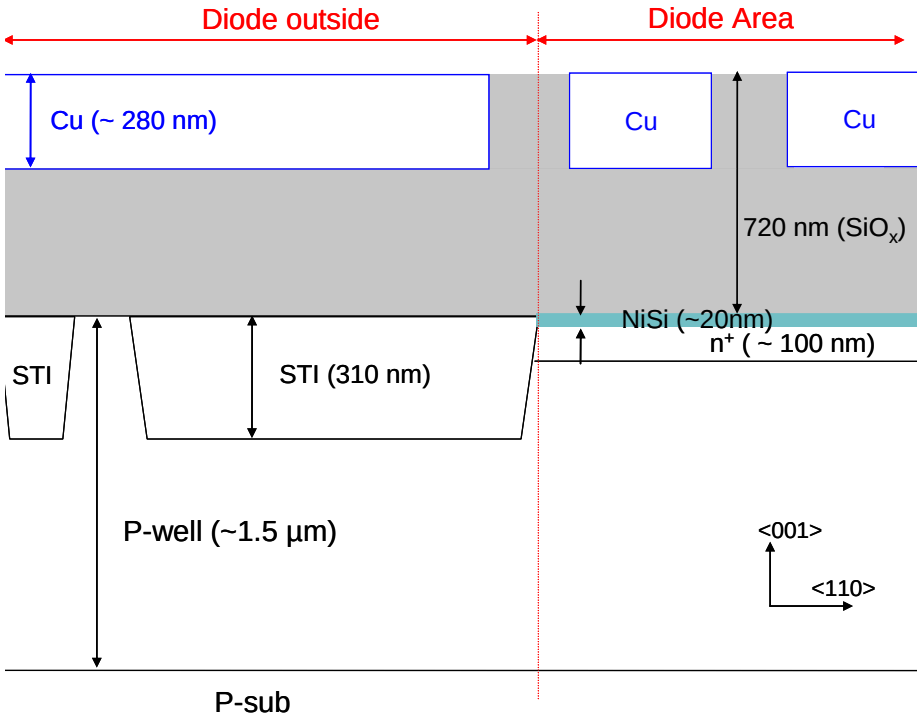


Figure 3-2. High speed measurement system for measuring current transients in diodes as a function of uniaxial stress.

Although the maximum applied stress (~240 MPa) in this investigation is about 16% of that produced by process- induced stressors (~ 1.5 GPa), the experiments still show the dominant mechanisms in the effects of stress on SETs; this approach is analogous to previous works describing the effects of stress on unirradiated MOS devices [17, 19, 34-37, 73, 107].

3.3 Experimental Results and Discussion

The effect of the applied mechanical stress on maximum current and charge collection is characterized by monitoring laser-induced current transients at each uniaxial stress value. Increasing tensile stress results in lower maximum currents (I_{max}) and collected charges (Q) than those measured under no stress, as shown in Figure 3-4 for times up to 10 ns after the laser pulse strikes the device. Each transient curve is measured using an averaging technique (100 points) in the sampling oscilloscope. Q is obtained by integrating the measured transient as a function of time. The data points



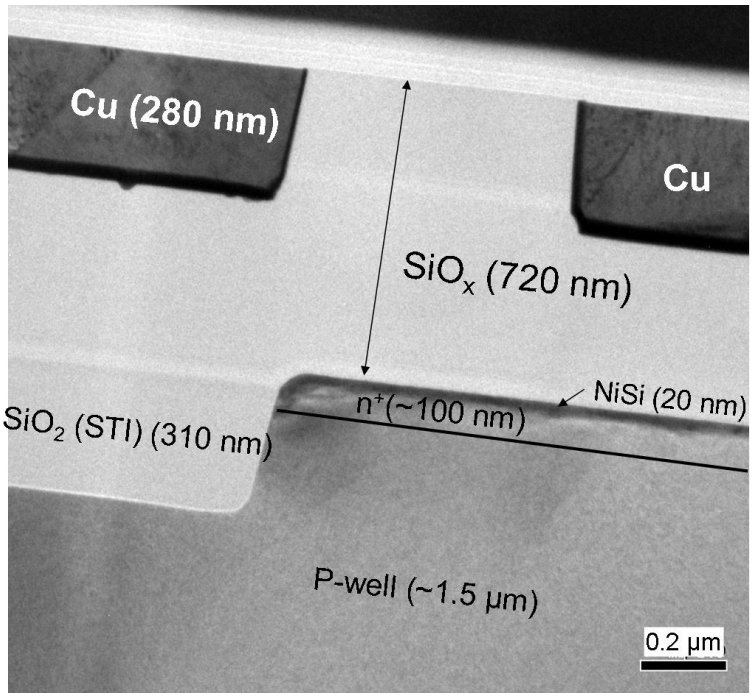


Figure 3-3 Cross section of N+/P diode A) Schematic through TEM and EDS analysis (not to scale) B)TEM image. [Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes, IEEE Transaction on Nuclear Science, , IEEE Trans. Nucl. Sci., vol. 56, pp. 3203, Figure2, Dec. 2009]

are the average *Q* at each level. The error bars in the data points represent the standard deviation in the data at that stress level. Opposite to tensile stress, compressive stress increases I_{max} and *Q*. A decrease/increase in I_{max} and *Q* under tensile/compressive stress can be explained by a 1-D transient analytical solution [108].

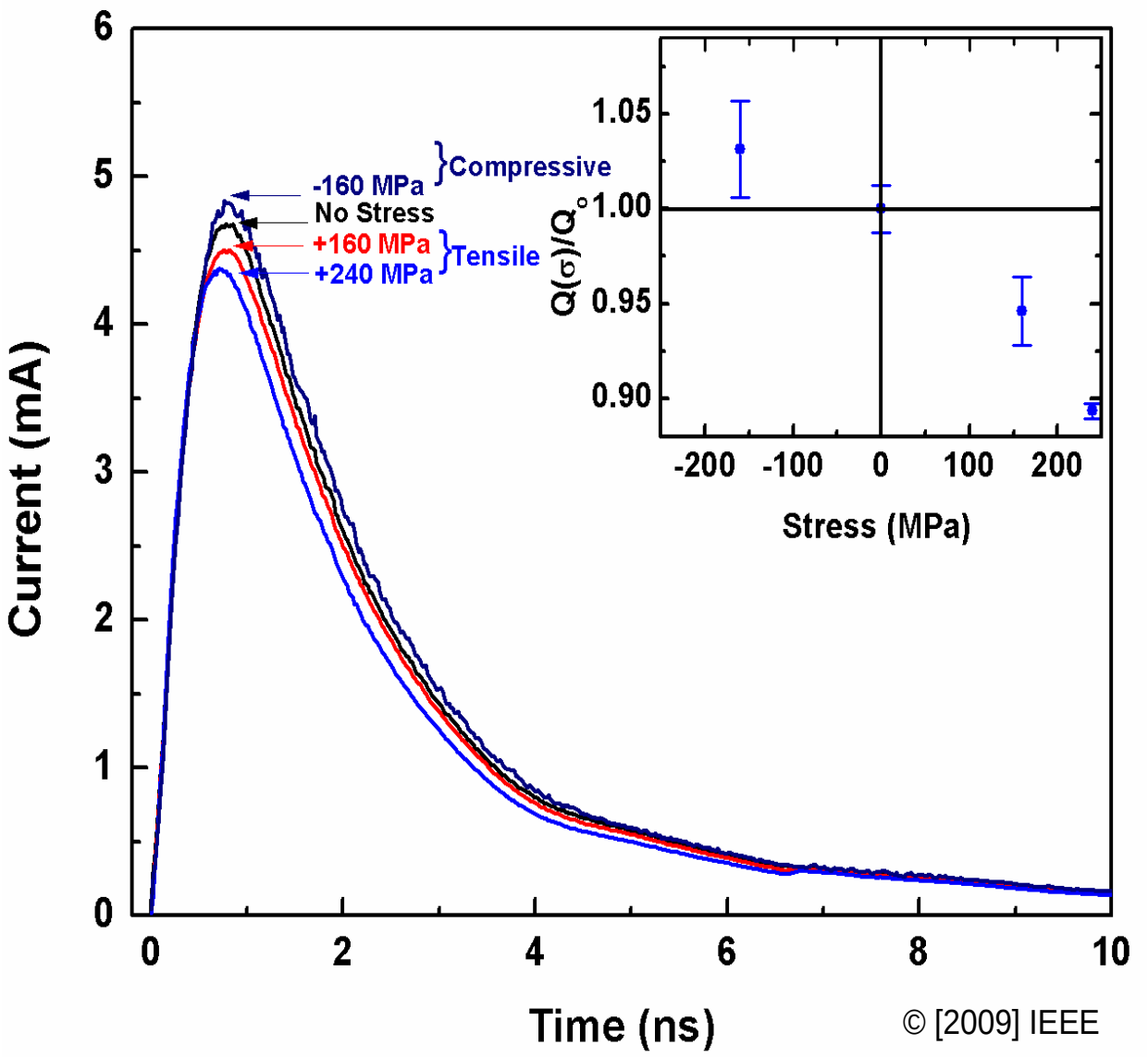


Figure 3-4 Laser-induced current transients and the ratio of collected charge measured as a function of <110> uniaxial mechanical stress. [Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes, IEEE Transaction on Nuclear Science, IEEE Trans. Nucl. Sci., vol. 56, p. 3205, Figure 3 , Dec. 2009]

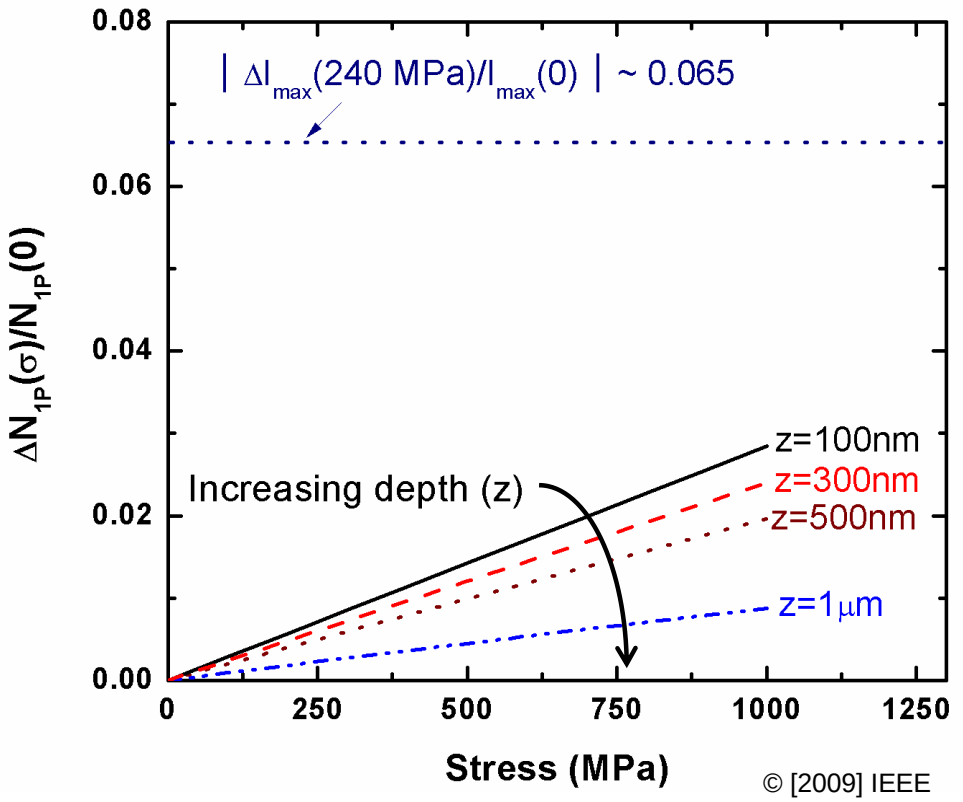


Figure 3-5. The number of laser-generated electron-hole pairs as a function of depth (z) and <110> uniaxial tensile stress.[Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes, IEEE Transaction on Nuclear Science, , IEEE Trans. Nucl. Sci., vol. 56, p. 3205, Figure 4, Dec. 2009]

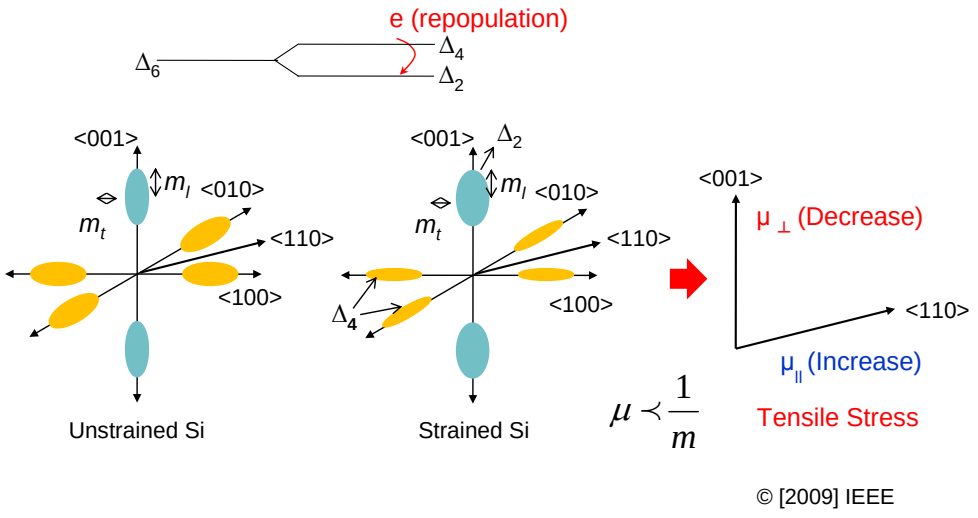


Figure 3-6. Uniaxial tensile stress effect on electron mobility [97]. [Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes, IEEE Transaction on Nuclear Science, , IEEE Trans. Nucl. Sci., vol. 56, pp. 3206, Figure 5, Dec. 2009]

Current transients (*I(t)*) are proportional to $N\mu_{n\perp}$ in the solution [108], where *N* is the number of laser-generated electron-hole pairs and $\mu_{n\perp}$ is electron mobility along the <001> direction. $\mu_{n\perp}$ is the dominant contribution for electron mobility, because electrons are mainly moving in the <001> direction due to applied field along the <001> direction for the large diodes used in the experiment. *N* as a function of depth in Si is defined as [100]

$$N(z) = \frac{\alpha(\sigma)}{\hbar\omega}\exp(-\alpha(\sigma)z)\int_{-\infty}^{\infty} I_0(z,t)dt \tag{3-1}$$

where α is the absorption coefficient of Si, $\hbar\omega$ is the photon energy (2.1 eV), *z* is depth in the Si, I_0 is the intensity of the laser beam, and *t* is the time. α depends on the band gap [109], where a normalized stress dependent α is defined as

$$\frac{\Delta\alpha(\sigma)}{\alpha} = \frac{\Delta E_g(\sigma)}{\hbar\omega - E_g} << 1, \quad \hbar\omega > E_g \tag{3-2}$$

where σ is the mechanical stress, and E_g is the Si band gap (1.12 eV). Based on (3.1) and (3.2), a change in *N* as a function of uniaxial tensile stress and the depth into Si is plotted in Figure 3-5. Since stress-induced bandgap narrowing in Si is minimal (~0.01 eV at 240 MPa of both compressive and tensile stress) [34], an increase in α of Si for this range of mechanical stress is negligible [109]. As a result, there is no significant increase calculated in *N* at each depth under mechanical stress, less than 1% at 240 MPa of tensile stress, as shown in Figure 3-5. [100].

Since the change in *N* due to stress is minimal, a ~6.5% decrease in I_{max} at 240 MPa of tensile stress is caused mainly by a decrease in electron mobility along the <001> direction. Likewise, for compressive stress, an increase in I_{max} results from an increase in electron mobility along the <001> direction, because strain-induced band

gap narrowing is very small (~0.01 eV at 240 MPa). This suggests that a decrease/increase in electron mobility along the <001> direction under tensile/compressive stress ($\Delta\mu_{n\perp}$) results in a decrease/increase in I_{max}. The experimental results and qualitative analysis both can be explained by previous results on piezoresistance (π) coefficients in Si [110, 111].

The π coefficient represents changes of mobility resulting from applied stress,

$$\pi = -\frac{\mu(\sigma) - \mu(0)}{\sigma\mu(0)} = -\frac{\Delta\mu}{\sigma\mu(0)} \tag{3-3}$$

where $\mu(\sigma)$ and $\mu(0)$ are the mobility with and without stress, respectively, and $\Delta\mu$ is the change in the mobility. Changes (increase or decrease) of the electron mobility result from changes of the average electron effective mass (m^*), due to repopulation of electrons under mechanical stress [37, 97, 111]. For example, Figure 3-6 shows that tensile stress splits the conduction bands into Δ_2 and Δ_4. Electrons repopulate from the Δ_4 valley into the Δ_2 valley. The Average effective mass along the <110> direction ($m_{//}$) decreases under tensile stress in the same direction, but the average effective mass along the <001> direction ($m_{\perp}$) increases under tensile stress in the <110> direction [97]. Thus, <110> tensile stress decreases the electron mobility along the <001> direction ($\mu_{n\perp}$), because μ is inversely proportional to m^* [97]. The opposite dependence is expected with compressive stress. The concept of the π coefficient is implemented in current-transient simulations for diodes under mechanical stress in the next section.

Q is also proportional to the funneling length, $L = (1+\mu_{n\perp}/\mu_{p\perp})W$, where $\mu_{p\perp}$ is the hole mobility along the <001> direction, and W is the depletion width [30, 31]. A change in hole mobility along the <001> direction ($\Delta\mu_{p\perp}$) under uniaxial mechanical stress is negligible (~ 0.3% at 250 MPa) [110]. Therefore, the change of the collected charge

(ΔQ) as a function of the applied mechanical stress is also dominated by the change in electron mobility ($\Delta\mu_{n\perp}$).

By applying the same concepts for analyzing *I(t)* and *L* as in the N+/P diodes above, it is possible to predict how current transients in P+/N diodes would change under mechanical stress. Since *I(t)* is proportional to $N\mu_{p\perp}$ and $\Delta\mu_{p\perp}$ (~ 1% at 1 GPa) is not significant, the change in I_{max} is not expected to be significant under stress. *Q* is likely to increase with tensile and decrease with compressive stress, because *L* is equal to $(1+\mu_{p\perp}/\mu_{n\perp})W$ [112] and affected by $\Delta\mu_{n\perp}$. However, further experimental data and simulation in P+/N diodes as a function of uniaxial stress will be discussed in Chapter 4.

Table 3-1. Values of Smith's piezoresistance (π) coefficients (10^{-5} MPa $^{-1}$)[111].

	Electron	Hole
π_{11}	-102.2	6.6
π_{12}	53.4	-1.1
π_{44}	-13.6	138.1

3.4 Simulation Results and Discussion

3.4.1 Baseline Simulation Results under No Stress

Based on the previous experimental analysis, FLOODS simulations are performed to understand the mechanisms of carrier transport under uniaxial stress and to predict how high stress (~1GPa) affects the current transients in diodes. The Masetti and Brooks-Herring mobility models are used to account for carrier transport in a high injection case [113]. Shockley-Read-Hall and Auger band-to-band recombination models are also considered [113, 114]. The number and distribution of electron-hole pairs generated by the laser pulse is calculated by a single-photon absorption (SPA) equation [99, 100].

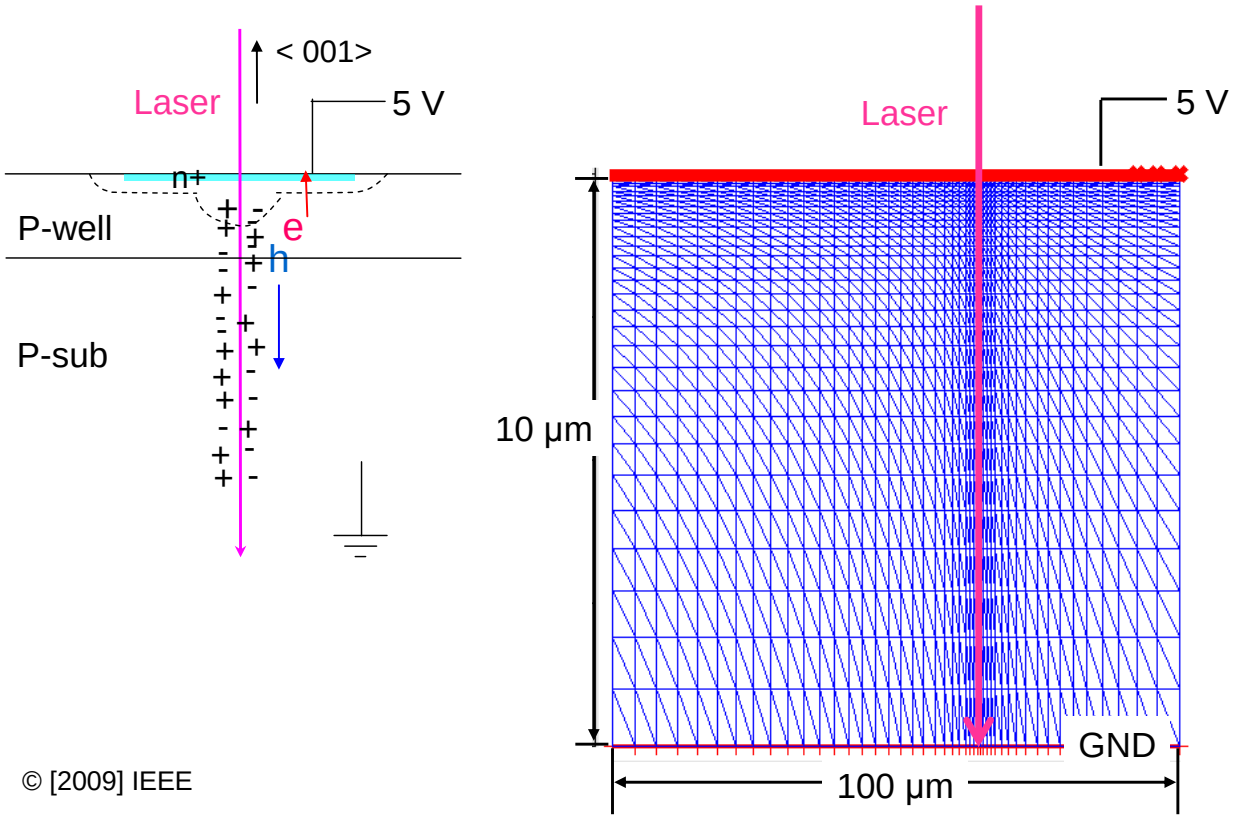


Figure 3-7. Schematic of laser-induced current transients and 2-dimensional simulation structure of an N+/P diode. [Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes, IEEE Transaction on Nuclear Science, IEEE Trans. Nucl. Sci., vol. 56, pp. 3206, Figure 6, Dec. 2009]

Before analyzing the effects of stress on current transients, baseline simulations under no stress are performed. These results are matched to the measured current transient under no stress. It is very important to understand the physics that dominates current transients in an unstressed case in order to predict the results under a stressed case. A 2-dimensional simulation structure, shown in Figure 3-7, is built based on analysis of the structure and material of the N+/P diodes, as shown in Figure 3-3. The width and depth of the diodes are 100 μm and 10 μm, respectively. The SiO_x, Cu dummy patterns, and NiSi are not implemented in the simplified FLOODS simulations.

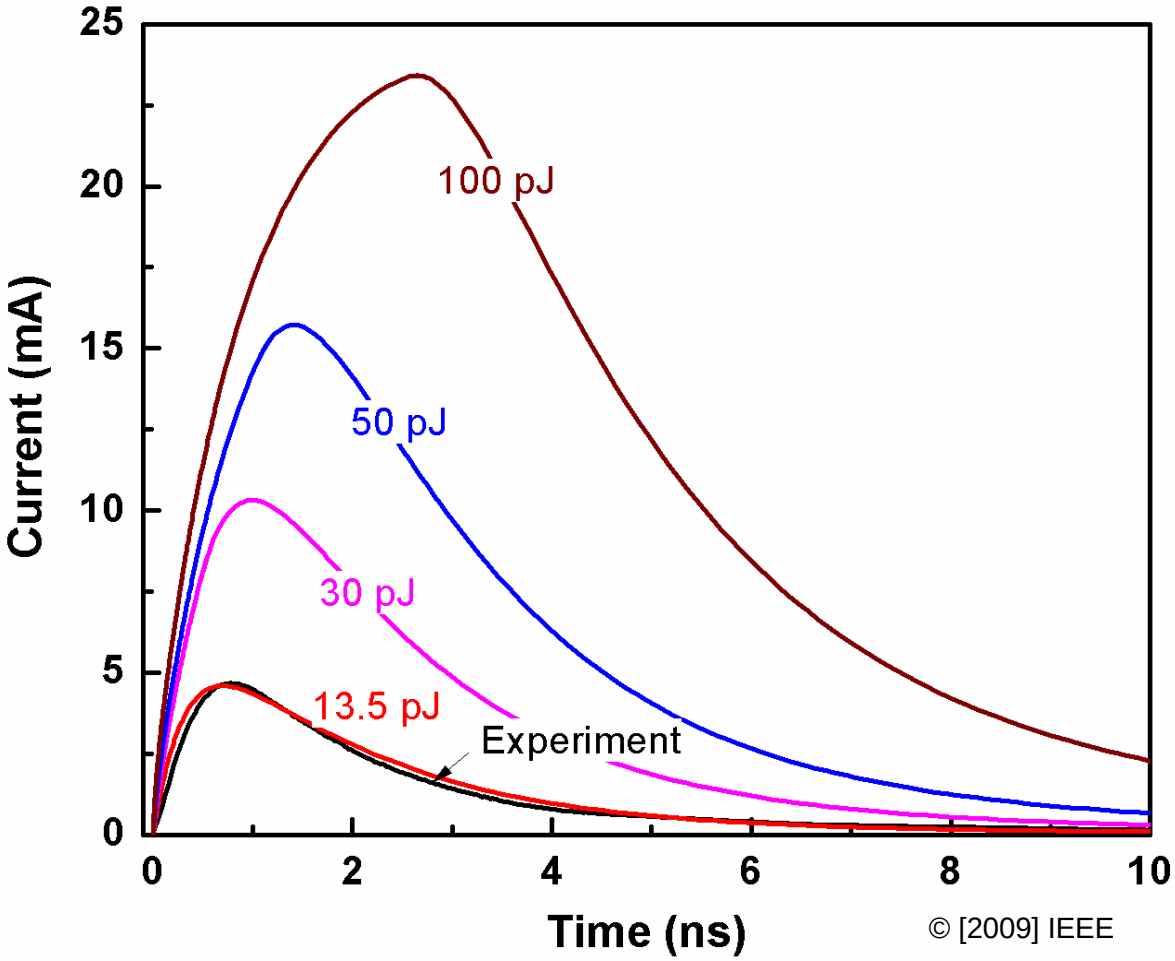


Figure 3-8. Simulated energy dependence of laser-induced current transients. [Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes, IEEE Transaction on Nuclear Science, , IEEE Trans. Nucl. Sci., vol. 56, pp. 3206, Figure 7, Dec. 2009]

However, the omitted layers can reduce laser energy due to the reflection, absorption, and transmission properties of each material [99, 106]. Figure 3-8 shows that a decrease in laser pulse energy results in a decrease in the peak current and charge collection. The simulated result for the case of pulse energy of 13.5 pJ agrees with the experiment result, as shown in Figure 3-8. However, the pulse energy (13.5 pJ) is much different from the measured pulse energy (218 pJ). The discrepancy can be explained by the absorption, reflection, and transmission properties of each layer over the active region of the diode. Since 43% of the spot area of incident laser is occupied by Cu

dummy patterns which block the laser [100], only 57% of incident laser energy is transmitted. Next, only 78% of the energy is transmitted through the 720 nm SiO_x, due to reflection losses at the interfaces [99]. Lastly, 16% of the energy is transmitted through NiSi, based on [106]. Therefore, the calculated pulse laser energy reaching the diode active area is ~15.5 pJ, ~7.1% (= 0.57 x 0.78 x 0.16) of the incident energy. If the thickness of each layer varies by ~10% and the composition of the $NiSi_x$ also varies, the calculated laser energies range from 12.5 to 22 pJ. The collected charge in the simulation (12.8 pC) agrees well with the average collected charge in the experiment (12.3 pC). As a result, the amount of energy used in the simulations to produce agreement with the experiments, 13.5 pJ, is reasonable.

3.4.2 Simulation Results under Stress

A piezoresistive mobility model based on Smith's π-coefficients as shown in Table 3-1 is used to consider mobility enhancement as a function of mechanical stress [110, 111, 114]. The 6 x 6 piezoresistive model is defined as

$$\begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \begin{bmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{23} \\ \sigma_{13} \\ \sigma_{12} \end{bmatrix} = \begin{bmatrix} \Delta\rho_{11}/\rho_{11} \\ \Delta\rho_{22}/\rho_{22} \\ \Delta\rho_{33}/\rho_{33} \\ \Delta\rho_{23}/\rho_{23} \\ \Delta\rho_{13}/\rho_{13} \\ \Delta\rho_{12}/\rho_{12} \end{bmatrix} = \begin{bmatrix} -\Delta\mu_{11}/\mu_{11} \\ -\Delta\mu_{22}/\mu_{22} \\ -\Delta\mu_{22}/\mu_{22} \\ -\Delta\mu_{23}/\mu_{23} \\ -\Delta\mu_{13}/\mu_{13} \\ -\Delta\mu_{12}/\mu_{12} \end{bmatrix} \quad (3\text{-}4)$$

where π_{ij}, σ_{ij}, ρ_{ij}, and μ_{ij} are components of the piezoresistance coefficient, mechanical stress, resistivity, and carrier mobility, respectively, and $\Delta\rho_{ij}/\rho_{ij}$ and $\Delta\mu_{ij}/\mu_{ij}$ are fractional changes in resistivity and mobility. Since the doping densities and dopant type are different in each region of N+/P diode, the doping dependence of the π-coefficients derived by Kanda [115] is used (Figure 3-9 and 3-10).The piezoresistance

coefficients are multiplied by piezoresistance factor, *P(N,T).*Temperature (*T*) used in the simulation is 300K, because the experiment was done in room temperature and no wafer heating effect is observed.

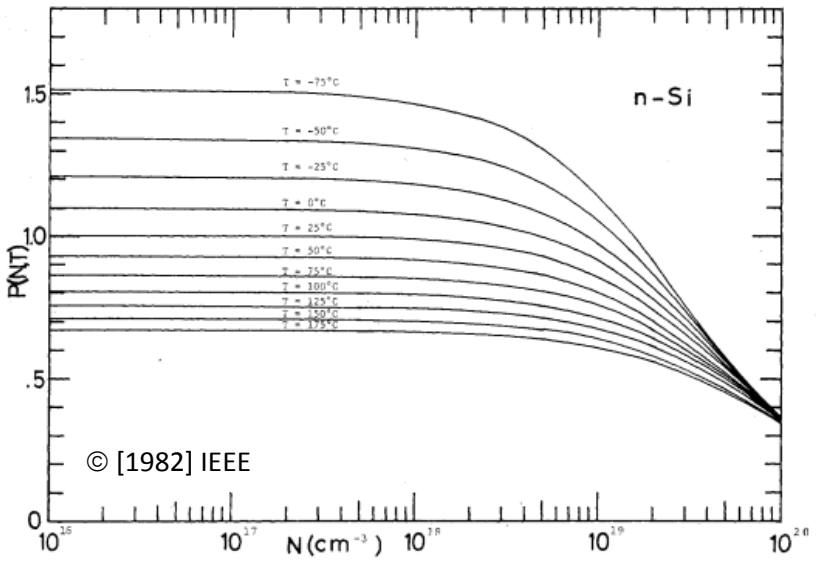


Figure 3-9. Piezoresistance factor *P(N,T)* as a function of doping density (*N*) and temperature (*T*) for n-type Si. [Reprinted, with permission, from Y. Kanda, "A Graphical Representation of the Piezoresistance Coefficients in Silicon," *IEEE Trans. Electron Dev.,* vol. 29, pp. 68, Figure 8 , Jan., 1982]

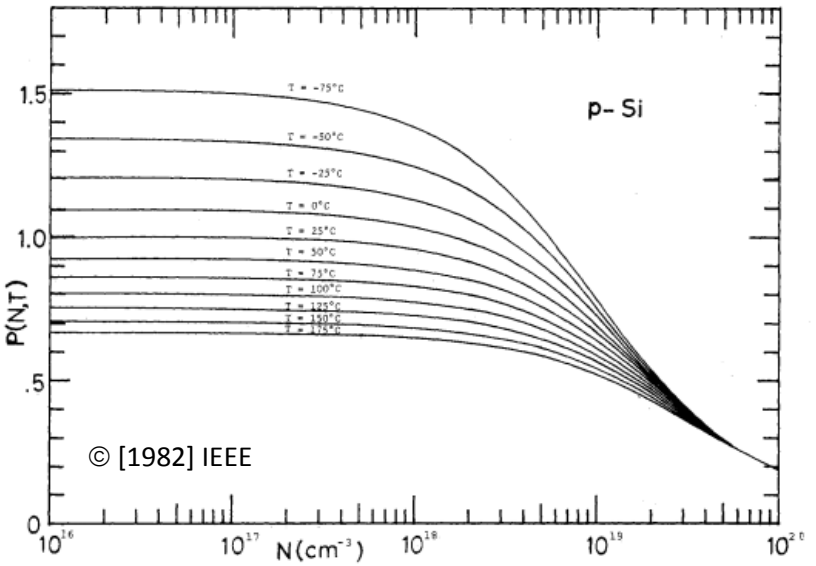


Figure 3-10. Piezoresistance factor *P(N,T)* as a function of doping density (*N*) and temperature (*T*) for p-type Si. [Reprinted, with permission, from Y. Kanda, "A Graphical Representation of the Piezoresistance Coefficients in Silicon," *IEEE Trans. Electron Dev.,* vol. 29, pp. 68, Figure 8 , Jan., 1982]

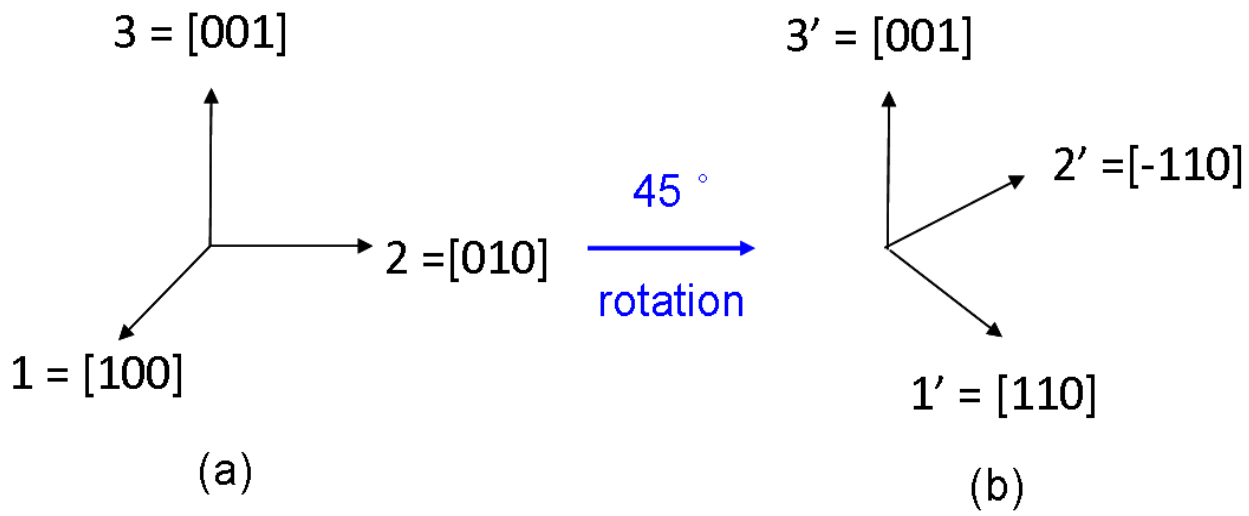


Figure 3-11. Transformation of the Cartesian coordinates system for two demensional FLOODS simulation. A) original B) transformed.[116]

Since two dimensional FLOOD simulation in N+/P diode are performed to minimize simulation complexity and reduce simulation time, a two dimensional piezoresistive model is used to predict the effect of uniaxial stress on current transient in N+/P diode. The details of transferring three to two dimensional piezoreistive matrix are discussed by Cummings in detail [116]. 3X3 piezoresistive model for two dimensional simulation is expressed as

$$\begin{bmatrix} \pi_{11} & \pi_{13} & 0 \\ \pi_{13} & \pi_{33} & 0 \\ 0 & 0 & \pi_{44} \end{bmatrix} \begin{bmatrix} \sigma_{11} \\ \sigma_{33} \\ \sigma_{13} \end{bmatrix} = \begin{bmatrix} \Delta\rho_{11}/\rho_{11} \\ \Delta\rho_{33}/\rho_{33} \\ \Delta\rho_{13}/\rho_{13} \end{bmatrix} = \begin{bmatrix} -\Delta\mu_{11}/\mu_{11} \\ -\Delta\mu_{33}/\mu_{33} \\ -\Delta\mu_{13}/\mu_{13} \end{bmatrix} \tag{3-5}$$

Since uniaxial stress is applied to the diodes along the <110> direction via a wafer bending set up, the original Cartesian coordinates system is transformed to the modified Cartesian coordinates system for two dimensional simulation, as shown in Figure 3-11. The transformed piezoresistive matrix for the new cordinates system using directional cosine [110, 115, 116] is defined as

$$\begin{bmatrix} \pi'_{11} & \pi'_{13} & 0 \\ \pi'_{13} & \pi'_{33} & 0 \\ 0 & 0 & \pi'_{44} \end{bmatrix} \begin{bmatrix} \sigma'_{11} \\ \sigma'_{33} \\ \sigma'_{13} \end{bmatrix} = \begin{bmatrix} \Delta\rho'_{11}/\rho'_{11} \\ \Delta\rho'_{33}/\rho'_{33} \\ \Delta\rho'_{13}/\rho'_{13} \end{bmatrix} = \begin{bmatrix} -\Delta\mu'_{11}/\mu'_{11} \\ -\Delta\mu'_{33}/\mu'_{33} \\ -\Delta\mu'_{13}/\mu'_{13} \end{bmatrix} \quad (3\text{-}6)$$

where π'_{ij}, σ'_{ij}, ρ'_{ij}, and μ'_{ij} are components of the piezoresistance coefficient, mechanical stress, resistivity, and carrier mobility, respectively, and $\Delta\rho'_{ij}/\rho'_{ij}$ and $\Delta\mu'_{ij}/\mu'_{ij}$ are fractional changes in resistivity and mobility.

Table 3-2. Values of transformed piezoresistance (π) coefficients (10^{-5} MPa $^{-1}$) used in two-dimensional FLOODS [116]

	Electron	Hole
π'_{11}	-31.2	71.8
π'_{13}	53.4	-1.1
π'_{33}	-102.2	6.6
π'_{44}	-13.6	138.1

The 3X3 piezoresistive matrix (3.6) for new coordinates system is implemented to simulate current transients in N+/P diodes as a function of <110> uniaxial stress. For <110> uniaxial stress, the value of both σ'_{33} and σ'_{13} are 0 MPa. The range of σ'_{13} from -1GPa to 1GPa is used in FLOODS simulation, as shown in Figure 3-12. From Eq. (3-6), currents are calculated as a function of mechanical stress. Current densities are expressed as

$$\begin{bmatrix} \frac{\mu'_{11}-\Delta\mu'_{11}}{\mu'_{11}} & \frac{-\Delta\mu'_{13}}{\mu'_{13}} \\ \frac{-\Delta\mu'_{13}}{\mu'_{13}} & \frac{\mu'_{33}-\Delta\mu'_{33}}{\mu'_{33}} \end{bmatrix} \begin{bmatrix} J_{1'}(0) \\ J_{3'}(0) \end{bmatrix} = \begin{bmatrix} J_{1'}(\sigma) \\ J_{3'}(\sigma) \end{bmatrix} \quad (3\text{-}7)$$

where $J_{i'}(0)$ and $J_{i'}(\sigma)$ are current density components with and without stress based on a new transformed coordinate system, respectively.

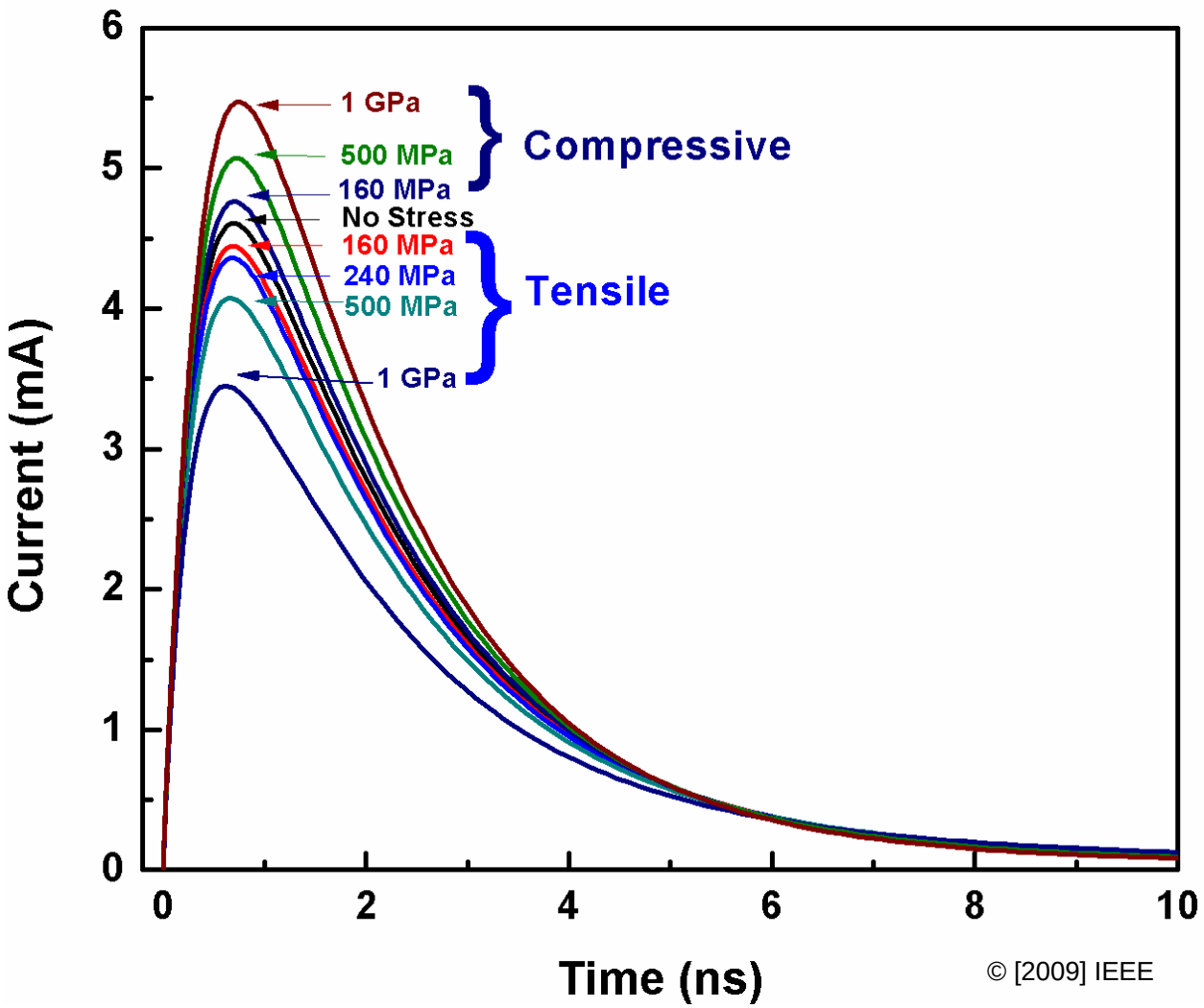


Figure 3-12. Simulated laser-induced current transients as a function of <110> uniaxial mechanical stress. [Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes. IEEE Transaction on Nuclear Science, , IEEE Trans. Nucl. Sci., vol. 56, pp. 3207, Figure 8, Dec. 2009]

The simulated current transients in Figure 3-13 show the same trend as the experimental data in Figure 3-4. I_{max} and Q in the simulations also agree with the experiments, as shown in Figure 3-13 and 3-14. The data points in the experiments are the average I_{max} and Q at each stress level. The error bars in the data points represent 95% confidence interval in the data at each stress level. The simulation results predict that I_{max} and Q under 1 GPa of tensile stress will decrease by ~23% and ~21%,

respectively. Analogous to tensile stress, 1 GPa of compressive stress increases I_{max} and Q by 17% and 13%, respectively. These experiment and simulation results for strained N+/P diodes show that uniaxial stress changes the shape of current transients and collected charges.

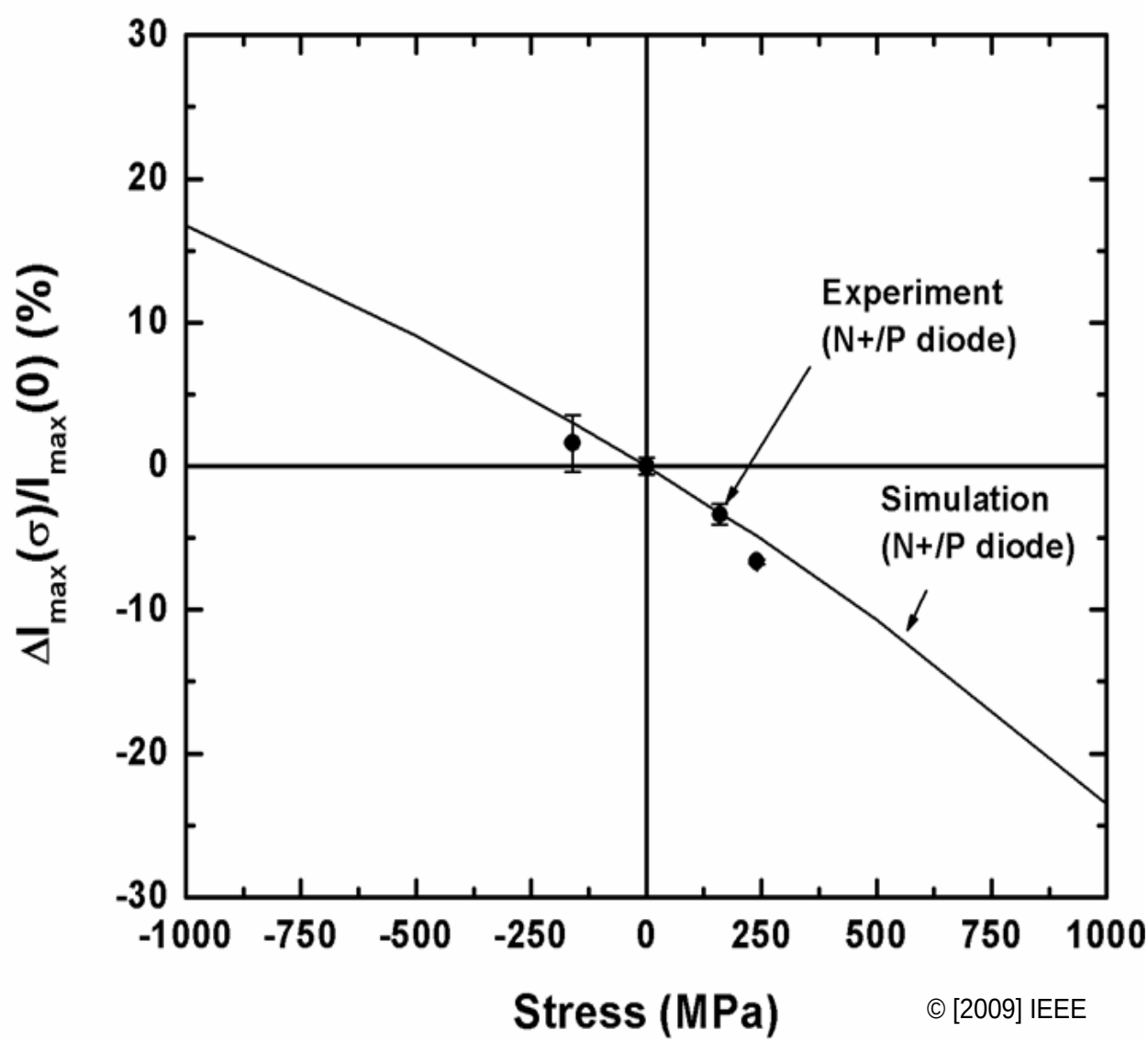


Figure 3-13. Peak current (I_{max}) in N+/P diodes as a function of mechanical stress. (positive (+) : tensile, negative (-): compressive). [Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes, IEEE Transaction on Nuclear Science, , IEEE Trans. Nucl. Sci., vol. 56, pp. 3203-3209, Dec. 2009]

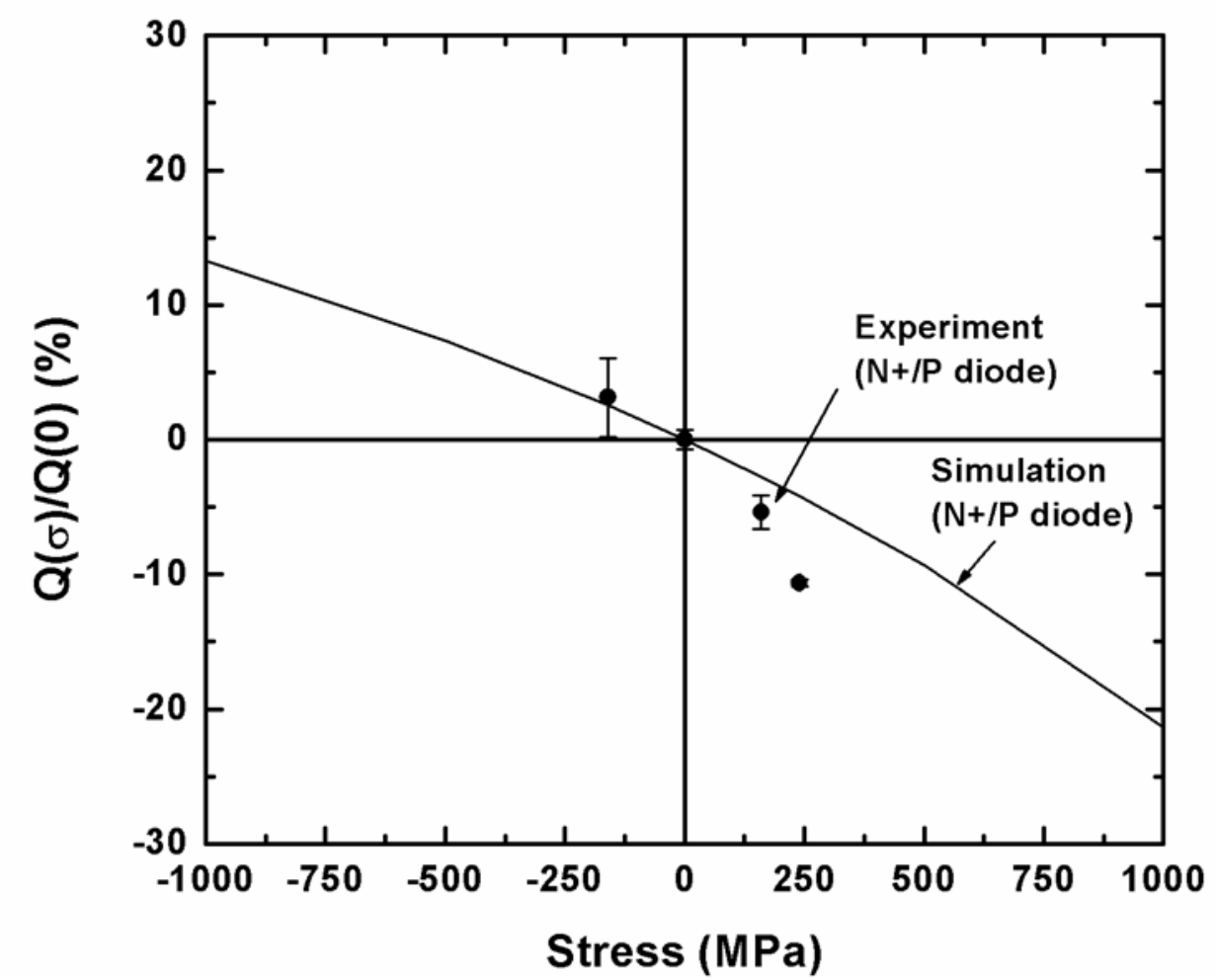


Figure 3-14. Collected charges in N+/P diodes (*Q*). (positive (+) : tensile, negative (-): compressive) [Reprinted, with permission, from H. Park, et al., Laser-Induced Current Transients in Strained-Si Diodes, IEEE Transaction on Nuclear Science, , IEEE Trans. Nucl. Sci., vol. 56, pp. 3203-3209, Dec. 2009]

3.5 Correlation between Transients in N+/P diode and nMOSFET

To apply the strain engineering concepts for mitigating SETs and SEUs in deep submicron MOSFETs, we need to understand the differences and similarities between these large diodes and deep submicron MOSFETs. The junction area of the large junction N+/P diodes used in the experiment is much larger than the diameter of the e-h pair cloud generated by pulse laser or ion strike. However, the size of source/drain junctions in submicron MOSFETs is expected to be comparable or smaller than that of a radiation-generated e-h pair cloud [117, 118]. While out-of-plane transport of generated

carriers dominates the current transients in large N+/P diodes, both out-of-plane and in-plane transport of radiation-generated carriers under mechanical stress should be considered for scaled MOSFETs. Therefore, it is very important to understand how current transients in submicron MOSFETs vary as a function of mechanical stress.

Based on the N+/P diodes analysis, it is concluded that the piezoresistive mobility model is useful to simulate current transients in devices as a function of uniaxial stress. FLOODS simulation in submicron nMOSFETs can predict the trend of peak current and collected charges as a function of uniaxial stress. Alpha particle-induced current transients in process-induced strained nMOSFETs was simulated using FLOODS by Cummings [116]. The size of junction in nMOSFET is 0.1 μm. The simulated peak current and collected charge trends in STI stressed nMOSFETs are similar to those measured in externally stressed N+/P diodes using the bending setup, as shown in Figure 3-15 and 3-16. With both STI induced stress and externally applied stress is present in the bulk of the nMOSFET as well as the surface [116, 119-121]. Similar to the N+/P diode case, Cummings suggested that the electron mobility change along the <001> direction is dominant factor for altering the shape of current transients in submicron nMOSFETs [116].

For logic devices in commercial off-the-shelf (COTs) chips, <110> uniaxial stress is applied to the channel of nMOSFETs using tensile SiN capping layers [15-17]. Carrier mobility along the channel (in-plane) direction is enhanced due to stress induced in the channel by the capping layers [15, 122, 123]. Unlike STI induced stress, the SiN capping layer-induced stress is only confined to the surface of Si [116, 119, 121]. Therefore, the simulated current transient in SiN capping layer-induced stressed

nMOSFETs done by Cummings shows no significant change compared to that in unstressed nMOSFET [116].

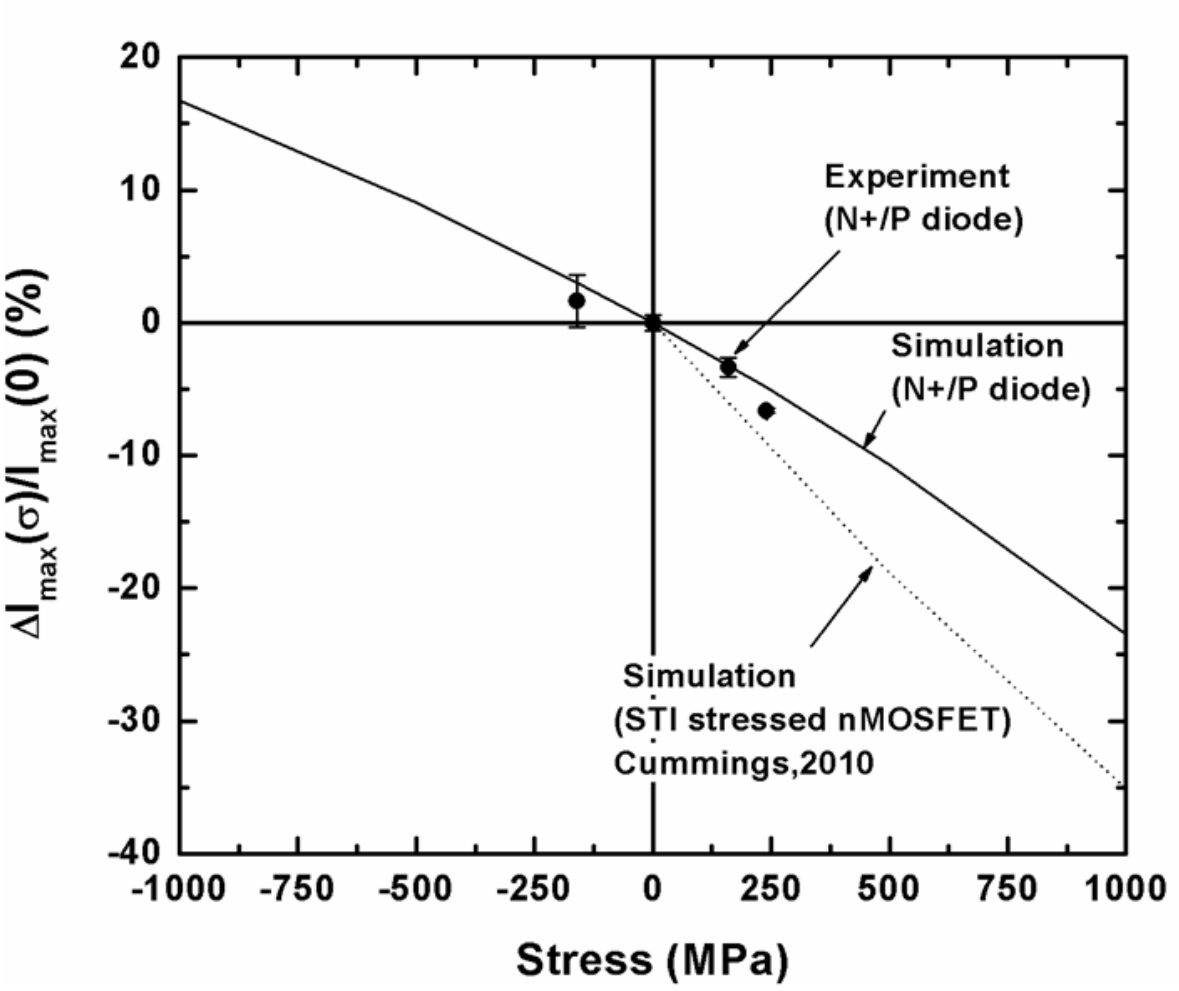


Figure 3-15. Peak current (I_{max}) in N+P diodes and nMOSFETs [116] as a function of mechanical stress. (positive (+) : tensile, negative (-): compressive)

Other process stressors such as the stress memorization technique (SMT) [17, 77, 124] and metal gate [21, 53] are emerging to apply stress to the channel in MOSFETs. Since the applied stress using these stressors is also confined to surface of Si [125], it is expected that there will be no significant change in current transients in SMT or metal gate-induced stressed MOSFETs. Since strained Si engineering shows the potential to control the shape of SETs or enhance the device performance without degrading the devices, further experiment and simulation work is required to evaluate the effects of the

process induced stress on the reliability of submicron MOSFETs under radiation environment.

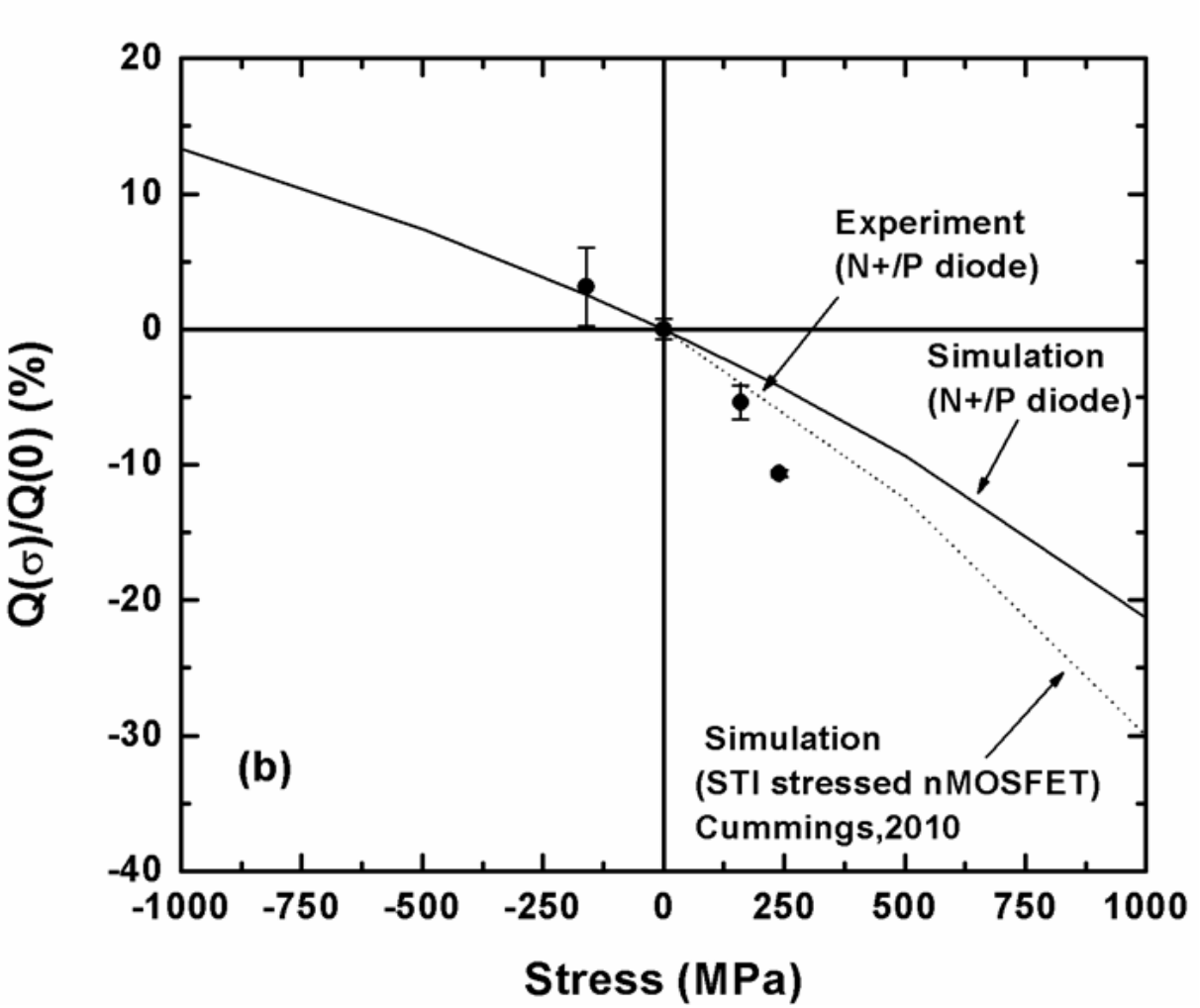


Figure 3-16. Collected charges (*Q*) in N+/P diodes and nMOSFETs [116]. (positive (+) : tensile, negative (-): compressive)

3.6 Conclusion

Uniaxial tensile stress in Si N+/P diodes decreases the maximum peak current and collected charge for laser-induced current transients. Quantitative analysis and FLOODS simulation results suggest that this can be attributed to the degradation of electron mobility along the <001> direction. Uniaxial compressive stress shows the opposite trend. The simulated peak current and collected charge trends in STI-induced

stressed nMOSFETs [116] agree with the experimental and simulated results in N+/P diodes. Therefore, uniaxial strain engineering has the potential to control the shape of single event transients and the amount of charges collected in deep submicron nMOSFETs. Furthermore, these results suggest that strained-Si technology will have a significant beneficial impact on SETs and SEUs at the circuit level.

CHAPTER 4
LASER-INDUCED CURRENT TRANSIENTS IN STRAINED-SI P+/N DIODES

4.1 Introduction

We studied the physics of laser-induced current transients in uniaxially stressed N+/P diodes in Chapter 3. It was understood that uniaxial stress can alter the shape of the current transient and change the amount of charge collected due to the change in electron mobility [126]. However, the effects of mechanical stress on current transients on P+/N diodes have not been reported. The effects of externally applied uniaxial stress on hole current transients in Si P+/N diodes is investigated in this chapter. The correlation between laser induced current transients in P+/N diode and alpha particle induced current transient in pMOSFETs is explained using FLOODS simulation, because the P+/N diode are representative of the source/drain junctions that are responsible for hole charge collection in p MOSFETs [116], as shown in Figure 4-1.

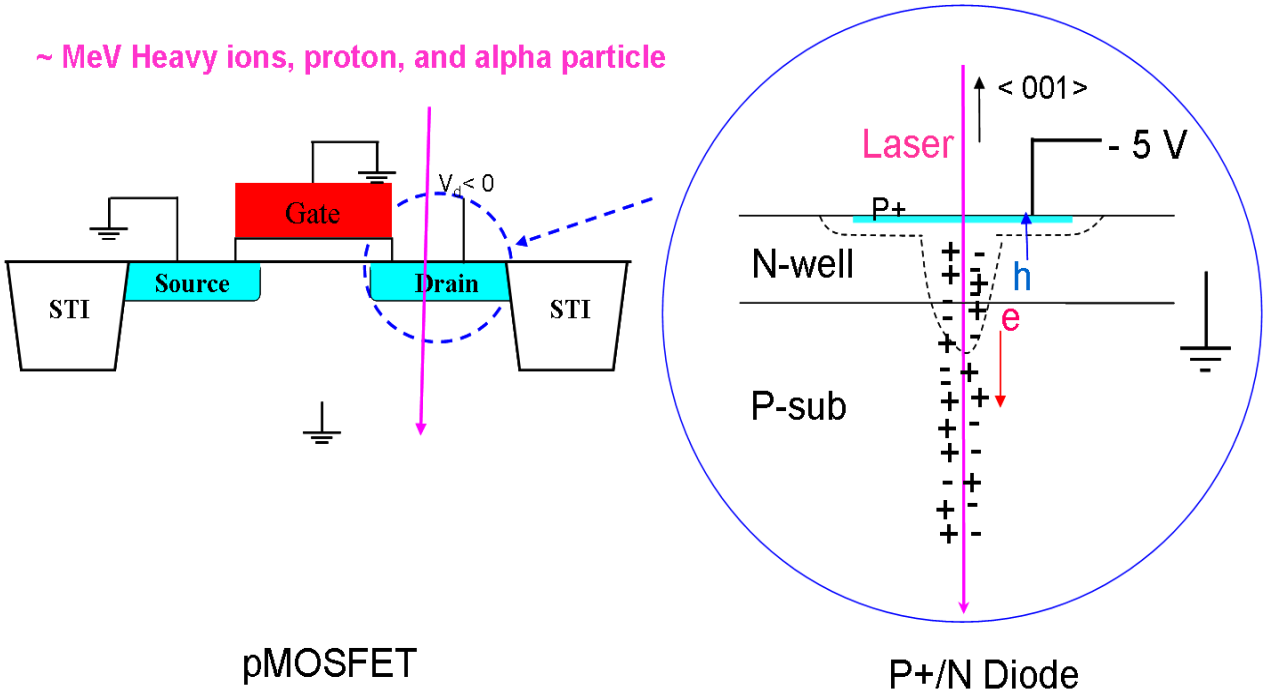


Figure 4-1. Motivation for measurement of P+/N diode.

4.2 Experimental Setup

Similar to the current transient measurement in N+/P diodes in Chapter 3, laser induced current transients in P+/N diodes are measured under controlled external mechanical stress, applied via a four-point bending setup [35]. The samples are irradiated using a picosecond pulsed laser [99, 100], as shown in Figure 4-2. A direct measurement system is built to characterize transients in P+/N diodes [101, 102]. The diode is connected to a ground-signal-ground (GSG) probe tip (DC to 40 GHz), a bias tee (10 kHz to 40 GHz), and a Tektronix TDS8200 digital sampling oscilloscope with 80E03 sampling module (20 GHz bandwidth). A cavity-dumped dye laser with a wavelength of 590 nm, pulse energy of 5.9 pJ, and pulsewidth of 1 ps is used to generate electron-hole pairs in the diode. The laser is focused to a spot size of 6.3 μm full-width-half-maximum diameter at zero degree incidence. Hole current transients on the P+/N diode are measured for stress values ranging from 70 MPa compressive to 220 MPa tensile under –5 V reverse bias.

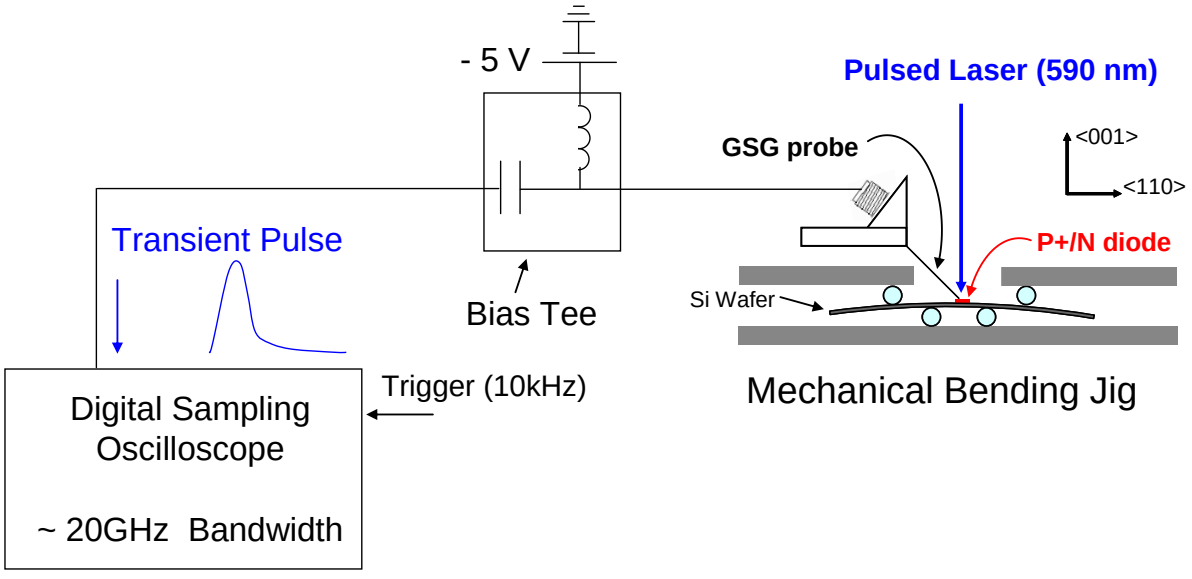


Figure 4-2. Laser-induced current transient measurement system in P+/N diode using a four-point bending setup.

The samples used in this study are P+/N diodes on a (001) Si wafer fabricated by a standard 130-nm CMOS technology similar to the N+/P case in Chapter 3. Large active area diodes (50 µm × 100 µm) are used for the experiment. The doping densities of the P+, N-well, and P-substrate are ~10^{20}, ~5X10^{17}, and ~10^{16} cm^{-3}, respectively [104]. The P+ and N-well depths are ~0.1 µm and ~2 µm. Transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDS) analyses show that nickel silicide (NiSi), silicon oxide (SiO_x), and copper (Cu) dummy patterns are present on the top of the diode, as shown in Figure 3-3. The thicknesses of the NiSi, SiO_x, and Cu layers are 20 nm, 720 nm, and 280 nm, respectively.

4.3 Experimental Results and Discussion

The effect of stress on the peak current and charge collection is characterized by monitoring laser-induced current transients in P+/N diodes for varying mechanical uniaxial stress values as shown in Figure 4-3. Tensile stress increases both peak current (I_{max}) and collected charge (Q) for the moderate range of stress considered in these experiments, as shown in Figure 4-7 and 4-8. However, compressive stress decreases Q *and* I_{max}. Q is obtained by integrating the measured current transient as a function of time. The normalized change in I_{max} as a function of uniaxial stress is observed to be larger than that in Q. The percent changes of I_{max} *and* Q are ~2.9 % and 0.9% at 100 MPa, respectively. Similar to previous results on the N+/P diode that showed a decrease (increase) in electron carrier mobility along the <001> direction and a decrease (increase) in peak current and collected charge [126], hole mobility along the <001> direction may be dominant factor for explaining the stress dependence of I_{max} *and* Q in P+/N diode.

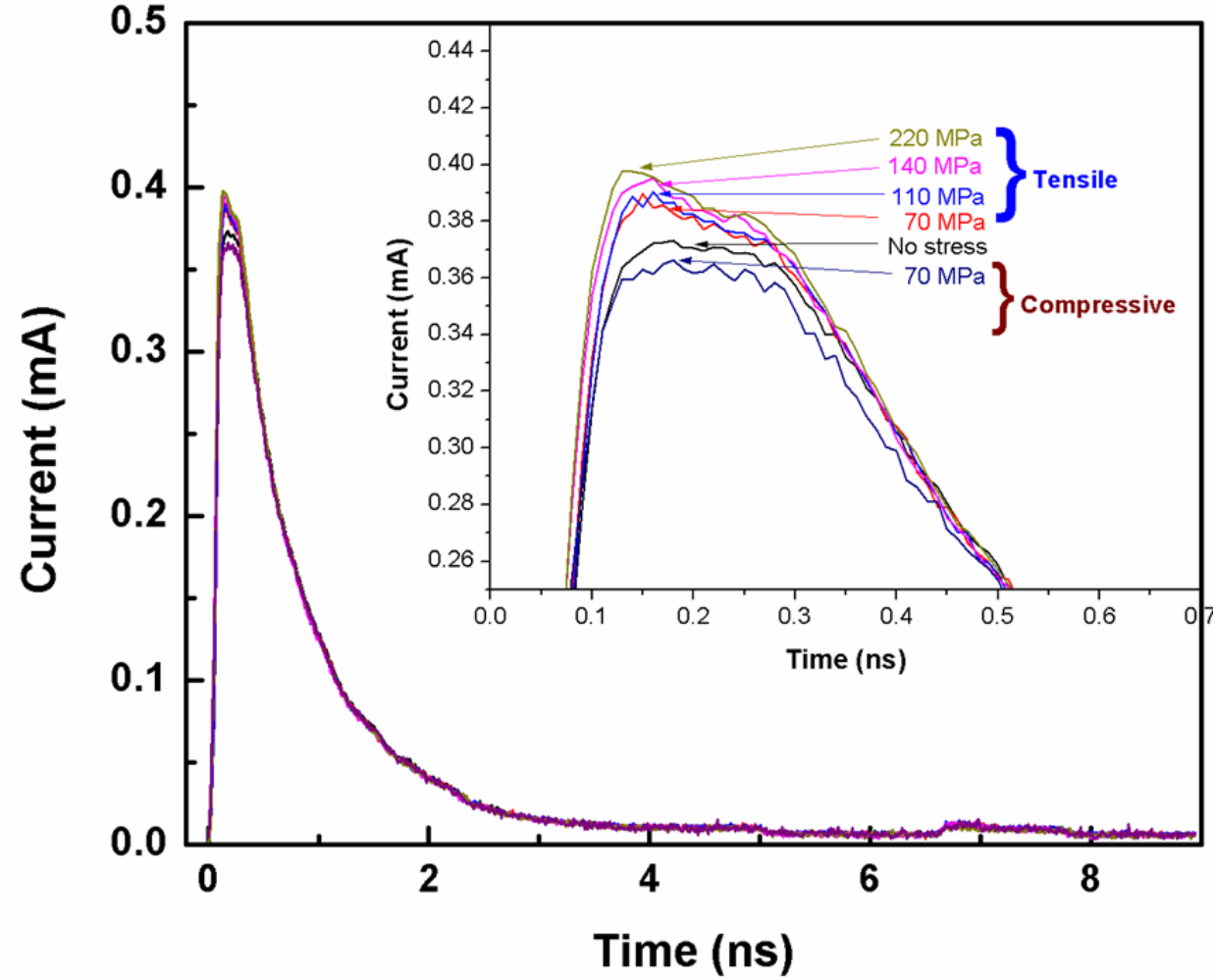


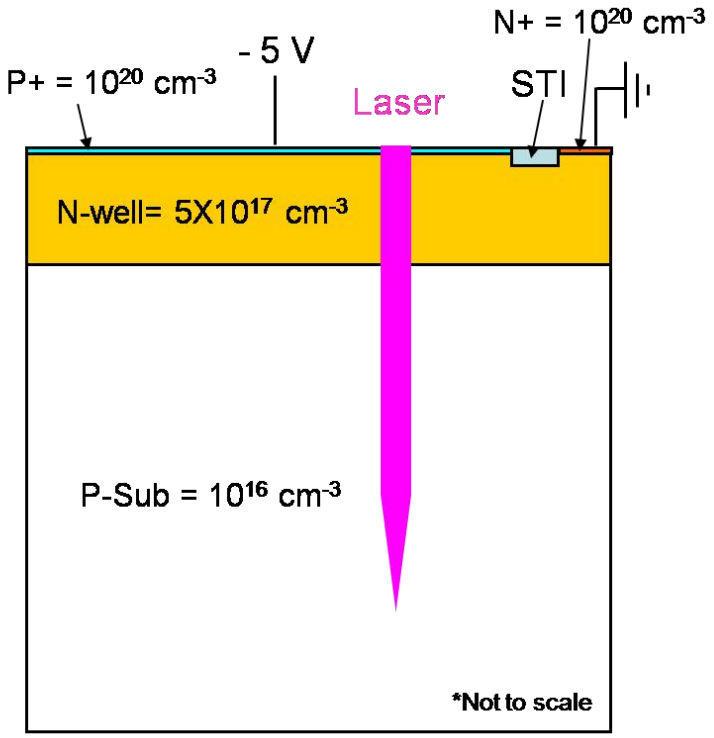
Figure 4-3. Laser-induced current transients in P+/N diode as a function of <110> uniaxial mechanical stress.

To understand the nature of the dominant mechanism for change I_{max} *and* Q in the P+/N diode as function of uniaxial stress, it is very important to understand the concept of piezoresistance (π) coefficients. The stress dependence of hole current transients can be analyzed using π-coefficients in Si [110, 111]. The π-coefficient represents the normalized change of mobility resulting from applied stress ($\pi_{coef} = -\Delta\mu / (\sigma\mu_o)$, where σ is the amount of applied stress, and μ_o is the mobility with no stress). The extracted change of hole mobility along the <001> direction ($\Delta\mu_{p\perp}$) from I_{max} and Q measured as a function of stress, as shown in Fig. 4-6 and 4-7, is ~ 2.9 % and ~ 0.9 % at 100 MPa,

respectively. However, based on previous results in Si done by Smith et al. [111], $\Delta\mu_{p\perp}$ due to uniaxial mechanical stress is expected to be only ~ 0.1% at 100 MPa [110, 111]. The extracted $\Delta\mu_{p\perp}$ from I_{max} (~2.9% at 100 MPa) is much larger than the calculated $\Delta\mu_{p\perp}$ from the π-coefficients (~ 0.1% at 100 MPa) [111]. Since the calculated $\Delta\mu_{p\perp}$ from the π-coefficients is much smaller than other $\Delta\mu$ from the π-coefficients, π-coefficients in other directions could be contributing to the observed larger peak current change in the experiment. The extracted $\Delta\mu_{p\perp}$ from Q in the experiment (~ 0.9% at 100 MPa) is within experimental error of the calculated $\Delta\mu_{p\perp}$ from the π-coefficients (~ 0.1% at 100 MPa) [111]. Since Q comes from integrating current transients as a function of time, it may represent the average change of hole mobility as a function of time. In a later section in this chapter discussing the correlation between P+/N diode and pMOSFETs, we will clarify which π-coefficient component dominates the peak current and collected charge in P+/N diode and pMOSFETs, respectively. We first present detailed FLOODS simulation results on uniaxially stressed P+/N diodes in the following section. These results are important for understanding some aspects of the correlation between P+/N diodes and pMOSFETs.

4.4 Simulation Results and Discussion

FLOODS is used to understand the primary contributing mechanisms in hole current transients in P+/N diodes and to predict how high stress (~ 1GPa) can affect I_{max} and Q. Similar to the previous N+/P diode simulation in Chapter 3, Shockley-Read-Hall and Auger band-to-band recombination models are used [113, 114]. A single photon absorption (SPA) equation [99, 100] for the photon energy (2.1eV) above Si band gap (1.1eV) is also considered to calculate the number and distribution of electron-hole pair generation. A unified mobility model developed by Cummings [127] considering



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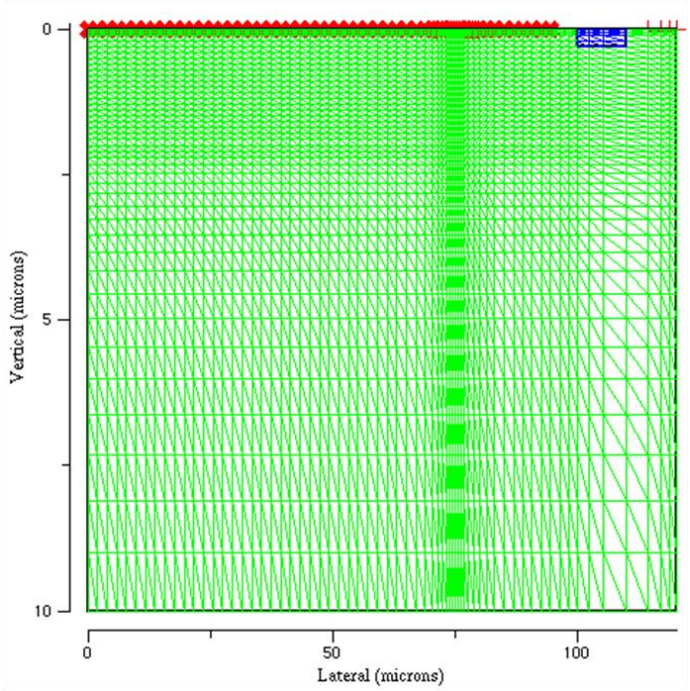


B

Figure 4-4. Details of two dimensional structure of 100µm junction size P+/N diode in FLOODS. A) simulation structure B) grid.

majority carrier mobility, minority carrier mobility, carrier-carrier scattering, and temperature dependence is used to simulate carrier transport in the high injection case. A piezoresistive mobility model based on Smith's π- coefficients [110, 111, 114] is used to simulate carrier mobility enhancement as a function of mechanical stress because N+/P diode results in Chapter 3 show that it is a useful model for simulating the effect of mechanical stress on current transients.

The two dimensional device structure and grid used for P+/N diode simulations in FLOODS are shown in Figure 4-4. The width and depth of the simulation structure are 120 μm and 10 μm, respectively. The P+ junction width is 100um. Shallow trench Isolation (STI) separates the P+ contact from the N-well contact to allow both contacts to be present on the top of the simulation structure. There is no intentional STI stress in the structure. N+ doping (10^{20} cm^{-3}) is implemented to reduce the contact resistance of the N-well. The applied bias of P+ and N+ are -5V and 0V, respectively.

Current transient simulations in the P+/N diode under no stress are performed to understand the dominant physics. The range of transmitted energy through the Cu metal pattern, SiO_x, and $NiSi_x$ layers is calculated to be ~ 0.32 to 0.7 pJ, considering the optical properties such as reflection, transmission, and absorption in each layer [99, 106]. The method for calculating the amount of laser energy reaching the active area of diodes was explained in Chapter 3. The simulated current transient with pulse energy of 0.65 pJ matches the experimental result, as shown in Figure 4-5. It is reasonable to use 0.65 pJ in the simulation because the value is within the calculated range of energy from ~ 0.32 to 0.7 pJ.

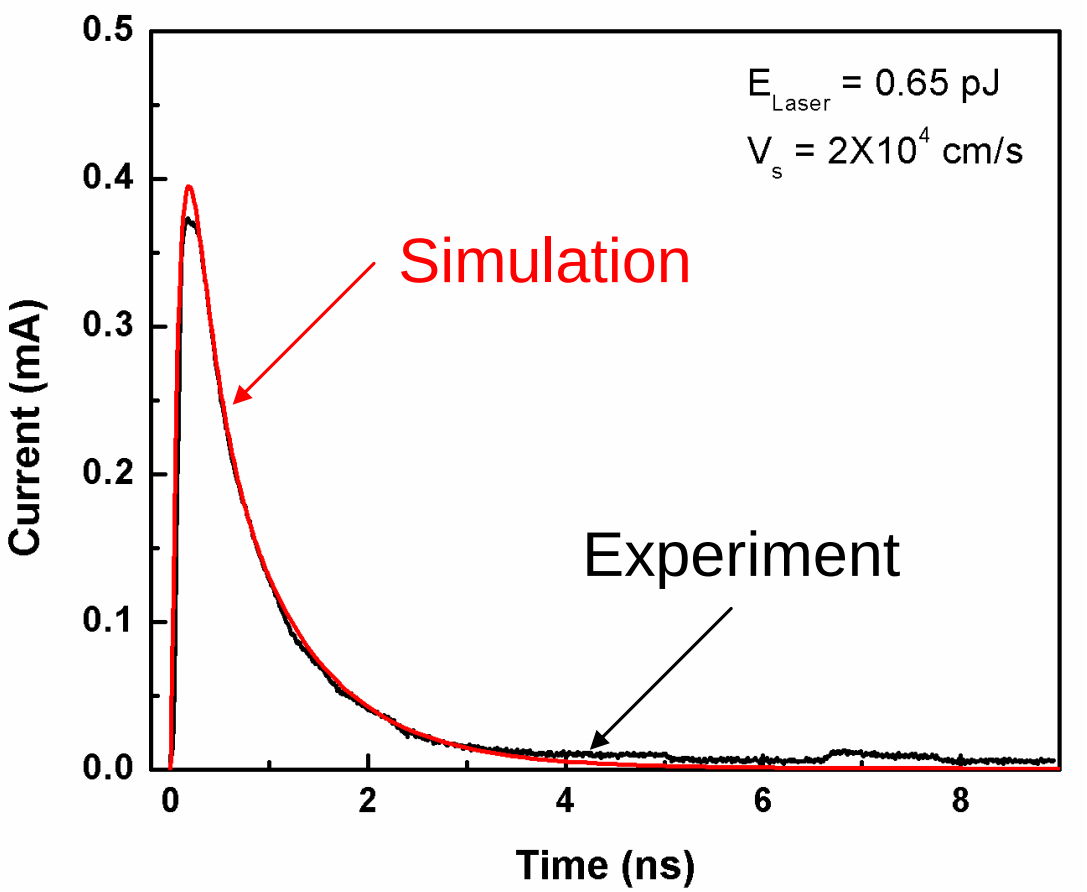


Figure 4-5. Comparison of experiment with simulation of current transients in P+/N diodes under no stress.

The simulated current transient in Figure 4-6 agrees with the experimental results in Figure 4-3. The extracted value of I_{max} and Q as a function of <110> uniaxial stress from the simulations (Figure 4-6) have comparable trends to those in the experiments as shown in Figure 4-7 and 4-8. The simulation results predict a decrease in I_{max} and Q under 1 GPa of compressive uniaxial stress of ~ 17% and ~1%, respectively. In the case of 1 GPa of tensile uniaxial stress, I_{max} and Q are expected to increase by ~ 12.5 % and 1.4%, respectively. The interesting point here is that the normalized change in I_{max} is 10 times larger than the normalized change in Q in the P+/N diode case. This is in stark contrast to the N+/P diode case where the normalized change in I_{max} and Q were comparable to each other. As briefly discussed in the experimental results, this

phenomenon in the P+/N diodes could arise from differences in electron and hole mobility in the <001> and <110> directions. Changes of hole mobility along the <110> direction or electron mobility along the <001> or <110> directions may affect the hole peak current due to very small change of hole mobility along the <001> direction (~1.1% at 1GPa of uniaxial stress). In the next section discussing the correlation between P+/N diodes and pMOSFETs, we investigate which of the three mobilities (hole mobility in <110>, electron mobility in <110> and electron mobility in <001>) could be the dominant factor for determining the normalized change in I_{max} and Q in the P+/N diode.

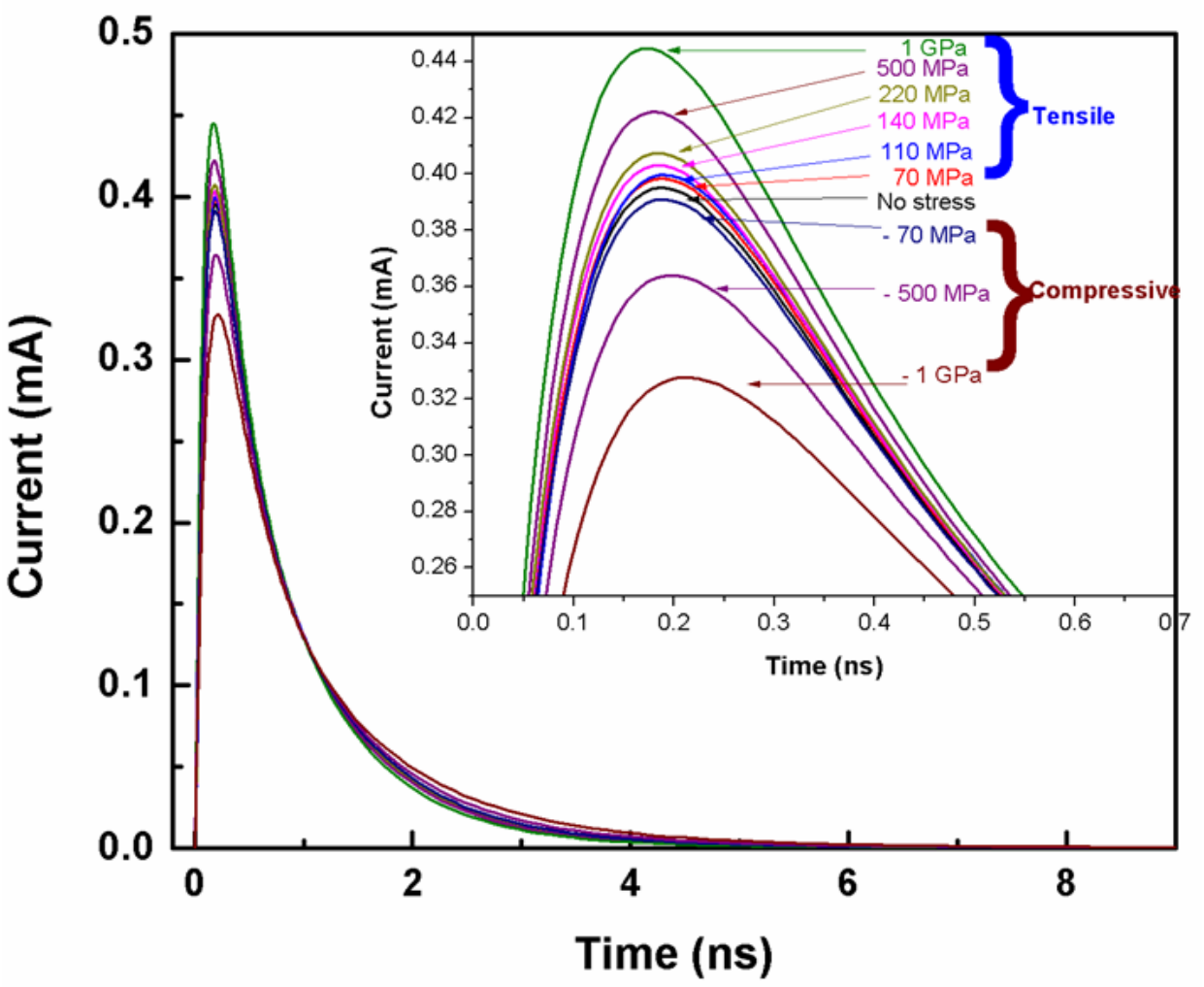


Figure 4-6. Simulated laser-induced current transients in P+/N diode as a function of <110> uniaxial mechanical stress.

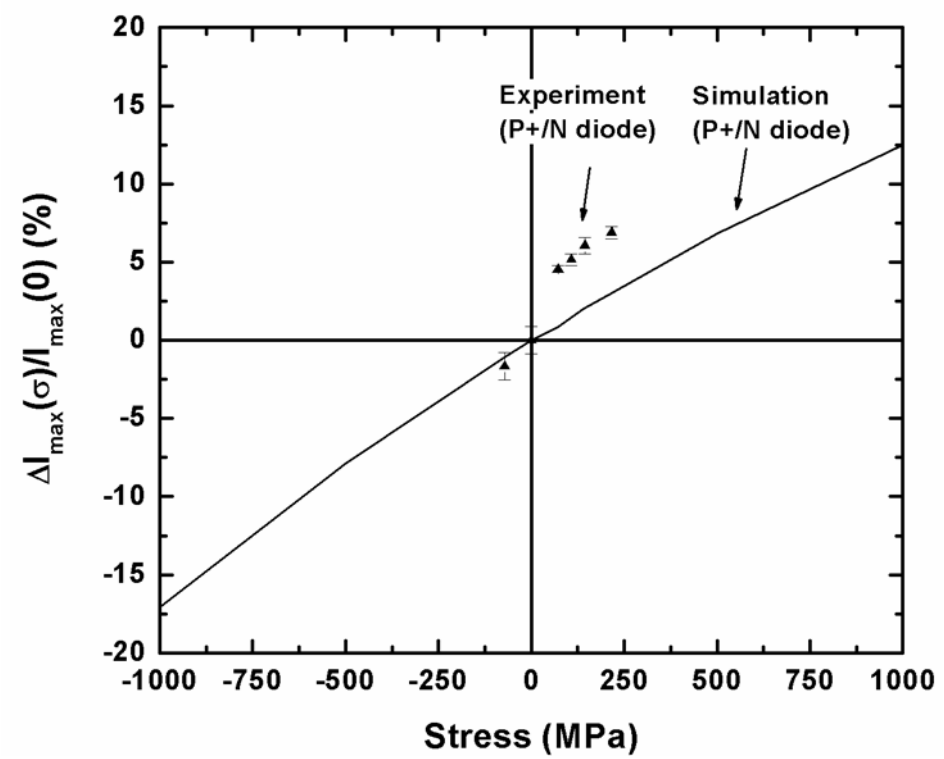


Figure 4-7. Change in peak current (I_{max}) in P+/N diode as a function of <110> uniaxial stress. (positive (+): tensile, negative (-) : compressive)

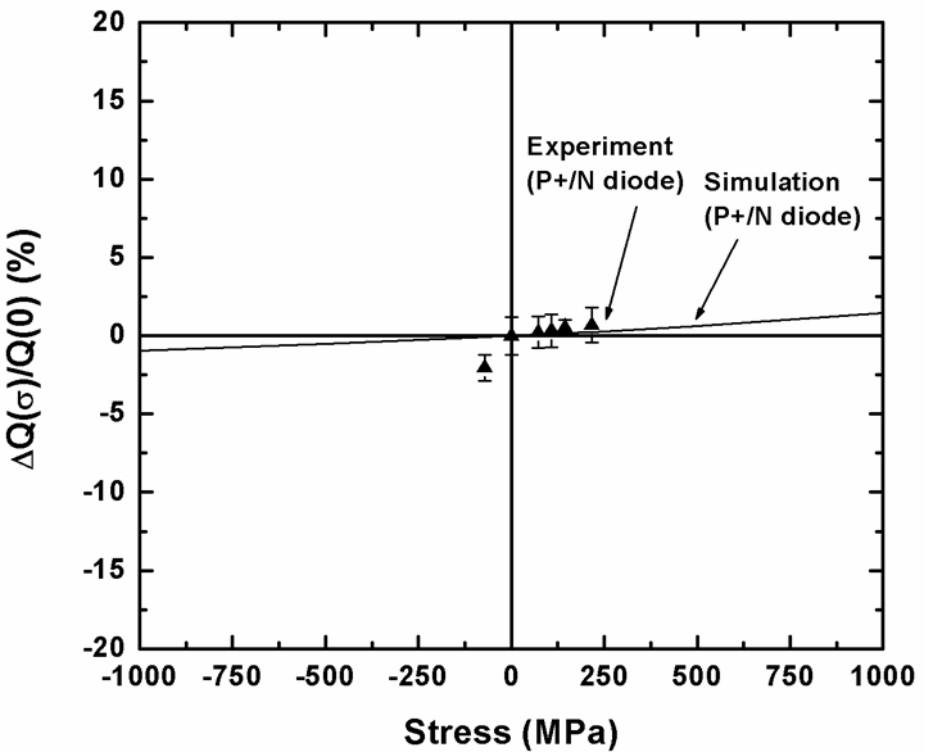
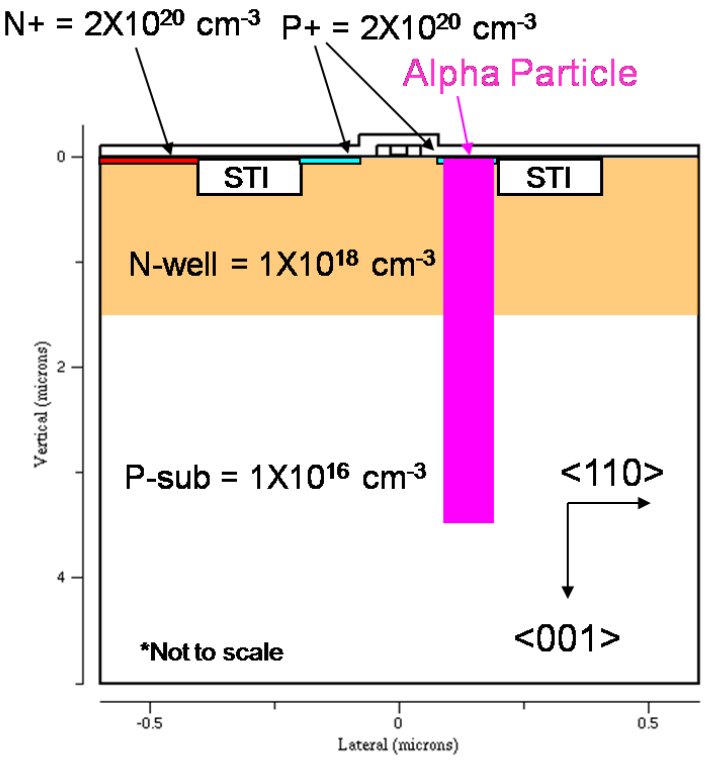


Figure 4-8. Change in collected charge (Q) in P+/N diode as a function of <110> uniaxial stress. (positive (+): tensile, negative (-) : compressive)

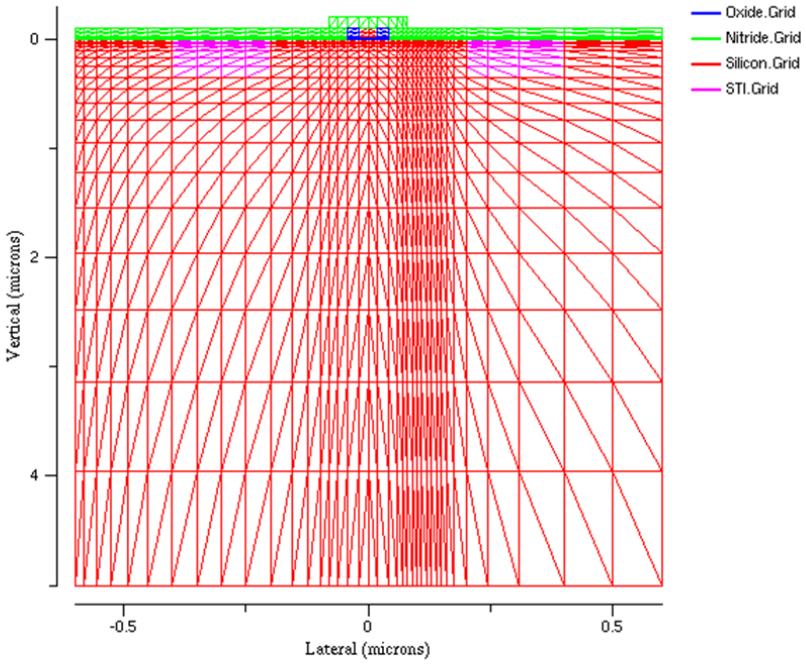
4.5 Correlation between Transients in P+/N diode with pMOSFET

To provide physical insight into the impact of uniaxial strain engineering on single event transients (SETs) in deep submicron pMOSFETs, simulation results of alpha particle-induced transients in pMOSFETs with process-induced strain are compared with those of laser induced transients in P+/N diodes. Previous simulation results by Cummings [116] on alpha particle induced current transient in uniaxial compressive stressed pMOSFETs (by SiN capping layer and SiGe epitaxial growth) show that there is no significant difference of hole peak current and collected charge between the unstressed and stressed cases. Stress from the SiN capping layer and SiGe epitaxial growth is confined near the Si surface [116, 119, 121]. Therefore, he suggested that there is negligible impact on the transient shape and amount of collected charge due to stress. However, he also suggested that shallow trench isolation (STI) extending deep into the bulk Si [116, 119, 121] similar to wafer bending (or global stress) can change the peak current and collected charge in MOSFETs.

While simulation results of alpha particle induced transients in STI stressed nMOSFETs has been reported [116], the effects of uniaxial stress on SETs in STI stressed pMOSFET have not been investigated yet. In this section, simulation results on alpha particle induced transients in STI stressed submicron pMOSFETs are presented. The two dimensional device structure and grid used for pMOSFET simulations in FLOODS are shown in Figure 4-9. The physical gate length of pMOSFETs used in the FLOODS simulation is ~ 35 nm [116, 128]. The width and depth of the simulation structure are 0.6 μm and 5 μm, respectively. The P+ junction width is 0.1um. Shallow trench Isolation (STI) separates the P+ contact from the N-well contact to allow both contacts on the top of the simulation structure. N+ doping ($2X10^{20}$ cm^{-3}) is



A



B

Figure 4-9. Details of two dimenisional structure of 0.1μm junction size pMOSFET used in FLOODS. A) device details B) grid

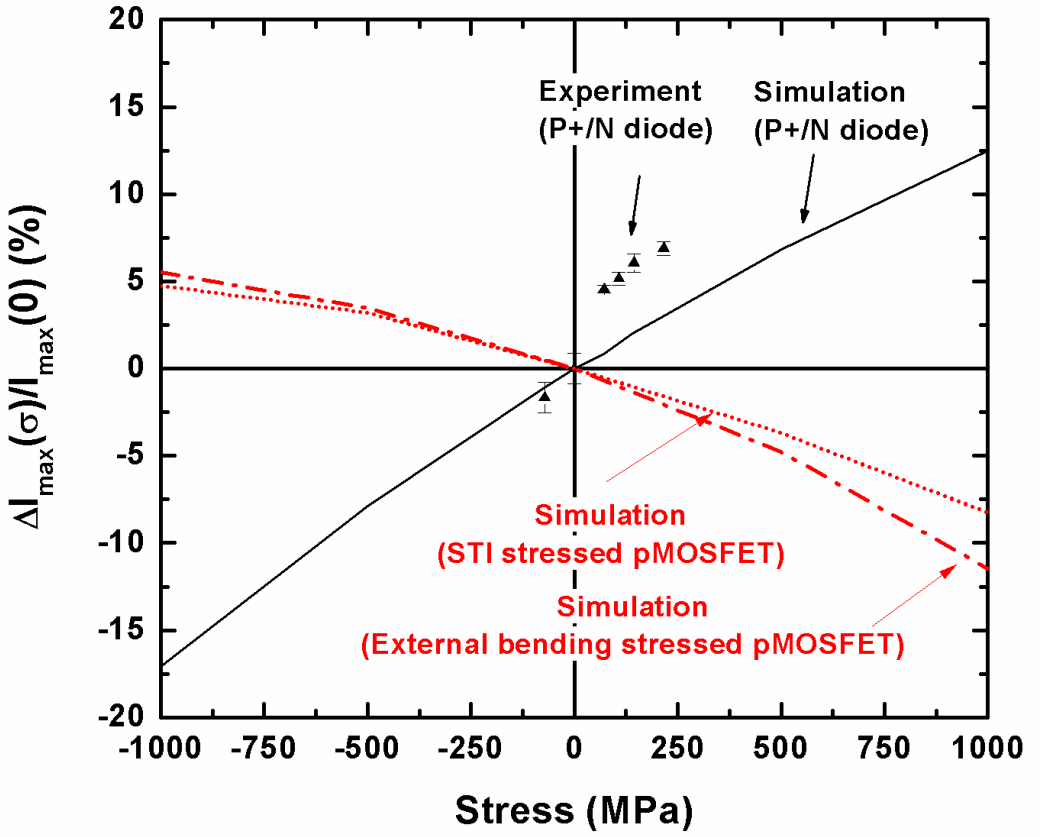


Figure 4-10. Change in peak current (I_{max}) in pMOSFETs and P+/N diode as a function of <110> uniaxial stress. (positive (+): tensile, negative (-) : compressive)

implemented to reduce the contact resistance of the N-well. The doping densities of the P+, N-well, and p-substrate are $2X10^{20}$, 10^{18}, and ~10^{16} cm^{-3}, respectively. The applied drain bias in pMOSFET is -1V. Gate, source, and body in the device are grounded.

Florida Object Oriented Process Simulator (FLOOPS) simulation tool [103] is used to create uniaxial stress using STI along the <110> channel direction. Similar to the diode experiments, a piezoresistive mobility model based on Smith's π-coefficients [110, 111] is used to simulate mobility enhancement under mechanical stress. To induce the current transient, a 1 MeV alpha particle strike on the drain of the pMOSFET is considered so as to represent the worst case scenario [116]. The 1/e radius of the alpha particle is 50 nm [129]. The electron-hole pair distribution is assumed to be Gaussian [114, 129].

We previously observed similar trend between transients in N+/P diodes and nMOSFETs in Chapter 3. However, the simulated peak current results in STI stressed pMOSFETs are opposite to the experiment and simulated results in external bending stressed P+/N diode as shown in Figure 4-10. We systematically investigate the following factors to identify the dominant contributor to the observed difference between P+/N and pMOSFETs:

1. Method of stress introduction (external bending stress vs STI)
2. Differences in simulation conditions – (a) bias (b) radiation source and (c) junction size

We simulate alpha particle-induced transients in external bending stressed pMOSFETs and compare the simulation results to those of STI induced stress in Figure 4-10. It was observed that the simulated peak current trend in external bending stressed pMOSFETs is opposite to those in external bending stressed P+/N diodes. However, the simulated peak current trend in external bending stressed pMOSFETs are comparable to those in STI induced stressed pMOSFET. Since STI induced stress extending deep into the bulk Si [116, 119, 121] is similar to that applied via wafer bending, the comparable simulated results of peak and collected charge trends in external bending and STI-induced stressed pMOSFET are reasonable.

Next, we study the effect of differing bias conditions (-5V in P+/N diode and -1V in pMOSFETs), differing radiation source (laser in P+/N diode and alpha particle in pMOSFETs), and differing junction size (100 μm in P+/N diode and 0.1 μm in pMOSFET). Simulation results show that the peak current trend is independent of radiation source and bias condition. However, junction size differences play an important role, as shown in Figure 4-11.

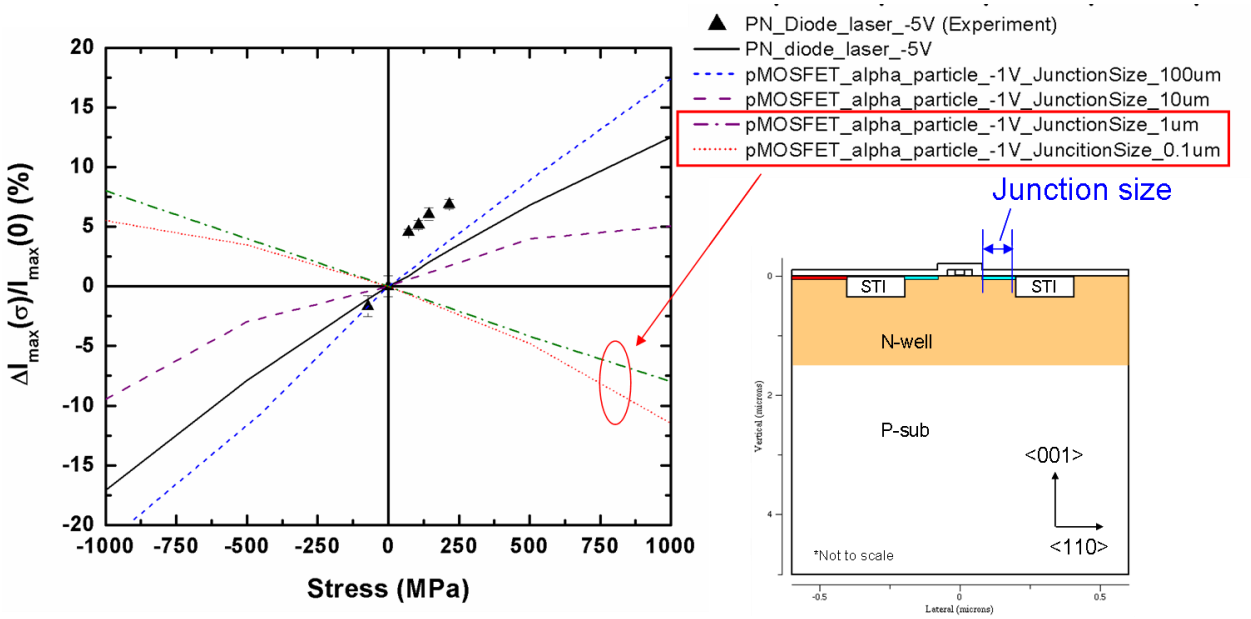


Figure 4-11. Change in peak current (I_{max}) in P+/N diode with <110> uniaxial stress and pMOSFETs under <110> uniaxial stress with different junction size. (positive (+): tensile, negative (-) : compressive)

As junction size in pMOSFETs decreases from 100 µm to 0.1 µm, it is observed that the peak current trend in pMOSFETs as function of stress is changed, as shown in Figure 4-11. The peak current trend in large junction size pMOSFETs such as 100 µm and 10 µm is similar to those in 100 µm junction P+/N diodes qualitatively. However, the peak current trend in small junction size in pMOSFETs such as 1 µm and 0.1 µm is opposite to those in 100 µm junction P+/N diode. Since the junction size in the submicron pMOSFETs simulation structure is ~ 0.1 µm, the simulated peak current trend in pMOSFETs is opposite to those in 100 µm junction P+/N diode. Based on these simulation results in Figure 4-11, it is concluded that there is a correlation between the peak current trend and the junction size. The differences in the junction size lead to differences in charge transport /collection mechanisms between the P+/N diodes and pMOSFET cases. Keeping in mind that the junction sizes in today's MOSFETs are about 0.1 um or smaller, it becomes quite important to understand the differences in

transport/collection effects between large junction (100 μm) P+/N diode and small junction (0.1 μm) pMOSFET. The physics of the differing charge transport/collection mechanisms could be understood by looking at the π-coefficients involved in these two structures.

To evaluate which π-coefficient component dominates the normalized change of peak current in 0.1 μm junction pMOSFET and 100 μm junction P+/N diode respectively, multiple simulations, each considering only one single π-coefficient are performed using a 3X3 piezoresistive matrix as described in Chapter 3. For convenience, we revisit the peizoresistive matrix equation described earlier:

$$\begin{bmatrix} \pi'_{11} & \pi'_{13} & 0 \\ \pi'_{13} & \pi'_{33} & 0 \\ 0 & 0 & \pi'_{44} \end{bmatrix} \begin{bmatrix} \sigma'_{11} \\ \sigma'_{33} \\ \sigma'_{13} \end{bmatrix} = \begin{bmatrix} -\Delta\mu'_{11}/\mu'_{11} \\ -\Delta\mu'_{33}/\mu'_{33} \\ -\Delta\mu'_{13}/\mu'_{13} \end{bmatrix} \tag{5-1}$$

where π'_{ij}, σ'_{ij}, ρ'_{ij}, and μ'_{ij} are components of the piezoresistance coefficient, mechanical stress, resistivity, and carrier mobility, respectively, and $\Delta\mu'_{ij}/\mu'_{ij}$ are fractional changes in and mobility in the transformed coordinate system, as shown in Figure 3-11.

For example, the 2-D piezoresistance matrix only considering π'_{11} of hole under uniaxial stress along the <110> direction is expressed as

$$\begin{bmatrix} \pi'_{11,h} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \sigma'_{11} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \pi'_{11}\sigma'_{11} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} -\Delta\mu'_{11,h}/\mu'_{11,h} \\ -\Delta\mu'_{33,h}/\mu'_{33,h} \\ -\Delta\mu'_{13,h}/\mu'_{13,h} \end{bmatrix} \tag{5-2}$$

where $\pi'_{11,h}$, σ'_{11}, and $\mu'_{ij,h}$ are components of the piezoresistance coefficient, mechanical stress, and hole carrier mobility, and $\Delta\mu'_{ij,h}/\mu'_{ij,h}$ are fractional changes in hole mobility in the transformed coordinate system, respectively, as shown in Figure 3-11.

Separate FLOODS simulations considering π'_{11} and π'_{13} individually for electrons and holes are performed, as shown in Figure 4-12 and 4-13. The peak current trend in external bending stressed 0.1 μm junction pMOSFETs is similar to those considering only π'_{11} of hole, as shown in Figure 4-12. The peak current trend in external bending stressed 100 μm junction P+/N diode agrees with those considering only π'_{11} of electron, as shown in Figure 4-13. These results provide insight about the different dominant π-coefficients that alter the peak current trend in small 0.1μm junction pMOSFET and large 100 μm junction P+/N diode cases due to the very small change in hole mobility along the <001> direction (~1.1 % at 1GPa of uniaxial stress).

Hole concentration contour plots at peak current conditions (Figure 4-14 and Figure 4-15) are used to visualize how π'_{11} of hole and electron could dominate peak current in small 0.1 μm junction pMOSFETs and 100 μm junction P+/N diode, respectively. Since the hole concentration contour spreads and becomes larger than the junction size, it is highly possible that holes need to travel along the <110> direction in order to be collected at the P+ junction as shown in Figure 4-14 for 0.1μm junction pMOSFETs. Therefore, π'_{11} of hole (the change in hole mobility along the <110> direction) dominates peak current trend in 0.1 μm junction pMOSFETs as a function of mechanical stress.

In contrast to the 0.1μm junction pMOSFETs, holes in the 100 μm junction pMOSFET are confined to large P+ junction. Thus, these holes do not have to travel along the horizontal <110> direction to be collected in P+ junction. The phenomenon is expected to be similar to that of large 100 μm junction P+/N diode shown in Figure 4-15. Therefore, as shown in Figure 4-11, the simulated peak current trend in 100 μm junction

pMOSFET as a function of <100> uniaxial stress is observed to be similar to the peak current trend in 100 μm junction P+/N diode.

Using the π-coefficient simulation results on 100 μm junction P+/N diode (Figure 4-13), we can understand why the peak current in large junction size device such as 100 μm junction pMOSFET and P+/N diode can be affected by π'_{11} of electron (the change in electron mobility along the <110> direction). The interesting point in the 100 μm junction P+/N diode case is that the π'_{11} of electron dominates the change in peak current as a function of stress, even if the amount of electron collected in P+ junction is less than 0.001% of peak current.

To understand why π'_{11} of electron dominates the hole peak current in the P+/N, we should understand how current transient simulations are performed in FLOODS, using the quasi-Fermi method [130-132]. The method involves self-consistently solving for three quantities – device potential (bulk and surface), quasi-Fermi potential of hole, and quasi-Fermi potential of electron – using Poisson equation and electron/hole current continuity equations. A change in electron mobility (with stress) in the current continuity equations can affect both the hole quasi-Fermi potential and the device potential. As a result, the hole concentration and the gradient of the hole quasi-Fermi potential are also affected, both of which control the hole peak current. Thus the electron mobility change (with stress) is self-consistently fed back into the hole current through the Poisson equation. This feedback mechanism is most likely to be responsible for the change in the peak (hole) current in the P+/N diode when uniaxial stress is present in the device.

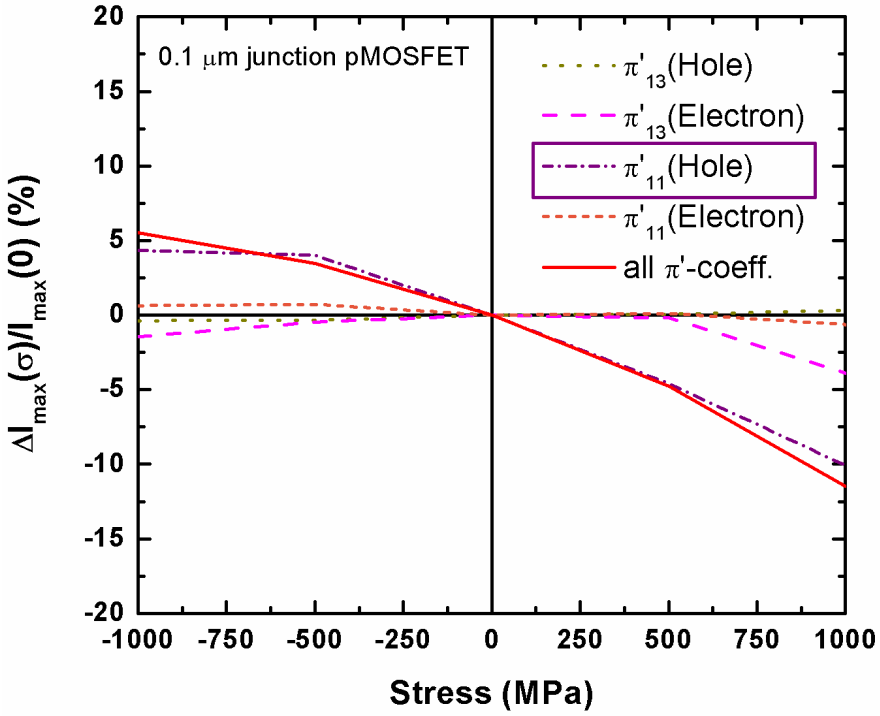


Figure 4-12. Change in peak current (I_{max}) in 0.1 μm junction pMOSFETs with each π-coefficient component as a function of <110> uniaxial stress. (positive (+): tensile, negative (-) : compressive)

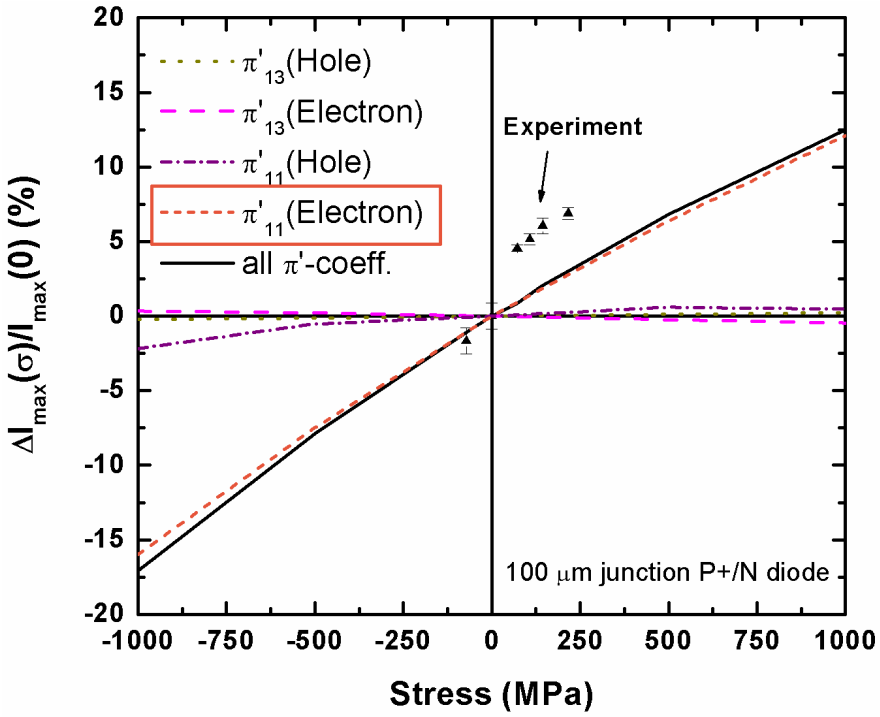


Figure 4-13. Change in peak current (I_{max}) in 100 μm junction P+/N diode with each π-coefficient component as a function of <110> uniaxial stress. (positive (+): tensile, negative (-): compressive)

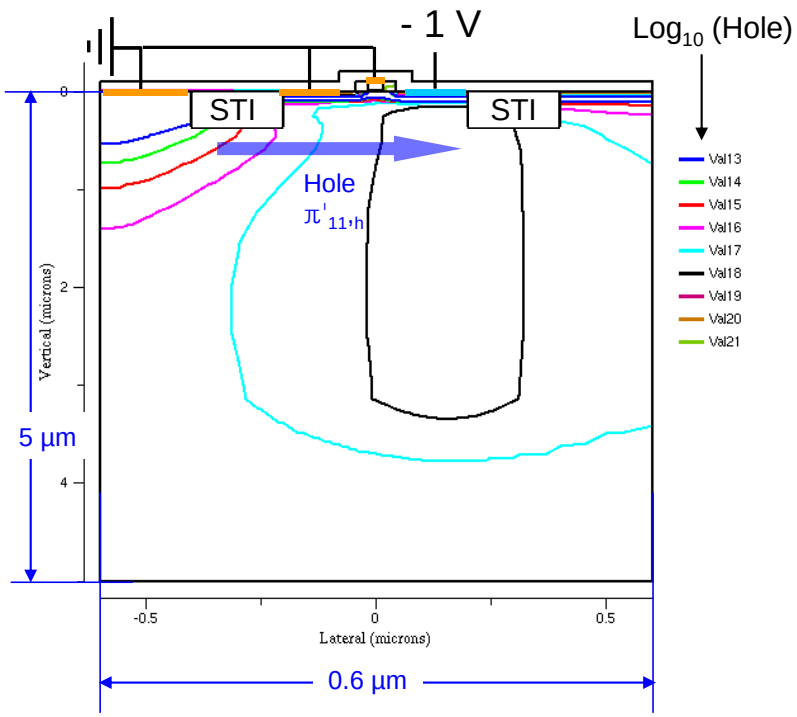


Figure 4-14. Hole concentration contour at peak current in unstressed 0.1 µm junction pMOSFET.

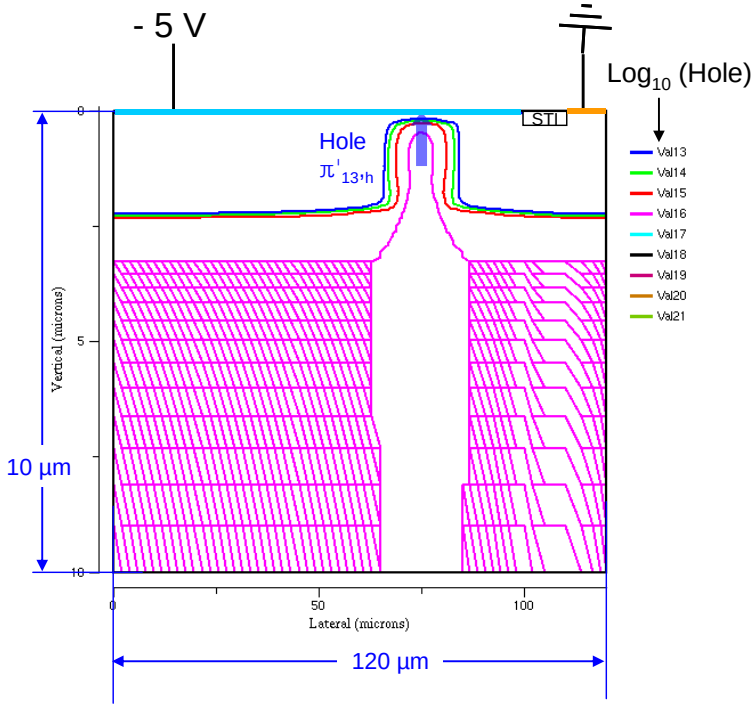


Figure 4-15. Hole concentration contour at peak current in unstressed 100 µm P+/N diode.

Overall, due to very small change in hole mobility along the <001> direction (~1.1 % at 1GPa of uniaxial stress), different π-coefficients produce the opposite peak current trend between 100 μm junction P+/N diodes and 0.1μm junction pMOSEFETs. However, in Chapter 3, the same peak current trend in the case of 100 μm junction N+/P diodes and 0.1μm junction nMOSFETs cases was observed. It is due to large change in electron mobility along the <001> direction (~53.4 % at 1 GPa of uniaxial stress), which dominates peak current in 100 μm junction N+/P diodes and 0.1μm junction nMOSFETs.

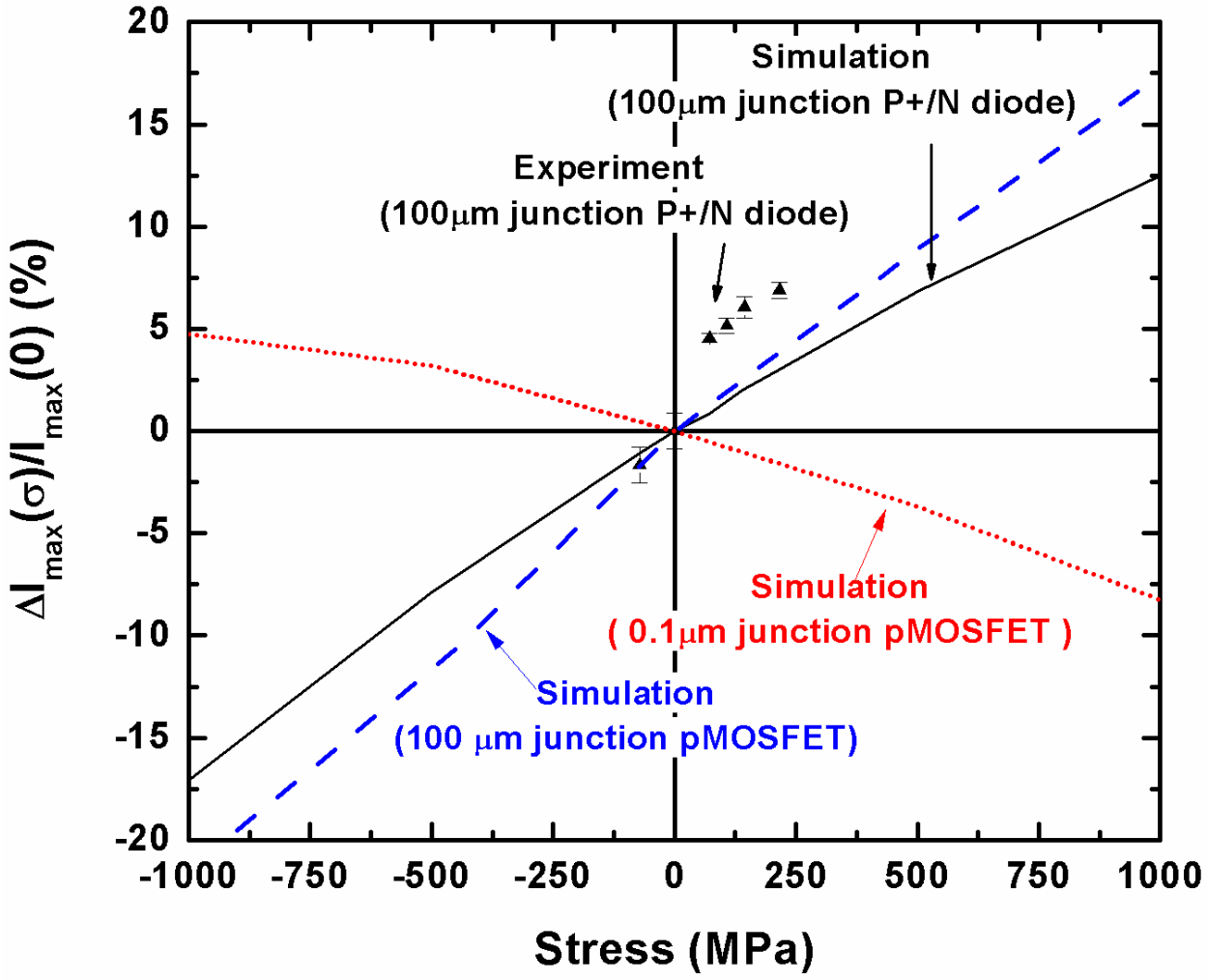


Figure 4-16. Change in peak current (I_{max}) in P+/N diode and pMOSFETs as a function of <110> uniaxial stress. (positive (+): tensile, negative (-) : compressive)

FLOODS simulations predict that the simulated peak current and collected charge trend in 100 um junction pMOSFETs is similar to those in 100 um P+/N diode.(Figure 4-16 and 4-17). It is also seen from simulations that a decrease in peak current and collected charge in 0.1 μm junction pMOSFETs would be observed with increasing STI induced tensile stress, as shown in Figure 4-16 and 4-17. It has been reported [116] that an increase in STI induced tensile stress also results in a decrease in peak current and collected charge in small 0.1 μm junction nMOSFETs. Since junction size in deep submicron MOSFETs is equivalent to or less than 0.1 μm, tensile STI stress along the <110> direction is expected to be beneficial for decreasing the peak current and collected charge in both deep submicron n- and pMOSFETs.

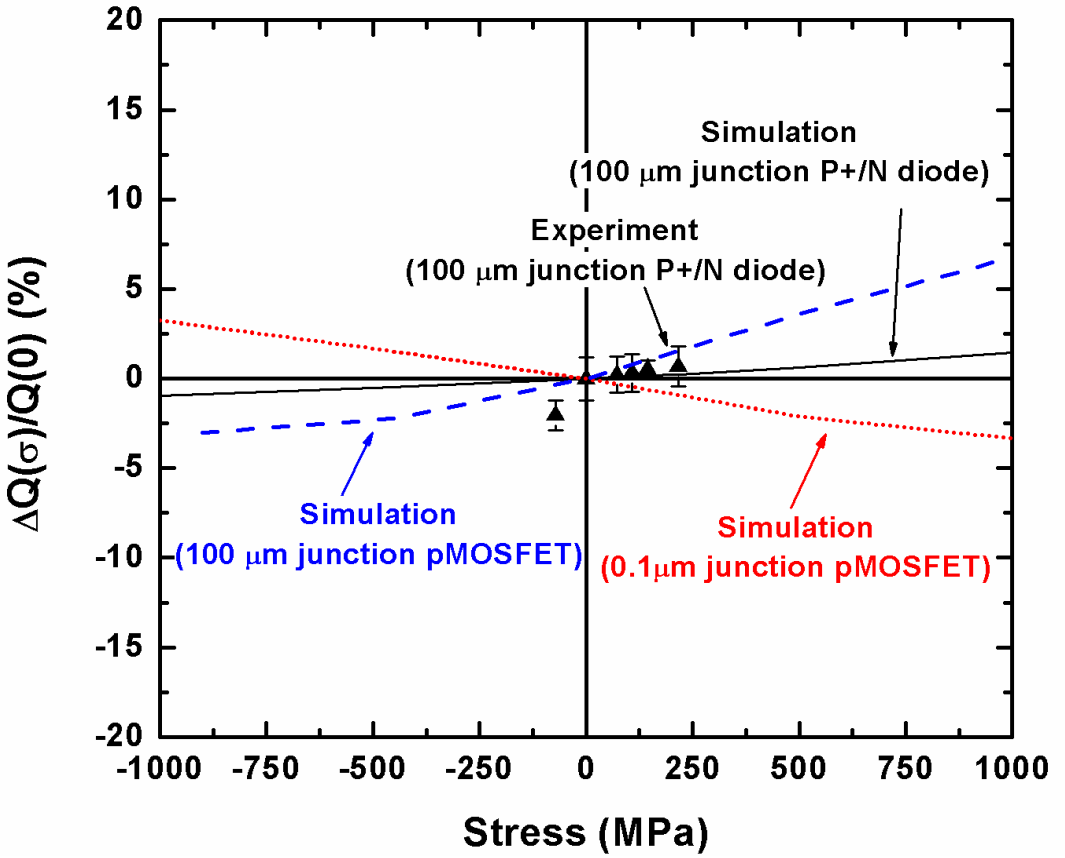


Figure 4-17. Change in collected charge (*Q*) in P+/N diode and pMOSFETs as a function of <110> uniaxial stress. (positive (+): tensile, negative (-) : compressive)

Simulation results of current transients in STI stressed n- and pMOSFETs and other process stressed n- and pMOSFETs (SiN capping layer and epitaxial growth) [116] provide insight about how strain engineering can impact drive current enhancement and single event transient (SET) response. Fortunately, in nMOSFETs, incorporating tensile SiN capping layer- and STI-induced stress is expected to increase drive current (mobility) enhancement and decrease peak current and collected charge simultaneously [116, 133, 134]. However, we should carefully engineer surface and bulk stress to optimize drive current enhancement and SET response (peak current and collected charge) in pMOSFETs.

Compressive stress enhances drive current in pMOSFET [15, 17, 18, 38], but tensile stress decreases peak current and collected charge. Compressive SiN capping and SiG epitaxial layer introduce stress that is confined to surface of pMOSFET [116, 119, 121]. Since the drive current enhancement is related to surface stress engineering, these two stressors improve drive current without adversely impacting SET response [116]. Tensile STI stress decreases peak current and collected charge in pMOSFET, because it can extend deeper into bulk of the device. When tensile STI stress is present simultaneously with compressive SiN capping layer/SiGe epitaxial layers, the tensile nature of STI stress somewhat compensates the compressive stress in the surface of the device induced by SiN capping layer and SiGe epitaxial layer.

Typically, compressive stress induced by SiN capping layers and SiGe epitaxial growth (~2.4 GPa) [76, 77] is larger than the tensile stress introduced by STI (~1GPa) in the surface of the device [116]. Therefore, some amount of compressive stress would be still present in the surface even after compensation. This compressive stress will

enhance the drive current (through hole mobility improvement). Since the bulk of the device is under tensile stress from the STI, the SET response is also improved simultaneously. Thus, by choosing a proper combination of stress levels, it is possible not to degrade device performance while having all three stressors (compressive SiN capping, compressive SiGe epitaxial layer, and tensile STI) concurrently. From a design perspective, a trade off between drive current enhancement and SET response from uniaxial strain engineering should be considered while designing transistors for radiation hardened applications.

4.6 Conclusion

Peak current and collected charge trends in small 0.1 μm junction pMOSFETs as a function of uniaxial stress are found to be opposite to those in 100 μm junction P+/N diode. For 0.1 μm junction pMOSFETs, the main contribution for the observed stress induced change in peak current and collected charge comes from the stress induced changes in hole mobility change along the <110> direction. For 100 μm junction P+/N diode, the electron mobility change along the <110> direction is the main contributor. Based on our findings, we recommend tensile STI as a good candidate to mitigate SETs and SEUs in deep submicron pMOSFETs in agreement with [116]. The STI induced tensile stress extends both in the surface and bulk as is well known [116, 119-121]. For nMOSFET devices, the addition of tensile STI is completely beneficial – both drive current and SET response is improved simultaneously. For pMOSFET devices, the amount of tensile stress introduced by STI needs careful consideration. The use of multiple surface strain stressors (SiN capping layers and SiGe epitaxial layers) and bulk strain engineering (using tensile STI) would likely be necessary to ensure that there is no degradation in device performance while improving SET response. Previous results

on total ionizing dose effects on strained MOSFETs indicate that the benefits of strain in the channel region are maintained after irradiation [133, 134]. Therefore, uniaxial strained Si technology is an attractive option for space applications.

CHAPTER 5
SUMMARY AND RECOMMENDATION FOR FUTURE WORK

5.1 Summary

The effect of uniaxial stress on (a) threshold voltage shift and carrier mobility in nMOSFETs under radiation and (b) current transients in Si diodes under radiation are studied in this work. Controlled external uniaxial stress is applied via a four point bending setup while the devices are irradiated. Device simulation using FLOODS is used to understand the effect of uniaxial stress on current transients in Si diodes.

Radiation induced charge trapping and mobility degradation are investigated in uniaxially stressed HfO_2 based nMOSFETs. Both uniaxial tensile and compressive stress in nMOSFETs are beneficial in reducing the threshold voltage shift resulting from decreasing the amount of positive charges in HfO_2 and/or SiO_x. The reduction of threshold voltage shift is attributed to the reduced trap activation energy in HfO_2 and/or SiO_x for devices under stress. There is no significant electron mobility degradation in uniaxially stressed nMOSFETs after a total dose of 5 Mrad(SiO_2) irradiation. These results provide the insight that uniaxial strain engineering has the potential to enhance the transistor performance without incurring significant radiation damages.

Electron current transients in uniaxially stressed N+/P diodes are studied both experimentally and theoretically. Uniaxial tensile stress in the diodes decreases the maximum peak current and collected charge for laser-induced current transient in N+/P diodes. Uniaxial compressive stress shows the opposite trend. Device simulations performed using FLOODS validate the experimental results. Using the peizoresistive mobility model implemented in FLOODS, it is possible to predict the effect of high (~1GPa) uniaxial stress on current transients in N+/P diode. Quantitative analysis of

experimental results and FLOODS simulation results suggests that the change in peak current/collected charge can be attributed to the change in the electron mobility along the <001> direction. The trends observed in our analysis of peak current and collected charge in externally stressed N+/P diode directly correlate to the results in STI stressed nMOSFETs as explained in [116].

Similar to analysis of electron current transient in N+/P diode, hole current transients in P+/N diode and pMOSFETs are also investigated as a function of uniaxial stress. Increasing tensile (compressive) stress results in an increase (decrease) in peak current and collected charge in P+/N diode. However, the trends observed in the peak current and collected charge in externally stressed P+/N diode do not correlate to those observed in pMOSFETs, unlike N+/P diodes and nMOSFETs. Very small hole mobility change along the <001> direction as a function of uniaxial stress (~1.1% at 1GPa) [111] and different junction size (~0.1 μm in pMOSFET and 100 μm in P+/N diode) lead to opposite trends observed between P+/N and pMOSFETs. The dominant factor for increasing/decreasing peak current and collected charge in P+/N diode and pMOSFETs is most likely electron mobility change along <110> direction and hole mobility change along the <110> direction, respectively.

Based on simulation results in STI stressed nMOSFETs [116] and pMOSFETs, tensile STI is a good candidate to mitigate SETs and SEUs in deep submicron pMOSFETs, because it is possible to introduce stress into the Si bulk region [116, 119-121]. Previous results on TID effects on strained MOSFETs indicate that the benefits of strain in the channel region are maintained after irradiation [133, 134]. Therefore,

commercial uniaxial strained Si technology is an attractive cost-effective option for space applications.

5.2 Recommendation for Future Work

The thickness of high-k dielectrics reduces with continued MOSFET scaling. Although radiation induced charge trapping in thinner high-k dielectrics has been studied recently, the effect of uniaxial stress on radiation induced charge trapping and mobility degradation in such devices has not reported yet. Therefore, it is very important to research on TID effects on these devices.

This work focused on understanding the physics and modeling of radiation effects as a function of stress at the device level. A study on the effects of uniaxial stress on SETs and SEUs at the circuit level (using simple circuits such as inverters, ring oscillators, and SRAMs) is strongly recommended to further investigate the viability of uniaxial strain engineering for radiation hardened technology.

Additionally, other destructive radiation damages, SEGR and SEB, in uniaxially stressed devices are recommended for investigation.

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BIOGRAPHICAL SKETCH

He received his B.S. degree in Materials Science and M.S. degree in Program in Micro/Nano System from Korea University, Seoul, Korea, in 2002 and 2006, respectively. He received his Ph.D. degree in Electrical and Computer Engineering at the University of Florida, Gainesville FL in the fall of 2011.

He was a process integration engineer in 2003 for LG Display, Korea. During that period, he was involved in developing large size LCD TV panels. He interned at Intel Corporation, Santa Clara, CA from June to December 2011 working on electrical characterization of phase change memory devices. His current research is focused on electrical measurements, characterization, and modeling of strained-Si devices.