COMPARATIVE STUDY OF SUBSTRATE, DIFFUSION BARRIER, AND DEPOSITION METHOD EFFECTS ON COPPER METALLIZATION

BY

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To my father Kuo-Wen Chen, and my mother Bao-Chu Hsieh

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Microelectronic devices have been moving toward smaller and smaller dimensions with increasing functionality. For example, the first generation cell phones were simply used to make phone calls in the 1980s. Thirty years later, the size of the cell phones decreased, and they are used not only as telephones but also as small computers with a wide variety of functions. It is a result of continuing miniaturization of the devices in circuits over the last few decades.

For copper (Cu) interconnects, the mean-time-to-failure has been used as an estimate of how reliable the interconnects are, and it is an average time for a device to encounter failure. The mean-time-to-failure has been shown to be proportional to the average grain size and the intensity ratio between (111) and (200), which are the two

most intense peaks in Cu X-ray diffraction (XRD) spectra. In other words, the growth of strong (111) texture, large and uniform size grains are desired.

For the substrate effect study, it has been known that a smooth and strongly textured copper seed layer is needed to promote the development of highly textured, large grains in the electroplated Cu film, no significant difference in Cu(111) texture was found in the case when silicon (Si) substrate, Si(111) was used as a substrate compared to Si(100). As for the diffusion barrier effect study, Cu seed layers grown on different diffusion barriers had different strengths of (111) texture and the grain size distributions varied drastically. However, those variations ceased when Cu was subsequently electroplated. This might be a result of the formation of an oxide in the Cu seed layer before Cu electroplating (EP). In regard to deposition method effects, sputtered Cu seed layers were found to have much stronger (111) texture than chemical vapor deposition (CVD) Cu seed layers. Additionally, sputtered Cu seed layers had good adhesion to the underlying layers and passed the adhesion tests, but CVD Cu seed layers showed poor adhesion performance. Those discrepancies disappeared again in the electroplated Cu films, and were attributed to the formation of Cu oxide in the Cu seed layers before electroplating of Cu.

CHAPTER 1
INTRODUCTION

1.1 Background

The vast progress in technology over the last few decades has led to a continuous development of miniaturization in microelectronic integrated circuits (ICs). As computer and electronic devices, such as an iPad or cell phone, become indispensible parts of our lives, the demand for higher processing speeds for ICs and functionality of a chip increase. This results in a decrease in interconnect dimensions and an increase in device integration levels. In addition, another advantage following the advance in miniaturization is the lead to a lower cost.[1]

Many materials have been found applicable as a substrate for semiconductor integrated circuits (ICs), including silicon (Si), germanium (Ge) and gallium arsenide (GaAs), etc. Each of them has importance in specific applications. For example, GaAs is important in integrated microwave functions, and Si is used in most of today's ICs due to the fact that Si is the most abundant element on earth, and the ease of growth of silicon oxide (SiO_2), which can act as a good insulator for integrated circuits.

To see how fast the number of transistors that can be put on a chip grows, Moore's Law, an empirical law proposed by Gordon Moore, describes that the number of transistors on an integrated circuit can be doubled approximately every two years.[1] As a

matter of fact, three to four decades ago, the speed of integrated circuits was mainly increased by scaling down the size of the transistors. Scaling of the devices is accompanied by a decrease in the size of the interconnects. However, as the shrinking dimensions continue, the integrated circuit speed is not dominated by the speed of transistors anymore, but the interconnect delay instead. The predominance of the increase in interconnect delay surpasses the effect of scaling of the device when the dimension is smaller than 150nm. The change in interconnect time delay with different technology node has been reviewed and predicted.[2] Additionally, shrinkage of dimensions of the interconnects results in a higher current density in the transistors, which will affect the performance of the device and shorten the lifetime and the reliability of the metal interconnects.

Cu has been suggested as an advanced interconnect material since 1997.[3] IBM first demonstrated that devices with Cu interconnections had a 40-50% decrease in the resistance of Cu wiring relative to Au (Cu) wiring. The new Cu fill scheme, damascene electroplating for Cu, was then developed by IBM. The superfilling feature provided by electroplating can be used to deposit Cu interconnects without voids. Process steps involved in dual damascene are shown in Figure 1-1.

1.2 Challenges to Interconnections

According to the dimensions, interconnects can be local interconnects, semiglobal interconnects, and global interconnects. Local interconnects are very short interconnects that are used at device level. Semiglobal interconnects are interconnects that are used to connect devices within a block. Global interconnects are interconnects that are used to connect components between different blocks and are thus very long. Figure 1-2 shows the schematic diagram of the hierarchy of interconnects.

1.2.1 Resistive-Capacitive (RC) Time Delay in Interconnects

The RC time delay in metal-oxide-semiconductor (MOS) can be represented in terms of circuit response.

$$V_{out}(t) = V_{out}(max)[1-exp(\frac{-t}{RC})] \quad (1\text{-}1)$$

where $V_{out}(t)$ is the output voltage at time t, $V_{out}(max)$ is the maximum output voltage, R is the resistance of the metal line, and C is the capacitance of the circuit.

It can be shown that for a simple system, such as in Figure 1-3, the time delay, τ_L, is roughly equal to 0.89RC.The line resistance is given by:

$$R = \rho\frac{L}{WH} \quad (1\text{-}2)$$

where ρ is the resistivity of the interconnect, and L, W, and H are the interconnect's length, width, and height, respectively. The capacitance between the silicon substrate and the metal interconnect is given by:

$$C_{ox} = K_{ox}\varepsilon_0\frac{WL}{Xox} \quad (1\text{-}3)$$

where X_{ox} and K_{ox} are the thickness and the dielectric constanst of the oxide layer, respectively, and ε_0 is the permittivity of free space. The capacitance between different metal lines is:

$$C_m = K_{ox}\varepsilon_0\frac{HL}{l} \quad (1\text{-}4)$$

where L_s is the distance between two metal lines. For the simple structure, the total line capacitance can be represented as:

$$C = K_l(C_{ox}+C_m) \quad (1\text{-}5)$$

where K_l is a factor approximated by 2. So the time delay can be shown as:

$$\tau_L = 0.89\ K_l K_{ox}\varepsilon_0\rho\frac{L^2}{WH}\left(\frac{W}{Xox} + \frac{H}{l}\right) \quad (1\text{-}6)$$

Let λ be the smallest dimension achievable for each technology generation, which is also assumed to be equal to W, X_{ox}, H, and l, the time delay therefore becomes:

$$\tau_L = 3.56K_{ox}\varepsilon_0\rho\frac{L^2}{\lambda^2} \quad (1\text{-}7)$$

λ is getting smaller as the technology progresses whereas the length of the interconnect may or may not be decreased with the advance of the miniaturization

depending on which level of interconnect is being discussed. For local interconnects, L is usually decreased as λ decreases, which results in no net change in time delay. However, for global interconnects, L increases with a decrease in λ due to the fact that chip area increases as the device dimension shrinks, which requires longer global interconnect to connect all areas of devices. The average length of longest global interconnects in a circuit is given by:

$$L_{max} = \frac{\sqrt{A}}{2} \quad (1\text{-}8)$$

where A is the chip area. Plugging this into Equation 1-7 the global interconnect delay becomes:

$$\tau_L = 0.89 K_{ox} \varepsilon_0 \rho \frac{A}{\lambda^2} \quad (1\text{-}9)$$

Since the chip area A will keep decreasing as the technology progresses and λ is getting smaller, the time delay for global interconnect is increasing.

1.2.2 Electromigration in Interconnects

In addition to RC time delay in the interconnects, electromigration is another primary focus. As devices keep miniaturizing, electromigration becomes a more prevalent. The reliability of ultralarge scale integrated circuits (ULSI) because of the ever-increasing current density in the interconnects. Electromigtration occurs when the momentum of the high energy electrons is transferred to the surrounding metal atoms,

which results in the movement of metal atoms in the direction of electron flow. The movement of the metal atoms in the interconnect leads to failure of the circuit by forming either voids or hillocks. Voids are formed where there is a net depletion of metal atoms, and hillocks are generated where there is a net accumulation of metal atoms.[4,5] To overcome this problem, the introduction of a new material with higher electromigration resistance is needed.

Many factors have been known to affect the electromigration reliability, including grain size, grain size uniformity, crystal orientation, the layers surrounding the metal lines (i.e. diffusion barrier layer and passivation layer), and the metal interconnect material.

Previously, aluminum (Al) was used as the metal for interconnect lines and electromigration has been a major reliability concern. Grain boundaries have been known to be the fastest diffusion path for electromigration in Al-based interconnects.[6] Therefore, improvement of Al electromigration resistance was realized by growing grains of larger size with respect to linewidth, and eliminating the grains which are oriented in a way such that their grain boundaries are parallel to the direction of electron flow. In addition, alloying of aluminum is another way to improve electromigration resistance.

Although the addition of Cu in Al was shown to have higher electromigration resistance than solely Al as an interconnect material, it still cannot provide good

resistance against electromigration as the current density increases.[7,8] Consequently, Cu has been selected as an alternative for IC interconnect material. Compared with Al and its alloy, Cu offers not only higher electromigration resistance, but lower electrical resistivity.[9,10] These properties make Cu more tolerant of higher current densities in today's miniaturized devices and more robust against eletromigration failure. The introduction of copper as a new interconnect material has also necessitated new processing schemes and investigation of material properties. For example, it was reported that the electromigration lifetime of copper interconnects cannot always be improved by forming larger grain size. This implies that the fastest diffusion path of metal in copper interconnects might be different from that of aluminum,[11] where the grain boundary is considered to be the fastest diffusion path. Instead, the top surface of Cu is so far the fastest diffusion path. This can be attributed to the difference in surface/interface condition between copper and aluminum. It has been suggested that copper surfaces and interfaces between copper and its surrounding layers provide faster diffusion path for copper.[12,13] Thus, the surface and interface property control becomes a more important issue regarding the interconnect reliability.

In addition to higher eletromigration resistance, Cu also offers lower electrical resistivity, which helps decrease RC delay in ICs. Although silver has the lowest bulk

electrical resistivity, it doesn't show good electromigration resistance. Copper is preferred over silver since its bulk electrical resistivity is still low, and the eletromigration resistance is expected to be higher due to higher melting point, which indicates stronger copper-copper bonds.

For copper interconnects the mean time to failure (MTTF), an estimate of the average time for the device to encounter failure, is affected by the microstructure of the copper interconnects. Vaidya and Sinha proposed that the dependence of MTTF on the microstructure of the Cu metal interconnect can be expressed as the following equation:[14]

$$\mathrm{MTTF} \propto \mathrm{G} = 3\left(\frac{\mathrm{S}}{\sigma^2}\right)\ln\left[\frac{\mathrm{I}(111)}{\mathrm{I}(200)}\right] \tag{1-10}$$

where G is the geometrical factor, S is the average grain size, σ is the standard deviation of the grain size, and I is the X-ray diffraction peak intensity of specific orientation. That is to say, in order to increase the electromigration resistance, material for the interconnect lines and the fabrication scheme should be chosen and the experimental condition is to be optimized in such a way that the geometric factor is maximized by forming large grain size, smaller standard deviation, and higher (111) peak intensity with respect to (200).

1.3 Challenges to Copper (Cu) Metallization

As mentioned above, the replacement of interconnect material with copper introduced many challenges in IC fabrication; new processing methods are needed. dual-damascene deposition is a new technique introduced in copper metallization.[15-17] The properties of materials have to be investigated more extensively and a fundamental understanding of the diffusion mechanism is required. For example, as stated previously, researchers suggested that the applicability of the correlation between interconnect reliability and microstructure of the material in Al-based interconnects is to be questioned when it comes to copper interconnects, which means a different electromigration mechanism in copper. The stability of copper with its surrounding layers should also be considered. Diffusion of copper into silicon substrate is one of the most important issues that need to be solved.

1.3.1 Diffusion of Cu in Silicon (Si)

Diffusion of Cu atoms into dielectric and silicon substrates causes deterioration of device performance. This phenomenon arises from the concentration gradient between two layers. The Fick's law relates the diffusive flux to the concentration as:

$$J = - D(\frac{\partial C}{\partial x}) \quad (1\text{-}11)$$

J is the atomic flux at position x, C is the atomic concentration, D is the diffusion coefficient. The diffusion coefficient is temperature dependent, which is usually expressed by Equation 1-12.

$$D = D_o e^{-\frac{E_a}{RT}} \quad (1\text{-}12)$$

where D_o is a constant, E_a is the activation energy for diffusion, R is the universal gas constant, and T is the temperature in Kelvin (K). Experimental observations suggested that the activation energy for diffusion depends on the melting point of the material being diffused through Equation 1-13.

$$Ea \propto AT_m \quad (1\text{-}13)$$

where A is a constant, T_m is the absolute melting point of material.

In aluminum-based interconnect systems, Ti/TiN is generally used as diffusion barrier and adhesion promoter. When copper is applied as interconnect material, diffusion becomes an even more serious problem because of the higher diffusivity of copper into Si and SiO_2. The diffusion coefficient of Cu is $2x10^{-5}$ cm^2/s at 500℃, which is much higher than that of Al in silicon ranging from $3x10^{-15}$ to $1.3x10^{-13}$ cm^2/s at 900℃. The fast diffusion of copper in silicon and silicon oxide results in copper precipitates and causes device failure. Furthermore, diffusion of copper into dielectric is another critical problem since it decreases the breakdown voltage of the dielectric.

A diffusion barrier is therefore needed between copper and the dielectric. Appropriate candidates for copper diffusion barriers are characterized by high melting points, good adhesion to copper and the underlying layer, and being chemically inert. Among elements existing in nature, refractory metals and their binary and ternary compounds are most desirable as diffusion barrier materials. The following are materials that have been studied for diffusion barrier applications are:[18-21]

- Refractory metals like titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), and ruthenium (Ru)
- Refractory metal alloys such as Ti_xW_{1-x}
- Refractory metal – silicon alloys and compounds such as TiS_2, W_xSi_{1-x}
- Refractory metal nitride and metal carbide such as W_2N, TaC
- Silicon-nitrogen and silicon carbon compound such as SiC, Si_3N_4

The most commonly investigated materials are titanium, tantalum, and tungsten-based compounds.

1.3.2 Patterning of Cu

One of the challenges accompanying the transition of metal interconnect material from aluminum to copper is the difficulty in patterning copper. Wet etching cannot be used because of its isotropic nature. Reactive ion etching (RIE) uses chemically reactive plasma to generate high energy ions that are used to remove materials formed on the

substrate. RIE still cannot be applied in copper patterning since Cu does not form volatile byproducts with this method. The failure of use of wet etching and RIE in copper pattering urged the development of new metallization schemes with respect to copper.

A known patterning process for Cu metallization is dual-damascene. In the damascene process, the dielectric layer is first deposited, and photolithography and etching are employed to pattern lines and vias in the dielectric. Subsequently, the diffusion barrier is deposited followed by copper film deposition. Excess diffusion barrier and copper is then removed through a process called chemical mechanical planarization (CMP). Process steps for dual-damascene are shown in Figure 1-1.

1.3.3 Advantages of Refractory Carbides and Refractory Nitrides

Although it has been known that refractory transition metals are good candidates as diffusion barrier materials, refractory metal nitrides and carbides are studied more extensively for several reasons. First, carbides and nitrides of transition metals have higher melting points than transition metals themselves, which is a desired feature of a diffusion barrier. Second, the incorporation of nitrogen and carbon increase the mechanical stability. There are many steps in fabrication processing, and the various processing conditions require better mechanical stability of the material. For example, deposition of different layers is accompanied by accumulation of stress. High stress

levels can result in the fracture of the diffusion barrier, which means that a path for copper diffusion is then opened. Formation of transition metal carbides and nitrides help to significantly increase mechanical stability. It is believed that the nitrogen and carbon atoms in transition metal nitrides and carbides consolidate the metal matrix and therefore improve the hardness of the material.

1.4 Problem Statement

Shrinkage of dimensions of microelectronics has led to the challenge of reducing the film thickness of diffusion barrier. International technology roadmap for semiconductor (ITRS), which is organized by a group of semiconductor industry experts, suggested that the thickness of barrier thickness will have to be scaled down to 24Å by 2013. This is driven by the fact that as the dimension of vias and copper lines decrease, the volume allowed for the diffusion barrier must be decreased as well or the volume for copper will be decreased. Since the diffusion barrier layer is part of the metal interconnect, the thickness of diffusion barrier is expected to be smaller so as to form a lower resistivity metal stack. As a result, the reduction in RC time delay of interconnect and current density can then be achieved. Therefore, researchers have been exploring different techniques to find out a decent process for ultra-thin diffusion barrier film deposition.

Since grain boundaries of diffusion barrier film are considered as a fast path of diffusion, elimination of grain boundaries by depositing single crystalline film is desired. However, the lattice mismatch between the diffusion barrier and the substrate makes deposition of a single crystalline film difficult. An amorphous microstructure is the second best choice to meet the requirement because its lack of long range order. An increase in the impurity level resulting from the formation of an oxide or halide in the diffusion barrier should be avoided because oxide impurities in the film lead to an increase in electrical resistivity. Nitrogen incorporation in the diffusion barrier film is believed to stuff the grain boundaries so that the diffusion path for copper through grain boundaries is blocked. Therefore, the presence of nitrogen in a diffusion barrier film is desirable.

The transition from aluminum to copper as the metal for interconnects facilitates development of different diffusion barrier materials, deposition techniques, and fabrication processes for the IC industry. Titanium nitride (TaN) was used as the diffusion barrier material in the aluminum-based interconnect era, but it is not an appropriate candidate for copper interconnects due to the major concern that its oxidation takes place over 500℃. TaN is an alternative for copper interconnects. It has been shown that physical vapor deposition (PVD) deposited TaN films have good performance as a diffusion barrier, but CVD and atomic layer deposition (ALD) deposited TaN films are

more resistive because of the preferential growth of Ta_3N_5 instead of TaN by CVD and ALD,[22] which means TaN cannot be used in future IC generations. As a result, investigation of new materials for the diffusion barrier application is needed. Furthermore, the dual-damascene process flow as mentioned before, is developed for copper metallization. Copper electroplating requires deposition of copper seed layer since the diffusion barrier film is not as conductive.[23,24] Therefore, more fundamental research and studies are required to better understand the relation between the new material and deposition process. Influence of type of diffusion barrier and deposition techniques used for not only diffusion barrier film, but also copper interconnect on reliability of integrated circuits is obvious as expected. Researchers have investigated the dependence of the copper electromigration phenomenon on different diffusion barrier materials, such as titanium (Ti), titanium nitride (TiN), and tantalum nitride (TaN). Copper seed layer deposition by different techniques have also been researched and discussed. For instance, copper seed layer deposition by electroless plating, CVD, and PVD has been reported. The dependence of diffusion barrier materials and the deposition method used in fabrication arise from the properties of the material used and the difference in microstructure and physical properties such as morphology. It is also important to consider processing the sample, either before and after deposition. It has been found

that heat treatment is beneficial to improving film reliability. For example, it has been found that electromigration resistance of the electroplated Cu film is enhanced by annealing, and the electromigration resistance is increased with an increase in annealing temperature within certain temperature range.

In the copper metallization scheme of dual-damascene, a copper seed layer is needed. The copper seed layer is expected to have a strong texture, a smooth surface, and good adhesion strength in order to promote the subsequent growth of a highly textured copper film by the following electroplating (EP), also known as electrochemical deposition (ECD). The interrelationship is complicated by texture, grain size of the diffusion barrier film, and the copper seed layer in the multistacked films. As a result, a thorough examination of the influences of the diffusion barrier layer has on the copper seed layer and the electroplated copper film is required. Barrier type effects on the microstructure and reliability of copper metallization will be discussed in my present work.

Depositing the copper seed layer can be done by PVD, which offers a fairly high deposition rate, strong texture, and good adhesion to the underlying film, but it is not suitable for technology beyond the 45nm generation due to its poor step coverage.[25] CVD provides better comformality so it is capable of filling features with high aspect

ratios.[26-29] However, the adhesion strength is reported to be weaker when deposited on certain diffusion barriers. Comparison of copper seed layers deposited by different techniques on various potential diffusion barriers is presented.

Additionally, the effects of orientation of the substrate have not yet been revealed to the best of my knowledge, so two kinds of substrates (Si(100) and Si(111)) are used for comparison while other reaction conditions and films deposited remained the same.

Copper bulk filling is done by electrochemical deposition, which has been shown to have lowest cost, highest production rate and ease of adoption. Numerous factors such as solution concentration of copper sulfate, pH value of the solution, and voltage applied are said to affect the film properties.[30] Deposition of copper fill by ECD under different conditions and its effects are also examined.

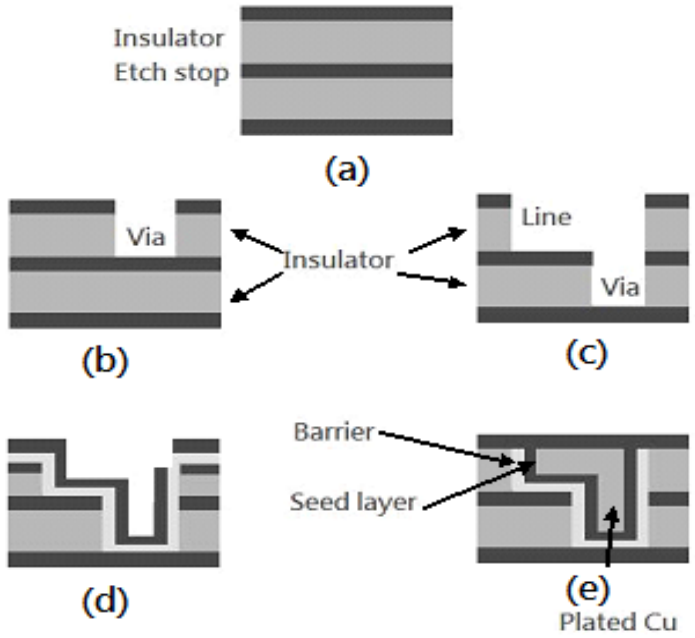


Figure 1-1. Process steps for the fabrication of a via and line level by the dual damascene approach. (a) Insulator deposition. (b) via definition. (c) line definition. (d) barrier and seed layer deposition. (e) plating and CMP.

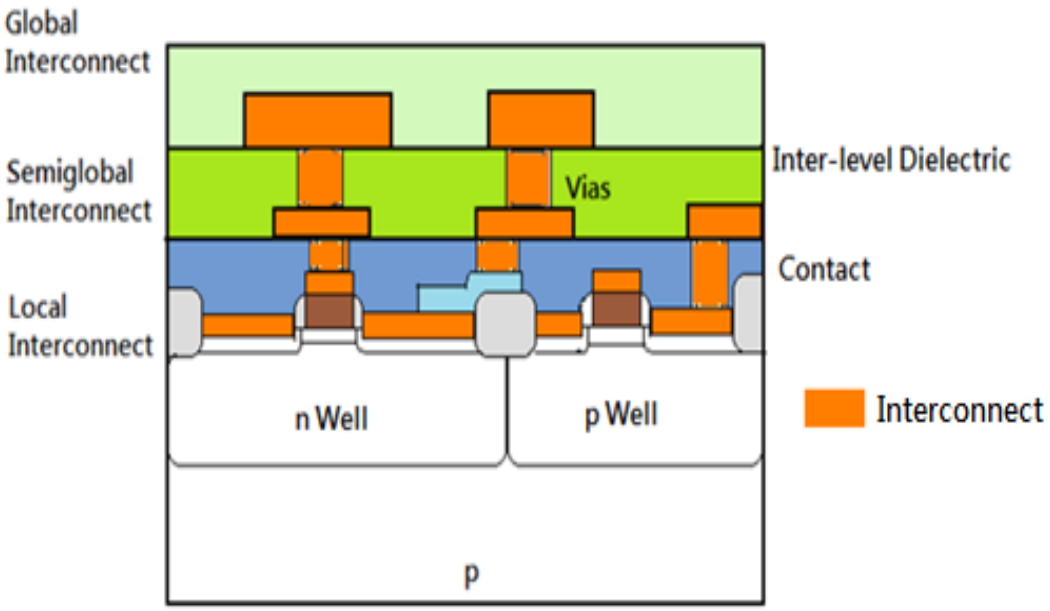


Figure 1-2. Schematic cross-section of a metallization structure.

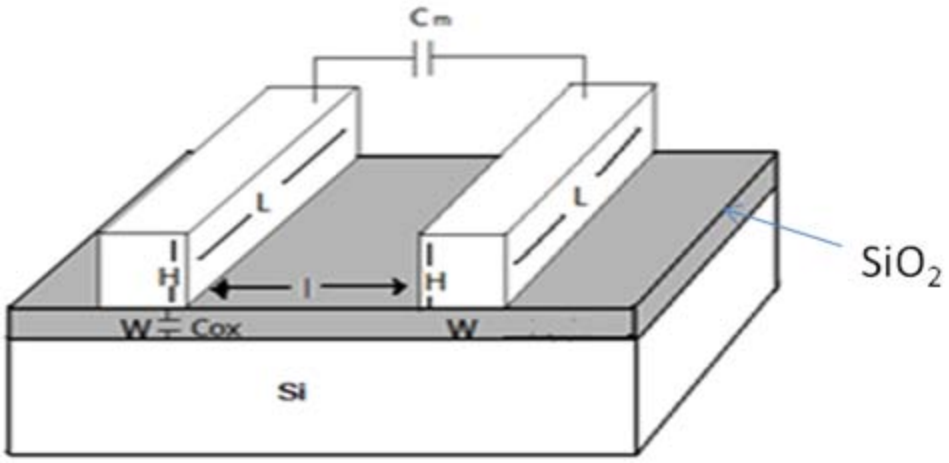


Figure 1-3. Interconnect structure for RC analysis. Two metal interconnects with dimensions of W, L, H lying on SiO_2.

CHAPTER 2
LITERATURE REVIEW

2.1 Deposition Methods for Thin Films

Several deposition techniques have been used in thin film deposition applications, including physical vapor deposition (PVD), chemical vapor deposition (CVD), and atomic layer deposition (ALD). Principles and characteristics of those deposition techniques will be explained and elucidated in this chapter.

2.1.1 Physical Vapor Deposition (PVD)

Evaporation, a physical deposition method, was used in early semiconductor fabrication but is not suitable for future IC generations. As the lateral dimension of electronic devices shrink, the ability to cover surface topography, which is also known as step coverage, becomes increasingly important. The poor step coverage of evaporation results in non-conformal and discontinuous films. Another disadvantage of evaporation is that the production of a well controlled alloy is difficult to achieve, which limits the use of evaporation. Sputtering, which had its debut in 1852, was used as an alternative to evaporation. Compared to evaporation, sputtering provides better step coverage and the feasibility of depositing compound materials and alloys. Other advantages of sputtering include composition consistency between the target material and deposited film can be slightly different, good film adhesion strength, and ease of deposition. In fact, step

coverage remains a critical issue as the scaling of microelectronics continues since sputtering fails to deposit conformal films in high aspect ratio features.

2.1.2 Chemical Vapor Deposition (CVD)

Chemical vapor deposition (CVD) resolves filling high-aspect-ratio conformality issues, and has become a widely accepted thin film deposition method in semiconductor industry. CVD involves homogeneous and heterogeneous reactions. There are many variants of CVD, such as plasma enhanced CVD (PECVD), low pressure CVD (LPCVD), metal-organic CVD (MOCVD), and atomic layer CVD (ALCVD or ALD). CVD has been widely used as a film deposition technique for dielectrics, metals, nitrides, and other materials.

The following is a brief introduction of the most versatile one used in IC industry. Metal organic chemical vapor deposition (MOCVD), also known as organometallic chemical vapor deposition (OMCVD) and vapor phase epitaxy (MOVPE), utilizes metal-organic compounds as a precursor. Since III-V semiconductors and their alloys have been grown by MOCVD successfully, the implementation of MOCVD becomes the most popular growth technique for compound semiconductors.

In a CVD reactor, metal organic precursors are transported by a carrier gas from a bubbler to the reaction chamber through connected tubing. Depending on the particular

precursor being used, careful control of temperature to avoid recondensation of the vapor in the tubing is necessary for some metal organic compounds. These compounds are then delivered to a heated substrate surface.

There are several advantages of MOCVD. For instance, because the precursor used in MOCVD may not necessarily contain halides as ligands, the byproducts formed may not be corrosive and would not need special handling. Consequently, the chances that the underlying layer is etched decrease. However, there are some drawbacks of metal organic precursors. For instance, the carbon containing ligand can result in byproducts that incorporate into the film as impurities. Although film compositions with the proper amount of carbon is beneficial, because it increases the mechanical stability of the deposited film, excess carbon incorporated in the film will lead to an increase in film resistivity and is not suitable for diffusion barrier application.

ALD is a variant of CVD, and its application in deposition of diffusion barriers and copper seed layers have been investigated.[31,32] Different from general CVD, precursors used in ALD are transferred into the reaction chamber in a sequential manner. In practice, one reactant is first introduced into the chamber and chemisorbs onto the surface of the substrates until the surface is saturated. Excess reactants are then purged away. After removal of non-reacted precursors of the first reactant, a second reactant is

sent to the surface to react with the chemisorbed first reactants. The reaction chamber is then purged again. Films grow by repeating this cycle, adding a monolayer of atoms with each introduction of reactant. The most impressive feature of this technique is that it can be used to grow very thin film with high precision due to its self-limiting growth nature. Besides, ALD also offers excellent conformality and low impurity level. ALD's growth rate is intrinsically slow, because only a fraction of layer can be grown per reaction cycle. The slowness is not an issue in future IC fabrication but rather a desirable feature since the thickness needed is always decreasing.

2.2 Characterization

Film properties depend not only on its material properties, but also microstructure and morphology of the deposited film. Therefore, characterization of the film is important. Some important information about the film includes composition, crystallography, surface roughness, electrical resistivity, thickness, morphology, and adhesion between two superposed layers. Summarized use and characteristics of several techniques are presented as the following.

2.2.1 X-Ray Diffraction (XRD)

X-ray diffraction (XRD) is a non-destructive analytical method that can be used to obtain crystallographic structure, degree of preferred orientation, physical properties

such as grain size, and chemical composition of materials. XRD is based on obtaining the scattered beam intensity of an X-ray beam as a function of incident and scattered angle. In powder XRD, identification of unknown material can be done by comparing the diffraction data with a database supplied by International Centre of Diffraction Data. When the film thickness is very thin (1 – 1000nm), the signals of the thin film are very weak, however, mostly very intense peaks stemming from substrate can be observed instead. To get a stronger signal from the film itself instead of that from the substrate, grazing incidence X-ray diffraction (GIXRD) can be utilized. The very small incidence angle of the primary beam results in longer path traveled by X-ray and therefore the information comes more from the thin film.

2.2.2 X-ray Photoelectron Spectroscopy (XPS)

Chemical composition of the film can be obtained by X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), energy dispersive X-ray spectroscopy (EDS), and others. XPS, also known as electron spectroscopy for chemical analysis (ESCA), is a powerful tool that can be used to measure the elemental composition of material quantitatively, and the oxidation state of each element. XPS is a surface analysis technique. Sample surface is irradiated by X-ray with a probe depth of 10nm. The functionality and capability of AES is similar to XPS. AES is surface sensitive

and it can be applied to obtain elemental composition of the film. In addition to composition determination, the use of argon sputtering equipped in both XPS and AES make it possible to perform depth profiling of deposited films. Another feature that XPS and AES have in common is that they can be used to detect most of the elements in nature, except for hydrogen and helium.

2.2.3 Energy Dispersive X-ray Spectroscopy (EDS)

Energy dispersive X-ray spectroscopy (EDS) is another analytical technique that has the ability to perform elemental analysis of material. However, this technique is considered as a way to determine composition of material only semi-quantitatively since the accuracy of the spectrum is dependent on so many factors. Elements that can be detected by using this technique are those with atomic number greater than four.

2.2.4 Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) is often used to measure surface morphology and topography of samples. The contrast shown on the SEM image also reveals information about atomic number difference. During operation, a high energy electron beam strikes specimen surface and interacts with atoms in the sample, and then ejected electrons are captured by a detector. Those electrons can be either secondary electron or back scattered electrons. Secondary electrons resulting from inelastic scattering of the

incoming electron beam near or at the specimen surface are generally insensitive to atomic number. Therefore, secondary electrons can provide very high resolution images of the specimen surface. Back-scattered electrons, on the other hand, arise from elastic scattering although they are also influenced by inelastic scattering. Back-scattered electrons are atomic number dependent: the higher the atomic number, the more electrons escape the surface of specimen. Thus, the image of back-scattered electrons can be used to obtain the distribution of elements in the specimen.

Techniques that are commonly used in determination of film thickness are cross-sectional scanning electron microscopy (XSEM) and transmission electron microscopy (TEM). Both SEM and TEM can provide highly accurate information about film thickness. The profilometer is another piece of equipment that can be used to measure film thickness. The vertical resolution of a profilometer is in the nanometer level, but accurate profiling of the film requires experienced operation. Another common use of profilometer is measurement of surface roughness.

2.2.5 Atomic Force Microscopy (AFM)

As mentioned above, a profilometer is an instrument that is used to measure surface roughness. Another apparatus that is also frequently used for the same purpose is atomic force microscopy (AFM). AFM is a destructive apparatus because the surface

is scanned across and scratched by a probe; a cantilever. The resolution of AFM can be a fraction of nanometer. AFM allows measurement of root-mean square (RMS) surface roughness and average grain size. The advantage of AFM over SEM is that AFM gives 3-dimensional profile of the sample, while SEM offers a 2-dimensional image of a sample. Furthermore, AFM does not require high vacuum environment, which lowers the cost on the equipment and maintenance.

2.2.6 Four Point Probe

Measurement of resistivity of thin films is usually done by the four point probe. Sheet resistance can be measured by passing current through two outer probes and simultaneously measuring the voltage through two inner probes. Knowing the thickness of the film, film resistivity can then be readily derived by multiplying the sheet resistance by the film thickness.

2.2.7 Scotch® Brand Tape Test

Scotch® brand tape test is the most common method used to determine adhesion strength qualitatively. A sticky tape is attached to the film and then removed to see how good the adhesion of the film is to the underlying layer. To determine the adhesion strength quantitatively, another technique, four point bend test, is one of the choices.

CHAPTER 3
EXPERIMENTAL TECHNIQUES FOR THIN FILM DEPOSITION AND CHARACTERIZATION

3.1 Substrates Used for Experiments and Precleaning of the Substrates

Substrates used in this study are 500-550μm thick p-type Si(100) doped with boron by Cemat Silicon S.A. and 505-545μm thick n-type Si(111) doped with arsenic by Crysteco. All the substrates are cleaned by a standard process described as the following:

Substrates dipped in boiling trichloroethylene (TCE) for 3 minutes

- Substrates dipped in boiling acetone for 3 minutes
- Substrates dipped in boiling methanol for 3 minutes
- Substrates dipped in boiling de-ionized water (DI water) for 30 seconds
- Substrates dipped in buffer oxide etch (BOE) solution for 2 minutes
- Substrates cleaned by swab soaked in acetone
- Substrates dried in continuous nitrogen flow

3.2 Description of the Sputtering Reactor

KJL® CMS-18 Multi-Source was used to deposit the diffusion barrier films: Ta, TaN, Ta/TaN multistack, W_2N, and part of the copper seed layers. It is a Combinatorial Material Science thin film sputtering system. The temperature of the process chamber was maintained at around 20℃. Since silicon oxide is formed very quickly in air atmosphere, before diffusion barrier/copper deposition, substrates were sputter-cleaned with argon ions in the reaction chamber for 60 seconds to remove silicon oxide formed

during the time of air exposure before entering the vacuum chamber. Deposition of each material was done by following recipes in the computer where deposition rates were known, although with certain level of error. By putting in the desired film thickness, the corresponding time of deposition was then determined. The thickness of the single-layer diffusion barrier, Ta, was 25nm. Since the deposition rate of Ta was 2.84Å per second, the deposition time was 88 seconds. The thickness of the single-layer diffusion barrier of TaN was also 25nm, given deposition rate of 0.83Å per second, the deposition time was 300 seconds. For the double-layer diffusion barrier of Ta/TaN, the thickness of each layer was set to be 20nm and 25nm, respectively. The deposition time of each layer was 71 seconds and 300 seconds, respectively. Deposition of W_2N was fabricated by reactive sputtering in argon/nitrogen atmosphere ($Ar/N_{2)}$.[33-36] It has been reported by researchers that W_2N phase is formed when the molar ratio of N_2 to Ar is greater than 1. Accordingly, the pressure set point of the chamber was 10 mTorr. The gas flow rate of Ar was 29.1sccm, and the gas flow rate of N_2 was 42.1sccm. The thickness of the W_2N film was 30nm, and the deposition time was 143 seconds since the deposition rate was 2.1Å per second.

3.3 Description of CVD Reactor

An in-house built chemical vapor deposition (CVD) reactor was used as another means to deposit copper seed layers. The reactor has two chambers, one used for atomic layer deposition (ALD) for diffusion barrier films, and the other is a CVD chamber designed for copper deposition. The reactor set-up permits in-situ transfers of samples. The system was equipped with gas lines for delivery of nitrogen, ammonia, helium, and hydrogen gas. The metal-organic gas lines were wrapped with heating tapes to avoid recondensation of vapor precursor in the tubing. Gas flow rates are controlled by an MKS mass flow controller. The precursor was kept in a quartz tube bubbler and was transported to the reactor by nitrogen, as a carrier gas, once the valves on inlet and outlet were open. The temperature of the bubbler bath was maintained at 45 to 46℃.

3.4 Precursor for Cu Deposition

The precursor used for copper deposition was copper (I) hexafluoropentanedionate vinyltrimethylsilane (copper(hfac)(vtms)).

3.5 Operating Procedure for CVD Reactor

3.5.1 Pretreatment for the Samples and CVD Deposition Procedure

Before copper deposition took place, the reaction chamber was first pumped down to base pressure of approximately 0.26 Torr, and then hydrogen gas was introduced into

the reactor to reduce the oxide formed on the substrate surface for 10 minutes at 200℃. After reduction of the oxide the precursor was delivered into the reaction chamber for copper deposition. The susceptor was heated by a resistive heater and the reaction temperature was kept at 185℃. The reaction time lasted 70 minutes for each run resulting in a copper seed layer with thickness around 70nm. The flow rate of hydrogen was fixed at 196sccm, and was 50sccm for the nitrogen carrier gas. The growth rate of copper was around 1 nanometer per minute and was determined by dividing thickness by reaction time. Details concerning copper film growth rate will be clarified later. After the reaction was completed, the heater was shut off while the reactor was still kept under vacuum. Samples were taken out from the reactor after about 2 hours to let them cool to near room temperature to prevent rapid oxide formation due to high thermal energy.

3.5.2 Growth Rate – Cu Seed Layer Deposition by Metallo Organic Chemical Vapor Deposition (MOCVD)

The growth rate of the MOCVD grown Cu seed layer was measured by depositing Cu films under identical conditions less the duration to allow growth of thicker Cu films. The thickness of the Cu film was measured by cross-sectional SEM, and the Cu growth rate was then determined by dividing the measured thickness by the reaction time.

Figure 3-1 shows the cross-sectional image of Cu film deposited on silicon substrate for 120 minutes. The Cu film was about 120nm thick so the growth rate of Cu film was 1nm/min.

3.6 Electroplating (EP) of Cu Bulk Fill

3.6.1 Parameters for Electrochemical Deposition

Electroplating (also called electrochemical deposition (ECD)) of Cu was performed to grow thicker Cu film. Samples deposited with a copper seed layer were attached to the cathode, which is a copper bar. A graphite bar was used as an anode. A saturated Calomel electrode (SCE) was used as the reference electrode. The solution consisted of 0.01M copper sulfate ($CuSO_4$), sulfuric acid (H_2SO_4) and deionized water. The pH value of the solution was adjusted to around 3 to 4, tested by hydrion papers. The applied voltage was set to be -500mV.

3.6.2 Growth Rate – EP Cu Fill

Again, the growth rate of electroplated Cu was determined by dividing the thickness of Cu electroplated on the Cu seed layer by the time of the reaction. A cross-sectional view of EP Cu on Ta was examined, and the thickness of EP Cu was around 800nm as shown in Figure 3-2.The reaction time for electroplating was 600 seconds for all runs. Thus, the growth rate was 1.33nm/sec.

3.7 Techniques for Thin Film Characterization

3.7.1 X-Ray Diffraction (XRD)

Thin film crystallinity was examined by a Philips APD 3720. The scattering angle, 2θ, was scanned from 25 to 70 and 40 to 55 2θ degree. X-ray radiation was generated by applying 40 kV and 20 mA to emit Cu K_α radiation. The wavelength of the emitted X-rays is 1.54Å. Peaks obtained from the XRD spectra were compared with reference spectra in the Joint Committee on Powder Diffraction Standards (JCPDS) database. The extent of crystallinity and phase of the material can therefore be determined by the relative peak intensities and the peak positions.

Peak positions in XRD can be used to calculate the lattice parameter of a unit cell. The inter-planar spacing, d, is obtained by using Bragg's law.

$$d = \frac{\lambda}{2\sin\theta} \quad (3\text{-}1)$$

where λ is the wavelength of the X-ray, which is 1.54Å. The lattice parameter, a, for a cubic cell can be acquired from the equation

$$\frac{1}{d^2} = \frac{1}{a^2}(h^2+k^2+l^2) \quad (3\text{-}2)$$

where h, k ,and l are Miller indices. For a hexagonal crystal, the lattice parameters, a and c, can be calculated by equation

$$\frac{1}{d^2} = \frac{4}{3a^2}(h^2+hk+k^2)+\frac{1}{c^2}(l^2) \quad (3\text{-}3)$$

Grain size can also be determined by XRD. The broadening of the peak is correlated to the grain size of the film by the Scherrer equation.

$$\tau = \frac{K\lambda}{\beta\cos\theta} \quad (3\text{-}4)$$

where K is the shape factor, λ is X-ray wavelength, β is the line broadening at half the maximum intensity (FWHM) in radians, and θ is the Bragg angle. τ is the mean size of the ordered domains, which may be smaller or equal to the grain size. The shape factor K is typically 0.9, but will vary with the actual shape of the crystal.

Data processing and analysis were done by using the software X'Pert Plus and performed Microsoft Excel. Background correction and smoothing of the curve were as to reduce the noise level and identify peaks in the spectra.

3.7.2 Scanning Electron Microscopy (SEM)

Morphology of the surface and thickness of the films was measured by a JOEL® 6335F FEG-SEM. Electrons were generated by applying 15 kV on a single crystal tungsten tip. Secondary electrons escaping from the surface after interaction with the sample were collected by a detector. Secondary electrons have lower energy and are generated near the surface. They can be used to obtain feature images (morphology/topography) of the film. Thickness of the films was obtained by measuring the cross-section of the films. For film thickness measurement, each sample was first

dipped into liquid nitrogen for 15 seconds and then scratched and cleaved into two smaller pieces with a diamond pen. The sample was then positioned vertically to allow examination of its cross-section. Copper tape was used to attach the samples to the stub and to avoid charging effect.

3.7.3 Four Point Probe

The film sheet resistance and resistivity were measured by a four point probe. The four point probe is a common method used for characterizing semiconductors, as it provides absolute measurement without the need of standard. Four tips are lined up in a row, and current is passed through the two outer tips and then the voltage across the two inner tips is measured. The distances between the tips are determined from mathematical derivation so a simple equation for sheet resistance is given by equation.

$$R_s = 4.53 \times \frac{V}{I} \tag{3-5}$$

where V is the voltage across the two inner tips and I is the current passing through two outer tips.

Once the sheet resistance is obtained, the resistivity of the film, ρ, can be calculated by Equation 3-6

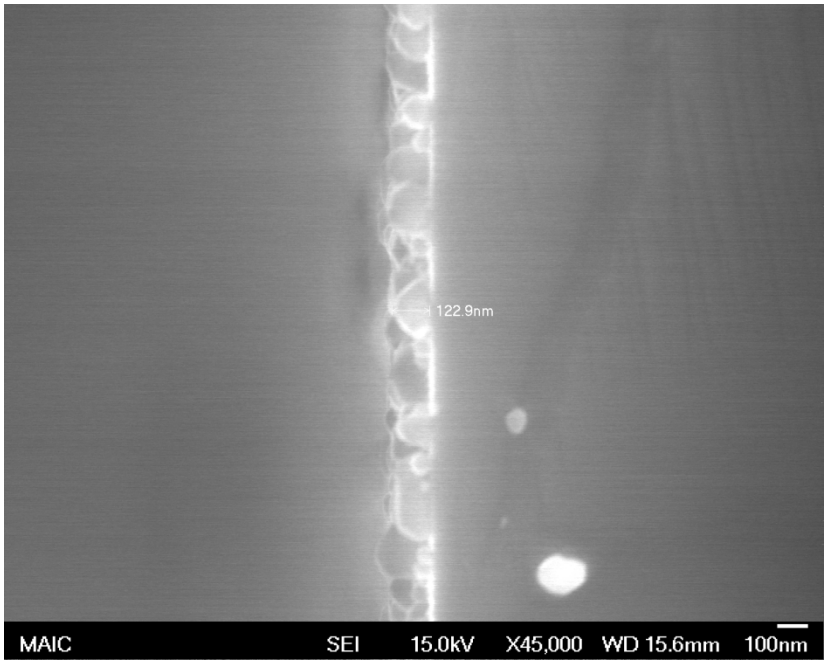
$$\rho = R_s \times t \tag{3-6}$$

where t is the film thickness, which can be obtained from cross-sectional SEM image.

3.7.4 Scotch® Brand Tape Test

Scotch® tape was used to test how adhesive the deposited film is to its underlying layer. Peeling of the films occurs when adhesion between the deposited film and the underlying layer is poor.

A)



B)

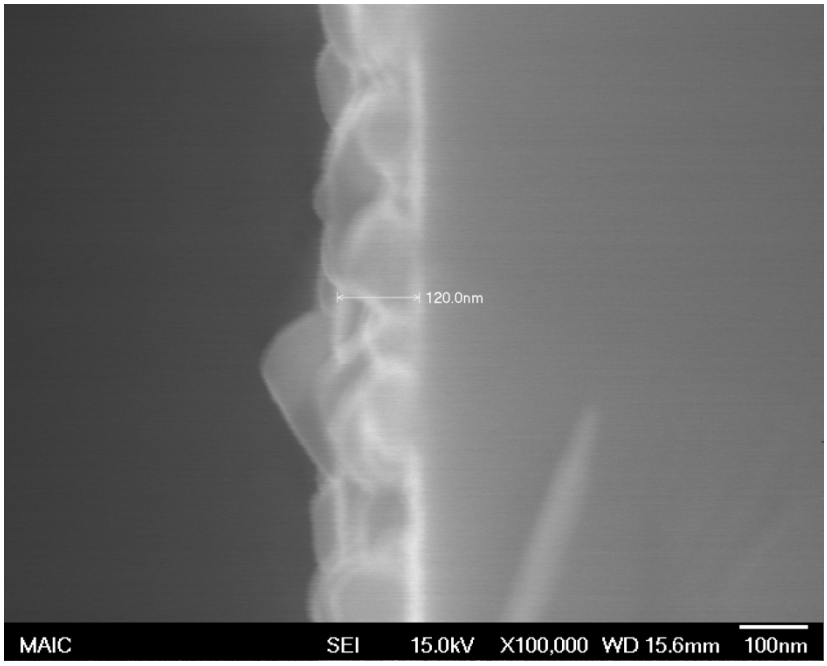
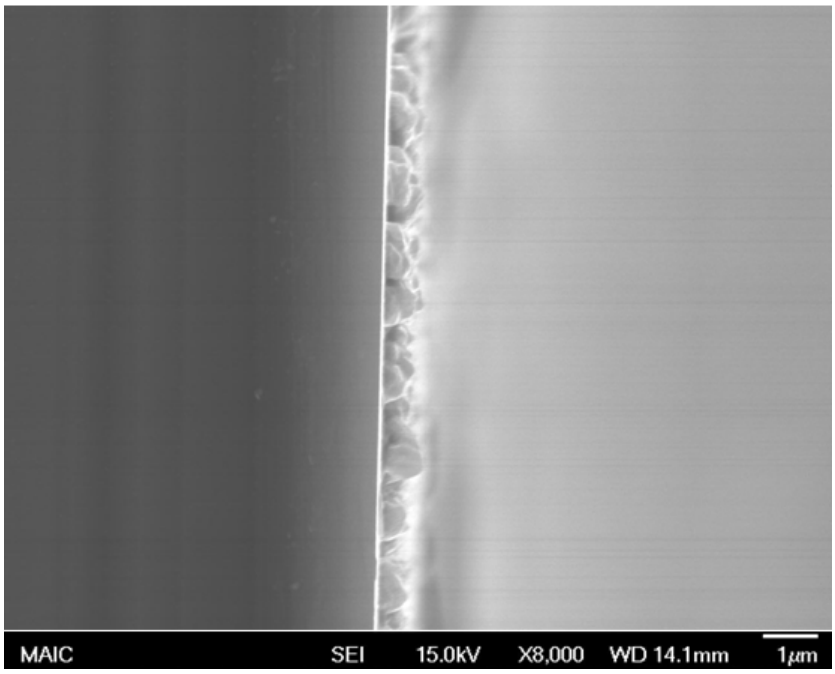


Figure 3-1. SEM cross-sectional images of Cu deposited by MOCVD for 120 minutes. A) X45,000. B) X100,000

A)



B)

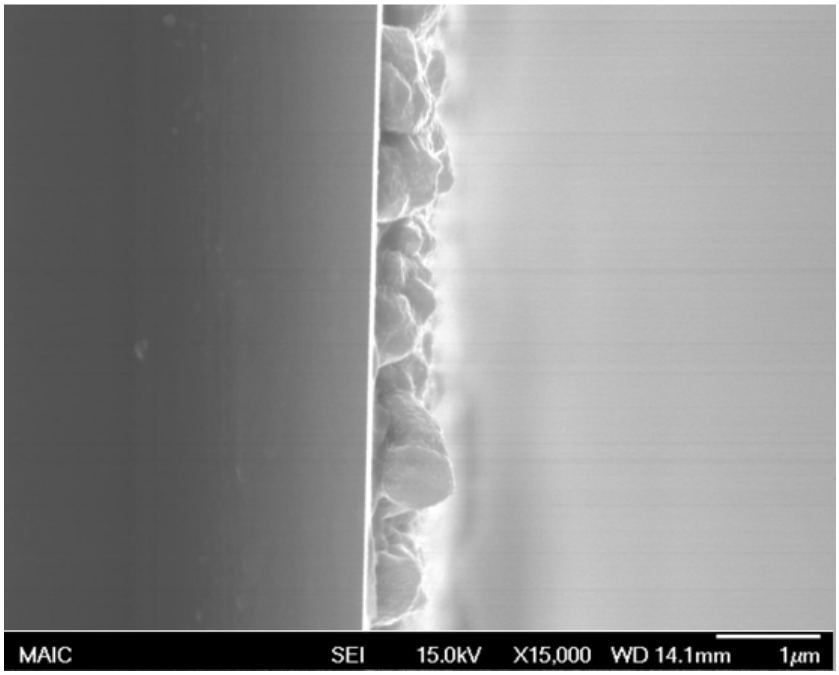


Figure 3-2. SEM cross-sectional images of EP Cu after 10 minutes. A) X8,000. B) X15,000.

CHAPTER 4
SUBSTRATE EFFECTS ON DIFFUSION BARRIER, COPPER SEED LAYER, AND COPPER BULK FILL

Two blanket silicon substrates with different crystallographic orientations (Si(100) and Si(111)) were used for subsequent diffusion barrier layer deposition, copper seed layer deposition, and bulk copper fill. The effects of the orientation of substrate have not been studied to the best of my knowledge. Two common and promising diffusion barrier systems Ta/TaN and W_2N were used here. To begin with, diffusion barrier films were deposited onto two different silicon substrates at the same time, which means that both films were grown under the exact same deposition condition including deposition time, deposition temperature, and deposition rate. The Cu seed layer was deposited by MOCVD and electrochemical deposition was performed to make thicker Cu layers, thereafter. After deposition of each layer, the film deposited was examined by XRD, SEM, four point probe, and an adhesion test. The dependence of substrate effect on diffusion barrier materials is discussed.

4.1 X-Ray Diffraction Measurement

4.1.1 Film Crystallinity

Figure 4-1A shows the XRD spectrum for Ta/TaN films deposited by sputtering. XRD spectra of Ta/TaN multilayer show that on Si(100) and Si(111) the Ta/TaN

multilayers are amorphous as indicated by amorphous humps in the spectra (not shown in the spectra here since they are background corrected), disregarding the crystal orientation of the substrate they were grown on. Only peaks of the silicon substrates (2θ = 69.23 for Si(100) or 2θ = 28.44 for Si(111)) appeared in the spectra. Since Ta/TaN films deposited on both Si(100) and Si(111) had poor crystallinity, the films were very likely amorphous and the grain sizes were very small. The crystal structure of W_2N is cubic. Three most intensive peaks of W_2N within the scanning range are expected to appear at 37.734, 43.848, and 63.734 2θ degrees. Again, the XRD spectra show that W_2N films were amorphous since no peaks appeared in the spectra for W_2N sputtered on Si(100) and Si(111).

Copper seed layers, 70 to 80nm thick, were deposited on each of the diffusion barriers on Si(100) and Si(111). The XRD measurement was conducted as to compare the degree of crystallinity of Cu seed layer with respect to different underlying substrates. In general, copper has a crystal structure of face-centered cubic (fcc), and for Cu metal its three most intensive XRD peaks show up at 43.297, 50.433, and 74.130 2θ degrees. It should be noticed that the 43.297 2θ degrees peak arises from (111) oriented planes, and 50.433 2θ degrees results from (200) planes. The texture of the Cu film is not always the strong (111) orientation, and the change in strength of (111) and the presence of

other peaks is related to many experimental factors.[37] Since the Cu(111) orientation shows the best resistance toward electromigration and has the lowest electrical resistivity of any textures, the XRD peak intensity ratio of $I_{(111)}$ to $I_{(200)}$ becomes a measure of how good the film is in terms of electronmigration resistance and electrical resistivity. However, determination of the intensity of peaks existing in the spectra was difficult since the background noise level was high and the amorphous hump introduced ambiguity. As a result, background correction was applied to data analysis. After the background was corrected for smoothing of the data was performed to reduce the noise level.

Figure 4-3 shows the background corrected XRD spectrum of the Cu seed layer deposited onto the Ta/TaN stacks on two types of substrates. On both substrate types, the $I_{(111)}/I_{(200)}$ ratio was 3.55. It can be referred from this result, that the substrate orientation has no bearing on the Cu seed layer.

When W_2N was grown as a diffusion barrier, the crystal orientation of the copper seed layer has to be discussed in a different way. The XRD spectra of the Cu seed layer on W_2N are shown in Figure 4-4. The $I_{(111)}/I_{(200)}$ ratio was 1.79 for the Cu seed layer deposited on W_2N/Si(100). When Si(111) was used as the substrate, the ratio $I_{(111)}/I_{(200)}$

was 3.2. Dissimilar to the result when Ta/TaN was used, Cu seed layer (MOCVD) deposited on W_2N had higher $I_{(111)}/I_{(200)}$ when Si(111) was applied as a substrate.

The texture of electroplated (EP) Cu on Cu seed layers was also examined in order to investigate how a change in substrate effects the electroplated Cu films. In the scanning range specifically performed from 40 to 55 2θ degrees, almost all the samples had a very intensive Cu(111) peak emerging at around 43.35 2θ degrees and a relatively smaller Cu(200) peak appearing at around 50.49 2θ degrees as shown in Figure 4-5. $I_{(111)}/I_{(200)}$ was calculated for each sample to demonstrate the degree of preferred (111) orientation as follows.

Results of electroplated Cu on a Cu seed layer deposited by MOCVD were obtained. Firstly, when Ta was deposited as an interlayer between TaN and electroplated Cu for better adhesion strength between TaN and Cu, $I_{(111)}/I_{(200)}$ was found to be 4.09 for electroplated Cu on MOCVD Cu seed layer/Ta/TaN/Si(100) and 3.49 for that on MOCVD Cu seed layer/Ta/TaN/Si(111). Secondly, Cu electroplated on MOCVD Cu seed layer/W_2N/Si(100) gave $I_{(111)}/I_{(200)}$ of 4.75, and that on MOCVD Cu seed layer/W_2N/Si(111) gave a value of 8.71.

4.1.2 Polycrystal Grain Size

The grain size can be estimated using the Scherrer equation assuming that the broadening of the peaks in the XRD spectra resulted from the crystallite grain size distribution. The most intense peak, the Cu(111) peak at around 43.3 2θ degrees, was used to determine FWHM and estimate the grain size.

Estimated grain sizes of Cu seed layer (MOCVD) are listed in Table 4-1 and Table 4-2. When the Ta/TaN stack was used as diffusion barrier, the average grain size of Cu seed layer deposited by MOCVD was 36.2nm when Si(100) was the substrate, and was 54.4nm when Si(111) was the substrate. When deposited on W_2N, Cu seed layer had the average grain size of 54.4 nm on Si(100) and 72.4nm on Si(111).

Table 4-3 and Table 4-4 show the estimated grain size of EP Cu on different diffusion barriers on different substrates. Grain sizes of electroplated Cu were also estimated by using the Scherrer equation. For Ta/TaN, the grain size was calculated to be 72.4nm for electroplated Cu on CVD deposited Cu seed layer/Ta/TaN/Si(100) and 61.9nm for electroplated Cu on CVD deposited Cu seed layer/Ta/TaN/Si(111). A slight difference in grain size was obtained for electroplated Cu on MOCVD deposited Cu when W_2N was used as a diffusion barrier. The estimated grain size was 89.0nm and

87.2nm for electroplated Cu on MOCVD deposited Cu/W_2N/Si(100) and that on CVD deposited Cu seed layer/W_2N/Si(111), respectively.

4.2 Scanning Electron Microscopy

Scanning electron microscopy was utilized to examine the morphology (i.g. grain size and shape of the grains) of Cu films deposited on top of Ta/TaN, and W_2N on two different substrates. Also, the grain size distribution was determined.

For diffusion barriers deposited by sputtering, no grains can be seen even under maximum magnification, X500,000. This might be a result from: (1) the diffusion barrier films deposited by sputtering were so smooth that the topography did not lead to change in contrasts from secondary electrons. (2) grains were too small to be resolved by SEM. (3) the deposited layer were not conductive enough and therefore charging of electrons took place. The cause can be figured out by either using TEM to get to higher magnification and see if grains can be resolved or coating the diffusion barriers to increase the electrical conductivity.

As for the Cu seed layer grown by MOCVD, surface morphology was examined by using SEM. Two magnifications (X30,000, and X70,000) were used to obtain the average grain size and the grain size distribution of the Cu seed layer. Five grains in

each of the SEM images with clear boundaries were chosen and their average grain sizes were measured.

SEM images of the Cu seed layers deposited by MOCVD onto the Ta/TaN bilayer system on Si(100) and Si(111) are shown in Figure 4-6. For the Cu seed layer deposited on Ta/TaN/Si(100), two groups of grains with slightly different grain sizes were observed; their size ranged from around 50nm to 170nm. A similar result was obtained for Cu seed layer deposited on Ta/TaN/Si(111).

A similar approach was taken for W_2N based diffusion barriers. As shown in Figure 4-7, the grains of the Cu seed layer were large. In both case, the average grain size was greater than 100nm. Since sufficiently many size grains were formed in the Cu film was observed in both cases, the size uniformity of the Cu seed layer was poorer. However, grains in the copper film were spherical.

The Cu seed layer seemed to be discontinuous on W_2N, as can be seen in the SEM images. The grain sizes varied drastically from 20nm to more than 200nm. This phenomenon occurred in both Si(100) and Si(111). The only difference was that the Cu seed layer on the Si(111) had larger grains and were more densely distributed. Therefore, the average grain size of Cu seed layer on Si(111) was slightly larger than that on Si(100).

The surface morphology for electroplated Cu was observed via SEM as well. SEM images are shown in Figure 4-8 and Figure 4-9. The grains of electroplated Cu were much larger than those deposited by MOCVD as discussed above. Normally two different sizes of grains were observed, including one group of larger grains with sizes 700 to 800nm, and the other group contained smaller grains whose diameters were just a few tens of nanometers.

4.3 Film Resistivity

Sheet resistance was measured by a four point probe and the resistivity was then readily calculated by multiplying the measured sheet resistance by the film thickness. Since the films were thin, the electrical properties of the film were not easy to measure because the measured values fluctuated drastically if not enough care was taken. In order to minimize instrumental error, the sheet resistance was measured five times and the average of those values was taken as the sheet resistance of that sample. All Cu seed layers here were deposited by MOCVD, followed by ECD for thicker films. All the films resistivities are listed in Table 4-3 to Table 4-4.

Ta/TaN on Si(100) had a sheet resistance of 4.88Ω with thickness of 90nm, and the film resistivity was therefore 43.92μΩ-cm. The same multi-stack Ta/TaN deposited on Si(111) had a sheet resistance of 1.55Ω, which corresponded to a film resistivity of

13.95μΩ-cm. Sheet resistances of W_2N measured were 124.8Ω for W_2N on Si(100) and 178.4Ω for W_2N on Si(111), which corresponded to film resistivities of 312μΩ-cm and 446μΩ-cm, respectively.

Since the deposition time for all experiments was fixed at 70 minutes, the thicknesses of Cu seed layers were all approximately 70nm. The sheet resistance of the Cu seed layer on the Ta/TaN stack on two types of silicon substrates was obtained. For Cu seed layer deposited on Ta/TaN on Si(100) and Si(111), the sheet resistances were 65.06mΩ and 67.68mΩ, respectively. The resistivity of Cu seed layer on Si(100) was 0.455μΩ-cm and was 0.473μΩ-cm for that on Si(111). The dependence of resistivity on orientation of silicon substrate in the Ta/TaN bilayer case was not significant.

When W_2N was deposited as a diffusion barrier, the difference in sheet resistance, as well as resistivity, was obvious. The Cu seed layer on Si(100) had a lower sheet resistance of 69.8mΩ compared with 129.2mΩ for that on Si(111). The calculated resistivities were 0.484μΩ-cm and 0.904μΩ-cm for the Cu seed layer on Si(100) and Si(111), respectively.

4.4 Scotch® Brand Tape Test

Scotch® tape tests were conducted to determine the adhesion strength of Cu films to its underlying layers qualitatively. Cu films grown on different types of Si substrates

were compared. For the Cu seed layer deposited by MOCVD when the Ta/TaN stack was used as a diffusion barrier, a small amount of Cu debris was removed by the tape after test (denoted as pass (fair)) regardless of the substrate used. The same thing occurred to the Cu seed layer (MOCVD) on W_2N, and even more Cu was found on the tape (denoted as pass (poor)) for the case when W_2N was deposited on Si(100). For EP Cu, removal of Cu happened for all the samples, complete removal of the Cu film was observed (denoted as fail) in the case where EP Cu was deposited on Ta/TaN/Si(111). Table 4-8 and Table 4-9 summarize the test results.

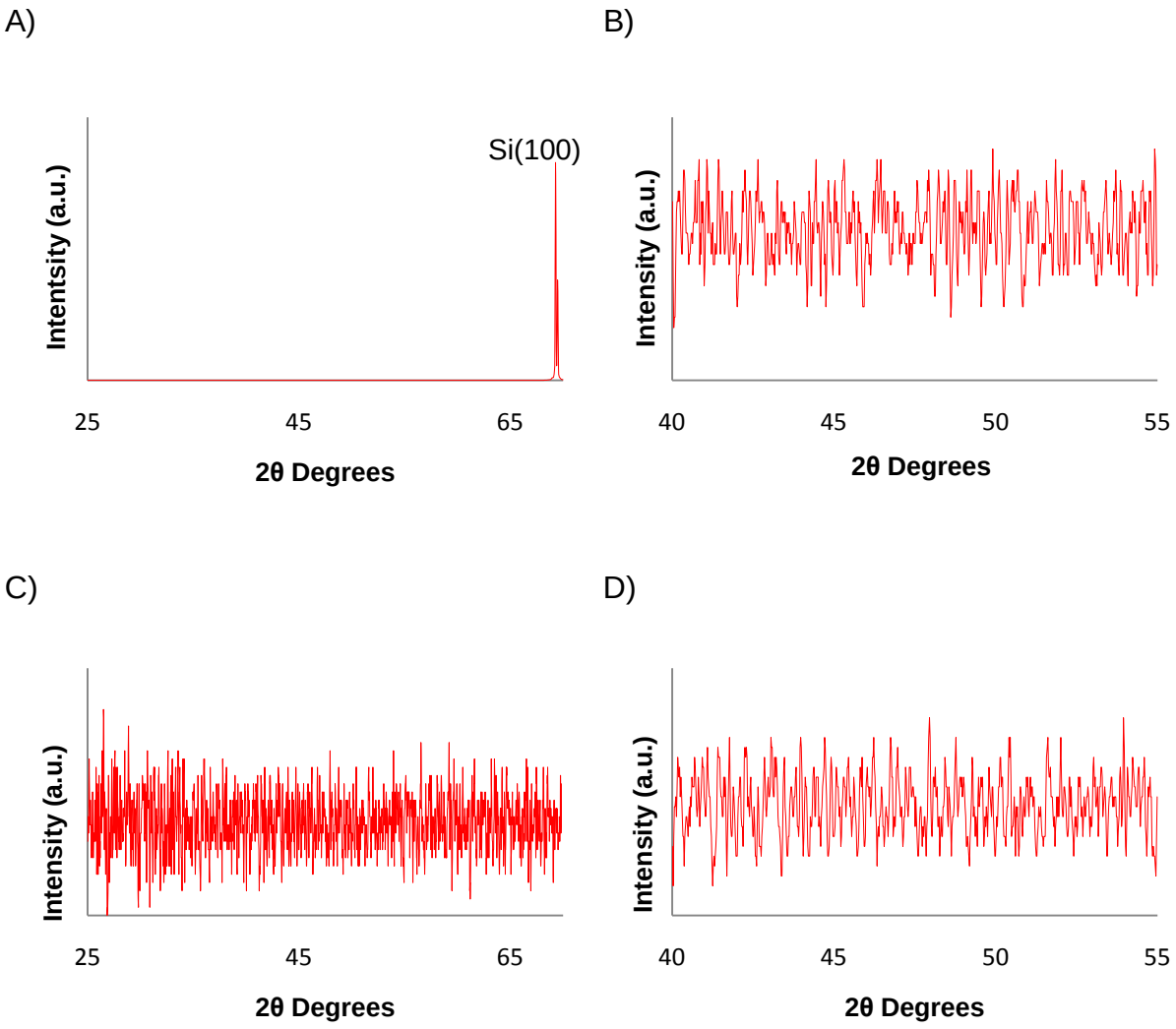


Figure 4-1. XRD spectra for sputtered Ta/TaN on different Si substrates. A) Si(100) with scanning range from 25 to 70 2θ degrees. B) Si(100) with scanning range from 40 to 55 2θ degrees. C) Si(111) with scanning range from 25 to 70 2θ degrees. D) Si(111) with scanning range from 40 to 55 2θ degrees.

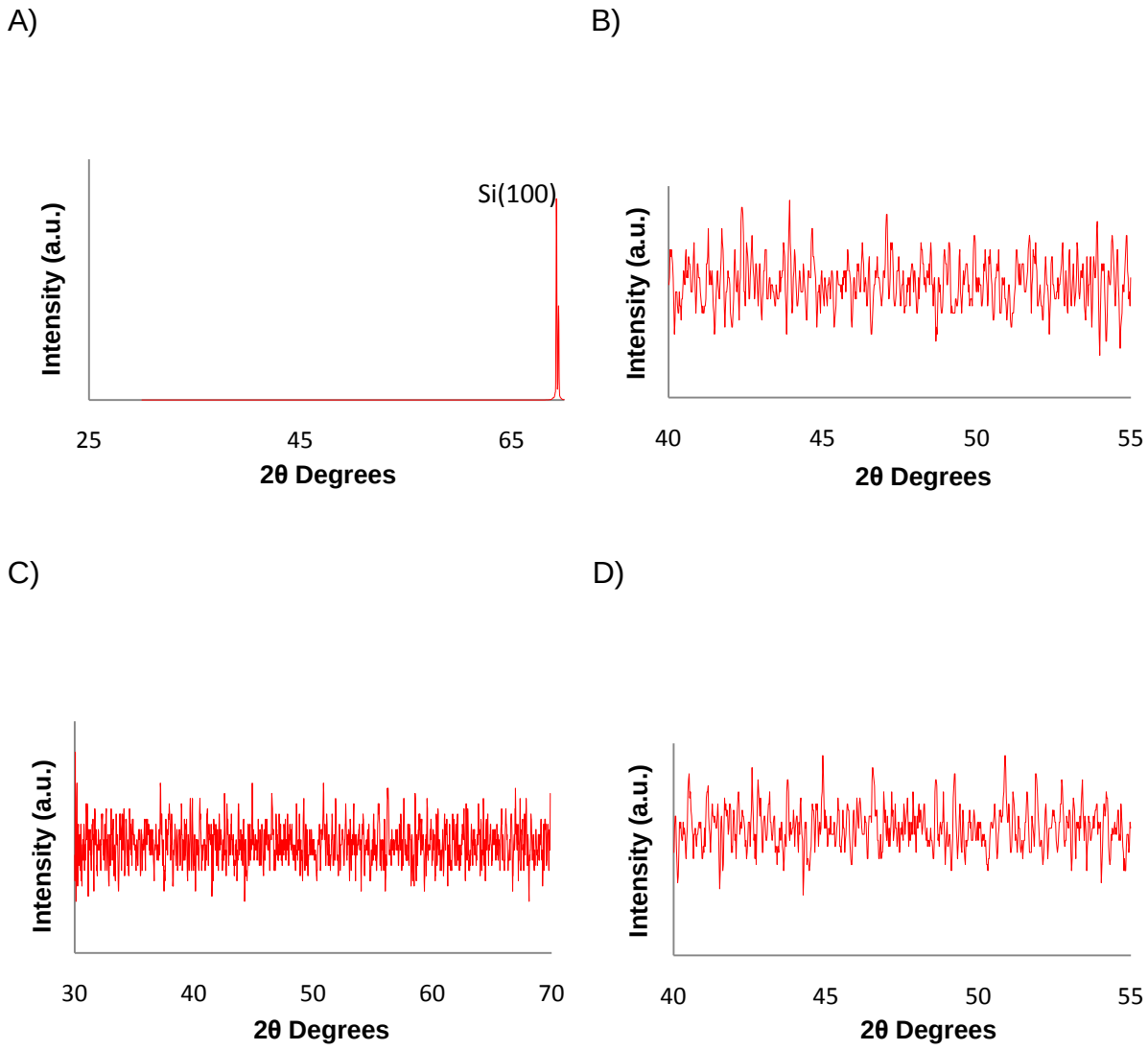


Figure 4-2. XRD spectra for sputtered W_2N on different Si substrates. A) Si(100) with scanning range from 25 to 70 2θ degrees. B) Si(100) with scanning range from 40 to 55 2θ degrees. C) Si(111) with scanning range from 25 to 70 2θ degrees. D) Si(111) with scanning range from 40 to 55 2θ degrees.

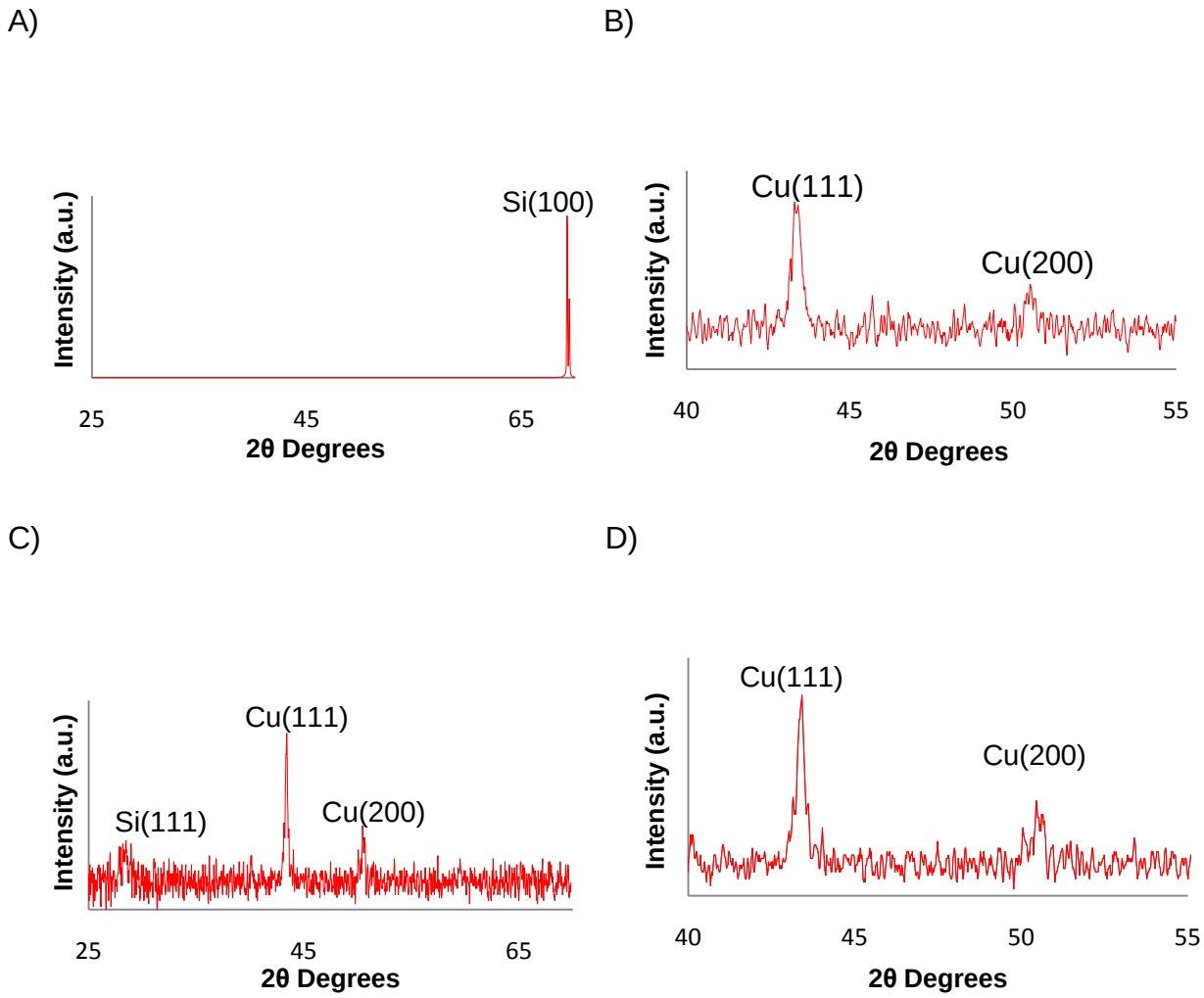


Figure 4-3. XRD spectra for Cu seed layer (MOCVD)/Ta/TaN on different Si substrates. A) Si(100) with scanning angle from 25 to 70 2θ degrees. B) Si(100) with scanning angle from 40 to 55 2θ degrees. C) Si (111) with scanning angle from 25 to 70 2θ degrees. D) Si(111) with scanning angle from 40 to 55 2θ degrees.

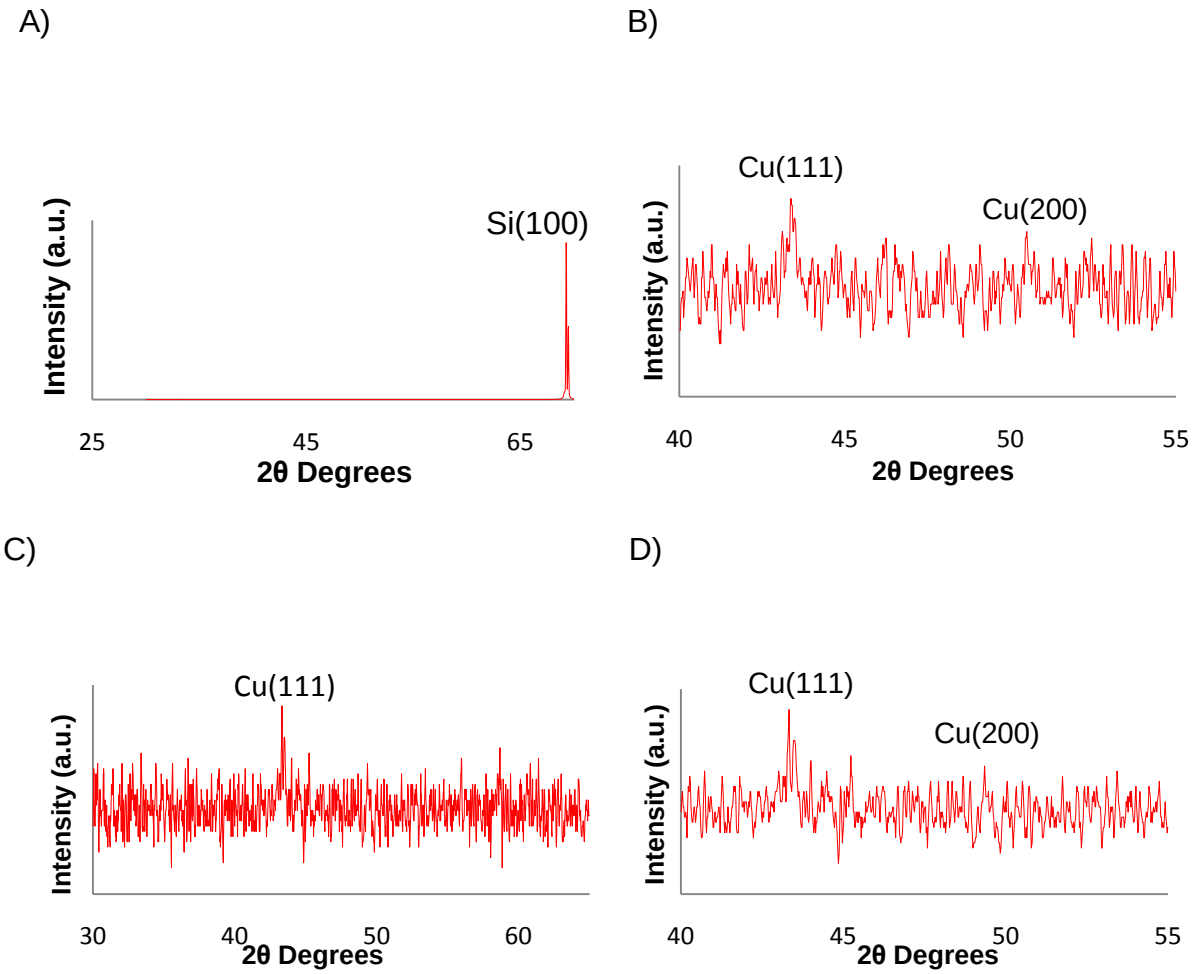


Figure 4-4. XRD spectra for Cu seed layer deposited by MOCVD on W_2N/Si(100) and W_2N/Si(111). A) W_2N/Si(100) with scanning angle from 25 to 70 2θ degrees. B) W_2N/Si(100) with scanning angle from 40 to 55 2θ degrees. C) W_2N/Si(111) with scanning angle from 30 to 65 2θ degrees. D) W_2N/Si(111) with scanning angle from 40 to 55 2θ degrees.

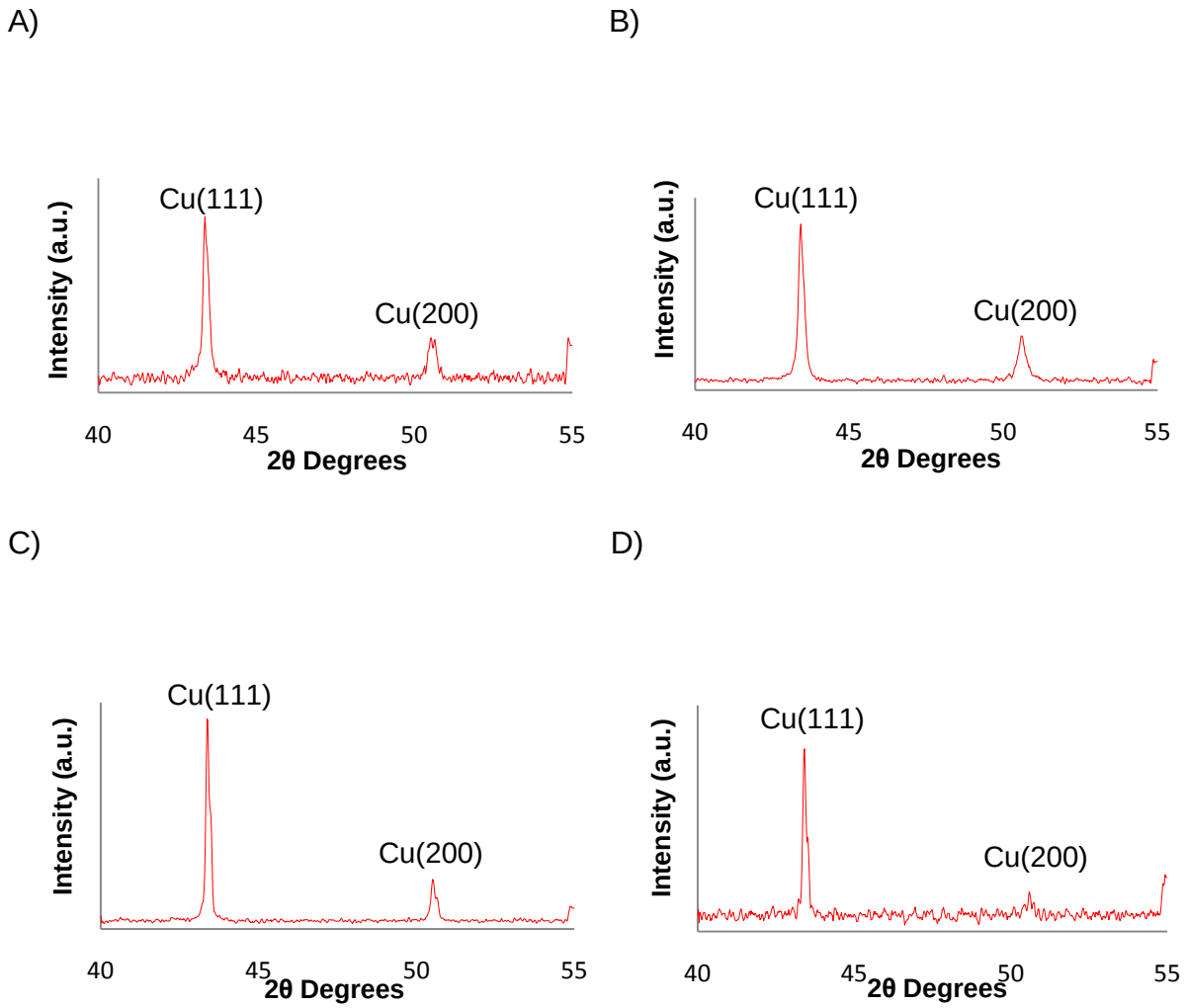


Figure 4-5. XRD spectra for electroplated (EP) Cu/Cu seed layer (MOCVD)/diffusion barriers/different Si substrates. A) Ta/TaN/Si(100) with scanning angle from 40 to 55 2θ degrees. B) Ta/TaN/Si(111) with scanning angle from 40 to 55 2θ degrees. C) W_2N/Si(100) with scanning angle from 40 to 55 2θ degrees. D) W_2N/Si(100) with scanning angle from 40 to 55 2θ degrees.

Table 4-1. Estimated grain size of MOCVD Cu seed layer/Ta/TaN on Si(100) and Si(111)

Ta/TaN	FWHM	2θ	Grain size (nm)
Cu seed layer/Ta/TaN/Si(100)	0.236	43.354	36.2
Cu seed layer/Ta/TaN/Si(111)	0.157	43.383	54.4

Table 4-2. Estimated grain size of MOCVD Cu seed layer/W_2N on Si(100) and Si(111)

W_2N	FWHM	2θ	Grain size (nm)
Cu seed layer/W_2N/Si(100)	0.157	43.459	54.4
Cu seed layer/W_2N/Si(111)	0.118	43.453	72.4

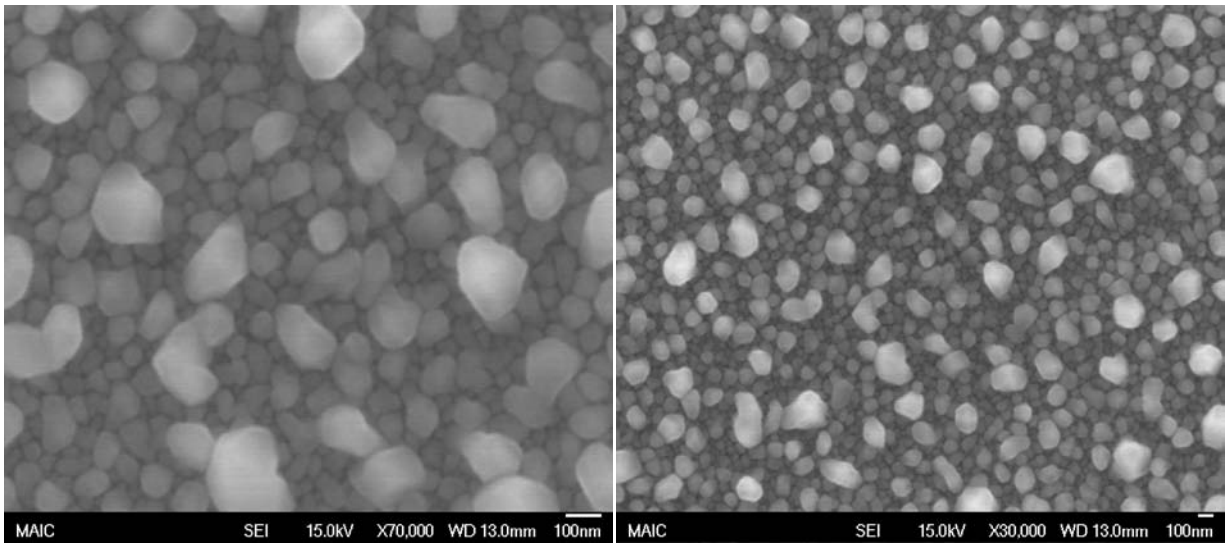
Table 4-3. Estimated grain size of EP Cu/Cu seed layer (MOCVD)/Ta/TaN on Si(100) and Si(111)

Ta/TaN	FWHM	2θ	Grain size (nm)
EP Cu/Cu seed layer/Ta/TaN/Si(100)	0.118	43.35	72.4
EP Cu/Cu seed layer/Ta/TaN/Si(111)	0.138	43.41	61.9

Table 4-4. Estimated grain size of EP Cu/Cu seed layer (MOCVD)/W_2N on Si(100) and Si(111)

W_2N	FWHM	2θ	Grain size (nm)
EP Cu/Cu seed layer/W_2N/Si(100)	0.096	43.37	89.0
EP Cu/Cu seed layer/W_2N/Si(111)	0.098	43.40	87.2

A) B)



C) D)

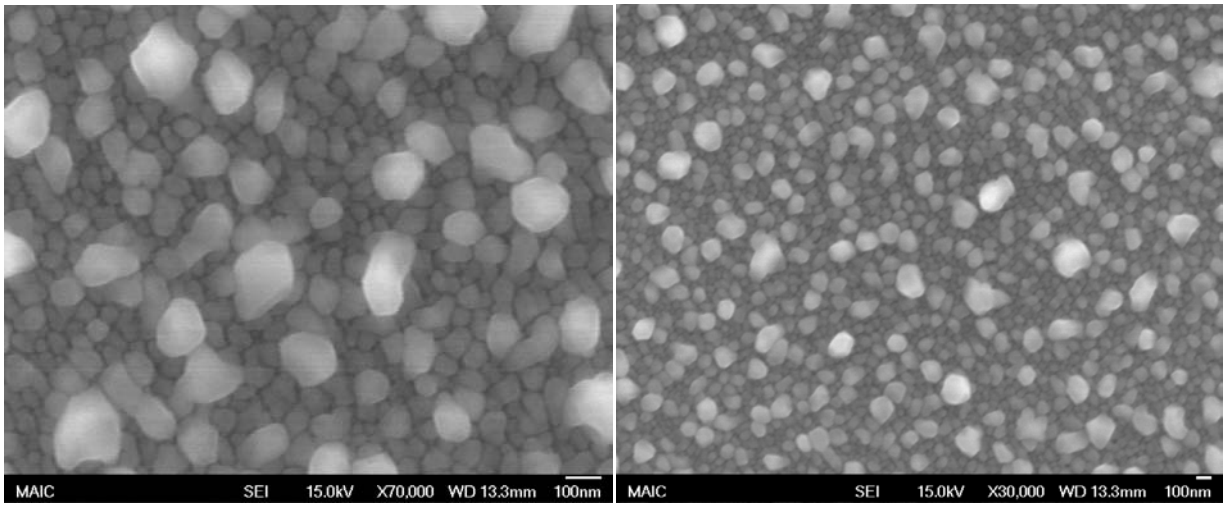


Figure 4-6. SEM images of Cu seed layer (MOCVD)/Ta/TaN on different Si substrates. A) Si(100) X70,000. B) Si(100) X30,000. C) Si(111) X70,000. D) Si(111) X30,000.

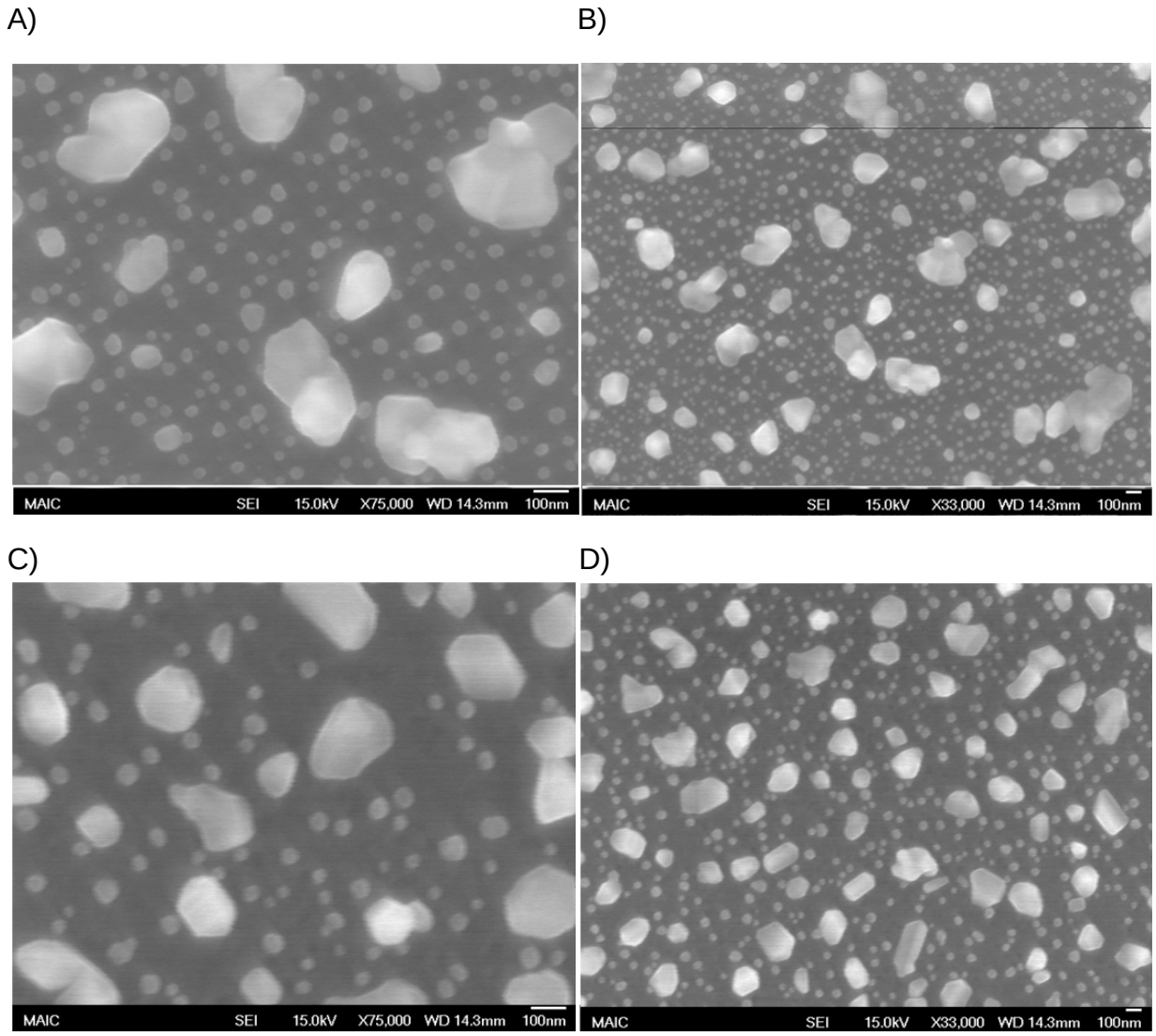


Figure 4-7. SEM images of Cu seed layer (MOCVD)/W_2N on different Si substrates. A) Si(100) X70,000. B) Si(100) X30,000. C) Si(111) X70,000. D) Si(111) X30,000.

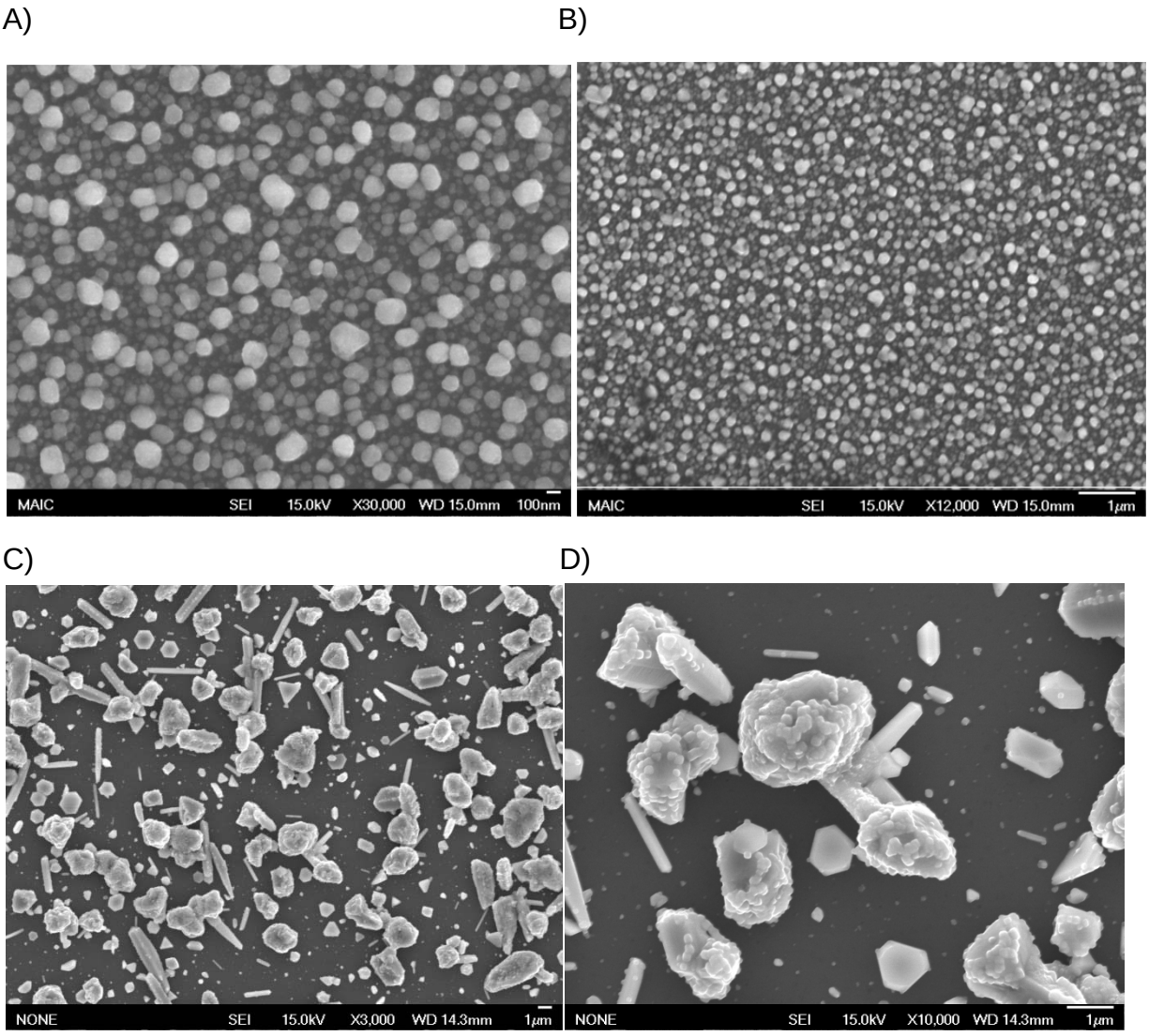
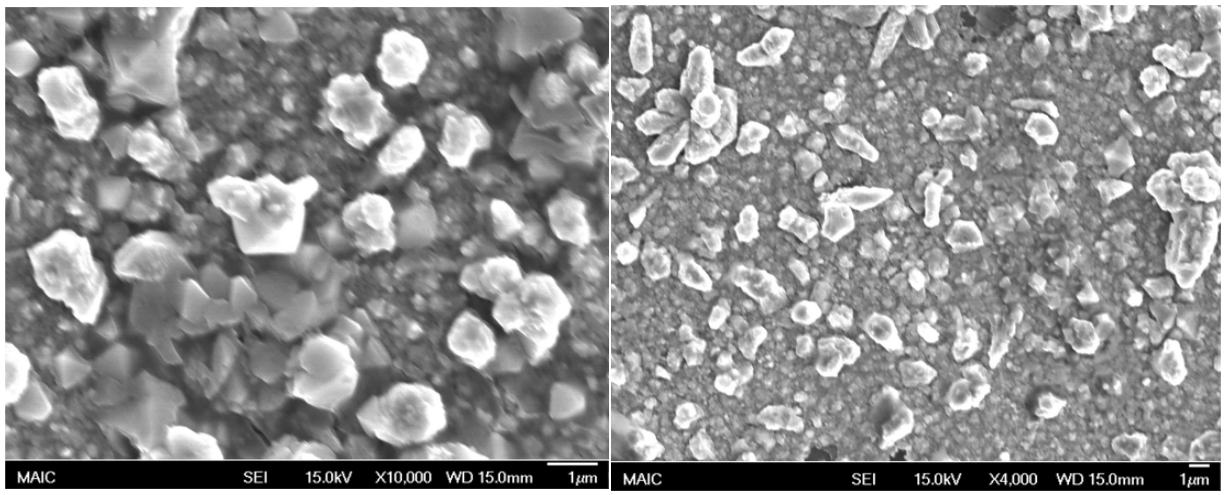


Figure 4-8. SEM images of EP Cu/Cu seed layer (MOCVD)/Ta/TaN on different Si substrates. A) Si(100) X30,000. B) Si(100) X12,000. C) Si(111) X30,000. D) Si(111) X12,000.

A) B)



C) D)

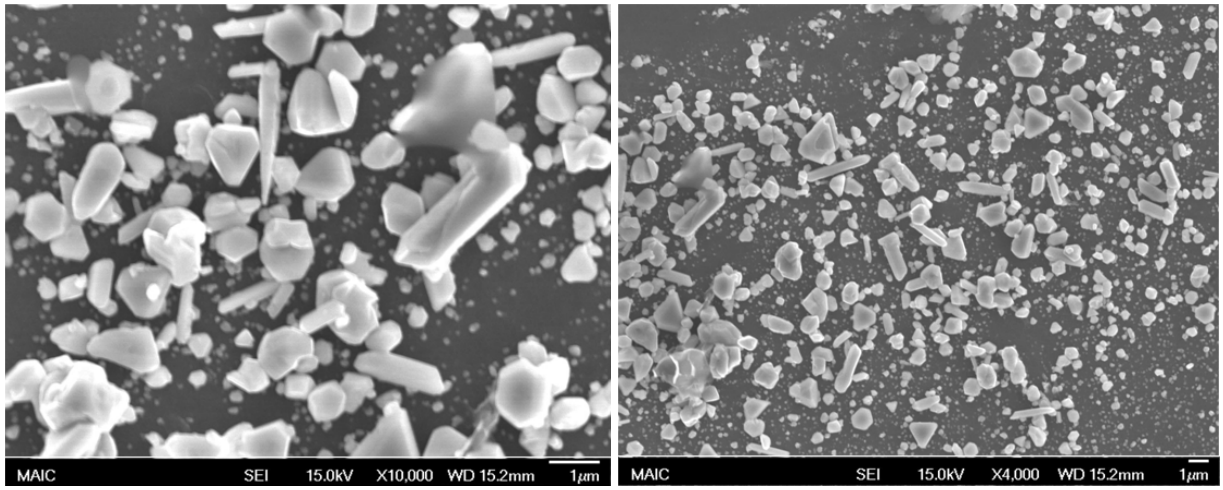


Figure 4-9. SEM images of EP Cu/Cu seed layer (MOCVD)/W_2N on different Si substrates. A) Si(100) X30,000. B) Si(100) X10,000. C) Si(111) X30,000. D) Si(111) X12,000.

Table 4-5. Film resistivity of Ta/TaN and W_2N on Si(100) and Si(111)

	Film resistivity (μΩ-cm)
Ta/TaN/Si(100)	0.455
Ta/TaN/Si(111)	0.473
W_2N/Si(100)	312
W_2N/Si(111)	446

Table 4-6. Film resistivity of Cu seed layer (MOCVD) on Ta/TaN/Si(100) and Ta/TaN/Si(111)

Ta/TaN	1	2	3	4	5	average resistivity	(μΩ-cm)
Cu seed layer/Ta/TaN/Si(100) (mΩ)	67.5	65.3	62.4	68.8	61.3	65.06	0.455
Cu seed layer/Ta/TaN/Si(111) (mΩ)	67.2	65.3	67.5	71.3	67.1	67.68	0.474

Table 4-7. Film resistivity of Cu seed layer (MOCVD) on Ta/TaN/Si(100) and Ta/TaN/Si(111)

W_2N	1	2	3	4	5	average	resistivity (μΩ-cm)
Cu seed layer/W_2N/Si(100) (mΩ)	74.9	74.3	61.6	69.6	65	69.1	0.484
Cu seed layer/W_2N/Si(111) (mΩ)	130	162	117	114.8	122.2	129.2	0.904

Table 4-8. Adhesion test for Cu seed layers deposited on different types of Si substrates

Ta/TaN	
Cu seed layer (MOCVD)/Ta/TaN/Si(100)	fail
Cu seed layer (MOCVD)/Ta/TaN/Si(111)	fail
W_2N	
Cu seed layer (MOCVD)/W_2N/Si(100)	fail
Cu seed layer (MOCVD)/W_2N/Si(111)	fail

Table 4-9. Adhesion test for EP Cu on different types of Si substrates

Ta/TaN	
EP Cu/Cu seed layer (MOCVD)/Ta/TaN/Si(100)	fail
EP Cu/Cu seed layer (MOCVD)/Ta/TaN/Si(111)	fail
W_2N	
EP Cu/Cu seed layer (MOCVD)/W_2N/Si(100)	fail
EP Cu/Cu seed layer (MOCVD)/W_2N/Si(111)	fail

CHAPTER 5
DIFFUSION BARRIER EFFECTS ON MOCVD DEPOSITED COPPER SEED LAYER, AND ELECROPLATED COPPER

Four different refractory metal systems (i.e. Ta, TaN, Ta/TaN, and W_2N) were used as diffusion barriers. All of them were deposited by sputtering onto Si(100) substrates following the same recipes described previously. Cu seed layers discussed here were deposited by metallorganic chemical vapor deposition (MOCVD) since CVD is an excellent technique for obtaining uniform step coverage on small feature sizes. Diffusion barrier effectiveness on MOCVD deposited Cu seed layer and the subsequent electroplated Cu fill were examined with respect to their texture, grain size, surface morphology, film resistivity, and strength of adhesion after deposition.

5.1 X-Ray Diffraction Measurement

5.1.1 Film Crystallinity

XRD spectra were obtained for all four diffusion barriers deposited on Si(100). XRD spectra for Ta, TaN, Ta/TaN, and W_2N are shown in Figure 5-1 and Figure 5-2. The spectra were obtained for angles from 30 to 70 or 30 to 55 2θ degrees. It can be seen that except for the intense substrate peaks sitting at around 33 and 69.2 2θ degrees, no other peaks were shown. Therefore, amorphous films were obtained via sputtering.

Cu seed layers deposited by MOCVD were examined by XRD. As shown in Figure 5-3A and Figure 5-3B, the XRD spectra for MOCVD deposited Cu seed layers on Ta have peak arising at around 43.21 2θ degrees, which is indicative of Cu(111). No peak for Cu(200) is found. For Cu seed layer deposited by MOCVD onto TaN, both Cu(111) and Cu(200) peaks appear at 43.40 and 50.18 2θ degrees, respectively, as shown in Figure 5-3C and Figure 5-3D. However, the Cu(200) peak was not very distinct from the background, and the $I_{(111)}/I_{(200)}$ was calculated to be 5.4. Shown in Figure 5-4A and Figure 5-4B are the XRD spectra for MOCVD Cu seed layers deposited on Ta/TaN. For this multistack diffusion barrier system, clearly two peaks arise at 43.45 and 50.51 2θ degrees from Cu(111) and Cu(200), respectively. The $I_{(111)}/I_{(200)}$ ratio was 3.55. When W_2N was employed as a diffusion barrier, as shown in Figure 5-4C and Figure 5-4D, both peaks for Cu(111) and Cu(200) appeared. The Cu(111) peak emerged at 43.46 and the Cu(200) peak showed at 50.51 2θ degrees and the calculated $I_{(111)}/I_{(200)}$ ratio was 1.79.

The Cu seed layer deposited by MOCVD therefore served as a conductive path for electrons. Cu fill was then electroplated onto Cu seed layer on various diffusion barrier systems and XRD measurements were conducted. The angles were scanned from 40 to 55 2θ degrees. The peak intensities for both Cu(111) and Cu(200) increase due to the

increase in film thickness from about one hundred to several hundred nanometers. XRD spectra for them are shown in Figure 5-5. For electroplated Cu on Cu seed layer (MOCVD)/Ta/Si(100), peaks for Cu(111) and Cu(200) are shown at 43.40 and 50.57 2θ degrees, and $I_{(111)}/I_{(200)}$ was calculated to be 4.04. For electroplated Cu on MOCVD deposited Cu/TaN, two distinct peaks for Cu(111) and Cu(200) appear at 43.36 and 50.52 2θ degrees are shown on the spectra, and the $I_{(111)}/I_{(200)}$ obtained was 3.02. For electroplated Cu on MOCVD deposited Cu/Ta/TaN, peaks for Cu(111) and Cu(200) show at 43.35 and 50.52 2θ degrees, with $I_{(111)}/I_{(200)}$ equaled 4.09. For electroplated Cu on MOCVD deposited on Cu/W_2N, peaks for Cu(111) and Cu(200) are shown at 43.37 and 50.51, respectively. The $I_{(111)}/I_{(200)}$ for it was 4.75.

5.1.2 Polycrystal Grain Size

Estimates of grain sizes were determined using the Scherrer equation. Table 5-1 shows the estimated grain size of Cu seed layer (MOCVD) grown on different diffusion barriers. The grain sizes estimated for Cu seed layer (MOCVD) deposited on Ta, TaN, Ta/TaN, and W_2N are 27.1, 43.4, 36.2, and 54.4nm. Since the peaks appearing in XRD spectra for electroplated Cu were much sharper than that of Cu seed layer deposited by MOCVD, the estimated grain sizes were expected to be larger. Table 5-2 shows the grain sizes of electroplated Cu on different diffusion barrier system estimated by

Scherrer equation. For Ta used as a diffusion barrier, the estimated grain size was 87.2nm. When TaN was used, the estimated grain size was 72.4nm. For Cu electroplated onto the Ta/TaN multilayer, the estimated grain size was also 72.4nm. For the case where was W_2N used as a diffusion barrier, the estimated grain size for electroplated Cu was 89.0nm.

5.2 Scanning Electron Microscopy

Nothing was seen in SEM images for all diffusion barriers deposited here by sputtering, and possible reasons have been discussed in Chapter 4. For Cu seed layers deposited by MOCVD, SEM was used to examine the surface morphology, grain size, and grain size uniformity as shown in Figure 5-6 to Figure 5-9. The grains of Cu seed layer deposited on Ta were by and large very uniform. The average grain size obtained from averaging five diameters of grains in the sample was about 70nm. Grains of Cu seed layer by MOCVD on TaN were not so sphere-like, instead their shapes were irregular. The average grain size for these were more than 90nm. For Ta/TaN, there seemed to be two groups of different size grains of Cu seed layer formed on top of the diffusion barrier system. The larger ones had diameter about 1.5 times that of the smaller ones. The size of the smaller grains was about 70nm, and that of the other was about 110nm. Grain size variation came to an extreme when W_2N was used as a diffusion

barrier. In this case, two groups of grain sizes were found; one with a grain size of around 20nm and the other with a grain size of 200nm. It should also to be noted that grains of the Cu seed layer deposited by MOCVD were loosely seated on the diffusion barrier, and the Cu film was therefore not continuous.

For bulk Cu electroplated on various kinds of diffusion barriers, grain sizes seemed to be less uniform than seed layer Cu as shown in the SEM images (Figure 5-10 to Figure 5-13). When Ta was employed as a diffusion barrier, small features were seen in the bulk Cu while the grain boundaries were not very clear and the grain size was hard to determine. When TaN was used, two definite groups of bulk Cu grain sizes were obtained. The grain size of the smaller grain group was about 100nm whereas the grain size of the larger group was more than 1μm. The larger grains were densely populated on top of the smaller ones. The grain size of electroplated Cu on Ta/TaN was different since the grain size was relatively more uniform compared to that in other cases. The grain size of the electroplated Cu was about 100nm. When W_2N was used, still two groups of different size grains were observed; one with grains larger than 1μm on top of the other one with smaller grains underneath.

5.3 Four Point Probe Measurement

Table 5-4 shows the sheet resistance and film resistivity of Cu seed layers deposited on diffusion barriers. The deposition time for diffusion barrier layers was set such that the film thicknesses for TaN, Ta, Ta/TaN, and W_2N 25nm, 25nm, 20nm/25nm, and 30nm, respectively. The thickness of the Cu seed layer deposited by MOCVD was 70nm.

The sheet resistance for Cu seed layer deposited on Ta was 94.04mΩ, and the corresponding film resistivities were 0.66μΩ-cm. The average sheet resistance of sputtering deposited Cu seed layer on TaN was 97.72mΩ, and its film resistivity was 0.68μΩ-cm. The film resistivity of Cu on Ta/TaN was 0.46μΩ-cm. The measured film resistivity for Cu film on W_2N/Si(100) was 0.48μΩ-cm.

5.4 Scotch® Brand Tape Test

Adhesion strength of Cu seed layers deposited by MOCVD and EP Cu films to their underlying layers were compared with respect to different diffusion barriers used. The results are listed in Table 5-5 and Table 5-6. Generally neither Cu seed layers nor EP Cu showed strong adhesion performance, Cu was more or less removed by the tapes after tests. Peeling of EP Cu happened when EP Cu was deposited on TaN.

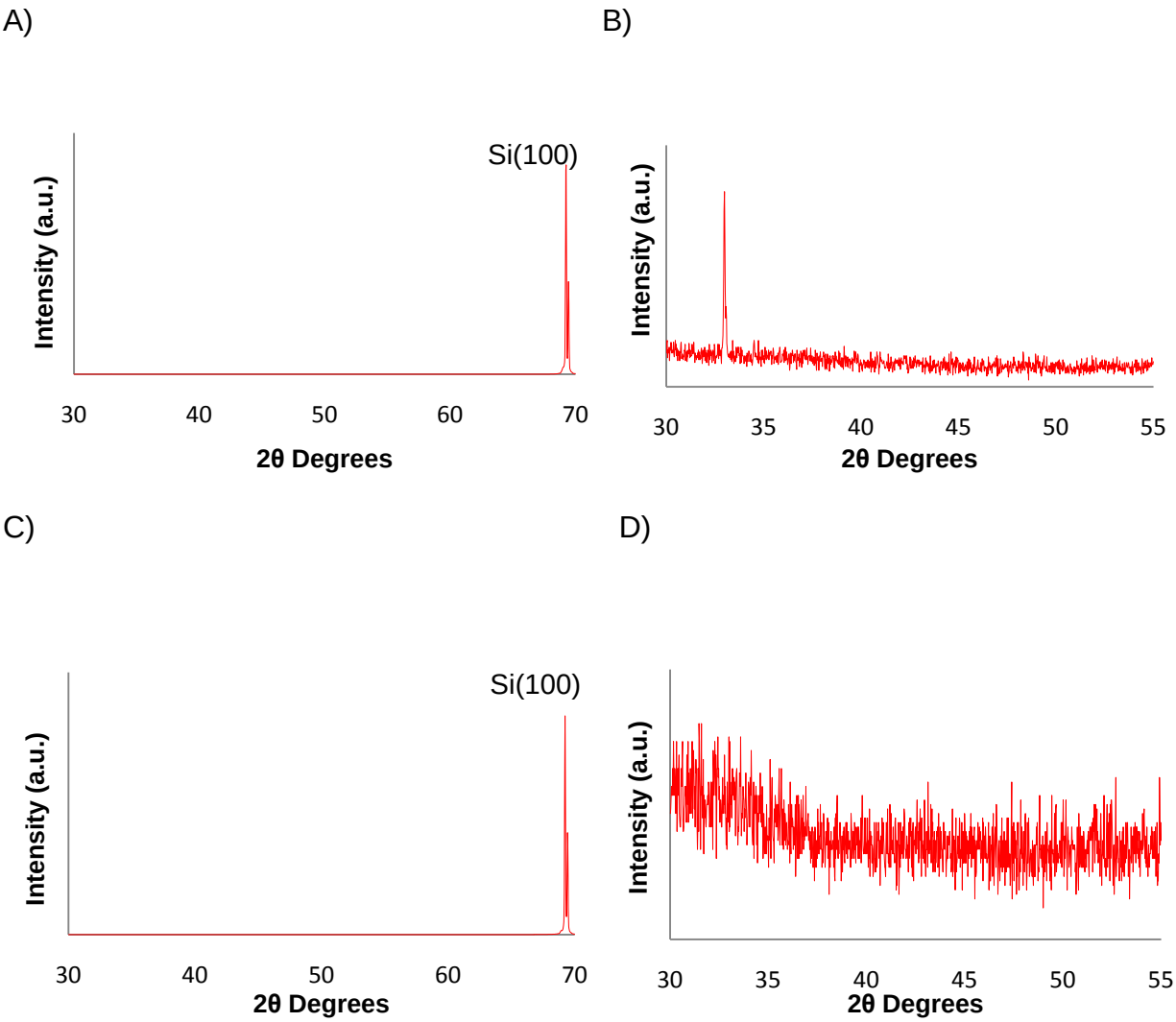


Figure 5-1. XRD spectra of A), B) Ta on Si(100). C), D) TaN on Si(100).

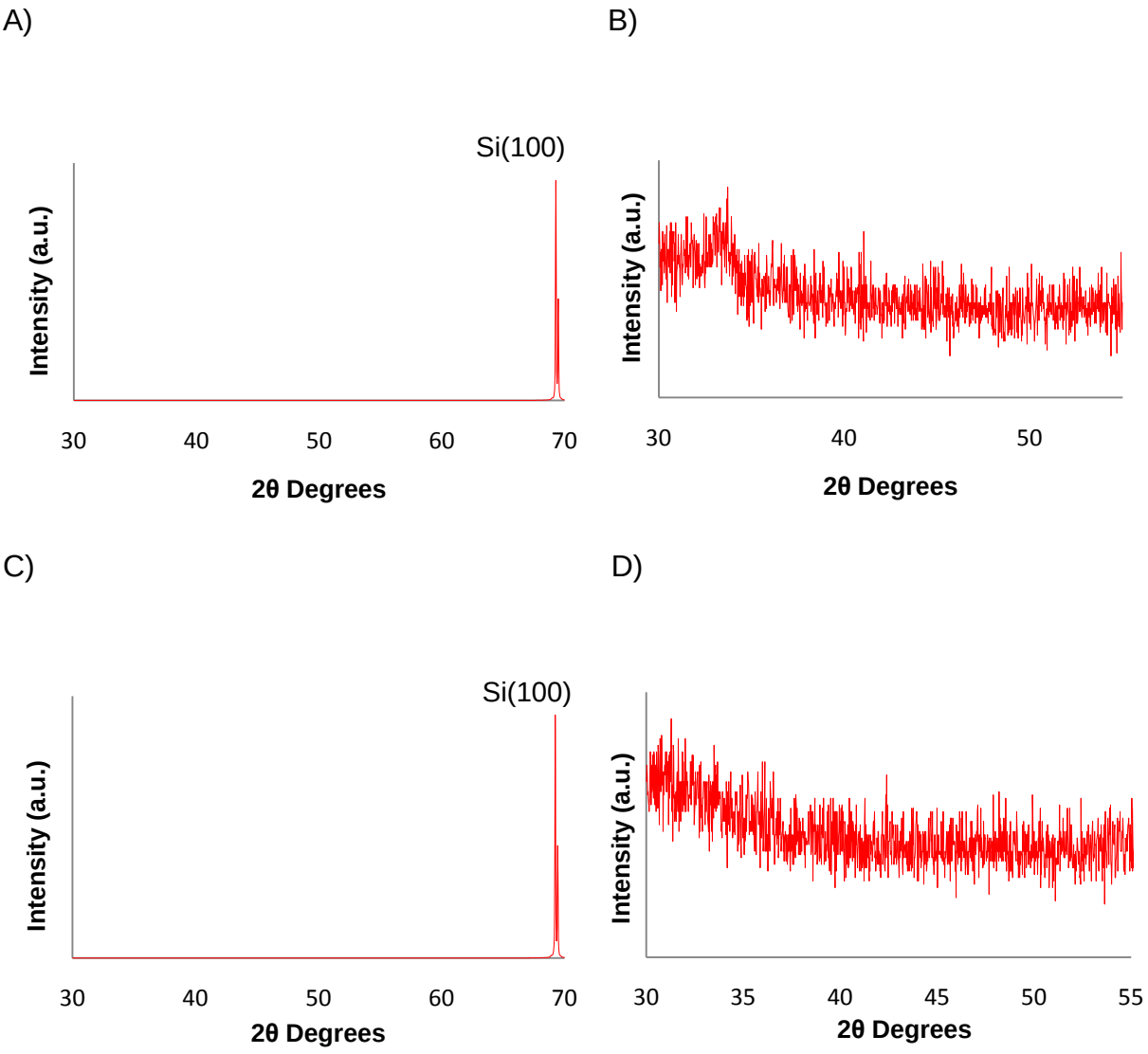


Figure 5-2. XRD spectra of A), B) Ta/TaN on Si(100). C), D) W_2N/Si(100).

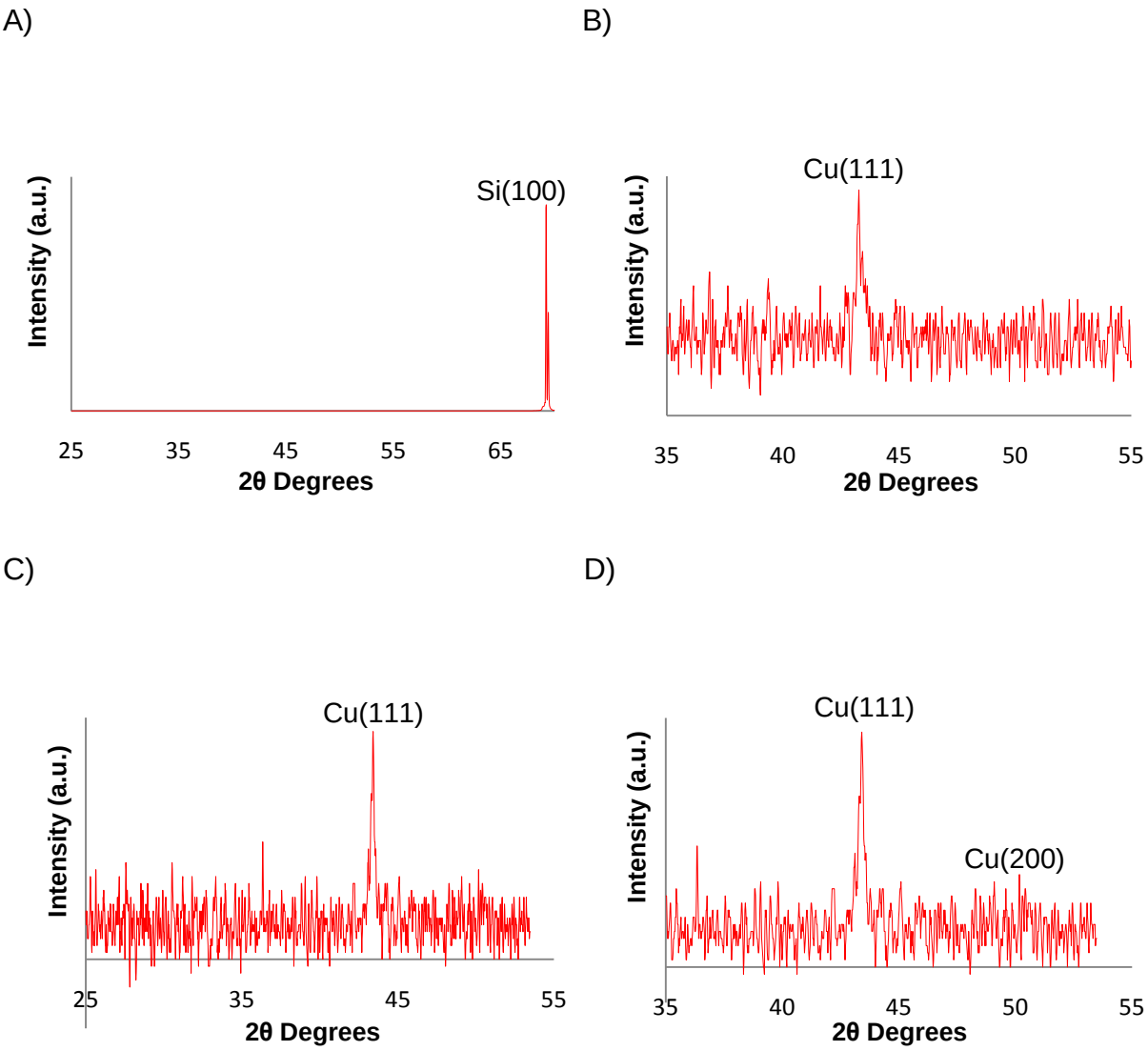


Figure 5-3. XRD spectra of A), B) Cu seed layer (MOCVD)/Ta/Si(100). C),D) Cu seed layer (MOCVD)/TaN/Si(100).

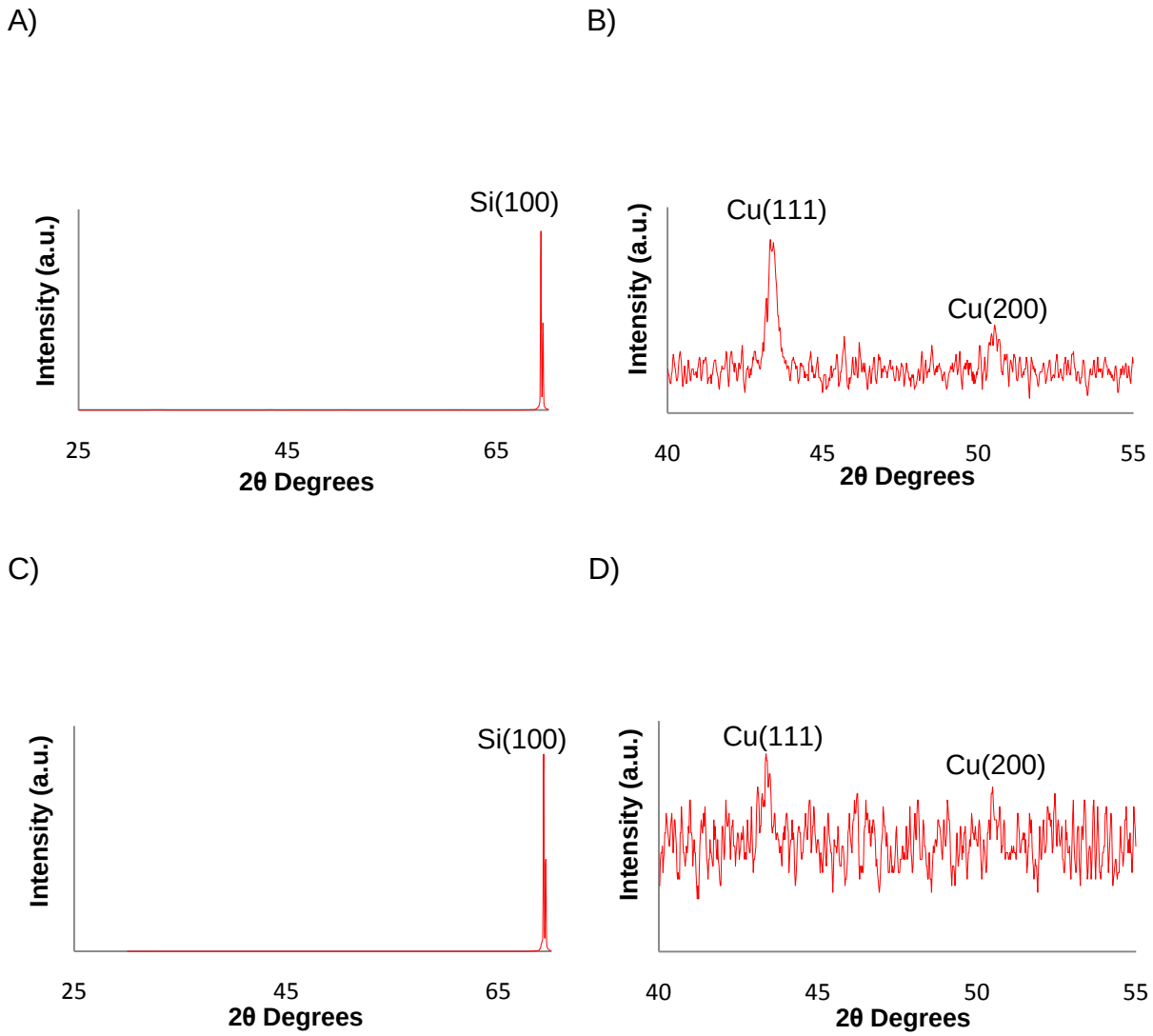


Figure 5-4. XRD spectra of A), B) Cu seed layer (MOCVD)/Ta/TaN/Si(100). C), D) Cu seed layer (MOCVD)/W_2N/Si(100).

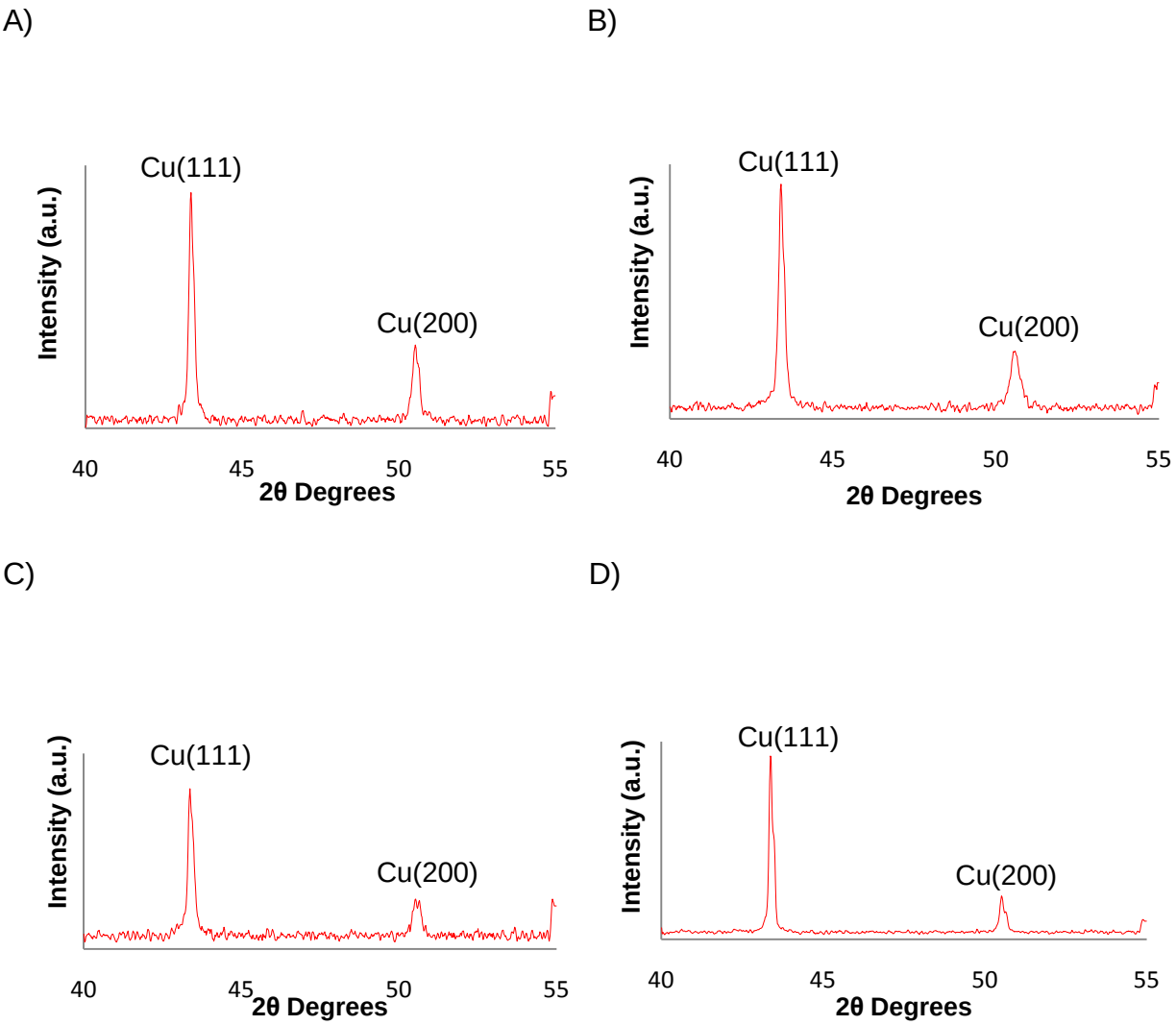


Figure 5-5. EP Cu on Cu seed layer (MOCVD) on diffusion barriers/Si(100). A) TaN. B) Ta. C) Ta/TaN. D) W_2N.

Table 5-1. Estimated grain size of Cu seed layer (MOCVD) deposited on diffusion barriers/Si(100)

Ta	FWHM	2θ	Grain size (nm)
Cu seed layer/Ta/Si(100)	0.315	43.21	27.1
TaN	FWHM	2θ	Grain size (nm)
Cu seed layer/TaN/Si(100)	0.197	43.40	43.3
Ta/TaN	FWHM	2θ	Grain size (nm)
Cu seed layer/Ta/TaN/Si(100)	0.236	43.35	36.2
W_2N	FWHM	2θ	Grain size (nm)
Cu seed layer/W_2N/Si(100)	0.157	43.46	54.4

Table 5-2. Estimated grain size of EP Cu/Cu seed layer (MOCVD)/diffusion barriers/Si (100)

Ta	FWHM	2θ	Grain size (nm)
EP Cu/CVD Cu seed/Ta/Si(100)	0.098	43.40	87.2
TaN	FWHM	2θ	Grain size(nm)
EP Cu/CVD Cu seed/TaN/Si(100)	0.118	43.36	72.4
Ta/TaN	FWHM	2θ	Grain size(nm)
EP Cu/CVD Cu seed/Ta/TaN/Si(100)	0.118	43.35	72.4
W_2N	FWHM	2θ	Grain size(nm)
EP Cu/CVD Cu seed/W_2N/Si(100)	0.096	43.37	89.0

A) B)

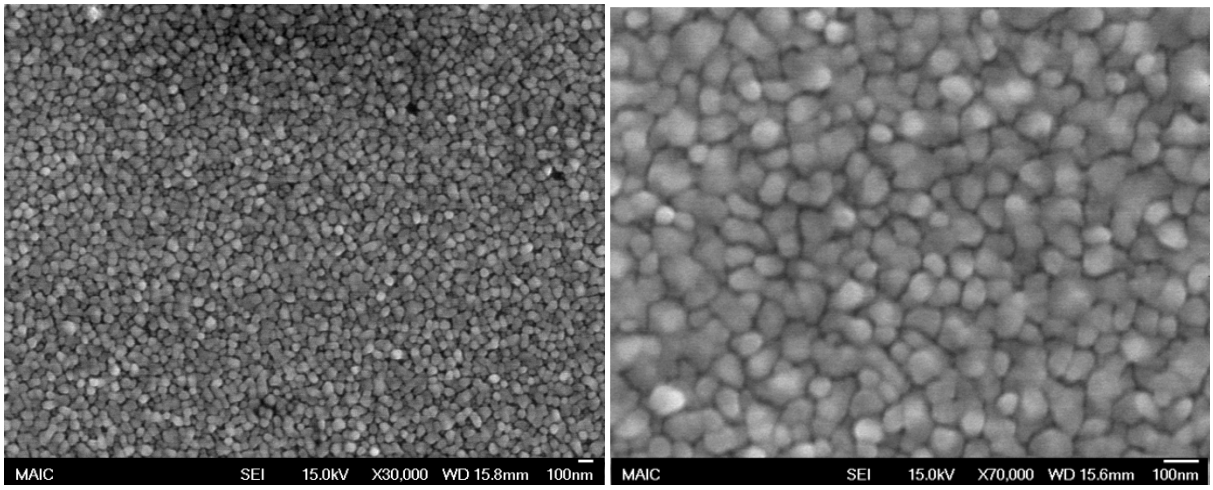


Figure 5-6. SEM images of Cu seed layer (MOCVD) on TaN/Si(100). A) X30,000. B) X70,000.

A) B)

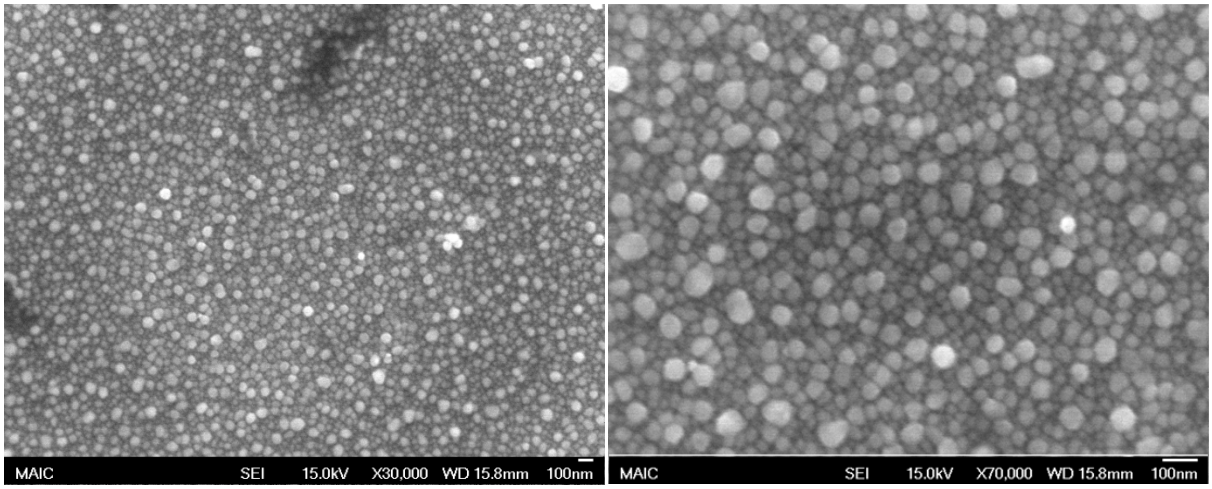


Figure 5-7. SEM images of Cu seed layer (MOCVD) on Ta/Si(100). A) X30,000. B) X70,000.

A) B)

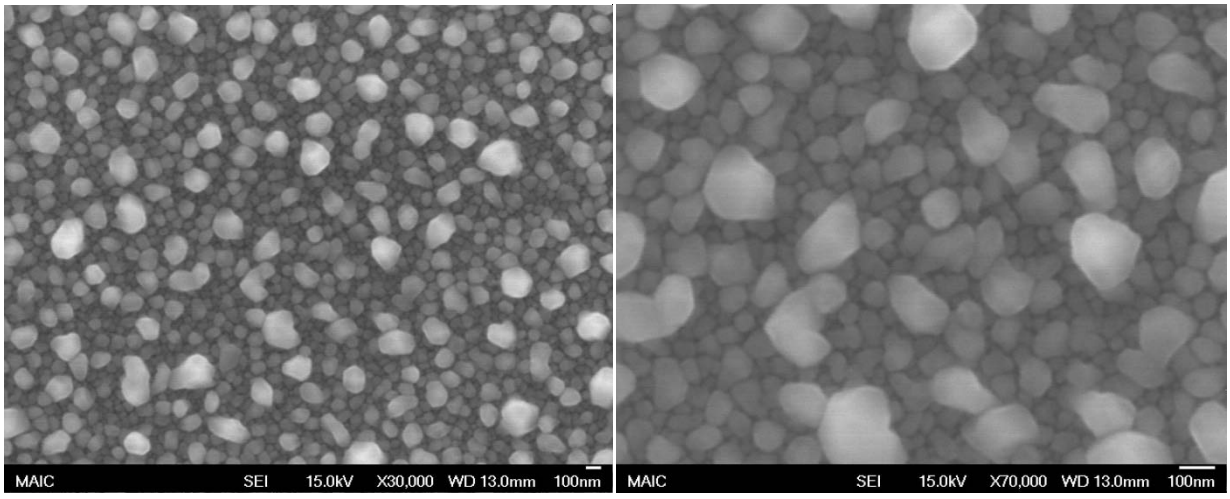


Figure 5-8. SEM images of Cu seed layer (MOCVD) on Ta/TaN/Si(100). A) X30,000. B) X70,000.

A) B)

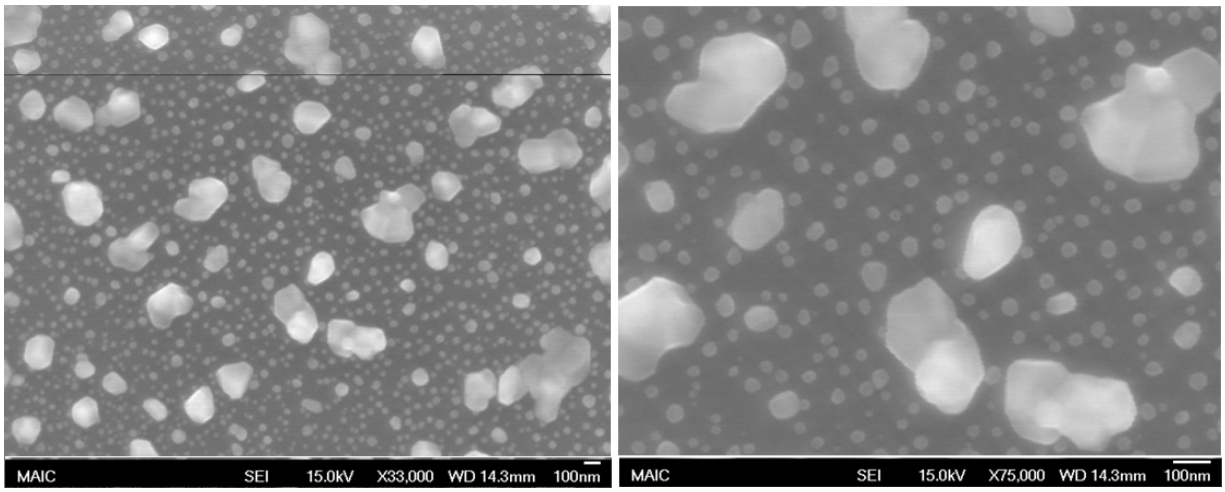


Figure 5-9. SEM images of Cu seed layer (MOCVD) on W_2N/Si(100). A) X30,000. B) X70,000.

A) B)

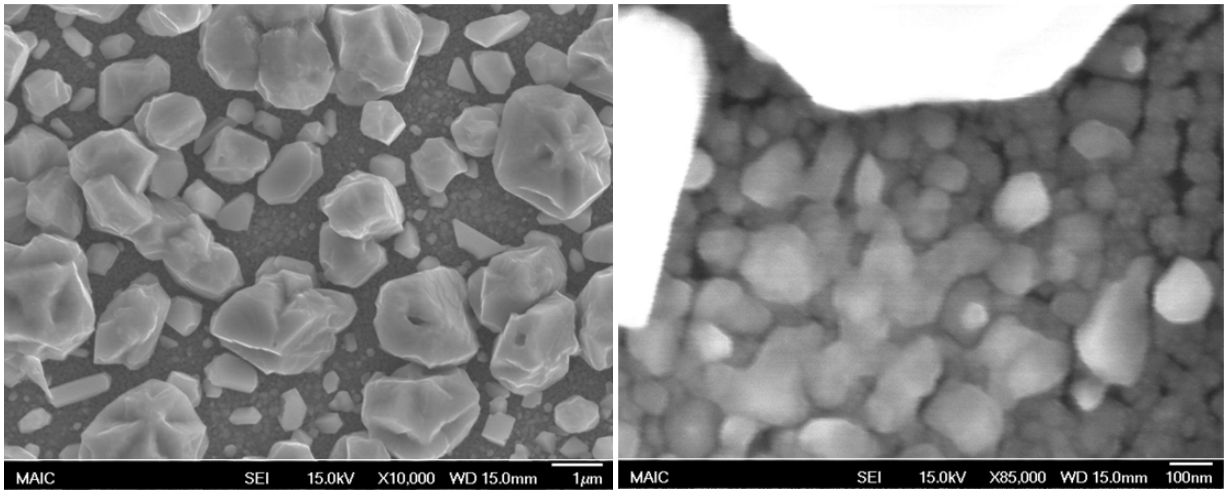


Figure 5-10. SEM images of EP Cu/Cu seed layer (MOCVD) deposited on TaN/Si(100). A) X10,000. B) X85,000.

A) B)

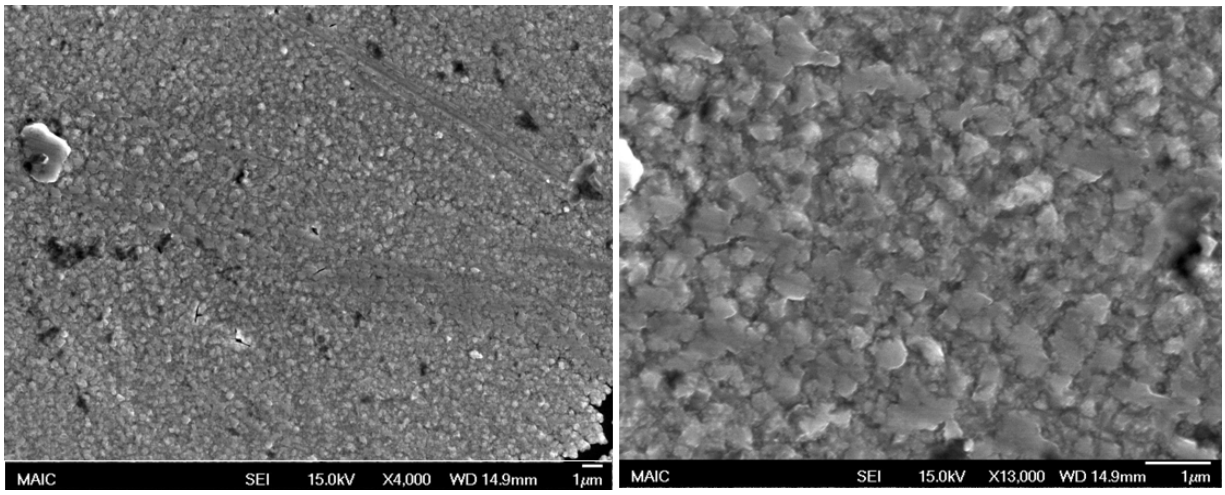


Figure 5-11. SEM images of EP Cu/Cu seed layer (MOCVD) deposited on Ta/Si(100). A) X4,000. B) X13,000.

A) B)

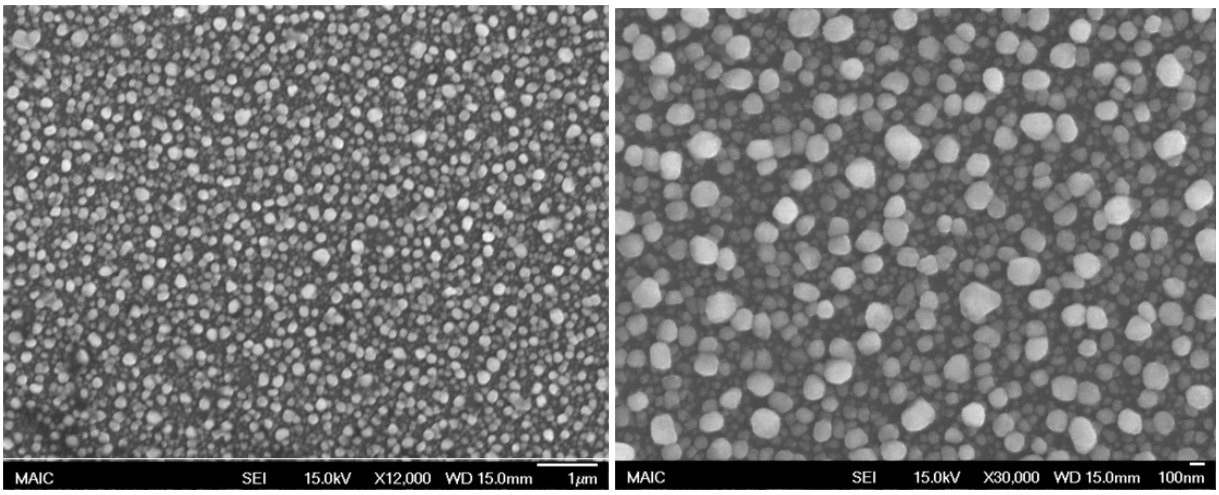


Figure 5-12. SEM images of EP Cu/Cu seed layer (MOCVD) deposited on Ta/TaN/Si (100). A) X12,000, B) X30,000.

A) B)

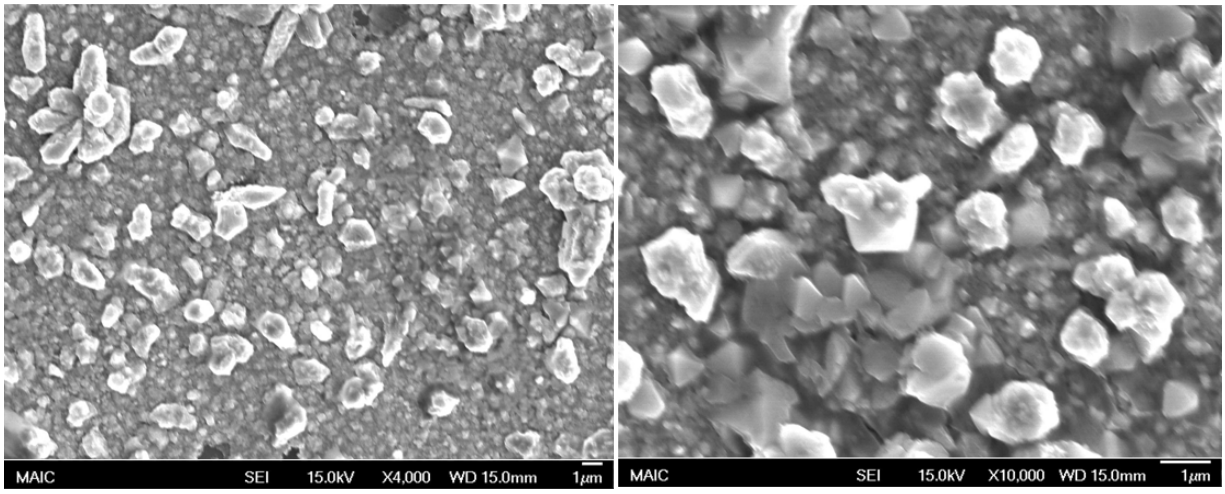


Figure 5-13. SEM images of EP Cu/Cu seed layer (MOCVD) deposited on W_2N/Si(100). A) X4,000. B) X10,000.

Table 5-3. Film resistivity of Cu seed layers (MOCVD) on diffusion barriers/Si(100)

	1	2	3	4	5	average (mΩ)	resistivity (μΩ-cm)
TaN							
Cu seed layer/TaN/Si(100)	105	99	100	88	94	97.72	0.684
Ta							
Cu seed layer /Ta/Si(100)	91	100	92	91	93	94.04	0.658
Ta/TaN							
Cu seed layer/Ta/TaN/Si(100)	67	65	62	68	61	65.06	0.455
W_2N							
Cu seed layer/W_2N/Si(100)	74	74	61	69	65	69.08	0.484

Table 5-4. Adhesion test for Cu seed layer deposited on different diffusion barriers

Ta	Tape test
Cu seed layer (MOCVD)/Ta/Si(100)	Fail
TaN	
Cu seed layer (MOCVD)/TaN/Si(100)	Fail
Ta/TaN	
Cu seed layer (MOCVD)/Ta/TaN/Si(100)	Fail
W_2N	
Cu seed layer(MOCVD)/W_2N/Si(100)	Fail

Table 5-5. Adhesion test for EP Cu deposited on Cu seed layer (MOCVD)/ different diffusion barriers

Ta	Tape test
EP Cu/Cu seed layer (MOCVD)/Ta/Si(100)	fail
TaN	
EP Cu/Cu seed layer (MOCVD)/TaN/Si(100)	fail
Ta/TaN	
EP Cu/Cu seed layer (MOCVD)/Ta/TaN/Si(100)	fail
W_2N	
EP Cu/Cu seed layer(MOCVD)/W_2N/Si(100)	fail

CHAPTER 6
DEPOSITION TECHNIQUE EFFECTS ON MOCVD DEPOSITED COPPER SEED LAYER, AND ELECTROPLATED COPPER

Physical vapor deposition (PVD) has been used successfully for thin film deposition in the IC industry. However, PVD is no longer an acceptable method of deposition for future miniaturized integrated circuits (ICs) since it is a line-of-sight deposition method, which results in poor step coverage of high aspect ratio features. CVD is now the predominant method used in industry for thin film deposition as it has been shown to have excellent step coverage. Film properties vary when different deposition methods are employed, therefore this part of the work was aimed at exploring the difference in film properties between Cu seed layers deposited by sputtering and MOCVD. The deposition method effects on the subsequent electroplated Cu films were examined as well.

PVD and MOCVD were used to deposit Cu seed layers on two different substrates (e.g. Ta/TaN and W_2N) on Si(100). Electrochemical deposition was then used to deposit thicker Cu films onto those Cu seed layers. Film properties were readily examined by different techniques.

6.1 X-Ray Diffraction Measurement

6.1.1 Film Crystallinity

Figure 6-1 shows the background corrected XRD in the case where Cu seed layer were deposited by MOCVD or sputtering onto Ta/TaN/Si(100). The ratio of $I_{(111)}/I_{(200)}$ was 3.55 for Cu seed layer deposited by MOCVD. In the case where Cu seed layer was deposited by sputtering, the ratios of $I_{(111)}/I_{(200)}$ increased to 6.93.

Figure 6-2 shows XRD spectra for Cu seed layers deposited by MOCVD and sputtering when W_2N was grown as a diffusion barrier. The crystal orientation of the Cu seed layer has to be discussed in a different way. The $I_{(111)}/I_{(200)}$ ratio was 1.79 for Cu seed layer grown by MOCVD. In the case where Cu seed layer was deposited by sputtering, the (200) peak seemed to be immersed in the background noise, and only the (111) peak appeared. Since the sputtered Cu seed layer had a stronger (111) peak, it is a better choice over Cu seed layer deposited by MOCVD in terms of crystallographic orientation.

The texture of electroplated Cu on two groups of Cu seed layers was also examined in order to investigate the deposition technique effects. In the scanning range from 40 to 55 2θ degrees, almost all the samples had a very intensive Cu(111) peak emerging at around 43.35 2θ degrees and a relatively smaller Cu(200) peak appearing

at around 50.49 2θ degrees. $I_{(111)}/I_{(200)}$ was calculated for each sample to demonstrate degree of preferred (111) orientation as follows.

First, results of Cu electroplated on sputtered Cu seed layer were obtained. $I_{(111)}/I_{(200)}$ was found to be 4.09 for electroplated Cu on MOCVD Cu seed layer/Ta/TaN/Si(100).Calculated $I_{(111)}/I_{(200)}$ for electroplated Cu on sputtered Cu seed layer/Ta/TaN/Si(100) was 4.16.

When W_2N was applied as a diffusion barrier, electroplated Cu on sputtered Cu seed layer/W_2N/Si(100) had a $I_{(111)}/I_{(200)}$ of 3.64, and Cu electroplated on MOCVD Cu seed layer/W_2N/Si(100) gave $I_{(111)}/I_{(200)}$ of 4.75.

6.1.2 Polycrystal Grain Size

Estimated grain size of Cu seed layers and EP Cu are listed in Table 6-1 to Table 6-4. The grain sizes were estimated by the Scherrer equation assuming that the broadening of the peaks in the XRD spectra resulted from the crystallite grain size distribution. Again, the most intensive peak, Cu(111), at 43.3 2θ degrees, was used to determine FWHM and estimate the grain size.

For CVD deposited copper films grown on Ta/TaN double layer diffusion barrier, the average grain size was 36.2nm when Si(100) was used as the substrate. For Cu seed layer sputter-deposited onto a Ta/TaN double layer, the estimated grain size for

was quite different and was 21.7nm. When deposited on W_2N, Cu seed layer formed by MOCVD had the average grain size of 54.4nm on W_2N/Si(100). On the other hand, for sputter deposited Cu seed layer on W_2N/Si(100), the estimated grain size of Cu on W_2N/Si(100) was 27.1nm. Larger grains were obtained when the Cu seed layer was deposited by MOCVD no matter which diffusion barrier system was used.

Grain sizes of electroplated Cu fill were also estimated using the Scherrer equation. Substrate effects were examined with respect to Cu seed layer deposited by two different techniques as well. For Cu seed layer deposited by sputtering and Ta/TaN multilayer was employed as a diffusion barrier, the estimated grain size of electroplated Cu on sputtered Cu/Ta/TaN/Si(100) was 87.2nm. For Cu fill electroplated onto Cu seed layer deposited by MOCVD, grain size was calculated to be 72.4nm.

When W2N was used, estimated grain size of electroplated Cu on sputtered Cu seed layer/W_2N/Si(100) was 71.2nm. Estimated grain size of electroplated Cu on Cu seed layer deposited by MOCVD on W_2N/Si(100) was 89.0nm.

6.2 Scanning Electron Microscopy

Just for Cu seed layer grown by MOCVD, surface morphology was examined using SEM. Two magnifications, 30,000X, and 70,000X, were used to obtain the average grain size and the grain size distribution of the Cu seed layer. However, grains of Cu seed

layers deposited by sputtering would not be seen under SEM, presumably became the surface of the sputtered Cu films was too smooth and the grains were too small. SEM images of EP Cu were observed for both types of Cu seed layers (deposited either by MOCVD or sputtering).

SEM images of surface morphology for electroplated Cu were observed and are shown in Figure 6-5 and Figure 6-6. Grains of electroplated Cu were much larger than those deposited by MOCVD as discussed above. Two different sizes of grains were observed. One group of larger grains had a size around 700 to 800nm, and the other group contained smaller grains whose diameters were just few tens of nanometers. For Cu electroplated onto sputtered Cu/Ta/TaN/Si(100), grains were closely packed and their sizes were pretty uniform and were about 700nm as shown in Figure 6-5.

For W_2N as a diffusion barrier two groups of grains were observed for EP Cu grown on Cu seed layer deposited by MOCVD, but not in the sputtered Cu seed layer case. EP Cu on MOCVD Cu had high population of grains that were larger than 1μm, however, there seemed to be smaller grains everywhere. Electroplated Cu on sputtered Cu/W_2N/Si(100) was found to have uniformly and closely packed grains with size about 0.8μm.

6.3 Film Resistivity

Film resistivities were measured by four point probe. The results were obtained from averages of five measurements for each sample.

The deposition time for each diffusion barrier was set such that the film thicknesses for Ta/TaN, and W_2N were grown to 20nm/25nm, and 30nm, respectively. Since the deposition time for all experiments was fixed to be 70 minutes, the thicknesses of Cu seed layers deposited by MOCVD were all approximately 70nm. On the other hand, the expected thickness of the sputtered Cu seed layer was 100nm.The sheet resistances and their corresponding resistivities of Cu seed layer for all of the diffusion barriers used are listed in Table 6-5.

The sheet resistance of Cu seed layer deposited by MOCVD on Ta/TaN on Si(100) substrate was obtained. For Cu seed layer deposited on Ta/TaN on Si(100), the sheet resistances were 65.06mΩ. The film resistivity of Cu seed layer on Si(100) was 0.455μΩ-cm. Sheet resistance and film resistivity for sputtering deposited Cu seed layer on Ta/TaN/Si(100) was 1172mΩ and 11.72μΩ-cm, respectively.

When W_2N was deposited as diffusion barrier, difference in sheet resistance as well as resistivity was obvious. Cu seed layer deposited by MOCVD on Si(100) had a sheet resistance of 69.8mΩ. The calculated resistivities were 0.484μΩ-cm for Cu seed

layer on Si(100). The sheet resistance of sputtered Cu on W_2N/Si(100) was 1.946Ω, and the film resistivity for sputtered Cu film on W_2N/Si(100) was 19.46μΩ-cm.

6.4 Scotch® Brand Tape Test

Adhesion strength was tested by using Scotch® tape and the results are listed in Table 6-6 and Table 6-7. Cu seed layers deposited by sputtering showed very strong adhesion to the underlying layer, no matter what kind of diffusion barrier was employed. Nothing was removed by the tape and no visible change on the film surface was observed. However, for Cu seed layers deposited by MOCVD, films remained on the substrates but very small amount of Cu debris was found on the tape after the test. For EP Cu, Cu films did not adhere to the underlying films very well no matter which technique was used to deposit the Cu seed layer. Significant amounts of Cu were found on the tape after tests. Moreover, complete removal of EP Cu and its underlying layer occurred when EP Cu was deposited on sputtered Cu seed layer on Ta/TaN/Si(100).

Film resistivity of Cu seed layers showed good consistency. For both diffusion barrier systems that were employed, MOCVD Cu seed layers possessed much lower film resistivities as shown in Figure 6-11.

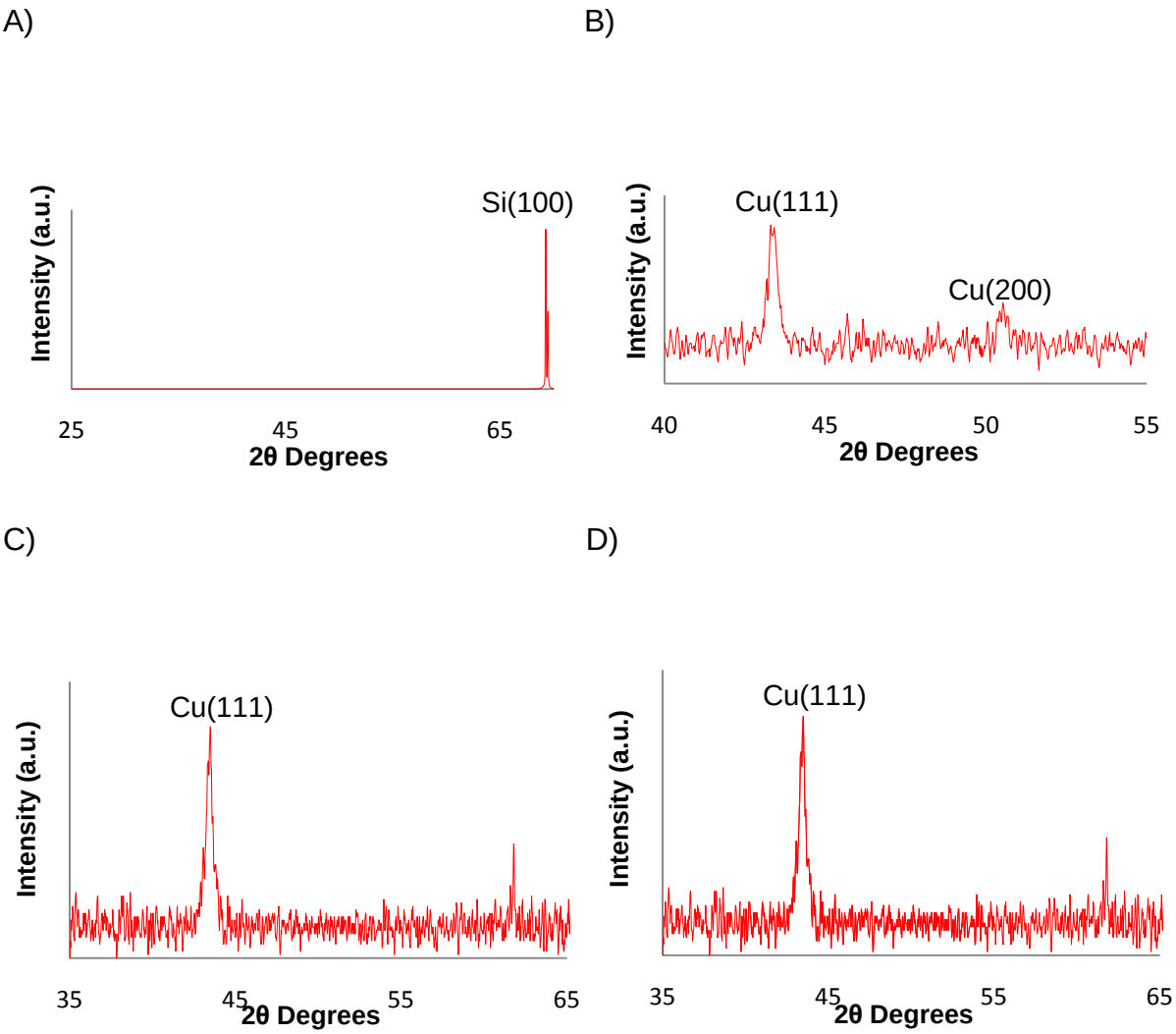


Figure 6-1. XRD spectra of Cu seed layers on Ta/TaN/Si(100). A) Cu seed layer (MOCVD) with angle scanning from 25 to 70 2θ degrees. B) Cu seed layer (MOCVD) with angle scanning from 40 to 55 2θ degrees. C) Cu seed layer (sputtering) with angle scanning from 35 to 65 2θ degrees. D) Cu seed layer (sputtering) with angle scanning from 40 to 55 2θ degrees.

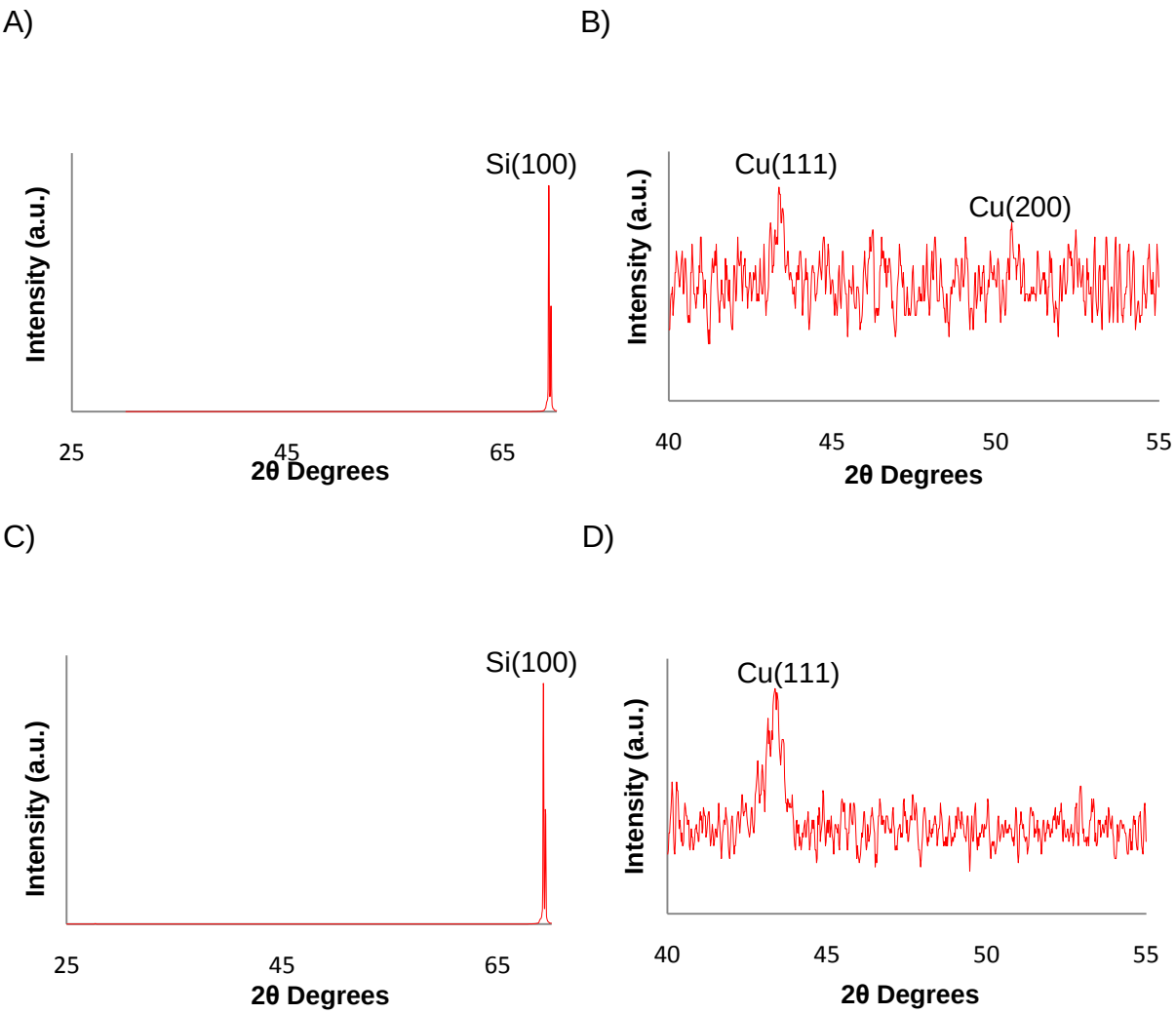


Figure 6-2. XRD spectra of Cu seed layers on W_2N/Si(100). A) Cu seed layer (MOCVD) with angle scanning from 25 to 70 2θ degrees. B) Cu seed layer (MOCVD) with angle scanning from 40 to 55 2θ degrees. C) Cu seed layer (sputtering) with angle scanning from 25 to 70 2θ degrees. D) Cu seed layer (sputtering) with angle scanning from 40 to 55 2θ degrees.

A) B)

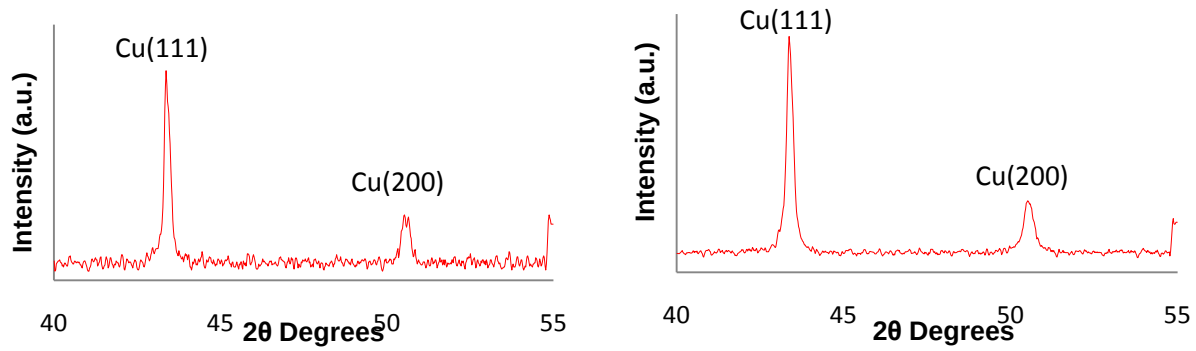


Figure 6-3. XRD spectra of EP Cu/Cu seed layer (MOCVD or sputtering)/Ta/TaN/Si (100). A) EP Cu/Cu seed layer (MOCVD)/Ta/TaN/Si(100), B) EP Cu/sputtered Cu seed layer/Ta/TaN/Si(100)

A) B)

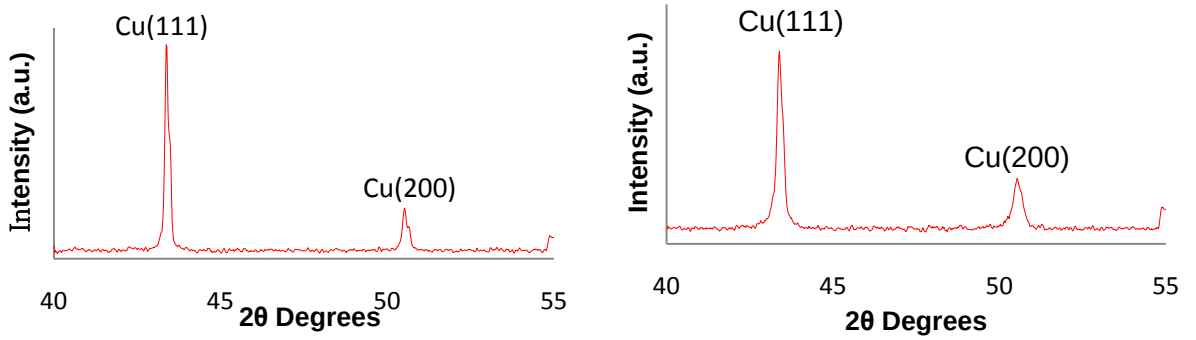


Figure 6-4. XRD spectra of EP Cu/Cu seed layer (MOCVD or sputtering)/W_2N/Si(100). A) EP Cu/Cu seed layer (MOCVD)/W_2N/Si(100). B) EP Cu/sputtered Cu seed layer/W_2N/Si(100).

Table 6-1. Estimated grain size of Cu seed layer on Ta/TaN/Si(100)

Ta/TaN	FWHM	2θ	Grain size (nm)
Cu seed layer (MOCVD)/Ta/TaN/Si(100)	0.236	43.35	36.2
Cu seed layer (sputtering)/Ta/TaN/Si(100)	0.315	43.49	27.1

Table 6-2. Estimated grain size of Cu seed layer on W_2N/Si(100)

W_2N	FWHM	2θ	Grain size (nm)
Cu seed layer (MOCVD)/W_2N/Si(100)	0.315	43.43	27.1
Cu seed layer (sputtering)/W_2N/Si(100)	0.315	43.29	27.1

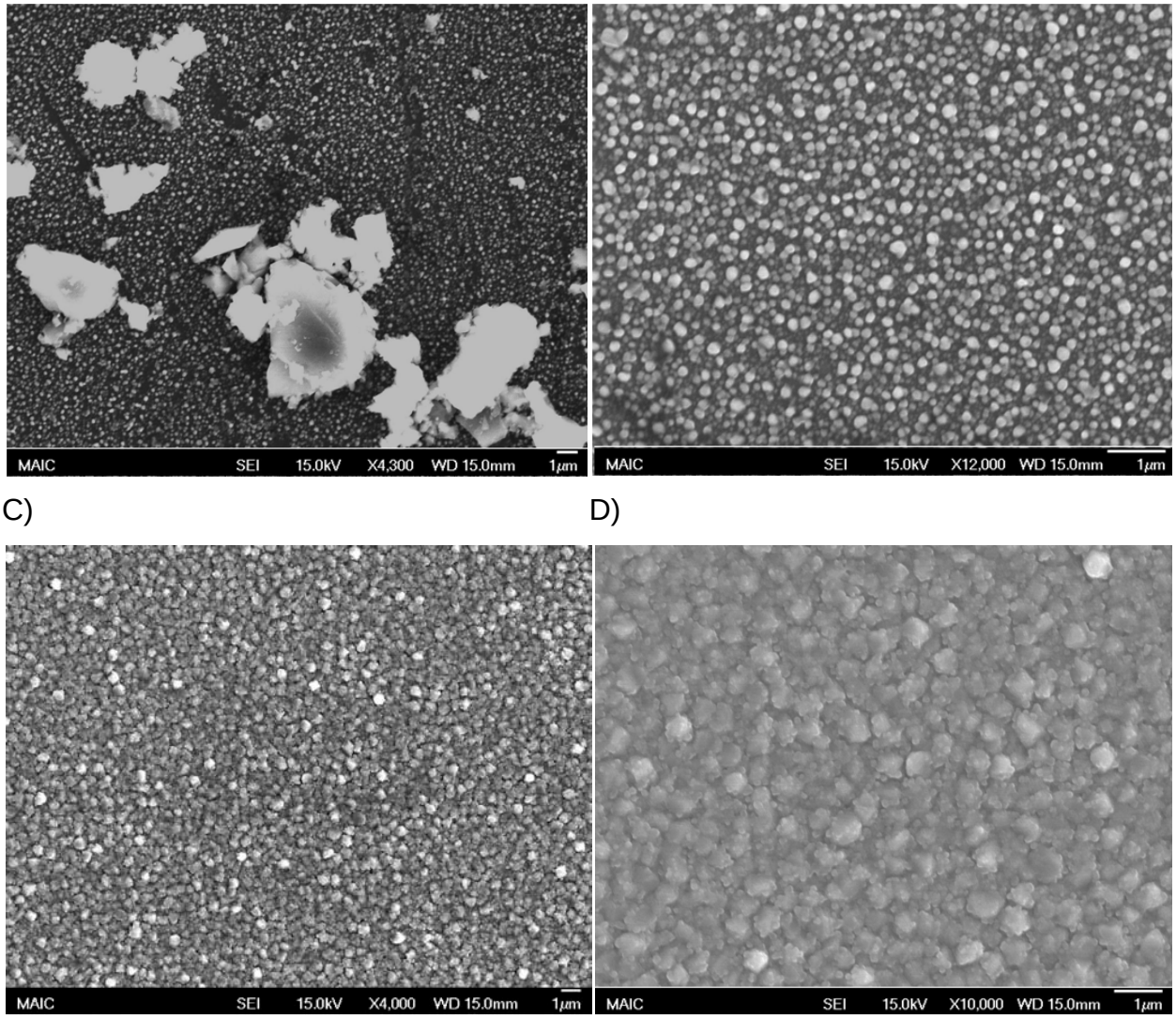
Table 6-3. Estimated grain size of EP Cu on Ta/TaN/Si(100)

Ta/TaN	FWHM	2θ	Grain size (nm)
EP Cu/Cu seed layer (MOCVD)/Ta/TaN/Si(100)	0.118	43.35	72.4
EP Cu/Cu seed layer (sputtering)/TaN/Si(100)	0.098	43.37	87.2

Table 6-4. Estimated grain size of EP Cu on W_2N/Si(100)

W_2N	FWHM	2θ	Grain size (nm)
EP Cu/Cu seed layer (MOCVD)/W_2N/Si(100)	0.096	43.37	89.0
EP Cu/Cu seed layer (sputtering)/W_2N/Si(100)	0.12	43.38	71.2

A) B)



C) D)

Figure 6-5. SEM images of EP Cu/Cu seed layer (MOCVD or sputtering)/Ta/TaN/Si(100). A) EP Cu/Cu seed layer (MOCVD)/Ta/TaN/Si(100) X4,000. B) EP Cu/Cu seed layer (MOCVD)/Ta/TaN/Si(100) X12,000. C) EP Cu/Cu seed layer (sputtering)/Ta/TaN/Si(100) X4,000. D) EP Cu/Cu seed layer (sputtering)/Ta/TaN/Si(100) X10,000.

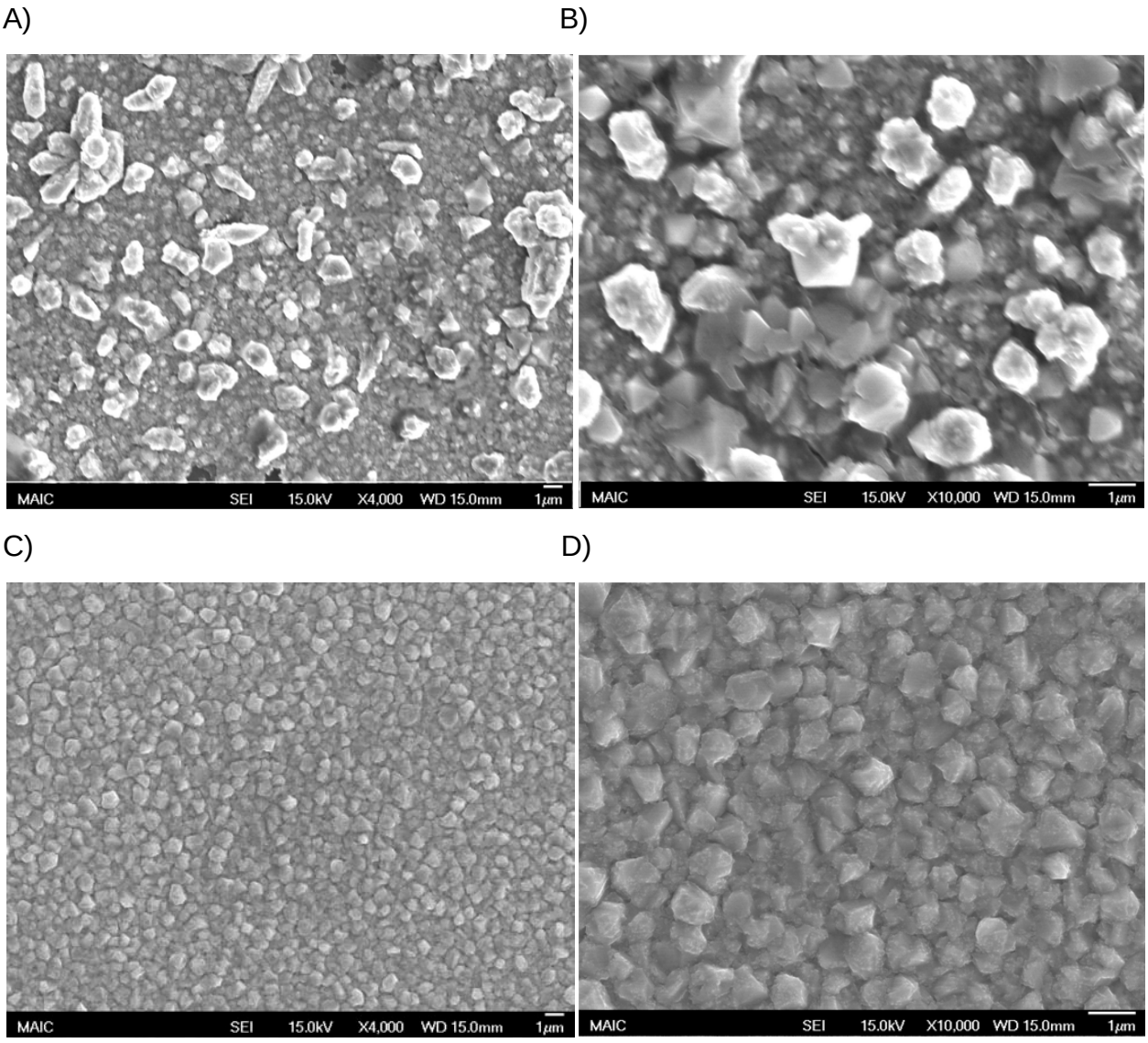


Figure 6-6. SEM images of EP Cu/Cu seed layer (MOCVD or sputtering)/W_2N/Si(100). A) EP Cu/Cu seed layer (MOCVD)/W_2N/Si(100) X4,000. B) EP Cu/Cu seed layer (MOCVD)/W_2N/Si(100) X10,000. C) EP Cu/Cu seed layer (sputtering)/ W_2N/Si(100) X4,000. D) EP Cu/Cu seed layer (sputtering)/W_2N/Si(100) X10,000.

Table 6-5. Film resistivity of Cu seed layer deposited on Ta/TaN and W_2N

	1	2	3	4	5	average (mΩ)	resistivity (μΩ-cm)
Ta/TaN Cu seed layer (MOCVD)/Ta/ TaN/Si(100)	67	65	62	68	61	65.06	0.45542
Cu seed layer (sputtering)/Ta/ TaN/Si(100)	1220	1210	1190	1140	1100	1172	11.72
W_2N Cu seed layer (MOCVD)/W_2N/ Si(100)	74	74	61	69	65	69.08	0.48356
Cu seed layer (sputtering)/ W_2N/Si(100)	2810	1790	1810	1760	1560	1946	19.46

Table 6-6. Adhesion test for Cu seed layer deposited by different techniques

Ta/TaN	Tape test
Cu seed layer (MOCVD)/Ta/TaN/Si(100)	pass
Cu seed layer (sputtering)/Ta/TaN/Si(100)	pass
W_2N	
Cu seed layer (MOCVD)/W_2N/Si(100)	fail
Cu seed layer (sputtering)/W_2N/Si(100)	pass

Table 6-7. Adhesion test for EP Cu deposited on Cu seed layers grown by different techniques

Ta/TaN	Tape test
EP Cu/Cu seed layer (MOCVD)/Ta/TaN/Si(100)	fail
EP Cu/Cu seed layer (sputtering)/Ta/TaN/Si(100)	fail
W_2N	
EP Cu/Cu seed layer (MOCVD)/W_2N/Si(100)	pass (fair)
EP Cu/Cu seed layer (sputtering)/W_2N/Si(100)	pass (poor)

CHAPTER 7
CONCLUSION

Crystallographic orientation of silicon substrate, i.e., Si(100) and Si(111), did not show an influence on (111) texture of Cu seed layer deposited by MOCVD or the subsequently grown EP Cu layer when Ta/TaN was used as diffusion barrier whereas effect of crystallographic orientation of silicon substrate was found to have an effect when W_2N was employed. In this case, Cu seed layers deposited on Si(111) had a stronger (111) texture, and the inheritance of (111) texture promoted stronger (111) texture in the subsequent EP Cu. With regard to grain size, Cu seed layer and EP Cu deposited on Si(111) had larger grains compared with that on Si(100) for both Ta/TaN and W_2N diffusion barriers. However, the grain size difference extinguished when Cu was electroplated on the seed layers. Higher electrical resistivity was found on Cu seed layer deposited on Si(111).

Sputtered diffusion barriers obtained here were amorphous, and the (111) texture of Cu seed layers varied with the diffusion barrier used. However, inheritance of (111) texture was not shown in the following EP Cu. Indeed, the strength of (111) texture of EP Cu did not change much no matter what diffusion barrier was used. Grain size of Cu seed layers was smallest when Cu seed layer was grown on Ta and was two times

larger when deposited on W_2N. Nevertheless, the size difference diminished again after Cu electrochemical deposition. Film resistivity for Cu seed layers deposited on various diffusion barriers did not show much difference.

Cu seed layers deposited by sputtering had stronger (111) texture than those deposited by MOCVD. However, stronger (111) texture obtained by sputtering did not result in a significant impact on the following EP Cu. Namely, $I_{(111)}/I_{(200)}$ were close for EP Cu on both sputtered Cu seed layer and MOCVD seed layer. In addition to not being a "line-of-sight" process, the merit of Cu seed layer deposited by MOCVD was that it grew larger grains compared to sputtering.

Since large Cu grains, uniform distribution, strong (111) texture, smooth and adhesive Cu, and low electrical resistivity of Cu are desirable features to achieve higher reliability in future IC metallization, Si(111) is a better substrate then Si(100) given the inheritance of (111) orientation in Cu grown on Si(111). Weak dependence was found regarding different diffusion barriers used, so the choice of diffusion barrier can be based on the performance of this layer to prevent Cu from diffusing through it. Techniques for Cu seed layer deposition did make difference in the grain size, (111) texture, and adhesion strength but not in the following EP Cu since EP Cu have been known to undergo a process called "self-annealing" or "room-temperature recrystallization" after

growth, which significantly alters its microstructure.[38-40] The MOCVD is better than then sputtering with respect to the ability of conformal step coverage.

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BIOGRAPHICAL SKETCH

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