RF FRONT-END CIRCUIT BLOCKS FOR MULTI-OCTAVE BANDWIDTH FREQUENCY AGILE SYSTEMS

By

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To my parents

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With a fast growing number of electronic devices accessing communication networks, wideband or multi-band frequency agile systems play a more important role than ever before. It is well known that they are safer and faster with higher capacity and more functions than narrowband systems with a fixed frequency. RF front-end circuits for multi-octave bandwidth frequency agile systems start to draw more attention of both academia and industry due to all their advantages over their narrowband counterparts. However, more challenging design demands and higher power consumption are also required for wider bandwidth circuits.

To meet the requirements of modern frequency agile RF front-end transceivers, two low-noise amplifiers (LNAs) are designed and fabricated in CMOS 90 nm and gallium-nitride high-electron mobility transistor (HEMT) technologies respectively. Various novel techniques are adopted and combined to achieve multi-decade GHz bandwidths and lowest power consumption among all previously published works. Complete simulation and measurement results are shown.

Another critical component is frequency synthesizers. A 14-band fast-hopping frequency synthesizer is presented for orthogonal frequency division multiplexing (OFDM) ultra-wideband (UWB) transceivers. To achieve the lowest power consumption, a novel system architecture is proposed. Transistor-level circuits are elaborated and fabricated in CMOS 0.13 μm process. The

chip mounted on a double-layer FR-4 printed circuit board (PCB) was measured by using a spectrum analyzer and a wideband oscilloscope. The complete set of measurement results is presented to demonstrate the performances with the lowest power consumption than all previously published full-band UWB frequency synthesizers.

CHAPTER 1
INTRODUCTION

People are always eager to integrate more functions into a single device. For example, cell phones are used not only as a type of wireless communication transmitting voice and text data, but also entertainment centers, navigation systems, and even as portable video meeting systems in the future. Different communication systems are based on different standards. As all-in-one devices, they are required to be compatible with all the standards. Furthermore, the number of users keeps growing drastically. The International Telecommunication Union estimated that mobile cellular subscriptions worldwide reached approximately 4.6 billion by the end of 2009 [1]. To admit such a huge number of devices, a few multiple-access techniques are utilized. No matter what multiple access technique is adopted, frequency division is ubiquitous, since data transfer has to occupy some amount of bandwidth. This means that in order to admit more devices with higher data transfer speed and capacity, the bandwidth and the number of frequency bands have to be increased. Additionally, with more devices accessing the network, reliability and security issues become more severe. Fixed narrowband systems are not as reliable or safe as they were in their early age. All of these reasons and motivations render multiband RF system design a very valuable topic in both academia and industry.

One of the most popular multiband RF systems is frequency agile (also known as frequency hopping) systems. Basically speaking, frequency agile systems are multiband RF systems with the capability of quick shifting its carrier frequency to increase data transfer speed, avoid jamming and mutual interference, account for atmospheric effects, or to make radio detection more difficult [2].

1.1 A Brief History of Frequency Agility

The concept of frequency agility is very classic and can be traced back to the end of 19th century when Nikola Tesla came up with the idea after demonstrating the world's first radio-controlled submersible boat in 1898 [3]. It was first tried by a German radio and television company, Telefunken, but was first published in 1908 by a radio pioneer, Johannes Zenneck, in his book *Wireless Telegraphy*. In World War I, the German military implemented it to prevent eavesdropping by British forces. This frequency-hopping communication occurs between fixed stations due to the big size of the equipment, but it could not be intercepted without knowledge of the sequence. The first sophisticated frequency-hopping equipment was probably SIGSALY, invented by the U. S. Army Signal Corp during World War II. This system worked so effectively that the Germans could not crack it. Although this idea came out more than a hundred years ago, the most famous inventors of frequency hopping are a movie star, Hedy Lamarr, and a composer, George Antheil, who received a U. S. patent for their "Secret Communications System" in 1942. It hopped between 88 frequencies by using a piano-roll and increased the immunity to enemies' detection and jam of radio-guided torpedoes [4].

Frequency agility was not widely used mainly due to the large size of vacuum tubes during the first half of the 20th century. In the 1960s, the invention of solid state devices dramatically shrank the size of electronic instruments and made frequency agility much easier to implement. Besides, amplifiers using solid state devices have a wider bandwidth, which boosted the effect of frequency agility. Passive electronically scanned array (PESA) radars, introduced in the 1960s, used a series of delays to drive an antenna array and electronically steer the radar beam by changing the delays based on the wave interference principle. The wide bandwidth property of solid state devices offers much greater frequency agility than a klystron. Thus, solid-state PESAs

are more resistant to jamming with its single microwave source changing its frequency from pulse to pulse [2].

1.2 Modern Application Overview of Frequency Agility

Frequency agility grew up from military needs to prevent radars from being detected, jammed or eavesdropped. Since efficient signal reception and processing require careful design and tuning of a receiver, frequency agility makes countermeasures much more difficult than a single fixed frequency system. A frequency agile radar can rapidly hop between different frequency bands. The jammer or eavesdropper must listen on all the possible bands and respond very fast to follow the sequence of the band switch. However, there is always a significant delay of this jammer response. During this delay period, all the countermeasures are actually ineffective. Hence, with a fast band switch, a wide frequency range, and a short time that a radar stays with a single band, the countermeasures are almost impossible without knowing the pseudorandom sequence. A good example is Active Electronically Scanned Array (AESA) radars widely mounted on modern advanced aircrafts and ships [5]. Each radar element of an AESA array has a different frequency and all the frequencies keep changing from pulse to pulse. Knowing the frequencies that are being broadcast, the AESA array can reconstruct a powerful echo by combining only the useful return signals. This complicated operation results in a very low power at each frequency. Enemies' radars see only wideband background noise if unaware of the active bands and the sequence.

Aside from the military use, cellular systems are also based on the principle of frequency hopping. When a cell phone starts up a call with a base station, the cell phone asks the base station for an idle frequency channel. When it leaves the serving range of the base station and enters the range of another base station, the cell phone switches its server under the control of a mobile telephone switching office (MTSO). Since the two base stations do not use the same

group of frequencies, the cell phone must negotiate with the new server to jump onto another frequency.

Radars of tower control at airports communicate with the nearby airplanes in a similar way as the cellular systems. To avoid interference, the radars of both the tower control and airplanes switch frequency bands very frequently with a more complicated algorithm than the cellular systems.

Frequency agility is also used on weather radars. Some frequencies have a high reflection coefficient on clouds whereas some can easily penetrate them. By switching between these frequencies, a complete image of the weather can be built up [2].

Recently, frequency agile systems find new application areas in wireless sensor networks and astronomical observation. S.W. Arms et al. from MicroStrain reported a frequency agile wireless sensor network capable of high speed data communications from a variety of sensors [6]. Continuous data transmission from 26 distinct nodes with 902-928 MHz band and 75kbaud is achieved. Figure 1-1 shows A) the photograph of the sensor node and B) the network using FDMA.

A next-generation radio telescope for solar observation is currently under design and construction. This telescope is using a frequency-agile radar array with a multi-decade GHz bandwidth (0.05 – 21 GHz), which is called Frequency-Agile Solar Radiotelescope (FASR) [7]. With two-decade bandwidth, it will produce a continuous, three dimensional record of the solar atmosphere from the chromospheres up into the mid-corona, as shown in Figure 1-2 A). The wideband frequency agility renders it a quantum leap beyond existing solar radio instruments with high spatial resolution, high spectral resolution, and high time resolution. Because of its importance, FASR is ranked as the highest priority by Solar and Space Physics Survey

Committee decadal review and by the Astronomy and Astrophysics Survey Committee decadal review, and supported by National Science Foundation (NSF) with the cooperation of seven prestige institutes and universities. Figure 1-2 shows the Artist's conception of FASR at the west arm of the VLA site.

Additionally, frequency agility can significantly increase data transfer rate. The wireless communication standard with the highest data transfer rate is IEEE 802.15.3a, also known as Ultra Wide Band (UWB). One of the popular techniques is multiband orthogonal frequency division multiplexing (MB-OFDM) which is based on a digital multi-carrier modulation method [8]. A complete-band MB-OFDM UWB system utilizes 14 bands ranging from 3.1 GHz to 10.6 GHz. The first 12 bands are placed in 4 band groups with 3 bands in each group. The rest two bands are grouped into the fifth group. The frequency separation of two adjacent bands and the bandwidth of each band are both 528 MHz. Figure 1-3 shows the band allocation. The transferring data is divided into 100 parallel data streams and carried by 100 orthogonal sub-carriers with 10 guard carriers. Each sub-carrier is modulated with a traditional modulation scheme at a low symbol rate, maintaining total data rates comparable to single-carrier modulation schemes with complex equalization filters. But since OFDM combines a large number of slowly-modulated narrowband signals instead of one rapidly-modulated wideband signal, channel equalizers can be significantly simplified. Moreover, it is capable of fast frequency hopping between the 14 bands in 7.5 GHz bandwidth and thus has high resistance to interference. With the ability of wireless high speed data link, MB-OFDM UWB systems can replace messy data cables between gadgets and instruments and all the devices can be arranged freely within a room range. Not only as a cable remover, UWB can also establish a more efficient wireless network and facilitate an easy control over all devices in the network.

There is another approach to implement UWB which is pulse based. This type of UWB has advantages of RF precision locating and tracking applications due to high sensitivity to time delay. In this dissertation, only MB-OFDM UWB will be considered.

1.3 Design Scope and Outline of This Dissertation

The scope of frequency agility is too broad for a Ph. D. study to cover. Even a single RF front-end transceiver of a frequency agile system for a specific application requires intensive work by a team of engineers. This dissertation focuses on integrated circuit (IC) design of RF front-end circuits at the block level for multi-octave bandwidth frequency agile systems such as MB-OFDM UWB, and multi-decade GHz bandwidth frequency agile systems such as FASR.

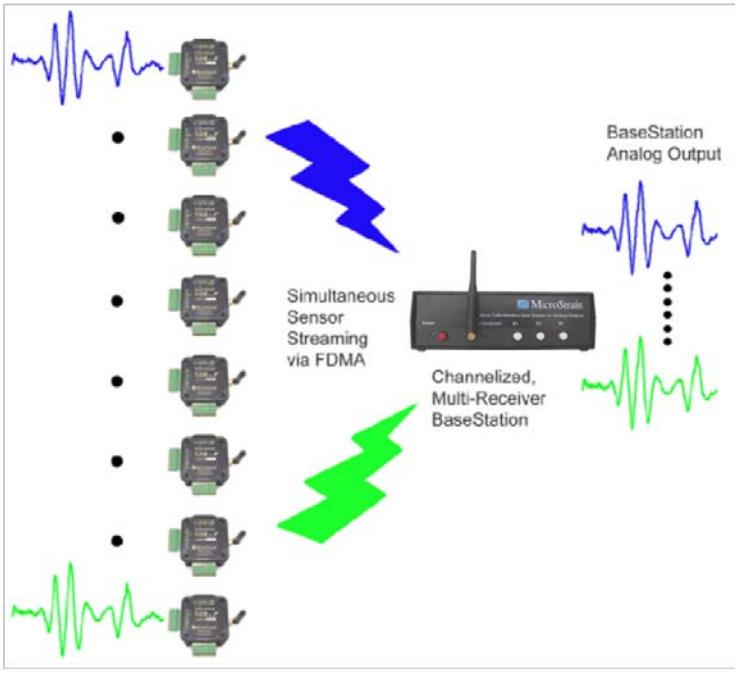
Figure 1-4 shows the block diagram of a simplified wideband direct-conversion receiver. RF signals are received by a wideband antenna. A prefilter following the antenna removes out-of-band interference. Then an LNA provides enough gain and bandwidth with good two-port matching, good isolation, low noise figure and adequate linearity. Note that pre-filtering can be significantly simplified or even eliminated if the LNA has high linearity and input power handling capability. The output of the LNA is split into two channels for synthesis of in-phase and quadrature signals. Mixers downconvert the amplified signals to baseband. A multiband frequency synthesizer provides in-phase and quadrature single tones to mixers. The colored blocks are main works of this dissertation. Although mixers are not of focus, Chapter 4 includes a large extent of mixer design.

Figure 1-5 shows the block diagram of a simple low-IF receiver using ADS. Since the LNA and the frequency synthesizer were designed for different applications and fabricated using different technologies, and other blocks such as filters and IF amplifiers in the receiver chain are not considered in this dissertation, the receiver design is not optimized and this simulation is only conceptual. In short it can only be treated as a quick-start example. The main specifications of

the CMOS LNA and the frequency synthesizer were inserted in the test bench. To increase the total gain, two identical CMOS LNAs are cascaded. The result shows that the total gain and the NF of the entire receiver system are respectively 48 dB and 7 dB. Figure 1-6 shows the input and output QPSK spectrum where the blue and the red are the input and the output respectively.

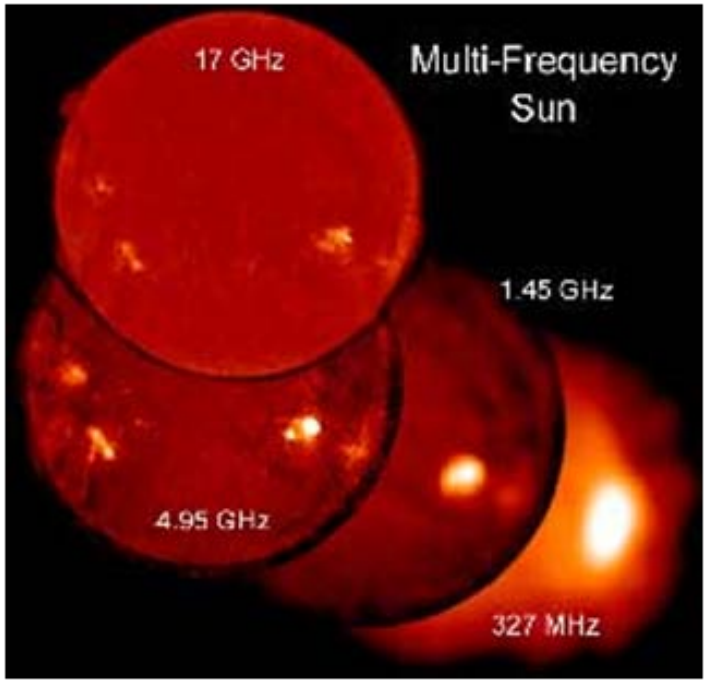
Chapter 2 presents a low-power multi-decade GHz bandwidth CMOS LNA. Four popular architectures of wideband LNAs are compared. The design and analysis of the proposed LNA is discussed step by step. Both simulation and measurement results are shown. Chapter 3 presents a multi-decade GHz bandwidth LNA using GaN HEMT MMIC technology. The GaN technology is introduced and the design, analysis and simulation and meansurement results of the LNA are given. In addition, the CMOS LNA and GaN LNA are compared. Chapter 4 demonstrates a new full-band MB-OFDM UWB frequency synthesizer with the lowest power consumption among all complete 14-band frequency synthesizers reported to date. Both the system-level and the transistor-level design are carefully considered, and complete measurement results are given.

A



B

Figure 1-1. A) Photo of one sensor node and B) the sensor network using FDMA [6].



A

B

Figure 1-2. A) Images of the solar atmosphere at different frequencies and B) artist's conception of FASR at the west arm of the VLA site [7].

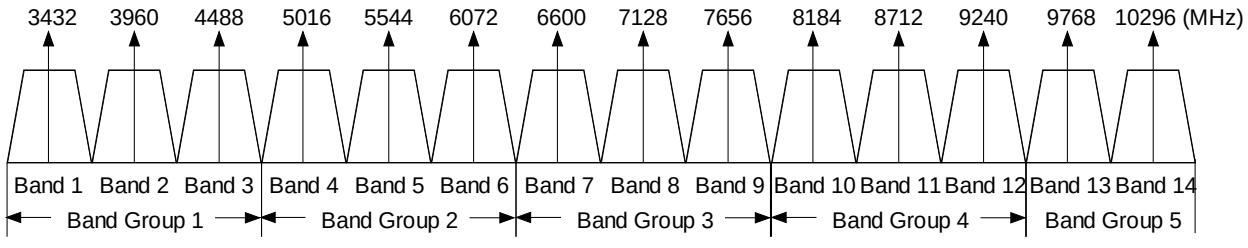


Figure 1-3. Band allocation of a complete-band MB-OFDM UWB system.

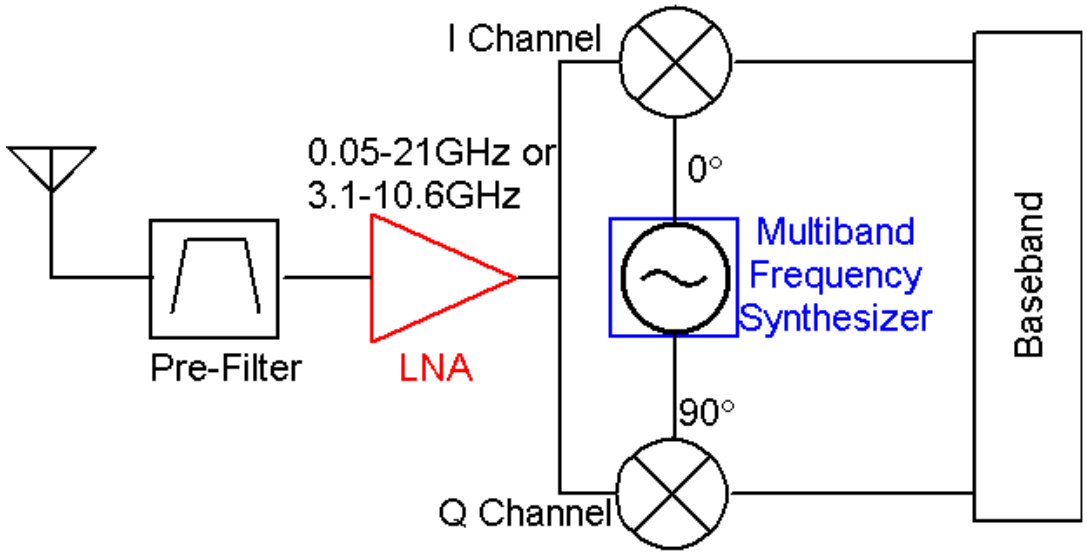


Figure 1-4. Block diagram of a simplified wideband direct-conversion receiver.

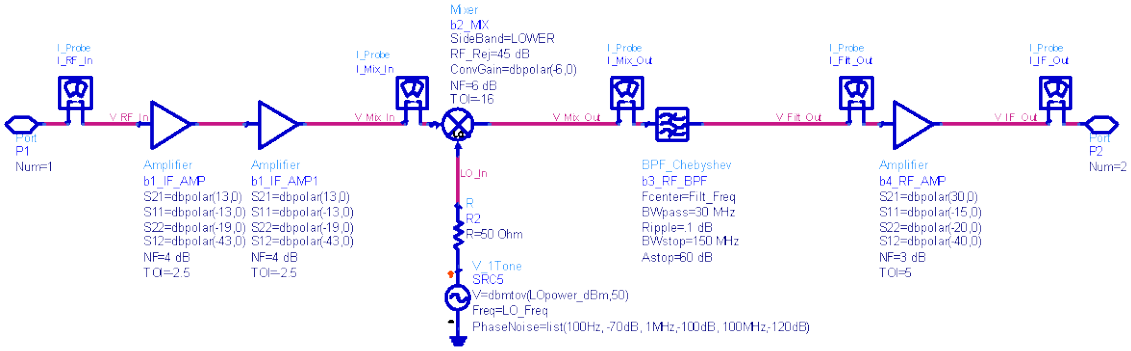


Figure 1-5. Block diagram and a simple low-IF receiver using ADS.

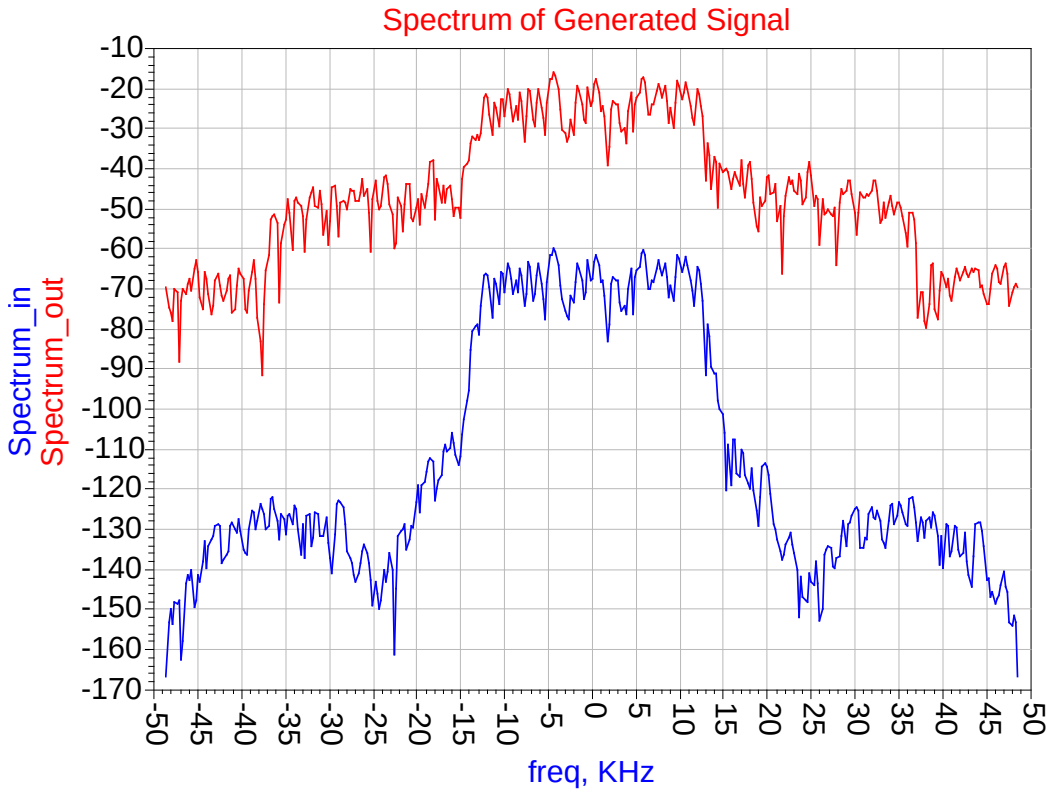


Figure 1-6. Input and output QPSK spectrum.

CHAPTER 2
DESIGN OF A LOW-POWER MULTI-DECADE GHZ BANDWIDTH LOW NOISE AMPLIFIER USING DIGITAL CMOS 90 NM TECHNOLOGY

2.1 Design Considerations of CMOS Wideband Low Noise Amplifiers

Most of the applications mentioned in Chapter 1 require low noise amplifiers (LNAs) to have adequate gain, good input matching, good output matching, good isolation for stability, low noise figure (NF), and adequate linearity over the entire wide bandwidth, while also ensuring low power and area consumption. It is very challenging to achieve all the requirements at the same time with multi-decade GHz bandwidth. In terms of architectures, most modern ultra-wideband LNAs can fall into four basic types, namely 1) filter-match architecture, 2) common-gate architecture, 3) distributed architecture, and 4) shunt feedback architecture.

The filter-match LNA was first proposed by Bevilacqua and Niknejad in 2004 [9]. Figure 2-1 shows the schematic, the die photograph and the noise figure. The input parasitic capacitor is merged into an input band-pass filter to extend the bandwidth of the input matching. Two LNAs were fabricated using standard NMOSFETs and triple-well NMOSFETs. For the standard NMOSFET LNA, 9.3 dB peak power gain with 2.3-9.2 GHz bandwidth and good two-port matching are achieved. However, with large chip area (five on-chip inductors and two on-chip capacitors), this architecture is not as popular as the other three due to its high noise figure and modest gain compared with devices documented in recent publications. In addition, since on-chip reactive components are highly limited and lossy due to parasitics, it is difficult to extend the bandwidth of the on-chip input filter.

Common-gate LNAs are slightly more popular than the filter-matched LNAs due to their simple input matching. The typical input transconductance and noise factor are respectively given by

$$G_m = \frac{1}{R_{in}} = g_m + g_{mb} + \frac{1}{r_o}, \tag{2-1}$$

and

$$F = 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_L}, \tag{2-2}$$

where

R_{in}: Input resistance

g_m: Transconductance of the input transistor

g_{mb}: Back-gate transconductance of the input transistor

r_o: Output resistance of the input transistor

γ: Noise parameter with a value of 2-3 in a deep-submicron CMOS process

$\alpha = g_m/g_{d0}$ with a value of less than unity

R_S: Source resistance with a typical value of 50 Ω

R_L: Load resistance at the drain node.

For typical common-gate LNAs, Equations 2-1 and 2-2 show that 1) the input resistance of 50 Ω limits the transconductance of the amplifiers, and 2) the load at the drain terminal must be much larger than the source resistance to reduce the noise factor which is not trivial over an ultra-wide bandwidth. To boost the input transconductance and reduce the noise figure, several complicated architectures are proposed. X. Li et al. presented a transformer-coupled common-gate LNA shown in Figure 2-2 [10]. C.-F. Liao et al. presented a noise-canceling configuration shown in Figure 2-3 [11]. Despite the complexity, the power gain of [10] (S21 ≤ 9.4 dB) and the noise figure of [11] (NF ≥ 4.5 dB) are still not as good as those of the common-source-based LNAs, and the bandwidth potential is almost exhausted by the parasitics of the introduced components.

Distributed architecture, first proposed by W. S. Percival in 1936, is the most popular choice to obtain multi-decade GHz bandwidth. This architecture maximizes the bandwidth of LNAs that a given process can achieve by trading delay instead of bandwidth for gain, and simultaneously guarantees good two-port matching. The overall gain is obtained by adding the gain of each stage linearly so that it is proportional to the number of stages. Even though the gain of each stage is lower than unity, theoretically, adequate gain can still be achieved by using a large number of stages. This means distributed architecture can work at very high frequencies. However, it is because the gain is added linearly, that each stage contribute to noise, whereas noise figure of other architectures is dominated by only the input transistor. Therefore its noise figure is typically higher than that of other architectures with a huge amount of power and area consumption (typical power consumption $\geq$ 50 mW [12]).

Although several low-power distributed amplifiers (DAs) have been published [13]-[14], the gain realized does not exceed 10 dB, the bandwidth is narrower than 10 GHz, the noise figure is higher and the area consumption is inevitably much larger than other architectures. Figure 2-4 shows a low-power example with 10 dB power gain, 2.7-9.1 GHz bandwidth, 5.4 dB average noise figure and the chip size of 1.85 mm x 0.85 mm. a popular figure of merit (FOM) is introduced and defined by

$$FOM = \frac{S21 \bullet BW\left(GHz\right) \bullet IIP3\left(mW\right)}{\left(F-1\right) \bullet P_{DC}\left(mW\right)}, \tag{2-3}$$

where

BW: -3 dB bandwidth

IIP3: Average input-referred third-order intercept point over frequencies

P_{DC}: Power consumption from DC power supplies,

In terms of the FOM defined by Equation 2-3, DAs can hardly be considered to be the best for ultra-wideband systems.

It is well known that negative shunt feedback can significantly enhance the bandwidth of the gain and input and output impedances by trading the gain. Besides their capability of wideband, this architecture inherits all the other benefits of negative shunt feedback, such as good linearity, insensitivity to device parameter variations and potentially simple bias scheme. Recently, more and more shunt-feedback LNAs using a feedback resistor with low noise figure and much lower power and area consumption are reported [15]-[20]. R.-L. Wang et al. presented a 3.1-10.6 GHz LNA using resistive feedback with a FOM defined by Equation 2-3 higher than most published DAs, which is shown in Figure 2-5 [20]. However, it is still very challenging to achieve a multi-decade GHz bandwidth.

In Chapter 2, a 0.1-20 GHz low-power self-biased resistive-feedback LNA is presented and analyzed. Notwithstanding the price of gain for bandwidth of a traditional resistive-feedback LNA, it will be shown later that the tradeoff can be broken by modifications to the conventional architecture. Before this LNA, only LNAs using distributed architecture are demonstrated to have a multi-decade GHz bandwidth with a lower -3 dB frequency close to DC.

2.2 Circuit Design and Analysis

In the previous section, four popular architectures of broadband LNAs are compared and the advantages of the resistive-feedback architecture are briefly discussed. In this section, this architecture is analyzed in much more detail and the design of the first multi-decade resistive-feedback LNA is discussed in great detail.

2.2.1 Traditional Resistive-Feedback LNA

Figure 2-6 shows the simplified schematic of a traditional resistive-feedback LNA. The resistor, Rs, represents the resistance of the input source and RL is the load resistance at the drain

of NMOSFET M1. Commonly, a capacitor Cblock in series with the Rf is used to facilitate individual DC biases of the gate and the drain. If Cblock is so large that the associated attenuation is negligible, the voltage gain, input impedance and output impedance at low frequencies without parasitic capacitances are given by

$$\left|A_{V0}\right| = \frac{g_m R_L - \frac{R_L}{R_f}}{1 + \frac{R_L}{R_f}} \tag{2-4}$$

$$Z_{in} = \frac{R_f + R_L}{1 + g_m R_L} \tag{2-5}$$

$$Z_{out} = \frac{R_f + R_S}{1 + g_m R_S}. \tag{2-6}$$

Equation 2-4 shows that if Rf is much large than RL and RL is much larger than 1/gm, a high gain is obtained which is close to its maximum value of g_mRL. Two-port matching of 50 Ω requires that equations 2-5 and 2-6 are equal, which results in Rs and RL are both equal to 50 Ω. Consequently, for a high gain, g_m must be much higher than 20 mA/V over a wide bandwidth, which is difficult and very power consuming for a CMOS process. Therefore an output buffer is required to match the output port.

For CMOS 90 nm process, since the parasitic capacitance across the gate and drain (C_{gd}) is about one third of the parasitic capacitance across the gate and source (C_{gs}) in saturation region if the smallest channel length is used, both C_{gs} and C_{gd} have to be taken into account when calculating the bandwidth. Using the method of open-circuit time constants [21], the bandwidth can be expressed as

$$BW \approx \left(\left|A_{V0}\right| \left(\frac{C_{gs}}{g_m} + \frac{R_S C_{gd}}{2} \right) \right)^{-1}. \tag{2-7}$$

When a short-channel MOS device is biased at a high drain current, the drain current is mainly limited by velocity saturation. The term, g_m/C_{gs}, is given by

$$\frac{g_m}{C_{gs}} \approx \frac{\frac{1}{2}\mu_n C_{OX} W E_{sat}}{\frac{2}{3} WLC_{OX}} = \frac{3}{4}\frac{\mu_n E_{sat}}{L}, \tag{2-8}$$

where E_{sat} is the electric field strength when the carrier velocity drops to half the value extrapolated from low-field mobility and can be treated as a constant. Equation 2-8 shows g_m/C_{gs} is nearly constant after the transistor is biased in strong saturation region and the minimum channel length is chosen. Consequently, equation 2-7 shows that the traditional resistive-feedback LNA trades its gain for bandwidth nearly linearly because it is a low-order system.

2.2.2 Modified Resistive-Feedback LNA with a Gate Inductor

To alleviate this tradeoff, the number of the orders should be increased. One popular approach is to introduce zeros to cancel poles by adding capacitors, such as a capacitor in parallel with the feedback resistor and neutralization capacitors. Simulations show that their effects of the bandwidth improvement are high up to around 10 GHz, but start to drop rapidly at higher frequencies due to parasitic capacitances and their variations. On the other hand, inductors which create resonance with the parasitic capacitances are much more effective at frequencies higher than 10 GHz. An inductor, Lg, is introduced into the feedback loop in series with the gate of M1 shown in Figure 2-7.

The detailed derivation of the voltage gain with C_{gs} and C_{gd} of M1 shows that it has three poles and two zeros. The two zeros are basically in tera-hertz range and have negligible effects. Since the detailed derivation is extremely involved and not very helpful to design, after some practical simplification and substitution of three times of C_{gd} for C_{gs}, the voltage gain and the input impedance can be approximated as

$$A_V(s) \approx \frac{-g_m R_L + \frac{R_L}{R_f}}{1 + \frac{R_L}{R_f} + sC_{gd}R_L + s^2 L_g C_{gd}\left(g_m R_L + 4\left(1 + \frac{R_L}{R_f}\right)\right) + 3s^3 L_g C_{gd}^2} \Rightarrow$$

$$A_V(\omega) \approx \frac{-g_m R_L}{1 + \frac{R_L}{R_f} - \omega^2 L_g C_{gd}\left(g_m R_L + 4\left(1 + \frac{R_L}{R_f}\right)\right) + j\omega C_{gd} R_L\left(1 - 3\omega^2 L_g C_{gd}\right)} \quad (2\text{-}9)$$

Equation 2-9 shows that Lg dramatically reduces both the real part and the imaginary part of the denominator at high frequencies, which is equivalent to a significant gain increase with little effect at low frequencies. Also, since the inductor Lg is inside the shunt feedback loop, the required value of Lg (0.6 nH) is reduced by about $|A_{v0}|$ and smaller than that of the traditional shunt feedback. The area consumption is thus significantly reduced. Figure 2-8 shows the simulation result of the bandwidth enhancement with Lg (with a PMOSFET load and a shunt-peaking common-source buffer).

2.2.3 Proposed Self-Bias Resistive-Feedback LNA

For a flat gain over frequency, the total shunt-feedback impedance should not be larger at low frequencies than that at high frequencies. This demands a large Cblock shown in Figure 2-7. A large on-chip capacitor not only occupies a large chip area but also brings large parasitic capacitances at both plates, especially for a digital CMOS process where Metal-Insulator-Metal (MIM) capacitors are not available. Those large parasitic capacitances are deleterious to the bandwidth. Considering a NMOSFET is an enhancement mode device with the gate bias voltage and the drain bias voltage of the same polarity, M1 can be self-biased through the feedback resistor Rf and thus Cblock and the associated parasitic capacitances are removed. Consequently, this improvement results in a wider bandwidth, a flatter gain, a simpler bias network and a smaller chip area.

To increase the maximum gain, a large load is demanded. For the same current and voltage drop, a PMOSFET can provide larger resistance with smaller chip area than a resistor. Moreover, the PMOSFET is able to counteract the effect of process variation by tuning its gate voltage. Hence, a much better control is obtained through the PMOSFET than a resistor.

Although Figure 2-8 shows bandwidth is enhanced by 40-50% due to Lg, it is still much less than multi-decade GHz. Furthermore, the parasitic capacitance at the drain of M1 has not yet been considered so far, which consists of the parasitic capacitances and of M1, Rf, the PMOSFET, the input transistor of the next stage. This total capacitance can be even larger than the input parasitic capacitance of M1 due to the miller effect which results from C_{gd} coupling. A time-domain interpretation of how inductors increase bandwidth is that fast current variation is delayed by inductors. As a result, more current is available to charge the parasitic capacitor associated with each node. Hence, faster variation is realized, which implies a wider bandwidth [21]. Based on this principle, an inductor in series with the drain of M1, Ld, splits the charging of the parasitic capacitances associated with the drain of M1 and the gate of the next stage and the load, and thus further boosts the bandwidth. The value of the inductor Ld (0.45 nH) is also reduced by the feedback loop. Nevertheless, Ld degrades the input matching at high frequencies through the coupling due to C_{gd1}. To overcome this drawback, a small inductor (Ls = 0.1 nH) is added in series with the source of M1. Another inductor in series with the source of M2, Lsp, maximizes the benefits of the principle and extends the bandwidth of the load. The schematic of the LNA with all the improvement mentioned above is shown in Figure 2-9.

The degradation of S21 at high frequencies due to the degeneration of Ls can be easily compensated by slightly increasing Ld. Figure 2-10 shows the gain boosting at high frequencies due to Ld and Lsp. The inductor Ld brings an exciting improvement by almost doubling the

bandwidth. Figure 2-11 shows the significant input matching improvement at high frequencies due to Ls. The inductor Ls eliminates the overshoot of the S21 resulting from Ld and thus increases the stability, as shown in Figure 2-11.

As discussed earlier, to reduce the required g_m and increase the freedom degree of the design, a common-source buffer with shunt peaking is employed to provide wideband output matching. With the output buffer, the schematic of the whole LNA is completed, which is shown in Figure 2-12.

The inductor Lsp not only enhances bandwidth but also suppresses the noise current of M2 resulting from source degeneration at high frequencies, as shown in Figure 2-13. Neglecting the noise of the output buffer due to the high gain of the first stage, the noise factor is approximately given by

$$F \approx 1+\frac{R_S}{R_f}+\frac{\gamma_1}{\alpha_1}\frac{1+\omega^2 C_{gs1}^2 R_S^2}{g_{m1}R_S}+\frac{\gamma_2 g_{d02}}{g_{m1}^2 R_S}\frac{1+\omega^2 C_{gs1}^2 R_S^2}{1+\omega^2 L_{sp}^2 g_{m2}^2}, \tag{2-10}$$

where g_{d02} is the drain-source conductance of M2 at zero V_{ds}. The second term is from the feedback resistor, the third term is from the input transistor, and the last term is from M2. As can be seen from equation 2-10, Lsp reduces the noise contribution of M2. Consequently, noise figure is not significantly degraded by M2 compared to a single inductor load but the gain is boosted by M2. In addition, the intrinsic gain of M2 reduces Lsp (0.25 nH) due to series feedback. No additional power or voltage-headroom consumption is introduced by the inductor.

2.3 Simulation and Measurement Results

The proposed wideband LNA was fabricated using UMC digital CMOS 90 nm process with nine metal layers. Since the top metal thickness is 0.8 μm, if only the top metal layer is used, the Q factor of inductors is not high enough due to relatively high parasitic series resistance. To increase the effective thickness of the conductor, metal layers 7-9 are in parallel

and connected tightly by intensive via farms. The total thickness increases from 0.8 μm to 1.8 μm without the counting thickness of vias. Symmetric inductors are chosen due to higher inductor values than regular spiral inductors in the same amount of area. All the inductors are optimized and simulated by using HFSS. Figure 2-14 shows the die photograph with the chip size of 0.5 mm x 0.7 mm including pads and the active area (including all inductors) of 0.26 mm x 0.45 mm. The LNA was measured on a probe station. S-parameters were obtained by using Agilent E8361A 10 MHz – 67 GHz network analyzer. Figure 2-15 shows the comparison of S11 and S21 between the simulation and measurement results. Figure 2-16 shows the comparison of S12 and S22 between the simulation and measurement results.

A good agreement was achieved over the entire bandwidth. The measured S21 reaches 12.7 dB as its peak value at 10 GHz, 11 dB at 0.1 GHz, and 9.71 dB at 20 GHz (-3 dB bandwidth). The LNA has a flat power gain across the whole 20 GHz bandwidth. The measured S11 is below -9 dB from 0.1 GHz to 1 GHz and below -10 dB in the rest of the band, and the measured S22 is below -10 dB over the entire bandwidth, which shows good input and output matching. The -3 dB bandwidth of the power gain is from a frequency below 0.1 GHz to 20 GHz. Good two-port matching is achieved from 0.1 GHz to 20 GHz.

High power gain and reverse isolation with good input and output matching indicate a good stability. The stability was examined by using the classic K-Δ test where the Rollet factor K and the auxiliary factor Δ are respectively defined as

$$K = \frac{1 - |S11|^2 - |S22|^2 + |\Delta|}{2|S12 \bullet S21|} \tag{2-11}$$

$$|\Delta| = |S11 \bullet S22 - S12 \bullet S21| \tag{2-12}$$

Plugging the measured S-parameters into Equation 2-11 and Equation 2-12, we get the measured Rollet factor above 5 and the auxiliary factor below 0.18 over the entire bandwidth, which shows the LNA is unconditionally stable within the extremely wide bandwidth, as shown in Figure 2-17.

The noise figure of the LNA was measured by using Agilent E4448A spectrum analyzer with the extended option 219. The default built-in preamplifier of option 219 has a bandwidth of up to only 3 GHz. To measure the noise figure at frequencies much higher than 3 GHz, a wideband high-gain external LNA is demanded. A Marki A-0120 LNA with 1-20 GHz bandwidth, 26 dB power gain and 3.5 dB noise figure was inserted. An Agilent Noise Source 346C_K01 with a bandwidth of 10 MHz to 26.5 GHz generated noise which was then injected into the input of the LNA to be measured. The noise source was driven by a +28V pulsed source from the back panel of the spectrum analyzer. After careful calibrations, the measured noise figure data from 1 GHz to 20 GHz were obtained. Figure 2-19 shows a good agreement between the measured and the simulated noise figure. The measured noise figure varying from 3.3 dB to 5.5 dB is around 3.6 dB and below 4 dB up to 17 GHz. It rapidly goes up at frequencies higher than 17.5 GHz due to the parasitics.

The small-signal linearity and the large-signal linearity were respectively characterized by IIP3 and input-referred 1 dB compression point (Input P1dB). For IIP3 measurement, two RF single-tone signals with 10 MHz separation were combined by a power combiner and then inputted into the LNA. The power of both the fundamental tone and two third-order intermodulation spurs (IMD3) were obtained by using Agilent E4448A spectrum analyzer. After calibrating out the loss of all the cables and the power combiner, IIP3 was determined by extrapolating the power data of the fundamental tone and IMD3 at all frequencies. Figure 2-19

shows IIP3 at 10 GHz as an example. It ranges from -4 dBm to -1 dBm over the entire bandwidth. For Input P1dB, only one RF single-tone signal was injected into the LNA instead. The Input P1dB was determined where the power gain drops by 1 dB compared to the small-signal one at each frequency. It ranges from -17 dBm to -12 dBm with 10-15 dB difference from IIP3.

The LNA excluding the output buffer derives 10.5 mA from a 1.2 V power supply, which is lower than all other previously published CMOS LNAs with similar bandwidth. The output buffer consumes 6.5 mA from the 1.2 V power supply. The performance of the proposed LNA is summarized and compared with recently published LNAs in Table 2-1 where FOM is the figure of merit defined in Equation 2-3. For a fair comparison, peak values in linear scale are used for S21 and average values are used for F and IIP3. Table 2-1 shows that the proposed LNA has the widest bandwidth with the highest FOM. The two low-power DAs in Table 2-1 show less than half of the FOM of this LNA. This suggests that for most wideband applications where DC-to-20 GHz bandwidth is more than enough, DAs are not the best choice, unless one wants to challenge the speed limit of a process.

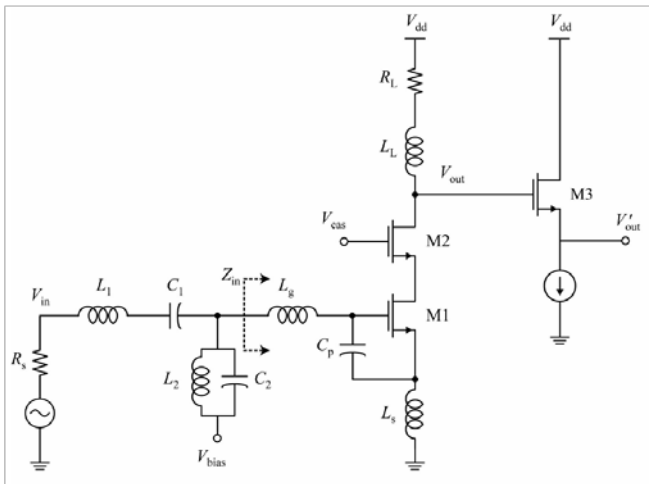
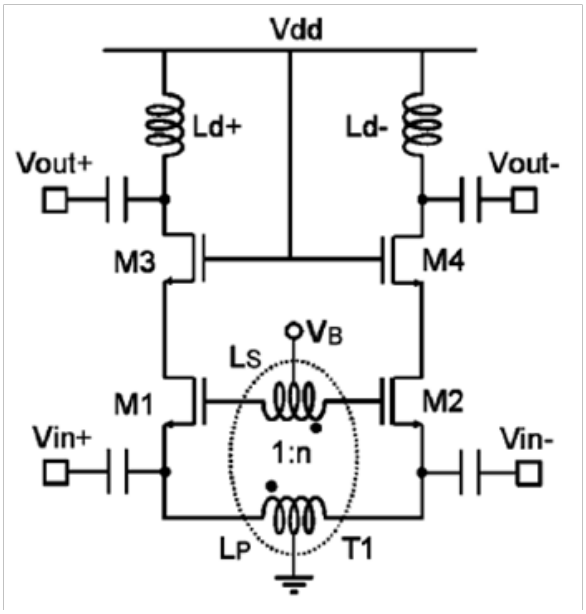
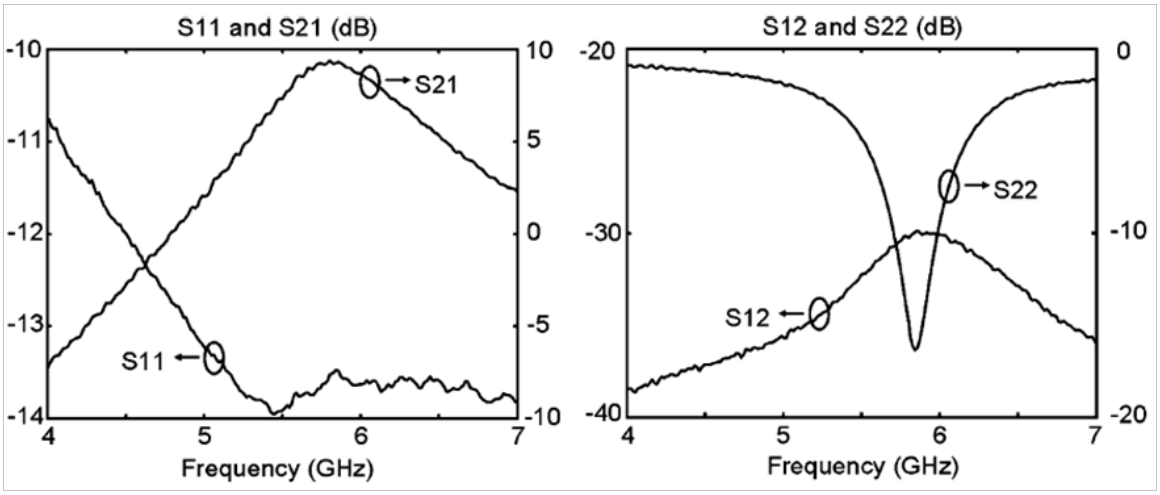


Figure 2-1. Results of A) schematic, B) die photograph and C) noise figure of the ultra-wideband CMOS LNA using filter-match architecture by Bevilacqua and Niknejad [9].



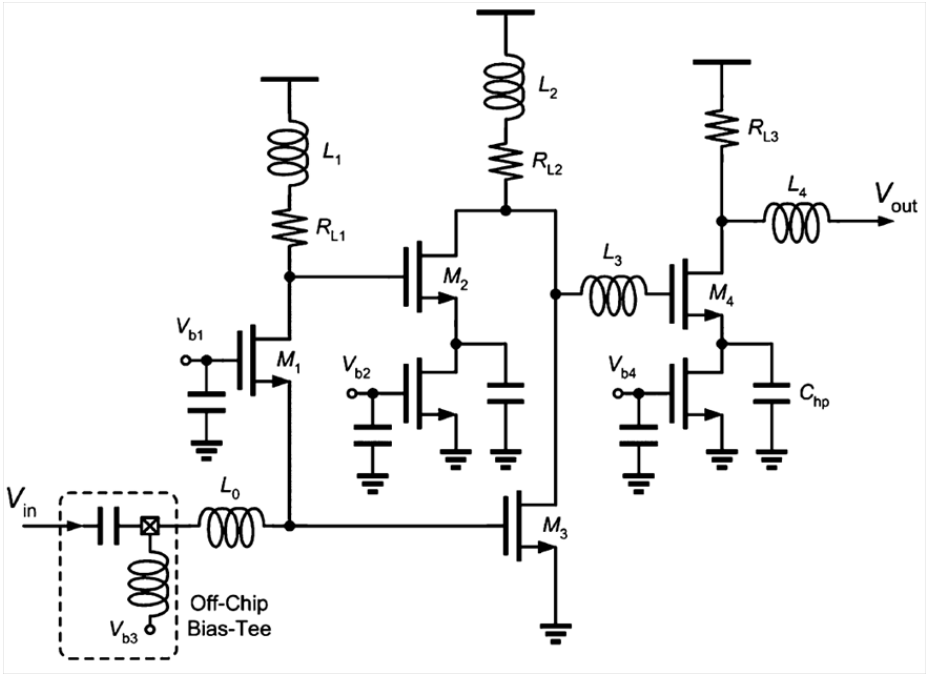
A



B

Figure 2-2. Results of A) schematic and B) S-parameters of the g_m-boosted common-gate LNA by X. Li et al. [10].

A



B

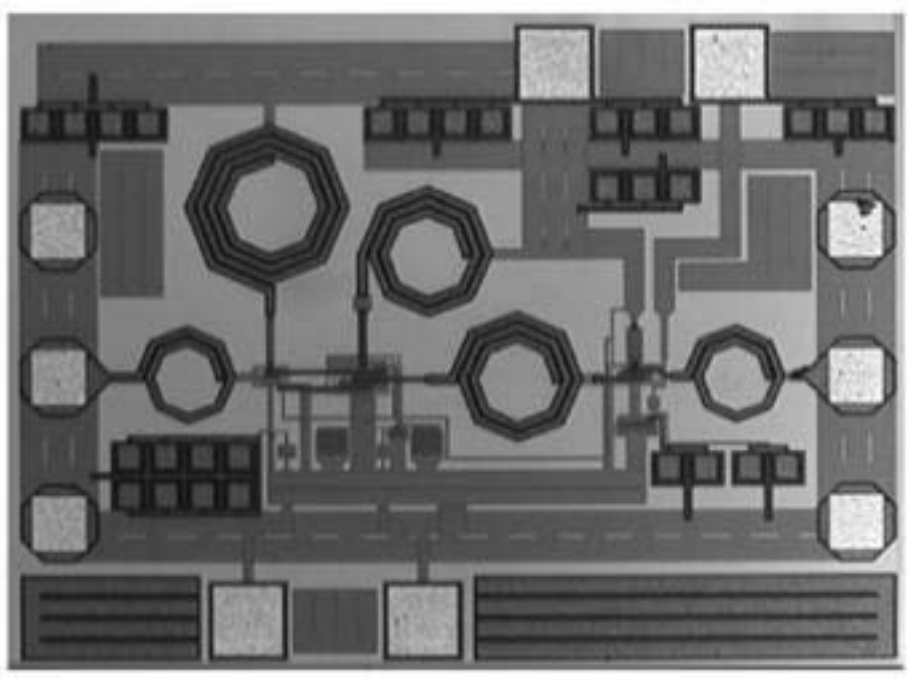
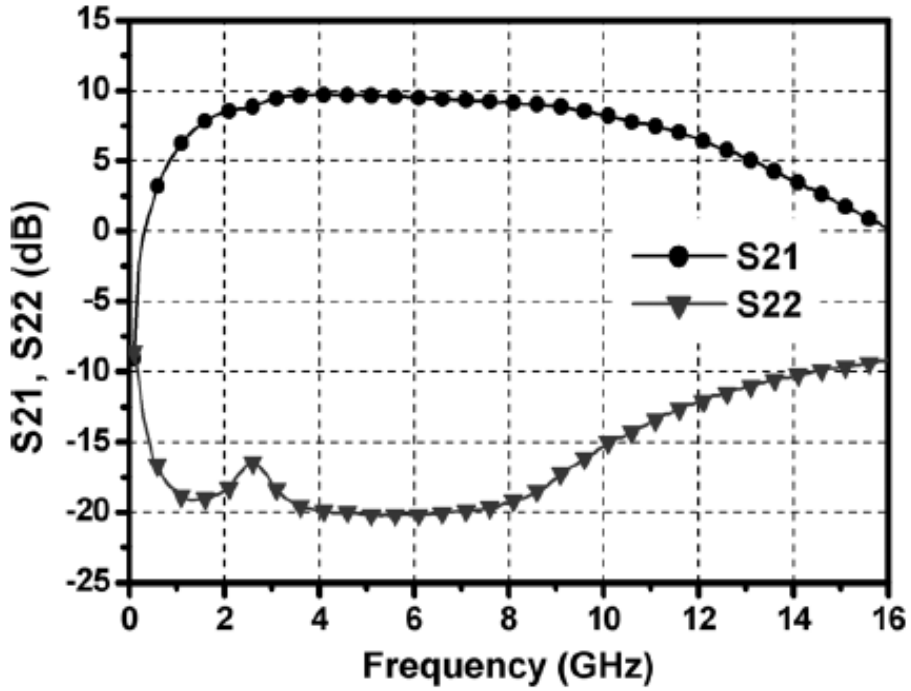


Figure 2-3. Results of A) schematic, B) die photograph, C) S-parameters and D) noise figure of the noise-cancelling common-gate LNA by C.-F. Liao et al. [11].

C



D

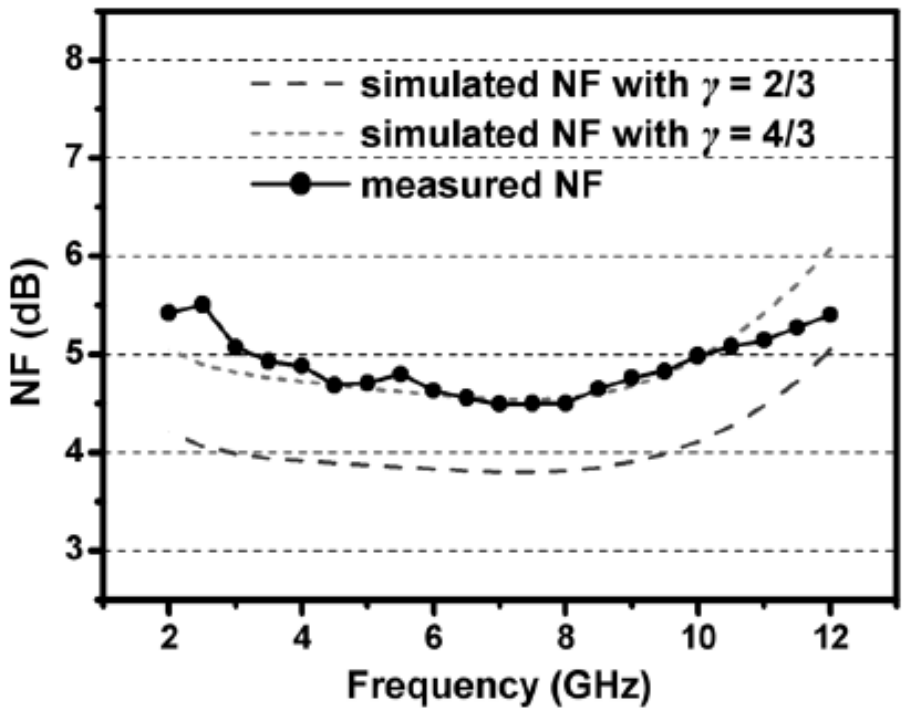


Figure 2-3. Continued

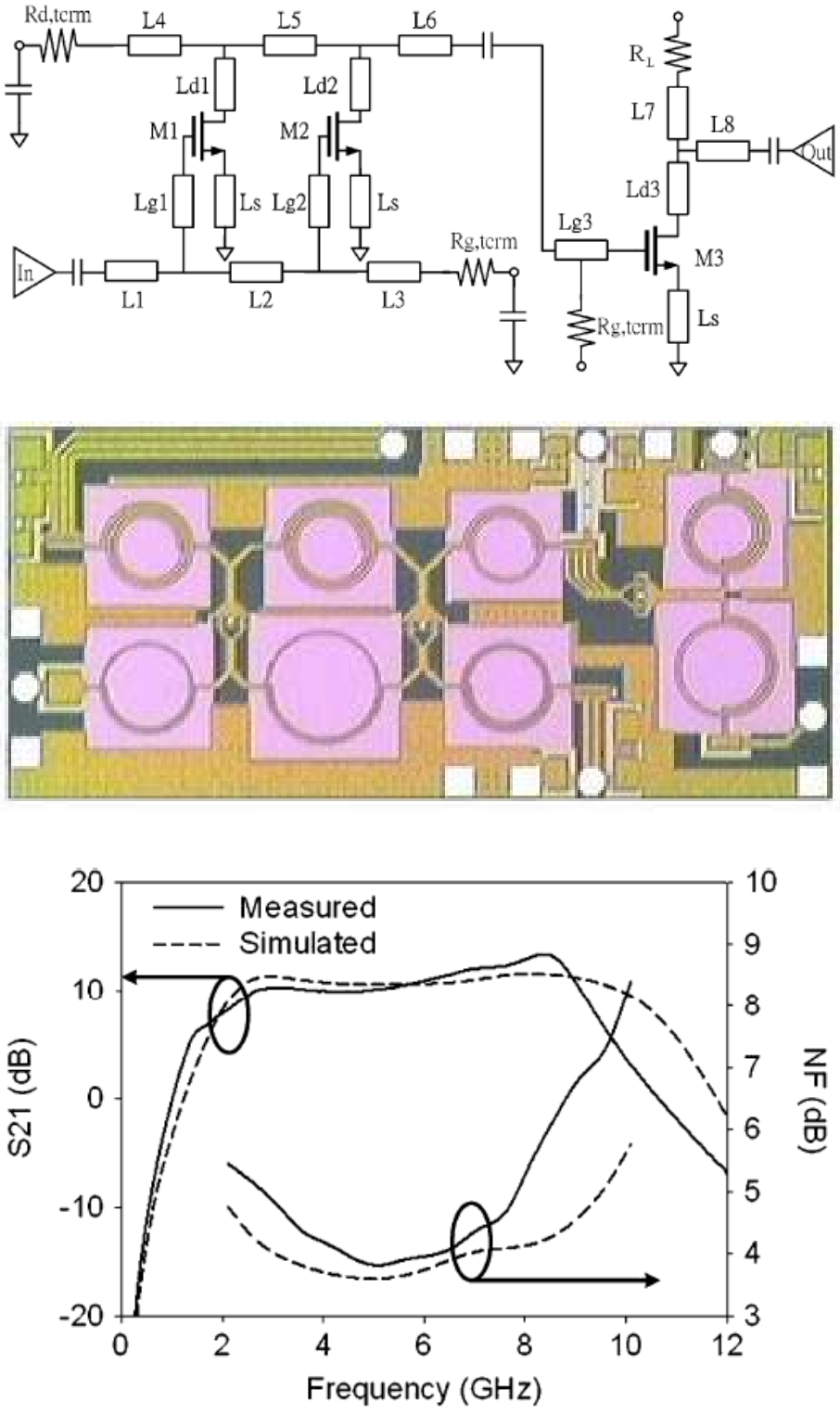


Figure 2-4. Results of A) schematic, B) die photograph, C) S-parameters and noise figure of the low-power DA by Y.-H. Yu et al. [13].

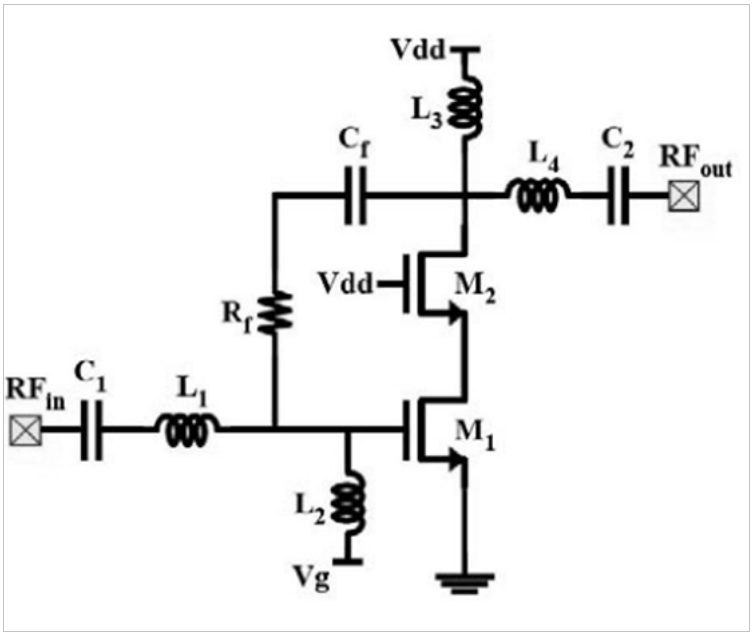
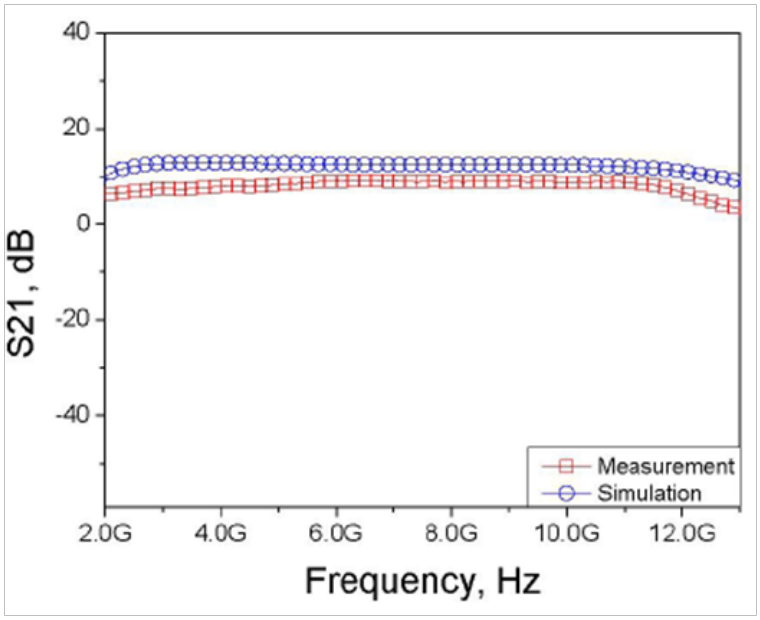


Figure 2-5. Results of A) schematic, B) die photograph, C) power gain and D) input matching of the resistive-feedback LNA by R.-L. Wang et al. [20].



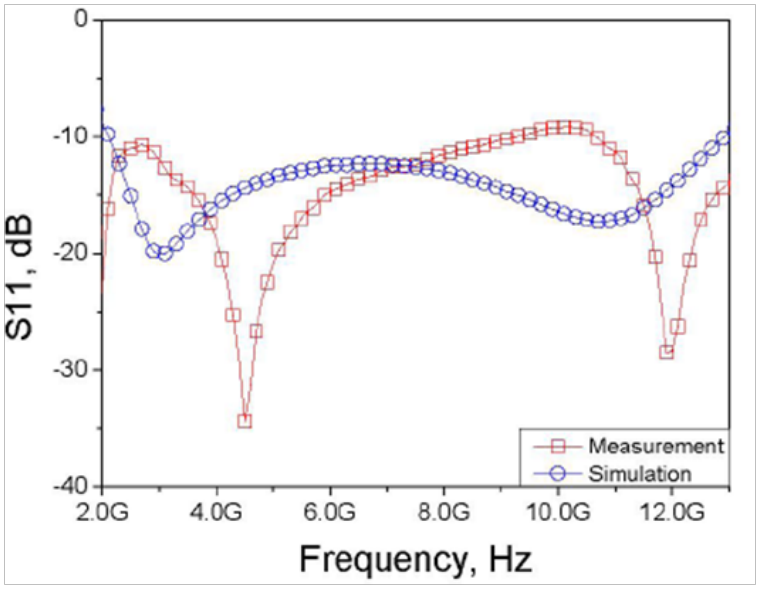


Figure 2-5. Continued

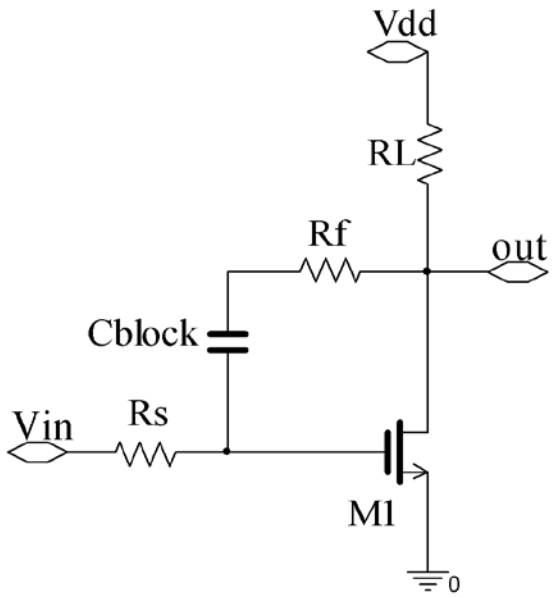


Figure 2-6. Simplified schematic of a traditional resistive-feedback LNA.

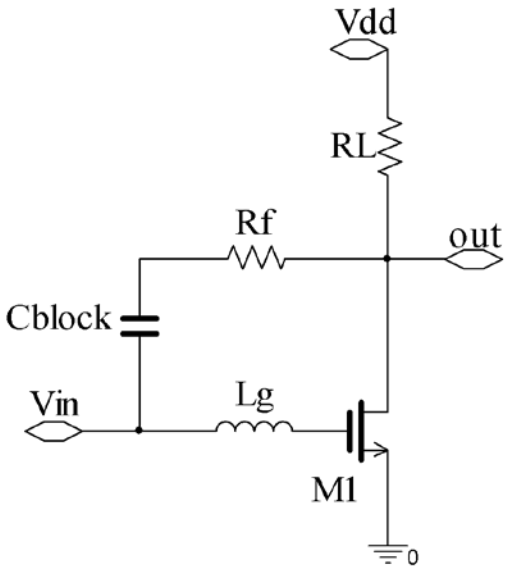


Figure 2-7. Schematic of a resistive-feedback LNA with an inductor in series with the gate.

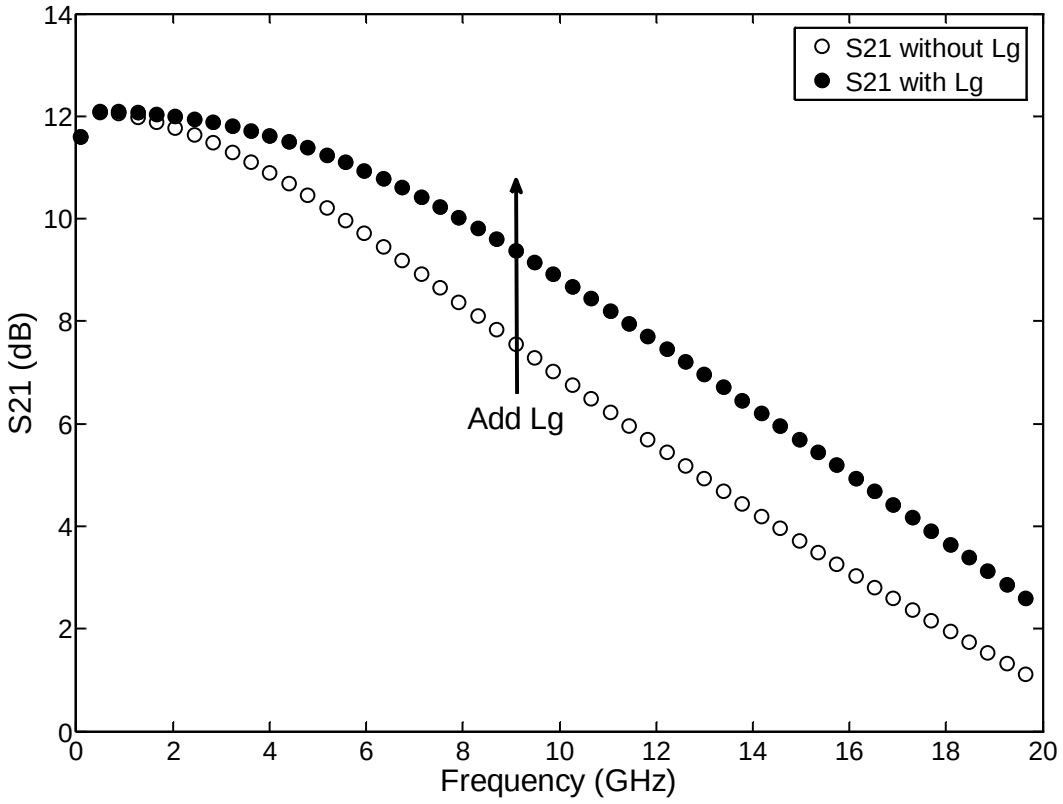


Figure 2-8. Simulation results of the gain-bandwidth product enhancement due to Lg. The simulation was based on schematic shown in Figure 2-7 with a PMOSFET load instead of the resistor RL and a shunt-peaking common-source buffer.

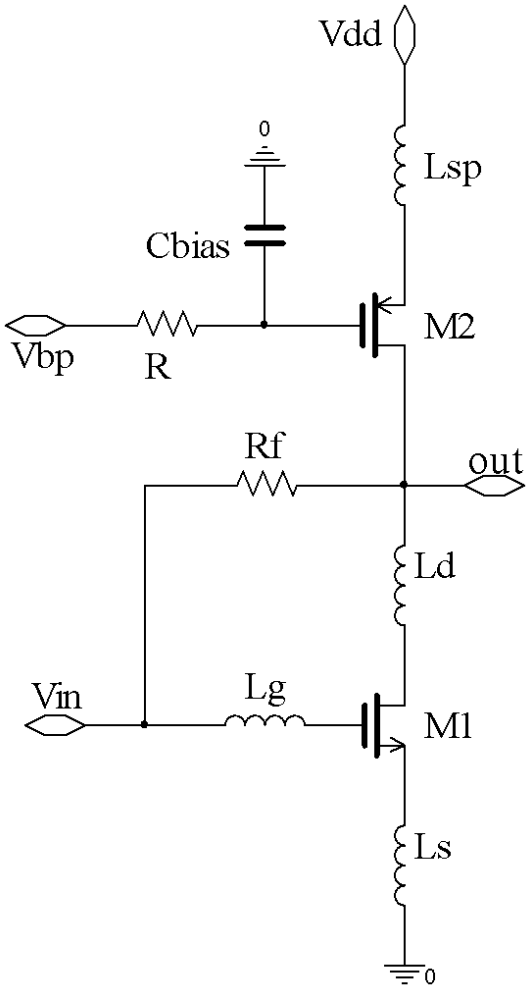


Figure 2-9. Schematic of the resistive-feedback LNA with 1) a PMOSFET load, 2) an inductor in series with the drain of M1, 3) an inductor in series with the source of M1, 4) an inductor in series with the source of M2, and 4) Cblock removal.

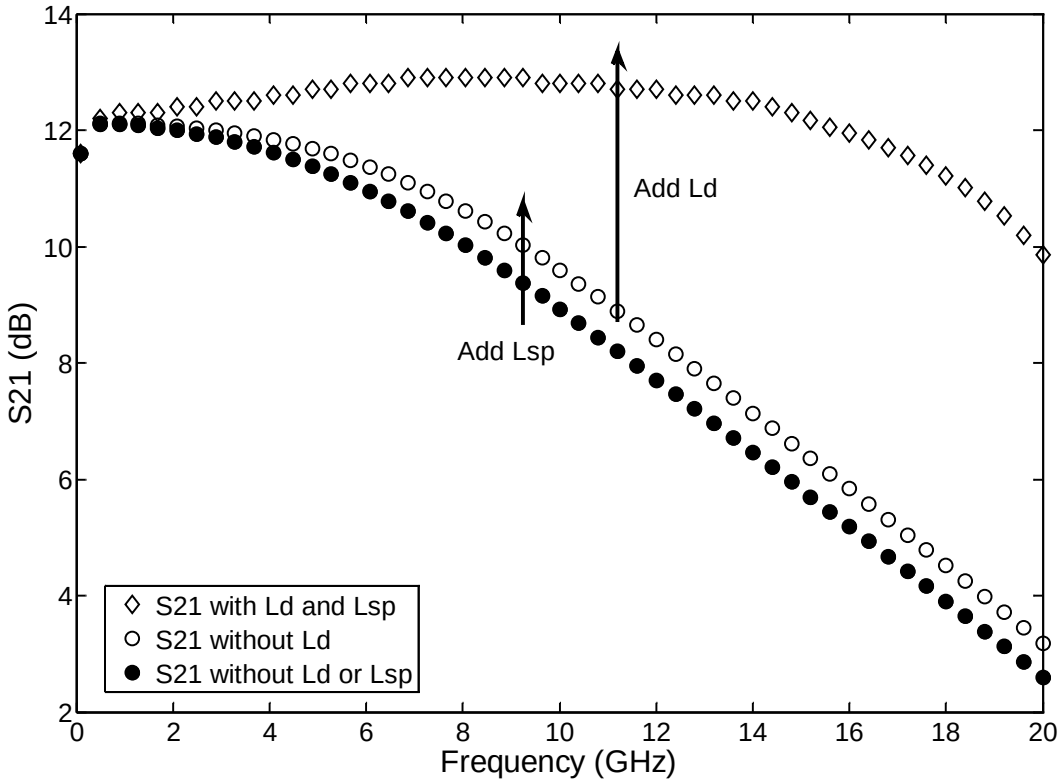


Figure 2-10. Simulation results of the gain-bandwidth enhancement due to Ld and Lsp. The bandwidth is increased by more than 100% by the two inductors.

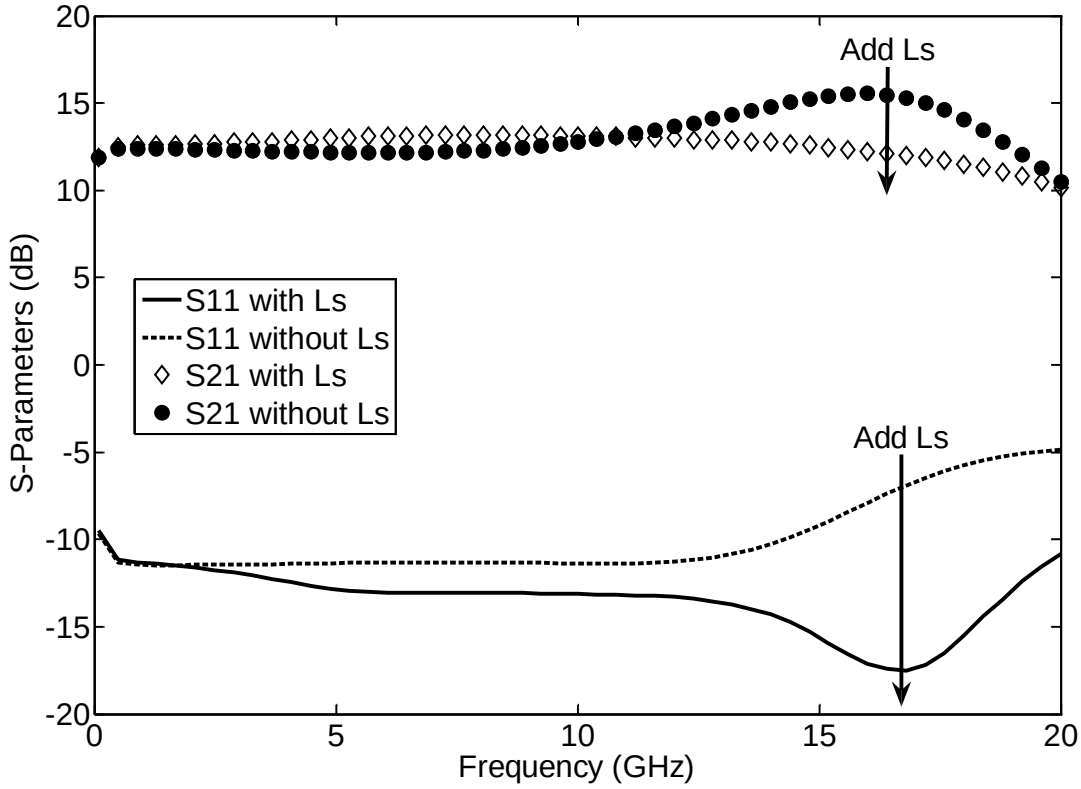


Figure 2-11. Simulation results of the improvements on S11 and S21 due to Ls.

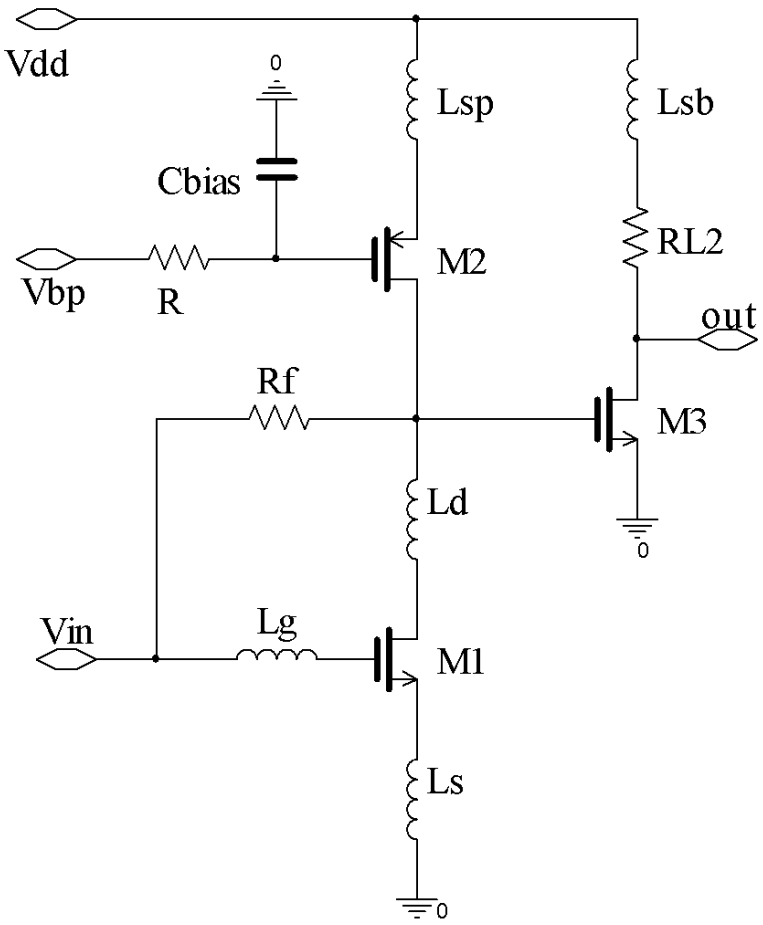


Figure 2-12. Simplified schematic of the proposed wideband LNA.

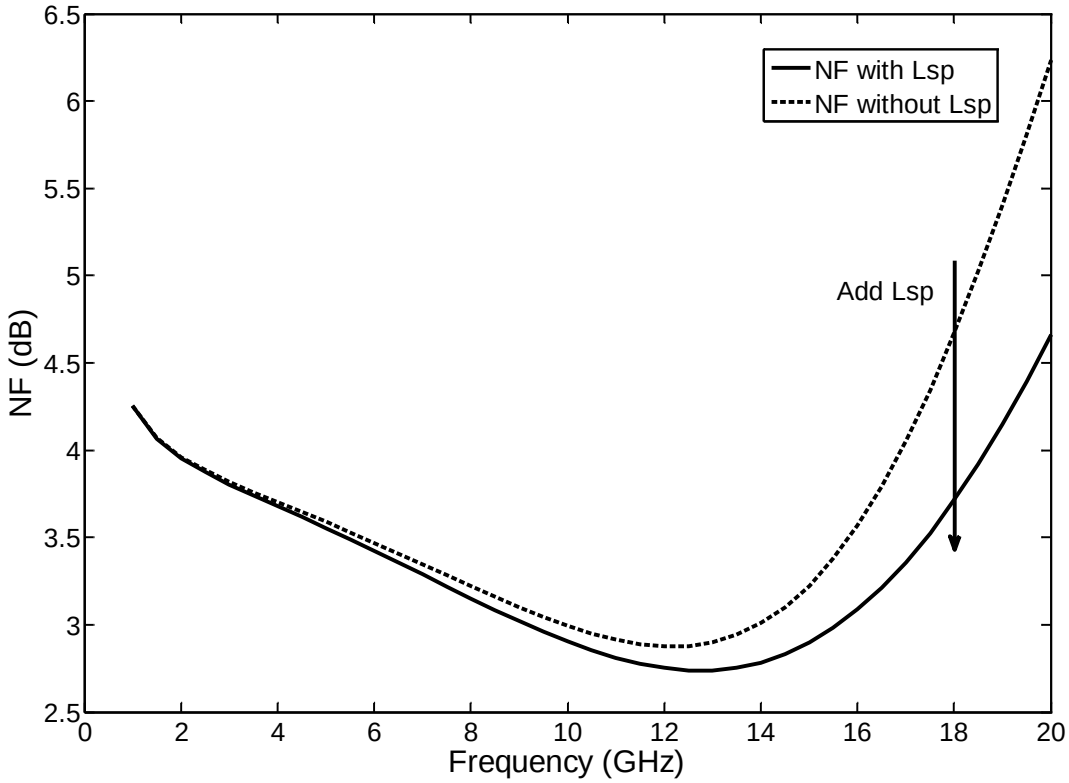


Figure 2-13. Noise figure improvement at high frequencies due to Lsp.

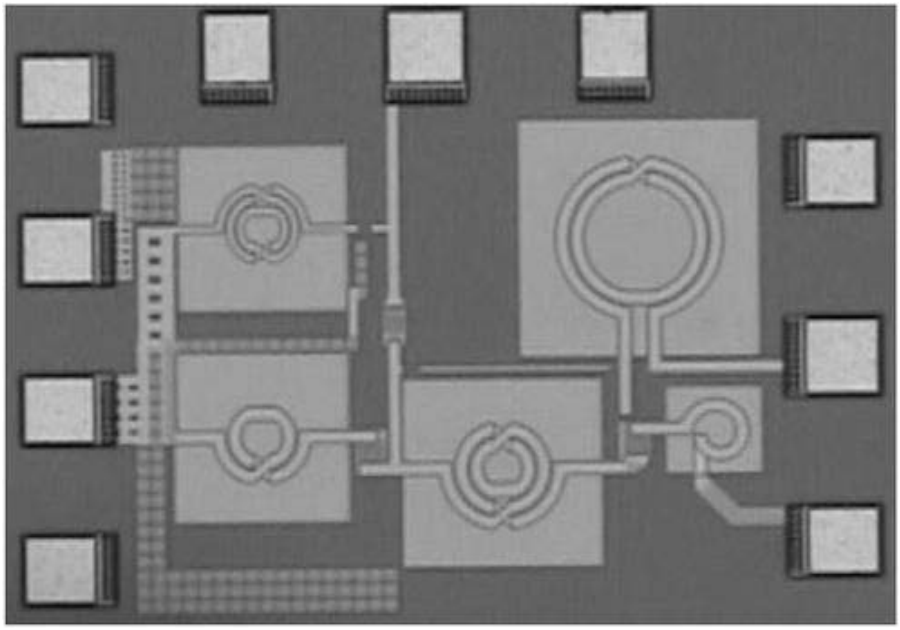


Figure 2-14. Die photograph of the proposed LNA. The chip size is 0.7mm x 0.5mm with the active area (including all the inductors) of 0.26mm x 0.45mm.

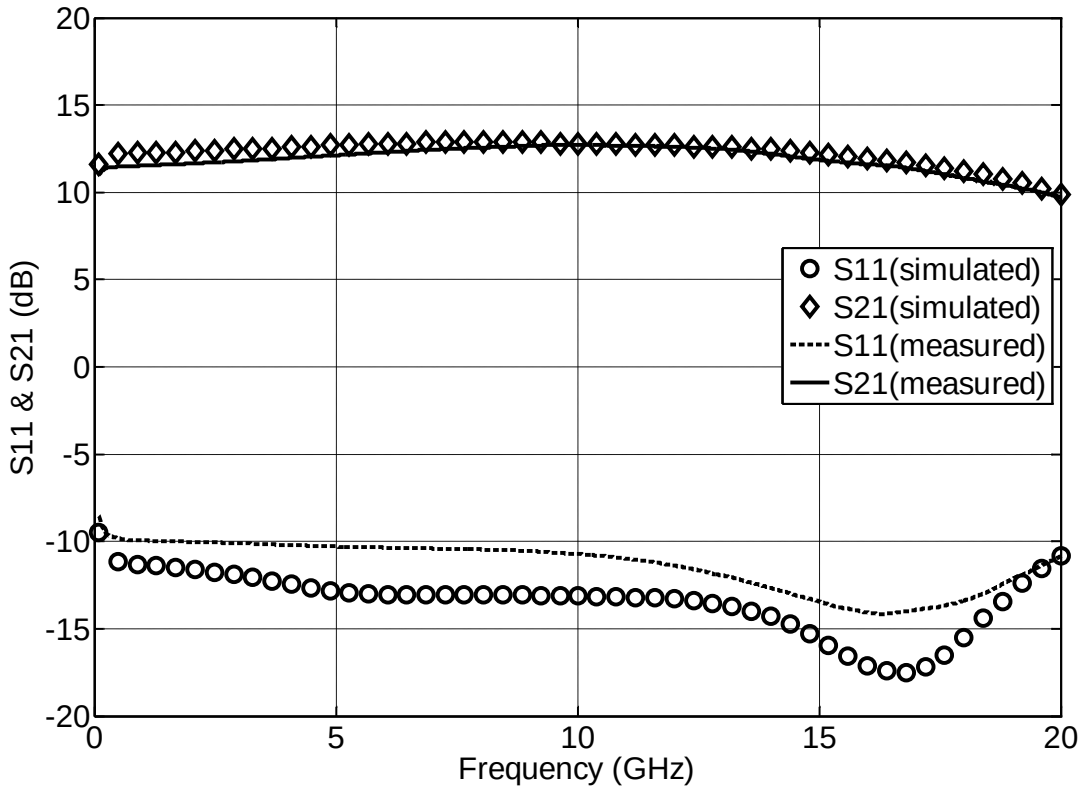


Figure 2-15. Simulation and Measurement results of S11 and S21 from 100 MHz to 20 GHz.

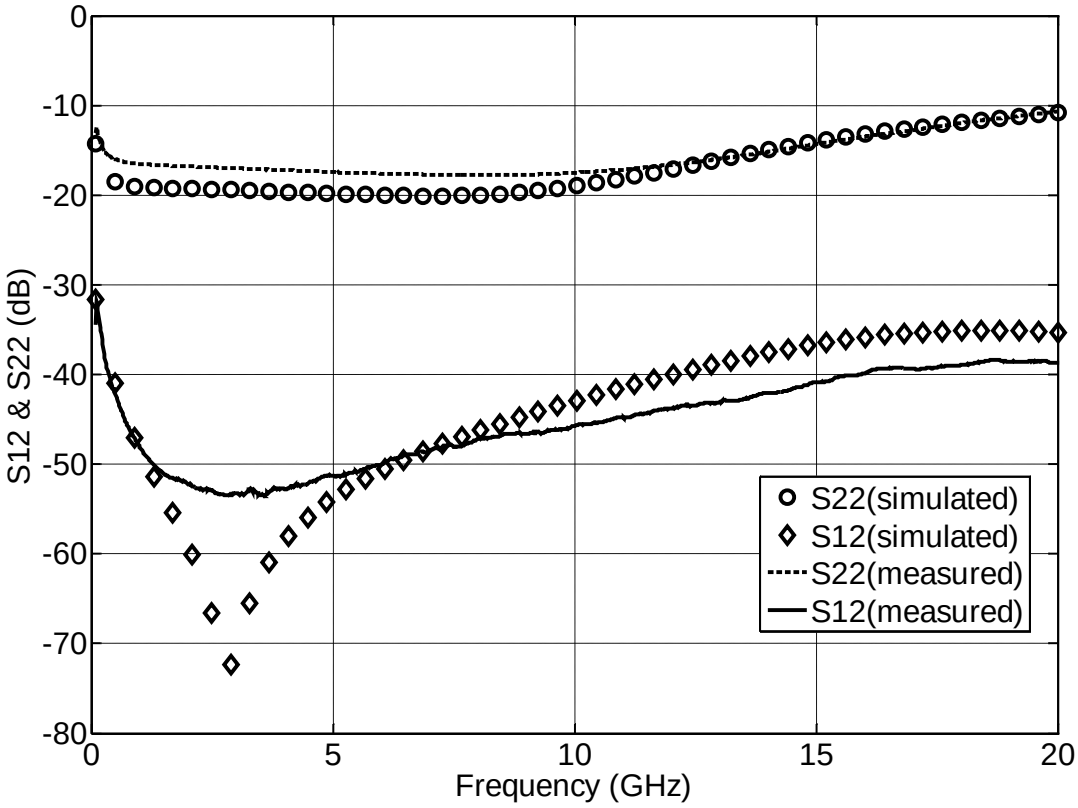


Figure 2-16. Simulation and Measurement results of S12 and S22 from 100 MHz to 20 GHz.

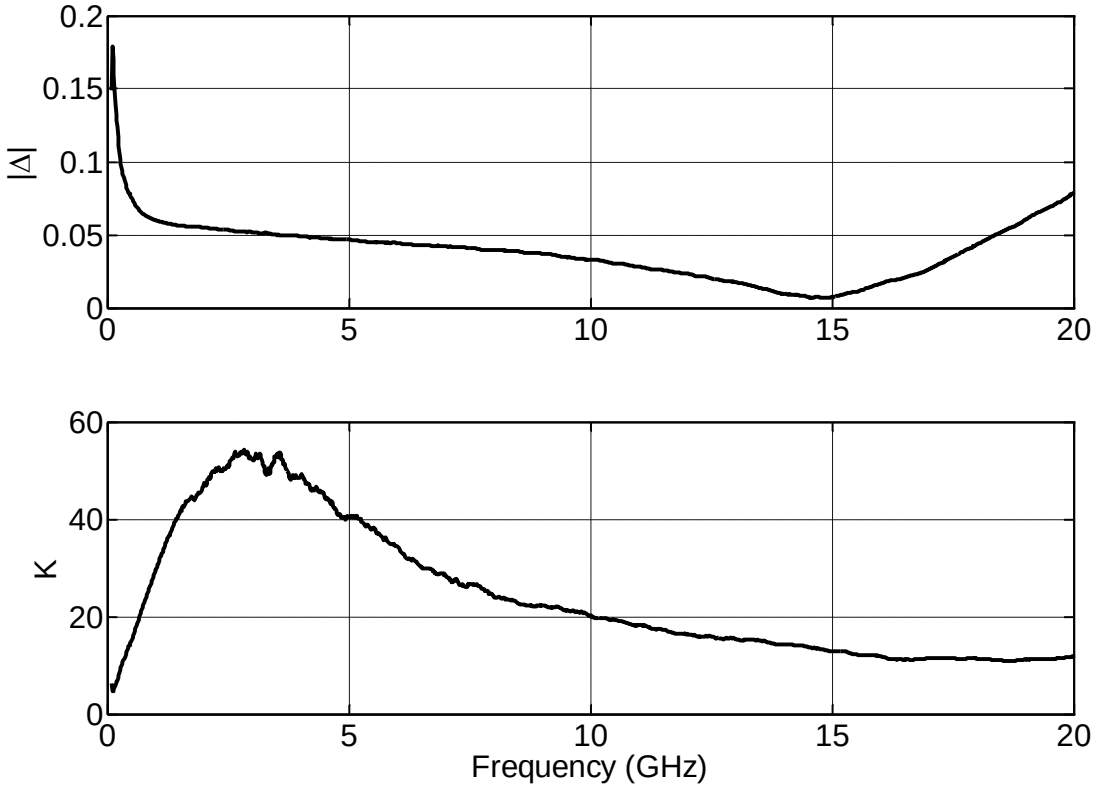


Figure 2-17. Rollet factor and auxiliary factor calculated from the measured S-parameters from 100 MHz to 20 GHz.

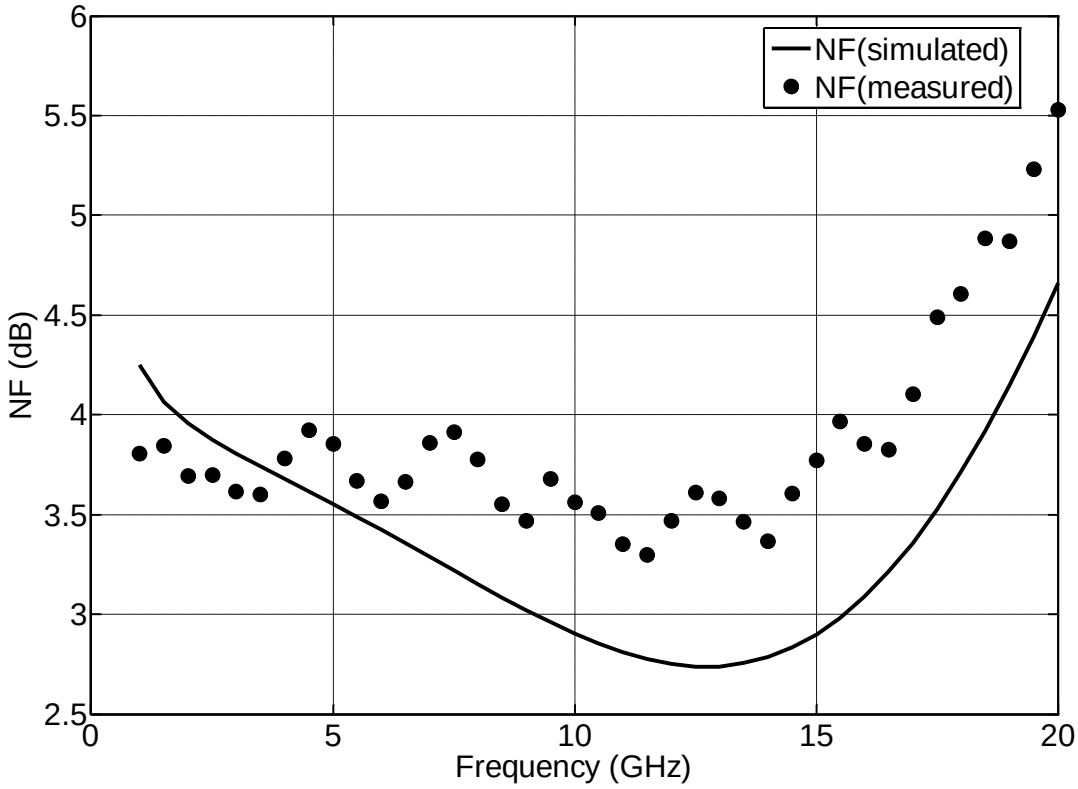


Figure 2-18. Simulation and measurement results of noise figure from 1 GHz to 20 GHz.

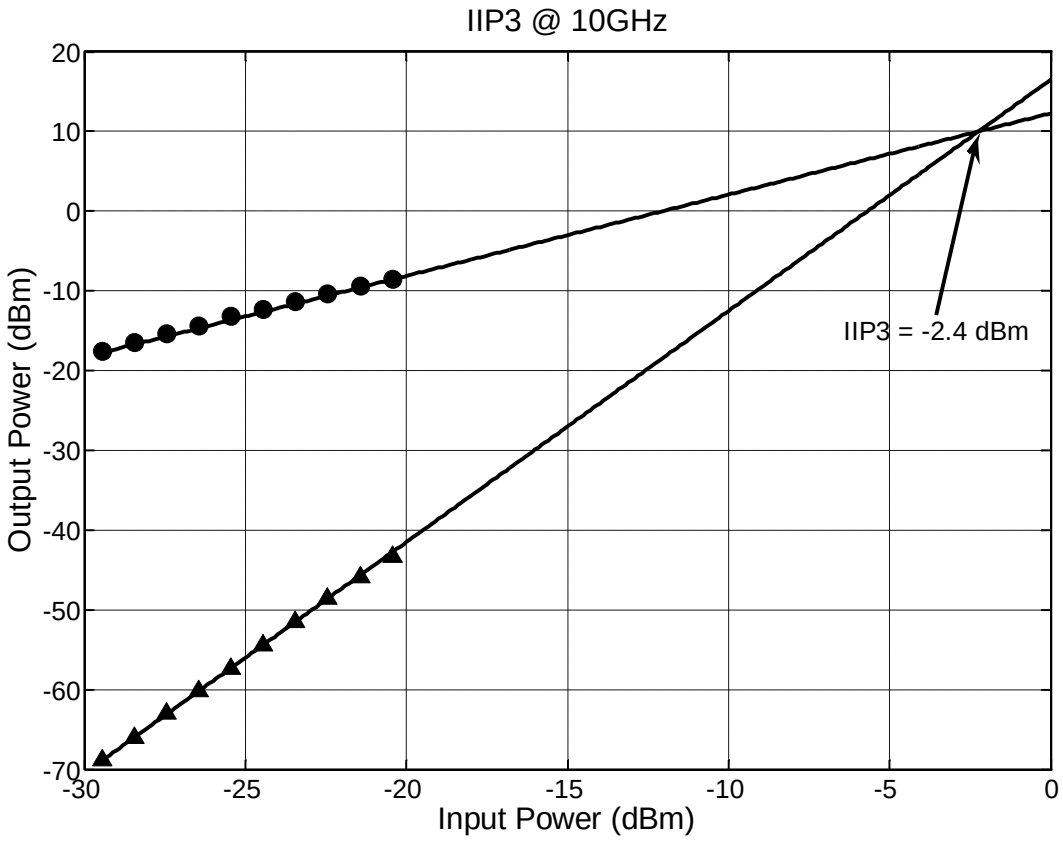


Figure 2-19. Measurement results of the two-tone test to determine IIP3 at 10 GHz.

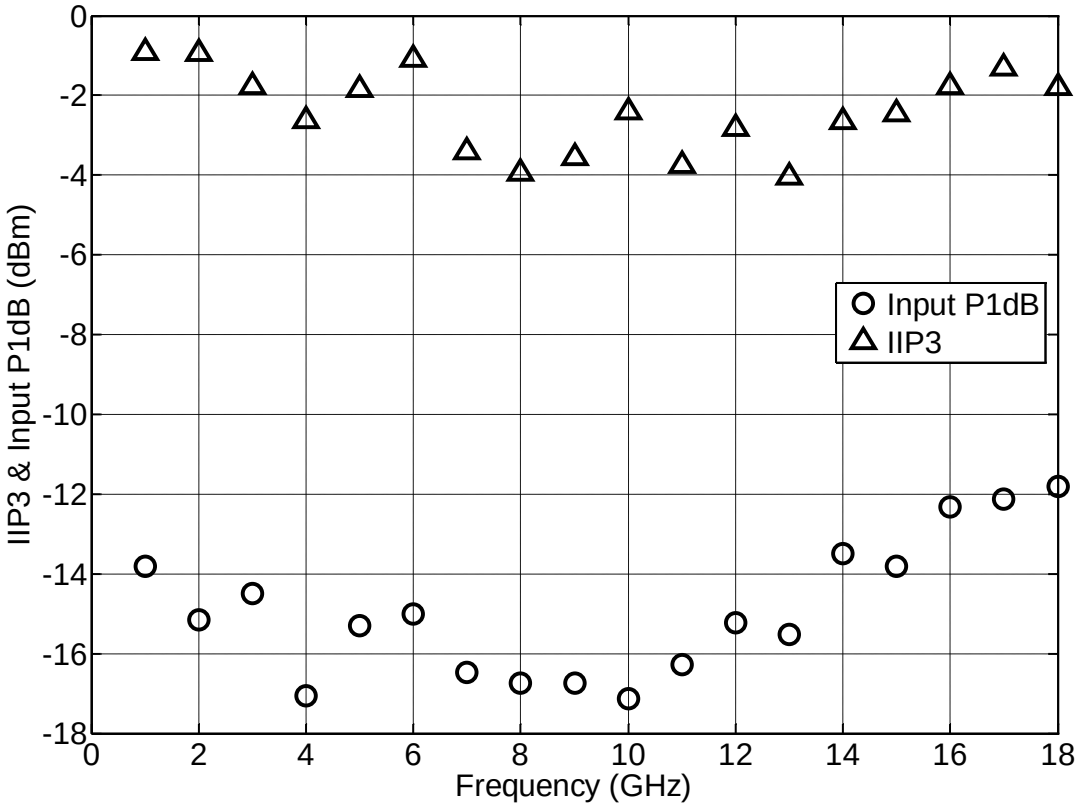


Figure 2-20. Measurement results of IIP3 and Input P1dB from 1 GHz to 18 GHz.

Table 2-1. Performance comparison with recently published works

	BW (GHz)	S21 (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	FOM	Topology	CMOS Technology
This work	0.1-20	12.7	4.4	-2.5	12.6	9.43	Feedback	90nm Digital
[15]	0.1-8	16*	4.6	-9	16	N/A	Feedback**	90nm Digital
[16]	0.2-9	10	6.1	-8	20	0.23	Feedback**	90nm Digital
	0.2-3.2	15.5	3.13	-9	25	0.51	Feedback**	90nm Digital
[17]	0.5-7	19	2.25	-8	42	2.71	Feedback	90nm RF
[18]	0.5-8.2	25*	2.35	-10.5	42	N/A	Feedback	90nm RF
[19]	4-8	24.4*	2.2	-7.7	9.2	N/A	Feedback	90nm RF
[20]	3.1-10.6	9.2	5.55	7.25	23.5	5.44	Feedback	0.18µm
[22]	0-6	15.3	3.85	-12	3.4	2.64	Feedback***	90nm Digital
[23]	2.9-11	16	4	N/A	9.5	N/A	Common gate	0.18µm
[13]	2.7-9.1	10	5.35	1	7	4.74	Distributed	0.18µm
[14]	0.04-6.2	8	5.2	3	9	3.73	Distributed	0.18µm

NF and IIP3 listed in this table are average values for fair comparison.
*Voltage gain
**Differential resistive feedback
***feedback using a source follower (all the other feedback is resistive)

CHAPTER 3
DESIGN OF A MULTI-DECADE GHZ BANDWIDTH LOW NOISE AMPLIFIER USING GAN HEMT MMIC TECHNOLOGY

3.1 Design Considerations of GaN HEMT MMIC Wideband LNAs

In Chapter 2, an LNA with multi-decade GHz bandwidth using UMC CMOS 90 nm process was reported. The detailed design, analysis and complete measurements were presented. It was demonstrated that CMOS technologies are capable of high gain, ultrawide bandwidth and low noise with scaling down of channel lengths. However, since its electron mobility and saturated electron velocity are much lower than those of III-V devices, the thickness of the oxide layer under the gate must be reduced to keep high drain current and transconductance. This leads to high parasitic capacitances (C_{gs} and C_{gd}) and low gate-drain breakdown voltage. Another drawback of CMOS processes compared with III-V semiconductor processes is its low junction breakdown voltage due to narrow band gap. Finally, regular CMOS processes cannot handle as much heat as III-V devices, which prevents them from being used for high voltage and high power applications. Although laterally diffused metal oxide semiconductor (LDMOS) transistors are developed for silicon CMOS to handle high voltage and high power systems, its retained low electron mobility and even higher device parasitic capacitances makes them unsuitable for applications at frequencies higher than 10 GHz.

On the other hand, Gallium-Nitride (GaN) high-electron mobility transistors (HEMT) technology has a much higher electron mobility and saturated electron velocity, a wider band gap, and better thermal conductivity. Recently, low noise property has been reported [24]-[25]. With all these advantages, high gain, highly linear and wideband low noise amplifiers are possible by using GaN technology. The combination of the high power capability, high linearity and low

noise can eliminate filters and protection circuits proceeding LNAs in receiver chains. Therefore, the overall noise figure and dynamic range of a receiver can be significantly improved.

Four architectures of ultra-wideband CMOS LNAs are discussed in Chapter 2. However, no filter-match LNA or common-gate LNA using GaN technology has been reported in the literature yet, and only the other two architectures can be found. K. W. Kobayashi et al. demonstrated two DAs using the conventional cascode DA topology and the capacitively coupled cascode DA topology [26]. Figure 3-1 shows the schematics, die photograph, S-parameters and noise figures. Both of the LNAs have a -3 dB bandwidth of 0-20 GHz with good two-port matching. A summary table of GaN MMIC DAs was given which shows that the two DAs have the widest bandwidth among all the GaN DAs. Despite a high output-referred third-order intercept point (OIP3) and output-referred 1 dB compression point (Output P1dB), the two LNAs consume 9000 mW and 12000 mW respectively.

Like CMOS LNAs, negative shunt-feedback GaN LNA can have a gain as high as those DAs and the potential to have a comparable bandwidth with the DAs. S. E. Shih et al. from Northrop Grumman Space Technology (NGST) reported several GaN MMIC LNAs using resistive-feedback architecture with much lower power consumption [27]-[28]. Dual-gate device structure is utilized to realize the cascode topology with much smaller parasitic capacitances, as shown in Figure 3-2. Two LNAs with a -3 dB bandwidth of 0.3-4.5 GHz and one 1.2-15 GHz LNA were presented in [27]. The gains of all the three LNAs are slightly higher and flatter than those of the DAs above but their input matching is not as good as that of those DAs. Except the first one, S11 of the other two is -8 dB or higher across their whole bandwidths. Figure 3-3 shows the results of the third one. Another LNA with the same device structure and similar schematic was presented in [28]. A peak gain of 18 dB, a -3 dB bandwidth of 0.3-5.5 GHz, and

2.8 dB average noise figure were achieved. Again, the input matching is not so good with S11 higher than -8 dB within the bandwidth.

In Chapter 3, it will be shown that a resistive-feedback LNA can attain not only a high gain but also a comparable bandwidth and two-port matching with DAs. A -3 dB bandwidth of 1-25 GHz with 13 dB peak power gain is achieved with dramatically lower power consumption and smaller area than the DAs in [26]. This GaN LNA is believed to have the widest bandwidth among all GaN HEMT MMIC LNAs reported to date. Process information and detailed design approach and will be presented. Complete simulation results will be provided and discussed. Finally, a comparison between CMOS technology and GaN HEMT technology will be briefly discussed.

3.2 GaN HEMT Device and Process

The proposed LNA was fabricated using NGST's AlGaN/GaN HEMT MMIC process [29]. The AlGaN/GaN material is formed by metal organic chemical vapor deposition (MOCVD) process on a 3-inch semi-insulating SiC substrate instead of GaN substrate to lower the cost. As shown in Figure 3-2 A), the structure consists of AlN nucleation layer, GaN buffer layer, AlN interlayer, AlGaN barrier layer and a GaN layer. All the layers are undoped. A separation of the electrons from their donors at the interface between the GaN buffer layer and AlN interlayer provides the HEMT transistor excellent high frequency performance with low noise and high power properties. Consequently a two-dimensional electron gas (2DEG) is generated, as the electrons are bound to a very thin layer where only two-dimensional movements are allowed. At room temperature, the carrier density of the 2DEG is typically $1x10^{13}$ cm^{-2} which results in a high mobility of 1600 $cm^2/(V \cdot s)$. All the superior performances of GaN HEMTs come at a price. The process is much more expensive than a CMOS process with similar feature length because of not only the materials but also accurately controlled layers and steep doping gradients.

The GaN HEMT gate with a length of 0.2 μm is made of Pt/Cu by using e-beam lithography and passivated with Si3N4 by using plasma-enhanced chemical vapor deposition (PECVD). Based on the measurements of the device, the gate-to-drain breakdown voltage, threshold voltage, peak transconductance, unity current gain frequency and unity maximum power gain frequency are respectively 60 V, -7 V, 300-500 mS/mm, 60-70 GHz and 80 GHz. Besides, the technology has two metal layers for interconnects with airbridges, NiCr thin film resistors and metal-insulator-metal (MIM) capacitors. The MIM capacitors are made up of the top metal layer, the first interconnect layer and two layers of Si3N4 dielectric. All the interconnects and inductors are using the thicker top metal layer due to low sheet resistance and parasitic capacitance.

Notwithstanding very different structure of the GaN HEMT from that of an NMOSFET, for the first order, the drain current obeys the classic square law like a long-channel NMOSFET. The drain current in triode region and saturation region are respectively given by

$$I_D = \mu_n C_H \frac{W}{L}\left((V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \tag{3-1}$$

$$I_D = \frac{1}{2} \mu_n C_H \frac{W}{L} (V_{GS} - V_{th})^2 , \tag{3-2}$$

where

μ_n: Electron mobility

$C_H = \frac{\epsilon_H}{d}$ where ϵ_H and d are dielectric constant and thickness of the AlGaN heterostructure.

V_{th}: Threshold voltage.

Equation 3-1 and Equation 3-2 show that the relationship between the drain current and the gate voltage is the same with that of a long-channel NMOSFET if ϵ_H, d and C_H are treated as ϵ_{ox},

t_{ox} and C_{ox} respectively. Most of the design approaches in Chapter 2 can be applied to GaN HEMT MMIC LNAs with some modifications.

3.2 Circuit Design

From circuit design point of view, one of the main differences between GaN MMIC process and a CMOS process is the size of the on-chip components of the former is much larger than the latter that the transmission line effects must be taken into account. In spite of the larger components, since the distance between the two metal layers and the substrate is over ten times than that of the CMOS 90 nm digital process, the parasitic capacitances may not be significantly higher than the CMOS process. Additionally, since the top metal layer is much thicker than that of the CMOS process, parasitic resistance and inductance are lower which leads to lower loss and attenuation of inductors and microstrip transmission lines. Considering the target upper -3 dB frequency is higher than 20 GHz, transmission line effects must be taken into account and thus all the interconnects are treated as transmission lines. To reduce the chip area, some lumped inductors and capacitors are replaced by microstrip lines with certain width and length. However, since a transmission line can be either inductive or capacitive at different frequencies, transmission lines must be carefully designed and adjusted. Even so they cannot thoroughly take the place of the inductors and capacitors within the bandwidth of interest. Some inductors and capacitors are still necessary. All the inductors and transmission lines were designed and simulated using Agilent ADS and Momentum to ensure accuracy.

Figure 3-4 shows the simplified schematic of the LNA. Wideband power gain and input matching are based on a shunt feedback resistor Rf. A capacitor in series with the feedback resistor and a shunt resistor Rbias are added for a negative bias voltage on M1. To simplify the external bias network, the gate biases of the two stages are connected such that only one gate bias voltage is required. The inductor Lg in series with the gate of M1 significantly enhances the

bandwidth. Transmission lines, TL1-3, acting as inductors at frequencies higher than 15 GHz, further extend the bandwidth by delaying high-frequency current variation. Consequently, the parasitic capacitance at each node is charged by more current in the same amount of time. In other words, the transmission lines increase high-frequency responses with less effect on low-frequency parts. As a result, a flat gain is achieved in an ultra-wide bandwidth. Simulation result in Figure 3-5 shows that TL1 at M1 drain node significantly increases the bandwidth, and the inductor Ls substantially improves the input matching at mid- and high- frequencies. Both Lg and Ls have small values due to the shunt feedback loop. The shunt-peaking technique is implemented by using TL4 at the first stage and TL5 and Ld at the second stage.

3.3 Simulation and Measurement Results

Figure 3-6 shows the die photograph with a chip area of 1.2 mm x 1.2 mm including pads. The active area including all inductors is 0.9 mm x 0.7 mm. The LNA was simulated using Agilent ADS and measured on wafer. Figure 3-7 and Figure 3-8 show a good agreement between the simulated and measured S-parameters. The measured S21 is relatively flat within the bandwidth, reaches 13 dB peak value at 10 GHz, and drops by 3 dB at 25 GHz. The measured S11 is below -10 dB from 1 GHz to 23.5 GHz and below -9 dB in the rest of 1.5 GHz bandwidth, which shows a good input matching. The LNA shows a good output matching and isolation over the entire bandwidth. The stability was also analyzed by the K-Δ test. The Rollet stability factor and the auxiliary factor respectively defined by Equation 2-11 and Equation 2-12 were calculated from the measured S-parameters. It shows that the LNA is unconditionally stable within the bandwidth. Simulation shows that unconditional stability is achieved both within and outside the bandwidth. The noise figure ranges from 2.5 dB to 3.3 dB with a 2.9 dB average value shown in Figure 3-8. The gate bias was designed to have the noise figure very close to the minimum noise figure.

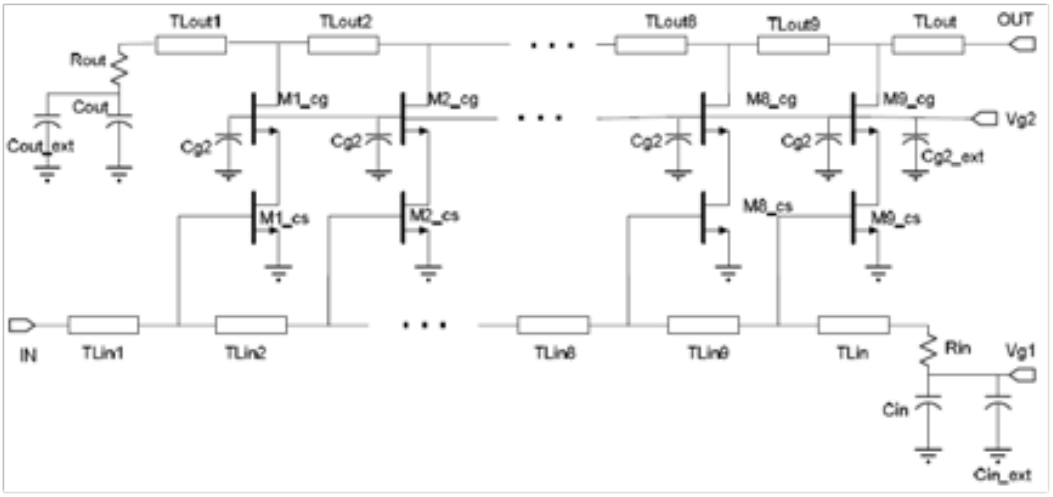
The linearity characteristics IP3 and P1dB were measured. Two RF sources with 11 MHz separation were fed into the LNA input to obtain the IP3 while one single RF source was used for P1dB. Figure 3-10 shows the fundamental output power and the third order intermodulation distortion (IMD3) as a function of the input power at 22 GHz. Figure 3-11 shows the OIP3 from 28.5 dBm to 33.5 dBm, and the Output P1dB from 17.5 dBm to 20 dBm, over the entire bandwidth.

The LNA was biased with a gate voltage of -3.5 V and a drain voltage of 12 V. The whole chip draws 75 mA from the power supply, resulting in a power consumption of 900 mW, which is significantly lower than previously published GaN MMIC LNAs with similar gain and -3 dB bandwidth. Table 3-1 compares this LNA with recently published GaN HEMT MMIC LNAs. For a fair comparison, the bandwidth is determined by the -3 dB bandwidth of input matching with -6 dB or lower, and the average noise figure, OIP3 and Output P1dB values within bandwidth are used. As shown in Table 3-1, this LNA achieves a larger FOM than two DAs with widest bandwidth. This indicates again that DAs are not the best in terms of the FOM, although they have the potential to the widest bandwidth.

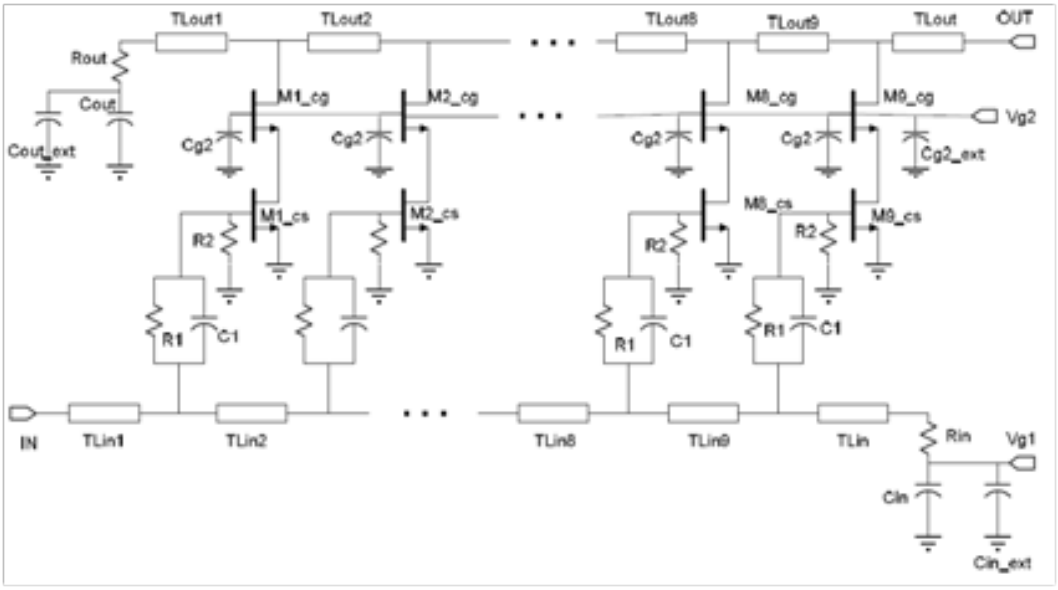
3.4 Comparison between wideband CMOS LNAs and GaN MMIC LNAs

Table 3-2 summarizes and compares the two processes and the two LNAs proposed in Chapter 2 and Chapter 3. Notwithstanding half of the unity current gain frequency, the GaN LNA exhibits a wider bandwidth when all the other small-signal performances are comparable mainly due to much higher electron mobility and thicker top metal. Also, the GaN LNA benefits from the much larger distance between the devices and the ground plane on the back of the wafer. The largest advantage of the GaN LNA is IP3 and P1dB which may be nearly 200 times higher than those of the CMOS. The GaN achieves a significantly higher FOM even though with higher power consumption and larger chip area. But the CMOS process is more compact and cheaper.

Moreover, PMOSFETs enable much more functions and topologies. Consequently, everything can potentially be integrated on a single chip which makes CMOS technologies much more attractive than GaN MMIC technologies for low-voltage low-power applications, whereas GaN technologies are of great interest to handle high frequency, high power, high linearity and low noise such as RF front-end of base stations and radars.

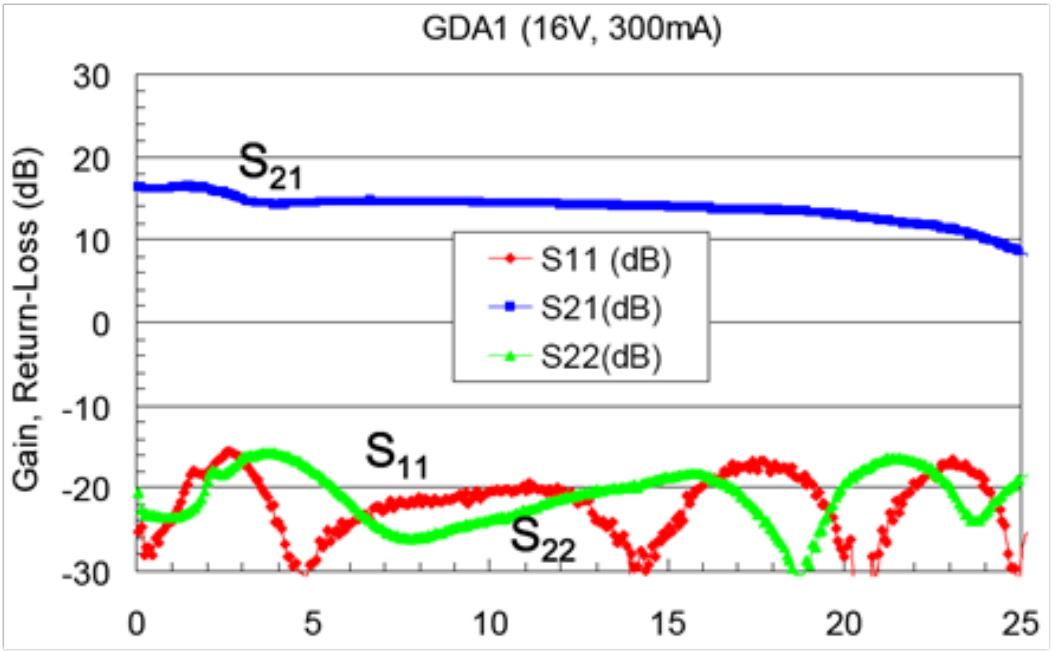


A

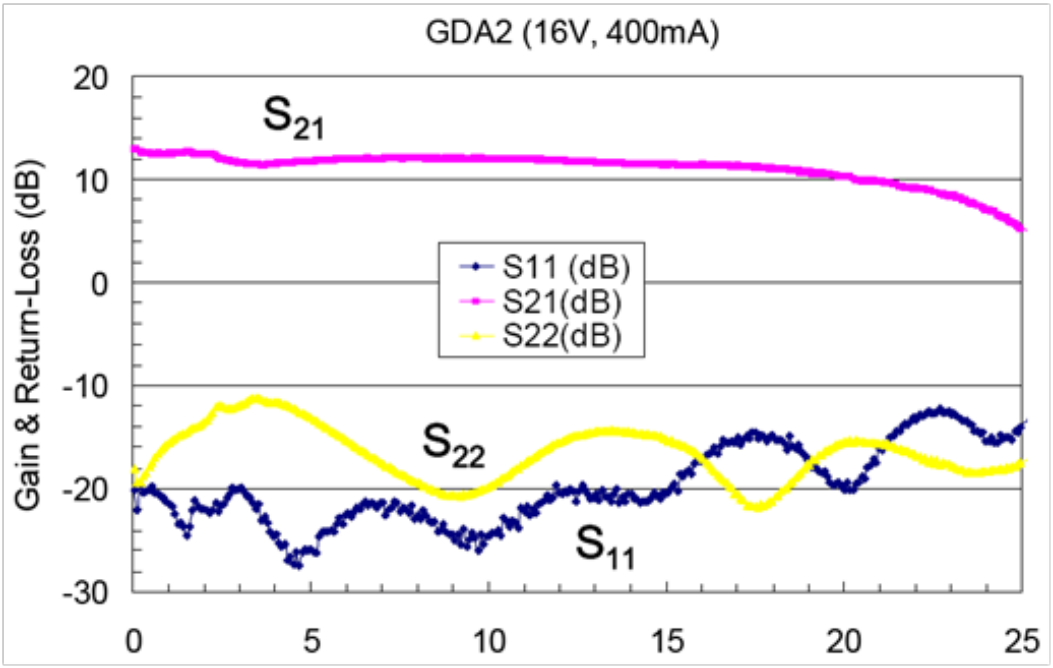


B

Figure 3-1. Results of A) B) schematics, C) D) S-parameters, E) noise figure and F) die photograph of the multi-decade GaN HEMT cascode DAs by K.W. Kobayashi et al. [26].

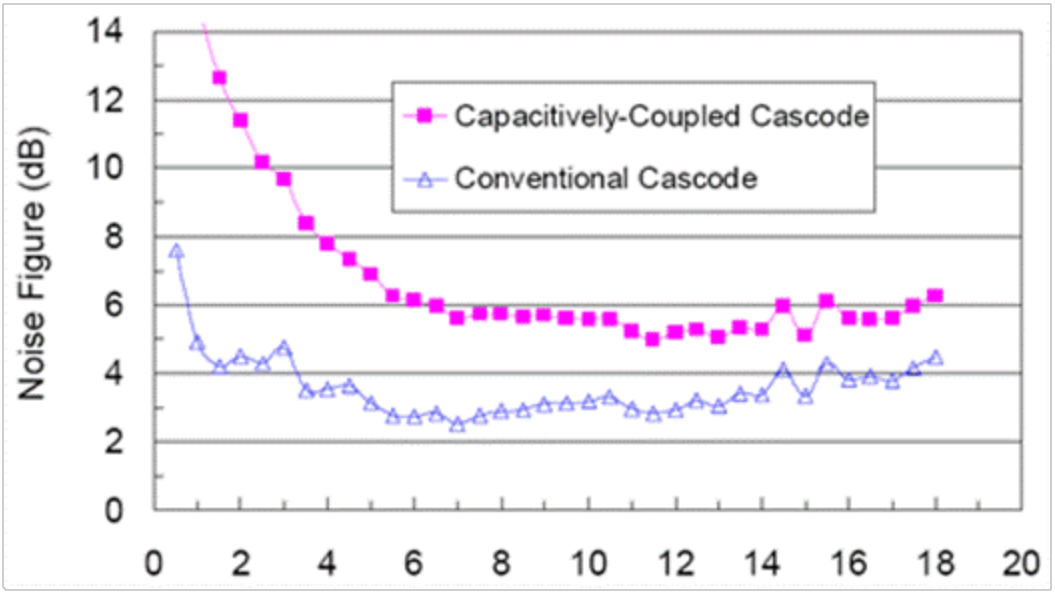


C

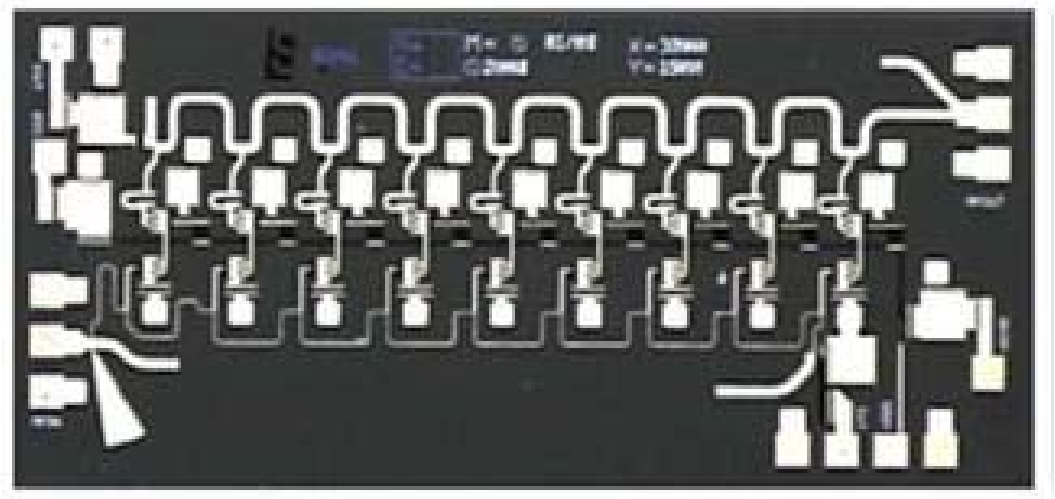


D

Figure 3-1. Continued

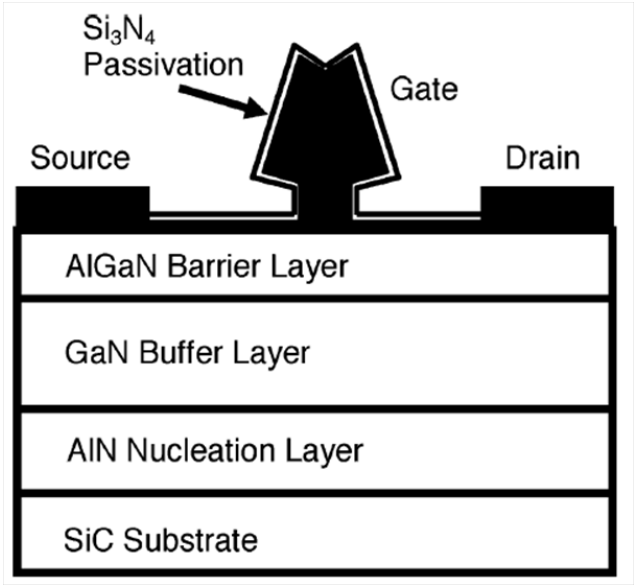


E

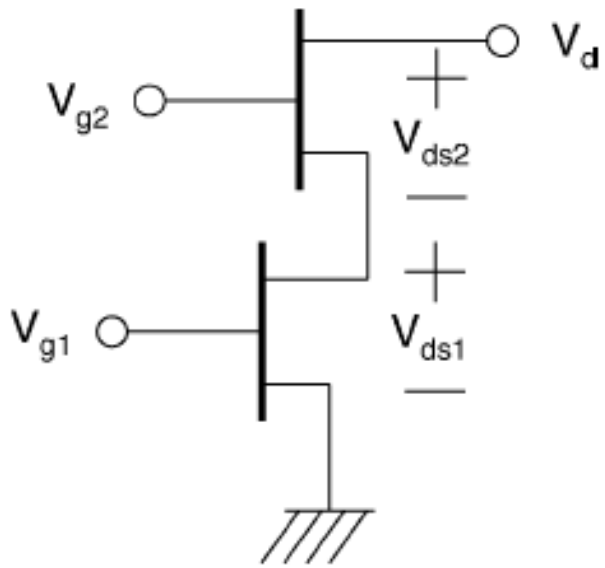


F

Figure 3-1. Continued

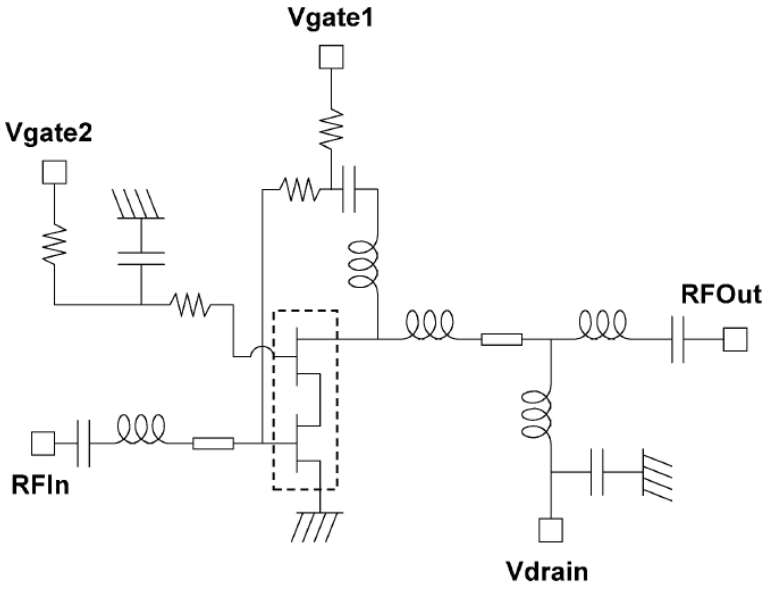


A

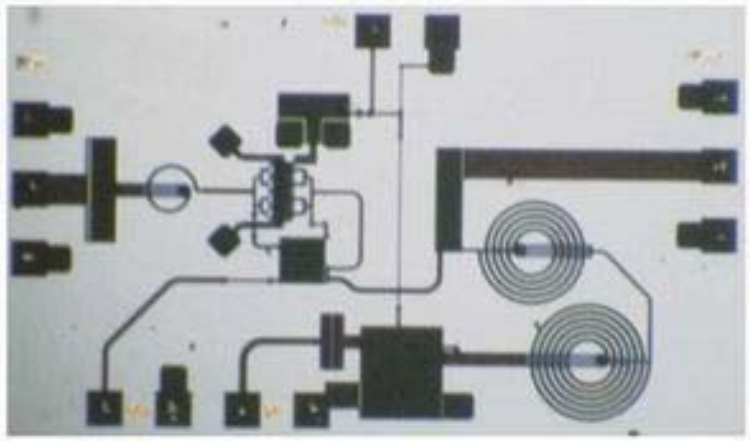


B

Figure 3-2. A) AlGaN/GaN dual-gate device structure and B) equivalent schematic of the dual-gate structure [27].

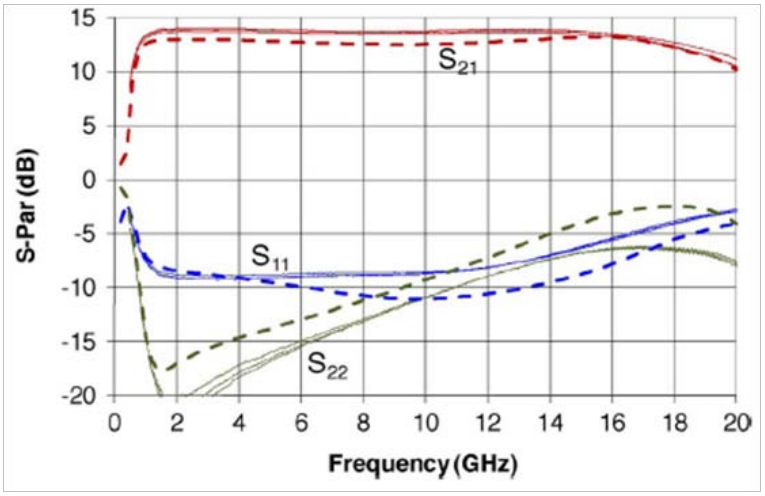


A

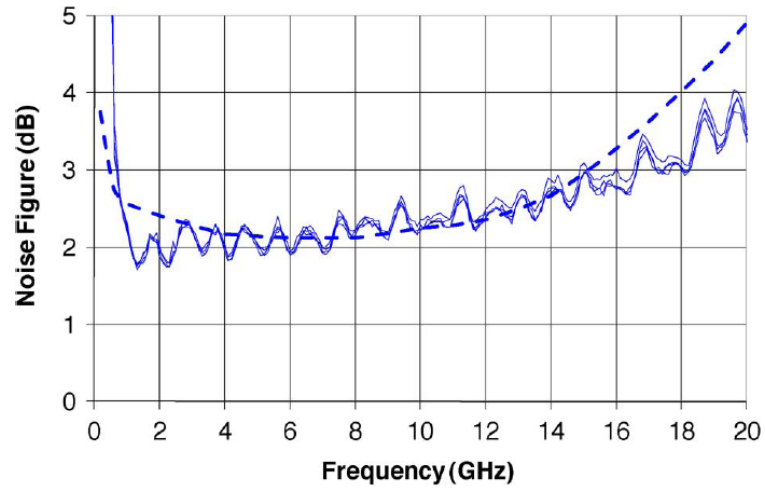


B

Figure 3-3. Results of A) schematics, B) die photograph, C) S-parameters and D) noise figure of the third GaN dual-gate HEMT LNAs by S.-E. Shih et al. [27].



C



D

Figure 3-3. Continued

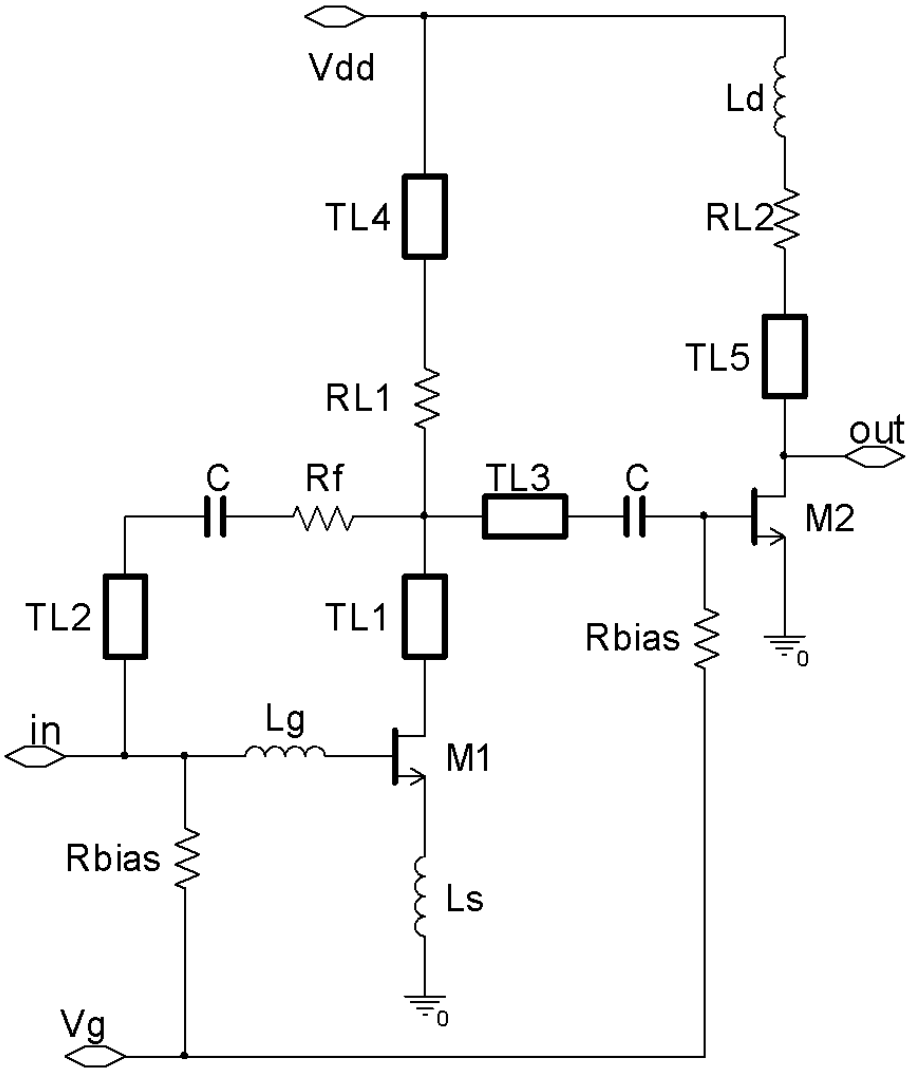


Figure 3-4. Simplified schematic of the GaN HEMT MMIC LNA.

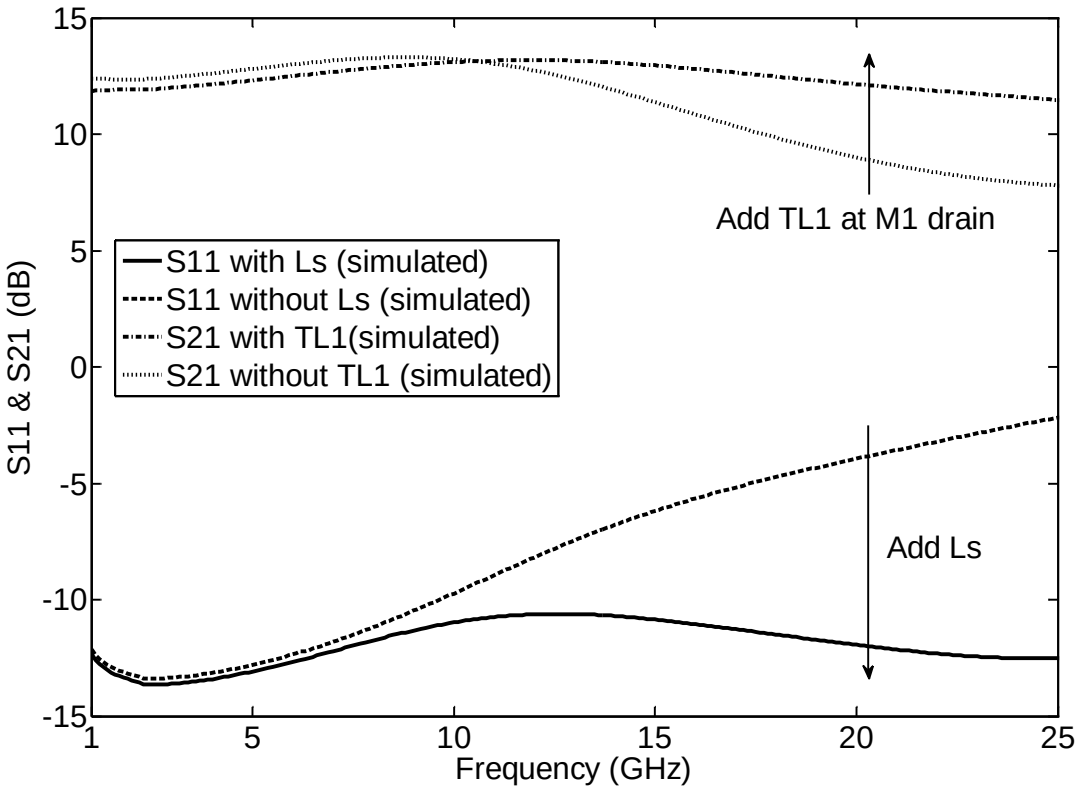


Figure 3-5. Simulation results of the bandwidth enhancement due to TL1 and Ls.

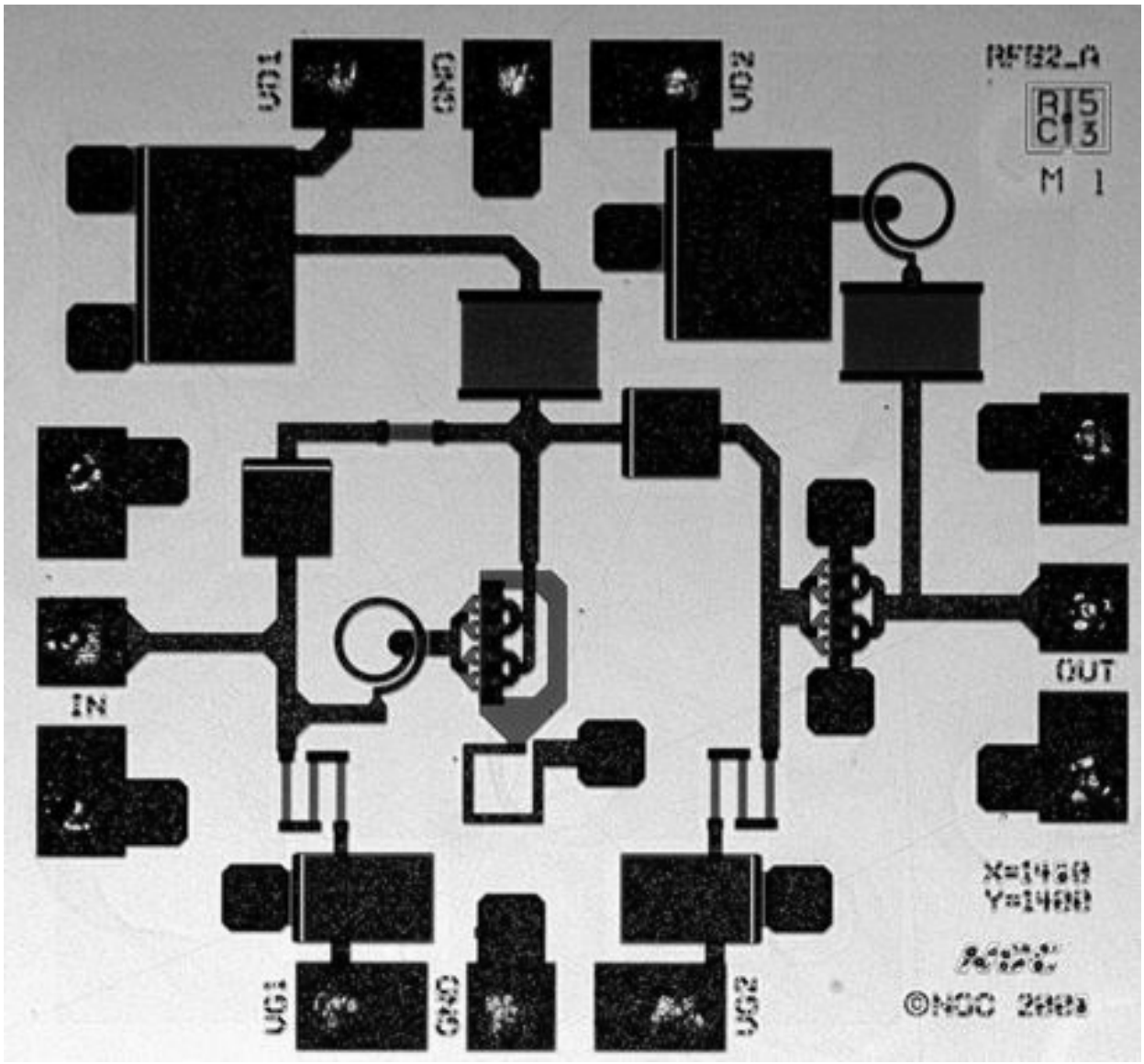


Figure 3-6. Die photograph of the proposed LNA. The chip size is 1.2mm x 1.2mm with the active area (including all the inductors) of 0.9mm x 0.7mm.

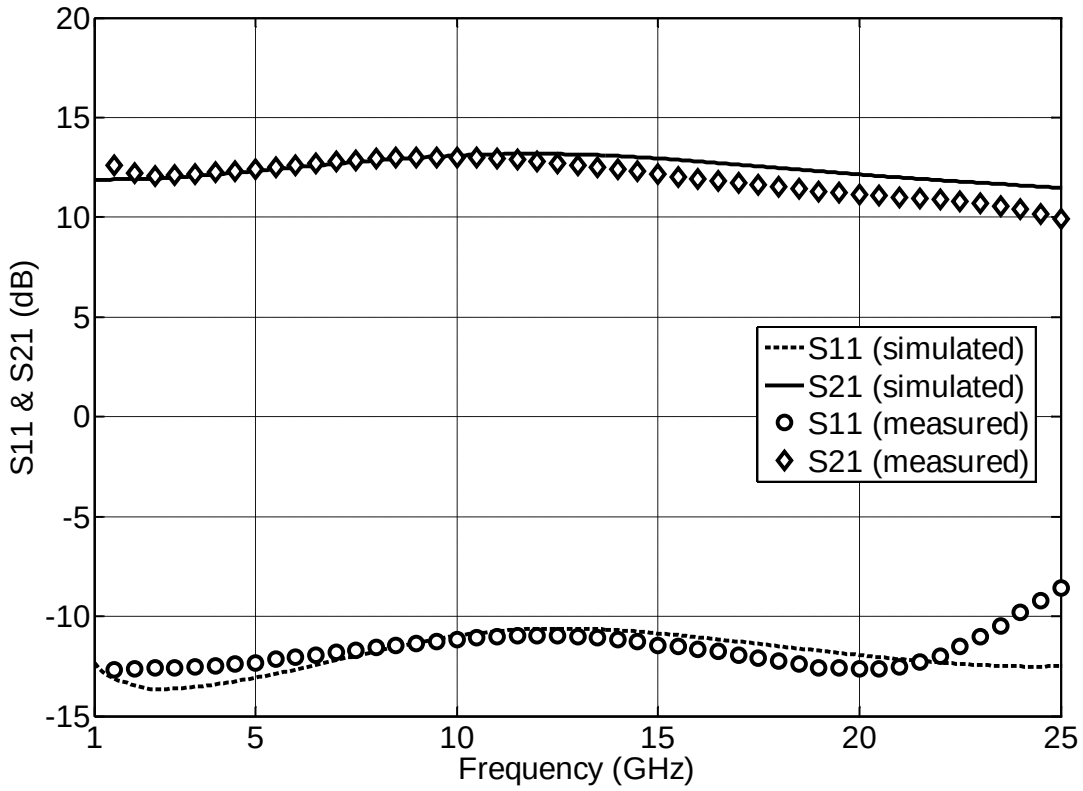


Figure 3-7. Simulation and measurement results of S11 and S21.

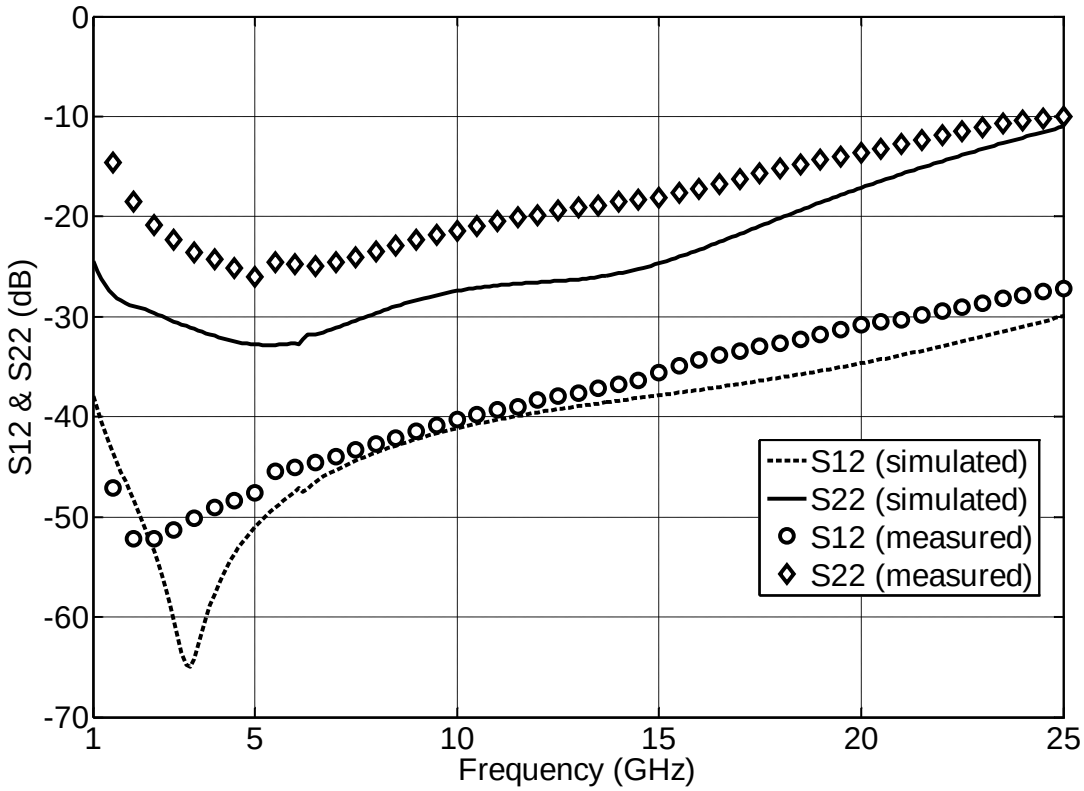


Figure 3-8. Simulation and measurement results of S12 and S22.

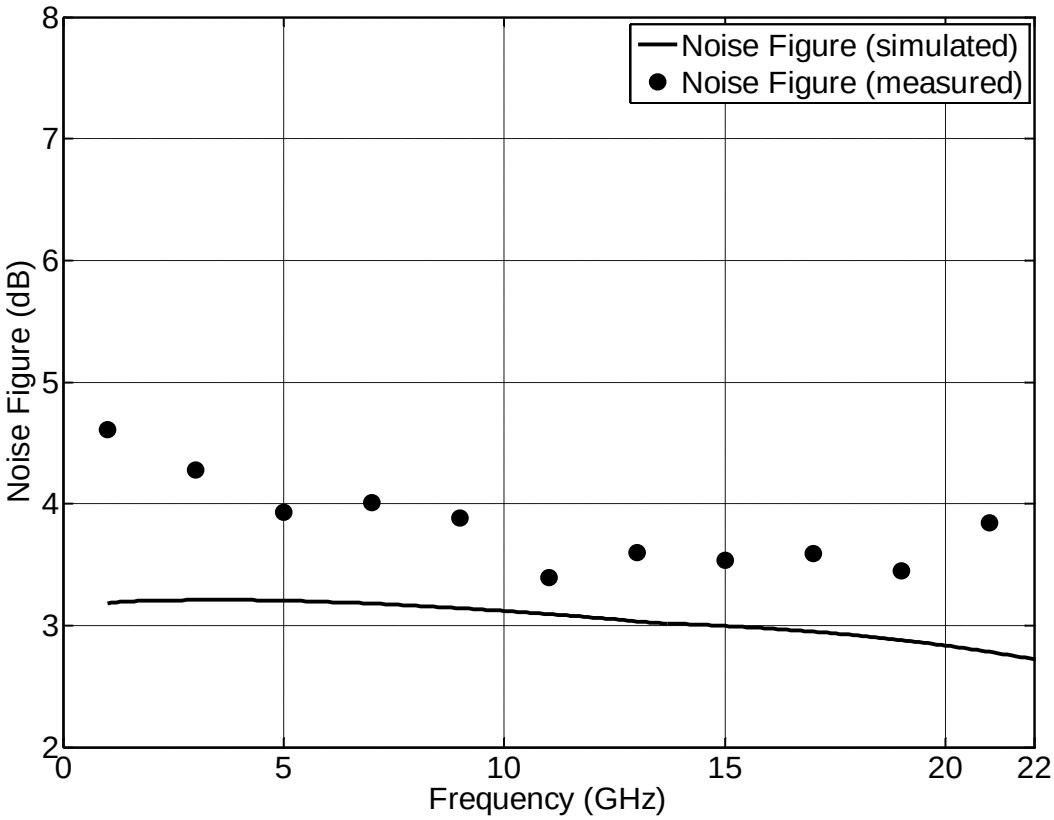


Figure 3-9. Simulation and Measurement results of noise figure from 1 GHz to 21 GHz.

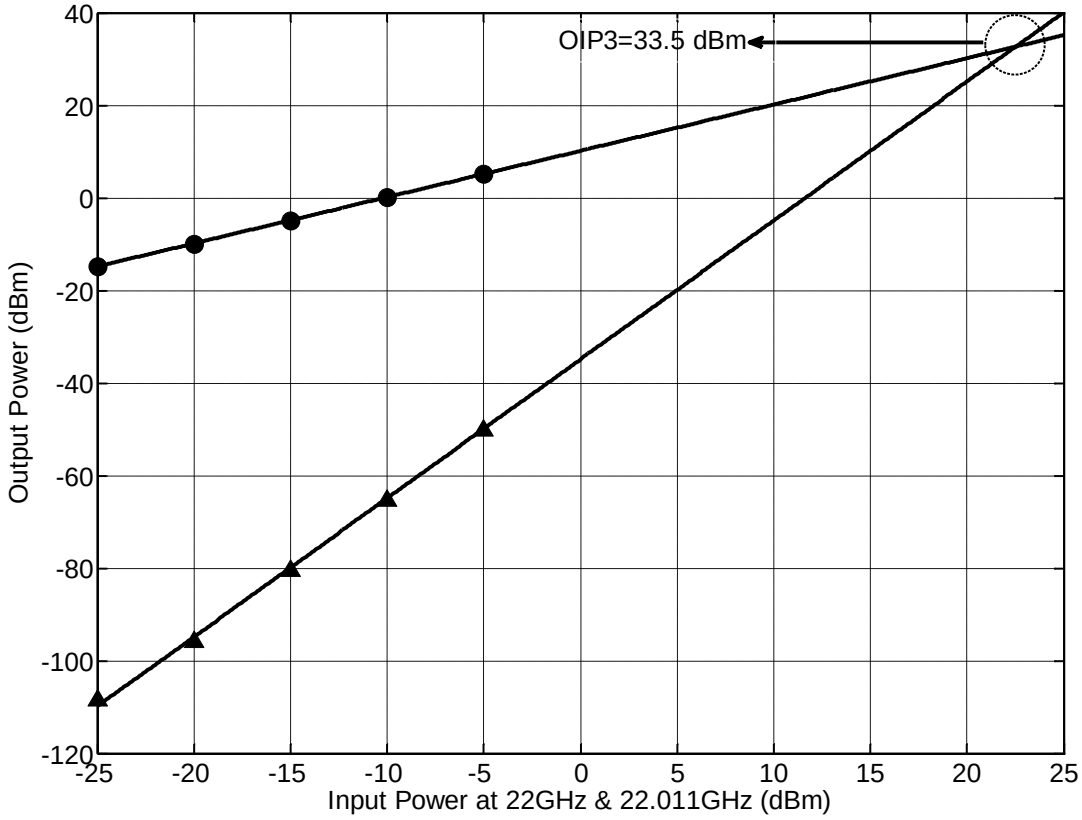


Figure 3-10. Measured fundamental output power at 22 GHz and IMD3.

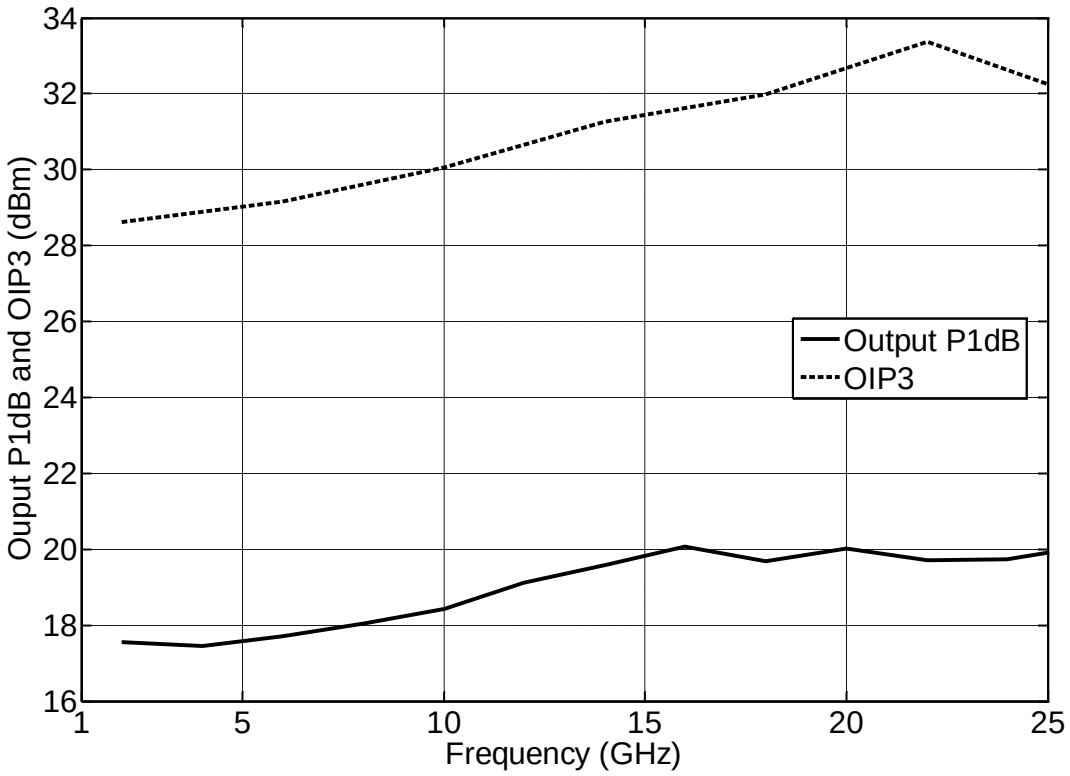


Figure 3-11. Measurement results of OIP3 and Output P1dB from 1 GHz to 25 GHz.

Table 3-1. Performance comparison with recently published works

	BW (GHz)	S21 (dB)	NF (dB)	OIP3 (dBm)	OP1dB (dBm)	Power (mW)	FOM	Topology	GaN HEMT
This work	1-25	13	3.9	31	19	900	22.9	Feedback	0.2µm
[27]	0.3-4.5	17.7	1.6	-	-	1000	-	Feedback	0.18µm dual gate
	1.2-15	13.3	2.4	-	-	500	-	Feedback	0.18µm dual gate
[28]	0.3-5.5	18	2.8	-	20	1000	-	Feedback	0.2µm dual gate
[30]	4-7.5	14.5	1.9	24	-	150	-	Common source	0.15µm
[29]	1-9.5	17.7	1.9	30	-	800	-	Common source	Dual gate
[26]	0-20	16*	4.7	40	28	9000	11.2	Distributed	0.2µm
	0-20	12.5*	9.5	41	30	12000	2.4	Distributed	0.2µm

* Small-signal S-parameters were measured using lower drain voltages (16V) and thus lower power consumption.

Table 3-2. Performance comparison of the two processes and the two proposed LNAs

	GaN	CMOS
-3 dB Bandwidth (GHz)	1-25	0.1-20
S21 (dB)	13	12.7
Noise Figure (dB)	3.9	4.4
OIP3 (dBm)	31	8.7
Output P1dB (dBm)	19	-3.3
Power (mW)	900	12.6
Active Chip Area (mm^2)	0.9 x 0.7	0.45 x 0.26
FOM	22.9	9.43
Topology	Resistive feedback	Resistive feedback
Technology	0.2 µm	Digital 90 nm
Transit frequency (GHz)	70	140

CHAPTER 4
DESIGN OF A LOW-POWER 14-BAND FAST-HOPPING FREQUENCY SYNTHESIZER

4.1 Design Considerations of Multi-Band Fast-Hopping Frequency Synthesizers

As introduced in Chapter 1, MB-OFDM UWB is a good example of wideband frequency agile systems for wireless communication applications. To avoid the extremely crowded 1-2 GHz band, the Federal Communications Commission (FCC) released 3.1–10.6 GHz for the use of UWB [31]. Based on the regulations, UWB is required to have a bandwidth of 500 MHz or higher, with a power spectral density (PSD) of -41.25 dBm/MHz or lower. Its spectrum consists of 14 bands with a bandwidth of 528 MHz for each band. The 14 bands are categorized into five groups, with three bands in each band group except the last two bands in band group 5, as shown in Figure 1-3. The first band group, called Mode 1, is mandatory, whereas the remaining four groups are optional for the system capability extension.

Except for the large number of bands and the ultra-wide bandwidth, another challenging requirement is from its frequency hopping diagram. Figure 4-1 shows the frequency hopping diagram of Mode 1. The settling time of frequency hopping is demanded to be shorter than the guard interval duration of 9.47 ns. This requirement is extremely difficult for a single VCO-based phase-locked loop (PLL). G.-Y. Tak et al. presented a PLL with a shortest settling time reported up to date. The settling time is around 150 ns still 15 times longer than the required value. To obtain a basic understanding, consider an integer-N PLL with a second-order loop as shown in Figure 4-2 [32]. The settling time is inversely proportional to the loop bandwidth, which is given by [33]

$$T_{settling} \propto \frac{1}{BW} \bullet \ln\left(\frac{f_{step}}{f_{error}}\right), \tag{4-1}$$

where

BW: Loop bandwidth

f_{step}: Amplitude of the frequency shift

f_{error}: Final desired frequency accuracy which is 1 kHz.

It is desirable for the reference frequency to be 10 times higher than the loop bandwidth, to avoid discrete-time effects and stability issues. Furthermore, Equation 4-1 is based on a linear feedback system. Nonlinear behaviors, such as cycle slips, substantially increase the settling time due to a large fstep of MB-OFDM UWB. Therefore, the input reference frequency of the phase-frequency detector (PFD) can be as high as 5 GHz to achieve a settling time lower than 9 ns. This poses great challenges to the design of both a GHz-range PFD and charge pump (CP) with low noise and mismatch and a GHz frequency reference source with low phase noise.

Although the bandwidth, the number of bands and the settling time are very challenging, other specifications are modest. Table 4-1 lists a summary of the minimum requirements of UWB frequency synthesizer [31].

4.2 Published Architecture Overview

All published MB-OFDM UWB frequency synthesizers can be categorized into four types of architectures, namely 1) multiple plain PLL multiplexing (PLL output frequency is fixed), 2) single-side band (SSB) mixing, 3) multiple frequency-hopping PLL multiplexing, and 4) delay-locked loop (DLL) based frequency multiplication.

The multiple PLL multiplexing architecture is the most straightforward and exploits three or more PLLs. This architecture was first implemented by B. Razavi et al. in 2005 [34]. Each band was generated by an independent PLL, as shown in Figure 4-3. Since all three PLLs are working at three different fixed frequencies and no frequency change is triggered, the settling time results from only the band-select action, which can easily be much shorter than 9 ns. Also, each PLL can be designed and optimized individually for a fixed frequency. The phase noise

requirement is easily met by using LC-VCOs. This architecture was then improved by K. Stadius et al. in 2007 [33]. It utilized three PLLs with 6 VCOs to achieve 6 bands as shown in Figure 4-4. Although the spurs are low with average power and area consumption, this architecture cannot be extended to 14 bands, simply because it will require 7 PLLs, 14 VCOs and a high-frequency 7-to-1 multiplexer. With a large number of PLLs and VCOs running on a single chip, the interfere will be significant due to the poor isolation of bulk CMOS processes, and most power will be wasted since only one PLL and VCO is selected at a time.

The SSB mixing architecture is the most popular [35]-[41]. It was first proposed by A. Batra et al. in [42]. Note that all the frequency bands and their middle frequencies are integral multiples of 264 MHz as shown in Figure 4-5. This property makes it possible to synthesize all the 14 bands by using only one or two plain PLLs with frequency divider chains. The outputs of the different stages of the frequency divider chains are selected and mixed by using SSB mixers. Then different frequencies are generated. Similarly, without frequency change, the settling time due to only SSB mixers and multiplexers can easily meet the specification. The drawback is that the outputs of the SSB mixers may contain a few undesired tones. As a result, the output spectrum is full of spurs some of which are higher than those of the first architecture. But the highest spur power of most SSB-mixing based synthesizers is from -35 dBc to -40 dBc which is 11-16 dB lower than the specification. The first 14-band CMOS UWB frequency synthesizer was reported by C.-F. Liang in 2006 [37]. Two PLLs were employed. With three stages of SSB mixers, three stages of multiplexers and two frequency divider chains (including a complicated quadrature divide-by-3 circuit), the block diagram is of high complexity, as shown in Figure 4-6. The power consumption is 162 mW which is the highest among all published synthesizers. Despite the high spurs generate by SSB mixers, it will be shown later that this SSB mixing

method is the only one with the capability of the full 14 bands so far. Also, it is extendable to frequencies even much higher than 10 GHz for other frequency agile systems with wider bandwidth.

Reviewing Figure 4-1, we can find that there is an alternative solution to release the 9 ns settling time to the symbol period of 312.5 ns. One PLL is employed to generate the present frequency for 312.5 ns. The other PLL will have 312.5 ns to settle down to the next frequency. When a multiplexer switches to the next frequency, the second PLL is ready. The two PLLs switch by turns. Using this scheme, compared to the first architecture, the number of PLLs can be reduced with an achievable switching time. The design target of the settling time should be less than 200 ns for a safety margin. This type of architecture was proposed by G.-Y. Tak et al. in [43] and a fast settling PLL was demonstrated as mentioned earlier. The block diagram is shown in Figure 4-7. Another PLL was employed to generate a high-frequency reference of 528 MHz. In spite of the simple looking architecture of the frequency synthesizer, the PLL design is quite elaborate and the whole synthesizer was not practically demonstrated in [43]. The power consumption of only the single PLL without even considering the buffer is 116 mW and the chip area is 0.7 mm x1.1 mm. With two PLLs and a 4-to-1 quadrature multiplexer, the power consumption will be more than 200 mW with nearly double chip area. The synthesizer covers only 6 bands. To obtain all the 14 frequencies, either VCOs with a very broad tuning range or more parallel VCOs with are needed. Also a very complicated high speed prescaler with a number of moduli is required. Larger frequency shifts will further challenge the settling time. Either way will drastically increase the power consumption. As a result, this architecture is probably the most power consuming. In summary, it is not the best choice due to the high power and area consumption and high demands on circuit design.

As discussed earlier, the 9 ns settling time is basically unachievable for VCO-based PLLs using the current CMOS technologies. However, it is realizable for DLL-based frequency synthesizers. This architecture was presented by T.-C. Lee et al. as shown in Figure 4-8 A) [44]. The three frequencies of Mode 1 are synthesized by an edge combiner which combines the output edges of all the selected voltage-controlled delay cells as shown in Figure 4-8 [45]. Since the DLL is a first-order system in nature, its loop bandwidth can be as wide as half of the reference frequency without stability issues. Hence, a much shorter settling time can be achieved using the same reference frequency with PLLs. To avoid undesired glitches on the feedback clock which will confuse the PFD, three independent PFD/CPs are used instead of directly switch between the outputs of different sets of delay cells. When the number of selected delay cells is changing, a settling time of 8 ns is achieved with good phase noise and moderate power consumption. This architecture may be the simplest with one single DLL (3 PFD/CPs) and an edge combiner. Nevertheless, the spur level is slightly higher than the other three architectures due to mismatch of the delay cells and the input transconductors of the edge conbiner. Another shortcoming is that it is not capable of quadrature output unless the number of delay stages is quadrupled, but half of the delay stages are wasted. The most severe drawback is that it is not extendable to higher frequencies. Take one of the higher frequencies 8712 MHz as an example. The minimum delay of each delay cell is demanded to be less than 57 ps. For some safety margin, we should pick 47 ps which is close to the minimum delay of 1:4 fanout inverters in CMOS 0.13 μm. But voltage-controlled delay cells have a dramatically larger minimum delay. More importantly, to reduce the mismatch between delay cells, transistors with longer channel length are required. The published synthesizer used 17 delay stages. For 14 bands, 39 delay stages with a 40 ps minimum delay of each stage are needed. What makes things worse is that quadrature

output demands 156 delay stages with 10 ps minimum delay! Moreover, for low mismatch of the edge combiner, an analog one using transconductors with large input transistors is much more preferable to digital edge combiners. The 39 input transconductors will significantly increase spur levels due to mismatch and consume a large amount of power. Apparently, two edge combiners with 68 transconductors are needed for quadrature output. Finally, 14 PFD/CPs and a 14-to-1 multiplexer will further complicate the whole system and increase power consumption. In short, the DLL-based architecture is not a good solution to UWB frequency synthesizers with more than 3 bands.

To sum up, only SSB mixing architecture can achieve 14 frequencies with potentially low power consumption and complexity, and it is highly extendable. A new 14-band frequency plan based on SSB mixing method is proposed in Chapter 4. Its power consumption is targeted for around 50 mW which is over three times lower than that of [37], and its complexity is also much lower.

4.3 Architecture of the Proposed Frequency Synthesizer

The objective of this design is to reduce the power consumption and complexity as much as possible while meeting all the specifications. First, frequencies running on chip should be as low as possible. The higher frequencies generation should be pushed as close to the output stage as possible. Second, only one plain PLL should be used and the frequency divider chain should be simplified compared to [37]. Third, filters reduce the power level of undesired tones at the output of SSB mixers. A simple and popular way to implement the filters is using LC tanks. In order to increase the effect of LC tanks, the frequencies of the two inputs of a SSB mixer should be as far away from each other as possible.

Figure 4-9 and Figure 4-10 respectively show the proposed frequency plan and the block diagram. Except the input and output of the PFD/CP, every arrow line is quadrature differential

signals which contain four signals with four different phases of 0º, 180º, 90º and 270º. The three mixers are quadrature SSB mixers containing four mixers. The whole synthesizer is based on one single plain PLL with a fixed output frequency of 8448 MHz which is 32 times of 264 MHz. The output frequency is then divided down to 264 MHz by a frequency divider chain. A SSB mixer, Mixer 1, shifts the output of the first divide-by-2 circuit to either 3960 MHz or 4488 MHz by mixing 264 MHz. Then the eight frequencies of 2376, 2904, 3432, 5016, 5544 and 6072 MHz can be synthesized by mixing 3960 or 4488 with 1056 MHz or 2112 MHz (Mixer 2). Now we have the first six frequencies. If the first two band groups are desired, then frequency synthesis is done. The frequencies of 2376 and 2904 MHz with color gray, as shown in Figure 4-9, are not required by MB-OFDM UWB, but they are intermediate for the generation of the other eight frequencies and will not be the output of the whole synthesizer. If the rest eight frequencies are needed, the lower eight frequencies are shifts up by simply mixing them with 4224 MHz (Mixer 3). As shown in Figure 4-10, before the output multiplexer, all the frequencies running on chip are lower than 6 GHz. To further save the power, Mixers 2 and 3 and all the associated multiplexers and buffers are switched off when they are not being used.

The purpose of the plain PLL is to just stabilize the output frequency and suppress the close-in phase noise. Therefore, the integer-N architecture with a traditional LC-VCO is sufficient. The reason why the frequency of 8448 MHz is chosen instead of 4224 MHz for the PLL is that quadrature signals with low I/Q phase mismatch are required for low image tones. There are basically four methods to generate quadrature phases using 1) a frequency divider, 2) a quadrature VCO (QVCO), 3) a multi-stage polyphase filter and 4) a DLL. The phase quality of the frequency-division method is the best, but it requires a VCO of a doubled frequency with higher power consumption. The QVCO method with a half working frequency can obtain

comparable phase quality to a frequency divider. However, at frequencies lower than 10 GHz, its power consumption is not lower than the first method due to two coupled VCOs but with a doubled area (inductors are doubled and larger). The phase quality of polyphase filters is sensitive to process variation and generally much worse than the first two methods due to component mismatch. The size of polyphase filters is big for low mismatch but then they can hardly work at high frequencies. The DLL-based method is suitable for frequencies lower than 1 GHz.

Unlike most other published SSB-mixing frequency synthesizers, the frequency divider chain consists of only divide-by-2 circuits. As discussed above, divide-by-2 circuits can generate the best quadrature phases with the smallest area and the lowest complexity.

Quadrature SSB mixers are the key blocks. Since their linearity and port-to-port isolation directly determine the spurs, double-balanced passive mixers are chosen and further save the power. To lower harmonic-tone-induced spurs, filters are necessary at both the inputs and outputs of SSB mixers. To take the benefits of LC-tank filters, frequency shifts are as far as possible. Except Mixer 1, frequency shifts to the adjacent band are avoided such that the closest spurs are over 2-8 GHz away from the desired center frequencies. Thus, quadrature calibration circuits are saved for Mixers 2 and 3.

The total power consumption is predicted to be 34 mW when Mixers 2 and 3 and the associated buffers are off and 57 mW when all the blocks are on, excluding the output buffer for measurements, which is the lowest among all the published 14-band UWB frequency synthesizers. Table 4-2 lists the estimated current consumption of each block.

Although this frequency synthesizer is originally designed for MB-OFDM UWB transceivers, it is straightforward to extend its bands higher than 10 GHz or lower than 3 GHz. Hence, this frequency synthesizer can be used for other wideband frequency agile transceivers with minor modifications.

4.4 Circuit Implementation

4.4.1 Quadrature SSB Mixers

As discussed in Section 4.3, the most critical blocks are the quadrature SSB mixers, because most spur tones are generated by the mixers. Not only each mixer mixes the fundamental tone and all the harmonic tones of its two inputs, but also its own nonlinearity and leakage from the two inputs to the output contribute to spur tones. To suppress the leakage, double-balanced mixers are necessary. All double-balanced mixers are either active or passive. The active mixers, based on Gilbert cells, typically have high gain but suffer from high NF and poor linearity. On the other hand, the passive mixers with low gain have much higher linearity. Since the wanted signals are just sinusoidal waves with large amplitudes in this system, linearity is more important than gain and NF. Double-balanced passive mixers are thus chosen.

In order to achieve single-sideband mixing, two mixers are needed. Figure 4-11 shows the block diagram of an SSB mixer. Since each SSB mixer should be capable of both up-conversion and down-conversion, the upper branch of the preceding buffers is able to swap the two quadrature inputs, whereas the lower branch is a regular buffer.

Conventionally the outputs of two double-balanced passive mixers are directly connected to each other [41] and [46], as shown in Figure 4-12. However, since the phase difference between the inputs of the two mixers is 90º, the RF inputs of the two mixers are shorted during two quarters of one LO period. This hurts the NF, gain and linearity. The degradation is more severe when the preceding stages at RF ports are voltage buffers, because they try to drive and

load each other. Consequently the power consumption is required to be much higher to maintain the performance. Figure 4-12 shows an example where RFI+ and RFQ+ are shorted (red arrows), and RFI- and RFQ- are shorted (blue arrows). As shown in Figure 4-13, LOI and LOQ overlap during two quarters of one period in color gray. One typical solution is to shape LO signals with 50% duty cycle into 25% duty cycle [46]. It works very well for low-frequency direct-conversion receivers with large attenuation of out-of-band spur tones owing to baseband filters. Nevertheless, for this ultra wideband system, the two inputs of each mixer should be close to sinusoidal waves as much as possible for low spur tones, because most of them fall in band and no simple tunable filter has high attenuation from 3-10 GHz. It is more difficult to generate 25% duty-cycle sinusoidal waves with a good control of duty cycle than square waves at high frequencies. Also the requirement of the matching of the four differential quadrature signals further complicates the generation and significantly increases power consumption. Another issue with 25% duty cycle is large second harmonic tone of LO. The second harmonic generates spurs by mixing with RF and its harmonics and leaking to the output. Although these spurs are attenuated by differential operation, any mismatches between transistors and loads walk them to the differential output. These mismatches can be reduced simply by increasing the sizes of the transistors and loads for low-frequency direct-conversion receivers. On the other hand, large devices cannot be adopted in this system due to tunable high-frequency inputs and outputs with the design objective of low power consumption.

The addition function in Figure 4-11 can be achieved in current domain instead of voltage domain to avoid the loading problem of the two buffers. Two transconductors with high input and output impedance are respectively placed at the outputs of the two passive mixers before connecting the outputs of the two transconductors together. Figure 4-14 shows the schematic of

the modified SSB mixer. To ensure high linearity and output impedance, degeneration resistors and cascode transistors are introduced. The degeneration resistors are connected as bridges to save some voltage headroom. Since the active part is merely a buffer, the linearity is still much higher with lower power consumption than that of Gilbert cells. The loads are LC tanks with variable switch capacitor arrays resonating at the wanted frequency to keep high voltage swing and suppress spurs. Symmetric inductors are used to make Q as high as possible, save chip area and better symmetry. The benefits of LC tanks are limited by low Q of on-chip inductors. A cross-coupled pair with a negative conductance is connected in parallel with the LC tank of each SSB mixer to boost the Q by cancelling some shunt conductance [47]. Degeneration resistors are used again for better linearity considering large-signal operations.

Since the transistors of the passive mixers cannot be very large, the LO leakage due to the transistor mismatch is a major source of spurs and have to be considered. Triple-well NMOSFETs are used to facilitate fine tuning of threshold voltage mismatch. Figure 4-15 shows the simplified cross section of a triple-well NMOSFET of UMC 130nm triple-well process. A Deep N-Well layer cuts an area out of the large P-Well for the triple-well NMOSFET. The threshold voltage can thus be adjusted individually by changing the voltage at its body terminal. The N-well and P-Well are respectively biased at the highest (V_{DD}) and lowest voltages (ground) on chip. Figure 4-16 shows the pattern of mismatch which results in the LO leakage. The LO leaks to the output only if there is a mismatch between the pair of M1-2 shaded in color blue and the pair of M3-4 shaded in color green. Other mismatch patterns have no effect on the LO leakage. Therefore, to simplify the adjustment, the body terminals of M1 and M2 are connected to the ground, whereas the body terminals of M3 and M4 are shorted and can be finely tuned externally. The RF-to-output leakage can also be calibrated out using the same approach.

However, with three quadrature SSB mixers in this system, the trimming would be too complicated if both LO and RF leakages are taken into account. Also, since the signal amplitudes at RF ports can always be chosen to be much smaller than LO signals, this issue is much less severe than the LO leakage. Besides, triple-well devices provide higher isolation from substrate coupling in the lower half bandwidth.

All mixers in the block diagram of the whole system must be capable of quadrature outputs which makes them consist of two SSB mixers. The quadrature output is generated by simply swapping I/Q of one input.

4.4.2 I/Q Calibration Buffers

The most image spurs at the outputs of the quadrature SSB mixers are in band, especially for Mixer 1 and Mixer 2. Although the outputs of current-mode logic (CML) frequency dividers typically have good I/Q balance, noticeable gain and phase errors due to device mismatches and routing asymmetries may still introduce high image spurs. Interpolating buffers are placed at inputs of Mixer 1 and Mixer 2 to minimize the errors [35]. It is worth to mention that, for Mixer 3, the wanted frequencies are about 4-30 times higher than the images spurs. A Q-boosted LC tank introduced above is sufficient to suppress the image spurs and meet the design target.

Figure 4-17 shows the schematic of the I/Q calibration buffer. It consists of two identical buffers. Each buffer has two identical differential pairs with drain nodes connected to a single pair of RC loads. The in-phase and quadrature-phase sinusoidal waves are superposed to respectively synthesize 45º and 135º outputs with 90º phase difference. The key is the relative phase between the two outputs. The bias voltages of the lower half circuit, Vbias and Vtail, are fixed, whereas those of the upper half are adjustable. Node Gain controls the amplitudes of both the two differential pairs by adjusting the common-mode tail current, and thus controls the amplitude of the 45º output, shown in color red. Node Phase controls the phase of the 45º output

by adjusting the differential-mode current, shown in color blue. Since the lower half is fixed, the maximum tuning range is ±45º which is sufficient to counteract non-idealities. Resistors are chosen for the loads instead of PMOSFETs for better linearity. To suppress harmonics of the outputs, switch-capacitor arrays are added in parallel with the load resistors.

4.4.3 Frequency Dividers

Wideband frequency dividers are essentially digital circuits. At low frequencies (~100 MHz or lower), rail-to-rail logic circuits are very efficient, since they derive current from power supplies only at logic transitions with extremely low static current. On the other hand, CML circuits have higher speeds with much lower power consumption at high frequencies, mainly because they require lower voltage swing to work properly [32]. Figure 4-18 shows comparison of current consumption for CMOS rail-to-rail and CML logic versus frequency. The power consumption can generally be given by

$$P_D = C_L V_{pp}^2 f \tag{4-2}$$

where C_L, V_{pp} and f are respectively load capacitance, voltage swing and frequency. Equation 4-2 shows that the power consumption decreases with the square of the voltage swing.

Thanks to the system-level design, only divide-by-2 circuits are needed. Five CML divide-by-2 frequency dividers are used to divide 8448 MHz down to 264 MHz. Each divide-by-2 circuit consists of two D-latches with a gain cell and a storage cell shown in Figure 4-19. Typically the gain cell and the storage of each D-latch share one single tail current source. Any mismatch between the two tail current sources directly leads to a mismatch between the in-phase output and the quadrature output [48]. To obtain a better match between I and Q outputs, the gain cells of the two D-latches share one tail current source, and the storage cells share another current source, shown in Figure 4-20. Another benefit from the CML frequency dividers is that

their outputs can directly be fed into any differential buffer in this system including the I/Q calibration buffers.

To divide 264 MHz down to 132 MHz, a conventional static divide-by-2 circuit is used instead of the CML due to lower power consumption in this frequency range and no I/Q match required.

4.4.4 Multiplexers

Similarly to the frequency dividers, CML type is adopted for multiplexers within the bandwidth. The performance of multiplexers also plays an important role on the output spur level due to finite isolation between unselected inputs to output. The isolation of the conventional CML multiplexers is not sufficient. The unselected signals leak to the output through C_{gd} and C_{sb} (source-body capacitance) of the input transistors and C_{gd} and C_{db} of its switch transistor shown in Figure 4-21 A) [49]. A coupling cancellation technique was proposed in [35] shown in Figure 4-21 B). This technique works well at relatively low frequencies. However, it increases the parasitic capacitances of both the input and the output with more complicated routing and almost twice area.

Switch transistors can be moved to the drain terminals of the input pairs [49]. When the first pair is switched off, not only its current drops to zero with zero gain, but also it is isolated by the cut-off-region transistors. This results in much higher isolation than the conventional topology but with smaller parasitic capacitances at the inputs and the output and simpler routing than that in [35].

4.4.5 PLL

Based on the discussion on the system level design, because of the fixed output frequency (8448 MHz) the design goals of the PLL are just low reference spurs and phase noise with adequate voltage swing for the frequency divider chain and low power consumption. For low

phase noise, the loop bandwidth and reference frequency should be high enough, and the division ratio (N) should not be large. The reference frequency is chosen to be 132 MHz, which results in a division ratio of 64. The loop bandwidth is determined based on the loop stability and 60º phase margin is chosen. Now the loop bandwidth can be set to be about 6.5 MHz, if the third-order loop filter is used. With such a high reference frequency and a wide loop bandwidth, the integer-N architecture will suffice. A clean and stable reference frequency source is fed into one of the inputs of a PFD. The PFD provides two signals to switch on a CP by comparing the phases of the reference source and a VCO output after division. The CP injects charges onto a loop filter, and then the loop filter converts the charges into a control voltage to tune the output frequency of the VCO. The last step is to divide the VCO output down to the same frequency with the reference and feed it into the other input of the PFD. Figure 4-23 shows the block diagram. The divide-by-64 circuit has already been discussed in section 4.4.3. The design of the rest blocks is discussed below.

For VCO design, an NMOSFET cross-coupled pair with a PMOSFET tail current source is chosen. The PMOS tail current source, with lower flick noise than the NMOS, ensures the Q of the LC tank. Due to a separate N-well it has a higher immunity to substrate coupling. Moreover, it blocks the coupling from V_{DD} by referring its gate bias voltage Vtail_p to Vdd. Since the dc voltage at the differential output (also the poly gates of the varactors) is slightly higher than half of V_{DD}, the control voltage from the CP with the loop filter can be directly fed into the VCO. Since the VCO is only to provide a fixed single-tone source, the tuning range is set to be just wide enough to counteract process, power supply and temperature (PVT) variations, which is around 20%. Two metal-oxide-metal switched capacitors are added in shunt with each output node, which reduces the required gain of the VCO to one half of that with varactors only. With

the power budget and the tuning range, the inductors and varactors can be determined. The inductors and varactors are optimized for highest Q to minimize phase noise.

Considering the frequency of the PFD inputs is slightly high, the popular RS-latch architecture is chosen with a higher speed than the conventional D-flip-flop-based architecture [50], as shown in Figure 4-25. The delay from either input to the output of rising edges of UP and DN is three gate delays if the output inverters is included. When both REF- and VCO- are low, reset is triggered with one gate delay of U9. As a result, the turn-on time of UP and DN is equal to the delay from node A to reset when the PLL is locked. If the turn-on time is too short, switch transistors of the CP may not be turned on due to the threshold voltage and finite speed. In other words, the CP is off with very small phase offsets between REF- and VCO-. Consequently, the loop is open when the phase difference between the two inputs is small, which means high phase noise at small frequency offsets. This problem is known as dead-zone effect. A typical solution is to add an even number of inverters to the reset path. However, this leads to a long turn-on time which deteriorates both phase noise and reference spurs. To guarantee to turn on the CP with the minimum turn-on time, NMOSFETs of U9 are sized relatively smaller with a lower speed of falling edges at Node reset.

Current leakage and mismatch between the up and down current sources of the CP dominate sources of the reference spurs. Furthermore, since the loop bandwidth is wide, the in-band phase noise of the VCO is dramatically suppressed, and the CP typically dominates the higher part of the in-band phase noise, especially around 1 MHz frequency offset. Due to these reasons it becomes the most important block of this PLL. The main design considerations are speed, noise and spurs. For the single-ended PFD and CP, there is an evitable timing mismatch between UP and DN, because the two outputs of the PFD respectively controls PMOSFETs and

NMOSFETs by using complementary pulses. Even if the delay can be compensated by adding a transmission gate, the PFD mismatch can hardly be sufficiently small due to different parasitic resistances and capacitances. Therefore, current steering architecture is chosen for the CP to obtain a higher immunity to the PFD mismatch and a high speed. The simplified schematic of the CP is shown in Figure 4-26 [51]. It takes both UP and DN and their complementary signals from PFD as its inputs. The effect of the mismatch is thus counterbalanced by the symmetry. A voltage follower forces the unused output to track the output voltage, in order to eliminate the charge sharing problem when switching.

Another issue of the CP core in Figure 4-26 is that the current of the transistor M1 is unavoidably different from that of M2 when the output voltage varies due to the finite output resistances. The widths of the UP and DN current pulses will be different for a fixed output voltage when the PLL is in the lock state. As a consequence, the reference spur level will be high. This effect is more significant when the cascode topology is not adopted for a wider tuning range. To mitigate this problem, a differential amplifier forces the current of M2 to follow that of M1 by comparing the unused output voltage with the replica bias.

To obtain more reference spur reduction from the loop filter, the third-order passive loop filter is used, as shown in Figure 4-27. The parasitic capacitance looking into the control voltage terminal of the VCO is absorbed into C3.

4.5 Measurement Results

The proposed MB-OFDM UWB frequency synthesizer was fabricated using UMC 130nm mixed-mode/RF CMOS process with triple-well devices and eight metal layers. The thick top metal layer with 2 μm thickness helps design of on-chip inductors with high Q. All the inductors are symmetric inductors to obtain better symmetry with higher Q and smaller chip area, and they are all optimized and simulated by using ADS Momentum. Figure 4-28 shows the die

photograph with bonding wires and the chip size of 1.8 mm x 1.9 mm including pads with electro-static discharge (ESD) protection, and the active area including all inductors of 1.2mm x 1.8mm. The frequency synthesizer was bonded on a printed circuit boards (PCB) and then measured. The dielectric of the PCBs is FR-4 for lower cost. For higher isolation, better tolerance to process variations and lower loss due to FR-4 at these high frequencies, Grounded Co-Planar Wave Guides (CPWGs) instead of microstrip lines are used for the input and output RF signals on the test boards. Figure 4-29 shows the photograph of the test PCB.

The input reference signal of 132 MHz was created by a signal generator. The spectrum and the phase noise of the output were measured by using Agilent E4448A spectrum analyzer. Figure 4-30 shows the spectrum at Band 8 (7128 MHz) with the highest spurs of -34 dBc. The spur level due to LO leakage is -39 dBc. Figure 4-31 shows the phase noise at Band 8 with -100 dBc/Hz at 1 MHz offset. The measured output power, phase noise at 1 MHz frequency offset and the highest spur level at each band are listed in Table 4-3. The loss of the cables and the baluns were de-embedded for the measured output power which is from 6 dB to 9 dB. An output buffer was used to match the outside impedance of 50 Ω solely for measurements and deliver the wanted frequencies off chip. The output power is slightly low and significantly varies with different bands partly due to long output bond wire of 2 mm and characteristic impedance variation of the CPWGs on the PCBs. Nevertheless, if the frequency synthesizer is used on chip and directly connected to mixers in a transceiver, this variation will be much smaller due to no output bond wires or the CPWGs.

The transient performance was measured by using a wide-bandwidth oscilloscope Agilent Infiniium DCA 86100B. External clocks of 10 MHz from a function generator Agilent 33220A control band switching. The measured band switching behavior with the longest settling time of

1.7 ns from Band 3 to Band 8 is shown in Figure 4-32. This settling time is much shorter than the required 9.47 ns guard interval duration. Channel 1 and Channel 2 are respectively the in-phase signal (the yellow waveform) and the quadrature signal (the green waveform), which shows that the frequency synthesizer is capable of I/Q outputs.

Excluding the output buffer, the entire frequency synthesizer derives only 25 mA from a 1.2 V power supply if only Band 2 and Band 3 are required with both Mixer 2, Mixer 3 and the associated buffers are off. It draws 40 mA if Band 1 and Band 4-6 are outputted which is popular, and 47 mA if the higher eight frequencies are required. The power consumption is the lowest among all previously published complete 14-band frequency synthesizers. Even the highest power consumption value of 56 mW is less than a half of the lowest reported to date (117 mW) [41]. The average value weighted to the number of bands is only 50 mW which is less one third of [37]. The performance is summarized and compared with recently published works including all 14-bands frequency synthesizers in Table 4-4. It shows that this work achieves the lowest power consumption with comparable performance to other published works.

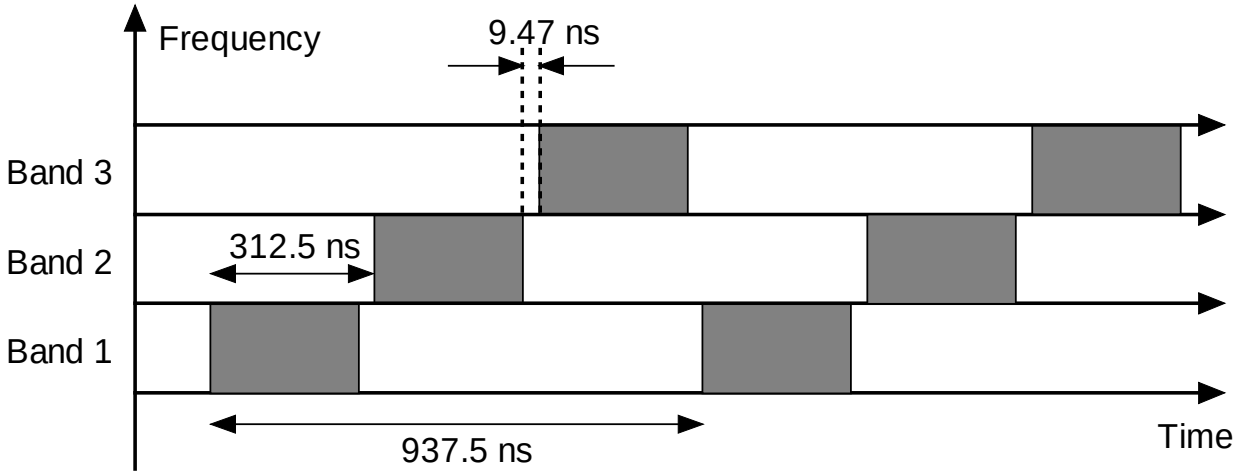


Figure 4-1. Frequency hopping diagram of Mode 1 MB-OFDM UWB.

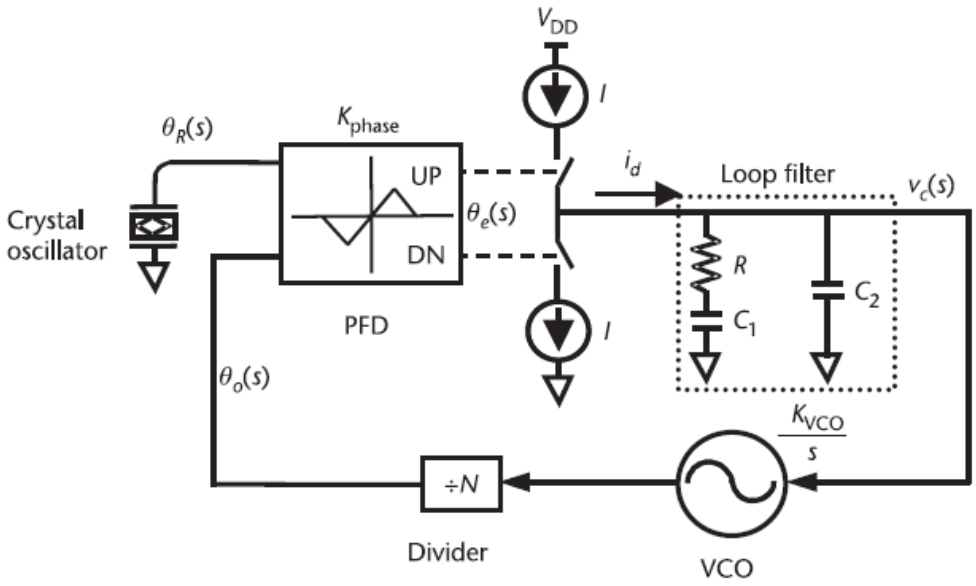


Figure 4-2. Block diagram of a second order integer-N PLL [32].

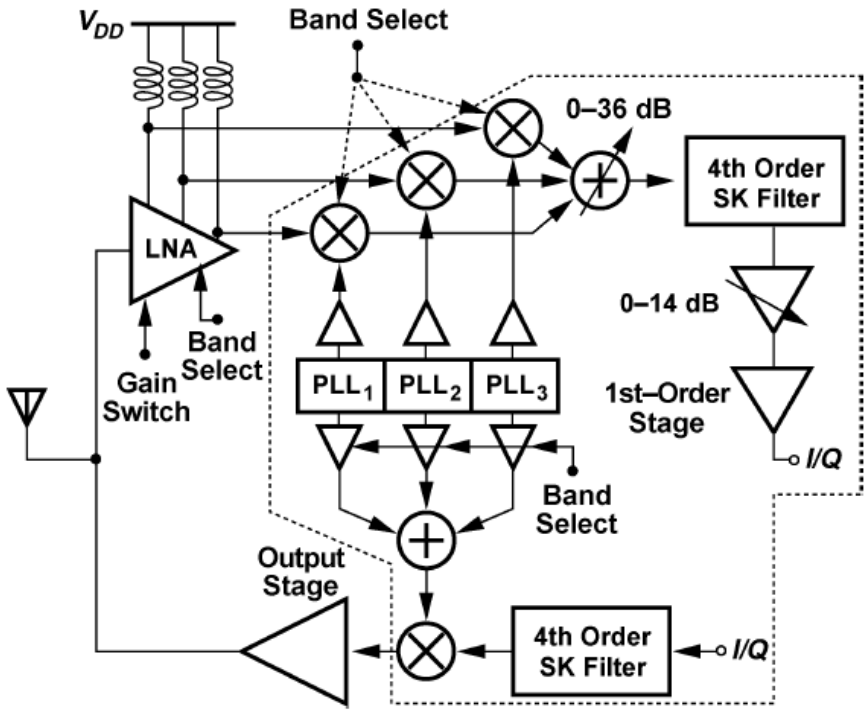


Figure 4-3. Block diagram of the 3-band frequency synthesizer reported by B. Razavi et al. [34].

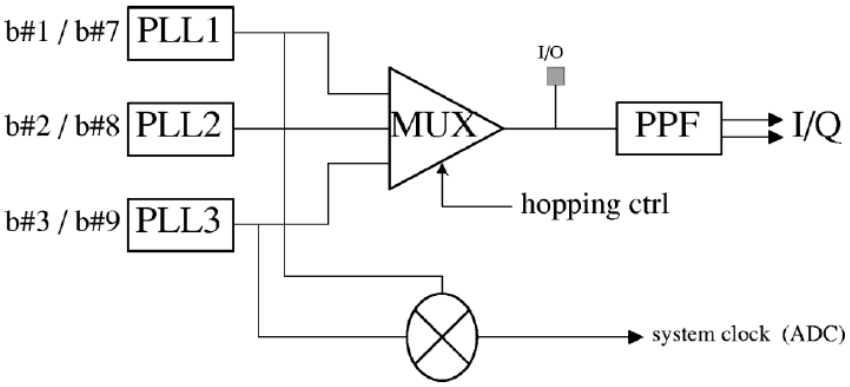


Figure 4-4. Block diagram of the 6-band frequency synthesizer reported by K. Stadius et al. [33].

	x 12	x 14	x 16	x 18	x 20	x 22	x 24	x 26	x 28	x 30	x 32	x 34	x 36	x 38	x 40
(MHz)	3432	3960	4488	5016	5544	6072	6600	7128	7656	8184	8712	9240	9768	10296	
264 x	13	15	17	19	21	23	25	27	29	31	33	35	37	39	

Figure 4-5. Common divisor of the frequency bands and their middle frequencies.

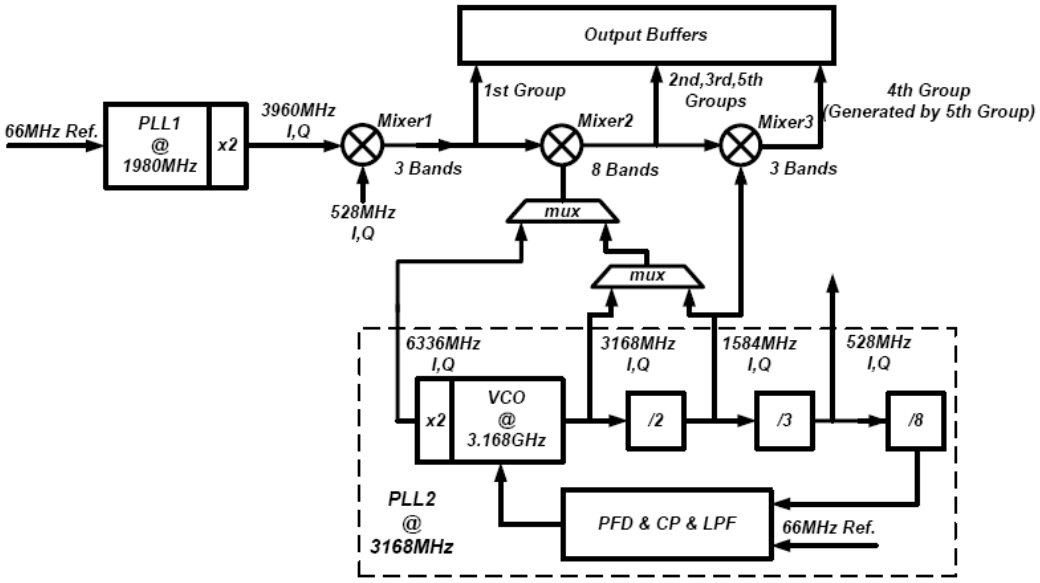


Figure 4-6. Block diagram of the 14-band frequency synthesizer reported by C.-F. Liang et al. [37].

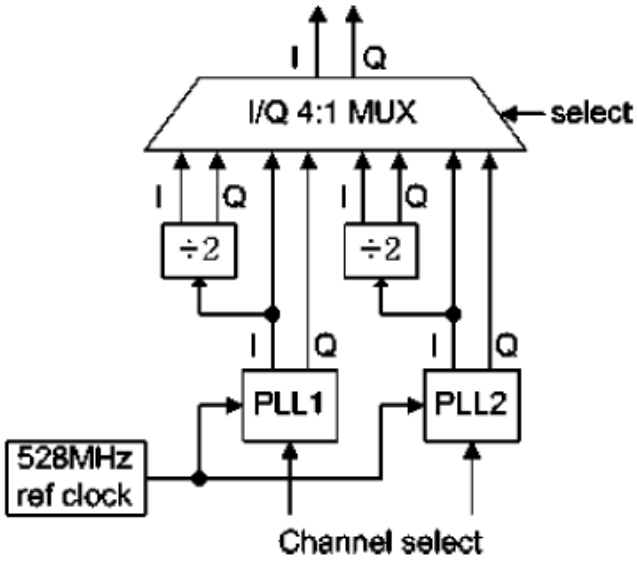


Figure 4-7. Block diagram of the frequency synthesizer using the third architecture proposed by G.-Y. Tak et al. [43].

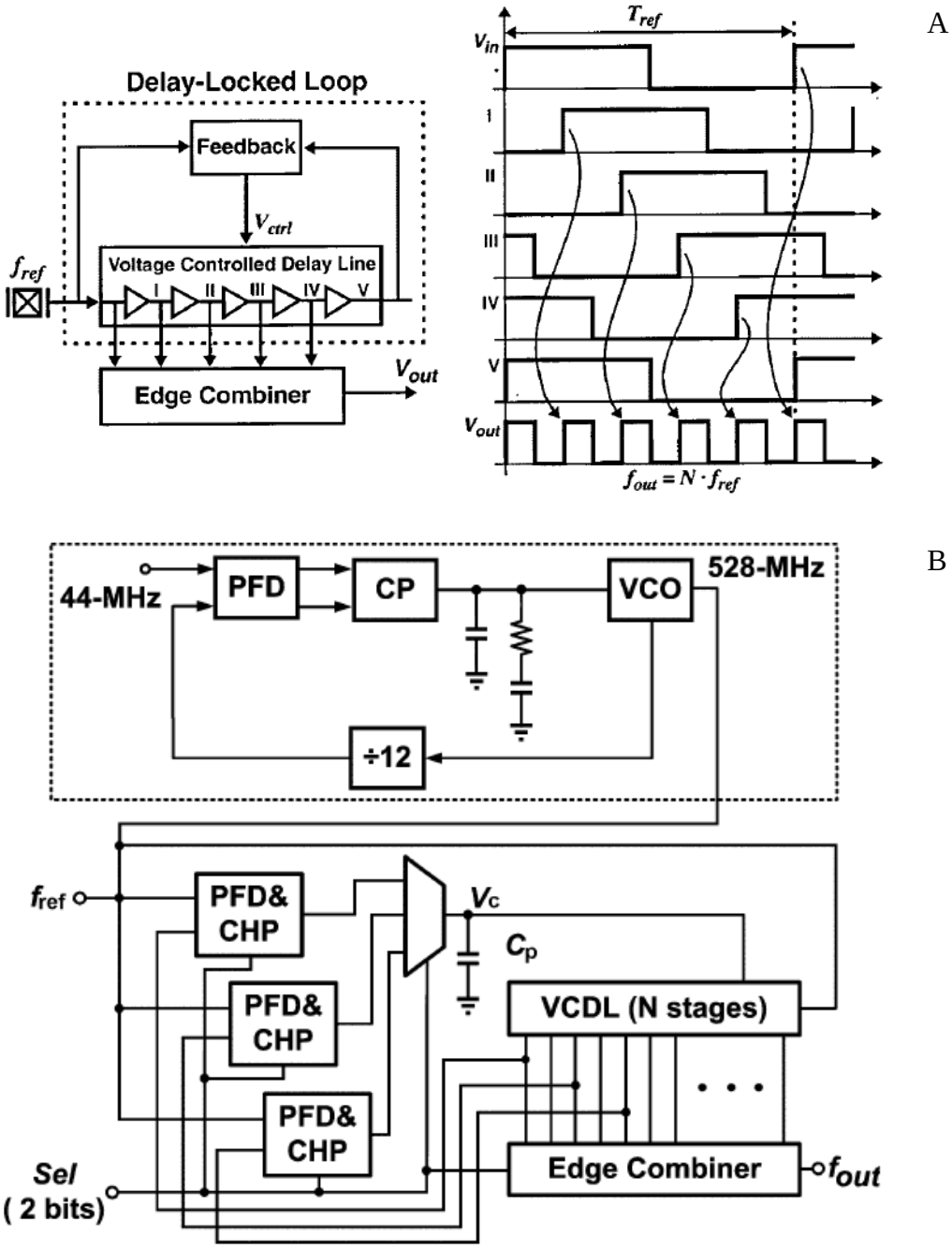


Figure 4-8. Block diagram of A) the DLL-based frequency multiplier by G. Chien [45] and B) the DLL-based Mode 1 UWB frequency synthesizer presented by T.-C. Lee et al. [44].

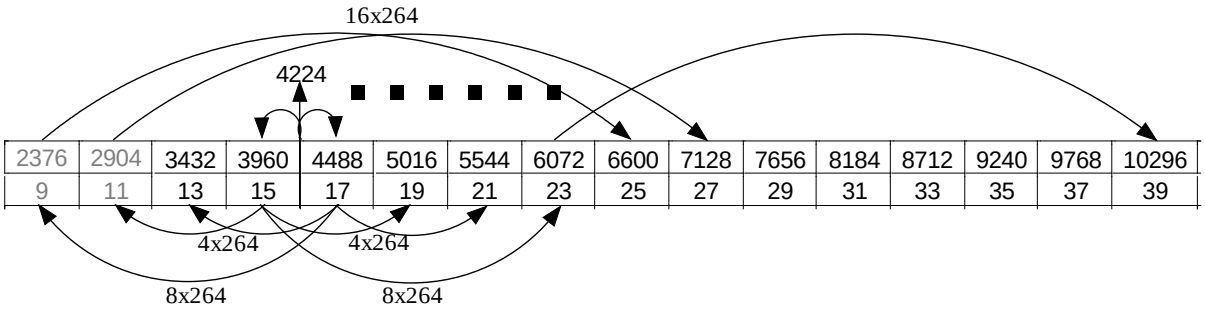


Figure 4-9. Frequency plan of the proposed 14-band frequency synthesizer.

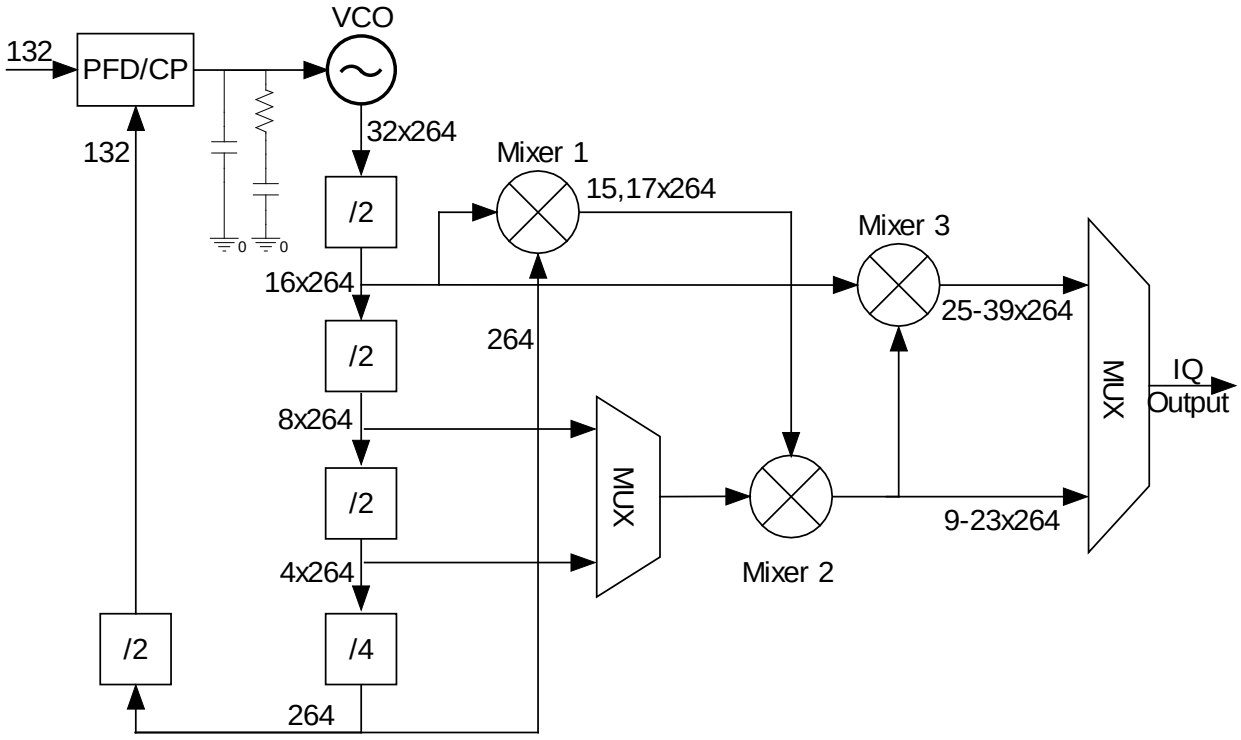
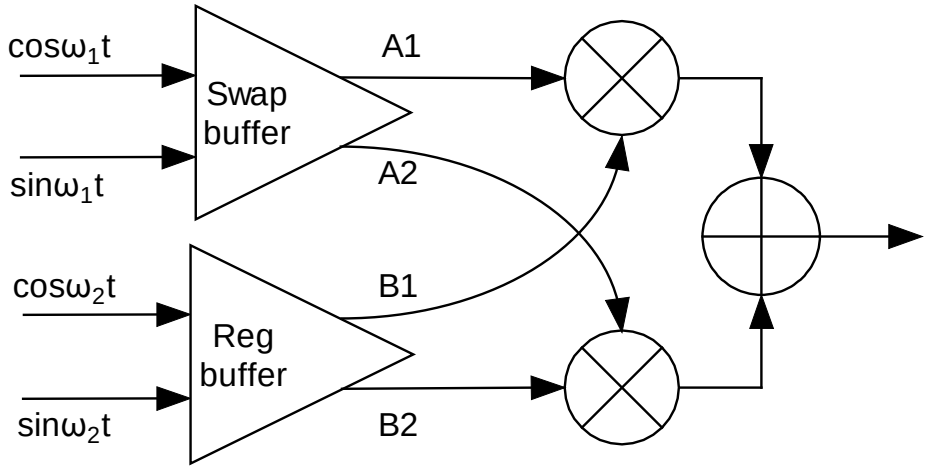


Figure 4-10. Block diagram of the proposed 14-band frequency synthesizer.



A1	A2	B1	B2	Output
$\cos\omega_1 t$	$\sin\omega_1 t$	$\cos\omega_2 t$	$\sin\omega_2 t$	$\cos(\omega_1-\omega_2)t$
$\sin\omega_1 t$	$\cos\omega_1 t$	$\cos\omega_2 t$	$\sin\omega_2 t$	$\sin(\omega_1+\omega_2)t$

Figure 4-11. Block diagram and the up-conversion and downconversion of an SSB mixer.

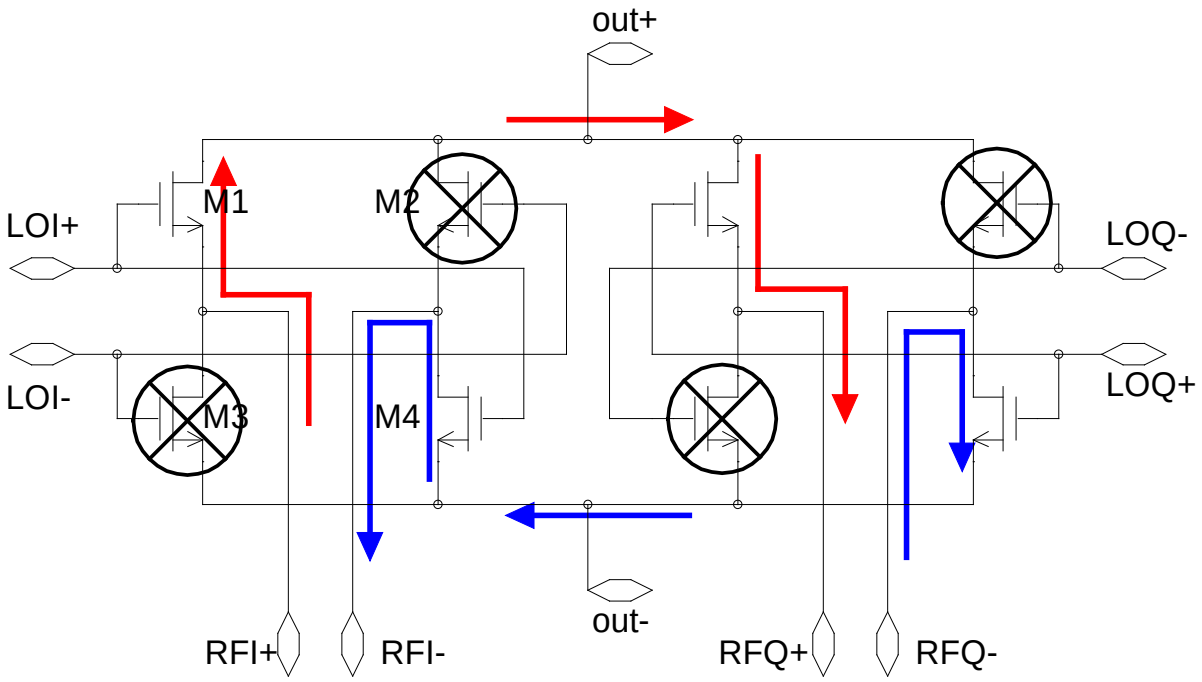


Figure 4-12. Schematic of the conventional passive SSB mixer.

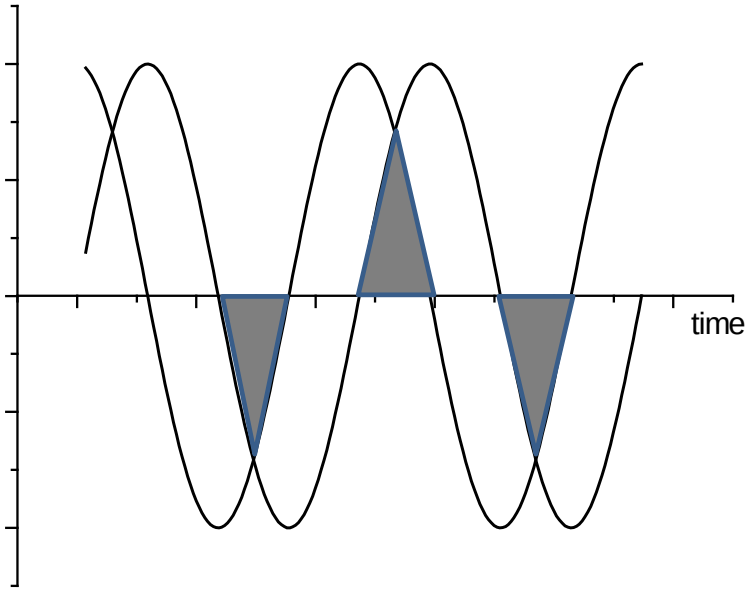


Figure 4-13. LOI and LOQ overlap during two quarter of one period in color gray.

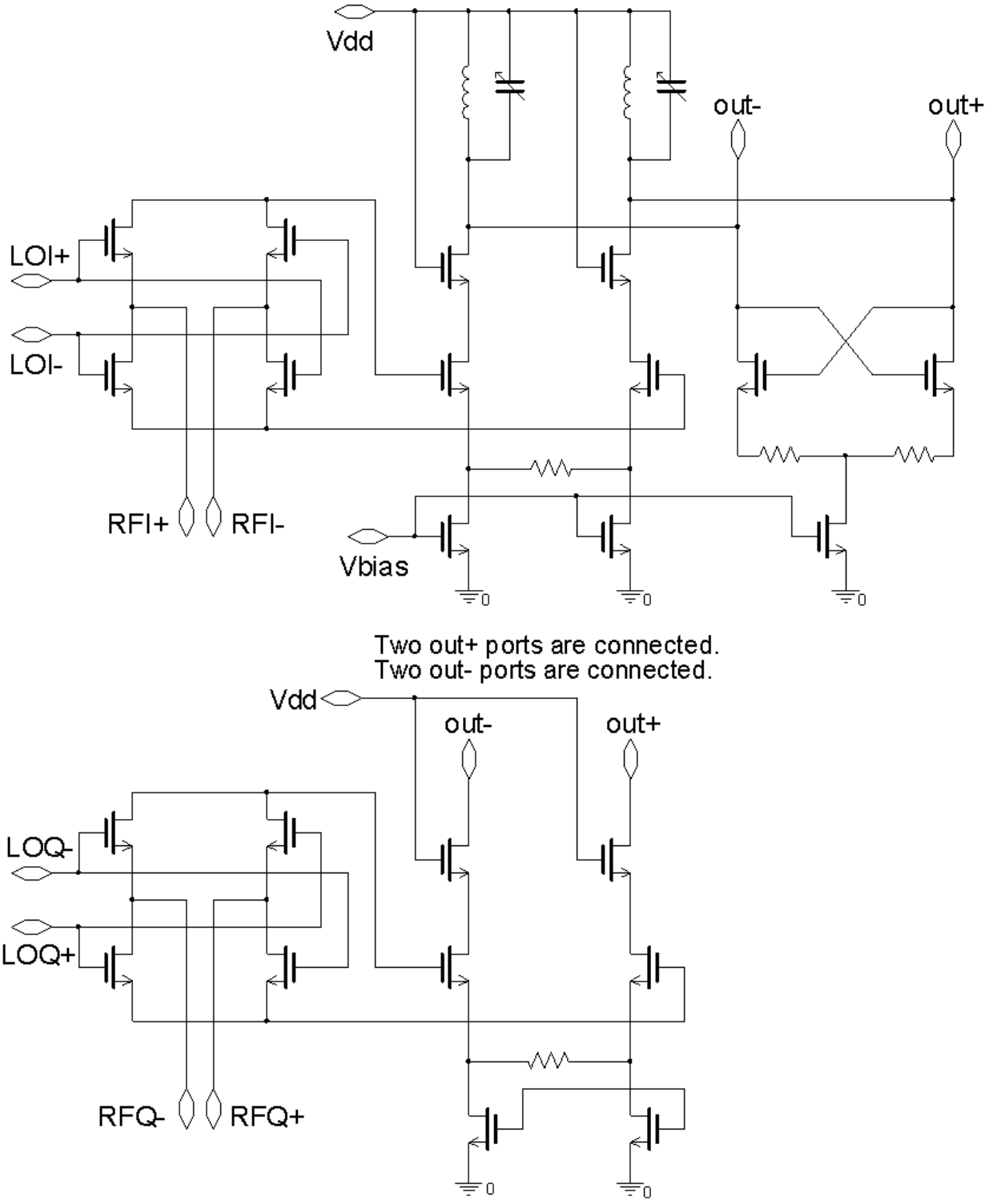


Figure 4-14. Schematic of the proposed SSB mixer.

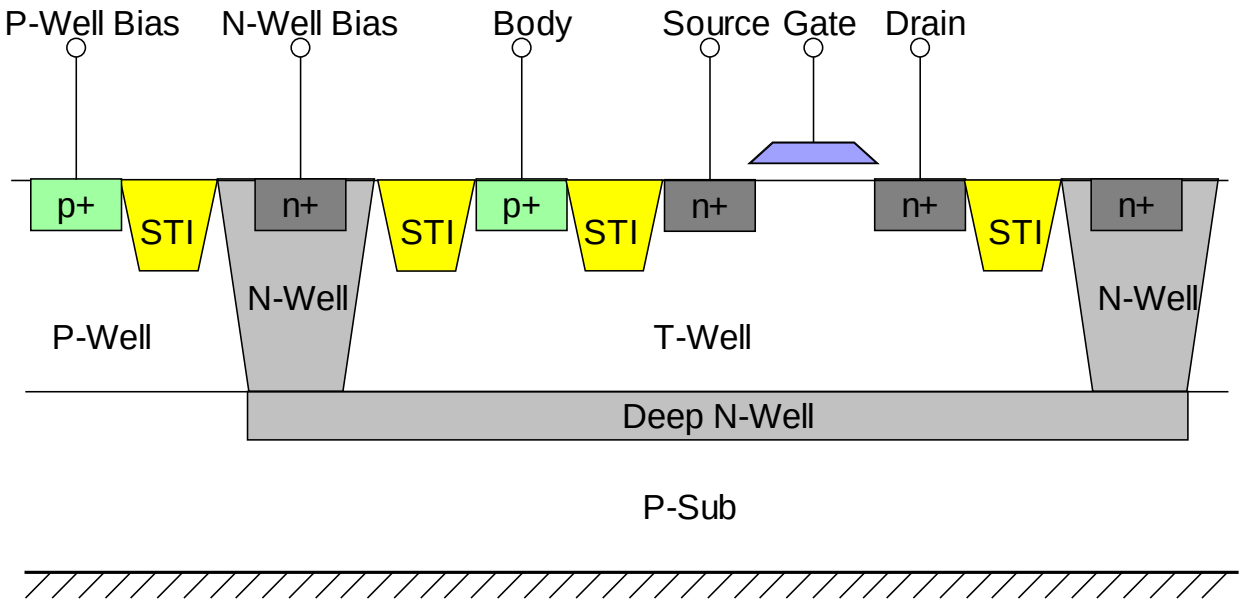


Figure 4-15. Simplified cross section of a triple-well NMOSFET of UMC 130nm triple-well process.

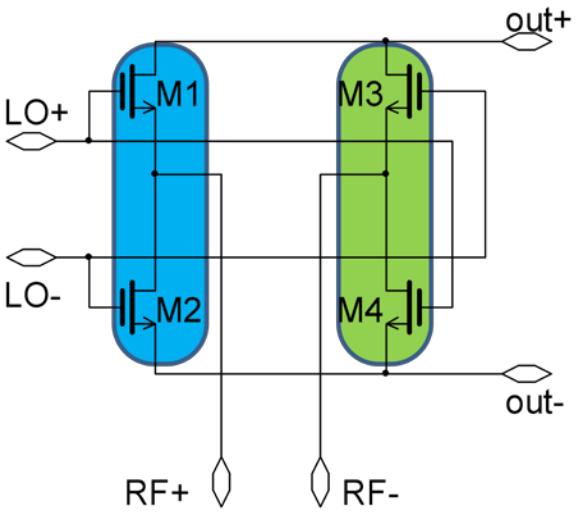


Figure 4-16. Pattern of mismatch which results in the LO leakage.

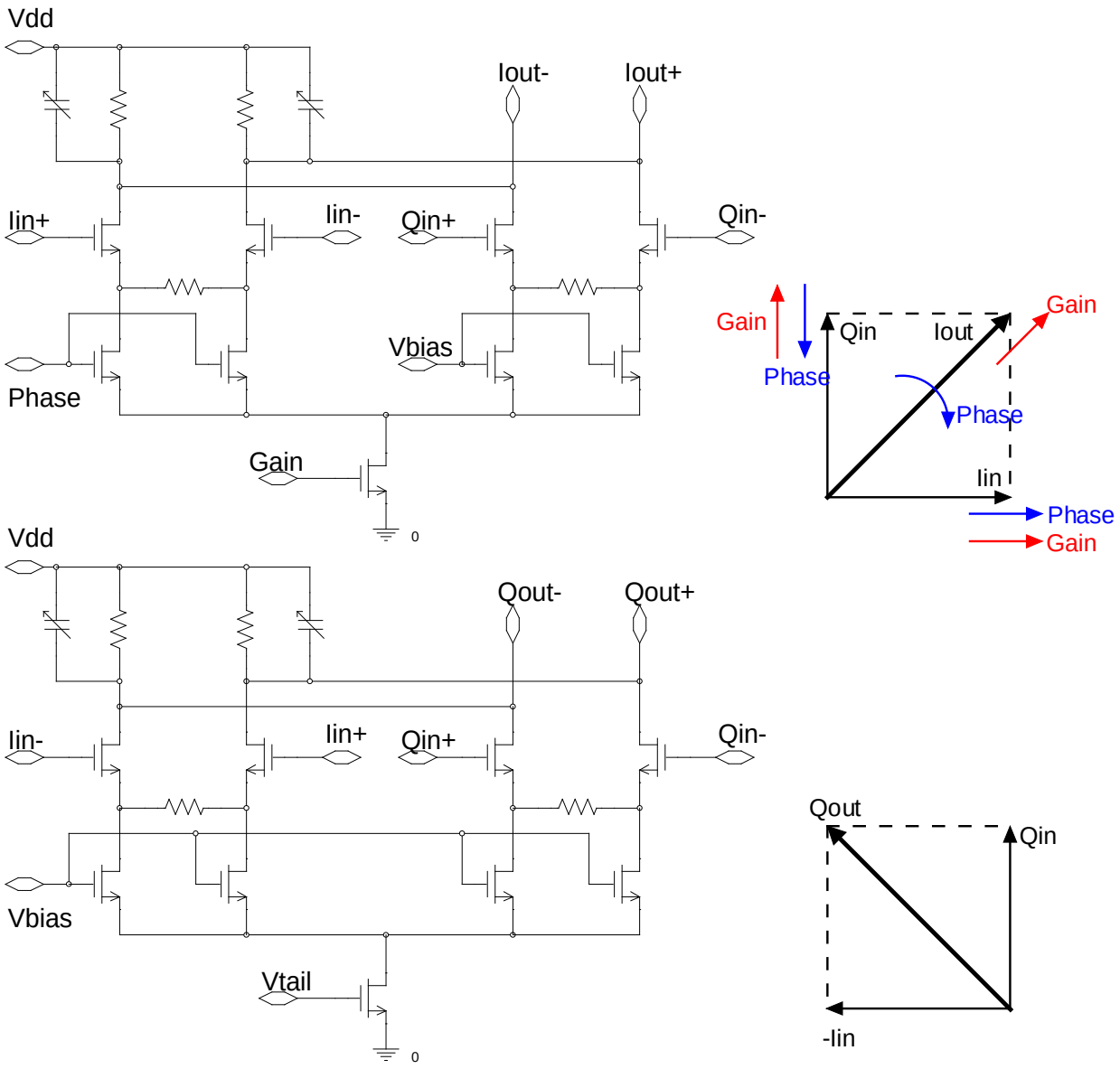


Figure 4-17. Schematic of the I/Q calibration buffers.

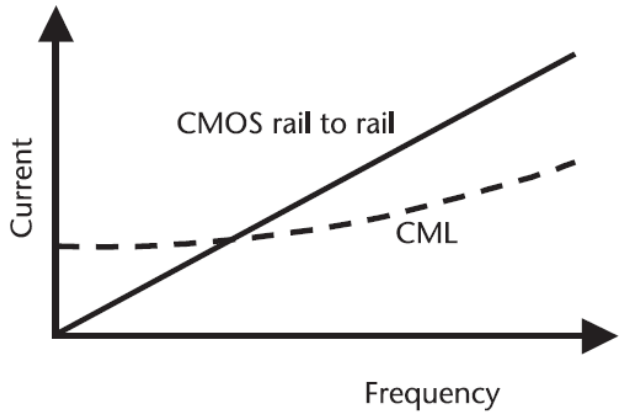


Figure 4-18. Comparison of current for CMOS rail-to-rail and CML logic versus frequency [32].

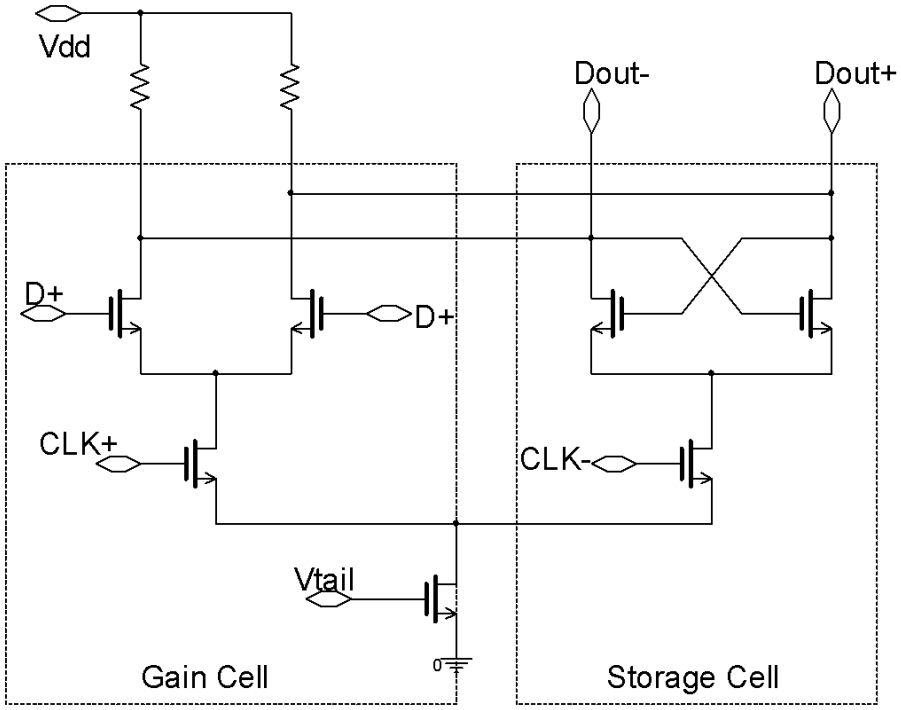


Figure 4-19. Schematic of a typical CML D-latch.

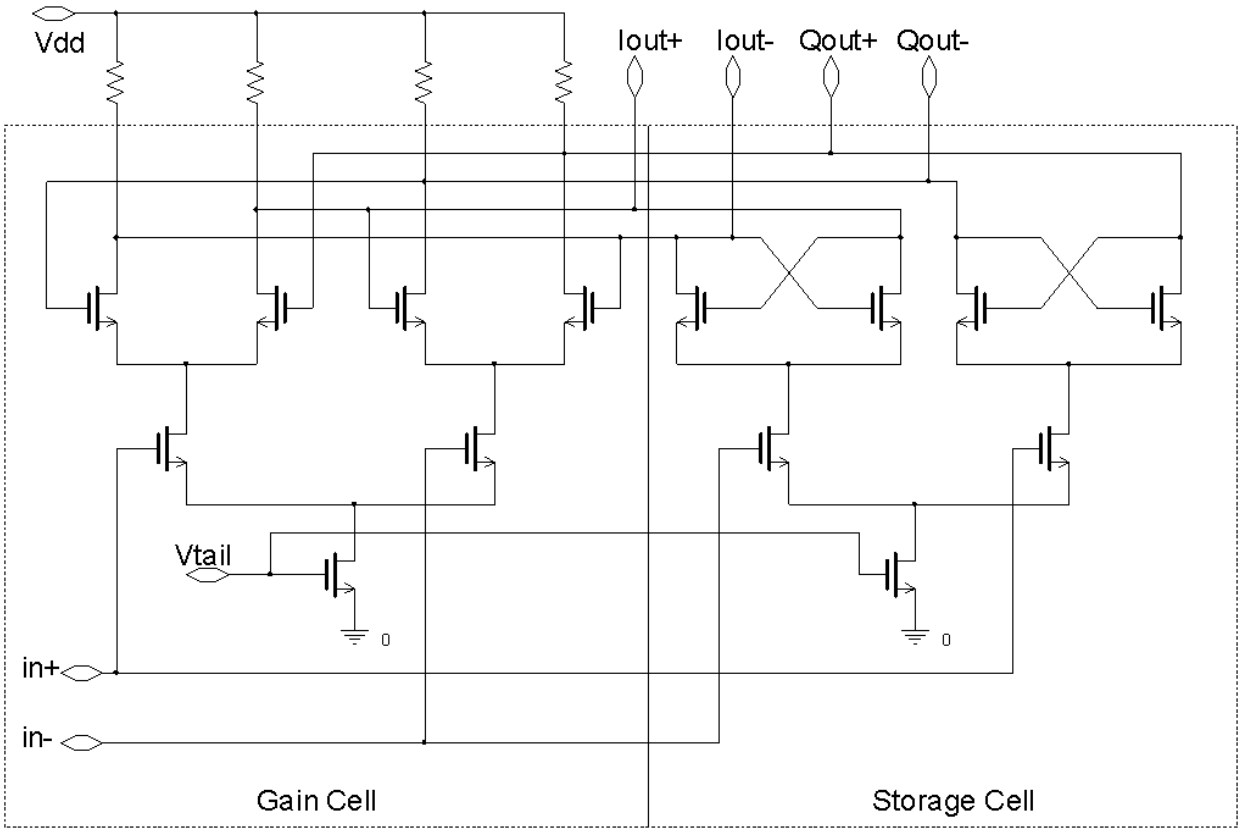


Figure 4-20. Schematic of the CML frequency divider.

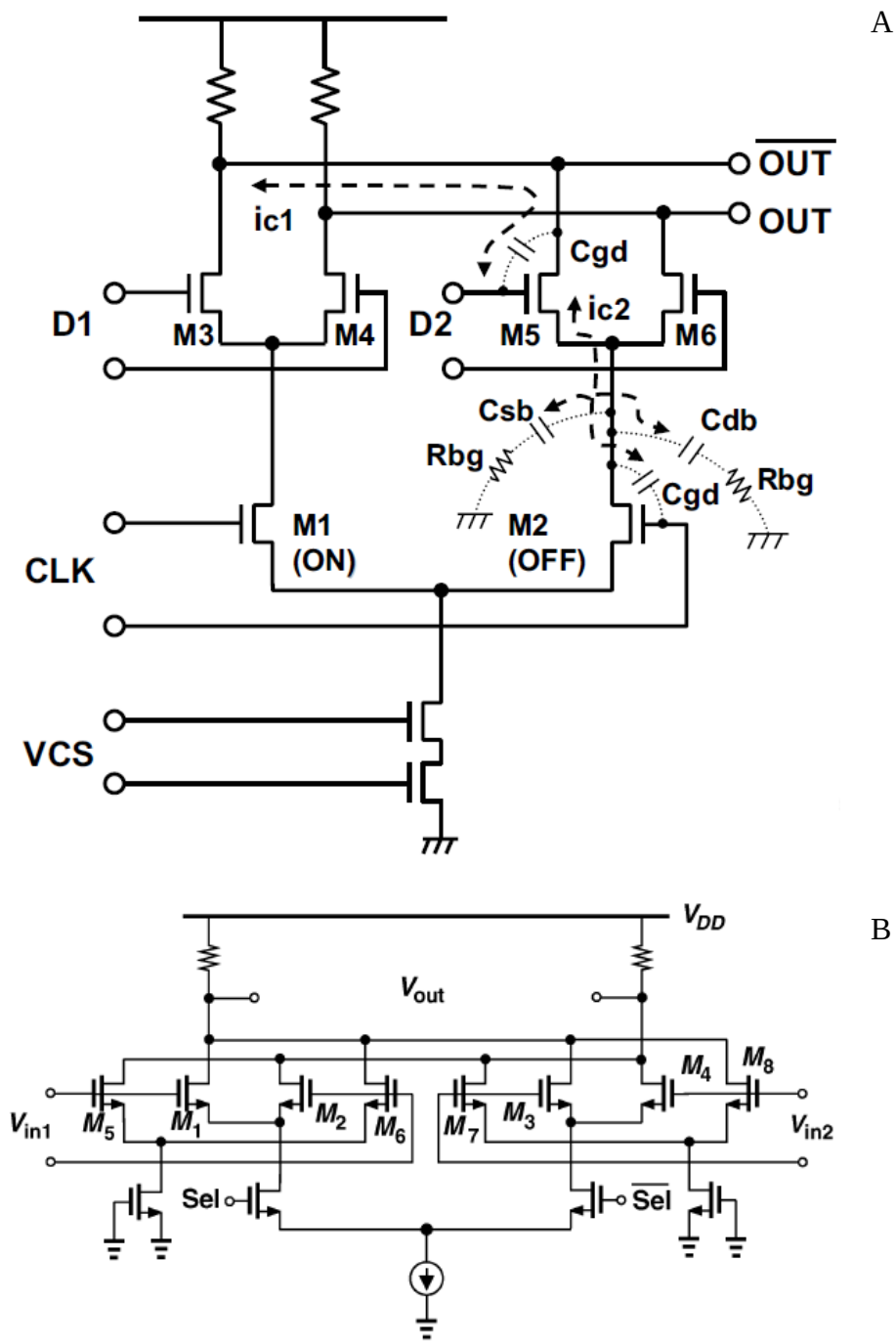


Figure 4-21. Schematics of A) a conventional CML multiplexer [49] and B) a coupling cancellation technique [35].

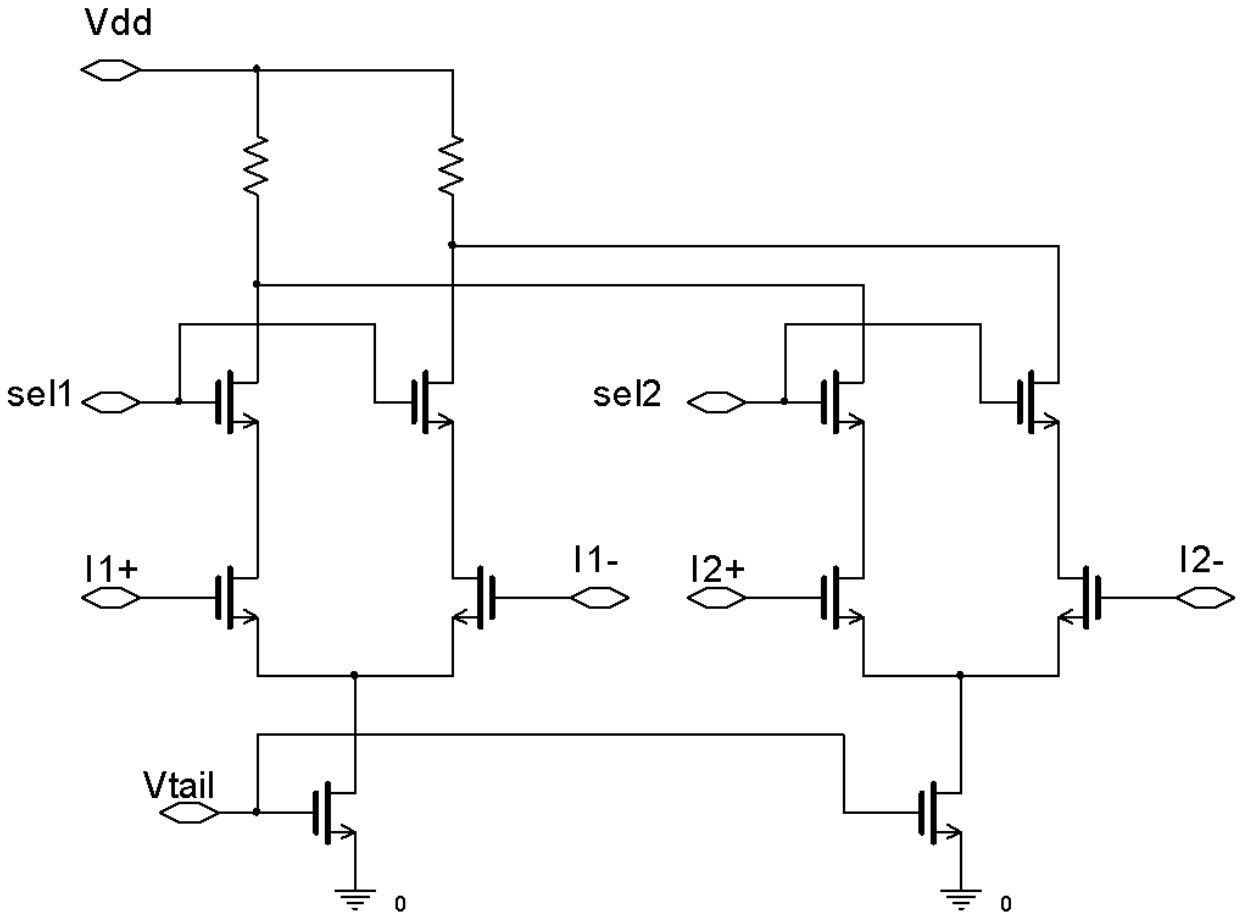


Figure 4-22. Schematic of the CML multiplexer with higher isolation proposed in [49].

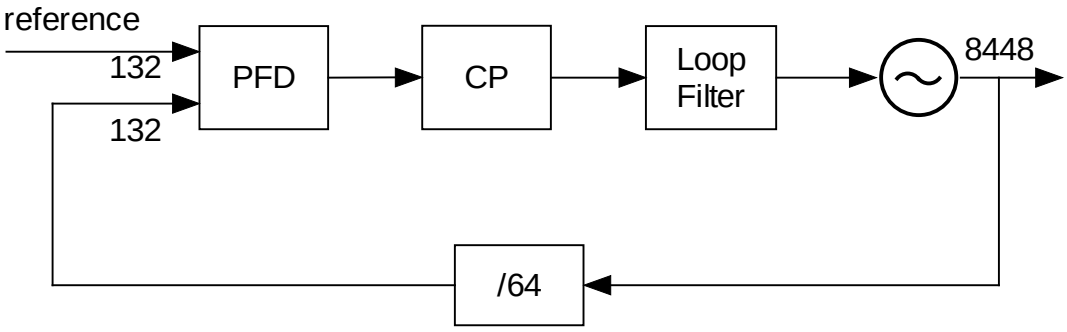


Figure 4-23. Block diagram of the integer-N PLL.

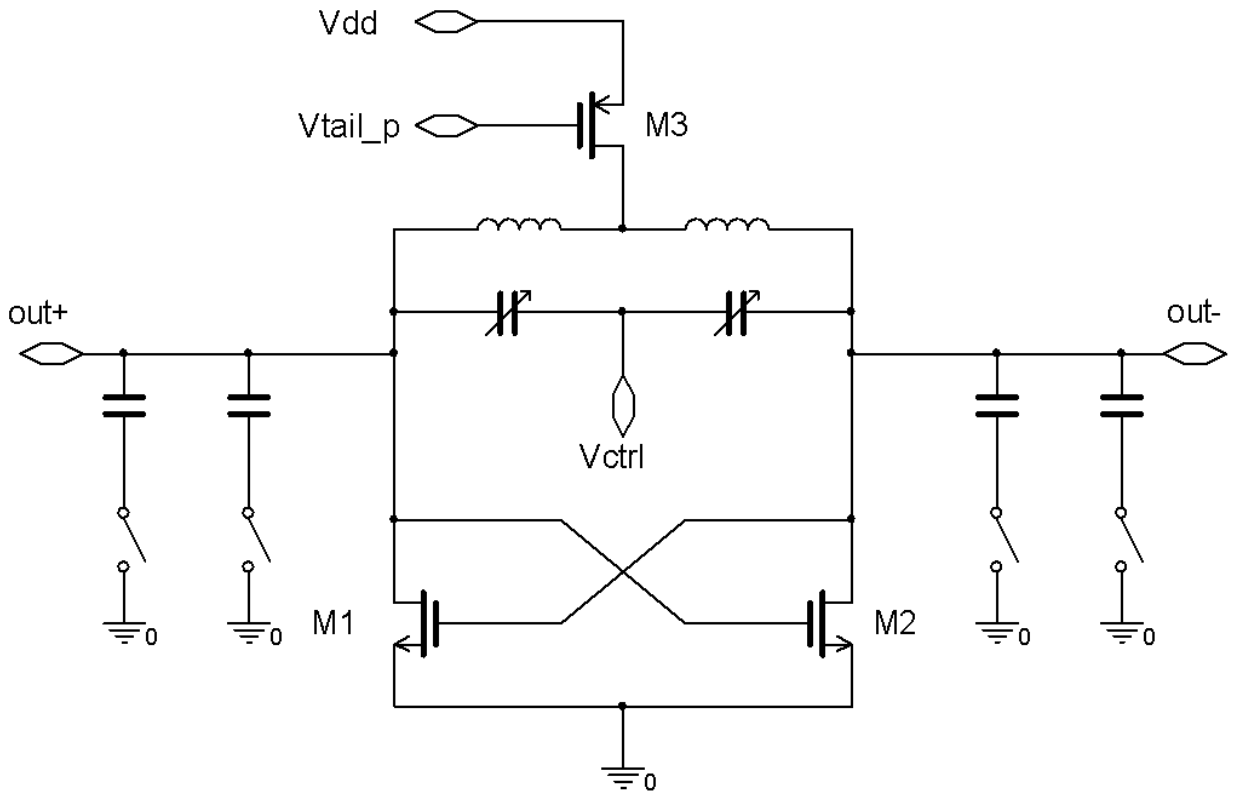


Figure 4-24. Schematic of the VCO.

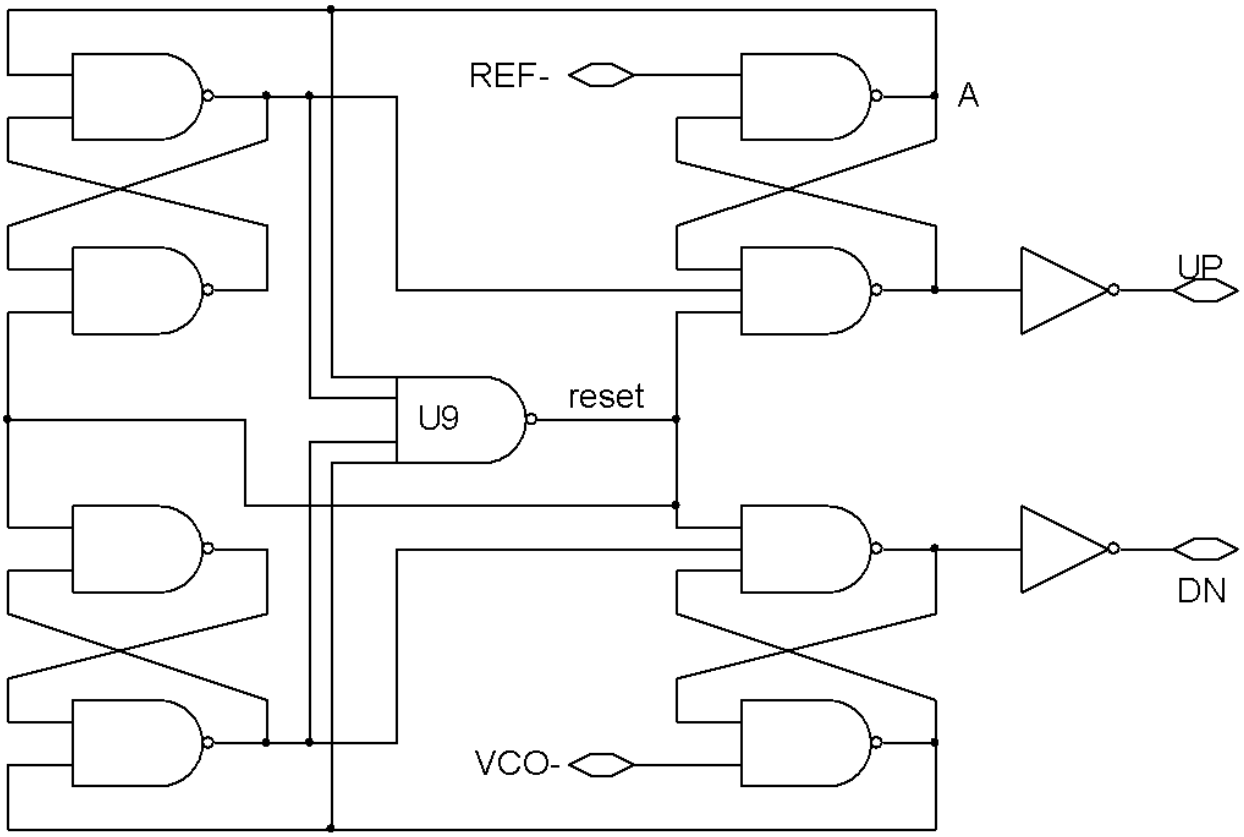


Figure 4-25. Gate-level schematic of the PFD.

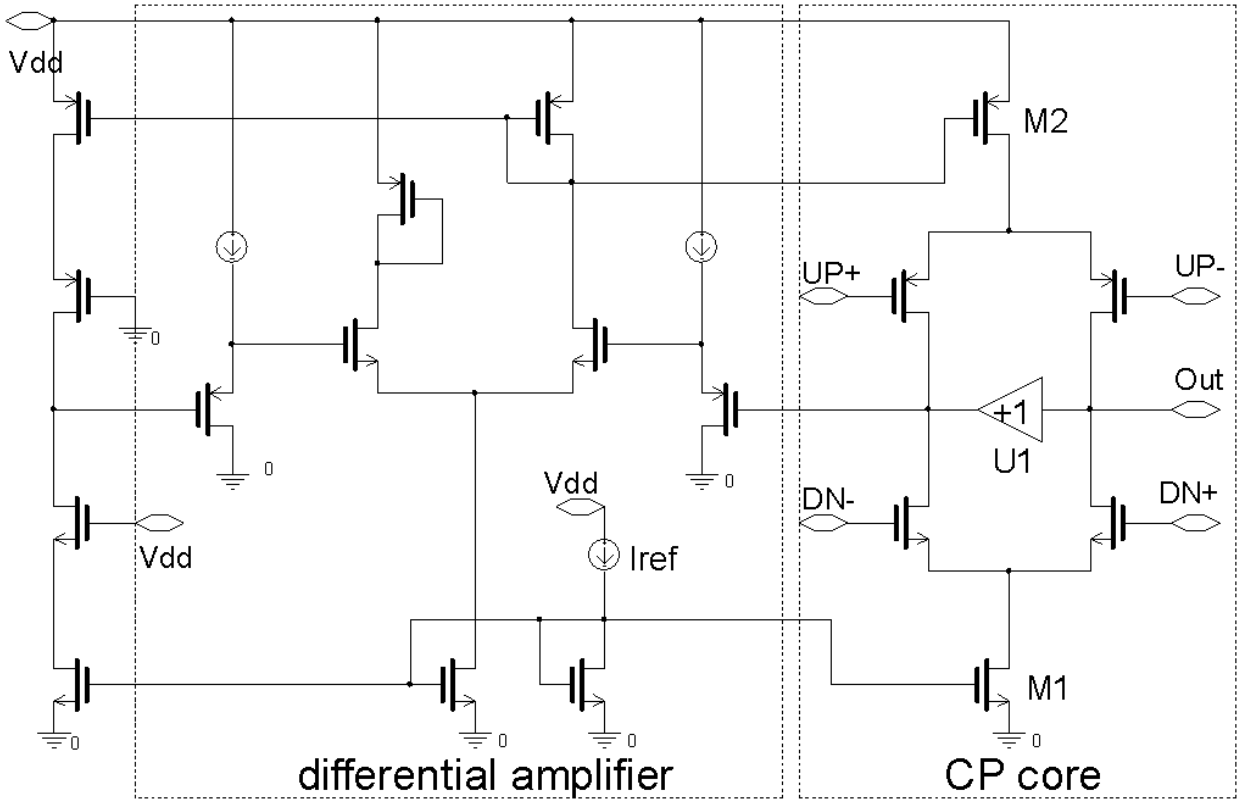


Figure 4-26. Simplified Schematic of the CP [51].

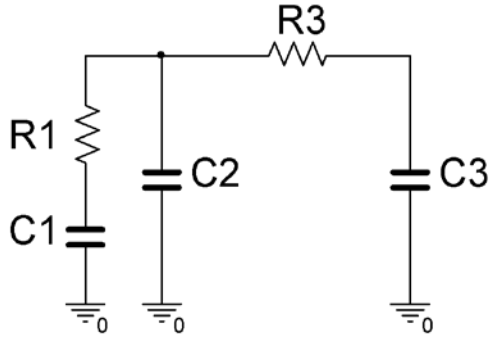


Figure 4-27. Schematic of the third-order passive loop filter.

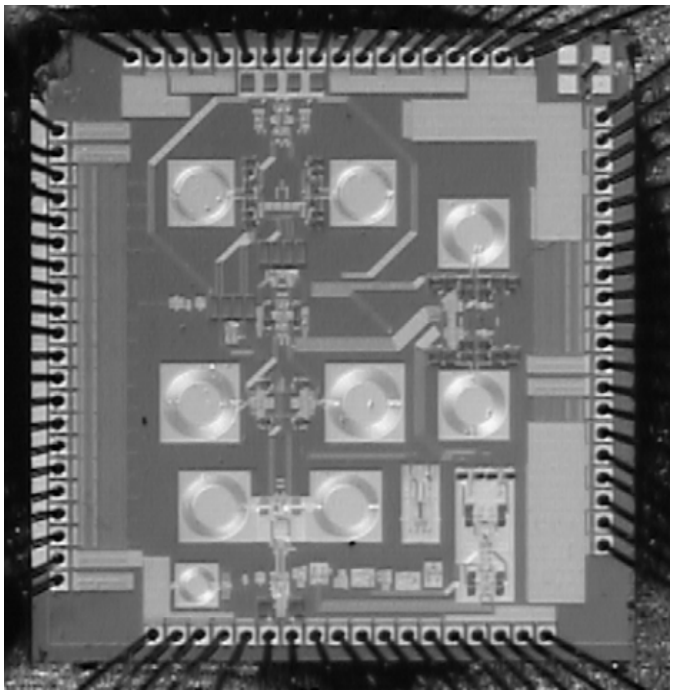


Figure 4-28. Die photograph of the proposed.

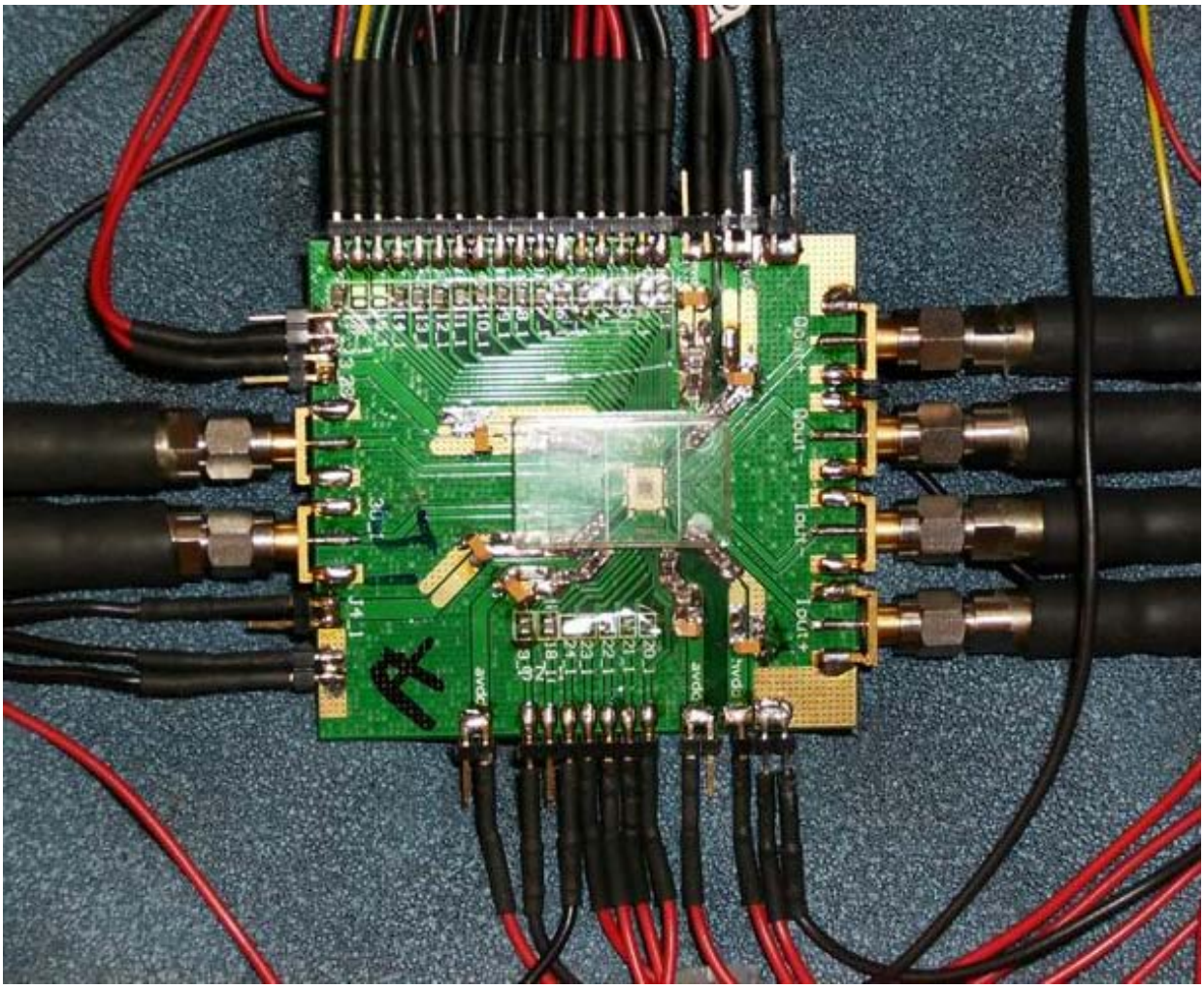


Figure 4-29. Photograph of the test board.

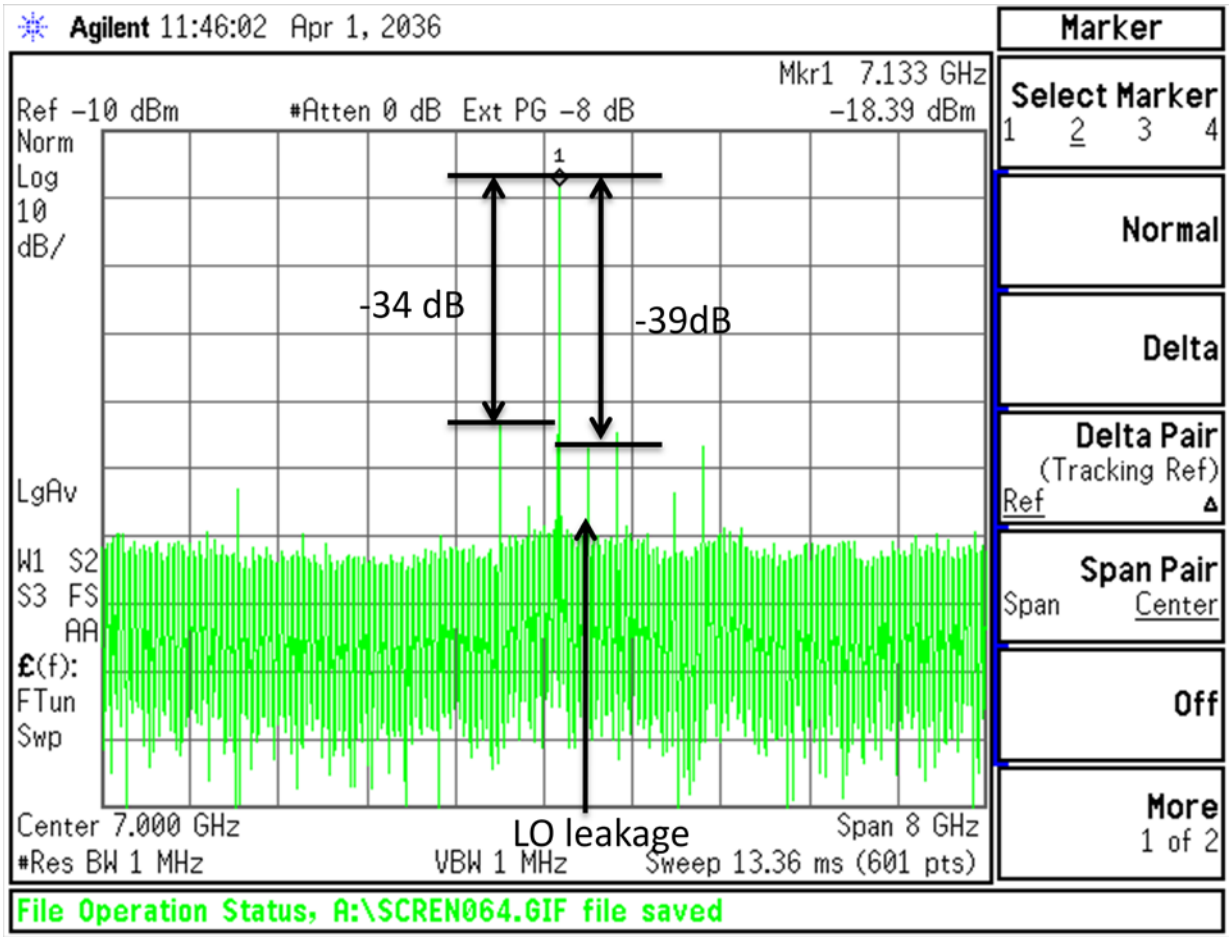


Figure 4-30. Output spectrum of the entire frequency synthesizer at Band 8 (7128 MHz).

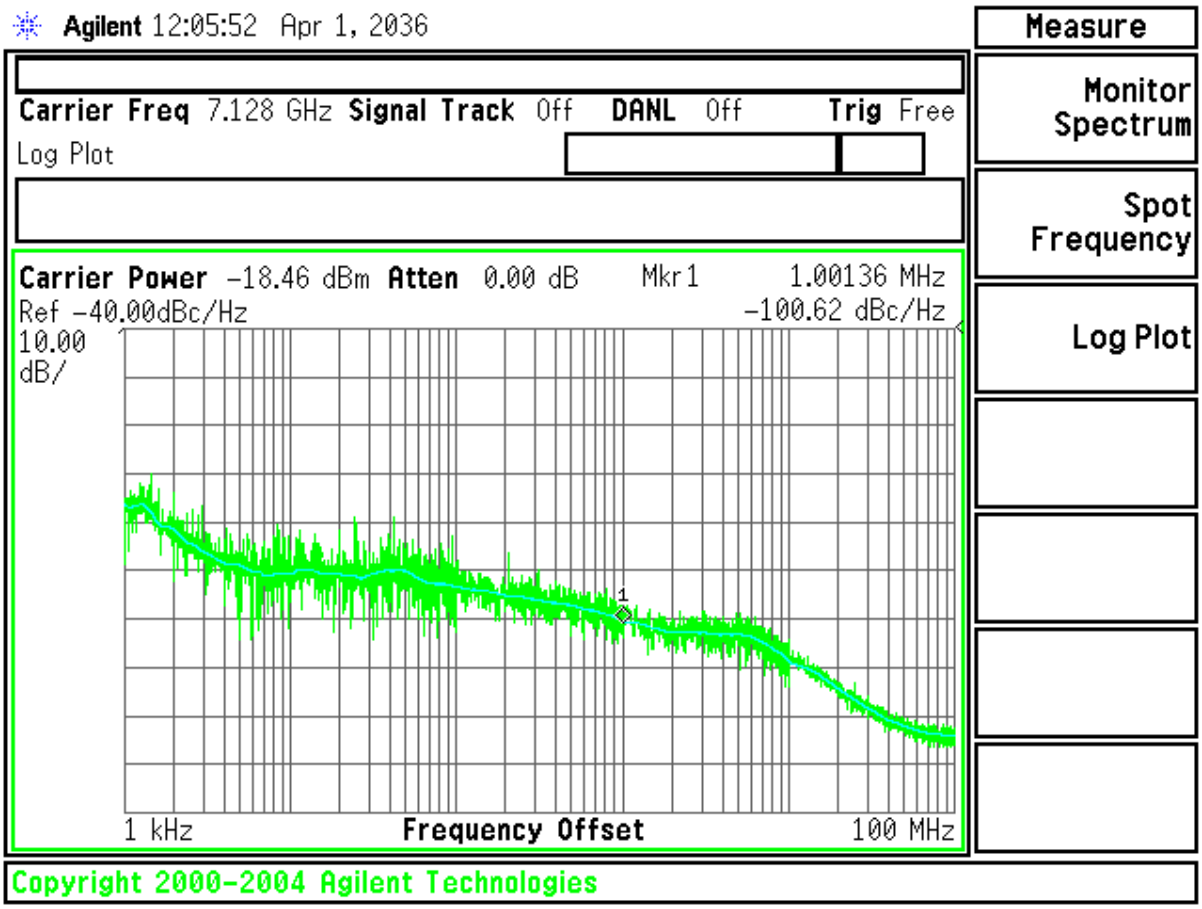


Figure 4-31. Phase noise of the output the entire frequency synthesizer at Band 8.

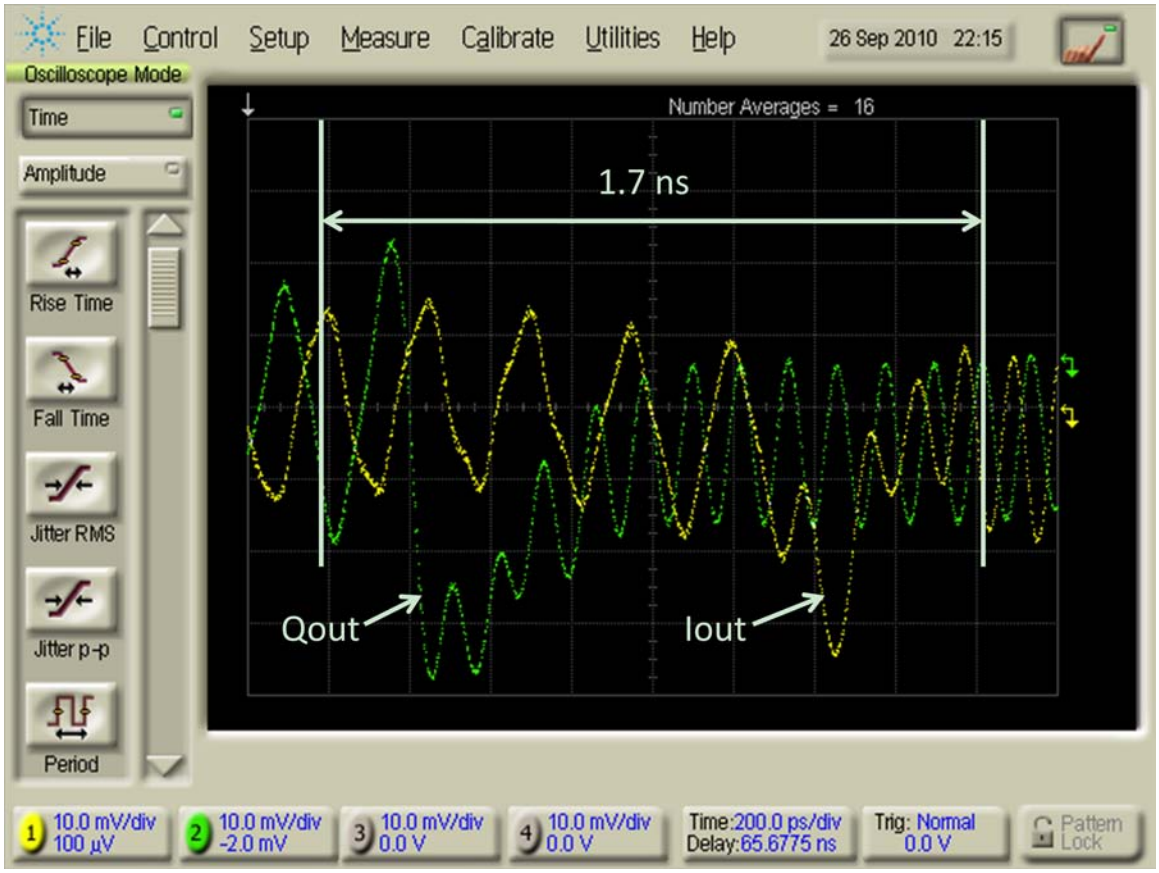


Figure 4-32. Band switching behavior with the longest settling time from Band 3 (4488 MHz) to Band 8 (7128 MHz).

Table 4-1. Summary of the minimum requirements of 14-band UWB frequency synthesizer

Bandwidth	3432 – 10296 MHz
Number of bands	14
Band spacing	528 MHz
Switching time between adjacent bands	< 9 ns
Phase noise	< 87 dBc/Hz at 1 MHz
Aggregate power of spurs	< -24 dBc

Table 4-2. Estimated current consumption of each block of the proposed frequency synthesizer

Blocks	Current Consumption (mA)
PFD+CP	2
VCO with a buffer	6
Frequency divider chain with buffers	7
IQ calibration circuits with filters	5
Mixer 1 with an output buffer	4
Mixer 2 with an output buffer	4
Mixer 3 with an output buffer	4
Multiplexers	15
Total	47

Table 4-3. Measured phase noise at 1 MHz frequency offset and the highest spur level at each band

Frequency (MHz)	Band	Output power (dBm)	Phase noise @ 1MHz (dBc/Hz)	Highest spur (dBc)
3432	1	-14.9	-103	-40
3960	2	-16.7	-106	-41
4488	3	-18.1	-105	-41
5016	4	-21.2	-101	-36
5544	5	-19.9	-101	-35
6072	6	-23.3	-100	-34
6600	7	-19	-100	-40
7128	8	-18.4	-101	-34
7656	9	-19	-100	-34
8184	10	-20.3	-98	-39
8712	11	-19	-99	-35
9240	12	-23.9	-97	-36
9768	13	-25.2	-96	-38
10296	14	-27.2	-93	-37

Table 4-4. Performance comparison with recently published works

	This Work	[41]	[37]	[52]	[40]
Number of bands	14	14	14	14	12
Output frequency (GHz)	3-10	3-10	3-10	3-10	3-9.5
Number of PLLs	1	1	2	VCO only	1
Phase noise @ 1MHz (dBc/Hz)	-100	-98*	N/A	-97*	-98
Highest spur (dBc)	-34	-37	-30	-35	-20

Table 4-4. Continued

	This work	[41]	[37]	[52]	[40]
Settling time (ns)	1.7	3	3	7	2
Power consumption (mW)	50**	117	162	59	47
CMOS technology	0.13 μm	0.18 μm	0.18 μm	0.13 μm	90 nm

*Phase noise of PLL only not the entire system.

**Average power consumption weighted to the number of bands (the highest is 56 mW).

CHAPTER 5
SUMMARY AND FUTURE WORK

5.1 Summary

This dissertation focused on RF front-end circuit block level for multi-octave bandwidth frequency agile systems. In Chapter 1, motivations of frequency agility was given and followed by a brief history. A number of modern applications were introduced. Among those applications, FASR and MB-OFDM UWB are two good examples that require multi-octave or multi-decade GHz bandwidth. To achieve such wide bandwidths, a 0.1-20 GHz LNA using CMOS 90 nm technology was reported in Chapter 2. To determine the architecture, four popular architectures were summarized and compared. Then resistive-feedback architecture was chosen. The traditional resistive-feedback LNA was modified and improved step by step and analyzed in great detail. Simulation and measurement results with a good agreement showed that this LNA obtains the highest FOM with 20 GHz bandwidth, a sufficient power gain and lowest power consumption. To handle high input and output power, a GaN HEMT MMIC LNA with an even wider bandwidth of 24 GHz was presented in Chapter 3. This bandwidth is the widest reported to date. The design and analysis principles are similar to those of the CMOS LNA due to similar transistor models. A complete set of simulation and measurement results was provided. A comparison between the CMOS LNA and the GaN HEMT LNA showed that despite higher power consumption with comparable small-signal performances to the CMOS LNA, the linearity is hundreds of times higher. Such a high linearity and a high capability of input power can remove filters and protection circuits preceding the LNA, and thus increase the minimum NF of the whole receiver. Another key block of RF front end, a frequency synthesizer, was then introduced in Chapter 4. Brief information of MB-OFDM UWB and specifications of its frequency synthesizers were given. Almost all published works were surveyed and grouped into

four different methods. The tradeoffs, benefits and drawbacks of the four types were discussed in detail. It was shown that only the SSB mixing method can achieve 14 bands with a high expansion capability. To lower power consumption and circuit complexity, a new frequency synthesizer was proposed. The frequency plan, block diagram and transistor-level circuit implementation were carefully designed and analyzed. Its power consumption is the lowest with comparable performance among all complete full-band UWB frequency synthesizers reported to date.

5.2 Future Work

With the demonstration of the two key circuit blocks of RF front-end for multi-octave bandwidth frequency agile systems, an entire receiver with a bandwidth from 3-10 GHz could be built with a wideband mixer in the future. As discussed in Chapter 4, the 14-band OFDM UWB frequency synthesizer could be extended to 18 GHz, if the VCO is replaced by a QVCO at 8448 MHz and one more SSB mixer is added. Therefore, with such a frequency synthesizer, the 20 GHz bandwidth LNA demonstrated in Chapter 2 and wideband mixers, a 3-18 GHz frequency-agile receiver is ready to build in future. Aside from the MB-OFDM UWB systems and FASRs for solar observation shown in Chapter 1, this system may also be used in Dopplar radar systems for vital sign detection.

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BIOGRAPHICAL SKETCH

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