A LOW VOLTAGE SUBTHRESHOLD ALL DIGITAL PHASE LOCKED LOOP FOR ULTRA LOW POWER BIOMEDICAL MICROSYSTEMS

By

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To my Mom, Dad, Bro and Megha

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Biomedical micro-systems have very stringent space and low power constraints and need to accomplish data sensing and communication in a cost effective way. A clock signal is required by on-chip analog and digital components for sampling or processing the gathered data as well as for synchronizing the system. Although the power constraints are rigid, the clock frequency requirements are relaxed as the majority of biomedical signals reside at low frequencies. Thus low power, low area, low frequency, low voltage operation and simple implementation are the key features required by a clock generator in order to be incorporated in implantable biomedical systems or sensor networks.

Off-chip components such as crystal oscillators can provide a very stable clock, but they are not suitable for these systems mainly because of their large size and high power consumption. Monolithic oscillators such as relaxation oscillators which consume low power and occupy significantly low area are preferred for clock generation. An efficient frequency calibration scheme is also needed to reduce drift in the oscillation frequency due to process variations [1]. Motivated by these factors, we present the

design of a very low power sub-threshold digital phase locked loop (DPLL) employing a ring oscillator, for clock generation in biomedical micro-systems. The DPLL can be used as a frequency multiplier with programmable gain factors to generate a signal at higher frequencies which is an exact multiple of the reference clock. Thus the local clock of the system can be synchronized to a wireless low frequency signal and enable data communication.

The main advantage of a digital implementation is that it remains functional even as the operating voltage is scaled down for decreased power consumption. A passive transceiver system employing the proposed DPLL was implemented in a 130nm CMOS process. It has a tunable output frequency range of 384 kHz -1.54 MHz. All blocks of the DPLL operate from a 260 mV supply in the sub-threshold region and consume an average power of 200 nW while producing an output frequency of 1.28 MHz. A Register Transfer Level (RTL) behavioral model of the DPLL was developed and its functionality was verified using mixed signal simulation tools in the Cadence suite. All blocks besides the digitally controlled oscillator (DCO) were implemented using synthesis and automated place and route tools.

CHAPTER 1
INTRODUCTION

1.1 Overview

The focus of this work is on the usage of a low voltage digital PLL as the clock generator block in low power biomedical micro-systems. PLLs have traditionally been made from analog building blocks, but with recent advancements in IC design technology the focus has shifted to their digital implementation as a result of various advantages such as reduced power and area. Low power and area are the primary requirements of a clock generator in biomedical systems as they have limited power resources and should incorporate functionalities such as sensing, data processing and communication in a simple and efficient way.

Operating circuits in the sub-threshold region reduces the power consumption significantly. Due to the relaxed frequency constraints in the targeted applications, sub-threshold logic can be used for implementing the digital circuits. Motivated by these factors we investigated the use a sub-threshold DPLL for synchronized clock generation in biomedical systems. Behavioral modeling and mixed signal simulation methodologies have been employed to quickly validate the functionality of the design. Automated place and route tools have also been used to reduce the turn-around time. Also, the behavioral model of the DPLL can be easily ported to other technologies without much modification.

1.2 Motivation

Wirelessly powered embedded systems with data transfer capability have been widely used in various applications. For example, a design of an implantable device which mimics the functionality of a photoreceptor is presented in [2], while a remotely

controlled implantable drug delivery system is described in [3]. In both these applications, the DC supply voltage is generated by rectification of the RF signal received at the antenna interface. In order to maximize the communication range, these systems require high RF-DC conversion efficiency and low power consumption building blocks.

A local clock is required by the baseband signal processing block for decoding the received data as well as for sending the generated data back. It can also be used by an analog interface which is connected to a temperature or humidity sensor in a wireless monitoring application. Reconfigurable property of the local clock can also prove to be very useful. With this additional feature, the system can adapt itself to communicate with other systems working at a different clock rate. Also, on-chip data can be modulated and sent back at a frequency away from the carrier to mitigate the effect of interference.

The clock frequency generated in these systems can drift with process and temperature variation, leading to synchronization failures. In this situation, the remotely sent commands cannot be interpreted properly to perform the desired operation by the system and the interrogator is unable to recover the backscattered data sent from the monitoring device. Thus, a careful design procedure is required to keep the power consumption and overall cost of implementation down. Various oscillator topologies with different tuning techniques have been proposed in the past to address these issues. However, PLLs have not been incorporated mainly because they are considered to consume too much power and area [4]. An extremely low power Digital Phase Locked Loop (DPLL) with a negligible area overhead is presented in this thesis to lock the oscillator to a desired frequency.

1.3 Thesis Organization

This thesis presents a design of a very low power DPLL suitable for biomedical micro-systems and addresses some of the implementation issues. A brief overview of analog and digital PLLs is presented in Chapter 2 along with a literature survey of various DPLL designs and oscillator topologies. A detailed analysis for deriving the timing jitter expressions for single ended ring oscillators working in the sub-threshold regime is also presented in this chapter. Implementation details of the system are described in Chapter 3 for explaining the design choices for each block. A functional verification methodology along with various simulation and measurement results is described in Chapter 4. Finally, various conclusions are discussed in Chapter 5.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction to PLL's

A Phase Locked Loop (PLL) is a control system with negative feedback that synchronizes an output signal with respect to both frequency and phase of an input signal. In locked state, the phase difference between the PLL's output and reference signal is either zero or remains constant [5]. A general block diagram of a PLL is shown in Figure 2-1, which consists of three main blocks, namely a phase detector (PD), a loop filter and a tunable voltage controlled oscillator. Initially, the PLL is in an unlocked state and the phase detector compares the two signals $U_{in}(t)$ and $U_{div}(t)$. Over time as the phase error ($U_{err}(t)$) builds up, the system adjusts the oscillator frequency such that this phase error is mitigated(ideally zero). The closed loop phase transfer function for the system is given by equation 2-1.

$$H(s) = \frac{\Theta_{div}(s)}{\Theta_{in}(s)} = \frac{K_o K_d F(s)/N}{s + K_o K_d F(s)/N} \tag{2-1}$$

Where K_o, K_d /s and F(s) are Laplace transforms of transfer functions of the phase detector block, voltage controlled oscillator and the loop filter respectively.

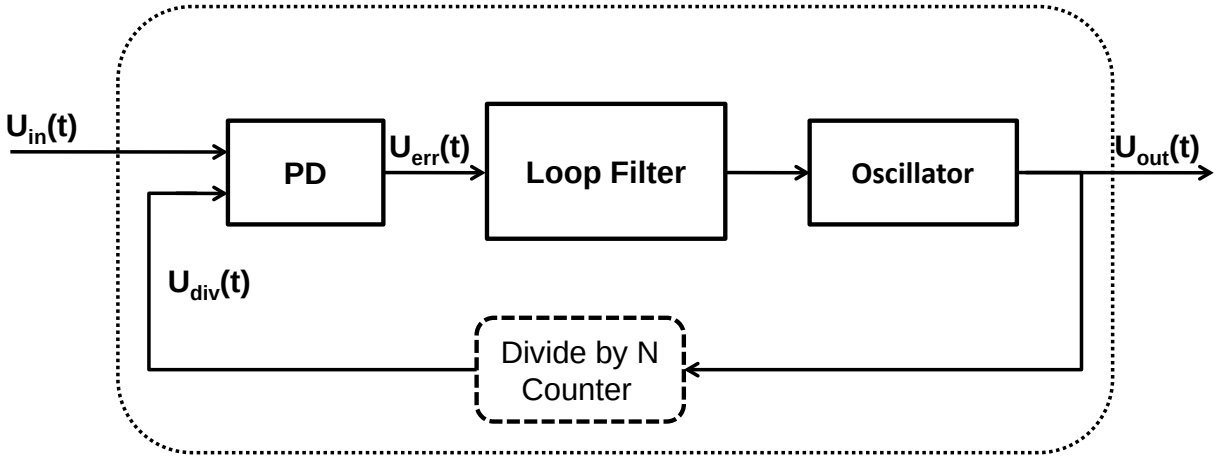


Figure 2-1. Block diagram of a PLL

In order to understand certain system concepts it is important to consider a particular PLL implementation.

2.1.1 Charge Pump Based Phase Locked Loop

The charge pump based PLL shown in Figure 2-2 is a classic example of an analog implementation. It consists of the combination of a phase frequency detector (PFD) and a charge pump which either charges or discharges the loop filter capacitor through switches (S1 and S2) based on the UP and DOWN signals. A phase detector block is an integral part of PLL systems as shown in Figure 2-1, however a frequency detection loop can be used in conjunction with the phase detector loop to increase the acquisition range [6]. Sequential logic phase and frequency detectors with a charge pump circuit are a cost effective solution to increase PLL system performance [7].

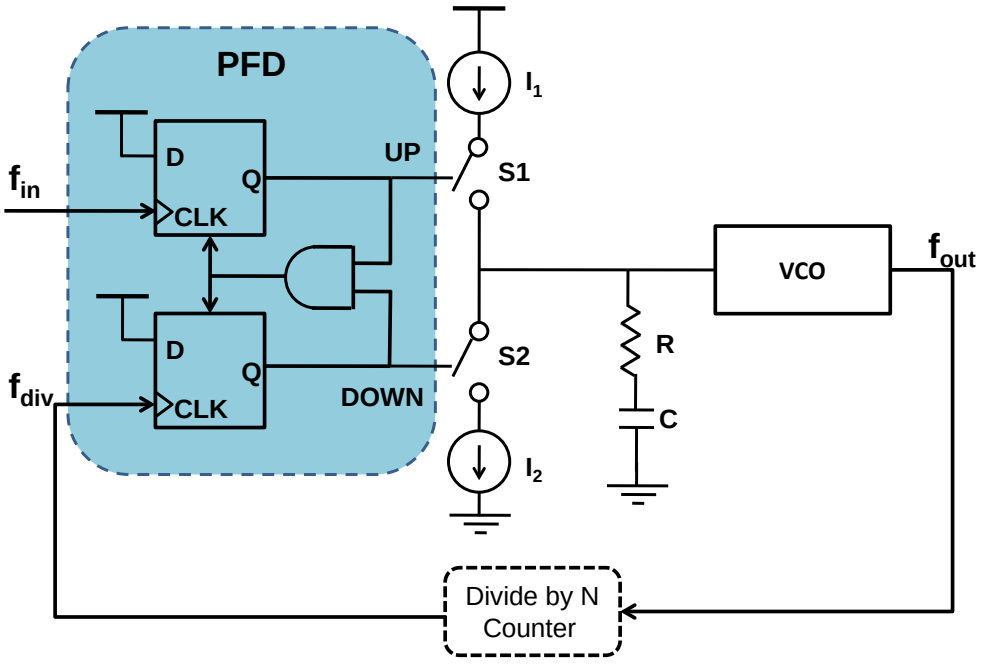


Figure 2-2. Charge pump PLL

The average value or duty cycles of the UP and DOWN signals can easily identify whether the input reference frequency (f_{in}) is less than or greater than the output

frequency (f_{out}) . Initially when f_{div} is far away from f_{in}, the PFD acts as a frequency detector and continuously pumps current in one direction into the loop filter to charge the capacitor which increases the output frequency f_{out}. When f_{in} and f_{div} are close, the PFD acts as a normal phase detector and a steady control voltage is supplied to the oscillator to maintain the locked state. This discrete time system can be approximated as a continuous time system as described in [6] whose open loop and closed loop transfer functions are given by equations 2-2 and 2-3.

$$H(s)_{open} = \frac{I}{2\pi}\left(R + \frac{1}{Cs}\right)\frac{K_{VCO}}{sN} \tag{2-2}$$

Since the open loop transfer function has two poles at the origin one due to the oscillator and the other one due to the loop filter, it is a Type-2 PLL.

$$H(s)_{closed} = \frac{\frac{IK_{vco}}{2\pi CN}(RCs+1)}{s^2 + \frac{I}{2\pi}\frac{K_{vco}}{N}Rs + \frac{I}{2\pi C}\frac{K_{vco}}{N}} \tag{2-3}$$

The closed loop transfer function can also be expressed in terms of damping factor (ζ) and natural frequency (ω_n) as in equation 2-4 and easily analyzed as second order systems.

$$H(s) = \frac{2\varsigma\omega_n s + \omega_n{}^2}{s^2 + 2\varsigma\omega_n s + \omega_n{}^2} \tag{2-4}$$

By comparing equation 2-3 with 2-4, the natural frequency and damping factor can be expressed as in equations 2-5 and 2-6, where R and C are the passive components of the loop filter and I_1 and I_2 are the charge pump currents ($I=I_1=I_2$).

$$\omega_n = \sqrt{\frac{IK_{vco}}{2\pi CN}} \tag{2-5}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{ICK_{vco}}{2\pi N}} \tag{2-6}$$

A magnitude response of the closed loop transfer function $|H(j\omega)|$ for different damping factors is shown in Figure 2-3. The frequency axis is normalized by the natural frequency ω_n which allows this plot to be valid for second order Type 2 PLL's in general [5].

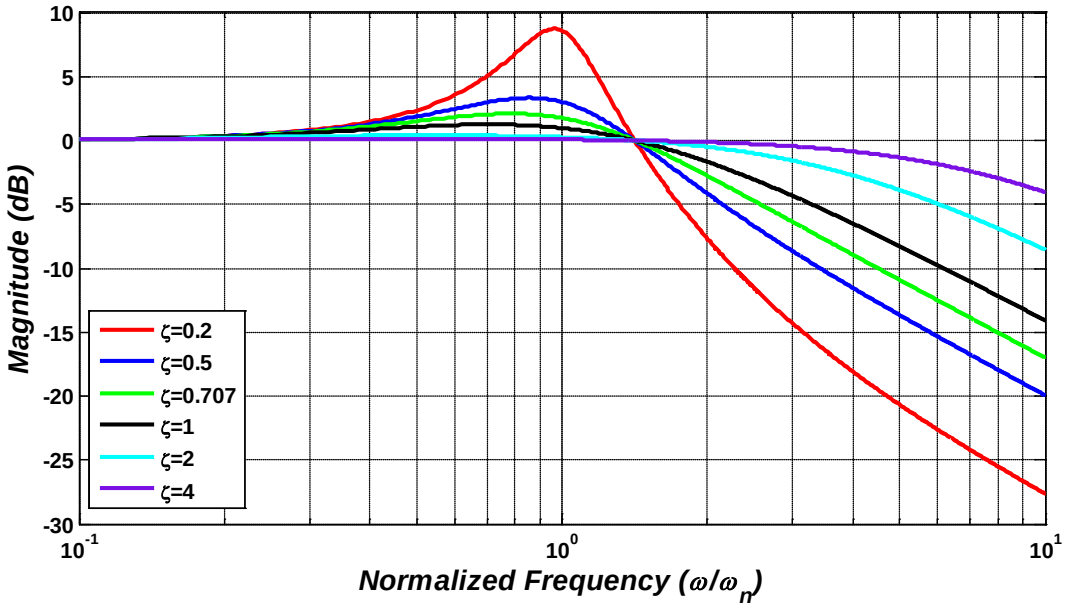


Figure 2-3. Magnitude response of the closed loop transfer function for different damping factors

Low values of τ (less than 1) result in poles with complex values, and the peaking in magnitude is mainly due to poles being located close to the imaginary axis of the s-plane. However at higher values of τ, the slight peaking in $|H(j\omega)|$ arises mainly due to the location of the zero. By increasing loop gain (in turn damping factor) the nearest pole and zero come closer, affectively reducing peaking of $|H(j\omega)|$ [8]. We can see in Equation 2-3 that the system has a zero at $(-1/RC)$ which is necessary to make the system stable. Without the resistor in place, the system will simply have two poles at the

origin which will contribute to a total phase shift of -180° at the unity gain frequency, making the system oscillatory. In general for a type-n PLL, n-1 zeroes are required to make it stable [8]. By choosing values of R, I and K_{VCO}, a sufficiently high damping factor can be realized and location of the zero can also be adjusted.

As stated earlier, a PLL system tends to minimize the phase error between the input ($f_{in}(t)$) and the divided signal ($f_{div}(t)$). The error transfer function is given by equation 2-7 and the magnitude plot is shown in Figure 2-4. For input frequencies less than the natural frequency (ω_n), the phase error is quite small and is further suppressed by keeping the damping factor high.

$$H_{err}(s) = 1 - H(s) = \frac{s^2}{s^2 + 2\varsigma\omega_n s + \omega_n{}^2} \tag{2-7}$$

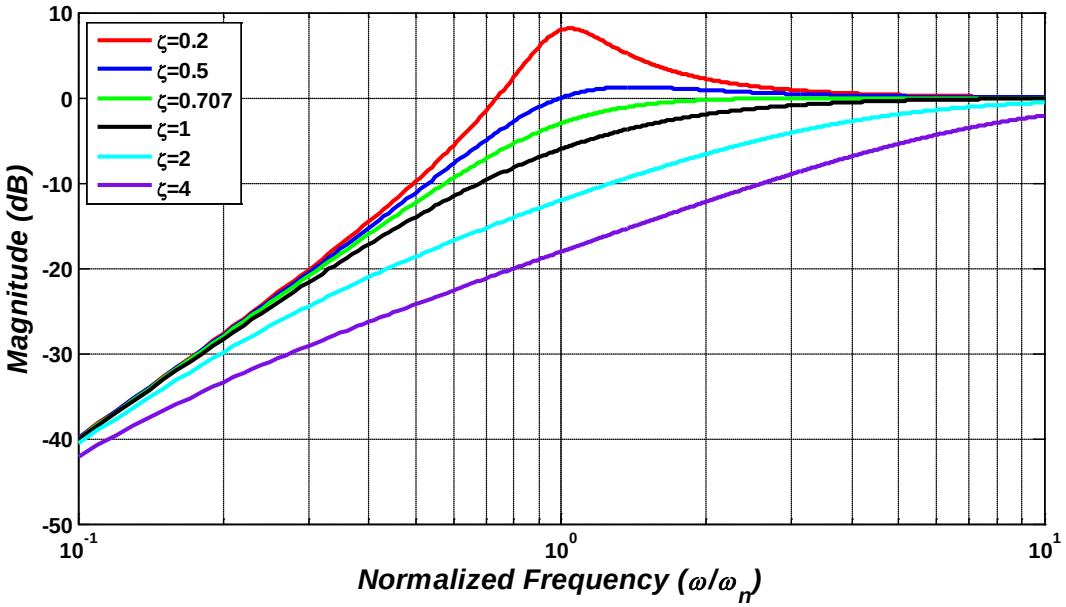


Figure 2-4. Magnitude response of the error transfer function for different damping factors

The performance of charge pump PLLs is limited by various circuit level non-idealities such as current mismatches between I_1 and I_2, as well as clock feed through.

All these factors introduce ripple into the control voltage which disturbs the locked state of the PLL. Normally the loop bandwidth is kept around one tenth of the input frequency. Thus for low frequency signals, the size of the loop filter capacitor and resistor has to be made very large to meet this bandwidth criteria.

2.1.1.1 PLL Response to a Phase Step

When the PLL is in a locked state and there is a change in the phase of the input reference clock, the PLL is always able to recover from such a perturbation. This can be understood by the following analysis. If a phase change of $\Delta\theta$ occurs in the incoming signal as shown in equation 2-8 (Laplace transform shown in equation 2-9), The error transfer function of the PLL is given by equation 2-10. By substituting s=0 it can be seen that the error always evaluates to zero.

$$\theta_i(t) = u(t)\Delta\theta \tag{2-8}$$

$$\theta_i(s) = \frac{\Delta\theta}{s} \tag{2-9}$$

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{s^2}{s + K_o K_d F(s)/N} \frac{\Delta\theta}{s} \tag{2-10}$$

2.1.1.2 PLL Response to a Frequency Step

If the input frequency changes by a factor of $\Delta\omega$, then the PLL experiences a phase change of $\Delta\omega$*t at the input. The Laplace transform for this phase change is given by equation 2-11 and the error transfer function is given by equation

$$\theta_i(s) = \frac{\Delta\omega}{s^2} \tag{2-11}$$

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{s^2}{s + K_o K_d F(s)/N} \frac{\Delta\omega}{s^2} \tag{2-12}$$

As can be seen for s=0, the steady state error does not reduce to zero. This means that there will always be a steady state error due to the frequency step at the input which can be reduced by keeping the loop gain of the PLL high.

2.1.2 Digital Phase Locked Loops

Several digital PLLs for different applications have been reported in [9-11], [12] because of their numerous advantages, some of which are lower chip area, lower power consumption, faster behavioral simulations and most importantly robustness against technology parameter variations. A block diagram for a typical linear DPLL is shown in Figure 2-5. It consists of a phase detector followed by a time to digital converter (TDC) to digitize the phase error followed by a digital loop filter and a digitally controlled oscillator. The resolution of the TDC is critical as it determines the amount of phase error that can be measured and ultimately filtered out. There are several ways to implement a TDC. A simple version can be made by using inverters as delay elements in the signal path as in [13]. Two counters clocked by a high frequency signal have been used in [9] for digitizing the phase error. The s-domain loop transfer functions for this class of DPLL can be obtained by applying the linear analysis techniques already described in Section 2.1.1 however, a discrete time z-domain model can more accurately predict the system behavior [14] since it is a sampled system. A detailed design procedure is described in [15] to obtain the value of various loop parameters by using an analogy between a charge pump PLL and a linear digital PLL. Also, the s-domain transfer functions can be converted to the continuous time z-domain model by using bilinear transforms. The main advantage of a digital PLL is that it requires a considerably small loop filter compared to that of the charge pump based PLL. The

digital components can also be operated at lower supply voltages to reduce the power consumption.

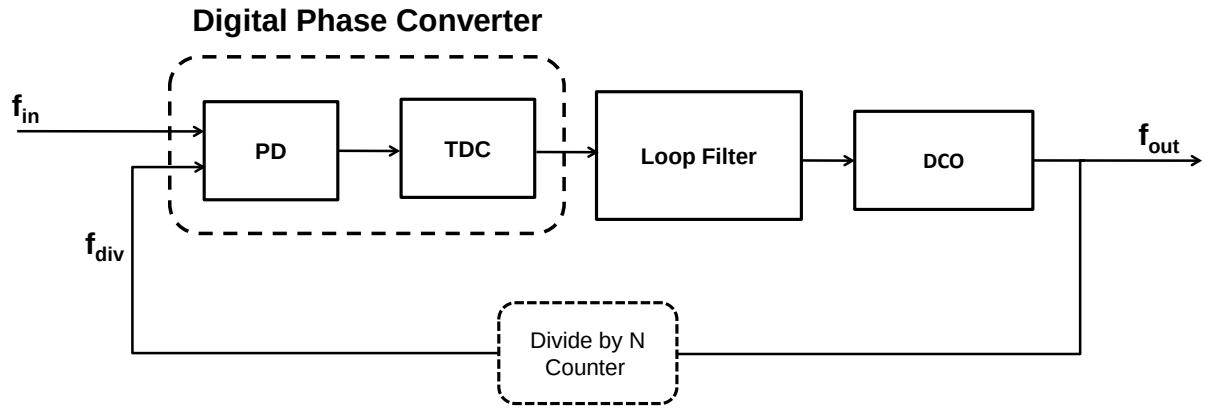


Figure 2-5. Digital phase lock loop

2.1.3 Bang-Bang Digital Phase Locked Loop

A PFD with a TDC is not only hard to design but also occupies substantial chip area and consumes excessive power, therefore it is not suitable for low power applications. An alternative to this approach is to use a binary phase and frequency detector (BPFD) where the phase/frequency difference is represented by only a single bit. Several bang-bang PLL (BB-PLL) designs are described in [10], [16] and [17]. Some limitations of this topology include increased frequency acquisition time and limited jitter performance. A block diagram for a BB-PLL with a proportional (K_P) and integral (K_I) path loop filter is shown in Figure 2-6. The single bit PFD output indicates whether f_{in} is leading or lagging the f_{div} signal. This information is used by the loop filter which operates at the divided down clock frequency to generate a control word to adjust the DCO frequency. In the locked state, a BB-PLL does not maintain a fixed phase difference, rather the control word changes between two relatively close values on each reference clock cycle.

Because the BPFD makes the system highly non-linear, system dynamics of a second order digital BB-PLL cannot be analyzed using either s or z-domain models. Some of the key results of the time-domain analysis of [18] are discussed here. One of the necessary conditions for locking is given by equation 2-13.

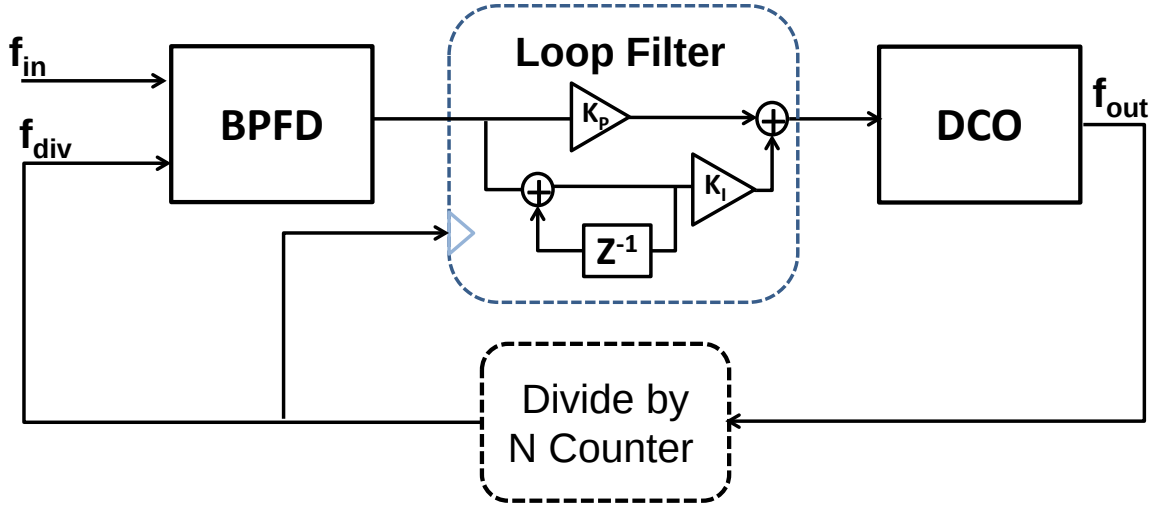


Figure 2-6. Bang-bang PLL

$$-1 < \left[x_0 = \frac{T_r - NT_{dco}}{NK_P K_T} \right] < 1 \qquad (2\text{-}13)$$

Where T_r is the reference clock period, T_{DCO} is the DCO free running period, K_T is the period gain constant of the DCO and NK_PK_T is the quantization step of the divided down clock. If this condition is not met, the time difference (Δt) between T_r and the divided down clock period (T_{DIV}) will never converge and the PLL will not lock. This implies that if the free running oscillator frequency is initially far away from the reference, the proportional path constant has to be sufficiently high.

The ratio of the proportional (K_P) and integral (K_I) path constants determine the stability of the BB-PLL. The other necessary condition for locking is given by equation 2-14, where D is the delay in the loop.

$$\frac{K_I}{K_P} < \frac{2}{2D+1} \tag{2-14}$$

The expression for the peak to peak jitter (J_{PP}) is given by equation 2-15 and it can be seen here that by minimizing K_I, D and N, the jitter can be reduced in the system. Increasing K_I helps in decreasing the locking time but this comes at the expense of increased jitter. Although having a higher value of K_P helps in ensuring stability, it cannot arbitrarily be kept very high as it also increases the quantization step of the proportional path which results in more jitter.

$$J_{pp} = NK_P K_T \left[2(1+D) + (1+D)\left(\frac{K_I}{K_P}\right) + (1+D)^3 \left(\frac{K_I}{K_P}\right)^2 + O\left(\frac{K_I}{K_P}\right)^3 \right] \tag{2-15}$$

These findings are in close agreement with those of [16] which mainly highlight the effect of the loop filter parameters on the stability of a low power, compact and low jitter DPLL. In the locked state, a linear discrete time model has been used to account for the results. The loop filter transfer function for the integral and proportional path digital filter (F(z)) is given by equation 2-16 and the closed loop transfer function for the entire DPLL (H(z)) is given by equation 2-17. From the root locus analysis described in this paper, it was shown that increasing K_P drives the system towards stability while increasing K_I mainly affects the closed loop bandwidth.

$$F(z) = K_P + \frac{K_I}{1 - z^{-1}} \tag{2-16}$$

$$H(z) = \frac{K_{dco}(K_P + K_I)\left(z - \frac{K_P}{K_P + K_I}\right)}{z^2 - \left(2 - \frac{K_{dco}(K_P + K_I)}{N}\right)z + \left(1 - \frac{K_{dco}K_I}{N}\right)} \tag{2-17}$$

2.2 Design Considerations for Low Power PLLs

After gaining an insight in the working of a PLL we now discuss some of the design issues that need to be considered for low power design.

2.2.1 Low Power Oscillator

Several on-chip clock generation schemes for low power applications have been reported, some of which are summarized in Table 2-1.

Table 2-1. Performance summary of various low power oscillators

Reference	Oscillator topology	Supply Voltage	Power Consumption	Operating Frequency
[19]	Injection locked divider /	0.5 V	6.7 µW	52 kHz-625 kHz
[20]	Relaxation	1 V	1.5 µW	52 kHz-625 kHz
[21]	Relaxation	0.8 V	320 nW	1.52 MHz
[22]	Current starved with digital caliberation	1.5 V	40 µW	2.2 MHz
[23]	Current starved ring	0.8 V-1 V	191 nW-306 nW	1.28 MHz
[4]	Current starved ring	-	0.4 µW	500 kHz
[20]	Current starved ring	0.7 V-1.2 V	200 nW	2.45 MHz

Ref. [19] describes a dual-path clock generator composed of injection locked dividers and a RC resonator. Here, the reference clock is derived directly from the RF carrier which guarantees high accuracy, however this scheme consumes too much power (7 µW approximately). By using a RC relaxation oscillator described in [21], the power consumption can be reduced. However, a huge area is required by the on-chip resistors and capacitors. Since, the output frequency is mainly determined by the value of these passive elements, it is unreliable. A voltage controlled oscillator consisting of a current starved ring oscillator with digitally calibrated bias current has been used in [22]. Although the ring oscillator alone consumes about 9.5 µW, the digital calibration

scheme requires about 31μW of power. Current starved ring oscillator based topologies described in [4] and [23] can be a good choice as they strike a balance between low power, area and frequency deviation [20] and also because they do not rely on passive components such as resistors, capacitors and inductors [24], [27] and [29].

LC oscillators are also a popular choice in PLLs because of their superior phase noise properties. However, in order to obtain a low oscillation frequency in the range of a few Megahertz, the size of the on-chip inductor and capacitor has to be kept substantially high. Also, the tuning range of LC oscillators is only in the range of 10-20% [25]. Thus, an LC oscillator cannot cater to the requirements of biomedical sensor network systems.

Ring oscillators are an attractive alternative mainly because of their simple architecture, low area, wide tuning range and ease of integration. Here, an odd number of inverters are connected in feedback to generate a periodic signal whose frequency is determined by the delay of each inverting stage. By increasing the delay of each cell, low oscillation frequencies can be easily obtained. However, this comes at the expense of a poor phase noise resulting in timing jitter, as single ended ring oscillators are more susceptible to variations in supply voltage. Due to the low speed requirements in the biomedical systems, this timing jitter can be tolerated since the emphasis is on low power consumption. Although ring oscillators with differential delay cells are more immune to various noise sources, they are not suitable in the applications of interest mainly because of their high power consumption and area requirements.

2.2.2 Sub-threshold Operation of Digital Circuits

Sub-threshold operation refers to operating circuits at a supply voltage (V_{DD}) lower than the threshold voltage (V_T) of a transistor. It involves charging and discharging the

load capacitor with the sub-threshold leakage current and is able to achieve minimum energy consumption with limited speed performance [26-27]. It has been incorporated in low power applications such as a FFT processor and hearing aids [28-29], and can be applied in biomedical micro-systems which have very limited power available. For the 130nm technology, the threshold voltages for n-MOS and p-MOS are 0.38mV and -0.33mV respectively. The expression for sub-threshold leakage current is given by equation 2-18 [29].

$$I_{DS} = I_{DS0} e^{\frac{V_{GS}-V_T}{nVth}} \left(1 - e^{\frac{-V_{DS}}{V_{th}}}\right) \quad (2\text{-}18)$$

Where I_{DS0} is the drain current when V_{GS} is equal to V_T (equation 2-19) [30]

$$I_{DS0} = \mu_0 C_{ox} \frac{W}{L} (n-1) V_{th}^2 \quad (2\text{-}19)$$

V_{th} is the thermal voltage and n is the sub-threshold slope factor given by equations 2-20 and 2-21 respectively.

$$V_{th} = \frac{kT}{q} \quad (2\text{-}20)$$

$$n = 1 + \frac{C_d}{C_{ox}} \quad (2\text{-}21)$$

For $V_{DS} > 4V_{th}$, equation 2-18 can be reduced to equation 2-22. At higher values of V_{DS} the exponential term becomes negligible.

$$I_{DS} = I_{DS0} e^{\frac{V_{GS}-V_T}{nVth}} \quad (2\text{-}22)$$

2.2.3 Jitter and Phase Noise in Ring Oscillators

Besides power savings, there are some additional benefits of using single ended ring oscillators (Figure 2-7) in terms of spectral characteristics. Ref. [31] derives the

expressions for phase noise and timing jitter for both single ended and differential ring oscillators by using impulse sensitivity functions (ISF is a time-varying constant that can determine the phase shift due to a noise source) and states that single ended ring oscillators have lower phase noise than their differential counterparts for a given power and frequency. It also states that the timing jitter in single ended oscillators can be minimized by equalizing the rising and the falling times.

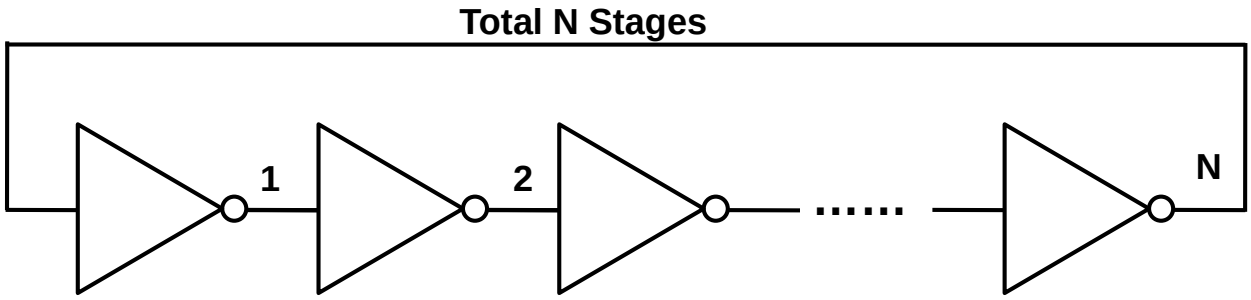


Figure 2-7. Single ended ring oscillator with identical N stages

Ref. [32] derives the expression for phase noise in ring oscillators in terms of power dissipation, temperature, frequency of oscillation and offset frequency by analyzing the time domain jitter. Some of the key results are discussed here. The variance of timing jitter for switching based relaxation and ring oscillators is directly proportional to the variance in the control voltage at the input. This variance in the control voltage at any time t is given by equation 2-23 [32].

$$\overline{\Delta V_c(t)}^2 = \frac{kTR}{CR_n}(1-e^{-2t/RC}) + \sigma_0^2 e^{-2t/RC} \qquad (2\text{-}23)$$

Where k is the Boltzmann constant, T is the temperature, R and C are the net resistance and capacitance at the input node, R_n is the equivalent thermal noise resistance and σ_0^2 is the variance of the control voltage at t=0. The variance in switching time jitter can be calculated by substituting equation 2-23 in equation 2-24 [32].

$$\overline{\Delta T_o}^2 = \overline{\Delta V_c(t)}^2 \left| \frac{dV_c}{dt} \right|^{-2} \tag{2-24}$$

In the model used for calculating the expressions for timing jitter of a ring oscillator similar to the one shown in Figure 2-7, each inverter (Figure 2-8) can either be in ON or OFF states. In the ON state, a constant current I either charges or discharges the load capacitor while in the OFF state no current is drawn from the supply.

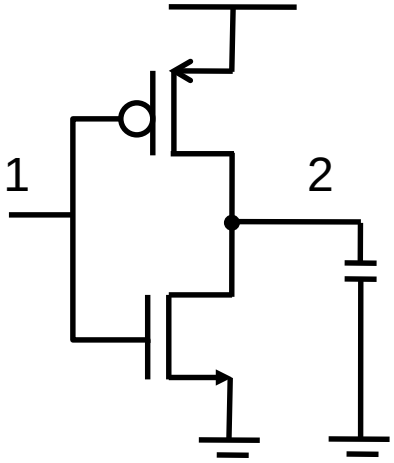


Figure 2-8. An inverter stage in the ring oscillator

In the ON state the output resistance is $1/g_{ds}$ while in the OFF state the output resistance will be $1/g_{d0}$. Where g_{d0} is given by equation 2-25.

$$g_{d0} = g_{ds}\big|_{V_{DS}=0} \tag{2-25}$$

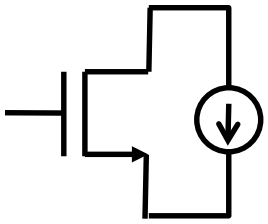
If the oscillator is working in the sub-threshold region then the output conductance g_{ds} can be calculated as in equation 2-26 by substituting the value of I_{DS} from equation 2-18.

$$g_{ds} = \frac{dI_{DS}}{dV_{DS}} = \frac{I_{DS0} e^{\frac{V_{GS}-V_T}{nVth}} . e^{\frac{-V_{DS}}{V_{th}}}}{v_{th}} \tag{2-26}$$

The output conductance (g_{d0}) at $V_{DS}=0$ is then given by equation 2-27.

$$g_{d0} = \frac{I_{DS0} e^{\frac{V_{GS}-V_T}{nVth}}}{V_{th}} \tag{2-27}$$

The thermal noise for a transistor can be represented by a parallel current source connected between the drain and source of a transistor as shown in Figure 2-9.



$$\Delta I^2 = 4kTG\Delta f = \frac{4kT\Delta f}{R_n}$$

Figure 2-9. Noise represented by a parallel current source in a transistor

For a transistor operating in the sub-threshold region, the equivalent noise resistance (R_n) is given by equation 2-28 [33].

$$R_n = \frac{2}{g_{d0}} \tag{2-28}$$

After representing the exponential function in terms of its Taylor series and substituting $\sigma_0^2 = \frac{kT}{C}$, assuming $t << RC$, equation 2-23 can be represented as equation 2-29 [32].

$$\overline{\Delta V_c(t)}^2 = \frac{kT}{C}\left(1 + \frac{2t}{R_n C} - \frac{2t}{RC}\right) \tag{2-29}$$

Now substituting $R_n = 2/g_{d0}$, $R = 1/g_{ds}$ and $t/C = V_{DD}/2I$ in equation 2-29, it can be represented as equation 2-30. For the condition $V_{DS} > 4V_{th}$, g_{ds} can be neglected.

$$\overline{\Delta V_c(t)}^2 = \frac{kT}{C}\left(1 + \frac{g_{d0}V_{DD}}{2I} - \frac{g_{ds}V_{DD}}{I}\right) \tag{2-30}$$

Using equation 2-30, the variance switching time jitter (equation 2-24) is given by equation 2-31.

$$\overline{\Delta T_s}^2 = \frac{kTC}{I^2}\left(1+\frac{g_{do}V_{DD}}{2I}\right) \tag{2-31}$$

In a ring oscillator with N stages, there are 2N independent switching events in each period. Thus, the net timing jitter for a ring oscillator operating in the sub-threshold region is given by equation 2-32.

$$\overline{\Delta T_0}^2 = \frac{2kTT_0^2}{NCV_{DD}^2}\left(1+\frac{g_{do}V_{DD}}{2I}\right) \tag{2-32}$$

Here the nominal period oscillation (T_0) is given by equation 2-33 [32].

$$T_0 = \frac{NCV_{DD}}{I} \tag{2-33}$$

Now substituting the values of g_{d0} and I corresponding to the sub-threshold region of operation from equations 2-27 and 2-22 respectively, the expression of timing jitter for the ring oscillator is given by equation 2-34.

$$\overline{\Delta T_0}^2 = \frac{2kTT_0^2}{NCV_{DD}^2}\left(1+\frac{V_{DD}}{2V_{th}}\right) \tag{2-34}$$

For an oscillation frequency of f_0, the power consumption for a ring oscillator with N stages is approximately given by equation 2-35 . Thus, the relationship between timing jitter and power consumption at a given oscillation frequency (f_0) is given by equation 2-36. We can clearly see that the timing jitter is inversely proportional to the power consumption and should decrease in value at the expense of more power.

$$P = NCV_{DD}^2 \tag{2-35}$$

$$\overline{\Delta T_0}^2 = \frac{2kT}{Pf_0}\left(1+\frac{V_{DD}}{2V_{th}}\right) \tag{2-36}$$

Once the variance of timing jitter is determined, the phase noise at a given offset frequency can also be calculated by using equation 2-37 [32].

$$PN(\Delta f) = \frac{f_0^3 \overline{\Delta T_0}^2}{\left(\pi f_0^3 \overline{\Delta T_0}^2\right)^2 + \left(\Delta f\right)^2} \tag{2-37}$$

Thus at much higher frequency offsets, the phase noise can be approximated by equation 2-38.

$$PN(\Delta f) = \frac{2kT}{P}\left(1 + \frac{V_{DD}}{2V_{th}}\right)\left(\frac{f_0}{\Delta f}\right)^2 \tag{2-38}$$

For validating this model a ring oscillator with three inverters (Figure 2-10), operating in the sub-threshold region was designed and simulated in Cadence SPECTRE (APPENDIX A). The W/L for the p-MOS and n-MOS was set to (2µm/120nm) and (1.58 µm/120nm) respectively. At 250mV the oscillation frequency was 34.8MHz and the power consumption of the inverters in the ON state turned out to be 80nW approximately.

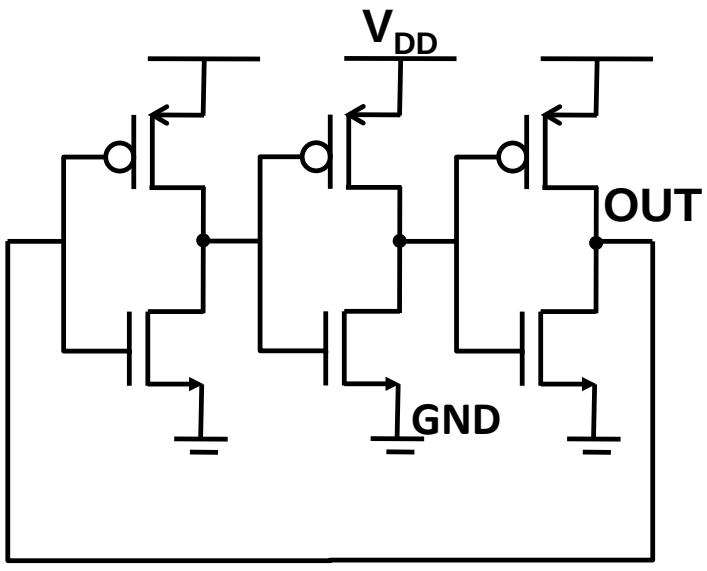


Figure 2-10. Ring oscillator to verify the phase noise model

The simulated and the predicted phase noise from equation 2-37, for this oscillator are compared in Figure 2-11. From this plot, we can see that the phase noise at an offset frequency of 1 MHz is -93.74dBC/Hz. The expected value of the phase noise at this offset frequency from equation 2-38 is -90.2dBc/Hz (at room temperature).

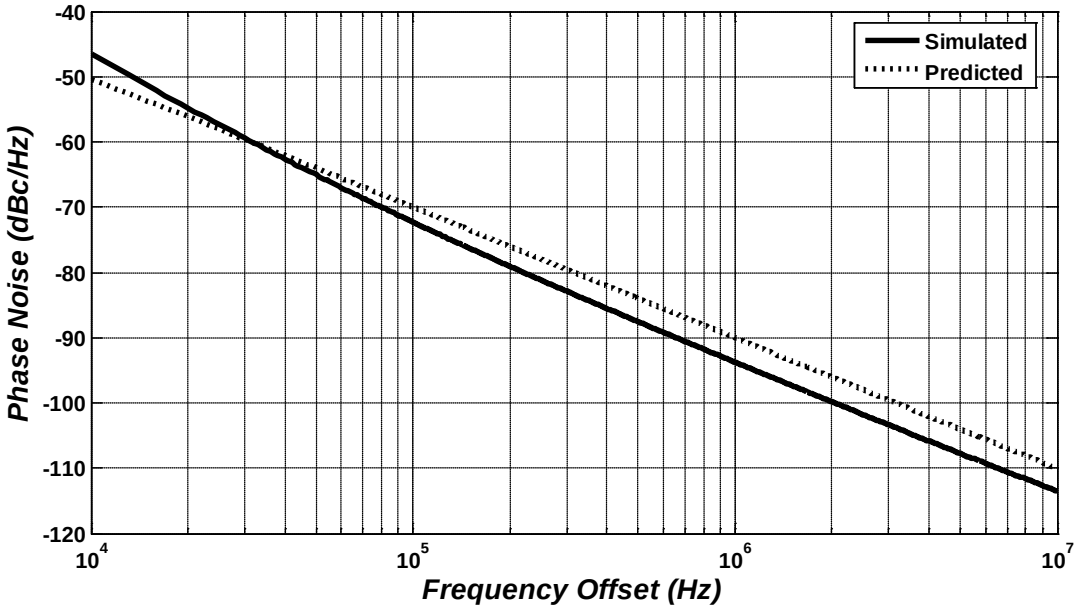


Figure 2-11. Comparison of simulated and expected phase noise for a ring oscillator running at 34.8MHz

Further, the oscillation frequency was varied by adding more inverter stages in the ring oscillator and keeping the supply voltage the same i.e at 250mV. The expression for minimum achievable phase noise for ring oscillators is given by equation 2-39 [32].

$$PN(\Delta f) = \frac{7.33kT}{P}\left(\frac{f_0}{\Delta f}\right)^2 \tag{2-39}$$

The phase noise is computed for different oscillation frequencies by using both formulas (equation 2-39 and equation 2-38) and are results are mentioned in Table 4-1. We can clearly see that the value given by equation 2-38 is more close to the simulation result. Thus, we can use this model for a better estimate of the phase noise

performance of a ring oscillator working in the sub-threshold region for a given power constraint.

Table 2-2. Comparison of phase noise at 1MHz offset frequency at different oscillation frequencies

Number of stages in the Oscillator (N)	Oscillation Frequency (MHz)	Power Consumption (nW)	PN at 1MHz Offset (dBc/Hz) (eq. 2-39)	PN at 1MHz Offset (dBc/Hz) (eq. 2-38)	PN at 1MHz Offset (dBc/Hz) (Simulation)
3	34.8	58	-91.9	-97.62	-93.74
5	20.3	52.5	-96.25	-101.87	-98.3
7	14.43	52.9	-99.23	-104.86	-101.8
9	11.22	53.25	-101.45	-107	-104.5

CHAPTER 3
SYSTEM ARCHITECTURE

3.1 Basic Architecture of the System

A simplified block diagram for a typical passive biomedical micro-system is shown in Figure 3-1. It consists of an antenna port, a power management unit comprised of a voltage rectifier, voltage regulator and bias circuitry, an ASK modulator/demodulator, a clock generator and a digital baseband signal processor.

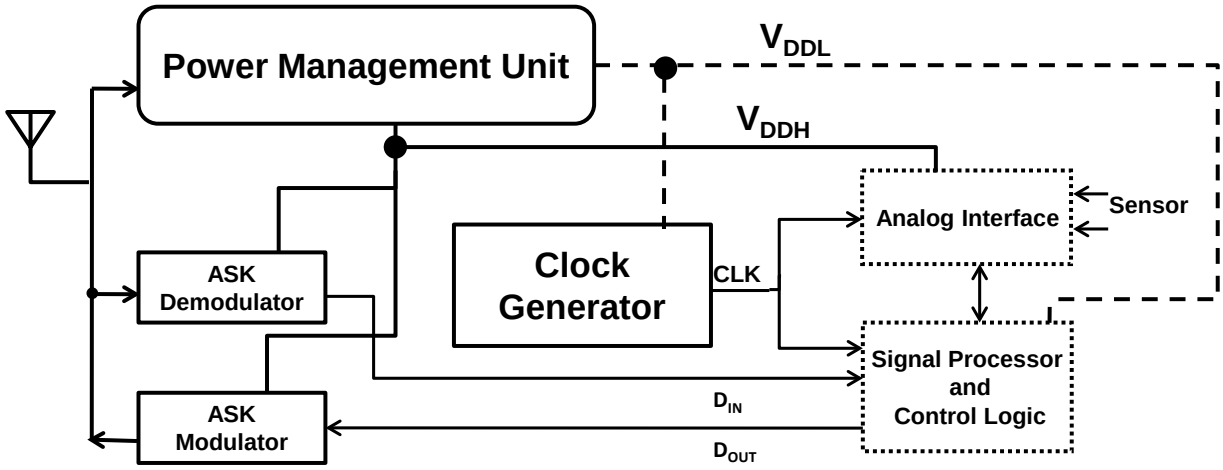


Figure 3-1. Block diagram of a typical biomedical micro-system with sensing and data communication capability

The power management unit is one of the most important components of the entire system as it provides the required voltages needed for operation by the various blocks and its efficiency is critical to system performance. The device is powered up by continuously sending a RF wave, which is rectified into a DC voltage. The power efficiency of the system can be improved by separating the supplies for analog and digital blocks (V_{DDH} and V_{DDL}). Digital blocks can be operated at a lower supply voltage which results in power savings. This allows the analog blocks to be unaffected by the voltage spikes which appear due to signal transitions in the digital blocks. Although, the

dynamic power dissipation decreases with the supply voltage scaling, the leakage current increases as it is exponentially dependant on the supply voltage [34].

The reference clock and commands for configuring the system are sent as ASK modulated signals along with the carrier. This information is extracted by the ASK demodulator and provided to relevant blocks. The backscattering scheme described in [22] is generally employed for sending the data back to the interrogator where the antenna impedance is varied between either a perfect match or complete mismatch i.e a short.

3.2 Digital Phase Locked Loop

Figure 3-2 shows the functional block diagram of the sub-threshold DPLL operated from a 260mV supply.

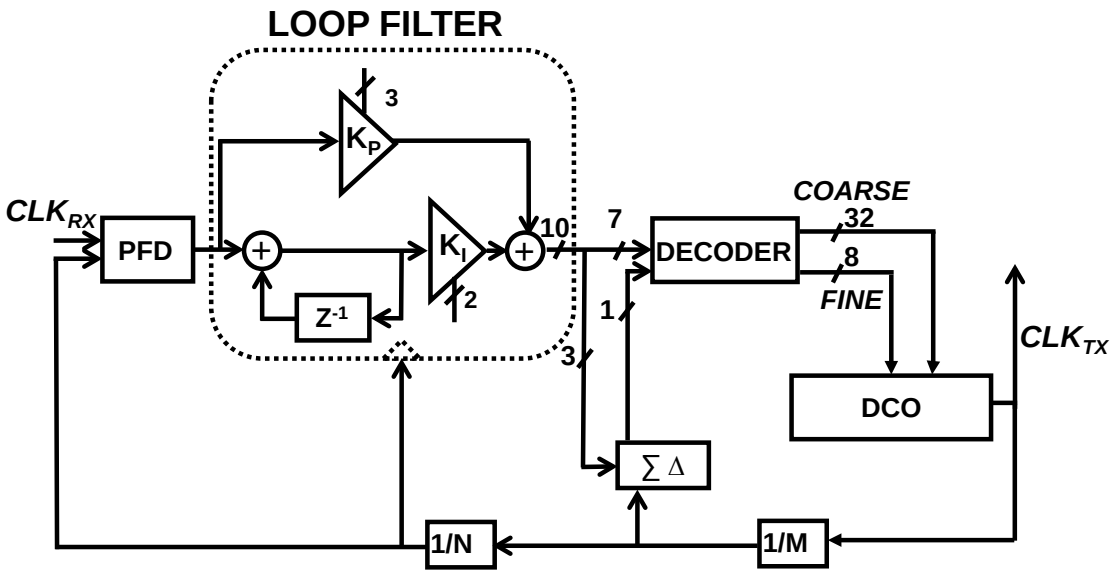


Figure 3-2. Implemented digital phase lock loop

A binary phase and frequency detector (BPFD) compares the divided down clock from the digitally controlled oscillator (DCO) with the extracted reference clock (CLK_{RX}) from the ASK demodulator to generate a single bit early/late signal. The digital loop filter

with programmable proportional (K_P) and integral (K_I) path gains is updated on every cycle of the divided down (1/(M*N)) clock producing a 10-bit output based on the early/late signal. Out of these 10 bits, the 3 least significant bits are used by a sigma-delta ($\Sigma\Delta$) sampled at 1/M of the output clock (CLK_{TX}) frequency to produce a bit-stream. The sigma delta output, along with the remaining 7 bits from the loop filter output, forms an 8-bit control word for the DCO. The five most significant bits (MSBs) of the control word are used for tuning the coarse delay stage through a 5-to-32 bit decoder (COARSE [31:0]) and the three least significant bits (LSBs) control the fine tuning cell through a 3-to-8 thermometric decoder. In order to keep the hardware complexity of the loop filter low the programmable constants are chosen to be a power of 2. Multiplication/division operations are performed by left/right shifting of the bits based on the value of K_I.

3.2.1 Bang-Bang Phase Frequency Detector

A digital phase detector can be implemented in many ways, such as a XOR gate or a J-K flip flop where the duty cycle of the output indicates the phase difference between the two signals being compared. These phase detectors can track the phase error only when the error is confined within a very small range [5]. This limitation can be overcome by using a phase frequency detector (PFD). A low pass filter is required to be used with the previously mentioned phase detectors to determine the DC content of the output.

A bang-bang phase and frequency detector (BBPFD) is a special case where the phase difference between its input signals is quantized by a single bit resolution. In this DPPL design, a BBPFD similar to [35] has been used and is shown in Figure 3-3. In this implementation, a conventional PFD is followed by a sampling flip flop. The UP signal

goes high whenever F_{REF} arrives and the DOWN signal goes high at the rising edge of the F_{DIV} signal. By sampling the UP signal with the DOWN signal, the sign of the error is determined. Thus a '1' output specifies that the divided down clock is lagging the reference signal and DCO frequency needs to be increased. The output (E/L) remains either high or low for the entire period of the divided down clock. The output signal does not have a 2π periodicity as it provides just the direction of error corresponding to all phase differences at the input and because of this, the transition dynamics are very smooth [10].

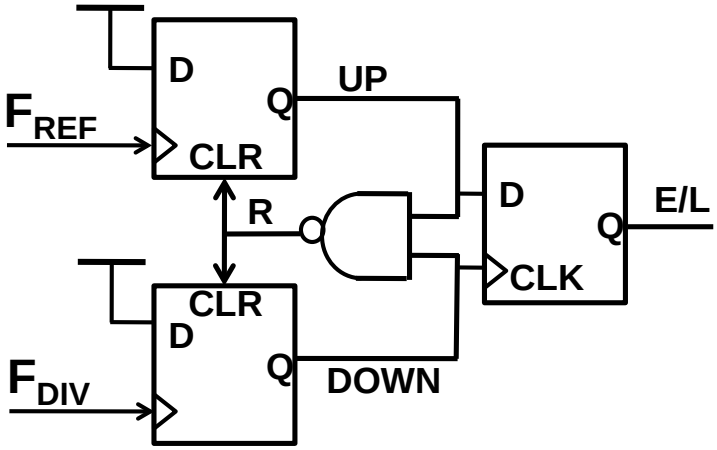


Figure 3-3. Bang-Bang PFD

3.2.2 Digital Loop Filter

A digital loop shown in Figure 3-4, with programmable integral and proportional path constants, has been used in this design. It operates at the divided down clock frequency and while in the locked state, it computes the control word every reference clock cycle. Based on the PFD output (E/L) the value stored in a 13-bit accumulator is incremented or decremented on each rising edge of the clock, followed by a multiplication by the integral path constant (K_I). In order to keep the implementation simple, K_I is chosen to be a power of 2 and multiplication is performed by simply shifting

the bits of the accumulator which generates a 10-bit result. The proportional path constant (K_P) is directly added to this result and a 10-bit control word (CW) is obtained after checking for overflows. The values of K_P and K_I affects the closed loop characteristics of the entire DPLL and a root locus based analysis approach is described in [16] and [10]. K_P affects the damping factor and K_I affects the bandwidth. A larger value of K_I also helps in fast frequency acquisition in the intial phase when the PLL is unlocked but results in a longer phase capture time [36]. As discussed earlier, a higher damping factor is required to make the system more stable. However, a higher value of K_P also increases the jitter in the system. This is due to the control word changing by a factor of ($2*K_P$ +1) whenever the PFD output toggles. A higher value of K_P/K_I is required to meet the stability criteria described by equation 2-14. In the present design, K_P and K_I are both programmable and their ratio can assume a maximum value of (7/0.125=28) corresponding to different system requirements.

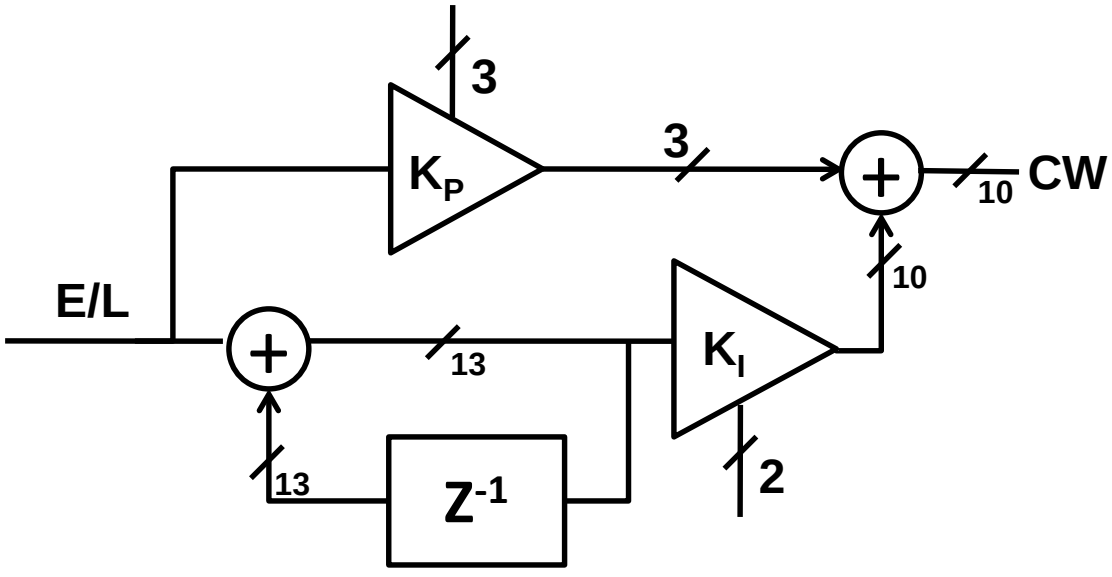


Figure 3-4. Digital loop filter

3.2.3 Sigma Delta Modulator

A first order sigma delta modulator shown in Figure 3-5 has been used to obtain an increased frequency resolution for the DPLL. It operates at a higher frequency than the loop filter and oversamples the loop filter output by a factor of M. The 3 LSBs from the 10-bit control word output of the loop filter (CW) are added to the previous value of the accumulator and the generated carry out bit is supplied as the output (SD_OUT). The sigma delta also has a high frequency noise shaping transfer function that shifts the phase noise toward higher frequencies; the noise is ultimately filtered out because of the low pass phase response of the PLL [10].

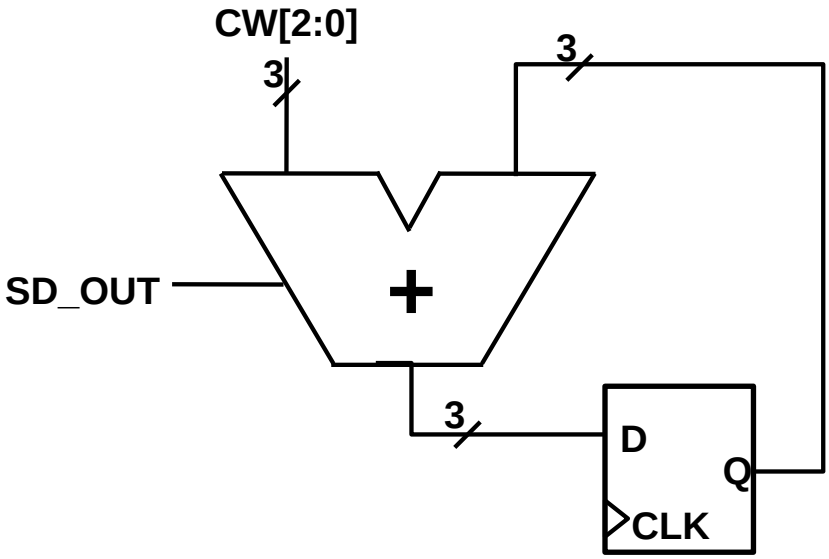


Figure 3-5. Sigma delta modulator

3.2.4 Digitally Controlled Oscillator

As discussed in section 2.2.3, a ring oscillator topology consists of an odd number of inverters are connected in a feedback loop and the oscillation frequency (equation 3-1) is determined by the delay of each stage (τ). In order to have a low oscillator, frequency either a large number of stages has to be used or the delay of each stage has to be increased substantially. A ring oscillator based DCO topology with tunable

coarse and fine delay stages, shown in Figure 3-6, has been implemented to work at very low supply voltages. By operating the inverters in the sub-threshold region, the delay of each stage increases dramatically. Further, connecting the outputs of all the coarse delay stages together increases the output capacitance of the coarse delay stage.

$$f_{osc} = \frac{1}{2N\tau} \tag{3-1}$$

The coarse tuning stage is implemented as a 32-to-1 delay select path architecture with tri-state buffers acting as selection switches. The shortest coarse delay path consists of 3 inverters while the longest path consists of 65 inverters. The five most significant bits of the control word are used for tuning the coarse delay stage through a 5-to-32 bit decoder (COARSE[31:0]). A variable number of inverters have been used for coarse delay selection in [37] and [11]. However, the frequency resolution of the coarse delay stage alone is not sufficient and a fine delay stage is required to obtain an increased resolution. The fine tuning stage has tri-state buffers connected in parallel with inverters that are activated by an 8-bit thermometric code (FINE [7:0]), based on the remaining 3-bits of the control word. The shunted tri-states control the current drive strength at each node and determine the delay in the loop. The fine delay stage covers one coarse-tuning step to obtain a monotonically rising frequency response, failure to ensure this could lead to an unstable PLL [9]. The 32 coarse delay steps and 8 fine delay steps together allow the DCO to have the capability of generating 256 different frequencies. Each course delay stage adds a delay of approximately 28ns, while each tri-state buffer in the fine delay stage changes the delay by about 3ns.

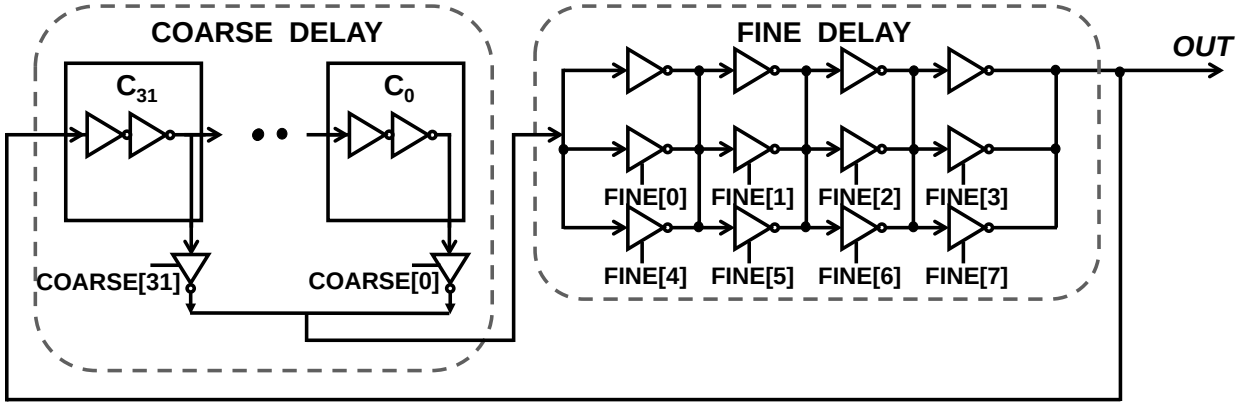


Figure 3-6. Digitally controlled oscillator

The simulated DCO response is shown in Figure 3-7 for the TT corner with a supply voltage of 260 mV. As can be seen, the DCO frequency changes linearly for lower values of the control word but the response becomes non-linear for higher values of the control word. The DCO frequency is also very sensitive to the supply voltage variations while operating in sub-threshold region. This problem was overcome by using a voltage regulator to produce a constant supply voltage.

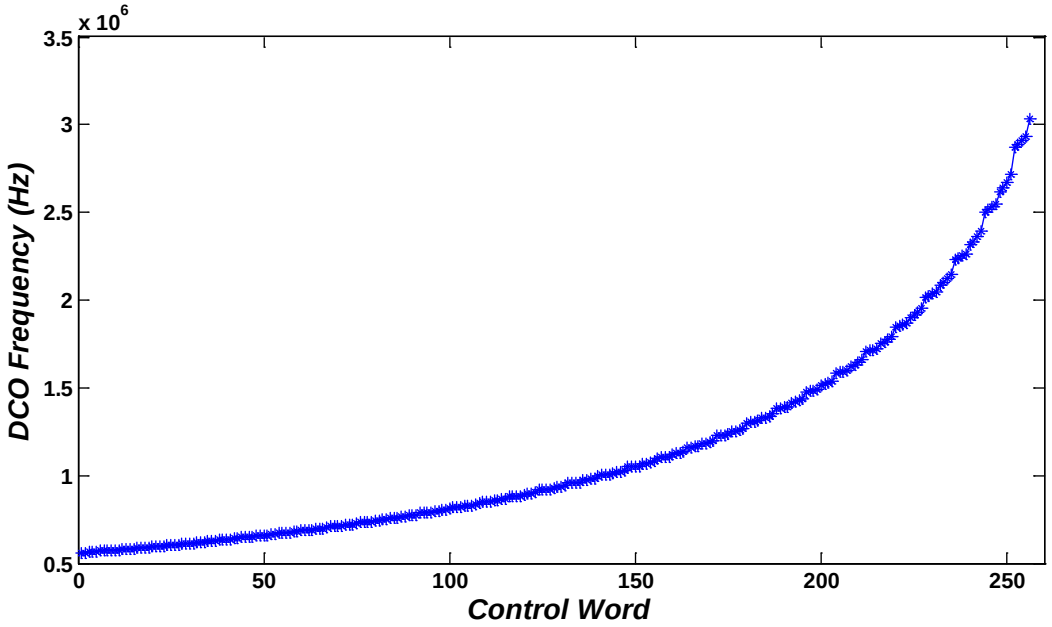


Figure 3-7. Frequency versus control word

3.3 Sizing of Digital Circuits in Sub-threshold Region

All the blocks of the DPLL described in previous sections are operated in the sub-threshold region to significantly reduce the power consumption. Also by reducing the supply voltage, leakage current due to the Drain Induce Barrier Lowering (DIBL) effect can be significantly reduced since it is directly proportional to the supply voltage. The current equations for the sub-threshold region of operation are discussed in Section 2.2.3. The focus of discussion of this section is the I_{ON} to I_{OFF} ratio which can be used as a measure of robustness for digital circuits as in [29]. I_{ON} (ON current) is the current that the MOSFET can source when it is fully turned on. I_{OFF} (OFF current) is the current that leaks through the MOSFET even when it is turned off. At high operating voltages this ratio is significantly large and ensures robustness of the circuit. But in the sub-threshold region of operation this ratio can get quite low, leading to slow charging or discharging of the output node and can cause circuit failures. Figure 3-8 shows that the I_{ON} to I_{OFF} ratio for an n-MOS transistor (130nm) can approximately have a maximum value of 4000 in the sub-threshold region.

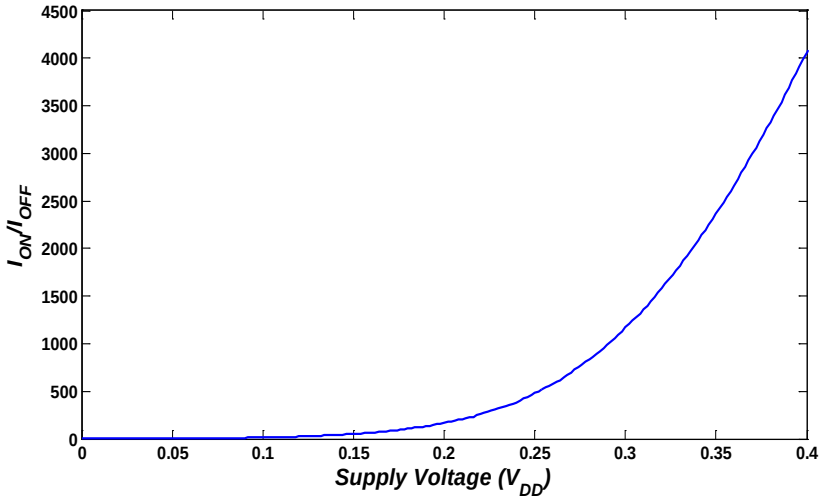


Figure 3-8. I_{ON} to I_{OFF} ratio in sub-threshold region

Thus, care has to be taken while sizing the gates to ensure functionality across all process corners. The effect of I_{ON} to I_{OFF} ratio on the sizing of the digital circuits operating in the sub-threshold region can be understood from the following discussion. In the super-threshold regime, CMOS digital circuits are usually sized such that the drive strengths of PMOS and NMOS transistors are roughly equal. A typical sizing ratio of 2:1 is often chosen, where the PMOS is sized twice the size of the NMOS. This sizing is chosen so that the PMOS and NMOS can source the same amount of current to charge or discharge the load. This is usually done to have roughly equal rise and fall delays resulting in a trip voltage of $V_{DD}/2$ and obtain a high noise margin. This sizing ratio doesn't hold well in sub-threshold regime. This is because the current doesn't follow the same quadratic profile with respect to the drain, source, gate and bulk voltages in the sub-threshold region. For proper functioning of the digital circuit, the ON complimentary NMOS and PMOS networks should be able to provide enough drive current to pull down or pull up a node when the other network is OFF within the time period of the desired frequency of operation. With process scaling, the leakage current of the transistors increases. Added to the sub-threshold current is the gate leakage current whose impact becomes more significant with every successive technology generation. This OFF state leakage current can be significantly large enough to prevent a node from being pulled up or down in the sub-threshold regime, where the I_{ON} and I_{OFF} ratios are drastically low.

For example in Figure 3-9, consider the inputs A=1 and B=1 which are applied to the NAND gate. When operated at very low voltages (in sub-threshold), the two PMOS's in parallel might supply enough leakage current to prevent the ON-state NMOS's from

pulling down the output node. The fact that the NMOS's are in series does not help this situation either because it further reduces the available current. With the added unpredictability of the PMOS's being faster than the NMOS's, the output node might always be stuck at logic '1'. Increasing the operating voltage would mitigate the problem, as the effect of the leakage current (I_{OFF}) on the overall charging/discharging behavior of the output node would be significantly reduced. This would happen because operation at higher voltages increases I_{ON}, allowing it to be much larger than I_{OFF}. In the light of the discussion above, a minimum operational voltage for different gates was found with an output swing limited to 10%-90% of the supply voltage across different process corners. It was found that for 130 nm technology, standard cells were functional for 160 mV supply with a P/N ratio of 2:2. Therefore the digital blocks are guaranteed to function by operating at 250 mV.

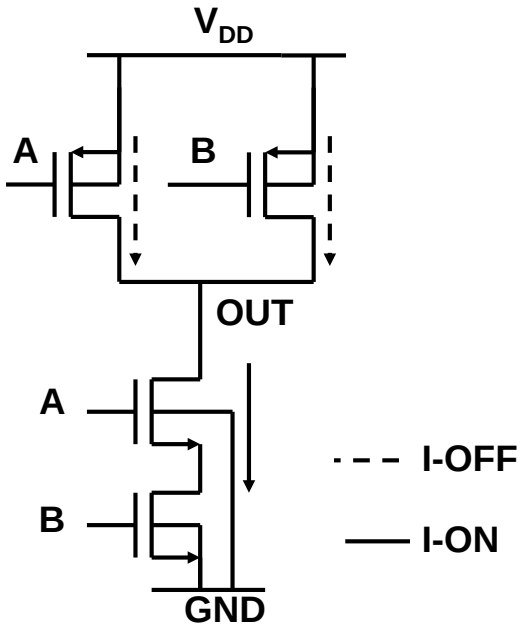


Figure 3-9. Leakage induced problems in a NAND gate operating in sub-threshold region

CHAPTER 4
SIMULATION AND MEASUREMENT RESULTS

4.1 Simulation Environment

For mixed signal systems, the designer has to be extremely careful of the interactions between the digital and analog blocks. As stated in Section 2, PLLs can have pure analog, digital or mixed signal implementations. It is extremely difficult to simulate a PLL system because of the “mixed analog-digital” nature of internal signals [38] and feedback. It needs to also be simulated for a large number of reference clock cycles to capture the transient response since a PLL shows a highly non-linear behavior prior to locking. In order to verify the correct functionality (whether it ever locks to a frequency) and evaluate other performance parameters such as timing jitter, device level simulations using circuit simulators such as SPECTRE or SPICE result in extremely impractical and long simulation time. Behavioral modeling techniques described in [39-40], and mixed signal simulation techniques described in [35] and [38] offer a promising solution to the problem of effectively verifying the functional behavior of the PLL as well as expedite the entire simulation process.

4.1.1 Behavioral Model

Behavioral modeling involves describing the function of a block with the use of concise, approximated mathematical equations or simple pseudo logic like code. There are no transistor level schematics, rather tools such as MATLAB, C, Verilog or System Verilog are used to describe the functionality of a block. It empowers the designer to quickly integrate the blocks and perform system level simulations to analyze the feasibility and try out different configurations.

Functionally equivalent Verilog codes for various sub blocks such as the PFD, loop filter, DCO and programmable divider corresponding to the bang-bang digital PLL described in Section 3.2.1 were written. The entire DPLL system was simulated in Model-Sim for verifying the locking characteristics and analyzing the effect of the loop parameters on the system stability and acquisition time. A linear model of the DCO, producing a square wave and having 256 control steps was developed. The relation between the DCO output frequency (F_{OUT}) and the control word (CW) from the digital loop filter is given by equations 4-1 and 4-2,where F_H and F_L are the highest and lowest frequencies of the DCO respectively.

$$F_{out} = F_L + K_{DCO} * CW \tag{4-1}$$

$$K_{DCO} = \frac{(F_H - F_L)}{256} \tag{4-2}$$

The effect of increasing the proportional path constant K_P can be seen in Figure 4-1. In this particular simulation setup, a reference frequency of 16 kHz was chosen with a multiplier factor of 64 to obtain a 1.024 MHz output clock. As stated earlier in section 2.1.3, increasing K_P effects the damping factor and results in a reduced frequency acquisition time, however this comes at the cost of increased jitter. Since each time the output of the PFD changes, the control word changes by a factor of $(2 \times K_P \pm K_I)$, thus higher the value of K_P, the higher the control word ripple will be. Next, to analyze the benefit of using a sigma delta modulator, it was shut off without changing any of the previous set of input parameters. As seen in Figure 4-2, the ripple in control word increases. This is because the sigma delta modulator pushes the noise towards higher

frequencies which is ultimately filtered out due to the low pass response of the PLL.

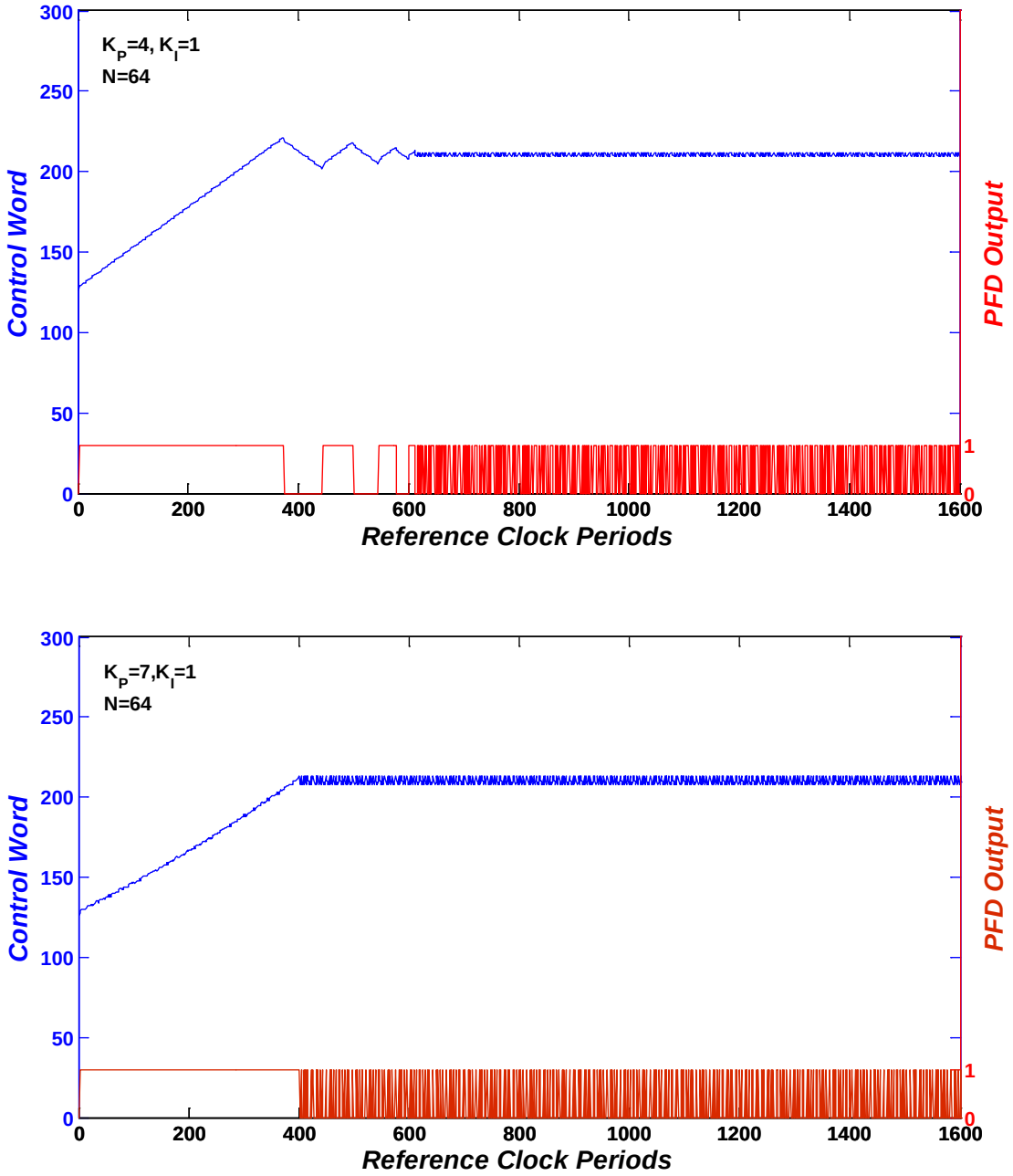


Figure 4-1. Control word versus time for two different values of K_P

To analyze the PLL response to a frequency step, a 16 kHz reference clock was applied at the input followed by a 12.5 kHz clock. As can be seen in Figure 4-3, the PLL first locks to the 16 kHz clock and the control word settles down to produce an output

frequency of 1.024 MHz. The PLL locks to the new frequency after the reference clock changes.

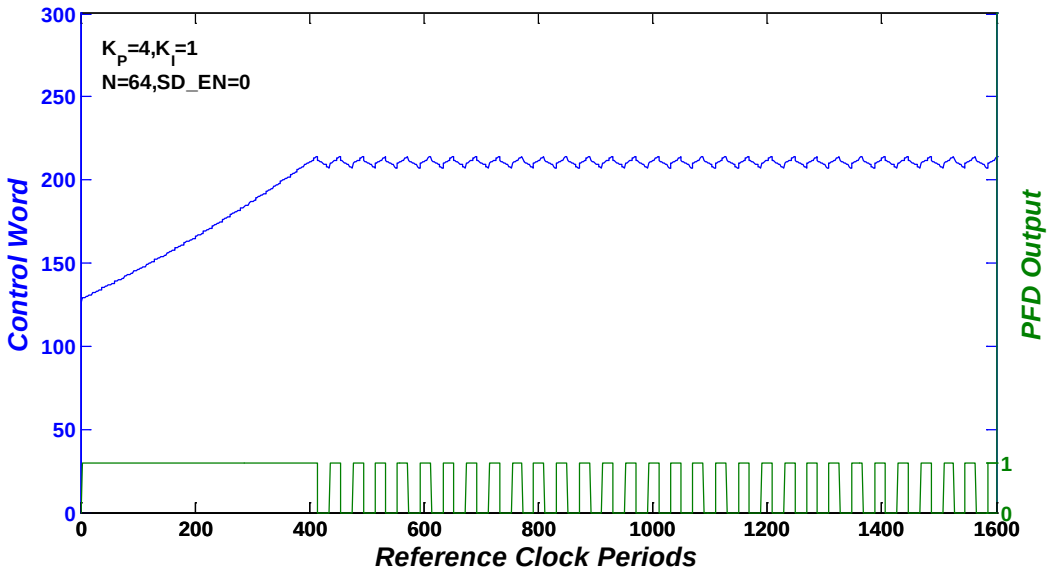


Figure 4-2. Control word versus time with the sigma delta modulator disabled

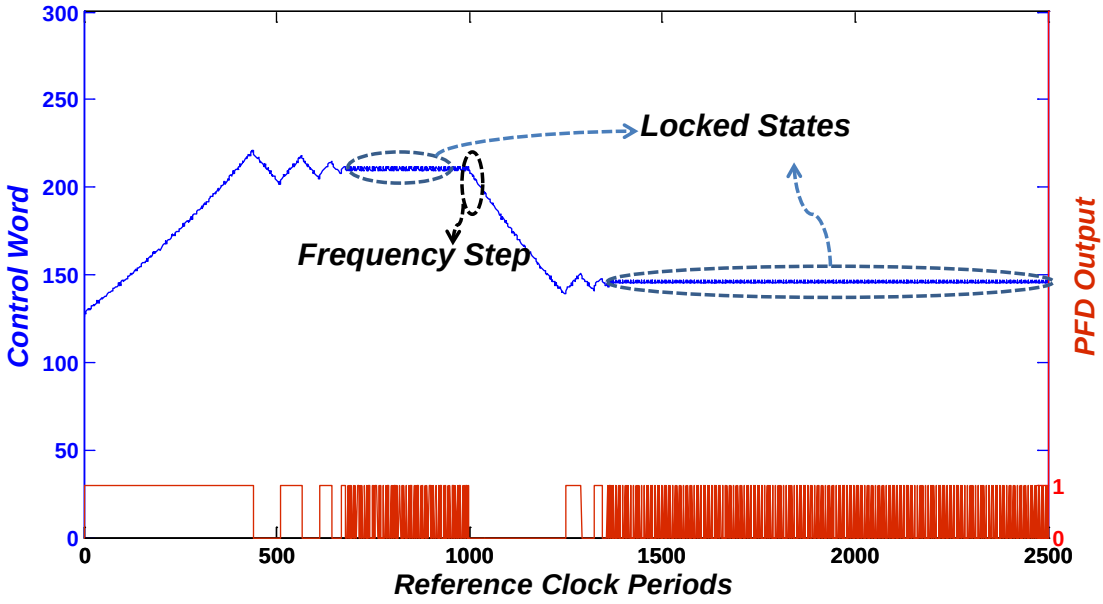


Figure 4-3. DPLL response to a frequency step

For phase step simulation, the reference frequency is initially set to 16 kHz and later a 75 degree phase shift is applied at the input. As can be seen in Figure 4-4, the

PLL is able to quickly recover from the phase step and the control word reaches its previous value again.

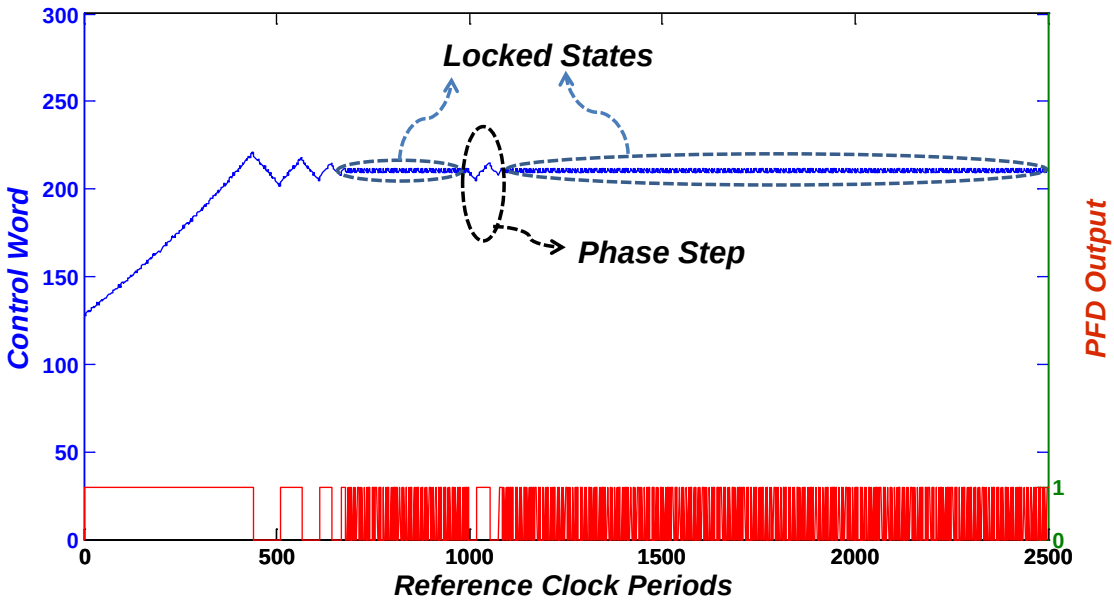


Figure 4-4. DPLL response to a phase step

4.1.2 Mixed Signal Simulations

After behavioral modeling is complete and system specs have been decided, critical blocks in the system can be replaced by their transistor level schematics for simulations. Cadence design suite comes with a large number of simulators which facilitate integration and simulation of sub-blocks implemented at different levels of abstraction. For this particular system, the Verilog model for the DCO was replaced by its transistor level counterpart operating from a 260 mV supply. In the mixed simulation mode, the blocks are connected to each other and then the hierarchical editor is invoked to notify the tool which view (abstraction level) of a particular block is to be used in the simulation. Cadence uses Spectre Verilog to simulate such a schematic which contains some blocks with only Verilog models and some with complete transistor level implementation. Next, design partitioning takes place and necessary interface elements

are placed between the transistor level and code level implementations. These interface elements behave as ADCs or DACs and it is possible to specify properties such as propagation delay, rise/fall times and input/out levels

To demonstrate a locked state in the first simulation setup, a reference frequency of 20 kHz is applied at the input and the multiplier gain is set as 64. Figure 4-5 shows that the PLL locks with the DCO frequency of 1.28 MHz. Next, a frequency step simulation is performed by first setting the reference clock to 40 kHz and later changing it to 33 kHz with the multiplier gain set as 32. As can be seen in Figure 4-6, the PLL first locks with an output frequency of 1.28 MHz and later with 1.06MHz. Although mixed signal simulations are more accurate, they take significantly more time to run than behavioral level simulations. However, the required run time and resources are far less than the complete transistor level simulations.

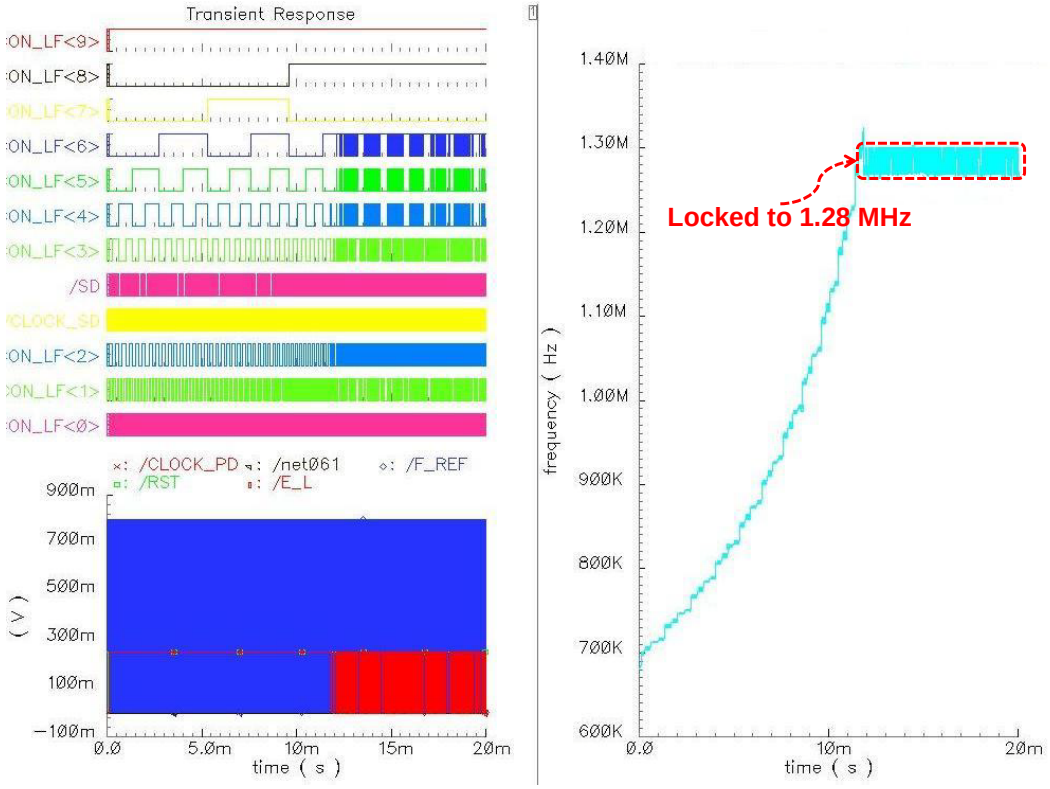


Figure 4-5. Mixed signal simulation for lock acquisition

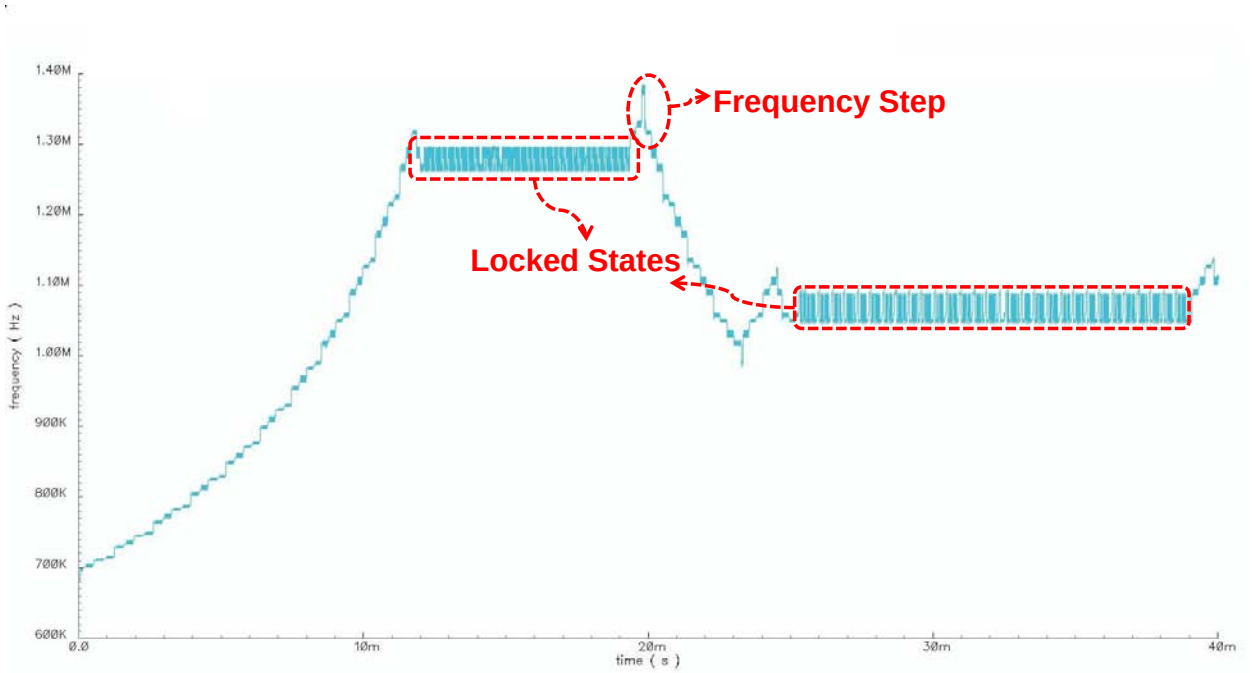


Figure 4-6. Mixed signal simulation for frequency step

4.1.3 Synthesis of Digital Blocks

After verifying the functionality of the system by using the above mentioned simulation techniques, synthesis of digital blocks is carried out using various tools. Synopsys DC compiler was used to produce an optimized netlist for the behavioral Verilog model based on the provided 130nm standard cell library information. After putting the timing constraints in place, timing slack was checked for any set up and hold time violations. The optimized netlist can also be tested using the same set of test fixtures which were incorporated with the previous behavioral simulations. Next, Cadence Encounter was used to perform automated place and route on the netlist to generate the layout for this design. The layout of the chip is shown in Figure 4-7, where the top half consists of the synthesized components and a custom DCO is integrated at the bottom.

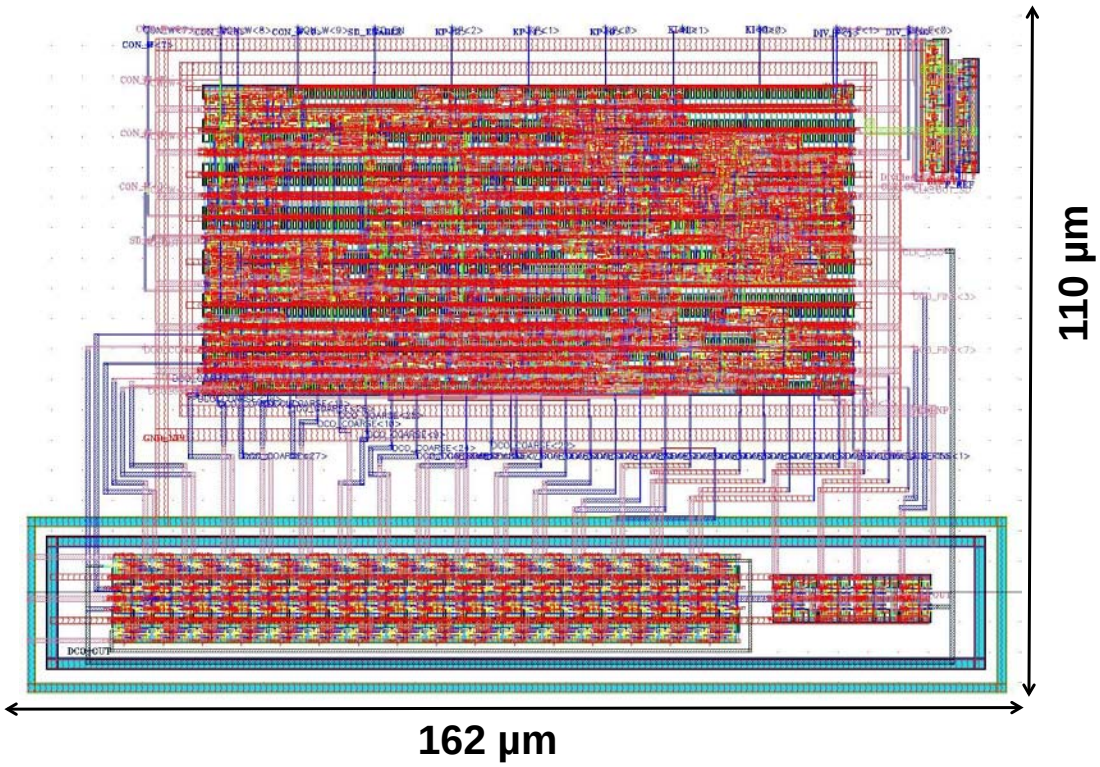


Figure 4-7. Chip layout

4.2 Measurement Results

The passive transceiver system, consisting of a RF-DC multiplier, on-chip power management circuitry, ASK demodulator (envelope detector) along with the digital PLL, was implemented using a130 nm CMOS process. A die photo of the entire chip, with dimensions of 1.67 mm by 1.27 mm, is shown in Figure 4-8. The DPLL occupies an area of 0.17 mm^2.

4.2.1 Test Measurement Setup

The packaged chip was mounted on a PCB which consists of various input and output terminals connected to an oscilloscope through SMA connectors (Figure 4-9). The necessary operating voltages for the DPLL, I/O pads and level converters were supplied through DC voltage generators. An ammeter with a 1nA resolution was connected in series with the PLLs supply voltage to measure the average power

consumption. An 8-channel ADC bus on the oscilloscope was used to observe the control word from the loop filter.

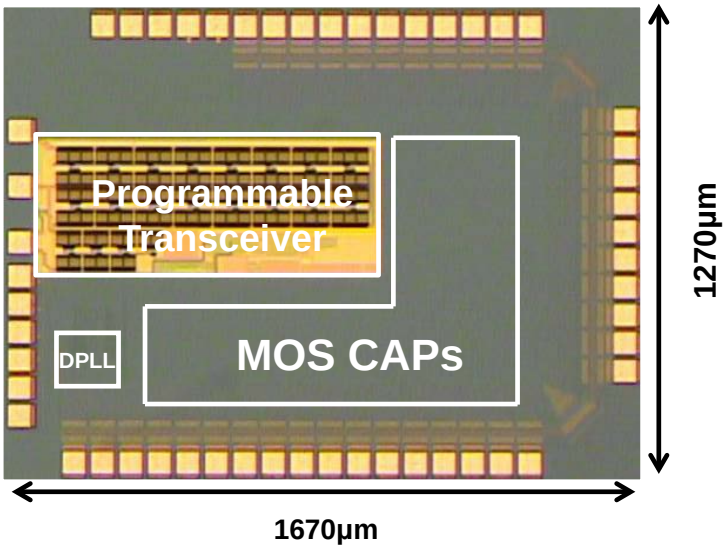


Figure 4-8. Die photo of passive transceiver with DPLL

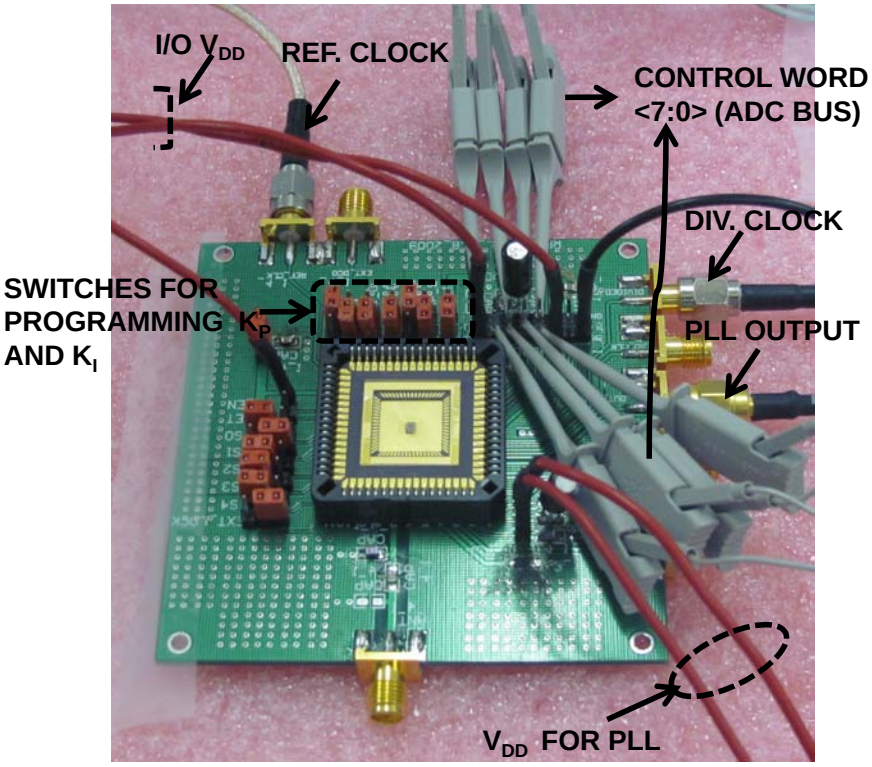


Figure 4-9. Packaged chip mounted on a PCB for testing

4.2.2 Test Cases

First, a reference frequency of 40kHz was applied at the input with the division ratio (M x N) set to 16. The value of K_P was set to 3'b001 (1) and K_I to 2'b01 (0.5). The expected DCO frequency is 640kHz in the locked state, this can be seen from the timing waveforms shown in Figure 4-10, where the rising edge of the reference clock (CLK_REF) is properly phase aligned with the rising edge of the divided clock (CLK_DIV) from the DCO. The observed control word (CW) toggles between (0XA2 and 0XA3) and the DCO frequency (CLK_OUT) is 640MHz approximately. Signal E_L is the output of the binary phase and frequency detector. All these signals are internally 250mV and have been level converted to 1.2 V before sending them to the digital output pad. The measured spectrum of the DCO signal is shown in Figure 4-11. The jitter measurements results for this set up are shown in Figure 4-12, the RMS and peak-to-peak jitter for the PLL output are 84.44ns and 518.18ns respectively while consuming 100nW of power at a supply voltage of 250mV.

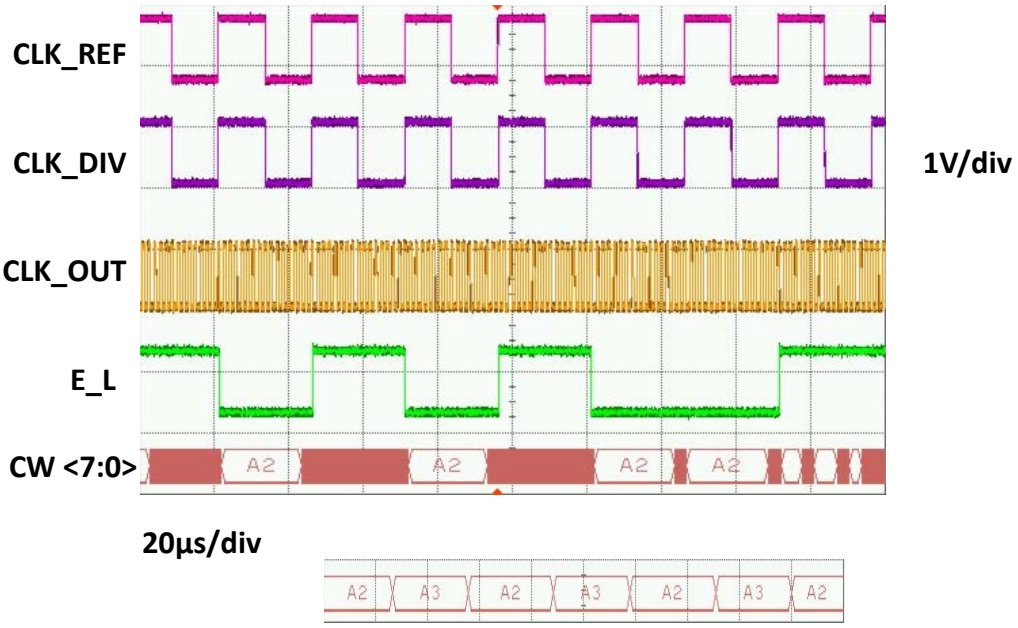


Figure 4-10. Measured waveforms for reference frequency of 40kHz and multiplier ratio set to 16

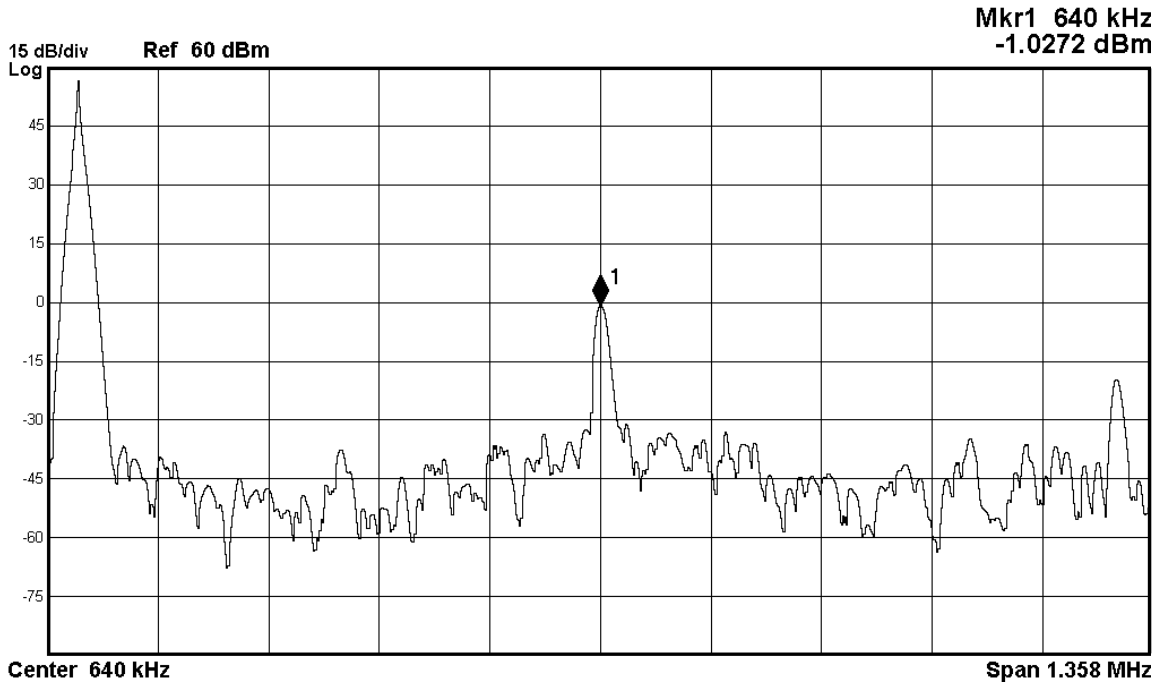


Figure 4-11. Spectrum of PLL output with oscillation frequency of 640kHz

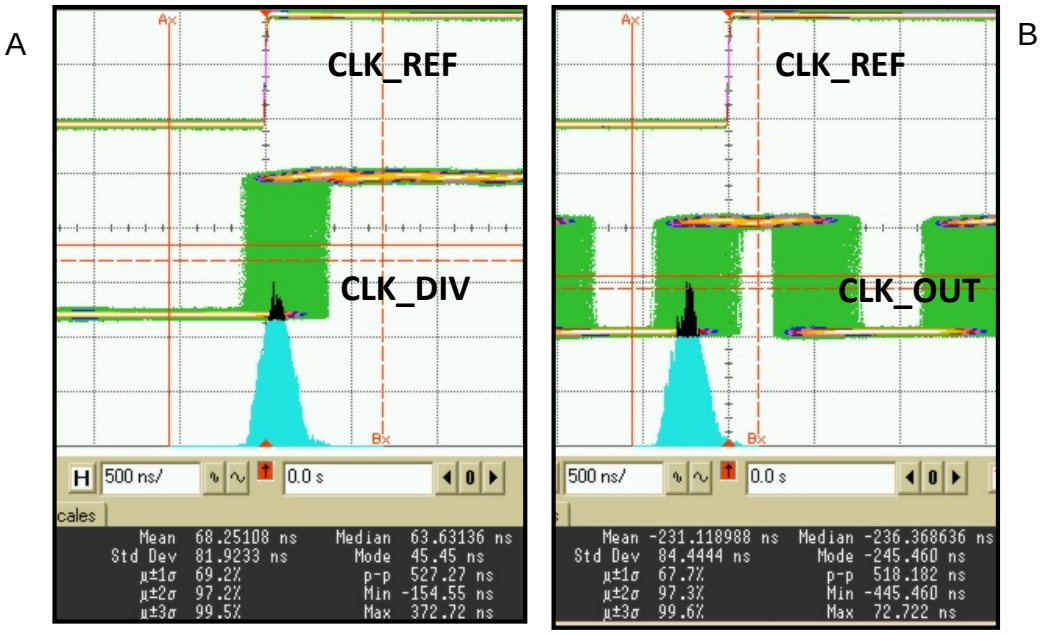


Figure 4-12. Jitter histrograms for 40kHz reference clock A) Divided clock B) PLL output clock

Next, the input frequency was changed to 20kHz without changing the rest of the input parameters such as the supply voltage, multiplier ratio, K_P and K_I values. The expected PLL output frequency is 320kHz. The measured spectrum of the PLL output

signal shown in Figure 4-13 confirms that the PLL locks with the DCO frequency fixed at 321kHz.

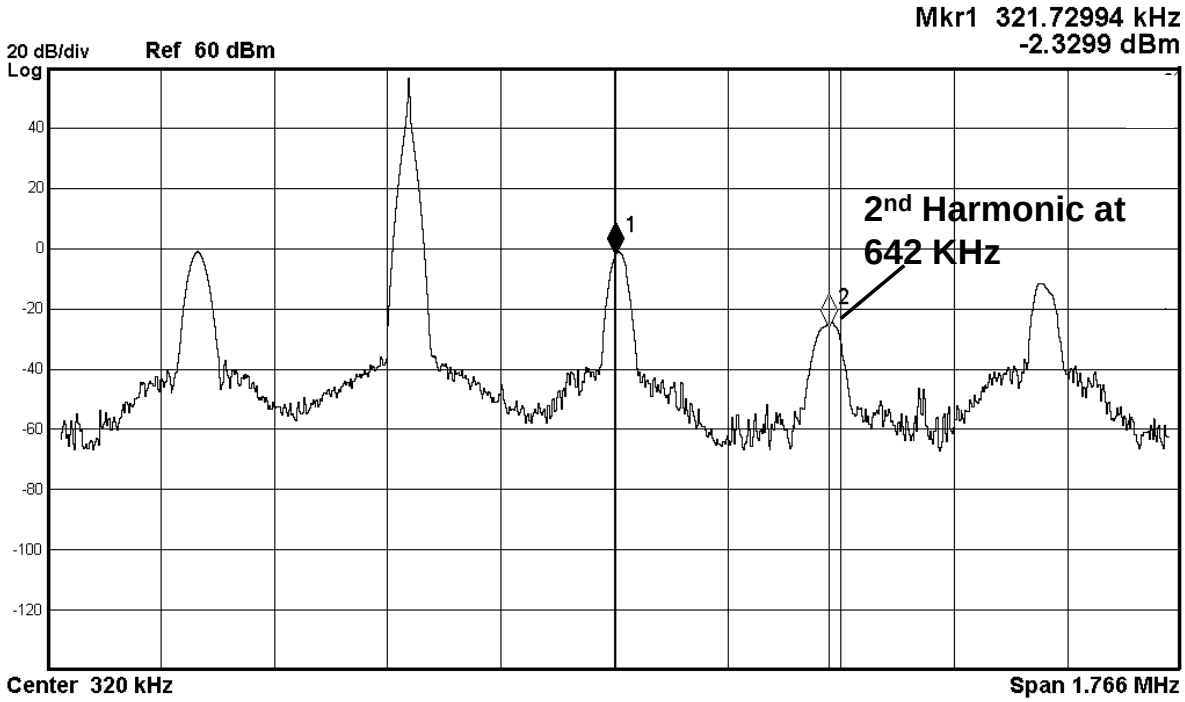
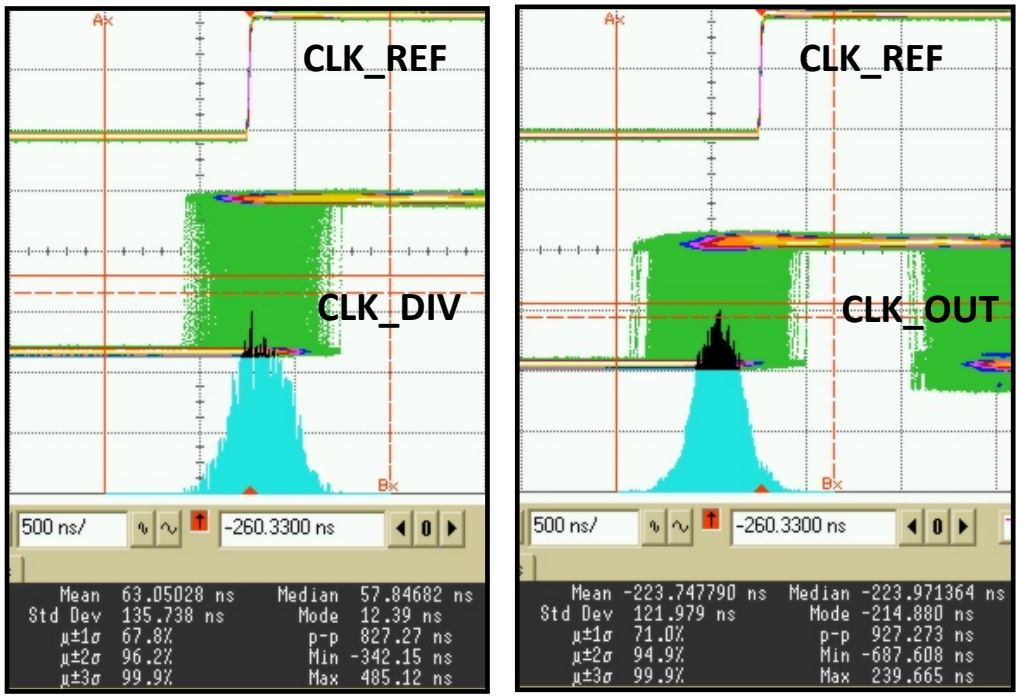


Figure 4-13. Spectrum of PLL output with oscillation frequency of 321kHz

A



B

Figure 4-14. Jitter histrograms for 20kHz reference clock A) Divided clock B) PLL output clock

The jitter measurements results for this set up are shown in Figure 4-14. The RMS and peak-to peak jitter for the PLL output frequency of 320 kHz approximately are 122ns and 927.23ns respectively. It can be seen here that jitter increases with decrease in the oscillation frequency.

Next, the control word of the DCO was fixed at 126 by keeping the RESET signal low and the supply voltage was varied. The oscillator frequency corresponding to this control word increases with each successive supply voltage step. In Section 2.2.3 the expressions for the variance of timing jitter for a ring oscillator operating in the sub-threshold region were derived. The standard deviation of the timing jitter can be calculated by substituting $T=300^0K$ and $k=1.38 \times 10^{-23}\ JK^{-1}$ and taking the square root of equation 2-36 The measurement results for the timing jitter are compared against the expected result in Table 4-1.

Table 4-1 Comparison of theoretical and measurement results for ring oscillator

Supply Voltage (mV)	Oscillation Frequency (f_0)	Power Consumption	σ_{T0} (Theoretical))	σ_{T0} (Measured)
150	46.28kHz	16.5 nW	6.48ns	725.36 ns
200	149kHz	32 nW	2.89ns	210 ns
250	453.58kHz	75 nW	1.18ns	42.57 ns
300	1.3MHz	225 nW	0.43ns	27 ns
350	3.7MHz	784 nW	15ps	12 ns
400	6.47MHz	1.7 µW	8.9ps	3.44 ns
450	11.52MHz	3.73 µW	4.3ps	2 ns
500	19.57MHz	7.88 µW	2.38ps	1.46ns

We can see that the measured standard deviation of the timing jitter is much higher compared to the expected value. This is because this model only considers the noise due to the output resistance at each node and the effect of other noise sources such as the power supply voltage noise and substrate noise has not been accounted for. The level converter and the digital output pad buffer in the signal path also

contribute to the noise component. As predicted by the model the timing jitter reduces with an increase in the supply voltage and oscillation frequency. The measurement results for peak-to-peak jitter at different supply voltages are shown in Figure 4-16.

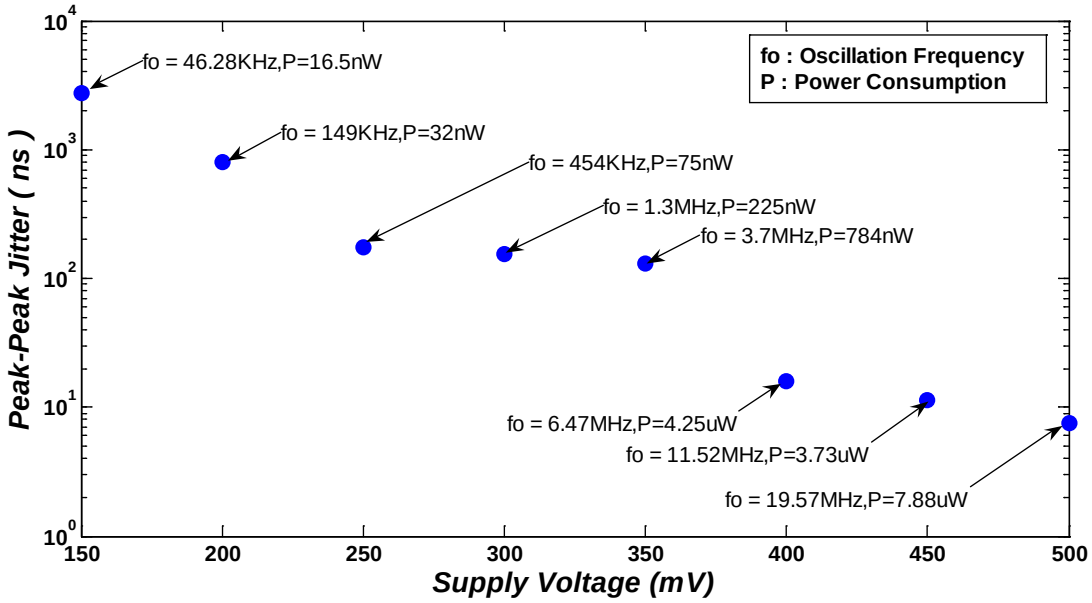


Figure 4-15. Peak to peak jitter for different supply voltages and oscillation frequencies

The change in the oscillation frequency at each voltage step can be understood as follow. The oscillation frequency for a ring oscillator is roughly determined by equation 4-3, where V_{DD} is the supply voltage and I is the ON current (equation 2-22) as explained in Section 2.2.3. The ratio of the frequencies corresponding to two different supply voltages (V_{DD1} and V_{DD2}) should roughly be given by the relation in equation 4-4.

$$f_0 = \frac{I}{NCV_{DD}} \tag{4-3}$$

$$\frac{f_2}{f_1} = \frac{I_2}{I_1}\frac{V_{DD1}}{V_{DD2}} \tag{4-4}$$

Substituting the values of the ON current corresponding to sub-threshold region of operation equation 4-4 reduces to equation 4-5.

$$\frac{f_2}{f_1} = e^{\frac{(V_{GS2}-V_{GS1})}{nV_{th}}} \frac{V_{DD1}}{V_{DD2}} \quad (4\text{-}5)$$

Since $V_{GS} = V_{DD}$ here, relationship between the two frequencies is given by equation 4-6, where n~1.5 and V_{th}~26mV.

$$\frac{f_2}{f_1} = e^{\frac{(V_{DD2}-V_{DD1})}{nV_{th}}} \frac{V_{DD1}}{V_{DD2}} \quad (4\text{-}6)$$

Thus, when the supply voltage changes from 200mV to 250mV the oscillation frequency should change by a factor of 2.9. As can be seen from Figure 4-15 that indeed the oscillation frequency changes by a factor 3.

To determine the locking range of the PLL, the reference frequency was swept for different supply voltages. The division ratio was fixed at 32 and the value of K_P and K_I were fixed at 3'b001 and 2'b00 respectively. For the typical-typical (TT) and slow-slow (SS) design corners, the measurement results are shown in Figure 4-16 (A) and (B) respectively. We can see that at 250mV supply voltage, the tuning range of the PLL is from 310kHz to 1.5MHz and the power consumption ranges from 62.5nW to 185nW. The highest supply voltage at which the PLL is functional is 500mV, after which the oscillator stops working. This is because at this voltage, the p-MOS becomes too strong and the output node gets stuck at logical '1' and is not able to discharge through the n-MOS.

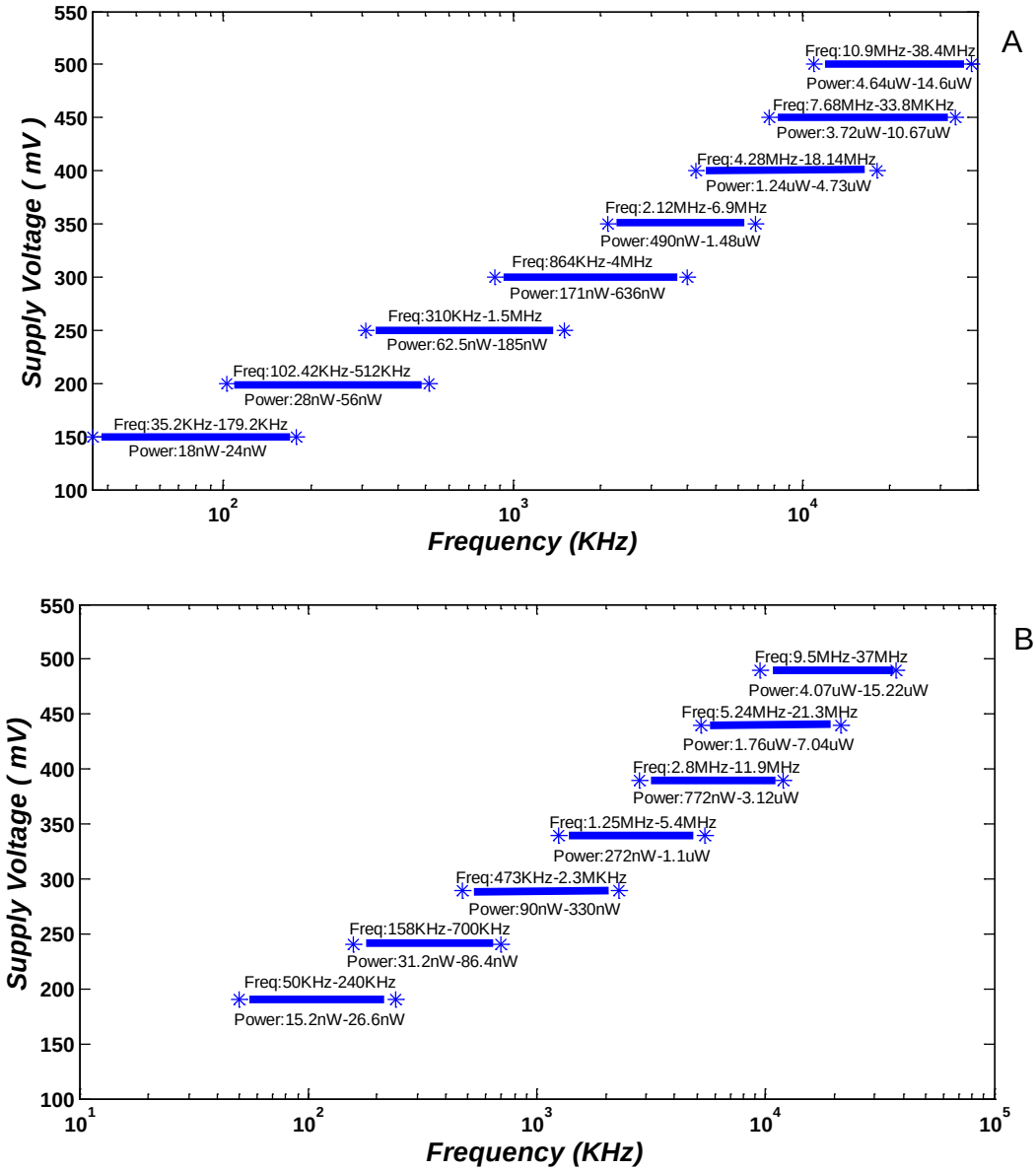


Figure 4-16. PLL lock range and power consumption at different supply voltages A) typical-typical TT design corner B) slow-slow SS design corner

CHAPTER 5
CONCLUSIONS

Miniature embedded systems used in various biomedical applications have very stringent power, size and cost constraints. They are powered by a wireless RF signal which can also contain additional information such as the reference clock. Due to the limited power available and DC voltage fluctuations, designing a clock generator is extremely challenging. In this thesis, a low-power on-chip clock generator was proposed that can provide a 385kHz to 1.54MHz clock at 260mV for digital baseband processing blocks and a backscattering modulator. The clock generator consumes ~200nW and is based on a sub-threshold DPLL which synchronizes the on-chip clock to an externally controlled low-frequency ASK signal that modulates the incident RF carrier. A single ended ring oscillator has been utilized in this DPLL design mainly because of the low area and power overhead.

There are several benefits of using the proposed clock generator. It enables the frequency tuning over a large range of frequencies. By using the DPLL as a frequency multiplier simultaneous communication with more than one peer can take place as each one can be programmed to work at different frequencies. While the area overhead is negligible, a relatively stable clock can be obtained in a cost effective way. The Verilog model of the DPLL can be easily ported to other technologies. Most importantly, a high system efficiency is achieved by operating the digital components of the DPLL in the sub-threshold region. Because of low voltage headroom, the static power dissipation of digital circuits is decreased considerably as it is exponentially dependant on the VDS of the transistors. The expressions derived in Section 2.2.3 can be used for designing a sub-threshold ring oscillator to meet the phase noise specifications of a design.

APPENDIX A
PHASE NOISE SIMULATION IN CADENCE

The phase noise simulations were performed by performing the following steps which are described in the Cadence help documents. Both PSS and PNOISE analyses should be chosen to simulate phase noise in Cadence.

The steps for PSS (periodic steady state) analysis are described as follows.

- Perform the transient simulation and determine the frequency of oscillation and the time after which the frequency stabilizes.
- In the analog design environment window chose the analysis type as “pss”.
- Set “Beat Frequency ” as the oscillation frequency obtained from transient simulations
- Set “Output harmonics” as “Number of harmonics” and type in a number between 3 -5.
- Choose “Accuracy Defaults” as either conservative or moderate.
- Put a sufficiently large value in the “Additional Time for Stabilization” textbox.
- The “Save Initial Transient Results” tab can be left blank.
- Click on the check box to enable the “Oscillator” tab and select the output node from the schematic. The reference node should be set as ground.
- The “Sweep” checkbox can be left blank
- Click on the “Enabled” checkbox.

Once this is done, the next step is to complete the set up for the “pnoise” simulation for which the following steps need to be performed.

- In the analog design environment window chose the analysis type as “pnoise”.
- Select “Sweep Type” as “relative” and “Relative Harmonic as 1.
- Specify the frequency offset range for which the phase noise has to be determined.
- Select “Sweep Type” as automatic.

- Select the number of “Sidebands” between 3 to 5.
- Select “Output” as voltage and select the output node from the schematic.
- Select ground as the negative output node.
- Select “Input Source” as none and select sources in the “Noise Type” tab.
- Activate the “Enabled” checkbox.

After completing all the above mentioned steps, click the “netlist and run” button from the analog design environment window. After the simulation is complete go to the results tab and select “Main Form”. Choose “pnoise” in the “Analysis” section and select “Phase Noise” as the function. Click the “Plot” button. The phase noise plot should pop up.

LIST OF REFERENCES

[1] K. Choe, O. D. Bernal, D. Nuttman and Minkyu Je, "A precision relaxation oscillator with a self-clocked offset-cancellation scheme for implantable biomedical SoCs," in Solid-State Circuits Conference - Digest of Technical Papers, 2009, pp. 402-403,403a.

[2] W. Liu, K. Vichienchom, M. Clements, S. C. DeMarco, C. Hughes, E. McGucken, M. S. Humayun, E. De Juan, J. D. Weiland and R. Greenberg, "A neuro-stimulus chip with telemetry unit for retinal prosthetic device," *IEEE Journal of Solid-State Circuits,* vol. 35, pp. 1487-1497, 2000.

[3] T. B. Tang, S. Smith, B. W. Flynn, J. T. M. Stevenson, A. M. Gundlach, H. M. Reekie, A. F. Murray, D. Renshaw, B. Dhillon, A. Ohtori, Y. Inoue, J. G. Terry and A. J. Walton, "Implementation of wireless power transfer and communications for an implantable ocular drug delivery system," *Nanobiotechnology, IET,* vol. 2, pp. 72-79, 2008.

[4] Meng-Lin Hsia, Yu-Sheng Tsai and O. T.Chen, "An UHF passive RFID transponder using A low-power clock generator without passive components," in *IEEE International Midwest Symposium on Circuits and Systems,* 2006*,* pp. 11-15.

[5] R. E. Best, *Phase-Locked Loops: Design, Simulation and Applications.* New York: McGraw-Hill, 2007.

[6] B. Razavi, *Design of Analog CMOS Integrated Circuits.* McGraw Hill Higher Education, 2003.

[7] F. Gardner, "Charge-Pump Phase-Lock Loops," *IEEE Transactions on Communications,* vol. 28, pp. 1849-1858, 1980.

[8] F. M. Gardner, *Phaselock Techniques.* Hoboken, NJ: Wiley-Interscience, 2005.

[9] T. Olsson and P. Nilsson, "A digitally controlled PLL for SoC applications," *IEEE Journal of Solid-State Circuits,* vol. 39, pp. 751-760, 2004.

[10] J. A. Tierno, A. V. Rylyakov and D. J. Friedman, "A Wide Power Supply Range, Wide Tuning Range, All Static CMOS All Digital PLL in 65 nm SOI," *IEEE Journal of Solid-State Circuits,* vol. 43, pp. 42-51, 2008.

[11] Duo Sheng, Ching-Che Chung and Chen-Yi Lee, "A fast-lock-in ADPLL with high-resolution and low-power DCO for SoC applications," in *IEEE Asia Pacific Conference on Circuits and Systems,* 2006, pp. 105-108.

[12] R. B. Staszewski, J. L. Wallberg, S. Rezeq, Chih-Ming Hung, O. E. Eliezer, S. K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, Meng-Chang Lee, P. Cruise, M. Entezari, K. Muhammad and D. Leipold, "All-digital PLL and transmitter for mobile phones," *IEEE Journal of Solid-State Circuits,* vol. 40, pp. 2469-2482, 2005.

[13] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg and P. T. Balsara, "Time-to-digital converter for RF frequency synthesis in 90 nm CMOS," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2005,* pp. 473-476.

[14] J. P. Hein and J. W. Scott, "z-domain model for discrete-time PLL's," *IEEE Transactions on Circuits and Systems,* vol. 35, pp. 1393-1400, 1988.

[15] V. Kratyuk, P. K. Hanumolu, Un-Ku Moon and K. Mayaram, "A Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-Loop Analogy," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 54, pp. 247-251, 2007.

[16] A. M. Fahim, "A compact, low-power low-jitter digital PLL," in *Proceedings of the 29th European Solid-State Circuits Conference,* 2003*,* pp. 101-104.

[17] Yehui Sun and Hui Wang, "Analysis of digital bang-bang clock and data recovery for multi-gigabit/s serial transceivers," in *Custom Integrated Circuits Conference,* 2009, pp. 343-346.

[18] N. Da Dalt, "A design-oriented study of the nonlinear dynamics of digital bang-bang PLLs," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 52, pp. 21-31, 2005.

[19] L. Lincoln, K. Leung and H. C. Luong, "A 7-μW clock generator in 0.18-μm CMOS for passive UHF RFID EPC G2 tags," in *33rd European Solid State Circuits Conference,* 2007, pp. 412-415.

[20] Chi Fat Chan, Weiwei Shi, Kong-Pang Pun, Lai Kan Leung, Ka Nang Leung and Chiu-Sing Choy, "A low-power signal processing front-end and decoder for UHF passive RFID transponders," in *IEEE International Symposium on Circuits and Systems,* 2009, pp. 1581-1584.

[21] R. Barnett and Jin Liu, "A 0.8V 1.52MHz MSVC relaxation oscillator with inverted mirror feedback reference for UHF RFID," in *Custom Integrated Circuits Conference,* 2006, pp. 769-772.

[22] Jong-Wook Lee and Bomson Lee, "A Long-Range UHF-Band Passive RFID Tag IC Based on High- Design Approach," *IEEE Transactions on Industrial Electronics,* vol. 56, pp. 2308-2316, 2009.

[23] F. Cilek, K. Seemann, G. Holweg and R. Weigel, "Impact of the local oscillator on baseband processing in RFID transponder," in *International Symposium on Signals, Systems and Electronics,* 2007, pp. 231-234.

[24] Chi-Fat Chan, Kong-Pang Pun, Ka-Nang Leung, Jianping Guo, Lai Kan Leung and Chiu-Sing Choy, "A Low-Power Continuously-Calibrated Clock Recovery Circuit for UHF RFID EPC Class-1 Generation-2 Transponders," *IEEE Journal of Solid-State Circuits,* vol. 45, pp. 587-599, 2010.

[25] X. Zhao, R. Chebli and M. Sawan, "A wide tuning range voltage-controlled ring oscillator dedicated to ultrasound transmitter," in *Proceedings. the 16th International Conference on Microelectronics,* 2004, pp. 313-316.

[26] Myeong-Eun Hwang and K. Roy, "ABRM: Adaptive -Ratio Modulation for Process-Tolerant Ultradynamic Voltage Scaling," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 18, pp. 281-290, 2010.

[27] A. Wang, A. P. Chandrakasan and S. V. Kosonocky, "Optimal supply and threshold scaling for subthreshold CMOS circuits," in *IEEE Computer Society Annual Symposium on VLSI Proceedings,* 2002, pp. 5-9.

[28] C. H. -. Kim, H. Soeleman and K. Roy, "Ultra-low-power DLMS adaptive filter for hearing aid applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 11, pp. 1058-1067, 2003.

[29] A. Wang and A. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," *IEEE Journal of Solid-State Circuits,* vol. 40, pp. 310-319, 2005.

[30] B. H. Calhoun, A. Wang and A. Chandrakasan, "Modeling and sizing for minimum energy operation in subthreshold circuits," *IEEE Journal of Solid-State Circuits,* vol. 40, pp. 1778-1786, 2005.

[31] A. Hajimiri, S. Limotyrakis and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-State Circuits,* vol. 34, pp. 790-804, 1999.

[32] R. Navid, T. H. Lee and R. W. Dutton, "Minimum achievable phase noise of RC oscillators," *IEEE Journal of Solid-State Circuits,* vol. 40, pp. 630-637, 2005.

[33] S. Liu, J. Kramer, G. Indiveri, T. Delbruck and R. Douglas, *Analog VLSI: Circuits and Principles* The MIT Press, 2002.

[34] A. Ashry and K. Sharaf, "Ultra low power UHF RFID tag in 0.13 µm CMOS," in *International Conference on Microelectronics,* 2007, pp. 283-286.

[35] D. Bhatia, *Digital Aided Synchronization and Mixed Signal Modeling of High Frequency Dc-Dc Converters [Electronic Resource].*Gainesville, FL: University of Florida, 2009.

[36] Jri Lee, K. S. Kundert and B. Razavi, "Analysis and modeling of bang-bang clock and data recovery circuits," *IEEE Journal of Solid-State Circuits,* vol. 39, pp. 1571-1580, 2004.

[37] Ching-Che Chung and Chen-Yi Lee, "An all-digital phase-locked loop for high-speed clock generation," *IEEE Journal of Solid-State Circuits,* vol. 38, pp. 347-351, 2003.

[38] B. A. A. Antao, F. M. El-Turky and R. H. Leonowich, "Mixed-mode simulation of phase-locked loops," in *Proceedings of the IEEE Custom Integrated Circuits Conference,* 1993, pp. 8.4.1-8.4.4.

[39] F. Herzel and M. Piz, "System-level simulation of a noisy phase-locked loop," in *European Gallium Arsenide and Other Semiconductor Application Symposium,* 2005, pp. 193-196.

[40] M. Hinz, I. Konenkamp and E. -H. Horneber, "Behavioral modeling and simulation of phase-locked loops for RF front ends," in *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems,* 2000, pp. 194-197, vol.1.

BIOGRAPHICAL SKETCH

Tanuj Aggarwal was born in 1984 in Rishikesh, India. He received his bachelor's degree in Information and Communication technology from Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT), Gandhinagar, India in 2007 and master's degree in Electrical and Computer Engineering from University of Florida, Gainesville, Florida in 2010 respectively. He worked as a Research Assistant in the Integrated Circuit Research Lab (ICR) from June 2008 to May 2010. The focus of his research was the implementation of low power digital circuits for wireless communication applications. His research interests include design and implementation of low power digital circuits, development of design flows to aid fast simulation and verification of mixed signal systems and computer architecture.