RF/MICROWAVE/MILLIMETER WAVE EMBEDDED DETECTORS

By

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TABLE OF CONTENTS

page

LIST OF TABLES

LIST OF FIGURES

Abstract of Dissertation Presented to the Graduate School
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Testing millimeter wave circuits can be a challenging undertaking. Expenditures required for vendors' test solutions at those frequencies are costly. Moreover, as vertical integration is gaining momentum, the ability to determine functionality of every layer is crucial. Circuits operating at millimeter wave frequencies are especially susceptible to process variations. Yield is significantly affected if any of the layers is not functional to specifications. To mitigate these effects, a slew of strategies need to be implemented. Process variation monitoring circuits should be included. Non-invasive Built-In-Self-Test (BIST) circuitry is necessary to enable self-repair, self-healing of mmWave circuitry. All these factors call for innovation of simple circuits capable of performing alternate RF tests. This dissertation discusses simple topologies of amplitude detectors suitable for millimeter wave BIST. The detectors can be implemented in different technologies; they occupy a small area, have low power consumption, a wide operating frequency range, negligible loading effects, and a suitable dynamic range. Detectors act as virtual probes that convert RF amplitude information into DC or low frequencies. The detectors' response is discussed over multiple operating conditions with special attention to issues relevant to BIST applications. A differential detector that measures the pure differential

component of a mixed mode signal is also presented. This detector is further enhanced to measure both components of mixed mode signals including common mode. System applications are presented to illustrate the advantages of each detector topology reported in this dissertation. Finally, this dissertation concludes with a summary and proposed future work section.

CHAPTER 1
INTRODUCTION

Challenges in High Frequency Test

The RF test engineer constantly tackles new sets of issues to keep up with technological advances. The engineer is required to develop test solutions for highly complex circuits without affecting profit margins [1]. Devices under test (DUT) become more complex as they pack more functionality into an ever shrinking form factor. For example, Multiple-Input-Multiple-Output (MIMO) technology is used in most recent standards (802.11n, WiMax, LTE). MIMO has stringent synchronization requirements throughout the entire transceiver chain. To minimize measurement related errors when testing MIMO systems, it is important to maintain accurate time and phase alignments [2]. Additionally, many system architectures are emerging by taking advantage of an abundant electronic processing power. Advanced radars emulate the mechanical rotation associated with standard radars by electronically scanning a multitude of stationary circuits. However, data extracted from the stationary circuits needs to have an accurate phase match; then, data can be post-processed to accurately resolve an image [3]. Pulse-to-pulse phase is an important specification in advanced radar systems [4]. Therefore, most modern electronic applications have strict tester specifications. Additionally, to boost the overall testing efficiency in mass production applications, the ITRS keeps increasing the goal for RF multi-site testing [5]. Multi-site testing enables parallel measurements which decreases the overall test time; however it complicates the test setup.

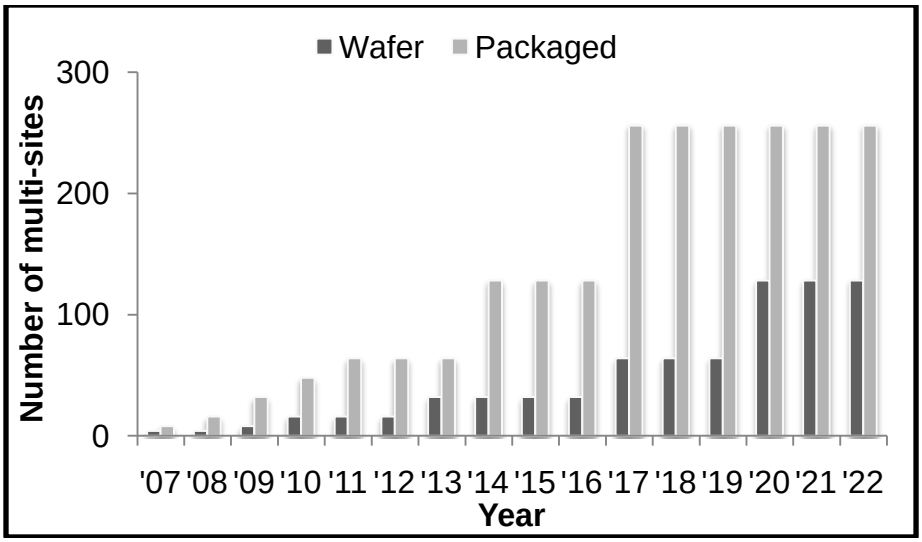


Figure 1-1. ITRS prediction of multi-site testing required for RF products

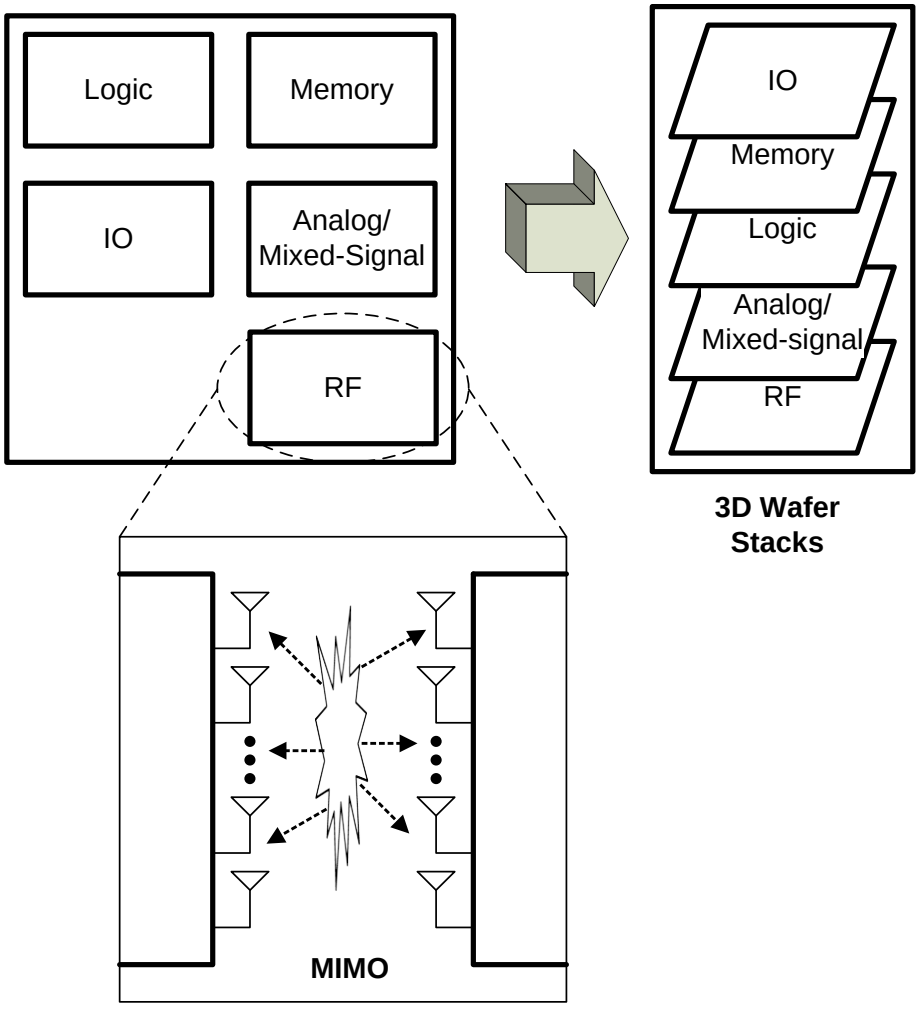


Figure 1-2. Complicated devices under test

As described above, the test engineer has to test multiple DUTs in parallel. These DUTs are further complicated because of their MIMO architecture. Also, innovative architectures demand tight specifications to enable new functionalities. These are only some of the complications associated with the DUT itself. The test engineer has to also deal with another set of problems related to the test equipments.

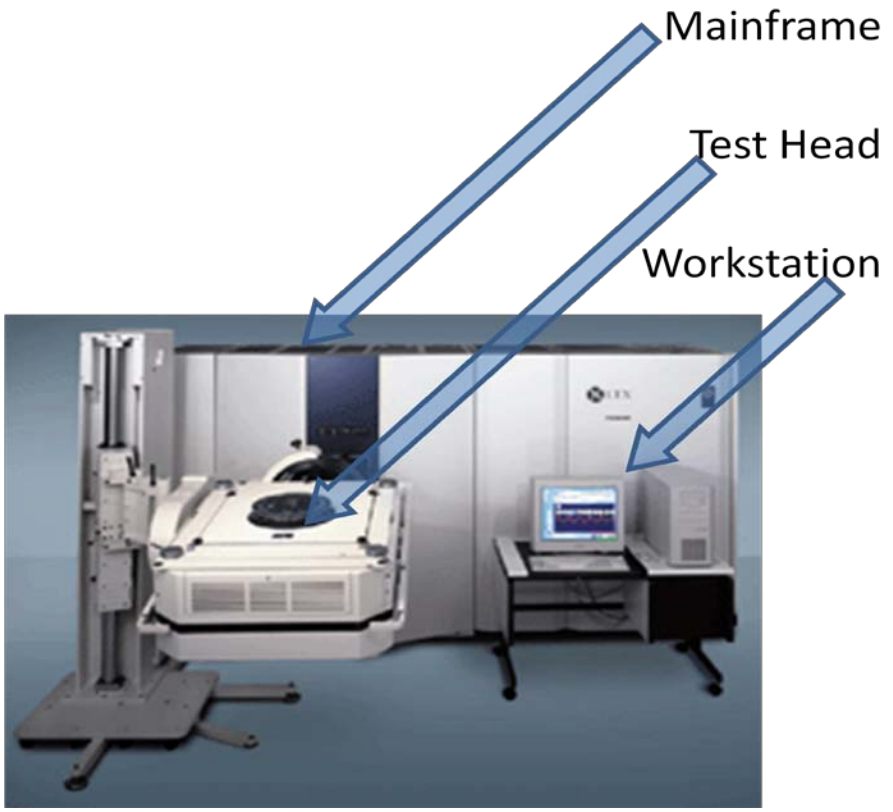


Figure 1-3. Automatic Test Equipment (ATE). Courtesy of LTX

The ITRS Test Roadmap identifies testers' inaccuracies as one of the difficult challenges facing the test industry [5]. Extensive calibration is needed to take into account errors associated with the measurement setup. Also, commercial test solutions need synchronization units to synchronize all their instruments in addition to phase-matching or phase-tracking coaxial cables to connect the DUT to the instruments. However, the longer the cables the more difficult matching becomes [3]. Also, the higher

the frequency of operation, the longer the electrical length becomes. Consequently, the cables performance becomes more sensitive to dielectric variations, bends, and temperature. Therefore, the long cables required for the conventional test solutions are more sensitive to temperature variations because of their greater thermal mass [3].

Proposed Solution

All these issues demand innovation of novel alternate test solutions. To lower testing costs, [1] moved RF test on the probe interface board. This solution uses customizable modular test circuits which effectively eliminate some of the trade-offs of generic solutions. For example, the publication [1] reports a design of a synthesizer that is customized for a GPS test applications. Whereas a generic vendor solution needs to cover a wide range of operating frequencies, this customized solution can afford to operate at a bandwidth that is only satisfactory for its targeted test application. The customized solution has better phase noise attributes because of the smaller bandwidth. Also, since this solution is easily customizable, the frequency band is easily modified by replacing its Voltage Controlled Oscillator (VCO) to cover other test applications. Up to this point, discrete components were used to achieve this. However, different approaches should be considered for mmWave frequencies. Specifications of regular printed circuit boards are no longer suitable at higher frequencies. Once circuits' size becomes comparable to few wavelengths, PCB design can become challenging [6]. Low loss, high density, good match, and low coupling are difficult to achieve with CPW or microstrip lines at mmWave frequencies [7]. The PCB designer has to balance a number of tradeoffs. For example, the designer needs to physically separate and shield the interconnect lines to minimize coupling. Conversely, the interconnect lines need to be matched to minimize amplitude and phase mismatch which in turn necessitates

close spacing. In [7], micromachining is used to leverage coaxial lines which are better suited to operate at higher frequencies. They implement micro-coaxial lines on a PCB that support pure TEM (transverse electromagnetic) propagation up to .5THz range. Therefore, miniaturization is one way to deal with issues at mmWave frequencies. Our goal is take advantage of miniaturization by designing modules for a tester-on-chip. Thus, test circuits could be embedded on the DUT when possible; and, for test applications that do not warrant any performance penalty, a hybrid solution that integrates a tester-on-chip into a tester-on-board is proposed. However, by moving the testers on chip, post fabrication customization is not easy; therefore, the proposed solution may lose a degree of freedom compared to the discrete component solution. This means that testers-on-chip may need to adopt some of the same approaches of the generic vendor solutions. [8] describes how Software Defined Radio (SDR) strategies may be adopted in designing the next generation of RF instrumentations. For example, a frequency-multiplier/differential-quadrature-generator for SDR applications, reported in [9], has attributes required for on-chip signal generation; it is tunable and occupies a small area. The circuit can be cascaded with the synthesizer described in [1] as seen in Figure 1-4 which illustrates this architecture. The synthesizer can generate a low phase noise signal with a fine frequency tuning resolution. The critical signals' paths are shortened by moving them as close to the DUT as possible. Generation of higher frequencies and differential quadrature is done on-chip to minimize errors associated with the test setup. On the measurement side, the test development engineer needs to borrow concepts from SDR topologies as well. By having a general purpose receiver front-end, a number of alternative test approaches become possible such as design of a

true synthetic instrument. Synthetic instruments implement many measurements using one test setup. For instance, an Error Vector Magnitude (EVM) measurement can characterize an entire transceiver; while a traditional transceiver test setup measures S-parameters, noise figure, compression point and a number of other specifications; with each of these requiring a different measurement setup.

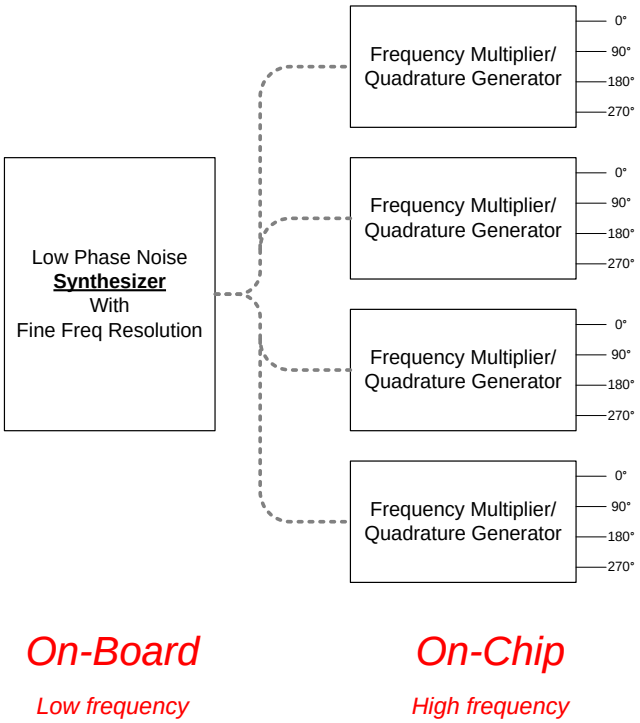


Figure 1-4. Architecture of signal generation for on-chip on-board tester for multi-sites

On another note, embedding test circuits on the DUT is also necessary nowadays. In the ever increasing world of integration in electronics, test access points are scarce. Multi-chip packaging offers increased capability at the expense of an increased complexity [10]. Currently, levels of integration reached another height with wafer stacking. 3D wafer stacking presents a new set of challenges for the test engineer. Even, expensive troubleshooting techniques such as non-contact probing (laser or thermal infrared) become virtually impossible [11]. These techniques become exponentially difficult as the number of layers in a chip increases. Therefore, non-

invasive BIST circuits can be useful to increase the number of test access points. BIST circuits can be described as virtual probes. Their role is not only limited to enabling more test capability, they also allow many alternative strategies. In applications that are prone to yield issues, BIST can facilitate self-repair and self-healing of DUTs.

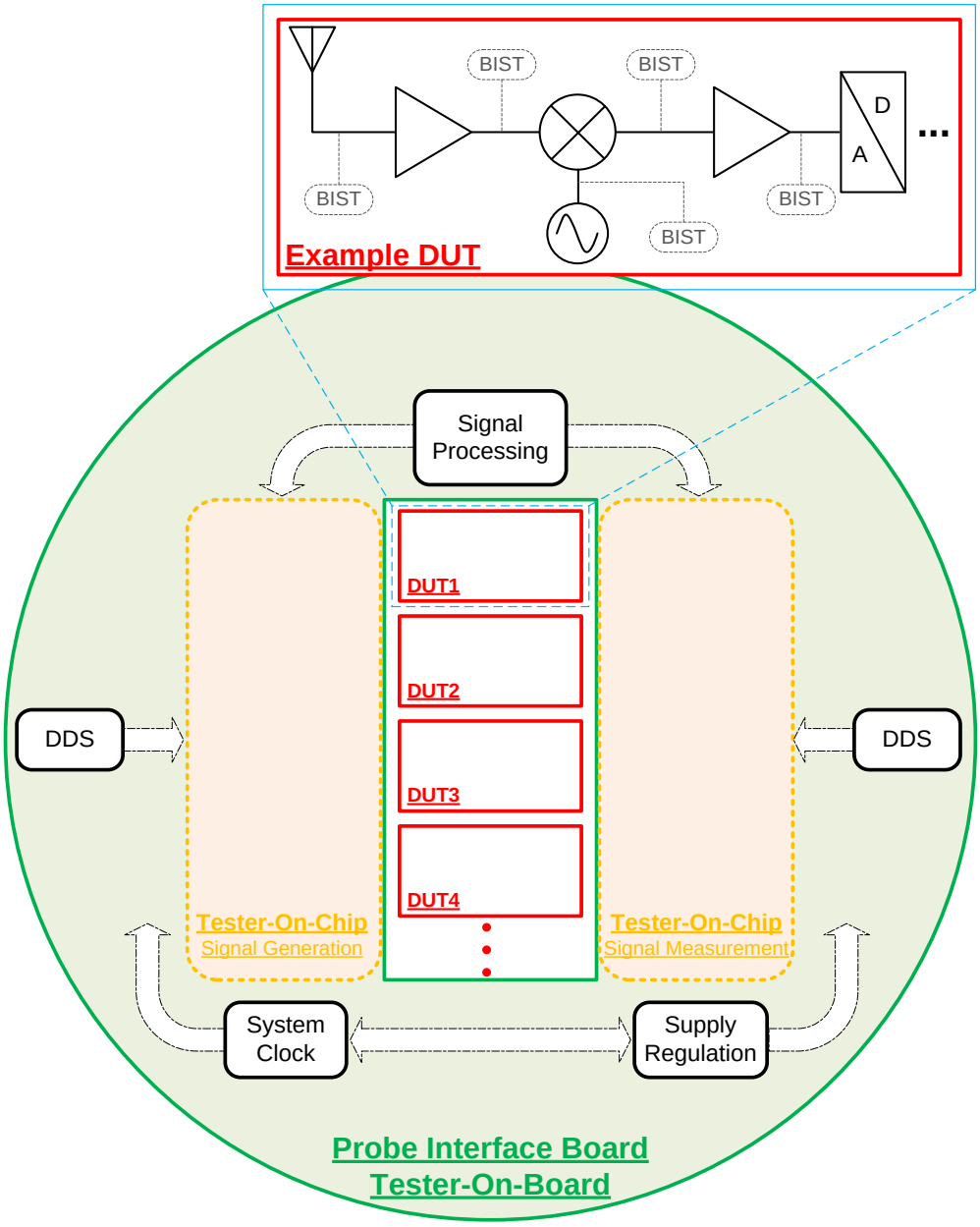


Figure 1-5. Alternate test architecture - Tester-on-chip-on-board and embedded BIST

Figure 1-5 shows the overall test architecture described above. It includes the proposed hybrid solution of on-chip-on-board testers for production test. This drawing is

a high level drawing that does not reflect the true scale. The on-chip tester should occupy a considerably smaller area. The figure also shows how BIST circuits allow access to internal nodes on the DUT. Figure 1-6 shows how a tester-on-chip can be integrated within a probe. This is a low cost solution suitable for characterization test.

Figure 1-6. Alternate test architecture - Tester-on-chip-on-probe for characterization test

As previously mentioned, current market conditions put pressure on the semiconductor industry to seek new business models. Because it's difficult to assess future market conditions, short time-to-market is essential. Lean, agile organizations trim their processes which easily facilitates their adaptation to changing market conditions. In the semiconductor industry, the development cycle isn't flexible because of the finality of the hardware product; thus, suitable lean thinking principles are limited.

However, the strategies proposed in this dissertation can be implemented to reduce capital investments and to shorten the design cycle for example. By using alternate test strategies, the overall test cost can also be lowered by decreasing test time and re-using economical resources. Additionally, unnecessary wafer re-spins can be eliminated if failures locations are detected efficiently. BIST allows insight to previously inaccessible nodes easily locating faulty circuit subcomponents. This is not the only way BIST fulfill the lean thinking methodology; BIST can be useful beyond reducing the design cycle time. Given the way semiconductor devices are shrinking (geometries), it is inevitable to adopt new approaches to deal with process variations. BIST can enable self-healing of the DUT. Easy adaptability is one of the basic premises of the lean thinking principle. It can also affect the DUT once it is deployed. So, for example, as the DUT ages or its operating conditions changes, it should be adaptable and self-repair itself. BIST circuits can monitor important metrics, therefore, allowing the DUT to adapt to its operating conditions. Widespread adoption of BIST circuits, especially RF-BIST, is usually received with some resistance. However, because of the severity of issues the semiconductor industry is set to face according to ITRS projections, many players in the industry realize that cooperative test approaches are necessary [12]. Finally, BIST is a necessity since integrated circuits are penetrating new markets that demand constant verification of functionality such as medical applications, and imaging for automotive collision avoidance and homeland security.

Organization of the Dissertation

This section provides an overview of this dissertation. The first chapter mentions the issues the test industry is facing to keep up with technological advances. It also discusses alternative test solutions and how the herein proposed work fit among those

solutions. This dissertation proposes modules for a low cost integrated test approach. This methodology combines embedding non-invasive circuits on the DUT and embedding other test circuits on a test board.

Chapter 2 is a comprehensive analysis of a MOS amplitude detector for millimeter wave BIST. The detector's response is investigated in different operating regions. A simplified RF-to-DC conversion gain equation for detection in the saturation region is derived. Two conversion modes are uncovered in the subthreshold operation region. The first mode has a linear RF-to-DC proportionality which applies only to relatively large signal levels. A new equation for small signal detection is introduced. The body effect was investigated in the saturation region and subthreshold's two modes. Detection in the triode region is also discussed.

In Chapter 3, the amplitude detector's response is characterized in detail. For instance, the circuit's RMS detection dynamic range is presented in different operating regions. The next section discusses envelope measurements when the detector is stimulated with amplitude modulated inputs instead of single-tone inputs. This is followed by a discussion of the detector's settling time. It is important to describe the important metrics that affect the settling time as it directly impacts the overall test time. A novel bandwidth equation that takes into account the detector's loading effects on the circuit under test is introduced for BIST applications. Finally, the detector's accuracy when it is subjected to environmental and process variations is discussed under different operating conditions.

Alternate simple MOSFET topologies are proposed in Chapter 4. Two topologies that minimize the crossover region in subthreshold are described. Subthreshold

detectors have a large crossover region where neither the linear nor the square law modes are accurate. In the crossover region, when the input has a varying crest factor, the detector cannot estimate the input's amplitude accurately. A topology with extended RMS detection dynamic range is introduced in this section as well. Finally, a new detector that operates in three operating regions (saturation, subthreshold, and triode) is introduced. This new detector topology is advantageous because of its flexibility; the same topology can be customized for different applications by changing its biasing region.

Chapter 5 touches on mixed mode signals. It presents a detector that measures the pure differential component of a port under test. Another topology that improves upon the differential detector is unveiled. The common mode component of a mixed mode signal can be measured with a minor modification to the previous topology.

In Chapter 6, system applications for the single ended and differential detectors are discussed. An LNA example is used to showcase the trade-offs associated with each of the single ended topologies proposed in this dissertation. Additionally, compact Six-port reflectometers topologies that measures S-parameters which require differential detectors are reported.

Chapter 7 is a summary of all the accomplishments and proposes future work.

CHAPTER 2
MOSFET AMPLITUDE DETECTOR

Introduction

Amplitude detectors that realize RF-to-DC conversion are commonly used in RF BIST. The RF input's amplitude is converted to DC through the non-linear properties of a rectifying circuit. Many amplitude detectors operate by implementing a V/I (voltage to current) conversion, then RF-to-DC conversion, and finally an I/V (current to voltage) conversion. V/I conversion circuits in previous publications limit the bandwidth to few GHz [13] [14]. For those circuits, amplification is necessary for efficient rectification. Then, RF-to-DC conversion is usually done using a half-wave rectifier [13], or using the translinear loop principle [14]. The RF-to-DC conversion is usually realized in the current domain; thus, an I/V converter is needed to convert the resulting DC current to a DC voltage.

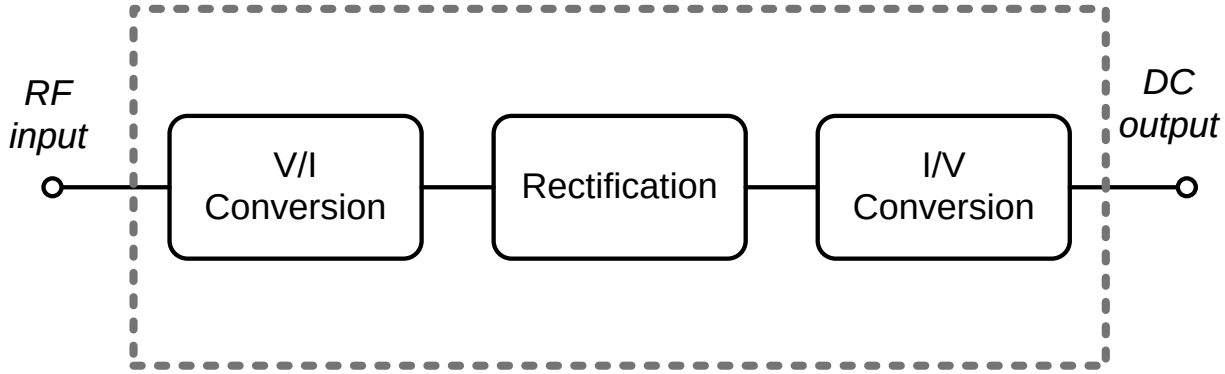


Figure 2-1. Stages in amplitude detection

There exists another class of detectors that do not require amplification before rectification, where detection is based on the non-linear properties of a single device. For instance, the popular classic diode detector belongs to this category. For BIST applications, it is important for the amplitude detector to be compatible with standard MOS processes to cover most products. This section focuses on simple detectors

based on MOS technology. The first MOS detector to the author's knowledge was designed by Vittoz in 1977 [15]. This MOS detector operates in the subthreshold region. In 1990, a patent was filed for a MOS detector based on the square-law model of the transistor [16]. In 1998, a paper from ENST Paris published two MOSFET structures [17]. The two designs used the non-linear properties of the transistor channel to obtain a DC value that is proportional to the RF input. In recent years, [18], [19], [20], and [21] reused these topologies or other variants for BIST purposes.

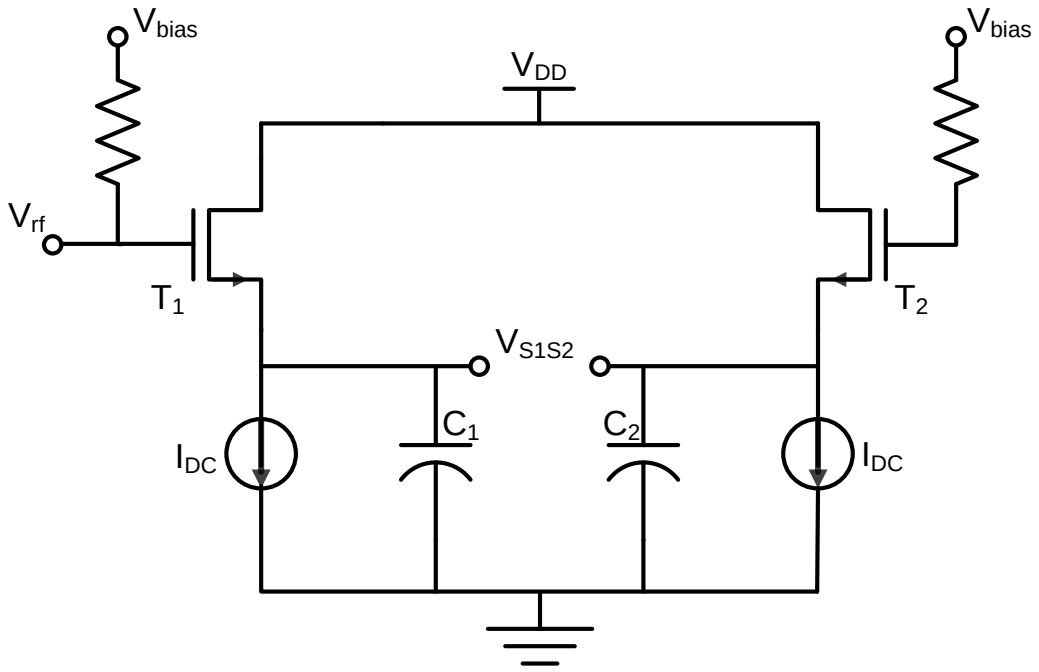


Figure 2-2. Meyer's detector MOSFET equivalent

In this chapter, an analysis of a configuration popularized by Meyer [22] is presented. [22] reports a BJT version of the detector; while Figure 2-2 shows a MOSFET equivalent version. In this topology, the first step of rectification V/I conversion occurs through the drain current equation $I_d = f(V_{rf})$; the drain current is a function of the RF input voltage. RF-to-DC conversion takes place through the non-linear properties of the transistor T_1 where the drain current is the main source of non-

linearity; as a result, the RF current generates an equivalent DC current. The last step of rectification, I/V conversion, is created through the gate-source junction. From Figure 2-2, the total DC current through transistor T_1 consists of the quiescent current $I_{DC\text{-}quiescent}$ in addition to the DC current created from the RF input signal $I_{DC\text{-}rf}$

$$I_{DC} = I_{DC-quiescent} + I_{DC-rf} \quad (2\text{-}1)$$

At steady state, since the bias current source I_{DC} is constant, then the current $I_{DC\text{-}rf}$ is proportional to the current $I_{DC\text{-}quiescent}$. Also, the gate-source voltage of the rectifying transistor changes proportionally to the DC quiescent current $I_{DC\text{-}quiescent}$; hence, I/V conversion is obtained as the source voltage of the rectifying transistor T_1 changes proportionally to the DC current $I_{DC\text{-}rf}$. Thus, as explained above, all the steps necessary for amplitude detection can happen using a simple transistor configuration. V/I conversion, RF-to-DC conversion, I/V conversion are all functions that are carried out using one transistor. The distinctive idea is that the RF-to-DC conversion occurs before amplification. As long as the rectifying transistor is biased properly, the Meyer topology can generate a noticeable voltage change; then amplification at DC can ensue if necessary. This detection strategy extends the bandwidth of the detector well above the millimeter wave range, as opposed to being limited by the bandwidth of conventional V/I converters. Figure 2-3 shows measurements results of a MOS detector at two different frequencies. The two plots do not overlap because pad and probes effects were not fully de-embedded from the measurement results. Full details regarding the calibration associated with the measurement setup are presented in APPENDIX A. Since testing the detector requires an absolute measurement, as opposed to ratioed, this calibration procedure is necessary.

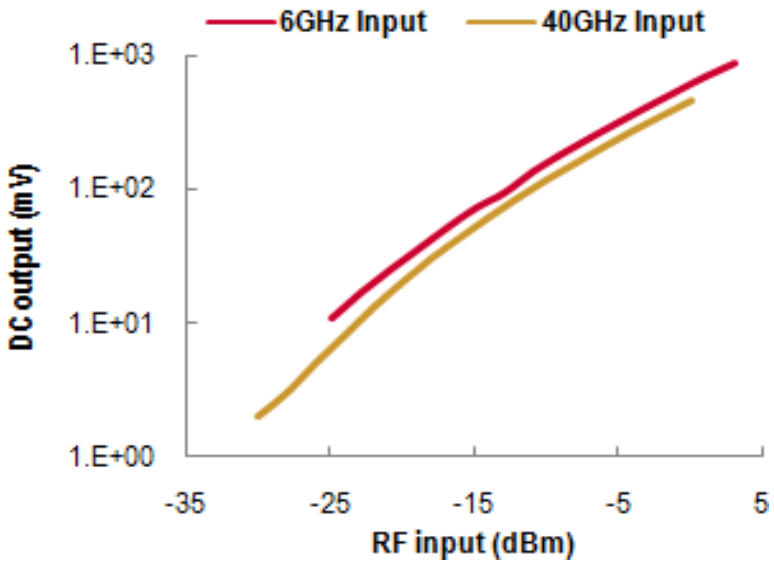


Figure 2-3. Measurement of MOSFET detector

Alternate test methods which use amplitude detectors usually belong to two categories. The first method treats detectors as implicit feature extractors and relies on statistical analysis to estimate DUT specifications from detector measurements [23]. The second school of thought identifies detector structures whose outputs can be directly mapped to the DUT specifications; for example, [24] directly extracts gain and IIP3 of a DUT using rms detectors without resorting to learning steps. Both methods need the detector's response to have strong correlation to the DUT specifications. This sometimes requires significant pre or post processing for the first method; the second method's drawback is usually the long list of assumptions required to achieve the direct correlation. In the next sections, the focus is to present simple design guidelines to dispel the disadvantages associated with the second method. The detector's response is characterized across multiple operating conditions to increase the reader's insight into this detector topology which, hopefully, will enable a wider use of this and similar RF BIST topologies.

Saturation Region

The following analysis assumes that the dominant source of non-linearity in MOS transistors emerges from the drain current. To simplify the derivations below, the long channel model is used. An analysis of short channel effects is done in [20], which uses a slightly different topology; nevertheless, it operates in saturation as well. The publication [20] determines that the detector still functions even when short channel effects are taken into account. When a MOSFET is biased in the saturation region, the long channel drain current is

$$I_d = \frac{\mu * C_{ox}}{2} * \frac{W}{L} * (V_{gs} - V_t)^2. \quad (2\text{-}2)$$

When the detector is stimulated with an RF input, the equation above becomes

$$I_d = \frac{\mu * C_{ox}}{2} * \frac{W}{L} * \left((V_{gs} - V_t) + V_{rf}\right)^2, \quad (2\text{-}3)$$

where V_{rf} is $V_{rf} = A * cos(\omega t)$. To calculate the output voltage V_{S1S2} in Figure 2-2, the drain current through transistor T_1 is equal to the bias current I_{DC} at steady state. Given that equal bias currents are applied to transistors T_1 and T_2 which are identically sized, the following equation results

$$\left((V_{gs1} - V_{t1}) + V_{rf}\right)^2 = (V_{gs2} - V_{t2})^2$$

$$(V_{gs1} - V_{t1})^2 + A^2 cos(\omega t)^2 + 2(V_{gs1} - V_{t1}) A \cos(\omega t) = (V_{gs2} - V_{t2})^2.$$

Also, since $\cos(\omega t)^2 = \frac{1+\cos(2\omega t)}{2}$, the equation above can be simplified further into

$$(V_{gs1} - V_{t1})^2 + \frac{A^2}{2} + \frac{A^2}{2} cos(2\omega t) + 2(V_{gs1} - V_{t1}) A \cos(\omega t) = (V_{gs2} - V_{t2})^2$$

The low pass filter (Capacitor C_1) at the output cancels the terms $\cos(\omega t)$ and $\cos(2\omega t)$. And only the DC terms will remain. Therefore,

$$(V_{gs1} - V_{t1})^2 + \frac{A^2}{2} = (V_{gs2} - V_{t2})^2$$

$$V_{gs1} = V_{t1} \pm \sqrt{(V_{gs2} - V_{t2})^2 - \frac{A^2}{2}}$$

Since the transistor is biased in the saturation region, $V_{gs1} > V_{t1}$. Then,

$$V_{gs1} = V_{t1} + \sqrt{\left((V_{gs2} - V_{t2})^2 - \frac{A^2}{2}\right)}$$

$$V_{gs1} + V_{s2g} = V_{s2g} + V_{t1} + \sqrt{\left((V_{gs2} - V_{t2})^2 - \frac{A^2}{2}\right)}$$

$$V_{s1s2} = (V_{gs2} - V_{t1}) - \sqrt{\left((V_{gs2} - V_{t2})^2 - \frac{A^2}{2}\right)} \qquad (2\text{-}4)$$

By definition, the threshold voltage is dependent on the source to body voltage V_{sb}. Then, it is possible for the two threshold voltage to be different $V_{t1} \neq V_{t2}$ since the voltage V_{s1} changes proportionally with V_{rf}. When the body of transistor T_1 is tied to ground, then the voltage V_{s1b} is not constant when V_{rf} changes. As a result, the threshold voltage V_{t1} will change as well. On the other hand, if the body and the source of the transistor are tied together, such as the case of triple well transistors, then the two threshold voltages are equal $V_{t1} = V_{t2}$. The two threshold voltages are also equal for very small input signals since V_{s1} does not vary substantially compared to V_{s2}.

Using Taylor's series expansion, equation (2-4) becomes

$$V_{s1s2} = \frac{1}{4(V_{gs2} - V_{t2})} A^2 + \frac{1}{32(V_{gs2} - V_{t2})^3} A^4 + \cdots \qquad (2\text{-}5)$$

This will be discussed in the following section. Figure 2-4 shows simulation results of the detector's RF-to-DC response when it operates in the saturation region. It also shows the response when the detector is biased in the subthreshold region. Further details regarding this operating region will be discussed in the following section. Figure 2-4 also shows dashed lines that represent the best fit line of the detector's response. For the saturation region, the plotted best line is a second-order equation. As predicted

from the Taylor's expansion equation (2-5) , for smaller signal levels, there is good conformance between the detector's response and the second order best fit plot. For those input levels, the detector implements a sum of squares function which is needed for RMS detection. As the input signal levels increases, the detector's response starts deviating from square law rectification.

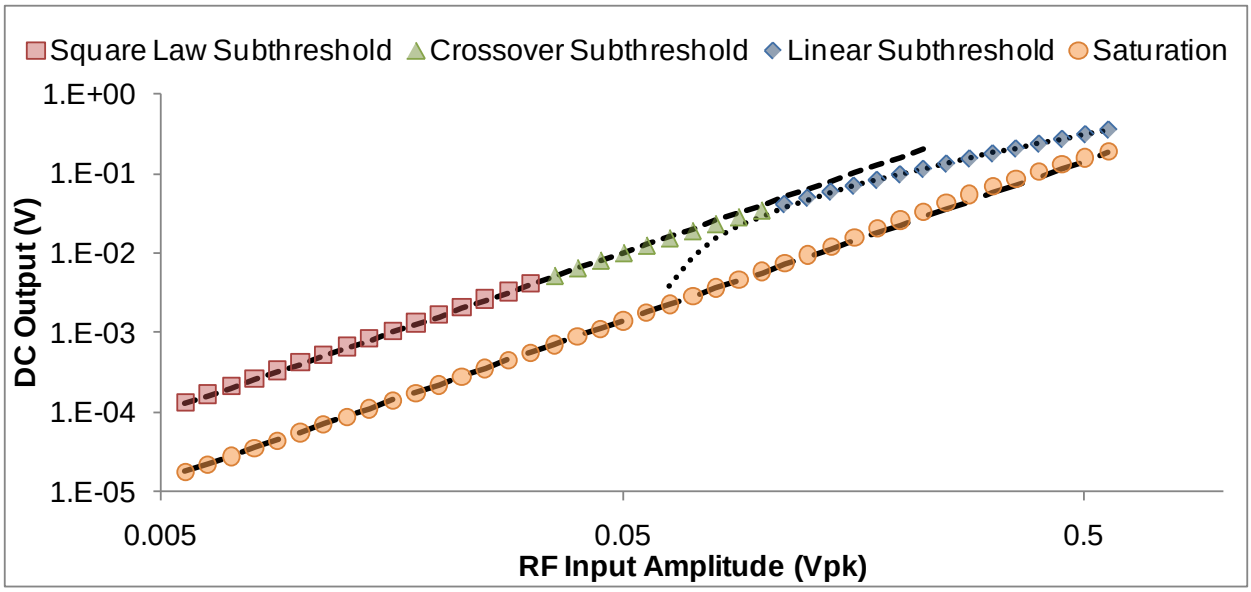


Figure 2-4. Detector's response in saturation and subthreshold

Subthreshold Region

Depending on the application, it is possible to operate this detector in the subthreshold (weak inversion) region. In that operating region, MOS transistors have similar characteristics to BJT devices [25]. In subthreshold, the drain current I_d becomes

$$I_d = I_{d0} * e^{\frac{V_{gs}-V_t}{nV_T}} \quad (2\text{-}6)$$

Also, the collector current for a bipolar transistor is [26]

$$I_c = I_s * e^{\frac{V_{BE}}{V_T}} \quad (2\text{-}7)$$

As seen in the previous two equations, both the subthreshold and bipolar currents have an exponential format. Then, to obtain the MOS detector's output, only a slight modification to the BJT Meyer detector's output equation is necessary.

The equation for the Meyer Detector [22] is

$$V_{e1e2} = A - \frac{V_T}{2} * \ln\left(\frac{2\pi A}{V_T}\right) \tag{2-8}$$

The manipulated equation for MOS detector in subthreshold is

$$V_{s1s2} = A - \frac{nVT}{2} * \ln\left(\frac{2\pi A}{nV_T}\right) \tag{2-9}$$

The preceding equation (2-9) does not take into account the body effect. [21] does an analysis that assumes the body is tied to ground. In that case, the output equation is slightly different

$$V_{s1s2} = \frac{A}{n} - \frac{VT}{2} * \ln\left(\frac{2\pi A}{nV_T}\right). \tag{2-10}$$

An extension taken from a publication [27] which uses the Meyer's BJT topology can be applied to the MOS version when biased in subthreshold. [27] indicates that equation (2-8) derived for bipolar detectors is only accurate for inputs that are larger than 100mV. That paper also reports an equation for input amplitudes lower than 30mV

$$V_{e1e2} \approx \frac{A^2}{4V_T} \tag{2-11}$$

By the same token, this can be extended to MOS detectors such as

$$V_{s1s2} \approx \frac{A^2}{4nV_T} \tag{2-12}$$

However, this equation is only valid for triple well MOS transistors. When the body effect is considered, the drain current for transistors in subthreshold is (assuming that $V_{ds} >> V_t$)

$$I_d = I_{d0} * e^{\frac{Vg - nVs - V_t}{nVT}}.$$

After further manipulations, the new equation for the subthreshold detector with body effect for small signal levels is

$$V_{s1s2} = \frac{A^2}{4n^2 V_T} - \frac{V_{t1} - V_{t2}}{n} \quad (2\text{-}13)$$

Further simplification to this equation can be done; since it was derived for small signal levels, the difference between the two threshold voltages V_{t1} and V_{t2} is negligible. The equation can be rewritten such as:

$$V_{s1s2} \approx \frac{A^2}{4n^2 V_T} \quad (2\text{-}14)$$

Comparing equations (2-12) and (2-14) , the body effect contributes an additional *1/n* factor. Irrespective of the body effect, we have determined in this section that the detector's response in the subthreshold region vary according to the input signal level. For large signal levels, the detector's response is mostly linear according to equation (2-9) which means that the detector measures peak values. Figure 2-4 shows that in the linear subthreshold mode, simulation results closely match a best fit line derived using linear regression analysis. For the square law subthreshold mode (small signal levels), second order regression analysis was necessary to obtain the best fit line as predicted by equation (2-12). In that mode, the detector implements RMS measurements. In this section, short channel effects were ignored since they are insignificant in the subthreshold region [18]. For low bias current levels, the channel field strength is low; the effects of velocity saturation are minimal as long as V_{gs}-V_t < .1*$\xi_c L$ [26].

Body Effect Summary

The following table shows a summary of all the equations presented before for the DC output of the MOSFET detector.

Table 2-1. Summary of RF-to-DC conversion equations

	Saturation	Subthreshold	
	All inputs	*Small input*	*Large input*
Triple well	$(V_{gs2}-V_{t2})-\sqrt{\left((V_{gs2}-V_{t2})^2-\frac{A^2}{2}\right)}$	$\frac{A^2}{4nV_T}$	$A-\frac{nV_T}{2}\ln\left(\frac{2\pi A}{nV_T}\right)$
Body effect	$(V_{gs2}-V_{t1})-\sqrt{\left((V_{gs2}-V_{t2})^2-\frac{A^2}{2}\right)}$	$\frac{A^2}{4n^2V_T}$	$\frac{A}{n}-\frac{V_T}{2}ln\left(\frac{2\pi A}{nV_T}\right)$

As seen in the table above, the body effect impacts the RF-to-DC conversion of MOS detectors. In the saturation region, the body effect appears through the threshold voltage V_{t1}. The threshold voltage is [26]

$$V_t = V_{t0} + \gamma(\sqrt{2\phi_F + V_{sb}} - \sqrt{2\phi_F})$$

When the detector's body is tied to ground, V_{sb} increases with higher input signal levels; which in turn increases the threshold voltage V_{t1}. In equation (2-4), a larger threshold voltage V_{t1} translates into a smaller detector's DC output; however, its overall impact is small due the square root in equation (2-4). Moreover, for very small input levels, the input's amplitude effect on the threshold voltage is minimal since the DC voltage in the source terminal of transistor T_1 varies weakly when the input is small. Therefore, the body effect in detectors biased in the saturation region is not significant. For detectors operating in the subthreshold, the body effect appears as a *1/n* factor. The effect of this factor is also minimal since *n* is usually a number between *1<n<2*. Comparing simulations of a triple well detector to simulations with a standard transistor, the worst case difference between the DC outputs of the amplitude detectors was in the order of 10%.

Triode Region

All the previous analyses were done assuming that V_{ds} of the rectifying transistor is high. Let's investigate operation in the triode region. Similar to the previous sections, the drain current is assumed to be the dominant source of nonlinearity. In the triode region,

$$I_d = \frac{\mu * C_{ox}}{2} * \frac{W}{L} * \left((V_{gs} - V_t)V_{ds} - \frac{{V_{ds}}^2}{2} \right).$$

This equation shows that the RF input at the gate terminal will not generate any non-linearity. This is the case because the drain current equation given above does not have any non-linear term in the term V_g. For the Meyer topology, the RF-to-DC conversion is generated because the current has higher order proportionality to the voltage V_g. For example, in the saturation region, the RF-to-DC conversion happens because the drain current follows the square law equation. Specifically, the voltage V_g which consists of the bias Voltage plus the RF input gets squared. But in this case, for the triode region, the voltage V_g is linearly proportional to the drain current I_d. However, measurement results show a weak RF-to-DC conversion that occurs in the triode region. This may happen because of the mobility's dependence on the voltage V_{gs}, non-linearities in MOS parasitic capacitances, and leakage of the RF signal through the substrate or parasitics to a non-linear junction.

Summary

In this chapter, we introduced a class of detectors that is suitable for mmWave BIST. Carrying-out all the stages necessary for detection using a single transistor enables operation at very high frequencies. A compilation of the detector's responses across multiple operating regions and different signal levels was presented. This was

done for detectors with and without the body effect. There was compelling motivation to gather all the equations into a single document as they were scattered across multiple publications. Also, the preceding literature did not clearly describe the conditions of operation associated with each equation. Moreover, the detector's responses were simplified; it is important to determine the type of proportionality each response has. A Taylor's series expansion was used for the first time to simplify the saturation response. Also, the detector has a linear and square-law proportionality depending on its operating region and the input signal level. When the detector has a linear proportionality, it is a peak detector. And when it has square-law proportionality, it is an RMS detector. Finally, it was determined that detection in the triode region is not possible with this topology. The measurement results presented in Figure 2-5 were part of joint collaboration effort using a colleague's MOS detector circuit [28]. Figure 2-5 shows the detector's response across multiple operating regions. So, in this chapter, the detector's building blocks were introduced. Next chapter presents a more profound characterization of the detector's response.

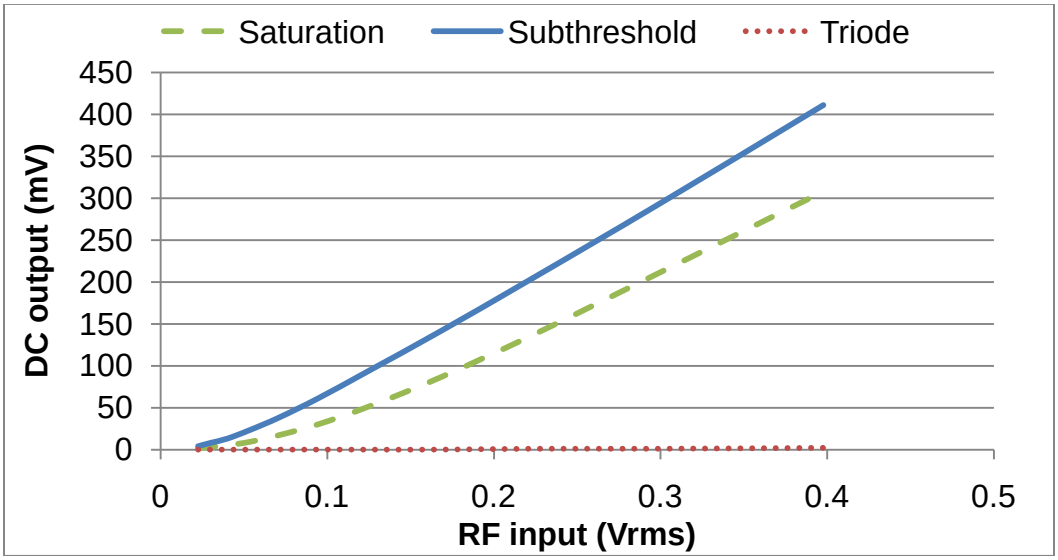


Figure 2-5. Measurement results in different operating regions

CHAPTER 3
DETECTOR'S RESPONSE

RMS Detector

Subthreshold Region

The previous analyses assume a single tone continuous wave (CW) signal was used to stimulate the input of the DUT. This is adequate from many BIST applications; for example, when measuring gain, it is sufficient to stimulate the DUT with a time invariant input and measure the detector's output at steady state. However, to do multi-tone tests [29] or measurements involving different waveforms shapes RMS detectors are important. Calorimetric sensors that rely on thermal dissipation are very accurate RMS detectors. This technique cannot be applied in BIST because of thermal coupling from adjacent circuits and slow response time. Another implementation uses diodes with a square law behavior. Diodes suffer from high noise levels, high temperature coefficients, and high performance Schottky barrier diodes (SBD) are not available in standard CMOS processes. [14] designed an RMS detector based on the translinear principle using a BiCMOS technology. However, the bandwidth is restricted to 1GHz due to the performance of the V/I converter circuit. [30] states that the BJT Meyer detector is an RMS detector for low input signal levels (<30mV). For larger signals, the detector acts more like a peak detector. As a result, RMS detection is not possible for larger signal values unless attenuators are used. To extend the dynamic range of this detector, [30] used a number of attenuators to decrease high signal levels so that the detector operates in the RMS mode. This technique can be used for the MOSFET Meyer detector as well when it operates in the subthreshold region; so that the detector

operates in the square-law-subthreshold mode. RMS measurements require adding the squares of each input harmonic to obtain the total power.

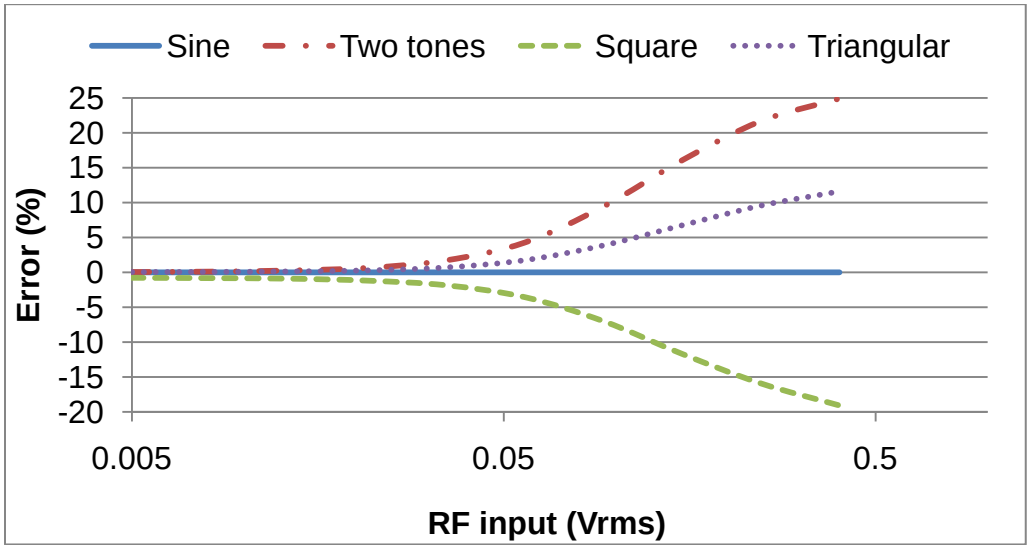


Figure 3-1. Relative error of the detector's output to various waveform shapes

Figure 3-1 shows simulation results of the detector when it operates in the subthreshold region when various waveform shapes with equivalent RMS amplitude are used as stimulus to the detector. The error relative to the detector's response when stimulated with a single tone is plotted for each waveform respectively. As predicted, the error in the square-law mode (low signal levels) is small. On the other hand, as the signal enters the linear mode, the detector's response to different waveform shapes varies. For example, each harmonic in a two tones signal has an amplitude of $a/\sqrt{2}$. And the single tone's RMS equivalent amplitude is a. In the square-law subthreshold mode, the DC term proportional to each tone in the two tones signal is squared. This realizes the following function $(a/\sqrt{2})^2 + (a/\sqrt{2})^2 = a^2$, which is equivalent to an RMS operation. However, in the linear-subthreshold mode, the detector performs a linear conversion. In that case, the detector will overestimate the RMS power because the two

tone signal peak amplitude is $a/\sqrt{2} + a/\sqrt{2} > a$. From Figure 3-1, the rms detection error is lower than 6% when V_{rms}<70mV for the two tones input.

Saturation Region

The RF-to-DC conversion equation in both BJT and MOS Meyer detectors consists of a series with an infinite number of terms. Approximating square law behavior is only possible in a specific range when higher order terms can be neglected. This means that when the MOS detector operates in the saturation region, RMS detection can be achieved in a certain range. Once the sum of squares is achieved through detection, any post processing such as the square root function or linear-to-decibel conversion which might be required to complete RMS measurements can be done off chip since the output of the detector is DC. When the detector is stimulated with a periodic signal of any shape

$$V_{rf} = \sum_{i=1}^{N} A_i \cos(\omega_i * t + \phi_i).$$

In the saturation region, the drain current becomes

$$I_d = \frac{\mu C_{ox}}{2} \frac{W}{L} * \left({V_{ov}}^2 + 2 V_{ov} V_{rf} + {V_{rf}}^2 \right)$$

where the overdrive voltage V_{ov} is equal to the gate to source voltage minus the threshold voltage V_{gs}-V_t. For the Meyer topology, the term $2V_{ov}\,V_{rf}$ is eliminated by the low pass filter. Using Volterra algebra, the only DC components that remain from ${V_{rf}}^2$ are $\frac{1}{2} * \sum {A_i}^2$. None of the other cross modulation terms that results from ${V_{rf}}^2$ are translated to DC. The square law behavior of the drain current in the saturation region makes RMS detection possible. The MOS detector's output when it operates in the saturation region given any periodic RF stimulus is

$$V_{s1s2} = V_{ov} - \sqrt{{V_{ov}}^2 - \frac{1}{2} * \sum {A_i}^2}. \tag{3-1}$$

Applying the Taylor series expansion to the equation above

$$V_{s1s2} = \frac{1}{4 * V_{ov}} * \sum {A_i}^2 + \frac{1}{32 * {V_{ov}}^3} * \left(\sum {A_i}^2\right)^2 + \cdots \tag{3-2}$$

Equation (3-2) can be simplified further into

$${V_{s1s2}}' = \frac{1}{4 * V_{ov}} * \sum {A_i}^2. \tag{3-3}$$

However, this equation is accurate only in a certain range. Solving the following inequality will determine this range

$$\frac{{V_{s1s2}}' - V_{s1s2}}{V_{s1s2}} < Err.$$

This inequality describes when the simplified equation deviates from the actual equation within a certain threshold. Its solution is given with the following inequality

$$\sum {A_i}^2 < (8|Err| - 8Err^2){V_{ov}}^2. \tag{3-4}$$

Let's use an example to clarify this further. Let's set $Err = 6\%$, then the range where the detector conforms to square law within a 6% error is $\sum {A_i}^2 < .45{V_{ov}}^2$.

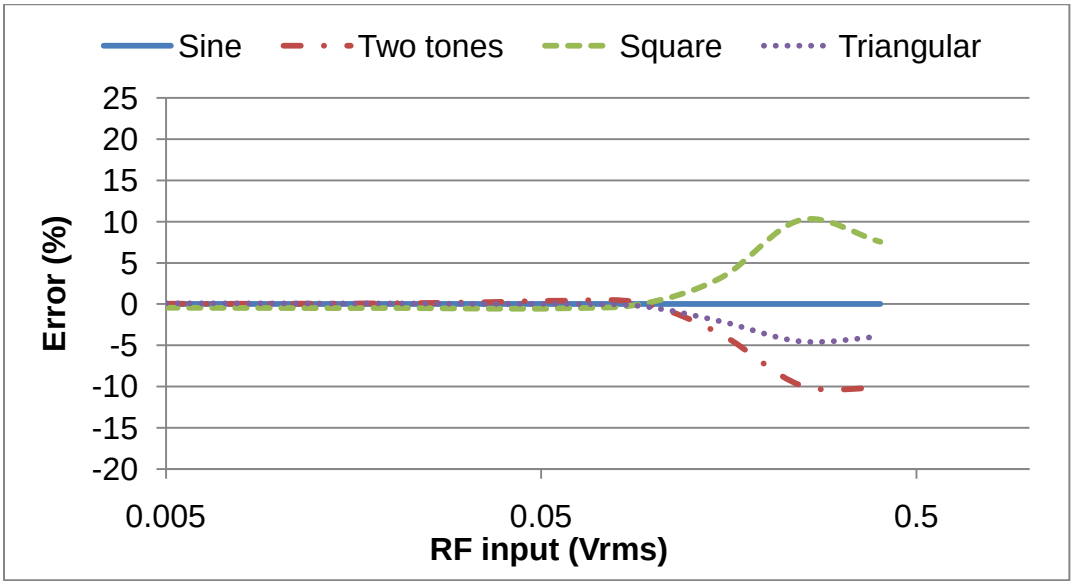


Figure 3-2. Relative error of the detector's output to various waveform shapes

Figure 3-2 shows that the detector outputs RMS values with good accuracy for low signal levels; as the signal's amplitude starts increasing, the response deviates from RMS detection. Similar to the analysis done for the subthreshold region, let's use a two tones example to uncover the cause. For low signal levels, since the detector follows the square-law, RMS detection is accurate because $(a/\sqrt{2})^2 + (a/\sqrt{2})^2 = a^2$. For higher input signal levels, higher order terms become significant. RF-to-DC conversion occurs through even order terms in the drain current $(\cos(\omega t)^2, \cos(\omega t)^4, \ldots)$. As explained above, if the drain current displayed ideal square law behavior, the detector's response will be the same irrespective of the signal's shape. However, for example, if the drain current has a fourth order component, RMS detection of a two-tone signal is no longer accurate relative to single tone. For the two tones input, by using Volterra algebra, the DC term created from a fourth order drain current term$(a/\sqrt{2} * \cos(\omega_1 t) + a/\sqrt{2} * \cos(\omega_2 t))^4$ is $3/8((a/\sqrt{2})^4 + (a/\sqrt{2})^4) = 3/16a^4$. But for the equivalent single tone stimulus, the DC value generated from the fourth order term is $3/8a^4$. This time, the detector underestimates the two tones RMS value relative the single tone RMS value. From Figure 3-2, RMS detection is accurate within 6% up to V_{rms}<190mV for the two tones input. The theoretical value derived from inequality (3-4) gives V_{rms}<208mV. Let's keep in mind that this theoretical inequality (3-4) was derived assuming an ideal square law current that is the dominant source of non-linearity. It does not take into account cross modulation between the harmonics, and second order effects such as the short channel, body effects, or higher order terms in the drain current. The inequality only accounts for the effects of ignoring higher order term in equation (3-2). This is not the same as the results shown in Figure 3-2 which plot the difference of the response to

different input shapes relative to the response with a single tone input. It should be known that even the single tone detector's response deviates from the square law behavior at higher signal levels. To sum up, any deviation from RMS detection results from higher order terms which become significant at higher input signal levels. In any case, the purpose of this section was to demonstrate that, when compared to subthreshold detectors or bipolar detectors, saturation detection has a wider dynamic range with accurate RMS detection characteristics. This range can be increased by increasing V_{ov}. However, there is a limit to this method; as V_{ov} is increased, short channel effects such as mobility degradation become dominant which limits RMS detection accuracy.

This section discussed RMS detection and its dynamic range for both subthreshold and saturation MOS detectors. It was shown theoretically and through simulations that RMS detection in the saturation region can be tuned by changing V_{ov}. Sources of errors which cause the detector to deviate from implementing a sum of squares function were discussed through examples as well.

Envelope Detector

The previous section only considers the detector's DC output. Recent developments in RFIC test extract more specifications from the envelope of an RF modulated signal using alternate test methodologies [31]. Another publication [32] uses a non-linear regression method to map the envelope's amplitude into third order intercept (TOI) specification of a DUT. The detector discussed in this dissertation can effectively be used to measure the envelope of an RF signal. The detector can track the envelope of amplitude modulated (AM) signals or digital modulations based on

amplitude shift keying (ASK). The bandwidth of the low pass filter at the output of the detector should be high enough for baseband frequencies associated with the envelope. Also, the filter's bandwidth should be lower than the carrier frequency. This bandwidth is sometimes referred to as video bandwidth. Let's look at the RF-to-DC conversion in different operating regions when the detector is stimulated with a modulated signal

$$V_{rf} = A_c\big(1 + m(t)\big)cos(\omega_c t). \tag{3-5}$$

A_c is the amplitude of the carrier, $m(t)$ is the baseband data signal, and ω_c represents the carrier frequency. In the previous sections, we determined that the RF-to-DC conversion follows a square law behavior in the saturation region and in the square-law-subthreshold mode. Thus, the detector's output in both regions is

$$V_{s1s2} \approx \beta * \Big(A_c\big(1 + m(t)\big)\Big)^2. \tag{3-6}$$

β is a constant which depends on the operating conditions of the detector.

In the linear-subthreshold, the equation becomes

$$V_{s1s2} \approx \beta * \Big(A_c\big(1 + m(t)\big)\Big). \tag{3-7}$$

In the linear subthreshold, the carrier amplitude can be extracted from the DC output. The envelope's amplitude can then be extracted from the frequency content of the baseband (BB) signal. In the saturation and square-law-subthreshold regions, the DC output is no longer proportional to the carrier's amplitude only. Because of the squaring, some envelope information will show up at DC as well. In case the envelope is a sinusoidal wave with frequency ω_m, equation (3-6) becomes

$$V_{s1s2} \approx \beta {A_c}^2 \left(1 + \frac{{A_m}^2}{2} + 2A_m cos(\,\omega_m t) + \frac{{A_m}^2}{2} cos(\,2\omega_m t)\right). \tag{3-8}$$

If the envelope's amplitude A_m is small, the term associated with $2\omega_m$ can be neglected. It should be noted that there are many sources of errors that make the

detector deviate from these ideal envelope detection equations. For example, in the saturation region short channel effects may become important which will make the detector a non-ideal square law device. In the linear subthreshold, the logarithmic error term may be significant. One should also consider that if the signal levels are high, especially if the modulation index (depth) is high, it is possible that the conversion equation changes from linear proportionality to square-law proportionality. This happens because the detector's operation in the two subthreshold modes depends on the signal level. Distortion to the envelope can also occur because of inappropriate output filter bandwidth or small bias current levels. With careful design and a suitable calibration method, it is possible to use this detector as an envelope detector.

As seen in the Figure 3-3, the amplitude detector can act as an envelope detector as well. The detector is stimulated with an AM modulated signal with a 70GHz carrier frequency, 100MHz modulation rate, and 50% AM depth.

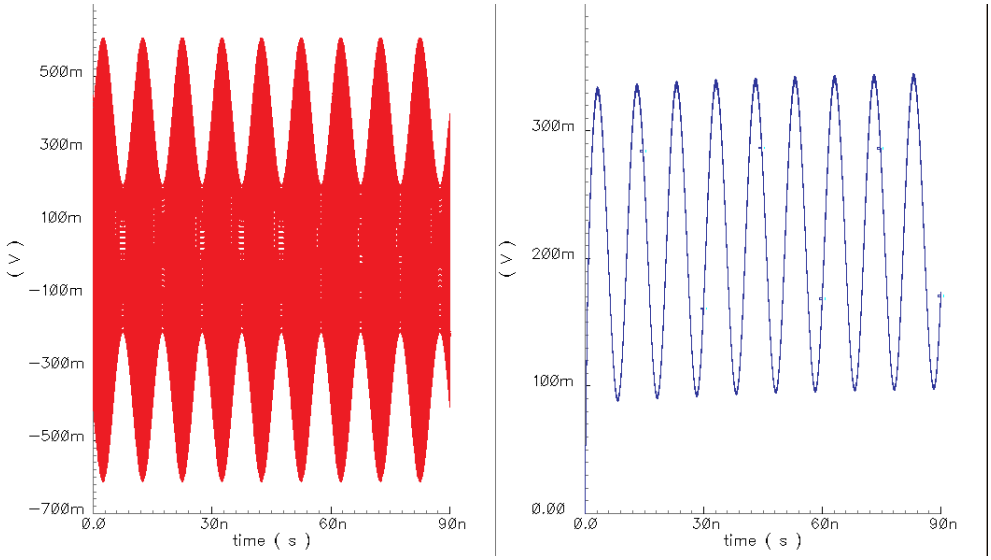


Figure 3-3. AM modulated signal to the left. Output of the detector to the right

Figure 3-4 shows measurement results of the detector with an AM modulated signal at three different carrier frequencies 5GHz, 9GHz, 13GHz. For those three carrier

frequency, the AM depth was set to 50%, and AM Rate was 1 KHz. It should be noted that the AM rate is low because the detector was not initially designed for envelope measurements. The amplitude of the detector's output is plotted as the input signal level is swept. The amplitude of the baseband (BB) signal at detector's output which was measured using an Oscilloscope is effectively proportional to the RF signal strength.

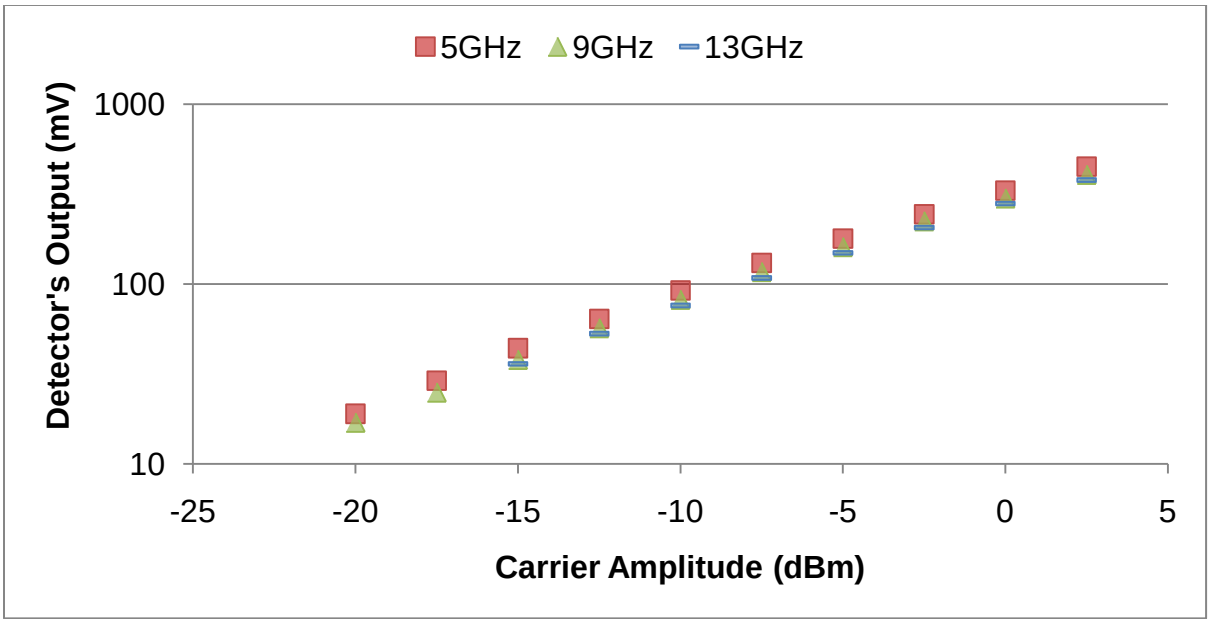


Figure 3-4. Measurement of the detector's output when input is modulated

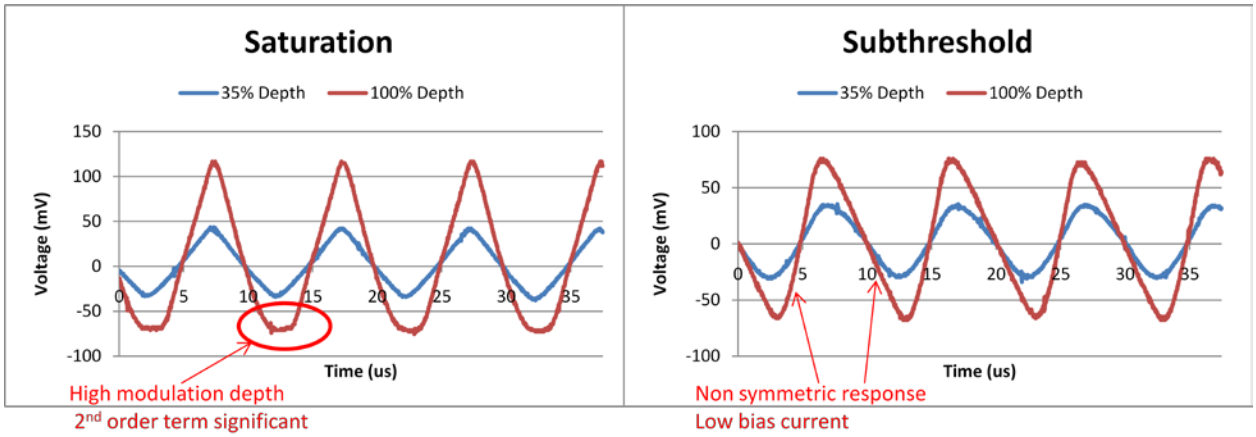


Figure 3-5. Oscilloscope capture of detector's response to a triangular AM input

Further Oscilloscope captures are shown in Figure 3-5 from a circuit presented in [28] and designed jointly with a colleague. The following figure shows the detector's

response when it is stimulated with 10GHz triangular AM modulated signal. The Modulation Rate is 100KHz. The detector was biased at two different operating points and two different modulation depths were used to expose the different responses. As previously mentioned, simple calibration methods can be used to extract the exact envelope as long as the detector's output filter is suitable. The next section discusses factors that are relevant to the output filter design.

Settling Time

All the previous equations were derived at steady-state; discussion the settling time of the amplitude detector is necessary. Settling time is important because it directly impacts the overall test time. Also, if the detector is to be used as an envelope detector, we need to take into account the effects of the time variant stimulus over the detector's response. [33] discusses the importance of the detector's response speed in applications with high crest fact (ratio of peak and rms value). Therefore, we need to incorporate another dimension, time, into this analysis. In this section, important metrics related to detector's time domain response are discussed.

The settling time of the detector's response needs to be fast; however, it should be limited to reject ripples at the output of the detector [13]. [34] discusses in detail the output ripples of the low pass filter in RMS detectors. In the frequency domain, this means that the video bandwidth should not extend all the way to the carrier frequency. Therefore, there is a limitation on the minimum settling time of the detector. As for the maximum settling time, it needs to be fast enough to correctly track the input's envelope or meet test time specifications. Moreover, charge and discharge times are distinctly different since they are not always equal (cf. Figure 3-5 "subthreshold"). Previous publications [22], [27], and [35] define the discharge rate (droop rate) as

$$\frac{\Delta V}{\Delta t} = \frac{I_{DC}}{C} \tag{3-9}$$

where the capacitance *C* refers to the capacitor used in the low pass filter, and the current I_{DC} is the DC bias current. Therefore, current and low pass filter capacitance determines how fast and how slow the output voltage changes. It should be noted that equation (3-9) is only an approximation of the discharge rate. Among other assumptions used to derive the equation, the amount of current discharging the capacitor C is only equal to I_{DC} when the rectifying transistor is completely turned off. This assumption is not always true especially in the case of modulated input signals. The total current flowing out of the discharging capacitor is equal to $I_{DC} - I_{T1}$, where the current I_{T1} is the DC current in transistor T_1 in Figure 3-6. The DC current I_{T1} can be decomposed into the transistor's quiescent current and the DC current converted from the RF input. For the charging rate, the total current flowing into the capacitor C is $I_{T1} - I_{DC}$.

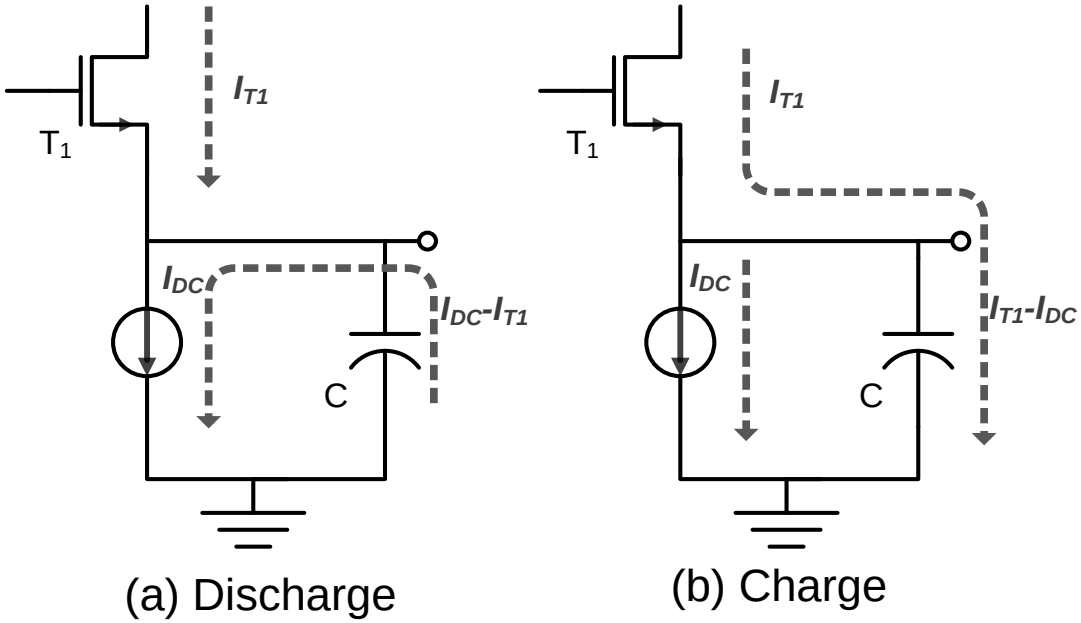


Figure 3-6. Discharge and charge paths

The detector's speed is almost always limited by the discharge time. The discharge time is mostly limited by I_{DC}; while, the charging current is set by I_{T1} which

can be large compared to I_{DC}. The instant an RF input is applied to a transistor, a large current can be generated from RF-to-DC conversion. In the linear subthreshold, the total DC current through transistor T_1 is

$$I_{T1} = I_{d0} e^{\frac{V_{gs1}}{nV_T}} \left(e^{\frac{A}{nV_T}} \Big/ \sqrt{2\pi\, A/nV_T} \right). \tag{3-10}$$

As seen in this equation, if A is really large, the charging time of the detector in subthreshold can be really fast due to the multiplicative effect. The settling time of detectors depends on many factors such as the operating region, the capacitor C in the LPF, the input signal level, and the aspect ratio of the rectifying transistor. It was important to show that the settling time of the detector does not only depend on the bias current I_{DC}. One can deduce from the simplified equation (3-9) that increasing the current I_{DC} always makes the detector faster. This is not always true; for example, in the saturation region the current that charges the capacitor is

$$I_{T1} - I_{DC} = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(\left(V_{gs1} - V_t\right)^2 + \frac{A^2}{2} \right) - \frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{gs2} - V_t\right)^2 \tag{3-11}$$

As can be seen in the equation above, if the bias current is increased by changing V_{OV} which is equal to the gate-to-source voltage minus the threshold voltage, the effect is minimal on the charging current. The charging rate is not faster in this case, because the change in bias current (I_{DC}) is cancelled by the change in the quiescent current (I_{T1}). Also, the DC current generated from the rectified RF input is not dependent on V_{OV} in this case. Therefore, the rectified current is constant regardless of the change in V_{OV}.

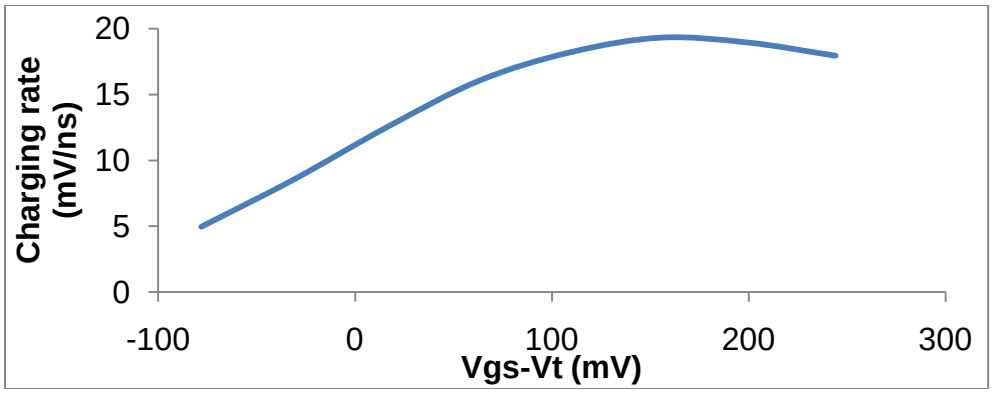


Figure 3-7. Charging rate as V_{OV} is swept

The settling time in detectors is not as straight forward as it seems to be. However, an important deduction can be made. Decreasing the low pass filter capacitor value will always make the settling time faster. This is also the case when the aspect ratio of the rectifying transistor is increased. Increasing the bias current generally helps, especially with increasing the discharge rate. And finally, the charging rate in subthreshold detectors is not always as slow as might be perceived. This is the case, because rectification in subthreshold can produce a current that is several factors of the quiescent current.

Frequency Response

Up to this point, all the equations presented for the detector's RF-to-DC conversion are not frequency dependent. The RF-to-DC conversion gain is equal to DC output of the detector over the RF input. Then, this detector could be described as passive frequency translation device. Therefore, the detector bandwidth is not limited by the gain-bandwidth product since the device does not amplify signals. At this point, according to the previous statement, it should be clear that the common perception that subthreshold detectors can only work at low frequencies is not true. The bandwidth in detectors should be different from the conventional methods used to define bandwidth.

A common equation used to define detector's bandwidth in the literature [20], [21], [22], and [27] is

$$f_{3dB} = \frac{1}{2\pi C_g * R_g}. \quad (3\text{-}12)$$

where,

R_g: is the series resistance looking into the input of the rectifying transistor.

C_g: the gate capacitance.

It should be clear that this equation is calculating the effects of the gate series resistance as if the detector is a standalone circuit stimulated with a 0Ω source. Since the detector is employed for BIST, bandwidth should also consider the loading effect the detector has on the circuit under test (CUT). In modern processes, the detector's load is mainly equal to the rectifying transistor's gate capacitance. This is usually only few *femto*Farads. Therefore, the detector will have minimal effect on the CUT. That capacitance can easily be absorbed into the matching networks. In case the CUT cannot be modified, an alternate equation that reasonably represents the bandwidth of the embedded detector is defined. Let's first identify all the variables needed to derive this equation.

Loss: the maximum loss that the CUT can tolerate from the detector's loading effects.

Z_L: the impedance looking into the node to be tested.

The following example is derived in the context of a detector at the output of the CUT. When the detector is used at the input of a CUT, the equation will hold true as well.

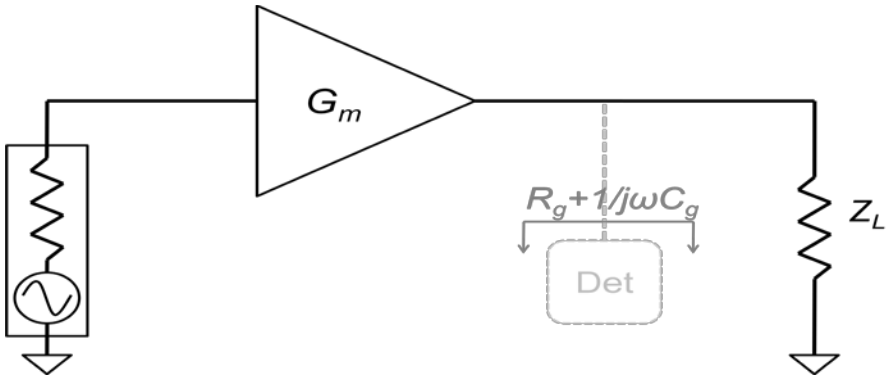


Figure 3-8. Loading effects of the detector on the DUT

The gain of a CUT without the detector is $G_m * Z_L$, where G_m stands for the transconductance of the CUT. The gain of the CUT with the embedded detector is $G_m * \left(Z_L \,||\left(R_g + \frac{1}{j2\pi f C_g}\right)\right)$. Therefore, the loss caused by the detector's loading is

$$Loss = \frac{\left(Z_L \,||\left(R_g + \frac{1}{j2\pi f C_g}\right)\right)}{Z_L} \tag{3-13}$$

After further manipulations, solving the equation above for the tolerable loss frequency, the new formula which accounts for detector's loading effects on the DUT is obtained

$$f_{Loss} = \frac{1}{2\pi C_g} * \sqrt{\frac{1 - Loss^2}{Loss^2\left(Z_L + R_g\right)^2 - {R_g}^2}}. \tag{3-14}$$

To give this equation some meaning, let's give an example using commonplace values in modern processes. Let's set R_g= 5Ω, C_g= 4fF, Z_L= 50Ω, and the tolerable loss to *Loss*= .1dB which is a conservative value. The corresponding frequency where the CUT will experience a relative gain loss of .1dB is $f_{Loss} = 110GHz$. The 3dB frequency defined by equation (3-12) is 796*GHz*; the loss to the CUT at that frequency is 18dB and is not 3dB as one might assume. In any regards, one should look at both of these frequencies when using detectors for BIST. In addition, these equations are only accurate to a first degree since transistor parasitics do vary with biasing, frequency, and signal levels. Also, one should consider that if passive elements (such as ac coupling

capacitors) are used at the input of the detector, the bandwidth is considerably affected by the attributes of these passive elements. Both Figure 3-9 and Figure 3-10 show the impact of using a coupling capacitor at the input of the detector.

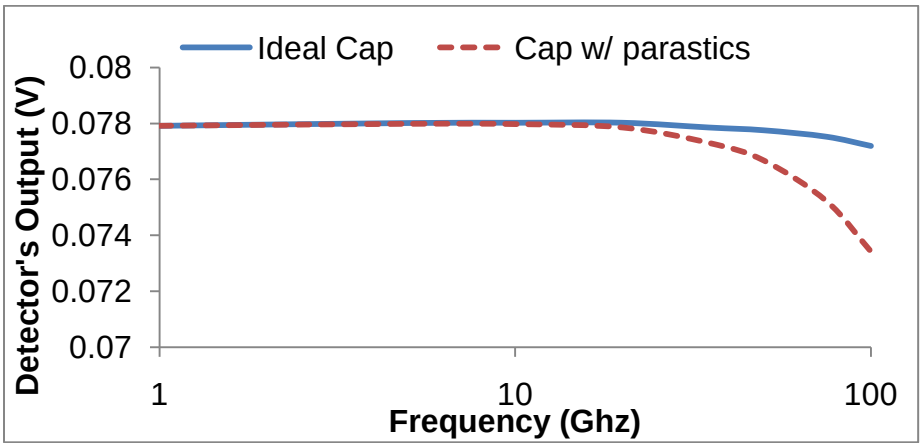


Figure 3-9. Detector's output over frequency

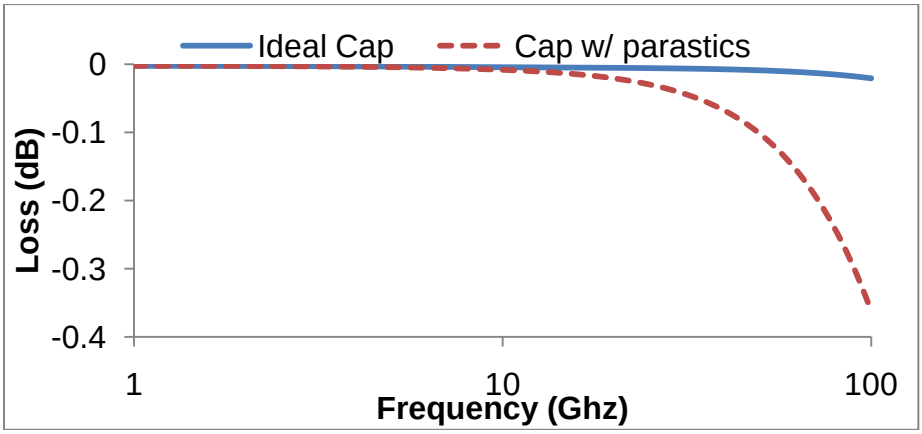


Figure 3-10. Loss to a DUT caused by the detector's loading effects

Detector's Accuracy

Any integrated circuit is set to experience environmental variations such temperature changes. These types of variations have to be accounted for early in the design stage for inclusion of mitigation strategies.

Temperature Variations

Temperature effects on the amplitude detector are investigated in the following section. The detector's response is not immune to temperature variations and several calibration methods were proposed in the literature to compensate for these effects.

First order calibration

Feedback loop using amplifier. Temperature compensation strategies have been widely investigated for all types of detector topologies. [36] reports a method to minimize temperature effects on diode detectors. Its compensation strategy is based on a feedback loop which uses an amplifier that adjusts the biasing conditions of the rectifying element as the temperature changes across a circuit used as a standard. The standard is a replica of the rectifying circuit without any input applied to it. This method eliminates the detector's dependence on current variations through the rectifying devices by assuming that temperature variation affects the rectifying device in the same manner as the standard. [37] and [38] share a similar temperature compensation scheme implemented for detectors that use transistors. [37] is a bipolar amplitude detector slightly different than the Meyer topology. [38] is a MOS detector; however, instead of measuring RF signals, it measures radiations. These detectors are included in this discussion because of their interesting temperature compensation strategies and since they are based on similar principles as MOS amplitude detectors by exploiting the non-linear properties of a transistor. Figure 3-11 shows the topology on which these two detectors are based; its major difference compared to the Meyer topology is the use of a resistor instead of current source.

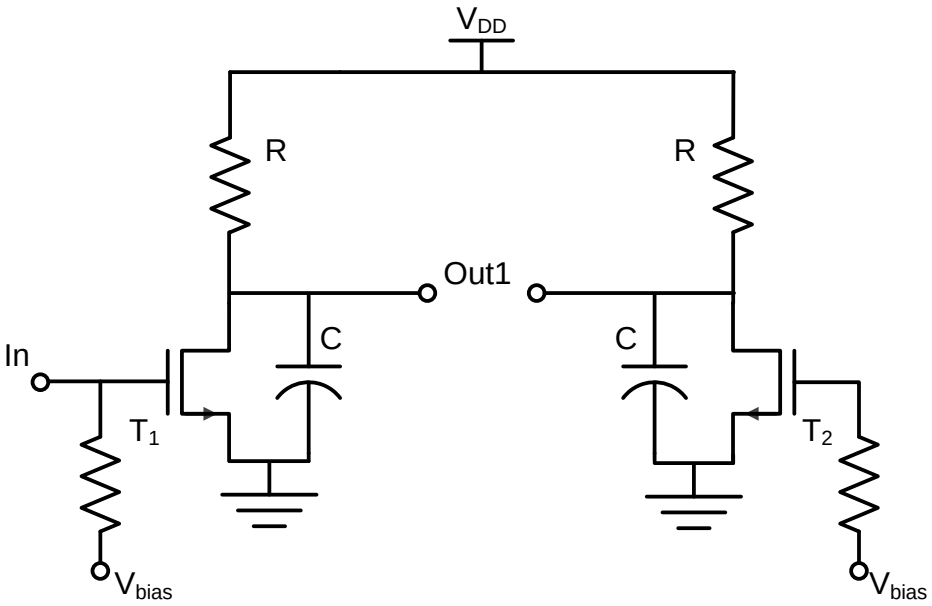


Figure 3-11. Detector using resistor

This topology was also reported in the literature [39] without any consideration to temperature effects. This detector's accuracy is greatly decreased since its output is highly dependent on temperature. For example, for small signal levels when the rectifying transistor is biased in subthreshold, the output of the detector is derived such as

$$\frac{V_{DD}-V_{d1}}{R}=I_s e^{\frac{V_{g1s1}-V_{t1}}{nV_T}}*\left(1+\frac{A^2}{2n^2{V_T}^2}\right) \quad (3\text{-}15)$$

$$\frac{V_{DD}-V_{d2}}{R}=I_s e^{\frac{V_{g2s2}-V_{t2}}{nV_T}} \quad (3\text{-}16)$$

where the voltage V_{d1} stands for voltage at the drain of transistor T_1, A is the amplitude of the high frequency input signal stimulating the detector, V_t is the threshold voltage, and V_T is the thermal voltage kT/q. The output of this detector is the difference between V_{d2} and V_{d1}. Since the overdrive voltage (V_{gs}-V_t) across the two transistors T_1 and T_2 are the same, equation (3-15) can be subtracted from (3-16) to obtain:

$$Out1=R*I_s e^{\frac{V_{g1s1}-V_{t1}}{nV_T}}*\left(\frac{A^2}{2n^2{V_T}^2}\right) \quad (3\text{-}17)$$

This equation is highly dependent on temperature, especially through the exponential term. Several attempts have been made to minimize the temperature effects of the topology shown in Figure 3-11. [16], for example, proposes a closed loop system that changes the biasing of the amplitude detector dynamically as the temperature changes. It uses a temperature compensator circuit in conjunction with a diode used as reference. The patent, however, does not disclose any information regarding the temperature compensation circuit.

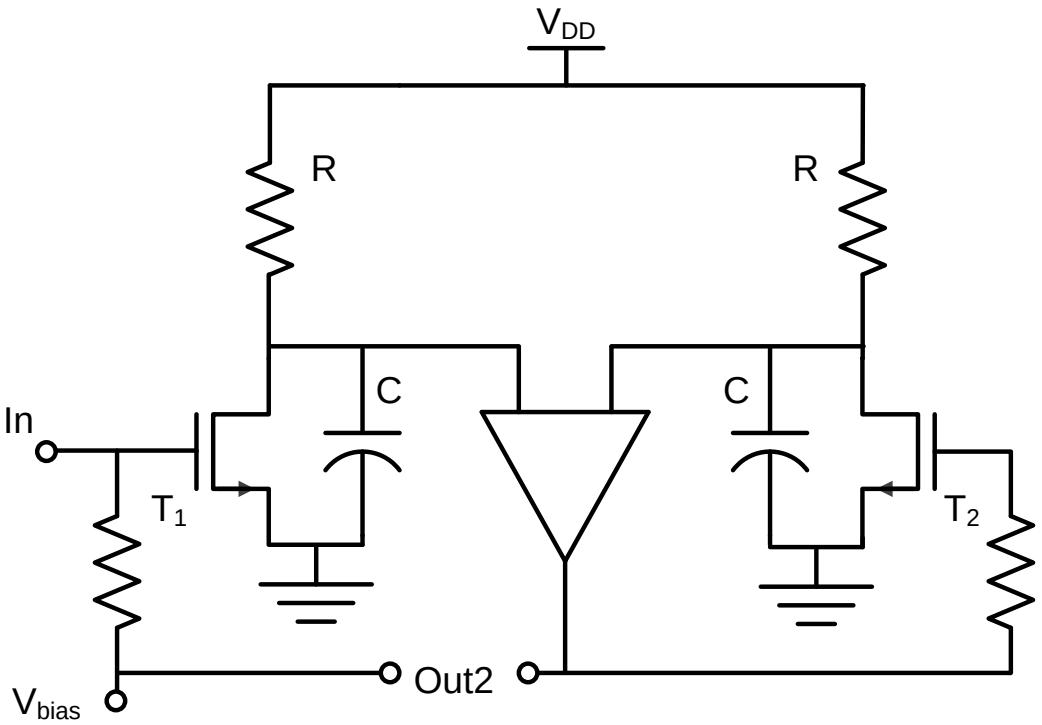


Figure 3-12. Detector using feedback to compensate for temperature variations

Another feedback method employed in [37], [38] which minimizes temperature effects is shown in Figure 3-12. After the feedback loop settles when the detector is stimulated with an RF input, the currents trough transistor T_1 and T_2 should be equal.

$$I_s e^{\frac{V_{g1s1}-V_{t1}}{nV_T}} * \left(1 + \frac{A^2}{2n^2{V_T}^2}\right) = I_s e^{\frac{V_{g2s2}-V_{t2}}{nV_T}}$$

This equation is simplified such as

$$1 + \frac{A^2}{2n^2{V_T}^2} = e^{\frac{V_{g2g1}}{nV_T}}$$

Since the output of this topology is taken across the gates of the two transistors T_1 and T_2, and with some manipulations to the equation above, the detector's output is

$$Out2 = \frac{A^2}{2n\,V_T}$$

Unlike the output in equation (3-17), this detector is no longer exponentially dependent on temperature. Note that this equation is exactly the same as the Meyer topology equation. As can be seen, these compensation methods are not completely immune to temperature variations; nevertheless, they provide a first order compensation method.

Meyer topology. In the Meyer topology, a current source is used compared to the resistor used in [37], [38]. It was shown that the output of the topology in Figure 3-12 when feedback was used is similar to the Meyer topology output; thus, the Meyer topology does not require any additional compensation. Good accuracy can be achieved as first order temperature compensation is inherent within the Meyer configuration. [37] emphasizes the importance of bias currents in detectors; it leveraged the amplitude detector shown in [13] by using a fixed transconductance bias circuit. This allowed .5dB accuracy across process corners in the temperature range of 0°C to 70°C. Furthermore, the impact of using the current source can be verified by examining the theoretical equations derived for the MOSFET Meyer detector's output. Simulations below show the output's dependence on temperature across many regions of operation to comply with the spirit of this dissertation which attempts to present Meyer's detector response in the simplest way possible across different operating conditions.

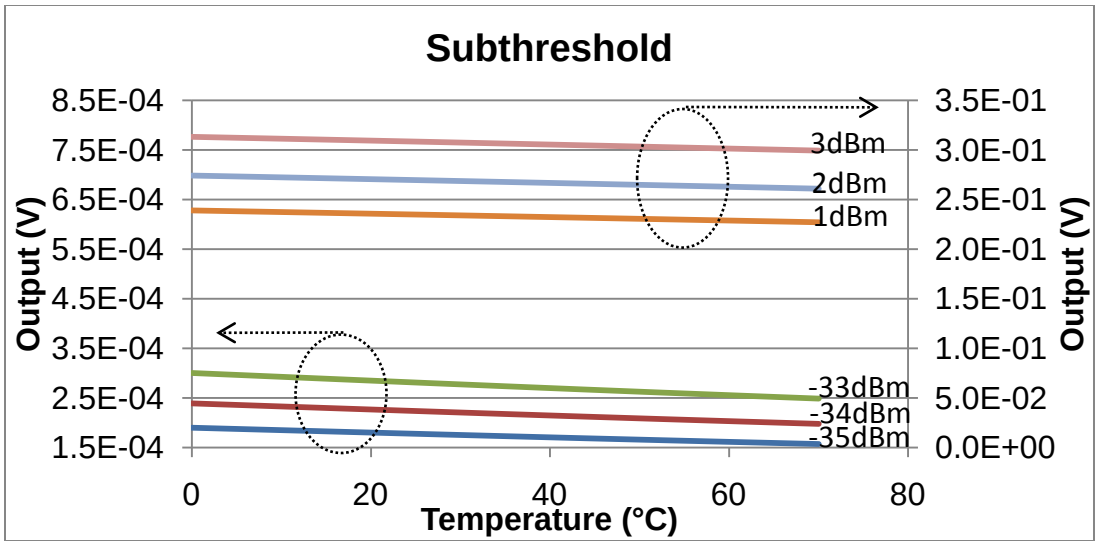


Figure 3-13. Subthreshold response vs. temperature

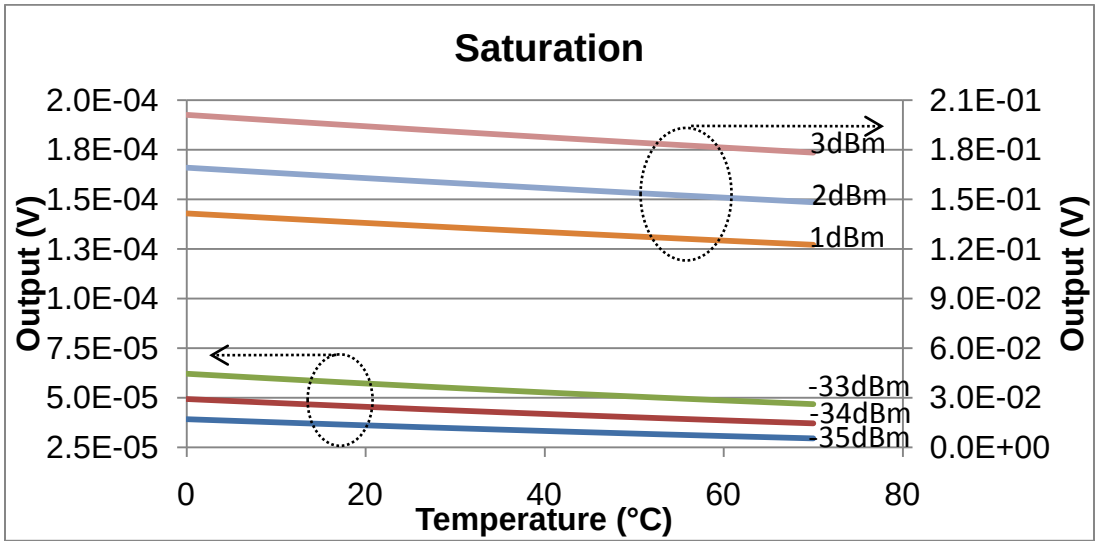
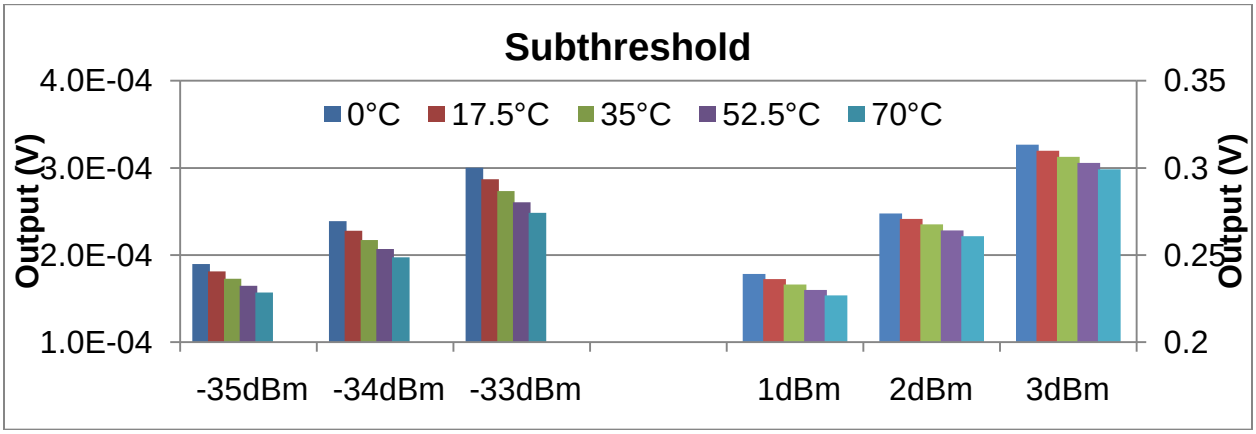


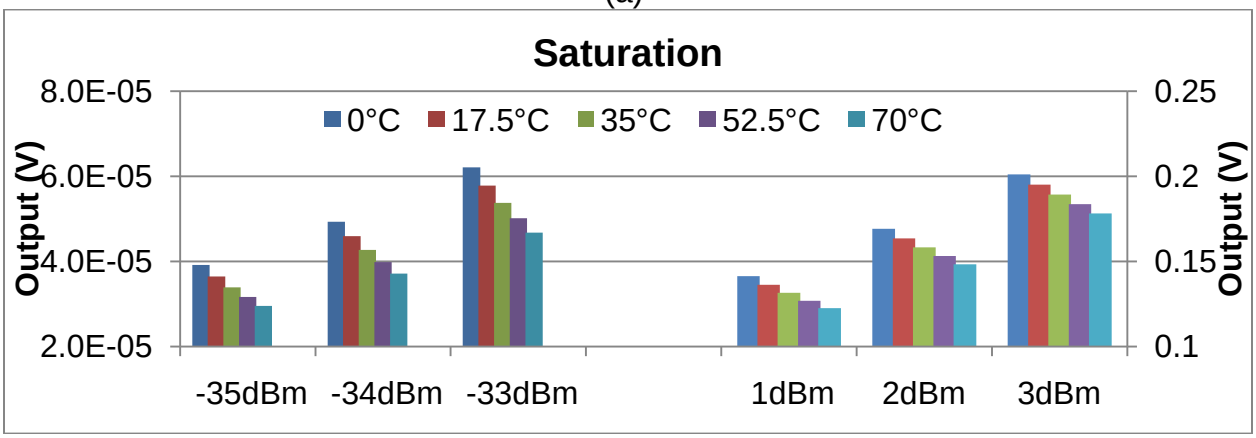
Figure 3-14. Saturation response vs. temperature

These plots show the response of the detector for small input signal levels (-35dBm to -33dBm) and large signal levels (1dBm to 3dBm) over the commercial temperature range [0°C, 70°C]. In subthreshold, as expected from the detector's output theoretical equations (2-9) and (2-12), temperature is more dominant for smaller input levels compared to larger input signal levels. For instance, when the input level is 2dBm, the output varies between [262mV, 276mV]; for 1dBm, the corresponding output varies between [228mV, 241mV]. Since there is no overlap between the two ranges, the

detector can predict signal level with an accuracy that is better than 1dB. Another way to represent the previous data is shown below.



(a)



(b)

Figure 3-15. Detector's response vs. temperature

As seen in the plots above, the detector accuracy over temperature is set by variations in smaller input signal levels. In subthreshold, the accuracy of the detector is ±.5dB; in the saturation region, the error is larger amounting to ±.65dB. Additionally, the accuracy of the detector is highly dependent on the operating point of the rectifying transistor.

Figure 3-16 summarizes the temperature effects depending on the operating region of the rectifying transistor. The graph shows values for how many parts per million per degree Celsius the detector's output changes. This is calculated by dividing

the difference of the detector's output at the two extreme temperatures (0°C and 70°C) by the detector's output at the center of that range. This value is then multiplied by 10^6 to convert it to *ppm* and then divided by the temperature range. The equation below summarizes how the detector's response temperature coefficient was calculated

$$x\,{}^{ppm}/_{°C} = \frac{out(0°C) - out(70°C)}{out(35°C)} * \frac{10^6}{70°C}$$

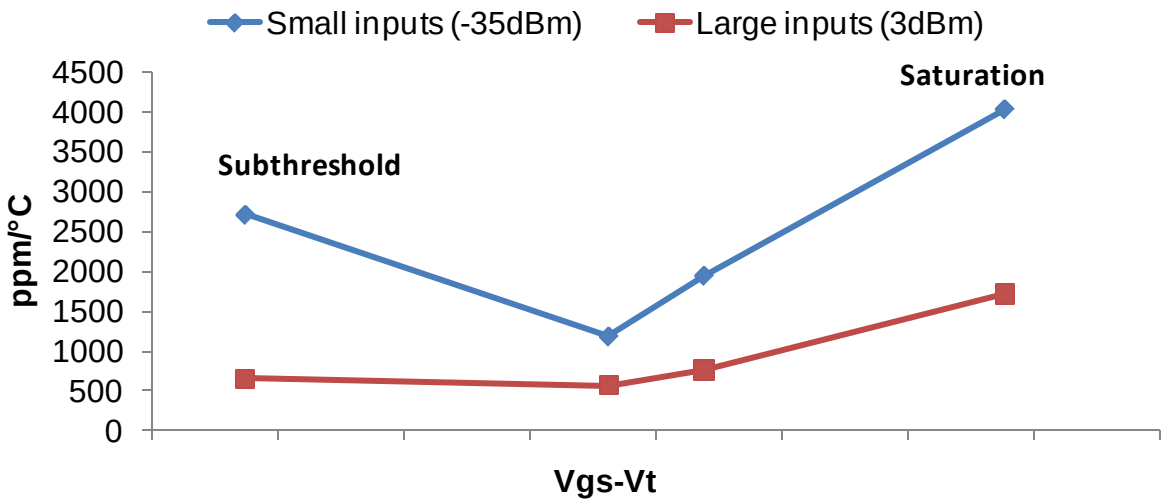


Figure 3-16. Temperature coefficient of the detector's response as function of the overdrive voltage

Figure 3-16 shows that the accuracy of the detector is set by lower amplitude inputs. It also confirms that the error in saturation is higher than the error in subthreshold as seen in Figure 3-13 compared to Figure 3-14. Interestingly, when operating around zero overdrive voltage whether in saturation (moderate inversion) or subthreshold, the detector's dependence on temperature decreases.

Ad hoc solutions

Finding the optimum operating point which minimizes temperature effects is one solution. A set of publications introduce ad hoc solutions to further improve the accuracy of the amplitude detector. [22] and [41] adopt minor modifications to the original Meyer

topology; nevertheless, the detector's accuracy is improved only for specific conditions. In Meyer's Peak detector [22], the output dependence on temperature can be eliminated by modifying the replica such as $I_2=2*I_1$ and $R_2=R_1/2$ when the input is a square wave. [41] shows that mismatching the current sources between the rectifying and the replica of the detector such as $I_1/I_2=sqrt(\beta)$ will improve the temperature performance of the reported detector topology. β is the portion of the input fed to the replica circuit set by the resistive divider circuit in that detector. Unfortunately, this improvement is only effective in the linear region (higher input signal levels) of the detector.

A possible workaround consists of designing a current mirror whose temperature coefficient cancels the temperature coefficient associated with the rectification process. Nevertheless, as seen in Figure 3-16, the detector's temperature coefficient changes with the input signal level. Consequently, this solution remains limited and can be applied in specific conditions only.

Temperature sensor

[38] suggests that in addition to employing the feedback method, more accuracy is possible by using an additional temperature sensor. If the temperature of the circuit is known, post processing of the detector's output can be done to estimate the RF input with more accuracy. This is the same strategy that is employed in commercial solutions such as standalone power sensors, where calibration data is stored in non-volatile memory and is used in combination with a temperature sensor to achieve a dynamic range in excess of 90dB [42].

Interestingly, the amplitude detector has implicit temperature sensing capability. [43] uses a non-linear mapping from a multitude of detectors to predict specifications

such as P1dB, IIP3, and noise figure within a 1dB error. This BIST methodology can account for temperature variations by using one of the detectors as a temperature sensor. So, in summary, [43] reports that non-linear mapping of several detectors' response can predict specifications of a DUT in the presence of process and environmental variations as the non-linear mapping provides an auto-calibration. In order for this method to be successful, the alternate test circuits (detectors) have to produce a measurement that can be strongly correlated to the specifications under test while accounting for environmental and process variations.

The highest levels of accuracy in amplitude detectors can be achieved by including a temperature sensor. [38], [42], and [43] all include a temperature sensing capability and apply correction factors to the amplitude detector using post processing methods.

Process Variations

The previous section dealt with temperature effects on the detector and offered some solutions to minimize those effects. Semiconductor devices also suffer from physical variations in addition to the aforementioned environmental variations. Physical variations are caused by changes in the semiconductor process since it's impossible to replicate the level of control over the process from one wafer lot to the next or wafer corners as well. The Meyer topology was preferred over other topologies since it provides superior performance compared to other detector structures of the same family type. Similar to temperature effects, process variations in the Meyer topology are also expected to be lower than the structure shown in Figure 3-11. The previous section discussed how severe temperature variations can affect that topology because its output depended directly on the current through the rectifying transistor when biased in

subthreshold. In addition to being highly dependent on temperature, the DC current in that structure is also heavily susceptible to process variations which also affect the accuracy of the detector.

[44] which uses the same structure as the one shown in Figure 3-11, derives the output of the detector when it's biased in the saturation region.

$$Vout = \frac{\mu C_{ox}}{4}\frac{W}{L}R * A^2 \tag{3-18}$$

Even in the saturation regions, variations in the topology which uses a resistor are higher than variations in Meyer topology. Equation (3-18) shows that the Figure 3-11 topology is susceptible to variations in the term *"$\mu C_{OX}W/L$"* as well as variations in the resistor R, while the Meyer topology is affected only by variations in the *"$\mu C_{OX}W/L$"* term. Therefore, first order compensation to process variations is also intrinsic within the Meyer detector topology in the saturation region.

Nevertheless, process variations are more severe with deeply scaled process technologies. As predicted by Pelgrom's models [45], the level of mismatch between two elements is inversely proportional to the size of the elements.

$$\sigma^2(\Delta P) = \frac{{A_P}^2}{WL} + {S_P}^2{D_x}^2$$

Where $\sigma^2(\Delta P)$ is the variance of the difference of parameter P, A_P and S_P are constants, W and L are the dimensions of the elements, and D_X is the distance between the elements. Moreover, this model only applies to intra-die variation. When inter-die variations, which include dies from different wafers or lots, the variance of the circuit is much larger and size is no longer critical. For the detector, as long as the size of the rectifying transistor is few times larger than the minimum size transistor in the process, the standard deviation of the detector's response reaches a minimum and size of the

rectifying transistor becomes irrelevant. These statements are summarized in Table 3-1 which shows Monte Carlo simulations results when the detector is stimulated with a 0dBm input. These Monte Carlo simulations were implemented using a “Skew” file provided by the foundry “IBM” which defines the statistical variation of the process parameters in the technology. The size of the detector was varied and the values shown in Table 3-1 are normalized to the minimum size transistor in the process. For all sizes, the detector was biased in the saturation region while maintaining the same overdrive voltage across the rectifying transistor.

Table 3-1. Monte Carlo simulations of different normalized transistor sizes

Size	Std Deviation mismatch only	Std Deviation mismatch + process
1x	0.8%	5.5%
4.25x	0.4%	3.2%
42.5x	0.1%	3.2%

The table shows that when only intra-die (mismatch only) variations are considered, only minor spreads of the detector’s response are produced and the detector is expected to be accurate. It is also obvious that the variations are proportional to the detector’s size as predicted by Pelgrom’s equation. However, when inter-die (mismatch + process) variations are included in addition to the intra-die variations, the distribution of the detector’s response has a much higher standard deviation. The standard deviation of the variations is highest for the minimum size transistor, but it seizes to decrease as the size of the rectifying transistor reaches a certain threshold as seen in the table above.

Process variations are also dependent on the operating region [46]. In this light, variations are presented across the different operating regions. From the theoretical equations derived for the detector’s output in different operating conditions, it was

predicted that subthreshold detection is less sensitive to process variations than saturation detection. Moreover, it is expected that detectors experience more variations for low input power levels compared to higher input power levels. The following figures show Monte Carlo simulations of the detector including process and mismatch variations (worst case condition).

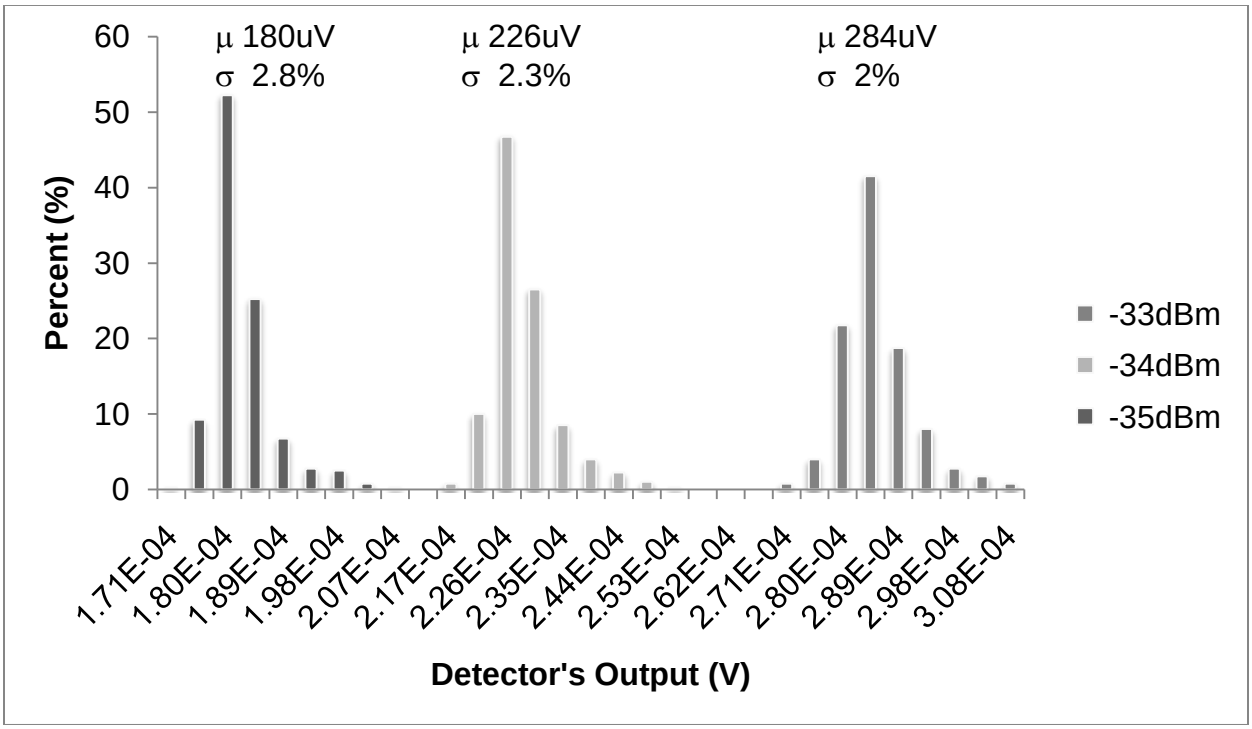


Figure 3-17. Variations of detectors response in the subthreshold region

μ in the plot above refers to the mean value, and σ refers to the standard deviation. It is seen that in the subthreshold region, the detector has an accuracy that is better than ±.5dB. The plot shows the response of the detector when stimulated respectively with the input power levels -33dBm, -34dBm, and -35dBm. For each input power level, the detector's response varies in a limited range which does not overlap with the other ranges that are associated with the adjacent power levels.

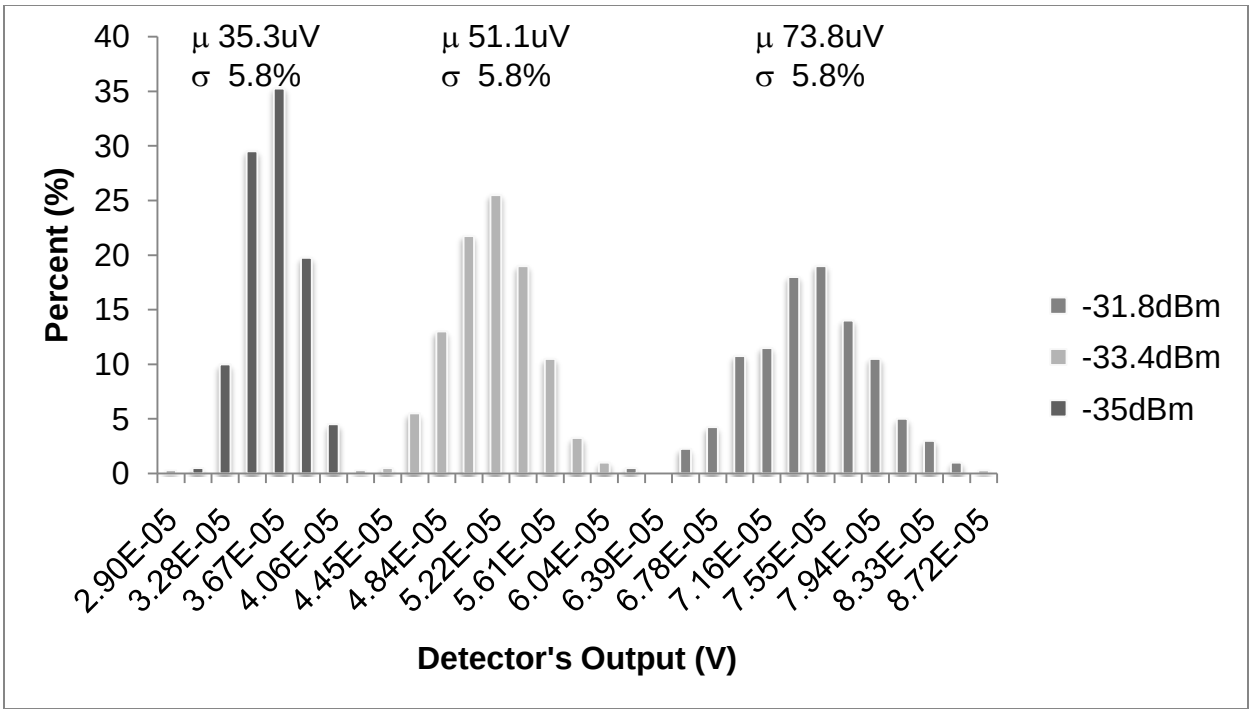


Figure 3-18. Variations of detectors response in the saturation region

In the saturation region, the accuracy of the detector is worse compared to the subthreshold region. The Monte Carlo plot above shows that the spacing required for adjacent power levels to achieve no ambiguity when predicting in the input power level is ±.8dB. Bear in mind that this value is dependent on the rectifying transistor's overdrive voltage.

Calibration

DC offset

The most significant variation in the MOSFET amplitude detector is a DC offset which arises between the rectifying part of the detector and the replica. [21], [44] states that this offset is constant and remains independent of the high frequency input. Hence, this dictates a one shot DC calibration for each detector to cancel the DC offset. Threshold voltage variations are expected to be the main cause of this offset which can be minimized by using triple well transistors [21].

Reference detector

As discussed previously, first order calibration of process variation is built-in the topology. When this first order compensation is not enough because higher levels of accuracy are required, more elaborate calibration methods are necessary. The simplest option is to include an extra detector in the wafer whose input can be probed so that it can be used to calibrate the remaining detectors since intra-die variations are small. The standard deviation of the detector's response is.7% when only intra-die variations are considered as seen in Figure 3-19 compared to 5.8% seen in Figure 3-18 when inter-die variation are taken into account as well. When a detector is calibrated and used as a standard, the accuracy of other detectors within the same die will become ±.1dB instead of ±.8dB when only mismatch is considered. Furthermore, the number of additional detectors used for calibration can be increased and placed in various wafer corners if intra-die variations are large.

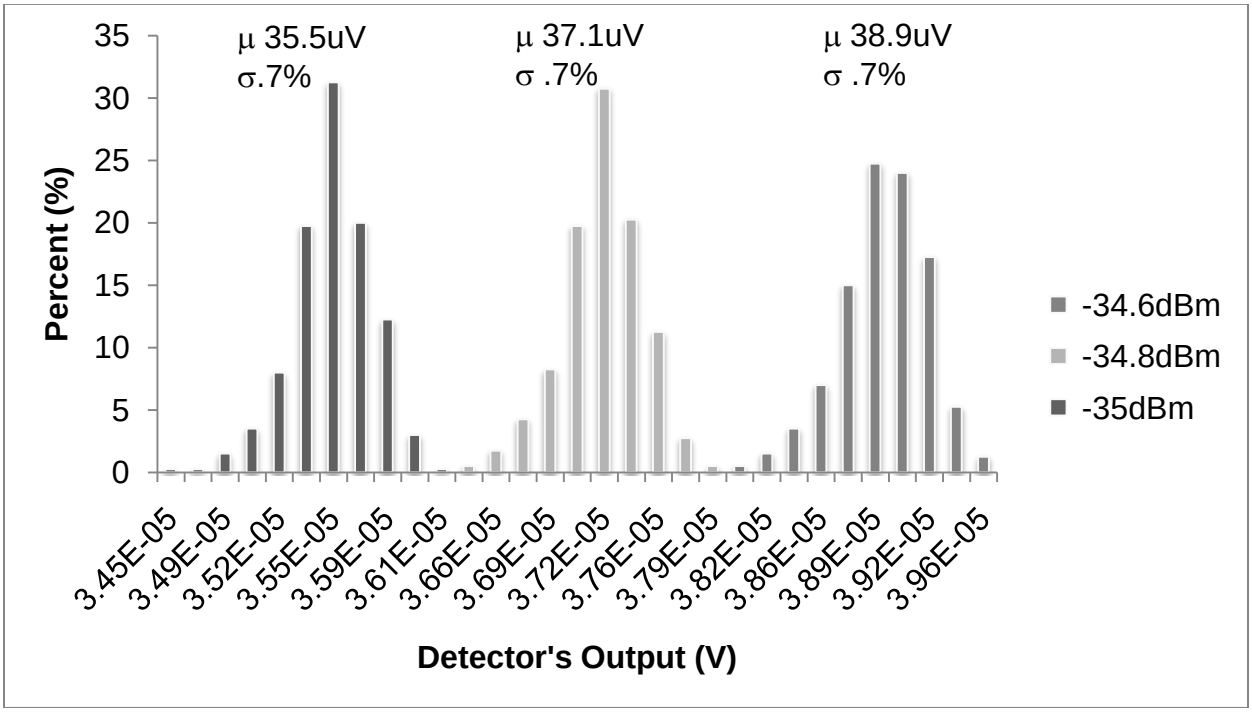


Figure 3-19. Monte Carlo in the saturation region considering only intra-die variations

Statistical methods

In deeply scaled process technologies, process variations become accentuated and the previous calibration methods might not be sufficient. [47] reports a promising method that calibrates detectors to higher accuracy levels. In addition to one detector which can be calibrated directly with an RF signal, the method relies on DC signals only for calibrating the remaining detectors. It uses statistical analysis to map the DC-to-DC response into the RF-to-DC response. In [47], the detector reaches accuracy levels better than 1% for signal levels higher than 200 mV.

[32] also uses statistical analysis to account for process variations; however, it calibrates the DUT and the detectors simultaneously. The method measures a number of samples using both conventional and the alternate test methods; then, it hinges on a statistical training which correlates the alternate test method to the actual specifications as it uses detectors whose outputs are directly correlated to the specification space.

On the other hand, [43] is not concerned whether the detector's response is directly linked to the specification space; it just identifies the detector as an implicit feature extractor and uses statistical mapping to extract further information from the alternate test measurement space. To guarantee strong correlation between the alternate test measurements and the DUT specifications, it uses a multitude of detector types. Bipolar detectors are used because of their current's exponential relationship in addition to Mosfet detectors for their square law relationship; however, this limits the method's feasibility to BiCMOS process only as it was originally proposed in [43]. Actually, the method can be adapted to standard bulk CMOS process knowing that MOSFET detectors can be biased in different regions to obtain exponential relationship in subthreshold and square law in saturation.

[29] optimizes the test pattern generation instead of using a multitude of detectors to find signals which can stimulate the alternate test method to achieve the strong correlation between the alternate test space and the specification space. This method's algorithms render it immune to process and environmental variations.

All these statistical methods rely on a fault dictionary that is built either from simulations or conventional measurements when possible; then a mapping engine can estimate the specifications of the DUT from the alternate measurement space after training. The alternate test methods are immune to process and environmental variations as long as there are strong correlations between the alternate test measurement space and the DUT's specification space.

Yield impact

Calibration benefits are not only limited to achieving higher levels of accuracy; another benefit is to detect catastrophic faults in the alternate test method that can be caused by random defects. Catastrophic faults in the detectors are critical since they directly impact the yield as they give a false reading; although this yield impact is expected to be low since the area occupied by the BIST circuitry is smaller compared to the DUT. Calibration methods have an inherent capability of detecting most failures. For example, measuring the DC voltage at the output without any RF stimulus can be used to locate catastrophic failures such as shorts and opens. Applying a low frequency input to the detector's output through a bias tee will have high fault coverage except failures between the DUT and the detector's input such as open. All the other calibration methods can also be used as well to detect catastrophic failures. At the very least, if failures are still a concern and yield loss is expected to be high, the BIST method can be used for binning the DUT to minimize test escapes faster in an initial wafer test.

DUTs can be sorted into pass, fail, and a third category which requires further test because of inconclusive BIST results.

Dynamic Range

In general, for CW signal, dynamic range in amplitude detectors is limited in the higher end by transistor breakdown. Unlike other active devices where compression point such as P_{1dB} puts a limit to the dynamic range, amplitude detectors are not affected by compression since they work through the exploitation of non-linearities of the rectifying devices. However, if the input is not a CW signal, detection accuracy depends on the input signal levels as discussed in the previous section. The lower end in the dynamic range of detector (sensitivity) can be limited by two mechanisms. The first factor which is inherent to the detector itself is noise sources such as shot noise, and flicker noise. The second limitation that affects the sensitivity measurements is the precision of the digital multi-meter (DMM). When the DMM limits the measurement capability, subthreshold detection is advantageous compared to detection in the saturation region. From the equations in Table 2-1, subthreshold detectors have a higher RF-to-DC proportionality coefficient than saturation detectors. For small signal levels, the saturation detector will have a DC output higher than the square-law-subthreshold detector only if $V_{gs} - V_t < nV_T$ when equations (2-5) and (2-12) are compared. This condition is not possible since the inequality means that the saturation detector is biased in moderate inversion. For higher signal levels, by comparing (2-5) and (2-9) and making some assumptions such neglecting the logarithmic term in equation (2-9), the saturation detector can have a higher DC output only when $A > 4(V_{gs} - V_t)$. This condition occurs only when the input signal is very large (breakdown),

or when the rectifying transistor is biased near subthreshold. Thus, from the discussion above, subthreshold detectors have a higher DC output for a given RF input level compared to saturation detectors. This makes them more sensitive compared to saturation detectors when measurements are limited by the precision of the DMM.

Summary

In this section, the trade-offs of detection in each operating region are recapitulated. The first section of this chapter showed that subthreshold detectors operate in two modes which limit their RMS detection dynamic range. The RMS detection range in the saturation region was larger as well as tunable as shown by inequality (3-4). On the other hand, subthreshold operation can be useful when power consumption needs to be minimized. However, the settling time of the detector's output is slow due to the low bias currents. Therefore, this detector cannot be used for high symbol rate applications. The frequency response of the detector was also discussed to show that the detector is suitable for mmWave BIST. Moreover, by comparing the equations in Table 2-1 as well as the simulation results in the previous sections, subthreshold detectors are more immune to environmental and process variations. Calibration methods to account for these types of variation were also reviewed. Finally, factors that limit the dynamic range were also reported. The benefits associated with each operating region of the detector are summarized in the table below.

Table 3-2. Comparing saturation and subthreshold detection

	RMS dynamic range	Power consumption	Video Bandwidth	Immunity to variations	Sensitivity
Saturation	+		+		
Subthreshold		+		+	+

CHAPTER 4
ALTERNATE DETECTOR TOPOLOGIES

MOSFET Detector Subthreshold Crossover Region

Introduction

As stated previously, the amplitude detector is not ideal; Linear or square-law behavior is only an approximation of the detector's actual response. Nonetheless, there exist some techniques to increase the detector's precision. Feedback loops can be used to increase the accuracy of peak detectors (Linear detection) [48], [49]. However, feedback loops which operate at the input signal's frequency severely restricts the bandwidth of the detector. [33] uses an open loop circuit with two mismatched detectors and some post processing at DC to minimize the detector's error. Nonetheless, this technique works for large signal levels only. For applications with large dynamic range, it is desirable to maintain one type of detection (RMS or Peak) over a wide range of signal levels. This section deals particularly with the subthreshold crossover region. Two topologies that minimize this region are introduced in this section.

Type II Detector

The subthreshold MOS amplitude detector, like the bipolar detector, has two separate detection modes; a linear detection mode for higher amplitudes and a square-law mode for lower amplitude input levels. Additionally, there exists a large crossover region where neither square-law or linear fit is accurate. [27] developed a technique that reduces the range of this crossover region in bipolar transistors by minimizing the effect of an error term in the linear mode. This same technique can be used for MOS transistors in the subthreshold region. Equation (2-9) shows that the detector's DC output is not exactly linearly proportional to the RF input's amplitude. It shows a

logarithmic term that is dependent on the input's amplitude which causes deviations from linear proportionality. Nevertheless, this error value is compressed as it is logarithmic. According to [27] which reported this method in bipolar detectors, this error is within 10% for inputs larger than 100mV. As seen in Figure 4-1, this technique works such that the DC output is referenced to a replica circuit whose input is a fraction of the RF input. This is different from the traditional Meyer detector where the replica has no RF input.

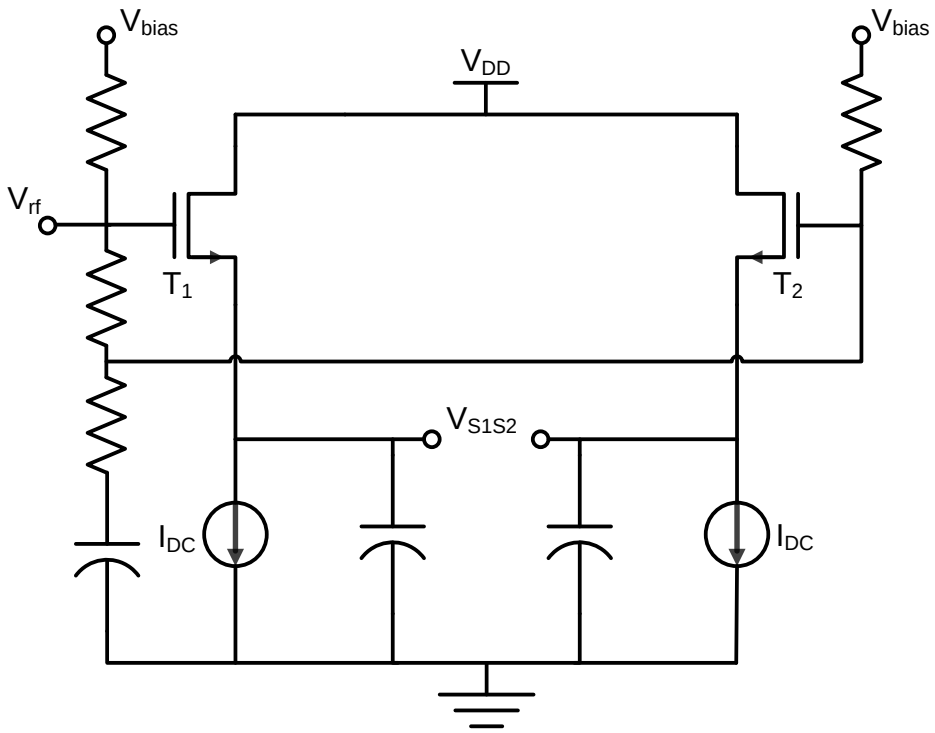


Figure 4-1. Type II MOS detector

The output of this MOS detector, named here type II, in subthreshold is given in the following equation

$$V_{s1s2} = (1-\beta)A + \frac{nVT}{2} * ln(\beta) \quad (4\text{-}1)$$

The term β is the fraction of the input stimulating the reference replica circuit. As can be seen in the equation above, the logarithmic term is no longer dependent on the input

signal's amplitude; this effectively makes the detector linear. Furthermore, for smaller RF input amplitudes. The output equation becomes

$$V_{s1s2} \approx \frac{(1-\beta^2)A^2}{4nV_T} \tag{4-2}$$

In the saturation region, if this technique is used, the type II detector output becomes

$$V_{s1s2} = \frac{1}{4(Vgs2 - Vt2)} * (1-\beta^2)A^2 + \cdots \tag{4-3}$$

Type III Detector

Another circuit that minimizes the subthreshold crossover region is presented in this dissertation. Unlike the type II detector that linearizes the subthreshold-linear mode, this circuit extends the subthreshold-square-law range. The circuit shown in Figure 4-2 averages the DC drain currents in the transistor pair T_{11} and T_{12}.

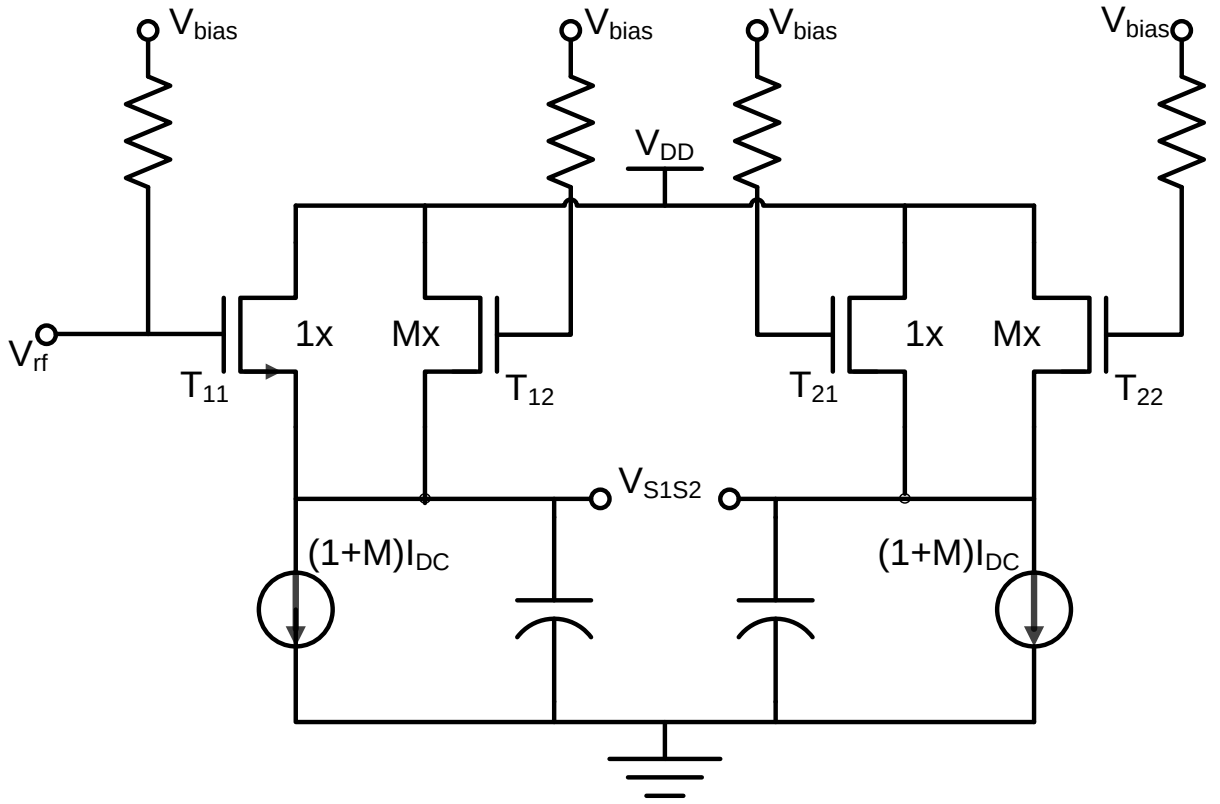


Figure 4-2. Type III MOS detector

As seen in Figure 4-2, only transistor T_{11} is stimulated with an RF input. In the subthreshold region, the following equations result

$$I_{DC.T11} + I_{DC.T12} = I_{DC.T21} + I_{DC.T22} \tag{4-4}$$

$$I_{d0}e^{\frac{V_{gs1}}{nV_T}} * I_0(b) + MI_{d0}e^{\frac{V_{gs1}}{nV_T}} = (1+M)I_{d0}e^{\frac{V_{gs2}}{nV_T}}$$

$$I_{d0}e^{\frac{V_{gs1}}{nV_T}} * \frac{I_0(b)+M}{1+M} = I_{d0}e^{\frac{V_{gs2}}{nV_T}}$$

$$e^{\frac{V_{S1S2}}{nV_T}} = \frac{I_0(b)+M}{1+M} \tag{4-5}$$

where *M* is the factor which relates the size of transistor T_{12} to transistor T_{11}, $b=A/nV_T$, and $I_0(b)$ is the 0th order modified Bessel function

$$I_0(b) = \sum_{k=0}^{\infty} \frac{\left(\frac{b^2}{4}\right)^k}{(k!)^2}$$

$I_0(b)$ can be approximated for small signal levels (square-law) such as

$$I_0(b) = 1 + \frac{b^2}{4}.$$

And the approximation used for $I_0(b)$ for large signal levels (linear-subthreshold) is

$$I_0(b) = \frac{e^b}{\sqrt{2\pi b}}.$$

For type III detectors, when $I_0(b)$ is approximated, the quantity $e^{\frac{V_{S1S2}}{nV_T}}$ in equation (4-5) deviates from the ideal value by

$$error_{III} = \frac{\left(\frac{approx\left(I_0(b)\right)+M}{1+M} - \frac{I_0(b)+M}{1+M}\right)}{\frac{I_0(b)+M}{1+M}}$$

$$error_{III} = \frac{approx\left(I_0(b)\right) - I_0(b)}{I_0(b)+M} \tag{4-6}$$

Whereas, the error for type I (Non-modified Meyer Topology) detectors, the quantity $e^{\frac{V_{S1S2}}{nV_T}}$ from equation (4-5) deviates from the ideal value when approximation is used by

$$error_I = \frac{approx\left(I_0(b)\right) - I_0(b)}{I_0(b)} \tag{4-7}$$

Therefore, by comparing equation (4-6) and (4-7), the error in type III detectors is always smaller than type I detectors.

Comparison Between the Three Types of Detectors

A numerical analysis was done using Matlab to compare the three types of detectors. The following table shows the theoretical and approximated output values V_{S1S2}/nV_T for each detector. For type II detectors, the value of β is set as $\beta = .5$; and for type III detectors, the value of *M* was set to *M=1*.

Table 4-1. Value of V_{S1S2}/nV_T for the three types of detectors

	Type I	Type II	Type III
Theoretical	$ln\left(I_0(b)\right)$	$ln\left(\frac{I_0(b)}{I_0\left(\frac{b}{2}\right)}\right)$	$ln\left(\frac{I_0(b)+1}{2}\right)$
Square-law approx.	$\frac{b^2}{4}$	$\frac{3b^2}{16}$	$\frac{b^2}{8}$
Linear approx.	$b - ln\left(\sqrt{2\pi b}\right)$	$\frac{b}{2} - ln\left(\sqrt{2}\right)$	$b - ln\left(\sqrt{8\pi b}\right)$

The Linear approximation for type I and type III in this table is not exactly linear; a best fit linear regression is used to linearize the approximations further. Deviations of these approximations from the theoretical values are computed and plotted in Figure 4-3 as a function of the input level *b*. The errors are highest in the crossover region which is defined as the range when the detector's output deviates by 8% from the linear or square-law approximations [27].

This section showed how the crossover region varies for each type of detector. Besides having a small crossover region, parasitics at the input of type III detectors are lower compared to type II detectors.

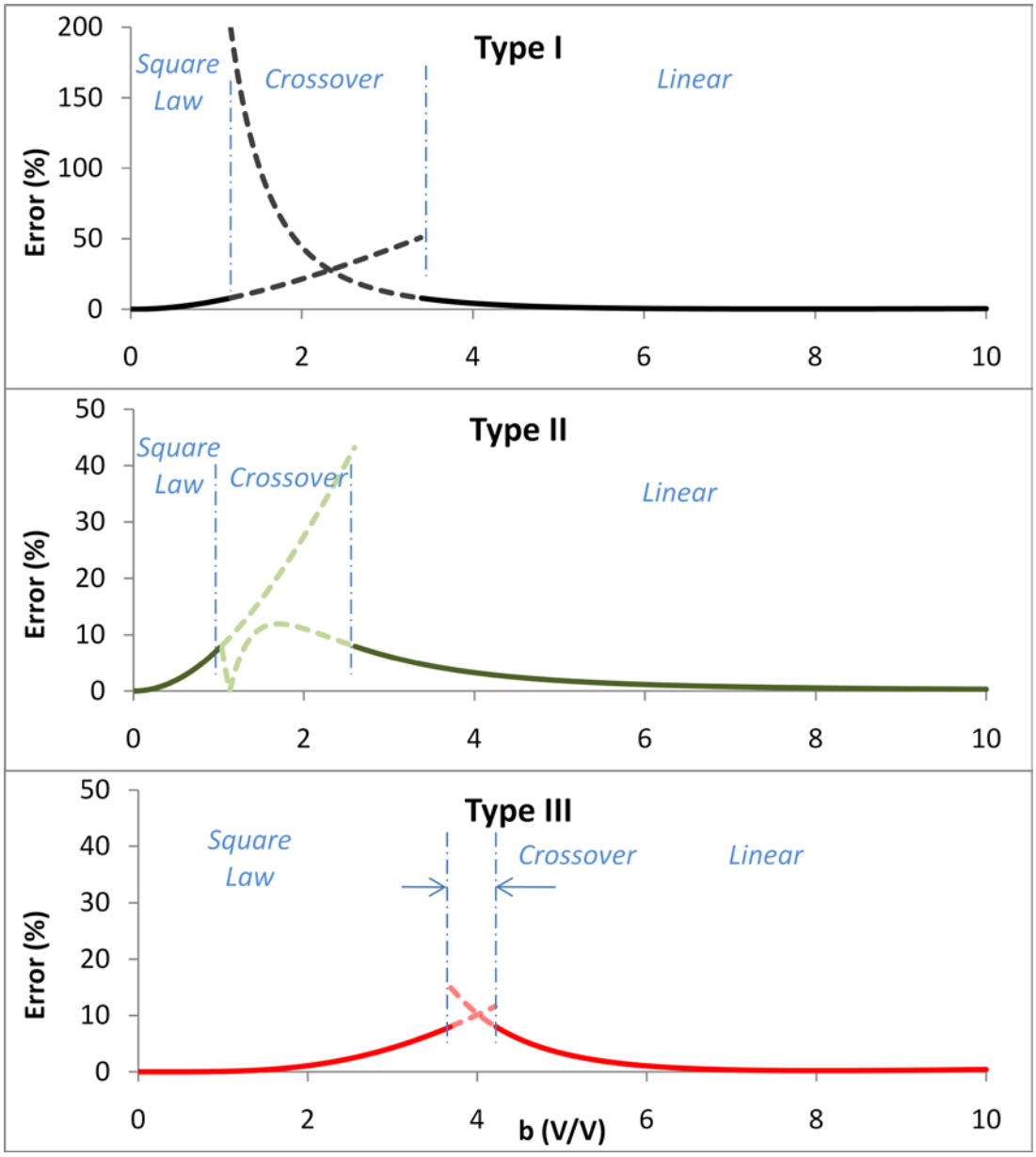


Figure 4-3. Error of approximated detector's output relative to the theoretical value

Additionally, the type III detector has a faster discharge rate when compared to the other two types. This is useful when lowering the low pass filter capacitance C, increasing the aspect ratio of the rectifying transistor, or increasing the bias current are not possible options due to the tradeoffs linked to each solution. The type III detector increases the speed of the detector using a somewhat hybrid approach of increasing the aspect ratio and increasing the bias current without the tradeoffs associated with

each approach. The type III detector increases the transistor count without increasing the loading effects on the DUT; it also increases the bias current without changing the operating point of the rectifying transistor. Therefore, this makes the discharge rate faster, which is important for applications with high symbol rates. This is especially beneficial in subthreshold since the video bandwidth is low in that region. The benefits of the Type III detector are not limited to what was discussed above. The next section will introduce advantages of using the type III detector in the saturation region.

Type III Detector in the Saturation Region

As discussed previously, square law response is desirable in many applications where the input is not a simple CW signal. There has been a wide interest in the industry to design detectors with extended RMS dynamic range. Many circuit techniques were developed to replace calorimetric detectors which are inherently square-law devices capable of working properly even for higher signal levels. The calorimetric detectors are not suitable for BIST from which arise the need to develop alternative solutions. [50] describes how the square law dynamic range of a diode can be extended by replacing it with a diode stack which consists of several diodes connected in series. The patent [50] explains that the response of the detector changes with the input signal levels because of an effect called the diode's junction capacitance modulation. When employing several diodes in series, this junction capacitance is decreased, thus, minimizing the amount of modulation. [51] presents a more sophisticated detector which combines diodes stacks with resistive attenuation network to achieve an even larger square law dynamic range. The use of diode stacks in addition to resistive attenuators is justified since high attenuation values cannot be

obtained in integrated circuits; parasitic coupling such as substrate leakage sets the limit of the maximum possible attenuation to 30dB or 40dB.

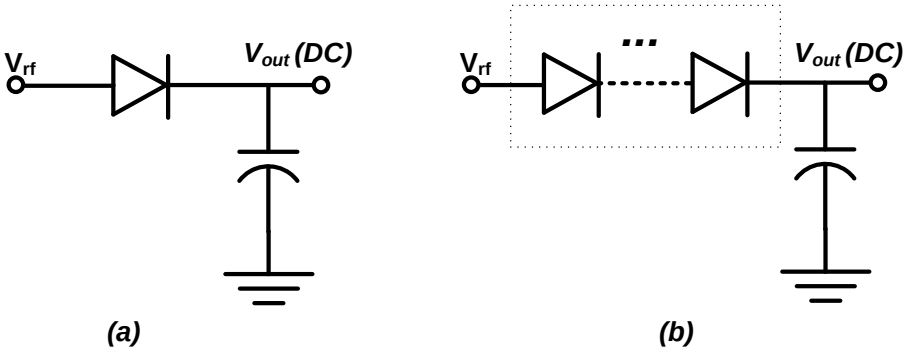


Figure 4-4. (a) Diode used for RMS detection, (b) Diode stack with increased RMS dynamic range

Using diode stacks effectively increases the square law dynamic range. Nevertheless, a method that is compatible with CMOS processes where high performance diodes are not readily available is required to extend the RMS dynamic range. Actually, square law detection is possible in MOS transistors when biased in the saturation region. Hence, a square law detector can be obtained by implementing the topology shown in Figure 4-5.

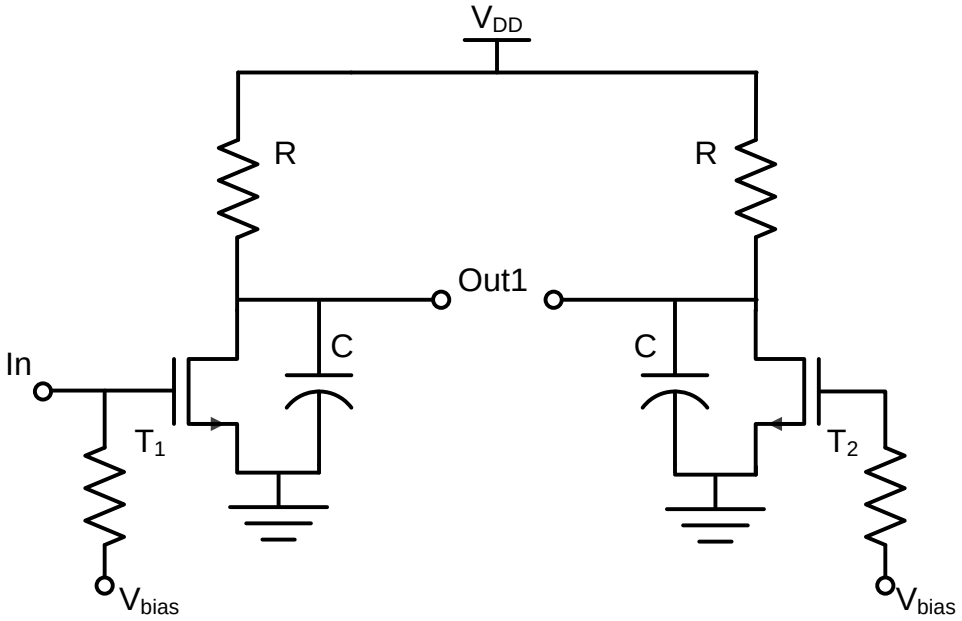


Figure 4-5. Detector using resistor

The output of this topology in the saturation region is

$$Vout = \frac{\mu C_{ox}}{4}\frac{W}{L} R * A^2$$

However, this topology's accuracy is heavily reliant on the attributes of the resistor *R*. More advanced detector topologies were developed to circumvent this issue. The MOSFET Meyer detector is more robust because it uses a current source instead. On the other hand, once a current source is used, the Meyer detector implements square law only up to a limited range of power levels as discussed in the previous chapters. In the saturation region, an inequality was derived to estimate the range of amplitudes for which the detector continues to exhibit square law response

$$\sum {A_i}^2 < 8(|Err| - Err^2){V_{ov}}^2$$

A_i is amplitude of each frequency tone in the input signal, and *Err* is the maximum acceptable error for deviations from the square law. More information regarding the derivation of this equation can be found in Chapter 3. This inequality shows that the square law range can be extended if the overdrive voltage across the rectifying transistor is increased. Increasing the overdrive voltage is effective only up to certain levels since it is associated with performance trade-offs. When the overdrive voltage is increased, short channel effects become important and process variations are more significant. However, more fundamentally, short channel effects cause the detector to considerably deviate from the square law proportionality. Alleviating problems attributed to short channel effects given a certain bias point is made possible only by increasing the size of the transistor. Nevertheless, this is not desirable since it directly impacts the detector's loading effects on the DUT. Therefore, there is a need to develop methods to extend the detector's square law response dynamic range.

The type III detector discussed in the previous section can extend the dynamic range without increasing the loading effects. Let's derive the detector's output in the saturation region to show how this works. The total DC drain current through transistors T_{11} and T_{12} when a high frequency input is stimulating the detector is

$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(\left(V_{gs1} - V_t\right)^2 + \frac{A^2}{2} + M\left(V_{gs1} - V_t\right)^2\right)$$

The current through the replica circuit is

$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}\left((M+1)\left(V_{gs2} - V_t\right)^2\right)$$

Solving for V_{s1s2} and applying the Taylor series expansion, the detector's output is

$$V_{s1s2} = \frac{1}{4\left(V_{gs2} - V_t\right) * (M+1)} * A^2 + \frac{1}{32\left(V_{gs2} - V_t\right)^3 * (M+1)^2} * A^4 + \cdots$$

The *(M+1)* factor in the denominator of the equation above achieves the same result as increasing the overdrive voltage without the associated trade-off of increased short channel effects. The *(M+1)* factor makes the higher order terms more negligible which in effect increases the RMS detection range. Figure 4-6 evaluates square law response through the calculation of the normalized linearity of the type I detector, increased overdrive type I detector, and type III topology with *M=1* and *M=10*.

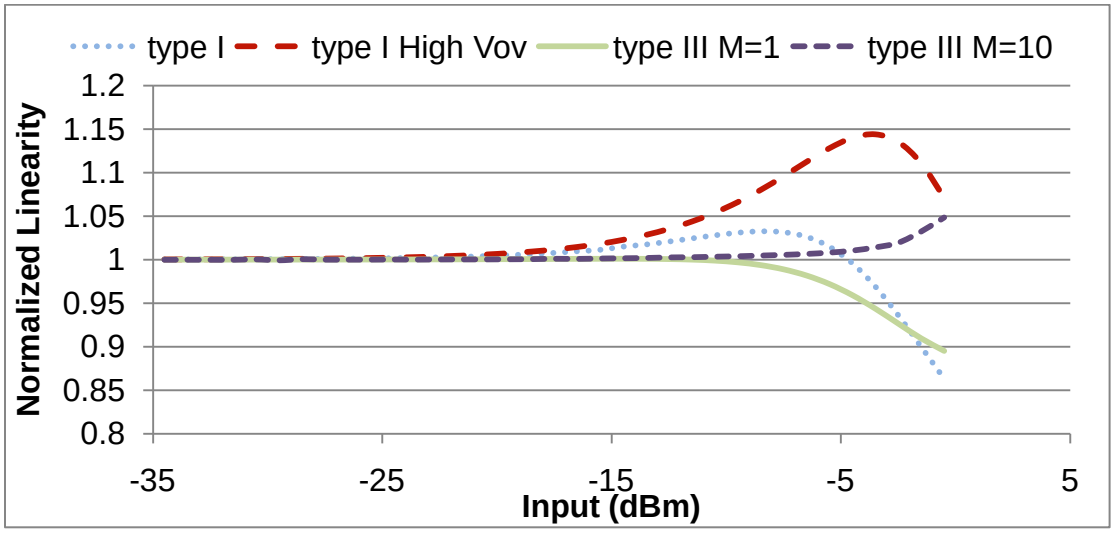


Figure 4-6. Normalized detection slope vs. input level

The following shows how the normalized linearity plot is obtained. The detector is a square law device when its output is

$$Out = A^2/k$$

where *Out* is the DC output of the detector, *A* is the amplitude of high frequency input, and *k* is a constant which depends on the operating conditions of the detector. In the decibel scale, the equation becomes

$$20\log(Out) = 20\log(A^2/k)$$

Since

$$P_{dBm} = 10\log\left(\frac{A^2}{2Z_0 * 10^{-3}}\right)$$

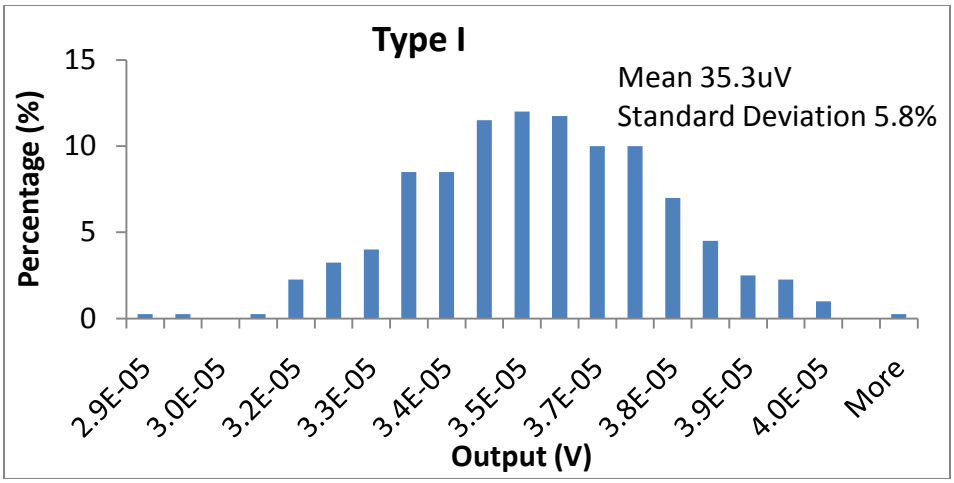
Z_0 is the system impedance. Then,

$$Out_{dBV} = 2 * P_{dBm} - C$$

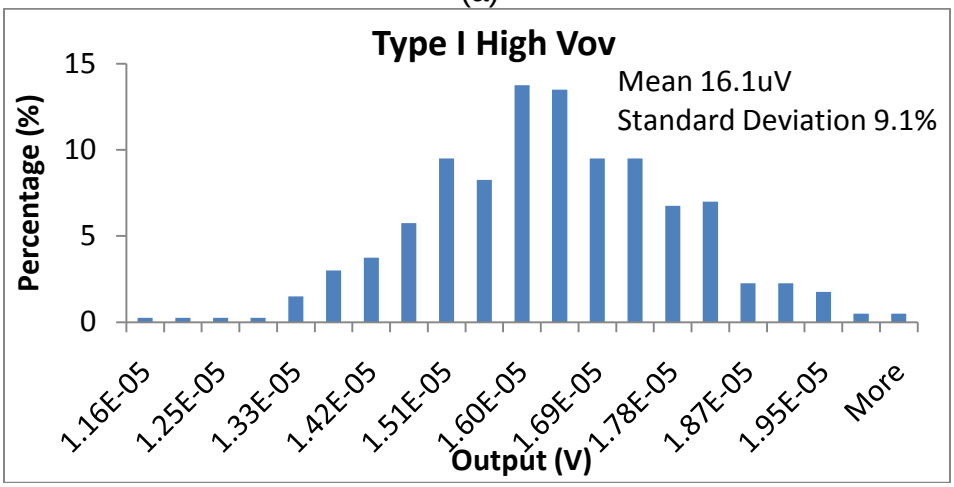
Therefore, when plotting the detector's response in a decibel scale, the slope of the detector's response should be equal to 2 when it's following the square law. The normalized linearity plot above is obtained by dividing the slope of the detector's response in decibel scale over the ideal slope of 2.

Figure 4-6 shows that the type I detector's response deviates from square law linearity by 2% starting around inputs higher than -12.5dBm. When the detector's overdrive is increased, deviation from square law occurs earlier because of short channel effects as the 2% error threshold is reached for signals that are larger than -15dBm. The type III detector with *M=1* conforms to square law linearity until -6.5dBm as seen in the figure above. And, the type III detector with *M*=10 increases the dynamic range further up to -2.5dBm. Additionally, the benefits of this detector are not limited to an increase in the square law dynamic range. Better accuracy compared to increasing the overdrive voltage is possible as seen in Figure 4-7 which shows Monte Carlo simulations. Monte Carlo simulations of type III with *M=10* were omitted since they are

large (σ=16%) relative to the other examples discussed above. The *M=10* example was only introduced to corroborate the theory discussed above which stated that the square law dynamic range can be increased with increasing *M*. Beyond these numbers which indicate the benefits of this topology, the most important asset of the type III detector is the introduction of another design-dimension which enlarges the performance trade-off space. Thus, this topology provides the designer with more freedom to customize and balance the detector's trade-offs depending on the targeted application.

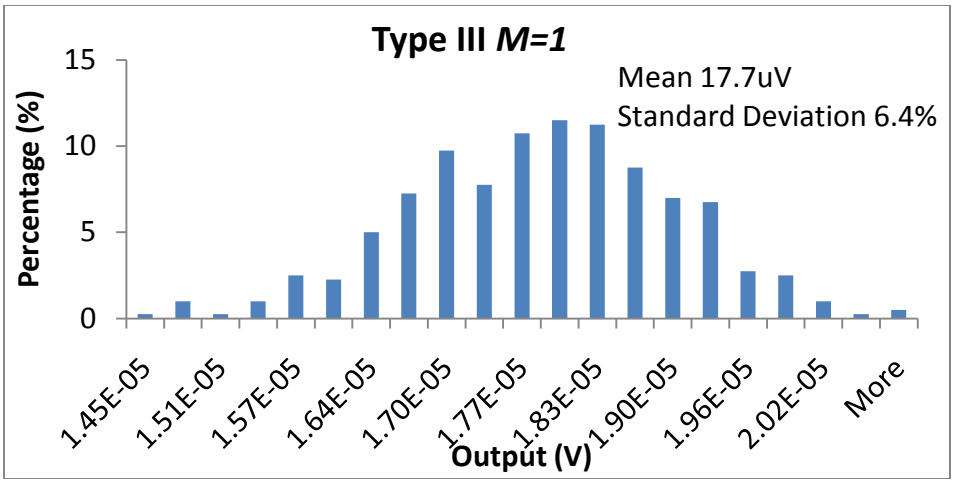


(a)



(b)

Figure 4-7. Monte Carlo simulation for detectors in the saturation region when stimulated with -35dBm input for (a) type I, (b) type I with increased overdrive, and (c) type III detector with *M=1*.



(c)

Figure 4-7. continued

Monte Carlo simulations implemented using the foundry's Skew file in Figure 4-7 show that the type III detector's response has a slightly higher standard deviation compared to the type I detector when biased at the same overdrive voltage. On the other hand, increasing the overdrive voltage leads to a higher sensitivity to process variations compared to using the type III detector as seen in Figure 4-7 (b). Furthermore, temperature simulations of this type III detector showed that the detector have the same accuracy as the type I detector of ±.65dB in the saturation region when both type I and type III are biased at the same overdrive voltage.

Multiple-Regions Detector

As mentioned in the triode section in Chapter 2, the Meyer topology has a very weak response when biased in the triode region. Figure 4-8 shows measurements of the RF-to-DC response in the subthreshold and triode regions for the Meyer topology. The figure shows that the triode response is approximately two decades smaller than the subthreshold measurements.

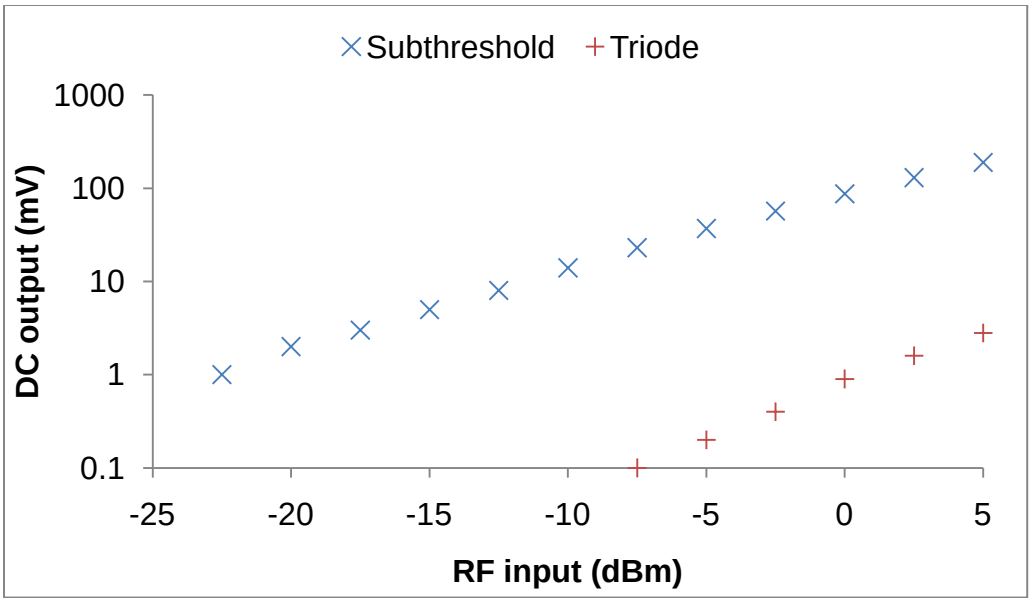


Figure 4-8. Subthreshold response vs. triode response

Looking at the triode drain current equation, the current is quadratically proportional to the voltage V_{ds}

$$I_d = \frac{\mu * C_{ox}}{2} * \frac{W}{L} * \left((V_{gs} - V_t)V_{ds} - \frac{{V_{ds}}^2}{2} \right)$$

Therefore, some non-linearity can be generated if the RF input signal is applied at the drain or at the source. If the RF input is applied to the drain, efficient rectification in subthreshold and saturation is not possible. As a reminder, in the saturation and subthreshold regions, non-linearities in the drain current were created from the current's higher order proportionality to the voltage V_{gs}. Thus, applying the RF input at the source will maintain strong non-linearity for the detector in all regions of operations. The topology of this new detector is shown in Figure 4-9.

Figure 4-10 compares measurements of this new detector and measurements of the Meyer detector when they operate in the triode region. This new detector has much better performance in the triode region. The performance of this new detector is

expected to be similar compared to the Meyer topology in the saturation and subthreshold regions.

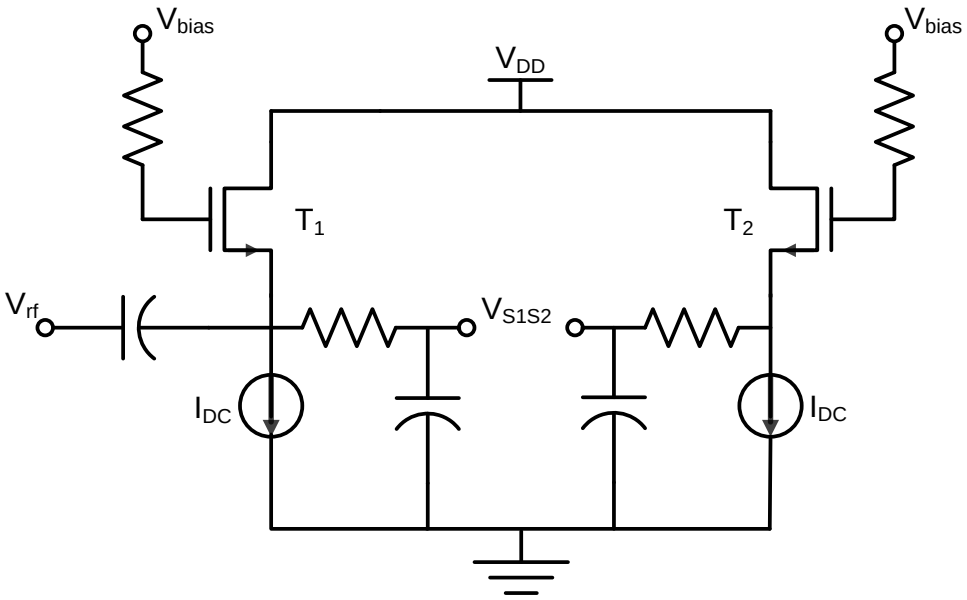


Figure 4-9. New detector – multiple-regions detector

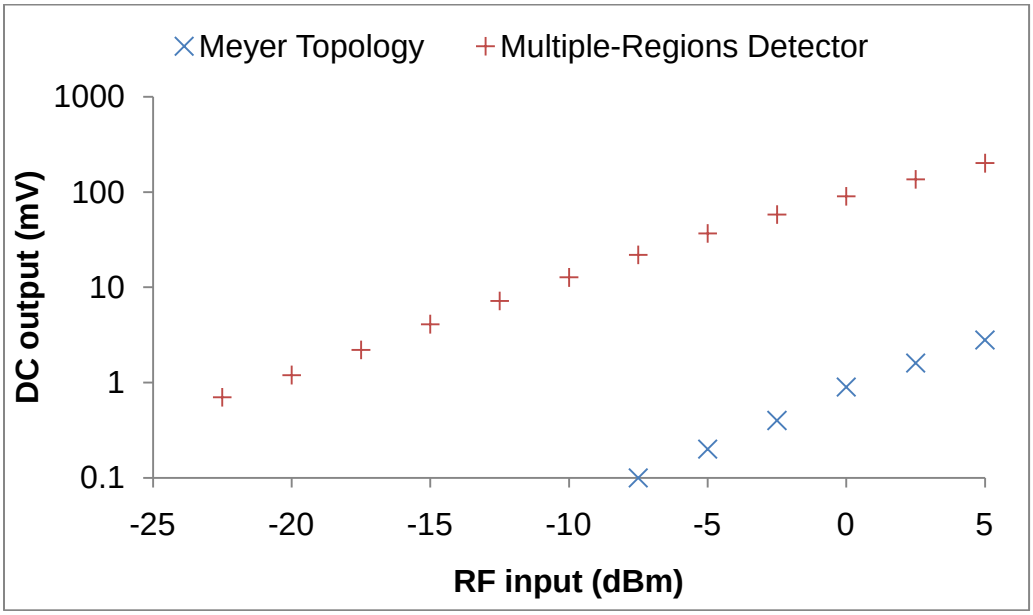


Figure 4-10. Power sweep of the RF input level for the Meyer and new detector in triode

When an RF input *(Acos(ωt))* is stimulating this detector, the drain current for the saturation region and the subthreshold detectors is respectively

$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{gs} - V_t - Acos(\omega t)\right)^2$$

$$I_d = I_{d0} * e^{\frac{V_{gs} - V_t - Acos(\omega t)}{nV_T}}$$

These equations are almost the same as the Meyer detector equations with one minor difference; The RF input amplitude is negative since it is applied at the source instead of the gate of the rectifying transistor. These two equations can be rewritten such as

$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{gs} - V_t + Acos(\omega t + \pi)\right)^2$$

$$I_d = I_{d0} * e^{\frac{V_{gs} - V_t + Acos(\omega t + \pi)}{nV_T}}$$

Now, knowing that the detector is an amplitude detector which cannot discriminate phase differences, these equations will yield the same results as the Meyer topology. Thus, all the equations that were derived for the Meyer topology in the saturation and subthreshold regions can be applied to this new detector.

In the triode region, the detector's response needs to be derived as there is no symmetry between the gate and source in that region. When the high frequency content is filtered at the detector's output, the DC drain current through the rectifying transistor T_1 becomes

$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}\left((V_{gs} - V_t)V_{ds} - \frac{{V_{ds}}^2}{2} + \frac{A^2}{4}\right)$$

Solving for V_{s1s2}, while ignoring the body effect, yields the following equation

$$V_{s1s2} = (V_{gs2} - V_t) - \sqrt{(V_{gs2} - V_t)^2 - \frac{A^2}{2}}$$

This equation is the same as the saturation equation (2-4) for the Meyer topology. The Taylor series expansion applied in Chapter 2 for the Meyer topology can be applied for this multiple-regions detector when it's operating in triode as well.

$$V_{s1s2} = \frac{1}{4(V_{gs2} - V_t)} * A^2 + \frac{1}{32(V_{gs2} - V_t)^3} * A^4 + \cdots \qquad (4\text{-}8)$$

This expansion showed that the detector can be approximated as a square law detector if the higher order terms in equation (4-8) are ignored. Hence, this multiple-regions detector can exploit some of the benefits attributed to the Meyer detector in the saturation region, namely the extended square law range, without the associated increase in power consumption.

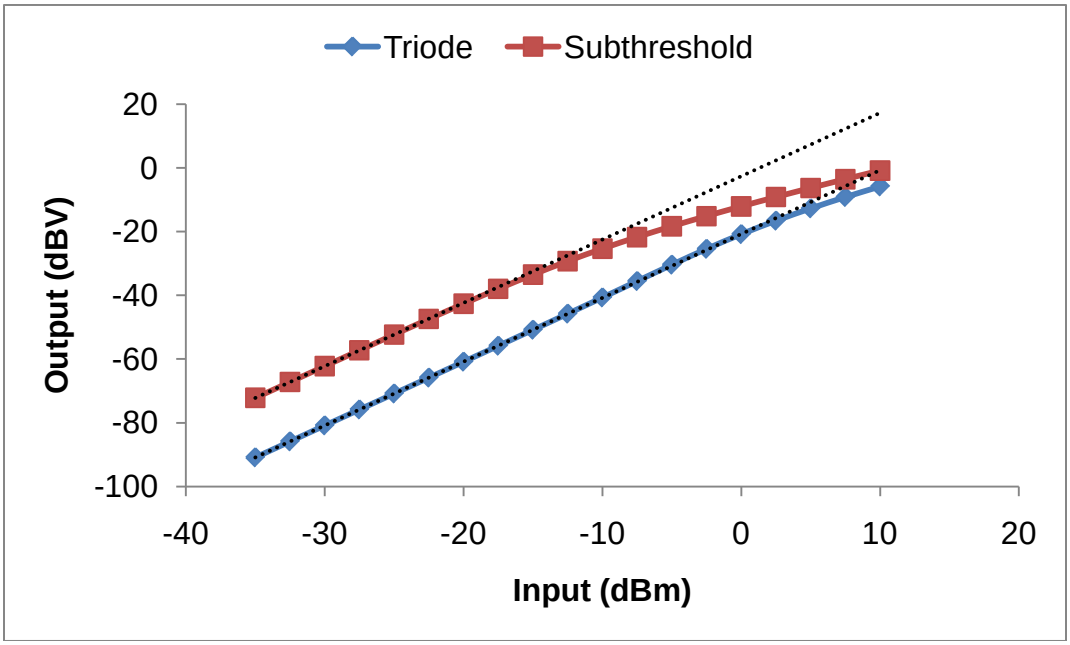


Figure 4-11. Simulation results of the multiple-regions detector's response

In the subthreshold region, the square law mode is recognizable for small signal levels; for large signal levels, the detector's response becomes linear. The plot also shows dashed lines which represent ideal square law response to illustrate the range where the detectors' response is also square law. When the detector is biased in triode region, the square law response dynamic range is larger as seen in Figure 4-11. The response of the detector's follows the ideal square law response for most input power levels. This is also confirmed in the measurement results below where the slope of the triode response in logarithmic scale is ≈2.

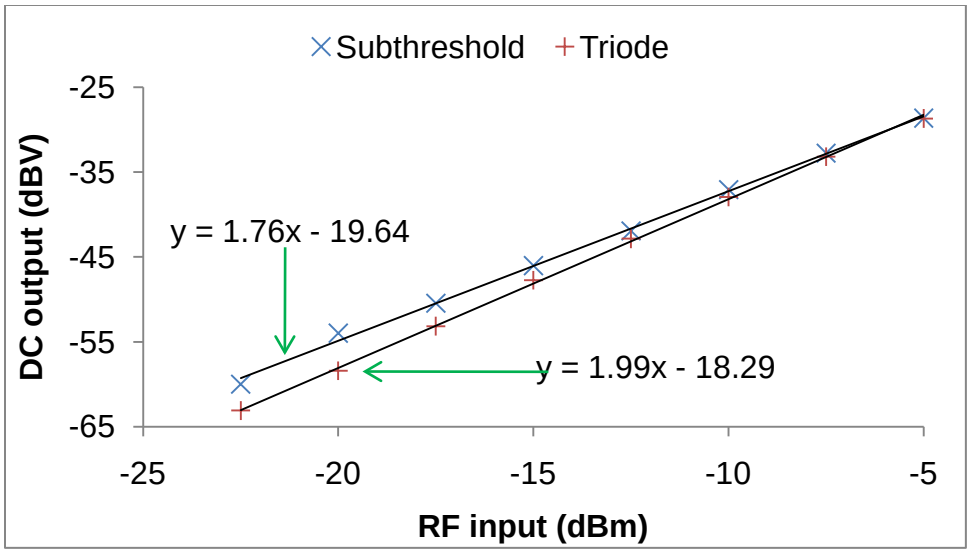


Figure 4-12. Measurement of the detector in logarithmic scale

Additionally, the inequality which was derived for the saturation region Meyer detector showed that the square law dynamic range is directly proportional to the overdrive voltage of the rectifying transistor.

$$\sum {A_i}^2 < 8(|Err| - Err^2){V_{ov}}^2$$

This inequality can be applied to the triode multiple-regions detector since it has the same RF-to-DC conversion as the saturation Meyer detector. Moreover, this square law dynamic range in the triode can be extended to larger values compared to the Meyer detectors since short channel effects become relevant in the saturation region for higher overdrive voltages which distorts the detector's response from square response. In the triode region, the drain-to-source voltage is low which minimizes velocity saturation effects [26].

Another advantage of this detector when operating in the triode is to have extended square-law performance without the required additional current consumption associated with the saturation region. However, the trade-off is increased sensitivity to process variations (Monte Carlo) when operating in triode. Bear in mind that this

problem is alleviated somewhat since the detector is useful because of its extended dynamic range, specifically for large signal levels where process variations are not as problematic in detection as for small signal levels. Monte Carlo simulations for the multiple-regions detector in triode show ~7% standard deviation when the input power is 0dBm, and ~14% for -35dBm input; while the variations due to temperature have similar levels compared to the Meyer detector topology. Also, because of the increased number of passives at the input of the detector, the bandwidth of the detector will be highly dependent on the attributes of these passive elements. Table 4-2 summarizes the trade-offs of each operating region. The key advantage of this multiple-regions detector is its flexibility; the structure can be customized depending on its targeted application by only changing its operating point.

Table 4-2. Trade-off of each operating region

	Power consumption	Accuracy	Square law dynamic range	Video bandwidth
Saturation	+	++	++	+++
Subthreshold	+++	+++	+	+
Triode	+++	+	+++	+

CHAPTER 5
MIXED-MODE DETECTION

Introduction

Measurements of mixed-mode S-parameters are essential for characterizing differential circuits and historically have been performed using 4-port network analyzers [52]. For BIST applications, replicating this architecture on-chip is not possible as it would require a large chip area. Another way to measure differential circuits is to use a balun coupled to a single-ended detector. However, this approach typically exhibits narrow-band behavior, or involves a larger and more costly silicon footprint [53]. Such solution can also introduce more uncertainty in the measurement, making it less desirable in BIST applications.

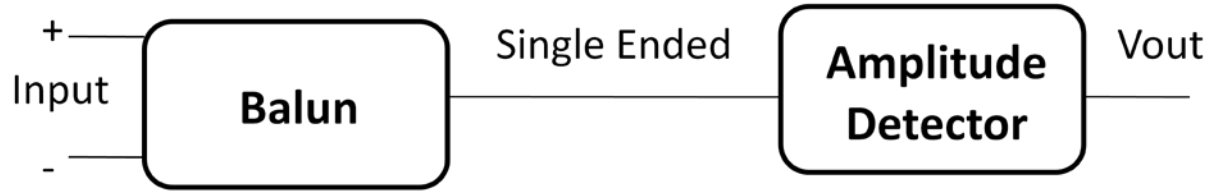


Figure 5-1. Conventional measurement method for differential signals

A number of publications used a detector based on a differential-pair topology which does not account for common-mode signals or assumes common-mode signals are negligible [21], [24], [35], and [54]-[58]. The circuit in Figure 5-2 simply acts as two single ended amplitude detectors whose outputs are averaged together into one output. If this circuit is stimulated with the following inputs

$$In+ = A * cos(\omega t + \theta_1)$$
$$In- = B * cos(\omega t + \theta_2)$$

The output of the detector is

$$Out = \frac{f_{det}(A) + f_{det}(B)}{2}$$

where $f_{det}()$ is the function the detector implements when it relates the RF input's amplitude to the DC output. This output does not have any dependence on the phases θ_1 or θ_2 since the detector measures amplitude only. Differential pairs work well in their traditional implementation which is when the output is the same frequency as the input; the output will retain phase information in this case. However, for amplitude detectors, the output is DC and has no phase information. Therefore, these pseudo-differential pair detectors cannot discriminate phase information making them unsuitable for measurement of a signal's differential component.

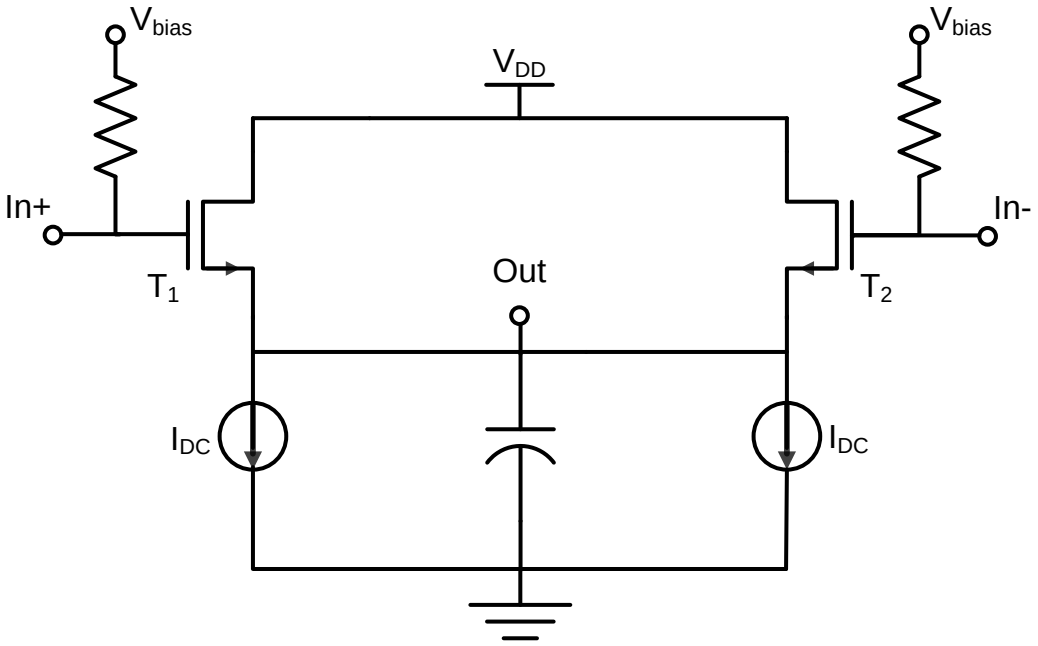


Figure 5-2. Detector using a differential pair

A design that is suitable for BIST applications which overcomes this limitation is presented in [59] and [60]. As seen in Figure 5-3, the classical diode detector is slightly modified by including an additional capacitor at the diode's cathode. Since the input to this detector is applied directly across the diode junction, a subtraction function between the input's two branches is performed. As a result, the circuit will reject any common-

mode signal, and the rectified output is proportional to the difference between the two input branches which is equivalent to the differential component A_{diff}.

$$A_{diff} = \sqrt{A^2 + B^2 - 2ABcos(\theta_1 - \theta_2)}$$

For a pure differential input where $A=B$ and $\theta_1-\theta_2=180°$, the differential component simplifies to $A_{diff}=2A$. For a pure common-mode input where $A=B$ and $\theta_1-\theta_2=0°$, the differential component simplifies to $A_{diff}=0$.

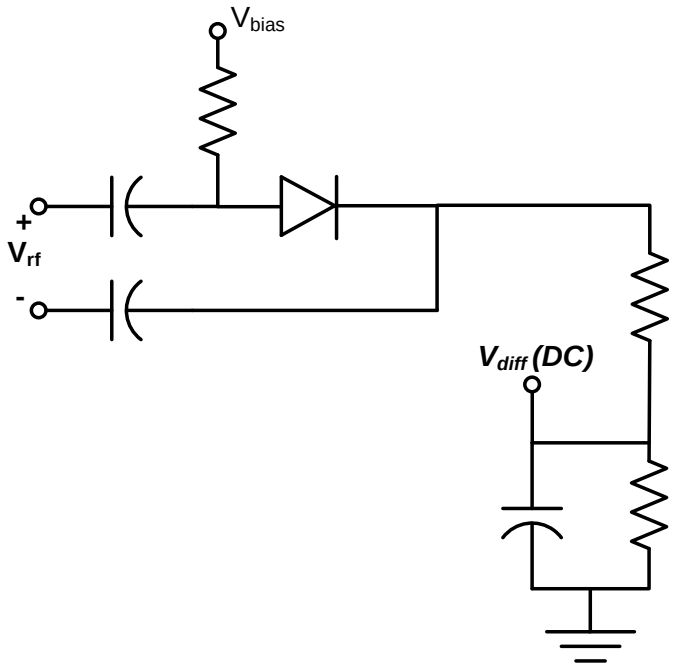


Figure 5-3. Differential diode detector

It's worth mentioning that this circuit was intended in its original publication [60] for ports that are not referenced to a common ground in a six-port junction circuit, more explicitly, ports where ground is not available. There was no clear indication that the circuit can be used for amplitude detection of differential circuits. [41] is the first one to identify the circuit as such, it leveraged this circuit and replaced the diode with a BJT transistor to make the detector compatible with a larger set of commercial semiconductor processes. Additionally, the idea of applying the input across a junction

was adapted to the single-ended Meyer detector topology [22] as shown in Figure 5-4. This structure is more robust to process and environmental variations since it uses a current source instead of a resistor. The topology shown in Figure 5-4 was also introduced by a different author in [61]; however, the patent reports only narrowband performance and describes the circuit as a peak detector. Detectors are known to be wideband devices; their bandwidth is limited by the parasitics in the path leading to the non-linear junction capacitance [22]. These parasitics are small and become significant only around f_t of the rectifying device. The circuit exploits the nonlinear properties of transistors, making rectification possible without prior amplification which extends the bandwidth of the detector into the mm-Wave range. Additionally, the detector in [61] should be identified instead as an amplitude detector since it exhibits peak detection only for a limited range of input levels as will be shown in the following sections.

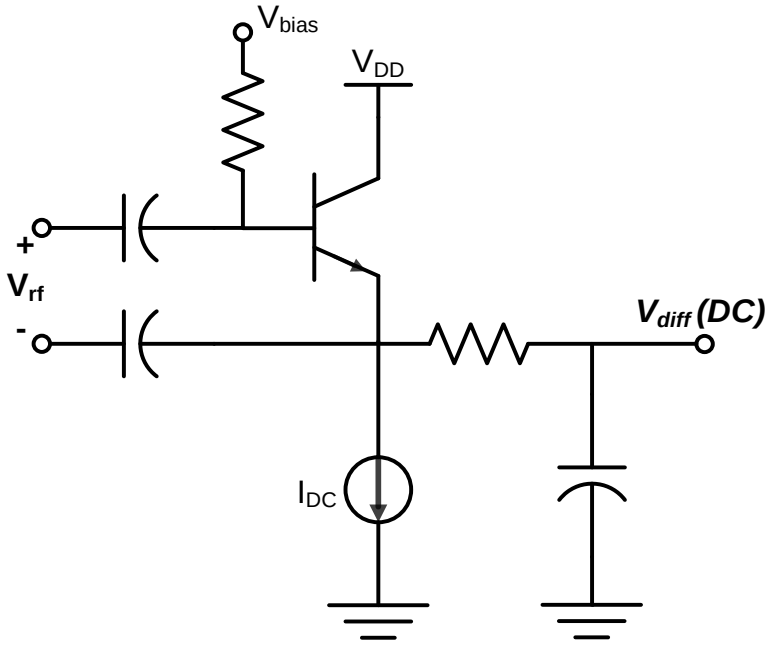


Figure 5-4. Bipolar differential detector

Furthermore, for BIST applications, the detector should have minimal loading effects on the DUT. The impedance looking into the emitter is high if the bias current

I_{DC} is low. However, this circuit might present a slight impedance imbalance between the two branches of the port under test. [41], [61] further enhanced this differential detector by developing a balanced version. As seen in Figure 5-5, the circuit in Figure 5-4 is duplicated and the two branches of the input are switched. The input across the base-emitter junction of Q_1 is V_{rf} . The base-emitter junction of the second transistor Q_2 sees $-V_{rf}$. Therefore, each branch of the port under test sees one base and one emitter; hence the name balanced detector.

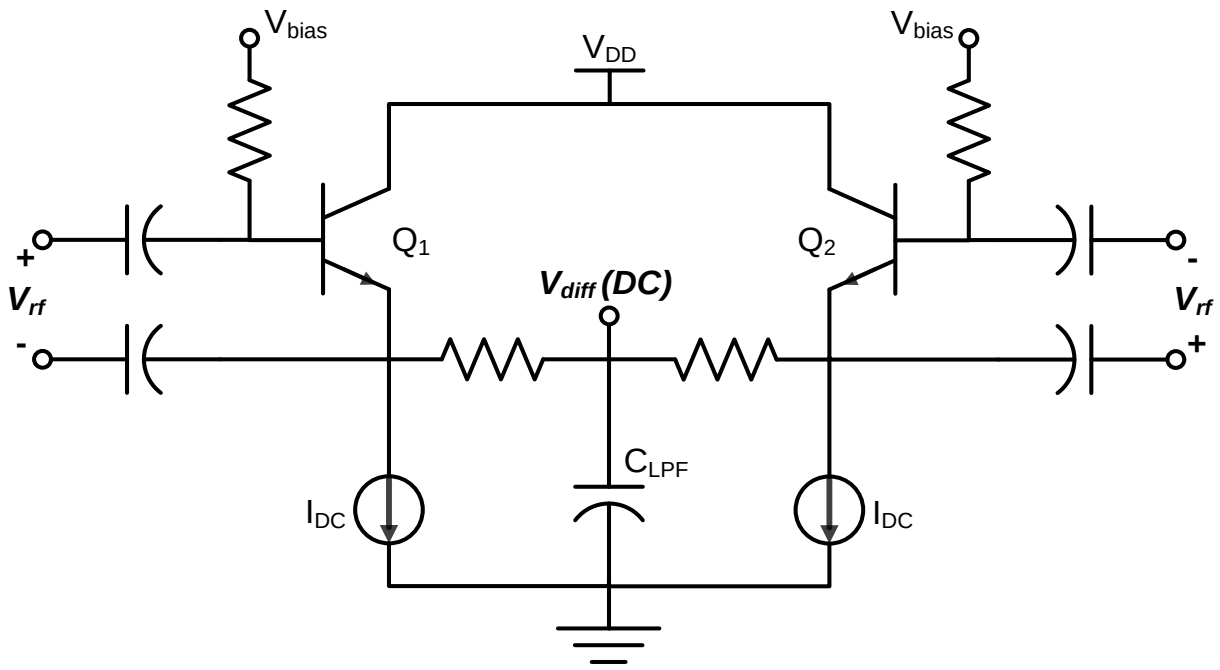


Figure 5-5. Balanced differential detector

The advantage of the balanced detector is a balanced load to the CUT. However, the disadvantage is a bigger circuit area, especially the four input coupling capacitors. This section introduced amplitude detectors capable of measuring the differential component; where differential detection is obtained as the input branches are applied across the base-emitter junction to replicate the subtraction function. If the input is applied across transistor branches which do not perform the subtraction function, true

differential detection is not possible as was the case in the topology shown [62]. Hence, investigation of the conditions for which differential detection is possible is necessary; especially since transistors can be biased in more operating regions compared to diodes. The next section provides a detailed analysis of the differential detector which was lacking in the previous literature [41], [61] as well as measurement results.

Key Details for Design of Differential Detectors

Alternate test methods which use amplitude detectors usually belong to two categories. The first method treats detectors as implicit feature extractors and relies on statistical analysis to estimate DUT specifications from detector measurements [23]. The second school of thought identifies detector structures whose measurements can be directly mapped to the DUT specifications; for example, [24] directly extracts gain and IIP3 of a DUT using rms detectors without resorting to learning steps. Both methods need the detector's response to have strong correlation to the DUT specifications. This sometimes requires significant pre or post processing for the first method; the second method's drawback is usually the long list of assumptions required to achieve the direct correlation. In this section, the focus is to present simple design guidelines to dispel the disadvantages associated with the second method as well as sources of error to the detector's response, and finally characteristics of the detector's response.

The dominant source of rectification, when a BJT transistor is used, stems from the non-linearities generated in the collector current. The Ebers-Moll equations express the currents of a BJT transistor in all its operating regions [26]. The collector current is

$$I_c = I_s\left(e^{\frac{V_{be}}{V_T}} - 1\right) - \frac{I_s}{\alpha_R}\left(e^{\frac{V_{bc}}{V_T}} - 1\right)$$

In the forward active region, the equation simplifies to

$$I_c = I_s e^{\frac{V_{be}}{V_T}}$$

When a detector is stimulated with a high frequency input, this equation becomes

$$I_c = I_s e^{\frac{V_{be}+(A\cos(\omega t+\theta_1)-B\cos(\omega t+\theta_2))}{V_T}} \quad (5\text{-}1)$$

Equation (5-1) shows how the subtraction operation occurs when one of the input signal branches is applied to the base and the other input branch is applied to the emitter of the BJT transistor. When a series expansion of the exponential term is implemented, non-linear terms are generated including a DC value that is proportional to the input difference. Conversely, in the other operating regions, the second term in the Ebers-Moll equation is significant rendering differential detection impossible. The following equation depicts the collector current when stimulated with a high frequency input. It shows a second term that is not proportional to the differential component of the input signal.

$$I_c = I_s\left(e^{\frac{V_{be}+(A\cos(\omega t+\theta_1)-B\cos(\omega t+\theta_2))}{V_T}} - 1\right) - \frac{I_s}{\alpha_R}\left(e^{\frac{V_{ce}+A\cos(\omega t+\theta_1)}{V_T}} - 1\right) \quad (5\text{-}2)$$

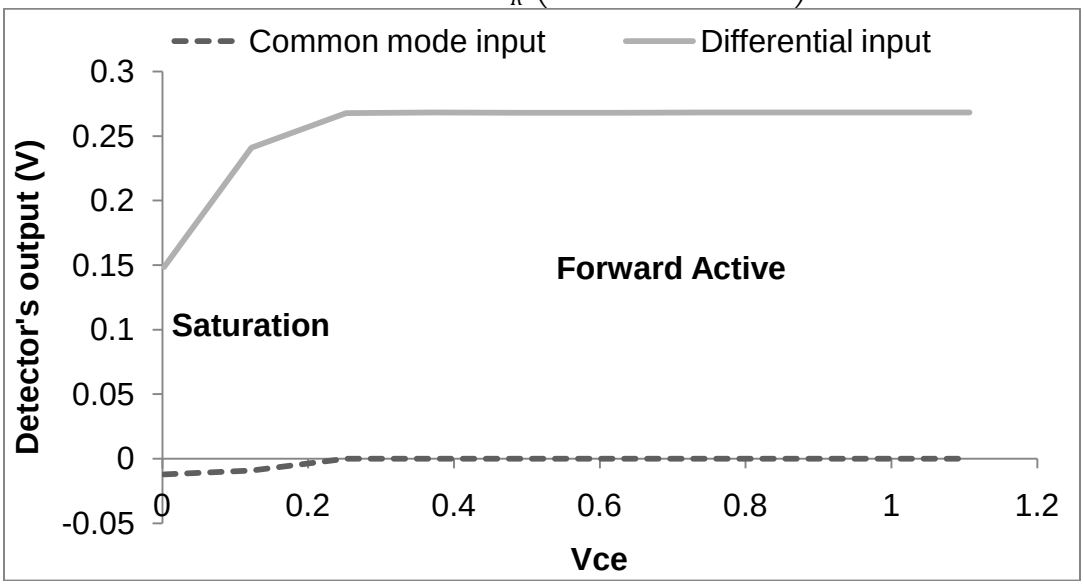


Figure 5-6. Differential detector's response to pure differential and pure common mode stimulus respectively

When biased in the forward active region, the detector responds to the differential stimulus and is indifferent to the common-mode stimulus as expected. As Vce across the rectifying transistor is decreased, the detector no longer exhibits properties that are associated with true differential detection as predicted by equation (5-2).

Also, it's worth noting that even in the forward active region, any deviations from the subtraction function between the input's two branches will create cross mode terms in the detectors. Cross mode terms for this detector are defined as a differential response to a common-mode stimulus; ideally, the response to common-mode stimulus should be zero for a true differential detector. In reality, signal distortions can be produced because of imbalances between the base and emitter paths into the rectifying transistors; these can be minimized by adopting careful design practices. Additionally, sources of non-linearity are not only limited to the base-emitter junction; instead, any second order effect or junction in the transistor might cause an undesirable rectification. When the high frequency input's two branches are not referenced to each other's across all the sources of non-linearity, imbalances are created which generate the cross mode terms. For example when the Early effect is taken into account, equation (5-1) becomes

$$I_c = I_s e^{\frac{V_{be}+\left(A\cos(\omega t+\theta_1)-B\cos(\omega t+\theta_2)\right)}{V_T}}\left(1+\frac{V_{ce}-B\cos(\omega t+\theta_2)}{V_A}\right)$$

If V_A is small, an imbalance is introduced since this equation deviates from ideal subtraction necessary for differential detection. Alternatively, it's possible to reduce this imbalance, for example, by shorting the base and collector of the rectifying transistor and slightly modifying the design. The simplified equation (5-1) ignores these second order effects as they are negligible when the rectifying transistor is biased in the forward

active region. This assumption is confirmed by the simulation shown in Figure 5-6 and measurement results in Figure 5-7; both Figures show a negligible common-mode response compared to the differential response.

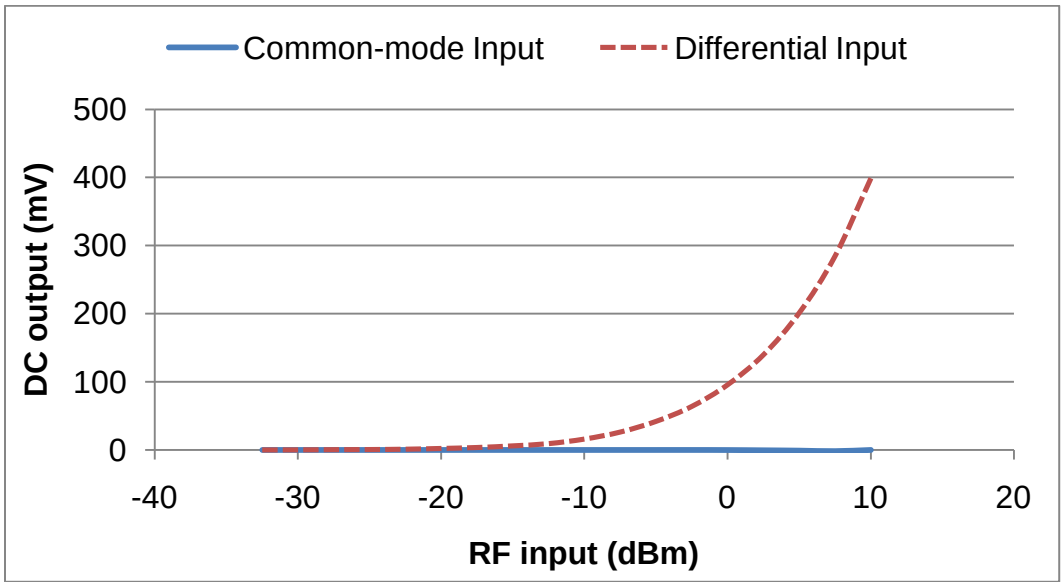


Figure 5-7. Measurement results of the BJT balanced differential detector.

Furthermore, rectification depends on another parameter besides the operating region of the detector; the input's amplitude affects the type of response the detector exhibits. Since it was established that this detector is only an extension of the single ended Meyer detector, the output equations derived for the single ended Meyer topology in [27] can be applied to the differential detector as well. The outputs are derived for designs that include a replica circuit which is usually used as a reference to cancel the quiescent DC offset voltage at the output of the detector.

For small signal levels (lower than -20dBm), the differential detector output is

$$V_{diff}(DC) = \frac{{A_{diff}}^2}{4V_T}$$

For large signal levels (larger than -10dBm),

$$V_{diff}(DC) = A_{diff} - \frac{V_T}{2} ln\left(2\pi \frac{A_{diff}}{V_T}\right) \quad (5\text{-}3)$$

These equations confirm that detector is an RMS detector for small signal levels and a peak detector for large signal levels as the logarithmic term in equation (5-3) can be ignored when the input's amplitude is large. These equations as well as the plot in Figure 5-8 confirm that the detector's response change with the operating conditions as it performs an RMS or peak measurement depending on the input signal level.

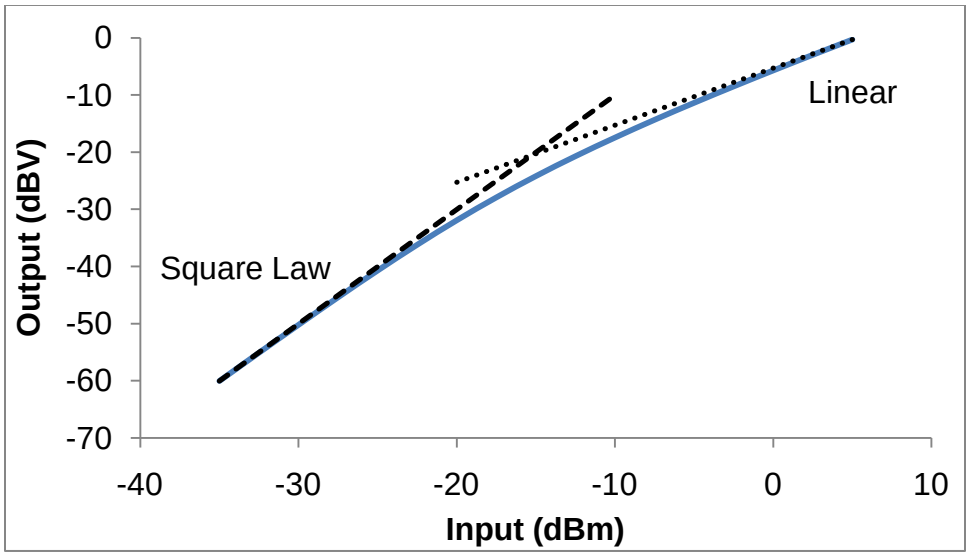


Figure 5-8. Detector's dependence on the input's amplitude

As seen in the Figure 5-8, when the detector's response is plotted in a logarithmic scale, the slope of the response is twice as high for smaller inputs compared to the slope at higher input levels. A slope of 2 in the logarithmic scale indicates that the detector's output is proportional to the square of the input which is equivalent to RMS detection. A slope of 1 means that the detector is a peak detector since its output is linearly proportional to the amplitude of the input.

Mixed Mode Detectors

The true differential detection potential of the topology was introduced in the previous section. In this section, an additional improvement is introduced by also enabling measurements of the common-mode component of a port under test. This

added capability will allow more insight into the circuit such as measurements of pure-mode gains and cross-mode gains. For example, if the measured differential gain of a circuit was lower than expected, it's not possible to troubleshoot using differential measurements only. Conversely, if the common-mode signal's amplitude is known, then diagnosis of certain faults such as coupling from adjacent circuit blocks or insufficient differential gain in the DUT itself becomes possible.

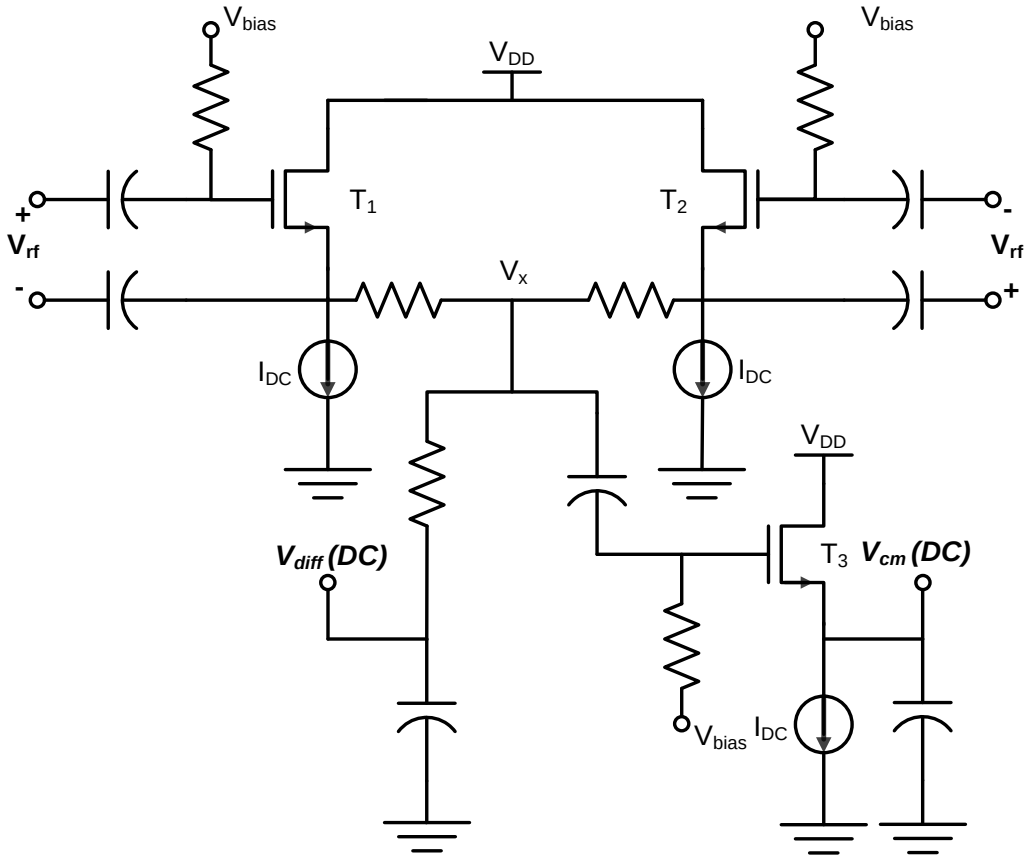


Figure 5-9. Mixed-mode detector

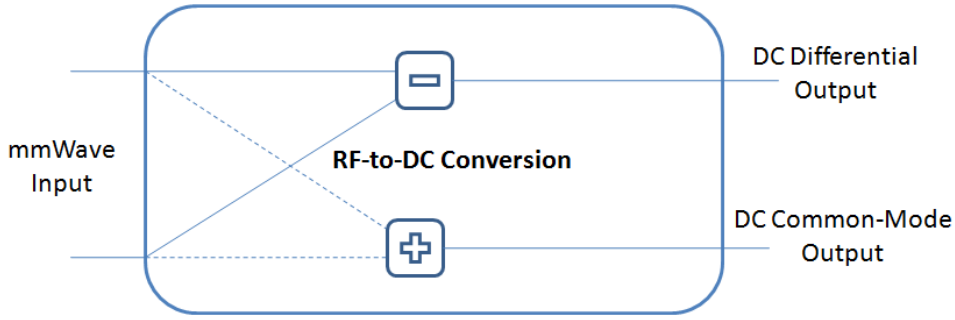


Figure 5-10. Simplified diagram of mixed-mode detector

With a careful look at the circuit in Figure 5-5, the $V_{diff(DC)}$ node is a virtual ground for differential signals only. For common-mode signals, the capacitor C_{LPF} shorts that node in Figure 5-5. With a small design change, the signal in that node can be routed to another detector to measure the amplitude of the common-mode component. The modified circuit in Figure 5-9 shows how the common-mode signal's amplitude A_{cm} can be detected.

$$A_{cm} = \frac{\sqrt{A^2 + B^2 + 2ABcos(\theta_1 - \theta_2)}}{2}$$

Node V_X in Figure 5-9 also represents the differential DC output and should be accessible for measurement purposes as seen in the Figure. Another modification was implemented in this design cycle. To make this detector compatible with standard bulk MOS processes, the BJT transistors were replaced by MOS transistors.

As seen in Figure 5-9, the circuit has two DC outputs. In addition to the DC differential output, there is a DC common-mode output. The added capability of measuring common-mode signals was implemented without increasing the loading effects on the DUT. The circuit also maintains its symmetrical structure to present a balanced load to the DUT.

The 3D plot in Figure 5-11 shows that the differential DC output responds to pure differential RF stimulus only. Even when the common-mode RF stimulus level is swept, the differential DC output is constant. Now, for the common-mode response of the mixed-mode detector, the circuit responds to common-mode RF stimulus only as shown in Figure 5-12.

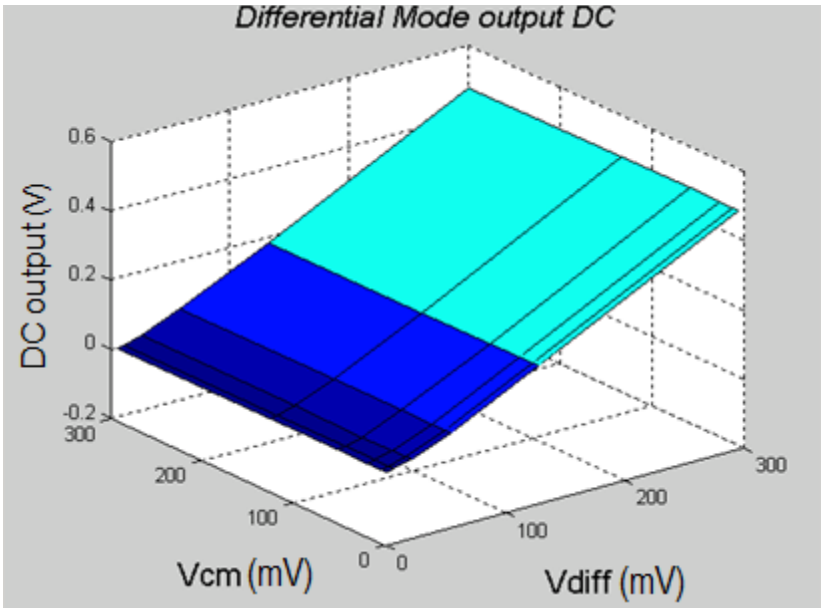


Figure 5-11. Differential response to mixed-mode stimulus

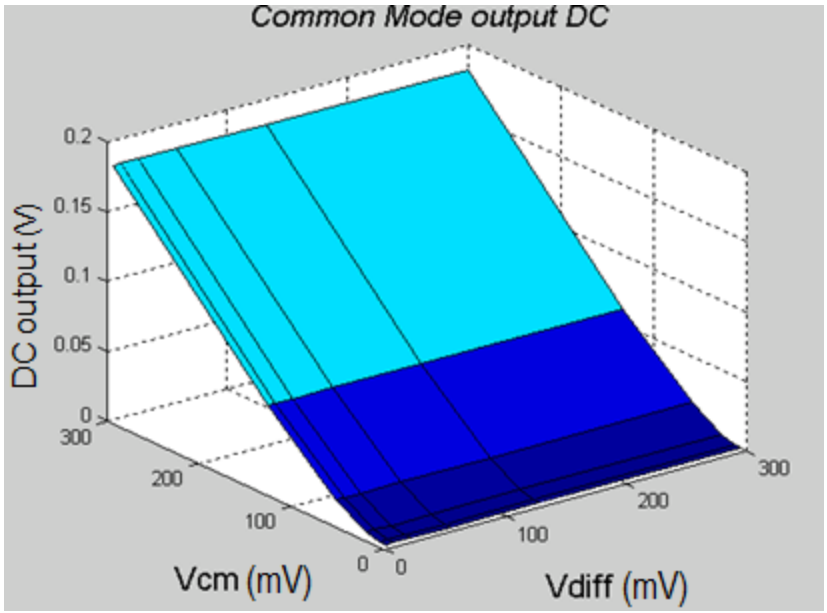


Figure 5-12. Common-mode response to mixed-mode stimulus

Similar to the BJT version of the differential detector, the MOS version cannot perform differential detection in all the operating regions. When the detector is stimulated with a high frequency input, the drain current when the rectifying transistors are biased in the saturation (5-4), subthreshold (5-5), and triode (5-6) respectively is

$$I_d = K' \left(V_{gs} - V_t + \left(A\cos(\omega t + \theta_1) - B\cos(\omega t + \theta_2)\right)\right)^2 \quad (5\text{-}4)$$

$$I_d = I_{d0} e^{\frac{V_{gs} - V_t + \left(A\cos(\omega t + \theta_1) - B\cos(\omega t + \theta_2)\right)}{nV_T}} \quad (5\text{-}5)$$

$$I_d = K' \left(V_{gs} - V_t + A\cos(\omega t + \theta_1) - B\cos(\omega t + \theta_2)\right) * \left(V_{ds} - B\cos(\omega t + \theta_2)\right) - K' \left(V_{ds} - B\cos(\omega t + \theta_2)\right)^2 \quad (5\text{-}6)$$

with $K' = \frac{\mu C_{ox}}{2} \frac{W}{L}$.

As seen in the saturation and subthreshold equations (5-4) and (5-5), differential detection is possible since the drain current is a function of the difference between the input's two branches. In the triode region, the drain current in (5-6) has some error terms that are proportional to only one of the input's branches. Thereby, differential detection is not possible in the triode region. Also, long channel models are used in order to simplify the analysis. Differential detection is still possible since equation (5-7) which accounts for short channel effects (velocity saturation) is still balanced between the gate and source [26]. Also, mobility degradation due to lateral fields has balanced effects on differential detection.

$$I_d = K' \left(V_{gs} - V_t\right)^2 \left(1 - \frac{V_{gs} - V_t}{\xi_c L}\right) \quad (5\text{-}7)$$

where ξ_C is the critical electrical field. Furthermore, in subthreshold and triode operating regions, short channel effects are negligible.

For common-mode detection, the input branches are summed before they are measured using a single ended detector. [28] shows that single-ended detection is only possible in saturation and subthreshold when the input is applied to the gate of the rectifying transistor.

In addition, the cross mode terms which occur in this mixed-mode detector are not limited to the differential response to common-mode stimulus as was the case for the

topology in Figure 5-5; there is another cross mode term which consists of the common-mode response to differential stimulus. This term depends mostly on imbalances in the common-mode signal path. It is not affected by second order non-linear effects like the differential detector as common-mode detection exploits a single ended structure. Furthermore, The MOSFET differential detector portion exhibits more significant cross mode detection compared to the BJT detector in the previous section. Second order non-linear effects such as the Early effect were shown in the previous section to cause these cross mode terms in the differential detector topology. The MOSFET design was implemented in a non-epi (low doping) substrate making channel length modulation effects substantial. The Early effect is inversely proportional to the doping levels in the channel [26]. While the Bipolar design was designed using SiGe HBT devices in a BiCMOS process which typically has a higher base doping concentration [63]. As mentioned in the previous section, it is possible to minimize these effects by modifying the topology and connecting the gate of the rectifying transistors to their drain.

Below are the equations showing the detector's response in different operating regions. The body effect was ignored when these equations were derived.

In the saturation region, the output is

$$V_i(DC) = \frac{A_i{}^2}{4V_{ov}} + \frac{A_i{}^4}{32V_{ov}{}^3} + \ldots \tag{5-8}$$

where subscript *i* can be replaced by subscript *diff* or *cm*, and V_{ov} is the overdrive voltage across the rectifying transistor (V_{gs}-V_t). When the higher order terms are ignored in equation (5-8), the detector performs rms measurements.

In the subthreshold region, for small input levels, the output is

$$V_i(DC) = {A_i^2}/{4nV_T}$$

For large signal levels, the output is

$$V_i(DC) = A_i - \frac{nV_T}{2}\ln\left(2\pi\frac{A_i}{nV_T}\right)$$

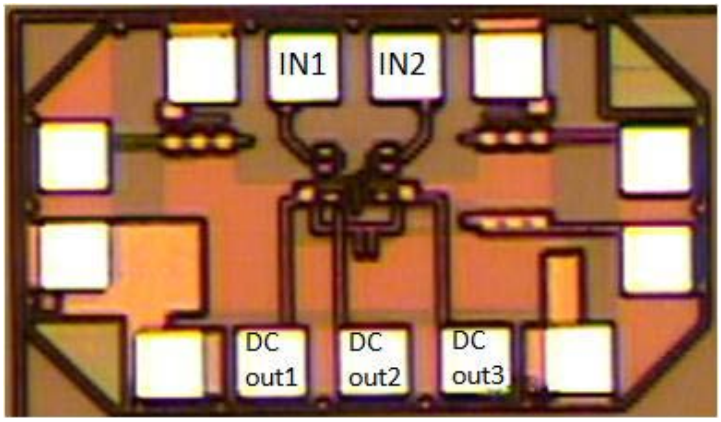


Figure 5-13. Picture of mixed-mode detector

This circuit was fabricated in an IBM8HP process. It occupies an area of 0.59mm^2 including pads, 0.045 mm^2 without pads. The detector consumes 0.5mW of static power including power consumed by a current reference circuit; otherwise, power consumption was a mere 8μW when accounting for the detection circuit only. The detector's output settling time is approximately 100ns. The detector's measured dynamic range is at least 30dB. This mixed-mode detector was measured at different frequencies. The detector was simulated to work at millimeter wave frequencies up to 70GHz, which is the range where the detector's mixed-mode reflection coefficients (S_{dd11} and S_{cc11}) remain below -10dB when referenced to a 50Ω environment. This means that at lower frequencies, the detector can be embedded into a DUT without any customization; on the other hand, the detector's load should be integrated into the matching network design at higher frequencies. The degradation in the frequency response was mostly due to the quality of the passive circuits that were used. Figure 5-14 shows measurements of the

differential DC response when the detector is stimulated with a pure differential and pure common-mode signal. The detector only responds to pure differential stimulus. Figure 5-15 for measurements of the common-mode DC output shows the opposite behavior of differential DC output. The response stays near zero when the input is a pure differential signal.

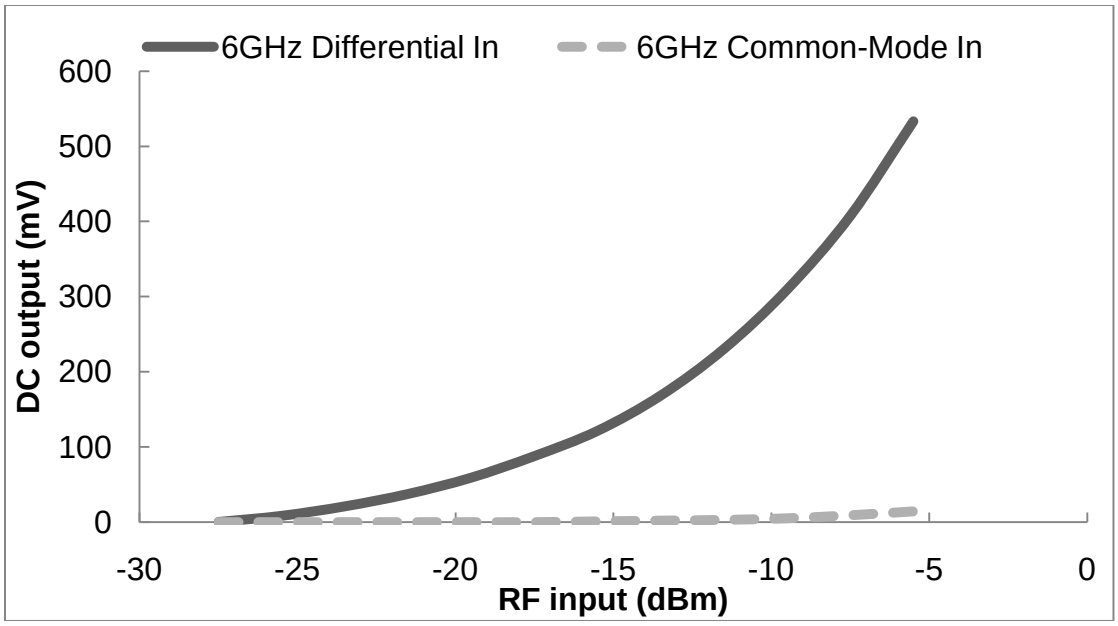


Figure 5-14. Measurement of differential DC response.

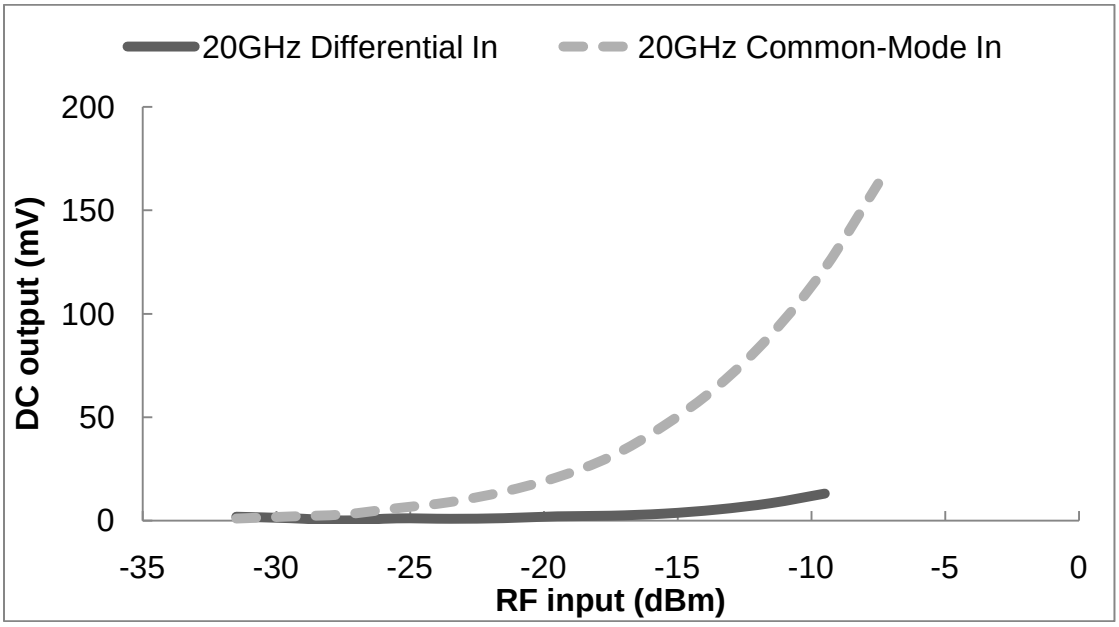


Figure 5-15. Measurement of common-mode DC response

In Figure 5-14 and Figure 5-15, small cross mode detection is evident at higher input levels and increases as the signal's frequency is increased. Besides errors which are inherent to the detector, a portion of this error is due to the measurement setup where it was difficult to supply pure mode stimulus all the way to the probe tips. There are commercial solutions to solve this issue such as Agilent's N5242 four port network analyzer which offers automated calibration of the measurement setup [64]. [65] is another solution that presents a manual method to generate pure mode stimulus. All the measurements in this chapter are presented for the purpose of verifying the functionality of this circuit and should not be taken for absolute values since calibration of the test setup to verify the detector was not possible at the time of measurement. Furthermore, due to instrumentation constraints, mixed-mode measurements were limited to 20GHz, whereas single-ended measurements were implemented up to 40GHz to verify the circuit further. Finally, unlike previous designs that ignore the common-mode signals, this new design outputs a DC voltage that is proportional to the true differential component and another DC output that is proportional to the true common-mode component.

Calibration

Since these detectors are an enhanced version of the Meyer single ended detector, all the merits associated with the single ended topology can be extended to the detector topologies presented in this chapter. The output equations derived for the detector show that first order immunity to process variations and temperature variations is inherent within the detector's topology.

First, similar to the single ended detector, a DC offset which arises between the rectifying part of the detector and the replica needs to be taken into account. This offset

can severely limit the dynamic range of the detector if it's not removed. [21], [44] states that this offset is constant and remains independent of the high frequency input in the single ended detector topology. This observation can be upheld for mixed-mode detectors as well since the DC offset is not dependent on the high frequency input. This offset is removed by performing one time DC measurement at the beginning of testing.

Monte Carlo simulations were implemented using the foundry's "Skew" file and variations at the differential DC output $V_{diff(DC)}$ had a standard deviation of 4.5% when the detector was stimulated with a differential input of -35dBm; this standard deviation value means the detector will have 1dB accuracy in 99% of cases. The detector experiences the highest variations when the input power is low; hence, the use of -35dBm to measure the maximum amount of variations. For the common-mode output, the standard deviation is 6.4% when the input was pure common-mode and 1dB accuracy is possible for only 93% of cases. The standard deviation is higher for the common-mode detector compared to the differential detector because of the number of additional passives in the common-mode signal path. Nevertheless, more fundamentally, the detector's accuracy is only as good as the current source used in the design. A MOSFET peaking current source was used because of its potential to generate low current values. The MOS peaking current source was biased at an operating point which minimizes the detector's temperature dependence; [66] showed that for MOS transistors there is an operating point where the mobility temperature dependence cancels the effect of temperature on the threshold voltage. The detector's overall accuracy was better than 1dB in the commercial temperature range of 0°C to 70°C. Regrettably, at the time of circuit tape-out, process variations for the current

source were not fully considered and the final design was not robust to process variations as the simulated standard deviation of the current generated by the source was 28%. Even with this high value, the standard deviation of the detector's response was much lower than the standard deviation of the current source which attests to detector's immunity to variations. When the detector is simulated with an ideal current source, the variations are much lower, below 2%. When only mismatch (intra-die variations) is considered in Monte Carlo simulations, the standard deviation is below 1%. Since intra-die variations are smaller, an increased accuracy can be achieved when an extra detector whose input can be probed is included to be used as a reference for calibration purposes. Calibration of this detector is also possible by using a single ended input which simplifies the calibration process. Using single ended stimulus is equivalent to applying a differential and a common-mode signal simultaneously such as $A_{single-ended}=A_{diff}/2+A_{cm}/2$. This results in calibrating the differential detection portion in addition to the common-mode detection portion at the same time. Furthermore, the detector can be calibrated by applying a low frequency single ended input at the $V_{diff}(DC)$ output using a bias-T in an unconventional way. The choke port of the bias-T can be used to measure the DC output of the detector and the low frequency signal can be coupled through the capacitor port. When detectors are embedded in a DUT, high frequency external access to the detectors' inputs for calibration purposes is not possible.

More elaborate calibration methods are also possible as process variations become important in deeply scaled process technologies. Several methods were developed to calibrate single ended amplitude detectors; they can be extended to the

mixed-mode detector since most variations are associated with the active elements in the topology. [47] relies on DC signals only for calibrating the detector by using statistical analysis to map a DC-to-DC response into the RF-to-DC response. [29], [32], and [43] use statistical analysis to account for process variations by calibrating the DUT and the detectors simultaneously. The methods rely on a defined dictionary that can be built either from simulations or actual measurements assuming the DUT can be measured using conventional methods; then a mapping engine can estimate the specifications of the DUT from the alternate measurement space. The alternate test methods are immune to process and environmental variations as long as there are strong correlations between the alternate test measurement space and the DUT's specification space.

CHAPTER 6
SYSTEM APPLICATIONS

Introduction

The purpose of this chapter is to introduce concrete examples to clearly demonstrate the effectiveness of the amplitude detectors reported in the previous chapters. First, a setup that uses single ended detectors to measure specifications of an LNA is discussed in the next section. Another section, discusses multi-port reflectometers that employ differential and single-ended detectors. This chapter sheds more light on the numerous trade-offs discussed previously and indicates examples of suitable applications for each type of detector.

LNA Example

As seen in Figure 6-1, two detectors can be used to measure gain and compression point P-1dB of a Low Noise Amplifier (LNA). Similar topologies were previously published in [13], [24], [31], [41], [43], [54], and [67]-[69]. In addition to gain and compression point, other parameters can be estimated through further analysis of the amplitude detectors' output. For example, [69] estimated the Noise Figure and reflection coefficient relying on simplified equations that are accurate for specific conditions discussed in more details in [70]. [31] extracts Noise figure, and P-1dB by applying wavelet analysis on the detector's output when the LNA is stimulated with a two-tone stimulus. Statistical regression analysis was also employed in [43] to estimate IIP3 in addition to the previous specifications. The stimulus in that methodology was simplified by using a single-tone input; however, this entailed use of two types of detectors at the output of LNA. [54] uses two tones stimulus and non-linear mapping to extract TOI as well; moreover, [24] improved upon the method reported in [54] by

deriving an equation which directly relates the detector's output to TOI without resorting to any statistical methods. Thus, there is abundant literature that discusses the capabilities of amplitude detectors. In this section, the focus is to delve into the details of various sources of errors that might corrupt estimation of the specifications from the setup shown in Figure 6-1. Among other errors, the discussion is mainly limited to errors that stem from the inherent workings of the amplitude detector. As previously discussed, the detector's response varies with the operating region, different signal levels, and signal shapes. Therefore, what has lead to this detector's flexibility can easily lead to its downfall if not carefully considered. Whether these alternate test methods use implicit or explicit detectors, the strong correlation needed between the detector's measurements and the DUT specifications might not be maintained when the detector's type of response changes. The detectors' response need to have a large dynamic range to cover a wide range of applications without necessitating complex customizations. Accordingly, the advantages of each of the detector topologies discussed in the previous chapters are introduced in this context.

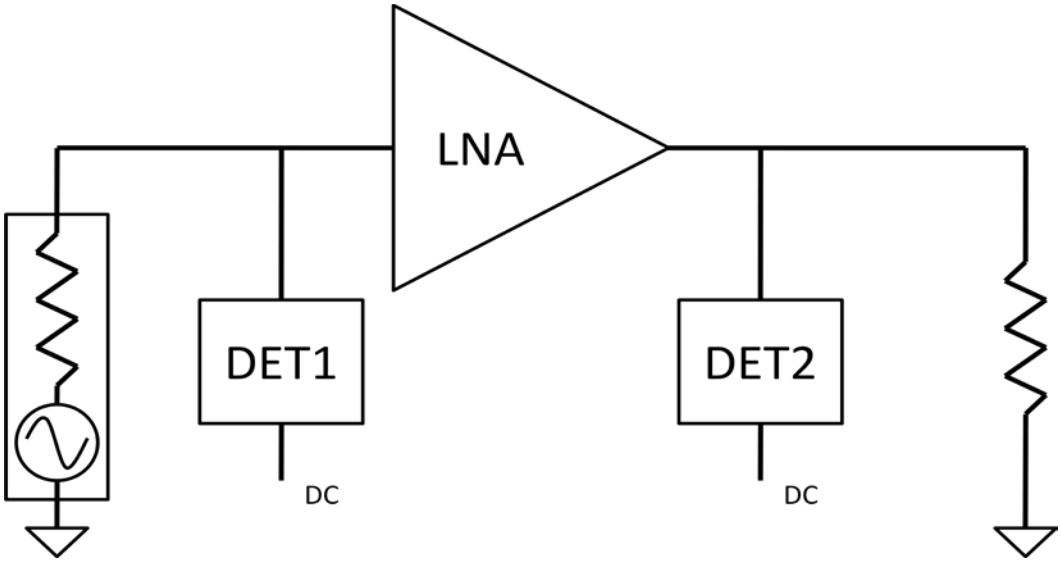


Figure 6-1. Detectors for measuring gain and compression of an LNA

It's worth mentioning that the discussion in this section is limited to gain measurements for the sake of simplicity. Gain is one of the simplest DUT specifications; if it is not accurately estimated, none of the other specifications can be predicted. [68] measures the gain by including an amplifier after det1 and variable gain amplifier (VGA) after det2. For a given input power, this method estimates the gain of the LNA by sweeping the gain of the VGA. To measure the compression point, this method might be inefficient since sweeping the gain of the VGA is necessary for every input signal level. Additionally, [68] does not explicitly state the dynamic range of the reported alternate test setup. The P-1dB compression point estimated using the method published in [67] is accurate within 1dB of the actual compression point. However, this accuracy is achieved within a limited dynamic range making the method prone to errors. [67] sweeps the input power level to extract gain and compression point by comparing the respective input powers where det2 and det1 output the same DC value. For example, given that det2 outputs a DC value x at input power P_a and det1 had that same DC value x when the input power was P_b, then the gain of the DUT is P_b-P_a. This method has a limited dynamic range because, as shown in the previous sections, the detector's type of response varies with the input signal's amplitude. If the input signal level is in one range (i.e. square law subthreshold mode) and the output signal level is another range (i.e. linear subthreshold mode), then the gain extracted using this method is not accurate. This can be seen in Figure 6-2 which shows that gain estimated using the method described above (blue curve) starts deviating from the actual gain (red curve) as the input signal is increased.

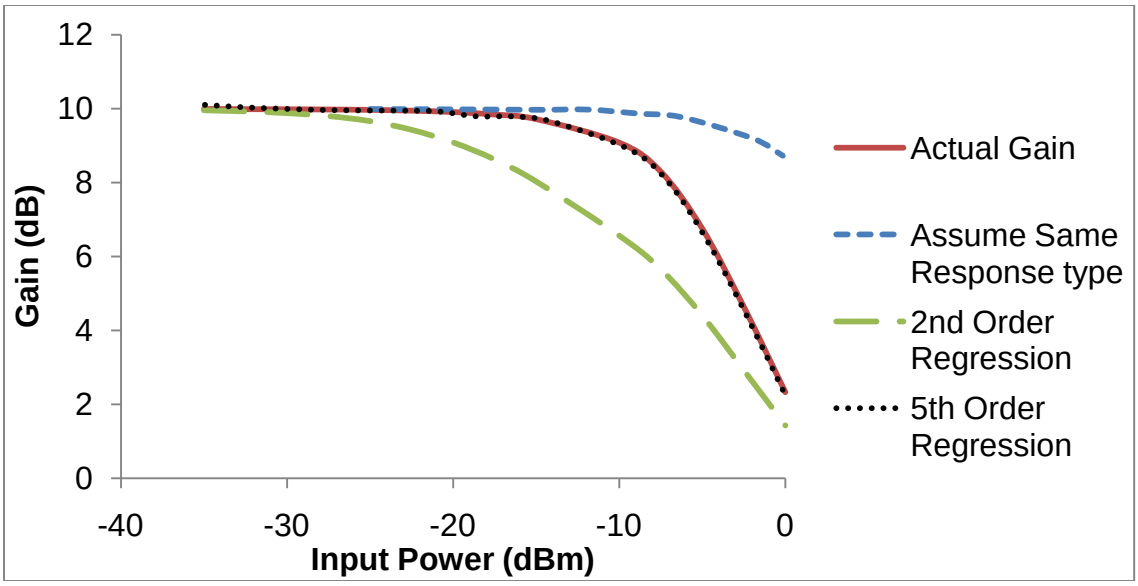


Figure 6-2. Actual gain compared to different methods used to estimate the gain

Alternately, higher order fitting of the detector's response yields accurate estimations of the DUT specifications. As seen in Figure 6-1, the first detector can be characterized as it is connected to the signal source. By sweeping the input signal's power level, the RF-to-DC conversion equation of the detector can be obtained. Assuming that det2 is well matched to det1, the two detectors will have the same RF-to-DC conversion equation. The next step is to derive the inverse function of the RF-to-DC conversion equation. Finally, by measuring the DC value of det2, the gain of the DUT can be calculated. Figure 6-2 shows that when the detector's response is fitted with a 5^{th} order regression equation, accurate estimation of the LNA's gain is obtained by following the steps discussed above.

On a side note, higher order regression analysis might mean longer characterization time unless there are good matching conditions across the wafer, temperature stability, and good biasing strategy. Aside from the process variations issue, all the other conditions are required to maintain good accuracy for conventional commercial test setups as well. Provided that these conditions are met, the time

required to compute or retrieve from a memory module the RF amplitude given a DC output from det2's should be considered as it can be substantial. Higher order regression is possible only when the processing unit experiences some idle time margin. Overall testing time consists of the time required to setup the measurement in addition to the time needed for the actual measurement. For example, the index time of high performance membrane probes is in the tens of milliseconds; a settling time associated with any change to the test stimulus also exists [1]. Therefore, the time margin required for the test setup dictates the accuracy that can be achieved with this alternate test method when higher order regression is needed.

Achieving a larger detection dynamic range without sacrificing test time is possible by using some the strategies or structures reported in the previous chapters. Figure 6-2 also shows that 2^{nd} order regression accurately predicts the LNA's gain at low power levels. This is consistent with the theory discussed in Chapter 2 which stated that the detector's response follows the square law for small signal levels and deviates from that type of response as the input signal level is increased. Chapter 3 uncovered that the square-law response dynamic range can be increased by increasing the overdrive voltage across the rectifying transistor. This is beneficial since the LNA's gain can be extracted over a large dynamic range without resorting to higher order regression analysis. Figure 6-2 showed that gain is accurately estimated for the four curves as long as the input power is small; however, accurate estimation of P-1dB depends on the method that is used. On the other hand, if the LNA's gain is larger than the amplitude detectors' dynamic range, even estimation of the gain is no longer possible. Figure 6-3 shows that the dynamic range of the alternate test method can be increased by raising

the overdrive voltage across the rectifying transistor in the detector. Although, as discussed in Chapter 3, there is limit to this method since short channel effects become dominant when the overdrive voltage is too high as seen in both Figure 6-3 and Table 6-1.

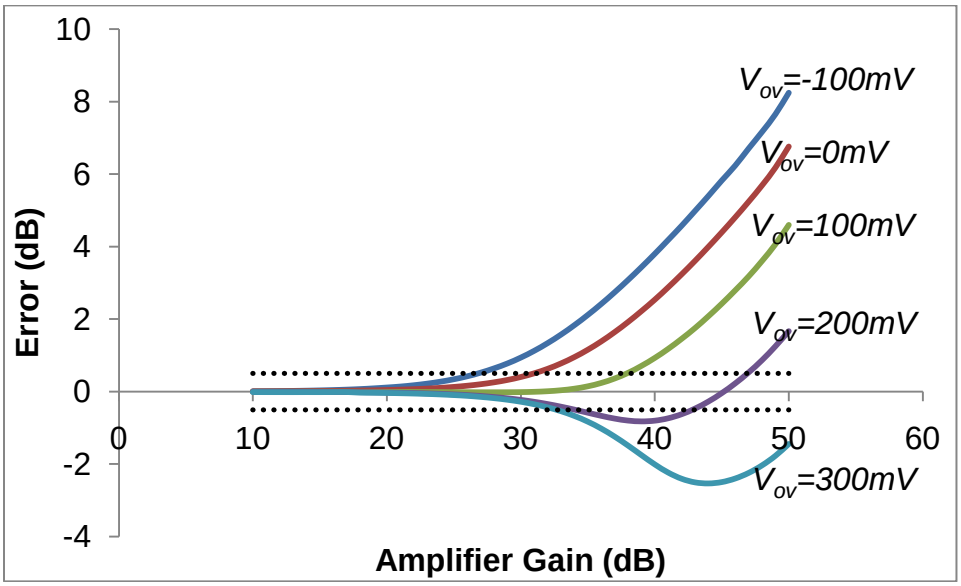


Figure 6-3. Error between ideal gain and gain estimated from detectors that are biased at different overdrive voltages

Table 6-1. Maximum gain estimated by the detectors within .5dB accuracy

V_{ov}	-100mV	0V	100mV	200mV	300mV
Gain	27dB	31dB	38dB	34dB	32.5dB

In Chapter 4, novel detector topologies were introduced to minimize the ranges where the detectors exhibited non-ideal response. Among the many benefits of the novel type III detector, it is capable of increasing the square law dynamic range even further by circumventing short channel effects. Figure 6-4 and Table 6-2 show the maximum gain that can be measured by the detectors within .5dB accuracy by increasing *M*, a factor introduced in Figure 4-2.

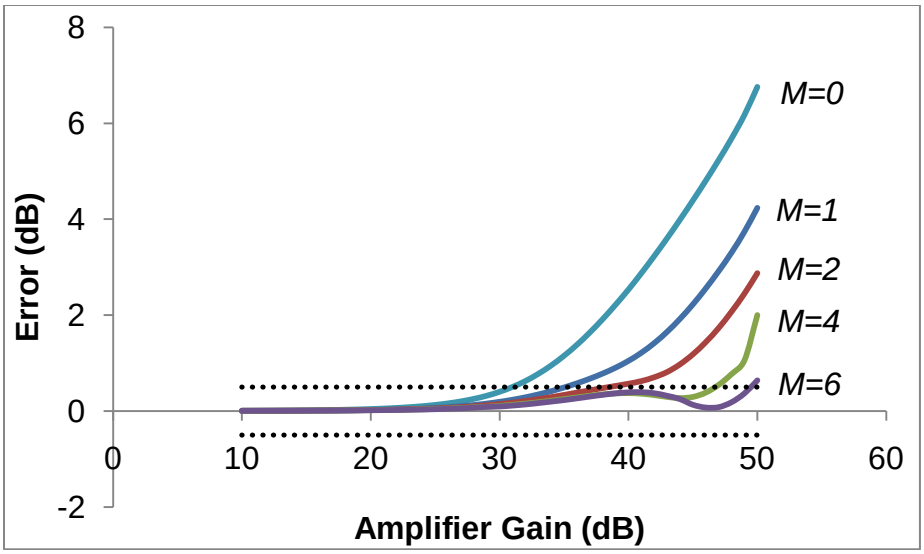


Figure 6-4. Error between ideal gain and estimated gain from type III detectors

Table 6-2. Maximum gain estimated by the typeIII detectors within .5dB accuracy

M	0	1	2	4	6
Gain	31dB	35dB	38.5dB	46.5dB	49.5dB

Additionally, Chapter 4 also introduced a novel topology advantageous because of its flexibility; the multiple-regions detector can operate in subthreshold, saturation, and triode where each of these operating regions is associated with certain trade-offs which were summarized in Table 4-2. For example, operation in triode has the largest square law dynamic range as seen in Figure 6-5 since short channel effects are minimal in that region compared to operation in the saturation region. Also, static power consumption is lowest in the triode region which is indicated by the numbers adjacent to the plots in Figure 6-5. However, triode detectors have a long settling time which increases the overall test time or lowers the video bandwidth and they possibly suffer from a higher sensitivity to process variations compared to operation in the saturation and subthreshold regions.

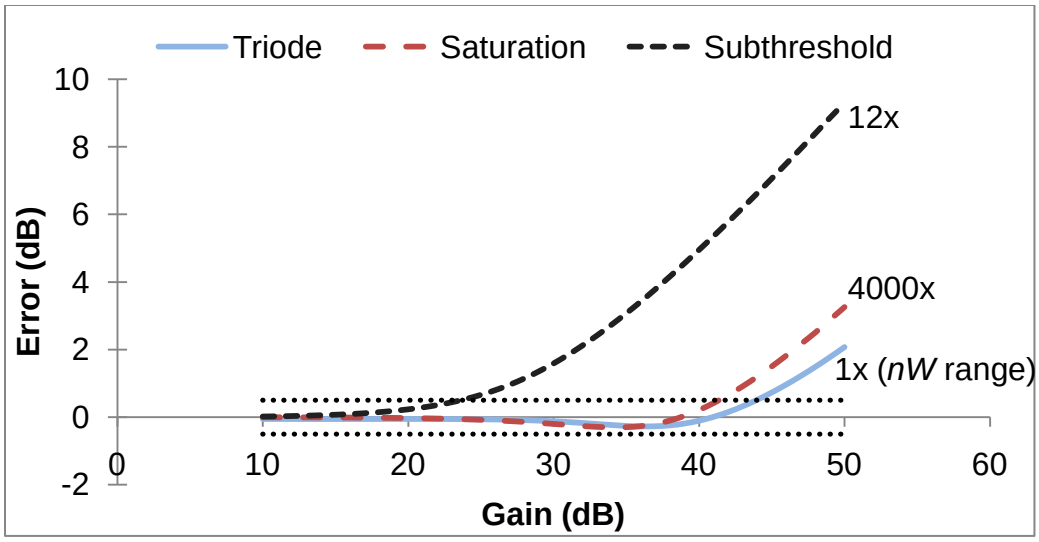


Figure 6-5. Error between ideal gain and estimated gain from the multiple-regions detectors

Finally, both the type III and multiple-regions detectors extend the square law dynamic range which enables lower test time and accurate measurements of the DUT specifications for a larger set of applications. The difference between the two detectors is that type III is advantageous in high frequency circuits since it has less parasitics at its input path compared the multiple-regions detector; it also offers extended dynamic range without decreasing the video bandwidth. Therefore, it is appropriate for production testing that requires complicated measurements such as P-1dB and IIP3. On the other hand, the multiple-regions detector offers flexibility since the same structure can be used in different situations. For example, in characterization test where time is not of the essence, operation in triode is advantageous since extended dynamic range is achieved in that operating region. When the product is qualified for production, the multiple-region can be operated in the saturation region because of its fast settling time. Provided that there is a high correlation between gain and IIP3, the larger dynamic range in triode might not be necessary in production test. Now that the trade-offs of each operating regions were dissected, there is a limitless number of applications where

the flexibility offered by these detectors is beneficial. Furthermore, all these concepts can be projected onto the mixed-mode detector from Chapter 5 when the DUT is a differential with the exception of operating in triode as it was determined in Chapter 5 that differential detection is not possible in that region. The type III topology can be adapted to the differential detector; however, it requires the use of inductors.

Multi-port Reflectometers

Introduction

Measurement of S-parameters which characterize the DUT's matching, gain, and reverse isolation is essential in RF circuits. S-parameters are represented by complex vectors with amplitude and phase information; they are commonly measured using vector network analyzers. Figure 6-6 shows a simplified architecture of a network analyzer. This high level diagram shows the main building blocks of a network analyzer's port which consists of couplers and detector structures.

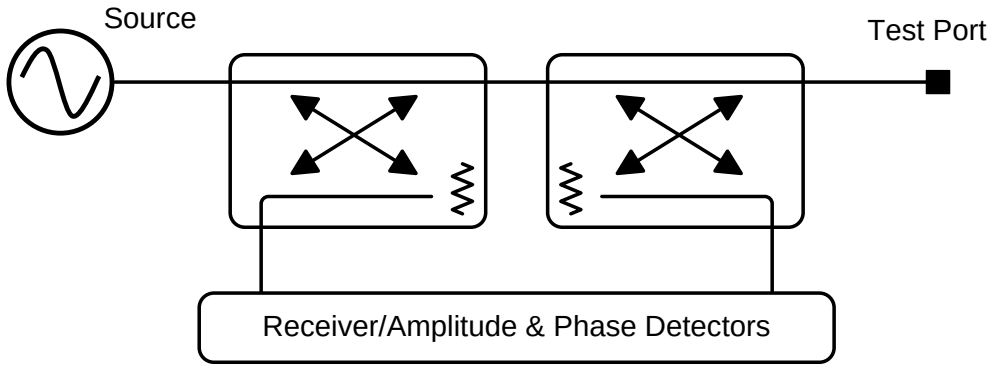


Figure 6-6. Vector network analyzer port

An alternative to this architecture is the multi-port reflectometer which does not employ phase detectors. The topology uses a multitude of amplitude detectors to calculate magnitude and phase of S-parameters. This allows the structure to achieve a wider bandwidth compared to the heterodyne architecture implemented in network analyzers; however, the simplicity of the multi-port hardware is compromised by

complicated calibrations which are required to account for imperfection of the multi-port topology. Additionally, [71] states that there is a trade-off between the power dissipated in the multi-port topologies and their bandwidth. For alternate test applications such as the tester-on-chip-on-board or the tester-on-chip-on-probe discussed in Chapter 1, multi-port reflectometers are advantageous compared to the trade-offs associated with heterodyne architectures. Multi-port techniques were subject to great deal of research since the publication of classic papers from NIST in the 1970's [72]. Moreover, multi-port reflectometer circuits are attractive in many applications beyond the one discussed here because of their low cost, wide bandwidth capability [73]. In this chapter, the discussion is limited to the introduction of this family of circuits especially since the focus of this chapter is to demonstrate applications for the detectors that were reported in the previous chapters. To sum up, the intent is to use these multi-port reflectometers as a vehicle to demonstrate the effectiveness of the amplitude detectors.

Figure 6-7 shows a six-port reflectometer (SPR) structure suitable for on chip integration that was published in [74]. The phase shifter is implemented using two inductors and a capacitor as seen in Figure 6-8 [74].

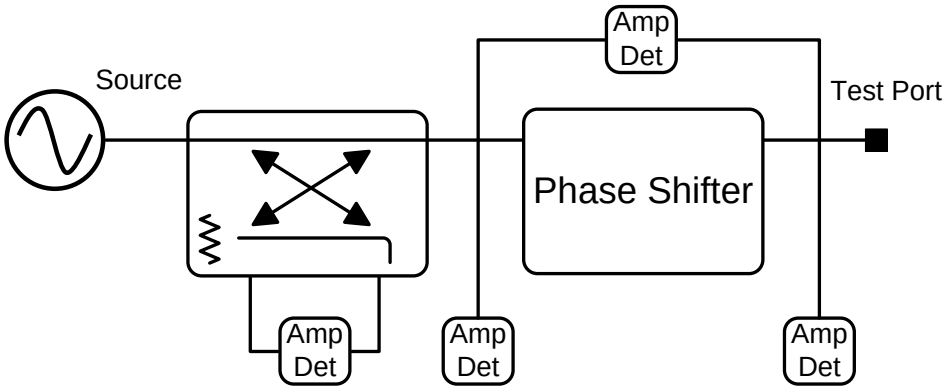


Figure 6-7. Six-port reflectometer port

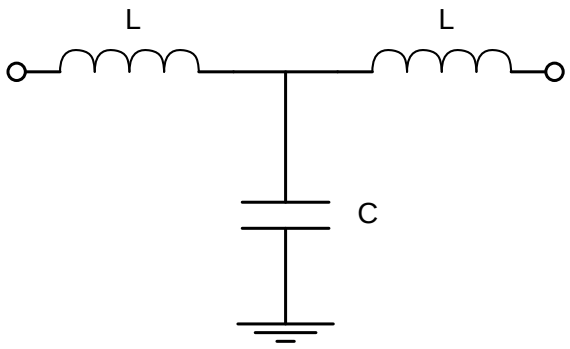


Figure 6-8. Phase shifter

The coupler is implemented using a resistive structure as seen in Figure 6-9. Where,

$$Ra * Rc = {Z_0}^2 \tag{6-1}$$

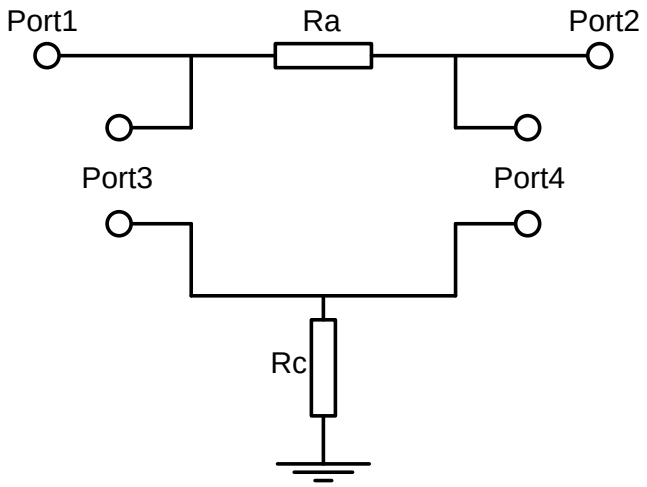


Figure 6-9. Wheatstone bridge

In Figure 6-7, port1 of the Wheatstone bridge is connected to the signal source; and port2 is connected to the phase shifter. [59] reports an S-parameter matrix for this bridge.

$$[S] = \begin{bmatrix} 0 & \frac{1}{1+Ra/Z_0} & \frac{1}{1+Rc/Z_0} & 0 \\ \frac{1}{1+Ra/Z_0} & 0 & 0 & \frac{1}{1+Rc/Z_0} \\ \frac{1}{1+Rc/Z_0} & 0 & 0 & \frac{1}{1+Ra/Z_0} \\ 0 & \frac{1}{1+Rc/Z_0} & \frac{1}{1+Ra/Z_0} & 0 \end{bmatrix} \tag{6-2}$$

Compact Multi-Port Reflectometers

Besides the motivations introduced in the previous section, this opportunity is exploited to propose novel multi-port topologies which might be beneficial for the proposed alternate test methodologies; though, it is difficult to envision employing these six-port networks for BIST purposes because of their large size and loss introduced in the signal path. Even a novel SPR topology introduced later in this chapter which is more compact and less lossy than the circuit in Figure 6-7 occupied .5mm^2 for a targeted operation around 5GHz using a 130nm technology. Therefore, it is hardly justifiable to use Multi-port circuits in BIST knowing that many specifications can be measured by amplitude detectors only. Yet, SPR circuits are suitable for tester-on-chip on-board or on-probe solutions as mentioned previously. Given these applications, design in CMOS is no longer a restriction since these alternate test circuits are not targeted for embedded test. As mentioned in Chapter 5, SiGe HBT differential detectors are superior over their bulk MOS counterparts because they are less sensitive to early voltage effects. Hence, SiGe HBT detectors were employed in all the circuits that are introduced in this section.

By inspecting the S-parameter matrix (6-2), port3 is isolated from port2; while a portion of the signal from port1 is transmitted to port3. Also, port4 is isolated from port1 despite the fact that it measures a portion of the signal incident from port2. Then, a detector in port3 can measure the magnitude of the forward wave *a1* incident from port1 and a detector in port4 can measure the magnitude of the wave *a2* reflected from port2 as seen in Figure 6-10. Thus, two differential detectors are sufficient to measure the magnitude of the reflection coefficient; on the other hand, two single ended detectors embedded at any nodes of the Wheatstone bridge network cannot measure the

reflection coefficient since there are three unknowns *a1*, *b2*, and *a2* (*b1=0* since $S_{11}=0$ from matrix (6-2)).

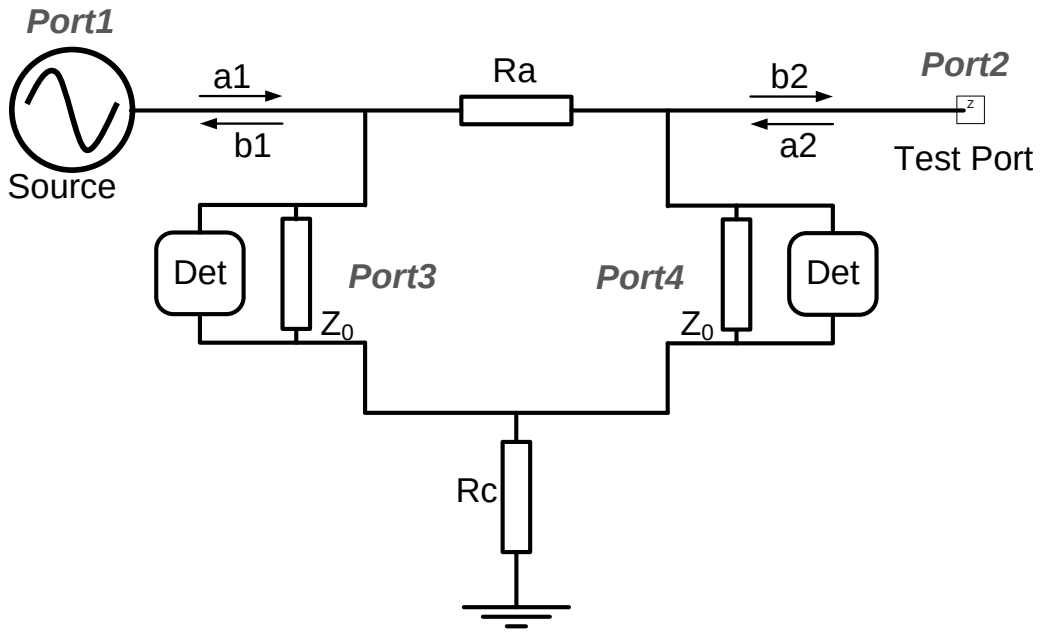


Figure 6-10. Wheatstone bridge for measurement of S-parameters' magnitude

The circuit in Figure 6-10 is equivalent to a single port in a scalar network analyzer which measures the magnitude of S-parameters. The following equations which characterize the circuit in Figure 6-10 can be solved to express the magnitude of the reflection coefficient Γ

$$b2 = S_{21} * a1$$
$$|a2| = \frac{A_{rev}}{|S_{42}|}$$
$$|a1| = \frac{A_{frwd}}{|S_{31}|}$$

where S_{xx} are the S-parameters from matrix (6-2), and A_{rev} is the amplitude measured by the detector across port4 in Figure 6-10, while A_{frwd} is measured by detector across port3. The equations simplify to

$$|\Gamma| = \left|\frac{a2}{b2}\right| = \left|\frac{A_{rev}}{S_{21} * A_{frwd}}\right| \quad (6\text{-}3)$$

Equation (6-3) shows that this network can only measure the magnitude of the reflection coefficient. This circuit was simulated with different loads and the results are summarized in Table 6-3 and Figure 6-11 showing that a worst case deviation from the ideal values of 1.6%.

Table 6-3. Comparing ideal and estimated reflection coefficients

Actual Γ	.5	-.5	.5∠58°	.5∠-58°	.5∠122°	.5∠-122°
Estimated Γ	.4995	.4494	.492	.507	.492	.507

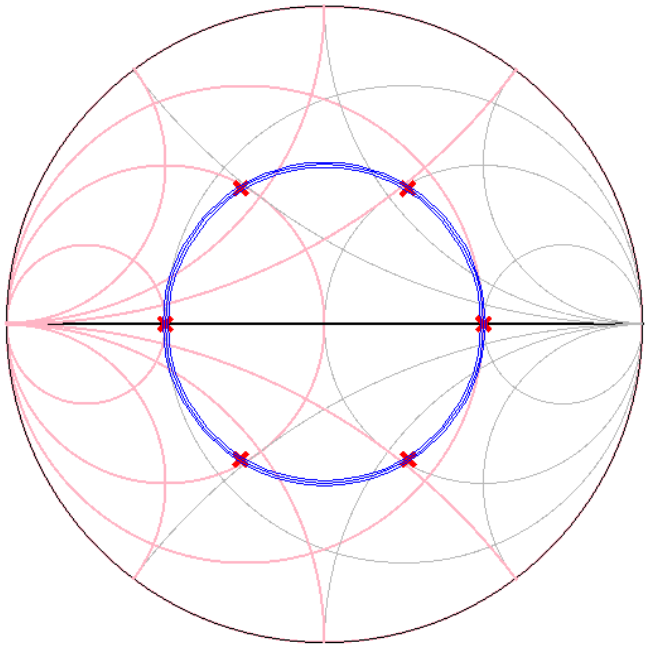


Figure 6-11. Smith chart showing ideal and estimated reflections coefficients

To measure the magnitude and phase of the reflection coefficient, multi-port reflectometer theory dictates the use of at least three amplitude detectors; additionally, a fourth detector is used to overdetermine the system so that it is robust to imperfections. The placement of the additional detectors onto the Wheatstone bridge as shown in Figure 6-12 allows measurements of the reflection coefficient over only two quadrants in the complex plane. This circuit can only resolve phase information from 0° to 180° since differential detectors have some phase ambiguity as they output the same value for signals with opposite phases.

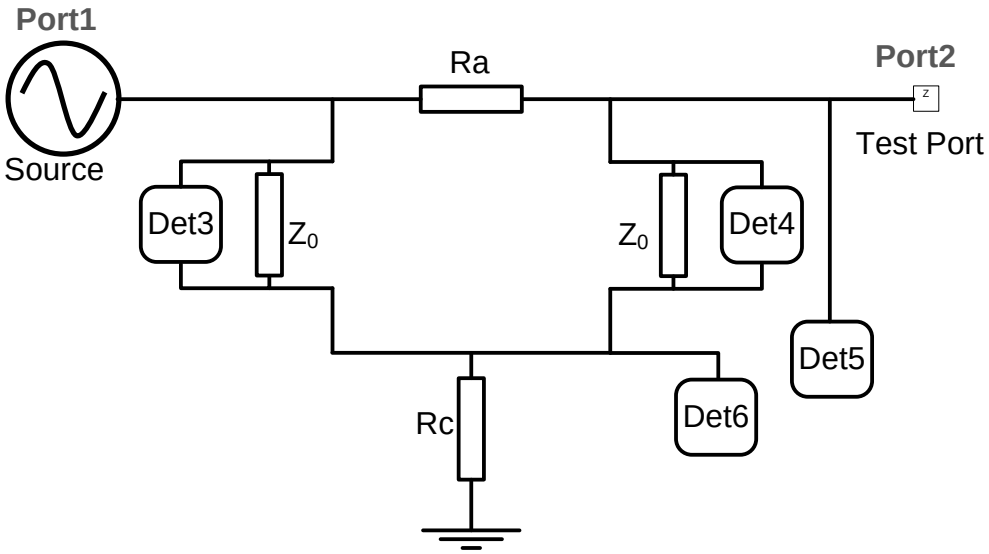


Figure 6-12. Circuit that measures S-parameters' magnitude and absolute value of phase

Multi-port reflectometers also require elements that can shift the phase of the waves across the multitude of amplitude detectors to measure the complex reflection coefficient. The SPR structure shown in Figure 6-7 dealt with this issue by using a phase shifter. In this dissertation, a new circuit which combines the phase shifter into the Wheatstone bridge is shown in Figure 6-13.

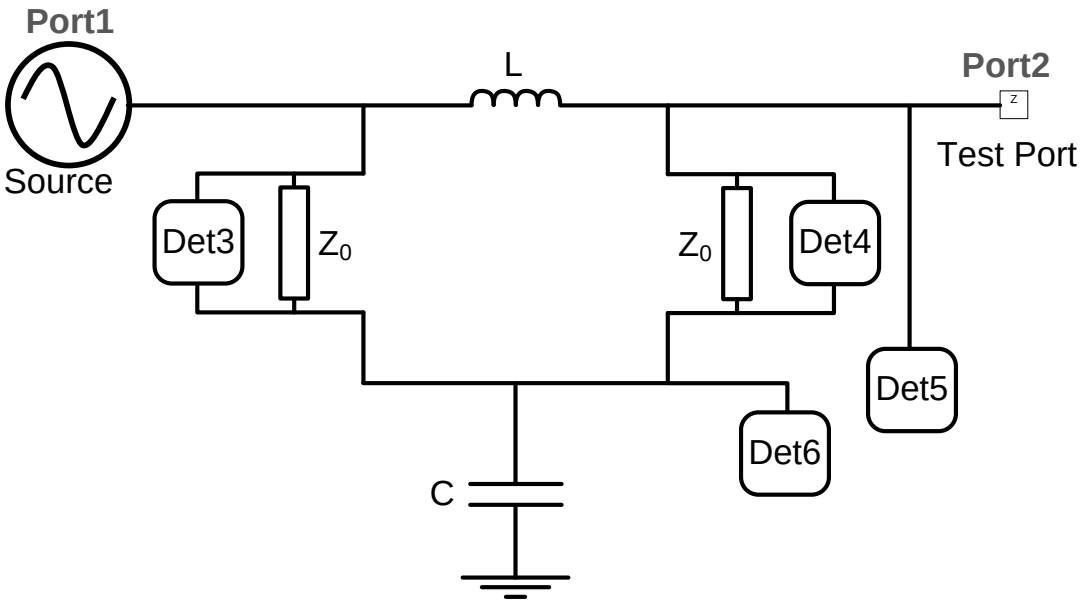


Figure 6-13. Compact six-port reflectometer

Figure 6-13 shows that inductor L and capacitor C replaced resistors Ra and Rc from Figure 6-12 respectively. To maintain the properties of the Wheatstone bridge, the following equation need to be satisfied

$$Z_L * Z_C = {Z_0}^2$$
$$\frac{L}{C} = {Z_0}^2 \quad (6\text{-}4)$$

This new SPR can fully measure phase and magnitude of Γ and contains a lower number of passives compared to the other structure. The topology shown in Figure 6-7 has four resistors, two inductors and one capacitor for the bridge and phase shifter. This proposed structure has just two resistors, one inductor and one capacitor.

Moreover, multi-port reflectometers, such as the circuit in Figure 6-7, somewhat deviate from the traditional definition of a reflectometer since they synthesize forward and reflected waves instead of directly measuring them. The circuit in Figure 6-13 reverts back as it embodies the traditional definition of a reflectometer; the circuit also relies on multi-port theory since it uses amplitude detectors only. [75] specifically argued against multi-port circuits that are based on the traditional reflectometer topology stating that the circuit's dynamic range is entirely dependent on the dynamic range of the detectors' that are used. For alternate test applications that do not require 100dB dynamic range such as the applications targeted in [75], use of the structure in Figure 6-13 is advantageous because of its compact structure. Additionally, the structure still maintains one of the key conditions for robust multi-port design such as correction for input's power fluctuations; multi-port theory is significantly simplified when one of the ports is proportional to the incident power [75].

In the most general case of SPR circuits, a 6x6 matrix constituted from the interactions between each of the ports' incident and reflected waves needs to be solved

to synthesize the waves at the port under test [73]. However, if the design of the SPR is constrained to certain conditions such as the ones discussed above, a graphical method can be used to solve for the reflection coefficient of the port under test.

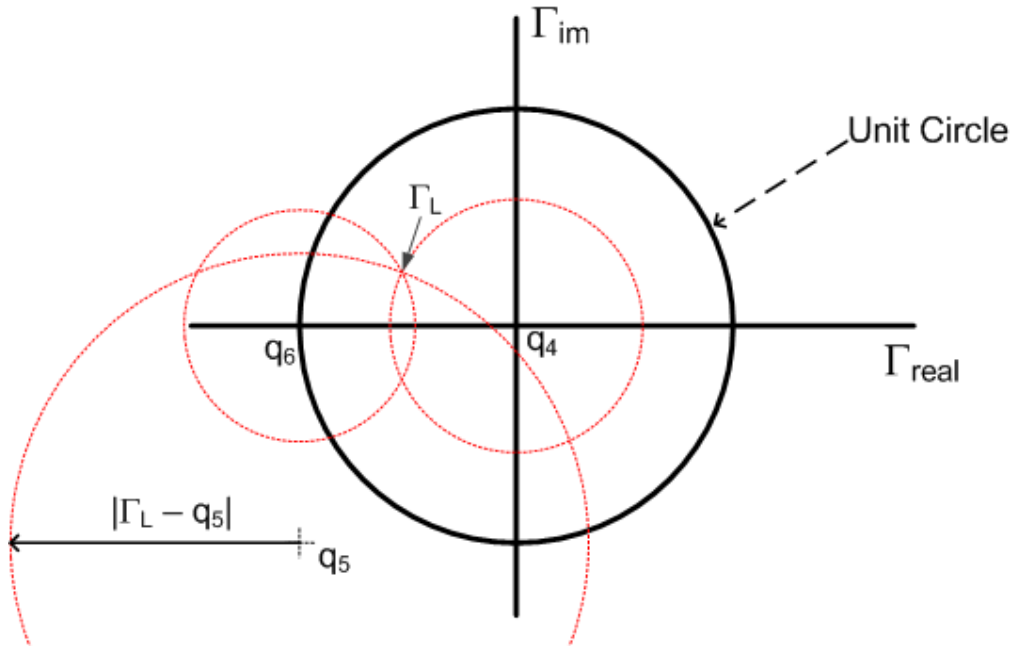


Figure 6-14. Graphical method to measure the reflection coefficient

Each SPR can be characterized by its q-points which are inherent to the circuit and are independent of the characteristics of the port under test [75]. The q-points cannot be collinear as was the case of the circuit in Figure 6-12 because two possible values of Γ are obtained. As seen Figure 6-14, the q-points of the circuit in Figure 6-13 are not collinear, thus, allowing measurements of the reflection coefficient since the three circles intersect at single point. Only readings from the amplitude detectors, which set the radii of the circles shown in Figure 6-14, are needed to estimate the reflection coefficient of the port under test. This method was applied to the circuit in Figure 6-13, and the results are summarized in Figure 6-15. The circuit estimates the reflection coefficient of a port under test within a certain error which can be minimized by implementing calibration methods. As previously mentioned, SPR are attractive

because of their hardware simplicity; however, their disadvantage is the painstaking complicated calibration needed to increase their accuracy which was extensively covered in the previous literature [73]. The simulation results in Figure 6-15 show raw measurement data which does not include any calibration method. The deviations arise from the fact that only second order was used to estimate the power levels at the input of each detector. Additionally, although the SPR was simulated with imperfections including non-ideal passive elements which constituted the network and parasitics from the detectors, ideal values in conjunction with the detectors' readings were used to calculate the estimated reflection coefficients. Nevertheless, Figure 6-15 shows that the compact SPR topology in Figure 6-13 is functional demonstrating that differential and single ended detectors are valuable.

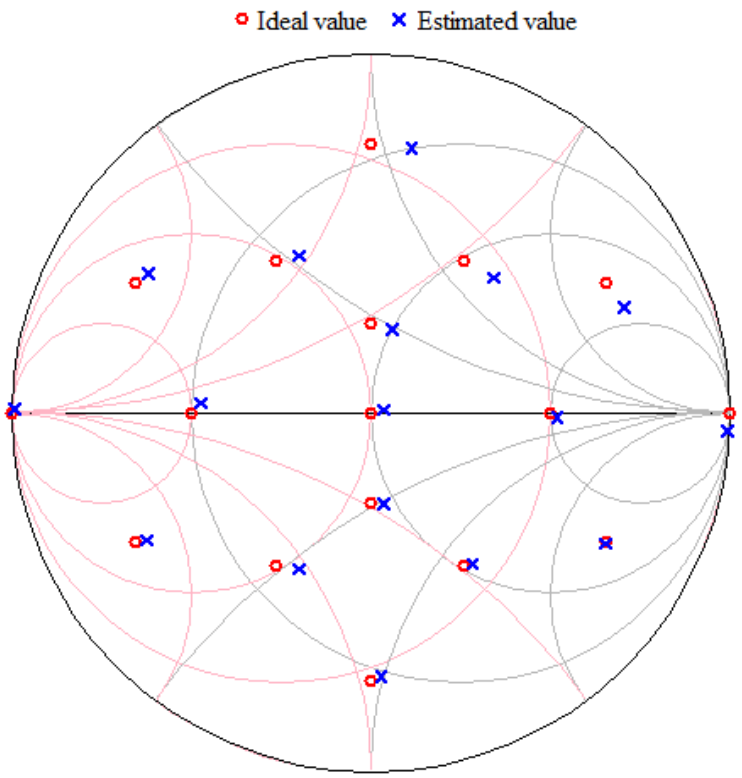


Figure 6-15. Smith chart showing reflection coefficients measured by the compact SPR

CHAPTER 7
SUMMARY AND SUGGESTIONS FOR FUTURE WORK

Summary

This dissertation discussed amplitude detectors which are appropriate for high frequency low-cost alternate test strategies. For RF-BIST, only simple test circuits with a strong correlation to the DUT's specifications can enable mainstream deployment. Along these lines, a simple, wideband, compact and non-invasive amplitude detector was indentified. The detector was used as a basis to report novel contributions with the hope of presenting simple design methodologies and improvements to standardize RF-BIST. The most significant contribution of this work was to identify key parameters which affect the detector's response. The dissertation also proposed simple techniques and minor modifications to the topology to increase the design space and offer flexibility which widens the range of practical applications. Additionally, these methods were projected onto a mixed-mode detector that is suitable for testing differential DUTs.

The dissertation started by deriving simple equations which describe the detector's response in key operating conditions which are the detector's operating region and input signal power level. Further analysis of the detector topology compared major detector specifications such as the detector's video bandwidth, static power consumption, accuracy in environmental and process variations, and dynamic range in each of the key operating conditions. A trade-off summary of each of these specifications is reported to offer simple parameterized design choices.

Furthermore, the most significant contributors which cause deviation of the detector's response were identified. Novel design methodologies and simple modifications were proposed to minimize these deviations as they affect the detector's

the dynamic range. The benefits of an increased dynamic range are two-folds; a larger set of applications can be targeted without requiring complex customization, increased accuracy can be achieved without resorting to complicated calibration methods.

Additionally, a compact, wideband true differential detector structure is identified which is also based on the simple detector topology discussed above. Besides analyzing the detector's response according to its operating conditions, sources of error in differential detection are also discussed for the first time. Additionally, the structure is improved to include common-mode detection capability without increasing the loading effects on DUT.

Finally, a chapter showing applications for these detectors is presented at the end.

Suggestions for Future Work

The success of RF-BIST hinges on the simplicity of the alternate test structures. Complicated methods cannot be used unless RF design becomes synthesizable like digital circuits. Until that happens, RF circuit designers will resist adopting any complicated test methods especially if they entail increase of the design cycle time. The motivation of this dissertation was to identify key parameters which affect the detectors the most; then attempt to simplify all the effects and offer solutions so that parameterized detector topologies can be offered or easily designed. Efforts along this path should be continued to expand the library of simple useful circuits, and hopefully, foundries can start offering alternate test IP part of their design kits.

Once universal test circuits that are strongly correlated to the DUT specifications become available, there is bound to be some post-processing of the alternate test response. Alternate test responses are very difficult to formalize to directly extract complicated specifications [76]; although, recent successes were reported in [24]. The

ATE industry, that is perennially agonizing to seek profitable business models, can hopefully adopt alternate RF test by at least working on post processing the output of the BIST circuits. I believe that the ATE industry can play a large role in adopting or developing efficient algorithms to lower test costs. Up to now, laudable efforts have surfaced such as the collaborative test advocated by [12]; nonetheless, this work was not targeting RF test.

In parallel, a new research area which seeks novel methods for self-healing of RF circuits is attracting a lot of interest [77], [78]. Developing these solutions is especially critical as vertical integration is gaining momentum and process variations effects increase in deeply scaled technologies. This new research area is monumental as there is a tremendous amount of topics to be explored as self-healing need to work on the system level, sub-component level, and even the transistor level.

APPENDIX
ONE PORT CALIBRATION

When testing detectors, the raw measured data is not consistent with simulations as shown in the graph below. The plot in Figure A-1 compares uncalibrated measurement results to simulation results of a detector. The RF input frequency is swept from 300MHz to 3GHz while keeping the RF input power level in the signal generator constant at 0dBm. Ideally, the curves are supposed to be flat since the input power is constant. The simulation results show that the output DC voltage is constant from 1.2GHz to 3GHz. The roll off for frequencies lower than 1.2GHz is due to the use of small on-chip coupling capacitors. But the curve of interest here is that of the uncalibrated results. For that curve, the DC output decreases as the frequency increases. This loss pattern is consistent with cable insertion loss. Therefore, we need to account for the measurement setup losses. Some measurements like S-parameters are ratioed measurements and do not need an exact power level. The only requirement for the power in that case is to maintain a small signal level that is above the noise level. Detector measurements require knowing the exact power level at the input of the DUT.

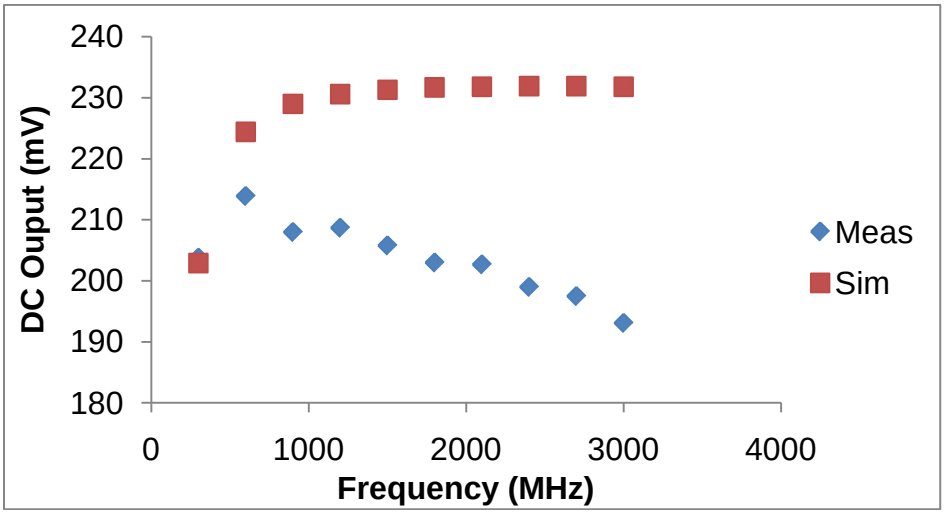


Figure A-1. Uncalibrated measurement and simulation results

Modern VNAs have a capability that accounts for insertion loss in the measurement setup that is called source power calibration. It calibrates the VNA so that the power is constant at a reference plane across the swept parameter range. This setup requires a power meter, and it is fairly easy to do. In case this equipment is not available, calibration has to be done manually. There is a detailed analysis of this approach in this reference [79]. This analysis is called one-port calibration and will allow us to know the exact power level at the input of the DUT. It moves the reference plane all the way to the probe tips by taking into account non-idealities in the measurement setup. This technique is explained in Figure A-2.

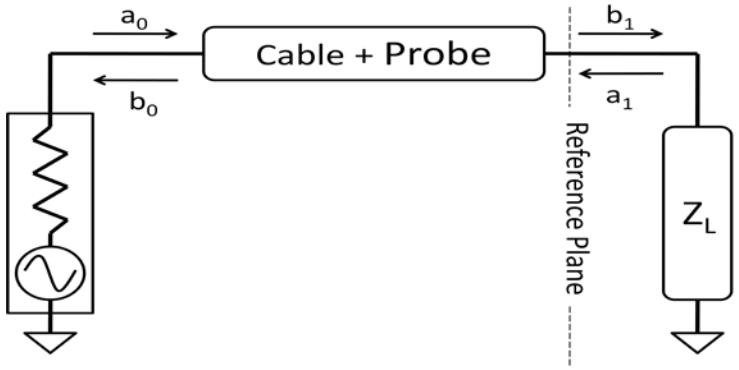


Figure A-2. Forward and reverse waves at different points in the measurement setup

The power at the output of the signal generator is

$$P_{meas} = \frac{1}{2}(|a_0|^2 - |b_0|^2) \tag{A-1}$$

where a_0 and b_0 are the incident and reflected peak waves. The actual power displayed in the signal generator is the available power

$$P_{avail} = \frac{|a_0|^2}{2} \tag{A-2}$$

The available power is equal to the measured power when the system is perfectly matched as there is no reflection which makes b_0=0. However, the actual power

delivered to the load might be different. From Figure A-2, the load power can be defined such as

$$P_{load} = \frac{1}{2}(|b_1|^2 - |a_1|^2) = \frac{|b_1|^2}{2}(1 - |\Gamma_{load}|^2) \quad \text{(A-3)}$$

In [79], an error-adapter network is defined to model the errors in the measurement setup. This hypothetical error adapter is shown in Figure A-3. This network has three types of errors:

- Directivity error e_{00}: represents the signals that are reflected at the discontinuity between the signal source reference plane and the cable.
- Frequency response errors e_{10} and e_{01}: represent the transfer function from the port of the signal source to the load under test.
- Port match error e_{11}: represents the reflection caused by the mismatch between the load and the impedance looking backward into the error network.

This network allows us to link the actual waves a_1, b_1 to the measured waves a_0 and b_0.

$$b_1 = a_0 * e_{10} + a_1 * e_{11} \quad \text{(A-4)}$$

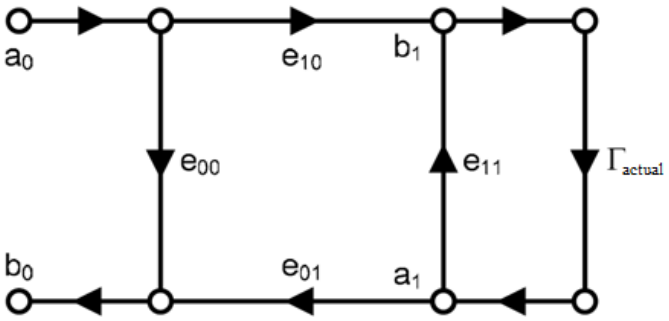


Figure A-3. Hypothetical error adapter network

This becomes

$$b_1 = \frac{a_0 * e_{10}}{1 - \Gamma_{load} * e_{11}} \quad \text{(A-5)}$$

To calculate P_{load}, we have to calculate the errors represented by the hypothetical error adapter network. By doing a Short-Open-Load (SOL) calibration to the error network, [79] derives the following equations.

$$e_{00} = \Gamma_{meas-load} \tag{A-6}$$

$$e_{11} = 1 - 2 * \frac{\Gamma_{meas-load} - \Gamma_{meas-short}}{\Gamma_{meas-open} - \Gamma_{meas-short}} \tag{A-7}$$

$$e_{01}e_{10} = 2\frac{(\Gamma_{meas-open} - \Gamma_{meas-load})(\Gamma_{meas-load} - \Gamma_{meas-short})}{(\Gamma_{meas-open} - \Gamma_{meas-short})} \tag{A-8}$$

where $\Gamma_{meas-load}$ is measured by terminating the measurement setup with 50Ω, $\Gamma_{meas-short}$ is measured by a short as a load, and $\Gamma_{meas-open}$ is measured by using an open load. Please, note that at very high frequencies open, short, and load using the calibration substrate have parasitics. These should be accounted for by entering the values into the VNA's calkit. [79] states that in practice, the terms e_{01}, e_{10} cannot be distinguished from each others. Furthermore, in our measurement setup, the cables and the probes are passive. Therefore, we can assume that $e_{10} = \sqrt{e_{01}e_{10}}$. Now, the last remaining piece of the puzzle to calculate P_{load} is to derive the actual reflection coefficient Γ_{load}. This is given in [79] as:

$$\Gamma_{load} = \frac{\Gamma_{meas} - e_{00}}{e_{11} * (\Gamma_{meas} - e_{00}) + e_{01} * e_{10}} \tag{A-9}$$

where Γ_{meas} refers to the reflection coefficient measured by the VNA when the probe is landed on the DUT. By substituting equations (A-5) into (A-3), the power at the load becomes

$$P_{load} = \frac{1}{2}\left|\frac{a_0 * e_{10}}{1 - \Gamma_{load} * e_{11}}\right|^2 (1 - |\Gamma_{load}|^2) \tag{A-10}$$

Using equation (A-2),

$$P_{load} = \left|\frac{e_{10}}{1 - \Gamma_{load} * e_{11}}\right|^2 (1 - |\Gamma_{load}|^2) * P_{avail} \tag{A-11}$$

The first term $\left|\frac{e_{10}}{1-\Gamma_{load}*e_{11}}\right|^2$ in the equation represents the loss associated with the measurement setup. The second term $(1-|\Gamma_{load}|^2)$ represents the power loss due to the mismatch between the source impedance and DUT input impedance. Therefore, we can now derive an equation for an ideal source power. Let's call this source power $P_{avail-cal}$, which is a calibrated version of the raw measurement power P_{avail}. The intent in this derivation is to compare measurement results to simulations.

$$P_{load} = (1-|\Gamma_{load}|^2) * P_{avail-cal} \quad \text{(A-12)}$$

Substituting (A-11) in (A-12), the calibrated (simulation) power is

$$P_{avail-cal} = \left|\frac{e_{10}}{1-\Gamma_{load}*e_{11}}\right|^2 * P_{avail} \quad \text{(A-13)}$$

where P_{avail} is the raw measurement available power. It is the power displayed by the signal generator.

Furthermore, power detectors may require knowing the actual power at the input of the detector. However, amplitude detectors may require knowing the actual voltage. Therefore, it is necessary to derive an equation for the actual voltage V_{load} as well.

$$P_{load} = \frac{|V_{load}|^2}{2*|Z_L|^2} * Re(Z_L). \quad \text{(A-14)}$$

The impedance Z_L can be derived from the previously calculated Γ_{load} as shown below

$$Z_L = \frac{1+\Gamma_{load}}{1-\Gamma_{load}} * R_s. \quad \text{(A-15)}$$

R_s represent the source impedance. Also, P_{avail} is defined such as

$$P_{avail} = \frac{|V_s|^2}{8*R_s}. \quad \text{(A-16)}$$

By substituting equation (A-12), (A-13), and (A-16) into equation (A-14), the voltage across the input of the DUT is:

$$|V_{load}| = \sqrt{\left|\frac{e_{10}}{1-\Gamma_{load}*e_{11}}\right|^2 (1-|\Gamma_{load}|^2) * \frac{|Z_L|^2}{4Re\{Z_L\}*R_s}} * V_s. \quad \text{(A-17)}$$

This equation is used for an input source with 50Ω impedance. When the load is exactly matched, the reflection coefficient becomes $\Gamma_{load} = 0$. Then equation (A-17) becomes

$$V_{load} = \frac{|e_{10}|}{2} * V_{in}. \tag{A-18}$$

But when the detector is high impedance, $\Gamma_{load} = 1$ and equation (A-17) becomes

$$V_{load} = \left|\frac{e_{10}}{1 - e_{11}}\right| * V_{in}, \tag{A-19}$$

because

$$\lim_{Z_L \to \infty} (1 - |\Gamma_{load}|^2) * \frac{|Z_L|^2}{4Re\{Z_L\} * R_s} = 1. \tag{A-20}$$

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