TRANSMITTER FOR WIRELESS INTER-CHIP DATA COMMUNICATIONS

By

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To my parents and my sister

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Chair: Kenneth K. O
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The dramatic fluctuation of gasoline price is a major concern for all. Hybrid electric vehicles with ~ 2 times higher fuel efficiency have drawn lots of attention in the last few years. In order to replace costly photo-couplers used in hybrid engine controller boards, silicon based solutions are utilized to suggest the feasibility to lower cost and increase data rate.

This dissertation presents the design of an electronic isolator using inductive coupling fabricated in the UMC 130-nm mixed mode CMOS process. It can achieve 70-V DC isolation and around 160-MHz data transmission rate while drawing ~ 22 mA. It only occupies 0.52 mm^2, which is 3 times smaller, compared to the isolators using a capacitive coupling method. The electronic isolator is designed to provide sufficient isolation of high and low voltages coexisting in the same board. It can be used in RS-232 and IEEE 1394 applications.

The channel characteristics including antenna pair gain and delay spreads at 24-GHz in a printed circuit board for controlling hybrid engines with and without a metal cover are characterized using a 3-mm on-chip dipole antenna pair. At a 15-cm separation, the antenna pair gain can be improved by ~10 dB with a metal cover ~ 3.5 cm above the PCB and the maximum excess delay can be reduced to ~ 1.1 ns from ~ 16.5 ns, which is acceptable for recovery of clock

and data for a 400 Mchip/sec system. It has been verified that on-chip dipole antennas can be used for wireless communication in the hybrid engine controller board.

Wireless interconnection using two separate wireless transceivers can operate with two different ground potentials that have large difference. A fully-integrated CDMA transmitter with an on-chip dipole antenna operating at 16.8 GHz fabricated in the UMC 130-nm CMOS process is demonstrated. It supports 7 signal levels with a 16.8-GHz carrier and 400-Mbps data rate. It includes a PLL, divider chains, a double balanced Gilbert cell up-conversion mixer, a power amplifier (PA), attenuators, a digital coder, a duplexer, and a 4-mm on-chip dipole antenna. The PA used in the transmitter chain can achieve 10-dBm saturated output power and ~ 22-% maximum PAE. Most of the rise and fall times are around 200 ps. The worst case is 800 ps for the level 0 to level 2 transition. The CDMA transmitter occupies ~ 5.2 mm^2 and consumes 198 mW.

A bus interconnected with wireless links on a printed circuit board in which multiple sets of devices/chips can simultaneously communicate and control signals can be broadcasted to multiple devices has been presented in the dissertation. A gold bond wire with ~ 1-mil diameter is co-optimized with a bond pad to resonate at ~ 60 GHz. With a metal cover representing an enclosure for an electronic system (2-mm from a printed circuit board), the antenna pair gain at 10-cm separation is ~ -53 dB including the effects of two nearby bond wires located 300 μm away. This is sufficient for building an inter-chip 1-Gbps radio link with bit error rate of 10^{-12}. The bond wire antennas should also be useful for general purpose over the air communication in the 60-GHz unlicensed band.

CHAPTER 1
INTRODUCTION

1.1 An Overview of a Hybrid Control Board System

The dramatic fluctuation of gasoline price is a major concern for all. Hybrid electric vehicles (HEV's) with ~ 2X higher fuel efficiency have drawn lots of attention in the last few years [1]-[4]. Use of HEV's also reduces carbon dioxide emission, which is good for environment. However, hybrid vehicles are usually more expensive than regular vehicles, which slows their adoption. Lowering the manufacture cost is the key to cut down the selling price of HEV's. The hybrid engine controller board (also called as inverter board) is a part of HEV's. The main goal of this research is to find a way to replace photo-couplers used in the board by using complementary metal oxide semiconductor (CMOS) technology, which will alleviate the cost problem, and increase data transmission rate.

1.1.1 Challenge to Replace Photo-Couplers

A hybrid engine controller board shown in Figure 1-1 is $25 \times 15 \times 6$ cm^3. High voltage (>300 volt (V)) motor driver section and low voltage (3-12 V) control section coexist in the same board. Presently, high-low voltage interface is isolated by photo-couplers. Usually, the data transmission rate for photo-couplers is 1 Mbps or 10 Mbps. It is lower than the speed of on-chip isolators, which can achieve data transmission rate of 100 Mbps or even higher. A photo-coupler with cost of ~ $1 or higher is significantly costly compared with silicon based solutions. However, photo-couplers usually can handle high isolation voltage up to few thousand volts, which is challenging to achieve using pure CMOS approaches. Nevertheless, the higher data rate, higher integration level, and lower cost are attractive. Approaches for handling the high isolation voltage is need for CMOS implementation.

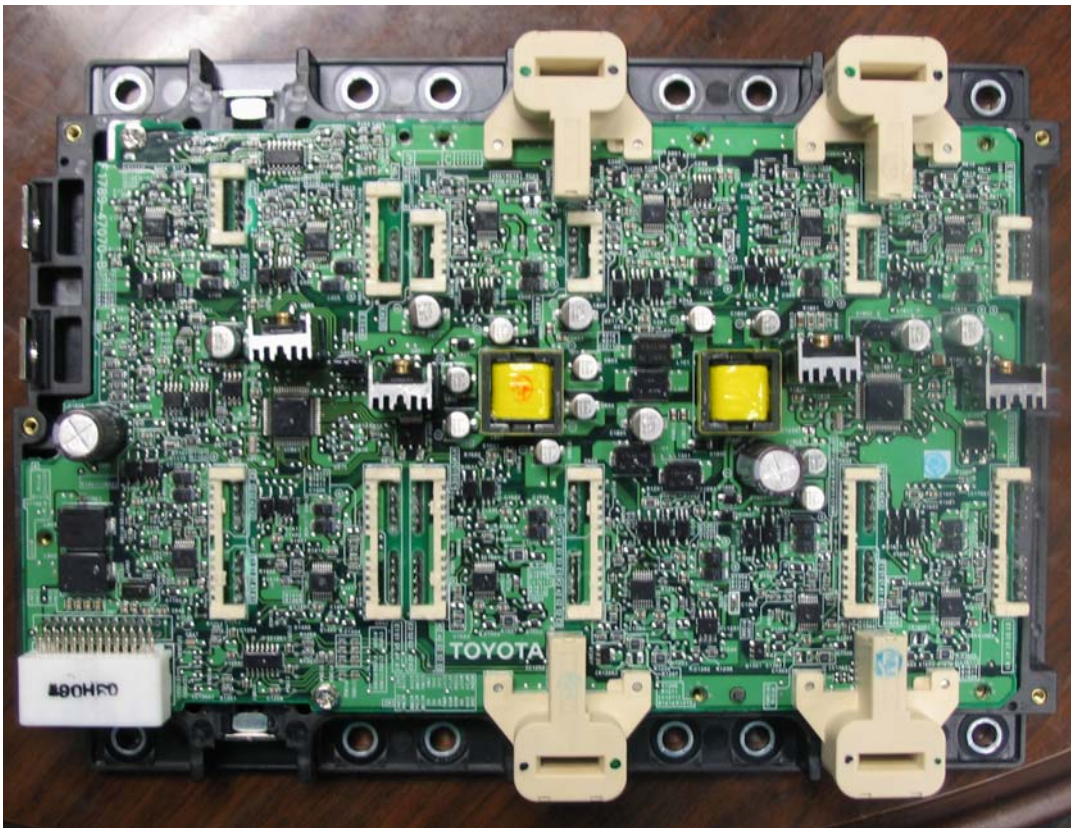


Figure 1-1. Toyota hybrid engine controller board (25× 15 × 6 cm^3).

1.1.2 Potential Solutions

The main concern for replacing photo-couplers using mainstream CMOS technology is the breakdown voltage. A potential solution is to increase the breakdown voltage. For this particular application, a CMOS isolator must be able to withstand 300-V ground potential difference between high and low voltage sections in the board. Using CMOS isolators can reduce cost by a factor of 4 times or even higher.

The second potential solution is use of "wireless interconnects." An on-chip antenna is the key to implement this. On-chip antennas have been extensively studied [5]-[7] in both indoor and outdoor environment and are integrated with other circuit blocks to form receiver and transmitter chains for wireless communications above 20 GHz [8] [9]. Two separate wireless

Table 1-1. Link margin analyses for CDMA link.

CDMA Link	
Transmission range	15 cm
TX power/Channel (Total power ~ 10 dBm)	2 dBm
Propagation Loss @ 16.8 GHz $(\lambda/4\pi R)^2$	41 dB
Antenna Gain (0.25λ = 3.2 mm)	-7 dB
Received power	-53 dBm
Thermal Noise [kT (^oK)]	-173.8 dBm/Hz
Bandwidth (50 MHz)	77 dB
E_b/N_o for BER of $1x10^{-13}$ for ASK	14.5 dB
RX noise figure	8 dB
Sensitivity	-74.3 dBm
Link margin	21.3 dB

transceiver integrated circuits can operate with two different ground potentials to handle the large voltage difference. Using wireless interconnects can also increase data transmission rate, lead to smaller chip area, and eliminate wiring traces on the board. Of course, they can also cost less.

The inverter board is used with a metallic enclosure on the top. The wireless channel on the PC board will be a multi-path rich environment, which is expected to be difficult for wireless communications. The performance of on-chip dipole antennas should be re-evaluated in the inverter board in a metallic enclosure to determine the feasibility of the approach. Table 1-1 shows the link margin analysis, typically used for conventional channels. This should be acceptable, however, it does not account for the multiple path effects. The multi-path effects are discussed in Chapter 3.

1.2 An Overview of Bond Wire Antennas

It has been demonstrated that CMOS technology is suitable for a wide range of wireless applications, such as wireless clock distribution [10]-[18], wireless interconnects [19] [20], and inter and intra-chip communications [5], etc. However, as the operating frequency increases, package may have more significant impact on the wireless transceiver performance. When the operating frequency is increased to 60 GHz or higher, bond wire lengths become comparable to

that of wavelengths. This will make bond wire to be an efficient radiator and could be used for inter-chip data communication.

The wireless interconnects could be used to relieve the packaging cost problem of integrated circuits with a large number of I/O pins. Referring to the 2003 SIA's International Technology Roadmap for Semiconductor (ITRS), at 35-nm technology generation or in year 2012, the number of pins in packaged chip will be on the order of 1000-5000. Of these, ~35%, or ~350 to 1750 pins will be I/O pins. Use of wireless interconnects by reducing the number of traces in printed circuit boards (PCB's) can simplify the PCB construction, and reduce size and cost [5], shown in Figure 1-2.

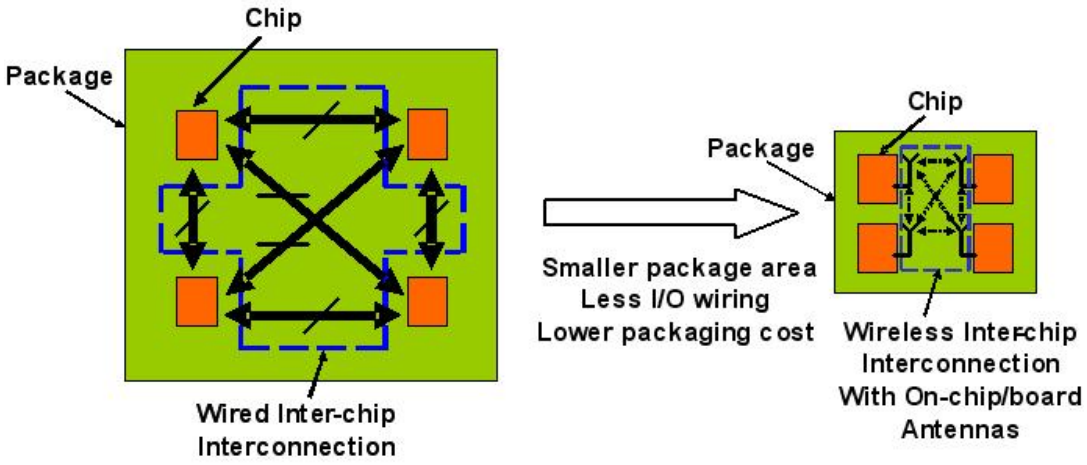


Figure 1-2. Wireless links can be used to form a bus in which multiple devices can communicate at the same time. Use of this can also lead to smaller package area, fewer I/O pins and lower cost.

1.3 Organization of the Dissertation

This research focuses on replacing photo-couplers in the hybrid engine controller board using mainstream CMOS technology. The solutions should provide the advantages of lower cost, higher data transmission rate, easy to use, smaller area consumption, and higher integration level. The electronic isolator design is discussed in Chapter 2. On-chip transformers design, circular triple-well technique, and circuit architecture are presented. Double-layer inductors are used to

achieve higher inductance per unit area to implement transformers in limited space. On-chip isolators using mixed-mode 130-nm CMOS technology that can achieve higher data transmission rate of ~ 160 MHz with 70-V isolation voltage is described.

Chapter 3 describes the channel characteristics in the hybrid engine controller board. A 3-mm on-chip dipole antenna pair is used to characterize antenna pair power gains and time delay spreads. These are used to model the multiple path effects at 24 GHz. The wave propagation behavior in the board has been investigated for two cases, with and without a metal cover. The maximum excess delay is ~ 1.1 ns at 15-cm separation for the case with a metal cover, which is acceptable for recovery of clock and data for a 400-Mchip/sec system, which suggests that wireless communication using on-chip dipole antennas in the inverter board is feasible.

Chapter 4 discusses the code division multiple access (CDMA) transmitter chain design. It includes a mixer, a power amplifier (PA), a digital coder, a Phase-Locked Loop (PLL), divider chains, a duplexer, attenuators, and a 4-mm on-chip dipole antenna. The multi-level PA capable of supporting 7 levels with 400-Mbps wireless data transmission rate is presented. The single-ended PA fabricated in the 130-nm CMOS foundry process can achieve 10-dBm saturated output power with ~ 22-% maximum PAE while consuming 45.75 mW. The transmitter chain is characterized in frequency and time domains separately. The measurement results demonstrate that it is feasible to build the radio link to transmit CDMA signals using an amplitude shift keying (ASK) modulation scheme.

Chapter 5 presents bond wire antennas operating at ~ 60 GHz. A gold bond wire with ~ 1-mil diameter is co-optimized with a bond pad to resonate at ~ 60 GHz. With a metal cover representing an enclosure for an electronic system (2-mm from a printed circuit board), the antenna pair gain at 10-cm separation is ~ -53 dB including the effects of two nearby bond wires

located 300 μm away. This is sufficient for building an inter-chip 1-Gbps radio link with bit error rate (BER) of 10^{-12}. The bond wire antennas should also be useful for general purpose over the air communication in the 60-GHz unlicensed band

Finally, the summary and suggested future work is described in Chapter 6.

CHAPTER 2
ELECTRONIC ISOLATOR DESIGN

2.1 Introduction

In order to develop an alternative to more costly photo couplers, an electronic isolator that can implement in CMOS has been investigated. Photo-couplers are conventional components used for data transmission and isolation of high-low voltages coexisting in the same board. Electronic isolators should be able to support a higher data transmission rate and help to reduce cost by a factor of 4 times or even higher. The grounds can be isolated by coupling signals. There are two ways. One is capacitive coupling and the other is inductive coupling. Several papers using capacitive coupling method in silicon on insulator (SOI) technology are reported in [21]-[23]. It has been shown that the isolator can achieve 2.3kV ac isolation and 100-MHz signal transmission in an area of 1.5 mm^2 [23]. This approach however, requires a larger space than the isolators using an inductive coupling method. Inductive coupled interconnects have been proposed for inter-chip data communication as well as that in 3D system [24]. This chapter presents the design of an electronic isolator using inductive coupling fabricated in the UMC 130-nm mixed mode CMOS process for lower cost. The isolator can achieve 70-V DC isolation and around 160-MHz data transmission rate while drawing ~ 22 mA. It only occupies 0.52 mm^2, which is 3X smaller, compared to the isolators using capacitive coupling method.

2.2 Transformer Design

The electronic isolator design includes a transformer, a transmitter and a receiver. The 1:1 transformer is designed to use double-layer inductors. By using double-layer inductors, higher inductance per unit area can be achieved [25]. The lower inductor needs to be connected with upper inductor in a way such that the currents produced by both inductors flowing in the same direction [26], shown in Figure 2-1. In transformer design, the magnetic coupling coefficient

depends strongly on the separation distance between primary and secondary inductors. A closer separation increases the coupling coefficient. M7 (metal 7 layer) and M8 are designed to be used in series to form the primary inductor and M56 (shunt M5 and M6) and M34 (shunt M3 and M4) are used in series to form the secondary inductor. Lower metal layers usually have higher sheet resistance due to their thinner thickness. Therefore, metal conduction loss can be reduced by shunting 2 metal layers together, which is the other key to improve the transformer performance.

The vertical separation between M6 and M7 is 0.615 μm, which is fixed by the chosen technology. Besides the high coupling coefficient for the transformer, a high breakdown junction voltage is needed for high voltage isolation. The isolation voltage between the windings of the transformer is determined by the dielectric, SiO_2, thickness between them. Theoretically, a 1-μm thick SiO_2 layer can withstand 1000 V. 0.615-μm SiO_2 thickness should be sufficient to provide 300-V DC isolation.

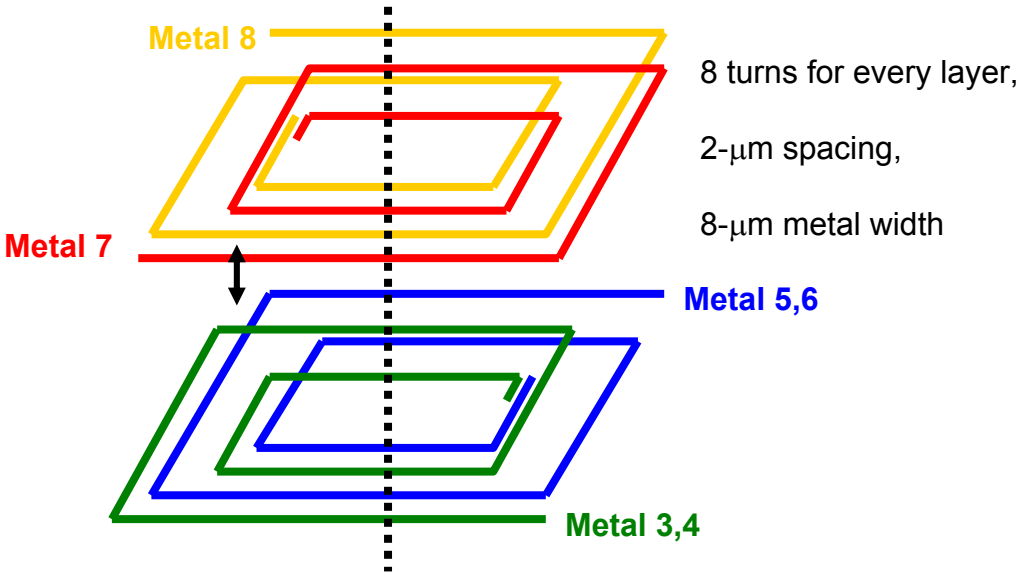


Figure 2-1. Double-layer inductors are used for the transformer design.

2.3 Circular Triple-Well Design

In order to support floating grounds, which can be around 300 V, it is important to have junctions with breakdown voltage greater than 300 V in 130-nm CMOS process. Therefore, the triple well structure, shown in Figure 2-2, has been used for this particular application. There is a T-well region inside the n-well region. Therefore, NMOS transistors can be placed in the T-well instead of in a regular p-well in p-type substrate. For this application, high breakdown voltage is required for the junction between deep n-well and substrate. On the other hand, the junction between T-well and deep n-well only has to handle 1.2-V difference, so there is no serious breakdown voltage requirement for this junction. If the junction between the deep n-well and substrate is smoother, the breakdown voltage will be higher [27]-[29]. Hence, a circular well structure is used to improve the junction breakdown voltage, shown in Figure 2-3. We also separate p-well region far away from deep n-well region (40-μm separation), shown in Figure 2-2 to prevent the breakdown between deep n-well and p-well occurring before the deep n-well to substrate breakdown. At the same time, p-well block layer (PWBLK) is used to form an un-doped substrate region, shown in Figure 2-3, for increasing the breakdown voltage.

According to Eq. (2-1) [30],

$$V_B = 60 \times \left(\frac{E_g}{1.1} \right)^{1.5} \times \left(\frac{N_B}{10^{16}} \right)^{-0.75}, \tag{2-1}$$

where V_B is the breakdown voltage, N_B is the impurity density, and E_g is the silicon energy gap, which equals to 1.12 eV. It is possible to achieve breakdown voltage exceeding 300 V by having an un-doped substrate region with 20-Ω-cm resistivity, shown in Figure 2-4. In addition to having triple well and the structure with a 20-Ω-cm substrate region, another structure with a polysilicon layer for potentially gating the surface is fabricated to investigate the possibility for

further improving the breakdown voltage. The idea is to adjust the field strength underneath polysilicon gate area to possibly increase the breakdown voltage.

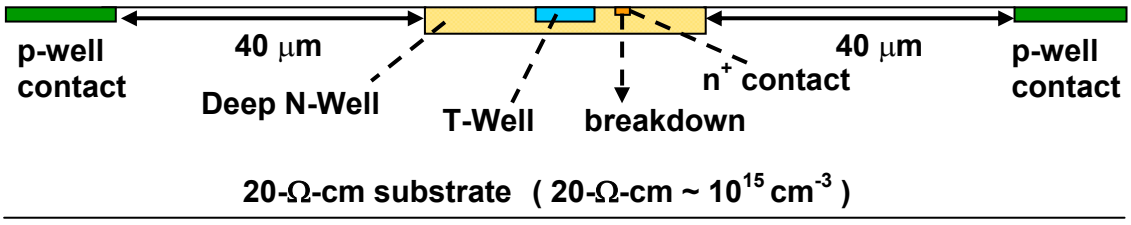


Figure 2-2. Triple well structure - Cross-sectional view.

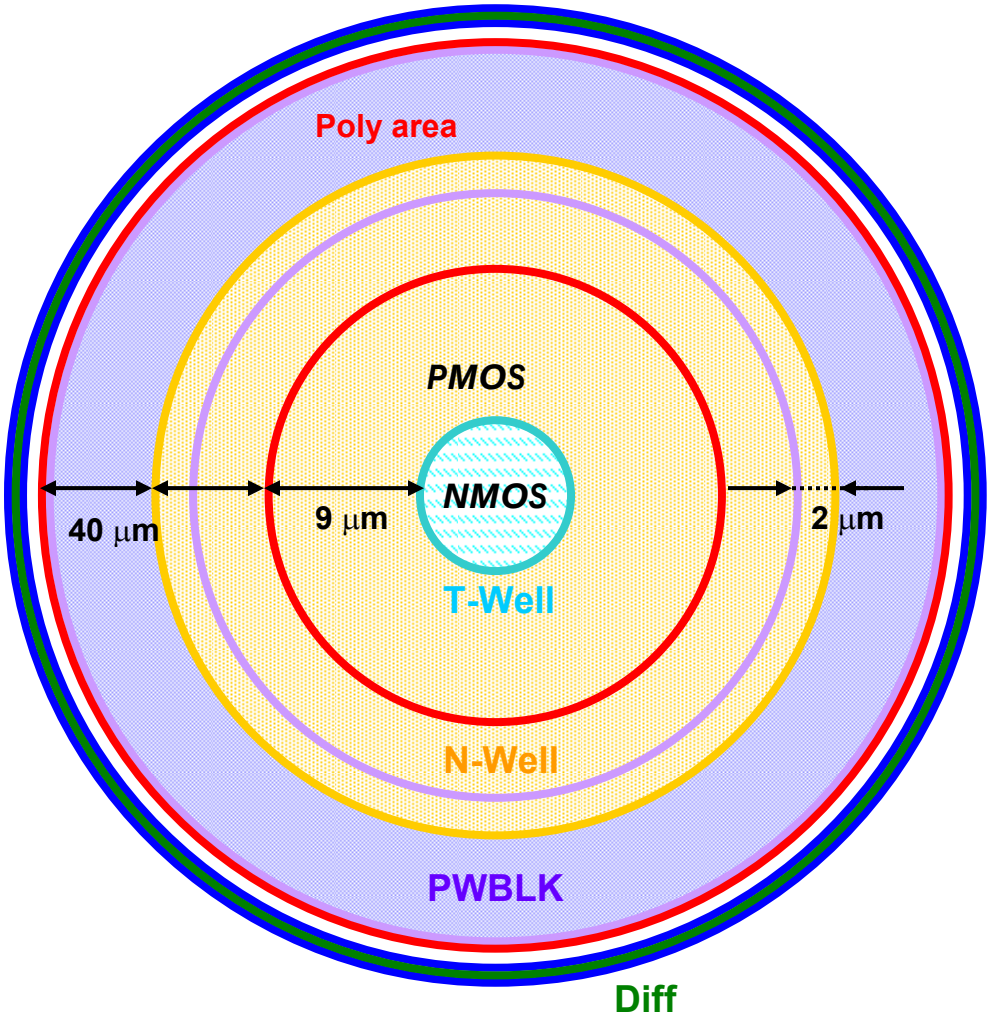


Figure 2-3. Circular triple well structure - Plane view.

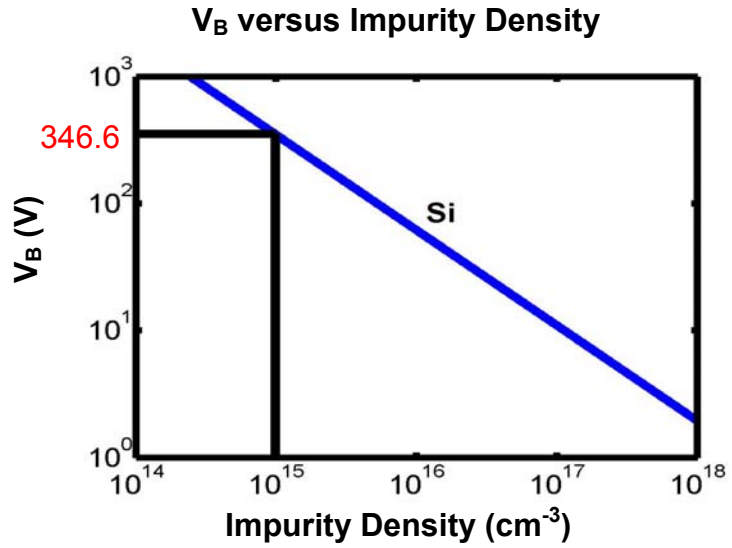


Figure 2-4. Theoretical plot of breakdown voltage.

2.4 Circuit Architecture and Measurement Results

Figure 2-5 shows the circuits built in the triple well structure. It is possible to have 0-V ground potential at the transmitter side and have 300-V ground potential at the receiver side, or vice versa. Therefore, circular triple well technique is applied for both transmitter and receiver sides. All NMOS transistors are placed in the T-well region and all PMOS transistors are placed in the n-well region. Metal connections are used to connect NMOS and PMOS transistors. Sinusoidal signal is applied at the transmitter input and passes through an inverter chain to form a square wave before applied to the transformer. Two inverter chains with 3 and 4 stages are used to generate 180-degree phase difference at the transformer input. The AC signal would be coupled inductively from the primary to the secondary. The coupled signal passes through a DC bias circuitry to be biased between 0 to 1.2 V or 300 to 301.2 V depending on the floating ground potential, and amplified by a sense amplifier. Finally, an inverter chain and a latch hold the signal from transformer to recover the square waveform. Figure 2-6 shows the simulated waveforms at different nodes of the circuits.

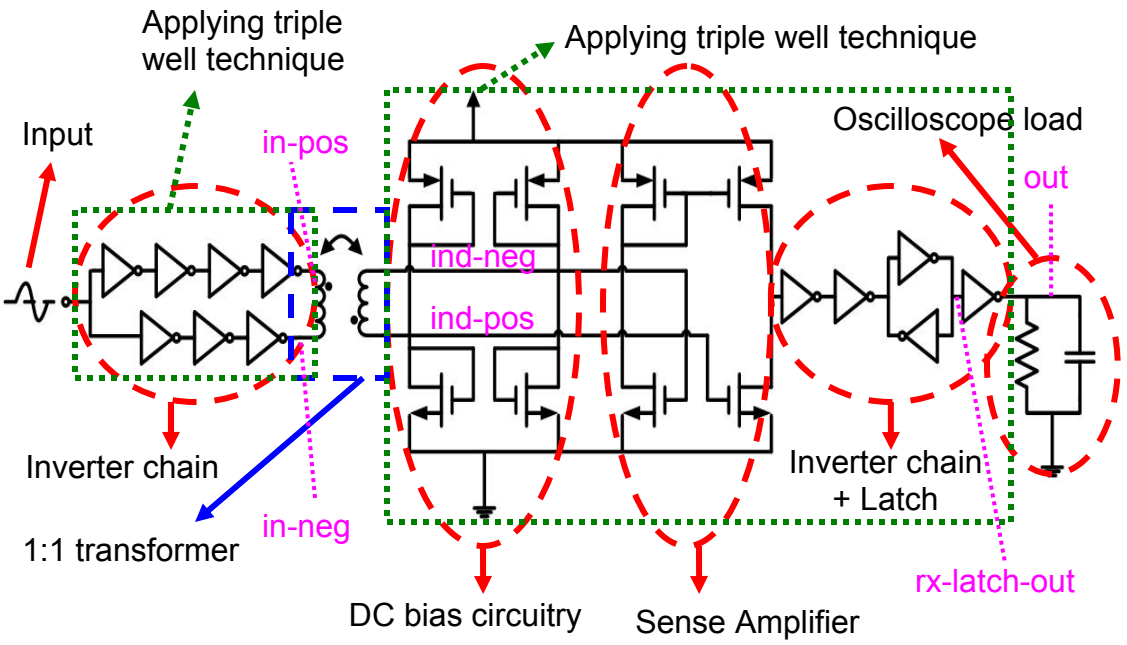


Figure 2-5. Circuit schematic.

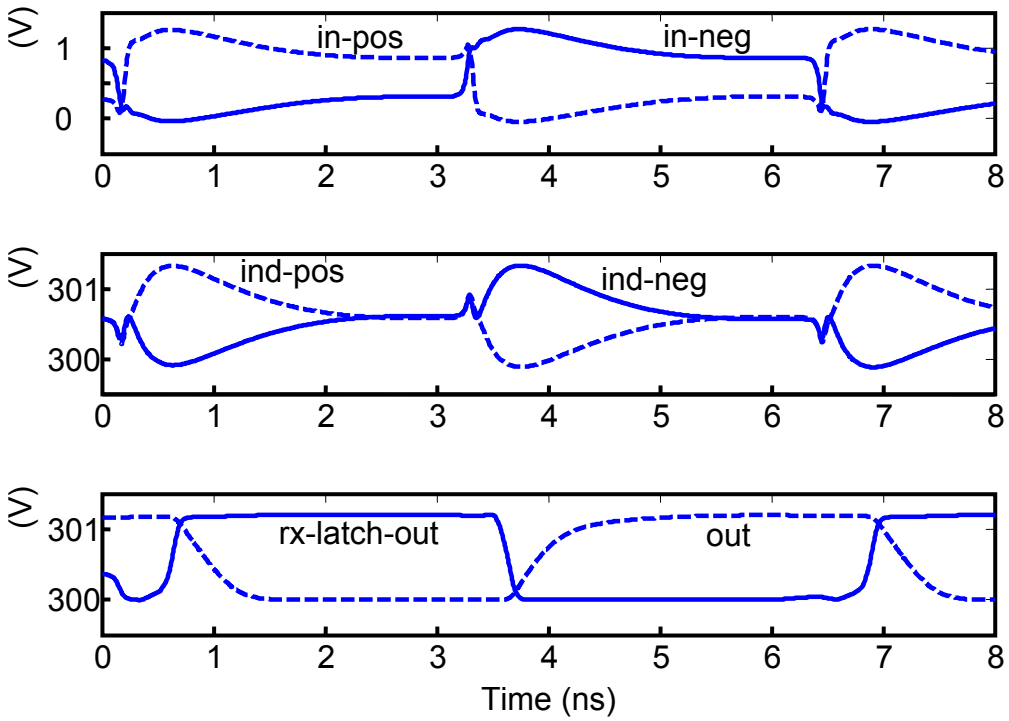


Figure 2-6. Simulated waveforms of 160 MHz at different nodes of the circuit. (Node names are shown in Figure 2-5) The floating ground potential equals to 300 V.

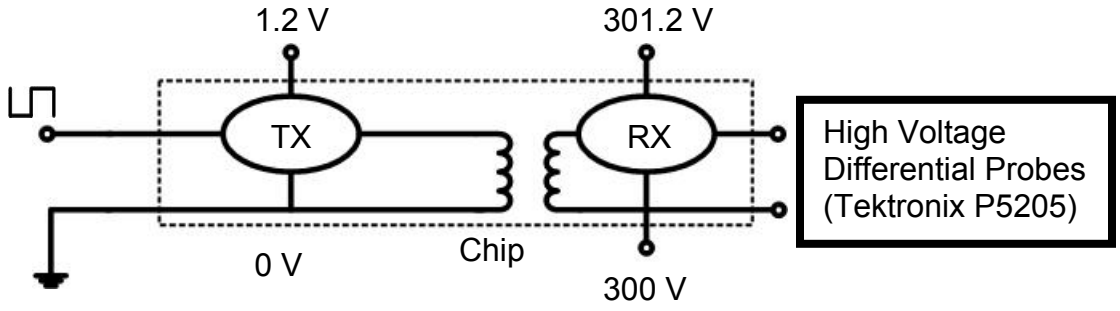


Figure 2-7. Measurement setup.

Due to the floating ground potential, a special differential probe is used to protect the equipment (Tektronix TDS 430A). For example, if the 300-V ground potential is applied at the receiver (RX) side, the high voltage differential probe is placed at the RX output to protect an oscilloscope. The measurement setup is shown in Figure 2-7.

The measurements show the isolator has around 70-V DC isolation, which is lower than the target. The reason for lower breakdown voltage performance is probably due to the small vertical junction depth. Although large separations of 40 μm and 52 μm are maintained horizontally between p-well region and deep n-well region, and n+ well contact and p-well region, the breakdown can still occur at the bottom side of deep n-well (with depth of ~ a few μm), as shown in Figure 2-2. The polysilicon gating was found to be not helpful for increasing breakdown, which is consistent with the breakdown limited by the small vertical junction depth.

The electronic isolator fabricated in UMC 130-nm mixed mode CMOS process is demonstrated to be not suitable for the hybrid engine controller board application. However, 70-V DC isolation is still exciting for bulk CMOS circuits. This chapter only presents circuits operating for 1.2-V voltage difference between supply voltage (V_{DD}) and reference ground potential, which could be 0 V or up to 70 V. If a high voltage MOSFET process is used, data level of higher voltage, like 3 V or 5 V, can be also applied. Incidentally, the 70-V DC isolation

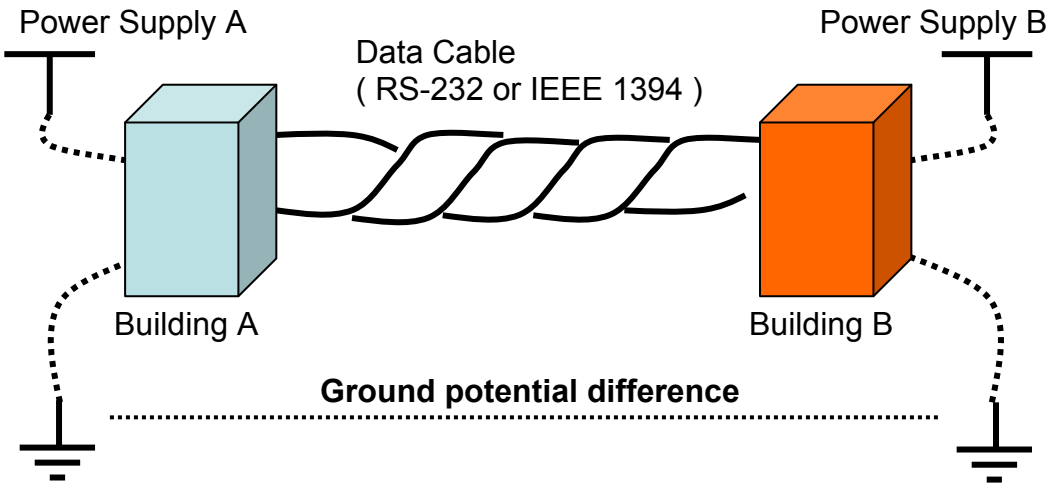


Figure 2-8. Ground potential difference between 2 buildings or 2 vendors, which could be happened for RS-232 or IEEE 1394 communication schemes.

is sufficient for RS-232 and IEEE 1394 applications.

RS-232 and IEEE 1394 are used for communications between 2 systems supplied by different vendors, located in two widely separated buildings, which may possibly have different ground potentials, shown in Figure 2-8 [31]. With the unknown ground potential difference, it is not only likely to damage equipment, but also make communications unreliable. Therefore, the on-chip isolators fabricated in 130-nm CMOS process can be utilized to provide DC isolation up to 70 V.

The die photo is shown in Figure 2-9, which only occupies 0.52 mm^2 (1.15 mm x 451 μm). Figure 2-10 shows the measurement results for circuits operating at 160-MHz frequency with 60-V floating ground potential. A high voltage differential probe modeled as 4-MΩ resistance in parallel with 7-pF capacitance is used at the circuit output to protect instruments from floating ground potential (Figure 2-7). Due to the large load of differential probe, the output waveform is not square. A larger driver should be added to drive the load. For actual use in a system, the load should be smaller and the square output waveform should be preserved. The data rate of 160 MHz is also significantly higher than the usual data rate of photo-couplers

(usually 1 Mbps to 10 Mbps). For the 130-nm CMOS process, data rate higher than 200 MHz should be possible.

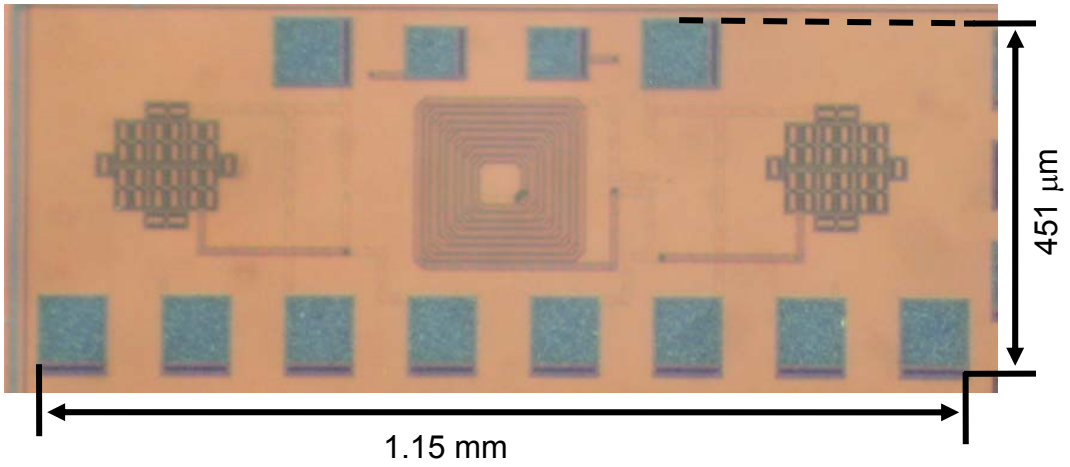


Figure 2-9. Die micrograph of the electronic isolator.

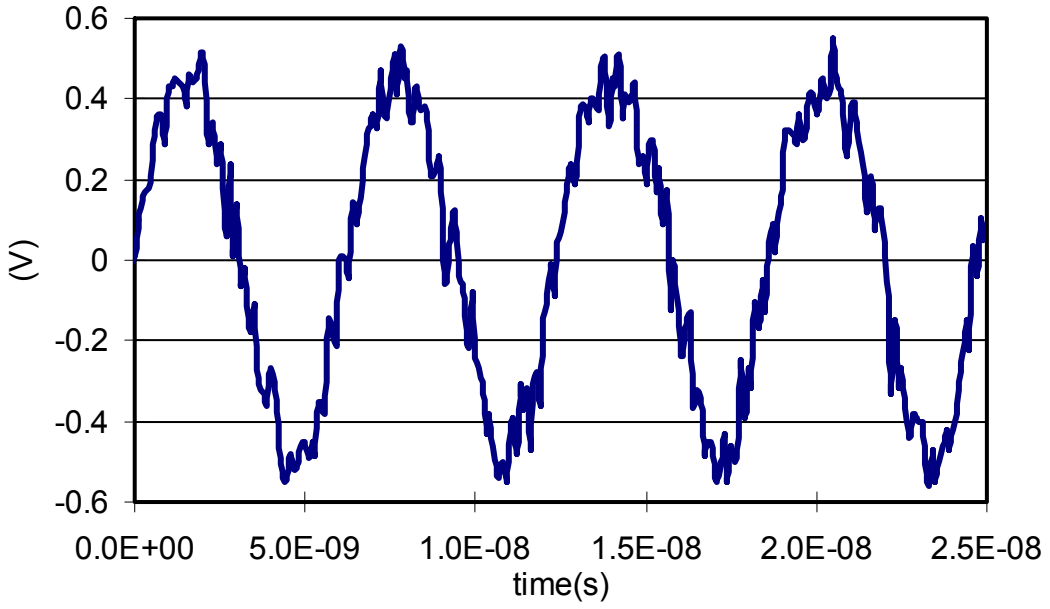


Figure 2-10. Output waveform of 160 MHz, floating ground potential equals to 60 V.

2.5 Summary and Discussions

An electronic isolator fabricated in CMOS process with 70-V DC isolation and around 160-MHz data rate is presented. A transformer using double-layer inductors was designed to

reduce area. A circular triple well design and the large separation between p-well region and deep n-well region were both used to increase breakdown voltage. Polysilicon gating of the surface was found to be not helpful for increasing breakdown voltage. Finally, a bias circuitry, a sense amplifier, an inverter chain, and a latch were built to recover the signal. Although the isolators' breakdown voltage is too low for use in the hybrid engine controller board, such isolation can be used in RS-232 and IEEE 1394 applications.

CHAPTER 3
CHANNEL CHARACTERISTICS

3.1 Introduction

As discussed in Chapter 2, the electronic isolators fabricated in 130-nm CMOS process only achieve 70-V DC isolation, which is not suitable for the hybrid engine controller board. Therefore, the second solution, "wireless interconnects", mentioned in Chapter 1 is investigated. On-chip antennas are a key to realize such a system. On-chip dipole antennas have been integrated in a 20-GHz down-converter [8] and a 24-GHz transmitter [9] as part of an effort to realize a true single chip radio which can enable radical reduction of communication system costs through simplification of design and manufacture. The wireless interconnects formed using single-chip radios will not only be lower cost but will also support much higher data rate potentially greater than 100's of Mbits/sec. Use of wireless interconnects will also eliminate the PCB area of metal traces for making connections to and from the photo-couplers.

In order to determine the feasibility of the wireless communication scheme in the board, the channel characteristics must be understood in advance. Channel characteristics are widely studied [5]-[7], [20], [32]-[36]. Most of them focus on transmission in the free space. However, inside an electronic system, there have not been any reports except the work at 2-12 GHz for a vertically mounted chip antenna on a mother board of a computer [37]. This chapter presents the characteristics of signal transmission at 24 GHz for waves from a horizontally polarized zigzag dipole antenna which is much easier to integrate. The measurements are made with and without a metal cover. The time delay spreads are measured to quantify the multiple path effects. The antenna pair gain can be improved by around 10 dB and the maximum excess delay spread can be reduced by around 15X when a metal cover is placed above the PCB.

3.2 Review of On-Chip Dipole Antennas

The study of antennas fabricated on semi-conducting substrate goes back to late 1980's. In 1986, an on-chip antenna integrated with a 95-GHz IMPATT diode oscillator on a high-resistivity silicon substrate was reported [38]. In 1988, an on-chip antenna integrated with a 43.4-GHz IMPATT diode oscillator on a GaAs substrate was reported [39]. As the circuit operating frequency increases, integration of antennas is becoming more compelling to circumvent the packaging problem. Instead of using high-resistivity or GaAs substrate, it is preferable to use mainstream CMOS technology because of its lower cost and higher integration level. However, lossy silicon substrates cause performance degradation. This and the methods to improve on-chip antenna efficiency have been both investigated in [40]. The on-chip dipole antennas are designed to be 3-mm long and zigzag shape, which is shown to have higher gain [16]. It is fabricated with an aluminum layer on a 20–Ω–cm and 670-μm thick silicon substrate with 3-μm thick oxide layer and 1.5-μm aluminum thickness and 30-μm aluminum width, shown in Figure 3-1. At 24 GHz, the on-chip dipole antenna pair gain versus distance plots are shown in Figure 3-2 [40] and the antenna pattern is shown in Figure 3-3 [40].

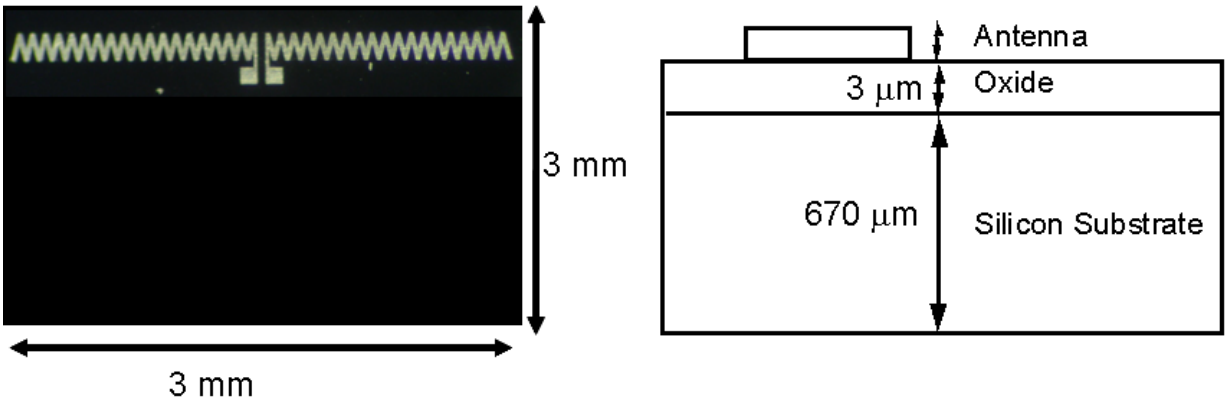


Figure 3-1. On-chip 3-mm long zigzag dipole antennas are fabricated using aluminum on a 20-Ω-cm and 670-μm thick silicon substrate with 3-μm thick oxide layer and 1.5-μm aluminum thickness and 30-μm aluminum width.

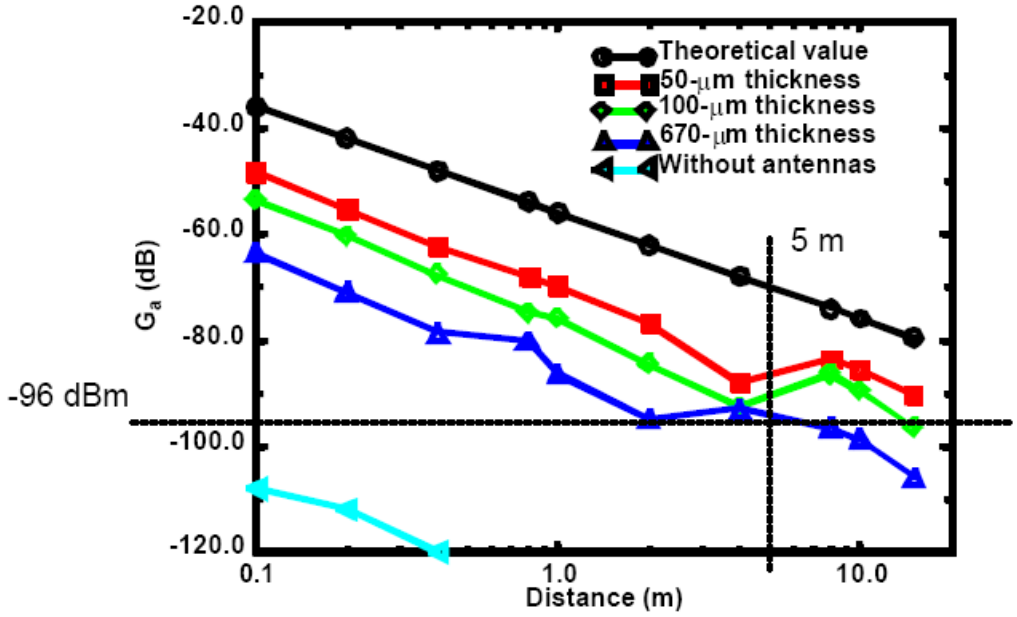


Figure 3-2. Antenna pair gain versus distance in the lobby at 24 GHz. 3-mm on-chip zigzag dipole antennas fabricated on a 20–Ω–cm substrate with a 3-μm oxide layer are used for these measurements at 50-cm height from the ground [40]. The substrate thickness is designed to be 50, 100, and 670 μm.

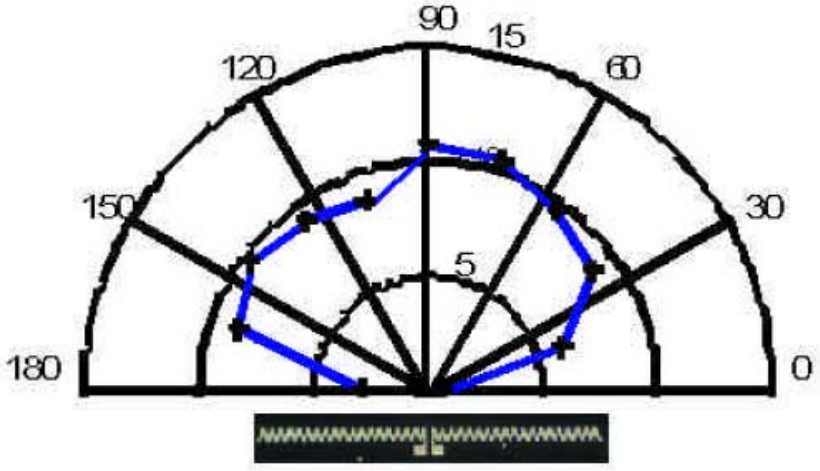


Figure 3-3. 3-mm zigzag antenna radiation pattern at 24 GHz [40].

By thinning the silicon substrate to 100 μm, the antenna pair gain can be improved by 10 dB [40]. The antenna performance would be better by transmitting at the 90-degree direction. For the wireless link in the hybrid engine controller board, the channel characteristics will be

strongly influenced by the components on the PCB. It is expected to be very different from the propagation in the free space. Therefore, PCB environment is described in detail in the next section.

3.3 PCB Environment and Measurement Setup

There are lots of obstacles in the PCB ($25 \times 15 \times 6$ cm^3). It, for example, includes transformers, capacitors, heat sinks, and socket connectors, as shown in Figure 3-4. Some capacitors and transformers are 2.5 cm high. Compared to the thin and small on-chip dipole antennas, those obstacles are relatively large. The transmitted signal will be scattered, attenuated, and multiple reflected while traveling through the obstacles. This is expected to be a challenging environment for wireless communication.

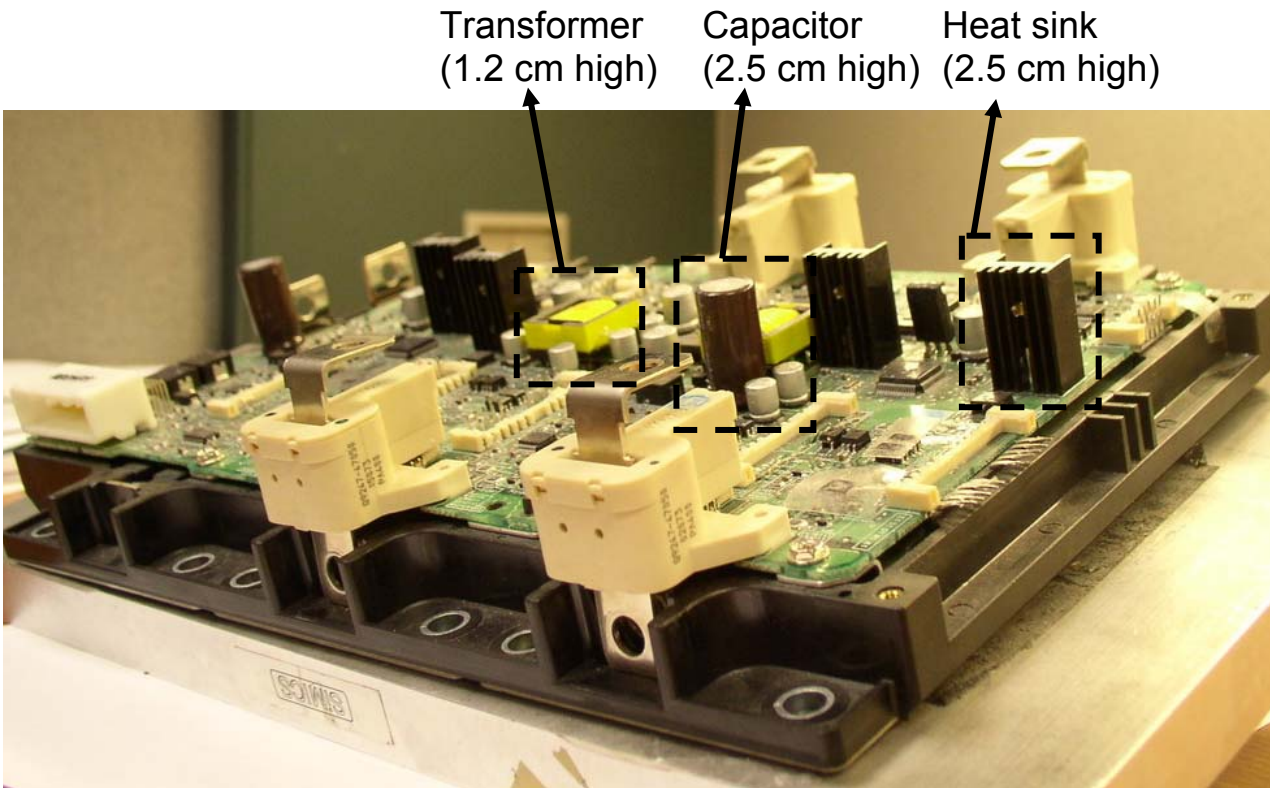


Figure 3-4. Numerous electronic components on a PCB such as transformers, capacitors, and heat sinks, are 1.2 to 2.5 cm high. These make the wireless communication on the PCB challenging.

The measurements were made without taking out any components of PCB. In [37], the antenna was placed vertically using a right angle connector with a heat sink and a CPU fan removed, which alters the channel characteristics. The on-chip dipole antenna measurements reported in this chapter, to emulate the eventual use scenario are made by either directly placing an antenna on the PCB surface or on the top surface of discrete IC components, which is ~ 2 mm above the PCB. From the free space measurement experience [40], on-chip dipole antennas close to ground have significantly degraded performance. However, this is necessary in this application. Large scale fading channel characteristics and time delay spread measurement are both used to characterize the channel characteristics.

The antenna pair gain measurement setup is shown in Figure 3-5. Antenna pair gain, G_a [5], is defined as

$$G_a = \frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2, \tag{3-1}$$

where λ is the wavelength in free space, R is the distance between the antenna pair, and G_t and G_r are the transmitting and receiving antenna gains. It includes probe chucks, cable connections, a signal generator, off-chip baluns, SS probes, and a vector network analyzer (VNA) [34].

The measured channel frequency response is converted into time domain (time delay spread) waveforms using inverse discrete Fourier transformation (IDFT) [41]. By using these time delay spread measurements, multi-path effects are quantified. The multi-path effects are expected to be particularly severe in the PCB. The measurement points on the PCB are shown in Figure 3-6. The points are chosen based on the feasibility for landing the high frequency probes. The separations between a pair of sampling points range from 6.5 to 25 cm. The time delay spread measurements are made at ~ 10-cm and ~ 15-cm separations with and without a metal

cover located ~ 3.5 cm on top of the PCB. The large scale fading channel characteristics are measured using the setup including a signal generator and a spectrum analyzer [34].

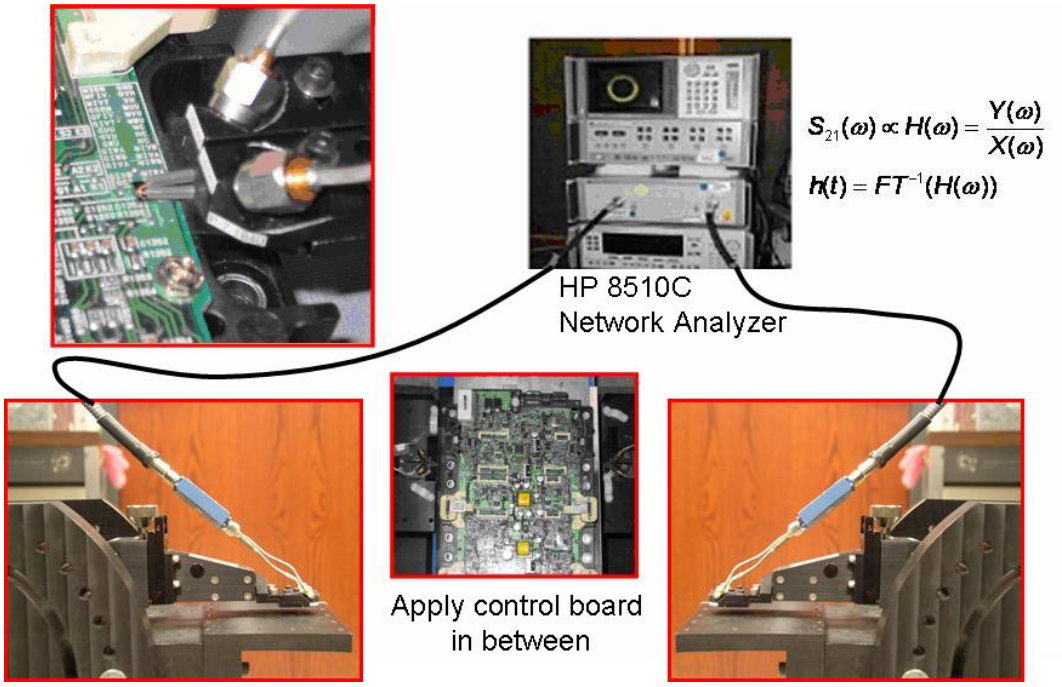


Figure 3-5. Measurement setup with a vector network analyzer (VNA) for measuring the impulse response of communication channels.

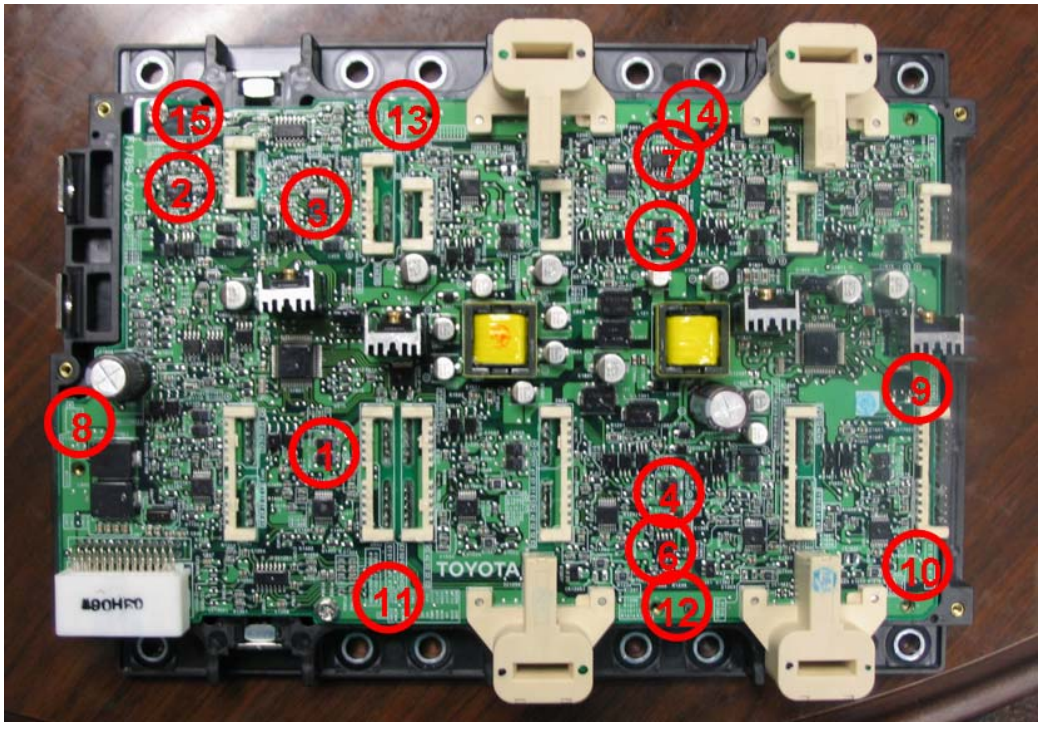


Figure 3-6. Measurement points chosen on the PCB.

3.4 Measurement Results and Discussions

Figure 3-7 shows G_a versus separation plot which represents the large scale fading channel characteristics measured using a setup with a signal generator and a spectrum analyzer. Without a metal cover, G_a can be as much as 20 dB below that for free space propagation. On the average, adding a metal cover leads to around 10-dB G_a improvement. If a transmitter is placed at the center of PCB, then the maximum required transmission range is around 15 cm to any point on this PCB. Table 1-1, shown in Chapter 1, summarizes the link margin analyses.

The 24-GHz receiver sensitivity is around -74.3 dBm for 50 Mbits/sec Amplitude Shift Keying (ASK) modulated data at bit error rate (BER) of 10^{-13}. The system will use spread spectrum with a chip rate of 400 Mchip/sec. Noise figure of 8 dB is reasonable based on [8]. The

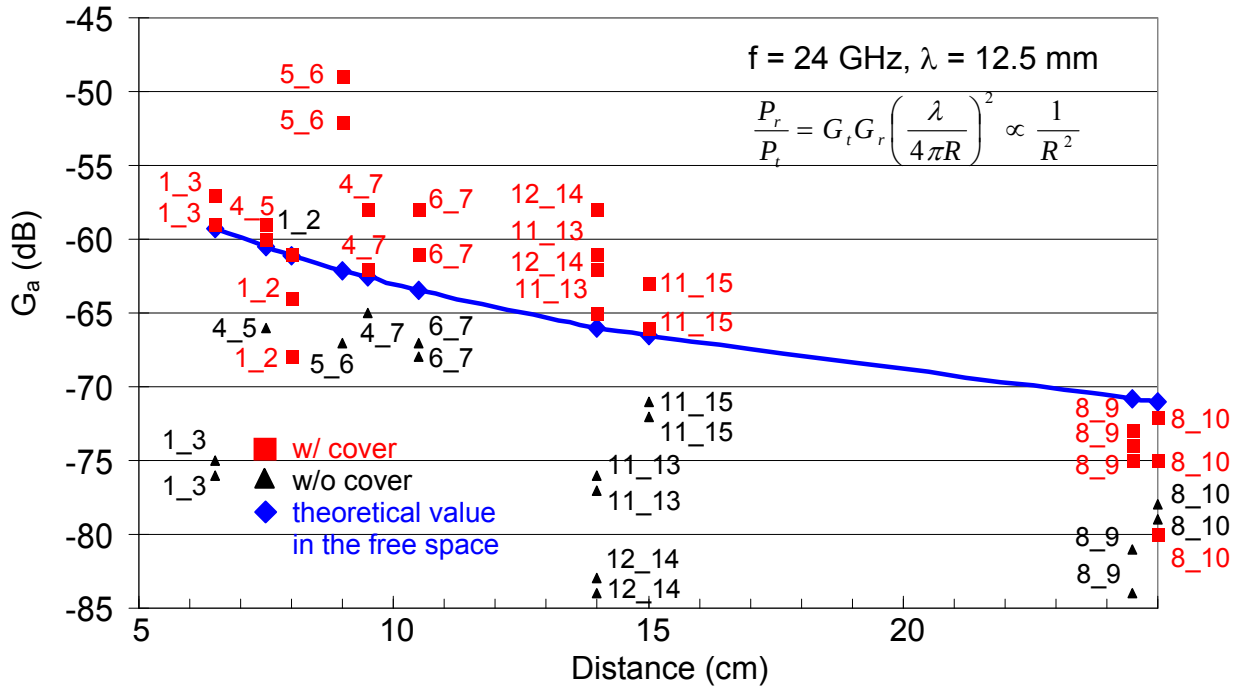


Figure 3-7. Large scale fading channel measurement results. (11-15 means TX is placed at sampling point 11 and RX is placed at sampling point 15.) Theoretical value is calculated based on Friis formula and using the measured on-chip dipole antenna gains of -12 dB.

lowest power level for the case with a metal cover is around -68 dBm, which is greater than the sensitivity. There is around 6-dB margin in the real operating environment. The antenna performance can be improved by thinning the silicon substrate, which should increase the link margin.

A concern for the G_a measurements is that the phase information is not included. In particular, signals from multi-paths could add to result in larger power. Especially, in the presence of a metal cover, the number of multi-paths contributing to the received power could be increased. If the time delays among the signals traveling on different paths exceed the tolerance for the clock data recovery (CDR) circuit in the receiver, CDR will not be able to recover the signal. To better quantify this, the time delay spreads have been measured and shown in Figure 3-8 for the cases with and without a metal cover at 10-cm and 15-cm separations. The channel response was measured between 15 and 26.5 GHz, and converted into the time domain waveform using IDFT.

Figure 3-8(a) shows the time domain measurement results with probes landing on a "thru" calibration structure. There is a single well defined peak with almost no time delay. The time domain channel characteristic measured in the PCB without a metal cover at 15-cm separation (point 1 to 10 in Figure 3-6) is shown in Figure 3-8(b). There are two dominant peaks at 0.63 and 1.05 ns. The second peak is slightly higher in magnitude. There are three additional peaks with magnitude that is approximately 50% of the dominant peak. In addition to these, there are numerous peaks with magnitude that is around 20% of the dominant peak up to 30 ns. The PCB is clearly a multiple path rich environment. In free space, 24-GHz signals transmission time should be around 0.5 ns for 15-cm separation. The mean excess delay, defined in Eq. (3-2) [41], is 1.86 ns, and rms delay spread, defined in Eq. (3-3) [41], is 2.75 ns.

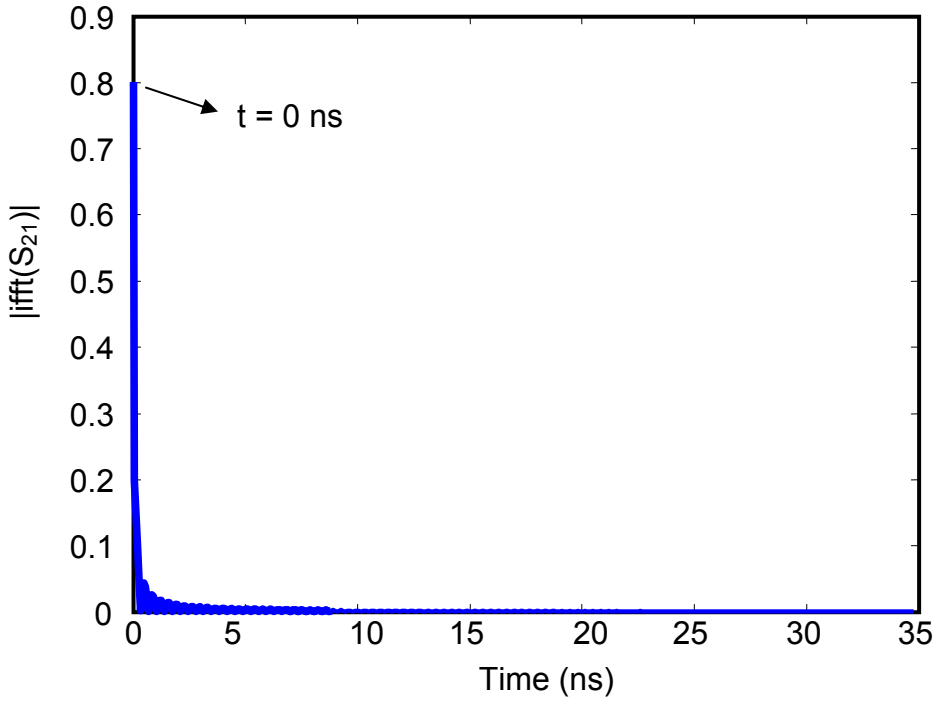


Figure 3-8(a). Time delay spread measurement results – probes landing on a "thru" calibration structure (almost negligible time delay).

$$\bar{\tau} = \frac{\sum_k a_k^2 \tau_k}{\sum_k a_k^2} = \frac{\sum_k P(\tau_k)\tau_k}{\sum_k P(\tau_k)} \tag{3-2}$$

$$\sigma_\tau = \sqrt{\bar{\tau^2} - \left(\bar{\tau}\right)^2} \tag{3-3}$$

$$\bar{\tau^2} = \frac{\sum_k a_k^2 \tau_k^2}{\sum_k a_k^2} = \frac{\sum_k P(\tau_k)\tau_k^2}{\sum_k P(\tau_k)}$$

where a_k is the relative amplitude of the detectable signal and $P(\tau_k)$ is the power level of the power delay profile at time τ_k. It will be challenging to implement a robust simple wireless communication system with 400-Mchips/sec chip rate for the channel with such characteristics. The chip period is 2.5 ns. Managing the rms excess delay of 2.75 ns will complicate the receiver design.

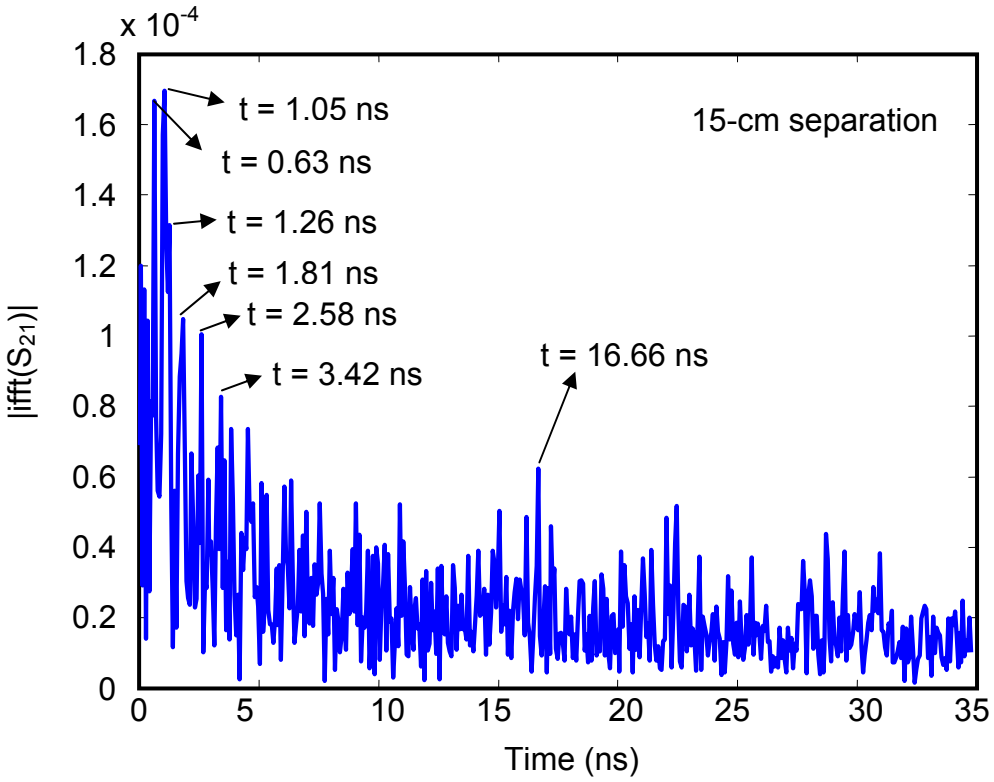


Figure 3-8(b). Time delay spread measurement results – PCB without a metal cover at 15-cm separation

Figure 3-8(c) shows the measurements for the case with a metal cover at 15-cm separation. Explicitly, there is one dominant peak at 0.63 ns and its amplitude is around 3-4 times higher than the case without a cover. Like the case without the cover, there are three additional peaks with magnitude that is approximately 50% of the dominant peak. Beyond 5 ns, there are no significant peaks. This channel is much simpler. The mean excess delay and rms delay spread are 0.35 and 0.41 ns, which are actually 81.2% and 85.1% smaller than the case without a cover. This is probably due to the fact that the signals reflected by the metal cover have an un-obstructed path and is significantly stronger than the signals propagating near the surface of the PCB with numerous electronic components. At 15-cm separation with a metal cover, the maximum excess delay from measurement is around 1.1 ns (4^{th} peak in Figure 3-8(c)). The 1.1-ns maximum excess delay is acceptable for proper CDR operation of the system with 400-

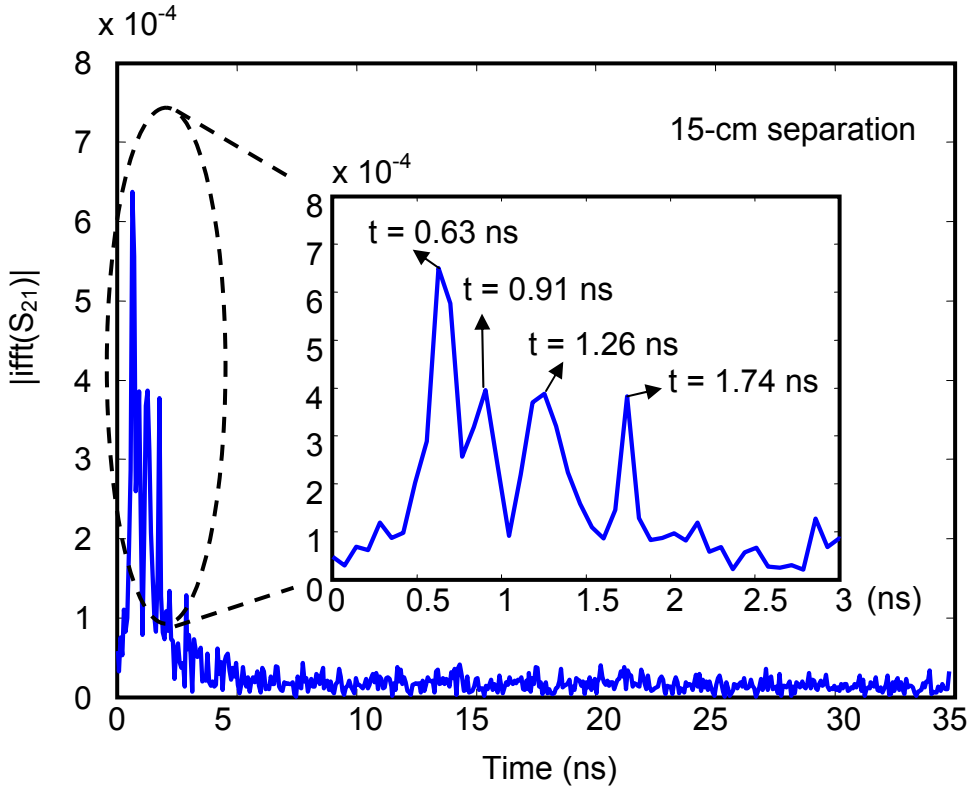


Figure 3-8(c). Time delay spread measurement results – PCB with a metal cover at 15-cm separation

Mchips/sec chip rate.

Figure 3-8(d) shows the measurement results for the case with a metal cover at 10-cm separation (point 4 to 7 in Figure 3-6). Once again, a single dominant peak is observed. The amplitude is approximately 4 times larger than that at 15-cm separation. The time delay of the maximum peak is 0.49 ns. The mean excess delay and rms delay spread are 0.11 and 0.18 ns. These measurements indicate that by properly selecting the transmitter and receiver positions in a PCB, reflections from a metal cover can be utilized to improve received power level and to reduce the delay spread thus relaxing the link margin.

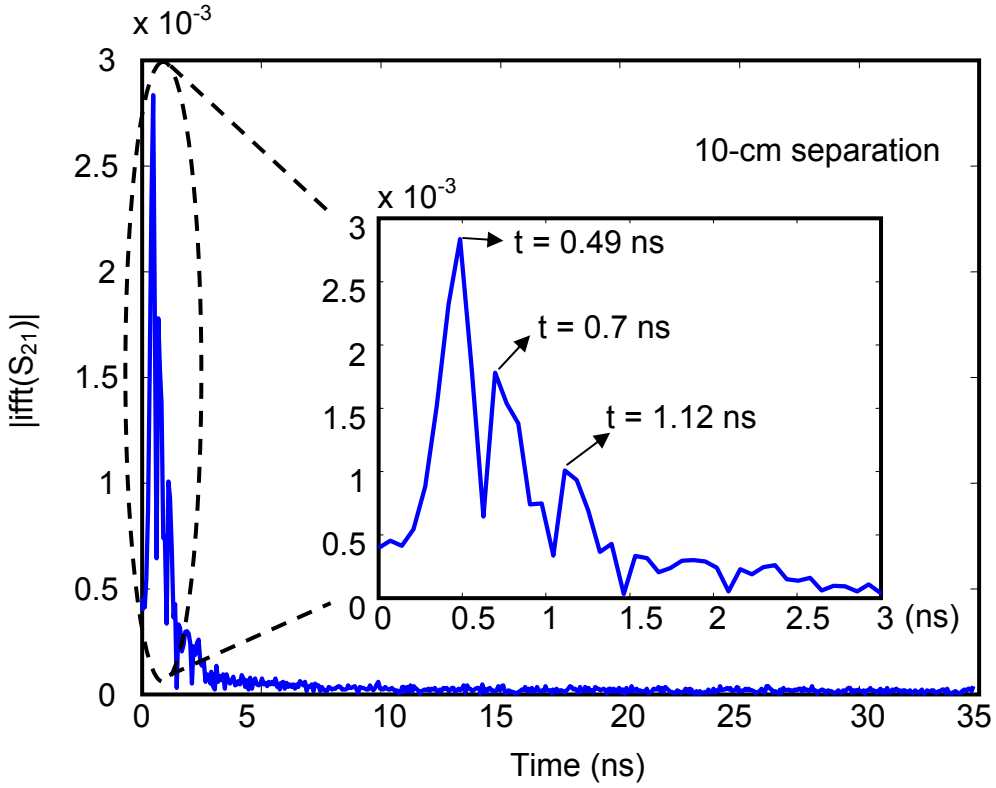


Figure 3-8(d). Time delay spread measurement results – PCB with a metal cover at 10-cm separation

3.5 Summary

Large scale fading channel characteristics and time delay spread in a printed circuit board for a hybrid engine motor controller have been measured at 24 GHz using 3-mm zigzag dipole antennas fabricated on 20-Ω-cm silicon substrates. With a metal cover located around 3.5 cm above the PCB, the antenna pair gain, G_a can be improved by ~ 10 dB. Furthermore the excess delay and rms delay can also be reduced. The maximum excess delay is around 1.1 ns at 15-cm separation, which is acceptable for recovery of clock and data for a 400-Mchip/sec system. By thinning the silicon substrate, the on-chip dipole antenna performance could be improved and further improve the link margin. It has been verified that on-chip dipole antennas can be used for wireless communication in the hybrid engine controller board.

CHAPTER 4
CDMA TX CHAIN DESIGN

4.1 Introduction

The hybrid engine controller board shown in Figure 4-1, has 2 dead-time controllers (D1 and D2) and 12 motor control nodes (M1, M2, …, M12). Each dead-time controller communicates with 6 motor control nodes. For example, D1 needs to communicate with M1, M2, …, and M6. In order to handle the multi-path rich environment, shown in Chapter 3, CDMA (code division multiple access) has been chosen for downlink (dead-time controller to motors) to simplify the transmitter design [42]. The uplink (motors to dead-time controller) uses FDMA (frequency division multiple access) to avoid the synchronization problem of CDMA [42] as shown in Figure 4-2. There is an additional channel assigned for temperature information from the motor.

Usually, CDMA has to deal with the near-far problem [43], [44]. The near-far problem is due to the varying received signal strengths resulting from distance variation between a receiver and several transmitters. The larger signal from a transmitter located nearer becomes a strong interferer to the signal from radios farther away. In addition, the signals from the transmitters also need to be synchronized in the presence of near-far problem. Mitigating these requires power control circuitry and significant digital base band processing. Using FDMA for uplink eliminates these problems.

Since there are a CDMA transmitter and a FDMA receiver (RX) on the same chip at the dead-time controller side, the frequency plan is especially important. The downlink (CDMA path) frequency band is between 15.6 GHz and 18 GHz, and the uplink (FDMA path) frequency band is between 24.2 GHz and 27 GHz (Figure 4-2). The 6-GHz frequency offset between the TX and RX is intentionally chosen to improve isolation. Table 4-1 shows the frequency allocation for

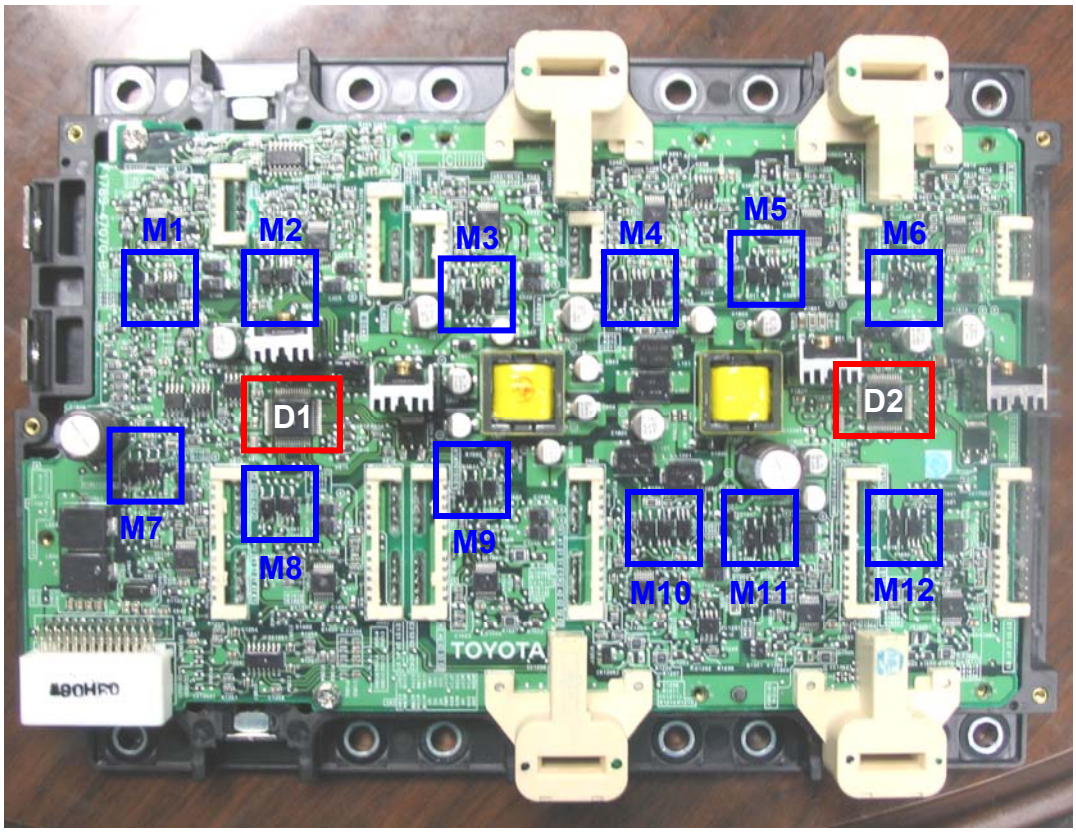


Figure 4-1. Board showing dead-time and motors (D1, D2: dead-time controller, M1-M12: motor).

the downlink and uplink. Using frequency bands above 15 GHz allows integration of a compact on-chip antenna with the circuit blocks. This enables a higher integration level, mitigates the packaging problems, and lowers the manufacturing cost. The spread spectrum technique is applied in the TX chain. Walsh codes are used to generate 8 orthogonal 8-bit codes for supporting up to 8 channels. For the present application, only 6 channels are needed, as shown in Table 4-1.

Figure 4-3 shows the block diagram for TX and RX chains for a dead-time controller. The TX chain includes a PLL, divider chains, a mixer, a power amplifier (PA), attenuators, a digital coder, a duplexer, and an on-chip dipole antenna. The PLL generates a 24-GHz carrier.

The signal is frequency divided down to 12 GHz and 4.8 GHz to generate the IF and LO inputs of the mixer. Following the mixer, the signal is up-converted to 16.8 GHz and passed through pre-drivers and a differential PA stage. The unwanted signals below or above the desired frequency band (15.6-18 GHz) would be filtered by the duplexer. Finally, the signal are transmitted out using a 4-mm on-chip dipole antenna. Based on the link margin analysis (Table 1-1), the power delivered to the antenna needs to be ~ 10 dBm, which can provide ~ 21-dB link margin. A digital coder is the control block, which provides the modulation control signal for the TX chain. It includes flip-flops, XNOR's, an adder, and an address decoder, shown in Figure 4-4 [45]. After the adder and address decoder, control signals are used for CDMA modulation. These are used to control the pre-driver stage to modulate the 16.8-GHz carrier. Details will be described in section 4.2.1.

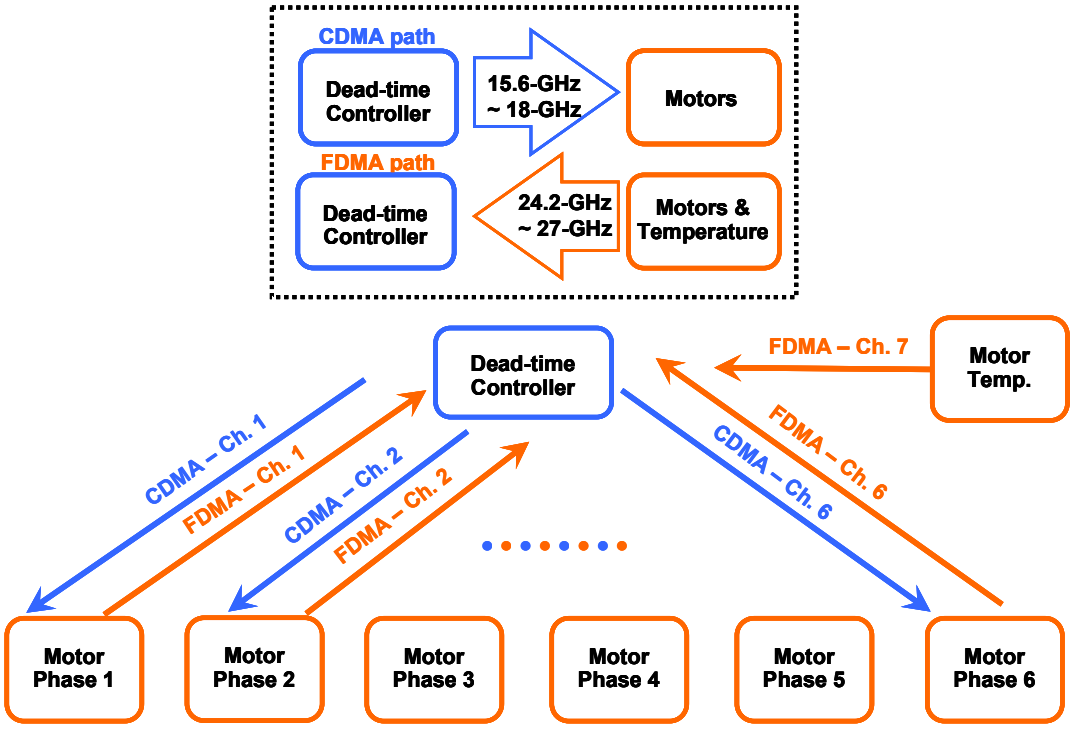


Figure 4-2. Downlink and uplink modulation schemes, and frequency allocation.

Table 4-1. Frequency plan for each motor and dead-time controller (frequency band unit: GHz)

TX Channel	Freq. Band	RX Channel	Freq. Band	Chip
Motor				
1	24.2-24.6	1	15.6-18, C1	1
2	24.6-25.0	2	15.6-18, C2	2
3	25.0-25.4	3	15.6-18, C3	3
4	25.4-25.8	4	15.6-18, C4	4
5	25.8-26.2	5	15.6-18, C5	5
6	26.2-26.6	6	15.6-18, C6	6
7	26.6-27.0			7
Dead-time controller				
1	15.6-18, C1	1	24.2-24.6	1
2	15.6-18, C2	2	24.6-25.0	1
3	15.6-18, C3	3	25.0-25.4	1
4	15.6-18, C4	4	25.4-25.8	1
5	15.6-18, C5	5	25.8-26.2	1
6	15.6-18, C6	6	26.2-26.6	1
		7	26.6-27.0	1

4.2 Sub-Blocks of Transmitter Chain

4.2.1 Power Amplifier

A power amplifier (PA) is a key block for the TX chain. Usually, a CMOS PA suffering from the lower breakdown voltage due to a thin gate oxide layer of mainstream CMOS technologies has lower output power compared to the PA's in III-V and bipolar technologies [46]-[50]. Achieving 10-dBm output power and good efficiency is challenging.

There are different types of power amplifiers, such as class A, B, C, D, E, and F. Figure 4-5 shows a typical schematic of class A power amplifier, which operates linearly across the entire input and output range. An RFC (RF choke) is used to provide the connection to the voltage supply. The matching network transforms the load impedance, 50 Ω, to lower impedance, R_T, at the drain node. The maximum voltage of drain node is $2V_{DD}$. The power delivered to the matching network (P_{del}) is

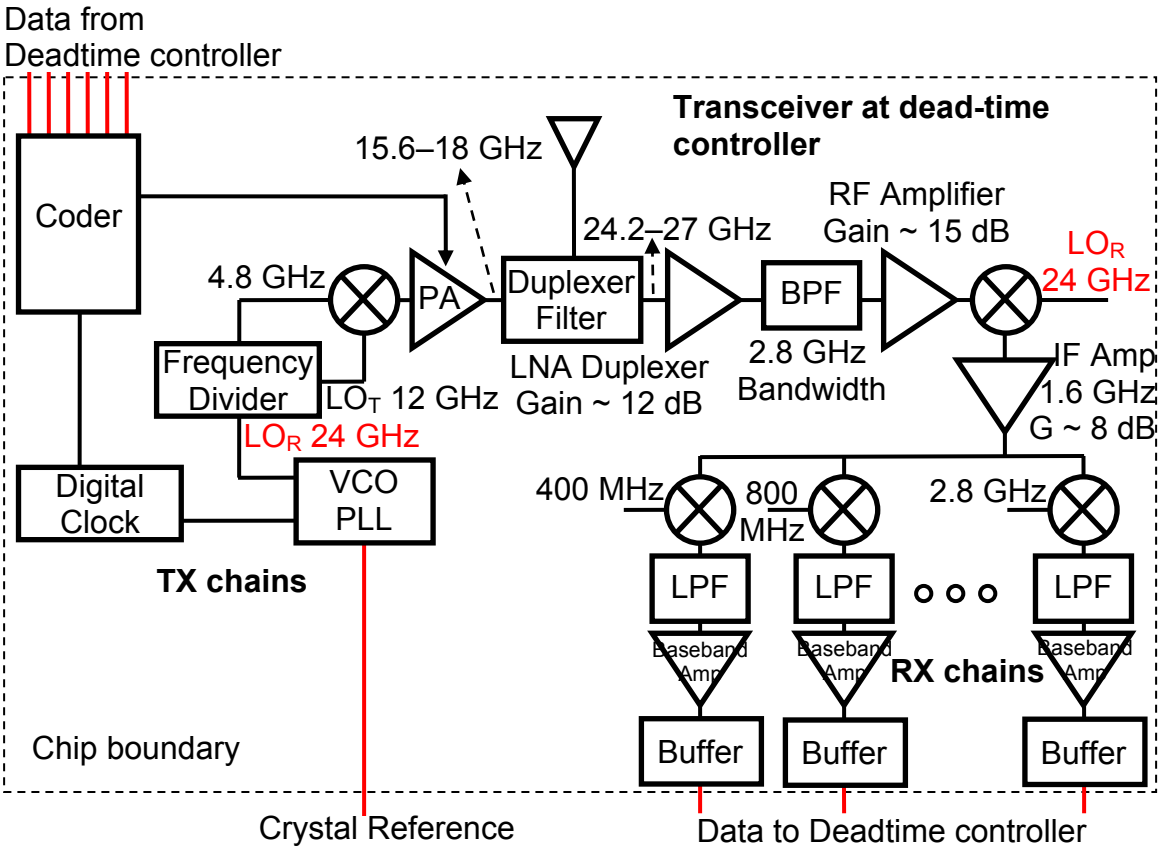


Figure 4-3. Block diagram for the transceiver in a dead-time controller.

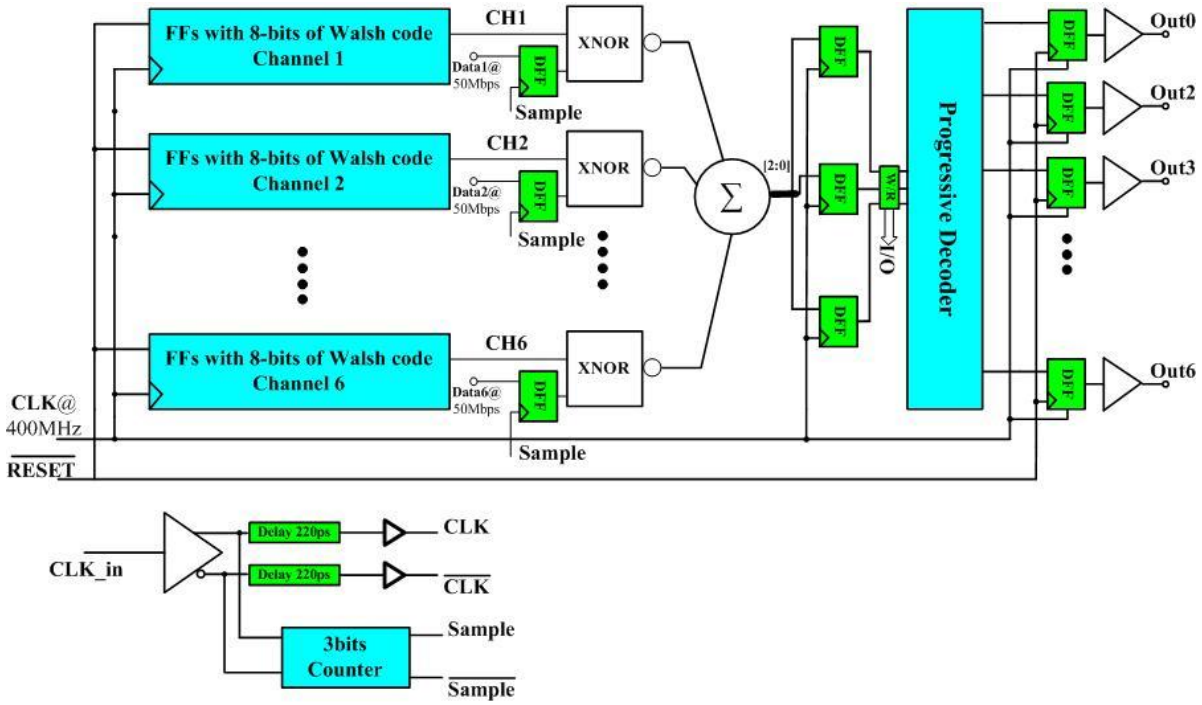


Figure 4-4. Block diagram for the digital coder of TX chain [45].

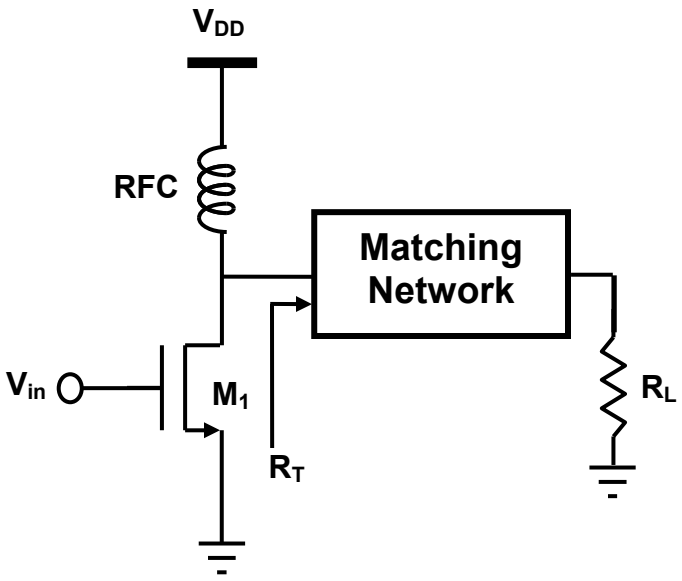


Figure 4-5. Schematic of the common source power amplifier.

$$P_{del} = \frac{\left(\frac{V_{DD}}{\sqrt{2}}\right)^2}{R_T} = \frac{{V_{DD}}^2}{2R_T} \tag{4-1}$$

A current of (V_{DD}/R_T) can be provided by the RFC. Therefore, the power consumption (P_{DC}) is $(V_{DD}/R_T)V_{DD}={V_{DD}}^2/R_T$. Consequently, the maximum drain efficiency is

$$\eta \equiv \frac{P_{del}}{P_{DC}} = \frac{\frac{{V_{DD}}^2}{2R_T}}{\frac{{V_{DD}}^2}{R_T}} = \frac{1}{2} \tag{4-2}$$

For class A PA, the maximum drain efficiency is just 50%. The low efficiency is due to the conduction angle for M_1, θ, of class A PA is 360˚, shown in Figure 4-6(a). If the conduction angle can be reduced, less power is dissipated. For example, the conduction angle of class B PA is only 180˚, which means the drain current is sinusoidal for one half cycle and zero for the other half cycle, as shown in Figure 4-6(b). It can lower the power consumption and improve PA efficiency. Assume the current (Figure 4-6(b)) is

$$i(\theta) = I_{\max}\cos(\theta), \quad -\frac{\pi}{2} \le \theta \le \frac{\pi}{2} \tag{4-3}$$

$$i(\theta) = 0, \quad \frac{\pi}{2} \le \theta \le \pi, \; -\frac{\pi}{2} \ge \theta \ge -\pi$$

The total current is

$$i(\theta) = a_0 + a_1\cos(\theta) + a_2\cos(2\theta) + \ldots \tag{4-4}$$

$$a_0 = \frac{1}{2\pi}\int_{-\frac{\pi}{2}}^{\pi/2} I_{\max}\cos\theta d\theta = \frac{I_{\max}}{\pi} = I_{dc}$$

$$a_1 = \frac{1}{\pi}\int_{-\frac{\pi}{2}}^{\pi/2} I_{\max}\cos^2\theta d\theta = \frac{I_{\max}}{2} = I_1$$

$$I_{\max} = I_{dc} + I_1 + I_2 + \ldots$$

The average drain current drawn from V_{DD} is given by

$$\overline{I_{DD}} = a_0 = \frac{I_{\max}}{\pi} = \frac{2V_{DD}}{\pi R_T} \tag{4-5}$$

The power consumption is $(2V_{DD}^2/\pi R_T)$.

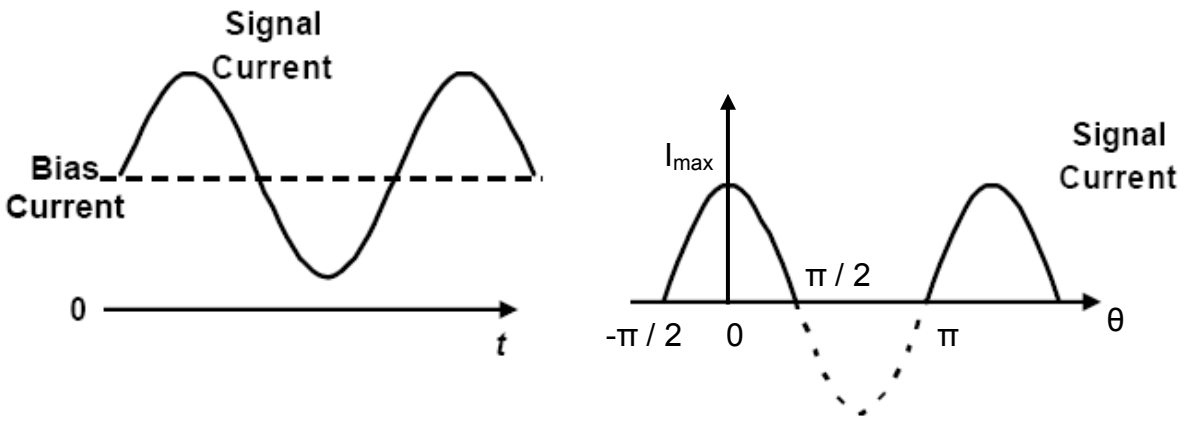
Therefore, the P_{del} is

$$P_{del} = \left(\frac{I_1}{\sqrt{2}}\right)^2 R_T = \frac{V_{DD}^{\;2}}{2R_T} \tag{4-6}$$

Thus, maximum efficiency is

$$\eta \equiv \frac{P_{del}}{P_{DC}} = \frac{\frac{2V_{DD}^{\;2}}{\pi R_T}}{\frac{V_{DD}^{\;2}}{2R_T}} = \frac{\pi}{4} \tag{4-7}$$

The other type of PA called class AB conducts between 50% and 100% of the cycle. It has the intermediate performance for efficiency and linearity, between class A and class B PA's.



(a) Class A type (θ =360°) (b) Class B type (θ =180°)

Figure 4-6. Transistor drain current and conduction angle, θ, for class A and B power amplifiers. However, class A, B, and AB power amplifiers all use active devices as a controlled current source.

There is another type of PA, in which an active device acts as a switch. Theoretically, switching type PA's should consume no power and achieve 100% efficiency. For instance, class E and class F PA's are switching type. The simple schematic is similar to that shown in Figure 4-5. The difference between class A and class E PA's is that the input signal for class E PA is expected to have a rectangular waveform. To reduce power dissipation, there should be small current when the drain voltage is finite, and small voltage when the current is large. Both conditions minimize the product of voltage and current, which reduces the power consumption.

Figure 4-7 shows a typical schematic of class E PA. It consists of a transistor, a capacitor C_1 shunted to ground, and a series network C_2 and L_1. The value of C_1, C_2, and L_1 are chosen such that V_x satisfies three conditions [51]:

(1) As the switch turns off, V_x remains low long enough for the current to drop to zero.

(2) V_x reaches zero just before the switch turns on.

(3) dV_x/dt is also near zero when the switch turns on.

From [51], the values of C_1, C_2, and L_1 can be chosen as,

$$L_1 = \frac{Q_L R}{\omega} \tag{4-8}$$

$$C_1 = \frac{1}{\omega R\left(\frac{\pi^2}{4}+1\right)\left(\frac{\pi}{2}\right)} \approx \frac{1}{5.447\omega R} \tag{4-9}$$

$$C_2 = C_1\left(\frac{5.447}{Q_L}\right)\left(1+\frac{1.42}{Q_L - 2.08}\right) \tag{4-10}$$

The inductor quality factor Q_L should be as large as possible. On the other hand, RFC used in Figure 4-7 has to be implemented by a regular on-chip inductor. Therefore, Q_L of on-chip inductors is a factor which limits the class E PA efficiency. The transistor of course has on resistance and finite switching time, which also limit the efficiency. Nevertheless, class E PA is still an attractive option for high frequency circuit design due to its high efficiency. It is suitable for communication systems with a constant envelop modulation.

Back to the hybrid engine controller board, the amplitude modulation scheme (ASK) is needed for the CDMA downlink, which means a linear PA should be used. At 20 GHz using

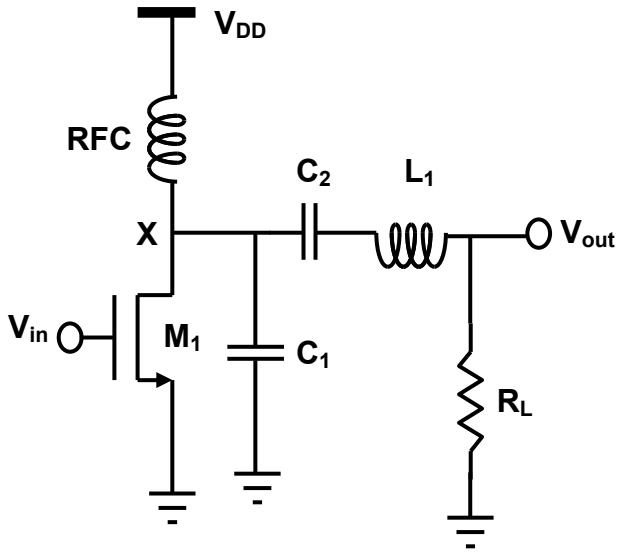


Figure 4-7. Schematic of a class E power amplifier.

single-ended class E PA with 9-dBm output P_{1dB} was reported [52]. It is possible to use the linear portion of a class E PA for this purpose. Due to the integration with an on-chip dipole antenna, a differential PA structure is adopted. Based on the specification mentioned previously, the output P_{1dB} should be around 10 dBm. Higher efficiency and lower power consumption can be possibly achieved compared with using a class A linear PA [53]-[55]. The comparisons of power amplifiers operating near 20 GHz is summarized in Table 4-2. In general, class E PA can achieve higher PAE performance.

Due to the diode detection process used in the RX chain at the motor side, the square-law operation of diode has to be considered [42]. Therefore, the desired multi-level signals at PA output should follow a square-root relation among N levels, where N equals to 2, 3, 4, 5 and 6. At RX side, these result in a constant voltage step between levels after diode detection.

There are several ways to realize multi-level amplitude modulation at the PA stage. One way is to modulate the supply voltage to control output power of PA, shown in Figure 4-8 [56], [57]. It has the disadvantage of sensitive to supply variation and requires a feedback loop for tracking and adjusting the PA envelope. Many approaches to improve efficiency by using non-linear PA's with a linearization circuit or linear PA's with an efficiency-enhancement circuit have been discussed in the literature [58]-[61]. However, use of a dc-dc converter to implement a dynamic voltage supply is needed. The dc-dc converter may be a boost, buck, or buck-boost type.

Table 4-2. Comparisons of power amplifiers operating near 20 GHz.

	Freq.	Technology	Classification	V_{DD}	Gain	P_{out}	PAE
[52]	18 GHz	0.13-μm CMOS	Class E	1.5 V	> 30dB	10.9 dBm	23.5 %
[52]	20 GHz	0.13-μm CMOS	Class E	1.5 V	26 dB	10.2 dBm	20.5 %
[53]	17 GHz	0.13-μm CMOS	Class A	1.5 V	11 dB	5 dBm ($@OP_{1dB}$)	2.4% ($@OP_{1dB}$)
[54]	17 GHz	0.13-μm CMOS	Class B	1.5 V	14.5 dB	17.1 dBm	9.3 %
[55]	24 GHz	0.18-μm CMOS	N/A	2.8 V	7 dB	14.5 dBm	5~6 %

It usually occupies a large area and leads to higher cost. On top of this, a chip rate of 200 Mchips/sec needs to be supported for the wireless interconnects system. This is challenging for the dc-dc converter.

The second way is to use a current-steering technique [62] to modulate the gate bias of pre-drivers, which can change PA output as shown in Figure 4-9. A similar idea was used to lower quiescent current at low output power to improve PA efficiency (adaptive bias control) [60], [61]. However, based on simulations, it has long fall time and precise gain control is also difficult by only adjusting gate bias without closed-loop control. This will make the design more complicated. A simple solution and architecture are required for a PA operating at higher frequencies (above 15 GHz), compared to WCDMA PA operating at a lower frequency band [63], [64].

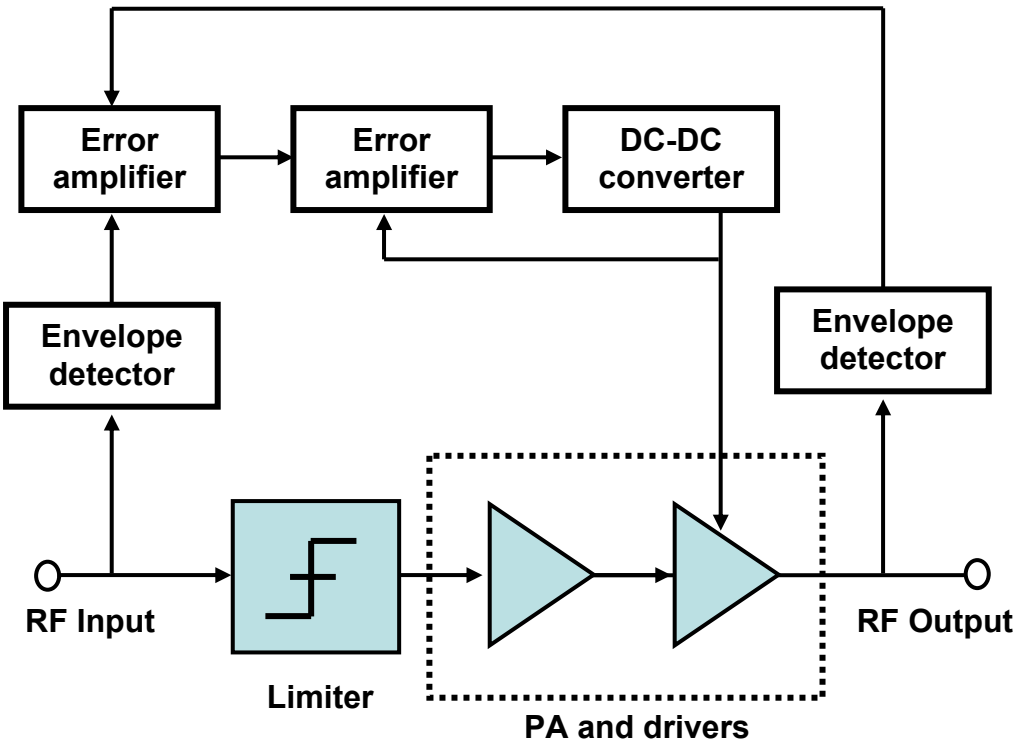


Figure 4-8. Kahn envelope elimination and restoration scheme with using a dc-dc converter.

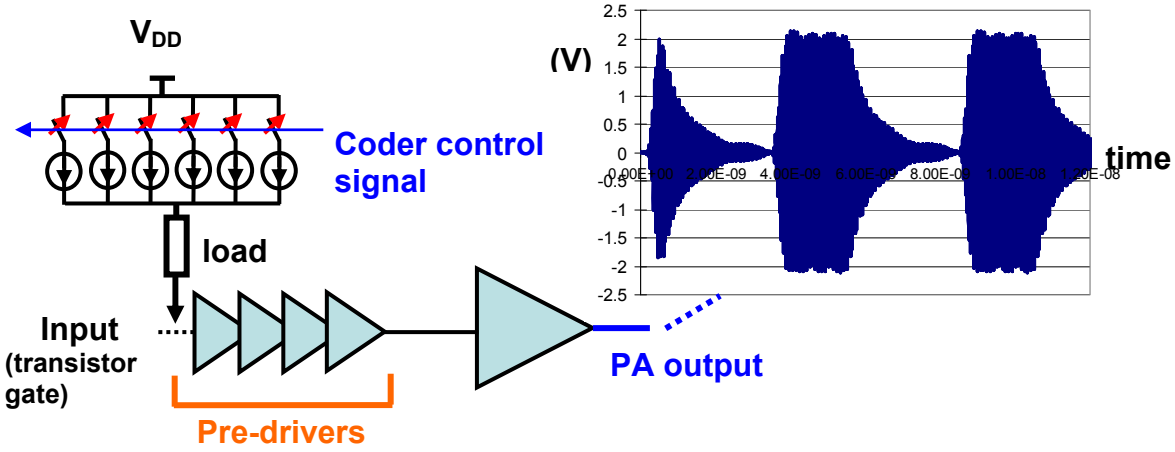


Figure 4-9. Modulate transistor gate bias.

Another method to modulate a PA and achieve multi-level signals at a PA output is to incorporate an attenuator. As shown in Figure 4-10, the attenuator can be placed at the signal path to adjust the signal strength. The single-ended class E PA structure and attenuators are shown in Figure 4-11. It has 4 pre-diver stages and one last PA stage. There are 7 attenuators with different transistor size to control 7 levels at PA output. The gate node of each attenuator is connected to corresponding coder output. There are 6 attenuators connected at the gate of 4th pre-driver stage. And there is one attenuator connected at the gate of second stage. The idea is that coder would increase or decrease the number of switches turned on to set the output power. Since the signal swing at the second stage is smaller than that at the 4th stage, the attenuator size for level 0 could be smaller if it is placed at an earlier pre-amplifier stage. This effectively minimizes the transistor size needed to control level 0 and mitigates the drivability requirement for the digital coder. Table 4-3 shows the truth table for the coding scheme. For level 6, only one attenuator is turned on. On the other hand, for level 0, all attenuators are turned on. The control scheme leads to smaller rise and fall time during transitions, because it turns on or turns off necessary attenuators only. It minimizes the capacitance change during transitions. The coder

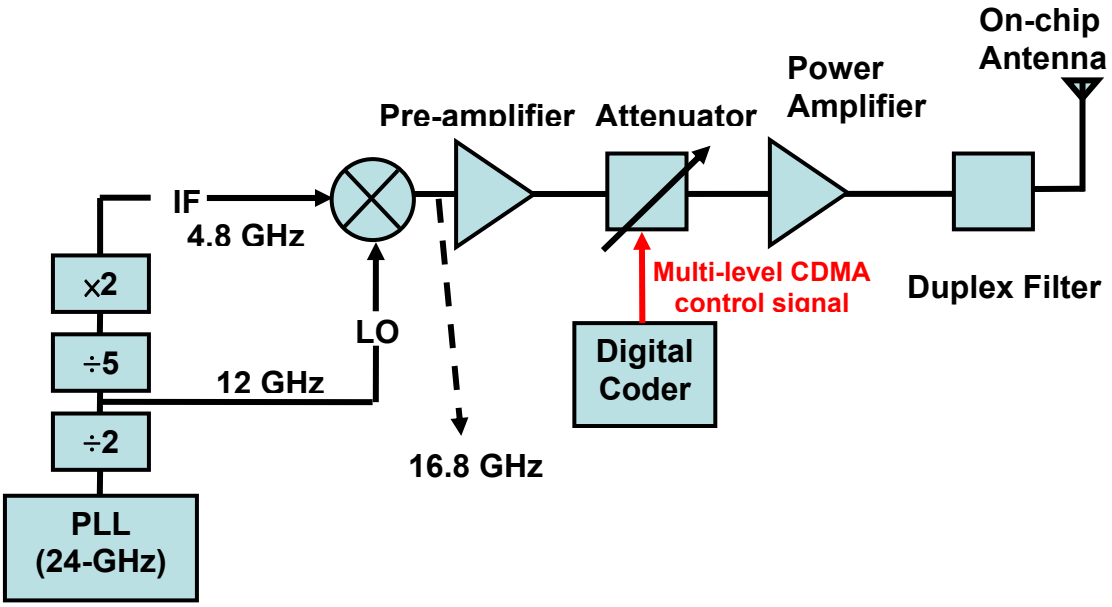


Figure 4-10. PA using attenuators for output power control and CDMA TX chain block diagram.

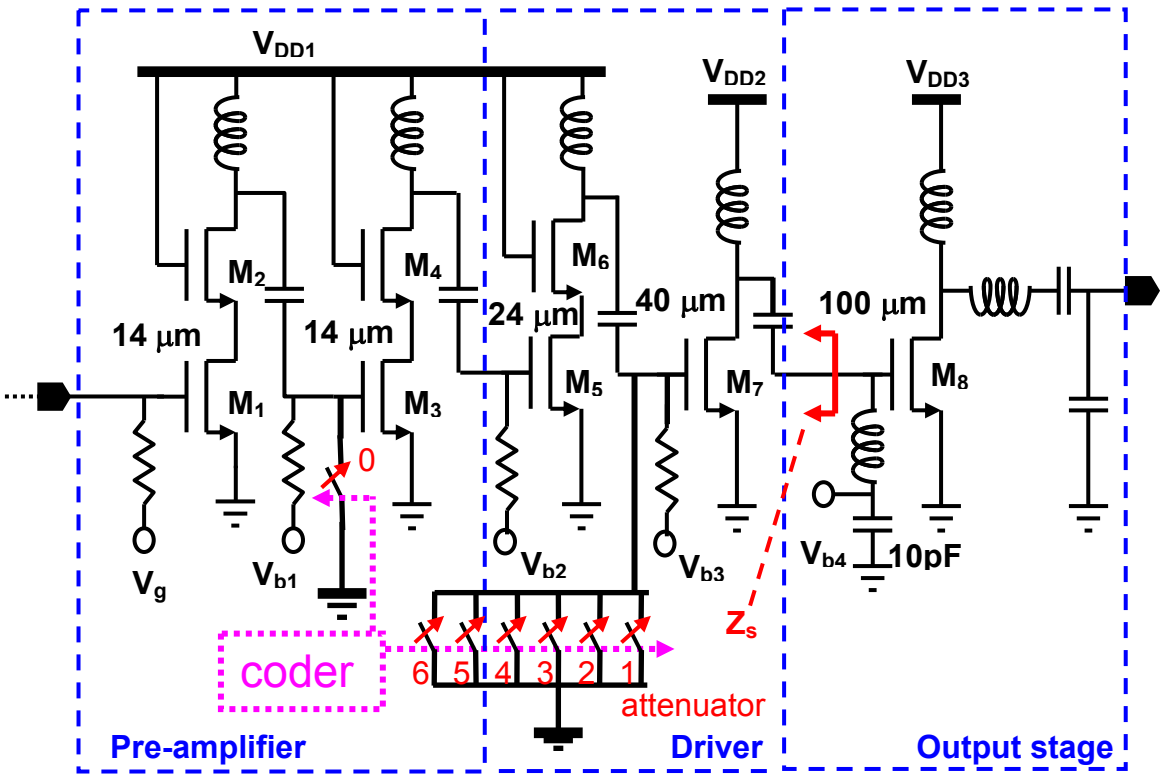


Figure 4-11. Schematic of a single-ended five-stage class-E CMOS power amplifier.

Table 4-3. Truth table of coding and the ratios between levels at TX side and after RX detection.

	att_0	att_1	att_2	att_3	att_4	att_5	att_6
Level 6	0	0	0	0	0	0	1
Level 5	0	0	0	0	0	1	1
Level 4	0	0	0	0	1	1	1
Level 3	0	0	0	1	1	1	1
Level 2	0	0	1	1	1	1	1
Level 1	0	1	1	1	1	1	1
Level 0	1	1	1	1	1	1	1

	Ideal ratio at TX side	After RX detection
Level 2 / Level 1	$\sqrt{2}$	2
Level 3 / Level 1	$\sqrt{3}$	3
Level 4 / Level 1	$\sqrt{4}$	4
Level 5 / Level 1	$\sqrt{5}$	5
Level 6 / Level 1	$\sqrt{6}$	6

requires a 400-MHz clock and input data rate is 50 Mbps. The PA output ought to have a 16.8-GHz carrier with an 400-Mbps envelope. The minimum output duration at an output is 2.5 ns. The target for rise and fall time of the envelope is 10 %, which is 250 ps. In order to provide the ability to adjust the level ratio after fabrication, five small switches with AND gates are added. It will provide extra flexibility for the measurements. D-flip flops added at the output of binary thermometer decoder help the synchronization of output signals.

As shown in Figure 4-11, the bias of class E PA (V_{b4}) is applied through an inductor. The inductor resonates with C_{gd} of last PA stage, which increases PA gain [52]. The pre-driver stages are designed to achieve high voltage gain. Meanwhile, the last PA stage is designed to maximize output power and efficiency. The concern for the inductive biasing technique is the self oscillation of last PA stage. Figure 4-12 shows the small signal model of the last PA stage [52]. The attenuators are placed at the input of 4^{th} common source amplifier. By turning on different combinations of attenuators, the impedance looking back toward the drain of 4^{th} pre-driver stage

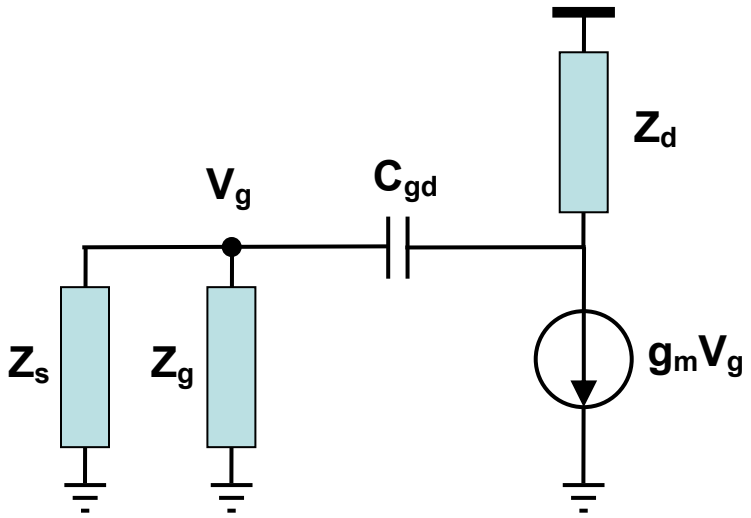


Figure 4-12. Small signal model of the last PA stage (common source amplifier).

(shown in the Figure 4-11) can be changed, which is represented as Z_s. The open loop gain of the PA stage is

$$T(s) = -g_m \left\{ Z_d \,//\left[\left(Z_g \,//\, Z_s \right) + \frac{1}{sC_{gd}} \right] \right\} \bullet \frac{\left(Z_g \,//\, Z_s \right)}{\left(Z_g \,//\, Z_s \right) + \frac{1}{sC_{gd}}} \tag{4-11}$$

The term, (Z_g // Z_s) affects the open loop gain and phase. The oscillation starts when the loop gain is greater than 1 and the phase change must equal to 360 degree [52]. The circuit is near oscillation condition without any RF input (16.8 GHz sinusoidal signal). With the RF input, the self oscillation is suppressed. In the frequency domain, only one single desired frequency peak is observed.

The attenuators placed along the signal path change the signal swing at the input of last PA stage. Especially for level 0, the signal strength is dramatically attenuated by the attenuators. Suppressing the self oscillation is a critical concern for this design to guarantee to have zero amplitude level 0. The key factor for this is properly setting Z_s.

The other design concern is the rise and fall time of output envelope. The rise time for level 0 to level N (N=6, 5, 4, 3, 2, 1) is dominated by the gate bias resistor at the second pre-

driver stage. The gate bias resistor is 5 kΩ, which is large to prevent the loading of 16.8-GHz carrier signal. However, the rise or fall time largely depends on the RC time constant of the equivalent network at the gate of second pre-driver. The attenuator settings change the equivalent RC network, shown in Figure 4-13. When the switch is OFF, the parasitic capacitance is only (C_{gd}+C_{db}). When the switch is ON, the parasitic capacitance is still around (C_{gd}+C_{db}). However, the on resistance of the switch is much smaller compared to the 5-kΩ bias resistor. The equivalent capacitance is relatively constant, which is roughly the sum of C_{db}'s of attenuators and C_{gg} of the pre-driver. It can be represented as C_{eq}. When the transition happened from level 0 to level N, the equivalent resistance changes from few tens ohms to 5 kΩ. Therefore, the RC time constant is

$$\tau = R_{eq} \times C_{eq} \tag{4-12}$$

In the above equation, R_{eq} is the equivalent resistance of the equivalent network. In simulations, the RC time constant is ~ 800 ps.

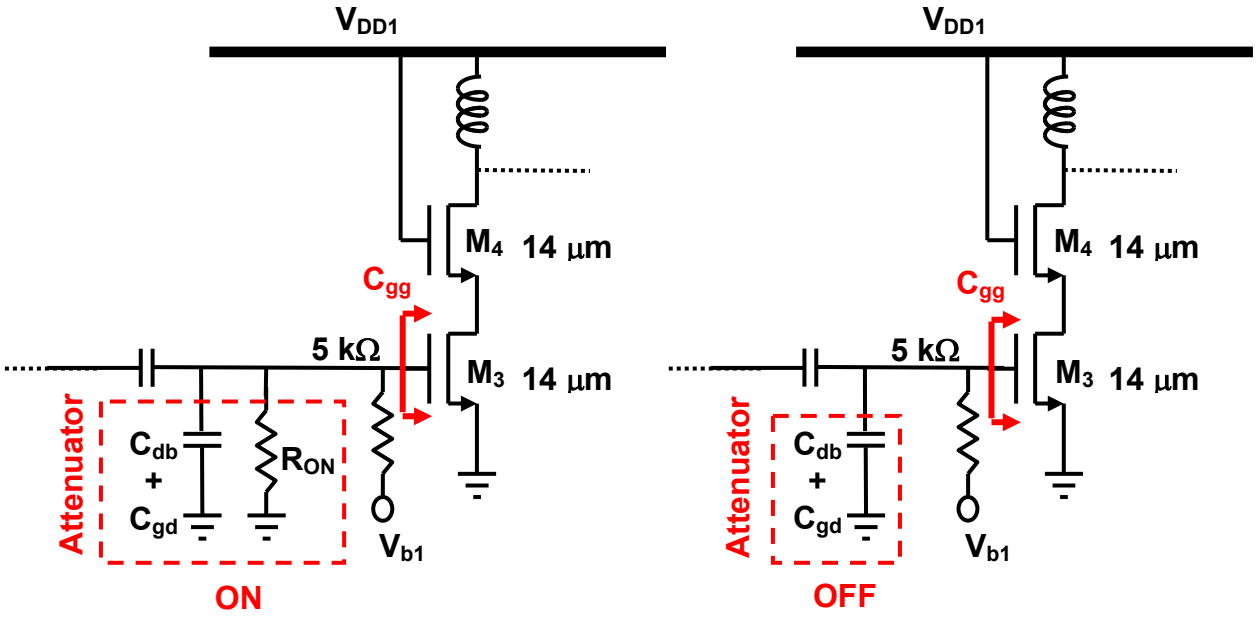


Figure 4-13. Lumped circuit models with the attenuator switched ON and OFF. The rise and fall times depend on the RC time constant of equivalent network at the gate node of second pre-driver.

In section 4.3, simulation results of the multi-level PA as well as the CDMA transmitter chain will be presented. Measurement setup and results will be presented in section 4.4.4.

4.2.2 Duplexer

For modern cellular phone systems, SAW (surface acoustic wave) filters are usually used to implement the duplexer function. However, the common working frequency band for SAW filters is only from around 20 MHz to 3 GHz, which is much lower than the frequencies needed for the hybrid engine controller board. An on-chip duplexer is designed based on the specifications in Table 4-4. The insertion loss targets of TX band (from 15.6 GHz to 18 GHz) and RX band (from 24.2 GHz to 27 GHz) are 3 dB. The other criterion is isolation between TX and RX should be 30 dB or better. It is challenging to realize the low insertion loss target using on-chip inductors.

Two 3rd order Chebyshev band stop filters (BSF) are also used to achieve lower insertion loss and sharper notch response at rejection bands (Figure 4-14 [40]). Figure 4-15 shows the schematic of the single-ended on-chip duplexer. It includes 3 inductors and 3 capacitors at TX and RX sides. L_{a1}, L_{a2}, and C_{a3} form a low pass filter (LPF) and C_{a1}, C_{a2}, and L_{a3} form a high pass filter (HPF). At TX side, the stopbands of LPF and HPF are overlapped to notch out RX signals, vice versa. Figure 4-16 is the micrograph of differential on-chip duplexer, which is fabricated in UMC 130-nm technology. The measurement results are discussed in section 4.4.1.

4.2.3 Mixer

Figure 4-17 shows a schematic of the double balanced Gilbert cell up-conversion mixer. Usually, LO power is large. A double balanced structure can alleviate the LO leakage problem due to the opposite phases. The input signals at IF and LO ports are provided from the PLL and divider chains, which are discussed in section 4.2.4. A 50-Ω input matching network of IF port is included for testing.

Table 4-4. Specification of the on-chip duplexer.

		Performance target
TX band (PA port)	Insertion loss	Below 3 dB for 15.6 ~ 18 GHz
	Return loss	Below 10 dB for 15.6 ~ 18 GHz
RX band (LNA port)	Insertion loss	Below 3 dB for 24.2 ~ 27 GHz
	Return loss	Below 10 dB for 24.2 ~ 27 GHz
Antenna port	Return loss	Below 10 dB for 15.6 ~ 18 GHz and 24.2 ~ 27 GHz
PA and LNA	Isolation (Rejection)	Below 30 dB for 15.6 ~ 18 GHz and 24.2 ~ 27 GHz

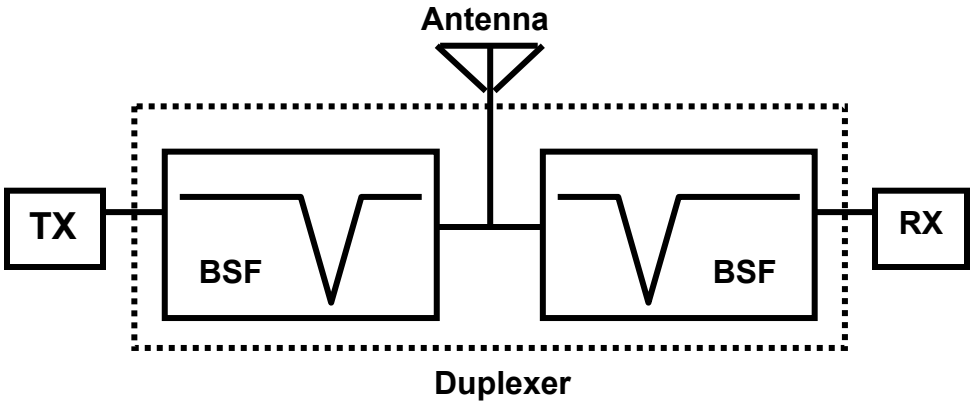


Figure 4-14. On-chip duplexer using two band stop filters [40].

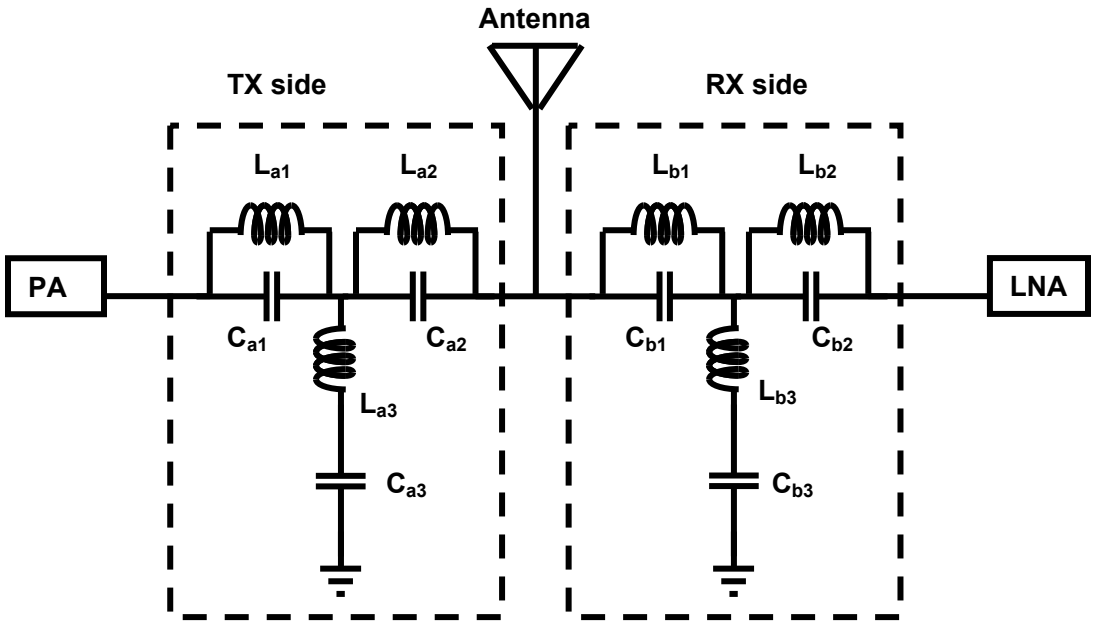


Figure 4-15. Schematic of the single-ended on-chip duplexer [40].

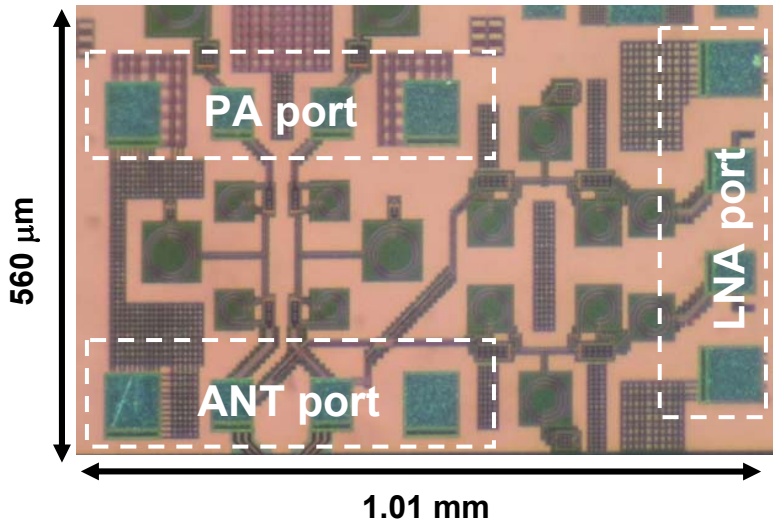


Figure 4-16. Die micrograph of the differential on-chip duplexer fabricated in the UMC 130-nm technology.

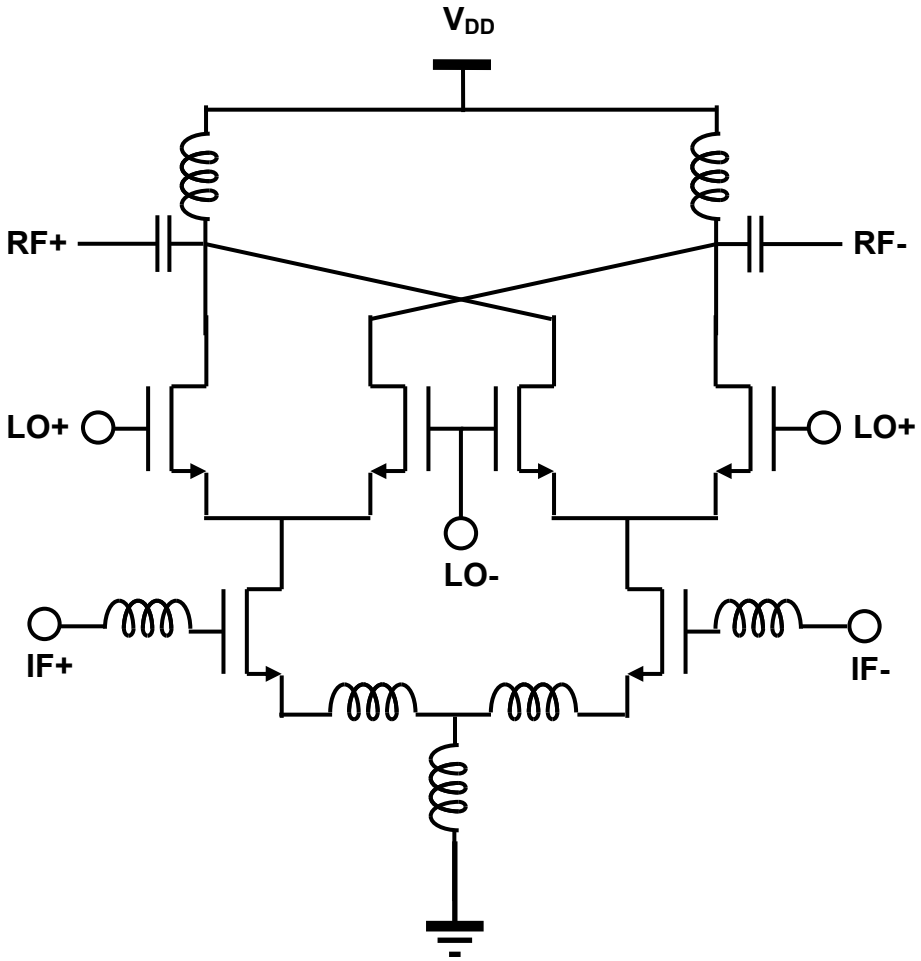


Figure 4-17. Schematic of double balanced Gilbert cell up-conversion mixer.

4.2.4 Divider Chain

As shown in Figure 4-10, a divider chain follows the PLL, which provides the 24-GHz carrier. The divider chain generates 12-GHz and 4.8-GHz signals for LO and IF signals for the mixer. The divider chain includes a divide-by-2 synchronous circuit, a divide-by-5 synchronous circuit, a multiply-by-2, and buffer stages. The most challenging block is the first divide-by-2 circuit, which has to work at 24 GHz [65]. The divider can operate up to 26 GHz with a 1.5-V power supply in the 130-nm CMOS technology. A divide-by-5 circuit is placed following the divide-by-2 circuit. It is the other challenging block [66]. The output load of divide-by-5 circuit has to be small to keep the loading of first divide-by-2 circuit. The divide-by-5 circuit should operate at 12 GHz [66].

Multiply-by-2 and phase-shift blocks are shown in Figure 4-18. The input of multiply-by-2 comes from the divide-by-5 output. One DCVSL buffer and three-stage inverter buffers are used to re-shape the waveform from the divide-by-5 block. The synchronous divide-by-5 is sensitive to the output load due to the fact that the 12-GHz input signal is connected to the output to form a loop. The output load is seen by the input 12-GHz signal. Therefore, the design challenge is to keep the load small for the divide-by-5 block to guarantee proper operation. A 2.4-GHz square wave is applied at M_1 and M_2 gates of frequency doubler. M_1 and M_2 will be turned on (linear region) and off (cut-off region) alternatively, like a switch. Therefore, the signals at node X will have frequency that is 2 times the input frequency, which is 4.8 GHz. 5-kΩ resistors are used to properly manage charging and discharging time constants, which are required to maintain sufficient amplitude at node X. The signal at node X is fed to an active balun to convert single ended signal to differential. The schematic of an active balun is shown in Figure 4-18 [67]-[69]. The differential 4.8-GHz signal is generated at the output of phase-shifter.

Two inductively loaded differential cascode buffers are used to amplify the signal before the mixer IF port. The tuned buffers band pass filter to knock down unwanted signals.

The divide-by-5 circuit output does not have 50% duty cycle. It has the ratio of T1 to T2 of 2:3, shown in Figure 4-18. The unequal duty cycle causes a mismatch problem and generates additional unwanted harmonics. In simulations, the widths of M_3 and M_4 have been intentionally mismatched as well as the load resistance R has been varied to account for +/- 20% variation to evaluate the robustness of design. By changing the widths of M_3 or M_4 from 16 μm to 12 μm or 20 μm, the mismatch of currents flowing through the two branches can be increased +/- 8.5%. This is significantly larger than the 3.5-% current mismatch expected for the process.

In addition to the 4.8-GHz signal, 2.4, 7.2, and 9.6-GHz signals as well as 2.4-GHz input signal mix with LO at 12 GHz, which generate 14.4, 19.2, and 21.6 GHz at the PA output. Table 4-5 shows the mismatch simulation results. It summarizes the signal strength difference between 2.4 and 4.8 GHz, 4.8 and 7.2 GHz, as well as 4.8 and 9.6 GH. It shows smaller signal strength

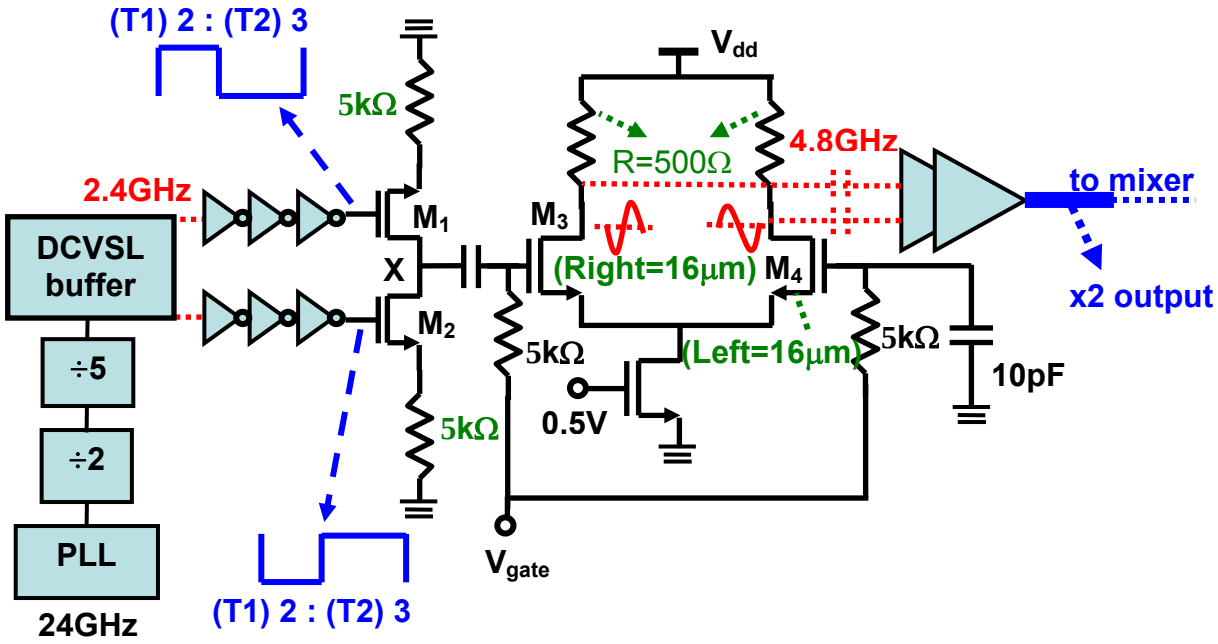


Figure 4-18. Schematic of multiply-by-2 and phase-shift blocks.

Table 4-5. Mismatch simulation results.

Cases	2.4-4.8 GHz	4.8-7.2 GHz	4.8-9.6 GHz
1x R, 16 μm (Right), 16 μm (Left)	43.93 dB	18.30 dB	46.46 dB
+20% R, 16 μm (Right), 16 μm (Left)	43.49 dB	18.39 dB	45.56 dB
-20% R, 16 μm (Right), 16 μm (Left)	44.46 dB	18.15 dB	47.51 dB
1x R, 16 μm (Right), 12 μm (Left)	44.12 dB	18.28 dB	50.46 dB
+20% R, 16 μm (Right), 12 μm (Left)	43.70 dB	18.38 dB	49.92 dB
-20% R, 16 μm (Right), 12 μm (Left)	44.63 dB	18.15 dB	50.98 dB
1x R, 12 μm (Right), 16 μm (Left)	44.11 dB	18.22 dB	42.78 dB
+20% R, 12 μm (Right), 16 μm (Left)	43.66 dB	18.31 dB	41.34 dB
-20% R, 12 μm (Right), 16 μm (Left)	44.67 dB	18.09 dB	44.57 dB
1x R, 16 μm (Right), 20 μm (Left)	43.82 dB	18.31 dB	44.52 dB
+20% R, 16 μm (Right), 20 μm (Left)	43.39 dB	18.39 dB	43.47 dB
-20% R, 16 μm (Right), 20 μm (Left)	44.38 dB	18.20 dB	45.76 dB
1x R, 20 μm (Right), 16 μm (Left)	43.82 dB	18.36 dB	49.12 dB
+20% R, 20 μm (Right), 16 μm (Left)	43.40 dB	18.45 dB	48.31 dB
-20% R, 20 μm (Right), 16 μm (Left)	44.36 dB	18.23 dB	49.48 dB

difference between 4.8 and 7.2 GHz. After the up-conversion mixer, 7.2-GHz signal will become 19.2 GHz, which is close to the desired frequency band (from 15.6 GHz to 18 GHz). Since there is a duplexer following the PA stage, the 19.2-GHz signal is attenuated by 3.7 dB. The interference concern from the mismatch should be taken in to consideration, which is discussed in section 4.4.5.

4.3 Simulation Results: Multi-Level Signal at PA Output

Figure 4-19 shows the TX chain simulation results of multi-level signals at the differential PA output. The target levels are 0.63, 0.93, 1.15, 1.34, 1.48, and 1.62 V. Although the desired output power is ~ 10 dBm, higher simulated output power is needed for margin. Although the inductor gate bias technique has been applied, the self oscillation is suppressed by the source impedance change as discussed in section 4.2.1. The level 0 switch is placed at the gate of second pre-driver stage to lower the drivability requirement for the coder.

As mentioned earlier, additive/subtractive coding scheme is used to reduce the rise and fall time of the output envelope. The output at level 0 can be minimized to close to 0 V (shown

in Figure 4-19(a)). Table 4-6 summarizes the simulated ratio between the output levels and attenuator sizes. The error percentage is calculated compared to the targets. The worst cases are the level 2 to level 1, and level 4 to level 1 ratios, which have ~ 7.0-% error. The biggest load for the attenuators is due to the level 0 switches, which is ~ 12 fF.

Figure 4-19(a) shows the simulation results for the differential PA with a decoder from 5 ns to 30 ns. The level information is (0241353246). The rise time and fall time at PA output are related to the equivalent RC network time constant. In the simulations, larger interconnection parasitics than actual are included to over-estimate the load for the coder. The simulation results shown in Figure 4-19(a) has ~ 32-% rise time (800 ps) from level 0 to level 2. It decreases the level-2 period to 1.6 ns instead of 2 ns simulation target (250-ps rise and fall times). Most of the rise and fall time for other transitions are within 10 %. This shows that it is feasible to achieve the multi-level PA outputs with a 16.8-GHz carrier and a 400-Mbps envelope. The measurement results as well as further discussions are presented in section 4.4.4. Figure 4-19(b) shows the simulated CDMA waveform at the TX output up to 180 ns.

Table 4-6. Simulation results of ratio between level N and level 1, where N equals to 2, 3, 4, 5 and 6.

Ideal ratio		Simulated value	Simulated ratio	Error (%)
Level6 / Level1	2.450	1.62 (L6) / 0.625 (L1)	2.59	5.7
Level5 / Level1	2.236	1.48 (L5) / 0.625 (L1)	2.37	6.0
Level4 / Level1	2.000	1.34 (L4) / 0.625 (L1)	2.14	7.0
Level3 / Level1	1.732	1.15 (L3) / 0.625 (L1)	1.84	6.2
Level2 / Level1	1.414	0.93 (L2) / 0.625 (L1)	1.49	7.0
Switch size (transistor width and length)				
Level 6 – (0.25 μm / 120 nm) x 1 => differential loading: 0.50- μm width				
Level 5 – (0.25 μm / 120 nm) x 3 => differential loading: 1.50- μm width				
Level 4 – (0.25 μm / 120 nm) x 5 => differential loading: 2.50- μm width				
Level 3 – (0.25 μm / 120 nm) x 6 => differential loading: 3.00- μm width				
Level 2 – (0.25 μm / 120 nm) x 6 => differential loading: 3.00- μm width				
Level 1 – (0.25 μm / 120 nm) x 9 => differential loading: 4.50- μm width				
Level 0 – (0.25 μm / 120 nm) x 36 => differential loading: 18.0- μm width				

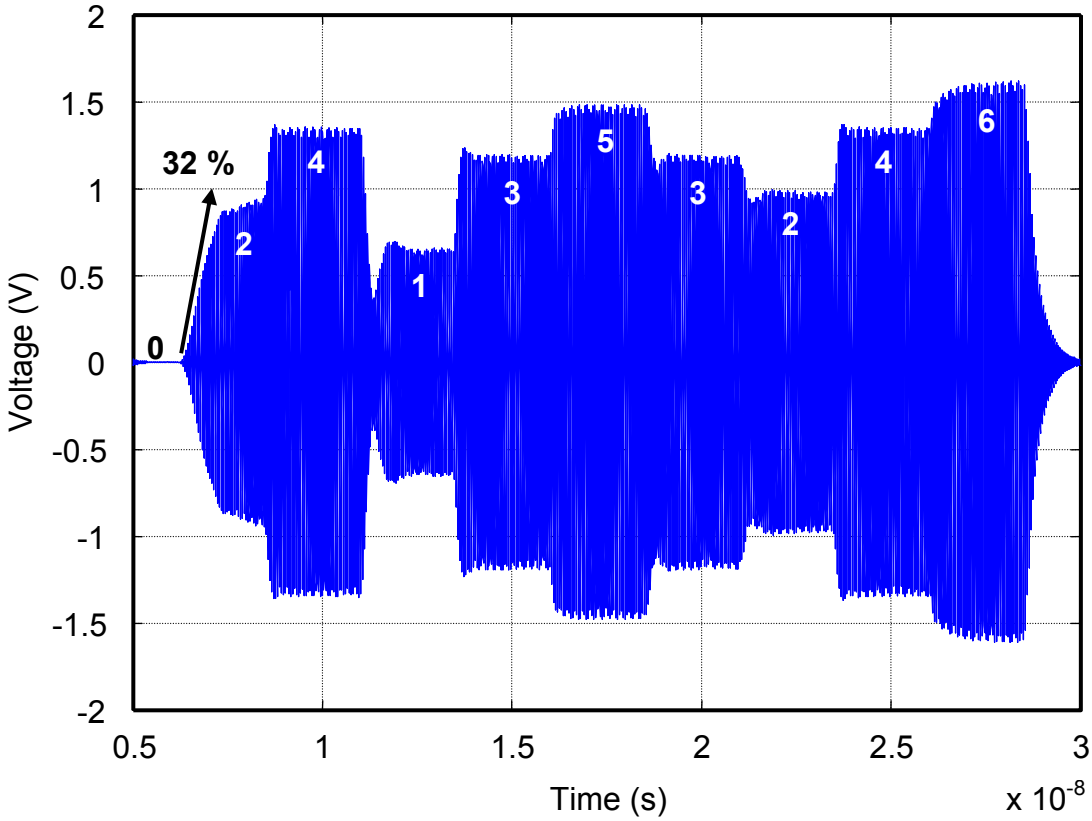


Figure 4-19(a). Simulation results of multi-level signals at differential PA output.

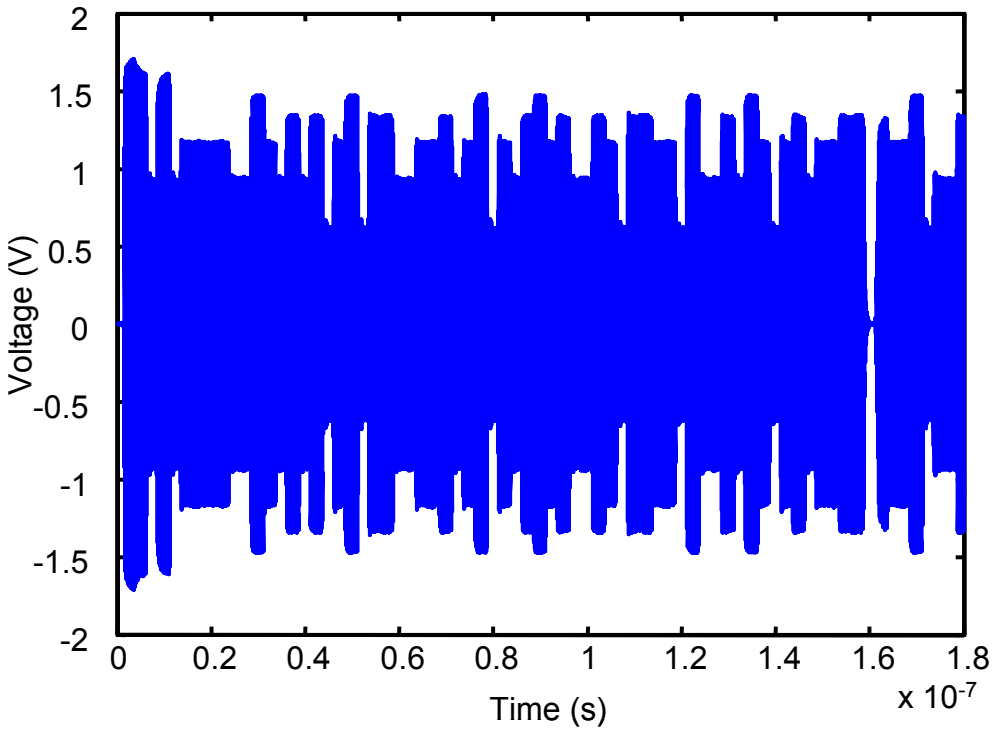


Figure 4-19(b). TX chain simulation up to 180 ns.

4.4 Measurement Results

4.4.1 Duplexer

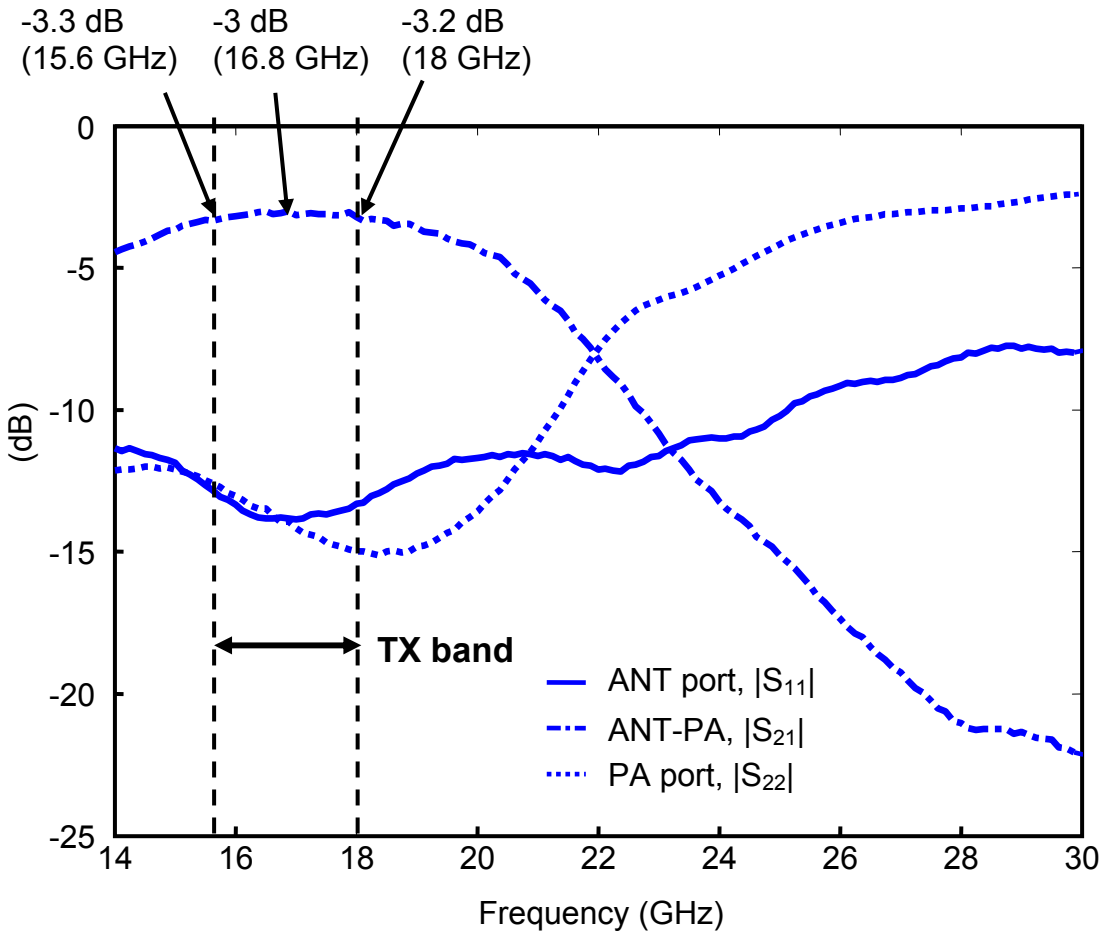


Figure 4-20. Plots of insertion loss and return loss between antenna (ANT) port and PA port. (TX band: 15.6-18 GHz)

Figure 4-20 shows the measured 2-port S-parameters between the duplexer PA and ANT ports. It shows that the insertion loss is ~ 3 dB from ~ 15.6 GHz to ~ 18 GHz. Return loss of the PA port and antenna port are below 10 dB within the desired band (from 15.6 GHz to 18 GHz). The insertion loss performance meets the specification.

Figure 4-21 shows the measured 2-port S-parameters between duplexer LNA and ANT ports. It shows that the insertion loss is ~ 6 dB at 25.6 GHz. The lowest insertion loss is ~ 3.3 dB at 30 GHz, which is higher than the target frequency of 25.6 GHz. Return loss of the LNA port

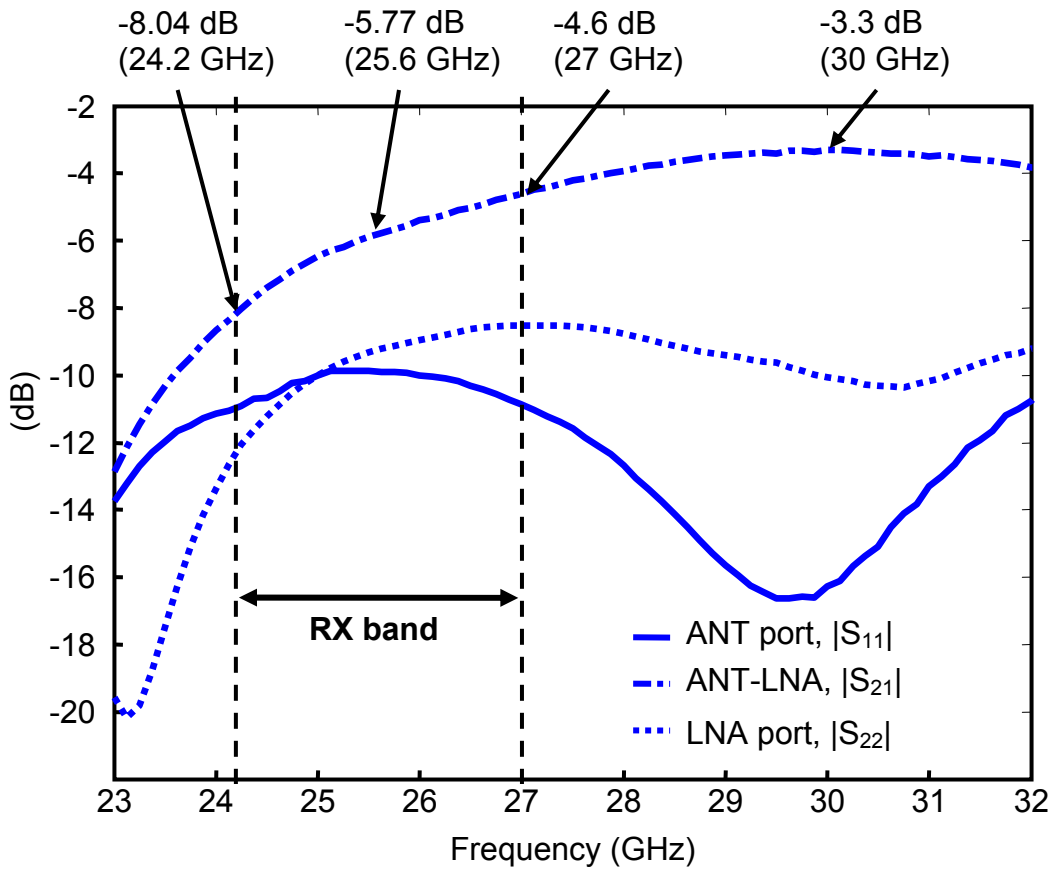


Figure 4-21. Plots of insertion loss and return loss between antenna (ANT) port and LNA port. (RX band: 24.2-27 GHz)

and antenna port are all around 10 dB within the desired band (from 24.2 GHz to 27 GHz). The insertion loss performance meets the specification except the frequency needs to be re-tuned from 30 GHz to 25.6 GHz.

PA output power is usually much larger than the received power at LNA port. Hence, the isolation between PA and LNA ports is important. High transmitted power can not affect LNA operation if the duplexer can provide good isolation between the two ports. As shown in Figure 4-22, the rejection is ~ 23 dB at ~ 16.8 GHz and 25.6 GHz. It is smaller than the 30-dB target.

By more precisely modeling the interconnection parasitics between on-chip passive components, the newly designed duplexer has better insertion loss performance at both TX and

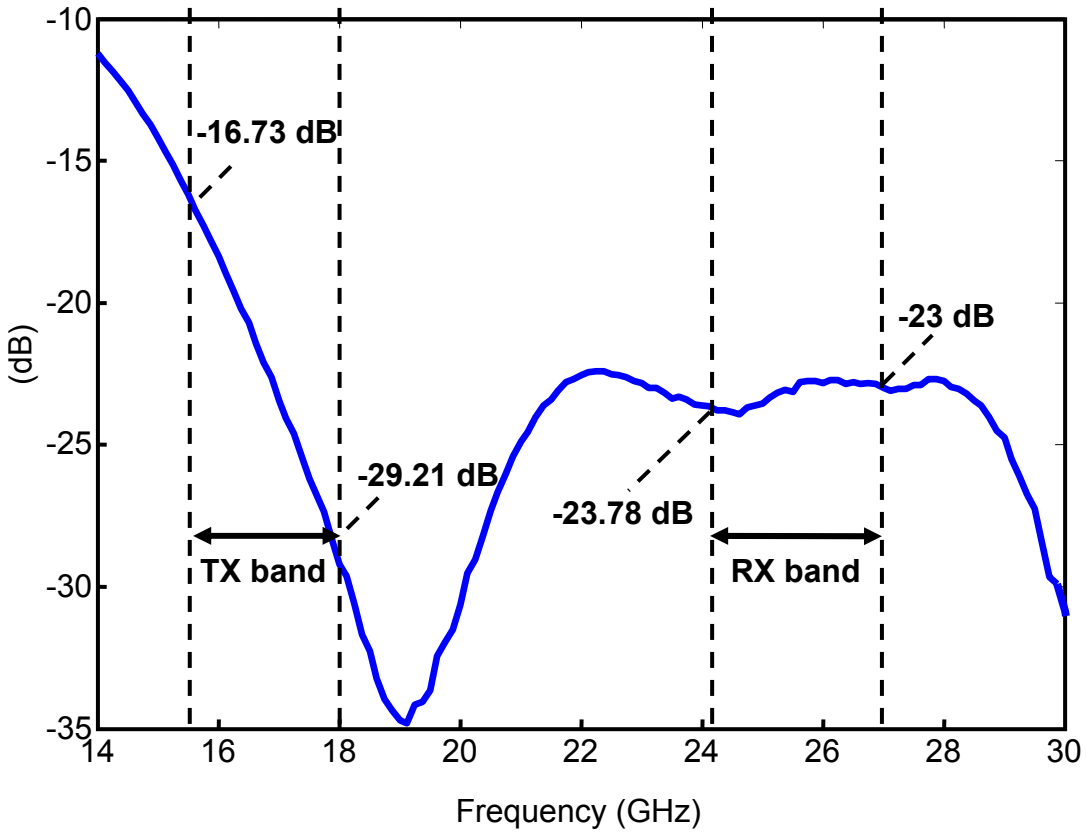


Figure 4-22. Measured insertion loss between PA port and LNA port.

RX bands. Especially, the insertion loss gets improved by 3 dB (improve from 6 dB to 3 dB) at TX band compared with the first design. The isolation between LNA and PA ports shows 5-dB degradation (degrade from 28 dB to 23 dB). The key factor improving the insertion loss is to arrange passive components close to each other, which leads to shorter interconnects (smaller parasitics). The compact design not only improves the insertion loss performance, but also saves the chip area.

4.4.2 24-GHz Phase-Locked Loop (PLL)

Figure 4-23 shows a die micrograph of the integer-N PLL. Its area is 1.2 by 0.6 mm^2. Figure 4-24 shows a block diagram of the integer-N PLL [66]. It consists of an LC-VCO, a 256

prescaler, a phase frequency detector (PFD), a charge pump, and a third- order passive loop filter. The output frequency is from 23.5 GHz to 24.5 GHz at digital tuning bits of 111.

The measured PLL output spectrum is shown in Figure 4-25. Figure 4-26 shows the measured phase noise at PLL output frequency of 24.01 GHz. The in-band noise at 50-kHz offset is -76.75 dBc/Hz. The phase noise at 1-MHz offset is -93.55 dBc/Hz and the out-of-band phase noise at 10-MHz offset is -114.03 dBc/Hz. The output spectrum was measured when the reference frequency is 93.75 MHz.

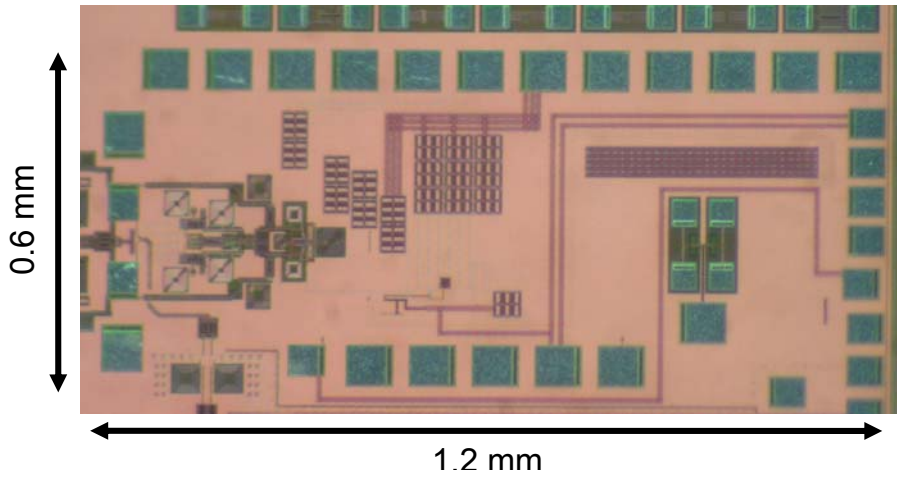


Figure 4-23. Micrograph of the integer-N PLL.

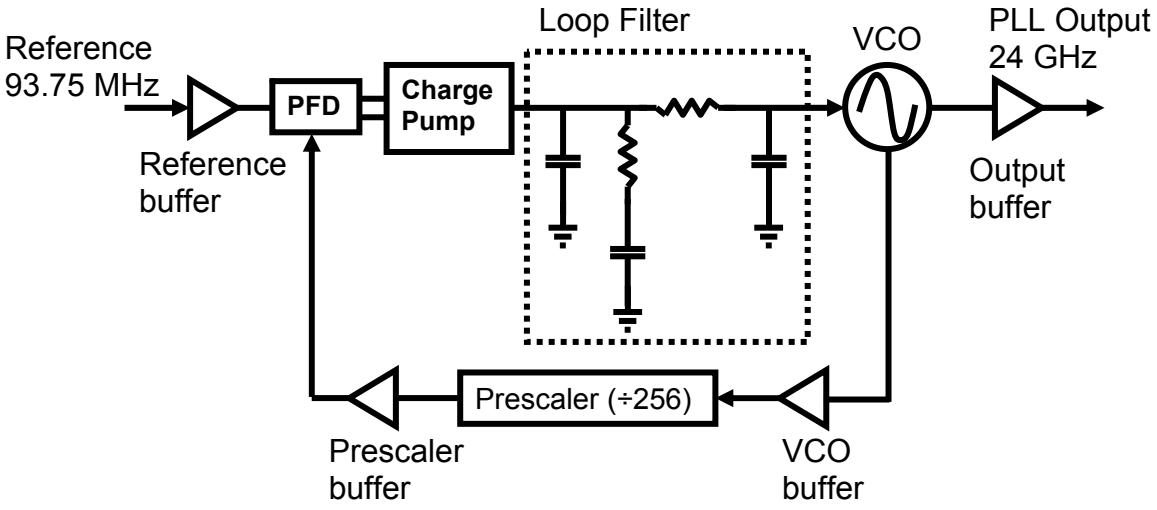


Figure 4-24. Integer-N PLL block diagram.

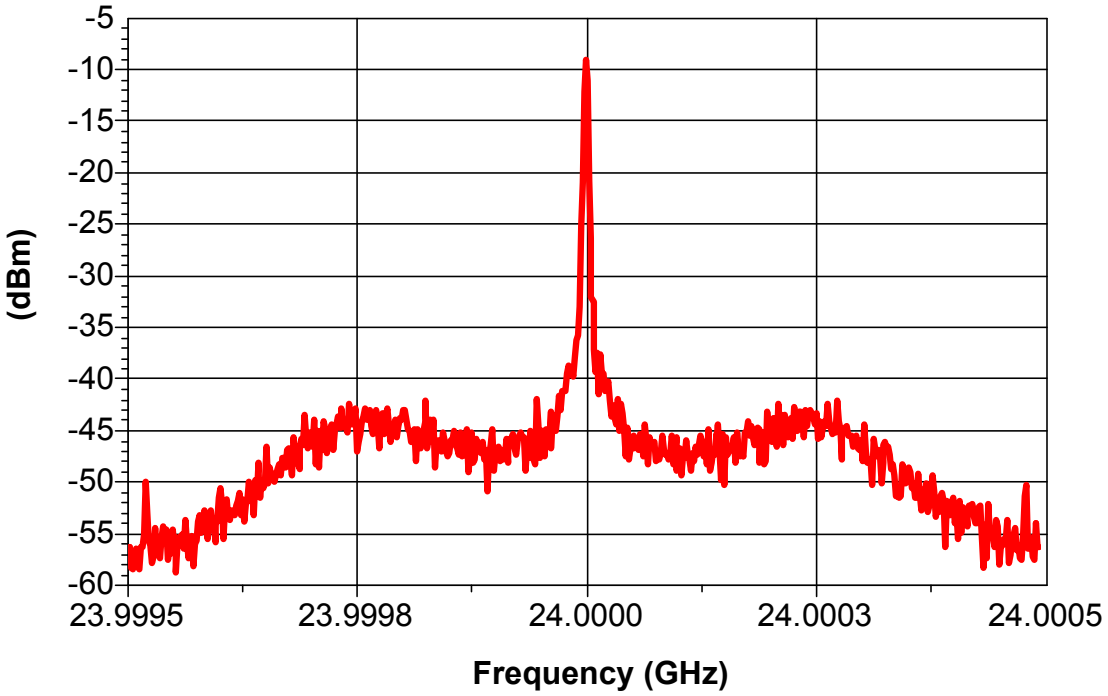


Figure 4-25. Measured PLL output spectrum (Span=1 MHz, RBW=3 kHz, VBW=100 Hz).

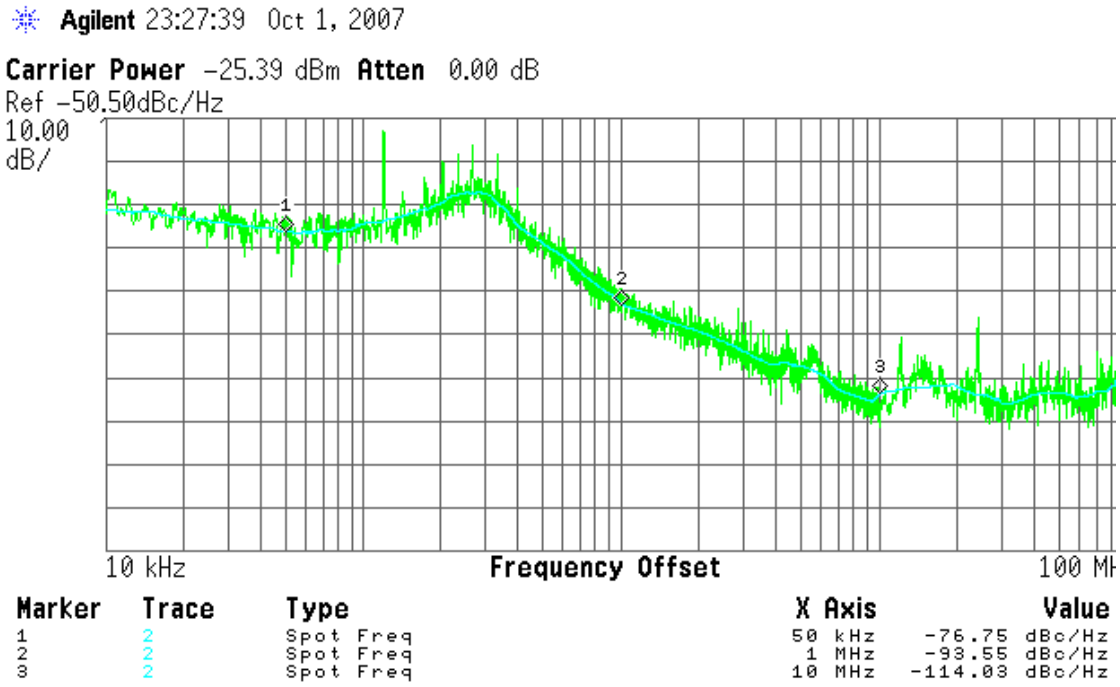


Figure 4-26. The PLL phase noise plot measured using an Agilent E4448A spectrum analyzer.

4.4.3 4-mm On-Chip Dipole Antenna

Figure 4-27 shows the 4-mm dipole antenna input impedance measurement results. Figure 4-27(a) shows $|S_{11}|$. Figure 4-27(b) shows the real part and imaginary part of input impedance. The imaginary part approaches zero at around 16.9 GHz and the real part is about 220 Ω. It means the 4-mm on-chip dipole antenna is resonant at the desired frequency band and well suited for use at 16.8 GHz. If the measured impedance is used for the duplexer simulation instead of using 50-Ω port impedance, the insertion loss between the PA and ANT ports and LNA to ANT ports degrade by less than 1 dB. The design for conjugate matching network at the interfaces requires more inductors and capacitors. It turns out that the matching network introduces more loss, while consuming a larger die area. Therefore, the duplexer is designed and implemented assuming a 50-Ω system.

4.4.4 Multi-Level Power Amplifier

Figure 4-28 shows the large signal measurement setup for frequency and time domains characterization. For frequency domain measurements, the output is connected to a power meter with a HP8485A power sensor. For the time domain measurement, the output is connected to an Agilent 86100B wide bandwidth oscilloscope. In order to characterize the time domain response of the multi-level PA, an on-chip divide-by-32 block is built-in to generate low frequency divided signal for oscilloscope triggering. The address decoder's inputs are fed from a Tektronix HFS 9009 Stimulus System, which can provide 4 synchronized signals up to 400 MHz. The clock is 400 MHz and the frequency of inputs for the address decoder is 200 MHz.

At 1.5-V supply for the driver stages and 1.2-V supply for the PA stage, Figure 4-29 shows the single-ended PA is able to achieve 10-dBm saturated power and ~ 22% PAE at 16.8 GHz while drawing 30.5 mA and consuming 45.75 mW. The output P_{1dB} (OP_{1dB}) is ~7.5 dBm,

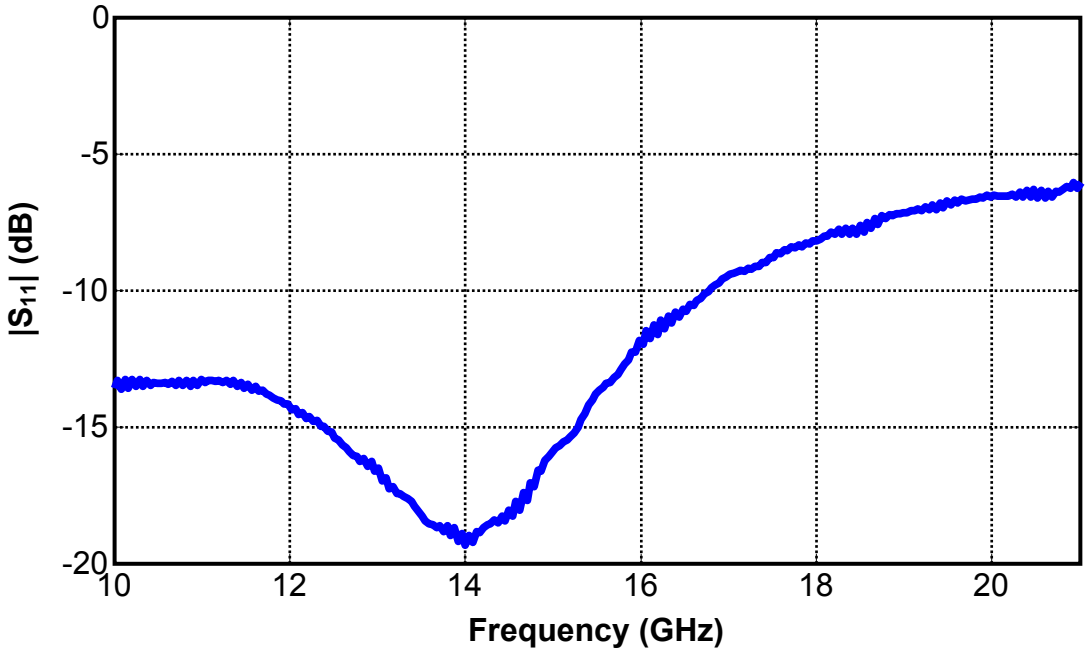


Figure 4-27(a). $|S_{11}|$ for 4-mm on-chip dipole antenna.

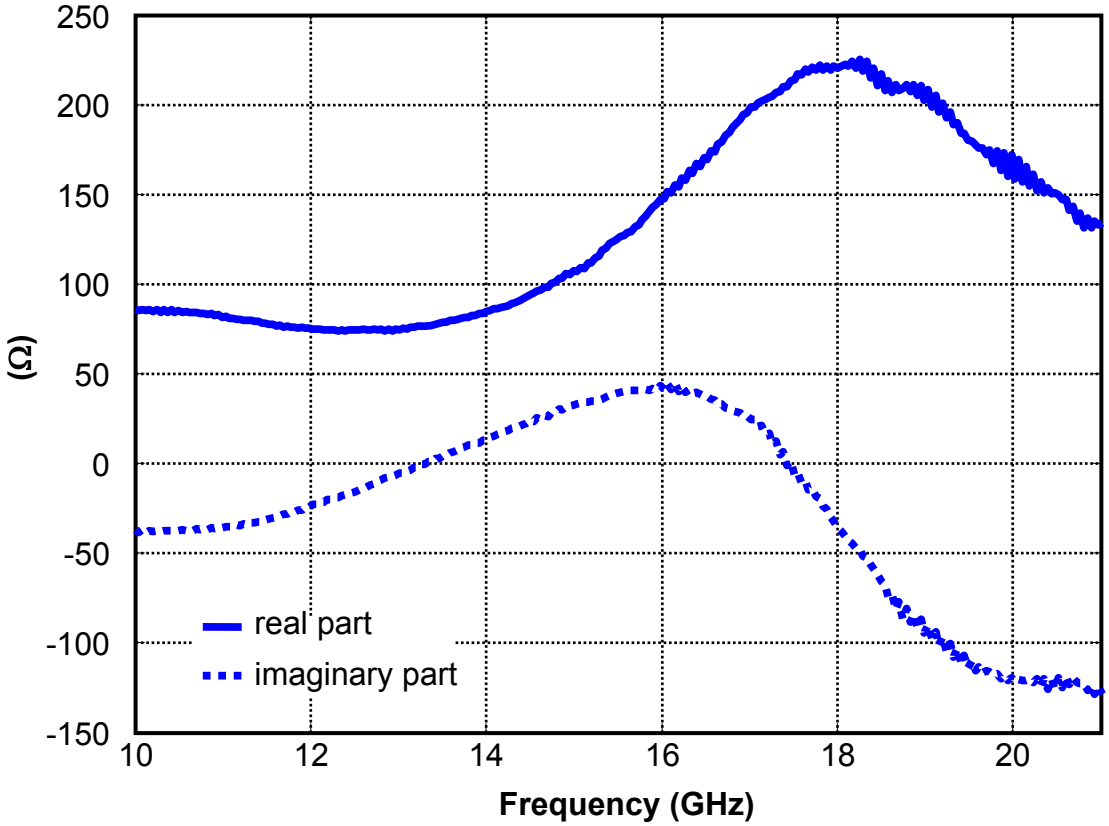


Figure 4-27(b). Input impedance for 4-mm on-chip dipole antenna.

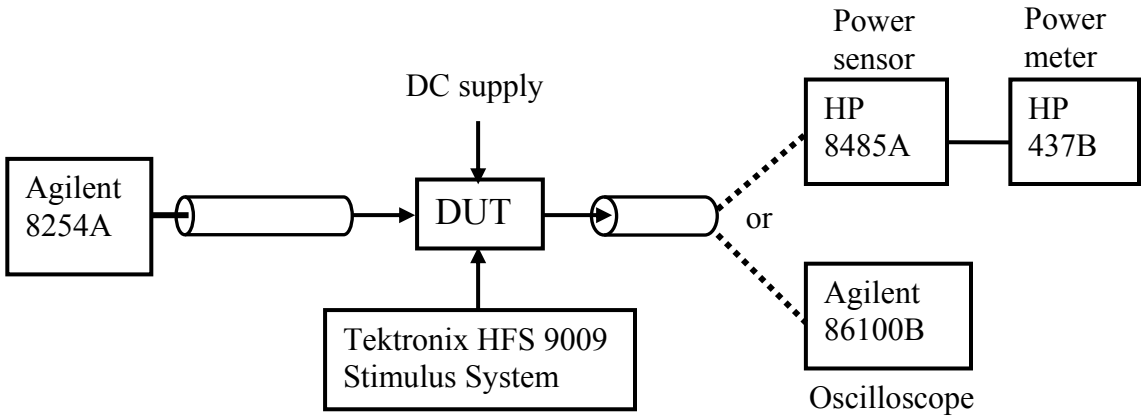


Figure 4-28. PA measurement setup for frequency domain and time domain.

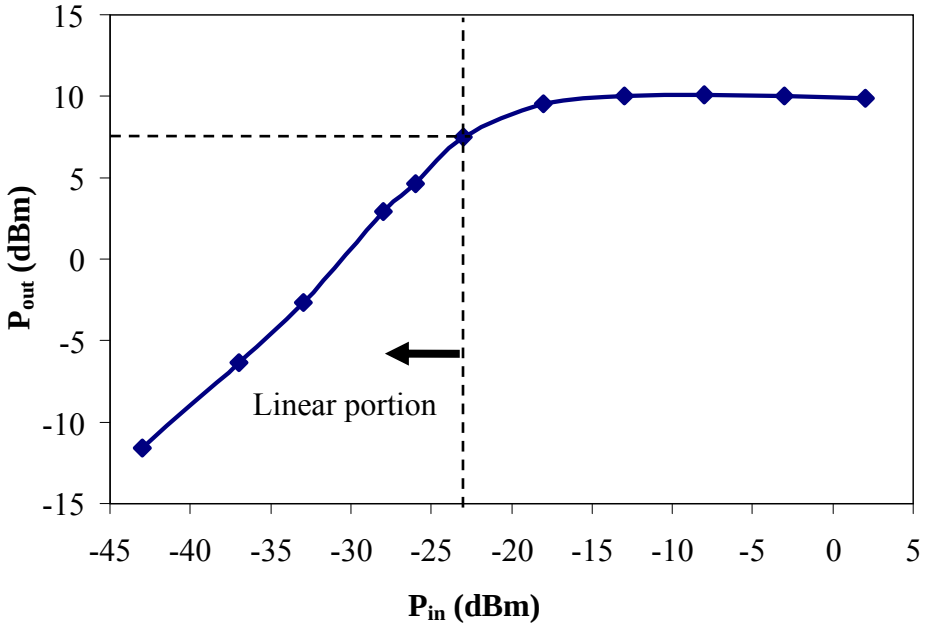


Figure 4-29. Output power vs. input power at V_{DD}=1.5 V for the driver stages and 1.2-V supply for the PA stage.

which corresponds to ~ 10.5-dBm OP_{1dB} for a differential PA structure. The idea is to use the linear portion below OP_{1dB} point for multi-level amplitude modulation.

Figure 4-29 shows that it is possible to provide enough linear power and lead to ~ 21-dB link margin based on the CDMA system analysis, shown in Table 1-1. The link margin analysis is for a fully differential transmitter structure, and receiver noise figure of 8 dB and sensitivity of -74.3 dBm.

By applying constant DC inputs to the address decoder, static level test can be performed. Figure 4-30(a) shows the static time domain measurement results for level 0 and level 6. Level 2 to level 5 measurement results are summarized in Table 4-7. After de-embedding the probe and cable loss, the corresponding output power for level 6 is ~7 dBm, which means the single-ended PA operates close to the OP_{1dB} point This is consistent with the original design. Figure 4-30(b) is the dynamic measurement results of a randomly chosen pattern (0241353246). The inputs and clock for the address decoder are generated from a Tektronix HFS 9009 Stimulus System. The rise and fall time of the 3 inputs and clock are set to be 200 ps, which is limited by the equipment. There are built-in inverter buffer chains for re-shaping the input waveform to be more square. Each level has ~ 2.5-ns period, which corresponds to the 400-Mbps data rate. Table 4-7 summarizes the measurement results of level ratio between level N (N=6, 5, 4, 3, 2) and level 1, and error percentage compared with the original specification. The maximum error percentage is ~ 16 % for the case level 3 to level 1. From the measurements, the worst rise time is ~ 800 ps from level 0 to level 2, which is consistent with the result of circuit analysis mentioned in section 4.2. If the bias resistor at the gate of second pre-amplifier stage decreases to 2.5 kΩ, the rise time

Table 4-7. Measurement results summary of static case.

	V_{peak} (mV)	Power (dBm)
Level 0	31.01	-20.17
Level 1	268.23	-1.43
Level 2	331.51	0.41
Level 3	390.39	1.83
Level 4	478.63	3.6
Level 5	577.43	5.23
Level 6	692.63	6.81

Ideal ratio		Measured ratio results	Error (%)
Level 2 / Level 1	$\sqrt{2}$	1.24	-12.30
Level 3 / Level 1	$\sqrt{3}$	1.45	-16.00
Level 4 / Level 1	$\sqrt{4}$	1.79	-10.75
Level 5 / Level 1	$\sqrt{5}$	2.15	-3.85
Level 6 / Level 1	$\sqrt{6}$	2.58	5.3

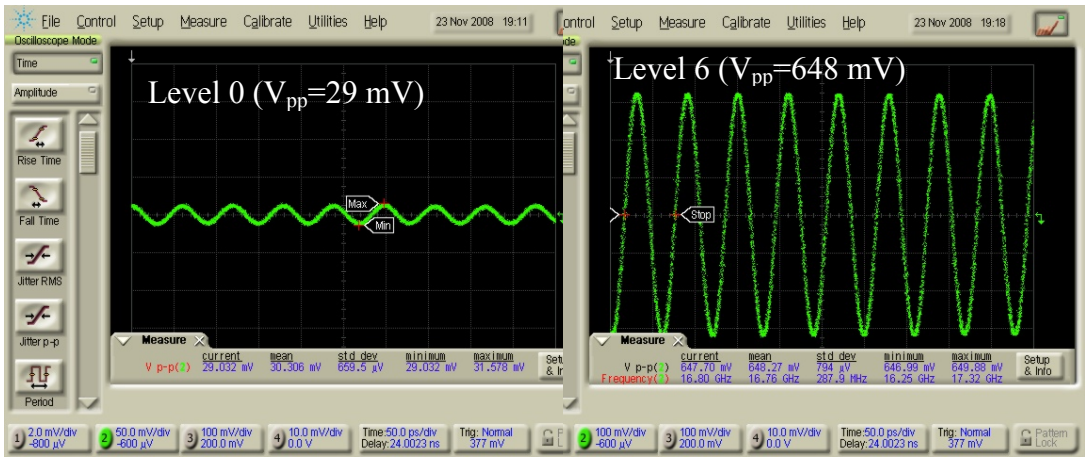


Figure 4-30(a). Static time domain measurement results for level 0 and level 6 operating at 16.8 GHz.

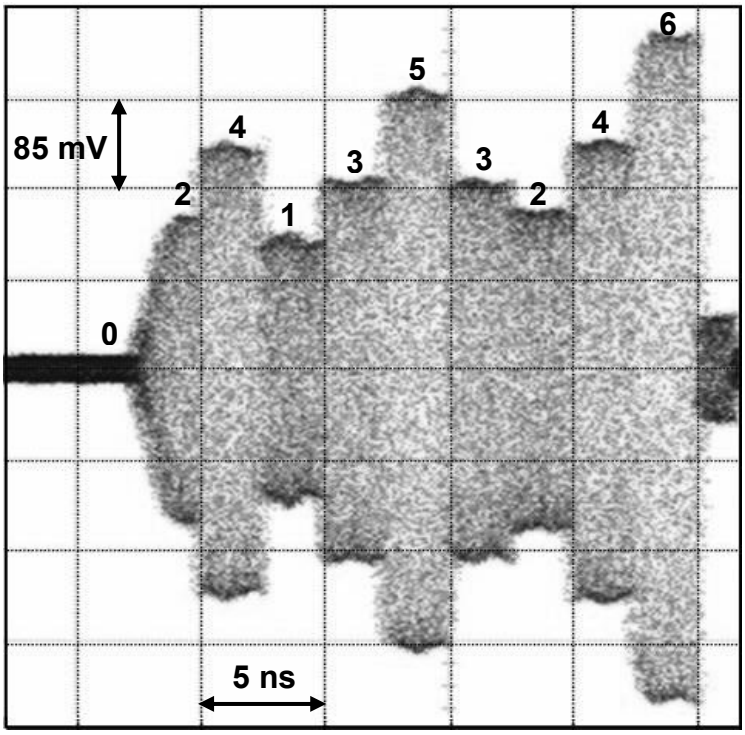


Figure 4-30(b). Dynamic time domain measurement results for pattern 0241353246.

(level 0 to level 2) can be improved to ~ 400 ps according to simulations. Other rise and fall times are all around 200 ps. Figure 4-31 shows the die micrograph. The differential class-E PA with an address decoder occupies ~ 1.37 mm^2 including pads.

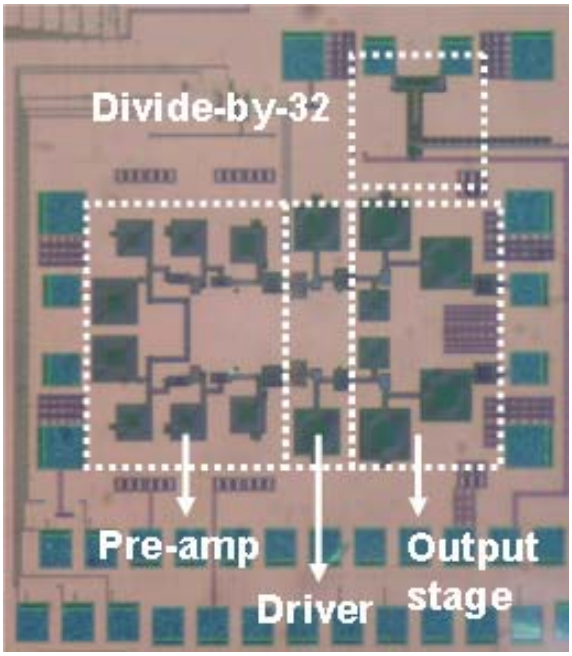


Figure 4-31. Die micrograph of the differential multi-level power amplifier. Chip size is 1.14 mm x 1.2 mm.

4.4.5 CDMA Transmitter Chain

A standalone coder, and the second one integrated with a full transmitter chain [45] are fabricated. To reduce the die area, these two coders share the same input, clock, and reset pads. The output of the standalone coder test structure is connected to its own output pads. The one integrated with TX chain is connected to the attenuator switches to provide the control signals. By inserting a simple bidirectional 3-bit bus between the adder and the decoder, shown in Figure 4-32, it is possible to apply input signals directly from an external signal generator and bypass the coder core blocks [45]. This provides flexibility for testing. The internal node, like the adder outputs can also be monitored through the 3-bit bus. This is critical for debugging the CDMA TX chain. Table 4-8 shows the control signal setup of the 3-bit bus. The coder occupies 336×276 μm^2. The TX chain testing is done on a PCB. The design considerations for the TX PCB are described in Appendix B.

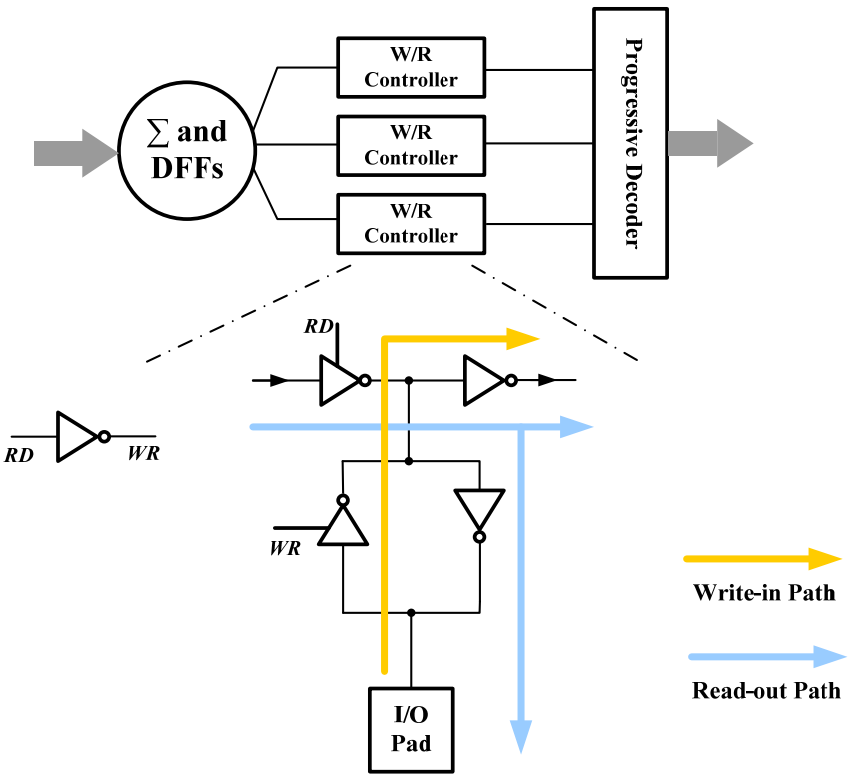


Figure 4-32. Bidirectional 3-bit bus design between the adder and the decoder. The read-out path is turned on when the "*RD*" is "1", while the write-in path is turned on when the "*RD*" is 0.

Table 4-8. Bidirectional 3-bit bus settings for different tests.

	RD_SL	***RD_TX***
Standalone: Read Out	1	0
Standalone: Write In	0	0
Coder with TX: Read Out	0	1
Coder with TX: Write In	0	0

Figure 4-33 shows the die micrograph and the PCB used in the transmitter chain measurements. The TX chain measurement was made by applying an external 24-GHz source due to the insufficient drivability at the interface between the PLL output and following divide-by-2 block. The buffer stages at this interface have to be re-tuned in the next tapeout. The tested blocks are shown in Figure 4-34. The dotted block, PLL, is bypassed. As mentioned in section 4.1, the 24-GHz signal is frequency divided down to 12 GHz and 4.8 GHz to generate the IF and

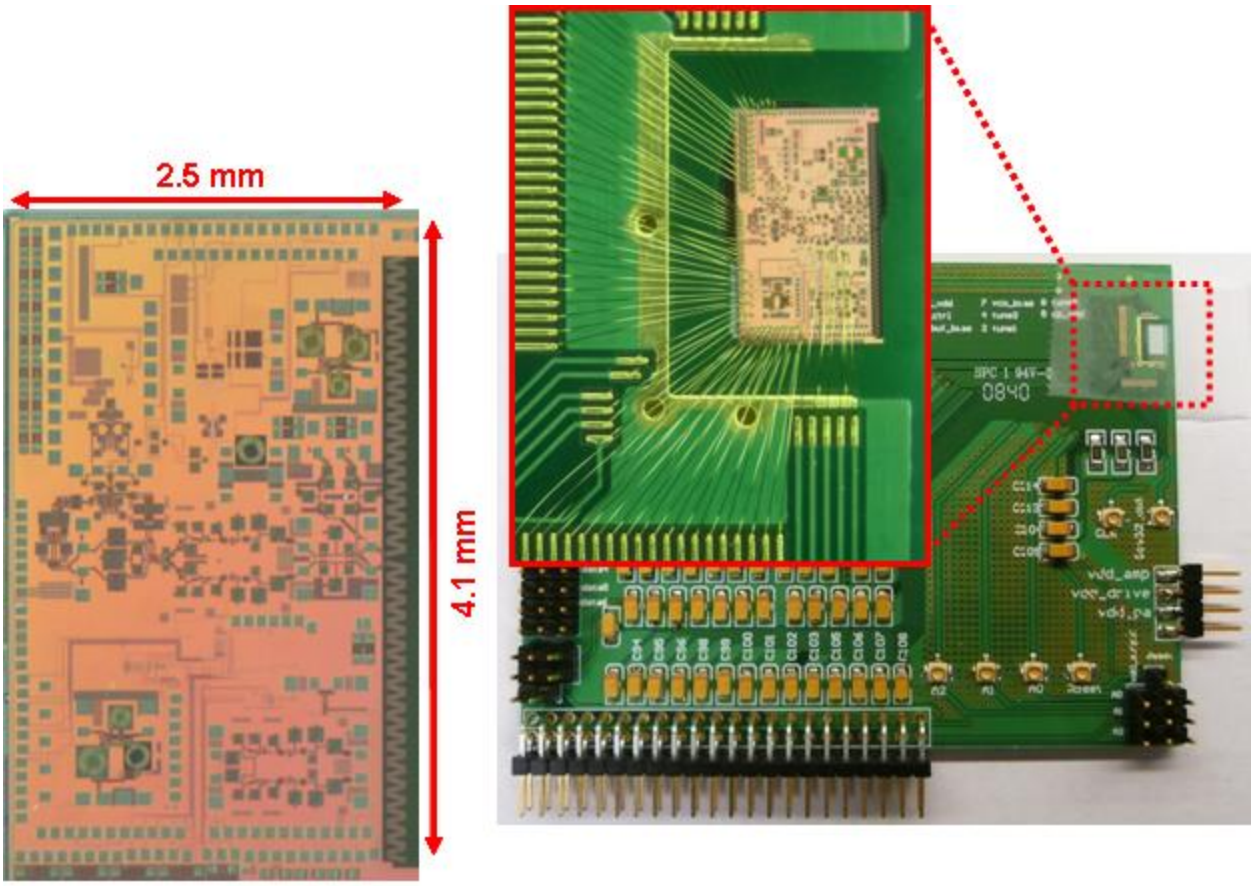


Figure 4-33. Micrograph of the CDMA TX chain and the PCB.

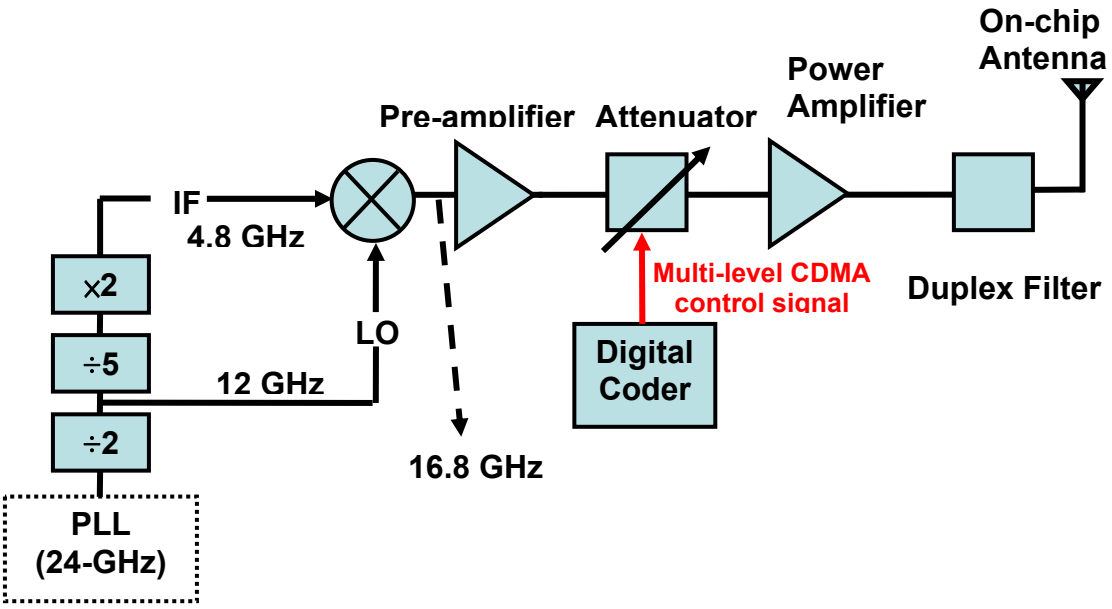


Figure 4-34. CDMA TX chain block diagram. The measurement was done using an external 24-GHz source due to the insufficient drivability at the interface between the PLL output and following divide-by-2 block.

LO inputs of the mixer. During the frequency division, unwanted harmonics are also generated, which show up at the TX output. For example, due to the inverter buffers at the output of divide-by-5 block, the odd-order harmonics of 2.4 GHz would be produced, like that at 7.2 GHz. Even order harmonics are also generated because the duty cycle is not 50 % at the divide-by-5 output (mentioned in section 4.2.4). All the harmonics will be up-converted with the 12-GHz LO signal. Therefore, lots of unwanted harmonics can be observed at the PA output, shown in Figure 4-35.

By observing the harmonic frequencies at the TX output, it is possible to infer that the divider chains and the mixer stage are properly functional. For example, the 12-GHz signal is generated from the divide-by-2 block and amplified by the LO buffers. The signal can couple through the other circuit blocks or ground plane and show up at the TX output. If the 12-GHz signal is shown at the TX output, that means the divide-by-2 circuit and LO buffers are operational. Based on this approach, multiply-by-2, divide-by-5, and mixer stages are all functional. Therefore, correct harmonic frequencies can be seen in the TX output spectrum (Figure 4-35). The TX band is from 15.6 to 18 GHz. The highest and closest unwanted signal is at 19.2 GHz, which comes from the 12-GHz LO mixing with the 7.2-GHz harmonic. The difference between the desired 16.8-GHz signal and 19.2-GHz unwanted interferer is ~ 10 dB, which is measured at duplexer output without the on-chip antenna connected. Since the antenna is tuned for use in 16.8 GHz, the 19.2-GHz interferer should be attenuated by 0.5 dB more due to the 4-mm on-chip dipole antenna. There are two small peaks besides the 16.8 and 19.2 GHz peaks. Those peaks are 400 MHz away from the main peaks. It comes from the leakage of the 400-MHz clock for the coder.

In order to verify the effect of the unwanted 19.2-GHz signal, the system simulation of the CDMA transceiver is performed in Advanced Design System (ADS) simulator. Figure 4-

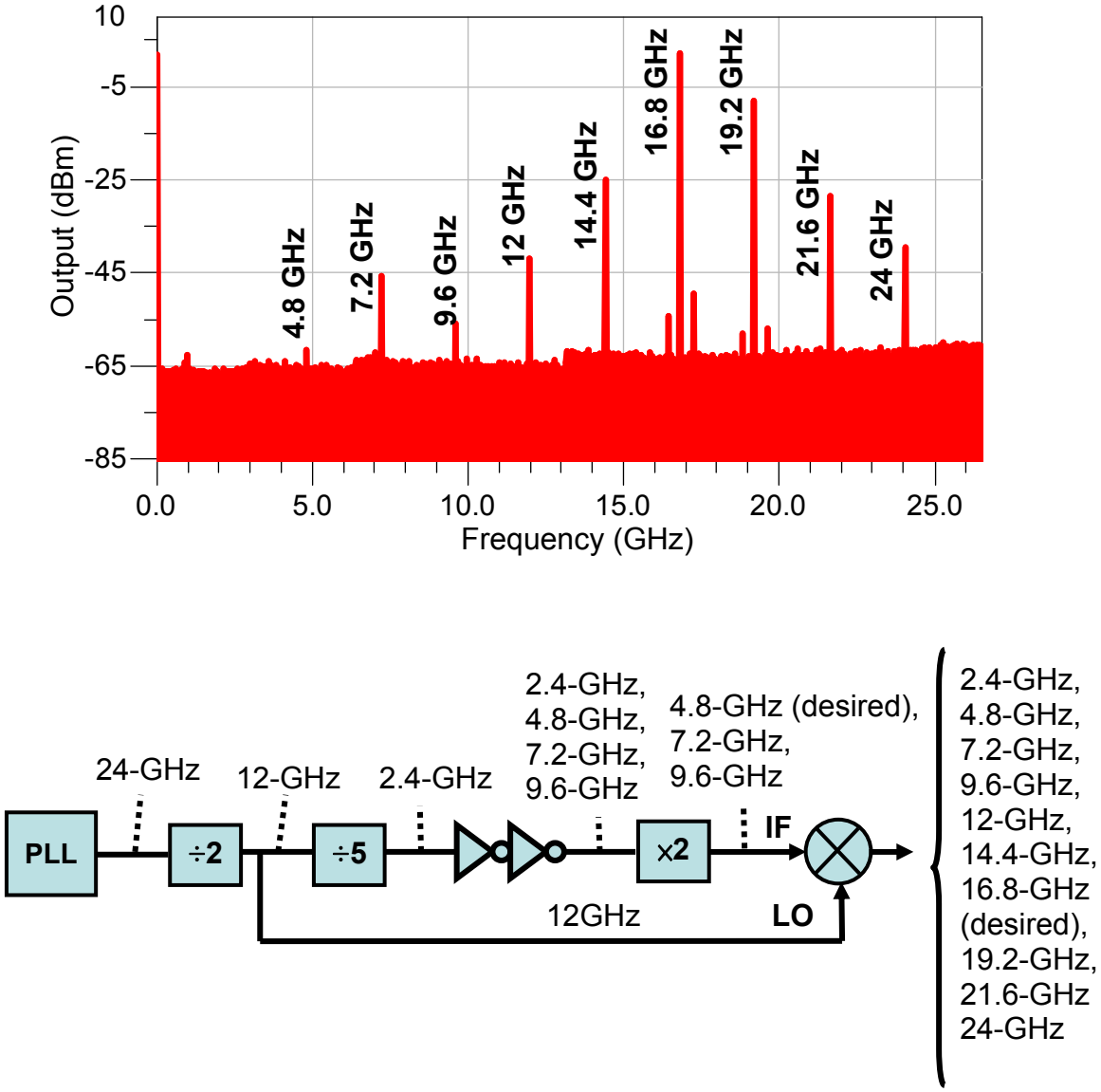


Figure 4-35. Output spectrum at duplexer output without multi-level amplitude modulation.

36(a) shows the block diagram for the CDMA TRX simulation and the spectrum at the TX output. It includes a desired 16.8-GHz carrier and an unwanted 19.2-GHz interferer (10 dB lower than the 16.8-GHz signal) with data modulated. The simulation results in Figure 4-36(b) show that the base band output of the CDMA receiver is the same for two cases (pure 16.8-GHz carrier at TX output; a 16.8-GHz carrier with an unwanted 19.2-GHz interferer). This implies that the effect from the 19.2-GHz interferer is tolerable.

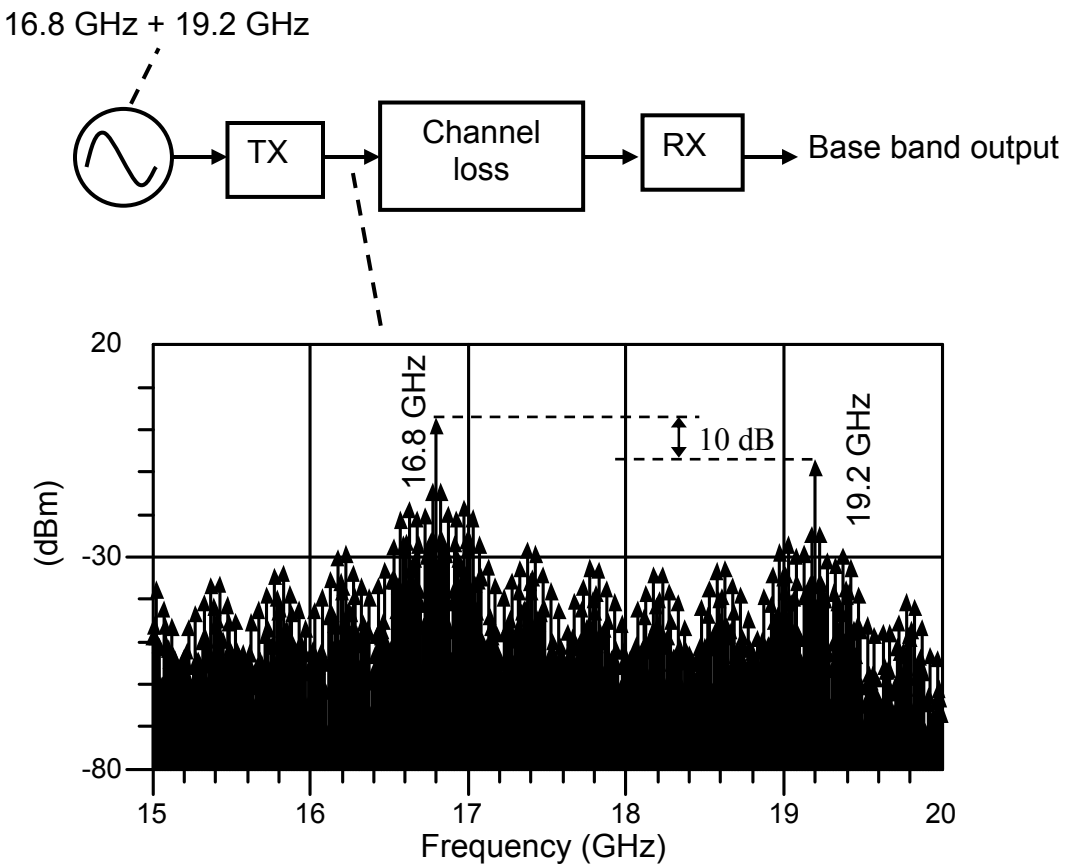


Figure 4-36(a). The CDMA TRX simulation block diagram and the spectrum at the TX output.

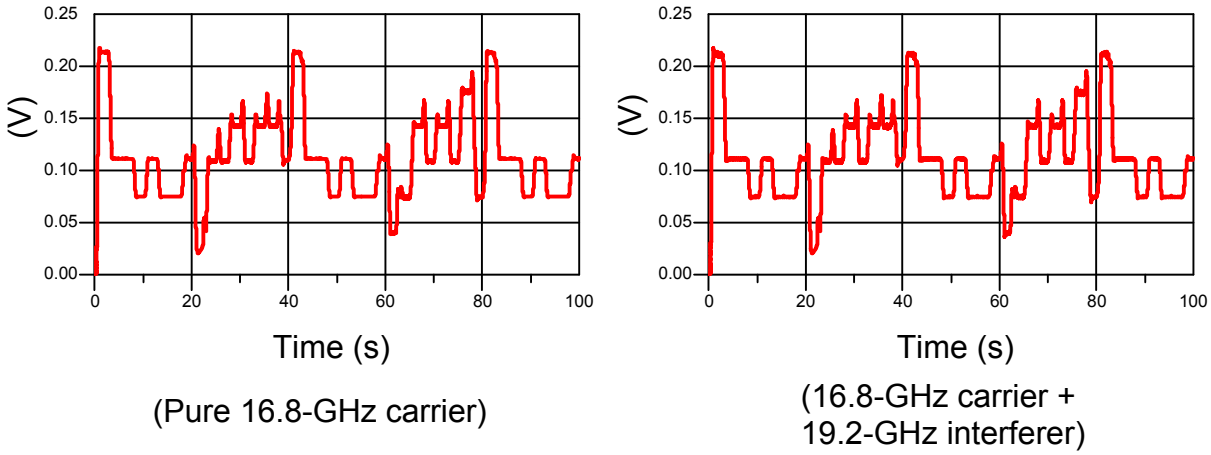


Figure 4-36(b). The base band output of the CDMA receiver for two cases (pure 16.8-GHz carrier at TX output; a 16.8-GHz carrier with an unwanted 19.2-GHz interferer).

In the TX chain characterization, the coder integrated with the 3-bit bus design has the option for testing with static levels before the dynamic measurement. The same method as the PA characterization is used. Constant external DC inputs for the address decoder are applied to check the static level performance with the proper settings for the 3-bit bus. The differential measurement results at duplexer output are summarized in Table 4-9. The level 6 is ~ 3.5 dBm, which is lower than the individual PA measurement result. This is probably due to the fact that input power is lower than expected at the input of first pre-amplifier. The similar results are observed in the PA standalone measurement if smaller input power is applied. The lower power and level ratio errors can be corrected by changing the attenuator sizes and re-tuning the interface at the mixer output and first pre-amplifier stage.

When the transmitter successfully operates with the digital coder, multi-level signals can be generated at the duplexer output. The measurement setup for the time domain measurement is the same as the one mentioned in Figure 4-28. The spectrum analyzer are used for the frequency domain measurements. Once again, in order to monitor the time domain multilevel signals, the on-chip built-in divide-by-32 block generates low frequency triggering signals (525 MHz).

Table 4-9. TX static measurement results at the duplexer output (cable and external balun loss are 4 dB).

	Power (using S.A.) (dBm)	Add back ~ 4 dB (dBm)	V_{peak} (mV)
L0	-39.5	-35.5	5.3
L1	-13.5	-9.5	105.9
L2	-12.0	-9.0	112.2
L3	-11.0	-7.0	141.3
L4	-9.5	-5.5	167.9
L5	-7.0	-3.0	223.9
L6	-0.5	3.5	473.2

Ideal ratio		Measured ratio results	Error (%)
Level 2 / Level 1	$\sqrt{2}$	4.47	OFF
Level 3 / Level 1	$\sqrt{3}$	2.11	-5.6
Level 4 / Level 1	$\sqrt{4}$	1.59	-20.5
Level 5 / Level 1	$\sqrt{5}$	1.33	-23.2
Level 6 / Level 1	$\sqrt{6}$	1.06	-25.0

Incidentally, for proper triggering, a periodic waveform is needed. Constant inputs to the digital coder are applied and XNORed with the output from the Walsh Code generator. Therefore, a periodic multi-level waveform is generated at the transmitter output. Figure 4-37(a) shows the differential time domain measurement results when the digital coder inputs are 111111. This corresponds to the dynamic output, 62333322. The output is AC-coupled. The waveform shown in Figure 4-37(a) is symmetrical with respect to the time axis. Although, there are lots of harmonics as described in Figure 4-35, the proper multi-level signal can still be triggered using the on-chip generated triggering signal. Each level has a 2.5-ns data period with 16.8-GHz carrier. The diode detection receiver will pick up the negative portion of waveforms and the 400-Mbps data will be fed into an ADC for de-modulating. The corresponding output spectrum for the same case (constant coder inputs = 111111) is shown in Figure 4-37(b). There are lots of harmonics with modulating data coming with every harmonic peak, which can be clearly seen in the output spectrum. From the measurements, the spreading effect is clearly observed. In the plot, the average power is captured.

Different coder inputs are also applied. Figure 4-38(a)-(b) shows the time domain and frequency domain measurements when the digital coder inputs are 000001. This corresponds to the dynamic output, 13424253. Figure 4-39(a)-(b) shows the time domain and frequency domain measurements when the digital coder inputs are 111000. This corresponds to the dynamic output, 33440433. For all the dynamic measurements, the clock frequency of the digital coder is 400 MHz, which is the original specification. The coder is fully functional and can be operated at the full rate.

All the 7 levels can be recognized in Figure 4-37, 4-38, and 4-39. Especially, the level 0 is close to zero as expected. That means the self oscillation of the last PA stage can be effectively

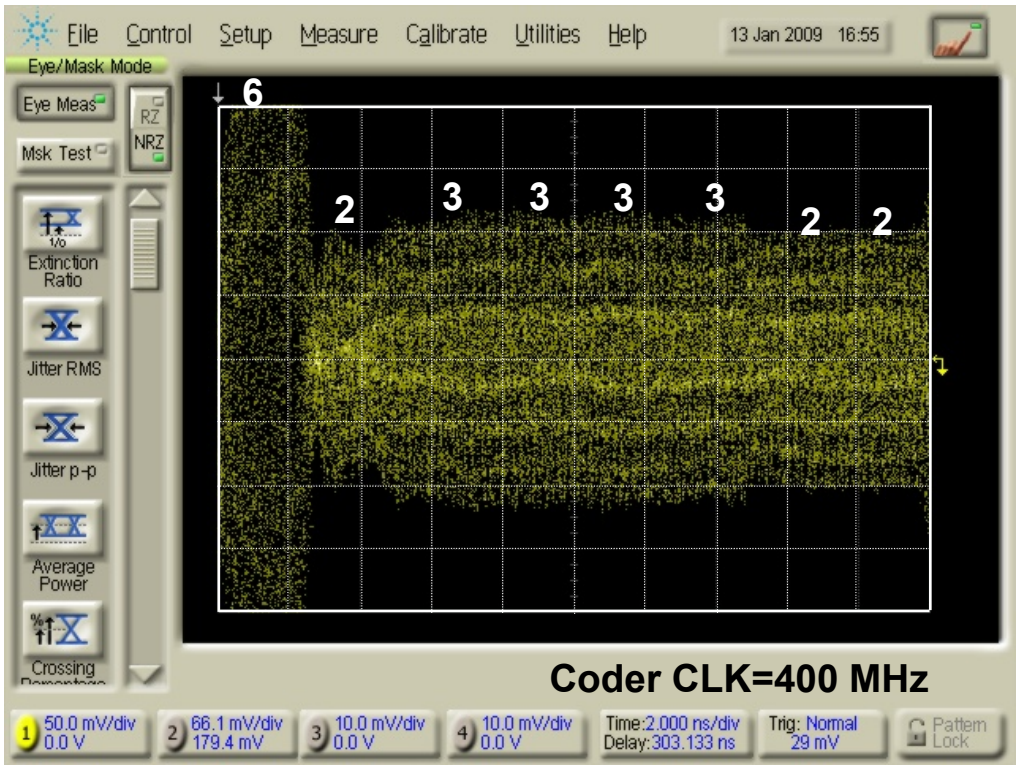


Figure 4-37(a). Time domain measurement when the digital coder inputs are 111111, which corresponds to the dynamic output, 62333322.

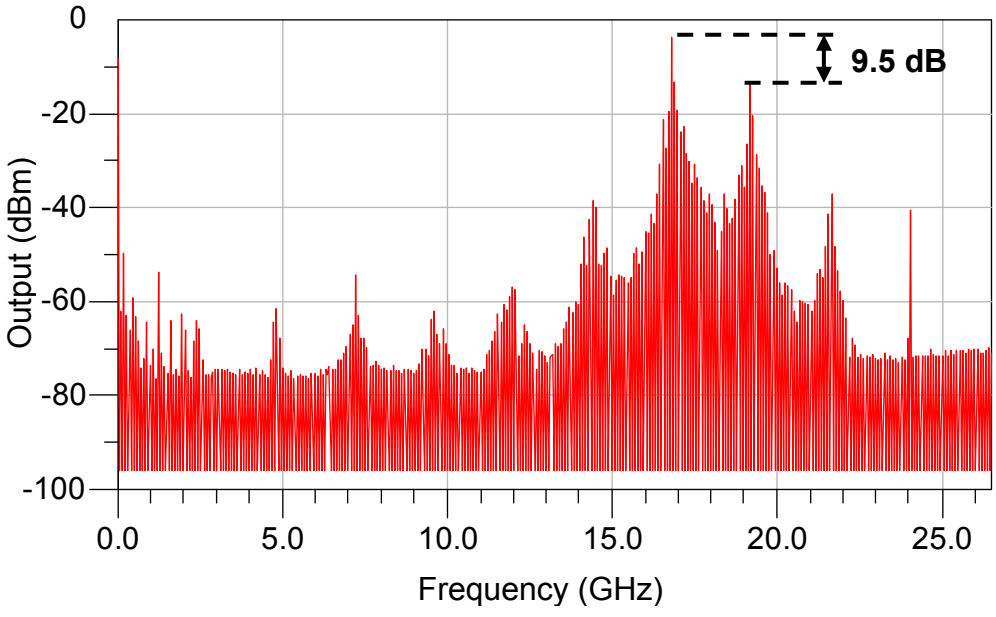


Figure 4-37(b). Frequency domain measurement when the digital coder inputs are 111111, which corresponds to the dynamic output, 62333322.

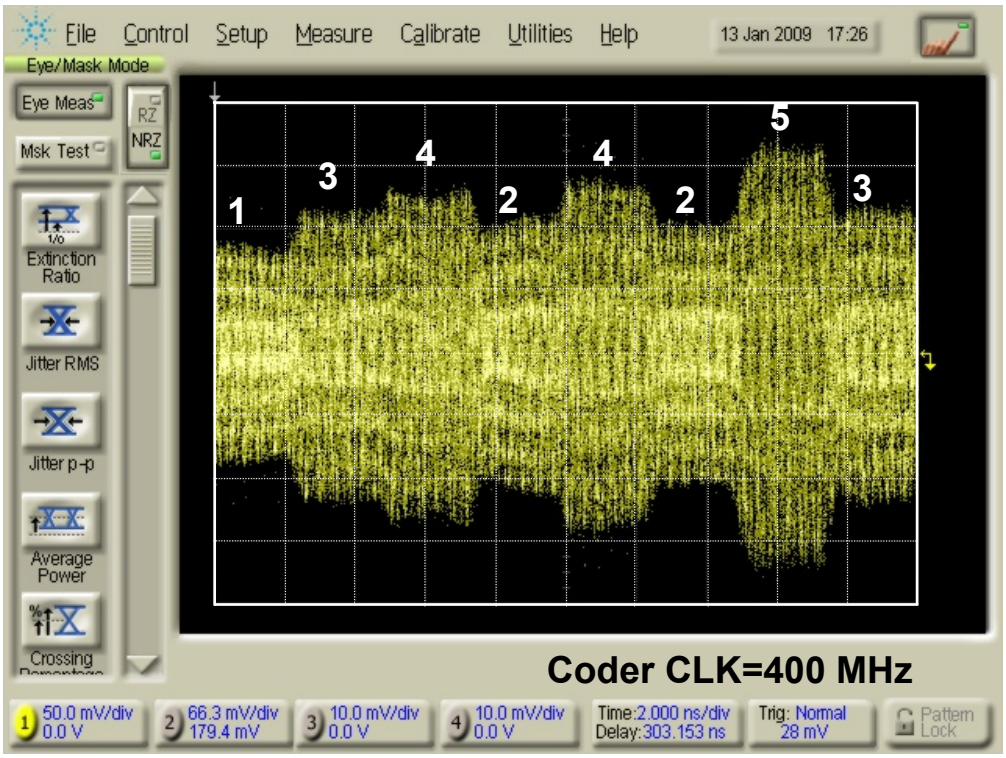


Figure 4-38(a). Time domain measurement when the digital coder inputs are 000001, which corresponds to the dynamic output, 13424253.

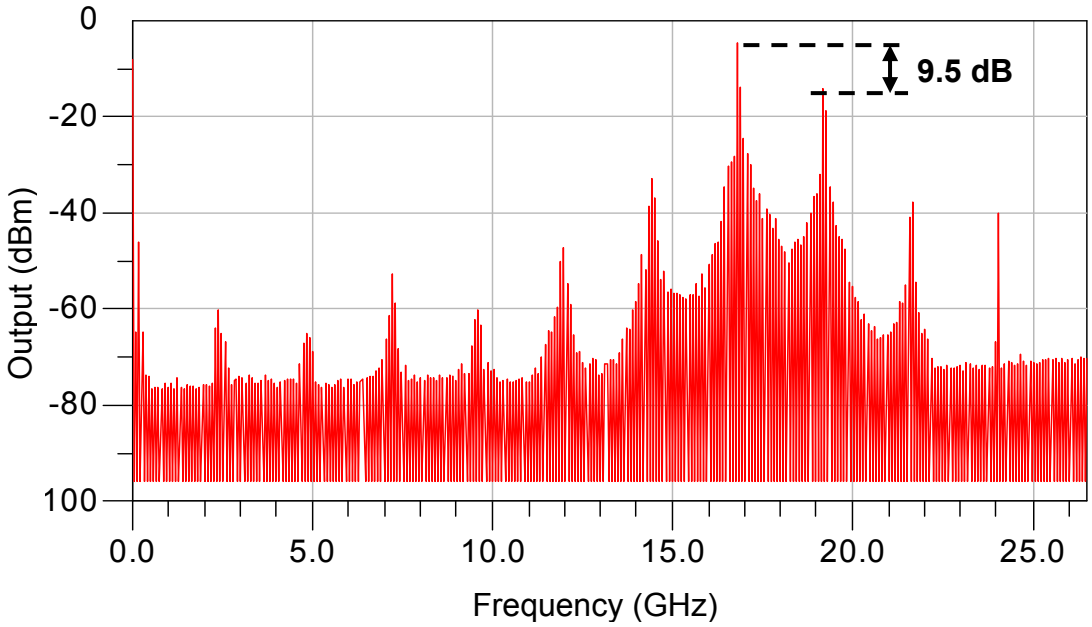


Figure 4-38(b). Frequency domain measurement when the digital coder inputs are 000001, which corresponds to the dynamic output, 13424253.

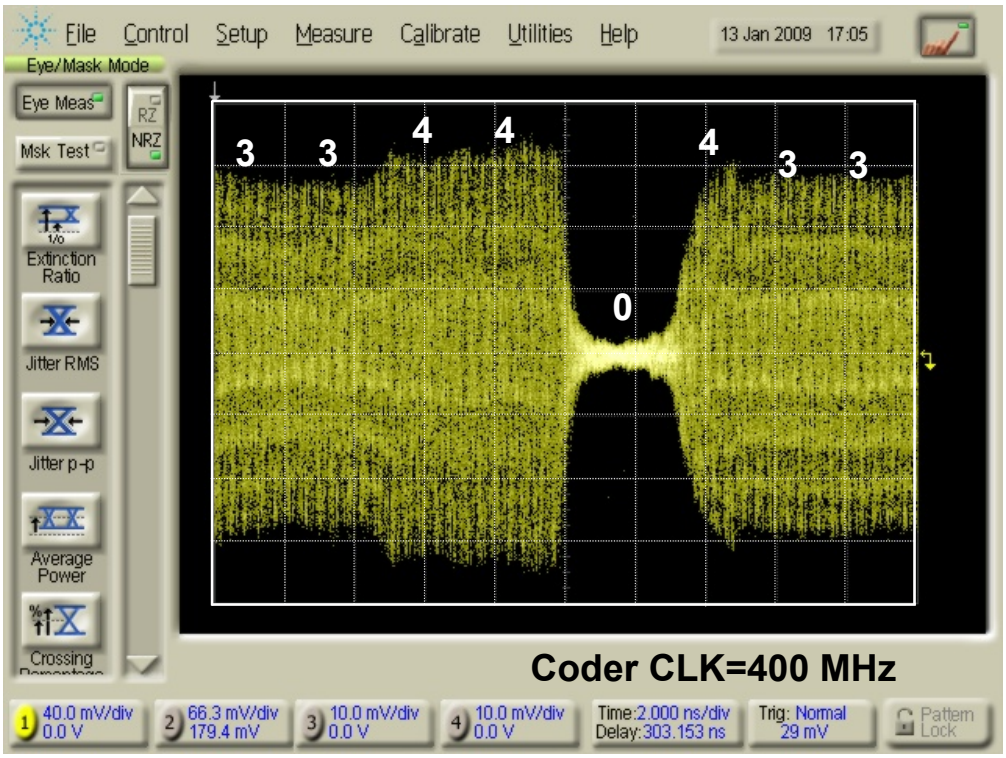


Figure 4-39(a). Time domain measurement when the digital coder inputs are 111000, which corresponds to the dynamic output, 3344043.

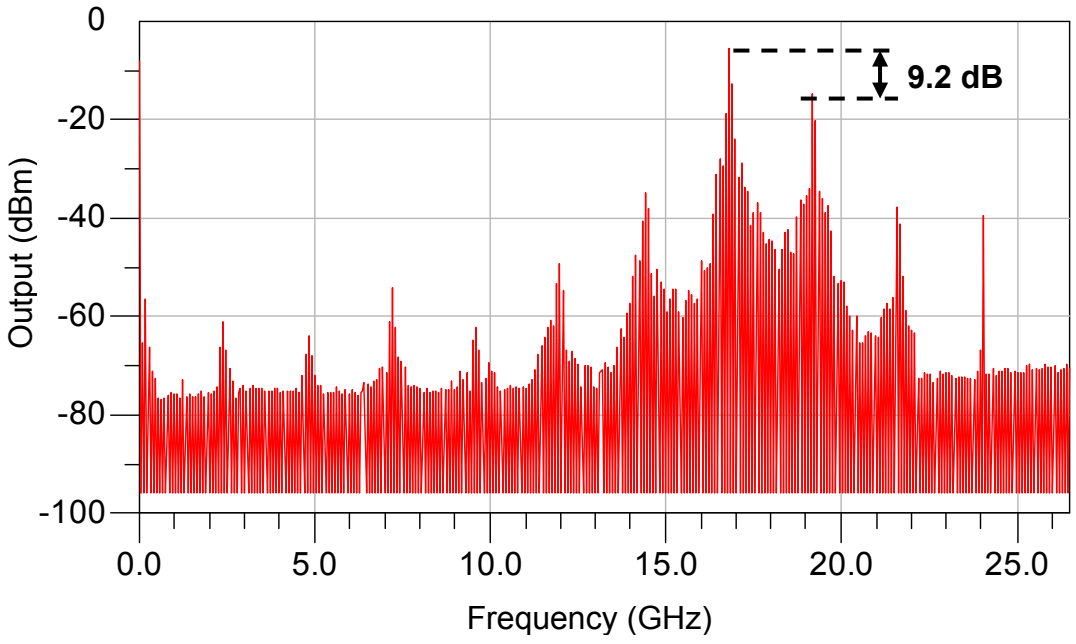


Figure 4-39(b). Frequency domain measurement when the digital coder inputs are 111000, which corresponds to the dynamic output, 3344043.

Table 4-10. Power consumption of TX blocks.

Component	Power Consumption	Performance
PLL	26.75 mW	Generating 24 GHz signal. Locking range: 23.5 – 24.5 GHz (digital tuning bits – 111) At 50-kHz, phase noise is -76.75 dBc/Hz. At 1-MHz, phase noise is -93.55 dBc/Hz. At 10-MHz, phase noise is -114.03 dBc/Hz.
Mixer	6.03 mW	Working fine.
LO buffer	13.81 mW	Working fine.
PLL output buffer + Divider chain (outside PLL) + Multiply-by-2 + IF buffer	56.41 mW	Working fine except PLL output buffer has to be re-tuned to provide bigger drivability for the following divide-by-2 block.
Pre-drivers (differential)	64.24 mW	At PA output, it can successfully generate 7 multi-level signals when coder clock is 400 MHz.
PA (differential)	29.64 mW	
Coder	1 mW	Working fine.
Total Power Consumption	197.88 mW	

suppressed. The CDMA TX chain can support 7 signal levels with a 16.8-GHz carrier and at 400-Mbps data rate. It occupies ~ 5.2 mm^2 and consumes 198 mW. Table 4-10 summarizes the power consumption of every block. Small modifications are needed to improve the TX chain overall performance. First, the PLL output buffers have to be re-tuned. Second, the interface between the mixer output and the input of first pre-amplifier has to be re-tuned. Finally, attenuator sizes need to be re-sized. Higher output power is expected after decreasing the attenuator sizes.

4.5 Summary

In this chapter, “wireless interconnects” concept is described. The simulation and measurement results of TX chain are presented. The CMOS PA with a digital coder can be used to implement multi-level ASK modulation at 400 Mbps . The PLL can successfully generate a 24-GHz carrier with reasonable phase noise performance. The reference 24-GHz signal from the PLL is divided down to 12 GHz and 4.8 GHz and up-converted to generate the 16.8-GHz carrier.

The measurement results of the single-ended PA indicate that it is feasible to provide sufficient linear power at 16.8 GHz. By using the linear portion of the class E PA, higher efficiency and lower power consumption can be achieved. The duplexer achieves ~ 3-dB insertion loss at 16.8 GHz, which already satisfies the specification. The return loss of PA port and antenna port are below 10 dB within the desired band (from 15.6 GHz to 18 GHz). The rejection between LNA and PA ports is ~ 23 dB at ~ 16.8 GHz and 25.6 GHz, which is smaller than the 30-dB target but should be still acceptable. The CDMA TX chain is fully functional except the drivability issue at the interface between the PLL output and divide-by-2 block. It can support 7 signal levels with a 16.8-GHz carrier. Some modifications are needed to improve the TX chain overall performance in a future tapeout.

CHAPTER 5
BOND WIRE ANTENNA DESIGN

5.1 Introduction

The demand for ever increasing functionality of IC's has been met by reducing the sizes of electronic devices and interconnections between them [70]. By having smaller and more advanced devices, circuits operating at higher frequencies can be realized. However, it requires corresponding improved technology for packaging. More and more off-chip connections are needed to satisfy the increased demand for functionality [71], which makes the chip-on-board (COB) package for IC's more challenging. But COB package is still a preferred choice due to its robustness and low cost. It also better tolerates die thermal expansion and placement uncertainty [72].

Lots of efforts have been made to predict and analyze inductance of bond wires [73]-[75]. The parasitic inductance of bond wires is likely to affect circuit tuning network and significantly affect overall circuit performance. Therefore, other advanced packaging techniques, such as BGA and Flip Chip, are being used [76], [77]. However, in terms of the cost point of view, packages using bond wires are still the cheapest. This is the motivation for developing other possible ways to achieve low cost, reasonable performance and mitigate parasitic effects. As discussed in Chapter 1, at millimeter wave frequencies, typical bond wire lengths approach a wavelength and a bond wire is expected to be a reasonable radiator, which could be used for inter-chip data communications. Figure 5-1 shows a cross-section of a Multi-Chip Module (MCM) package. It shows 2 chips mounted on the same substrate and both having bond wire connections to a PCB. Use of bond wire antennas for wireless inter-chip data communications or general purpose wireless communications may be possible.

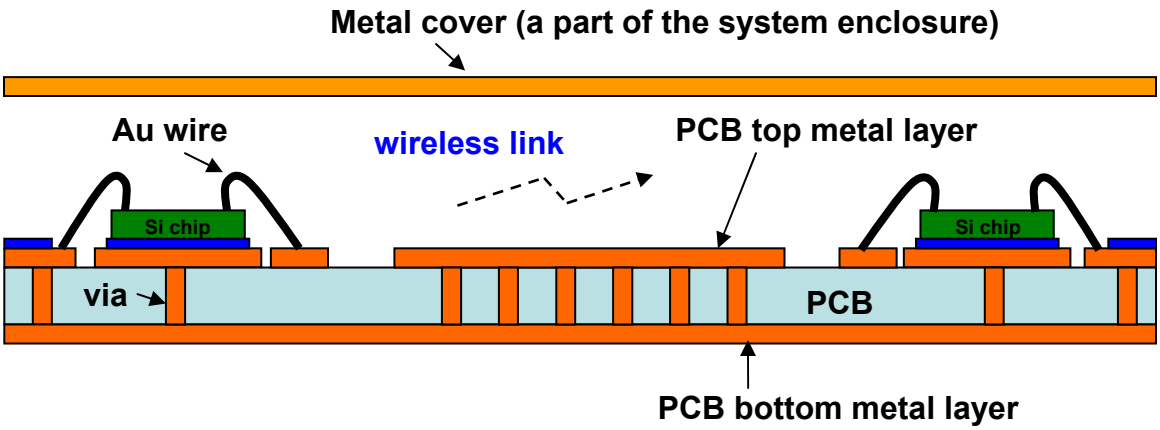


Figure 5-1. Multi-Chip Module package cross-sectional view.

As discussed in Chapter 3, the propagation medium is a parallel-plate waveguide, which is formed by the top metal layer of PCB and an aluminum metal cover which represents a part of an electronic system enclosure. Although on-chip dipole antennas have been extensively studied [5]-[7] in various environment, the radiation performance should be re-evaluated in this parallel-plate waveguide system. The other choice is to use slot antennas, which can also be fabricated on chip. But both of them as shown in Figure 5-2 ideally have E-field on the x-y plane and have weak vertical E-field [78], which is not optimal for use in a narrow-gap parallel-plate waveguide. Therefore, a bond wire acting like a monopole may be better because of higher vertical E-field.

A bus interconnected with wireless links, in which multiple sets of devices/chips on a PCB can simultaneously communicate and control signals can be broadcasted to multiple devices is proposed. The 60-GHz ISM band is a good choice because of its large available bandwidth, which is beneficial for high data rate communication at multi-giga bits per second (Gbps). Frequency division multiple access (FDMA) can be used to replace multiple I/O's by a transmitter or a receiver with one antenna. As shown in Figure 5-3, this should lead to area reduction and lower cost.

This chapter shows that when the bond wire length is properly (~1mm) chosen, it should be well suited for implementing antennas operating around 60 GHz. In fact, the measurements

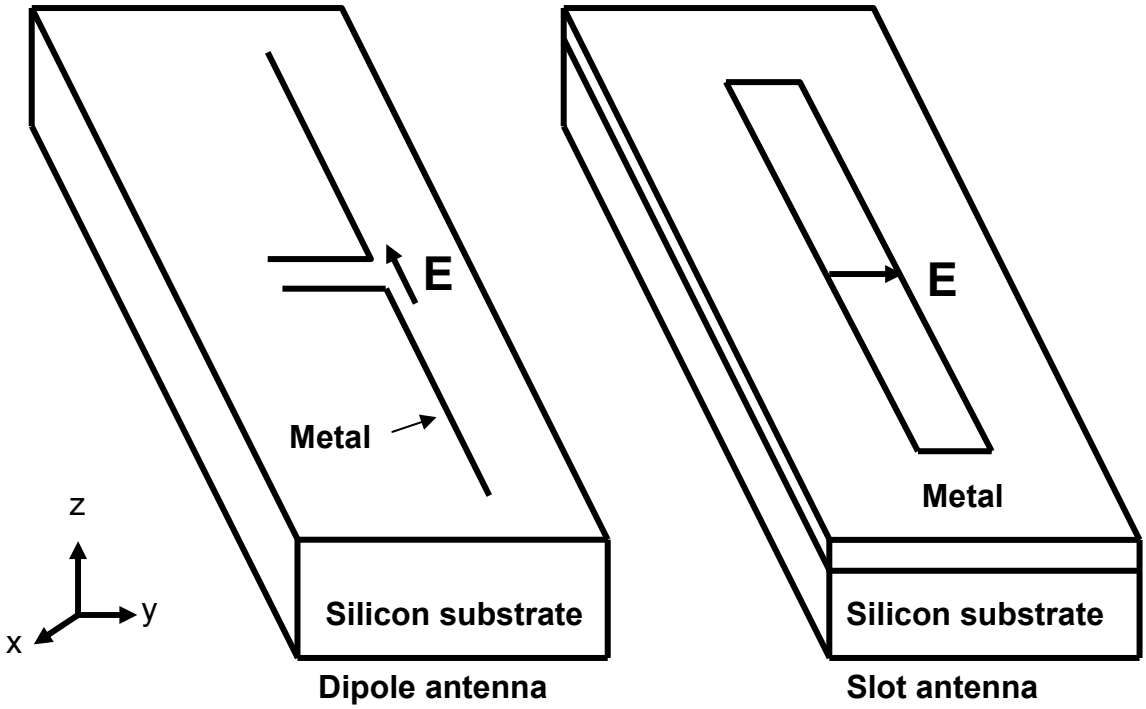


Figure 5-2. On-chip dipole antenna vs. slot antenna. The E-fields are both on x-y plane.

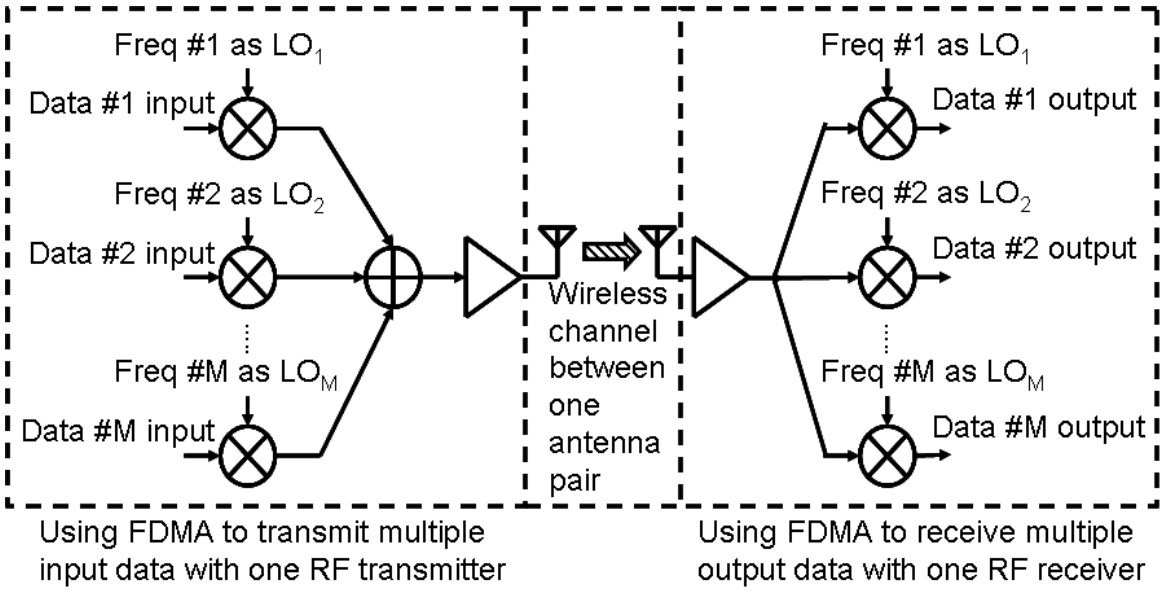


Figure 5-3. Frequency division multiple access (FDMA) is used to replace M I/O's by a transmitter or a receiver with one antenna to lower the I/O pin count.

show that bond wire antennas in the presence of a metal cover (2-mm gap to the PCB) should be sufficient for building a 1-Gbps radio link operating near 60 GHz with BER (Bit error rate) of 10^{-12} and 10-cm range. A potential problem with bond wire antennas is the length variation (~

+/– 50 μm) during manufacture, which causes match and efficiency to vary. The impact of this is bounded. The details of measurement setup and measurement results as well as discussion are presented in sections 5.2 and 5.3.

5.2 Measurement Setup, Test chips, and Test Boards

As shown in Figure 5-4, an antenna consists of a bond wire, a bond pad on a chip, and a bond pad on a PCB. The bond pads anchor a bond wire. The location of bond pad is a key factor determining the length of bond wire; hence, the characteristics of bond wire antennas. At 60 GHz, a wavelength (λ) is 5 mm in free space. The target bond wire length of 720 μm is only 0.144λ, and the antenna is expected to behave like a short monopole, which ideally has 4.77-dBi directivity [78].

The parasitic capacitance and resistance associated with the bond pads also are critical factors determining the matching and resonant behavior of antennas. In order to increase the distance between the top metal layer and on-chip ground shield, thus lowering the parasitic capacitance of bond pad, a ground shield is formed with the polysilicon layer instead of the metal 1 layer. The separation between the top metal layer and polysilicon ground shield is 3.5 μm. On the PCB side, the distance between the top and bottom metal layers is ~ 500 μm. Therefore, the parasitic capacitance of bond pad in PCB is ~ 80X smaller than that of an on-chip bond pad. These as mentioned make the antenna behave like a monopole.

The measurement setup in Figure 5-5 includes a signal generator, cable connections, GSG and GS probes, a harmonic mixer (50-75 GHz), a high power amplifier (55-65 GHz), and a spectrum analyzer [76]. The mixer, power amplifier, and spectrum analyzer can be replaced with a network analyzer for 2-port S-parameter measurements. Using these, antenna pair gain, G_a defined in Eq. (3-1) is measured. The antenna pair gain accounts for the input impedance

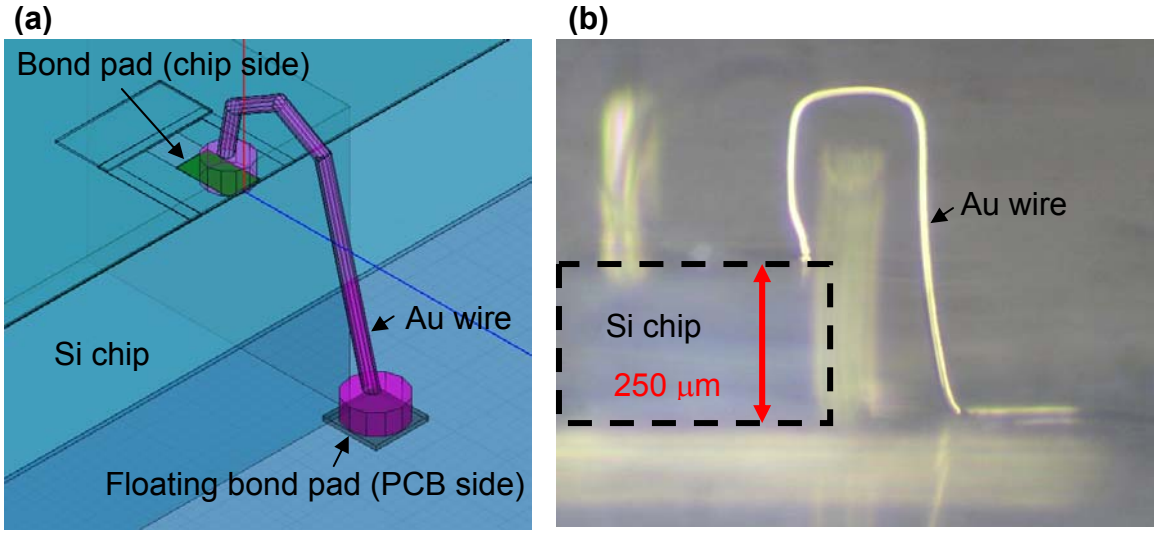


Figure 5-4. (a) Gold bond wire co-designs with an on-chip bond pad and a floating bond pad on the PCB. (b) Photograph showing the side view of the silicon chip and a gold bond wire. The estimated bond wire length is around 870 μm.

mismatch, gain of individual antenna and propagation loss.

Three types of test structures have been fabricated for the antenna pair gain measurement, antenna pattern measurement, and studying the effects of adjacent bond wires on antenna performance. Figure 5-6(a) shows a bond wire antenna test structure, a PCB and the corresponding HFSS simulation structure. The separations between transmitting and receiving antennas on the PCB are 1, 2, 4, 8, and 10 cm. The width of a gold-plated plane on the PCB is 1 cm. In order to characterize the bond wire antennas, a chip with 60 x 100 μm^2 pads shown in Figure 5-6(b) is also fabricated. All the test structures are fabricated in the AMI 0.6-μm CMOS process using 0.007-Ω-cm substrates with an 18-Ω-cm epitaxial layer with 3 metal layers. The total dielectric thickness (the top metal layer to substrate) is 3.8 μm.

A ball bond only occupies two-thirds of the bond pad area. The other one-third of bond pad is reserved for landing a high frequency probe, which is critical for good contact and simplification of de-embedding. The target bond wire length is 720 μm (bonded to a ~ 100 x 100

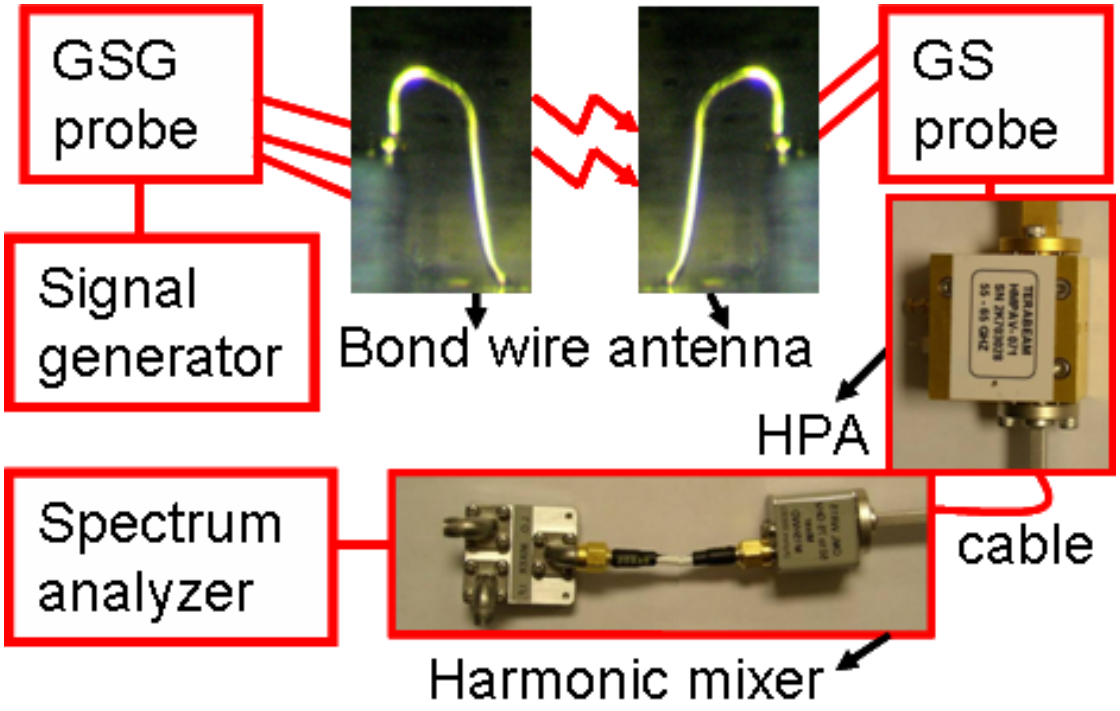


Figure 5-5. Antenna measurement setup. A ball bond only occupies two-third of the bond pad area. GSG and GS probes are landed on the area not occupied by the ball bond. (HPA: High power amplifier)

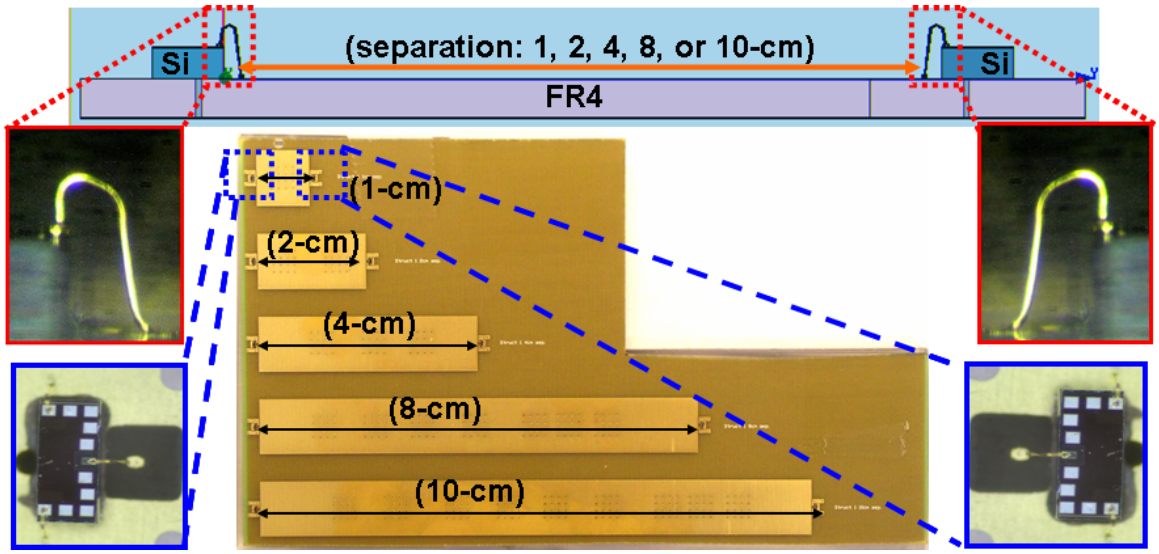


Figure 5-6(a). Side view of a bond wire antenna and photographs of test chip and PCB. The bond wire length is ~ 720 μm. The chip thickness is ~ 250 μm. Each antenna pair has 1-cm wide gold-plated metal trace on the PCB between transmitting and receiving antennas.

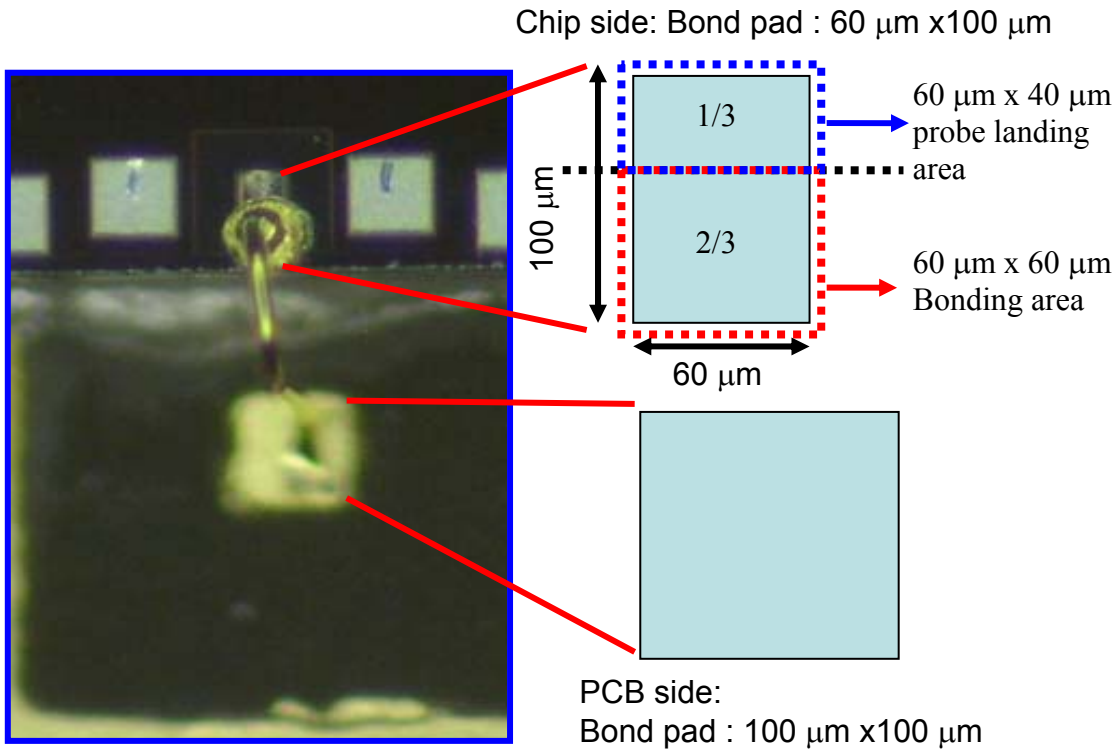


Figure 5-6(b). Bond pad design. Two-thirds of the bond pad area is for ball bonding and one-third is for probe landing.

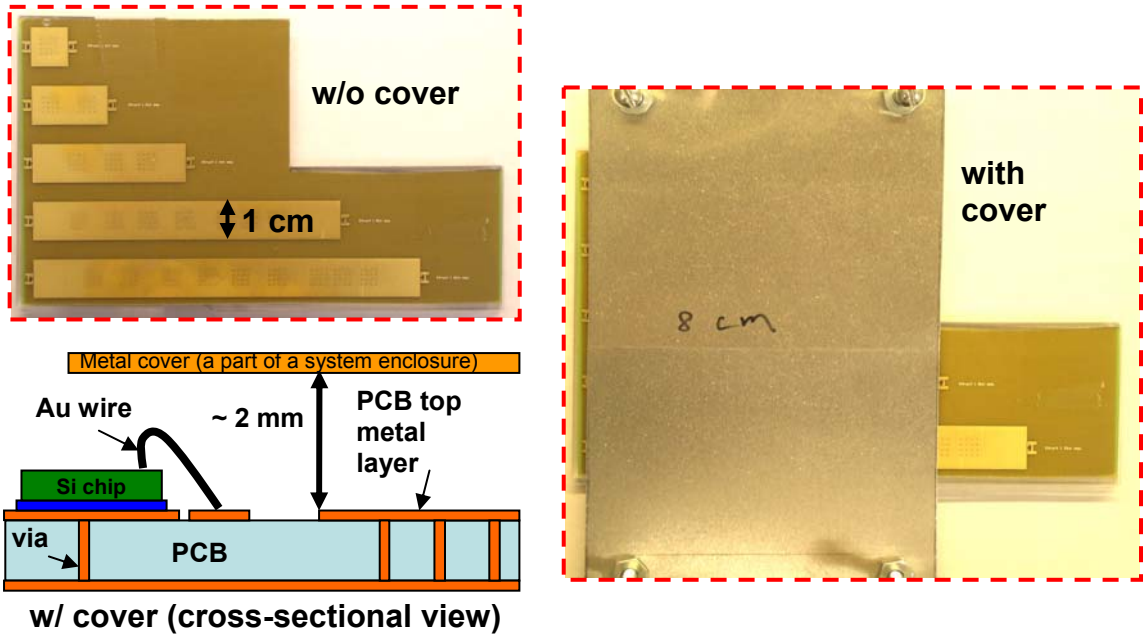


Figure 5-7. Antenna PCB with and without a cover.

μm^2 floating pad on the PCB), which resonates with an on-chip 60 x 100 μm^2 bond pad at ~ 60 GHz. FR4 is used for board fabrication because of its low cost and wide availability. The high frequency wave penetrating into FR4 is a concern because of its loss. However, a large metal ground plane usually present on PCB's mitigates this problem. As mentioned earlier, the thickness of FR4 board is ~ 500 μm. Together with an aluminum metal cover, they form a parallel-plate waveguide channel, shown in Figure 5-7. In real applications, the aluminum metal cover will be replaced by an enclosure for electronic systems. Two bond wires are used to connect the PCB ground and on-chip ground. There is also an option to have more ground bond wires to lower the parasitic inductance.

Figure 5-8(a) shows the PCB for antenna radiation pattern measurement. The board has a 2-cm radius semicircle with 9 measurement points at varying angles. The transmitting bond wire antenna is at the origin of semicircle. In order to reduce the effects from the surrounding environment during the pattern measurements, a mobile setup [79], shown in Figure 5-8(b), was placed in a ~ 7 m x 7 m room instead of using a shielded cage to emulate open space.

Figure 5-9 shows the PCB and chip for studying the effects of adjacent bond wires on antenna performance. The chip is the same as the one used in Figure 5-6. But there are two floating bond wires intentionally designed to sit 300-μm away from the center bond wire antenna. These are intended to emulate close by bond wires that are inevitable. The bond wire may not necessary to be used as an antenna but it may be used for DC supply or ground connections. The structure is used to characterize how floating wires can degrade antenna characteristic. It is critical to quantify this in advance during the step of system design. For instance, higher PA output power will be needed to compensate the loss in the transmitter design. The measurement results are shown in section 5.3.

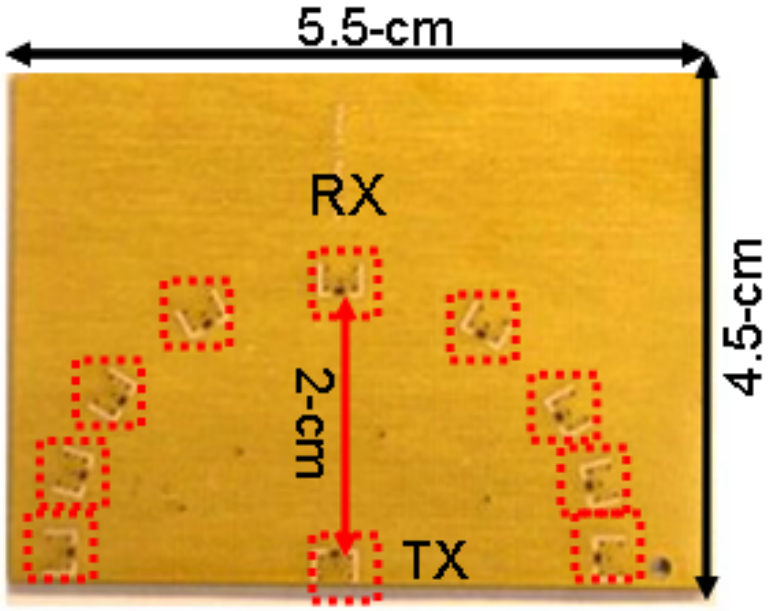


Figure 5-8(a). Test PCB for antenna pattern measurements. It has 9 measurement points on a 2-cm radius semicircle. The transmitting bond wire antenna is at the origin of semicircle.

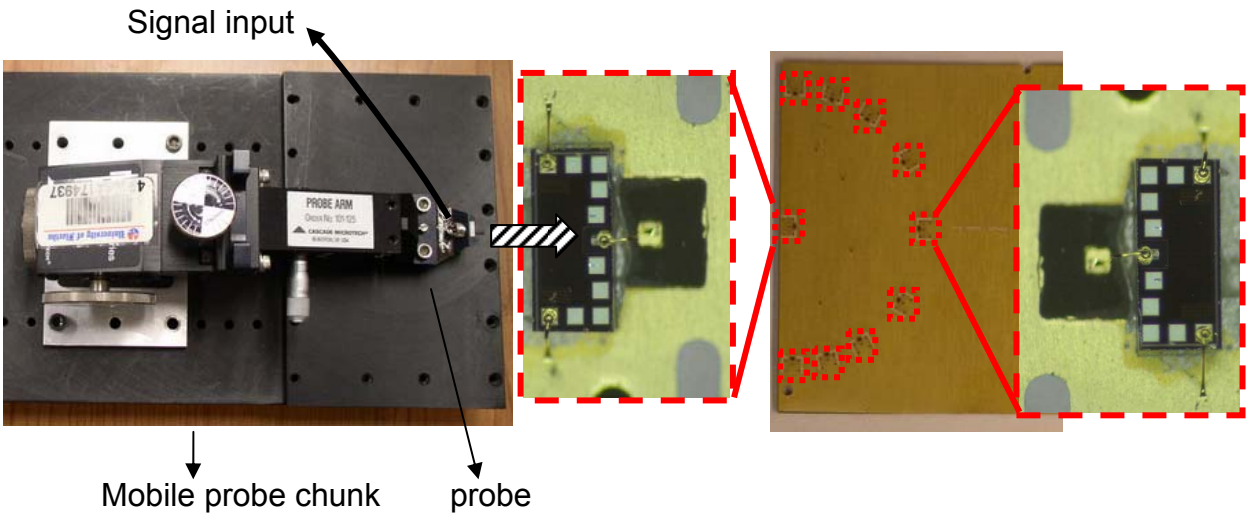


Figure 5-8(b). Mobile setup for antenna pattern measurement.

5.3 Measurement Results and Discussions

Input reflection coefficient, $|S_{11}|$ of bond wire antennas is a critical performance parameter. Figure 5-10 shows that the bond wire antennas resonate at ~ 55 GHz. The tuned

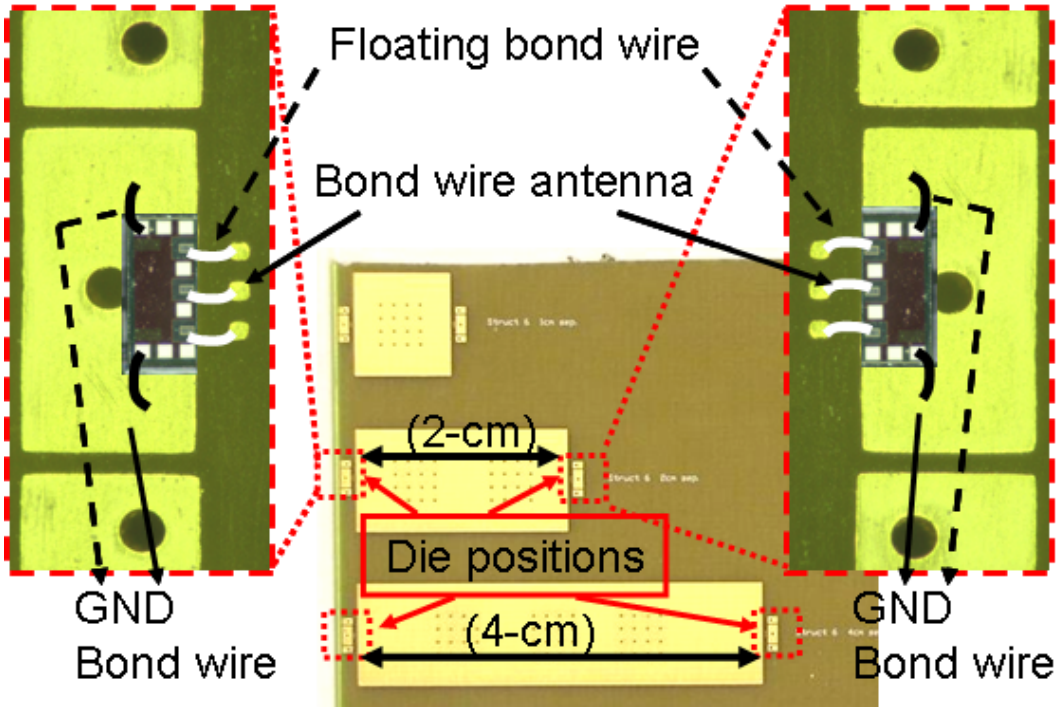


Figure 5-9. Test PCB and chips for bond wire antenna investigation of the effects of adjacent bond wires on antenna performance. There are two floating bond wires adjacent to the antenna. (The separation between the floating bond wire and the bond wire antenna is 300 μm.)

response can be adjusted by controlling the bond wire length. Lengthening tunes down the resonant frequency because of larger inductance. For frequencies between 55 to 64 GHz (~ 9 GHz), $|S_{11}|$ is less than –4 dB. At $|S_{11}|$ of –4 dB, ~ 60 % of incident power is delivered to the antenna for radiation. The corresponding mismatch power loss is ~ 2.2 dB. The tuned response can also be adjusted by varying the bond pad size.

Figure 5-11(a) shows the HFSS simulation results of tuned response shift due to the bond wire length variation of +/- 150 μm around 720 μm. As the bond wire length increases by 150 μm, the tuned frequency lowers to 56 GHz corresponding to that for the measurement results shown in Figure 5-12(a). The bond wire diameter is set to be 16 μm in the simulation. As the bond wire length decreases by 150 μm, the tuned frequency stays around 61 GHz. The bandwidth also becomes broader. This may be due to the fact that the antenna is becoming

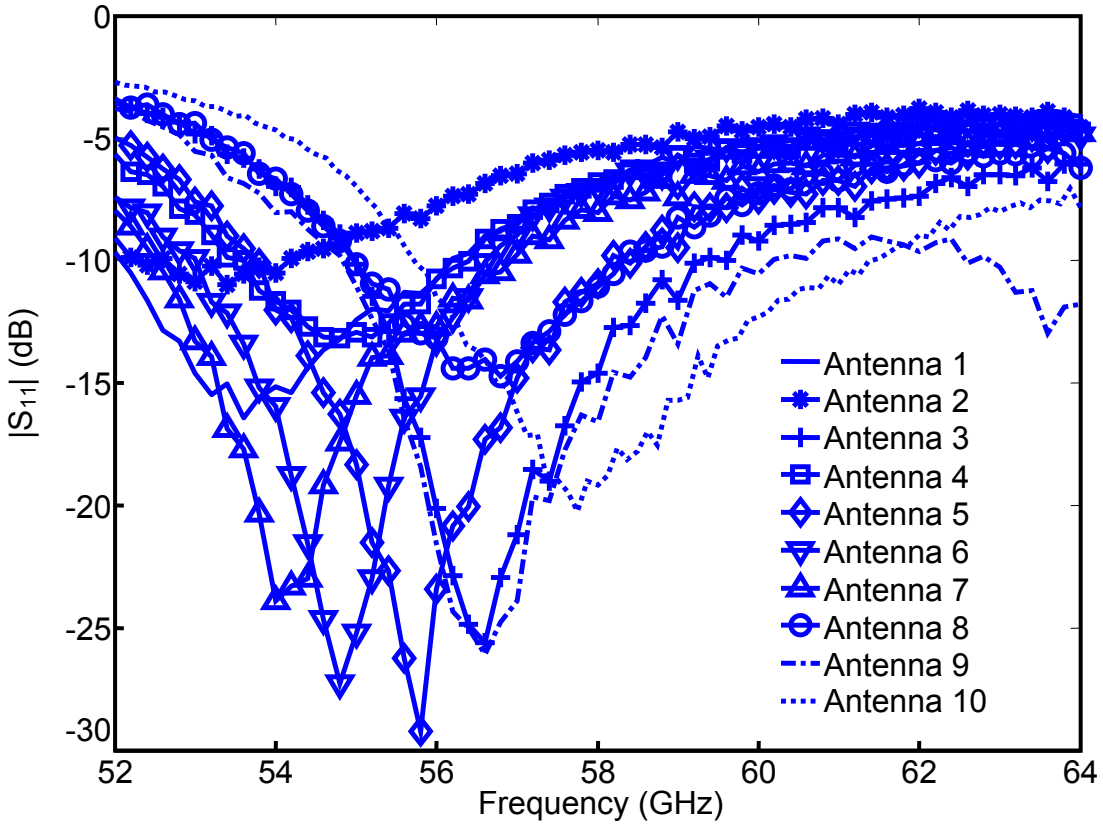


Figure 5-10. $|S_{11}|$ of bond wire antennas.

shorter, and $|S_{11}|$'s move away from the center of smith chart as shown in Figure 5-11(b). The capacitive tuned response implies that the reduced inductance of a shorter bond wire can not completely tune out the pad capacitance. A longer bond wire length and thinner bond wire diameter make the input impedance more inductive in the smith chart as the arrow shown in the plot indicates. In order to match the variation in Figure 5-10, the bond wire length must vary from 720 to 890 μm. This is significantly larger than that specified by the assembly company.

A photograph of side view of a bond wire is shown in Figure 5-4(b). The estimated bond wire length is ~ 870 μm, which is consistent with the 56-GHz resonant frequency. The simulation and measurement results in Figure 5-12(a) have the same resonant frequency. Despite the larger bond wire length variation than the +/- 50 μm specification by the assembly companies,

bond wire antennas could be practical for the use in the 57-64 GHz band applications if the 2.2-dB mismatch loss can be tolerated. When the bond wire length are controlled within +/- 50 μm as specified by the assembly houses, the tuned frequency is expected to be 58-61 GHz as suggested by the simulated plots in Figure 5-12(b). The corresponding mismatch loss is below 0.4 dB. To further reduce the mismatch loss and increase the antenna bandwidth, a varactor may be added in parallel with the on-chip bond pad to adjust the frequency tuning.

Figure 5-13 shows the antenna pair gains (G_a) versus separation at 55 GHz. The loss in the measurement setup is measured using a "thru" structure on a calibration substrate, and is used to de-embed the loss of antenna measurement setup [80]. The figure shows the computed path loss based on the Friis formula [81] and measured antenna pair gain with and without an aluminum cover. The gap between the aluminum cover and PCB was 2 mm. Such a gap is relevant for systems with a form factor similar to that of PCMCIA and some wireless local area network cards. For the case without a cover, G_a of the bond wire antenna pair is around 6 to 8 dB lower than the computed path loss for separations between 1 and 4 cm. This suggests that the gain of bond wire antenna is ~ -3 to -4 dBi. This is especially outstanding considering the fact that the bond pads are fabricated on a low resistivity substrate (0.007-Ω-cm).For the case with a cover, the waves are guided and the loss is lower as expected. At antenna separations greater than 4 cm, G_a for the case with a cover is at least 10 dB higher than that without. At 10 cm separation, G_a for the case with a cover is -41 dB. The Friis formula used in Figure 5-13 is given by

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{\lambda}{4\pi R} \right)^2 \tag{5-1}$$

where $(\lambda / 4\pi R)^2$ is the path loss.

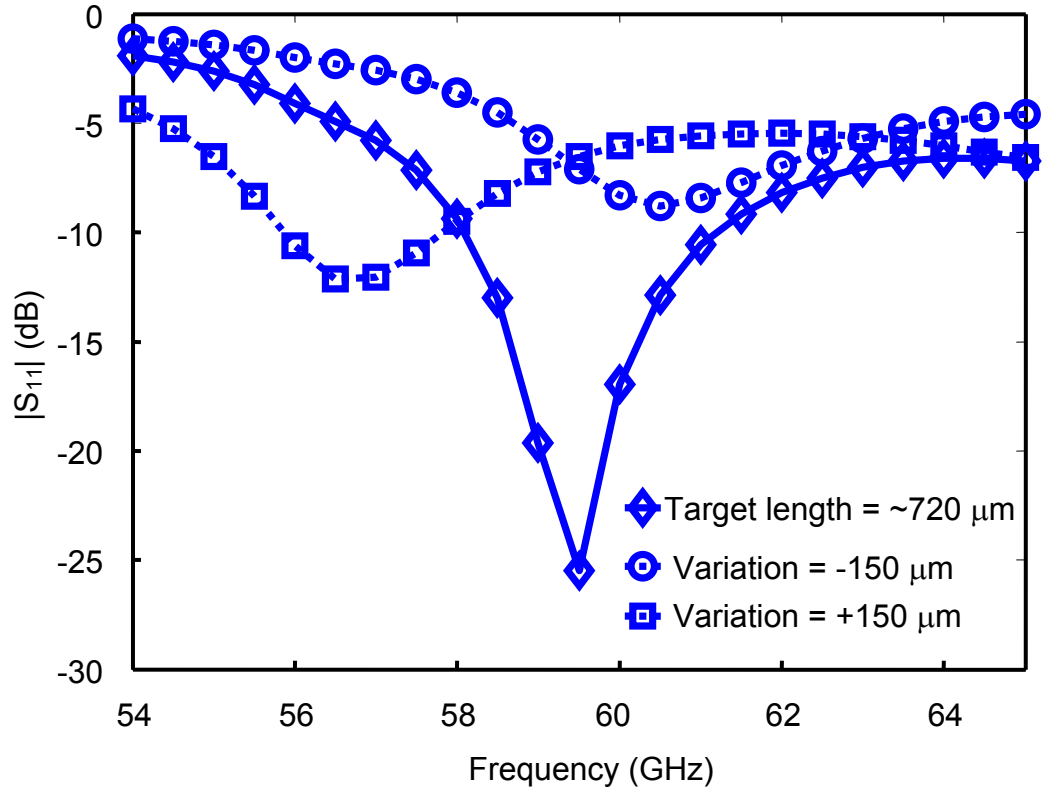


Figure 5-11(a). Simulated $|S_{11}|$ of bond wire antennas with +/- 150-μm length variation (HFSS).

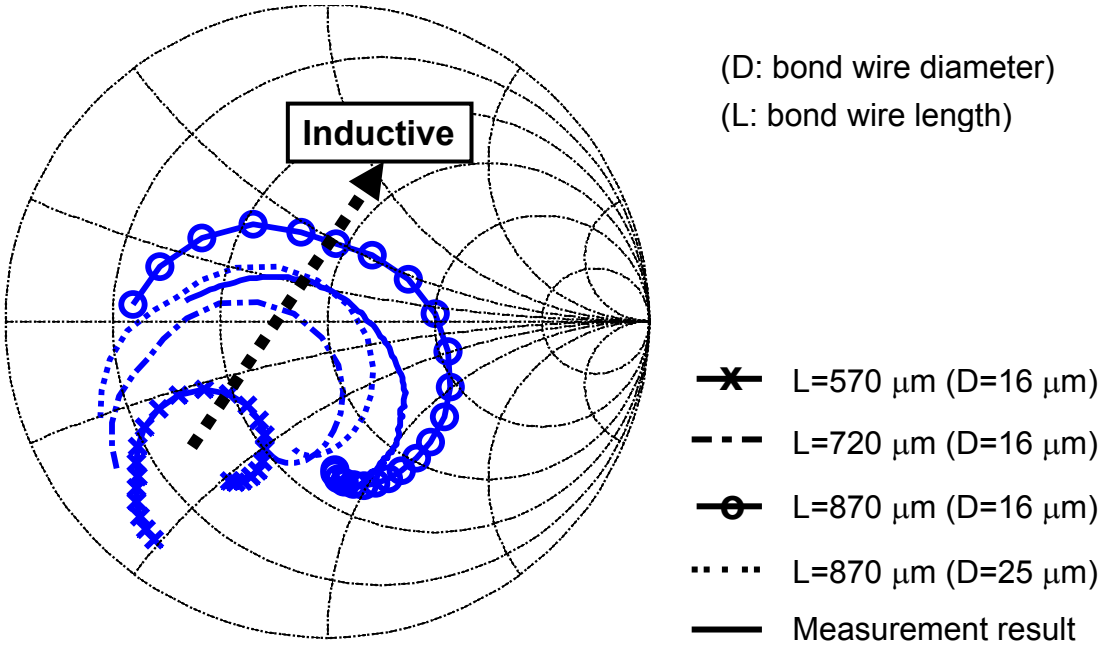


Figure 5-11(b). Simulated $|S_{11}|$ of bond wire antennas with +/- 150-μm length variation (HFSS) in a smith chart. A longer bond wire length and thinner bond wire diameter make the impedance more inductive.

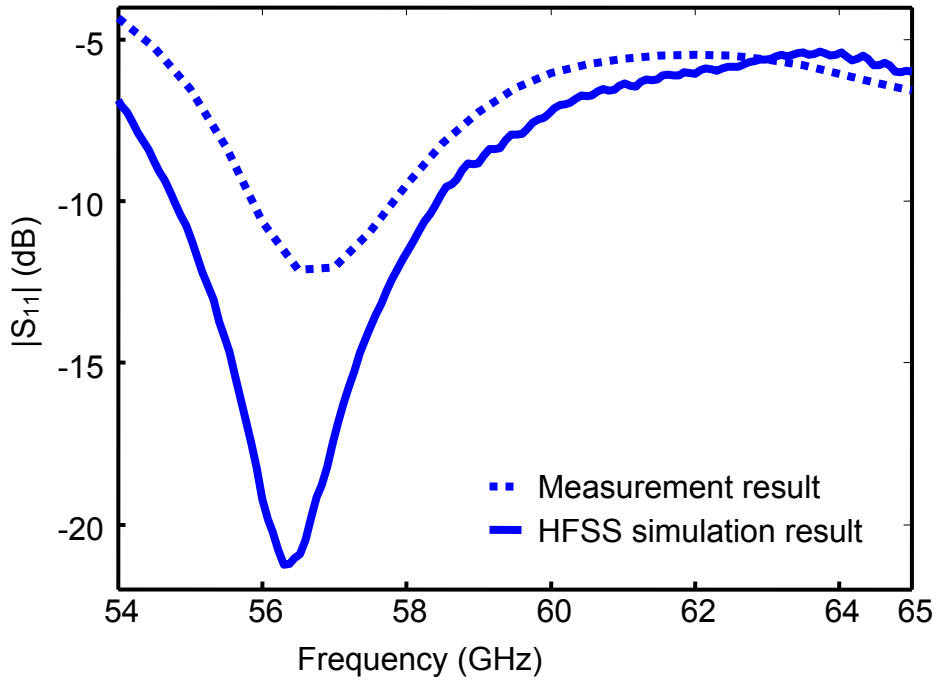


Figure 5-12(a). $|S_{11}|$ of the 870-μm bond wire antenna: HFSS simulated $|S_{11}|$ vs. measurements.

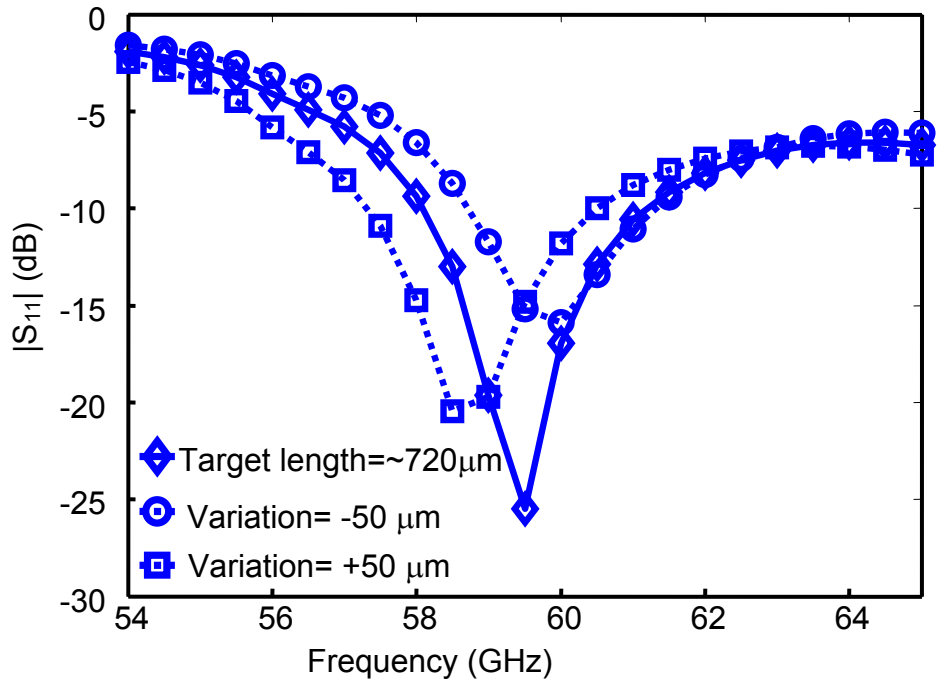


Figure 5-12(b). $|S_{11}|$ of bond wire antennas with +/- 50-μm length variation (HFSS simulation results).

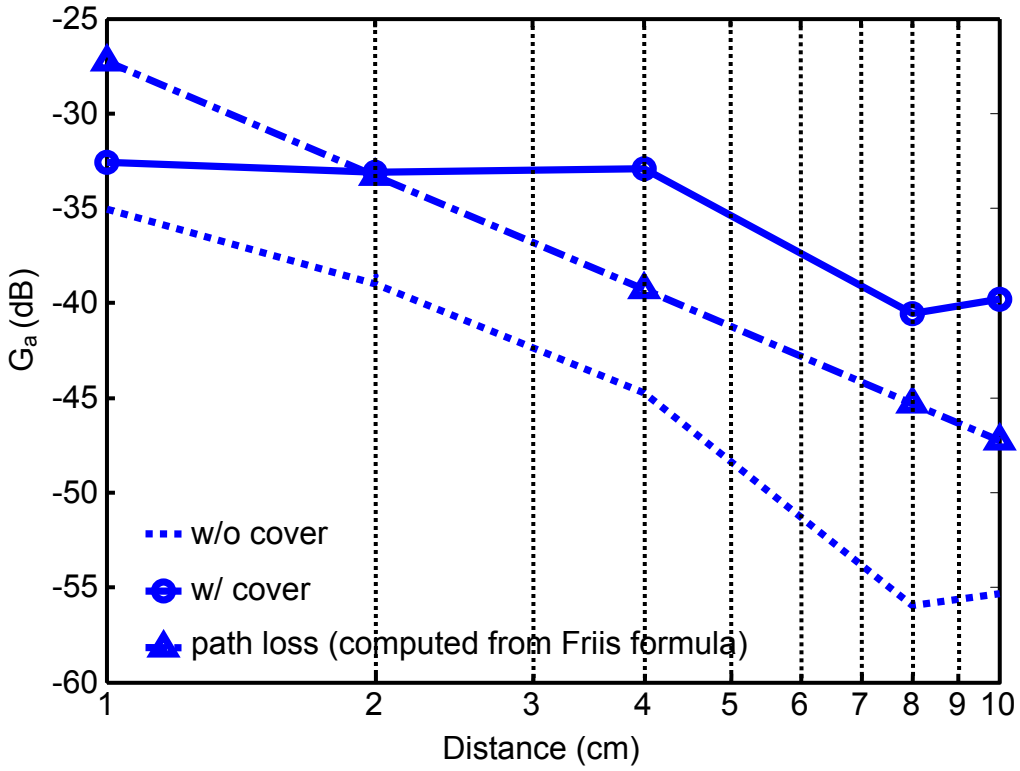


Figure 5-13. Antenna pair gain at 55 GHz, G_a vs. separation (up to 10 cm) plots of with a metal cover, without a metal cover, and calculated path loss from the Friis formula. (cover height: 2 mm from PCB)

The characteristic impedance of the parallel waveguide is

$$Z_0 = \frac{d}{w}\eta \tag{5-2}$$

where d is the gap between the top and bottom plates, w is the plate width, and η is the free space characteristic impedance, 377 Ω [82]. The characteristic impedance of parallel waveguide used in the measurement is ~ 75 Ω, which is close to the 50-Ω input impedance of antenna. If the gap is lowered to 1.33mm, the characteristic impedance of the waveguide can approach ~ 50 Ω. Based on the measurements, the input impedance of bond wire antennas shows similar $|S_{11}|$ characteristics for the case with and without an aluminum cover as shown in Figure 5-14. The solid line (with a metal cover) and dotted line (without a metal cover) almost overlap.

Figure 5-15 shows the HFSS 3-D pattern simulation results for the case of bond wire length = 870 μm at 55 GHz (without a metal cover), which indicates at θ=40 degree, ϕ=60 degree, the bond wire antenna has the highest antenna gain of ~ 0.4 dBi. The effective antenna gain is -3.2 dBi at θ=90 degree, ϕ=90 degree. This is close to the measurement mentioned in the previous paragraph. The radiation pattern without a cover in Figure 5-16 is measured using the PCB in Figure 5-8. The HFSS simulation used the structure shown in Figure 5-4(a), which includes a 720-μm bond wire, an on-chip 60 x 100 μm^2 bond pad, and a 100 x 100 μm^2 floating pad on the PCB (silicon substrate thickness is 250-μm and FR4 PCB thickness is ~ 500 μm).

Between 60 to 120 degrees, the G_a is almost constant and matches well with the HFSS simulations shown in Figure 5-16. The measured pattern shows slight asymmetry. A reason for

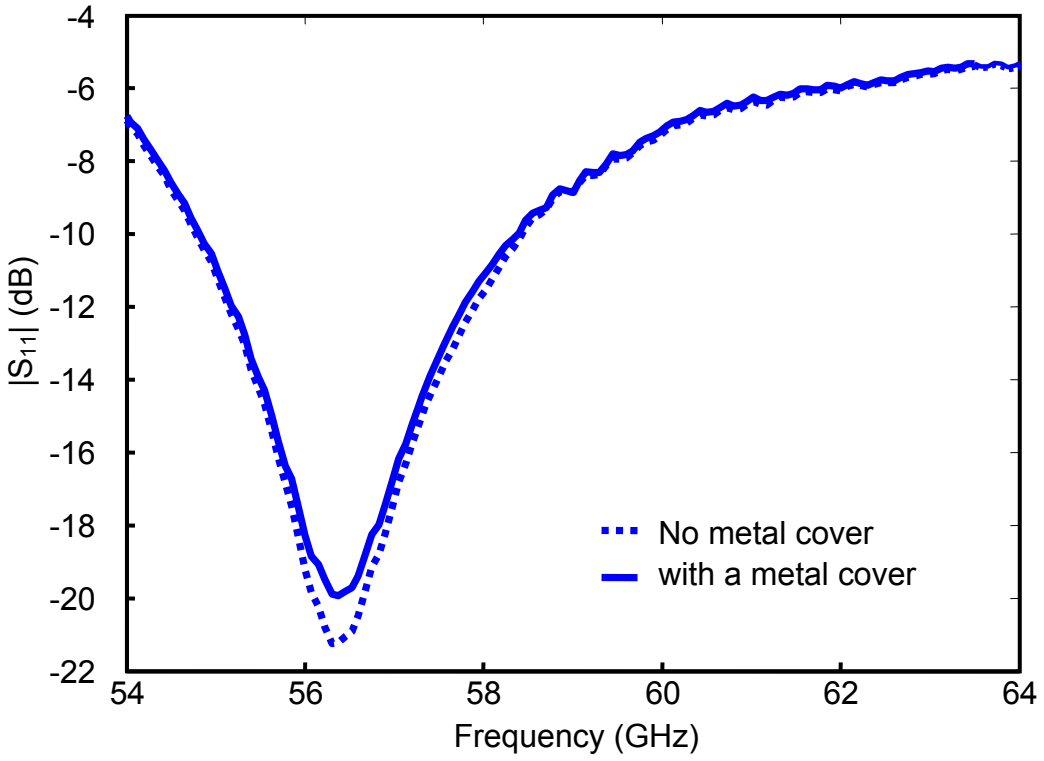


Figure 5-14. Measured $|S_{11}|$ of bond wire antennas for the cases with and without an aluminum cover. (cover height: 2 mm from PCB)

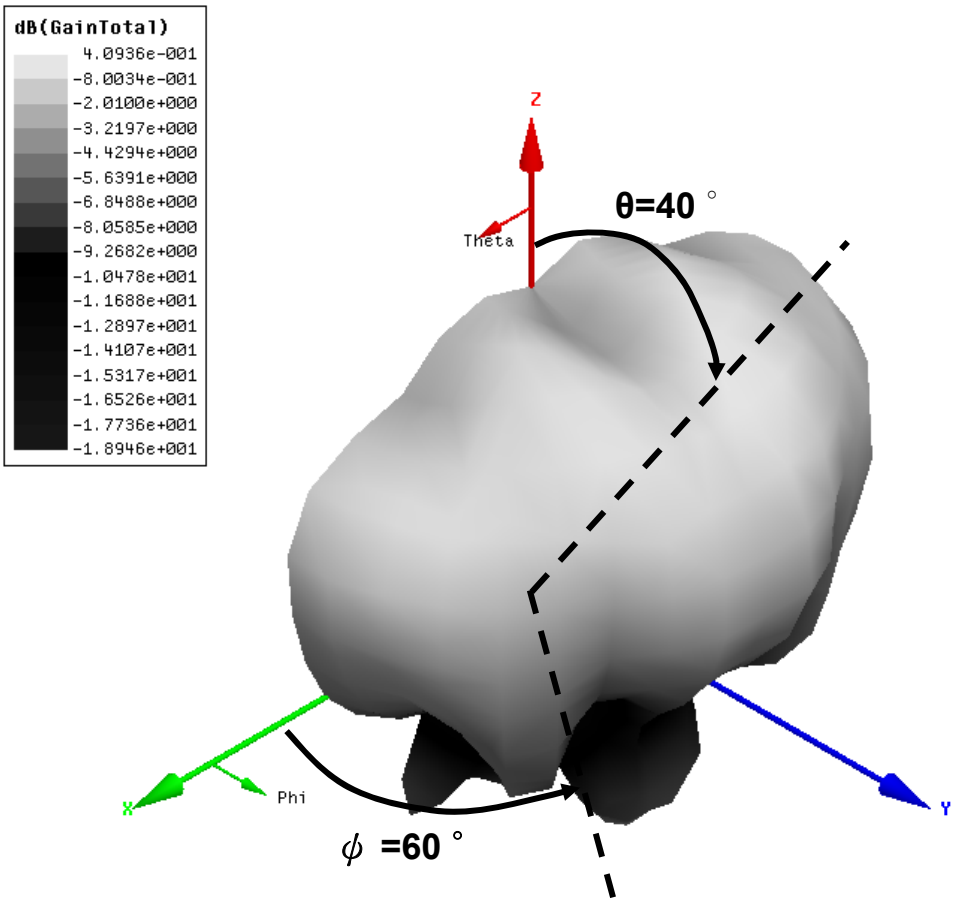


Figure 5-15. HFSS 3-D pattern simulation results when bond wire length = 870 μm at 55 GHz (without a metal cover).

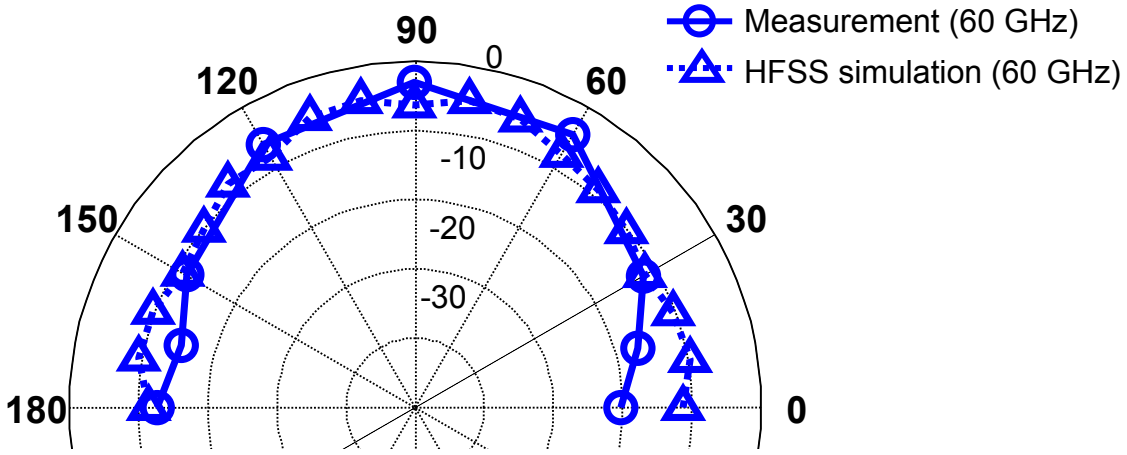


Figure 5-16. Radiation pattern (normalized) of a bond wire antenna measured using the PCB in Figure 5-9. The antenna has better G_a performance between 60° to 120°. (HFSS simulation results when θ=90°, ϕ=0° to 180°)

this may be that the transmitting bond wire antenna is not symmetrically placed with respect to the receiving antenna locations in Figure 5-8(a). In addition, the measured G_a's are 10 to 15 dB lower than that of simulations for angular positions outside the 60 to 120 degree range. This is probably due to the ground bond wires sitting on the sides of center transmitting antenna shown in Figure 5-8(b). The HFSS simulations including these ground bond wires show ~ 5-dB G_a degradation at 0 and 180 degree compared with that at 90 degree, which are in qualitative agreement with the measurements. Despite these, the antenna should still be useful for wireless interconnect applications.

Table 5-1 summarizes the link margin analysis for a 1-Gbps link operating at ~ 60 GHz using a frequency division multiple access (FDMA) scheme with BER of 10^{-12}. When the receiver sensitivity is -60 dBm or receiver noise figure is 10 dB, and the power delivered to the transmitting antenna is 3 dBm, the link margin at 10 cm is 22 dB. The transceiver requirements are modest and the margin is acceptable, which indicate that the measured G_a with a metal cover (2-mm gap) at 10 cm separation of ~ –41 dB is adequate. The bond wires adjacent to an antenna degrade the antenna pair gain (G_a). For instance, two floating bond wires located 300 μm away from the center bond wire antenna degrade the antenna pair gain at 10-cm separation by 12 dB to -53 dB. The measurement results are shown in Figure 5-18. Even if the degradation of G_a is 20 dB, it should be possible to establish a communication link.

Figure 5-17(a) shows the HFSS simulation structure used to study coupling between adjacent bond wire antennas. It includes 2 adjacent bond wires and the separations between them are varied (150, 300, and 600 μm). The dominant mechanism is the near field coupling and the structure can be modeled using circuit elements as shown in Figure 5-17(b). A distributed inductor model is used to represent the bond wire antenna. A coupling coefficient, *k* is the mutual

Table 5-1. Link margin analysis using Frequency Division Multiple Access (FDMA) scheme and direct conversion transceiver architecture.

Wireless I/O Data Path number	3
Data Rate/Data Path (Gbps)	1
Bit Error Rate (BER)	10^{-12}
Multiple Access Scheme	FDMA
Duplex Scheme	TDD
Frequency Channel number	3
Channel Bandwidth (GHz)	2
Channel Spacing (GHz)	3
Carrier Frequencies (GHz)	60, 63, 66
Modulation Scheme	DBPSK
Wireless Channel Length (cm)	10
Antenna pair gain at 10-cm separation (dB)	-41
Noise figure (dB)	10
Receiver Sensitivity (dBm)	-60
Transmitter Output Power (dBm)	3
Link Margin (dB)	22

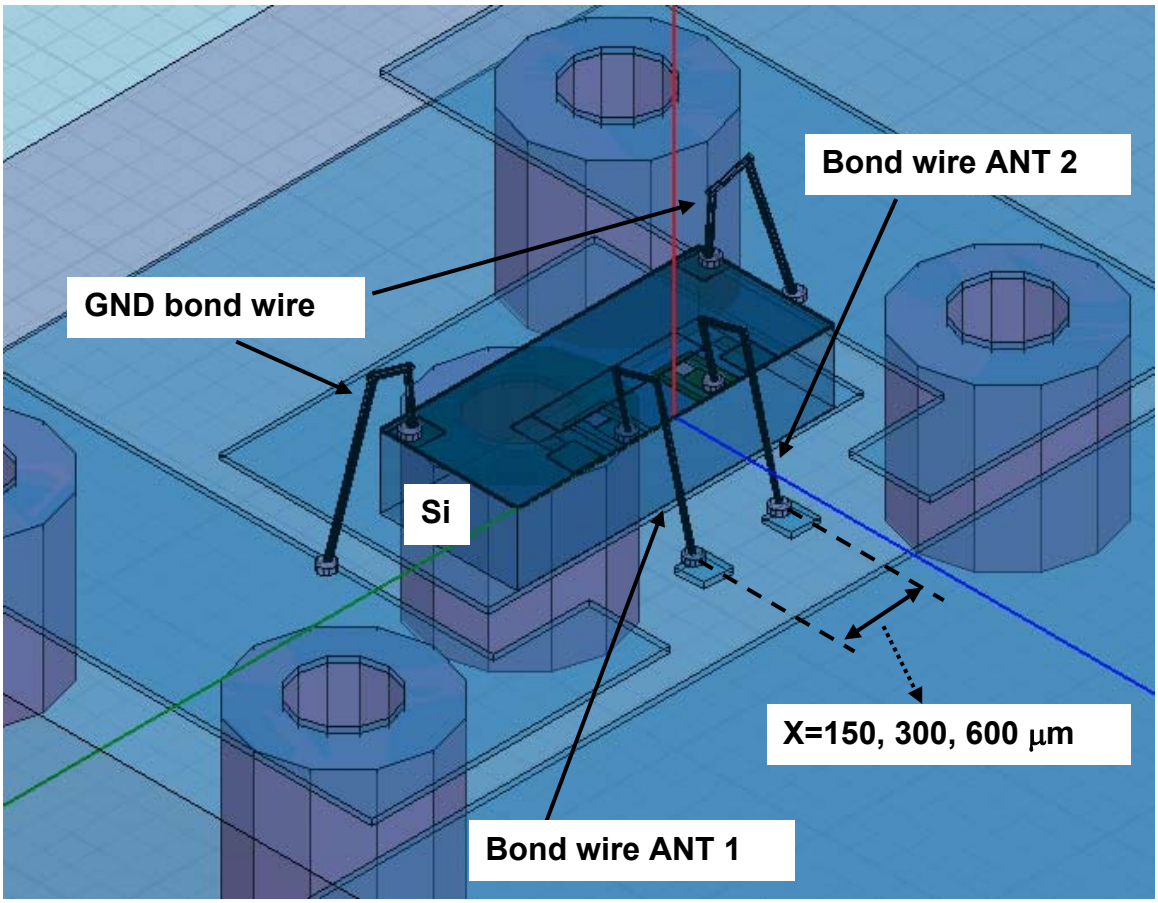


Figure 5-17(a). HFSS simulation structure for a bond wire antenna coupling study. The separations between two bond wires are 150, 300, and 600 μm.

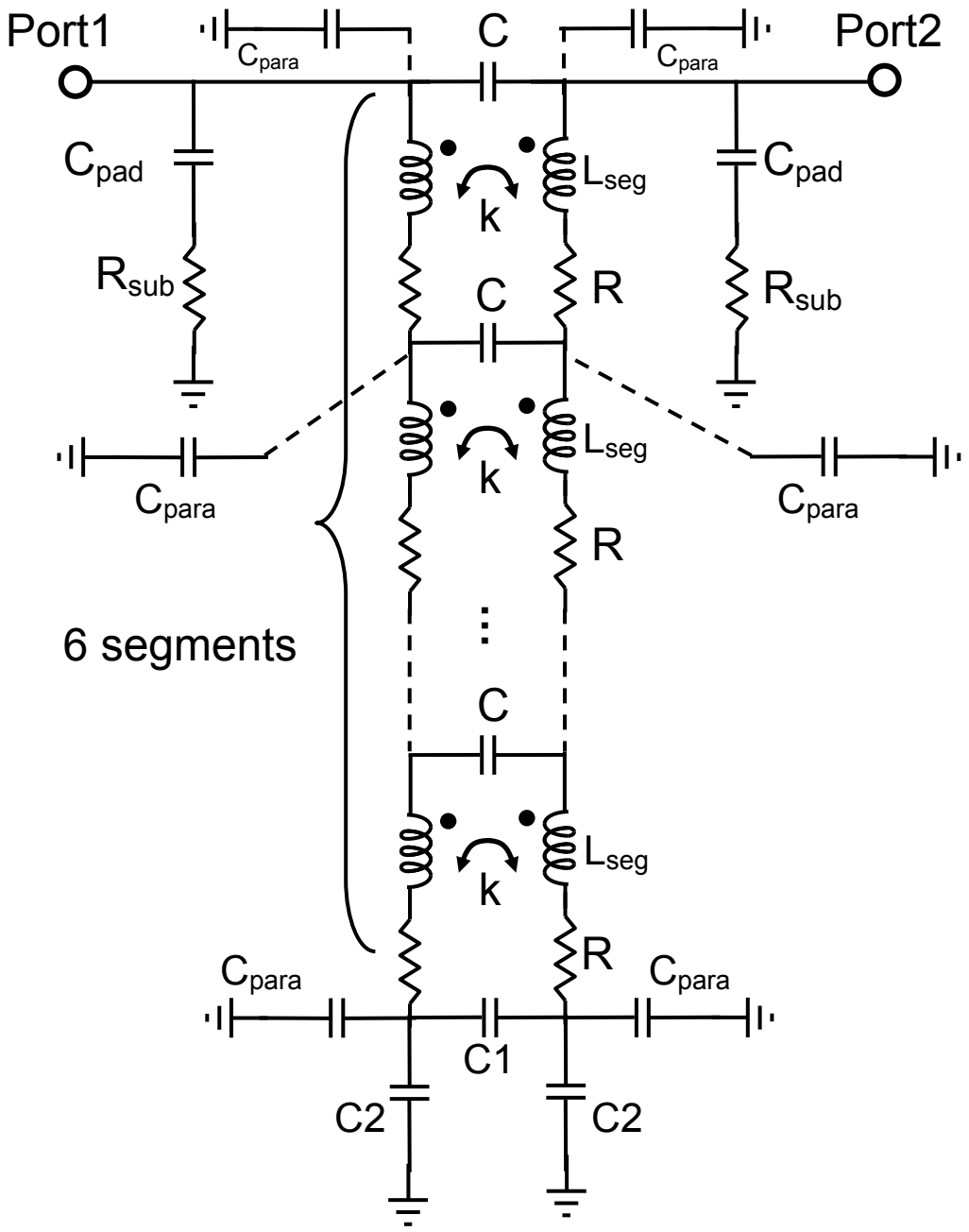


Figure 5-17(b). Circuit model for the bond wire antenna coupling. A distributed inductor model is used to represent the bond wire antenna.

inductive coupling factor. Figure 5-17(c) shows the HFSS and lumped circuit model simulation results of $|S_{11}|$, $|S_{22}|$, and $|S_{21}|$ for the 300-μm separation case. The bond wire antenna is tuned at ~ 60 GHz. The $|S_{21}|$ represents the coupling between two bond wire antennas. It increases from 58 to 62 GHz due to an increase of mutual inductive coupling. It starts to decrease above 62 GHz

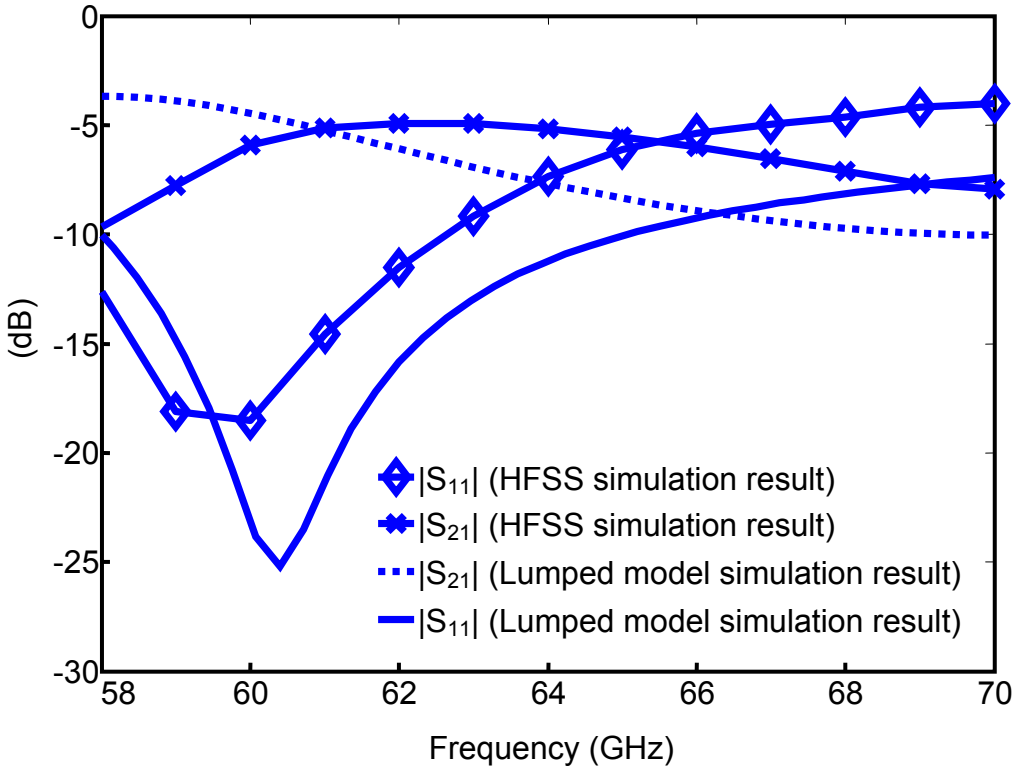


Figure 5-17(c). HFSS vs. circuit simulation results for the 300-μm separation case. The circuit model based simulations show a qualitative agreement with the HFSS simulations.

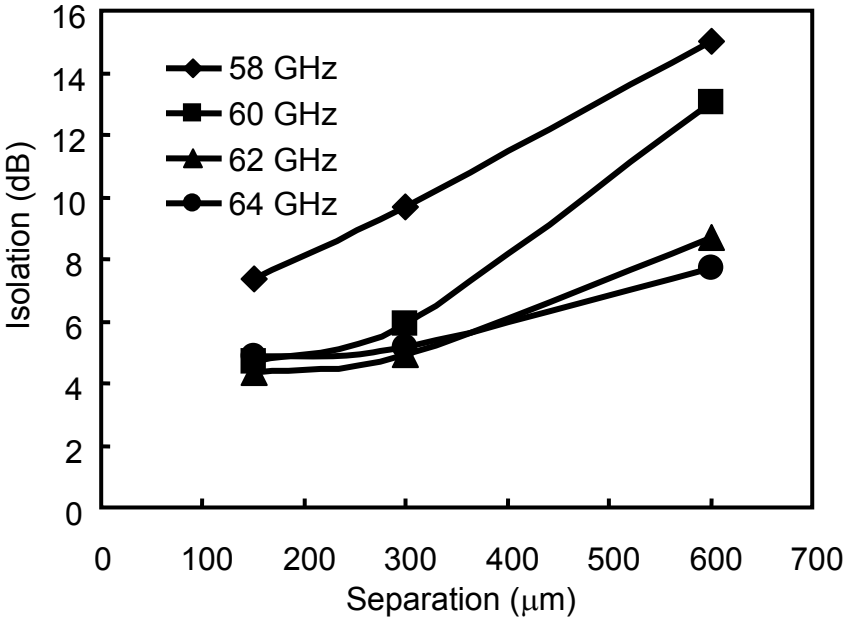


Figure 5-17(d). HFSS simulations of isolation between bond wire antennas at varying separations.

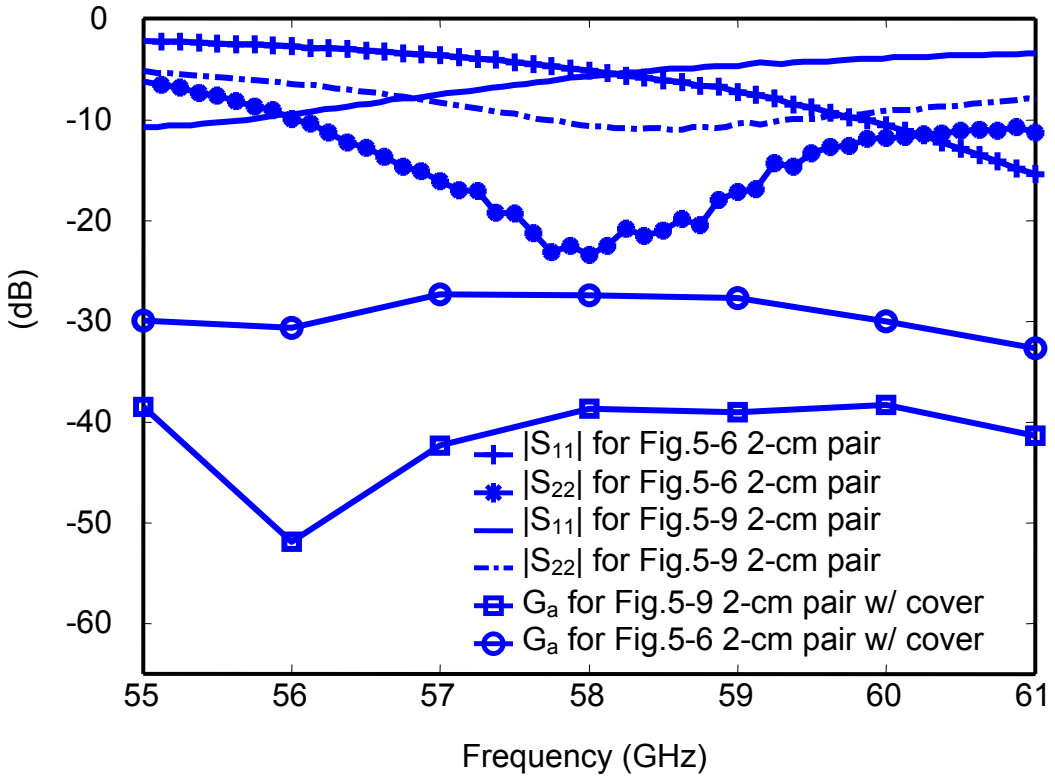


Figure 5-18. Interference measurement results (cover height 2 mm from PCB)

because the parasitic capacitance, C_{pad}, shunts the port to ground [83]. The lumped circuit model qualitatively agrees with the HFSS simulations. Figure 5-17(d) shows the HFSS simulated isolation versus different separations at various frequencies. The simulations indicate that a larger separation improves isolation. When the separation is 300 μm, the isolation is ~ 6 dB at 60 GHz. If the separation is increased to 600 μm, the isolation can be improved to ~ 13 dB. By offsetting the operating frequencies for adjacent bond wire antennas, it should be possible to further improve the isolation.

The bond wires adjacent to an antenna can also modify the antenna characteristics. Figure 5-18 shows that there is on the average, ~ 12 dB G_a drop due to the floating bond wires 300-μm away for the case with a cover. When this and the efficiency degradation due to the match variations are included, G_a is reduced to ~ -53 dB at 10-cm separation, and the link margin for a

1-Gbps radio link operating at ~ 60 GHz with BER of 10^{-12} is estimated to be ~ 10 dB, which is still acceptable.

5.4 Summary

This chapter demonstrated that a bond wire antenna is a realistic option for wireless inter-chip data communication. At 10-cm separation with a metal cover (2 mm gap), antenna pair gain, G_a of –41 dB provides link margin of more than 22 dB for a 1-Gbps radio link operating at ~ 60 GHz with BER of 10^{-12}. Isolation between two adjacent bond wire antennas separated by ~ 300 μm is ~ 6 dB. By offsetting the operating frequency of the antennas, isolation can be improved. It should also be possible to use bond wire antennas for general purpose over the air communication in the 60-GHz unlicensed band.

CHAPTER 6
SUMMARY AND FUTURE WORK

6.1 Summary

An electronic isolator using mainstream CMOS technology has been shown to be able to sustain 70 V. However, this is not sufficient for use in a hybrid engine controller board, which needs to handle at least 300-V DC isolation. To support 300 V and higher, "wireless interconnects" concept has been adopted. On-chip dipole antenna characteristics have been evaluated in a hybrid engine controller board which is a multi-path rich environment. The antenna pair gain and delay spread appear to be acceptable for the application, when a metal cover representing the system enclosure is present. The system block diagram of the CDMA TX chain shown in Figure 6-1 has been demonstrated. The PLL can successfully generate a 24-GHz carrier and the duplexer can provide reasonable insertion loss between PA and antenna ports and reasonable isolation between PA and LNA ports at the same time. The 4-mm on-chip dipole antenna is well suited for use at 16.8 GHz.

A multi-level PA capable of supporting 7 levels at 400-Mbps data rate is demonstrated. The single-ended PA fabricated in the 130-nm CMOS foundry process can achieve 10-dBm saturated output power with 22% maximum PAE while consuming 45.75 mW.

A TX chain with a digital coder can also successfully generate 7 signal levels with a 16.8-GHz carrier and 400-Mbps data rate. The whole CDMA transmitter occupies ~ 5.2 mm^2 and consumes 198 mW. Some modifications are needed to further improve the performance, which are described in section 6.2. Based on the measurements, it should be feasible to realize a CDMA transmitter for wireless interconnects to replace photo-couplers in the hybrid engine controller board. Lower cost and higher data rate can both be achieved.

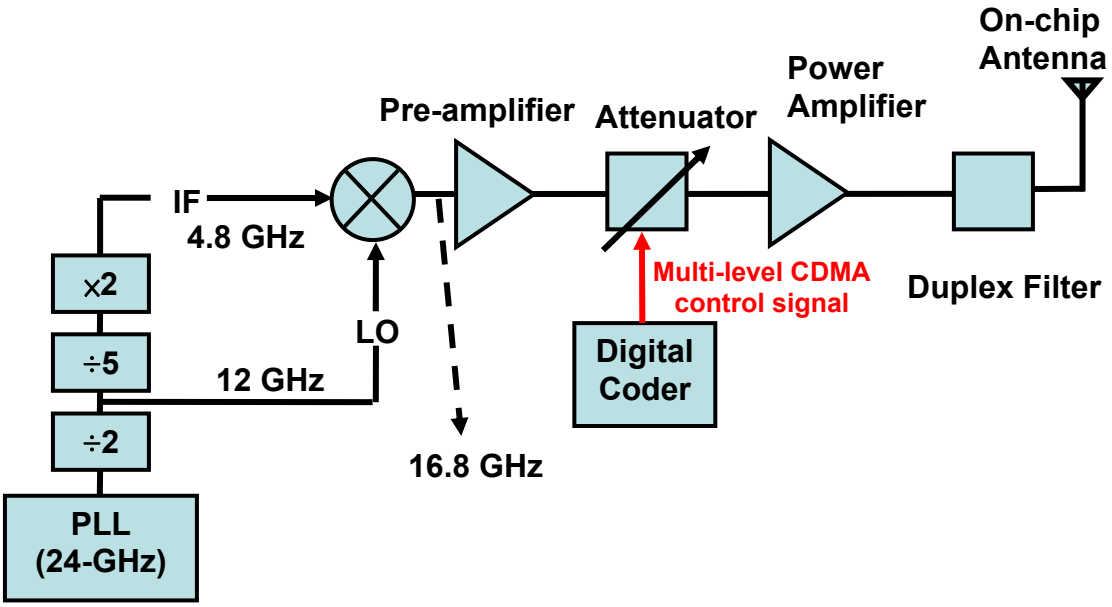


Figure 6-1. CDMA TX chain block diagram.

Bond wires have been shown to be a useful radiator at 60 GHz. The measurements and simulations are in qualitative agreement. It should be possible to use them for inter-chip data communication over free space to solve the packaging cost problem.

6.2 Suggested Future Work

(a) PLL output buffers have to be re-tuned. The interface between the mixer output and input of first pre-amplifier has also to be re-tuned. Finally, attenuator sizes need to be better optimized. Better output power performance and more accurate level ratios are expected after these modifications.

(b) Figure 6-2 shows the suggested measurement setup for the CDMA link demonstration. For the initial testing step, direct wire connection should be used. Eventually, the link demonstration should be performed by using on-chip dipole antennas. The first step is to see if the proper multi-level signal can be observed at the receiver base band output. Afterwards, the multi-level signal should be fed into the ADC block for final data de-modulation. BER test should be performed to compare the demodulated data with that applied at the inputs of CDMA TX. At the same time, a

CDR should be able to recover the 400-MHz clock that is suitable for use as a reference clock in the transmitter chain of motor side.

(c) Integrate the RF receiver circuits into a transceiver in the dead-time controller side. Full duplex system demonstration should be performed.

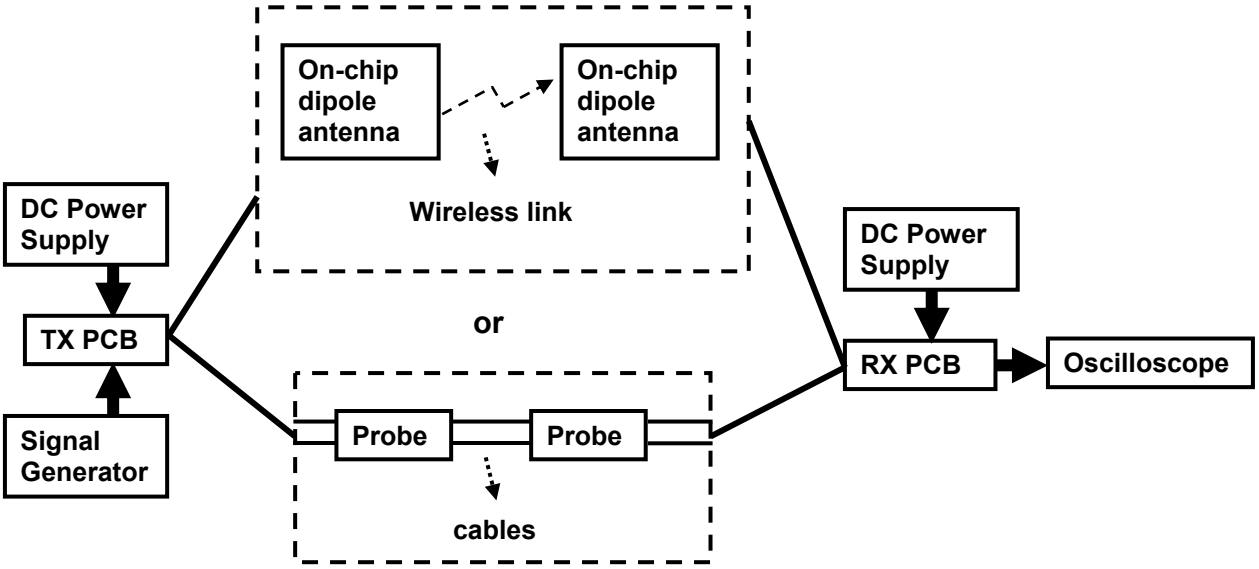


Figure 6-2. Suggested measurement setup for the CDMA link demonstration.

APPENDIX A
90 DEGREE ANGLE CALIBRATION FOR GS (SG) PROBES

Figure A-1 shows a calibration substrate CS-8 from GGB Industries Inc. There is a ring type calibration structure. This is the structure used for 90 degree angle calibration, which is required for duplexer characterization. There are open, short, load, and through calibration structures. By using the standard calibration steps, 90 degree angle calibration for GS (SG) probes can be accomplished.

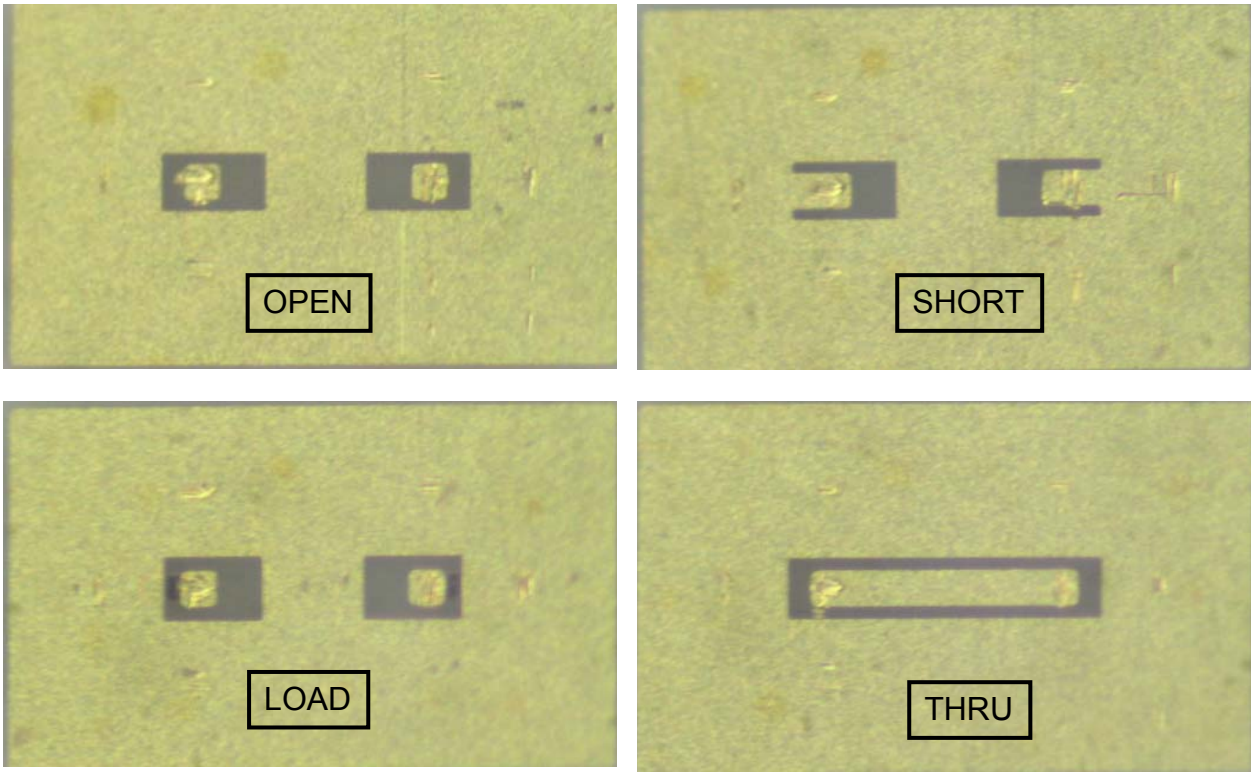


Figure A-1. Ring type calibration structures on the CS-8 calibration substrate.

APPENDIX B
CDMA TRANSMITTER PRINTED CIRCUIT BOARD DESIGN CONSIDERATIONS

There are several design considerations for the CDMA TX PCB. It has to have the flexibility to support multiple test scenarios. This is critical if certain blocks malfunction and need to be bypassed. Figure B-1 shows the layout of TX chain. Several internal nodes are brought out to GSSG pads for on-chip measurements and signal injection. For example, the PLL output pads are reserved for checking if the PLL is functional. An external source can also be used to drive the divider chain blocks and bypass the PLL block.

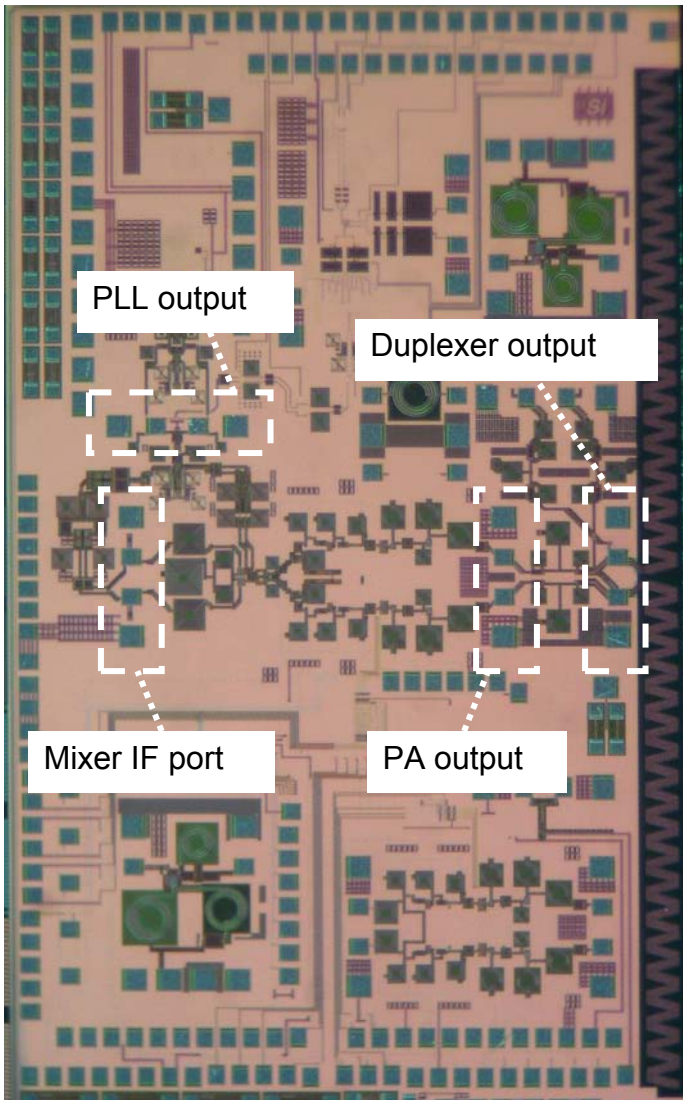


Figure B-1. Die micrograph showing internal testing nodes.

The internal node, mixer IF input, can be used to apply an external 4.8-GHz signal if the IF divider chain is malfunctions. The PA output pads are reserved for checking the output power level without the duplexer. The connection between the PA output pads and duplexer uses metal 8, which is convenient for laser cutting after fabrication. Similarly, the duplexer output pads are also reserved for checking the output power without the antenna. The TX chain should be carefully designed to account for the pad parasitics (Figure B-1). For testing scenarios other than the full transmitter, some bond wires have to be removed. Therefore, careful pad arrangement is also critical at the chip design phase.

The design of PCB also needs to take these issues into account to accommodate all the testing scenarios. Probe landing directions must have a clean PCB surface, which means the off-chip components could not be present along the landing path, shown in Figure B-2 (arrow

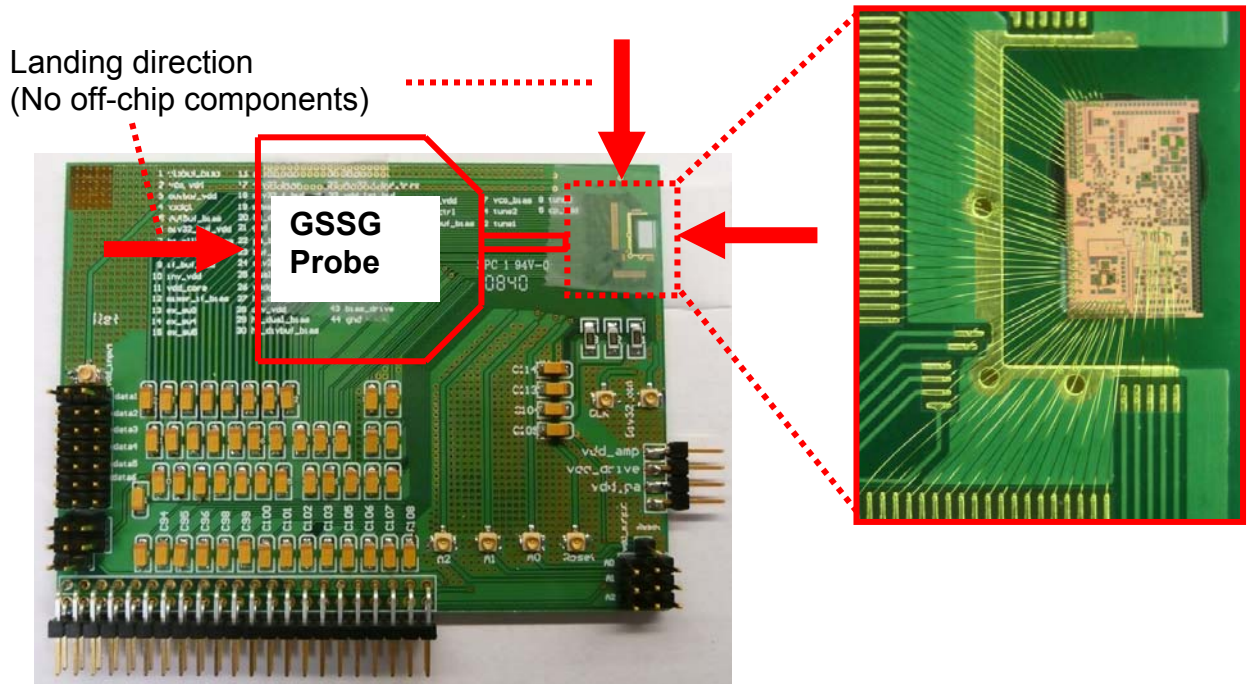


Figure B-2. TX chain testing PCB showing possible landing directions. There should not be off-chip components on the PCB surface along the landing direction.

direction means landing direction). Since the die is placed at a corner of the PCB, the concern for the probe landing is mitigated. The only design issue is to accommodate the lading for the mixer IF ports. As shown in Figure B-2, the landing direction is from the left. The PCB surface is specially design to not have off-chip components along the landing path.

Since there are over 50 bond wires for the transmitter chain, a careful pad arrangement is critical. In this work, a double row bonding scheme is adopted to save die area, shown in Figure B-3. The requirement for the double row bonding is to reserve sufficient separation between pads and rows. The reasonable separation between rows is 65 μm. The separation between pads is 25 μm. The pad size is 75 x 63 μm^2. Under this specific design, 0.8-mil gold wire is used for wire

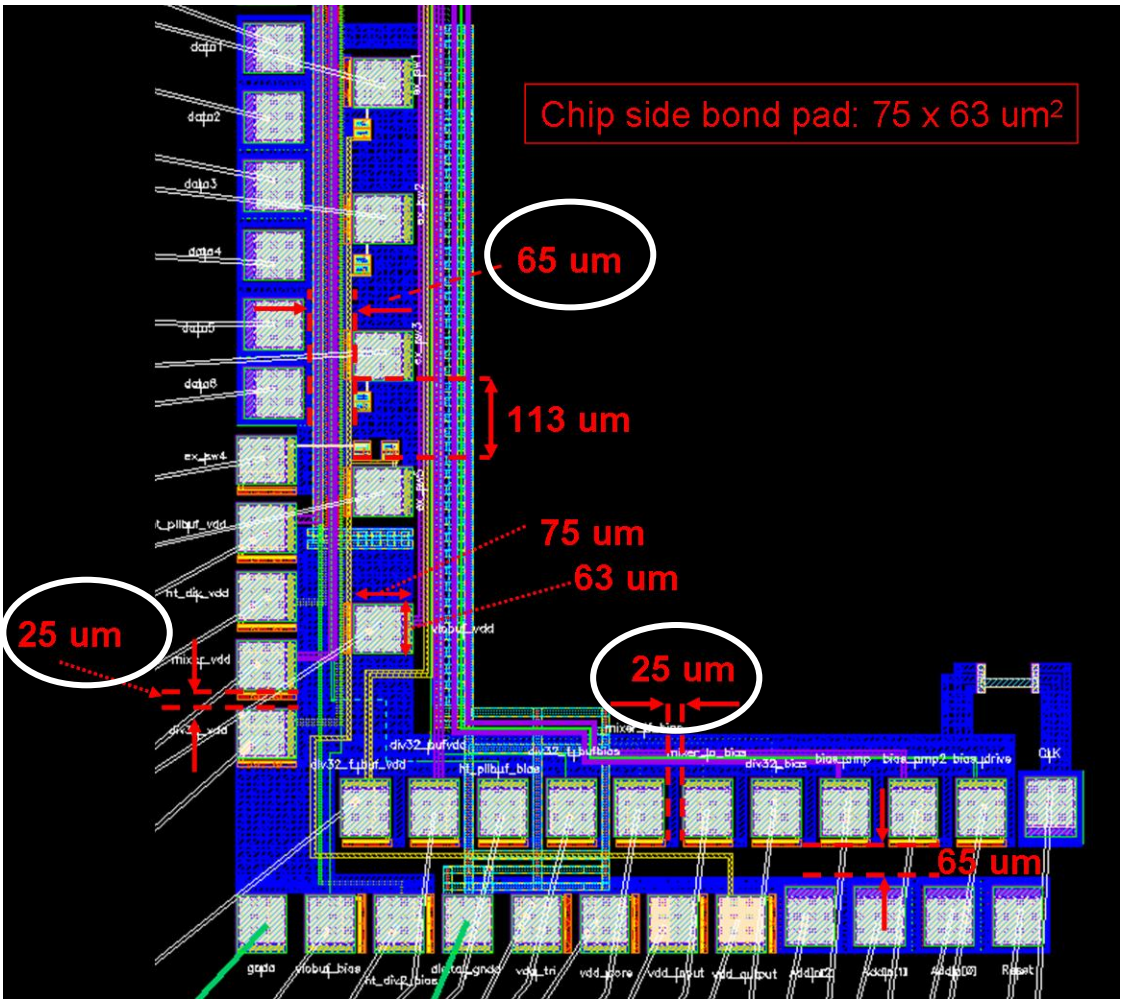


Figure B-3. Double row bonding design with the proper pad arrangement on the chip side.

bonding. The total bond wire number is 77. One important requirement for pad arrangement on the chip side is to put ground bond pads at the outer row. Since the ground bond pads on the PCB is closer to the chip edge than the other bond pads, shown in Figure B-4. The ground bond wires need to be bonded out first. The inner row bonding can have higher loop height to avoid touching the ground bond wires.

On the PCB side, a common finger length is 20 mil (5-mil finger width). In order to use double row bonding, 40-mil finger length is suggested by the bonding company for better

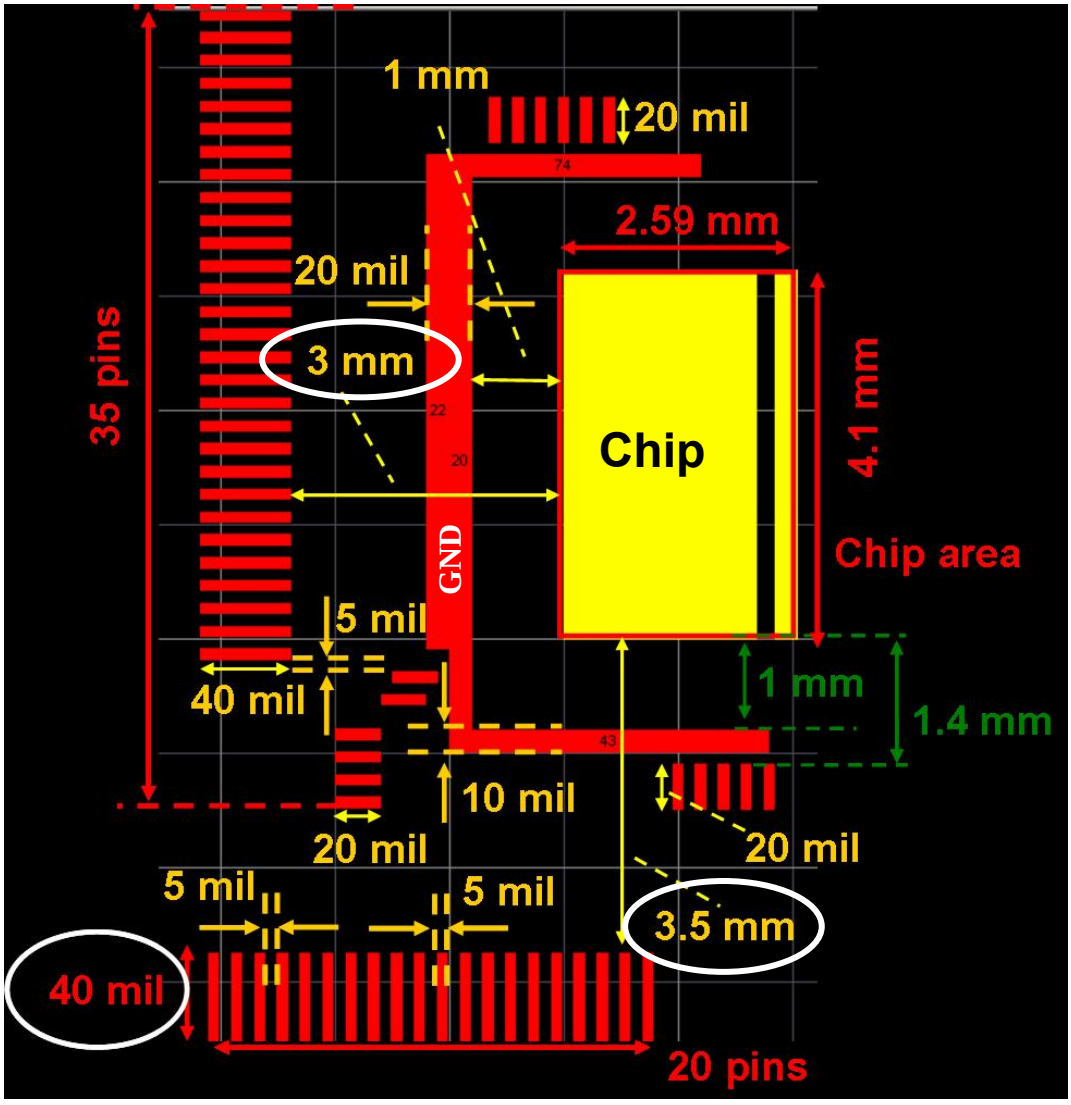


Figure B-4. Double row bonding design with a proper finger length on the PCB side.

bonding flexibility and may be able to tolerate slightly poor gold-plated surface shown in Figure B-4. Because there are lots of bond wires at the left hand side and bottom side, a larger separation between the chip edge and bond pads on the PCB is recommended. The separation is at least 3 mm, which is needed to properly angle bond wires so that they do not touch each other. The last concern here is the trace width. The assembly house has the minimum specification of 5-mil trace width. If the over-etching is happened, it is safer to design the PCB metal traces to be 6 mil.

LIST OF REFERENCES

[1] D. Hermance, and S. Sasaki, "Hybrid Electric Vehicles Take to The Streets," *IEEE Spectrum*, Vol. 35, Issue 11, pp. 48-52, Nov. 1998.

[2] Floyd A Wyczalek, "Market Mature 1998 Hybrid Electric Vehicles," *IEEE Aerospace and Electronic Systems Magazine*, Vol. 14, Issue 3, pp. 41-44, March 1999.

[3] A kira Kawahashi, "A New-Generation Hybrid Electric Vehicle and Its Supporting Power Semiconductor Devices," *IEEE Power Semiconductor Devices and ICs Symp. Dig. Tech. Papers*, pp. 23-29, 24-27 May 2004.

[4] T. P. Bohn, R.D. Lorenz, and E. R. Olson, "Measurement of In-Situ Currents in a Hybrid Electric Vehicle Integrated Power Module Using Giant Magnetoresistive Sensors," *IEEE Power Electronics in Transportation*, pp. 55-59, 2004.

[5] K. K. O, K. Kim, B. Floyd, J. Mehta, H. Yoon, C.-M. Hung, D. Bravo, T. Dickson, X. Guo, R. Li, N. Trichy, J. Caserta, W. Bomstad, J. Branch, D.-J. Yang, J. Bohorquez, E. Seok, L. Gao, A. Sugavanam, J.-J. Lin, J. Chen, F. Martin, and J. E. Brewer, "On-Chip Antennas in Silicon ICs and Their Application," *IEEE Trans. Electron Devices*, Vol. 52, Issue 7, pp. 1312-1323, July 2005.

[6] K. Kim. H. Yoon, and K. K. O, "On-chip wireless interconnection with integrated antennas," *Tech. Digest of IEDM*, pp. 485-488, San Francisco, 2000.

[7] Y. P. Zhang, M. Sun, and L. H. Guo, **"**On-chip antennas for 60-GHz radios in silicon technology,**"** *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1664-1668, July, 2005.

[8] Y. Su, J.-J. Lin, and K. K. O, "A 20-GHz CMOS RF down-converter with an on-chip antenna", *IEEE Int. Solid-State Circuits Conf Dig. Tech. Papers*, pp. 270-271, Feb. 2005.

[9] C. Cao, Y. Ding, X. Yang, J.-J. Lin, A. K. Verma, J. Lin, F. Martin, and K. K. O, "A 24-GHz transmitter with an on-chip antenna in 130-nm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 184-185, June 2006.

[10] R. Li, Xi. Guo, Dong-Jun Yang, and K. K. O, "Initialization of a wireless clock distribution system using an external antenna," *IEEE CICC Dig. Tech. Papers*, pp. 105-1080, 18-21 Sept. 2005.

[11] Xi. Guo, Dong-Jun Yang, R. Li, and K. K. O, "A Receiver with Start-up Initialization and Programmable Delays for Wireless Clock Distribution," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 1530-1539, Feb. 2006.

[12] R. Li, Xi. Guo, Dong-Jun Yang, and K. K. O, "Wireless Clock Distribution System Using an External Antenna," *IEEE J. Solid-State Circuits*, Vol. 42, no. 10, pp. 2283-2292, Oct. 2007.

[13] K. K. O, K. Kim, B. A. Floyd, J. Mehta, and H. Yoon, "Inter and Intra-Chip Wireless Clock Signal Distribution Using Microwaves: A Status of an Initial Feasibility Study," *IEEE Government Microcircuit Applications Conf.*, pp. 306-309, Mar. 1999, Monterey, CA.

[14] B. A. Floyd, K. Kim, and K. K. O, "Wireless Interconnection in a CMOS IC with Integrated Antennas," *IEEE Intl. Solid-State Circuits Conf.*, pp. 328-329, San Francisco, CA, Feb. 2000.

[15] B. A. Floyd, C.-M. Hung, and K. K. O, "A 15-GHz Wireless Interconnect Implemented in a 0.18-μm CMOS Technology Using Integrated Transmitters, Receivers, and Antennas," *IEEE J. Solid-State Circuits*, Vol. 37, no. 5, pp. 543-552, May 2002.

[16] K. Kim, *Dissertation* "Design and Characterization of RF Components for Inter- and Intra-Chip Wireless Communication," University of Florida, Gainesville, FL, 2000.

[17] Xi. Guo, *Dissertation* "CMOS Intra-Chip Wireless Clock Distribution," University of Florida, Gainesville, FL, 2005.

[18] R. Li, *Dissertation* "A Wireless Clock Distribution System Using an External Antenna," University of Florida, Gainesville, FL, 2005.

[19] B. Floyd, C.-M. Hung, and K. K. O, "A 15-GHz wireless interconnect implemented in a 0.18-μm CMOS technology using integrated transmitters, receivers, and antennas," *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 155-158, Japan, 2001.

[20] B. Floyd, *Dissertation* "A CMOS Wireless Interconnect System for Multigigahertz Clock Distribution," University of Florida, Gainesville, FL, 2001.

[21] N. Kanekawa, Y. Kojima, S. Yukutake, M. Nemoto, T. Iwasaki, K. Takami, Y. Tekeuchi, A. Yano, and Y. Shima, "An analog front-end LSI with on-chip isolator for V.90 56 kbps modems," *IEEE CICC Dig. Tech. Papers*, pp. 327-330, *2000*.

[22] Y. Kojima, M. Nemoto, S. Yukutake, T. Iwasaki, M. Amishiro, N. Kanekawa, A. Watanabe, Y. Takeuchi, and N. Akiyama, "2.3 kVac 100 MHz multi-channel monolithic isolator IC*," The 12th Int. Symp. Power Semiconductor Devices and ICs, 2000. Proc.*, pp. 309-312, 22-25 May 2000.

[23] N. Akiyama, Y. Kojima, M. Nemoto, S. Yukutake, T. Iwasaki, M. Amishiro, N. Kanekawa, A. Watanabe, and Y. Takeuchi, "A high-voltage monolithic isolator for a communication network interface," *IEEE Trans. Electron Devices,*, Volume 49, Issue 5, pp. 895-901, May 2002.

[24] Jian Xu, J. Wilson, S. Mick, Lei Luo, and P. Franzon, "2.8 Gb/s inductively coupled interconnect for 3D ICs," *Symp. VLSI Circuits, Dig. Tech. Papers,* pp. 352-355, 16-18 June 2005.

[25] M.Q. Gordon, T. Yao, and S.P. Voinigescu, "65-GHz receiver in SiGe BiCMOS using monolithic inductors and transformers," *Silicon Monolithic Integrated Circuits in RF Systems Dig. of Papers*, pp. 265-268, Jan. 2006.

[26] Mounir. Y. Bohsali, and Ali.M. Niknejad., "Microwave performance of monolithic silicon passive transformers," *RFIC Symp. Dig. Tech. Papers,* pp. 647-650, 2004.

[27] S. M. Sze, and G. Gibbons, "Effect of junction curvature on breakdown voltage in semiconductors," *Solid-State Electron*, Vol. 9, pp. 831-845, 1966.

[28] J. Akhtar, and S. Ahmad, "Breakdown voltage of a rectangular planar diffused junction with rounded corners," *IEEE Trans. Electron Devices,*, Volume 31, no. 12, pp. 1781-1783, Dec. 1984.

[29] C. Basavanagoud, and K.N. Bhat, "Effect of lateral curvature on the breakdown voltage of planar diodes," *IEEE Electron Device Lett.*, vol. 6, no. 6, pp. 276-278, June 1985.

[30] Sheng S. Li, *Semiconductor Physical Electronics*, Plenum Press, New York, 1993.

[31] Maxim application note 2045, May 21, 2003.

[32] Y.-J. Zheng, Y.-P. Zhang, and Y. Tong, "A Novel Wireless Interconnect Technology Using Impulse Radio for Interchip Communication," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 4, part 2, pp. 1912-1920, Apr. 2006.

[33] P. K. Saha, N. Sasaki, and T. Kikkawa, "A Single-Chip Gaussian Monocycle Pulse Transmitter using 0.18-μm CMOS Technology for Intra/Interchip UWB Communication," in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 204-205, June 2006.

[34] Jau-Jr Lin, Xiaoling Guo, Ran Li, J. Branch, J.E. Brewer, and K. K. O, "10x improvement of power transmission over free space using integrated antennas on silicon substrates", *IEEE CICC Dig. Tech. Papers*, pp. 697-700, Oct. 2004.

[35] Hyun Yoon, Hyun Yoon, Kihong Kim, and K. K. O, "Interference effects on integrated dipole antennas by a metal cover for an integrated circuit package", *Antenna and Propagation Society Int. Symp.*, vol. 2, pp. 782-785, July 2000.

[36] Jau-Jr Lin, A. Sugavanam, Gao Li, J.E. Brewer, and K. K. O, **"**On-wafer measurement setups for on-chip antennas fabricated on silicon substrates", *ARFTG Microw. Measurements Conf.*, pp. 221-225, Dec. 2004.

[37] Zhi Ming Chen, and Y.P. Zhang, **"**Inter-Chip Wireless Communication Channel: Measurement, Characterization, and Modeling**",** *IEEE Trans. Antennas and Propagation*, vol. 55, no. 3, pp. 978-986, March 2007.

[38] J. Buechler, E. Kasper, P. Russer, and K. M. Strohm., "Silicon High-Resistivity-Substrate Millimeter-Wave Technology," *IEEE Trans. Microw. Theory Tech.*, vol. 34, no.12, pp. 1516-1521, Dec. 1986.

[39] N. Camilleri, and B. Bayraktaroglu, "Monolithic Millimeter-Wave IMPATT Oscillator and Active Antenna," *IEEE MTT-S Int. Microw. Symp. Dig. Papers*, pp. 955-958, June 1988.

[40] Jau-Jr Lin, *Dissertation* "On-Chip Antennas for Short-Range Wireless Communications," University of Florida, Gainesville, FL, 2007.

[41] T. S. Rappaport, *Wireless Communications: Principles and Practice, 2nd ed.*, Prentice Hall, 2001.

[42] Swaminathan Sankaran, *Dissertation* "Recievers Using Schottky Barrier Diodes in CMOS," University of Florida, Gainesville, FL, 2008.

[43] John B. Groe, and Lawrence E. Larson, *CDMA Mobile Radio Design*, Artech House Publishers, 2000.

[44] Riaz Esmailzadeh, and Masao Nakagawa, *TDD-CDMA for Wireless Communications*, Artech House Publishers, 2002.

[45] Digital Coder first designed and synthesized by Wuttichai Lerdsitsomboon in 2007 and modified by Ruonan Han in 2008.

[46] T. Iwai, K. Kazuhiko. Y. Nakasha, T. Miyashita, S. Ohara, and K. Joshin, "42% high-efficiency two-stage HBT power amplifier MMIC for W-CDMA cellular phone systems," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no.12, pp. 2267-2572, Dec. 2000.

[47] P. Tseng, L. Zhang, G. Gao, and M.F. Chang, "A 3-V monolithic SiGe HBT power amplifier for dual-mode (CDMA/AMPS) cellular handset applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1338-1344, Sept. 2000.

[48] V.T.S. Vintola, M.J. Matilainen, S.J.K. Kalajo, and E.A. Jarvinen, "Variable-Gain power amplifier for mobile WCDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no.12, pp. 2464-2471, Dec. 2001.

[49] S. Luo, and T. Sowlati, "A monolithic Si PCS-CDMA power amplifier with 30% PAE at 1.9GHz using a novel biasing scheme," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 9, pp. 1552-1557, Sept. 2001.

[50] S. Hamedi-Hagh, and C.A.T. Salama, "A 1 V, 8 GHz CMOS integrated phase shifted transmitter for wideband and varying envelope communication systems," *IEEE CICC Dig. Tech. Papers*, pp. 447-450, 2003.

[51] N. O. Sokal, and A. D. Sokal, "Class E-A New Class of High Efficiency Tuned Single-Ended Switching Power Amplifier," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 168-176, June 1975.

[52] C. Cao, H. Xu, Y. Su, and K. K. O, "An 18-GHz, 10.9-dBm Fully-Integrated Power Amplifier with 23.5% PAE in 130-nm CMOS," *Eur. Solid-State Circuit Conf. Dig. Tech. Papers*, pp. 137-140, Sept. 2005.

[53] R. Thuringer, M. Tiebout, W. Simburger, C. Kienmayer, and A.L. Scholtz, "A 17 GHz linear 50 Ω output driver in 0.12 μm standard CMOS," *IEEE Radio Frequency Integrated Circuits Symp. Dig. Tech. Papers*, pp. 207-210, June 2003.

[54] A.V. Vasylyev, P. Weger,W. Bakalski, and W. Simbuerger, "17-GHz 50-60 mW power amplifiers in 0.13-μm standard CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 1, pp. 37-39, Jan. 2006.

[55] A. Komijani, A. Natarajan, and A. Hajimiri, "A 24-GHz, +14.5-dBm fully integrated power amplifier in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1901-1908, Sept. 2005.

[56] F. H. Raab, B. E. Sigmon, R. G. Myers, and R. M. Jackson, "L-band transmitter using Kahn EER technique," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 12, pp. 2220-2225, Dec. 1998.

[57] D. Su, and W. McFarland, "An IC for linearizing RF power amplifiers using envelope elimination and restoration," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2252-2258, Dec. 1998.

[58] P. Midya, M. Greuel, and P.T. Krein, "Sensorless current mode control - an observer based technique for DC-DC converters", *28th Annual IEEE Power Electronics Specialists Conf.*, vol. 1, pp. 197-202, 1997.

[59] G. Hanington, P. Chen, P. M. Ashbeck, and L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1471-1476, Aug. 1999.

[60] P. Midya, K. Haddad, L. Connell, S. Bergstedt, and B. Roeckner, "Tracking power converter for supply modulation of RF power amplifier," *32nd Annual IEEE Power Electronics Specialists Conf.*, vol. 3, pp. 1540-1545, 2001.

[61] B. Sahu, and G.A. Rincon-Mora, "A high-efficiency linear RF power amplifier with a power-tracking dynamically adaptive buck-boost supply," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 1, part 1, pp. 112-120, Jan. 2004.

[62] Adel S. Sedra, and Kenneth C. Smith, *Microelectronic Circuits, 4th ed.*, Oxford University Press, 1997.

[63] Y.S. Noh, and C.S. Park, "An intelligent power amplifier MMIC using a new adaptive bias control circuit for W-CDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 967-970, June 2004.

[64] B. Sahu, and G.A. Rincon-Mora, "A high efficiency WCDMA RF power amplifier with adaptive, dual-mode buck-boost supply and bias-current control," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 3, pp. 238-240, March 2007.

[65] Changhua Cao, and K. K. O, "A power efficient 26-GHz 32:1 static frequency divider in 130-nm bulk CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 11, pp. 721-723, Nov. 2005.

[66] Yanping Ding, *Dissertation* "CMOS Synthesizers for 24-GHz Radios," University of Florida, Gainesville, FL, 2007.

[67] Huainan Ma, Sher Jiun Fang, Fujiang Lin, and H. Nakamura, "Novel active differential phase splitters in RFIC for wireless applications," *IEEE Trans. Microw. Theory .Tech.*, vol. 46, no. 12, part 2, pp. 2597-2603, Dec. 1998.

[68] M. Rajashekharaiah, P. Upadhyaya, Deukhyoun Heo, and E. Chen, "A new gain controllable on-chip active balun for 5 GHz direct conversion receiver," *IEEE Int. Symp. on Circuits and Systems*, vol. 5, pp. 5115-5118, May 2005.

[69] Ta-Tao Hsu, and Chien-Nan Kuo, "Low power 8-GHz ultra-wideband active balun," *Dig. of Papers. Silicon Monolithic Integrated Circuits in RF Systems*, pp. 365-368, 2006.

[70] A. Ruiz, E. Vega, R. Katiyar, and R. Valentin, "Novel Enabling Wire Bonding Technology," *Electronic Compon. Tech. Conf.*, pp. 458-462, 2007.

[71] T. Ellis, "The Future of Gold in Electronics," Retrieved 02, 07, 2007, from www.gold.org.

[72] L. Larson, and D. Jessie, "Advances in RF packaging technologies for next-generation wireless communications applications," *IEEE CICC Dig. Tech. Papers*, pp. 323-330, Sept. 2003.

[73] Federico Alimenti, Paolo Mezzanotte, Luca Roselli, and Roberto Sorrentino, "Modeling and Characterization of the Bonding-Wire Interconnection," *IEEE Tran. Microw. Theory .Tech.*, Vol. 49, No. 1, pp. 142-150, Jan. 2001.

[74] Hai-Young Lee, "Wideband characterization of a typical bonding wire for microwave and millimeter-wave integrated circuits," *IEEE Trans. Microw. Theory .Tech.*, vol. 43, no. 1, pp. 63-68, Jan. 1995.

[75] Sang-Ki Yun, and Hai-Young Lee, "Parasitic impedance analysis of double bonding wires for high-frequency integrated circuit packaging," *IEEE Microw. Guided Wave Lett.*, vol. 5, no. 9, pp. 296-298, May 1995.

[76] Andrea Jentzsch, and Wolfgang Heinrich, "Theory and Measurements of Flip-Chip Interconnects for Frequencies up to 100 GHz," *IEEE Trans. Microw. Theory Tech.*, Vol. 49, No. 5, pp. 871-878, May 2001.

[77] U.R. Pfeiffer, and A. Chandrasekhar, **"**Characterization of flip-chip interconnects up to millimeter-wave frequencies based on a nondestructive in situ approach**,"** *IEEE Trans. Advanced Packaging*, Vol. 28, No. 2, pp. 160-167, May 2001.

[78] John D. Kraus, and Ronald J. Marhefka, *Antennas For All Applications, 3rd ed.*, McGraw-Hill, 2001.

[79] Jau-Jr Lin, Li Gao, Aravind Sugavanam, Xiaoling Guo, Ran Li, Joe E. Brewer, and K. K.O, "Integrated antennas on silicon substrates for communication over free space," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 196-198, April 2004.

[80] Jau-Jr Lin, Hsin-Ta Wu, and K. K. O, "Compact on-chip monopole antennas on 20-Ω-cm silicon substrates for operation in the 5.8-GHz ISM band**"** *Tech. Digest of IEDM*, pp. 947-950, Dec. 2005.

[81] C. A. Balanis, Antenna Theory, New York: Harper & Row, 1982.

[82] David K. Cheng, *Field and Wave Electromagnetics, 2nd ed.*, Addison-Wesley, 1989.

[83] Seong-Mo Yim, Tong Chen, and K. K. O, "The effects of a ground shield on the characteristics and performance of spiral inductors,**"** *IEEE J. Solid-State Circuits*, Vol. 37, no. 2, pp. 237-244, Feb. 2002.

BIOGRAPHICAL SKETCH

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