IMPACT OF MECHANICAL STRESS ON SILICON AND GERMANIUM METAL-OXIDE-SEMICONDUCTOR DEVICES: CHANNEL MOBILITY, GATE TUNNELING CURRENTS, THRESHOLD VOLTAGE, AND GATE STACK

By

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To my parents in Korea and family, Luke and Jin-Hwa
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Our study explores the impact of uniaxial mechanical stress on metal-oxide-semiconductor devices in terms of channel mobility, gate direct tunneling current, trap-assisted gate tunneling current, threshold voltage, high-k gate dielectric, and metal gate using four point wafer bending setup. Beyond 90 nm technology node, strained Si technology has been a mainstream in VLSI manufacturing technology. Therefore, it is important to properly understand strain effects on channel mobility and also other electrical parameters, such as gate leakage, gate stack, and reliability of MOS devices.

Process-induced uniaxial stress has been compared with substrate-induced biaxial tensile stress and its advantages on Si p-MOSFETs have been pointed out. The net band splitting from strain and confinement is additive for uniaxial compressive stress but subtractive for biaxial tensile stress. This results in larger hole mobility enhancement under uniaxial compressive stress.

Impact of uniaxial mechanical stress on gate direct tunneling current in Si and Ge MOS devices are investigated. Because of the different conduction edges of Si and Ge, opposing uniaxial mechanical stress dependence has been observed in gate direct tunneling currents of Si and Ge n-MOSFETs. Based on gate bias-dependent gate direct tunneling current under
mechanical stress, Ge conduction band deformation potentials have been extracted and agree well with theoretical calculations. We also measure gate direct tunneling current of Si and Ge p-MOSFETs under mechanical stress using carrier separation technique in order to investigate strain effects on subband structure in p-type inversion layer of Si and Ge. Due to larger strain-induced valence band edge splitting in Ge, the relative change in gate tunneling current in Ge is 3 times larger than that in Si under uniaxial tensile stress.

Strain effects on trap-assisted gate tunneling mechanism, including trap-assisted tunneling and Poole-Frenkel emission, are also investigated from both SiO₂ and nitrided hafnium silicate (HfSiON) gate dielectric Si MOS capacitors. A decrease in electron and/or hole trap activation energy results in an increase in trap-assisted gate tunneling current with both [110] tensile and compressive stresses. The dielectric constant of HfSiON also increases with mechanical stress, resulting from strain-induced N p band splitting, which reduces the band gap of HfSiON.
CHAPTER 1
INTRODUCTION

1.1 Overview of Strained CMOS Technology

Strain effects on semiconductors such as silicon (Si) and germanium (Ge) have been extensively studied to maintain historical performance improvement. Bardeen and Shockley introduced a deformation potential theory, explaining that the electron- or hole-phonon interaction causes a static displacement of the atoms, thus resulting in the conduction or valence band energy shifts[1]. Herring et al. and Pikus et al. quantified the conduction and valence band energy shift as a function of strain, respectively, based on deformation potential constants, which are important parameters in strained CMOS technology[2, 3].

The origin of strained-Si to improve CMOS devices can be traced to thin Si layer grown on relaxed SiGe substrates in 1980s[4, 5]. The thin Si layer takes the larger lattice constant of the SiGe and creates biaxial tensile stress. Wafer-based substrate strain was experimentally and theoretically studied by a large number of researchers for two decades[6]. In the 1990s, two other strained-Si activities started based on process-induced strain. First, high-stress capping layers deposited on MOSFETs were investigated as a technique to introduce stress into a channel.[7] Second, Gannavaram et al [8] proposed SiGe in the source and drain area for higher boron activation and reduced external resistance. It was this embedded SiGe literature that prompted Intel [9] to evaluate the technology, which resulted in larger than expected device performance enhancement, which, after considerable internal debate, was later attributed to uniaxial compressive channel stress[10]. Still, neither biaxial nor uniaxial stress was immediately adopted in CMOS logic technologies for several reasons. Biaxial stress suffers from defects and performance loss at high vertical electric fields[11]. Process-induced stress requires different stress types (tensile and compressive for n- and p-channel, respectively) to simultaneously
improve both n- and p-channel devices. However, inside Intel and in the industry, strain was becoming recognized as offering the best potential to enhance performance in sub-100-nm process technologies (significantly larger performance gain than high-κ gates, fully depleted silicon-on-insulator (SOI), or multi-gate devices). The only debate was on the best path to take (biaxial substrate versus uniaxial-process-induced stress)[12].

Careful analysis of the 1990’s biaxial and uniaxial strained-Si experimental data suggested that the industry adopt process-induced uniaxial strain. The key observations are as follows. First, uniaxial (versus biaxial) stress provides significantly larger hole mobility enhancement at both low strain and high vertical electric field due to differences in the warping of the valence band under strain[13]. Large mobility enhancement at low strain is important since yield loss via dislocations occurs at high strain. Second, uniaxial (as compared to biaxial) stress enhanced mobility provides larger drive current improvement for nanoscale short-channel devices. This results since the uniaxial stress-enhanced electron and hole mobility arises mostly from reduced conductivity effective mass (versus reduced scattering for biaxial stress), since uniaxial shear stress provides significant valence and some conduction band warping. Lastly, process-induced uniaxial stress causes approximately five times smaller n-channel threshold voltage shift. Since any threshold voltage shift needs to be retargeted by adjusting channel doping (for industry standard poly-Si gate devices on bulk or partially depleted SOI), the larger threshold voltage shift for wafer substrate-induced biaxial tensile stress causes approximately half of the stress-enhanced electron mobility to be lost[14]. Rarely is the stress-induced threshold voltage shift taken into account in the biaxial tensile-stress mobility data.

On the other hand, Ge and strained Ge are currently being investigated as a potential replacement to strained Si[15, 16]. To characterize strained Ge, accurate deformation potential
constants ($\Xi_d$ and $\Xi_u$) are required to model the strain induced energy level shifts and splitting. Recently, strain altered gate leakage current has been proposed as an accurate method to extract conduction band deformation potential constants and has been applied to Si with the results matching theoretical expectations\cite{17, 18}. For Si p-MOSFETs, uniaxial tensile stress increases while compressive stress decreases the gate tunneling current\cite{19, 20}. An opposite dependence exists in Si n-MOSFETs\cite{18, 21}. These results can be understood from the strain-altered out-of-plane effective mass, energy splitting, and carrier repopulation in Si inversion layer\cite{20}, which can be used to understand impact of strain on gate tunneling currents of Ge n- & p-MOSFETs.

Since Ge MOSFETs are usually incorporated with high k dielectric and metal gate, strain effects on metal/high-k dielectric gate stack, such as strain altered metal gate work function and high-k dielectric constant, can change the electrical parameters, such as the threshold voltage, gate leakage current, gate capacitance and so on.

Unlike SiO$_2$ technology, high-k dielectric technology suffers from trap-related problems (i.e. bulk and interface traps) which may result in a degradation of the benefit from strain technology. Even in SiO$_2$ devices, especially in nonvolatile memory (NVM) application, stress-induced leakage current (SILC) has become a major concern for the reliability of the tunneling dielectric, resulting from the generated interface trap due to the repeated high-field stress (Fowler-Nordheim stress)\cite{22, 23}. Therefore, it is important to understand impact of mechanical stress on trap-assisted gate leakage and dielectric breakdown.

1.2 How to Apply Strain to MOSFETs

This section describes two techniques used in commercial 90 and 65 nm logic technologies to introduce uniaxial stress into the Si channel. The techniques in production include high stress
tensile and compressive SiN capping layers and selective epitaxial SiGe deposited in recessed/raised source and drains.

The cost to implement process stressors is low at less than approximately 2-3% due to the comparatively few new process steps. Several process flows exist to introduce the epitaxial SiGe into a MOSFET[24-26]. The first consists of the steps shown in Fig. 1-1(a). The source/drain are etched creating a silicon recess. Next, SiGe (for p-channel) or SiC for n-channel is epitaxially grown in the source and drain. First generation embedded SiGe used ~17% Ge to create ~500MPa of channel stress. Future generations bring the SiGe closer to the channel and will likely increase the Ge concentration[25, 27]. Locating the SiGe closer to the channel will require reduced midsection thermal cycles to prevent any boron or Ge out-diffusion from the SiGe into the channel. To date a maximum of ~900MPa of stress has been created with embedded SiGe and impressive current improvements from 60-90% have been demonstrated on short devices (~35 nm)[25, 27].

Instead of embedded SiGe, dual stress liners (tensile and compressive capping layers) [28] are also being widely adopted[29, 30]. The advantages of a dual stress liner flow over epitaxial SiGe are reduced process complexity and integration issues. Recent progress in increasing stress of SiN films to ~3.0GPa for compressive and ~2.0GPa tensile [31] increases the attractiveness of this option. The capping films are introduced either as a sacrificial layer before source and drain anneal [28, 31, 32] or as a permanent layer post salicide (Fig. 1-1(b)). With 2-3GPa stress in the SiN, comparable performance to the first generation SiGe has been demonstrated. The process flow consists of a uniform deposition of a high tensile SiN liner post silicidation over the entire wafer followed by patterning and etching the film off p-channel transistors. Generally a thin etch stop layer is used under the liner to prevent any damage to the silicide. With highly selective
etches, the etch stop layer can be < 50Å which only slightly degrades the stress transfer into the channel. Next, a highly compressive SiN layer is deposited and this film is patterned and etched from n-channel regions.

Figure 1-1. Process architecture for strained Si (a) p-channel MOSFET process flow for the representative stacked gate transistor and TEM cross sectional view (source: Chipworks) and (b) dual stress liner with tensile and compressive silicon nitride capping layers.

In this work, instead of process-induced stress described above, four point wafer bending technique has been used to apply strain to MOS devices. Figure 1-2 and 1-3 show the fixture to simulate uniaxially strained MOSFETs as shown in figure 1-1.
Figure 1-2. Uniaxial four point wafer bending jig: two pairs of cylindrical rods are used and a sample is inserted between the pairs.

Figure 1-3. Uniaxial wafer bending jig. The displacement (d) is defined as d=d_i-d_f. (a) an unstressed sample (b) a stressed sample.
Such a bending structure has been well studied and a relation between the applied force and stress under uniform stress is given by [33]

\[
\sigma = Y \cdot \varepsilon = Y \cdot \frac{t \cdot d}{2a \left[ \frac{L}{2} - \frac{2a}{3} \right]}
\]  

Here, \(\sigma\) and \(\varepsilon\) are the stress and strain values at the center of the sample respectively, \(Y\) is Young’s modulus of Si along the stress direction, \(a = \frac{L - D}{2}\), and the deflection \(d\) is the vertical displacement between the upper and lower plates of the uniaxial jig when we apply stress. In Fig. 1.3, \(d\) is defined as \(d = d_i - d_f\), and actually measured by the change in micrometer graduations. The stress calibration of this setup has been done with both strain gauge and optical curvature measurements.

**1.3 Brief Description of Study**

The main purpose of our study is to understand the strain effects on Si and Ge MOSFET operations: channel mobility, gate tunneling currents (direct and trap-assisted tunneling mechanisms), threshold voltage, high k dielectric constant, and reliability related to dielectric breakdown.

The brief explanation of strain-induced mobility enhancement of Si MOSFETs is given and the physics behind some strained-Si experimental data is explored.

The strain effects on direct gate tunneling currents of Si and Ge MOSFETs are compared and explained. Based on experimental observations, qualitative analyses are made for both n- and p- MOSFETs. Next, deformation potential constants of Ge conduction band edge are extracted from the measured gate tunneling current under mechanical stress.
The impact of mechanical stress on gate leakage current based on trap-assisted conduction mechanism for Si MOS capacitors is discussed using constant voltage stressing and compared with strain-altered direct tunneling current.

Strain induced changes in gate leakage current and dielectric constant of nitrided Hf-silicate dielectric (HfSiON) Si MOS capacitors are explored with qualitative explanations.

Strain-induced threshold voltage shift models of different channel materials (Si and Ge) and gate stacks (Poly Si/SiO₂ and TiN/HfO₂) are discussed with theoretical modeling. Each component of model is analyzed thoroughly in conjunction with its underlying physical mechanism.

Impact of mechanical stress on time dependent dielectric breakdown of HfSiON is also investigated using controlled external applied mechanical stress and its mechanism is experimentally clarified.
CHAPTER 2
UNIAXIAL-STRESS-INDUCED CHANNEL MOBILITY ENHANCEMENT

2.1 Physics

When deciding on a strained-Si process flow, it is first necessary to comprehend the potential magnitude for electron versus hole mobility enhancement and whether the mobility enhancement results from reduced conductivity effective mass or scattering. Since the valence-band dispersion relationship for semiconductors depends on nearest neighbor atomic spacing, certain stress (in particular shear stress) warps the valence bands (although less so for conduction band but some warping for shear stress)[34]. The warping of the valence band provides dramatic changes to the constant-energy surfaces in $k$ space and can lead to large hole mobility enhancement via reduced conductivity mass in the channel direction. Mobility enhancement via reduced mass (as opposed to reduced scattering) is a key in nanoscale MOSFETs and often not appreciated. Only mobility enhancement from reduced mass (unlike reduced scattering) is maintained at the very short 15–20-nm channel lengths (35-nm gate length) devices currently in production[35, 36]. A strained-Si flow, which is scalable for multiple technology nodes, thus, needs to focus on reducing the hole conductivity mass with the goal of improving the n/p ratio from $\sim 2$ to $\sim 1$. Therefore, in this section, we will focus on strain-enhanced hole mobility from reduced conductivity mass. As a starting point, it is helpful to visualize the effect of strain on the valence-band constant-energy surfaces in $k$ space for bulk Si. Fig. 2-1 shows the surfaces obtained using six band $k \cdot p$ and band parameters in [37]. The strain-altered surfaces for the top two bands are shown at 1 GPa for the common stresses of interest: longitudinal compression on (001)[24, 25, 38, 39] and (110) hybrid wafer orientation [39] and biaxial tensile stress. [40] Note from the constant-energy surfaces in Fig. 2-1, the heavy and light hole bands lose their meaning and we label the bands (first, second, etc.) in this work. Some important differences in the band
structure under the various stresses at 500 MPa are summarized in Fig. 2-2 for the in-plane and out-of-plane conductivity effective masses and density of states at the band edge. We will refer to Fig. 2-2 in the next section during analysis of experimental data.

Before covering strain-altered hole mobility calculations, we will briefly cover a qualitative model for strain-enhanced electron mobility since the concepts are similar for electrons and holes. The important concepts to understand are strain-induced energy-level splitting, inversion-layer quantum confinement energy-level shifts, average mass change due to repopulation and band warping, two-dimensional (2-D) density of states, and interband scattering changes due to band splitting. All of these will be discussed in the following sections. A simple qualitative model is now presented to gain insight and to understand the more complex mathematics used elsewhere [11] and later in this work.

The electron mobility in bulk strained-Si along <110> direction is determined by occupation and scattering in the $\Delta_2$ and $\Delta_4$ valleys and can be expressed as

$$
\mu_{\text{eff}} = q \left( \tau_{\Delta_2} \frac{n_{\Delta_2}}{m_i} + \tau_{\Delta_4} \frac{n_{\Delta_4}}{m_i} \right) / (n_{\Delta_2} + n_{\Delta_4})
$$

(2-1)

where $q$, $n$, $\tau$, and $m$ are the electron charge, concentration, relaxation time, and conductivity mass in the MOSFET channel direction, respectively. Strain improves the mobility by increasing the electron concentration in the $\Delta_2$ valley. The repopulation improves the average in-plane conductivity mass (unstressed: $m_i = 0.19m_0$ versus $m_i = 0.98m_0$) and some further improvement is possible for stresses that warp the conduction valleys and lower $m_i$[34]. Reduced intervalley scattering by the strain-induced splitting between $\Delta_2$ and $\Delta_4$ plays some role (enhances long channel mobility) when the splitting becomes comparable or larger than the optical phonon energy. In addition to a low in-plane mass, a high out-of-plane mass for the $\Delta_2$ valley electron is
equally important since carrier motion perpendicular to the SiO₂ interface (taken as the z-direction in this paper) is quantized. This quantization in addition to strain alters the position of the energy levels. The quantization leads to bands becoming subbands since only discrete wave vectors $k_z$ are allowed. Including quantization, the total inversion-layer electron energy is given by discrete values of energy ($E_n$) added to the electron energy in the x- and y-directions (in the plane of the MOSFET)[41].

Figure 2-1. Hole constant energy band surfaces for the top band obtained from 6 band $k\cdot p$ calculations for common types of 1GPa stresses (a) unstressed, (b) biaxial tension, (c) longitudinal compression on (001) wafer, (d) longitudinal compression on (110) wafer. (Note significant differences in stress induced band warping altering the effective mass).
Each step in energy is called a subband with $E_n$ the energy of the bottom of the subband. As an example, self-consistent solution of Schrödinger and Poisson equation for 500 MPa of uniaxial tensile stress and an inversion-layer vertical field of 1 MV/cm gives the energy levels, as shown in Fig. 2-3. Since the subband separation is greater than $kT$, nearly all the electrons in most cases occupy the bottom two subbands [ground state $n = 0$ typically called $E_o$ (from $\Delta_2$) and $E_{o_1}$ (from $\Delta_4$)]. The ground state energy is significantly lower for the $\Delta_2$ valleys because of the higher quantization mass ($\Delta_2 : m_z = 0.98m_0$ versus $\Delta_4 : m_z = 0.19m_0$) which leads to increased splitting between the bottom two subbands and confinement and strain splitting being additive (for the common biaxial and uniaxial tensile stress). Note, the strong confinement in an MOSFET shifts the energy levels more than the moderate $\sim$ 500-MPa stress typically used in present-day production logic technologies. Thus, a high out-of-plane mass in the bottom subband (top subband for holes) is an important requirement for the strain altered band structure.

Lastly, in addition to a low in-plane and high out-of-plane effective mass, a high in-plane mass perpendicular to the channel direction is also important. The density of states per unit area for the quantized system is $2/(2\pi)^2 (\sqrt{m_x m_y / m_o}) dk_x dk_y$, which results in the density-of-states mass approximated by $m_{DOS}^{2D} = \sqrt{m_x m_y}$. Though strain does not significantly alter the electron subband density of states, as discussed next, a high $m_{DOS}^{2D}$ will be shown to be important for maintaining a hole concentration in the top subband.
Figure 2-2. Summary of key valence band parameters for top and second band for bulk Si under 500MPa stress. The conductivity and density of states effective mass is listed at Gamma point. Uniaxial compression is longitudinal along <110> channel direction. (Note significant differences for in-plane, out-of-plane and density of states masses).

Similar to strained enhanced electron mobility, hole mobility in an inversion layer can qualitatively be described as resulting from occupation and scattering in the top two bands

\[ m^* = \frac{\hbar^2}{d^2 \varepsilon} \quad m_{DOS}^{2D} = (m_x m_y)^{1/2} \]

However, hole transport is more complicated since strain significantly warps the valence band (as seen in Fig. 2-1) altering both the in and out-of-plane mass and \( m_{DOS}^{2D} \). Further, the mass changes with stress and is not constant in k space. As follows from the previous discussion on strain enhanced electron transport, an advantageous strain for holes needs to warp the valence band to create both a low in-plane and high out-of-plane mass and if possible a large mass in the plane of the MOSFET perpendicular to the channel direction (creates a large \( m_{DOS}^{2D} \)). Band calculations and measurements to be discussed next show uniaxial stress warps the valence band
creating most of these features. The strain altered band structure is calculated using 6 band $k\cdot p$, including quantum confinement via a self-consistent solution of Schrödinger and Poisson equation\[41, 42]. The mobility is calculated by a linearization of the Boltzman transport equation. The numerics confirm that the simple qualitative model captures much of the essential physics for understanding the physical mechanisms for mobility enhancement.

![Diagram](image.png)

Figure 2.3. Conduction valley energy level splitting under 500MPa of longitudinal uniaxial tensile stress: bulk and MOSFET inversion layer (1MV/cm). Note, energy level splitting from inversion layer confinement is larger than strained.

### 2.2 Strain Enhanced Hole Mobility

In a MOSFET, the 2-D surface confinement in the inversion layer also shifts the valence bands and the conduction valleys\[11, 43]. Whether the confinement-induced shift adds to or reduces (cancels) the strain-induced splitting simply depends on the magnitude of the out-of-plane masses (valence-band splitting is more complicated but this simple model captures the essential physics). Bands or valleys with a “light” out of plane mass will shift more in energy
relative to bands with a “heavy” mass (similar to the increasing ground state energy of a quantum well as the particle mass decreases). Hence, when the top most occupied band (or valley) has a lower out-of plane mass compared to the next occupied band, the splitting is reduced or lost with surface confinement. Fig. 2-4 pictorially shows the valence-band energy-level shift with confinement for both uniaxial and biaxial stress. $E_{\text{top}}$ represents the top band with large out-of-plane mass for uniaxial stress and small for biaxial stress (relative to the second band with masses given in Fig. 2-2). Hence, the top band will have a small shift in energy due to confinement for uniaxial stress but large shift for biaxial stress. $E_{\text{second}}$ represents the second band.

As seen in Fig. 2-4, the stress-induced band splitting ($E_{\text{top}} - E_{\text{bottom}}$) increases for uniaxial stress but decreases for biaxial tensile stress. Thus, although strain favors occupation of the top band for both types of stresses, confinement favors occupation of the top band for uniaxial compressive stress and the second band for biaxial tensile stress. The net band splitting from strain and confinement is additive for uniaxial compressive stress but subtractive for biaxial tensile stress. The competing effects of strain and surface confinement on the band splitting is the reason for the loss in mobility enhancement in biaxially strained-silicon p-MOSFETs at high electric fields. The undesirable light out of-plane mass created by biaxial tensile stress occurs in other material systems, such as Ge and III-V materials, and presents a fundamental problem in using this type of strain in inversion layer MOSFETs (dominant device type due to superior scaling properties).

To date, unlike biaxial stress [6], limited data exist for the maximum mobility possible for uniaxial stress. We used a set of scattering parameters that fit the experimental data for hole mobility enhancement under biaxial tensile stress[11]. The calculations include acoustic and optical phonon and surface roughness scattering. This set of scattering parameters shows that the
dominant mechanism responsible for biaxial tensile-stress mobility enhancement (at large stress) is reduced optical phonon scattering. Acoustic phonon scattering is only slightly altered due to the changes in the density of states. Surface roughness scattering is slightly changed by stress but uncertainty exists in the literature[11, 44, 45] and more work is needed especially for the (110) substrate. The calculations for biaxial stress are consistent with the previous work [11], although in this work, Schrödinger’s and Poisson’s equations are solved self-consistently. The model fit to the biaxial tensile-stress experimental data is shown in Fig. 2-5.

Figure 2-4. Valence energy band splitting calculated using 3 different models versus inversion charge density for longitudinal compression and biaxial tension stress. Note all models show the net band splitting from strain and confinement is additive for uniaxial compressive stress but subtractive for biaxial tensile stress.

Using the same scattering parameters, mobility enhancement for uniaxial stress on (001) and (110) wafers is calculated, as shown in Fig. 2-5, and compared to uniaxial stress data from from three references[6, 24, 46]. The mobility calculations use the full sixband subband structure
and Kubo–Greenwood linearization of the Boltzmann equation[16]. Where data exist (0 to \( \sim \) 600 MPa for uniaxial stress), the model shows good agreement. The maximum predicted Si inversion-layer hole mobility enhancement is estimated to be \( \sim 4 \) times higher for uniaxial stress on (100) wafer and \( \sim 2 \) times higher for biaxial stress on (100) wafer and for uniaxial stress on a (110) wafer. The larger maximum mobility enhancement on a (001) wafer results from the high density of states in the top band, as discussed previously but scattering differences also play a role. Scattering differences for various substrate orientations and stresses should be expected as captured in analytical scattering expressions.

First for acoustic phonon in the two dimensional inversion layer, the scattering time \( \tau_{ac} \) is expressed as \([11, 44, 45, 47]\)

\[
\frac{1}{\tau_{ac}} = \frac{D_{ac}^2 b_{mn} m_{DOS}^2 k_B T}{\hbar^3 \rho u_l^2} \propto (m_{DOS}^{2D}) \tag{2-4}
\]

where \( D_{ac} = 3.1eV [48] \) is the acoustic deformation potential constant of the valence band, \( m_{DOS}^{2D} \) is the density-of-state effective mass, \( \rho \) is the density, and \( u_l \) is the longitudinal sound velocity. The constant \( b_{mn} = \int_{0}^{\infty} dz |\phi_k^m(z)|^2 |\phi_k^n(z)|^2 \) is the form factor which defines the transition from initial state \( m \) to final state \( n \), and \( 2/b_{mn} \) represents the effective well width for the \( m \)-th subband.

Since the acoustic phonon energy is very small compared to the subband splitting, the acoustic phonon scattering mainly occurs via intraband scattering. Thus, stress-induced band splitting only weakly affects the acoustic phonon scattering time[13, 49]. As seen from Eq. 2-4, an increased density-of-states will decrease the acoustic phonon scattering time which is proportional to \( m_{DOS}^{2D} \). For uniaxial stress on a (100) wafer with a high density of states in the top
band, this slight negative effect on mobility (at least for uniaxial stress on (001) wafer) is offset
by the high hole density in the top band having a light conductivity mass in the channel direction.
Also, a large out-of-plane mass increases the acoustic phonon scattering time (decreases
scattering rate) since it decreases the effective well width (important for the high initial mobility
on (110) wafer).

Second, the optical phonon scattering time \( \tau_{op} \) is \([13, 45, 47, 49]\)

\[
\frac{1}{\tau_{op}} = \frac{m_{DOS}^2 b_{mn} D_{op}^2}{2 \rho \omega_\Theta \hbar^2} \left[ N_q \frac{1 - f(\varepsilon + k_\Theta - \Delta E)}{1 - f(\varepsilon)} + (N_p + 1) \frac{1 - f(\varepsilon - k_\Theta - \Delta E)}{1 - f(\varepsilon)} \right] \tag{2-5}
\]

where \( \Delta E \) is the band splitting energy, \( D_{op} = 10.5 \times 10^8 \text{ eV/cm} \) [50] is the optical deformation
potential constant of the valence band, \( f(\varepsilon) \) is Fermi-Dirac distribution function at energy \( \varepsilon \),
\( \Theta = 735 K \) is the Debye temperature and \( \hbar \omega_\Theta = 63 \text{ meV} \) is the optical phonon energy[47],
and \( N_q = [\exp(\hbar \omega_\Theta / k_\Theta T) - 1]^{-1} = [\exp(\Theta / T) - 1]^{-1} \) is the number of phonons from Bose-Einstein
statistics. Hole intervalley scattering is not significantly reduced for stress < 1GPa since the
band splitting is less than the optical phonon energy (60meV). Band splitting greater than
60meV (stress > 1GPa) is necessary to appreciably suppress intervalley phonon scattering. Also,
the correlation between the topmost two subbands, \( b_{mn} \) under uniaxial stress is smaller due to the
higher band splitting (strain and confinement being additive) and, therefore, the scattering rate is
less than that for biaxially stressed devices. Furthermore with the high out-of-plane mass
cauing larger subband splitting, the interband optical phonon scattering rate is less on (110) vs.
(001) devices.

Third, the surface roughness scattering relaxation time \( \tau_{sr} \) [11, 45] can be expressed as

\[
\frac{1}{\tau_{sr}} = \frac{q^2 E_{sy}^2 m_{DOS}^2}{2 \pi \hbar^3} \int_0^{2\pi} S(q) (1 - \cos(\theta)) \, d\theta \tag{2-6}
\]
where $E_{\text{eff}}$ is the transverse effective electric field in the inversion layer and

$$S(q) = \frac{\pi L^2 \Delta^2}{\left(1 + q^2 L^2 / 2\right)^2}$$

is the power spectrum of the roughness at the interface. $L$ is the correlation length ($L = 2.6\text{ nm}$) and is the average step height ($\Delta = 0.4\text{ nm}$). Differences in $\tau_{sr}$ for various stresses and substrates result from changes in the density-of-states and location of the inversion layer charge from the SiO$_2$ interface. There is also a fair amount of uncertainty in surface roughness scattering particularly on a (110) wafer since the commonly used universal mobility vs. effective oxide field $E_{\text{eff}}$ applies only to the (100) substrate[51, 52]. However, one can conclude since the effective well width depends heavily on the out-of-plane effective mass for each subband, the top subband for a (110) device having a very large out-of-plane effective mass (see Fig. 2-2), will lead to carriers significantly closer to the interface and greater surface roughness scattering.

![Figure 2-5](image)

Figure 2-5. Calculated and experimental data for longitudinal compressive and biaxial tensile stress enhanced mobility vs. stress (Biaxial stress= $\sigma_X+\sigma_Y$). Note, the maximum predicted Si inversion layer hole mobility enhancement is estimated to be ~4 times higher for uniaxial stress on (100) wafer and ~2 times higher for biaxial stress on (100) wafer and for uniaxial stress on a (110) wafer.
CHAPTER 3
STRAIN EFFECTS ON GATE LEAKAGE CURRENTS OF GERMANIUM (Ge) MOS DEVICES

3.1 N-Type Metal-Oxide-Semiconductor Field Effect Transistors

3.1.1 Ge Conduction Band Edge Shift and Splitting

Strain-induced energy shift and splitting alters the gate tunneling current. The Ge conduction band minima are located at the equivalent gamma (L) points[53]. Fig. 3-1 shows the conduction band constant energy ellipsoids around the L point. Since the centers of the diagonally opposite half ellipsoids are one wave vector apart, the 8 half ellipsoids can be combined into four equivalent full ellipsoids([111],[11$ar{1}$],[1$ar{1}$1],[$ar{1}$11]).[54] Due to the major axis along the Λ or [111] direction, uniaxial stress along [100] shifts but does not split the 4 ellipsoids, while splitting occurs for stress along [110], as shown in Fig. 3-2(b) and (c)[55]. Fig. 3-2(a) shows a schematic drawing of the direct tunneling process from the Λ sub-bands ($E_\Lambda$) in the inversion layer for uniaxial tensile stress. The strain-induced shift of the conduction band edge is given by [2, 56]

$$\Delta E_C^i(\sigma) = \Xi_d \left( Tr(e_{ij}) \right) + \Xi_u (\hat{k} \cdot e_{ij} \cdot \hat{k})$$

(3-1)

where $\Xi_d$ and $\Xi_u$ are the dilation and shear deformation potential constants of the conduction band, respectively, and $i$ denotes the various valleys. $Tr(e_{ij})$ is the trace of the strain tensor ($e_{ij}$)[57, 58] and $\hat{k}$ and $\sigma$ are a unit vector in reciprocal space and applied stress, respectively. In Fig. 3-2(b), stress along [100] causes a hydrostatic conduction band edge shift ($\Delta E_{\text{Hydro}}$) resulting in an altered HfO$_2$/Ge conduction band offset. The hydrostatic strain-induced conduction band edge shift can be expressed in terms of the deformation potentials [53] and is given by
\[
\Delta E^{\text{Hydro}}(\sigma) = \Xi^{\text{Hydro}} Tr(\epsilon_{ij}) = (\Xi_d + \frac{1}{3} \Xi_u) Tr(\epsilon_{ij}) \quad (3-2)
\]

where \(\Xi^{\text{Hydro}}\) is the hydrostatic deformation potential constant. Unlike stress along [100], stress along [110] leads to band splitting between the (110) plane and (\overline{1} 10) plane ellipsoids. The band splitting of each conduction band edge is given by [55]

\[
\Delta E^{\text{Shear}}_{\Lambda(110)}(\sigma) = \frac{1}{6} S_{44} \Xi_u \sigma_{<110>}
\]

\[
\Delta E^{\text{Shear}}_{\Lambda(\overline{1}10)}(\sigma) = -\frac{1}{6} S_{44} \Xi_u \sigma_{<110>}
\]

where \(\sigma_{<110>}\) is the uniaxial stress along [110] direction (positive for tensile stress) and \(S_{44}\) is the elastic compliance constant. A schematic drawing of the [110] stress effect on \(E_\Lambda\) is shown in Fig. 3-2(c).

Figure 3-1. Conduction-band constant energy ellipsoids are centered at the L point, and the major axis of eight half ellipsoids are along \(\Lambda\) or [111] direction. Out-of-plane effective mass and \(E_{\text{eff}}\) are defined along [001] direction.[54, 59] Note half of ellipsoids belong to (110) plane while the rest of ellipsoids belong to (\overline{1}10) plane.
Figure 3-2. Schematic band diagrams for direct electron tunneling from inversion layer in Ge MOS device. (a) Conduction band offset between HfO2 and Ge is from reference.[59] (b) Stress along [100] raises Λ energy level resulting from hydrostatic strain-induced energy level shift (ΔE_{Hydro}). (c) Stress along [110] causes shear strain-induced energy level splitting (ΔE_{Shear}) between (110) plane Λ valley [Λ(110)] and Λ(1̅10). Λ(110) energy level is raised while Λ(1̅10) energy level is lowered. Note ΔE_{Hydro} is additive for ΔE_{Shear}.

3.1.2 Theoretical Model

From the change in the stress altered tunneling current, the Ge deformation potential can be extracted[18]. The electron direct tunneling current density (I_c) can be expressed in terms of the electron charge density (n_i) and lifetime (τ_i) of each energy sub-band in the quantization layer, which are functions of stress,

\[ I_c(\sigma) = q \sum_i \frac{n_i(\sigma)}{\tau_i(\sigma)} \]  

(3-5)
where the subscript \( i \) denotes each sub-band belonging to the \( \Lambda \) valley of Ge. Above the threshold voltage, most electrons occupy each ground state for the \( \Lambda(110) \) and \( \Lambda(\bar{1}10) \) valleys.

The relative change of gate tunneling current due to the applied stress can be expressed as [18, 60]

\[
\frac{\Delta I_G(\sigma)}{I_G(0)} \approx A(0) \frac{\Delta n_{\Lambda(110)}(\sigma)}{n_{\Lambda(110)}(0)} - B(0) \frac{\Delta \tau_{\Lambda(110)}(\sigma)}{\tau_{\Lambda(110)}(0)} - C(0) \frac{\Delta \tau_{\Lambda(\bar{1}10)}(\sigma)}{\tau_{\Lambda(\bar{1}10)}(0)}
\]

(3-6)

where

\[
A(0) = \frac{-1 + \tau_{\Lambda(110)}(0) / \tau_{\Lambda(110)}(0)}{n_{\Lambda(110)}(0) / n_{\Lambda(110)}(0) + \tau_{\Lambda(110)}(0) / \tau_{\Lambda(110)}(0)}
\]

\[
B(0) = \frac{n_{\Lambda(110)}(0) / n_{\Lambda(110)}(0)}{n_{\Lambda(\bar{1}10)}(0) / n_{\Lambda(\bar{1}10)}(0) + \tau_{\Lambda(\bar{1}10)}(0) / \tau_{\Lambda(\bar{1}10)}(0)}
\]

\[
C(0) = \frac{n_{\Lambda(\bar{1}10)}(0) / n_{\Lambda(\bar{1}10)}(0)}{n_{\Lambda(110)}(0) / n_{\Lambda(110)}(0) + \tau_{\Lambda(110)}(0) / \tau_{\Lambda(110)}(0)}
\]

The charge density of electrons in the sub-bands is calculated from the self-consistent solution of the Schrödinger and Poisson equations[61]. The effective mass approximation is used for Ge[54, 62]. For a (100) surface oriented Ge device, the out-of-plane effective mass \( (m_n^*) \) can be defined as \( 3m_n m_t / (2m_t + m_n) \), where \( m_t \) and \( m_n \) are the longitudinal and transverse effective masses of the \( \Lambda \) valley, respectively \( (m_t = 1.64m_n \text{ and } m_n = 0.08m_0)[54] \). Once the basic Hamiltonian has been identified, the electron charge density is calculated by summing the contributions of each sub-band in the \( \Lambda \) valley. The electron charge density of each sub-band can be described by [63]

\[
n_i = \left( \frac{kT}{\pi \hbar^2} \right) g m_n^* \ln(1 + \exp\left( \frac{E_F - E_i}{kT} \right))
\]

(3-7)
where $k$ is the Boltzmann constant, $T$ is room temperature, 300K, $E_F$ is the Fermi energy, $m_d^*$ is the density of state electron effective mass in the $\Lambda$ valley ($m_d^* = 0.3 \, m_0$) [59], and $E_i$ and $g$ are the energy level of the $i_{th}$ sub-band and the degeneracy of the $\Lambda$ valley, respectively. Based on the finite difference method [61], the self consistent solution provides the charge density and the corresponding sub-band energy levels. The tunneling lifetime of the electron in each sub-band is approximated by [64]

$$\frac{1}{\tau_i} = \frac{T(E_i)}{\int \frac{1}{\sqrt{2m_n^*/[E_i - E_C(x)]}} dx}$$  \hspace{1cm} (3-8)$$

where $E_C(x)$ is the edge of the conduction band of Ge and $T(E_i)$ is the transmission probability calculated with a modified WKB approximation[63, 64]. An $E(k)$ dispersion proposed by Franz, which is consistent with two bands separated by an energy gap ($E_g^{HfO_2} = 5.8eV$), is used for the $E$-$k$ dependence of HfO$_2$ [65, 66] and an oxide effective mass, $m_{ox} = 0.18 \, m_0$ is used for this calculation[59]. The validity of the WKB approximation for high-$k$ dielectrics has been shown elsewhere[62].

### 3.1.3 Experimental Set-Up and Results

Four-point bending is used to apply uniaxial stress along the [100] and [110] directions on (100) surface oriented Ge MOS samples.[13] The Ge MOS devices consist of TiN metal gate on top of 3.0 nm HfO$_2$ gate dielectric on p-well substrate. Large area $10^{-4}$ cm$^2$ Ge MOS devices are used to eliminate the fringe leakage components. The electron gate tunneling current from the Ge substrate to gate is measured under inversion with positive gate bias and substrate grounded using a Keithley 4200 DC characterization system.
Fig. 3-3 shows the [100] stress-altered electron gate tunneling current for different gate biases. The tunneling currents increase with applied tensile stress. Unlike Si, stress along [100] does not result in any change in the average conductivity effective mass via electron repopulation—the inset shows the tunneling barrier height reduced by $\Delta E^{\text{Hydro}}$.

Fig. 3-4 plots the change in the electron gate tunneling current for mechanical stress along [110]. The change in the tunneling current for stress along [110] is slightly smaller than for stress along [100].

It is instructive to compare [110] tensile stress altered tunneling currents for (100) surface oriented Si and Ge n-MOS devices which is shown in Fig. 3-5. The trend for Si MOS devices can be found in several recent publications all showing similar results[19, 67]. An opposite stress dependence is observed with an increase in tunneling current for Ge and a decrease for Si. The key difference in the gate tunneling mechanism between Si and Ge devices is due to the position of conduction band minimum (X for Si and L for Ge)[54].

To understand the difference, strain effects on the conduction sub-band structure of Si and Ge are illustrated in Fig. 3-6. For Si, due to different out-of-plane effective masses of $\Delta_2$ valley (0.92$m_0$) and $\Delta_4$ valley (0.19$m_0$), electron repopulation between these two valleys plays an important role in strain-altered gate leakage current[18]. The decrease in the gate tunneling current of Si results from repopulation into the $\Delta_2$ sub-band with a larger out-of-plane effective mass. In addition, the $\Delta_2$ sub-band shift leads to an increased barrier height. In Ge, the out-of-plane effective masses of the 8-fold degenerate $\Lambda$ valleys are the same (0.12$m_0$)[54].

Since $\Lambda\langle 110 \rangle$ and $\Lambda\langle 110 \rangle$ have the same out-of-plane effective mass and barrier height (without the applied stress), $\tau_{\Lambda\langle 110 \rangle}(0)$ is identical to $\tau_{\Lambda\langle 110 \rangle}(0)$, resulting in $A(0)$ in (6) equal to zero. The
degeneracy of \( \Lambda(110) \) and \( \Lambda(\bar{1}10) \) also results in \( n_{\Lambda(110)}(0) = n_{\Lambda(\bar{1}10)}(0) \) and \( B(0) = C(0) \) in (3-6).

Thus for Ge, \( \Delta \tau(\sigma)/\tau(0) \) (second and third terms in (3-6)) is the dominant effect which is altered via strain by changes in the HfO\(_2\) to Ge barrier height, as shown in Fig. 3-2(c). At lower gate bias, the relative change of \( \tau \) as a function of stress is larger, based on (3-8). Therefore, the relative change of stress altered gate leakage current at lower gate bias is larger than at higher gate bias, consistent with the experimental data in Fig. 3-3 and 3-4. Also, we observe, in Fig. 3-5, the increase of the gate leakage current in Ge device is approximately 3 times smaller than the decrease in the Si device.

![Figure 3-3. The [100] tensile stress-altered gate tunneling current for Ge MOS device under different gate biases. Current is increased due to reduced barrier height resulting from \( \Delta E^{\text{Hydro}} \). The inset represents schematic band diagram of sub-band in inversion with no stress and tensile stress along [100].](image)

Figure 3-3. The [100] tensile stress-altered gate tunneling current for Ge MOS device under different gate biases. Current is increased due to reduced barrier height resulting from \( \Delta E^{\text{Hydro}} \). The inset represents schematic band diagram of sub-band in inversion with no stress and tensile stress along [100].
Figure 3-4. [110] tensile stress-altered gate tunneling current of Ge MOS device under different gate biases. Current is increased due to reduced barrier height of electrons in $\Lambda(110)$ energy level. The inset shows schematic band diagram with strain-induced sub-band splitting between $\Lambda(110)$ and $\Lambda(\overline{1}10)$ sub-bands.

Figure 3-5. The [110] tensile stress-altered electron gate tunneling current of Ge and Si devices at inversion charge of $10^{13}/cm^2$, where 1.2 V and 0.6 V gate biases are applied for Si and Ge MOS devices, respectively.[68] Si data are from reference [19] (measured from n-MOSFETs with N+ poly gate and SiO$_2$ dielectric). Note that strain-altered current is increased in Ge while decreased in Si due to the different position of conduction band minimum (X for Si and L for Ge).[54]
3.1.4 Extraction of Conduction Band Deformation Potentials

In this section, the conduction band deformation potentials of Ge are extracted from the strain-altered gate tunneling current. Since stress along [100] only causes a \( \Delta E^{\text{Hydro}} \) shift and no shear band splitting on the \( \Lambda \) valley structure, \( \Delta E^{\text{Hydro}} \) can be determined from the data in Fig. 3-3.

To extract \( \Xi^{\text{Hydro}} \) and capture the change in the tunneling current under the applied stress in the full range of gate voltages, Fig. 3-7 shows the change of slope in Fig. 3-3 or

\[
\frac{d[\Delta I_G(\sigma)/I_G(0)]}{d\sigma} \text{ versus applied gate bias.}
\]

\( \Xi^{\text{Hydro}} \) is used to fit the experimentally measured data[2, 53]. To illustrate the goodness of the model fit, maximum deviation curves are plotted in which \( \Xi^{\text{Hydro}} \) ranges from 1.2 to 1.5 eV. The model fits well with the data over the range of gate
bias from 0.5V to 1.1V. The same procedure is employed for stress along [110] to determine the two deformation potentials of $\Xi_d$ and $\Xi_u$. The slope of Fig. 3-4 was extracted and compared with fitting models over the entire gate bias range (0.5~1.1 V) in Fig. 3-8. The obtained values of deformation potential constants ($\Xi_d$ and $\Xi_u$) are compared with hydrostatic deformation potential constants ($\Xi_{\text{Hydro}}$) from stress along [100], based on $\Xi_{\text{Hydro}} = \Xi_d + \frac{1}{3} \Xi_u$ [53]. The best fitting values of $\Xi_d$ and $\Xi_u$ in Fig. 3-8 are in good agreement with $\Xi_{\text{Hydro}}$ in Fig. 3-7. The obtained deformation potentials ($\Xi_d = -4.3 \pm 0.3$ and $\Xi_u = 16.5 \pm 0.5$ eV) listed in Table 3-1 are close to the theoretical values by Fischetti et al. ($\Xi_d = -4.43$ and $\Xi_u = 16.8$ eV) [17].

Figure 3-7. Change in slopes ($d[I_G(\sigma)/I_G(0)]/d\sigma$) versus gate voltage with 95% confidence error bars for tensile stress along [100]. Best fits (① and ②) for the entire data set occur for $\Xi_{\text{Hydro}} = 1.3$ and 1.4 eV. Maximum deviations (③ and ④) from the data occur for $\Xi_{\text{Hydro}} = 1.2$ and 1.5 eV.
Figure 3-8. Change in slopes \( \left( \frac{d[\Delta I_G(\sigma)/I_G(0) / d\sigma]}{d\sigma} \right) \) versus gate voltage with 95% confidence error bars for tensile stress along [110]. Best fits (2, 3, and 4) for the entire data set occur for \( \Xi_d = -4.2 \) to -4.4 and \( \Xi_u = 16.5 \) to 16.8 eV. Maximum deviations (1 and 5) from the data set occur for \( \Xi_d = -4.1 \) and -4.5 and \( \Xi_u = 17.0 \) and 16.0 eV, respectively.

Table 3-1. Dilation (\( \Xi_d \)) and shear (\( \Xi_u \)) deformation potentials extracted from gate tunneling current of Ge MOS device under tensile stress along [100] and [110]. Comparison is made with previous theoretical and experimental results.[17, 53, 55, 69, 70] All quantities are in eV.

<table>
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<tr>
<th></th>
<th>Present Work</th>
<th>Literature</th>
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<tbody>
<tr>
<td>( \Xi_d )</td>
<td>-4.3 ± 0.3</td>
<td>-2, -3, -4.3, -6.6, -10.5, -12.3</td>
</tr>
<tr>
<td>( \Xi_u )</td>
<td>16.5 ± 0.5</td>
<td>15.1, 15.9, 16.2, 16.5, 16.8, 17.3, 19.3</td>
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3.1.5 Summary

In summary, measurement of the electron gate leakage currents under two different mechanical stress conditions provides a method to extract the Ge conduction band deformation potentials. For uniaxial tensile stress along [110] and [100], the change in gate leakage current for Ge is measured to be 3 times smaller than that of Si n-MOS device and opposite in sign. This reverse behavior occurs because tensile stress for Si causes electron repopulation into \( \Delta_2 \).
increasing the out-of-plane effective mass while, in Ge, a reduced tunneling barrier is the
dominant mechanism, resulting from the hydrostatic shift of the conduction band edge. Although
the hydrostatic shift of Si is larger than that of Ge, its contribution to the strain-altered gate
leakage current change in Si is not as critical as in Ge due to the primary role of electron
repopulation via shear strain-induced band splitting in Si.

3.2 P-type metal-oxide-semiconductor field effect transistors

3.2.1 Experimental Set-Up

Three different kinds of samples are used in this work: (1) Ge <110> channel/(100) surface
p-MOSFETs with TiN metal gate and 3.0 nm HfO2/interlayer (IL) stacked dielectric fabricated
on n-type Ge substrate, (2) Si <110> channel/(100) surface p-MOSFETs with p+ poly-Si gate
and 1.3 nm SiO2 fabricated on n-well, and (3) Si MOS capacitors with TaN gate and 2.5 nm SiO2
fabricated on p-type Si substrate.

Conventional carrier separation method is used to measure the electron and hole tunneling
currents for the Ge and Si p-MOSFETs[71-73]. Fig. 3-9 is a schematic illustration of carrier
separation and 4-point wafer bending. The electron (from the gate) and hole (from the substrate)
tunneling currents are measured with source and drain physically tied to ground and the gate
negatively biased. Mechanical uniaxial stress is applied longitudinal to the <110> channels of Ge
and Si MOSFETs. The hole and electron tunneling currents are measured using a Keithley 4200
dc characterization system. Devices with different areas are measured and the current density
exhibits no area dependence, which indicates a negligible edge tunneling effect[74]. To measure
the magnitude of metal gate work-function shift under mechanical stress, Si MOS capacitors
have been used for C-V measurements with HP 4294 to measure flat band voltage shift ($\Delta V_{FB}$).
3.2.2 Stress Altered Hole Tunneling Currents of Ge and Si p-MOSFETs

Fig. 3-10(a) shows the carrier separation for Ge and Fig. 3-10(b) for Si p-MOSFETs. For both type of devices, the gate current, \( I_G \), is nearly identical with the source/drain current, \( I_{S/D} \), showing hole tunneling current from inversion layer is the dominant mechanism consistent with previous studies[64, 76, 77]. In Ge device, \( I_{S/D} \) is lower and the portion of \( I_{SUB} \) in \( I_G \) is larger than that in the Si device due to 1) HfO₂ dielectric with larger equivalent oxide thickness and 2) TiN metal electrode with free electrons[73, 77].

Fig. 3-11 shows the relative hole gate tunneling current change in Ge and Si p-MOSFET as a function of applied external mechanical stress. Theoretical calculation for the stress altered hole tunneling current, based on the self-consistent solution to the Poisson and Schrödinger’s equation for Si and Ge, are also shown in Fig. 3-11[20]. A six band \( k \cdot p \) approximation is used for the calculation of charge density and out-of-plane effective mass[42]. The hole tunneling probability, based on a WKB approximation,[64, 65] is used to fit the experimental data. The
The measured data can be understood from strain altered out-of-plane effective mass and hole repopulation between the top two sub-bands (E₁ and E₂)[80]. Fig. 3-12 shows a schematic drawing of the hole tunneling process from E₁ and E₂ and the strain induced sub-band energy shift. For both Ge and Si, the strain altered out-of-plane hole effective masses of E₁ and E₂ are observed to be fairly constant at the Γ point for stress < ~200 MPa and listed in Fig. 3-12(c)[13]. The band splitting at low stress and moderate to high gate bias is set by confinement and with E₁ having larger strain altered out-of-plane effective mass becomes the top band[80]. Applied tensile stress causes the E₁ to E₂ band splitting to decrease resulting in hole repopulation from E₁ to E₂, as shown in Fig. 3-12(b)[19, 20]. For tensile stress, the hole tunneling current enhancements of both Ge and Si devices result from hole repopulation into E₂, which has a smaller tunneling barrier height (\( \phi_{B,2} < \phi_{B,1} \)) and out-of-plane effective mass (\( m_{E,2}^z < m_{E,1}^z \)).

Compared to Si, the larger increase in strain altered hole tunneling current of Ge can be explained by larger 1) stress induced valence band edge splitting and 2) change in hole tunneling attempt frequency.
The hole repopulation can be quantified from the valence band edge splitting ($\Delta E_v$) as a function of stress\cite{81}. Fig. 3-13 shows the valence band edge splitting in Ge and Si under no confinement, based on $\Delta E_v$ as follows: \cite{55}

\[
\Delta E_v = \frac{1}{2} \left[ b^2 (S_{11} - S_{12})^2 + 3\left( d \frac{d}{2\sqrt{3}} S_{44} \right)^2 \right]^{1/2} |\sigma_{[110]}| \quad (3-9)
\]

where $\sigma_{[110]}$ is the applied longitudinal stress, $S_{ij}$ is the elastic compliance constants and $b$ and $d$ are deformation potentials of valence band from Ref. \cite{17}. Note that $\Delta E_v$ of Ge is 1.5 times larger than that of Si, causing more hole repopulation in Ge.

Fig. 3-14 plots the hole charge density in the top three sub-bands (E1, E2, and E3) as a function of stress for a) Ge and b) Si, respectively. Note in this calculation, since the total charge density is approximately constant with applied stress, we use $\Delta N_1 + \Delta N_2 + \Delta N_3 = 0$, where $N_i$ is hole charge density of each sub-band\cite{20}. Since the 2D density of states of both Si and Ge do not change significantly at low stress (<200MPa)\cite{82}, hole repopulation from E1 to E2 mainly results from valence band edge splitting as seen in Fig. 3-13, leading to the larger increase in the hole tunneling of Ge, relative to Si.

The inversion-layer hole attempt frequency on gate dielectric barrier is also different for E1 and E2\cite{19}. Due to the larger mass ratio of Ge ($E_1/E_2=0.12/0.05$), compared to that of Si ($0.26/0.21$), the relative change of stress altered hole tunneling attempt frequency in Ge is larger, resulting in a larger increase in hole tunneling current for Ge.
Figure 3-10. Carrier separation measurement of a) Source/drain ($I_{SD}$) and substrate tunneling current ($I_{SUB}$) as a function of gate voltage ($V_G$) for Ge p-MOSFET. b) $I_{SD}$ and $I_{SUB}$ as a function of $V_G$ for Si p-MOSFET.
Figure 3-11. Relative change in $I_{S/D}$ of Si and Ge p-MOSFET as a function of stress. Symbols and lines are measured data and modeling, respectively. The magnitude of hole tunneling current change in Ge is approximately 4 times larger than that in Si.

Figure 3-12. Schematic band diagram for the hole gate tunneling current in a p-MOSFET on a (100) wafer. a) each subband has different tunneling barrier height. b) $E_1$ and $E_2$ subbands shift under stress results in hole repopulation into $E_2$ sub-band, which has lower tunneling barrier height and smaller out-of-plane effective mass. c) Strain altered out-of-plane effective mass for each sub-band is listed in table.
Figure 3-13. Valence band edge splitting of Ge and Si under tensile stress along [110] (not including confinement). Ge has larger valence band edge splitting than Si.
Figure 3-14. Charge density versus applied stress for the top (E₁), bottom (E₂), and third sub-bands (E₃) at an inversion charge density of $3.5 \times 10^{13} / \text{cm}^2$ for (a) Ge and (b) Si, respectively. Strain altered out-of-plane effective mass of each sub-band is denoted (e.g., $0.12 m_0$). Note, due to larger valence band edge splitting of Ge, hole repopulation in Ge is more than in Si.
3.2.3 Stress Altered Electron Tunneling Currents From Metal Gate

The carrier separation technique also allows the electron tunneling current via $I_{SUB}$ to be measured which is altered by strain due to a shift in the band offset between the gate electrode and dielectric [83]. Fig. 3-15 shows the relative change of $I_{SUB}$ as a function of stress for the Ge channel MOSFET. Due to the decreased TiN gate work-function with stress, $I_{SUB}$ increases, showing that the work-function of metal gate decreases under tensile stress.

To quantify the metal work-function shift, $\Delta V_{FB}$, where $V_{FB} = \phi_{MS} - \frac{Q_{OX}}{C_{OX}}$, is measured using capacitance-voltage measurement. Since the permittivity of SiO$_2$, the fixed oxide charge and the interface trapped charge does not change appreciably with applied stress [84] and the Fermi energy level of the silicon substrate only changes up to ~1mV at 200 MPa [85, 86], the metal work-function shift ($\Delta \phi_M$) can be approximated from $\Delta V_{FB}$. Fig. 3-16 shows the C-V characteristics of MOS capacitor with TaN gate and $V_{FB}$ is measured to increases/decreases with compressive/tensile stress.

Fig. 3-17 plots $\Delta \phi_M$ of the TaN gate as a function of stress, obtained from Fig. 3-16(b) and compared to the work-function shifts of bulk metals[87, 88]. The stress altered work-function in TaN gate follows a similar trend as that in bulk metal of Al and Cu. The TaN work-function increases/decreases by approximately 4 mV at compressive/tensile stress of 200 MPa.

The relative change in the stress altered electron gate tunneling current from the TaN gate to substrate is measured and plotted in Fig. 3-18[89]. The data is extracted at the gate bias of -1.7 V. The gate tunneling current increases/decreases with tensile/compressive stress. An analytical equation based on the electron direct tunneling model is employed to fit experimental data [90, 91].
\[ J = \frac{q}{4\pi^2 \hbar^2 m^*} \exp\left[-\frac{\sqrt{2m^*}}{\hbar} \phi_b(\sigma)^{3/2} d + \frac{(2m^* \phi_b(\sigma))^{1/2}}{2\hbar} qEd^2\right] \] (3-10)

where

\[ E =\frac{V_G - V_{FB} - \Psi_S}{d} \]

\[ \Psi_S = V_G - V_{FB} + qN_Sd^2 \varepsilon_{Si}/\varepsilon_{OX} - \sqrt{(V_G - V_{FB} + qN_Sd^2 \varepsilon_{Si}/\varepsilon_{OX})^2 - (V_G - V_{FB})^2} \]

where \( d \) is the oxide thickness and \( m^* (=0.5m) \) [92] and \( E \) is the effective electron mass and the electric field in the SiO₂ layer, respectively. Also, \( m \) , \( \Psi_S \) and \( \phi_b(\sigma) \) is the electron mass in the free space, the substrate bend bending and the effective barrier height as a function of applied stress, respectively. We used the effective oxide thickness, \( d^* = d - \delta (\delta = 0.08nm) \) instead of the physical thickness due to the surface roughness or the uncertainty of electrical measurement for the determination of the oxide thickness[90]. For modeling, \( \phi_b(\sigma) \) is estimated with the linear fit of \( \Delta \phi_M \) in Fig.3-17. Our calculation shows good agreement with measured data in Fig. 3-18. The relative change in electron tunneling current increases/decreases up to 1.0% under 200 MPa of tensile/compressive stress, resulting from the decreased/increased metal gate work-function by 4meV.
Figure 3-15. Relative change in $I_{\text{SUB}}$ of Ge p-MOSFET as a function of stress at gate bias of -2.8V. Due to decreased work-function of TiN gate, electron gate tunneling current from TiN gate increases up to ~4% with 100MPa of stress. The inset shows the decreased tunneling barrier height via strain by the decreased work-function of TiN gate.

Figure 3-16. The $V_{\text{FB}}$ shift under uniaxial stress. (a) C-V curve of MOS capacitor, measured at 100KHz. $V_{\text{FB}}$ is extracted from $C_{\text{FB}}$. (b) $V_{\text{FB}}$ shift as a function of tensile and compressive stress. $V_{\text{FB}}$ decreases/increases with tension/compression.
Figure 3-17. Work-function shifts of TaN, bulk Al and bulk Cu as a function of stress[87]. Work-functions of three different metals increase/decrease with compressive/tensile stress. Line is the linear fit of extracted data.

Figure 3-18. Relative changes in gate tunneling current of MOS capacitor with TaN gate as a function of stress. Symbols and lines are measured data and modeling, respectively.
3.2.4 Summary

Due to larger 1) stress induced valence band edge splitting and 2) change in hole tunneling attempt frequency in inversion-layer of Ge under uniaxial tensile stress, the change in stress altered hole gate tunneling current in Ge is \(~4\) times larger than that in Si. The work-function of the metal gate is measured to change with strain and decrease/increase \(~20\text{meV}\) for each \(1\ \text{GPa}\) of uniaxial tensile/compressive stress.
CHAPTER 4
IMPACT OF MECHANICAL STRESS ON DIRECT AND TRAP-ASSISTED GATE LEAKAGE CURRENTS IN P-TYPE MOS CAPACITORS

4.1 Introduction

State-of-the-art logic devices requires uniaxial stress to enhance transistor performance[80, 94]. Uniaxial stress is also being used in nonvolatile memory (NVM) to improve the retention time[95-97]. In NVM, trap-assisted gate tunneling current can be a dominate factor in the retention time[98] and the reliability of the tunneling dielectric[22, 23]. The high electric field during programming (Fowler-Nordheim tunneling) generates electron traps in the SiO$_2$ dielectric or at the SiO$_2$/Si interface, resulting in trap-assisted gate tunneling[98].

It has been reported that mechanical stress affects trap generation in MOS devices [99, 100], but less attention has been paid to mechanical stress-altered trap-assisted gate tunneling current[67]. In this work, we report for the first time, the effects of uniaxial stress on trap-assisted gate tunneling current using controlled applied mechanical stress and constant voltage stress (CVS).

4.2 Experimental Set-Up

Samples used in this work consist of MOS capacitors with TaN metal gate on top of 2.5 nm SiO$_2$ dielectric fabricated on p-type (100) Si surface substrate. Large area $10^5 \mu$m$^2$ devices are used to eliminate the fringe leakage components. The electric damage is created by -4.0 V of gate voltage for 50 seconds[101]. By monitoring the gate leakage current as a function of time at the fixed gate voltage, the CVS condition is adopted, where applied gate voltage generates traps, but does not cause dielectric breakdown. Due to the generated traps during CVS, trap-assisted tunneling becomes a dominant gate leakage mechanism, resulting in an increase in gate leakage current after CVS, compared to one before CVS[23]. Next, uniaxial 4-point external mechanical stress is apply along [110] direction while changes in the gate to substrate electron tunneling
current (negative gate bias) and electron gate tunneling from substrate to gate (positive gate bias) are measured[13]. The maximum gate voltage used during the gate leakage measurement ($V_G = \pm 1.7 \text{ V}$) is limited below the magnitude of the gate voltage in CVS condition ($V_G = -4 \text{ V}$) to ensure minimal gate oxide damage during this measurement.

4.3 Results and Discussions

To understand the effects of uniaxial mechanical stress on gate leakage current in samples before and after CVS, both gate and substrate injections are measured under tensile and compressive stresses. Figure 4-1 shows the relative change of gate leakage current in samples before (Fig. 4-1(a)) and after CVS (Fig. 4-1(b)) as a function of mechanical stress. The relative changes for gate and substrate injections are extracted at the gate voltage of -1.7 V and 0.8 V, respectively[89]. In samples before CVS where direct electron tunneling is a dominant mechanism, gate and substrate injections show an opposing dependence on mechanical stress, as shown in Fig. 4-1(a). Under tensile (compressive) stress, gate injection increases (decreases) while substrate injection decreases (increases). For sample after CVS where the dominant leakage current is trap-assisted tunneling current, both gate and substrate injection is increased under tensile and compressive stresses, as shown in Fig. 4-1(b). Fig. 4-1(b) also shows a larger slope for the change in gate and substrate injections under compressive stress as compared to tensile stress.

The effects of mechanical stress on direct and trap-assisted gate leakage currents can be understood with Fig. 4.2. Fig. 4.2(a) illustrates the impact of mechanical stress on direct gate tunneling for gate and substrate injections. Under gate injection, applied tensile (compressive) stress decreases (increases) the tunneling barrier height of electrons from gate to substrate via TaN gate work function shift, resulting in an increase (decrease) in gate leakage current[102].
Under substrate injection, mechanical stress-induced electron repopulation between $\Delta_2$ and $\Delta_4$ sub-bands in the n-type inversion layer changes the out-of-plane effective mass and tunneling barrier height of electrons in $\Delta$ sub-bands as previously reported [18, 19, 21, 103].

During CVS for thin SiO$_2$ (< 2.5 nm), energetic electrons injected from gate to the Si substrate breaking dangling bonds in the [111] direction, normally passivated by hydrogen at P$_{b0}$ and P$_{b1}$ centers at near the SiO$_2$/(100)Si interface [99]. These additional defects increase trap assisted tunneling currents [98, 101].

For trap-assisted gate tunneling, the detrapping of the SiO$_2$ electron plays a primary role in gate leakage current [104]. The trap activation energy, $\phi_T$, where $\phi_T = E_{OX}^{C} - E_{TRAP}$, determines the detrapping processes as illustrated in Fig. 4-2(b). Here, $E_{OX}^{C}$ and $E_{TRAP}$ are the conduction band edge of SiO$_2$ and trap energy level, respectively, and $\phi_T$ is a function of applied mechanical stress ($\sigma$) [105].

Uniaxial mechanical stress along [110] direction alters the structure of P$_{b0}$ and P$_{b1}$ centers, as illustrated in Fig. 4-3 [99, 106-108]. This affects the stability of interface traps, resulting in a change in $\phi_T$ [108]. In P$_{b0}$ center, compressive stress along [110] decreases bond angle $\Theta_1$ and increases the other bond angle $\Theta_2$, due to 1) (100) Si substrate surface structure and 2) dangling bond along [111] direction [99, 106]. For tensile stress along [110], it should have the opposite effect as that for compressive stress. The $\Theta$ decrease, $\Delta \Theta(\sigma) < 0$, means an increase in repulsive force between the dangling bond and at least one of the three back bonds, resulting in the less stable dangling bond, as described in Fig. 4-3(a) and table [106]. For P$_{b1}$ center, the dangling bond with unstrained $\Theta$ ($\Theta = 45^\circ$) is known to have minimum energy and either positive or negative $\Delta \Theta(\sigma)$ makes the dangling bond less stable, as shown in Fig. 4-3(b) [109]. Therefore, both compressive and tensile stresses along [110] cause a decrease in the trap activation energy.
at $P_{b0}$ and $P_{b1}$ centers, $\Delta \phi_T(\sigma) < 0$ [67, 99, 110], resulting in an increase in trap-assisted gate leakage current for both gate and substrate injections, as shown in Fig. 4-1(b). It is reported that a change in SiO$_2$/(100) Si interface trap activation energy under compressive stress is larger than one under tensile stress [105, 111, 112], matching with our results that the relative change of trap-assisted gate leakage current under compressive stress is larger than under tensile stress (observed for both gate and substrate injections in Fig. 4-1(b)).

4.4 Conclusions

Different dependences of gate leakage currents on uniaxial mechanical stress are observed from direct and trap-assisted gate tunneling currents. The CVS technique is used to generate traps at SiO$_2$/(100) Si interface and monitor interface trap-assisted gate leakage current in MOS capacitor with 2.5 nm thin SiO$_2$. Both mechanical tensile and compressive stresses along [110] increase trap-assisted gate leakage current via the lowering of trap activation energy of $P_{b0}$ and $P_{b1}$ centers, showing that uniaxial stress along [110] may not be applicable to improve the gate leakage of logic devices and the retention time of NVM devices when trap-assisted tunneling is a dominant mechanism in gate leakage current.
Figure 4-1. Relative change of gate leakage currents in MOS devices (a) before constant voltage stress (CVS) and (b) after CVS as a function of applied mechanical stress along [110] direction, respectively.
Figure 4-2. Schematic band diagrams for a) direct and b) trap-assisted gate tunneling mechanisms. Key parameters for mechanical stress-altered electron gate tunneling currents before and after CVS are summarized in table.

<table>
<thead>
<tr>
<th>Before CVS</th>
<th>After CVS</th>
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<td>Gate Injection</td>
<td>Substrate Injection</td>
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<tr>
<td>TaN metal work function</td>
<td>Si conduction band edge splitting</td>
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</table>

<table>
<thead>
<tr>
<th>Key Parameter for $J_0(\sigma)$</th>
<th>Trap activation energy</th>
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</table>

Figure 4-3. Schematic of SiO$_2$/(100) Si interface structure including P$_{b0}$ and P$_{b1}$ centers, showing mechanical stress-induced changes in dangling bond angles ($\Theta$) and interface trap activation energy ($\Phi_T$).
CHAPTER 5
STRAIN INDUCED CHANGES IN GATE LEAKAGE CURRENT AND DIELECTRIC CONSTANT OF NITRIFIED HF-SILICATE DIELECTRIC SILICON MOS CAPACITORS

5.1 Introduction

Hafnium silicate has been extensively studied as a gate dielectric material in advanced metal oxide semiconductor field effect transistors (MOSFETs) due to a high crystallization temperature, thermodynamic stability with Si, high permittivity and relatively large band gap (5.68 eV) [113-116]. Nitrogen incorporated Hf-silicate (HfSiON) has received attention since HfSiON minimizes interfacial layer formation and reduces boron diffusion from the poly-Si gate into the channel [117, 118]. Also, recent reports have explained additional advantages of nitrided Hf-silicate such as increased dielectric constant and improved reliability [119, 120].

Strained silicon technology has been adopted in high-k gate stack MOSFETs, showing strain can improve mobility similarly for Hf-silicate MOSFETs compared to SiO₂ MOSFETs [82]. However, to date, there is no systematic and quantitative result on the strain altered dielectric constant and gate leakage current of HfSiON dielectric film. In this work, we report on the effect of mechanically applied uniaxial stress on the gate leakage current and dielectric constant of Si MOS capacitors with HfSiON gate dielectric.

5.2 Experimental Procedures

The HfSiOₓ films are deposited directly on p-type (100) pre-cleaned (1% HF solution and DI water rinse) 8 inch Si substrates with a resistivity of 3-25 Ωcm using atomic layer deposition (ALD) at 300°C. The oxidizing agents for TEMAH and Si are O₃ and H₂O, respectively. HfSiOₓ film deposition is followed by nitrogen incorporation by rapid thermal anneal (RTA) at 650°C in NH₃ ambient for 60 s. MOS capacitors with Pt and Al gate electrode were fabricated using RF magnetron sputtering. All of the metals were deposited by Ar plasma assisted RF sputtering at a pressure of 15 mTorr and 150W RF (13.56 MHz) power. For all MOS devices, post metallization
annealing (PMA) was carried out in a tube furnace at 400°C in forming gas (10% H₂ / 90% N₂) ambient for 30 min. Capacitance-voltage (C-V) and current-voltage (J-V) measurements were measured with Agilent E4980A and Keithley 4200, respectively, using external mechanical uniaxial stress along the [110] direction [13]. To extract the frequency-independent device capacitance value and eliminate the effect of both series and shunt parasitic resistances, a two-frequency method is adopted [121]. The flat band voltage (\(V_{FB}\)) is extracted from the C-V measurements [122]. To reduce the electrical instability from HfSiON charging [123], a constant gate voltage (-1V) was applied for 160 s before J-V measurement. This reduces the J-V instability to less than 0.2% variation.

5.3 Results and Discussions

Figure 5-1 shows the C-V (a) and J-V (b) characteristics of Hf-silicate dielectric MOS capacitors. In order to verify the gate tunneling conduction mechanism, aluminum (Al) and platinum (Pt) electrodes are used due to their large bulk work function difference (\(\phi_{Al} \approx 4.1\) and \(\phi_{Pt} \approx 5.8\) eV) [124]. The accumulation capacitance values are almost identical (~1.2 \(\times\) 10\(^{-6}\) F/cm\(^2\)) resulting in an equivalent oxide thickness of 2.7 nm regardless of the gate electrodes[125]. The nearly identical accumulation capacitance and parallel shift of C-V curves for Pt and Al gate electrodes indicates that, regardless of gate material, a sharp interface and minimal interaction between the metal gate and dielectric film are maintained. Due to the difference in the work function of Pt and Al, a difference in \(V_{FB}\) and larger leakage current under negative gate bias is observed for the Pt devices. The larger leakage current in Pt devices can be explained by the following: (1) the dominant leakage current mechanism is hole tunneling from the substrate to gate as opposed to electron tunneling from gate to substrate[126], and 2) a higher built-in oxide field of the Pt device results from a larger work function as illustrated in the inset of Fig. 5-2.
Figure 5-1. The $C-V$ characteristics at 1MHz of the MOS device with Pt and Al gate on nitrided Hf-silicate film (a). The inset shows current density-voltage ($J-V$) measurements of both devices (b).

Figure 5-2. Poole-Frenkel ($\ln(J/E)$ vs $E^{1/2}$) plot of Pt and Al gate on nitrided Hf-silicate film at 25 $^\circ$C. Inset in figure shows a schematic band diagram for MOS capacitors with HfSiON dielectric and interlayer and metal gates (Pt and Al) under negative gate bias.
Fig. 5-2 shows the Poole-Frenkel (PF) plot for both metal electrodes with HfSiON gate dielectric. The slope of PF plot can be expressed as

\[
Slope(\sigma) = \frac{\Delta \ln(J / E)}{\Delta \sqrt{E}} = \frac{q}{kT} \sqrt{\frac{q}{\pi \varepsilon_r(\sigma) \varepsilon_0}}
\] (5-1)

where \(k\), \(T\), \(\varepsilon_r(\sigma)\) and \(\varepsilon_0\) are the Boltzmann constant, temperature, high frequency dielectric constant of the insulator under external stress, and vacuum permittivity, respectively. The high frequency dielectric constant without external stress extracted from the slope of the PF plot is 4.9. The refractive index, \(n\), given by the square root of the high frequency dielectric constant,\(^{127, 128}\) is found to be 2.23, showing that the extracted dielectric constant is within the range of refractive indices reported for HfSiON films (1.8~2.4)\(^{129}\).

The normalized change in strain-altered gate leakage currents for Al and Pt HfSiON MOS capacitor are shown in Fig. 5-3. Regardless of electrodes, an increase in normalized leakage current is observed for both tensile and compressive stresses. Recently, Choi et al suggested that a decrease in trap activation energy results in an increase in trap-assisted gate leakage current under mechanical stress\(^{130}\). Based on a decrease in hole trap activation energy under mechanical stress \(^{131}\) and a dominant hole tunneling gate leakage mechanism under negative gate bias in high-k dielectric\(^{132}\), an increase in PF emission-based gate leakage may result from a decrease in hole trap activation energy in high-k dielectric under both tensile and compressive stresses.

The measured normalized change in the strain altered dielectric constant of HfSiON, HfSiO\(_x\), and HfO\(_2\) are shown in Fig. 5-4. Unlike HfO\(_2\) and HfSiO\(_x\), the dielectric constant of HfSiON is observed to increase with both tensile and compressive stresses, as determined using two separate techniques, \(C-V\) curve and slope extraction from the PF plot shown in Fig. 5-2.
We propose that the incorporated nitrogen in Hf-silicate film may be the origin of the strain-induced dielectric constant change. The nitrogen incorporation creates a N\textit{p} band above the valence band edge of HfSiO\textsubscript{119}. The N\textit{p} band splitting by applied mechanical stress may lead to band gap narrowing of HfSiON, increasing the electronic transition from the N\textit{p} band to the conduction band\textsuperscript{133, 134}. This band gap narrowing should increase the HfSiON dielectric constant\textsuperscript{119}.

![Figure 5-3. Changes in gate leakage current of Si MOS capacitors with HfSiON dielectric as a function of applied stress.](image-url)
Figure 5-4. Changes in dielectric constant of HfSiON, HfSiOx and HfO2, measured from C-V and PF slope change.

To date, there have been no reports on strain altering the dielectric constant of SiON which is commonly used for gate dielectrics in advance logic technologies. One explanation is that for SiON, nitrogen incorporation into SiO2 primarily occurs at the SiO2/Si interface. XPS measurement results show no observed band gap narrowing of SiO2 due to N p band formation near valence band edge of SiO2[135]. Thus, the dielectric constant of SiON is not expected to change significantly for mechanical stress range (<100 MPa) used in this work.

5.4 Conclusions

The impact of four point wafer bending uniaxial stress on gate leakage and gate dielectric constant of Si MOS capacitor with HfSiON has been studied. A measured increase in strain-altered gate leakage is attributed to a decrease in hole trap activation energy in HfSiON. An increase in HfSiON dielectric constant is also observed under both tensile and compressive
stresses. Thus, in additional to strain enhanced channel mobility, strained HfSiON may provide a slight additional improvement via an increase in oxide capacitance.
CHAPTER 6
IMPACT OF DIFFERENT GATE STACKS AND CHANNEL MATERIALS ON
THRESHOLD VOLTAGE SHIFTS IN P-TYPE METAL OXIDE SEMICONDUCTOR FIELD
EFFECT TRANSISTORS UNDER MECHANICAL STRESS

6.1 Introduction

Uniaxial strained-Si has been adopted to increase performance in sub-90nm production
technologies[24, 31, 80]. Strain-induced threshold voltage, $V_{th}$, shift can be a critical issue[136].
However, little attention has been given to $V_{th}$ shift in uniaxial technology[137]. $V_{th}$ shift in Si p-
MOSFETs is generally regarded as insignificant without any quantitative explanation[138].

Because scaling has reached fundamental material limits for gate stacks and channels, we
can now scale with new materials and/or device architectures. TiN/HfO$_2$ gate stack and strained-
Ge have been expected to be substitutes for poly Si/SiO$_2$ gate stack and strained-Si because of
their smaller gate leakage and higher channel mobility, respectively[139, 140]. Therefore the
investigation of strain-altered $V_{th}$ shift of these devices is timely and worthy. In this work,
uniaxial strain-induced $V_{th}$ shifts of both Ge and Si p-MOSFETs with TiN/HfO$_2$ gate stacks are
explained and compared to poly Si gate stacks. The contribution of strain-induced mobility
change to measured $V_{th}$ shifts is also considered.

6.2 Threshold Voltage Shift Models

The $V_{th}$ shift for a Si p-MOSFET with a poly Si gate under mechanical stress can be
derived from [136, 137];

$$
\Delta V_{th}(\sigma) = -m\Delta E_g(\sigma) - (m - 1) \frac{kT}{q} \ln\left(\frac{N_c(0)}{N_c(\sigma)}\right) - m \frac{kT}{q} \ln\left(\frac{m_{dp}(0)}{m_{dp}(\sigma)}\right)
$$

(6-1)

where $\Delta E_g(\sigma)$, $m$, $N_c$ and $m_{dp}$ are the change in the band gap with stress, the body-coefficient,
the effective densities of states (DOS) in the 3-D conduction band and the 2-D hole DOS.
effective mass in the predominant sub-band, respectively. The same derivation can be used for Si and Ge p-MOSFETs with TiN gate, as shown in (6-2)

$$\Delta V_{th}(\sigma) = \Delta \phi_M(\sigma) + \Delta E_C(\sigma) - m\Delta E_g(\sigma) - (m - 1) \frac{kT}{q} \ln\left(\frac{N_C(0)}{N_C(\sigma)}\right) - m \frac{kT}{q} \ln\left(\frac{m_{\phi}(0)}{m_{\phi}(\sigma)}\right)$$ \hspace{1cm} (6-2)

where $\Delta \phi_M(\sigma)$ and $\Delta E_C(\sigma)$ are the changes in the gate work-function [102] and channel electron affinity and $\Delta E_C$ and $\Delta E_g$ contribute to the $V_{th}$, but with different signs. Here, $\Delta \phi_M$ is positive/negative under compression/tension[87, 102, 141]. Note that, in (6-2), a TiN gate device has both $\Delta E_C$ and $\Delta E_g$, while, in (1), a poly Si gate device has $\Delta E_g$ only. This is because both the Si channel and the poly Si gate are being strained in poly Si gate device[137].

Deformation potential theory is used to express $\Delta E_C$ and $\Delta E_g$ as a function of stress. Strain induces the hydrostatic shift and shear band splitting of conduction band edges, which can be expressed as; [53, 55, 84]

$$\Delta E_C^i = \Xi_d Tr(\varepsilon_{ij}) + \Xi_u \varepsilon_{ii} \hspace{1cm} (6-3)$$

where $\Xi_d$ and $\Xi_u$ are dilation and shear deformation potential constants, $Tr(\varepsilon_{ij})$ is the trace of the strain tensor ($\varepsilon_{ij}$) and $i$ denotes the various valleys (X for Si and L for Ge). For Si and Ge, $\Delta E_C$ and $\Delta E_g$ are calculated and listed in Table 6-1[17, 55].

Strain-induced changes in DOS-related terms also shift $V_{th}$ (last two terms in (6-1) and (6-2)). The change in the effective DOS in the 3-D conduction band is given by $N_C(0)/ N_C(\sigma) = m^*_c(0)^{3/2}/ m^*_c(\sigma)^{3/2}$.[142] In both Si and Ge, $N_C$-related term is negative, irrespective of the type of stress, because stress along [110] causes $m^*_c(\sigma) < m^*_c(0)$ via band splitting [137]. For low stress and moderate to high gate bias, the predominant sub-band in the hole inversion-layer can be determined by gate bias since the energy level splitting from
confinement is dominant[80]. Therefore, applied stress alters \( m_d\sigma \) only via valence band warping, resulting in \( m_d\sigma \) to increase/decrease with compression/tension[13, 80]. Therefore, \( m_d\sigma \)-related term is positive/negative with compression/tension. The contribution of \( N_c\sigma \) - and \( m_d\sigma \)-related terms are significant under tension because both of terms are negative, while under compression, the two terms are opposite in sign.

Both (6-1) and (6-2) were derived based on equal inversion charge at the threshold condition [136]. To relate these expressions to the measured \( V_{th} \) shift [143], the correction term is needed to account for the change in mobility in the strained channel and given;

\[
\Delta V_{th}(\sigma) = m \frac{kT}{q} \ln\left(\frac{\mu(\sigma)}{\mu(0)}\right)
\]  

(6-4)

### 6.3 Results And Discussion

Strain-induced \( V_{th} \) shifts are calculated and compared with wafer bending data. Fig. 6-1(a) plots \( V_{th} \) shifts of Si p-MOSFETs with poly Si and TiN gates, respectively. Under compression, the \( V_{th} \) shift in TiN gate devices is \( \sim 2/3 \) times of that in poly Si gate devices, while it is larger than that in poly Si gate devices under tension. This mainly results from subtractive \( \Delta E_c \) in TiN gate devices, as explained in Sec. 6.2. It is also found that, for poly Si gate devices, the \( V_{th} \) shift under compression is larger than tension, because there is larger band gap narrowing from compression and smaller contribution of DOS-related terms[84]. Fig. 6-1(b) plots \( V_{th} \) shifts of Ge and Si p-MOSFETs with TiN gate. Based on the calculation using (6-2), larger \( V_{th} \) shifts for Ge are expected under compression because, relative to Si p-MOSFET, the Ge channel has larger band edge shift terms \( (\Delta E_c(\sigma) - m\Delta E_g(\sigma)) \).

Next, the mobility correction term is considered. Uniaxial stress along [110] causes channel mobility to change significantly relative to biaxial strain[80]. The contribution of
mobility change to the $V_{th}$ shift, which has been regarded as insignificant in biaxial strain, may be critical in uniaxial strain [136]. Fig. 6-2 plots the strain-induced $V_{th}$ shift of Ge and Si p-MOSFETs with TiN gates with the mobility correction. The inset shows that the relative change in mobility of Si is slightly larger than that of Ge, which is extracted from measured drain current change [82, 93]. Based on mobility change, we calculate the contribution of mobility change terms, listed in Table 6-2, where model-predicted contributions of band-edge shift, DOS-related terms, and $\Delta\phi_M$ are also indicated. As expected, the contribution of mobility change to measured $V_{th}$ shifts is significant and even dominant for Si devices. Note that after the correction, the $V_{th}$ shift of Ge is slightly larger than that of Si, resulting in insignificant $V_{th}$ shifts of both Ge and Si p-MOSFETs with TiN/HfO$_2$ gate stacks.

6.4 Conclusion

Both Ge and Si p-MOSFETs with TiN gates are observed to have insignificant $V_t$ variation under uniaxial stress. The simple $V_{th}$ shift model including the mobility correction shows good agreements with the measured data from different types of p-MOSFETs, demonstrating its universality [144].
Table 6-1. Deformation potential constants used in this study [17] and $\Delta E_c$ and $\Delta E_g$ of Si and Ge, calculated at 300 MPa of uniaxial tension and compression along [110] direction.

<table>
<thead>
<tr>
<th></th>
<th>DEFORMATION POTENTIAL CONSTANTS [EV]</th>
<th>STRESS TYPE</th>
<th>$\Delta E_c$ [mV] @300MPA</th>
<th>$\Delta E_g$ [mV] @300MPA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>$\Xi_d=1.0$, $\Xi_u=9.6$ $B=-2.33$, $D=-4.75$ $\Xi_d+\frac{\Xi_u-a}{3}=0.29$</td>
<td>TENSION</td>
<td>-5.14</td>
<td>-3.48</td>
</tr>
<tr>
<td></td>
<td></td>
<td>COMPRESSION</td>
<td>-8.99</td>
<td>-10.6</td>
</tr>
<tr>
<td>Ge</td>
<td>$\Xi_d=-4.3$, $\Xi_u=16.5$ $b=-2.16$, $d=-6.06$ $\Xi_d+\frac{\Xi_u-a}{3}=-0.83$</td>
<td>TENSION</td>
<td>-5.52</td>
<td>-1.33</td>
</tr>
<tr>
<td></td>
<td></td>
<td>COMPRESSION</td>
<td>-8.68</td>
<td>-13.9</td>
</tr>
</tbody>
</table>
Table 6-2. Model-predicted, with m=1.3, contributions of band edge shifts, DOS change, $\Delta \mu$ and $\Delta \Phi_M$ terms. ($\Delta \Phi_M$ is estimated from [102])

<table>
<thead>
<tr>
<th>STRESS TYPE</th>
<th>THEORETICAL VALUE</th>
<th>EXPERIMENTAL VALUE</th>
</tr>
</thead>
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<tr>
<td></td>
<td>$\Delta V_{TH}$ FROM BAND EDGE SHIFT</td>
<td>$\Delta V_{TH}$ FROM DOS-RELATED TERMS</td>
</tr>
<tr>
<td></td>
<td>[mV] @ 100MPA</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>-1.46</td>
</tr>
<tr>
<td>COMPRESS ION</td>
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<td>0.13</td>
</tr>
<tr>
<td>Ge</td>
<td></td>
<td></td>
</tr>
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<td>TENSION</td>
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<td>-1.15</td>
</tr>
<tr>
<td>COMPRESS ION</td>
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<td>0.43</td>
</tr>
</tbody>
</table>
Figure 6-1. Plots of uniaxial stressed $V_{th}$ shifts of p-MOSFETs with (a) different gate stacks (poly Si/SiO$_2$ vs TiN/HfO$_2$) and (b) different channels (Ge vs Si). Symbols and lines are experimental data and calculated models, respectively. Note here that $\Delta V_{th} < 0$ would mean that the magnitude of $V_{th}$ (which is negative) is increased by stress.

Fig. 1(a)

Fig. 1(b)
Figure 6-2. Plots of $V_{th}$ shifts of Ge and Si p-MOSFETs with the mobility correction as a function of stress. Symbols and lines are experimental data and calculated models, respectively. The inset shows the relative changes in mobility of Ge and Si p-MOSFETs with TiN/HfO$_2$ gate stack as a function of stress.
CHAPTER 7
RELIABILITY OF NITRIDE HAFNIUM SILICATE GATE DIELECTRICS UNDER [110] UNIAXIAL MECHANICAL STRESS: TIME DEPENDENT DIELECTRIC BREAKDOWN

7.1 Introduction

State-of-the-art CMOS devices requires uniaxial stress to enhance the performance of transistor with high k gate stack[145]. Among the candidates for high-k dielectrics, nitrided hafnium silicate (HfSiON) is a promising material due to high crystallization temperature and thermodynamic stability with Si[146]. The reliability of HfSiON Si MOS device, such as time dependent dielectric breakdown (TDDB), bias temperature instability (BTI) and threshold voltage ($V_{TH}$) instability, and hot carrier injection (HCI) also has been extensively studied to help improve device lifetime[147].

It has been reported that applied mechanical stress changes TDDB and negative bias temperature instability (NBTI) in SiO$_2$ dielectric Si MOS device[100, 148-150] but less attention has been focused on impact of applied mechanical stress on TDDB and NBTI in HfSiON[111, 151]. Furthermore, most of these works have used process-induced strain, such as a nitride stressor, which can contain hydrogen and water and introduce ambiguity into the strain effect on device reliability[100, 152-154].

In this work, we report on the effects of both uniaxial tensile and compressive stresses on TDDB in HfSiON Si MOS devices using controlled applied external mechanical stress. From the mechanical stress dependence and thickness independence, possible degradation mechanisms are identified. Mechanical stress-induced BTI, HCI, and $V_{TH}$ instability of high k MOSFETs are also briefly discussed.
7.2 Experimental Setup

Samples used in this work consist of MOS capacitors with aluminum metal gate on top of 7 and 8 nm HfSiON dielectrics fabricated on p-type (100) Si substrate[155]. Samples with gate area of 0.000857, 0.0016, 0.0026, and 0.0052 cm² are used. Constant negative gate voltage stressing is performed with a gate leakage current compliance limit of 10 pA using a Keithley 4200 DC characterization system. We define the time to breakdown ($t_{BD}$) as the first sudden increase in the gate leakage current (soft breakdown), as shown in Figure 7-1[147, 156-158]. The steep increase in the gate leakage current upon onset of breakdown allows measurement of the breakdown event at a well-defined electric field. A custom built four point wafer bending setup is used to apply external mechanical stress along the [110] direction during constant voltage stressing (CVS)[13]. The impact of mechanical stress on the distribution of $t_{BD}$ and charge to breakdown ($Q_{BD}$) is monitored in the HfSiON MOS capacitor samples.

Figure 7-1. Current-time curve for 7 nm HfSiON dielectric Si MOS device during CVS
7.3 Experimental Results

In this section, experimental data on the distributions of $t_{BD}$ and $Q_{BD}$ in HfSiON Si MOS capacitors under both mechanical tensile and compressive stress is reported. Figure 7-2(a) shows $t_{BD}$ Weibull plots with different area samples with 7 nm thick HfSiON dielectrics, where an area-dependent $t_{BD}$ distribution is observed [159]. When the results are scaled by area as in Figure 2(b), the scaled $t_{BD}$ Weibull curves coincide which indicates an intrinsic breakdown mechanism. The area scaled $t_{BD}$ is computed based on the following equation.

$$F_j(t) = 1 - (1 - F_i(t))^{A_j/A_i} \quad (7-1)$$

where $F_j$ and $F_i$ are the probability of failure at area $A_j$ and $A_i$ [111, 160]. The Weibull slope ($\beta$) is 1.2, which is close to the published value [156].

To understand the impact of uniaxial mechanical stress on $t_{BD}$ in samples, CVS is performed with $V_G = -5.2$ and -7 V under tensile and compressive stresses, respectively. Fig.7-3 and 7-4 show impact of mechanical stress on $t_{BD}$ Weibull plots. Applied tensile stress reduces time to breakdown at 50% ($t_{BD,50\%}$) from 44 to 15 sec and $\beta$ from 1.4 to 1.1, respectively, as shown in Fig. 7-3(a) and (b). In addition, compressive stress, in Fig. 7-4(a) and (b), also reduces $t_{BD,50\%}$ from 24 to 7.3 sec and $\beta$ from 0.81 to 0.74, respectively. In summary, both applied tensile and compressive stresses degrade $t_{BD}$ of HfSiON dielectric, consistent with the previously reported data from process-induced strain and SiO$_2$ dielectrics [111, 148, 161].

Mechanical stress dependence on $t_{BD}$ can be investigated by (1) monitoring the relative change in gate injection current of HfSiON Si MOS device as a function of applied mechanical stress [149] and (2) mechanical stress-induced increase in HfSiON/Si interface trap generation during CVS [111]. In our previous work [155], we already observed an increase in gate injection current, based on Poole-Frenkel emission, under both tensile and compressive stresses, matching
with our mechanical stress dependence on $t_{BD}$ in this work. Hence, it is consistent with the observation that an increase in gate injection current results in a decrease of $t_{BD}$. [149].

It has been reported that, for gate stack with high-k dielectric thicker than 7~8 nm, $Q_{BD}$ for gate injection is equivalent with those for SiO$_2$ with a thickness identical to the interfacial layer [158]. In Fig. 7-5, $Q_{BD}$ for 8 nm thick HfSiON is measured and compared to $Q_{BD}$ in samples with 7 nm thick HfSiON in order to confirm this interfacial layer breakdown mechanism. Since interface quality is independent of the thickness of HfSiON [162], it shows almost similar $Q_{BD}$ distributions under 84 MPa of tensile and no mechanical stresses. Therefore, impact of mechanical stress on $t_{BD}$ in HfSiON Si MOS device can be explained by mechanical stress-altered trap generation in Si-rich HfSiON interlayer (IL) or at IL / (100) Si interface during CVS [111]. Both tensile and compressive mechanical stresses facilitate trap generation at IL / (100) Si interface or Si-O bond breaking in IL [99, 100, 105, 109, 111].

Figure 7-2. The $t_{BD}$ distributions and area scaled $t_{BD}$ distributions for different size samples under $V_G = -5.2$ V.
Figure 7-3. Uniaxial tensile stress effect a) on $t_{BD}$ distributions and b) on area scaled $t_{BD}$ distributions under $V_G = -5.2$ V.

Figure 7-4. Uniaxial compressive stress effect a) on $t_{BD}$ distributions and b) on area scaled $t_{BD}$ distributions under $V_G = -7$ V.
Figure 7-5. The Q_{BD} distributions for samples with two different HfSiON dielectrics thickness (7 and 8 nm) under tensile mechanical stress

7.4 Discussion

In this section, physical insight into impact of mechanical stress on reliability issues, such as BTI, HCI, thermal stress-induced subthreshold leakage and V_{TH} instability, will be provided based on how applied mechanical stress affects high k/Si interface trap generation and trap activation energy in high k dielectric.

In previous section, impact of mechanical stress on TDDB of 7 nm thick HfSiON Si MOS device with negative gate voltage stressing was discussed. If TDDB occurs in thin (< 3 nm) high k or with positive gate voltage stressing, it does not involved significant interface trap generation and may be dependent on high k layer not Si rich interlayer[158]. This can result in improved TDDB with mechanical stress if mechanical stress reduces gate tunneling current[149]. Since a dominant gate tunneling mechanism in thick (> 3 nm) high k MOS device is Poole-Frenkel emission[158] and mechanical stress increases Poole-Frenkel emission or trap-assisted gate
tunneling[130, 155], TDDB under mechanical stress may be improved only in thin (< 3 nm) high
k, where mechanical stress can decrease direct gate tunneling current[102].

It is widely proposed that NBTI also results from the generation of trap via Si-H bond
breaking at high k/Si interface[158, 163-165]. Fig. 7-6(a) shows high resolution TEM image of
HfSiON Si MOS capacitor, which contains SiO2-like Si rich interlayer. Since mechanical stress
makes Si-H bond less stable, as illustrated in Fig. 7-6(b) and (c)[109], both [110] tensile and
compressive mechanical stresses may degrade NBTI in high k Si MOSFETs [100, 166].

As discussed above, positive bias temperature instability (PBTI) may not generate
interface trap but involve charge trapping in high k bulk or high k/Si interface [158, 165]. This
may result in improved PBTI via mechanical stress-induced increase in charge detrapping in
thick (> 7 nm) HfO2 Si MOSFET [131]. An insignificant process-induced stress dependence of
PBTI in thin (3 nm) high k Si MOSFET has been already reported, resulting from negligible
charge trapping in thin high k layer [151, 167].

Thermal stress-induced sub-threshold leakage, which can degrade the retention time of
dynamic random access memory (DRAM) [168], also results from Si-H bond breaking at high
k/Si interface [168, 169]. Therefore, both [110] tensile and compressive stresses likely increase
thermal stress-induced sub-threshold leakage in high k Si MOSFETs via strain-enhanced
hydrogen depassivation at high k/Si interface [109].

It has been reported that HCI and $V_{TH}$ instability likely result from a trapping of charges in
the pre-existing traps in high k/Si interface and/or high k dielectric without creation of additional
traps [105, 107, 108, 158, 170]. Due to its technological importance, impact of external
mechanical stress on HCI has been aggressively studied, showing opposite trends[105, 107, 108,
170, 171]. Two strain-related models can explain this discrepancy: (1) a decrease in charge
trapping in relative thick gate dielectric via strain-altered trap activation energy[105, 107, 108] and (2) strain-induced Si band gap narrowing and an increase in impact ionization at drain edge[170, 171]. For both uniaxial tensile and compressive stresses, a decrease in a trapping of injected hot carriers in high k likely results in an improved HCI, [130, 131] while an increase in impact ionization may multiply a number of hot carriers, leading to an degradation of HCI [84].

In high k integration, $V_{TH}$ instability has been one of challenges[158]. As explained above, applied mechanical stress reduces electron or/and hole trap activation energy in high k/Si interface and/or high k dielectric[130, 131]. This results in (1) an increase in trap-assisted gate tunneling (or Poole-Frenkel emission) and (2) a decrease in charge trapping in high k[130, 131]. Therefore, $V_{TH}$ instability can be improved at the expense of an increased trap-assisted gate tunneling leakage under both uniaxial tensile and compressive stresses. Due to substantial reduction of gate leakage in high k device,[165] this trade-off will be beneficial for device performance.

Table 7-1 and Fig. 7-7 summarize impact of uniaxial mechanical stress on reliability issues with thick (~ 7 nm) high k Si MOSFETs as discussed above. Most of reliability issues in strained Si technology may be evaluated with impact of mechanical stress on trap activation energy in high k and on high k/Si interface trap generation.
Figure 7-6. Interface trap generation under mechanical stress. a) High resolution TEM image of HfSiON Si MOS capacitor. The gate dielectric is composed of Hf rich HfSiON and Si rich interlayer. b) Schematic of Si rich interlayer/ (100) Si interface including Si-H bonding. c) The calculated energies corresponding to the hydrogen position [109]. Here, $E_{Si-H}$ is Si-H bonding energy and $\sigma$ is applied uniaxial stress.

Figure 7-7. Schematic band diagram for key strain-related parameters for reliability issues. Here, $E_{A,H}$ and $E_{A,E}$ is hole and electron trap activation energy, $\sigma$ is applied uniaxial stress, $Q_{ot}$, $I_G$, and $N_{it}$ is trapped charge density, gate leakage, and the number of interface trap, respectively.
7.5 Conclusion

Uniaxial mechanical stress may not be beneficial for > 7nm thick HfSiON Si MOS device from the view point of reliability issues, such as TDDB, BTI and thermal stress-induced sub-threshold leakage[172]. Applied tensile and compressive stresses degrade TDDB in HfSiON Si MOS device, which results from mechanical stress-induced increase in (1) trap generation in HfSiON/Si interface during negative gate voltage stressing and/or (2) trap-assisted gate tunneling. For state-of-the-art strained-Si techniques, where up to 1.5 GPa of stress can be achieved in channel area, process-induced mechanical stress in HfSiON/Si interface is inevitable. Therefore, interface engineering, which can improve the quality of HfSiON/Si interface, may be required to improve TDDB, NBTI, and thermal stress-induced sub-threshold leakage of HfSiON Si MOSFETs together with strain engineering[152]. Uniaxial strain engineering shows the potential to decrease HCI and $V_{TH}$ instability in high k MOSFETs via a decrease in charge trapping.
Table 7-1. Measured and estimated reliability issues of thick (> 7 nm) high k Si MOSFET as a function of uniaxial mechanical stress.

<table>
<thead>
<tr>
<th>TDDB</th>
<th>$V_G &lt; 0$</th>
<th>KEY MECHANISM</th>
<th>KEY STRAIN-RELATED PARAMETER</th>
<th>TENSION</th>
<th>COMPRESSIO N</th>
<th>REF.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>POOLE-FRENKEL EMISSION &amp; INTERFACE TRAP GENERATION</td>
<td>TRAP ACTIVATION ENERGY &amp; SI-H BOND DEPASSIVATION</td>
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<td>DEGRADED</td>
<td>THIS WORK</td>
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<td></td>
<td>POOLE-FRENKEL EMISSION</td>
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<td>DEGRADED</td>
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<td>DEGRADED</td>
<td>[100, 151, 166]</td>
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<td>[131]</td>
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<td>[170, 171]</td>
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<td></td>
<td>TRAP ACTIVATION ENERGY</td>
<td>IMPROVED</td>
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<td>[105, 107, 108]</td>
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<td>$V_{TH}$ INSTABILITY</td>
<td>CHARGE TRAPPING</td>
<td>TRAP ACTIVATION ENERGY</td>
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<td>[131]</td>
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8.1 Summary

This study mainly focuses on externally applied mechanical uniaxial stress effects on Si & Ge MOSFETs in terms of channel mobility, gate tunneling leakage, and gate stack, such as high-k dielectric and metal gate.

The physics and advantages of uniaxial process induced stress are understood. Calculations and experimental data show that low in-plane and large out-of-plane conductivity effective masses and a high density of states in the top band are all necessary for large hole and electron mobility enhancement.

It is explained that, for n-MOSFETs under uniaxial tensile stress along [110] and [100], the change in direct gate tunneling current for Ge is measured to be 3 times smaller than that for Si and opposite in sign. This reverse behavior occurs because tensile stress for Si causes electron repopulation into $\Delta_2$ increasing the out-of-plane effective mass while, in Ge, a reduced tunneling barrier is the dominant mechanism, resulting from the hydrostatic shift of the conduction band edge.

This is followed by the study about the direct gate tunneling current of Ge and Si p-MOSFETs. Due to larger 1) stress induced valence band edge splitting and 2) change in hole tunneling attempt frequency in inversion-layer of Ge under uniaxial tensile stress, the change in stress altered hole direct gate tunneling current in Ge is ~4 times larger than that in Si. The work-function of the metal gate is measured to change with mechanical stress and decrease/increase ~20meV for each 1 GPa of uniaxial tensile/compressive stress.

Impacts of mechanical stress on direct and trap-assisted gate tunneling leakage current are also observed. The applied mechanical stress increases trap-assisted tunneling current via the
lowering of trap activation energy showing uniaxial stress may not be applicable to reduce gate leakage current when trap-assisted tunneling conduction is dominant.

The roles of HfSiON dielectric in strained Si technology are explored. Unlike HfSiOₓ and HfO₂, HfSiON shows strain altered increased dielectric constant, which allows scaling to achieve an increased gate capacitance.

Both Ge and Si p-MOSFETs with TiN gate are observed to have insignificant Vₜ variation under uniaxial stress. The simple Vₜ shift model including the mobility correction shows good agreements with the measured data from different types of p-MOSFETs (poly Si/SiO₂ vs TiN/HfO₂ gate stacks and Si & Ge channels).

Finally, impact of mechanical uniaxial stress on time dependent dielectric breakdown of HfSiON dielectric is studied. Under constant voltage stressing with negative gate bias, applied mechanical stress causes HfSiON/Si interface to become less stable. This results in more trap generation at interface and leads to a decrease in time to dielectric breakdown.

### 8.2 Recommendations for Future work

The demand for novel material and structure becomes increasing in the CMOS regime. With strain engineering becoming a mainstream in VLSI technology, there will be much interest in studying its effects in channel mobility of novel devices, such as FINFET with Ge or III-V channel.

While aggressive researches have been done on how strain improve channel mobility of planar novel channel devices, such as Ge and III-V, less attention has been paid to strain effect on reliability of these devices. As a part of future work, it is interesting to continue the work on impact of mechanical stress on reliability of novel channel devices, such as time dependent dielectric breakdown, hot carrier injection, bias temperature instability and so on.
The aggressive scaling of VLSI technology will push the channel length to ballistic transport regime and the importance of surface roughness scattering limited mobility gets significant. Therefore, it is interesting to study strain effects on physical surface roughness or/and surface roughness scattering in order to fully understand mobility enhancement mechanism in very short channel length devices.
LIST OF REFERENCES


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BIOGRAPHICAL SKETCH

Younsung Choi received the B.S. degree in material science and engineering, and the M.S. degree in physics from Yonsei University, Seoul, Korea, in 1998 and 2002, respectively. He is currently working toward the Ph.D. degree in electrical engineering at the University of Florida, Gainesville and has been with Dr. Thompson since 2004.

He was with the Semiconductor Research and Development Center, Samsung Electronics, Korea, as a process engineer from 2002 to 2004. During that period, he was involved in the dry etch process development of memory device. His current research involves electrical characterizations and theoretical modeling of strained-Si and Ge MOS devices.