IN-SITU CHARACTERIZATION OF HIGH SPEED I/O CHIP-PACKAGE SYSTEMS

By

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The evolution of high speed digital buses is pushing interface speeds up to frequencies of a few GHz making it difficult to create a working digital system in one design cycle and meeting the target time-to-market. With more functionality on the chip, designers have to cope with higher I/O densities, more signals coming out of a chip and tighter geometries. These higher performance requirements have a significant negative impact on system signal integrity. Thus, high-speed circuit and I/O designers cannot predict exactly what will happen after a chip is integrated with a package and a board. The influence of the package on the system performance must be understood and analyzed early in the design cycle and chip-package co-design is becoming essential to achieve time-to-market goal. In the chip-package co-design trends, it's important to construct and validate accurate modeling of the package and the PCB over tens of GHz frequency bandwidths. Conventional ways to model the package depend on the input from three dimensional full-wave EM solvers, two dimensional planar EM solvers, VNA, or TDR. Conventional solutions require excessive computation time (3-D solver) over simplification of the EM physics (2-D solver) or excessive characterization resources and time (VNA and TDR). Thus, there is a potential large discrepancy between the package performance and package model

predictions. This is made worse due to the very short rise/fall times, increasing complexities of IC packages and increasing IC port count.

The primary goal of this dissertation research is to develop a new and efficient experimental strategy that verifies and evaluates package electrical models for high-speed I/O interfaces. To do this, I/O test ICs are designed which can effectively validate signal integrity effects for high-speed I/O chip-package systems including simultaneous switching noise, package power/ground noise and crosstalk. Characterizing and validating the package electrical model with an I/O test IC provides accurate information since it closely matches real IC operating conditions. IBIS macromodels of I/O chip performance are extracted from 65nm CMOS I/O driver measurements using high impedance probes. IBIS macromodel based SPICE simulations and on-board measurements are compared to validate example IC package models over a 3 – 7 GHz range. Using the measured results, the dissertation discusses how to analyze package effects to empirically change the model so that the SPICE simulation can match the measured results. I/O test ICs including differential current-mode logic (CML) and single-ended gunning transceiver logic (GTL) I/O were designed with the Texas Instruments 65nm digital CMOS process. The I/O test ICs will fire different data patterns at different frequencies across multiple I/Os to look at the response of the chip-package system. In summary, the research presents a new experimental technique using I/O test ICs to determine the validity of IBIS I/O-package models at Gbit/sec data rate.

CHAPTER 1
INTRODUCTION

1.1 Trends in High-Speed I/O

A high speed interface channel consists of a chip, a package and a board as illustrated in Figure 1-1. Other elements such as sockets or cables can be included depending upon the application. When the data rate was just a few tens of MHz, these passive elements did not affect the signal and the designer could neglect the parasitic inductance and capacitance in interconnections.

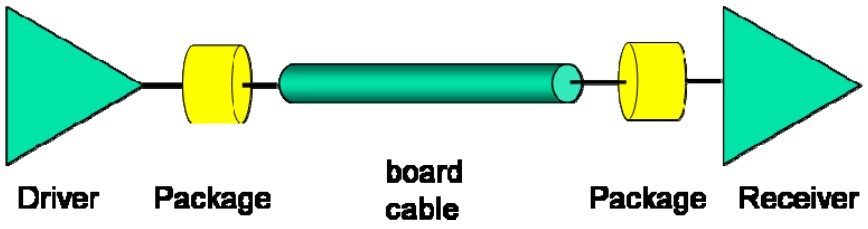


Figure 1-1. Chip-to-chip interface components.

As CMOS technology speed and circuit density increase, the data capacity needed to transmit and receive information through the I/O channel gets larger. According to Rent's rule shown in Figure 1-2 [1.1], the designer needs larger I/O pin counts as the number of gates increases as predicted by Moore's law because the data capacity needed to transmit and receive through the I/O channel gets larger. Figure 1-3 shows the drastic increase in the number of transistors integrated on microprocessors over the past three decades and the current trends in microprocessor's clock frequency [1.2]. As shown in Figure 1-4 (A), if more pins are added to increase the I/O bandwidth, signals get more distorted due to the pin-to-pin crosstalk. In order to meet the high data rate with a limited number of pins, there is fundamental trend in high speed transceiver IC that the resulting I/O works at Gbit/sec speeds and concentrates on minimizing pin count. This is called a point-to-point serial interface. Figure 1-4 (B) shows the basic structure.

The advantage of this structure is that it reduces the number of connections and allows a smaller package and board.

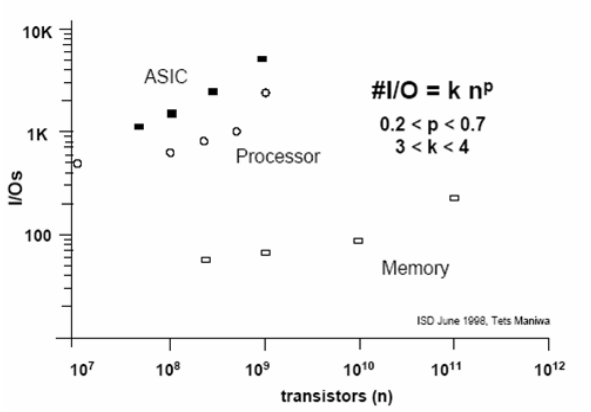
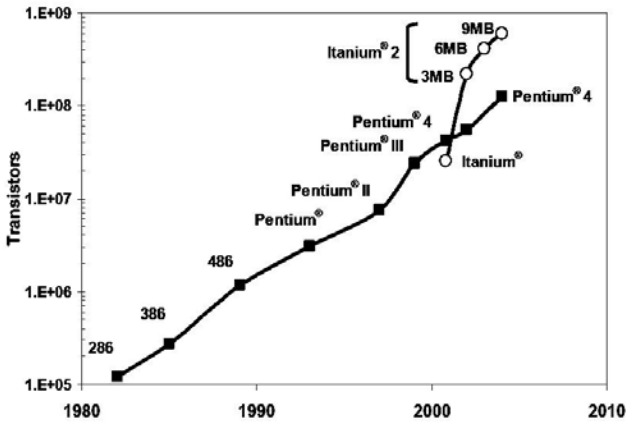
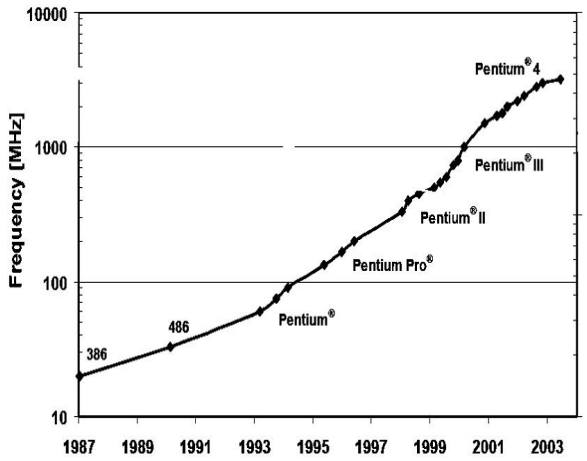


Figure 1-2. Rent's rule.



A



B

Figure 1-3. Moore's law. A) CPU transistor count trend. B) CPU clock frequency trend.

As the I/O bandwidth requirements grow over time, multiple serial interface ICs started being integrated in single chip to reduce the cost and board area. Figure 1-5 shows the evolution of a Gigabit Ethernet transceiver [1.3]. When a single multi-port transceiver is used in contrast to the multiple single port transceivers, the total pin count and board area can be reduced.

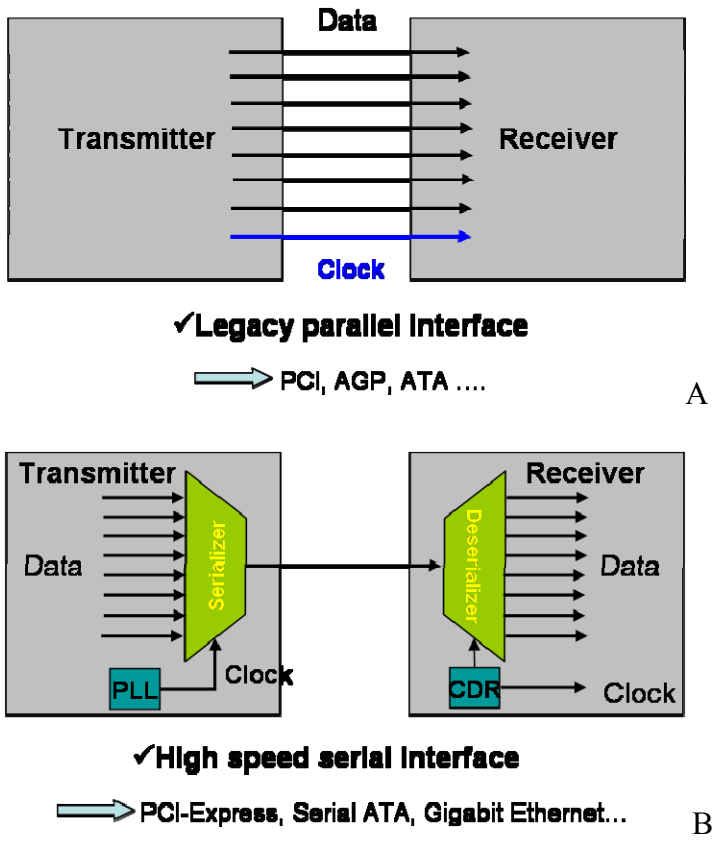


Figure 1-4. Trends in High-speed I/O. A) Legacy parallel interface. B) High speed serial interface.

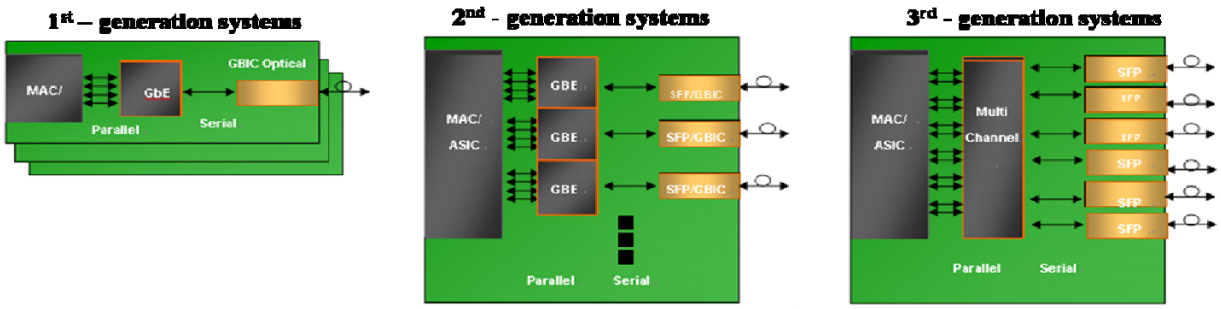


Figure 1-5. Evolution of Gigabit Ethernet transceivers.

1.2 Challenges in High-Speed I/O

Although high speed serial link IC technology is being developed, the package and board technology has not advanced as much and the propagation of signaling is affected by high frequency signal integrity effects associated with the package and PCB. These effects are due to the parasitic capacitance and inductance, and also the transmission line effects of interconnect, which make it really difficult to construct an accurate electrical model.

In the past, I/O designer didn't need accurate information about the package and board before he or she started designing the I/O circuits because the clock speed was just a few tens of MHz and the edge rate wasn't fast enough to consider transmission line effects. But today, the influence of package and board should be accurately predicted early in the design cycle. But, high bandwidth signals, increasing I/O port count, and increased package complexities cause increased discrepancies between prediction and actual I/O performance. This is the major bottleneck in high-speed I/O implementation and makes it hard for the I/O designer to optimize the circuits and succeed in a quick time-to-market. Moreover, faster edge rates require accurate modeling of the IC internal structure to over tens of GHz frequency bandwidth. The relation between edge rate and harmonic content for the square wave is explained in chapter 2. There are many types of electrical modeling tools available to analyze package inner conductor layouts and compute RLGC parameters. The quasi-static tools are the simplest to use and they are usually the fastest. These tools usually assume TEM (Transverse Electro Magnetic) transmission conditions. This is truer for stripline structures but only approximately true for microstrip structures. A example tool for this transmission line is the 2D boundary element method (BEM) which is a moment method-based technique. Another tool package designers frequently use is 3D field solver which can provide information about vertical structures and plane paths. It can be a moment method-based also but the solver discretizes the structure into segments to allow

solutions of Maxwell's equations in terms of current distribution. Each of these methods has significant problems at faster signal speeds due to non-TEM propagation and radiation losses and this result in breaking down the accuracy of the package electrical model. Even worse, due to the increase in the number of power/ground planes in multilayer packages, full-wave rigorous electromagnetic field solutions are becoming impractical because of the extremely high computational requirements and the difficulty in generating equivalent circuit models for time-domain circuit simulators [1.1]. Additionally, the models produced by these programs are just now beginning to be verified by direct measurements such as vector network analyzer (VNA) or time domain reflectometry (TDR). If package engineers directly measure the package with a VNA or using TDR, parasitic capacitance or inductance associated with a package can be extracted and validated in the frequency domain (s-parameter data) and time domain (impedance data). However, this validation method can be used only when a single I/O port is switching. Because high frequency package limitations typically appear as a signal integrity issue, especially package power and ground fluctuations due to simultaneous multiple I/O switching, multiple TDR and VNA heads for each I/O port are needed and there is often no accurate way to repeatedly connect this equipment to the package for a calibrated measurement. Figure 1-6 shows the example of BGA package signal routing being currently used for board design.

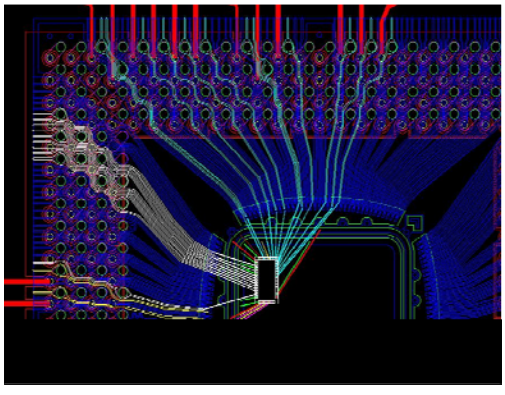


Figure 1-6. BGA package signal routing.

When I/O circuits are designed with inaccurate package models and experience non ideal loading effects, the high speed interface channel fails to work at speed. The whole channel may have to be redesigned under severe time pressure.

In order to solve this problem, the author designed I/O test ICs and performed at speed chip-package experiments to observe and verify the package performance prior to IC prototyping. Using this method, a package engineer can validate modeling data for package and get accurate signal integrity information including package ground/power noise, simultaneous switching noise, pin-to-pin cross talk and inter-symbol interference. This validation step with a test IC more closely matches the real operating conditions than any other characterization method such as simulation, using TDR, or using a VNA because one can see the effects of many IO ports switching. Through this additional validation step, the high speed I/O interface engineer will receive an accurate package model prior to chip tape-out that would greatly simplify his or her design task.

In summary, I/O test IC based chip-package system characterization allows 1) circuit and package designers to validate the package electrical model with respect to signal integrity parameters and 2) system designers to verify the chip-packaging system before commercial chips go to mass product level.

1.3 Package Electrical Model Verification

Package signal integrity is becoming crucial in multi-layer packages as device operating frequency is well into the multi-GHz range. Particularly, accurate package electrical models of power/ground supply networks and routed traces are key to the success in designing high speed I/O chip-package systems. Signal integrity parameters such as cross talk, simultaneous switching noise are directly related to the accuracy of a package electrical model. Therefore, in this research, signal integrity parameters are chosen to evaluate and validate the package electrical

performance and model. There are many papers suggesting different methods of package characterization and modeling [1.2]-[1.4]. However, only stand alone packages have been characterized so far and electrical performance, especially signal integrity, can be different after a package is assembled with real ICs. For the successful verification of package electrical models, I/O test ICs have been designed to provide a real chip-package signal environment. A novel IBIS (I/O Buffer Information Specification) macro model-based verification tool is presented in this research and Figure 1-7 shows a generic verification procedure. High impedance probing is performed to capture the signal right at the chip bond pads. The probe point includes I/O driver outputs and chip VDD/VSS nodes. Simulation and measurement results are compared with respect to the signal integrity performance such as waveform distortion due to a package inner trace, cross talk, inter-symbol interference and simultaneous switching noise. If the package model has some high frequency inaccuracies, discrepancies will occur between simulation and measurement. The advantage of this method is that different types of packages can be validated with the same I/O test IC, as illustrated in Figure 1-8. This will greatly reduce the time involved in overall package design procedures and is a method that successfully provides accurate package model to the I/O design engineer.

1.4 Full Channel Validation

The I/O test IC based characterization method can be applied to the full I/O channel validation which consists of driver, package, PCB board and receiver. After the package model validation, a full channel validation can be performed with low performance and low cost ATE (Automatic Testing Equipment). In this case, a more sophisticated I/O test IC which is presented in Appendix C permits the use of low performance ATE. Figure 1-9 shows how to validate the signal integrity performance for a full channel which consists of the driver-package-board-package-receiver. A clock and data recovery circuit is needed for a receiver IC in order to have

low speed data transferred to ATE and compared with transmitted data. Low cost validation is very important in high speed interface IC testing since high-speed testers above 1~2 GHz are prohibitively expensive for low cost IC production parts. Standard ATE performance has difficulties keeping pace with the data rates of the high-speed I/O ports [1.5]. The current generation of ATE on the market are NOT capable of testing gigabit transceivers at speed [1.6]. As an example, the Teradyne Catalyst tester can test up to 3 GHz but costs more than $1 million dollars. In addition to that, using the same I/O test IC supports multiple I/O standards (PCI Express, XAUI, HyperTransport, SATA, OC-192, etc) validation. This can be realized by using a wide tunning range PLL which operates over continuous range of frequencies and the technique explained further in Appendix C.

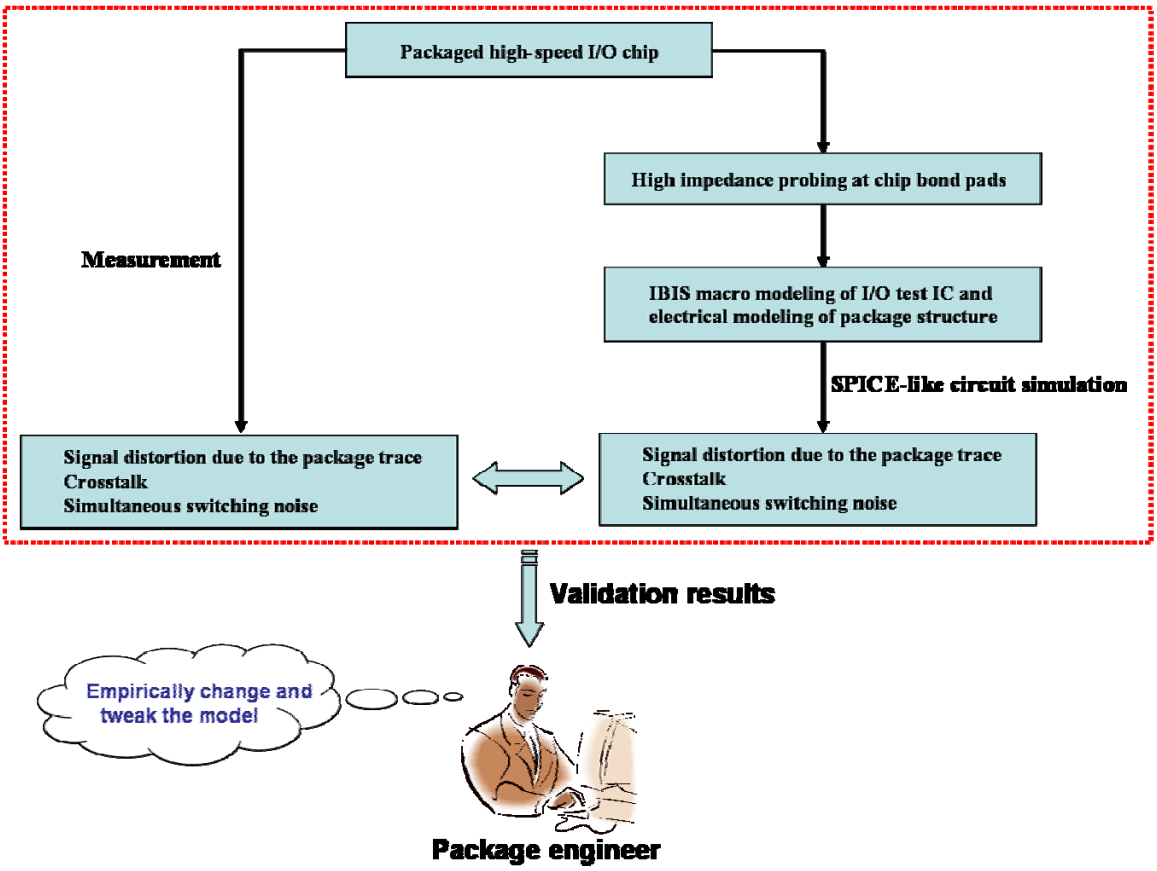


Figure 1-7. Overall validation procedure.

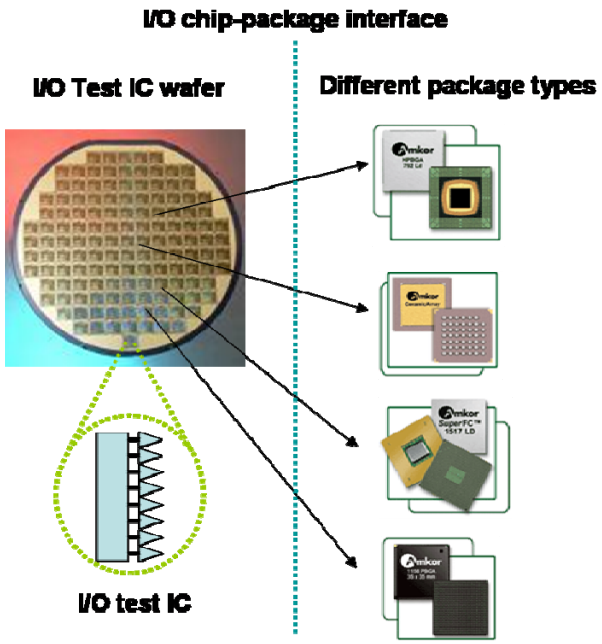


Figure 1-8. Validation of different packages with same I/O test IC.

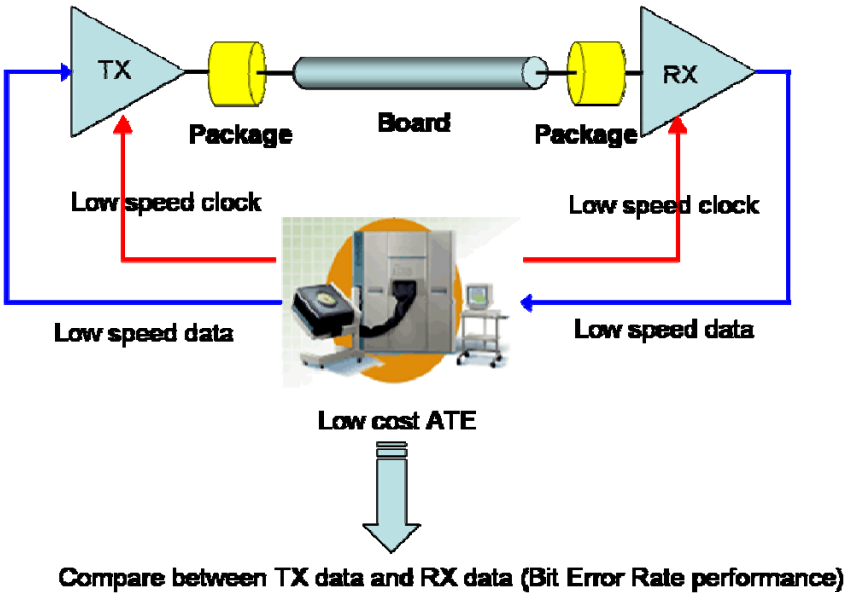


Figure 1-9. Full channel validation.

CHAPTER 2
THE EFFECT OF THE PACKAGE ON SIGNAL INTEGRITY

2.1 Introduction

IC technology trends toward higher speed and higher density devices have pushed package performance to its limits. As signal rise time becomes less than 100ps, the significant frequency content of digital I/O signals extends up to at least 10GHz. This necessitates the fabrication of packages capable of supporting very fast varying and broadband signals without degrading signal integrity [2.1]. The problem is that the package inner structure is getting more complicated as the data rate gets faster because more I/O pins are needed to take care of the fast data transfer rate. The larger and denser packages with longer signal paths give rise to transmission line effects requiring precise impedance matching. Moreover, there are serious ringing effects since the signal will get reflected back and forth. The closer spaced signal traces will end up with more cross talk due to the increased mutual inductance and capacitance. Package designers should consider transmission line losses as well. The attenuation of high frequency signals is primarily due to frequency dependent conductor loss (skin effect) and frequency dependent dielectric loss (loss tangent). Skin effect, which is proportional to the square root of frequency, leads to frequency dependent AC resistance. In lossy materials within package substrate layers, the frequency dependence of the dielectric constant causes dielectric leakage at very high frequencies. These effects result in reducing the signal amplitude and degrading the signal edge rate, which causes poor BER performance. Die shrinks, increasing package density on pc boards, and larger numbers of signals switching simultaneously are making power distribution a critical issue in the package [2.2]. The IR drop and ground bounce must be minimized in the package power and ground network. This chapter begins with the introduction of different package types and the evolution of modern package design. After that, package signal integrity is presented.

Why signal having fast edge rates experience serious signal distortion is explained in the first section which is followed by several sections explaining transmission line effects, power and ground bounce noise, simultaneous switching noise (SSN), cross talk and inter-symbol interference (ISI).

2.2 Classification of Modern Packages

IC packaging technology has been developed to meet the high speed I/O trends in the area of electronic equipment. Increased device complexity generates an explosion of new packaging technology to meet tighter electrical and thermal performance requirements. The fundamental roles of the IC package are

- Transferring signals into and out of the die.
- Delivering power to the die.
- Removing the heat away from the die.
- Protecting the die from outside.

Packages can be classified in many different ways, but in this section, they are categorized into two ways.

Lead frame vs. ball grid array: When connecting the package to the PC board, IC packages come in two primary varieties; these are lead frame packages and ball grid array (BGA) packages. Dual inline package (DIP), quad flat package (QFP) and small outline package (SOP) are lead frame type packages and were used in low speed, low pin count applications. The DIP was developed in the 1970's and pins are inserted into through-holes in the circuit board and soldered in place from the opposite side of the board [2.3]. Because of their poor high frequency performance and large area, this type of package was replaced by surface mount technology (SMT) packages. QFP and SOP are examples of SMT packages that allows higher pin count with a smaller package size. The lead frame package has high pin count limitation because the lead

frames are placed around the side of package. For example, the pin count of QFP is less than about 300 pins at present. As today's high performance chips require many I/O ports, significantly more than 300 pins, solder balls are replacing lead frames as the interconnect medium between packages and boards. This package is called ball grid array (BGA) and it was developed in the early 1990's. For BGAs, the package area increases linearly with pin count and can yield a more compact solution than a QFP which has an exponential relationship between package area and pin count [2.4]. In addition to that, the BGA package has low pin inductance in contrast to the lead frame package, allowing better high frequency performance. Nowadays, most high performance ICs use BGA packaging technology. Figure 2-1 [2.4] illustrates the size and weight reduction of IC packages over time. As shown in Figure 2-2 [2.4], more than 1000 package pins are expected to perform with an over 500MHz on-chip clock frequency. Figure 2-3 shows various package types.

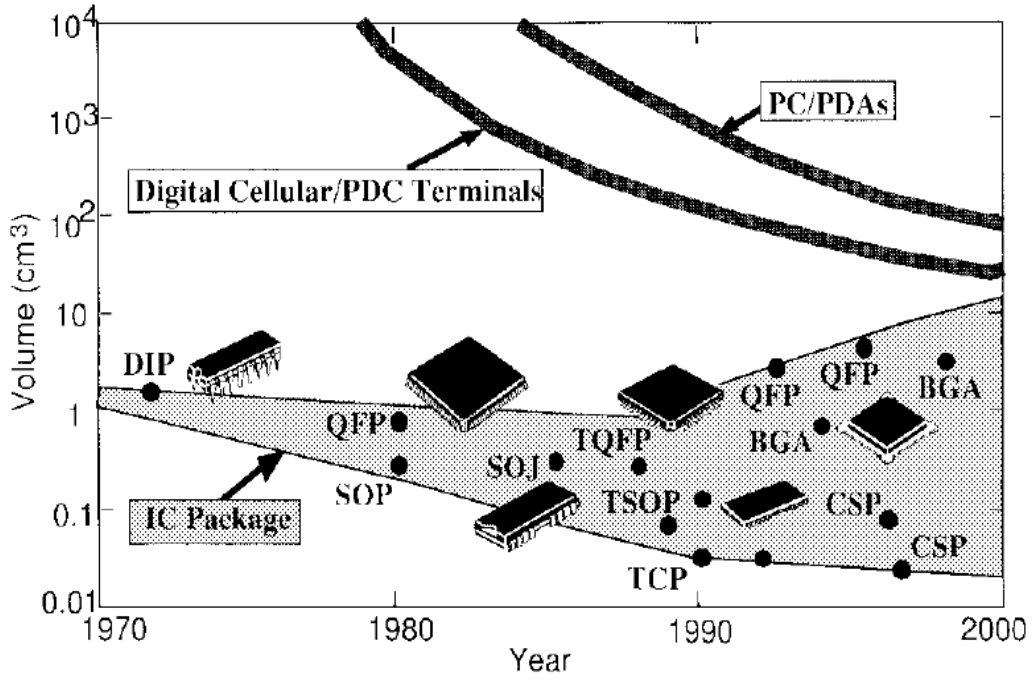


Figure 2-1. The size and weight reduction in IC packages.

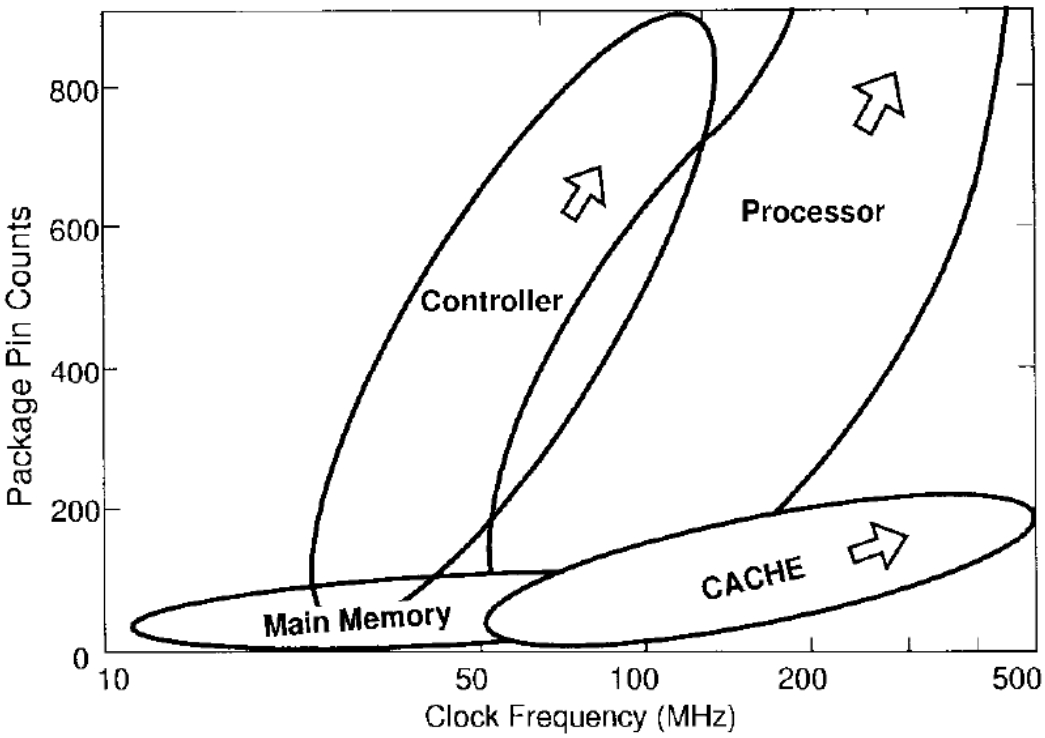
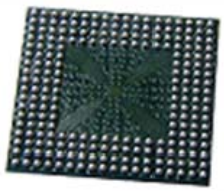


Figure 2-2. Package pin count versus clock frequency.

Dual inline package (DIP) **Small outline package (SOP)** **Quad flat package (QFP)** A



Ball grid array (BGA) B

Figure 2-3. Type of connection to PCB board. A) Lead frame package. B) BGA package.

Wire bond vs. flip chip: Wire bonding provides an electrical connection between the die and package by connecting the chip bond pads to the package fingers with aluminum or gold wires. An example of wire bonding is shown in Figure 2-4 (A). Wire bonding has inferior electrical properties, especially at high frequencies because the bond wire inductance in combination with the on-chip capacitance creates LC low pass filters. The inductance of a package bonding wire is typically about 1nH/mm. Flip-chip mounting require flipping the die upside down and attaching it directly to the substrate using solder balls. Solder balls have smaller inductance than bond wires, which allows better high frequency performance. Flip chips also allow the direct connection of bond pads throughout the die surface, resulting in higher pin counts and smaller chip size. Figure 2-4 (B) shows the flip chip attachment.

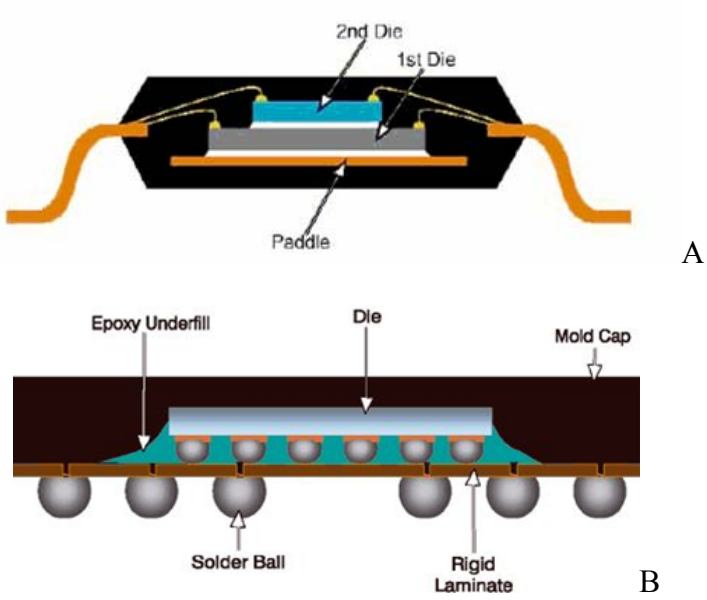


Figure 2-4. Type of die attachments. A) Wire bond package. B) Flip chip package.

A wire bond package doesn't seem to be a proper choice for high speed interface circuits because of bond wire inductance, but it has some advantages over flip-chip BGA.

- Low cost and high volume technology with easy probe access for testing
- Thermal and mechanical characteristics are better.

Because of these reasons, there is strong emphasis on using wire bonded devices, even in high performance applications. A comparison between wire bond and flip chip technology is shown in Table 2-1 [2.5].

Table 2-1. Comparison between wire bond and flip chip.

	Wirebond	Flip-Chip
Inductance	Much higher (1-5nH)	Much less (0.1nH)
Crosstalk	High	Virtually none
Cost	Cheap	High
Mechanical	Good	Physical tolerances tight since die must align to package.
Thermal	Back of die attached to package for maximum surface area contact and maximum heat transfer out.	Ugly: thermal coefficients of die and package must be similar or expansion will break bonds. Cooling is hard because die lifted off package by solder balls.
Die Size	Limits I/O since pads only around periphery.	Die size can be minimized even when many I/O's.

A paper shows the possibility of achieving a 40 Gb/s serial link with wire-bonded plastic BGA packages [2.6].

2.3 Package Signal Integrity

As the signal speed approaches the GHz range, the device package is not transparent to the IC and all packages have electrical properties that affect the system performance. These properties are due to the interconnect transmission inside the package. Small parasitic elements come into play and seriously degrade the signal waveform. When dynamic currents having fast rise and fall time meets the parasitic inductance in the package power and ground network, they creates power and ground rail fluctuations. Interconnects should be modeled using distributed

elements because they have transmission line effects and cause large reflections unless their impedance is tightly controlled. The impact of a package on IC performance increases as edge rate speeds increase. These effects are discussed in the following sections.

2.3.1 Edge Rate and Knee Frequency

Edge rate (rise/fall times) of a signal is important with respect to the signal integrity. According to the Fourier series, the edge rate determines the frequency content of the signal and an indication of how far in the frequency spectrum the signal's power lies. The knee frequency has been defined to provide a rough rule of thumb for this limit of a signal's frequency content and is defined as

$$f_{knee} = 0.35 / t_r$$

where, (2-1)

t_r *is rise time of the signal's edge*

The knee frequency is the frequency below which most of the energy of digital pulse is concentrated and Appendix B explains how to derive this formula. Figure 2-5 [2.7] shows the relationship between knee frequency and edge rate in digital signals. As illustrated in figure 2-6 [2.8], the signal edge gets shorter as more harmonic content is added. A common mistake is that the frequency content of a signal is determined mainly by its period. However, most signal integrity effects come from the signal edge rate, not from the signal period. This is why equation 2-1 is based on the rise time t_r. The common practice in digital design is to make signal edge rate to be 10% of period, which means up to 5th harmonic should be transmitted in order to have a relatively smooth square wave.

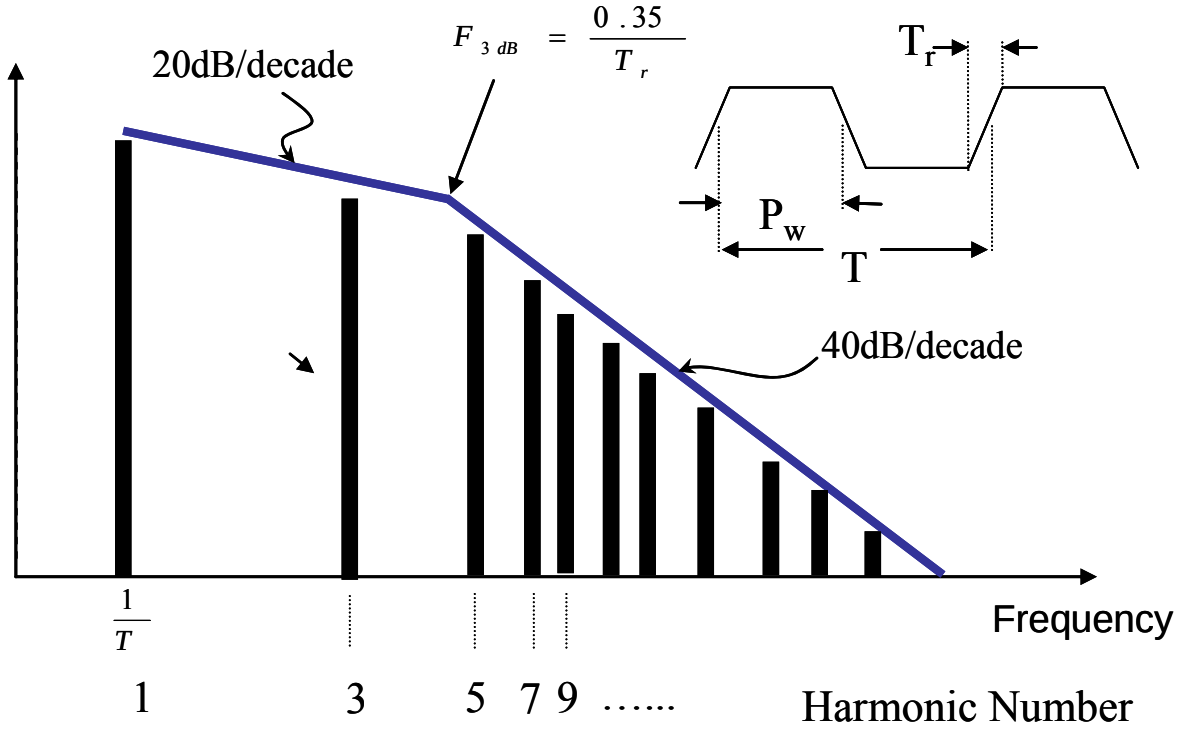


Figure 2-5. Relation between knee frequency and edge rate in digital signals.

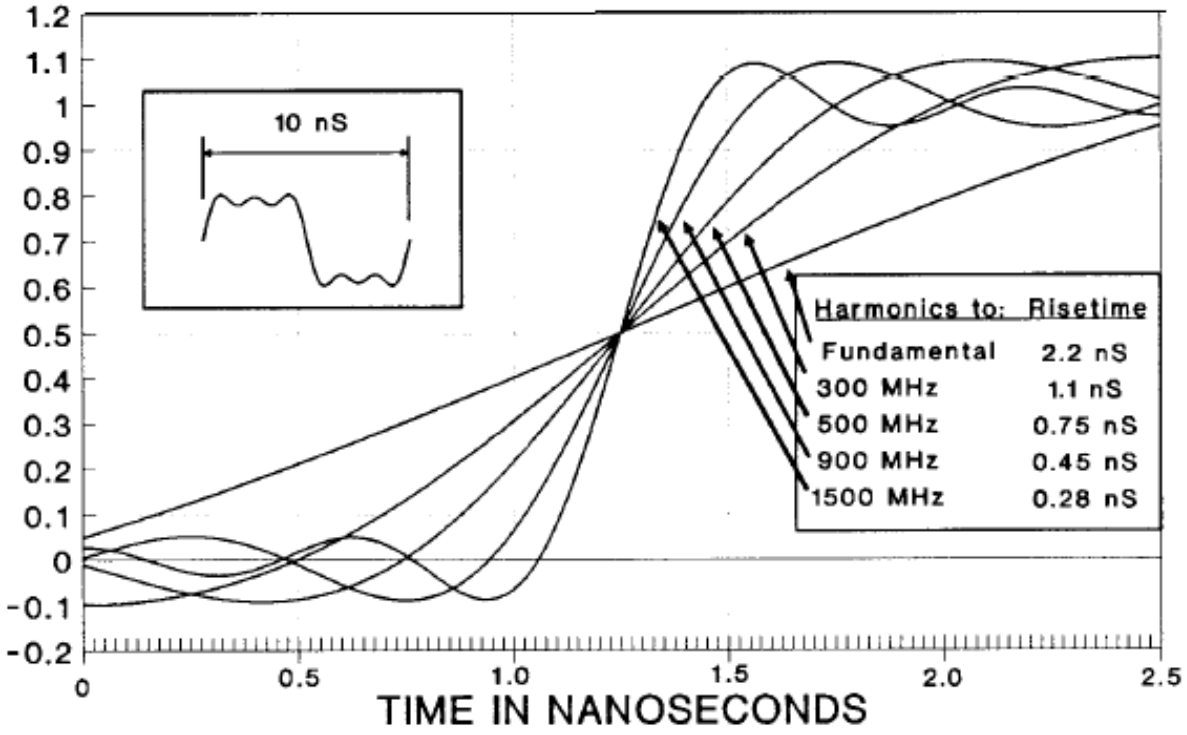


Figure 2-6. Rise time versus harmonic content for a 100MHz square wave.

2.3.2 Transmission Line Effects and Signal Reflection

Several decades ago, the highest frequency in digital microprocessor circuits was below 10 MHz. In the modern multi-Gbps serial links with edge rates down to 100ps, all interconnects of signal path must be treated as transmission lines. Equation 2-2 is the rule of thumb which determine when interconnects must be treated as a transmission line.

$$l_{trace} > l_{effective} / 2.5 \quad (2\text{-}2)$$

This equation means that trace has transmission line effects if the signal rise time is comparable to the round-trip propagation time because the voltage potential is not uniform along the trace. Transmission lines cause signal delay, dispersion, and attenuation as the signals propagate down the lines. Also, when a signal travels down a transmission line of characteristic impedance Z_0, and the line is terminated at the end with a load Z_L not equal to Z_0, all or part of the signal will reflect back off of the load at the end of the line [2.9]. Reflected signals interfere with propagating signals while they travel back to the source end. When there is impedance mismatch in source end, another reflected signal is generated and causes additional interference. Figure 2-7 [2.7] shows the example of a transmission line with multiple reflections. The signal may continue on for several round trips getting reflected up and down the transmission line and cause ringing and disruption of data signals until the signal finally becomes dissipated [2.9]. There are several ways to reduce the impact of reflections. The first method is to decrease the frequency of the signal such that the signal edge rate is larger than the round trip delay of signal. However, this approach is impossible for high speed systems with ICs, packages and boards. The second method is to terminate the transmission line with a termination resistor equal to the characteristic impedance of the transmission line. There are two termination methods, which are source terminations and load terminations. Source termination means that driver impedance is

controlled such a way that it has the same characteristic impedance as the transmission line. Load termination uses terminating resistor at the end of the transmission line to eliminate the reflection. Most of today's very high speed interface products adopt source and load terminations, which is called double termination. As the package trace length becomes longer, an on-die source termination resistor is attached to the I/O driver in order to remove the package stub effect. Because of the on-die terminations, the package is no longer a stub off of the motherboard transmission line; it is now an integral part of the line [2.10]. In this case, the package trace impedance should be tightly controlled.

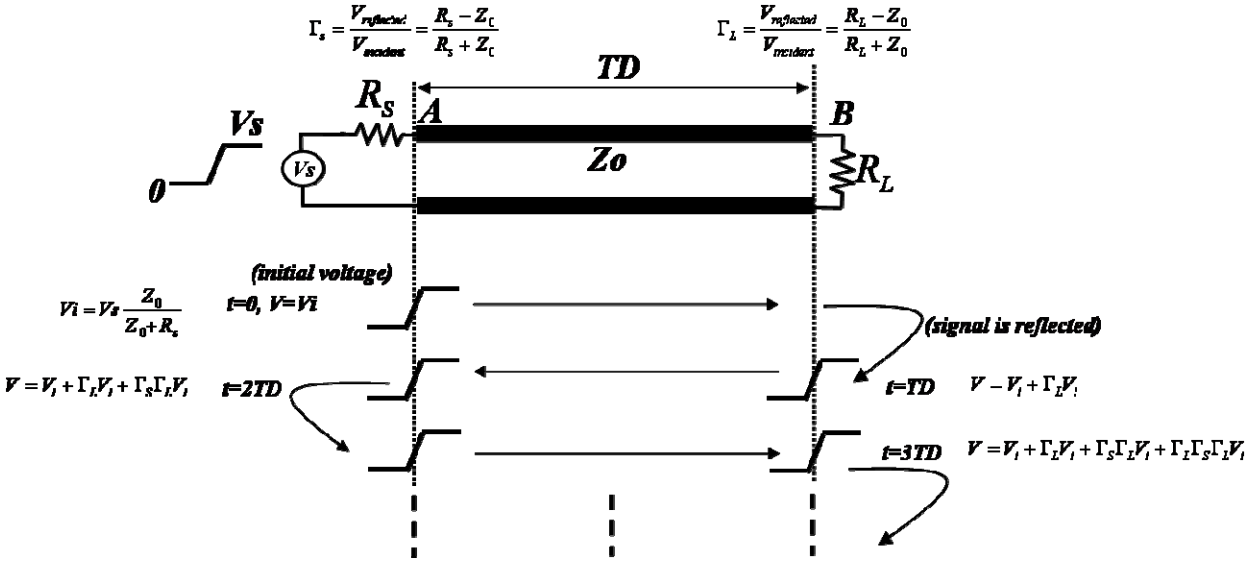


Figure 2-7. Example of transmission line with multiple reflections.

2.3.3 Power and Ground Bounce Noise

In mixed signal IC design, power and ground should be a good analog ground. In other words, the impedance associated with power distribution network should be kept to be very low. The problem is that when I/O drivers charge and discharge output capacitive nodes, sudden currents must be supplied by the board-level power through the inductive chip package and these generate ground and VDD bounce noise due to parasitic inductance. Figure 2-8 shows the basic

mechanism of generating ground and VDD noise. This type of noise is called $L\,dI/dt$ noise and proportional to the edge rate and parasitic inductance of the power supply network. The trend toward fast ICs has led to an increase in ground and power fluctuation (ground bounce and power droop). These effects can cause logic failure and serious jitter degradation of clock circuits such as Phase-Locked-Loop (PLL) and Clock and Data Recovery (CDR). This noise also results in corrupting the reference level of a receiver circuit. I/O drivers are designed such that they draw huge current from power supply network in order to drive large off-chip capacitive loads with reasonable amount of speed. This process causes large fluctuation in the power supply rails. This phenomenon is getting worse as the channel length of CMOS transistors goes to the deep submicron level. In addition to the parasitic inductance, non ideal return current paths act like a parasitic inductance and worsen the power rail fluctuation.

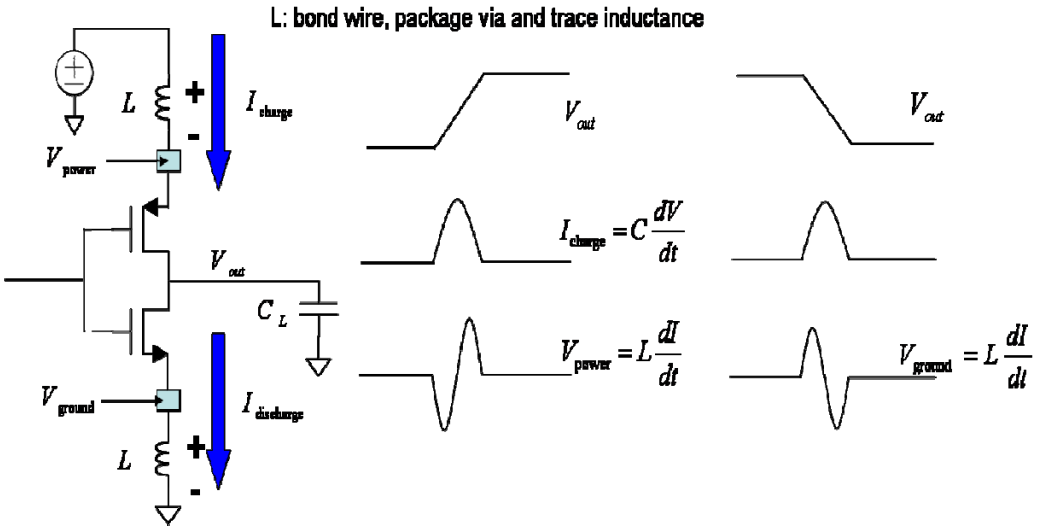


Figure 2-8. Basic mechanism of ground and VDD noise.

2.3.4 Simultaneous Switching Noise

Switching multiple output drivers on the same device is called simultaneous switching and this produces the worst case ground and VDD bounce noise. When all the drivers are switching

simultaneously, a large $L\,dI/dt$ will be generated and coupled to the power connection of the quiet nets. Since the SSN is proportional to the number of switching gates and many package design parameters, circuit designers must take these packaging effects into account at an early phase of circuit design [2.11]. For the simultaneous switching measurement procedure, one input is connected to a fixed low or high state while a specified number of other inputs are switched simultaneously. Figure 2-9 [2.7] shows the simultaneous switching noise mechanism.

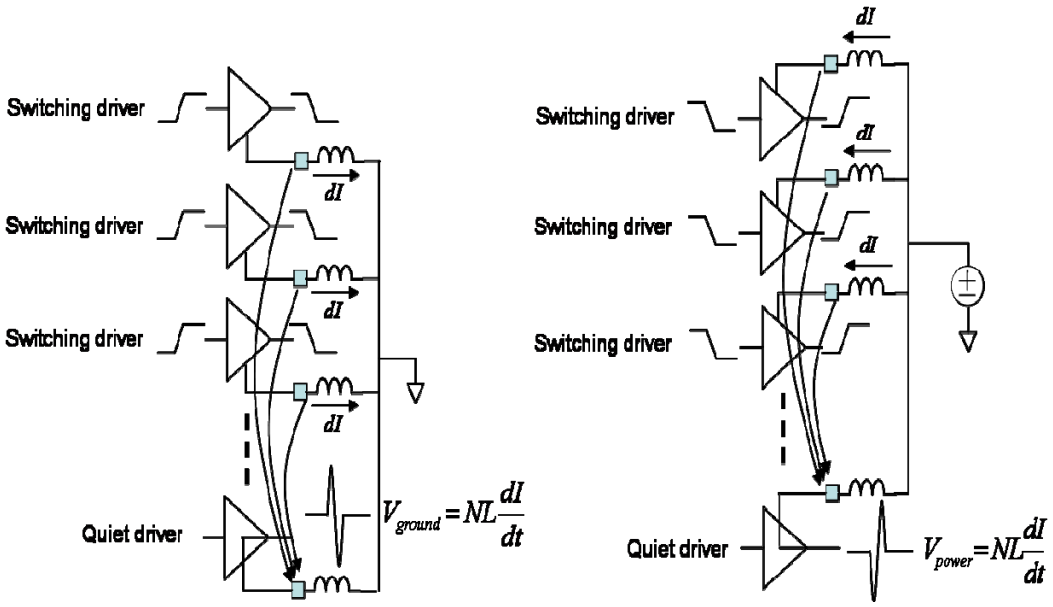


Figure 2-9. Simultaneous switching noise mechanism.

2.3.5 Crosstalk

As illustrated by figure 2-10 [2.5], crosstalk is the coupling of energy from one line to another via mutual capacitance (electric field) and mutual inductance (magnetic field). The amount of crosstalk due to the mutual capacitance C_m and mutual inductance L_m are given by

$$I_{noise,C_m} = C_m \frac{dV_{driver}}{dt}$$

$$V_{noise,L_m} = L_m \frac{dI_{driver}}{dt}$$

and the noise increases dramatically as the demands for the data rates go higher. Crosstalk will change the performance of the transmission lines in a bus by modifying the effective characteristic impedance and propagation velocities, which will adversely affect system-level timing and the signal integrity [2.7]. Fast edge rates couple more energy to adjacent lines because of the larger dV/dt and dI/dt of driver signal.

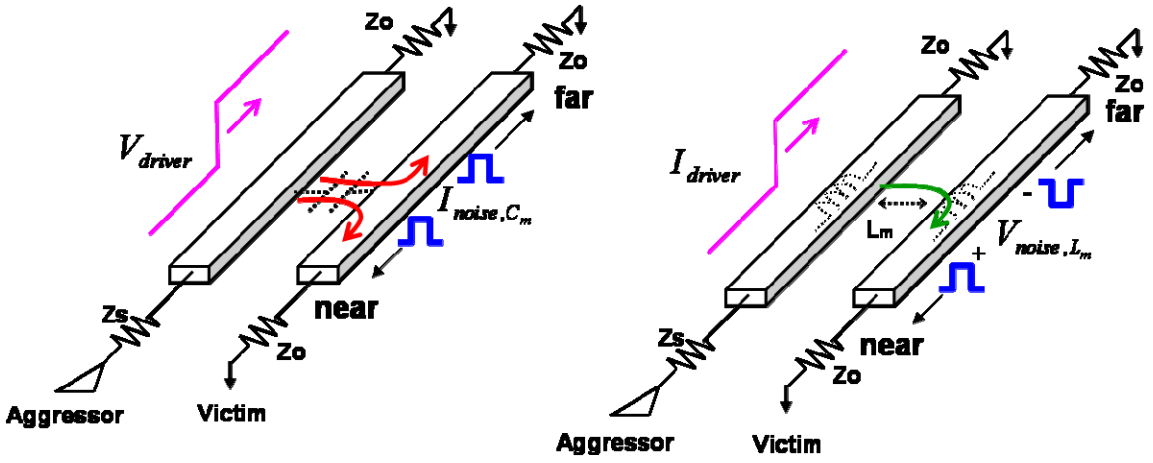


Figure 2-10. Crosstalk mechanism. A) Capacitive Crosstalk. B) Inductive Crosstalk.

Packages with tight pitch are more susceptible to pin-to-pin cross talk. When an aggressor injects a pulse, different types of coupling can be observed at the near end and far end of the line, which are called NEXT (near end cross talk) and FEXT (far end cross talk). As shown in Figure 2-11, the NEXT doesn't accumulate because it arrives at different time and it has duration of 2 times of the line delay. In the receiver side of victim line, because the coupled noise arrives at the same time, the FEXT accumulates and create a peak. FEXT occurs at one line delay. The amplitude of NEXT, as shown in Figure 2-11, is the sum of inductive and capacitive coupling and has the duration of a round trip delay of the transmission line. FEXT due to the inductive and capacitive coupling has the opposite polarity. Inductive coupling noise is usually larger than the capacitive coupling noise and the FEXT has negative amplitude. In order to minimize the

coupling effects, trace pitch should be large, which results in increasing the package and board size and cost. For example, the space between the differential lines should be at least 5 times larger than the dielectric thickness. If the designer needs a total 250 differential lines using the package having the ball grid pitch of 2.54mm, the board size is going to be around 25cm×25cm, which is not practical.

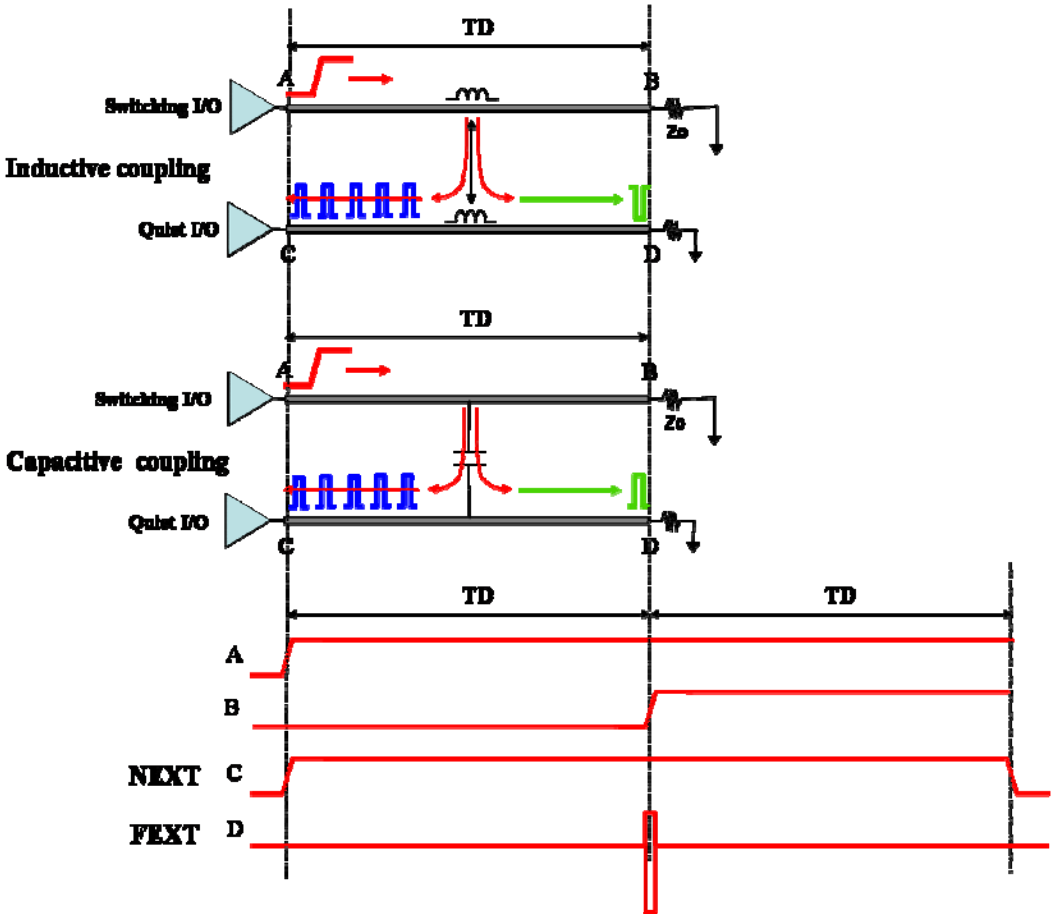


Figure 2-11. Near-end cross talk (NEXT) and far-end cross talk (FEXT).

2.3.6 High Frequency Transmission Line Loss Effects

At low frequencies, the current flows through the whole conductor and signal loss is dominated by the DC resistive losses. As the signal speed increases, new effects come out and start distorting the signal waveform. There are two frequency dependent losses, which are skin effect and dielectric loss. At high frequency, inductance for the inner conductor increases

pushing current to the outer conductor since current starts flowing through the path of lowest impedance. This is called skin effect and it causes the current to flow in a smaller area increasing the AC resistance. The resistance associated with skin effect is proportional to the square root of frequency according to 2-3

$$R_{skin} = \frac{\rho}{w\delta_s}$$

where,

$$skin\ depth\ \delta_s = \sqrt{\frac{1}{\sigma\pi\mu f}} \qquad (2\text{-}3)$$

w : *line width*

ρ : *resistivity*

σ : *conductivity*

Therefore, the total resistance consists of DC resistance and AC resistance. At low frequency, the total resistance stays at the DC resistance and it increases with $\sqrt{f}$ when skin depth is less than the conductor thickness. Figure 2-12 shows the frequency dependent resistance for microstrip line [2.5] and total resistance R_{total} that is given by

$$R_{total} = R_{DC} + R_{AC}\sqrt{f}$$

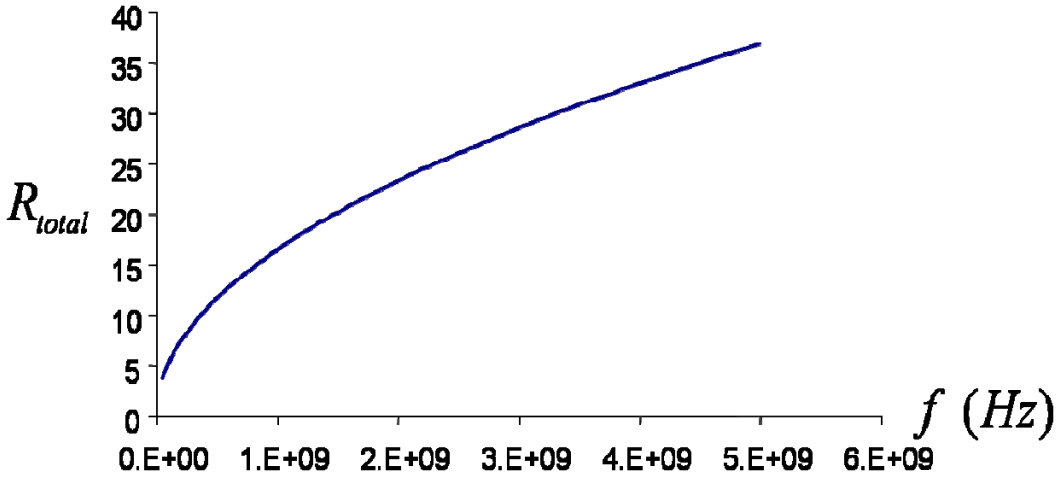


Figure 2-12. Frequency dependent resistance for microstrip line.

Additional high frequency effects caused by amplitude reduction and edge rate degradation is related to dielectric loss. Real dielectric materials have resistance and their value is frequency dependent. The mechanism for current flow in a dielectric is by the re-orientation of permanent electric dipoles in the material [2.12].

While a high frequency signal is traveling along the transmission line, the dipoles in a dielectric rotate back and forth. This gives rise to an AC current and the conductivity increases linearly with frequency because the motion of dipoles increases. Dielectric loss can be expressed in terms of loss tangent $\tan\delta$.

$$Dielectric\ loss = \pi f \tan\delta\sqrt{LC}$$

Dielectric loss of some common interconnect dielectrics are shown in Table 2-2 [2.12]. Relative cost means the cost of each material when the cost of FR-4 is 1. The transmission line loss is dominated by the skin effect at low frequencies. But as the frequency increases, dielectric loss associated with the loss tangent becomes dominant to over all loss.

Table 2-2. Dielectric loss of some common interconnect dielectrics

Material	ε	$\tan\delta$	Relative cost
FR-4	4.0-4.7	0.02	1
DriClad(IBM)	4.1	0.011	1.2
GETek	3.6-4.2	0.013	1.4
BT	4.1	0.013	1.5
Polymide/glass	4.3	0.014	2.5
CyanateEster	3.8	0.009	3.5
NelcoN6000SI	3.36	0.003	3.5
RogersRF35	3.5	0.0018	5

2.3.7 Inter-Symbol Interference (ISI) and Data Dependent Jitter (DDJ)

As signal travels along the lossy transmission line, the bandwidth of the signal is decreased because the high frequency components of signal are reduced, causing edge rate degradation. This phenomenon can be observed by creating an eye diagram with a random data pattern. An

eye diagram is created by laying individual periods of transitions on a net on top of each other [2.7]. If a signal bit time is small compared to the degraded edge rate, the next bit is affected by the unsettled previous bit and the eye diagram collapses. This is called inter-symbol interference (ISI) and is normally due to the dispersion of signals by attenuation and reflection in the transmission line. As shown in Figure 2-13, the amplitude and edge rate is degraded when a 10 Gb/s differential pseudorandom bit stream goes through 20cm differential PCB trace modeled by the W-element in HSpice. The W-element models frequency dependent losses and can be used to model lossy coupled transmission lines. The limited bandwidths of the packages and boards are another source of ISI and this is referred as data dependent jitter (DDJ) which depends on the random data pattern. In this case, previously transmitted data symbols create noise for the next transmitted data. Figure 2-14 shows the example of DDJ.

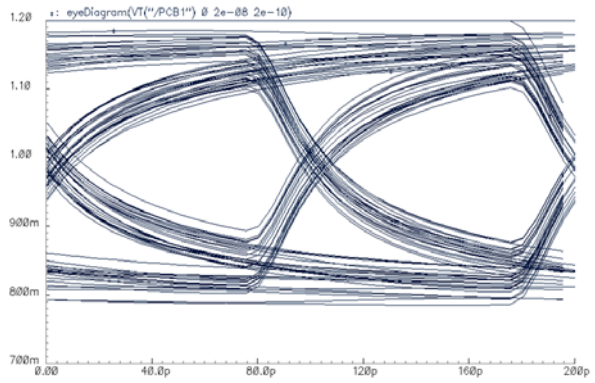


Figure 2-13. Eye diagram of a 10Gb/s PRBS after 20cm PCB trace.

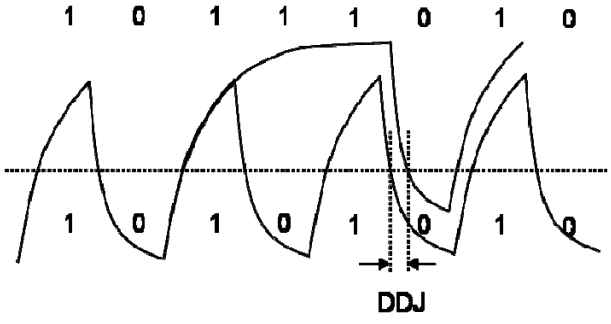


Figure 2-14. Example of data dependent jitter.

In summary, the background and basic mechanism of signal integrity issues such as signal reflection, power and ground rail fluctuation, SSN, crosstalk, frequency dependent losses, and ISI have been explained. The discussion focuses on how signal waveform can be distorted while they go through the package. The next chapter presents the circuit designs for I/O test ICs with respect to the architecture and circuit design in detail.

CHAPTER 3
DIFFERENTIAL I/O TEST IC DESIGN

3.1 Introduction

High speed I/O chip-package communication can be categorized into two areas, differential signaling and single-ended signaling. Differential I/O is normally used for Serializer-Deserializer (SerDes) products such as PCI express, Serial-ATA, and Gigabit Ethernet. The increasing number of ports and signal speed makes it hard to model and characterize the signal path which consists of package, socket, and PCB traces. In this research, a 4 port differential I/O test IC was designed to look at the signal integrity effects of the differential I/O chip-package system and validate the package electrical model having differential inner traces. This chip consists of a quad differential CML driver, a CML clock and data receiver, an on-chip bias circuit, and a de-skewing clock distribution. Figure 3-1 shows the overall block diagram of 4 port CML I/O test IC. This chip was designed and fabricated using the Texas Instruments 65nm digital CMOS process. Demonstration simulations were performed with Amkor RF package in order to show the performance and functionality.

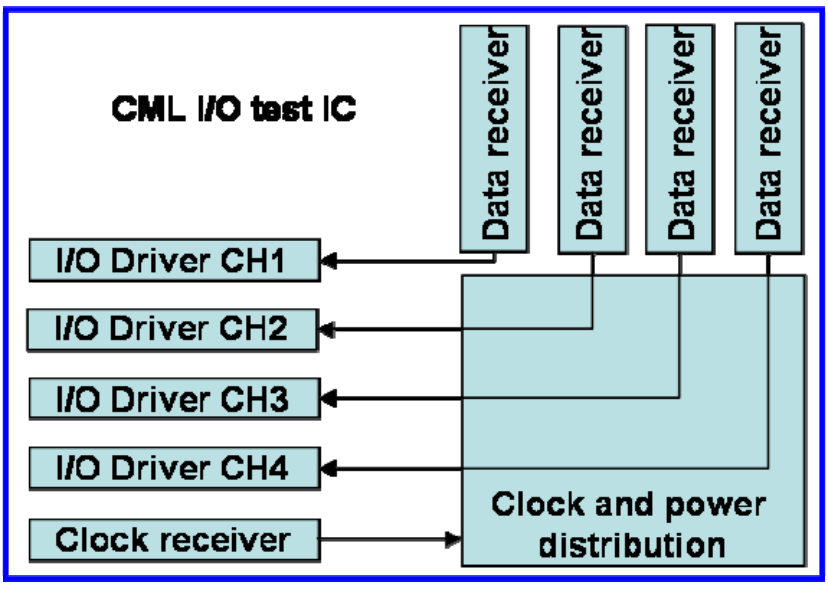


Figure 3-1. Overall block diagram of 4 port CML I/O test IC.

3.2 Design Details for 4 Port CML I/O Test IC

A 4 port CML I/O test IC consists of a core circuit block and CML differential I/O drivers. The core circuit block is composed of a CML clock and data receiver, an on-chip bias circuit, a de-skewing clock distribution. CML is differential amplifier which operates with a large input signal and it is important to have a good tail current source. Because there are many tail current NMOS transistors inside the chip, an on-chip bias circuit was designed to provide a reference current to the local voltage domain. The CML clock and data receiver take the clock and data signals from external test equipment and recover the signal waveform. In order to generate SSN, all quad drivers should fire the data at the same time. De-skewing clock distribution removes the clock skew between the flip-flops which provides synchronized data signals to the drivers.

3.2.1 On-Chip Bias Circuit

An on-chip bias circuit was designed using a wide swing constant transconductance reference circuit [3.1]. This circuit is based upon a bootstrapped self bias circuit having a source degeneration resistor, which shown in Figure 3-2 (a). The source degeneration resistor makes this circuit stable by reducing the positive feedback loop gain to be less than one. When I/O drivers fire fast switching signals to the package, there are power and ground rail fluctuations. This affects the output of the bias circuit. As shown in Figure 3-2 (b), the wide-swing cascode-current mirror was used in order to increase the output impedance and reduce the voltage head room. There are two stable operating points in this bias circuit, one of them is when all the currents are zero. A start up circuit is added to avoid this condition and start up current has been set to 10% of the bias current. The whole circuit schematic is shown in Figure 3-3. The external variable resistor was used to get a desirable bias current. The problem of using an external resistor is that the bias circuit can oscillate due to the chip-package parasitic capacitance, as shown in Figure 3-4. The loop gain of positive feedback is going to be larger than one at the high

frequency because of the large gain of common source NMOS. The problem could be solved by adding an on-chip resistor which provides one half of the total resistance value. Table 3-2 shows the variation of reference current when supply voltage has +10% ~ -10% variation from the nominal value. The ratio of fractional change of reference current to the variation of supply is 0.15 uA/V. The layout is shown in Figure 3-5.

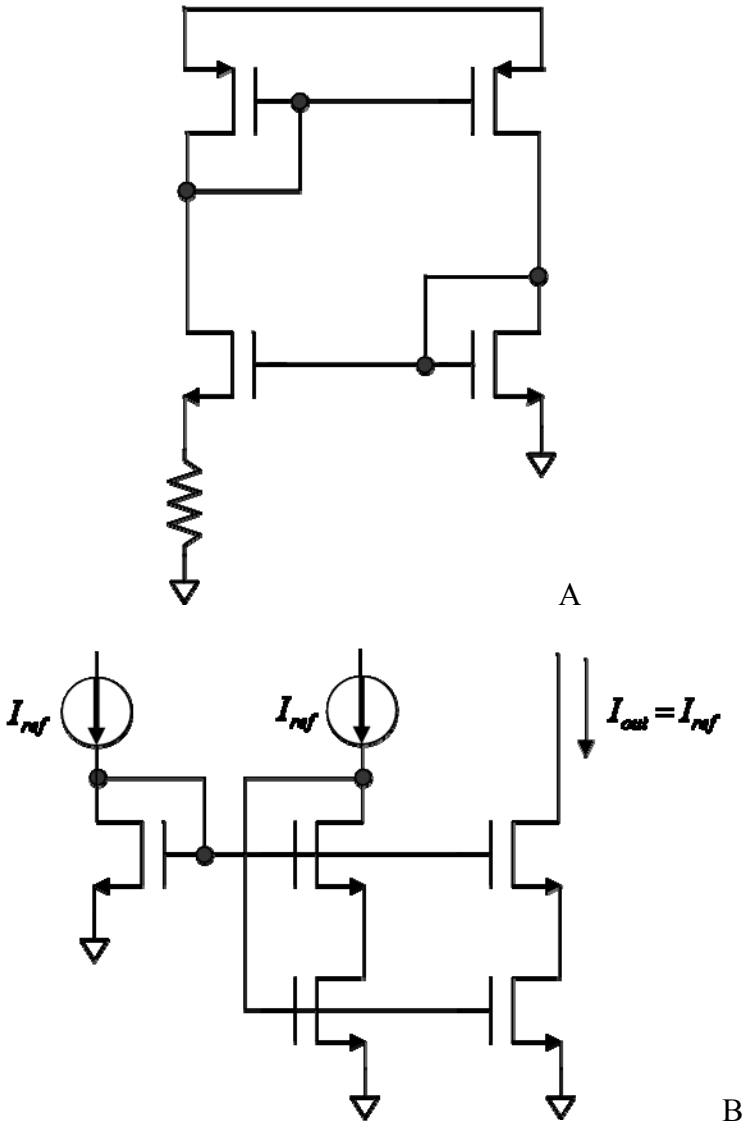


Figure 3-2. Schematic of basic building block. A) Bootstrapped self bias circuit. B) Wide swing cascode current mirror.

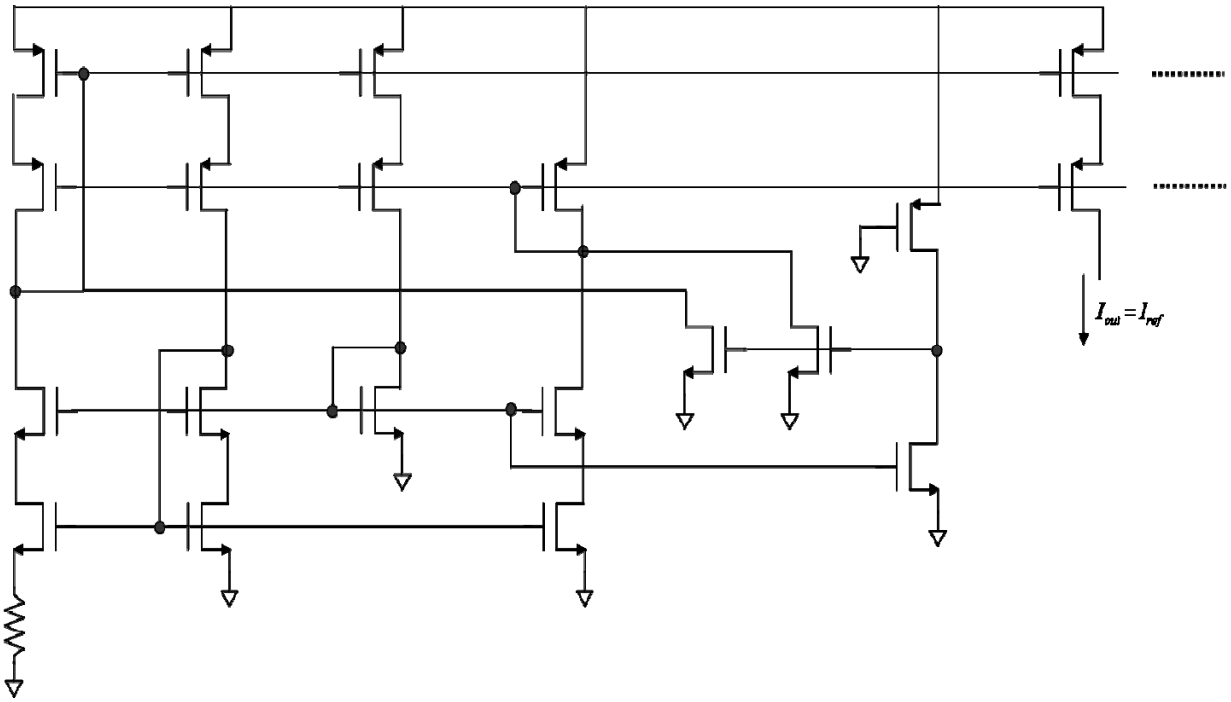


Figure 3-3. Wide swing constant-transconductance bias circuit.

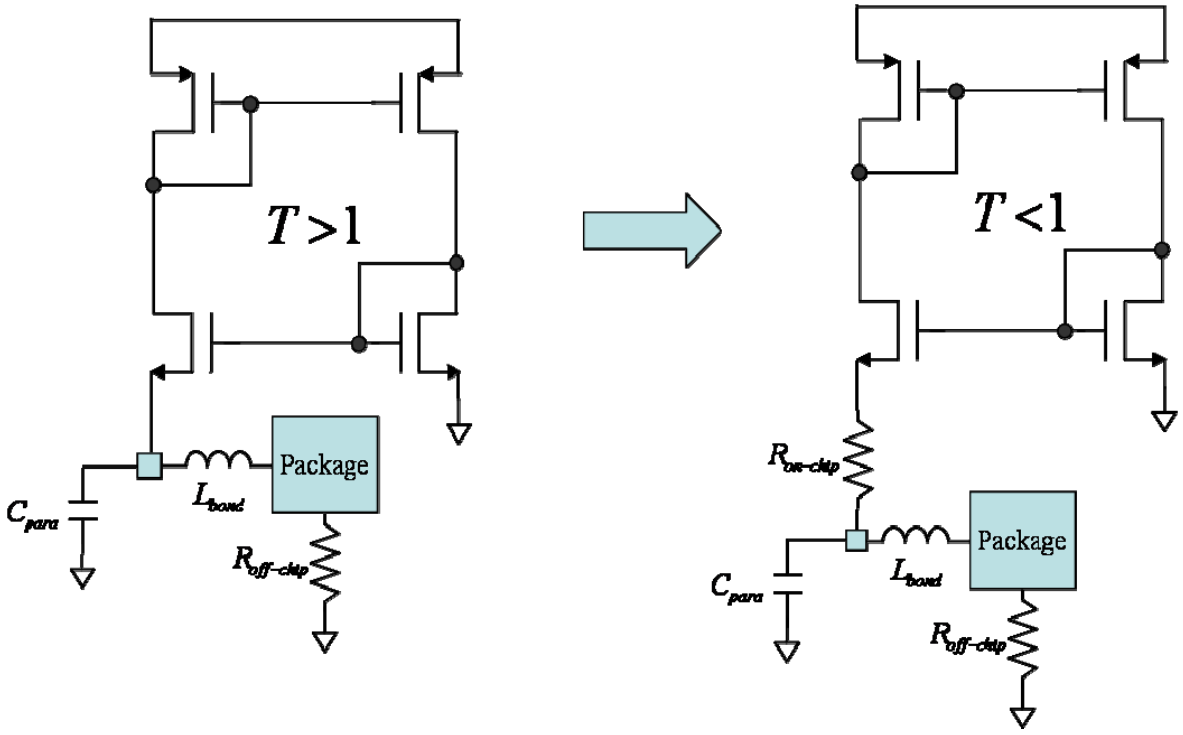


Figure 3-4. Oscillation problem due to the chip parasitic capacitance.

Table 3-1. The variation of reference current ($\Delta I_{ref} = 22.4uA$)

Supply	I_{ref}
1.32V (+10%)	633.2uA
1.2V	625uA
1.08V (-10%)	610.8uA

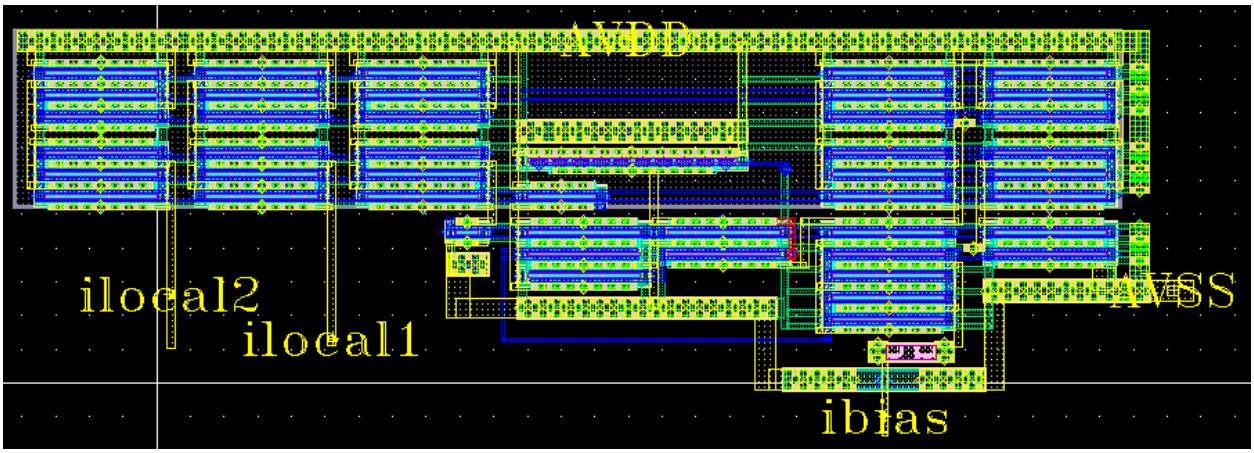


Figure 3-5. The layout of wide-swing constant transconductance bias circuit.

3.2.2 Skew Compensated Clock Delivery Network

Simultaneous switching noise can be investigated when all the I/Os fire the data across the package at the same time. When the skew between the channels caused by the clock propagation delay should be minimized, the designer uses skew compensated clock delivery [3.2]. Since the parasitic resistance and capacitance of interconnect give rise the RC delay, the clock buffer farthest from the clock receiver experiences the largest RC delay and causes the skew between the channels. When the clock buffer outputs are all shorted together via multi-drop connection, the shared line is charged or discharged through the same clock driver and thus the skew can be removed. Figure 3-6 shows the block diagram and schematic of skew compensated clock delivery. As shown in Figure 3-7(A), clock skew between the channels is less than 1ps. Figure 3-7(B) shows the clock skew when the clock buffer outputs are not shorted together.

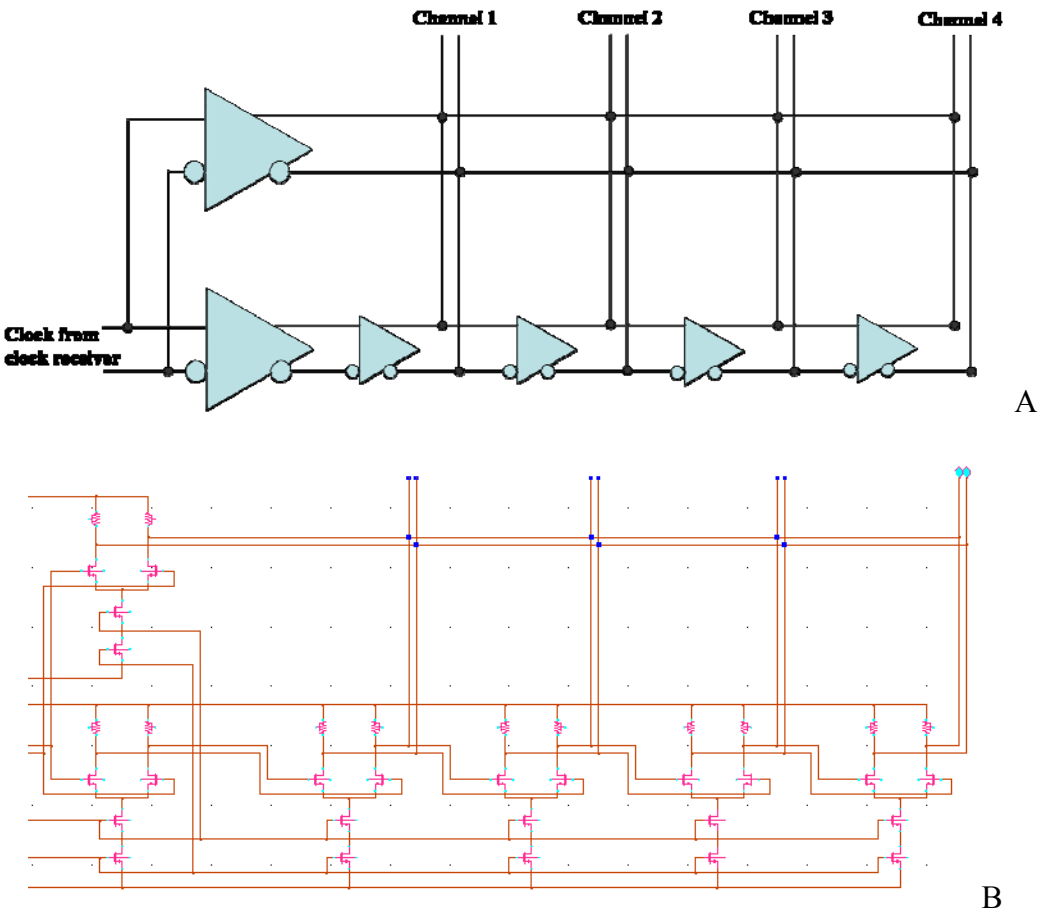
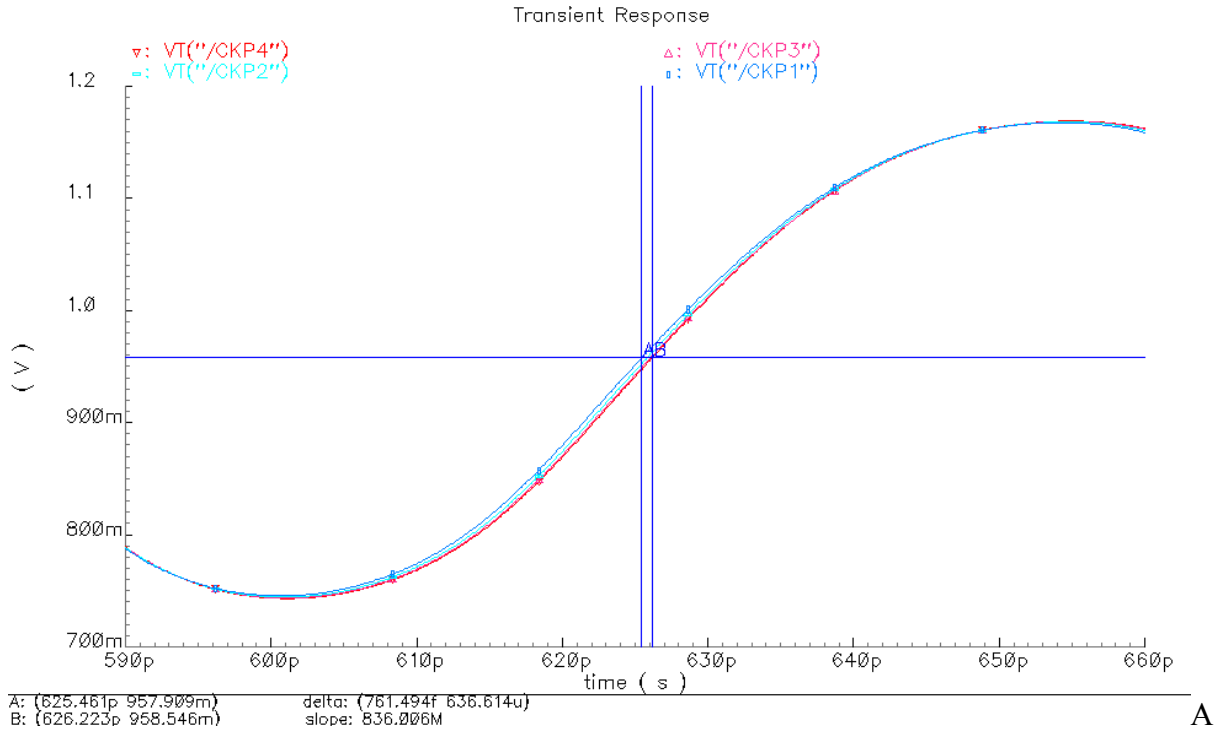
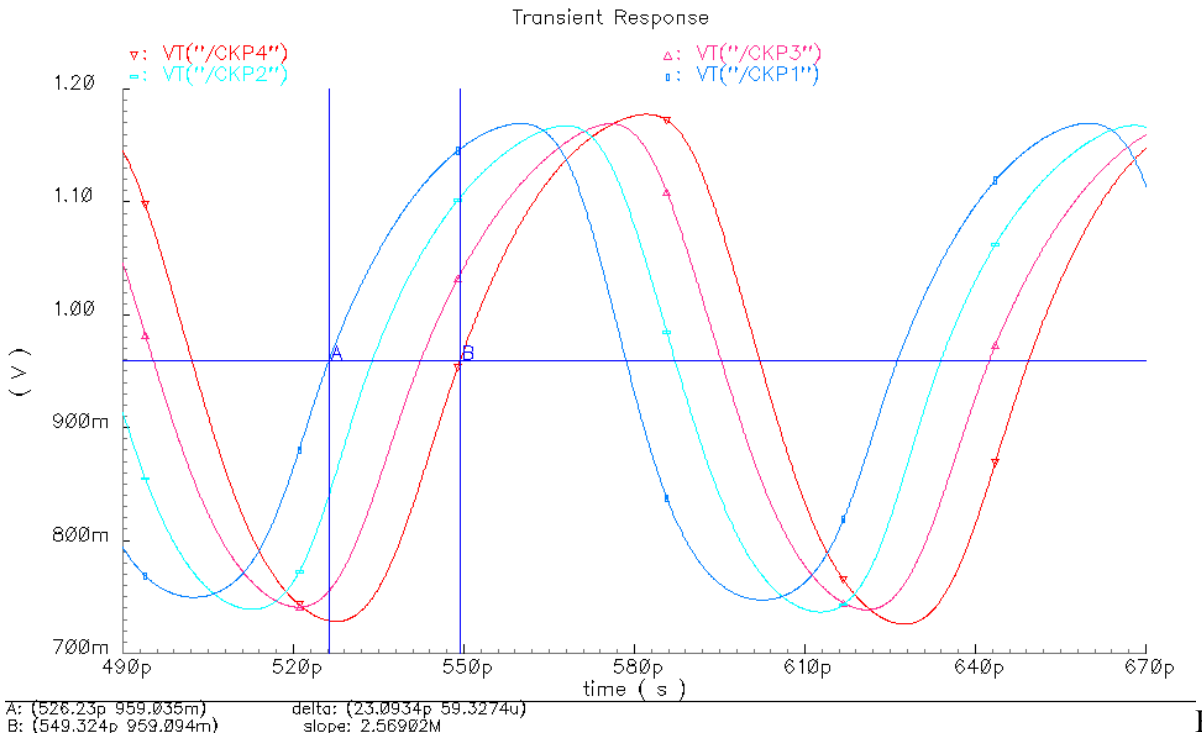


Figure 3-6. Skew compensated clock delivery network. A) Block diagram. B) Schematic.



A



B

Figure 3-7. Simulation results showing the clock skew. A) Maximum skew of skew compensated clock delivery network: $t_{skew} = 0.7\,p\,\text{sec}$. B) Maximum skew if the buffer outputs are not connected together: $t_{skew} = 23\,p\,\text{sec}$.

3.2.3 Current Mode Logic

Current mode logic (CML) is one of the most widely used logic styles for high speed digital circuits. This logic style was first implemented using bipolar transistors, but with advances in CMOS technology and the scaling-down of feature sizes, MOS implementation of CML became attractive. A CML buffer is based on a differential architecture. Figure 3-8 shows a basic differential architecture

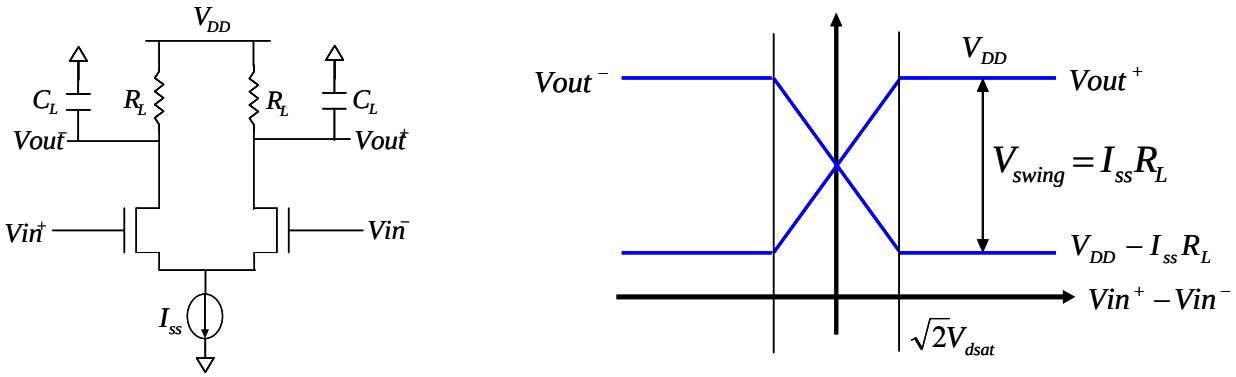


Figure 3-8. Standard CML buffer and transfer characteristic.

CML optimization has some parameter selection difficulty because the parameters $\left(W/L, R, I_{ss}\right)$ tend to be tightly coupled and do not allow independent selection. For low speed circuits, the tail current is decreased and the load resistors increased to maintain a constant swing on the outputs. Fast rise/fall times for the high speed gates are achieved by reducing load resistors and increasing the tail current.

The minimum differential input voltage $V_{\min}$ is required to fully switch the entire tail current I_{SS} to one side is given by [3.3]

$$V_{\min} = \sqrt{2}V_{dsat} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

For proper operation, the minimum gain of a CML buffer should be larger than $\sqrt{2}$. Figure 3-9 shows the DC transfer characteristic of a CML buffer designed with a 65nm CMOS process. All the sub blocks in the differential I/O test IC were designed using CML logic including the flip-flop which synchronized all the data to the system clock. Figure 3-10 shows the master-slave CML flip-flop and simulation results at10Gb/s.

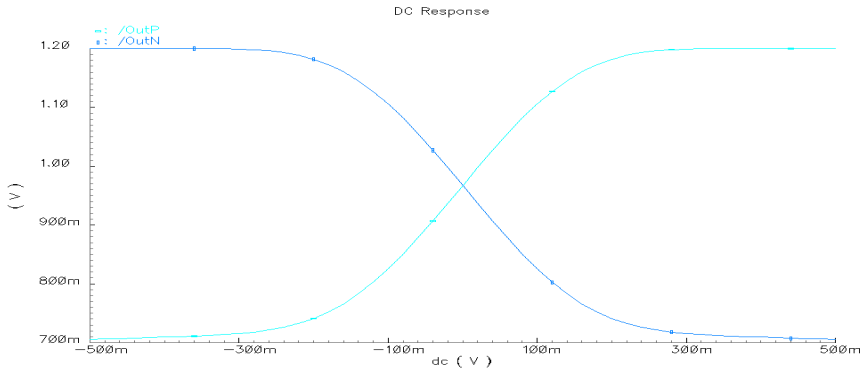


Figure 3-9. DC transfer characteristic of CML buffer designed with 65nm CMOS technology.

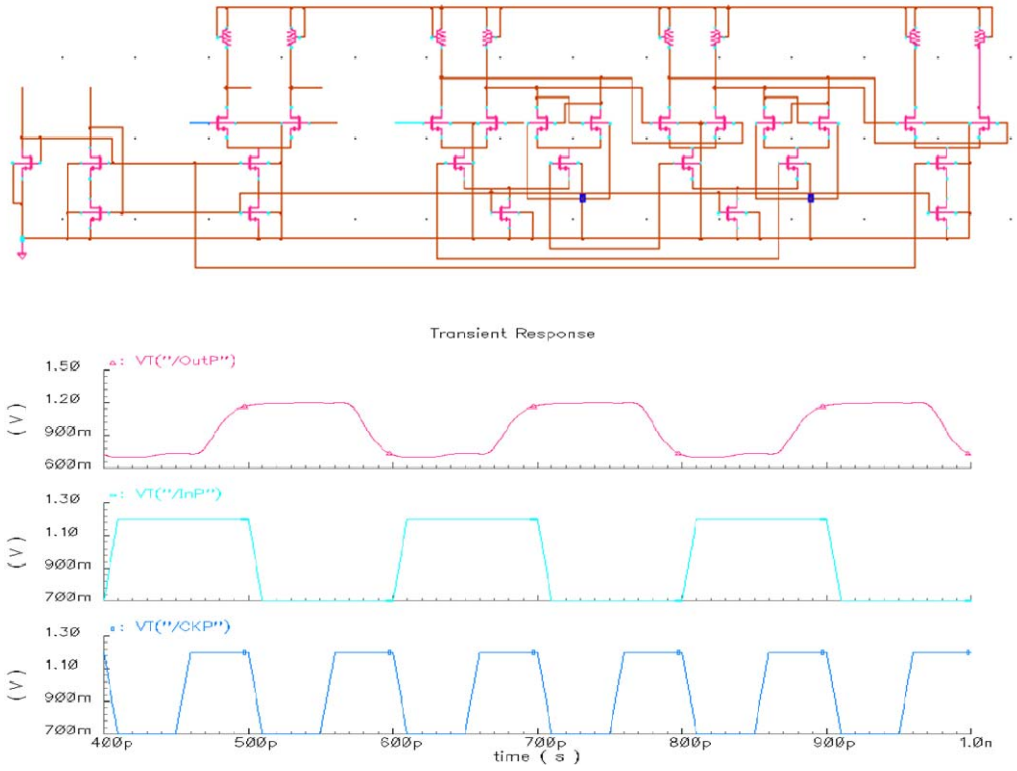


Figure 3-10. CML master-slave flip-flop and simulation results at 10Gb/s.

3.2.4 CML Clock and Data Receiver

When high speed signal travel through the PCB and package, the signal waveform can be seriously distorted because of the limited PCB and package bandwidth, which makes it necessary to use a signal restorer so that an internal flip-flop can successfully capture the data with enough timing margin. This problem can worsen in a wire-bonded package because of LC low pass filter effects due to bond-wire inductance in combination with on-chip parasitic capacitance. In the CML I/O test IC, the clock and data receiver which consist of cascaded CML buffers was designed to reconstruct the clock and data signals. In order to boost the signal swing to acceptable logical levels, a CML master-slave flip-flop was followed by an amplifying stage. Since the characteristic impedance of an on-chip transmission line is typically on the order of $50\,\Omega \sim 200\,\Omega$, the last stage of the CML buffer should be large enough to drive such a low impedance load. The number of stages and taper factor was decided by the maximum bit rate amplified. Two different simulations, which were AC small signal response and transient response, were used to get the 3dB pole frequency and the eye diagram. As the taper factor is decreased, the bandwidth is increased, but jitter and noise performance is degraded. In this design, 4 stages having taper factor of 2 were chosen to amplify the 10Gb/s data signals and Figure 3-11 shows the schematic and layout. Simulation results for AC data and an eye opening of 10Gb/s NRZ data are shown in Figure 3-12. Figure 3-13 shows the signal coming from the package and bond wire and the signal recovered from the buffer. The -3dB bandwidth of the clock buffer should be at least 10GHz in order to make the flip-flop successfully catch the 10Gb/s data since the fundamental frequency of the NRZ data is half of the clock signal. As shown in Figure 3-14, the 10GHz external clock becomes seriously degraded due to the package and bond wires. The recovered clock doesn't have a fast edge rate which results in large clock to Q delay for the flip-flop.

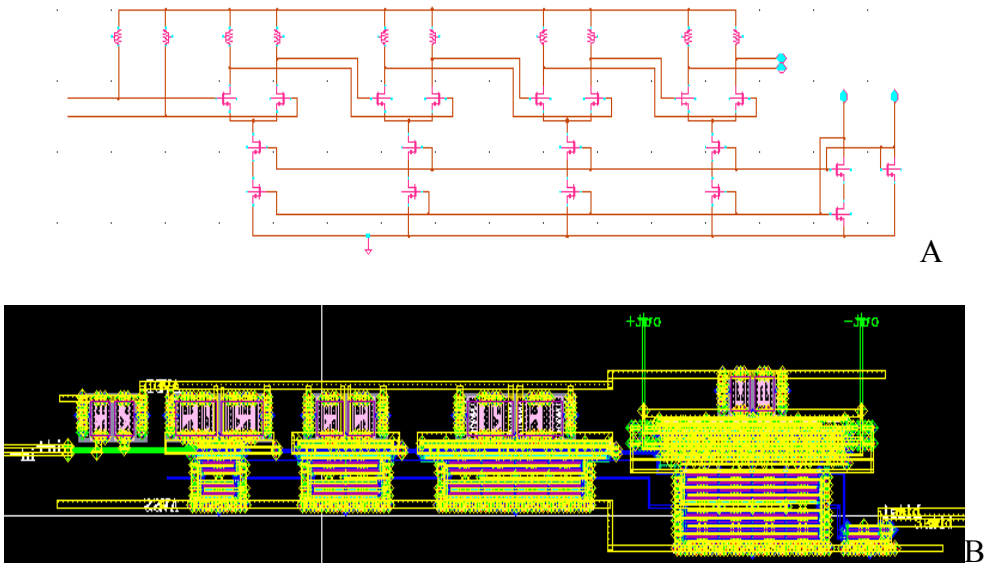


Figure 3-11. CML clock and data receiver. A) Schematic. B) Layout.

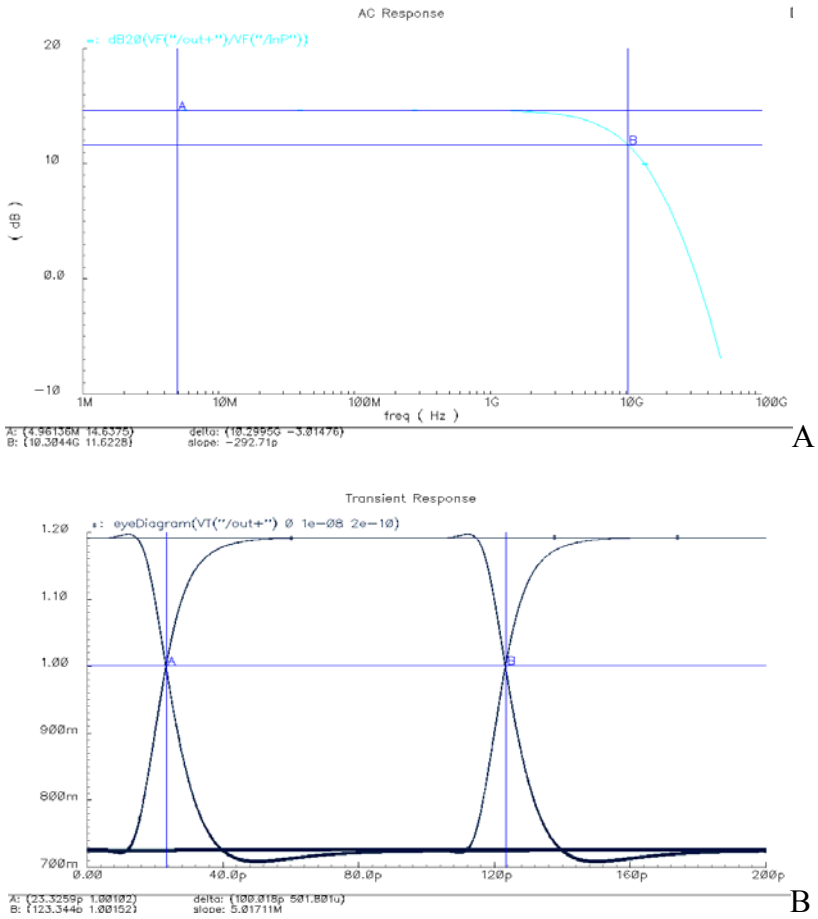


Figure 3-12. Simulation results of CML buffer. A) AC small signal response showing the -3dB bandwidth of 10GHz. B) Eye opening for 10Gb/s data.

The buffer bandwidth can be increased by reducing the taper factor, but more stages should be used to drive a large output buffer and this gives rise to poor clock jitter.

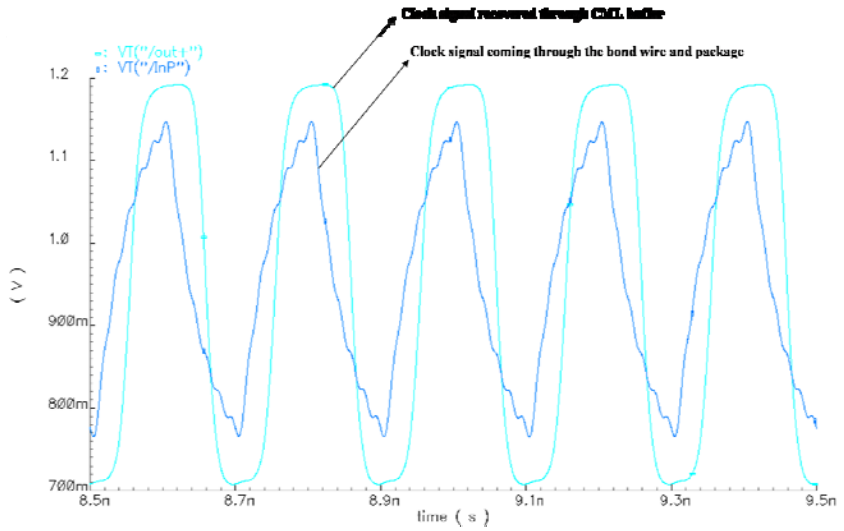


Figure 3-13. 5GHz clock signal recovered from the CML buffer.

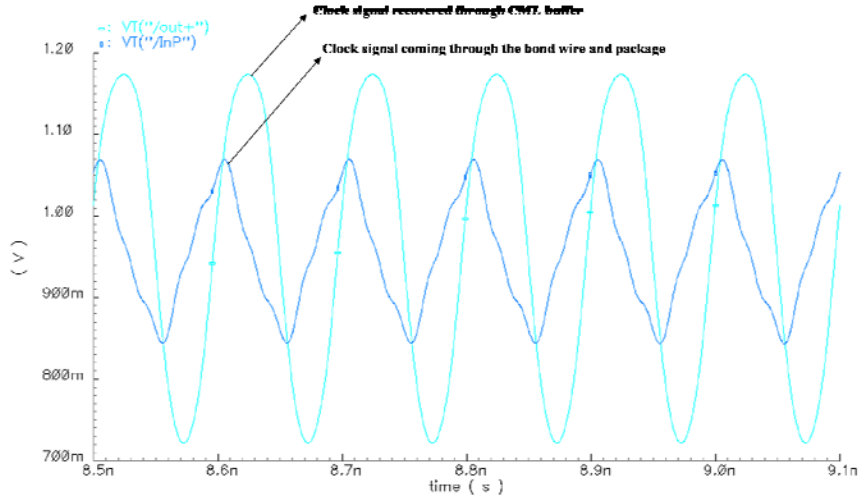


Figure 3-14. 10GHz clock signal recovered from the CML buffer.

Figure 3-15 shows a 1GHz clock and a 1Gb/s NRZ signal measured at the chip bond pads after the 5cm PCB trace and BGA package. The peak-to-peak values of the on-chip clock and data signals are 196mV and 360mV. These signals are amplified to sufficient amplitude levels through the CML buffer. As the required data rate is increased, an on-chip clean clock generator such as PLL is much preferred, especially for a wire-bonded package, in order to suppress the

fast jitter components at the input and provide an on-chip clean clock. The wide frequency tuning range PLL circuit was designed using a dual path approach and the design is explained in Appendix C.

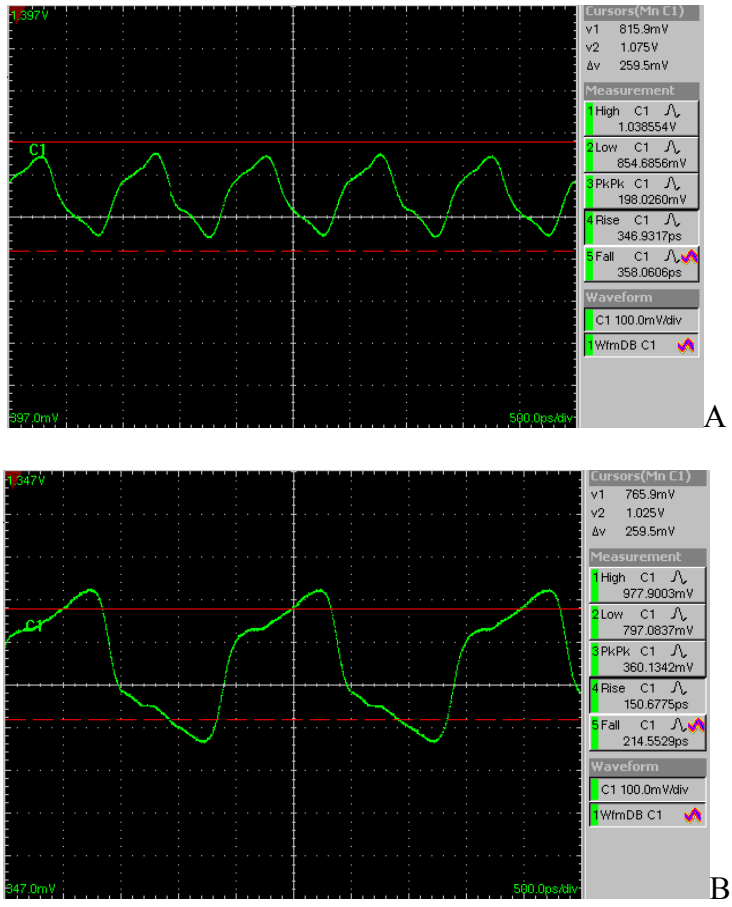


Figure 3-15. Measurement result of on-chip input signals. A) On-chip clock signal. B) On-chip data signal.

3.2.5 Differential CML I/O Driver Design

A CML I/O driver was chosen to investigate the differential I/O-Package-Board response and validate the package electrical model with differential traces. The CML I/O driver consists of cascaded CML buffer. There are several design parameters had to be determined and optimized. As shown in Figure 3-16, the output swing level was chosen according to the PCI Express standard, which is 0.5V single-ended swing. To drive an off-chip 50Ω (odd mode

impedance), the final CML buffer had to have large a tail current to get an enough voltage swing. For example, if the output swing was to be 0.5V and off-chip CML driver had to have an on-chip 50Ω termination resistor, the tail current should have been 20mA to generate 0.5V with total 25Ω resistor. The large CML buffer made it necessary to use a tapered buffer so that core logic doesn't have too much load capacitance.

Figure 3-17 (A) shows the tapered buffer. The number of stages N and the taper factor k are design parameters for the tapered CML buffer. In figure 3-16 (B), the bias current is gradually scaled up with the taper factor k and the transistor size also scaled up with the same taper factor to keep the V_{dsat} constant. The pull-up resistor is scaled down with the same taper factor to create the same voltage swing. There is a rule of thumb in optimizing the propagation delay of a CMOS tapered buffer. The rule is that 4 is the optimal taper factor when the intrinsic loading effect of inverter is considered. However, the goal of the driver design in this research is to achieve as fast edge rate as possible, so the bandwidth is a more important factor than the delay. As the taper factor is reduced, the bandwidth of each stage increases because the load capacitance of each stage decreases. However, as the number of stages increases, the power consumption increases and jitter performance is degraded. In this design, a taper factor of 2 was proven to have the maximum bandwidth through voltage-gain frequency-response simulations. Figure 3-17(C) shows the layout of 4 port CML drivers and each driver block is surrounded by the double guarding in order to suppress the switching noise due to the driver.

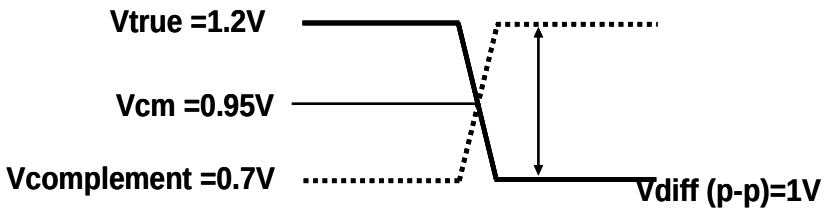


Figure 3-16. Output voltage level of CML I/O.

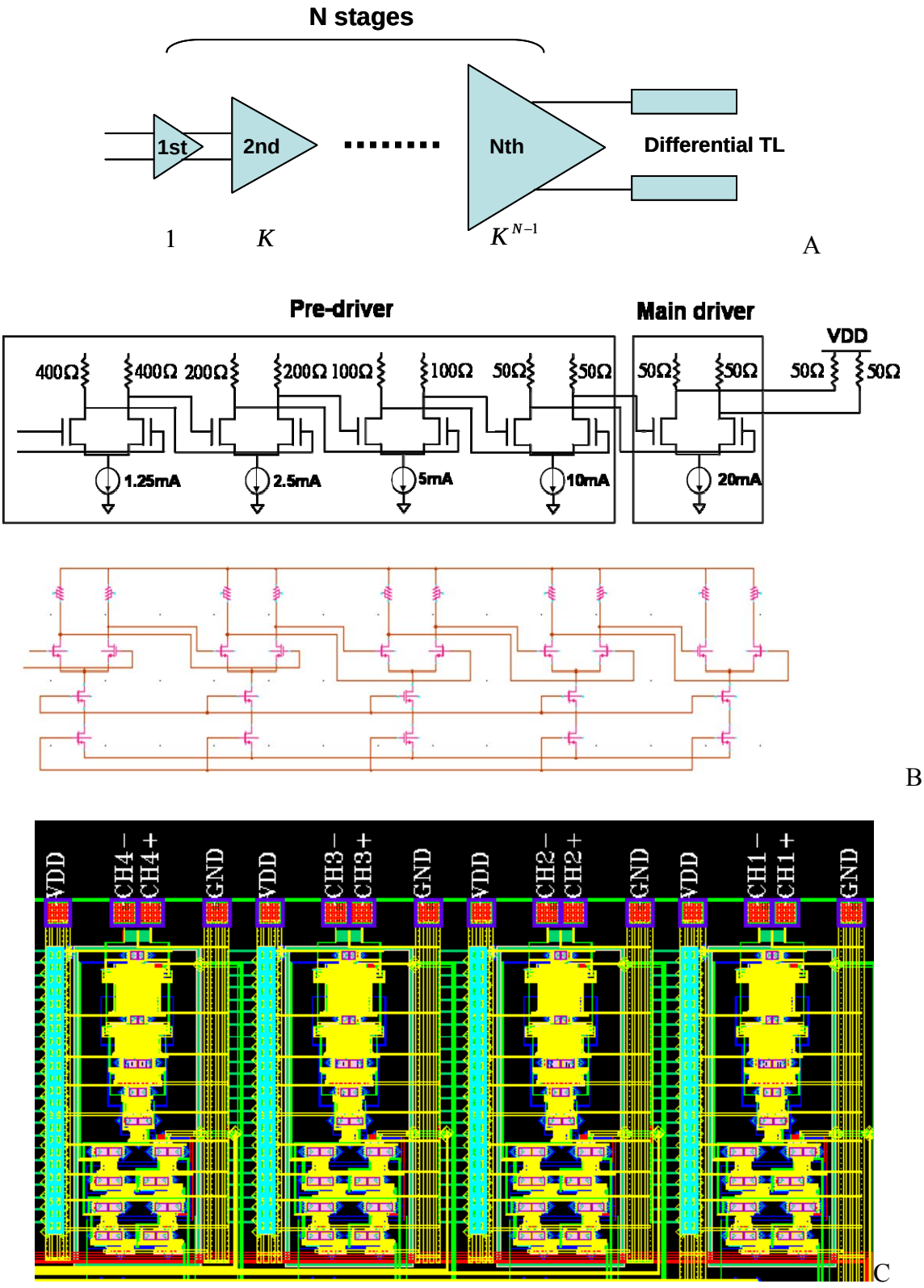


Figure 3-17. Tapered CML I/O driver. A) Tapered buffer. B) Schematic. C) Layout.

3.2.6 Band Limited Channel and Equalization

If the channel (package, PCB, etc) has a flat frequency response, it won't distort the signal it carries. However, practical channel components suffer from frequency dependent conductor loss due to the skin effect and frequency dependent dielectric loss due to the loss tangent, which causes frequency dependent attenuation of signals. In the time domain, the frequency dependent attenuation of the channel results in attenuation of the transmitted signal and spreads the energy of the transmitted signal into adjacent bits causing interference which is called ISI. Figure 3-18 shows the frequency response of a 10cm differential PCB trace modeled with the W-element in HSPICE. Simulation results show that the channel exhibits severe attenuation for signal frequency components beyond 3GHz. The effect of ISI in the time-domain is illustrated in Figure 3-19. The ideal transmitted signal having 50ps edge is the transmitted pulse with a 100ps bit time. After this signal go through a 10cm PCB trace, the peak normalized amplitude of pulse is 0.375, which is a 62.5% reduction in amplitude. In addition, the falling edge of this pulse spans 3.178 bit times, which causes serious ISI in the next transmitted data.

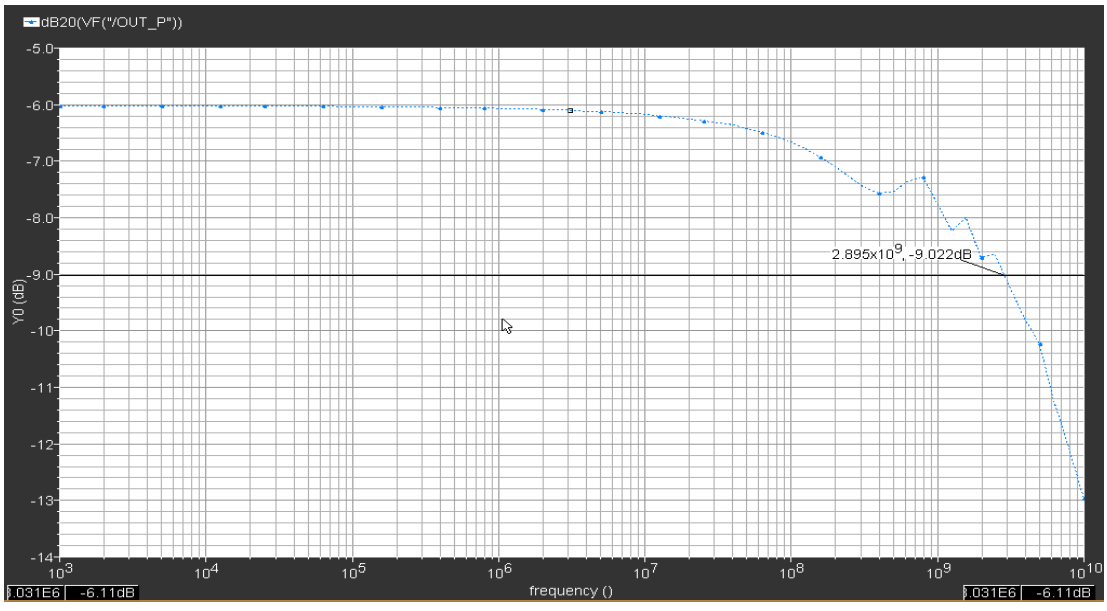


Figure 3-18. Channel frequency response of 10cm differential PCB trace.

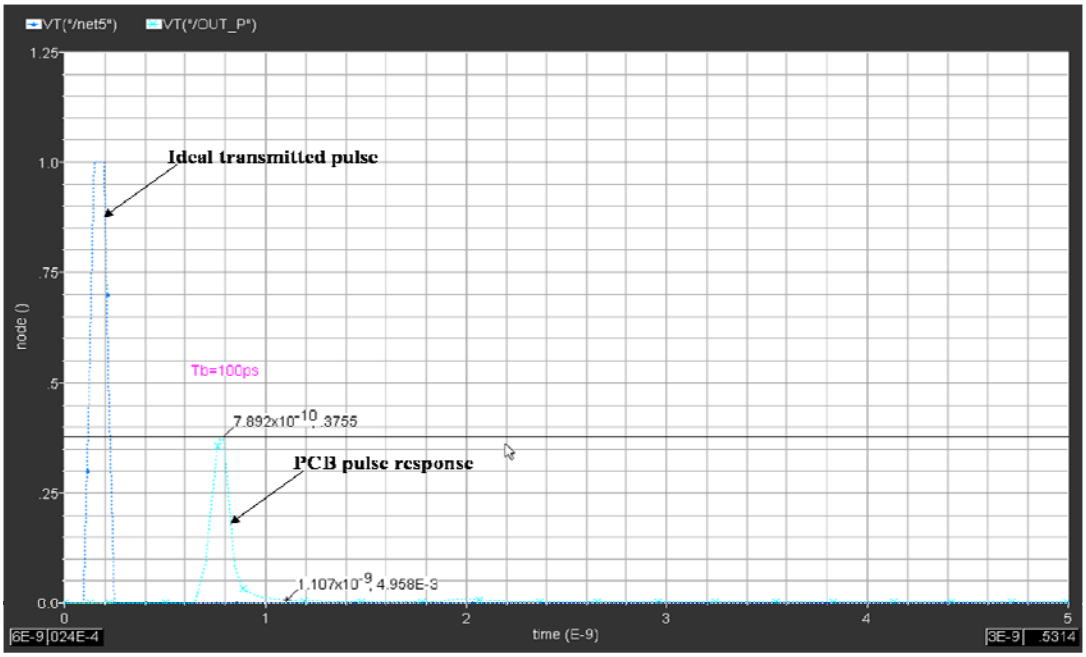


Figure 3-19. Pulse response of 10cm differential PCB trace.

In general, there are two methods to cancel the effect of ISI. First, a pre/de-emphasis driver can be implemented in the transmitter to pre-distort the transmitted signal as illustrated by figure 3-20. This is called "Linear equalization" and transmitter sends data through the FIR filter having a predetermined filter coefficient. Second, a post equalizer can be implemented in the receiver to compensate for the channel loss before the receiver attempts to recover the original data. This is called "Decision feedback equalization" and the filter coefficient can be adjusted through the feedback of the IIR filter in order to cancel out the spanned portion. Figure 3-21 shows the block diagram of decision feedback equalization.

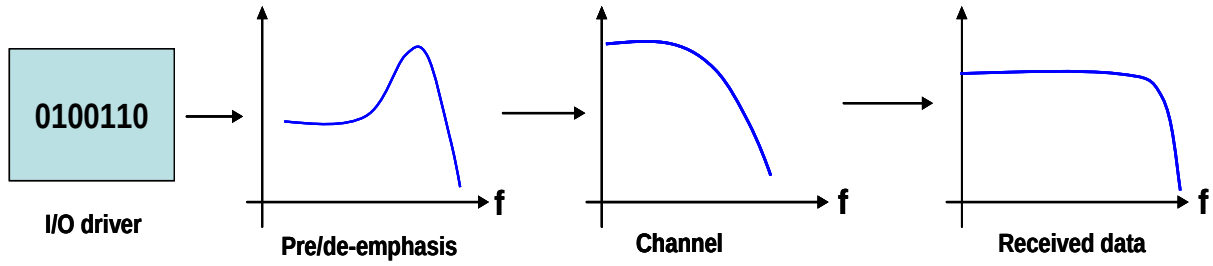


Figure 3-20. The idea behind pre/de-emphasis equalization.

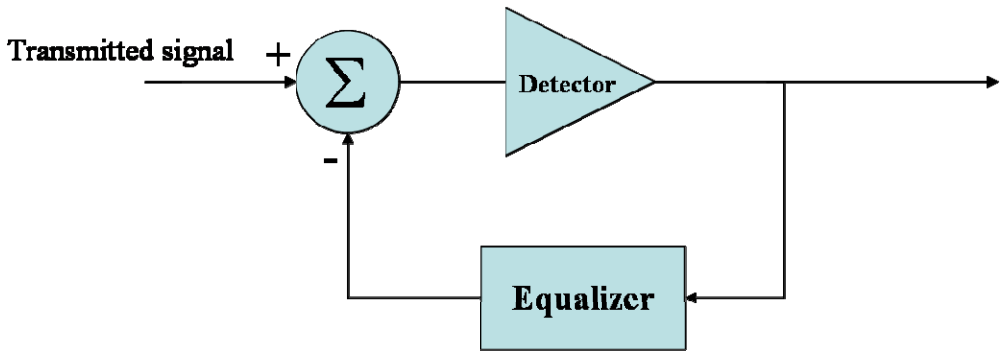
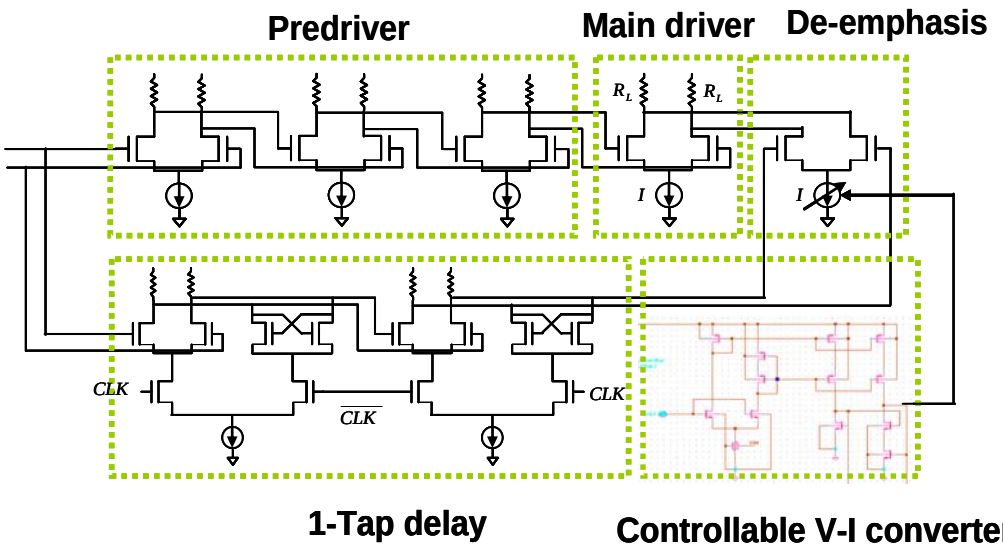
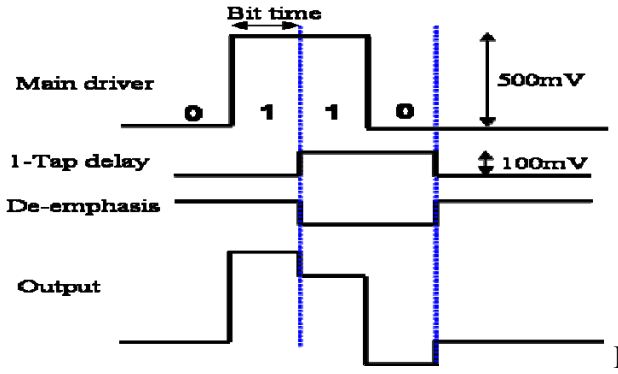


Figure 3-21. Block diagram of decision feedback equalizer.

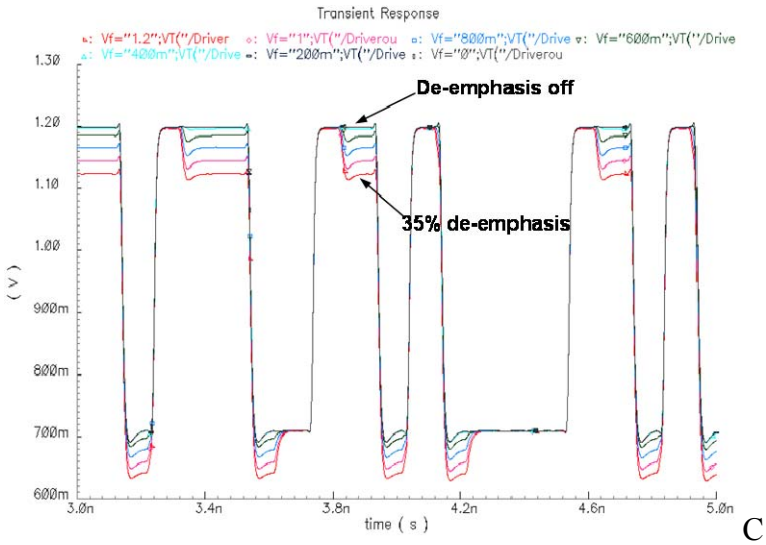
In this research, a 1-tap de-emphasis equalizer was chosen for the CML driver and the controllable V-I converter [3.4] was designed so that a de-emphasis level can be controlled from 0% (when Vctrl=0) up to 35%. De-emphasis levels can be defined as the ratio of maximum signal amplitude to the signal amplitude when de-emphasis level is changed. Figure 3-22 shows the CML driver with 1-tap equalizer circuit and the simulation results. The controllable V-I converter seamlessly changes the equalization level from 0 to 35%. Figure 3-23 shows the de-emphasis V-I converter and control voltage vs. the de-emphasis current.



A



B



C

Figure 3-22. CML driver with 1 tap de-emphasis circuit. A) Schematic. B) Equalization signal. C) Simulation result.

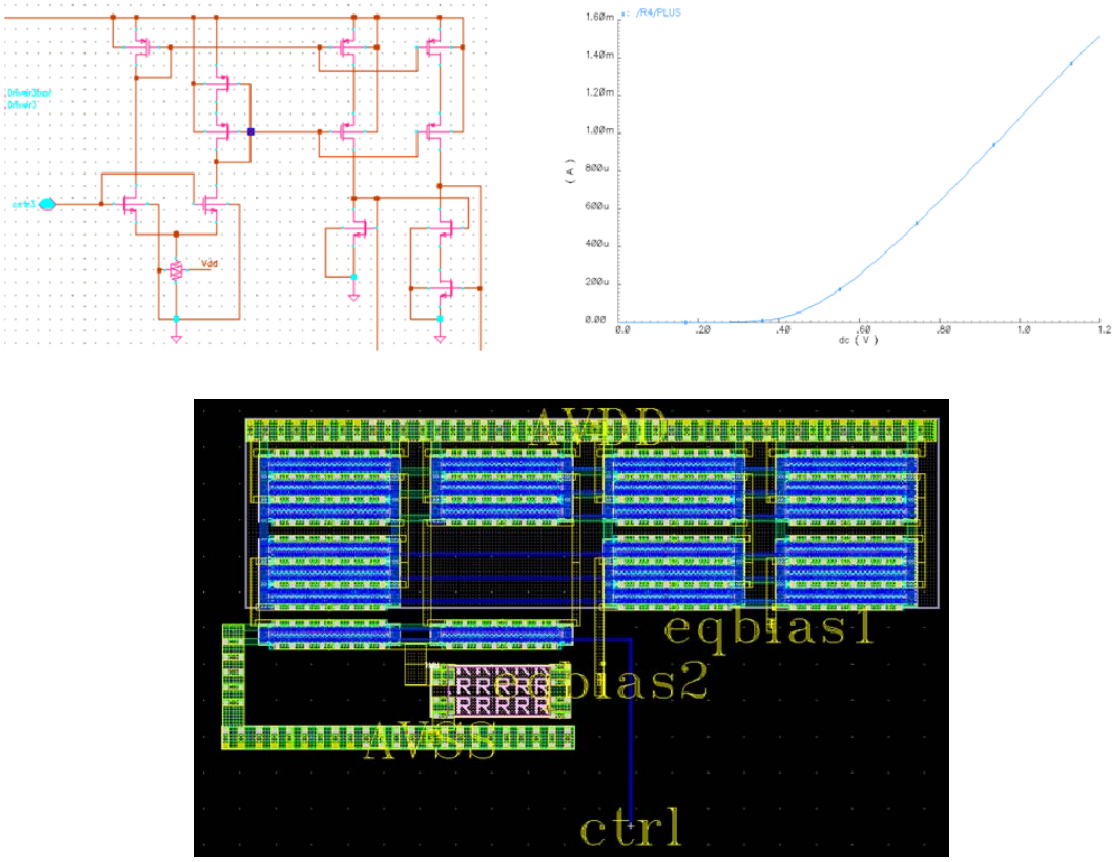


Figure 3-23. V-I converter. A) Schematic. B) Control voltage vs. de-emphasis current. C) Layout.

3.2.7 Simulation Results

A 4 port CML differential I/O test IC has been simulated with an Amkor lead frame package. This type of package was used for a 5GHz wireless LAN Power amplifier and has a down bond for the package ground to reduce the inductance. Figure 3-24 shows I/O pad arrangement and the chip layout. Power and ground pads are placed close together in order to reduce the bond wire inductance. This also helps to minimize the loop inductance associated with loop current path. The rise time of the output signal from stand alone CML I/O is 15ps which corresponds to a knee frequency of 23 GHz. The simulation was performed with 10Gb/s data and Figure 3-25 shows the simulation results of about 10Gb/s switching output and package

ground noise when four CML I/O drivers switch simultaneously. The 10Gb/s PRBS data was used to generate the eye diagram.

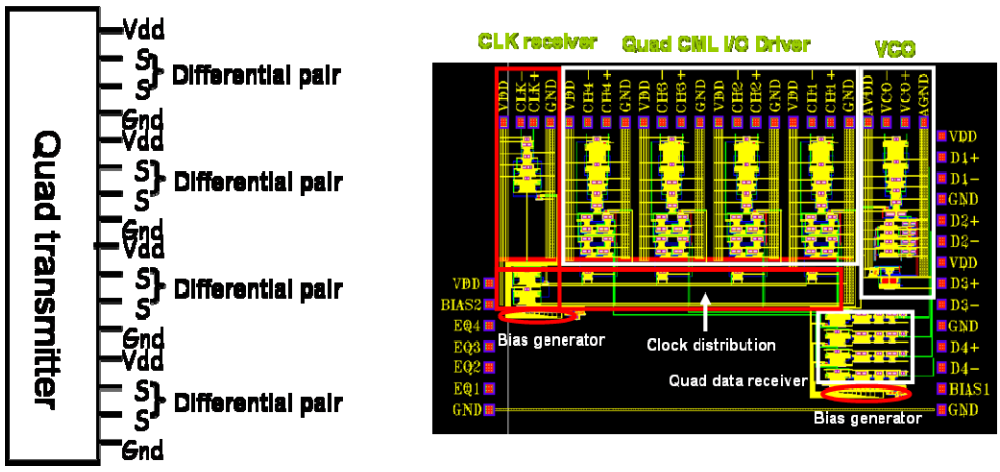


Figure 3-24. I/O pad arrangement and chip layout.

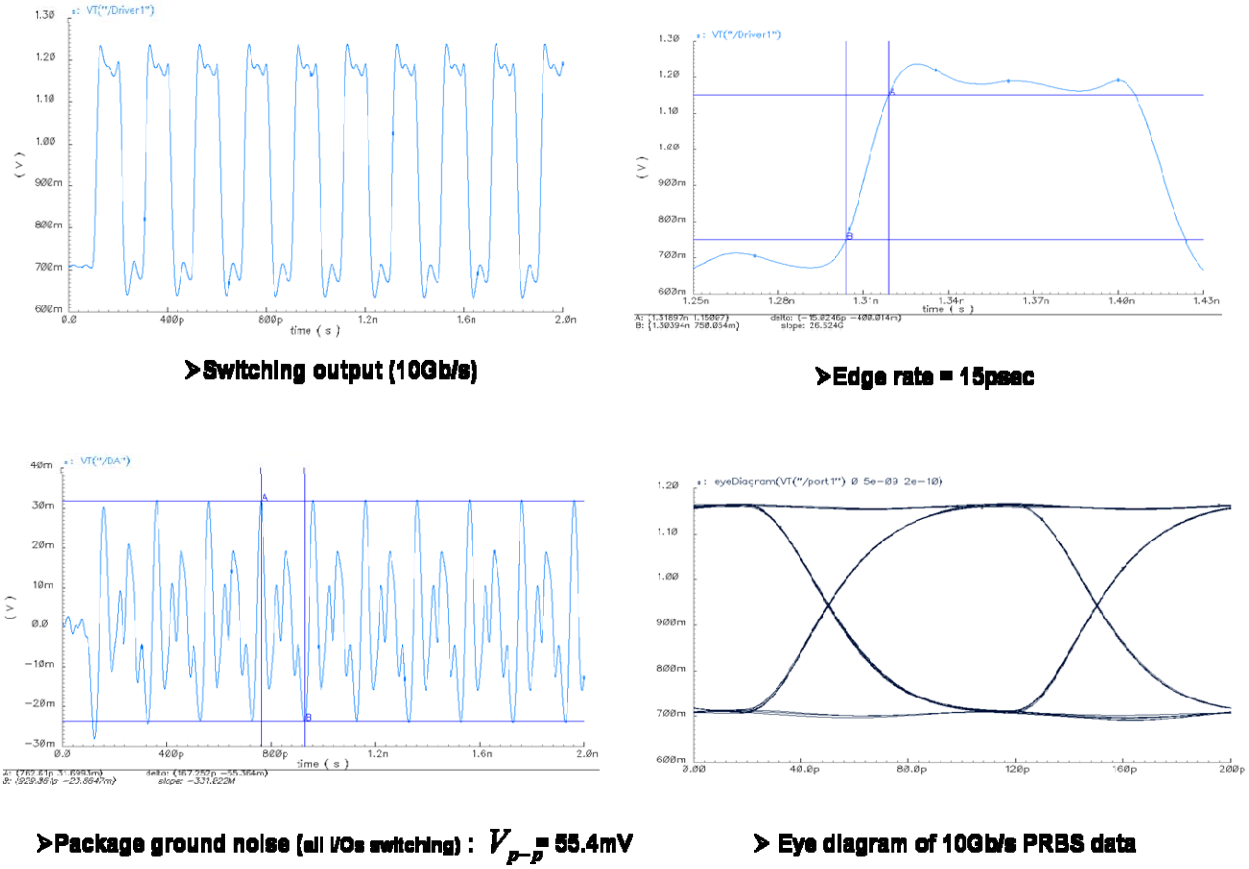


Figure 3-25. Simulation results of 4 port CML differential I/O test IC.

In summary, this chapter presented the circuit designs of the sub-blocks of a 4 port CML I/O test IC. Simulation results at 10 Gb/s were presented to show the chip performance and functionality. This chip is used to characterize signal integrity for a differential I/O test IC-package system and validate the corresponding package electrical model. The next chapter presents another important I/O test IC, a single-ended I/O test IC that can be used for single-ended I/O test IC chip-package systems.

CHAPTER 4
SINGLE-ENDED I/O TEST IC DESIGN

4.1 Introduction

Despite of its slow speed, single-ended I/O is still widely used for various bus applications because of its simplicity. In this chapter, two versions of single-ended I/O test ICs are presented, GTL (Gunning Transceiver Logic) I/O and push-pull I/O. These chips are used to look at the signal integrity for single-ended I/O chip-package and validate the package electrical model having single-ended inner traces.

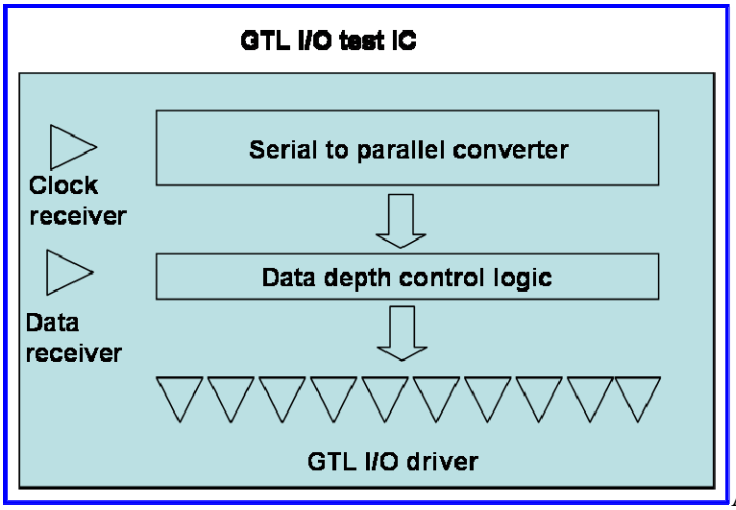


Figure 4-1. Overall block diagram of I/O test IC. A) GTL I/O test IC. B) Push-pull I/O test IC.

GTL I/O test chip includes 10 ports GTL I/O drivers, a GTL clock and data receiver, data depth control logic and 80 bits serial-to-parallel converter. A push-pull I/O test chip was composed of 10 ports push-pull I/O drivers, 40 bits of serial-to-parallel converter, a 4:1 multiplexer and a retimer block. Both chips were designed such that they fire different data patterns having different data depth across multiple I/Os. Experiments with different frequencies, different data patterns, different data depths and capturing the response of package have been performed. Figure 4-1 shows the overall block diagram of the GTL I/O and push-pull I/O test IC. The GTL I/O test IC was designed and fabricated using a Texas Instruments 65nm digital CMOS process. The push-pull I/O test IC was designed and fabricated using IBM7WL 0.18um BiCMOS process. Simulations were performed with Amkor RF package in order to show the performance and functionality.

4.2 GTL I/O Test IC

GTL I/O is widely used for personal computer applications, especially the front-side bus and the AGP, which is the interface between the processor (CPU or GPU) and the processor chipset [2.7]. GTL drivers generate faster edge rate signals than push-pull drivers since they don't have slow PMOS devices. They can be used to enabling validate single-ended package electrical models at higher frequencies. The GTL I/O test IC includes 10 ports of GTL drivers, GTL clock and data receivers and serial to parallel converter to fire different data patterns having different data depths across 10 GTL I/O drivers.

4.2.1 Serial-to-Parallel Converter having 80 Bit Serial IN – 10 Bit Parallel OUT

In order to load the serial data from external test equipment, a 80 bit serial IN buffer was designed that outputs 10 bit at a time and repeats the sequence indefinitely. The architecture and diagram of the basic cell are shown in Figure 4-2. The basic cell consists of a flip-flop and a multiplexer that selects (sel) parallel IN (pin) data when a select signal is1 and serial IN (sin)

data when select signal 0. When the select signal is 1, the register goes to the data load mode and starts loading the serial data. After loading the data, the select signal goes to 0 and the register starts firing the parallel data indefinitely with the period decided by the number of basic cells, which in this case is 8 bits. Therefore, a maximum data depth of 8 bits can be used to investigate the data dependent jitter. The power PC flip-flop, which was used in the IBM PowerPC 603 [4.1], was chosen as the design for the basic cell. As shown in Figure 4-3 (A), the structure is similar to the transmission gate MUX based master-slave flip-flop, but the transmission gate in the cross coupled inverter is changed to clocked inverter. Figure 4-3 (B) shows that the clock-to-output delay is 85 psec. The overall layout for serial to parallel converter is shown in Figure 4-3 (C).

4.2.2 Data Depth Control

Inaccurate package electrical models affect data dependent jitter simulations and this phenomenon can be investigated with a random data pattern as explained in Chapter 2. An 8bit periodic bit pattern allows the noise to settle partially prior to the next bit and resonances to be sufficiently exited. However, the package power and ground noise due to the simultaneous switching drivers are going to be investigated with a single bit transition more efficiently because it allows long term settling. The flip-flop having a clocked AND gate was used to control the data depth and maximum long term settling time. The package power and ground noise can be investigated with a data pattern of 01111111. Depth control of the signal comes from the external stimulus system and Figure 4-4 shows the schematic and layout of data depth controller.

4.2.3 GTL Receiver and Schmitt Trigger

Instead of using an inverter for clock and data input, a static differential receiver was designed since it is insensitive to power supply variation in contrast to the inverter, whose threshold voltage varies directly with variations in either power supply [2.3]. The Chappell amplifier [4.2] is widely used as a GTL receiver because of its self biasing property. Figure 4-5

shows the schematic and layout. The gate node of the tail current source is connected to the gate of PMOS current mirror with negative feedback as shown in Figure 4-5 (A). The feedback drives the bias voltage to the proper operating point. The charging and discharging time is accelerated through the positive feedback shown in Figure 4-5 (A).

The GTL test IC has control signals that come from the external stimulus system and experience signal distortion while they go through the PCB and package. In order to suppress the noise and restore the signal edge, a Schmitt trigger circuit was used. A simple inverter has a regeneration property and can recover the signal, but it doesn't have noise suppression capability. The hysteresis characteristic of a Schmitt trigger generates upper and lower switching thresholds according to the data transition and suppresses the glitch or ringing in a signal. There is another nice property in Schmitt trigger which is related to the positive feedback. If the signal has a very slow slope, the Schmitt trigger rectifies the slope and makes the transition very fast. Figure 4-6 shows the schematic, layout and transient response of a Schmitt trigger. The upper switching threshold V_M^+ is decided by the sizing of M1, M2 and is given by

$$\frac{K_1}{K_3} = \frac{W_1 L_3}{L_1 W_3} = \left[\frac{V_{\sup ply} - V_M^+}{V_M^+ - V_{thn}} \right]^2 \tag{4-1}$$

The lower switching threshold is decided by the sizing of M5, M6 and is given by

$$\frac{K_5}{K_6} = \frac{W_5 L_6}{L_5 W_6} = \left[\frac{V_M^-}{V_{\sup ply} - V_M^- - V_{thp}} \right]^2 \tag{4-2}$$

Simulation results show that the upper switching threshold is 960mV and lower switching threshold is 212mV. The noise between these two level is going to be suppressed.

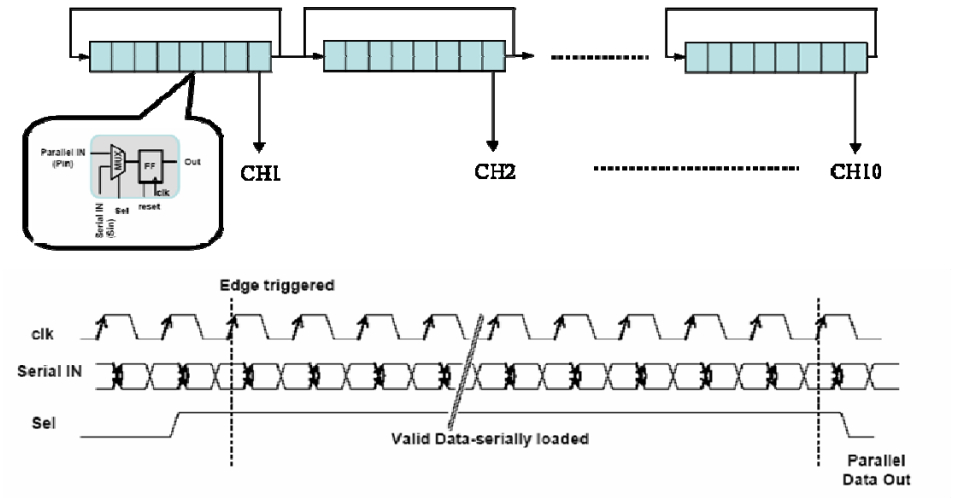


Figure 4-2. 80 bit serial IN – 10 bit parallel OUT.

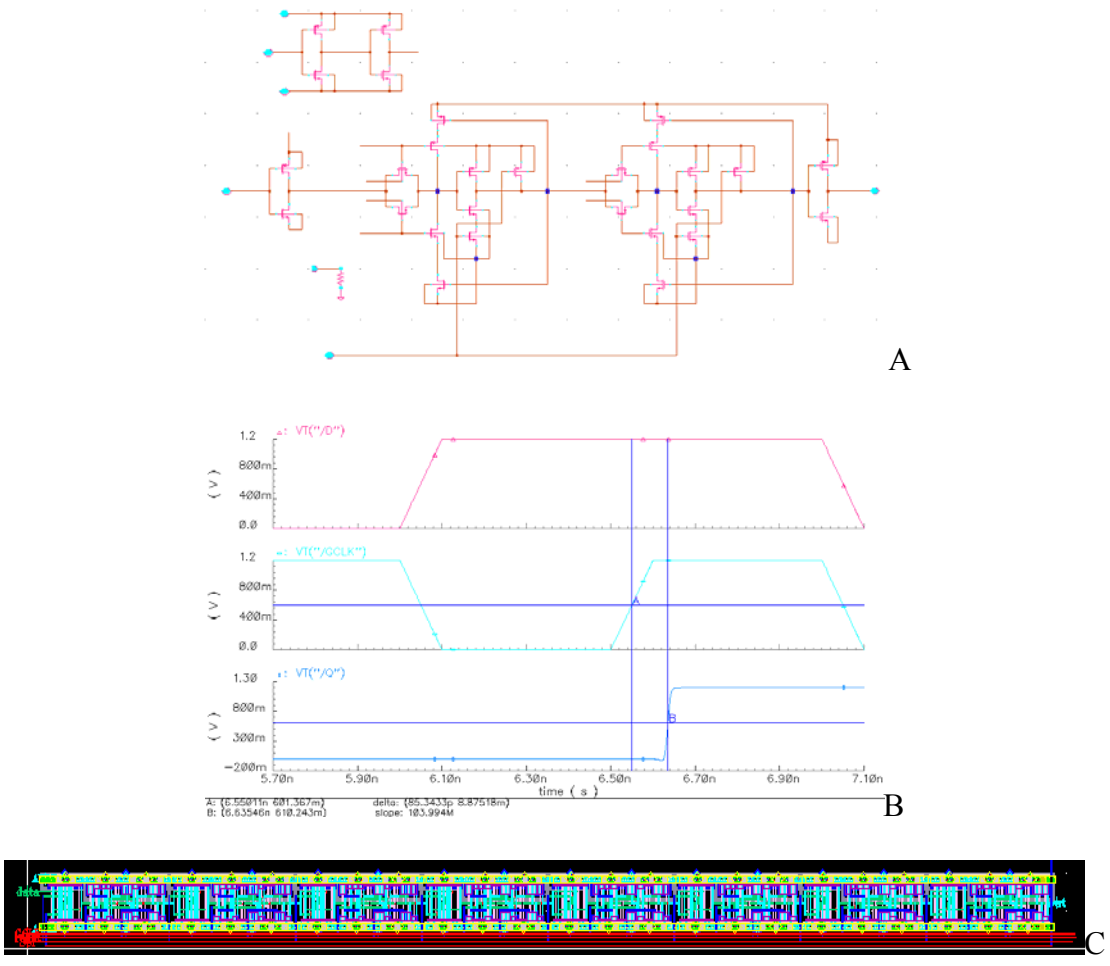
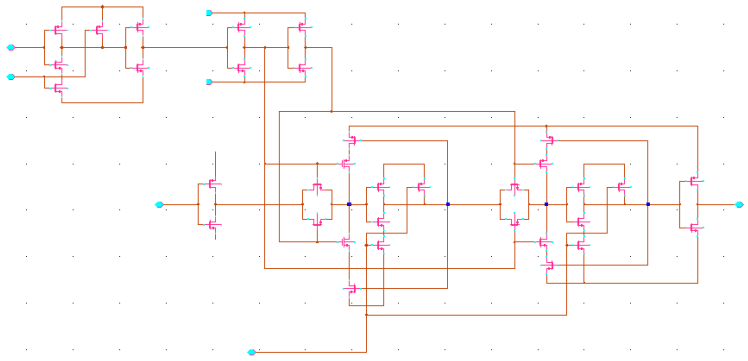
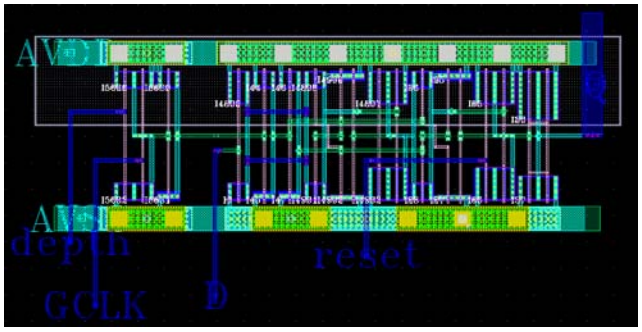


Figure 4-3. PowerPC flip-flop. A) Schematic. B) Clock-to-output delay = 85psec. C) Layout.

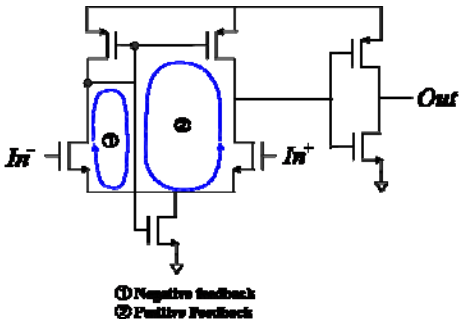


A

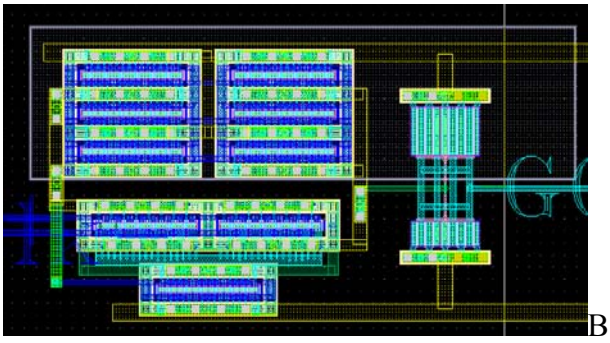


B

Figure 4-4. Data depth controller. A) Schematic. B) Layout.

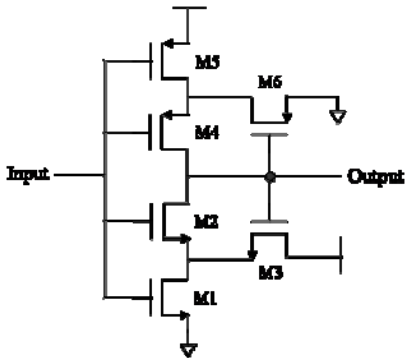


A

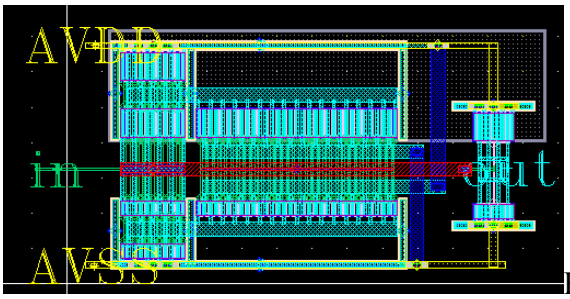


B

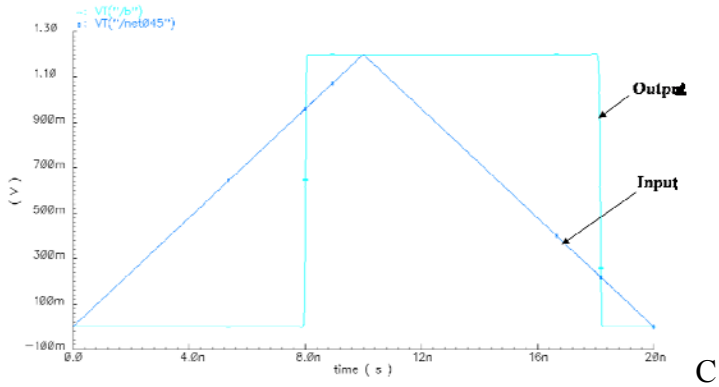
Figure 4-5. Chappell amplifier. A) Schematic. B) Layout.



A



B



C

Figure 4-6. Schmitt trigger. A) Schematic. B) Layout. C) The input and output of the Schmitt trigger.

4.2.4 GTL I/O Driver

GTL driver is simply an open drain circuit. It has an NMOS shunted to ground, and the other end of the transmission line is pulled up to the termination voltage. Turning the NMOS on and shunting the net to the ground generates a low signal. The NMOS typically has a very low equivalent resistance. Turning the NMOS device off and letting the termination resistor pull the net high generates a high transition.

Figure 4-7 (A) shows a 10 port GTL driver which has an off chip 50Ω load. The layout is shown in Figure 4-7 (B). The double guard ring which consists of p-sub and n+ well was used to absorb the switching noise generated from the driver.

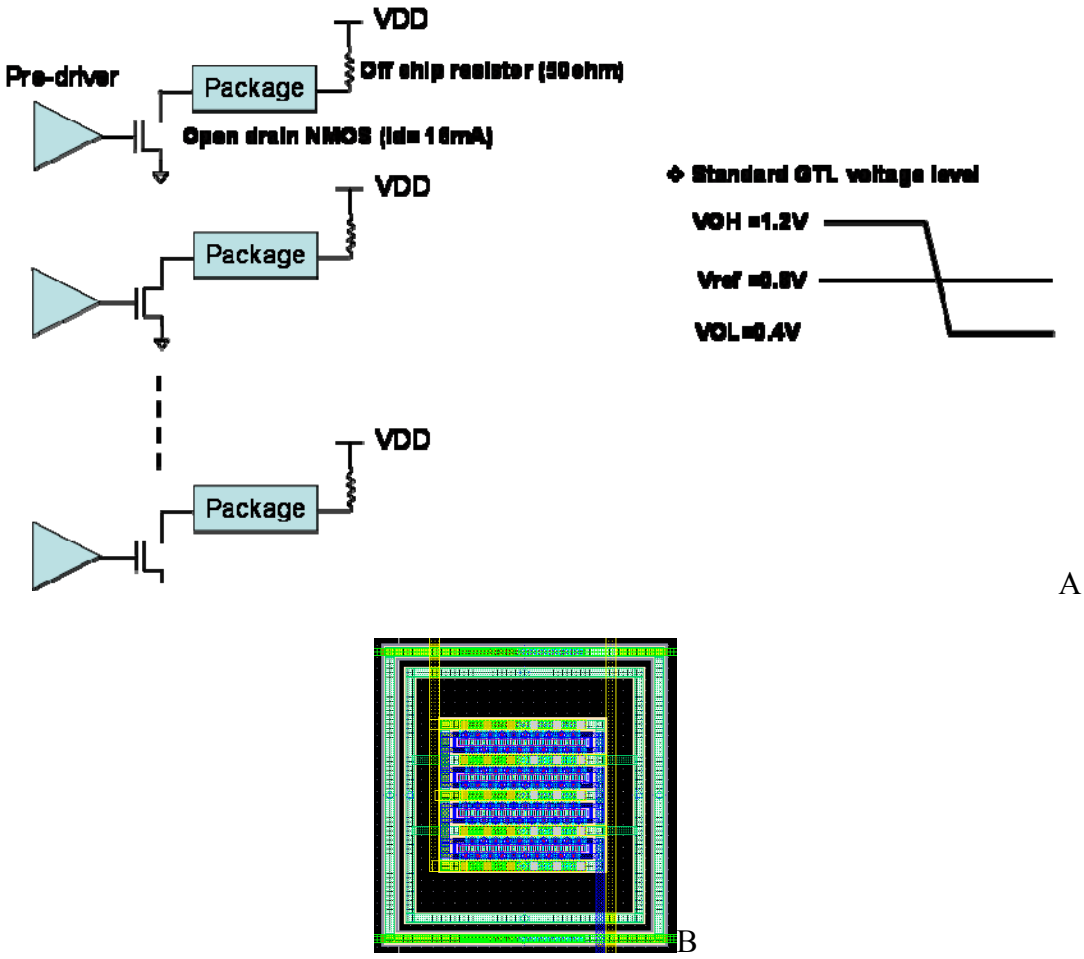


Figure 4-7. GTL I/O driver. A) 10 parallel GTL I/O driver. B) Layout.

4.2.5 Simulation Results

A 10 port GTL I/O driver was simulated with an Amkor wire bond RF package. Figure 4-8 shows I/O pad arrangement and chip layout. The signal and ground pin ratio was chosen to be 2:1 and two I/O pads are placed closely in order to investigate the crosstalk. The rise time of output signal at chip bond pad is 58 psec which corresponds to a knee frequency of 6 GHz. The simulation was performed with 1Gb/s data and Figure 4-9 shows the simulation results of 1Gb/s

switching output and package ground noise when ten GTL I/O drivers switch simultaneously. 1Gb/s PRBS data was used to generate the eye diagram.

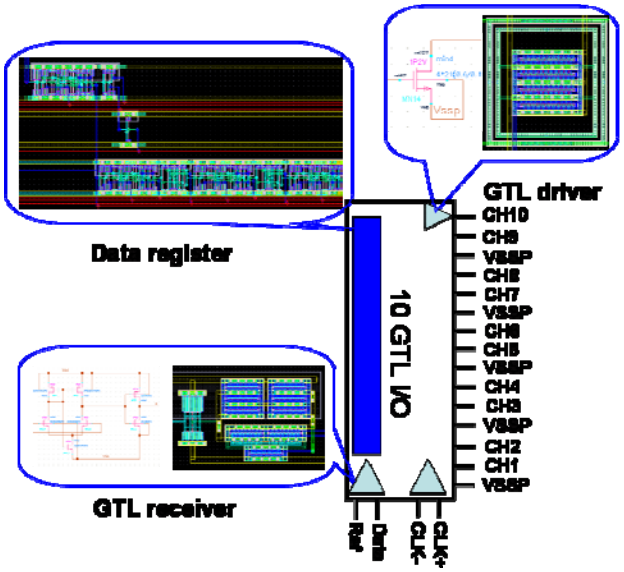


Figure 4-8. I/O pad arrangement and chip layout.

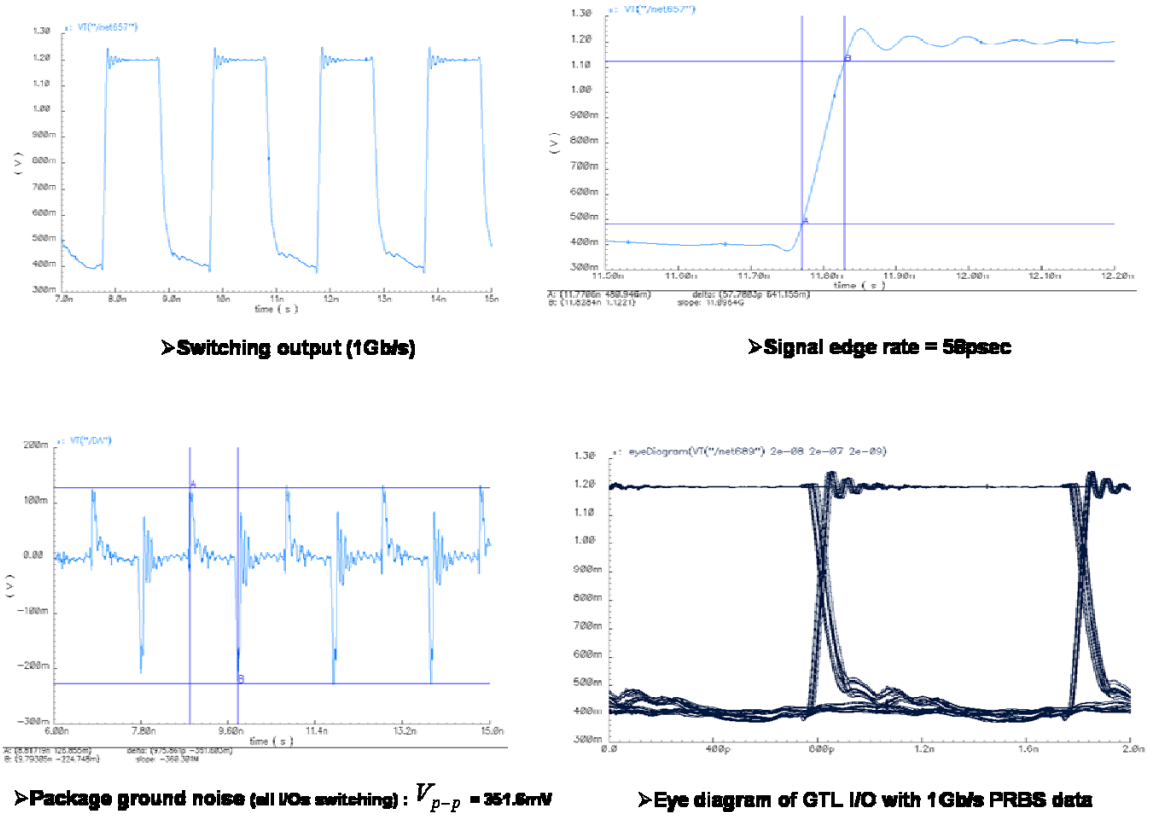


Figure 4-9. Simulation results of GTL I/O test IC.

4.3 Push-Pull I/O Test IC

In contrast to the GTL I/O driver, a push-pull I/O driver draws pull up and pull down current from the package power and ground ring allowing validation of the electrical model for the package power ring. However, the PMOS pull-up driver makes the signal edge rate much slower than the GTL driver, which limits the frequency resolution for package model validation. The push-pull I/O test IC consists of 40bits serial-to-parallel converter, 4:1 multiplexers, clock retimer and a 10 port push-pull I/O driver. Because of the use of a 4:1 multiplexer, this chip generates four times faster output signals than the input serial data. This chip was designed and fabricated using IBM7WL 0.18um BiCMOS process.

4.3.1 40 Bit Serial-to-Parallel Converter

The basic operation of the 40 bit serial-to-parallel converter is the same as the one used in GTL I/O test IC. 250MHz clocked 40 bit serial data from an external stimulus system are stored inside the basic cell and the IC fired 40 bits parallel data into 4:1 multiplexers when the select signal goes to low. Figure 4-10 shows the block diagram of this converter having ten 4:1 multiplexers. For the basic cell, transmission gate based master-slave flip-flops were used as shown in Figure 4-11 (A). The overall layout for serial-to-parallel converter is shown in Figure 4-11 (B).

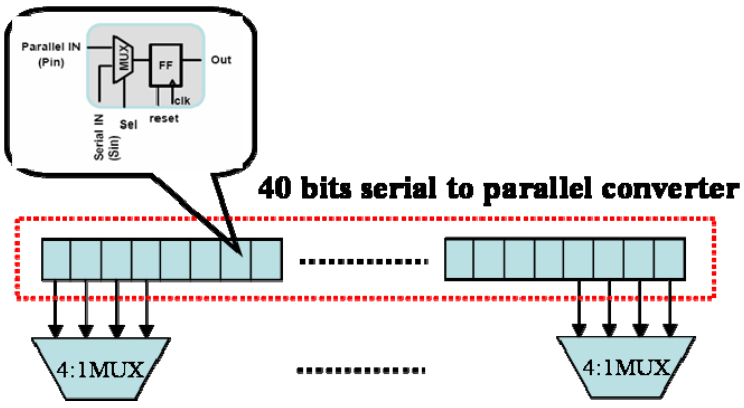
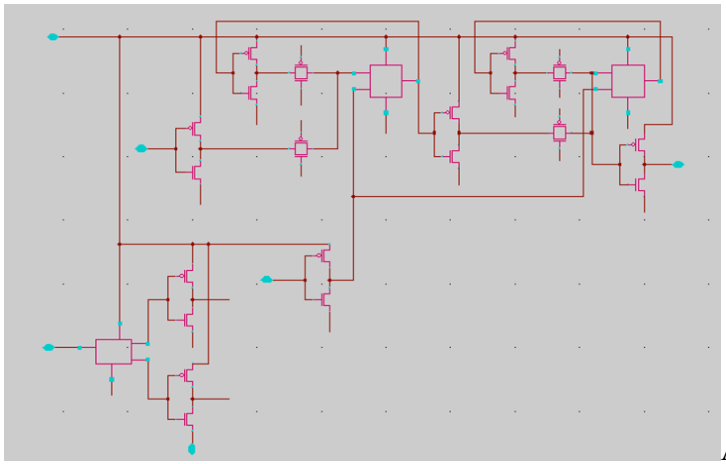


Figure 4-10. 40 bit serial-to-parallel converter and 4:1 multiplexers.


A

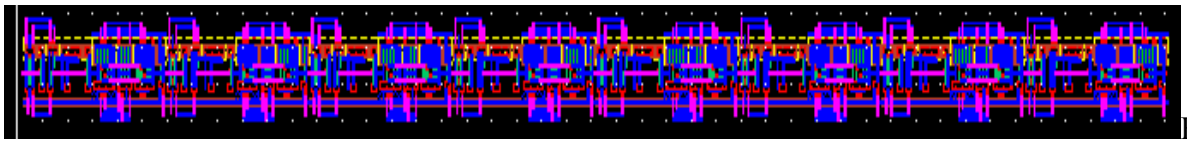

B

Figure 4-11. Flip-flop and serial-to-parallel converter. A) Transmission gate flip-flop. B) Layout for 40bits serial-to-parallel converter.

4.3.2 Single-Ended 4:1 Multiplexer

A 4:1 multiplexer was designed using a tree architecture which consists of three 2:1 multiplexers. A 2:1 multiplexer is composed of MSFF, MSMFF and a 2:1 selector. Figure 4-12 shows the block diagram of the 4:1 multiplexer. As shown in Figure 4-13 (A), MSFF and MSMFF in the 2:1 multiplexer make a one-half clock period time delay between their outputs so that the 2:1 selector has proper data timing. In this way, the output of the 2:1 multiplexer is 2 times faster than the input data. Figure 4-13 (B) shows the final 2:1 multiplexer generating 1 Gb/s output data. All the sub circuits were designed using single-ended CMOS logic and Figure 4-14 shows the layout.

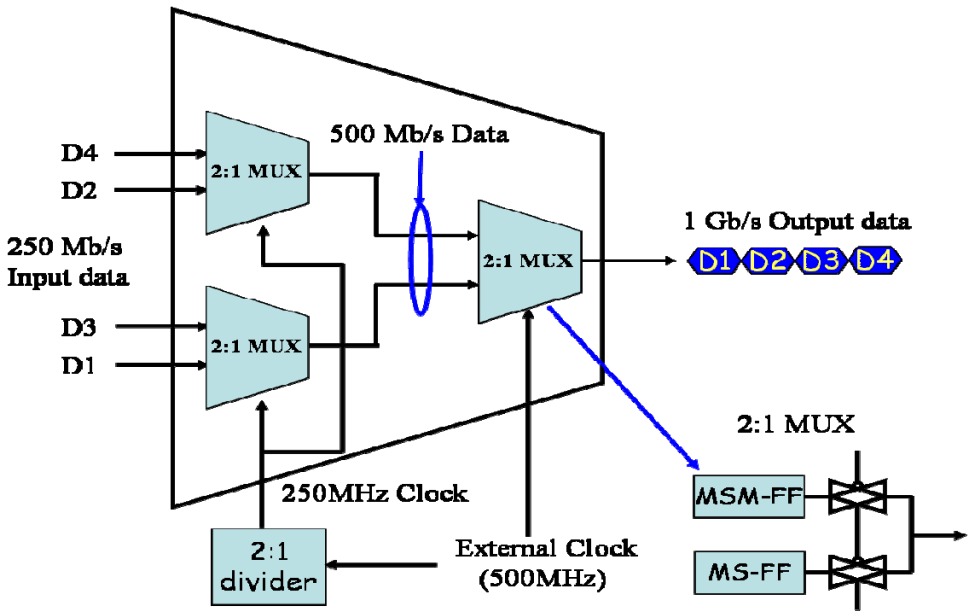


Figure 4-12. Block diagram of 4:1 multiplexer.

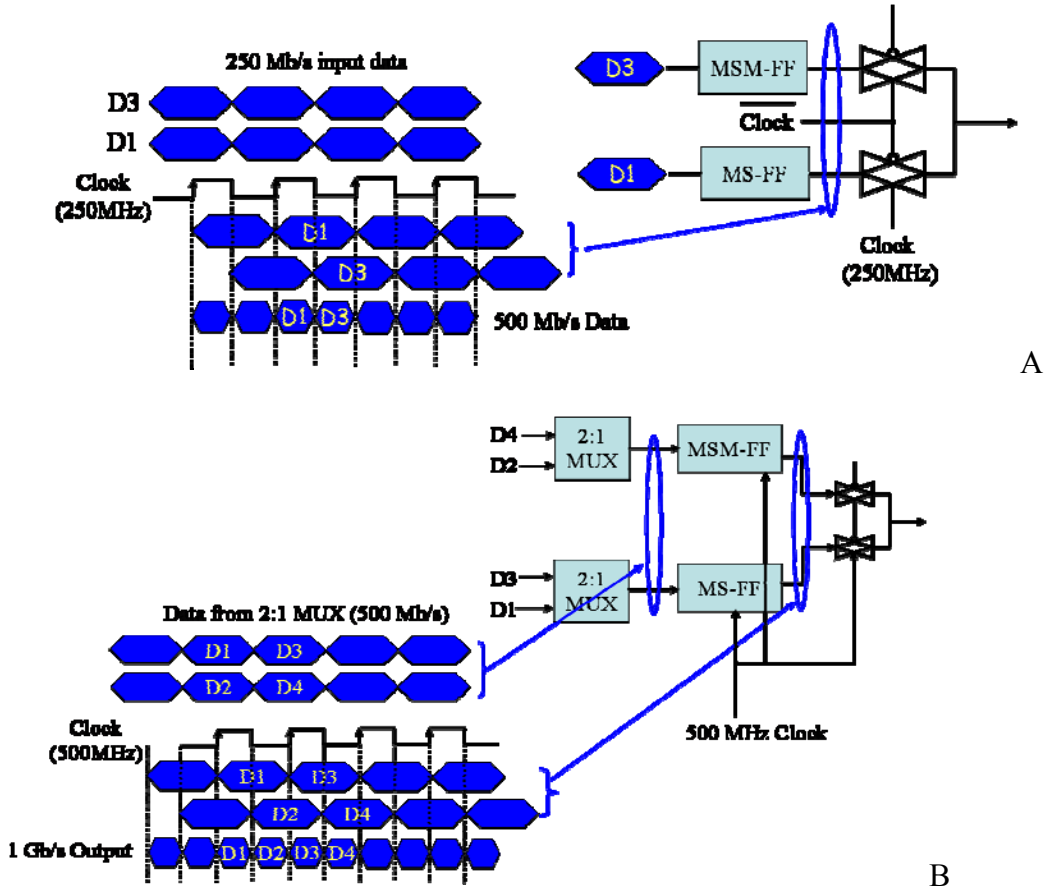


Figure 4-13. Tree multiplexer. A) 2:1 multiplexer. B) 4:1 multiplexer having 1Gb/s output.

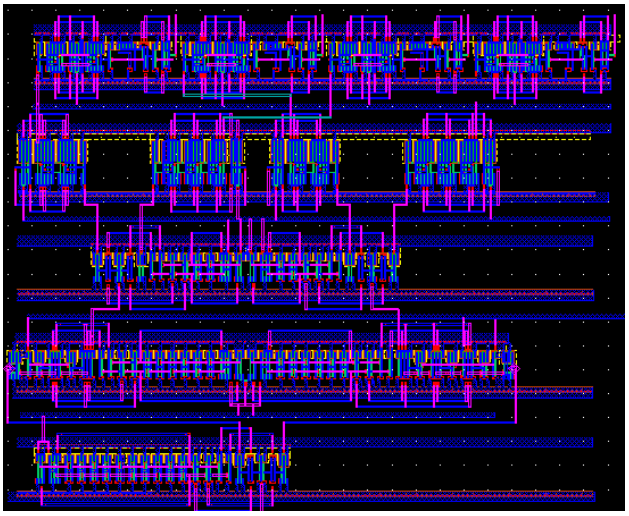


Figure 4-14. Layout of 4:1 multiplexer.

4.3.3 Clock and Data Retimer

There are two different clock domains in the push-pull I/O test IC. A 500MHz system clock was provided by an external stimulus system and a frequency divider that generates a 250MHz clock for the serial-to-parallel converter was on-chip. 4 retiming flip flops were used to synchronize the input data and select signals to the 250MHz clock. Because the output parallel data from the serial-to-parallel converter is transferred to the 4:1 multiplexer, the same inverter chain based clock drivers are used in order to minimize the clock skew between the 250MHz clock signals of the serial-to-parallel converter and the input 2:1 multiplexer in the 4:1 multiplexer. Figure 4-15 shows the overall block diagram for the clock and data retimer. In contrast to the GTL clock receiver which is NMOS input buffer, a rail-to-rail input buffer shown in Figure 4-16 was used to cover CMOS input levels.

4.3.4 Push-Pull I/O Driver

The push-pull I/O driver consists of a pre-driver and an off-chip driver. The size of the off chip driver was chosen such that it can generate V_{OH} of 1.5V with an off chip $50\,\Omega$ load.

Because this driver has large PMOS and NMOS devices, it generally needs a pre-driver in order to reduce the loading of the core circuits.

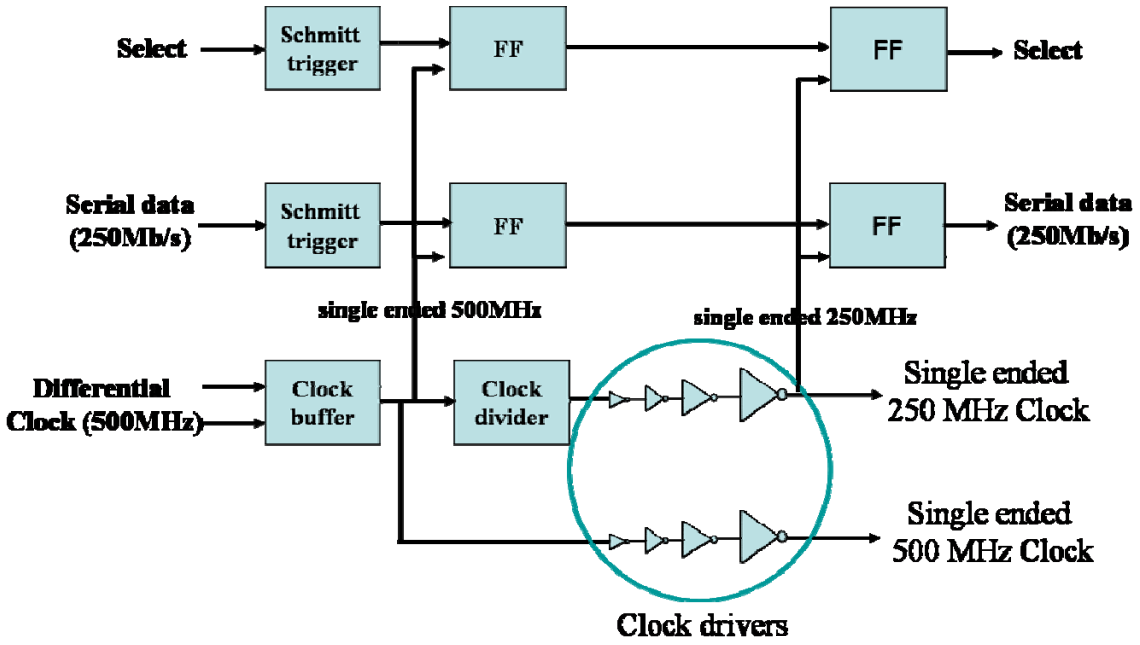


Figure 4-15. Clock and data retimer.

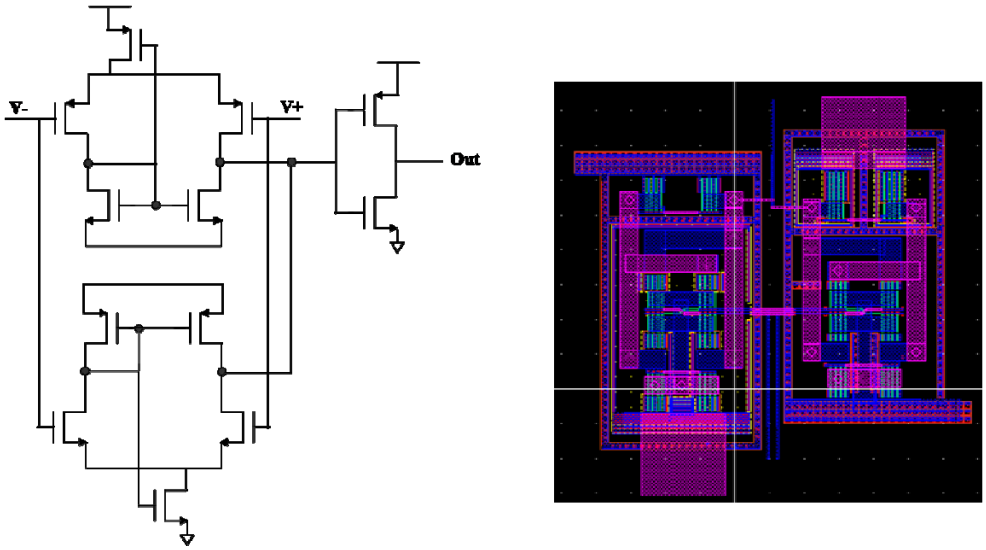
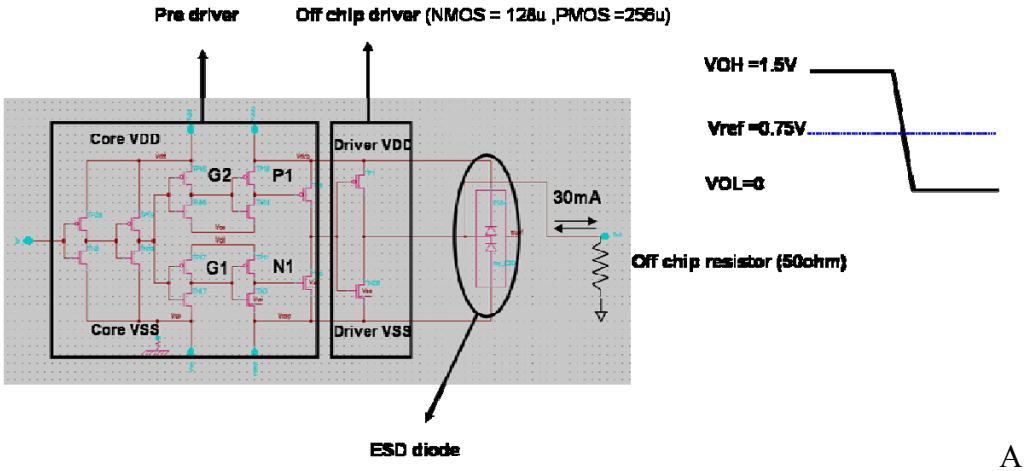


Figure 4-16. Rail-to-rail clock receiver.

To provide the best drive capability and noise immunity for the driver transistors, separate pre-driver inverters are connected to each PMOS and NMOS transistor. As shown in Figure 4-17 (A), P1 would momentarily be turned on when ringing on the off-chip-driver Vdd rail exceeds

core logic Vdd by a threshold voltage if its gate is connected to core logic Vdd. This can be avoided by using G2 to connect P1's gate [4.3]. Besides, P1 has the best drive capability because it is turned on by G2 which is connected to the clean core VSS.



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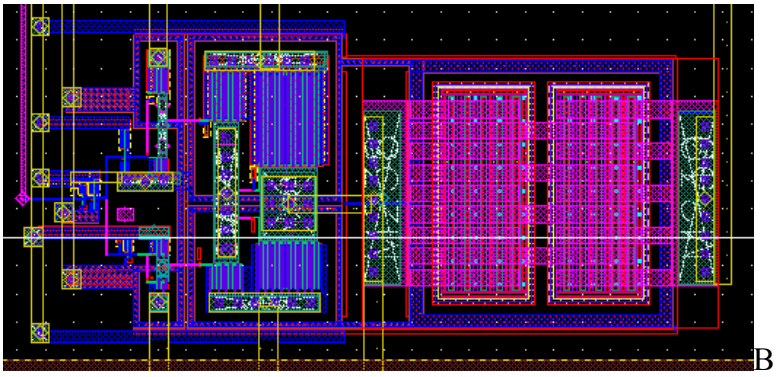


B

Figure 4-17. Push-pull I/O driver. A) Schematic. B) Layout.

4.3.5 Simulation Results

A 10 port push-pull I/O driver was simulated with the Amkor wire bond RF package. Figure 4-18 shows the I/O pad arrangement and chip layout. The rise time of the output signal at the chip bond pad is 100ps which corresponds to a knee frequency of 3.5 GHz. The simulation was performed with 1Gb/s data and Figure 4-19 shows the simulation results from a 1Gb/s switching output and package ground noise when ten push-pull I/O drivers switch simultaneously. A 1Gb/s PRBS data was used to generate the eye diagram.

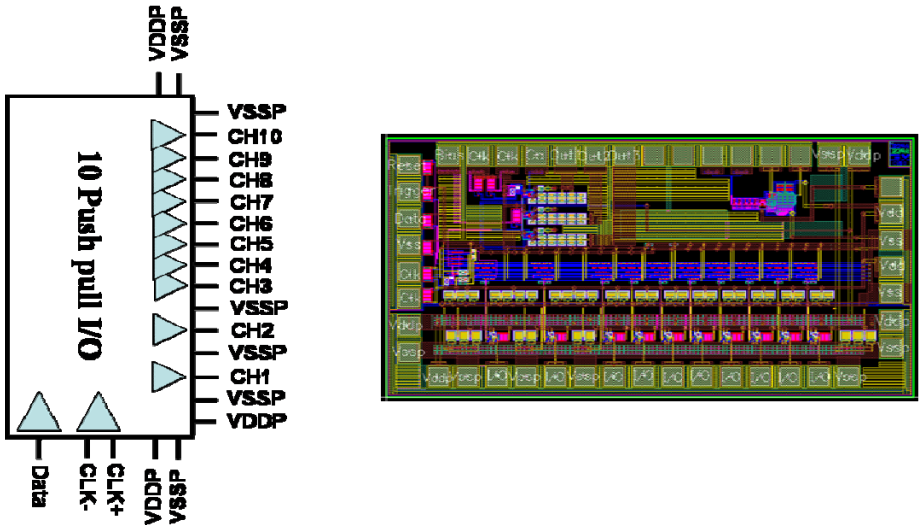


Figure 4-18. I/O pad arrangement and chip layout.

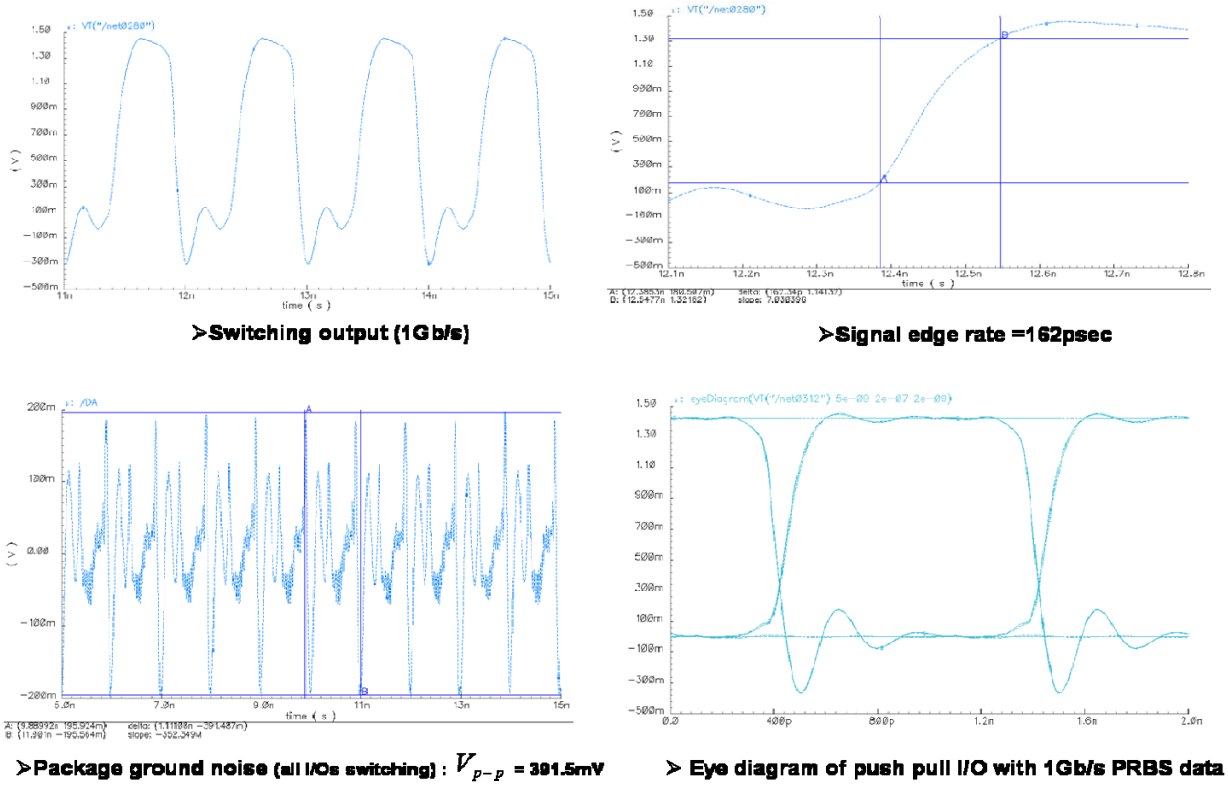


Figure 4-19. Simulation results of push-pull I/O test IC.

In summary, this chapter presented the circuit designs of the sub-blocks in the 10 port GTL I/O and push-pull I/O test IC. Simulation results at 1 Gb/s were presented to show the chip

performance and functionality. These chips are used to characterize signal integrity for single-ended I/O test IC-package systems and validate the corresponding package electrical models. The next chapter presents the concept of an IBIS macro model in detail and how an IBIS macro model created from I/O test ICs can be applied for signal integrity verification of complicated IC packages.

CHAPTER 5
PACKAGE MODEL VERIFICATION USING IBIS MACROMODEL

5.1 Introduction

This chapter shows how I/O test ICs can be efficiently used for signal integrity verification of a package electrical model. The concept of an IBIS macromodel based I/O test IC is introduced to show how real I/O test ICs can be represented in a SPICE-like circuit simulator. For demonstration purposes, 4 port push-pull I/O drivers had been simulated with an Amkor lead frame package to prove that the IBIS macromodel can effectively validate problems with package SPICE electrical models with respect to signal integrity performance.

5.2 The Background of IBIS Macromodel

As explained in chapter 1 shortly, there are procedures on how to use I/O test IC to validate the accuracy of package electrical model and this section explains in detail about the IBIS macromodel which is created from high impedance probing and time varying voltage source modeling. The basic idea of a package model verification is to compare the SPICE circuit simulation results, which is generated from IBIS macromodel-package SPICE model, to measurement results, which is generated from a actual I/O test IC-package system. If the test IC has the same measurement results as simulation, the whole I/O test IC chip-package system can be compared with SPICE-like circuit simulations and real measurement results with high accuracy. However, a real chip normally has process variations and that can be more than +/- 20%. As shown in Figure 5-1, the V-I curve for a 65nm NMOS has a +/- 20% process variation. Therefore, before performing the SPICE-like circuit simulation, an I/O test IC should be modeled in such a way that the model accurately reflects the I/O test IC's performance characteristics. This is similar to conventional buffer modeling and there are three general types of models for buffers used for simulations in digital systems: (1) linear models (2) behavioral

models, and (3) full transistor models [2.7]. Linear models assume that the I/O buffer has a linear I-V curve during the operation in order to model the buffer with a linear resistor. In contrast to a linear model, a behavioral model is more accurate because it uses I-V curves similar to real transistor curves.

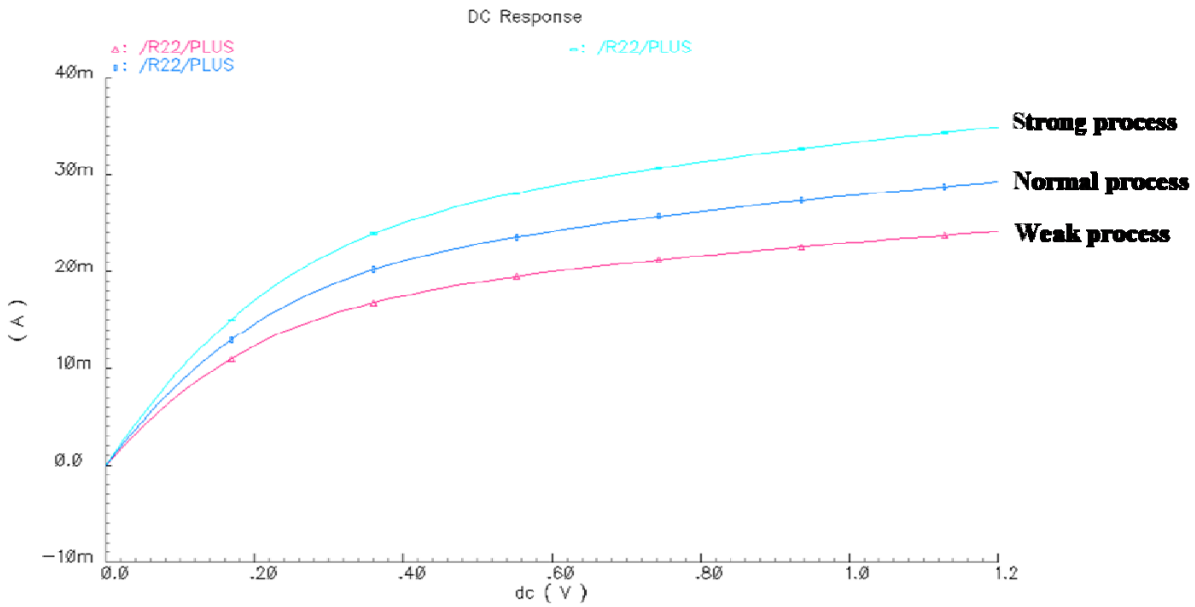


Figure 5-1. Process variation of V-I curve for a 65nm NMOS transistor.

A full transistor model is most accurate because it includes all the detailed information of a real transistor, but the simulation time is huge and it can disclose substantial information such as circuit connections and process parameters. Nowadays, most integrated circuit companies in the high-speed I/O area are using IBIS (I/O Buffer Information Specification) to model the I/O buffer. IBIS is a fast (25 times faster than a full transistor simulation) and an accurate behavioral method of modeling input/output buffers based on I-V (current/voltage) table data derived from measurement or full circuit simulation [2.9]. However, existing IBIS simulators work for low speed differential I/O and IBIS has limited capability to simulate transceivers and drivers that use pre-emphasis [2.9]. In order to overcome this problem, this research used an on-chip high impedance probing technique in order to create a IBIS macromodel for I/O test ICs. Since time

varying voltage amplitudes measured from the high impedance probes have dynamic buffer impedance information, these voltage sources will generate the same amount and direction of time varying current as present on the package. Dynamic current information is most important in validating the package model because all the signal integrity issues come from when signal and return current meet the non ideal interconnect associated with package. I/O test ICs are composed of a core circuit block and I/O buffers driving the off chip $50\,\Omega$ load. There can be many on chip pads to be probed and if the coupling between the I/O signals and core logic signals is sufficiently high, this will affect to the overall package signal integrity. Test ICs were designed such a way that all the input signals were placed orthogonally to the I/O signals. Therefore, they do not affect to the I/O buffer signals, removing the need for on-chip probing of input signal pads. However, supply and power pads for internal core logic gates should be probed because they affect the total amount of time varying current inside the package. Current transients due to the core logic gates switching activity give rise to signal fluctuation in power and ground layers in a multilayer package which couples to the I/O signal traces. In designs employing deep sub-micron technology, high operating frequency, and short rise and fall times, ground bounce due to switching in internal circuitry becomes a potential problem [5.1]. Many studies have been done to analyze the SSN effects caused by internal gate switching [5.2]. Because of this reason, all chip pads for power and ground (core VDD and VSS, I/O VDD and VSS) need to be probed in order to accurately model the I/O test IC. Figure 5-2 illustrates how transient currents and voltages are going to change in multilayer BGA package according to the switching activities of core logic and I/O buffer. Figure 5-3 shows the actual I/O test IC reproduced by IBIS macromodel.

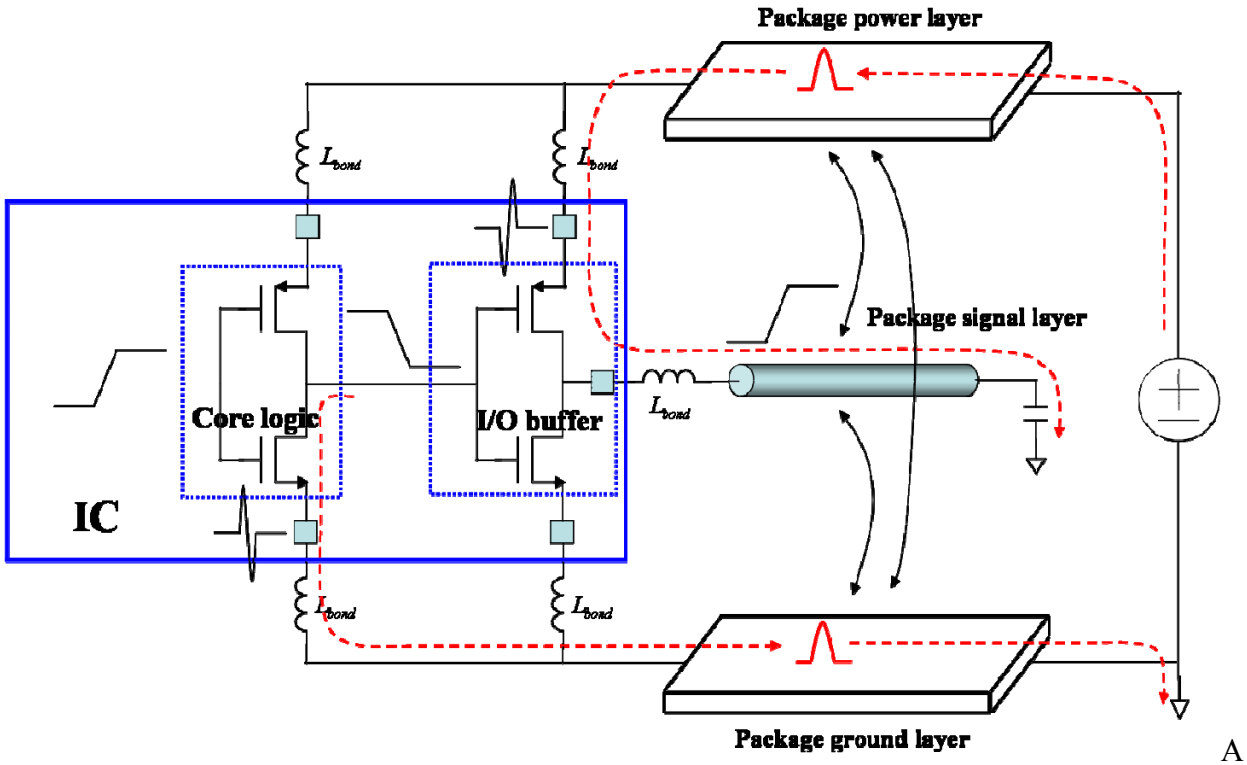


Figure 5-2. Transient current and voltage in multilayer BGA package. A) When I/O buffer switches from low to high. B) When I/O buffer switches from high to low.

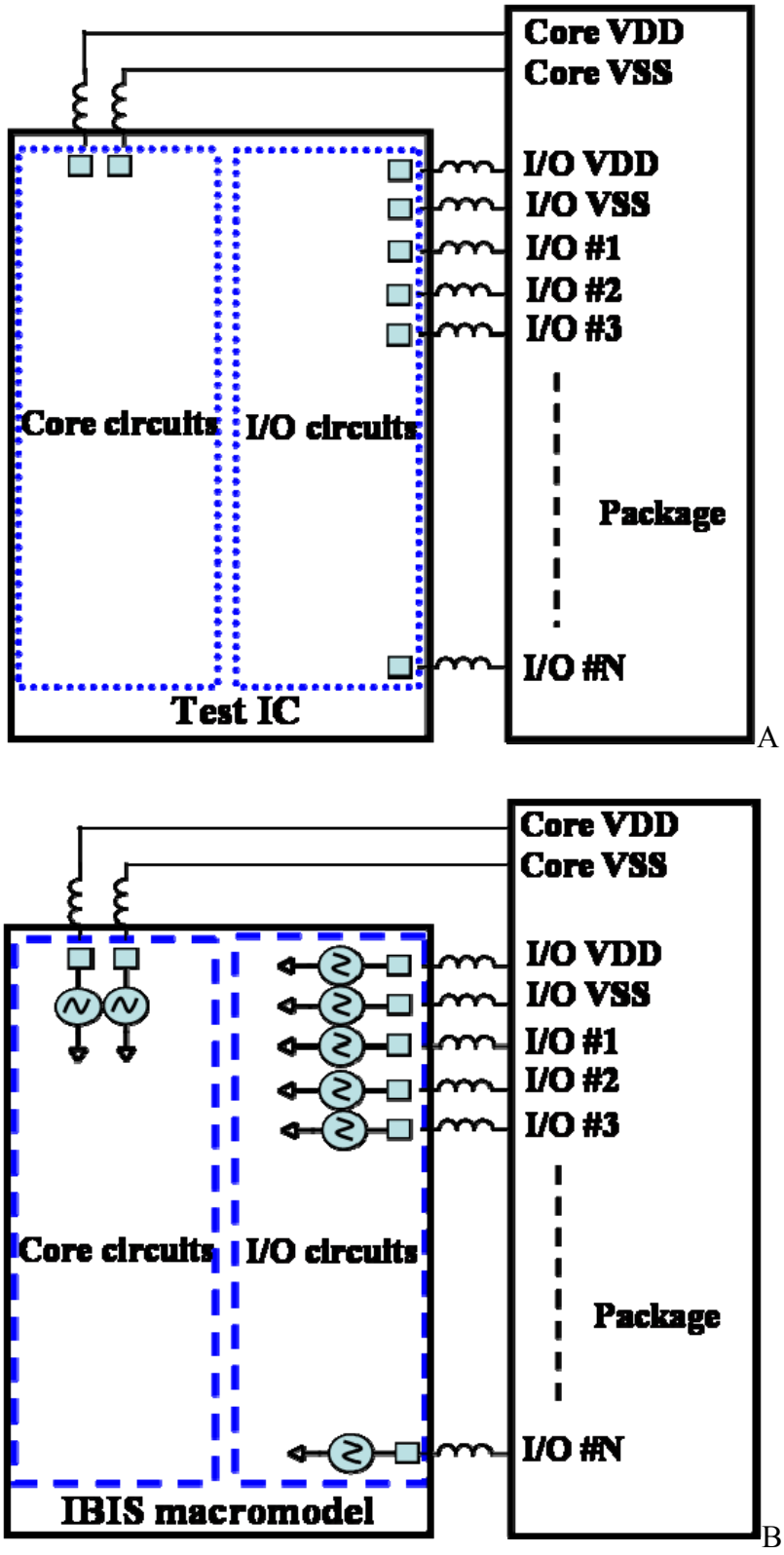


Figure 5-3. IBIS macromodel generation. A) Actual I/O test IC. B) IBIS macromodel.

5.3 Demo Simulation for Package Electrical Model Verification

In this section, simulation results are shown to prove how IBIS macromodel can be used to validate the package electrical model with respect to signal integrity performance. Figure 5-4 (A) shows a test IC which consists of I/O buffer and core logic. In this simulation, four port push-pull I/O drivers driving off chip 50Ω load were chosen for an I/O buffer and four inverters driving each I/O driver were used for core logic. Figure 5-4 (B) is IBIS macromodel for the test IC and is used for a SPICE-like circuit simulation. All simulations were performed with modified version of the Amkor lead frame package. Some portions of package element have been modified such that it is similar to a multilayer BGA package. A 50Ω transmission line whose length is 1cm had been added between bond wire and lead frame to look at the effect of the long package inner trace which causes propagation delay and signal reflection. The Amkor package is a single metal layer package which doesn't include separate VDD/VSS reference planes. Multi-layer packages such as BGA are becoming dominant for highly integrated VLSI chips because they provide power and ground rings which lead to a reduction in the VDD/VSS reference inductance. In order to investigate the effect of reference plane (VDD/VSS) parasitics, an equivalent circuit for power and ground in the Amkor package has been replace by a simple parallel LC circuit. Although the current distribution in the planes can be modeled by employing a network composed of many RLC-grid-type cells as shown in Figure 5-5, it is very cost-inefficient to evaluate the package performance with such a large network by using a general-purpose circuit simulator (i.e., SPICE) because of the huge amount of a computation time [5.3]. In this simulation, effective inductance values for partial power and ground planes calculated from [5.3] were used to represent the whole power and ground planes. However, actual measurement data was used for bond wire and lead frame and Figure 5-6 shows the Amkor package model modified from the original one.

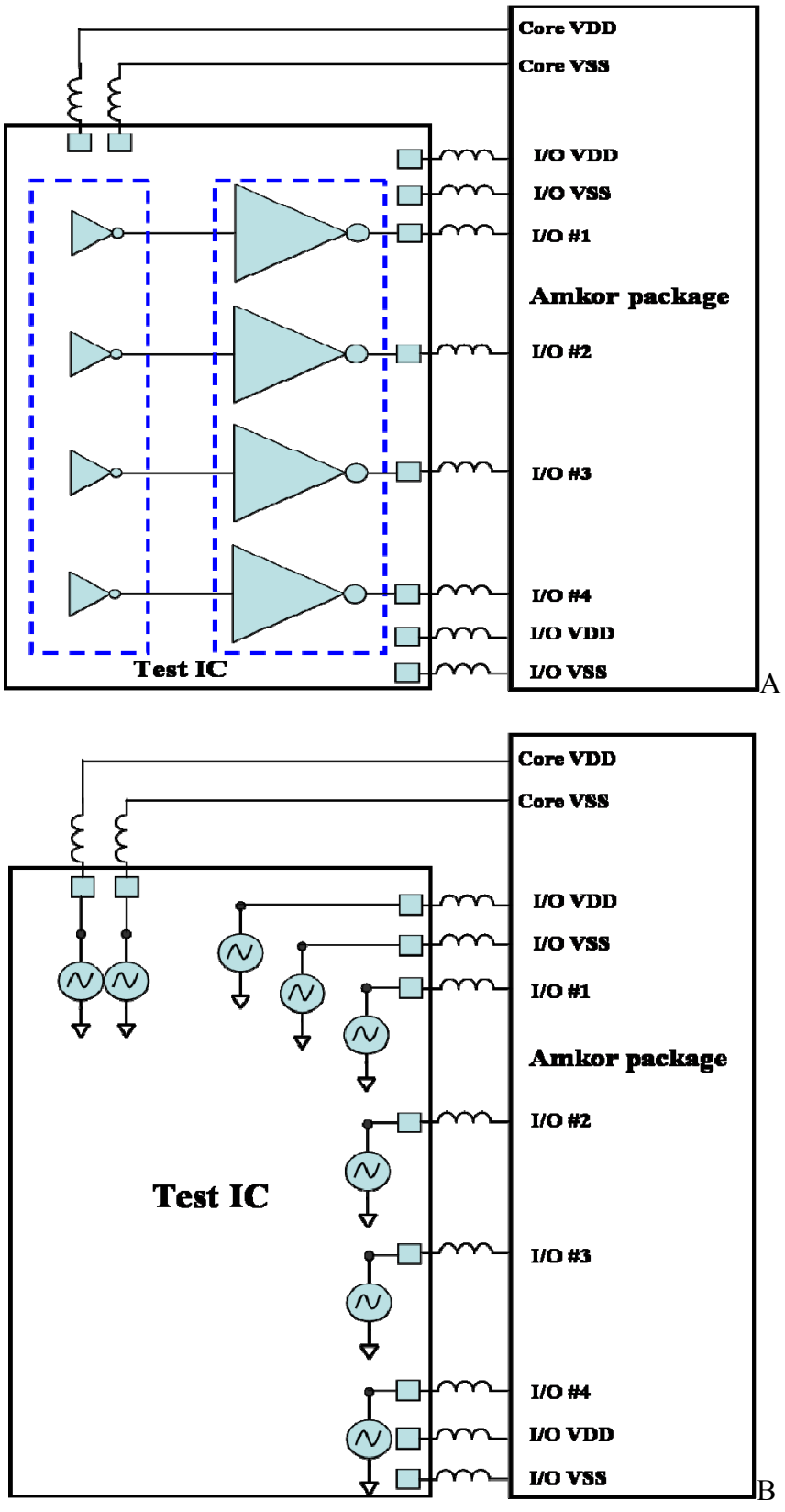


Figure 5-4. 4 port push-pull I/O test IC. A) Actual circuit. B) IBIS macromodel.

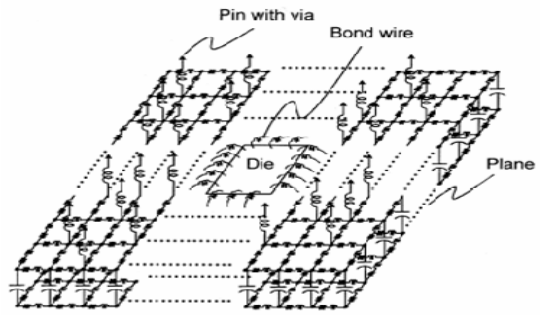
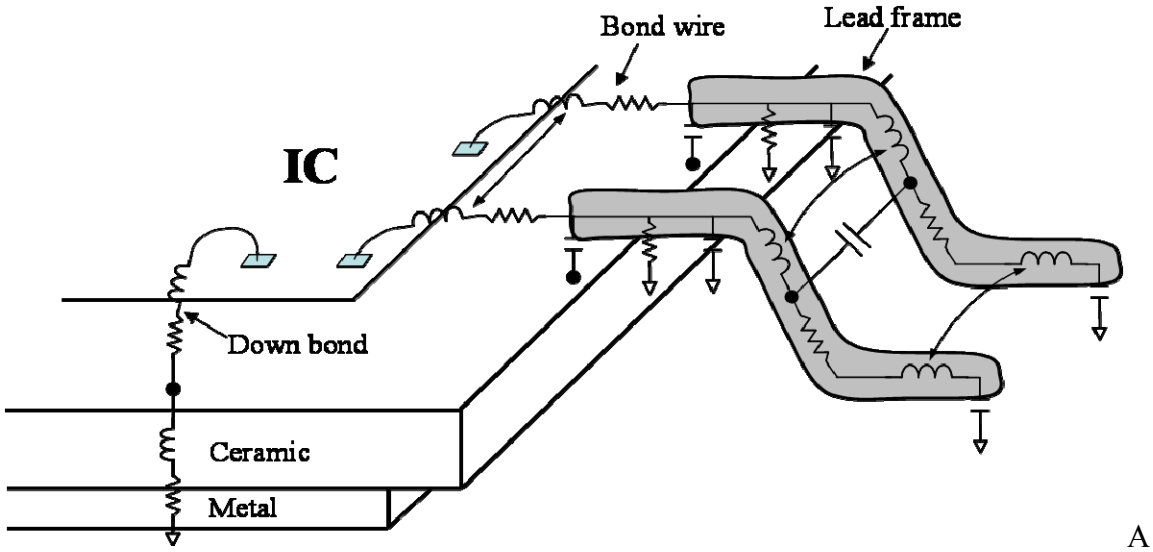


Figure 5-5. Distributed circuit model for a package power and ground layer.



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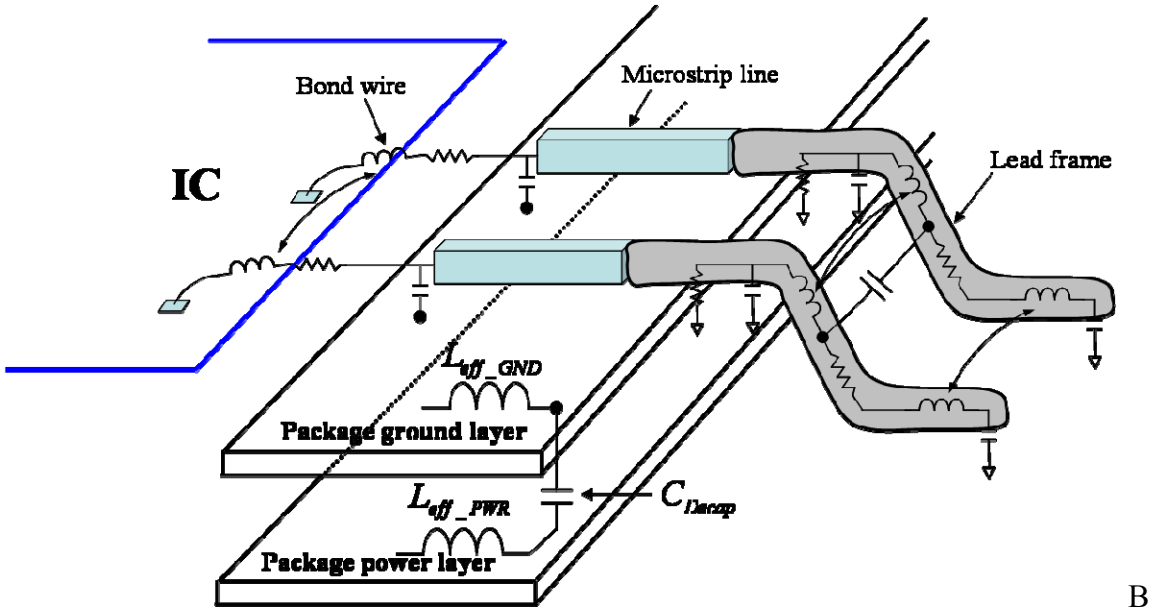


B

Figure 5-6. Amkor package model. A) Original package. B) Modified package.

The quality of IBIS macromodel needs to be evaluated by comparing the signal shapes from simulations of I/O test IC-package system utilizing IBIS macromodel as well as transistor-level SPICE model. Figure 5-7 shows this bench test schematically and the results of a full transistor model simulation are compared with a simulation utilizing the I/O test IC's IBIS macro model, as shown in Figure 5-8. The overall signal shapes are exactly same, indicating that IBIS macromodel can accurately reproduce the behavior of a full transistor model based I/O test IC.

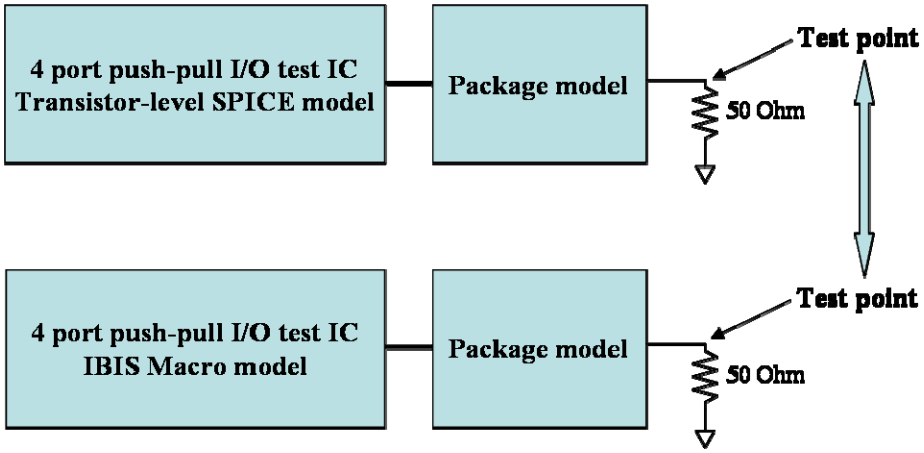


Figure 5-7. Schematic for bench test comparing full transistor model and IBIS macromodel.

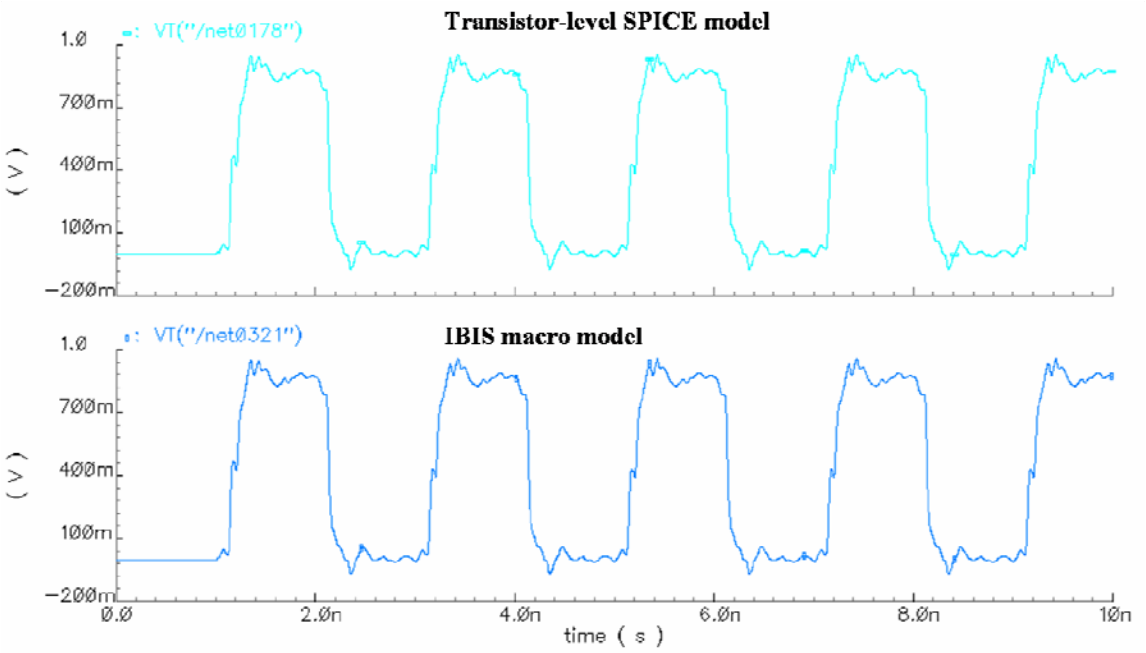


Figure 5-8. Simulation results showing the quality of IBIS macromodel.

The IBIS macromodel is best suited for package signal integrity analysis and model verification and four cases of signal integrity simulations performed are

Case 1) Package inner trace effects on signal waveform: propagation delay, ringing due to impedance mismatch, signal amplitude reduction due to the frequency dependent loss.

Case 2) Far end cross talk (FEXT): mutual coupling effects due to the mutual inductance and capacitance.

Case 3) Inter-symbol interference (ISI) or data dependant jitter (DDJ): a variation of signal amplitude and zero crossing point depending on data pattern.

Case 4) Simultaneous switching noise (SSN): package power and ground layer fluctuation due to the simultaneous switching drivers, the effect of incorrect electrical models for package reference (power and ground layer).

For case 1), only one driver is driven to switch while the other drivers are quiet and off-chip 50Ω on board probe point is compared between SPICE simulations and measurements. Figure 5-9 shows the I/O test IC and equivalent IBIS macromodel. Figure 5-10 is the simulation result when the components for signal path are incorrectly modeled and it shows that two output signals have different waveforms, different amplitudes and propagation delays. Package elements for signal paths consist of bond wires, package traces and lead frames and incorrect modeling information is hidden into the combined effects of many package elements. But this measured empirical information can help the package engineer to change the package model so that IBIS macromodel can match the real I/O chip-package system. Mutual coupling effect, which is case 2, can also be investigated by comparing the signal at the far end of quiet driver (FEXT).

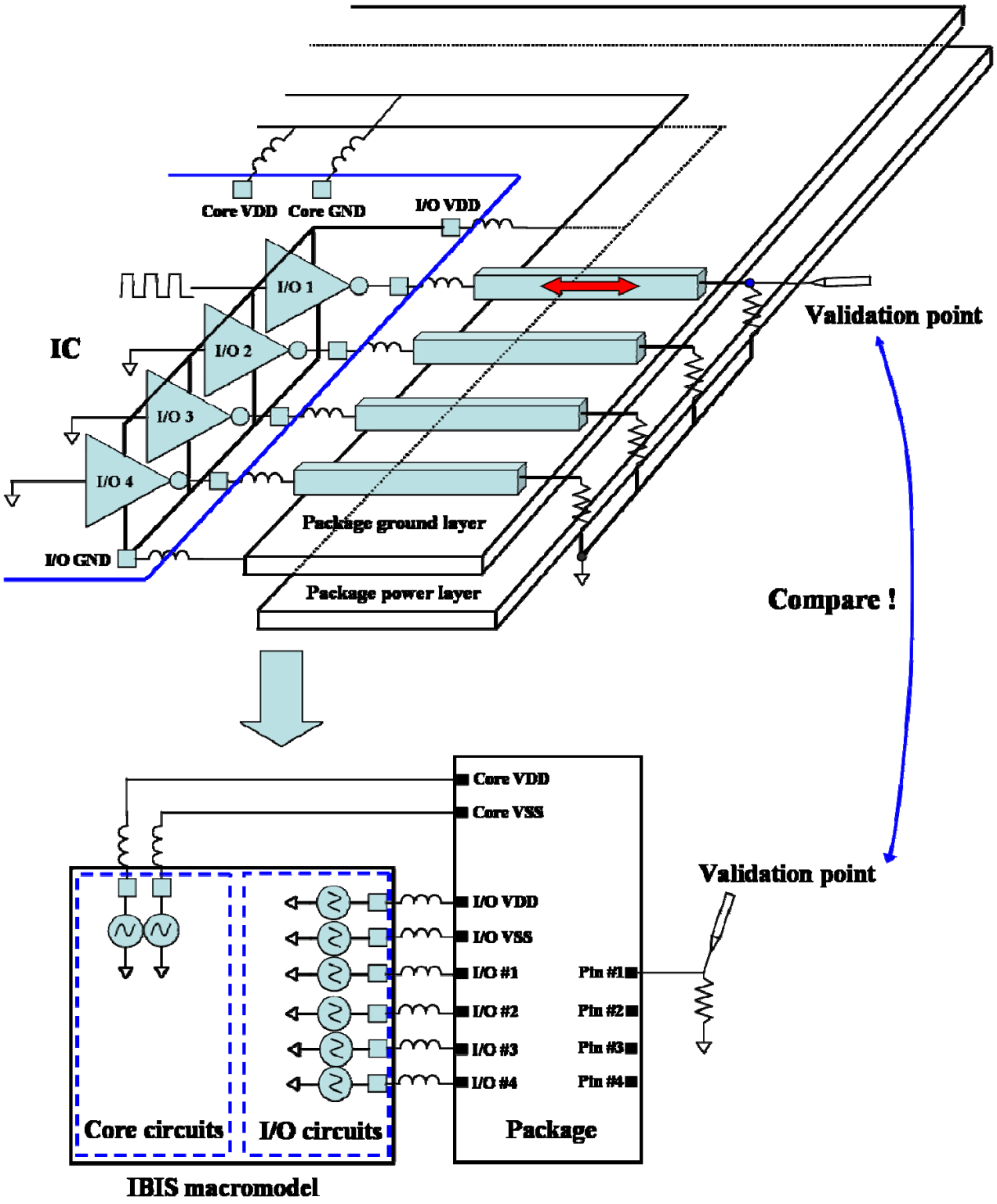


Figure 5-9. I/O test IC and equivalent IBIS macromodel.

Figure 5-11 shows the simulation results when mutual inductance and capacitance values are increased by 20%. Incorrectly modeled mutual coupling causes different amplitudes, but it doesn't change the waveform shape too much. A switching driver injects coupling noise to the quiet net through the mutual inductance and capacitance and the amount of noise depends on the signal rise time and mutual coupling factors. In other words, as an I/O test IC generates a faster signal edge rate, a smaller amount of incorrect mutual inductance and capacitance can be evaluated. An incorrect package model also creates different amounts of ISI, causing different eye diagrams. Figure 5-12 is the simulation result for an eye diagram when package traces and mutual inductances have incorrect values.

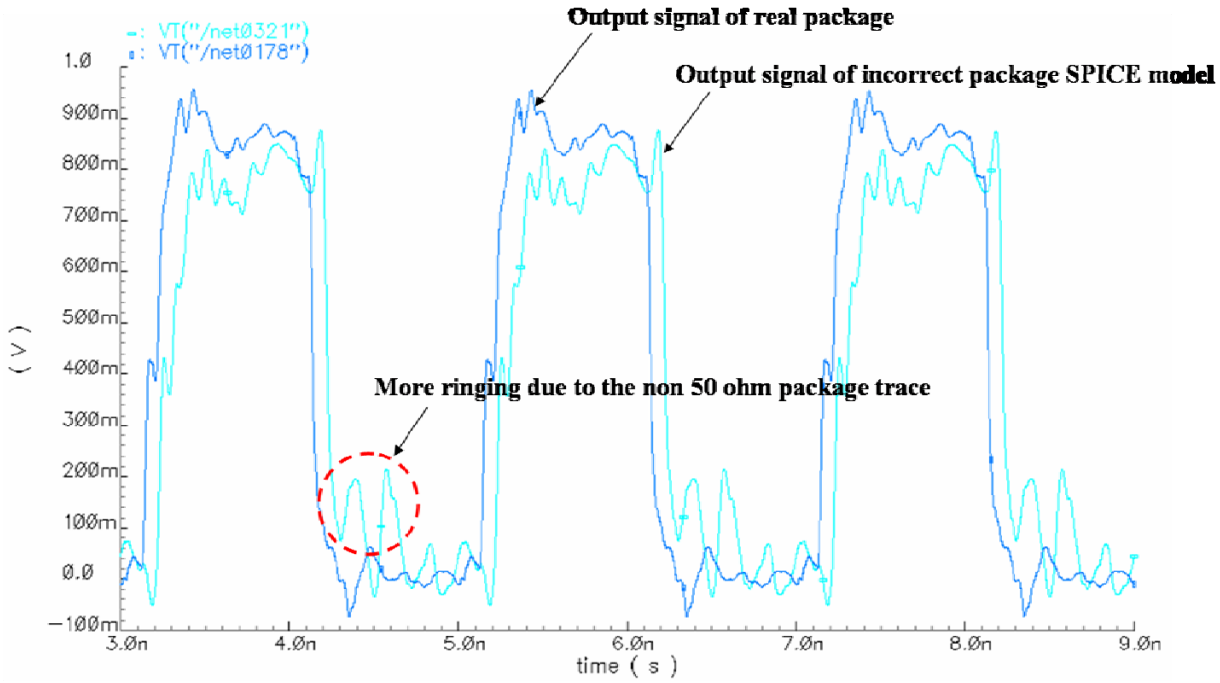


Figure 5-10. The effect of package trace on signal waveform.

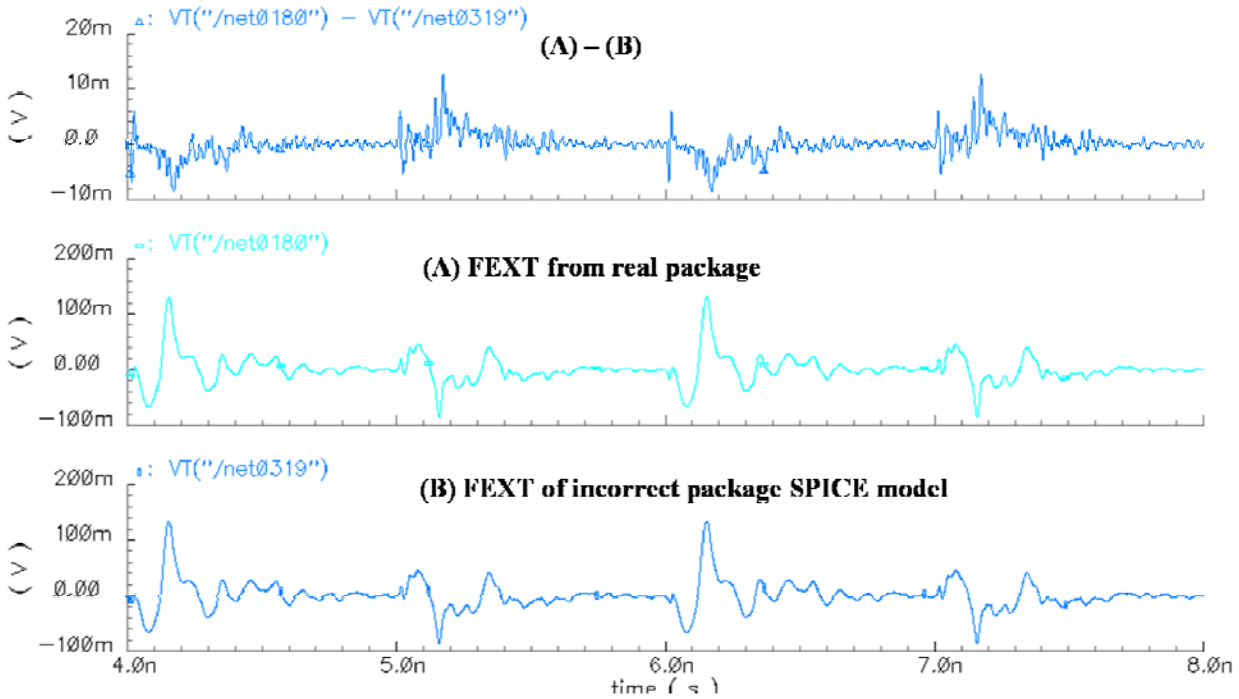


Figure 5-11. FEXT simulation results.

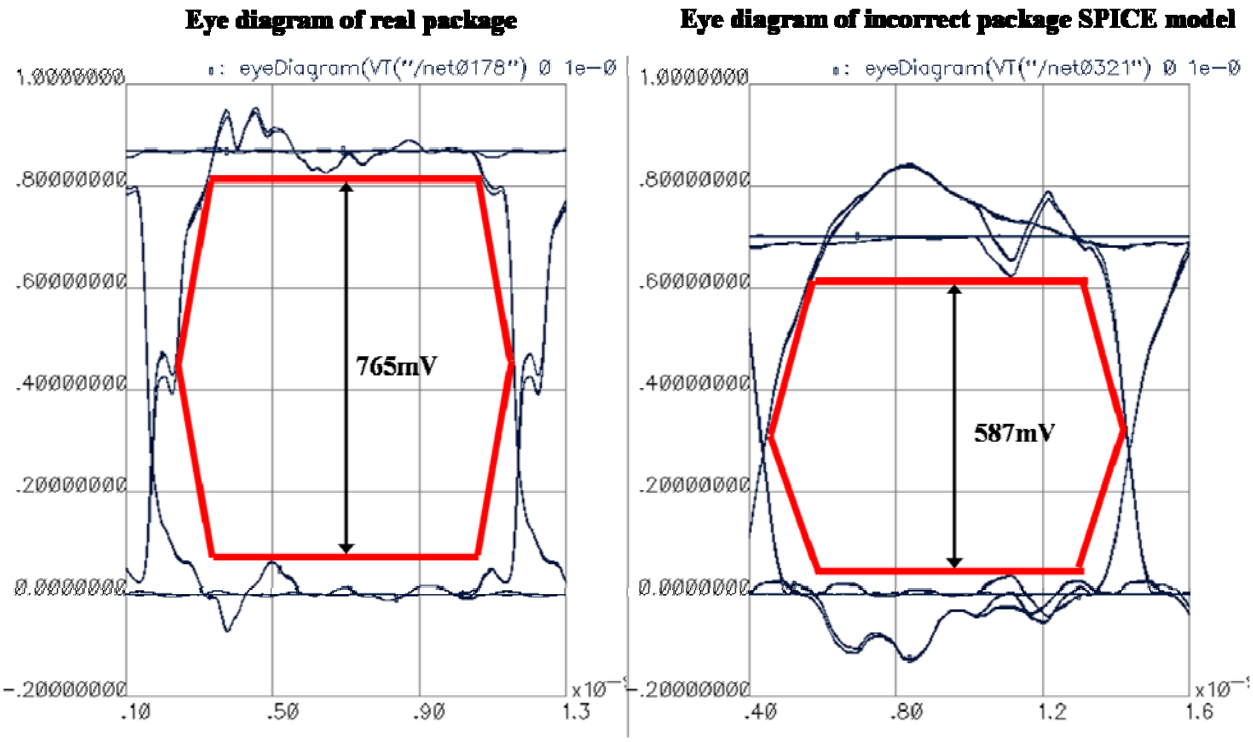
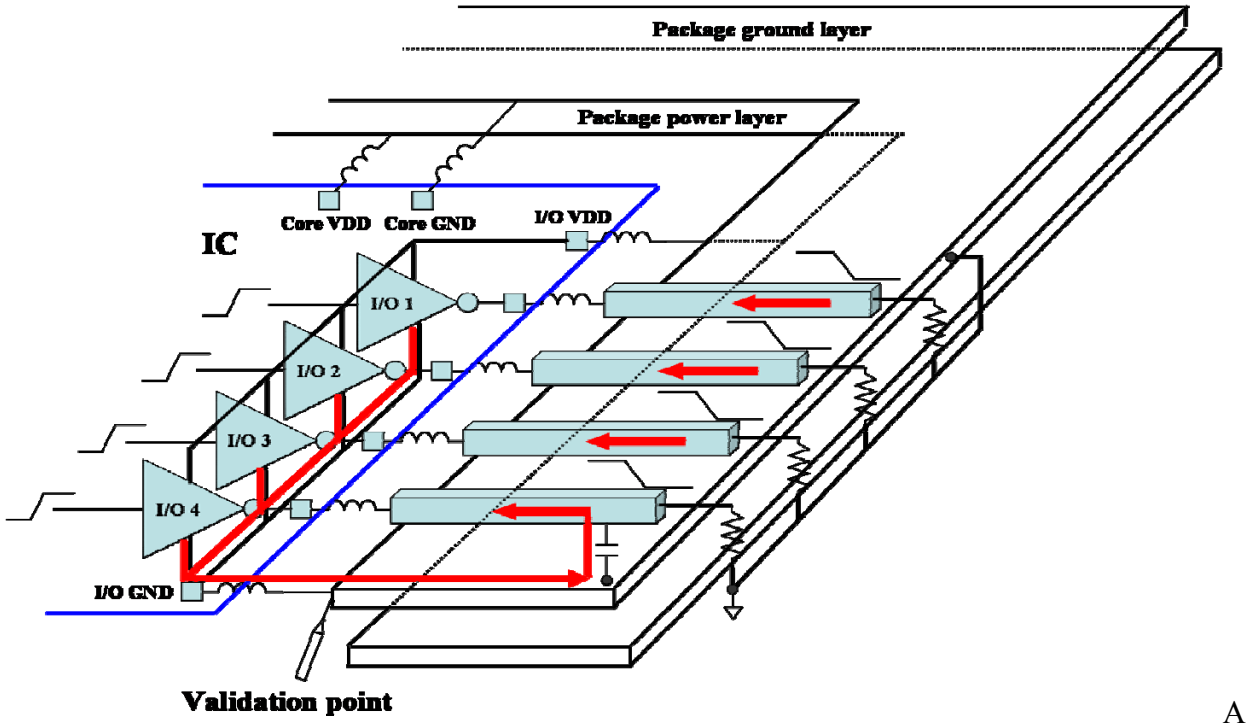


Figure 5-12. Eye diagram simulation results.

For case 4), all drivers are driven to switch simultaneously to inject current into the package power and ground plane. SSN is related to increases of the total current slew rate of the output buffers and the effective inductance of the power distribution system of the package and the board assembly [5.5]. Conventional modeling methodologies demonstrate that the on-chip parasitics and on-package parasitics are of great impact to the system level SSN. The driver circuits needs to be tuned such that the output waveform at the package pin, instead of the silicon pad, has proper voltage swing, rising/falling edge rate and duty cycle [5.6]. In other words, it requires IC/package co-simulation to estimate it precisely. Since the IBIS macro model already includes all the information about I/O circuit, SSN due to the incorrect package model can be precisely validated. Signals at the edge of package power and ground planes, which are close to the I/O test IC, are chosen to be the validation point because switching currents go through the reference planes and an incorrect model of the reference plane has a different signal waveform at this node. Figure 5-13 illustrates 3 dimensional current flowing when I/O buffers switch simultaneously. When the I/O drivers switch high-to-low, the drivers connect the ground plane to signal transmission line through a low impedance NMOS transistor. Current flows from the signal line to the ground plane. As the traveling wave propagates through the transmission line toward the driver end, charge flows out of the capacitance between the trace and the ground plane, discharging the trace down to ground. In this case, the current path is complete and there are no discontinuities for return current. When I/O drivers switch low-to-high, current flows from the power plane to the transmission line through the low impedance PMOS. However, charge flowing into the capacitance between the trace and the ground plane should be retuned to the power plane and there is a discontinuity between ground and power plane which increases loop inductance. In this case, the return current goes to the power plane through the decoupling



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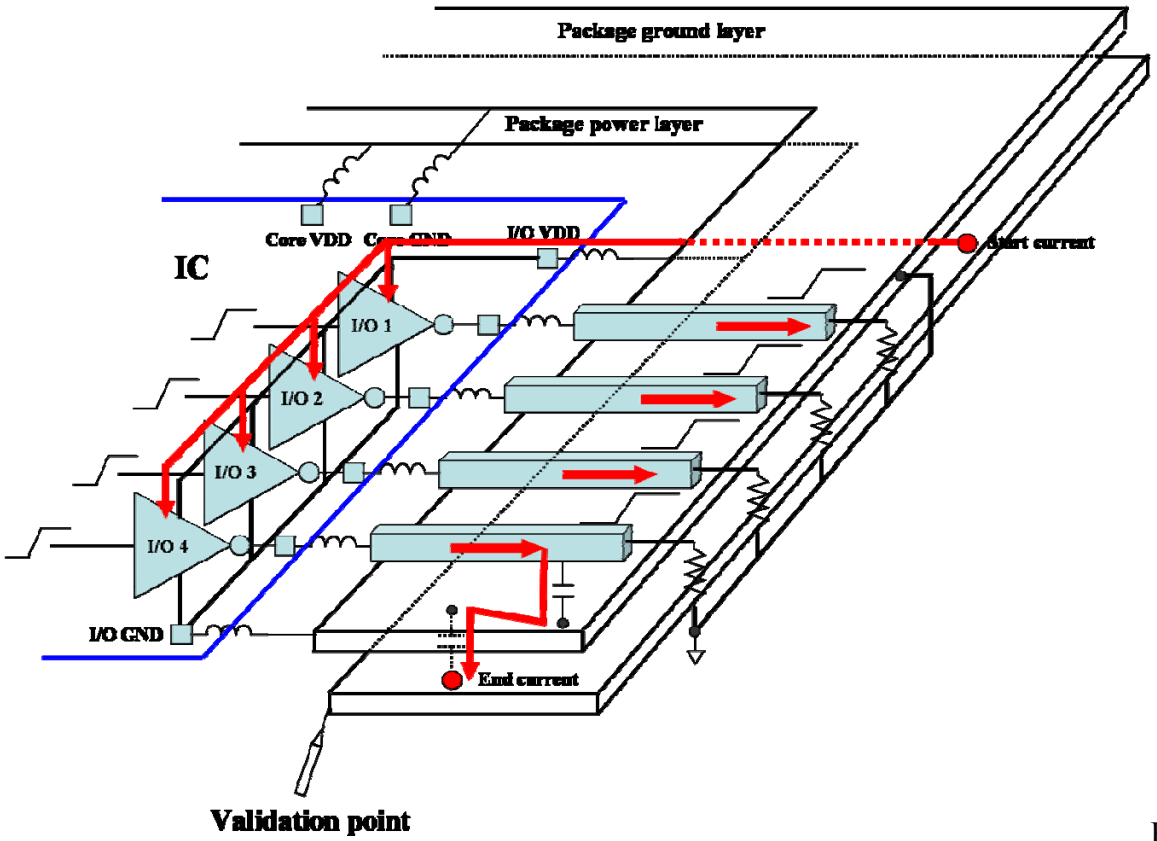
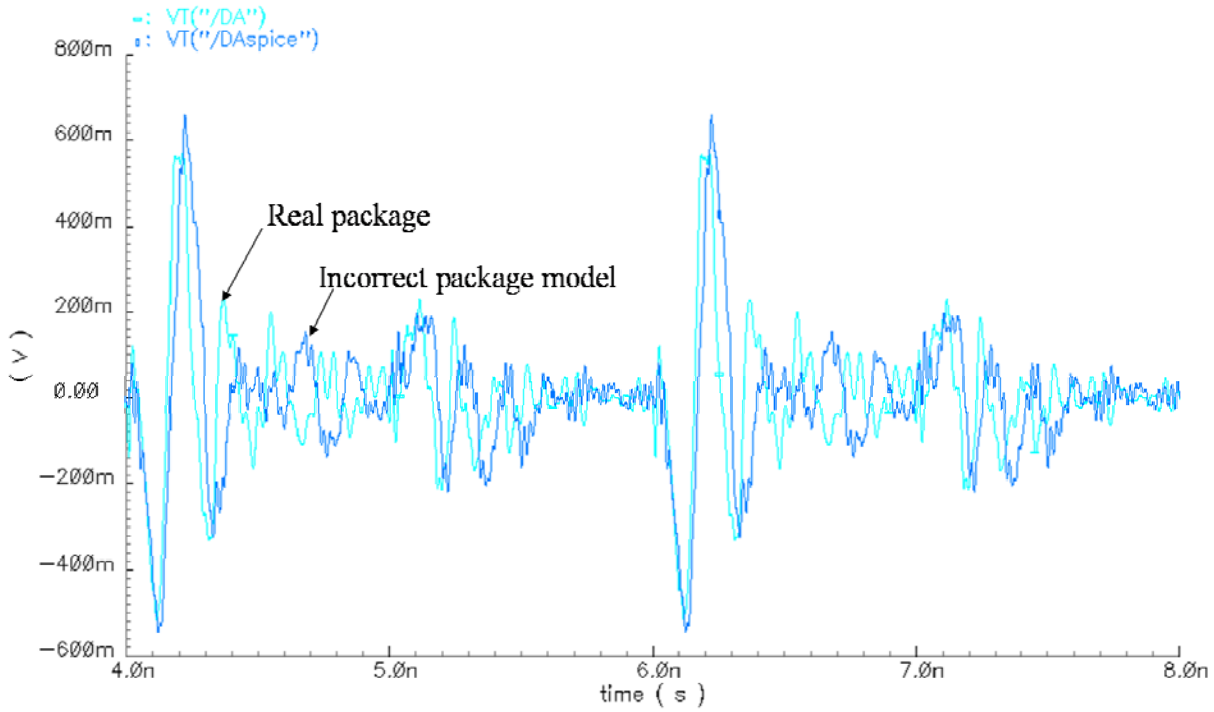


B

Figure 5-13. 3-D current flows for SSN. A) When all I/Os switch from high to low. B) When all I/Os switch from low to high.



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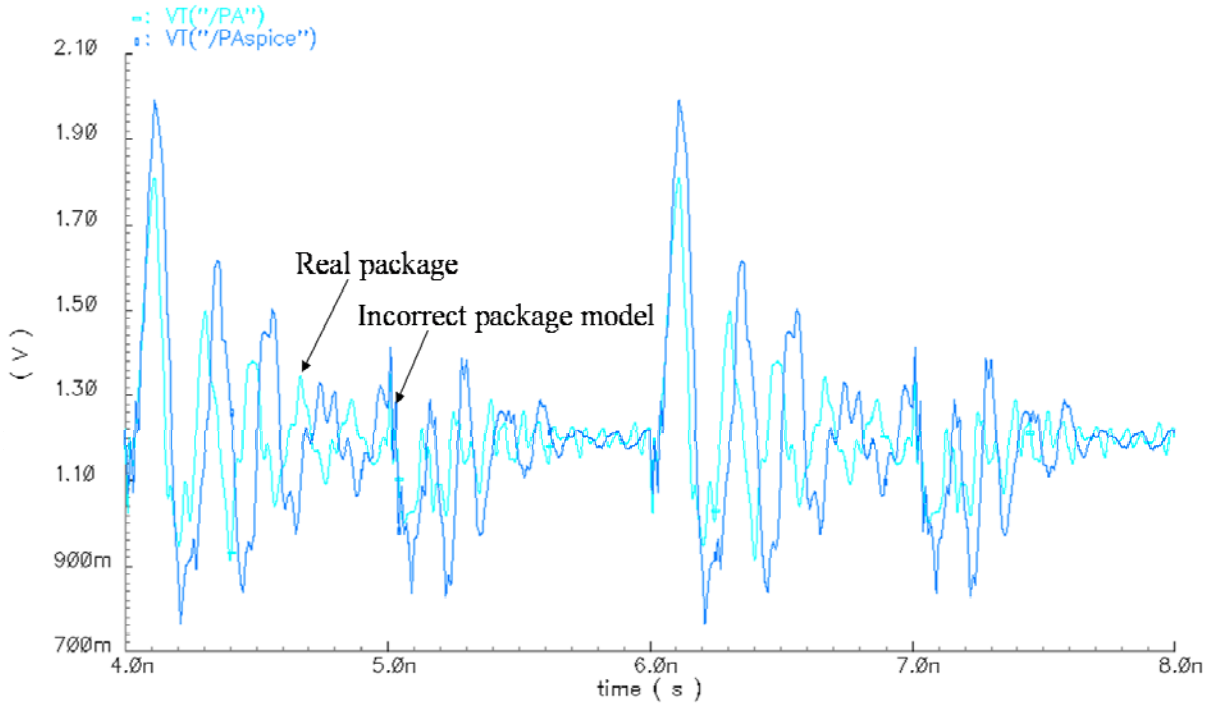


B

Figure 5-14. SSN simulation results. A) Package ground fluctuation. B) Package power fluctuation.

In this case, the return current goes to the power plane through the decoupling capacitances between the ground and power plane. Figure 5-14 show the simulation results showing the discrepancy between an incorrect package SPICE model and a real package when effective inductances for power and ground plane have +20% errors (L_{eff} for ground and power plane are increased by 20%, C_{decap} is decreased by 20%). An incorrect package SPICE model generates more noise than the real package because its L_{eff} value has become larger than the real value. Also, C_{decap} affects to the noise level by converting differential noise from power and ground layer into the common mode noise, which means a larger value of C_{decap} can reduce the peak noise value.

In summary, this chapter presented how an I/O test IC can be accurately reproduced by the IBIS macromodel. An IBIS macromodel is a fast accurate behavioral model which is best suited for signal integrity simulation. Four kinds of signal integrity simulation had been shown to prove that IBIS macromodel is very efficient in verifying signal integrity degradation due to the incorrect package model.

CHAPTER 6
MEASUREMENT RESULTS

6.1 Introduction

This chapter describes the measurement results from three I/O test ICs (Push-pull I/O, CML I/O and GTL I/O). All test ICs were assembled with the Texas Instrument Generic Ball Grid Array (GBGA) package in order to demonstrate the real commercial applications. This chapter starts with describing the GBGA package and then the measurement results for the I/O test ICs are shown to prove the performance and functionality. On-die measurements for CML I/O and GTL I/O had been performed with high impedance probes to report the maximum bandwidth of the test ICs. Finally, validation experiments for the GBGA package electrical model show the real commercial application of this research.

6.2 Generic Ball Grid Array (GBGA) Package

GBGA package is a wire bond BGA type package which allows for two-tier bonding to achieve higher pin counts. Figure 6-1 shows a cross section of GBGA package [6.1].

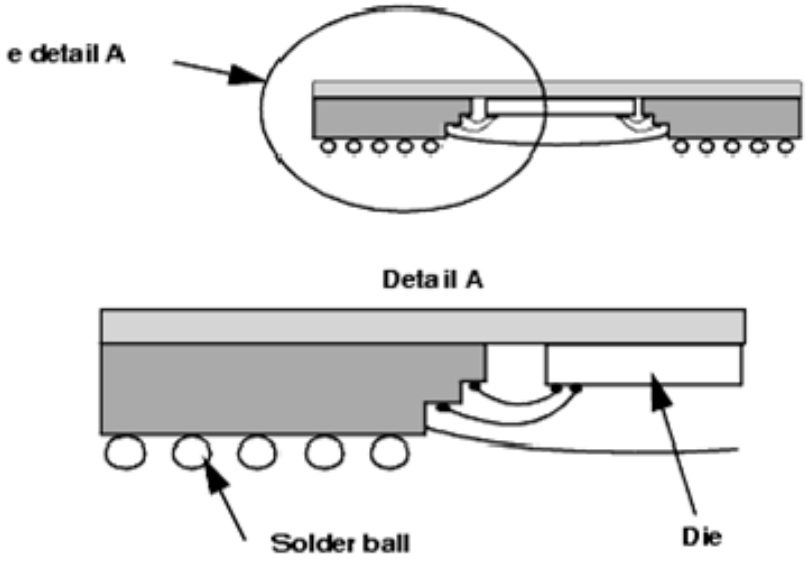


Figure 6-1. Cross section of GBGA package.

GBGA is die down package and has four metal layers to provide package design flexibility. As shown in Figure 6-2, there are two configurations that exist in BGA packages, which are die-up and die-down [6.2]. A die down BGA package has the advantage over the die-up part because it reduces the routing length allowing better signal integrity performance. Besides, a die-down BGA package typically has better thermal performance than the die-up BGA package since the heat that is generated in the die can be dissipated effectively from the backside of the die to the metal heat slug.

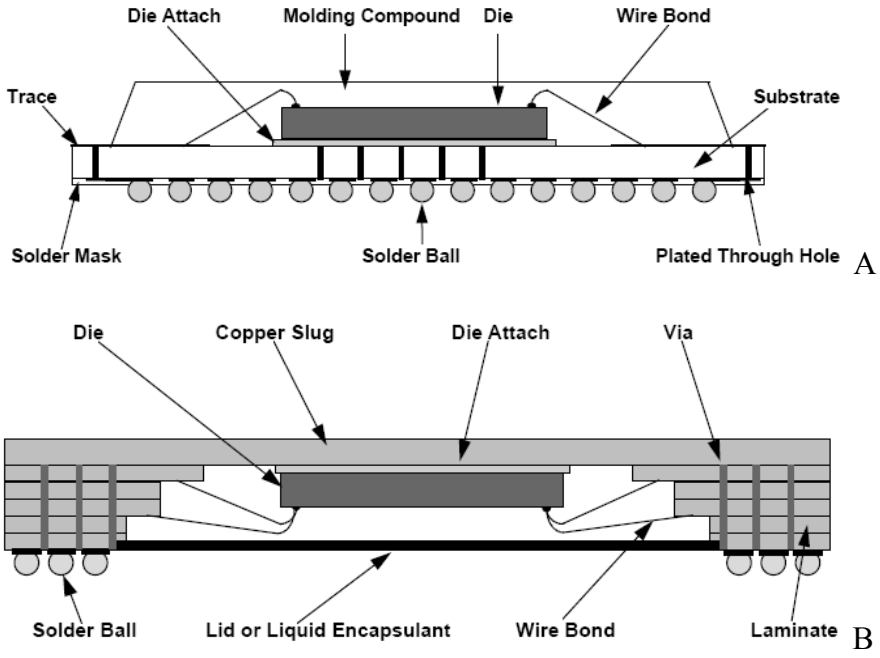


Figure 6-2. Die-up and die-down BGA package. A) Die-up BGA package. B) Die-down BGA package.

In GBGA package, the signal trace is directly connected to the solder ball without using the through-hole via, it has better high frequency performance. Figure 6-3 is the cross section of GBGA package. Bismaleimide triazine (BT) resin whose dielectric constant is 4.7 was used for substrate material and the die is attached to the package fingers with gold wire bonds. The top metal layer is for traces from ball connections to the central cavity with the IC chip. Second and fourth layers are the ground planes. Third layer is a power plane.

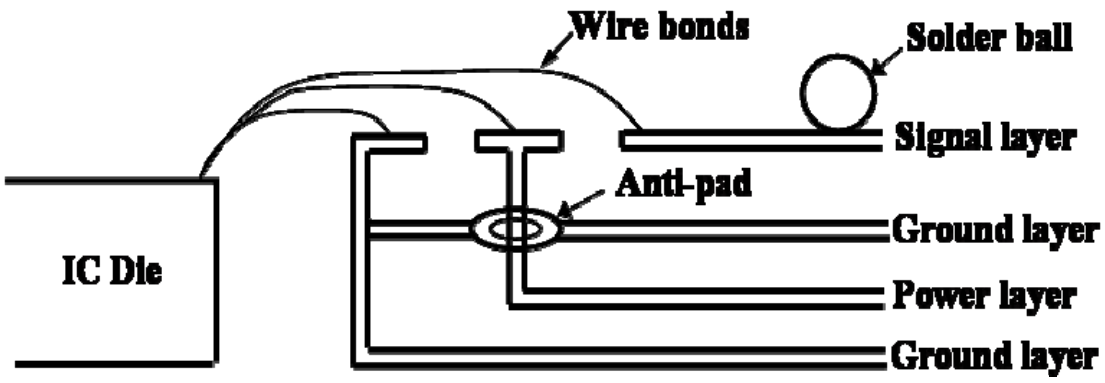


Figure 6-3. Cross section of GBGA package.

Figure 6-4 is the top views of the package stack up showing the traces, BGA solder balls (blue), and the central cavity with the IC die. Trace stubs at the end of the signal traces were made during the etching process and have high frequency effects because they change the trace characteristic impedance. Figure 6-5 is the isometric view showing package layers and Figure 6-6 is the close up of cavity area. Package power layers in layer 2, 4 are connected to the solder balls through the through-hole vias and Figure 6-7 is the close up of a corner showing via example connecting layers 1, 2, and 4.

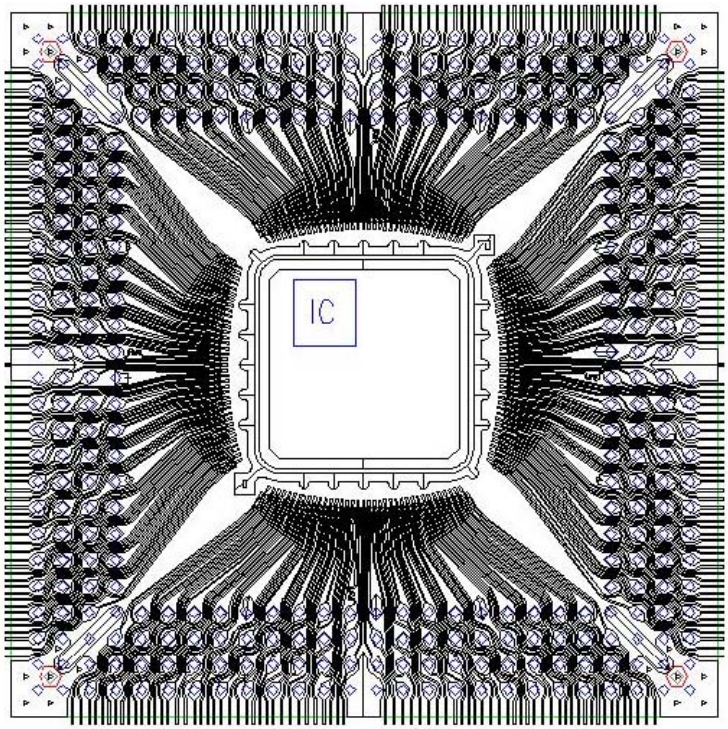


Figure 6-4. Top view of the package stack up.

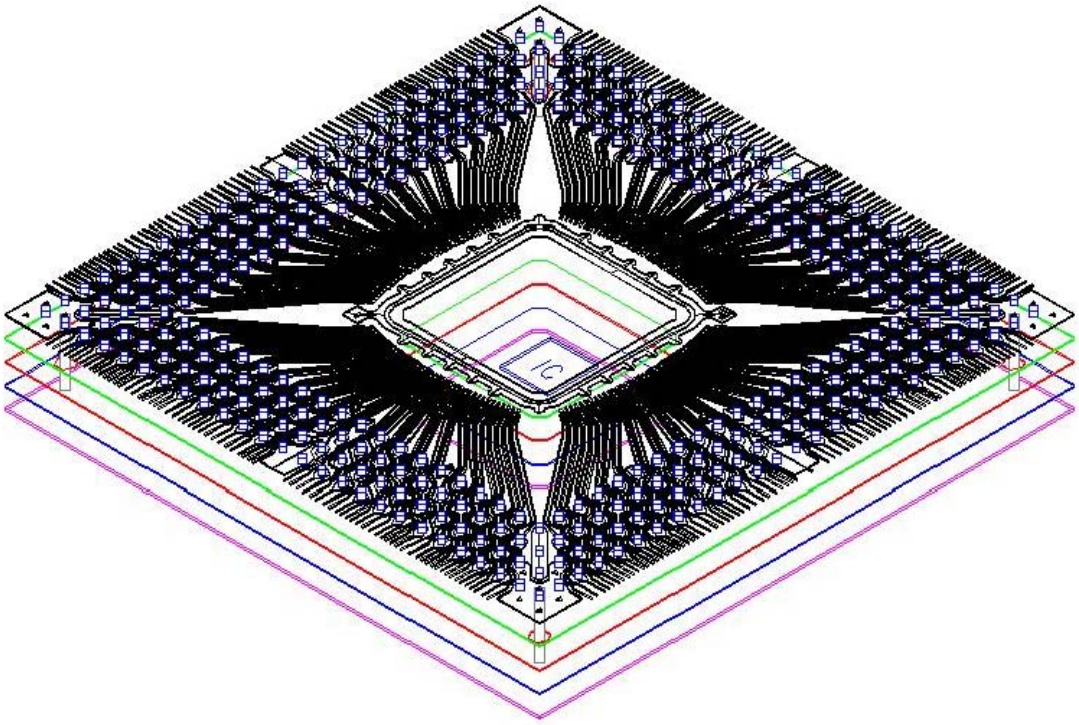


Figure 6-5. Isometric view showing package layers.

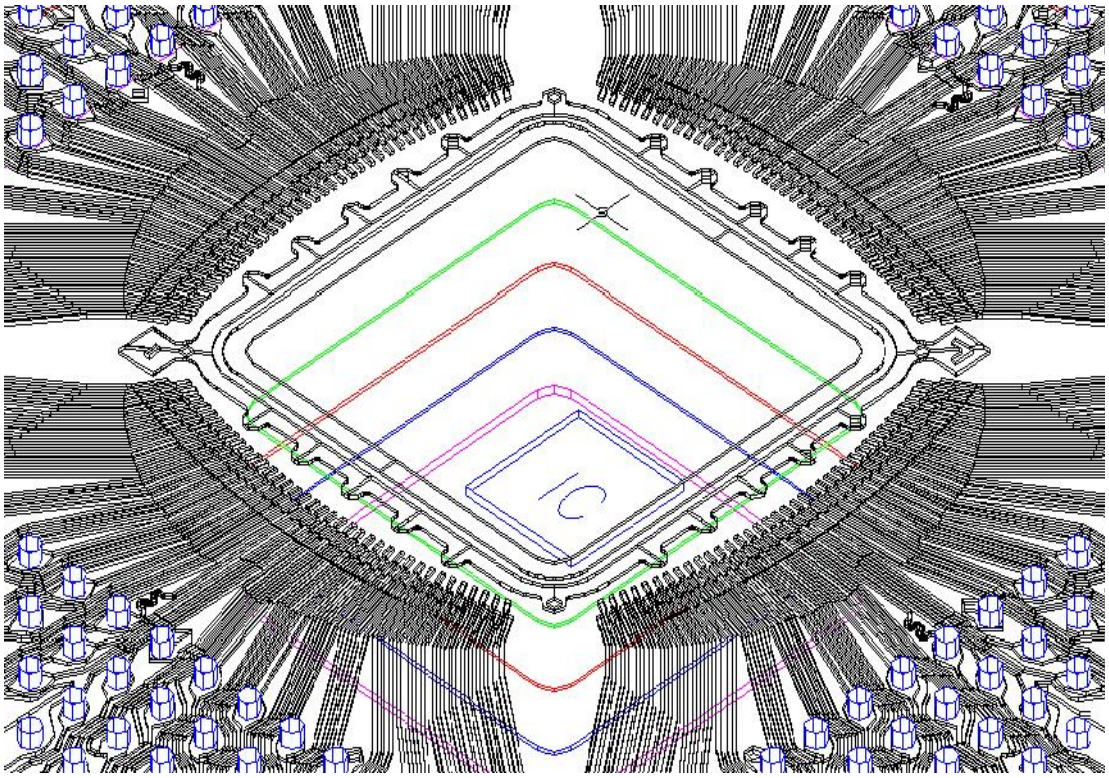


Figure 6-6. Close up of cavity area.

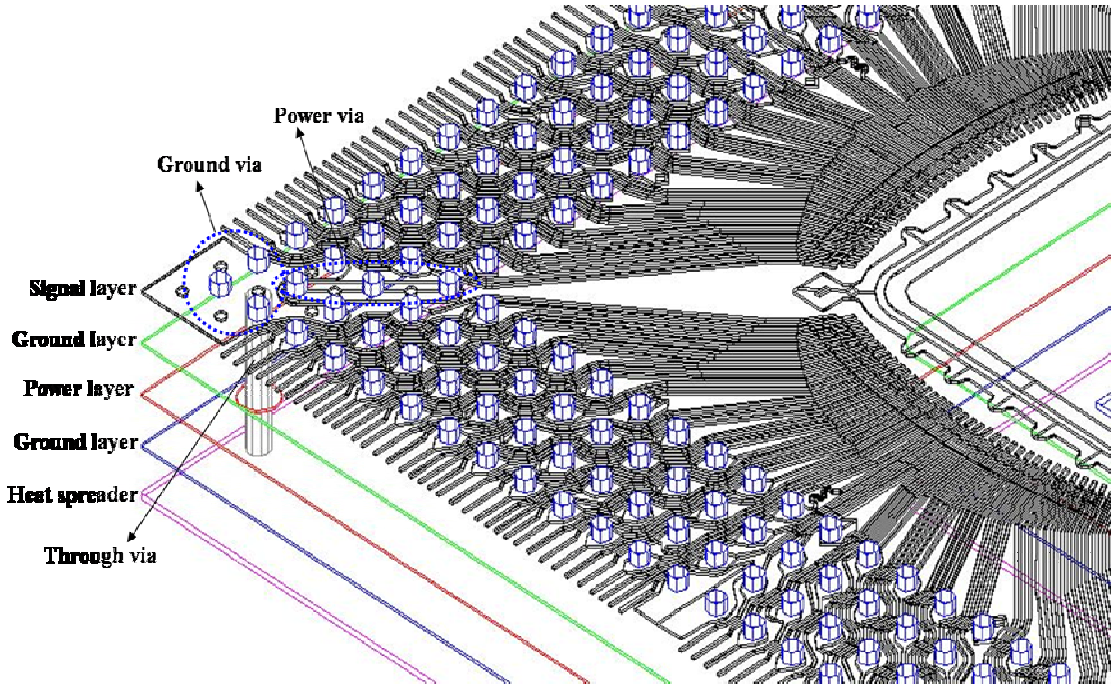


Figure 6-7. Close up of corner.

6.3 Measurement of Push-Pull I/O Test IC

The push-pull I/O test IC has been designed using IBM7WL 180nm technology with 1.8V power supply. Figure 6-8 shows the chip wire bonding and test board. The chip has been assembled with TI GBGA package having single-ended signal traces. Push-pull I/O drivers created test signals for the characterization of the package. Switching of these drivers generates ground bounce and power supply fluctuations. This chip also contained samplers [6.3] to measure these critical signals. These samplers not only help measuring signals but also help in debugging a packaged chip for functionality where the internal nodes are inaccessible for probing. Figure 6-9 shows the chip microphotograph.

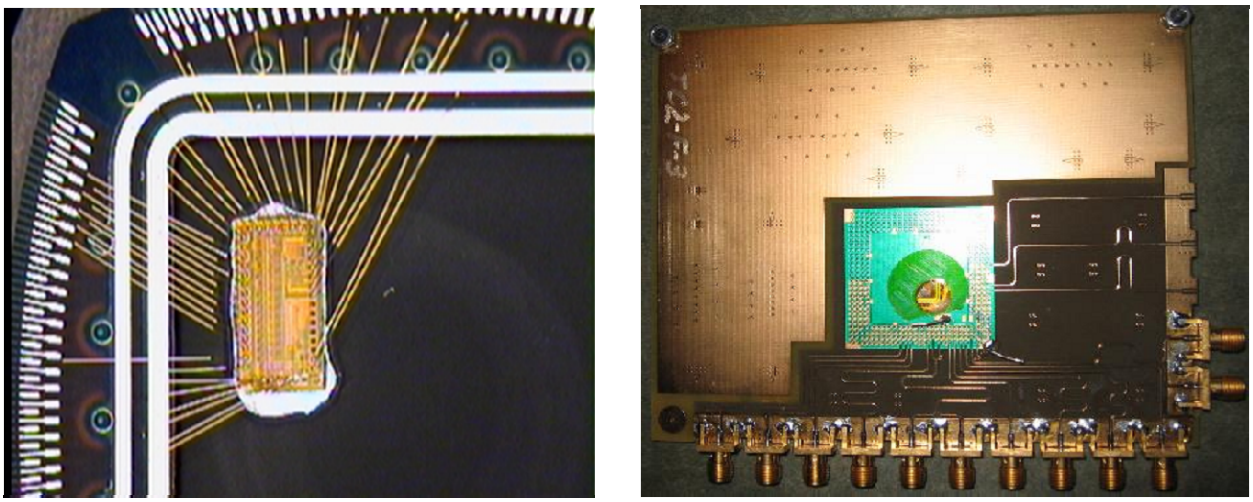


Figure 6-8. Wire bonding and board with the push-pull I/O test IC.

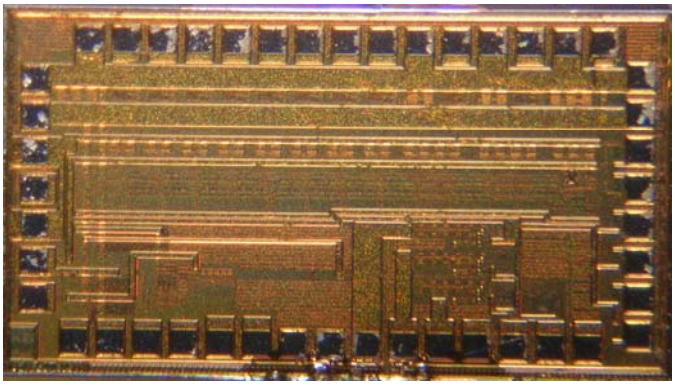


Figure 6-9. Chip microphotograph.

In order to verify the chip functionality, an on-die probe measurement was performed. Because the test chip has multiple I/O ports and there was no microwave probe which has multiple probe tips, a DC probe was used for measurement at very slow speed clock and data signals (10 MHz). Figure 6-10 shows the measurement setup and Figure 6-11 shows the switching of the I/O drivers.

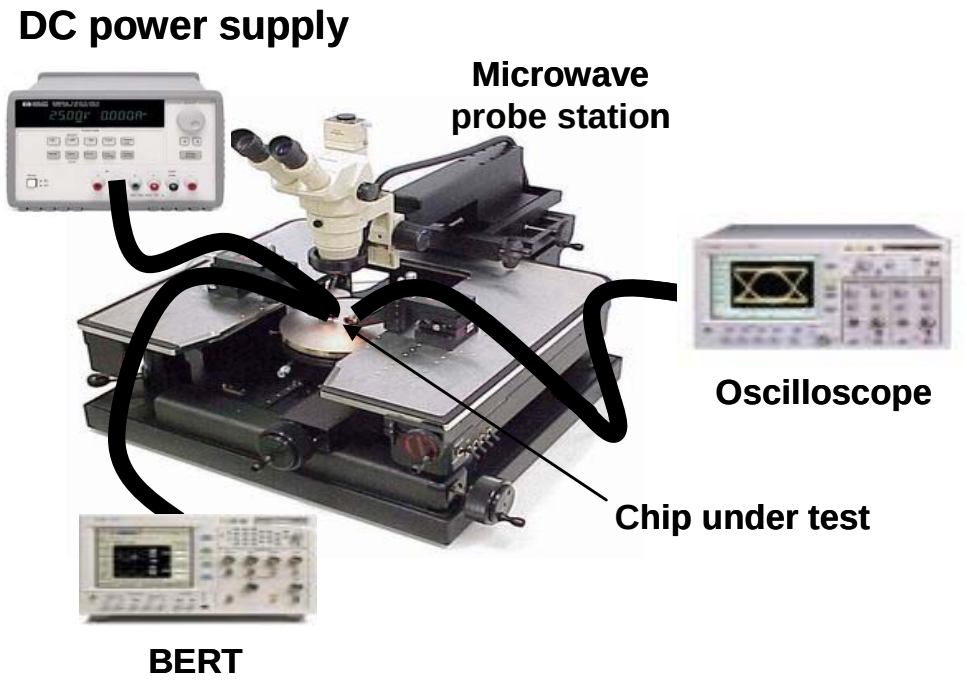


Figure 6-10. Measurement setup for push-pull I/O test IC.

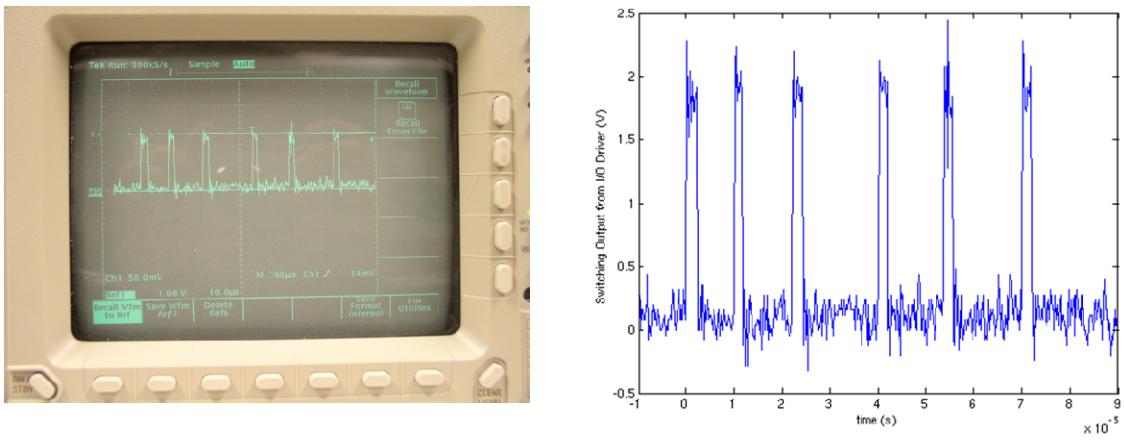


Figure 6-11. On-die measurement results for push-pull I/O test IC.

6.4 Measurement of CML I/O Test IC

The CML I/O test IC has been assembled with a TI GBGA package having differential inner traces and figure 6-12 shows the measurement setup. Tektronix DTG 5334 quad data generator launches the data and clock to make the I/O test IC fire the 4 parallel data channels and a 70GHz sampling oscilloscope captured the I/O signals and package ground/power noise.

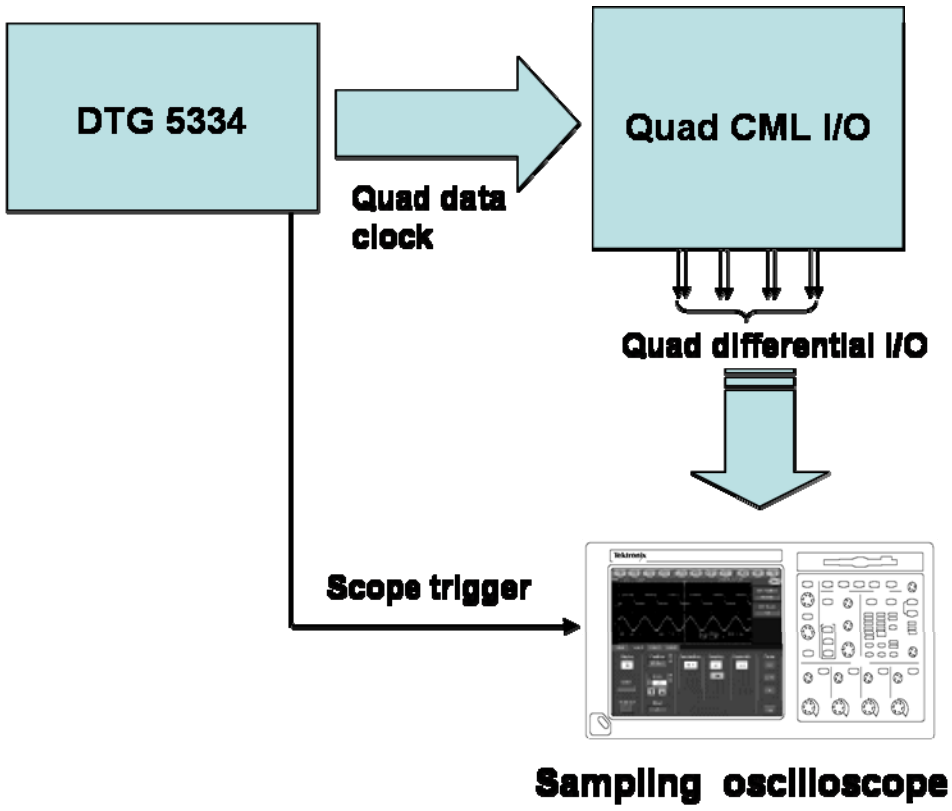


Figure 6-12. Measurement setup for CML I/O test IC.

Figure 6-13 shows chip microphotograph and test board. Figure 6-14 is the measurement results on a 50 Ω resistor on-board at the probe point. Jitter has been measured with different test equipment whose maximum data rate was 3.6Gb/s. Measured RMS jitter was 2% of the UI (Unit Interval of 3.6Gb/s = 278ps).

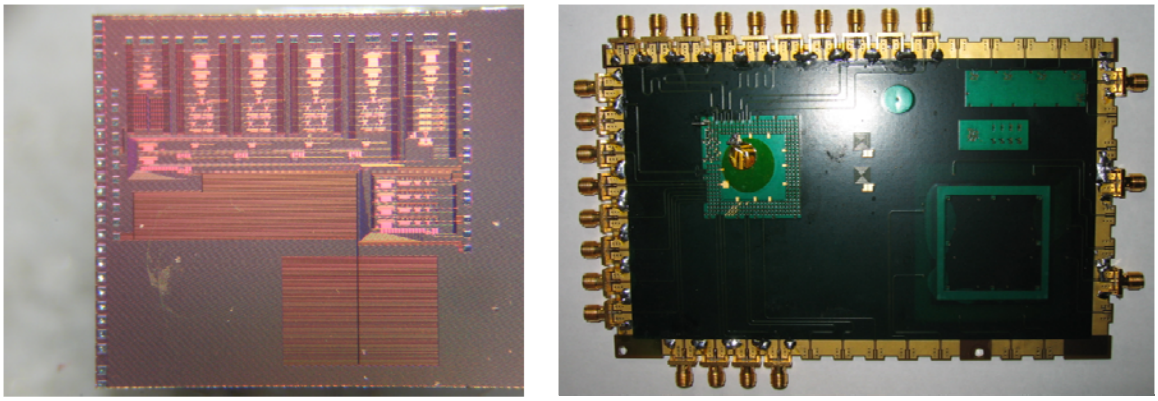


Figure 6-13. Chip microphotograph and test board.

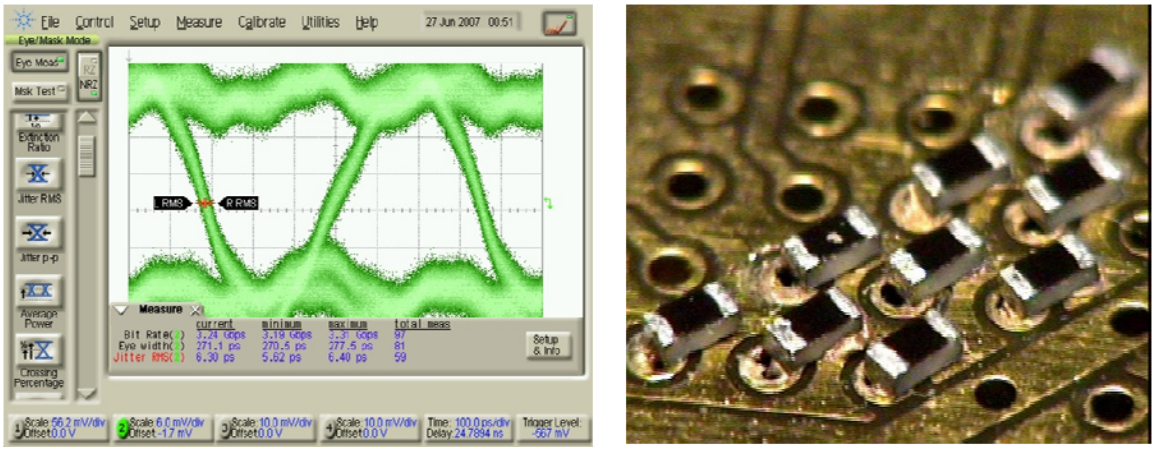


Figure 6-14. Measured eye diagram and 50 Ω on-board probe point.

Differential outputs from each I/O port were measured at the board and shown in Figure 6-15. All the measurements have been performed at a 1Gb/s data rate with a 12.5GHz active FET probe ($T_{r\_probe} = 28\,p\sec$) and a 70GHz sampling oscilloscope($T_{r\_scope} = 5\,p\sec$). On chip high impedance probing results at port 1 are shown in Figure 6-16. The rise time of the on-chip signal was 53.4psec and this is the composite rise time of the on-chip signal, probe and oscilloscope, which needs to be recalculated to get the true rise time of the on-chip signal. According to the Figure 6-17, the rise time of the on-chip signal is degraded due to the finite bandwidth of probe and oscilloscope and the composite rise time is given by

$$T_{r\_composite} = \sqrt{T_{r\_onchip}^{\ 2} + T_{r\_probe}^{\ 2} + T_{r\_scope}^{\ 2}}$$

Therefore, $T_{r\_onchip} = \sqrt{T_{r\_composite}^{2} - T_{r\_probe}^{2} - T_{r\_scope}^{2}}$ (6-1)

Now, the actual rise time of the on-chip signal is calculated by (6-1) and is 45psec which corresponds to a knee frequency of 7.8GHz. This is the maximum resolution of a CML I/O test IC and package elements below this frequency can be verified with the test IC. The fall time of the board level signal was 112.783pS, as shown in Figure 6-18.

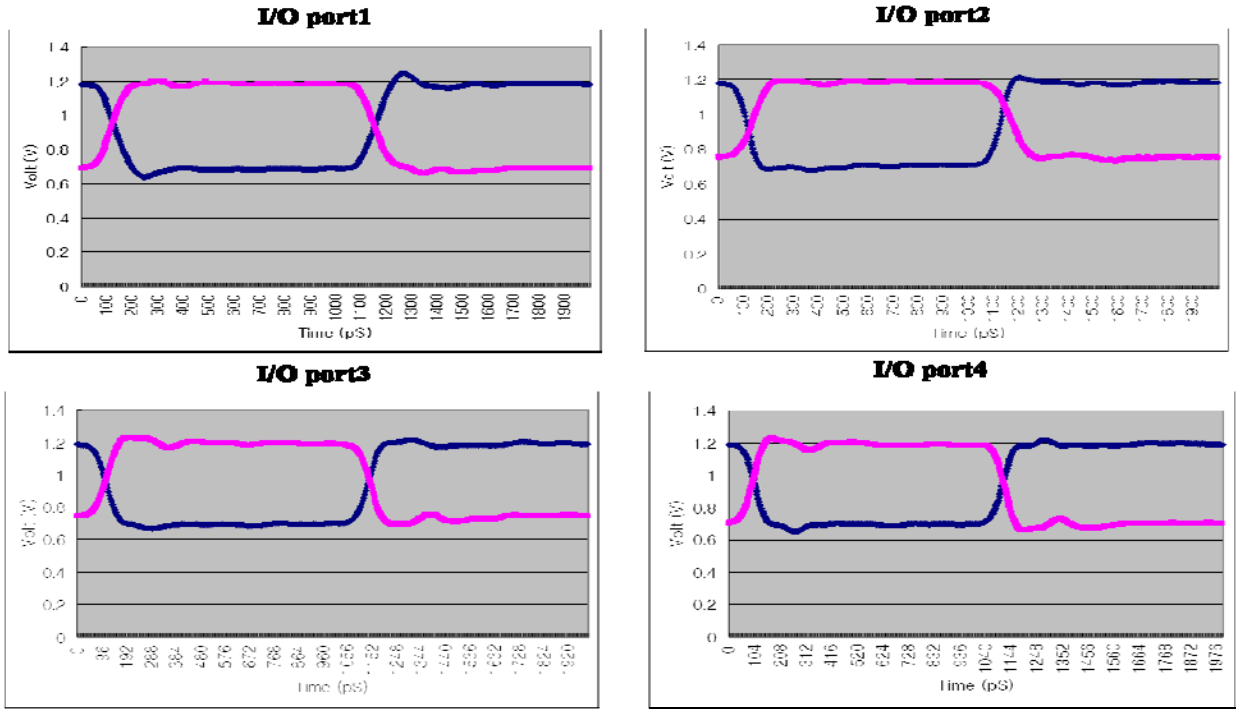


Figure 6-15. Differential signals from I/O ports measured at on-board probe points.

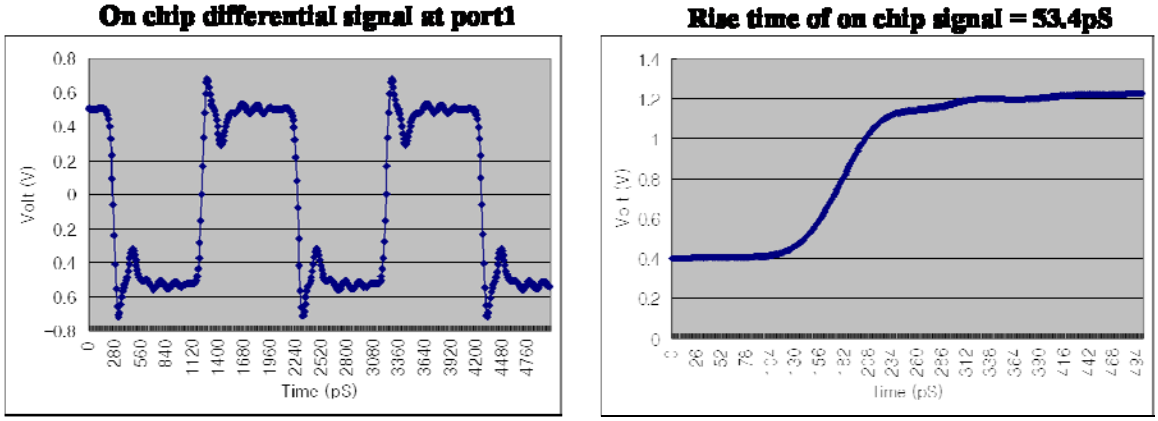


Figure 6-16. Port 1 differential signal and rise time measured at the on-chip bond pad.

After verifying the chip functionality, signal integrity effects of the I/O chip-package system have been measured and Figure 6-19 shows the measurement photo.

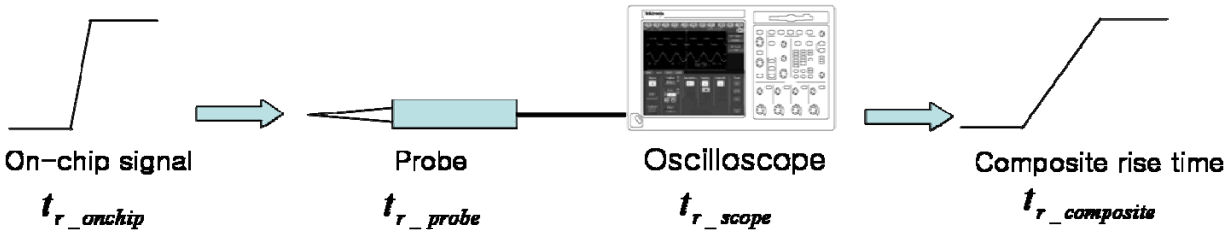


Figure 6-17. Rise time degradation due to the measurement equipments.

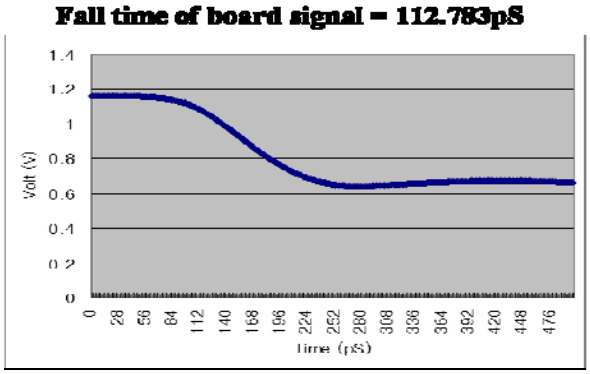


Figure 6-18. Fall time of the on-board signal.

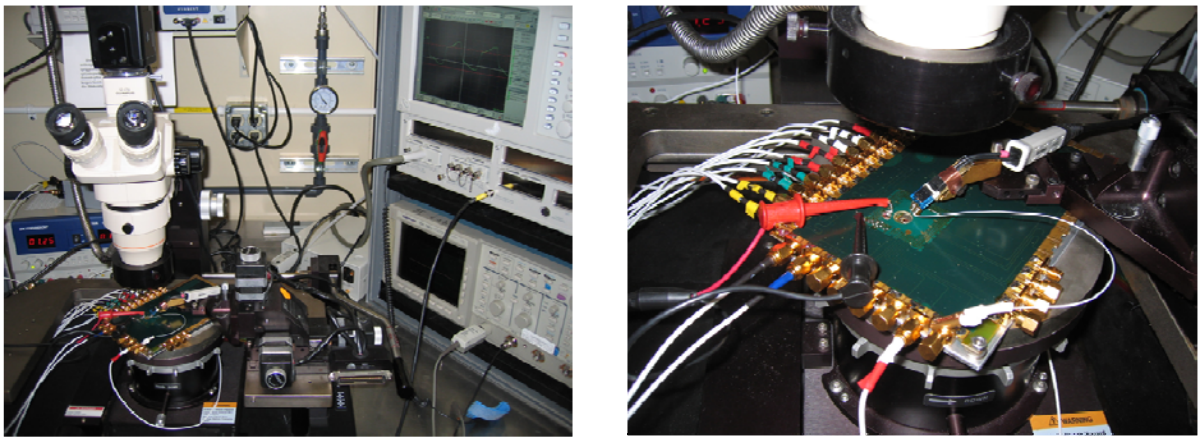
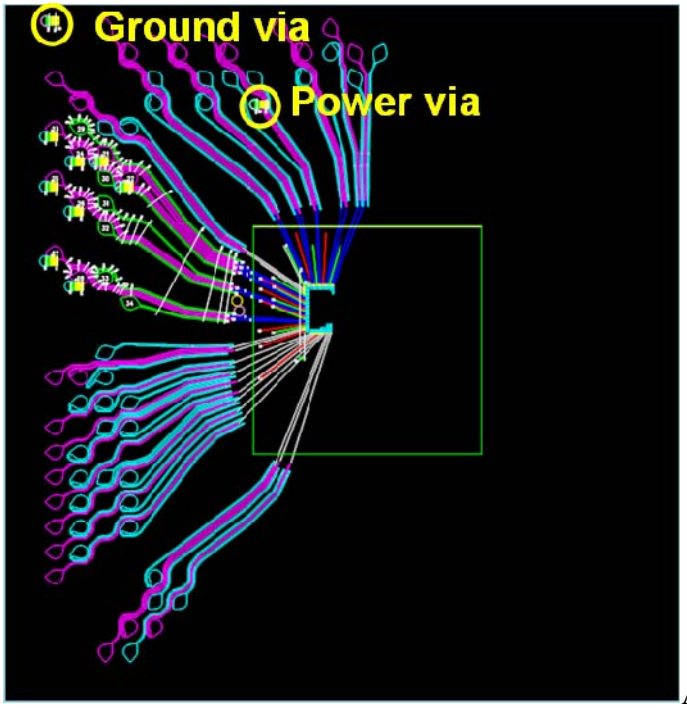


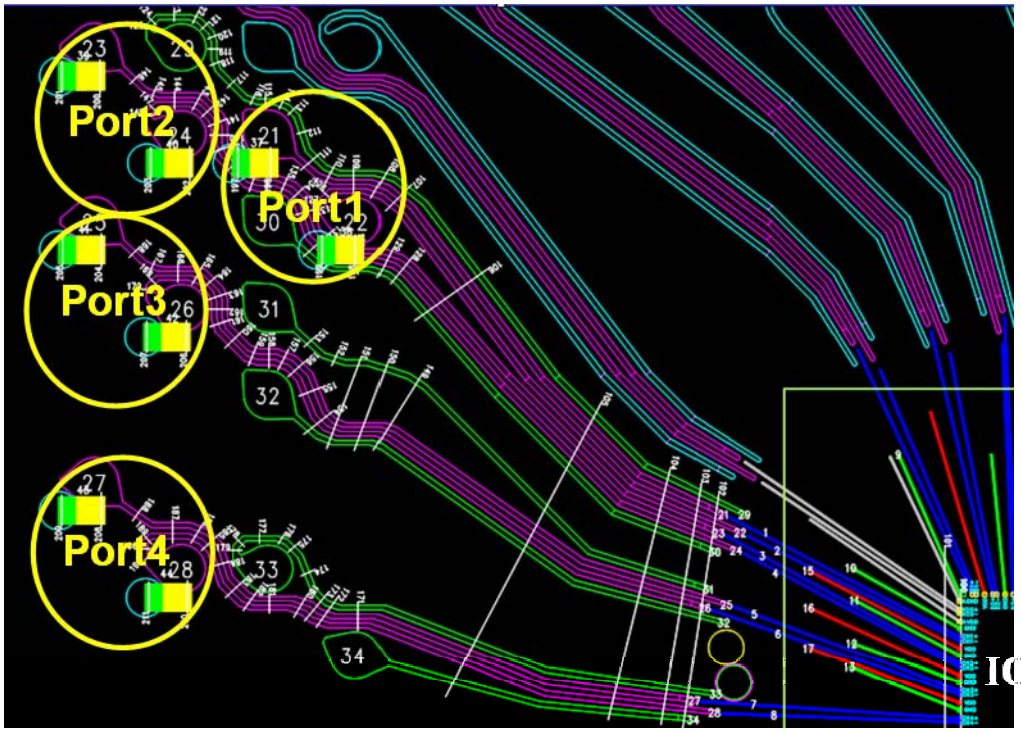
Figure 6-19. Measurement photo for CML I/O test IC.

Three kinds of signal integrity effects, which are package trace effect, crosstalk and simultaneous switching noise (SSN), have been measured to look at the response of I/O chip-package system. Figure 6-20 is the package CAD drawing showing the differential package

traces for each port. The package has been modeled with a 3-D modeling tool, where signal traces have been modeled with RLGC distributed circuits and meshed RLC distributed circuits have been used for package power and ground layer models. Power and ground layers are connected to the board power and ground layer through single through-hole via in order to look at the worst case switching noise. To look at the effects of differential traces, port 2 has been chosen because it has the longest trace. As shown in Figure 6-21(A), the on-chip signal from port2 showed distortion due to the bond wire inductance. This distortion was removed in the on-board signal, but the signal has experienced propagation delay, rise time degradation. Signal amplitude has been reduced only in the high frequency components which are contained around the signal edge. This attenuation is due to the high frequency loss effects such as skin effect and dielectric loss.

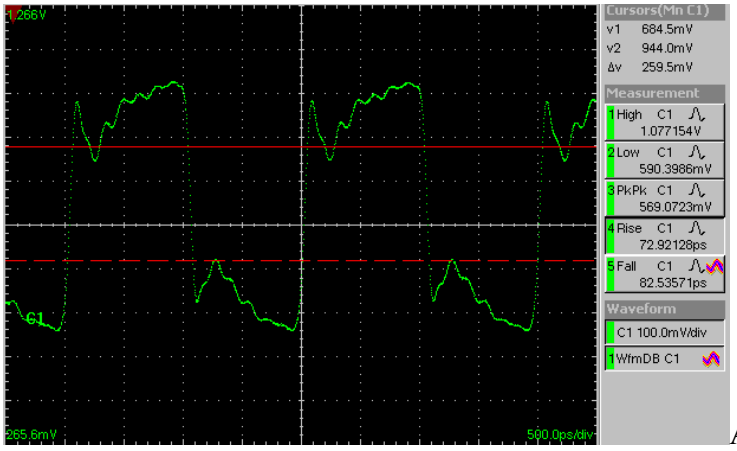


A

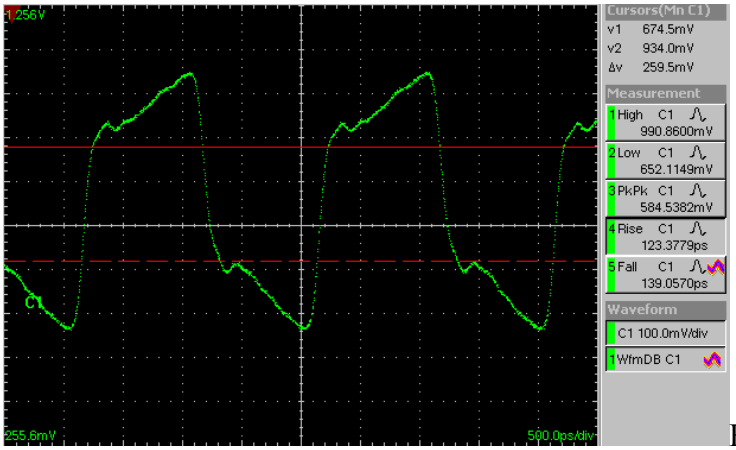


B

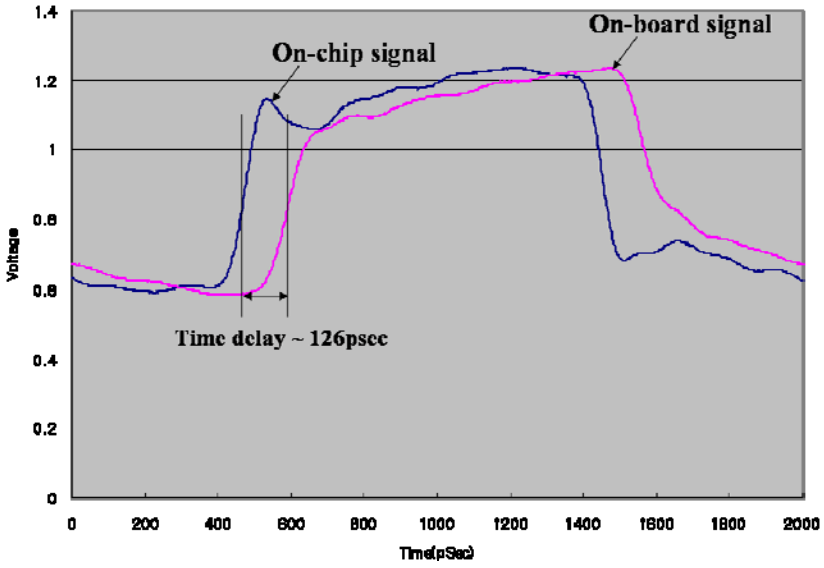
Figure 6-20. GBGA package having differential trace lines. A) Package CAD drawing. B) Zoomed picture showing differential traces.



A



B



C

Figure 6-21. Measured port 2 signals. A) On-chip signal. B) On-board signal. C) Overlapped plot.

In order to look at crosstalk effects, port 1- has been held to the V_{OL} while port 2 switches. Since port 1- is close to port 2+, on-chip and on-board signals at port 1- have been probed for NEXT and FEXT. Figure 6-22 (A) shows the measurement conditions for port1 and port2. As explained in Chapter 2, NEXT has a duration of 252pSec which corresponds to $2 \times T_D$ (T_D : propagation delay of bond wire and trace on BT resin) and FEXT has a peak at the middle of the NEXT pulse duration. The FEXT measurement result says that capacitive crosstalk is dominant between port1 and port2. Propagation delay of the BT resin is given by

$$T_D(126p\,\mathrm{sec}) = trace\ length\left(\approx \tfrac{2}{3}\,inch\right) \times \frac{\sqrt{\varepsilon_r\,(=4.7)}}{c\left(=3\times10^8\,m/\mathrm{sec}\right)}$$

For SSN investigation, all drivers have been set to switch simultaneously and package ground ring has shown to look at the worst case switching noise. Figure 6-23 (A) is the measurement result for ground fluctuations probed at a package ground layer which has peak-to-peak noise of 48.2mV. According to Figure 6-23 (B), the voltage amplitude of package ground noise depends on the input switching signals. When M1 or M2 is fully turned on, the CML buffer becomes a source follower and node V_P has maximum amplitude causing a larger tail current. This time varying current gives rise to the voltage fluctuations across the package parasitic inductor.

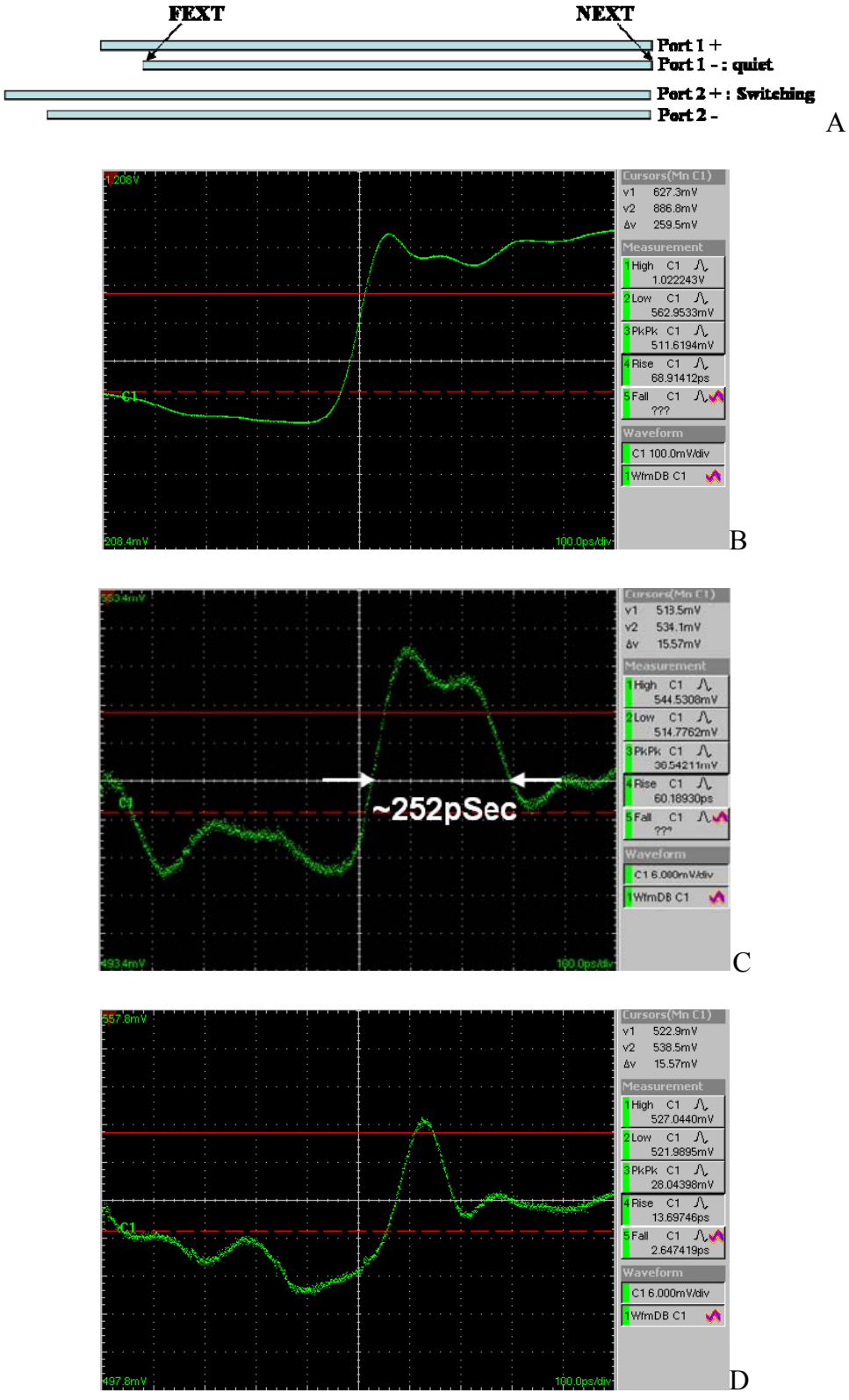
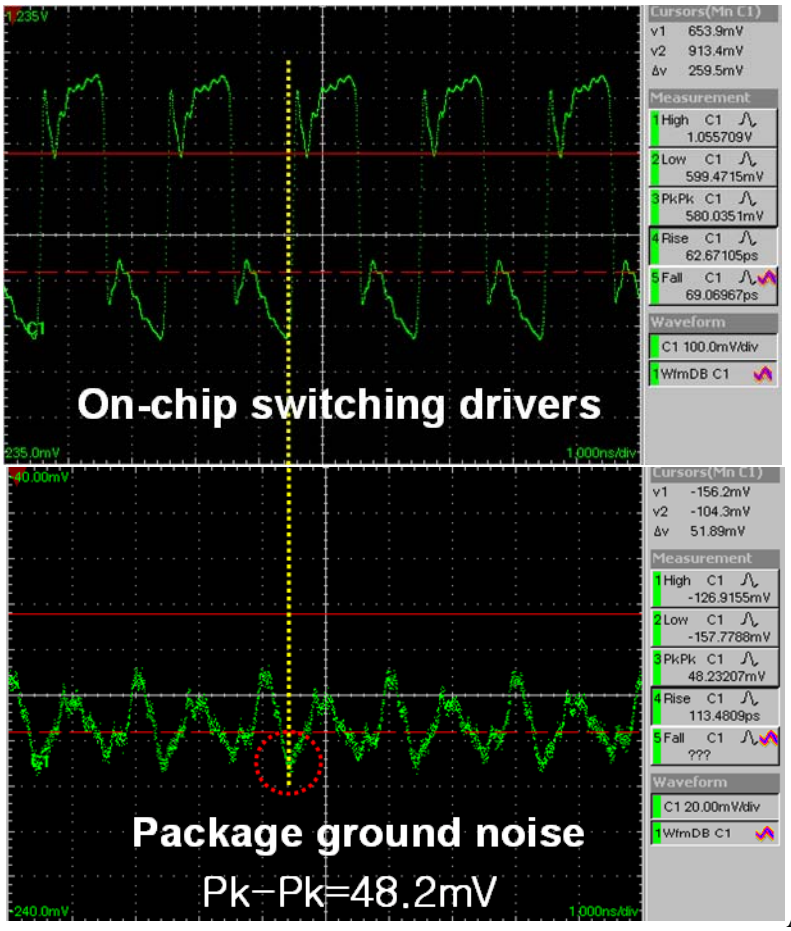
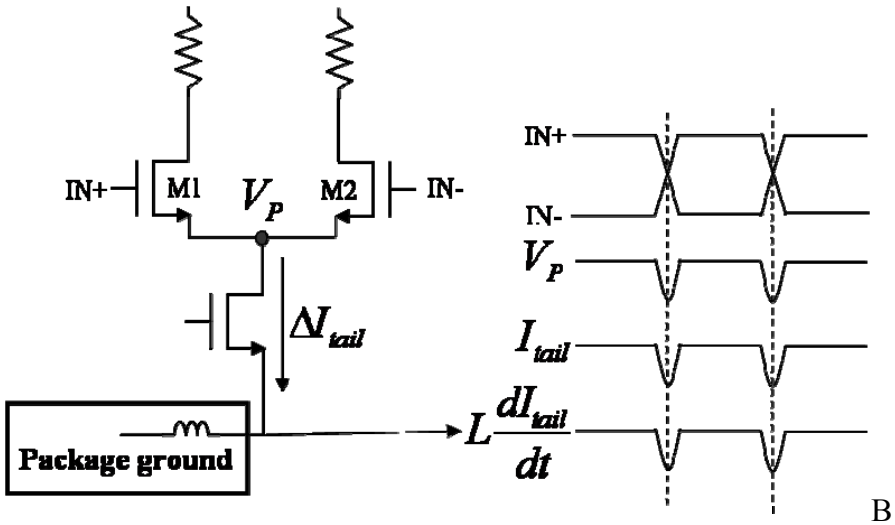


Figure 6-22. Crosstalk noise measurement results for CML I/O test IC. A) Measurement setup. B) Switching port2 +. C) NEXT. D) FEXT.



A



B

Figure 6-23. Package ground noise for CML I/O test IC. A) Measurement result for package ground noise. B) Ground noise mechanism of CML buffer.

Package SPICE model verification has been performed with above measurement results. On-chip signals including I/O pads and chip power/ground pads have been probed using 12GHz high impedance FET probes shown in Figure 6-25 and an IBIS macromodel for CML I/O test IC has been created and simulated in a SPICE circuit simulator in order to validate the package SPICE model.

For package trace model verification, on-board signal from port 2 was compared to SPICE simulation results. As shown in Figure 6-26, high frequency components in signal from SPICE simulation has larger peak amplitude compared to the measured signal. This is due to the inaccurate package SPICE models reflecting high frequency signal loss effect (inaccurate skin effect, dielectric loss, etc). FEXT measurement results were used for package crosstalk model verification. As shown in Figure 6-25, the maximum FEXT value from SPICE simulation is closely matched to the measurement result. Package ground layer model verification has been performed by getting all drivers to switch simultaneously. A package ground layer can be modeled with distributed mesh networks and package ground layer has different voltage waveforms at different nodes. In this research, a specific test point which is between port3 and port4 has been chosen for the package ground layer model verification. Figure 6-27 shows the test point for the package ground layer. Package ground noise has a negative peak when differential NMOS transistors in CML buffer are in the saturation region and this value has been used to verify the electrical model for the package ground layer. As shown in Figure 6-28, the peak value of the package ground noise from the SPICE simulation is closely matched to the measurement value. Although noise signal shapes are not exactly same as those from the measurement results, the peak amplitude is a much more important factor, especially in crosstalk and SSN.

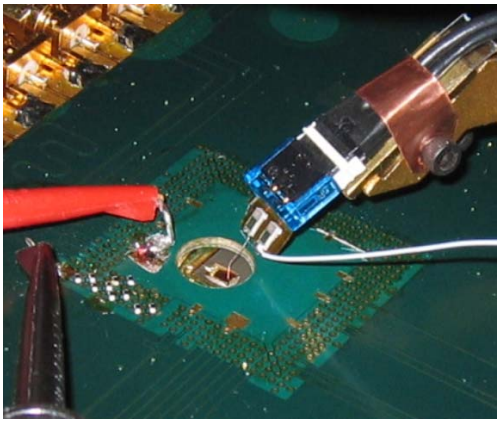
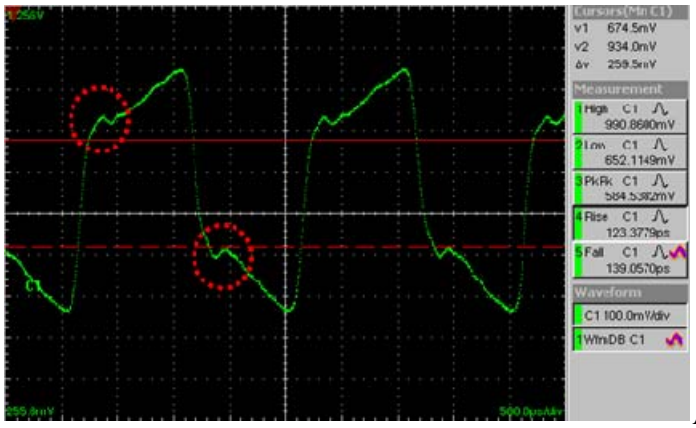
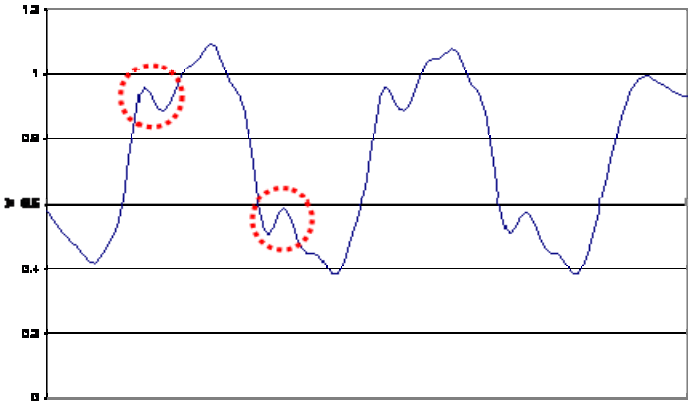


Figure 6-24. On-chip high impedance probing for CML I/O test IC.

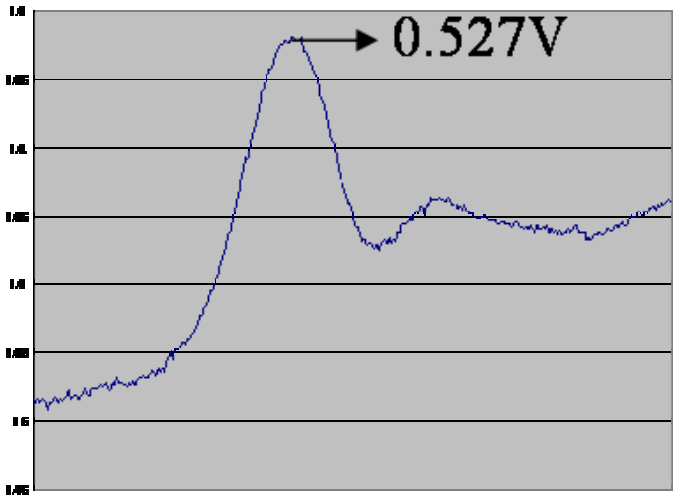


A

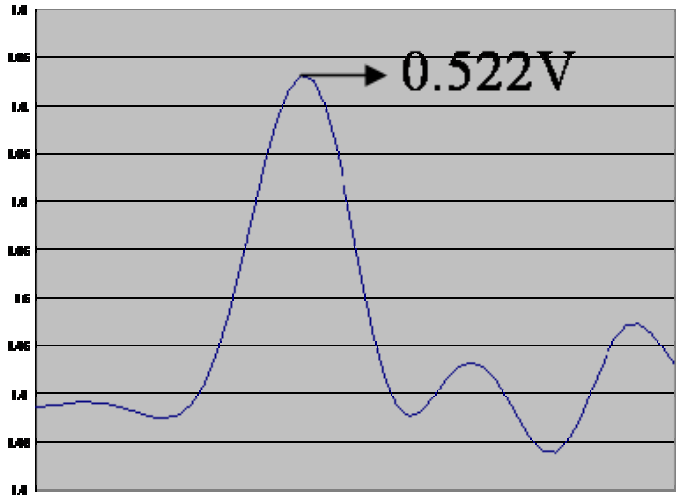


B

Figure 6-25. On-board signal comparison result for CML I/O test IC. A) Port 2 signal measured at on board. B) SPICE simulation result.



A



B

Figure 6-26. FEXT comparison result. A) Measured FEXT. B) SPICE simulation result.

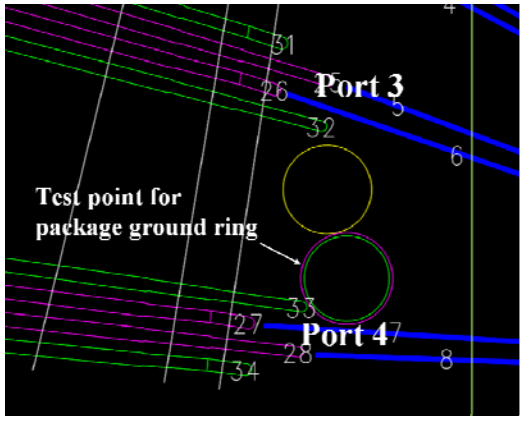


Figure 6-27. Test point for package ground layer.

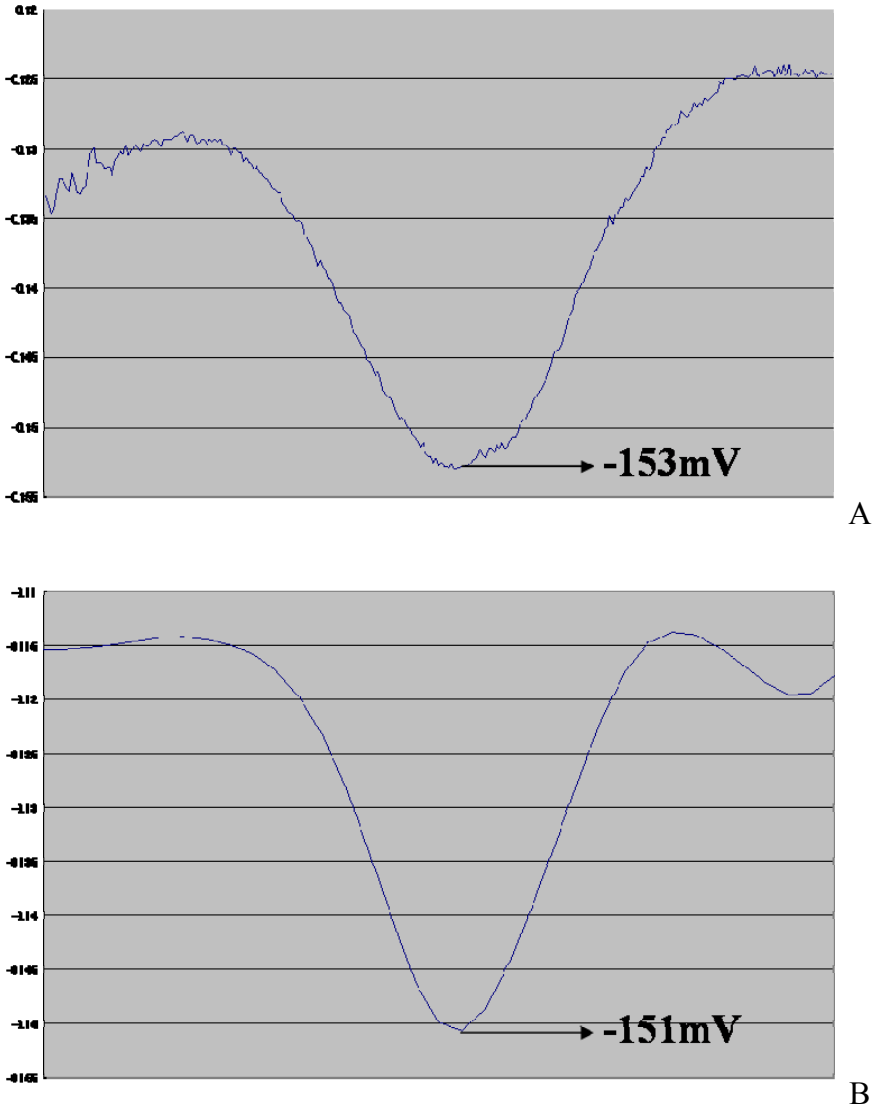


Figure 6-28. Package ground noise comparison result. A) Measured peak value. B) SPICE simulation result.

6.5 Measurement of GTL I/O Test IC

GTL I/O test IC has been assembled with a TI GBGA package having single-ended inner traces and figure 6-29 shows the measurement setup. The tektronix DTG 5334 stimulus system launches the data and clock and control signals to make the I/O test IC fire the 10 parallel data ports and the 70GHz sampling oscilloscope captures the I/O signals and the package ground /power noise.

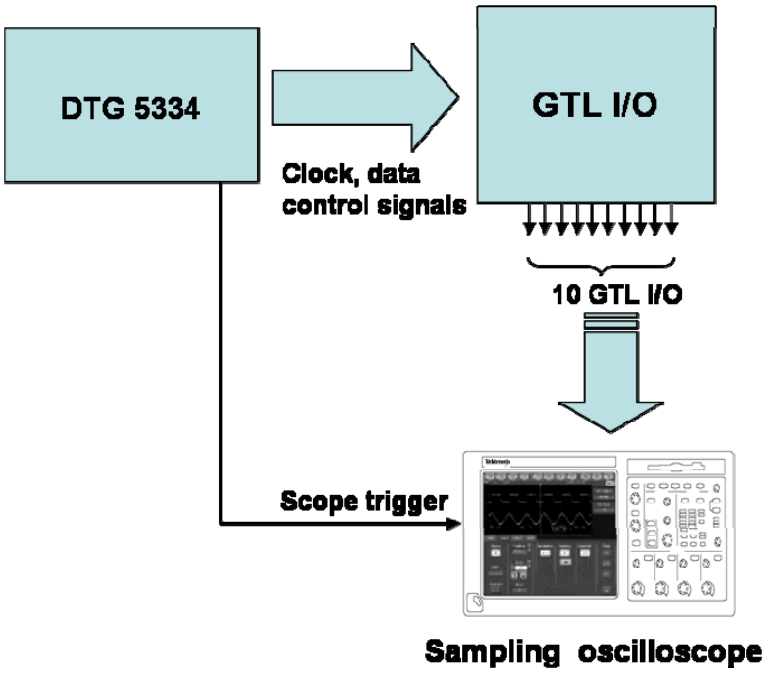


Figure 6-29. Measurement setup for GTL I/O test IC.

Figure 6-30 shows the test board and measurement setup. All the measurements have been performed at 100Mb/s instead of at 1Gb/s. This was because the clock signal was seriously degraded due to the PCB board traces. For the CML I/O test IC, the on-chip 50Ω and the CML clock buffer could have recovered clock signal distortion. But, in this research, the on-chip signal edge rate is much more important and the low frequency measurement is ok to investigate the signal integrity effects if the on-chip driver fires a fast edge rate signal to the package. High impedance probing has been performed to look at the chip functionality. Figure 6-31 shows the signals measured on-chip and on-board respectively. The rise time of the on-chip signal was 83psec and this is the composite rise time of the on-chip signal, probe and oscilloscope, which needs to be recalculated to get the actual rise time of on-chip signal. The actual rise time of on-chip signal was calculated using (6-1) and is 78psec which corresponds to a knee frequency of 4.5GHz. This is the maximum resolution of GTL I/O test IC and package elements below this frequency can be verified with this test IC.

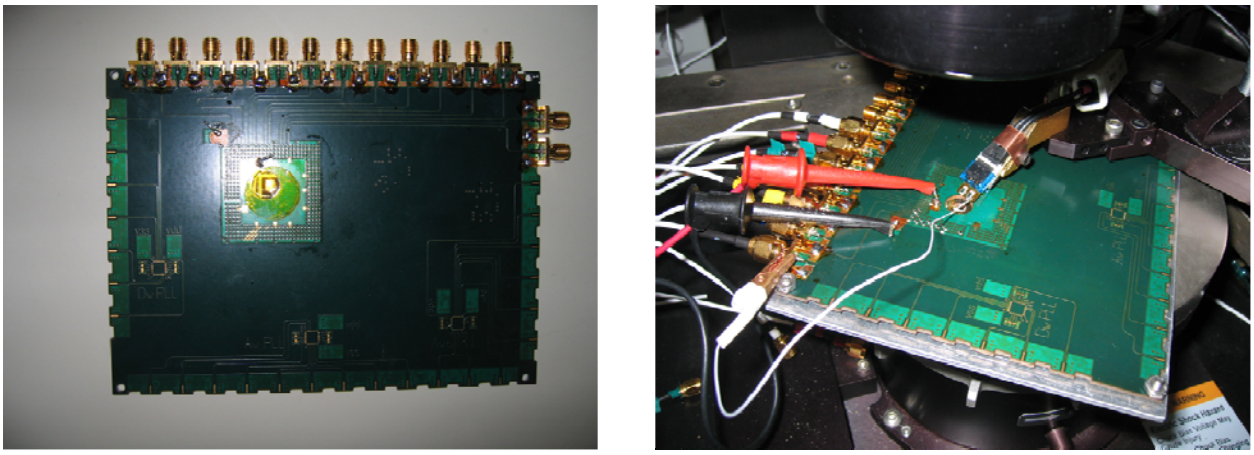


Figure 6-30. Test board and measurement setup for GTL I/O test IC.

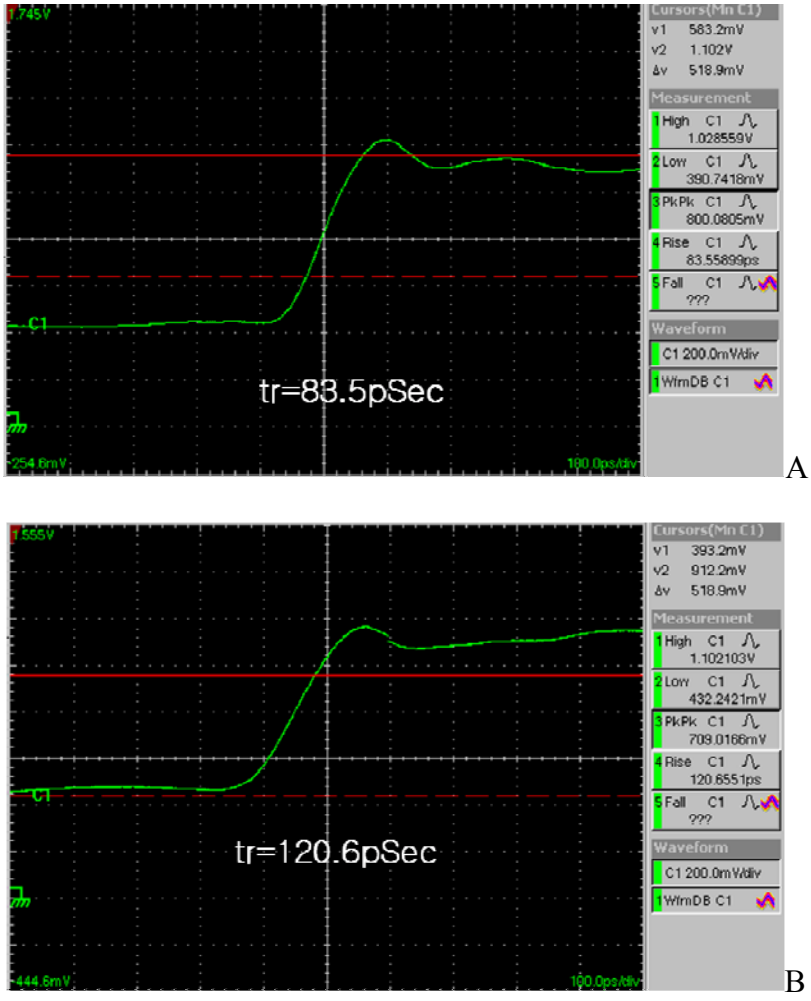


Figure 6-31. Measured on-chip and on-board signal. A) Rise time of on-chip signal. B) Rise time of on-board signal.

The programmability of the on-chip serial-to-parallel converter has been measured by programming an 8 bit data at port 10 and Figure 6-32 shows the measurement results of 4 different data patterns.

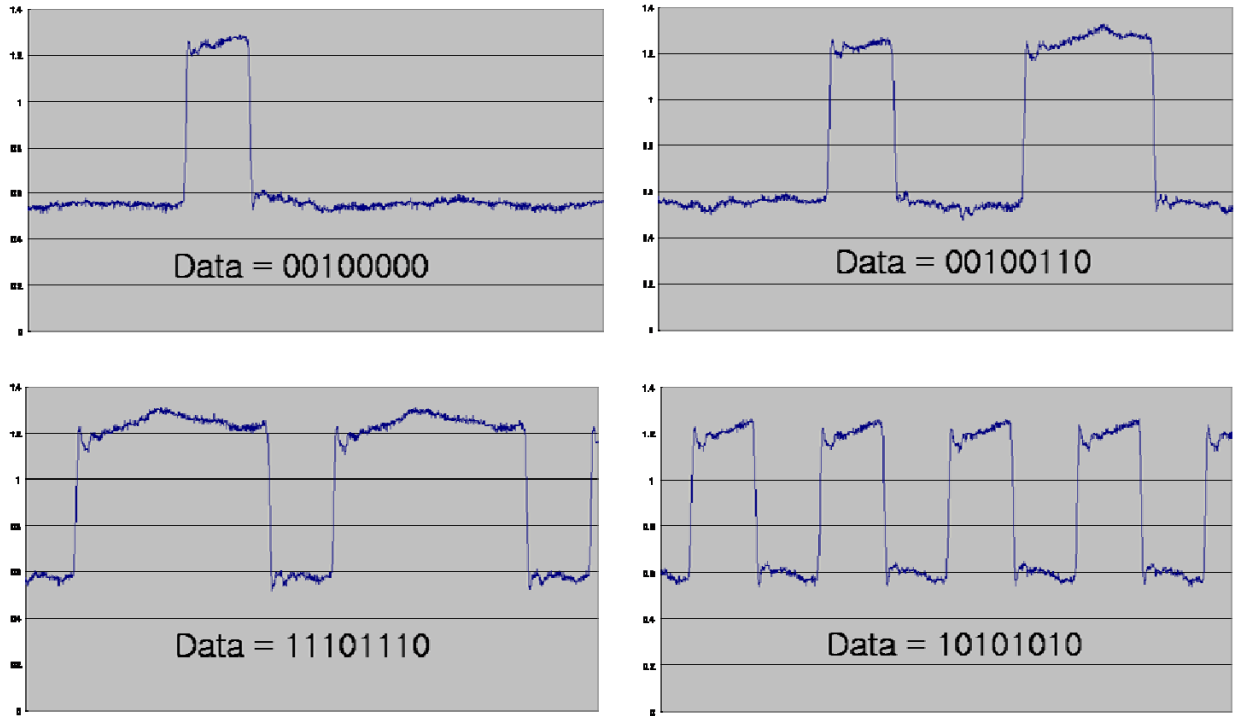
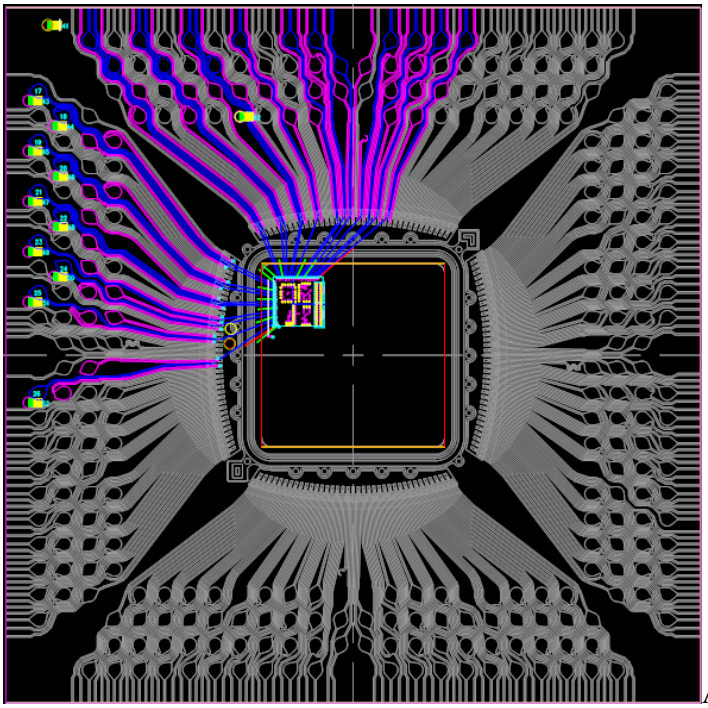


Figure 6-32. Measurement results for programmability of serial-to-parallel converter.

Package signal integrity has been measured with a GBGA package having a single-ended trace and Figure 6-33 is the CAD drawing which shows the package inner trace for 10 I/O drivers.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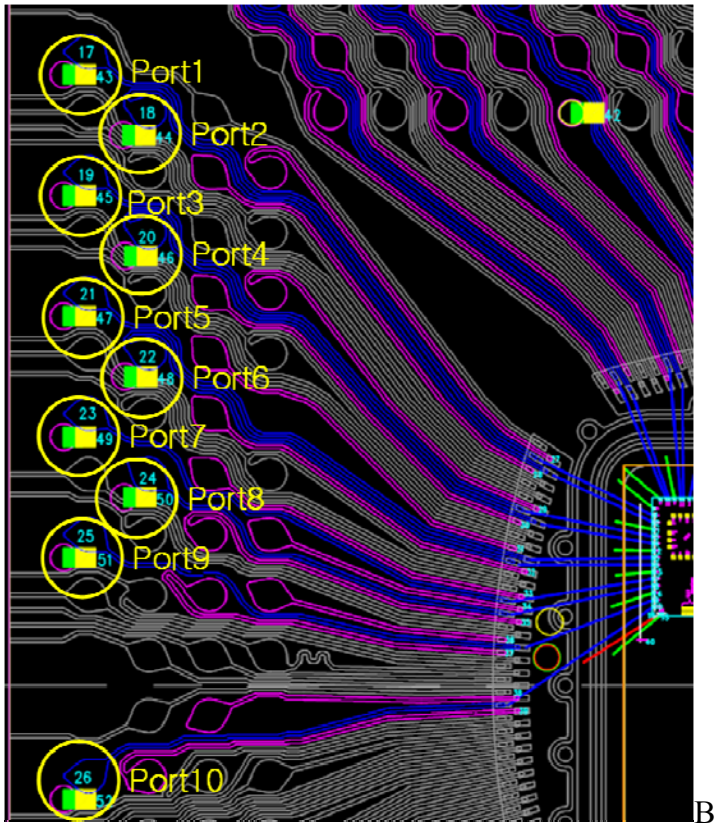
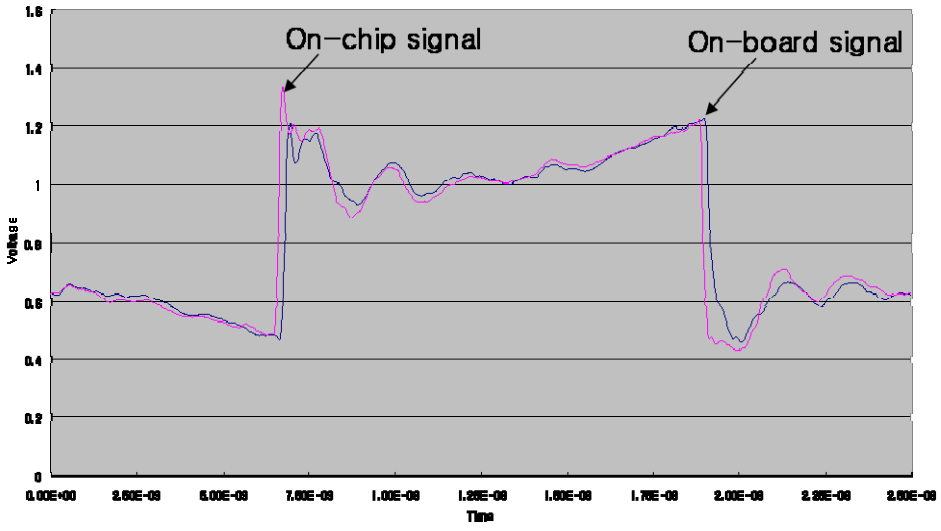


B

Figure 6-33. GBGA package having single-ended trace lines. A) Package cad drawing. B) Zoomed picture showing signal traces.

In order to look at the effects of package traces on the signal, port1 has been probed because of its longest trace line. As shown in Figure 6-34, on-board signal has experienced propagation delay, rise time degradation. Signal amplitude has been reduced only at the high frequency components which are contained around the signal edge due to the high frequency loss effects such as skin effect and dielectric loss.



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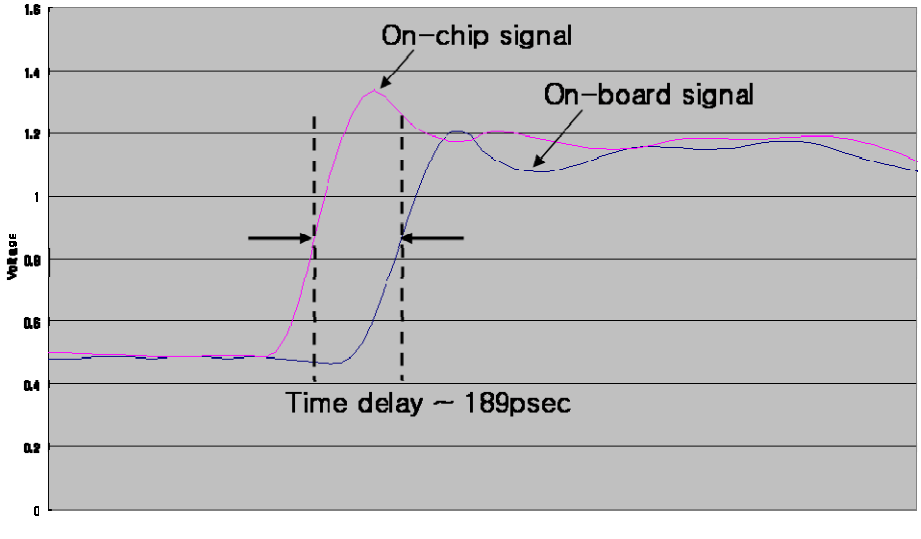
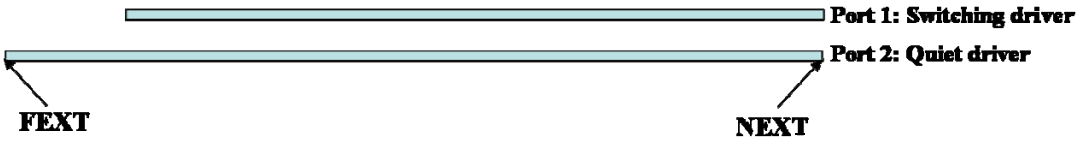


B

Figure 6-34. The effect of package trace on signal waveform. A) On-chip and on-board signal of port 1. B) Zoomed picture.

For crosstalk noise measurements, port2 has been kept quiet while port1 switches and near end and far end crosstalk noise have been captured at on-chip and on-board at port2. Figure 6-35 shows the NEXT and FEXT measurement results at port2. NEXT has a duration of 378pSec which corresponds to the $2 \times T_D$ (T_D : propagation delay of bond wire and trace in BT resin) and FEXT has shown pulse from a T_D after NEXT. FEXT measurement result indicates that the capacitive crosstalk is dominant between port1 and port2. Propagation delay for the single-ended trace line is given by $T_D(126p\sec) = trace\ length\left(\approx 2/3\ inch\right) \times \frac{\sqrt{\varepsilon_r (=4.7)}}{c\left(=3\times10^8\, m/\sec\right)}$

As the number of switching drivers is increased, the package power and ground layer experience power and ground rail fluctuations causing the signal waveform to be seriously distorted. In order to look at this effect, the on-board signal of port 10 has been probed with different numbers of switching drivers. As shown in Figure 6-36, the on-board signal of port 10 is getting distorted as the number of switching drivers is increased.



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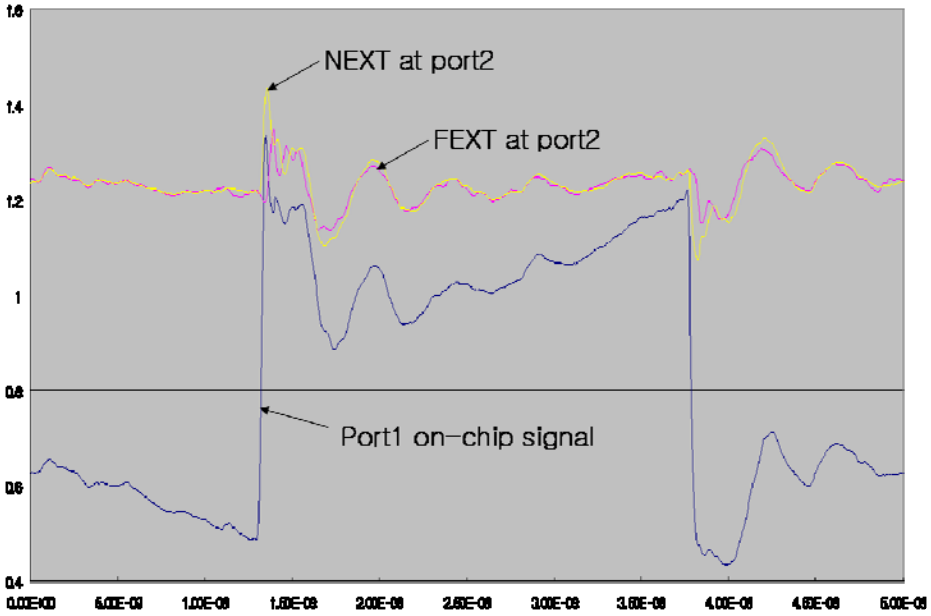

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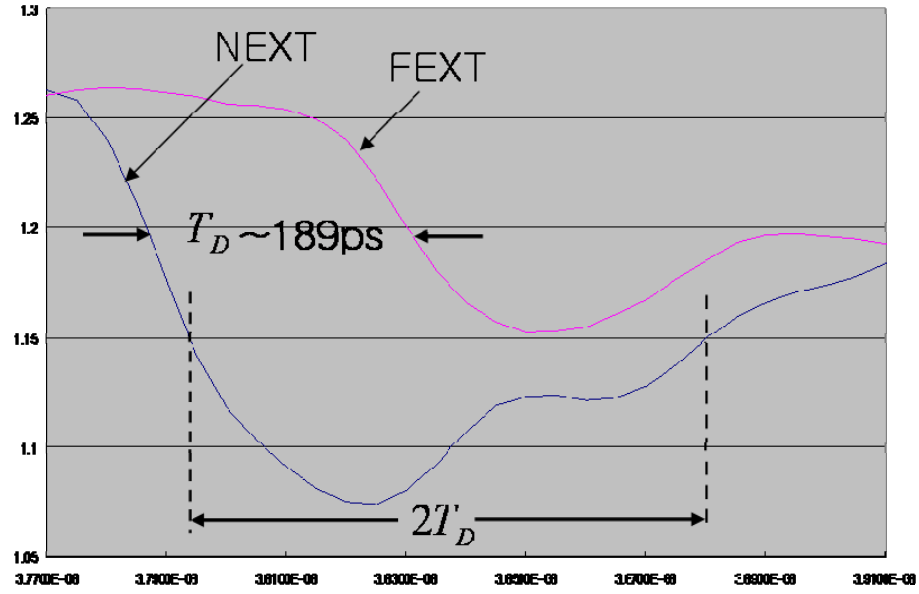


C

Figure 6-35. Crosstalk noise measurement results for GTL I/O test IC. A) Measurement setup. B) NEXT and FEXT measured at port2. C) Zoomed picture.

Figure 6-37 shows the package ground noise when all drivers switch simultaneously. The peak-to-peak value of the ground noise is as large as 655mV and the noise can generate huge amount of jitter in the on-chip clock network. In contrast, the CML I/O test IC generated package ground noise of less than 0.2V, which is why differential drivers are commonly used for high-speed I/O. The reason why package power and ground noise is huge is because the GBGA package was designed such that it has only single through-hole via for the ground and power layer in order to generate worst case switching noise. As shown in Figure 6-38, all the switching currents flow through the single via to go out to the board ground and power. Therefore, more vias need to be added to the package power and ground layer in order to reduce the noise level.

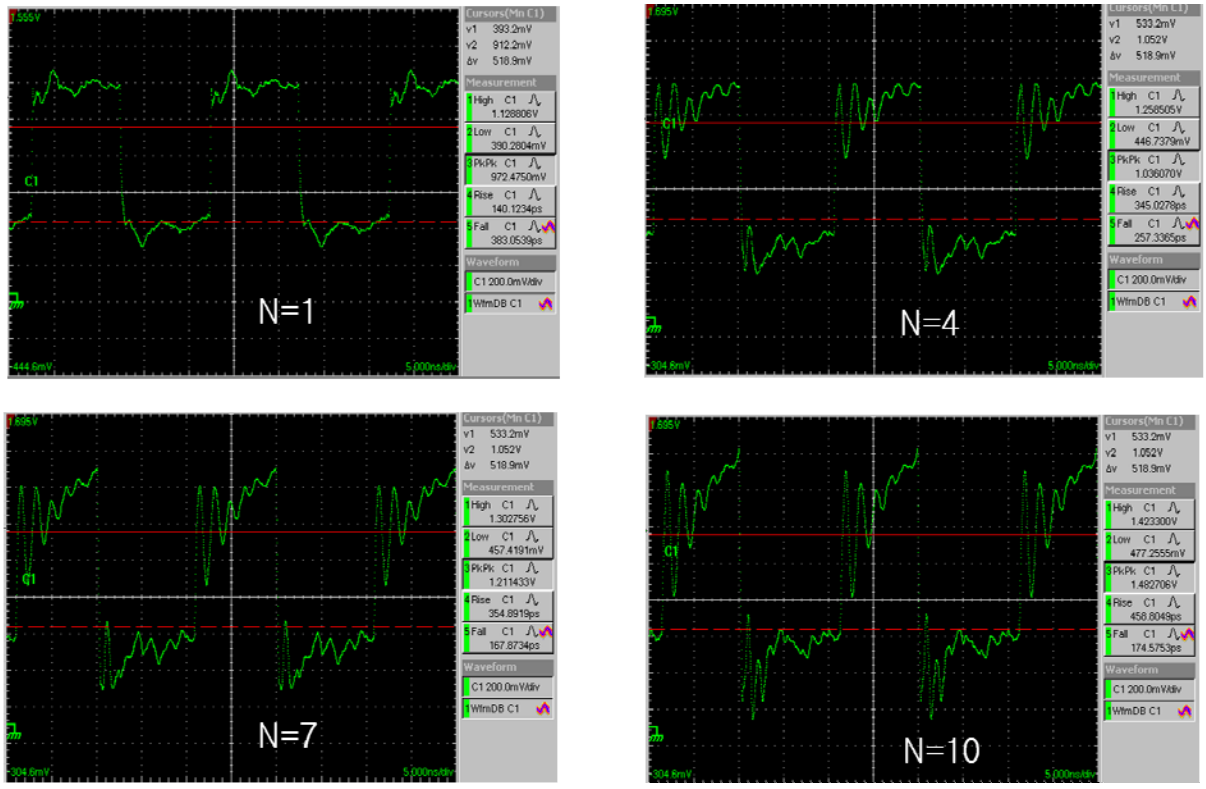
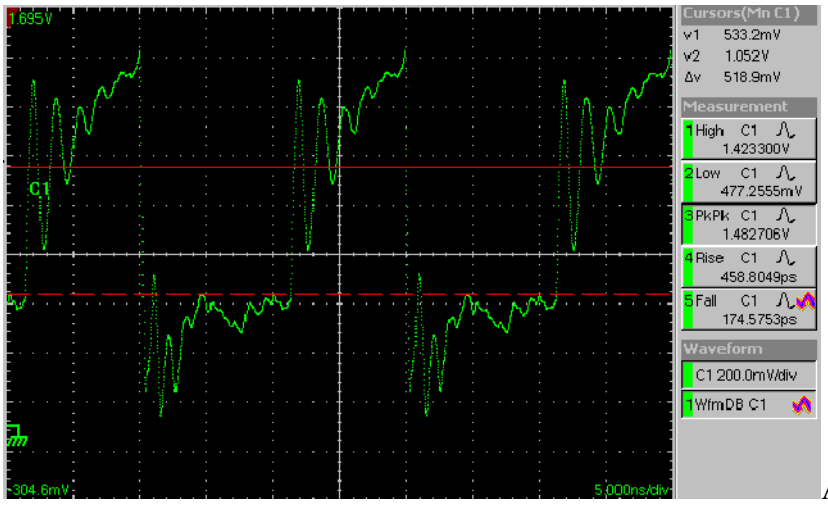
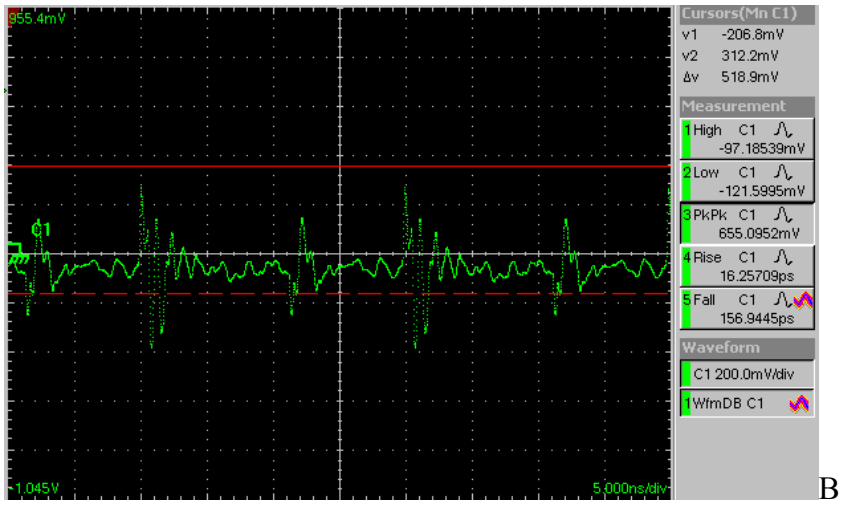


Figure 6-36. On-board signal of port10 (N = number of switching drivers).



A



B

Figure 6-37. The effect of SSN on signal waveform. A) Switching driver. B) SSN measured at package ground layer.

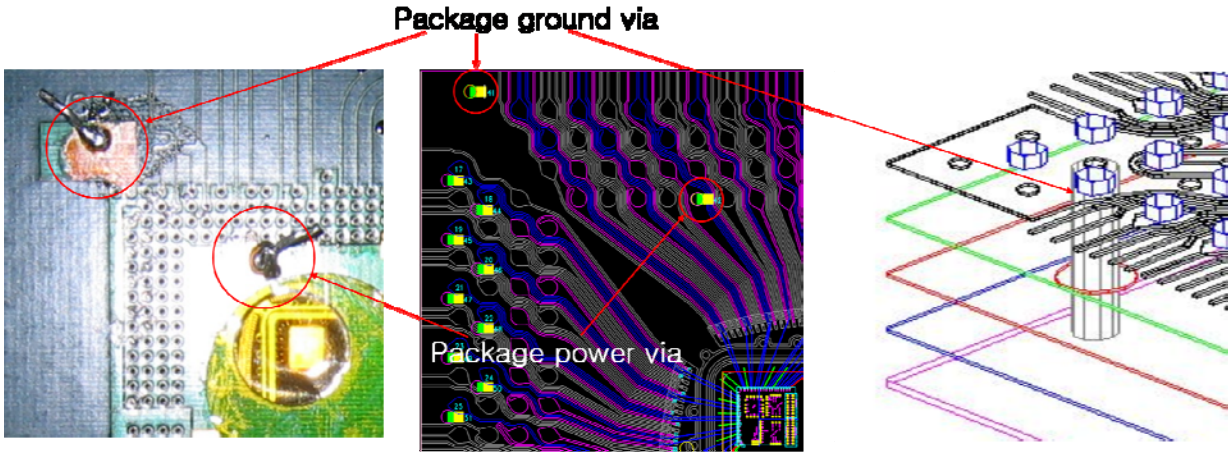


Figure 6-38. Ground and power via in GBGA package.

Figure 6-39 shows a zoomed picture indicating how peak noise is generated in a GTL I/O driver. When the open drain NMOS turns on and off, there are sudden currents flowing through the parasitic inductance of the package ground layer and these give rise to the large spike.

The above measurement results have been used for package electrical model verification with respect to signal integrity. For the CML I/O test IC, a 3-D modeling tool has been used for the package electrical model. But for the GTL I/O test IC, a 2-D modeling tool has been used to look at how accurately 2-D modeling tool could generate a package electrical model. The via model from 2-D modeling tool isn't accurate compared to the 3-D modeling tool. In addition, the 2-D modeling tool doesn't have the ability to model the distributed mesh network associated with package power and ground layer. Therefore, crosstalk and SSN verification showed large discrepancy in validation results. But 2-D modeling tool used RLGC distributed circuit for signal trace and the accuracy of trace model had been validated. On-chip signals including I/O pads and chip power/ground pads have been probed using a 12.5GHz high impedance FET probe shown in Figure 6-40 and IBIS macro models for the GTL I/O test IC has been created and simulated in the SPICE circuit simulator in order to validate the package SPICE model.

Figure 6-41 shows the on-board signals of port 1 from measurement and SPICE simulation. Propagation delay from SPICE simulation is closely matched to the measurement result. However, the waveform has a discrepancy in signal amplitude in the ringing portion. This is because the signal via had been modeled with 2D structure which has a different characteristic impedance from the actual via, which makes it necessary to use 3-D modeling tools.

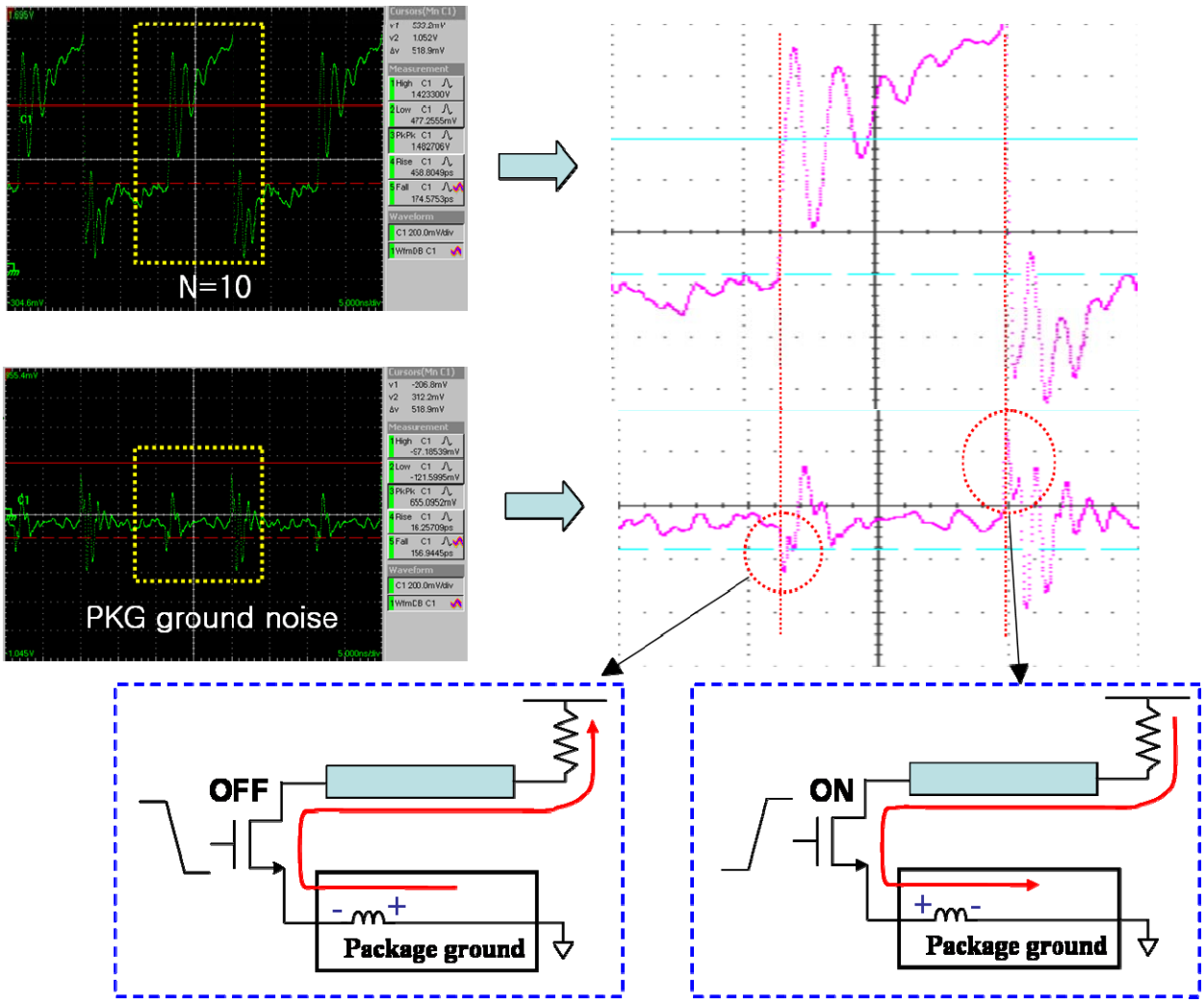


Figure 6-39. Package ground noise mechanism for GTL driver.

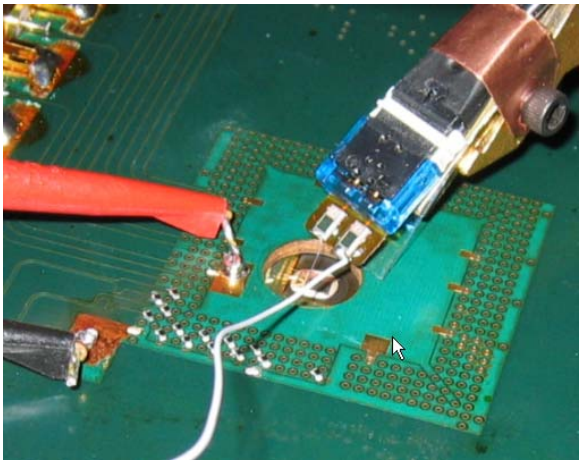


Figure 6-40. On-chip high impedance probing for GTL I/O test IC.

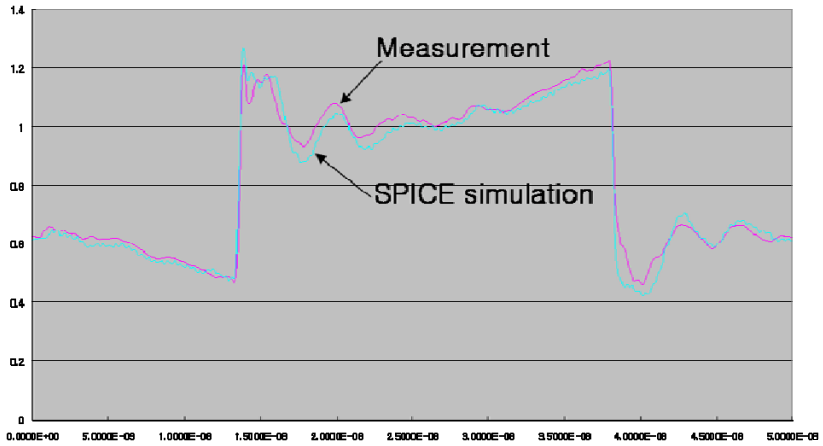


Figure 6-41. On-board signal comparison result for GTL I/O test IC.

In summary, this chapter presented the measurement results from the push-pull I/O test IC, the CML I/O test IC and the GTL I/O test IC. Three signal integrity effects, which are package trace effect, crosstalk, and SSN, have been measured with the I/O chip-package systems and key characterization data have been used for verifying the accuracy of package electrical models with respect to signal integrity. On-chip high impedance probing has been performed to generate IBIS macro models for CML and GTL I/O test ICs and SPICE simulation results have been compared with the measurement results to show how closely package electrical models are matched to the actual package performance.

CHAPTER 7
THE CRITERIA FOR THE ACCURACY OF PACKAGE ELECTRICAL MODEL

Important criteria for determining the accuracy of a package electrical model are defined in this chapter. The validation method provides useful information to empirically change IBIS models and achieve better accuracy. The criteria for model accuracy depend upon the IC application and data speed. For example, if a package is used for high data rate communication such as Gigabit Ethernet or SATA, then the package electrical model should be very accurate because a small inaccuracy can result in a poor BER. However, if the package is used for slow speed communication, the required accuracy can be relaxed because package parasitic elements do not affect the transmission of large transient signals very much. Even if the criteria are different according to application, an interpretation method to analyze the validation data needs to be developed. In Chapter 6, the accuracy of a package electrical model had been evaluated by comparing the signals from actual I/O driver measurement and SPICE simulation. In this case, the root-mean-squared value of signal difference is an obvious potential candidate for the criteria showing the accuracy of package electrical model. However, a root-mean-square (RMS) comparison of transient waveforms does not provide the specific information about where the discrepancies come. Many signal integrity effects are hidden in the summed effects of a root-mean-square calculation and each effect cannot be reported separately. The RMS information when the signal levels are stable at logic values is unimportant. But this state logic level information occurs for most of the waveform duration. Thus, this less important state logic level information affects the total RMS value and makes the RMS estimate meaningless. Therefore, in this research, instead of using the RMS value of total signal, a method by which one can observe only the key features of package signal integrity is presented; these features are propagation delay, edge rate, peak value on crosstalk and simultaneous switching noise. This is a more

efficient and meaningful approach than the total RMS value. The package evaluation and validation criteria can be categorized depending on the type of signal integrity effects.

Case 1) The accuracy of signal trace model: the propagation delay, the edge rate, the ringing due to impedance mismatch and the signal amplitude reduction due to the frequency dependent loss are used as a package validation and evaluation criteria.

Case 2) The accuracy of crosstalk model: the peak amplitude value of the FEXT is used as a package validation criteria.

Case 3) The accuracy of electrical model for package power and ground layer: peak amplitude of SSN is used as a package validation criteria.

The inaccuracy of the package electrical model is produced in the greatest part by propagation issues seen as data rates increase with shorter signal rise time. Non-ideal interconnect propagation issues include skin effect losses, dielectric losses, signal reflections, frequency dependent dielectric constants, etc. Propagation delay can be affected by the variations in the dielectric constants. In other words, the value of ε_r is not always constant for a given material but varies as a function of frequency and environment [2.7]. To ensure an accurate package electrical model, it is important to consider the frequency dependency of dielectric constant in the transmission line structure. Both the signal edge rate and amplitude can be affected by frequency dependent conductor and dielectric loss. In these high loss cases, the package engineer can improve the accuracy of package electrical model by increasing the package modeling frequency. In addition, if significant elements in the package can be modeled by broadband modeling instead of generating lumped package elements tuned to only a single frequency, then package electrical model has better correlation with actual package performance for transient signals. When a package trace has impedance discontinuities, it generates different

amounts of signal reflection and this affects the amount of undershoot and overshoot. In this case, the package trace impedance needs to be divided into much smaller sections and modeled by frequency variant RLGC distributed circuits in order to make a better modeled distributed line.

Accurate modeling of signal trace is critical in predicting accurate propagation delay, rise time, fall time and crosstalk noise. There are many ways to model the transmission line such as RC, LC, RLC and RLGC model. RC interconnect circuit model is the simplest model, but it is valid only at low frequencies because it doesn't include skin effect and dielectric loss. A frequency invariant lumped RLGC model is more accurate than simple RC model and has proven to be acceptable for moderate frequencies, but for fine line transmission line and higher frequency, more accurate models such as frequency variant RLGC circuit model are needed to predict accurate transmission line effect. In frequency variant RLGC models, frequency variant resistance, dielectric constant, capacitance and inductance could be successfully extracted and the values calculated from the models had a excellent agreements with s-parameter measurement results [7.1]. Also, frequency variant RLGC model provides accurate prediction of FEXT noise compared to other interconnect circuit models, especially when the signal rise time is a few tens of picoseconds [7.2]. Package models are made with the simplest model that is accurate in order to speed up simulation. Therefore, package model verification is necessary to maintain accuracy.

Figure 7-1 shows the validation results describing the accuracy of a package trace model used in GTL I/O test IC. The signal from measurement has 120.6ps rise time, but the signal from SPICE simulation shows a rise time of 70.6psec. This is due to the incorrectly modeled high frequency signal loss effects such as skin effect and dielectric loss. This measurement information shows package engineers that it is necessary to increase the frequency of model such

that it can reflect higher frequency transients. Figure 7-2 shows the zoomed picture of Figure 7-1 indicating that the waveforms have a slight discrepancy in the signal amplitude in the ringing portion due to an incorrect via model. As mentioned in Chapter 7, the GBGA package had been modeled with a 2-D modeling tool. The signal traces in the package are connected to an on-board 50 Ω resistor through the via. The via is 3-D structure and should be modeled with 3-D modeling tools in order to be accurate. As shown in Figure 7-3, a via can normally be modeled by a pi-network in 2-D modeling tools. The series inductance represents the via barrel and the capacitors represent the via pad capacitance on the different layers.

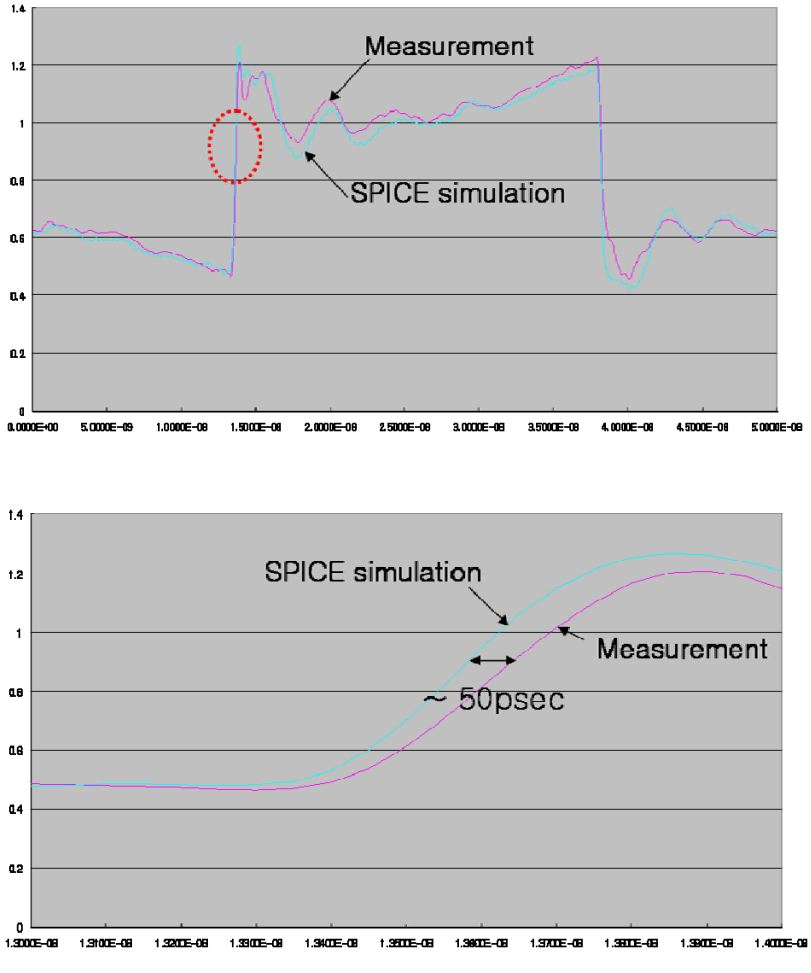


Figure 7-1. The accuracy of signal trace model. A) Signals from GTL I/O test IC. B) Zoomed picture showing signal rise time.

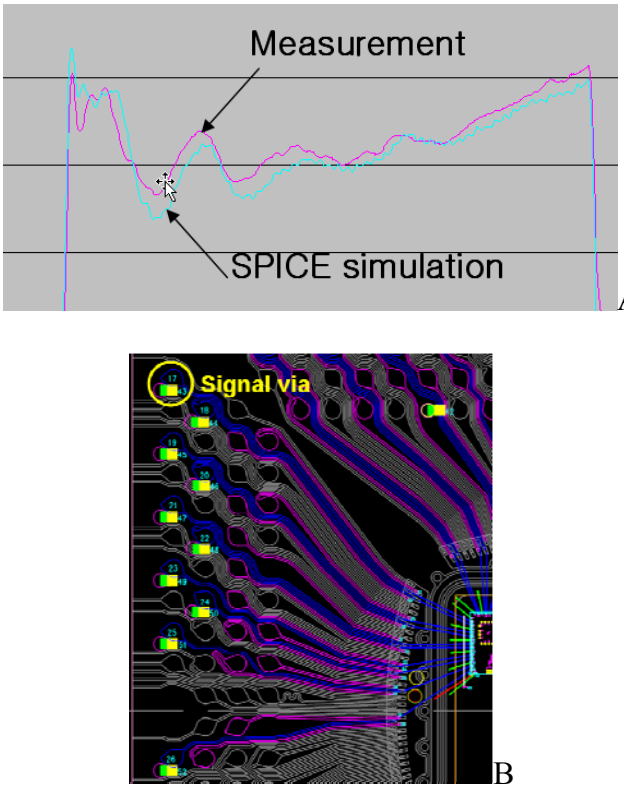


Figure 7-2. The effect of inaccurate signal via model. A) Zoomed picture. B) GBGA package having signal via.

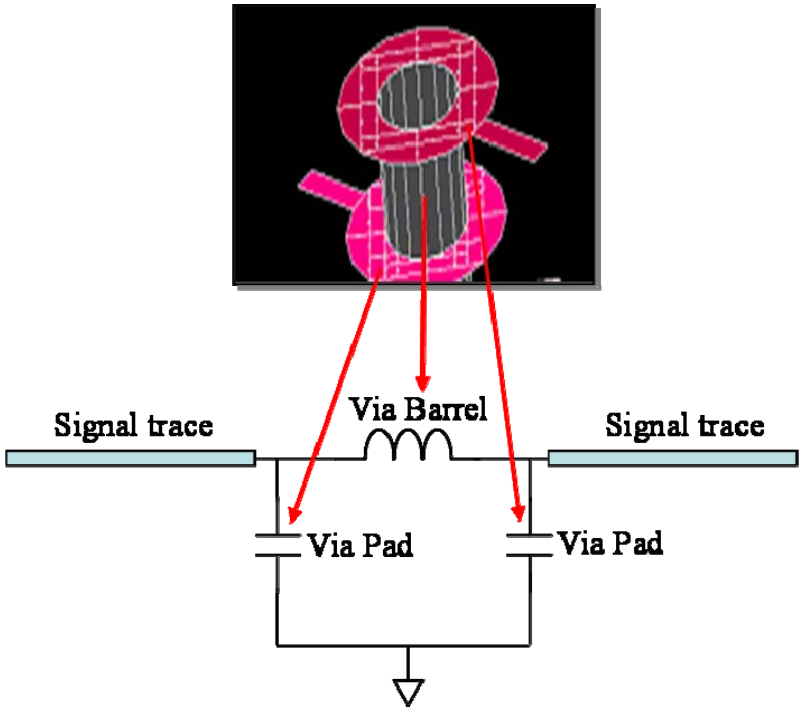
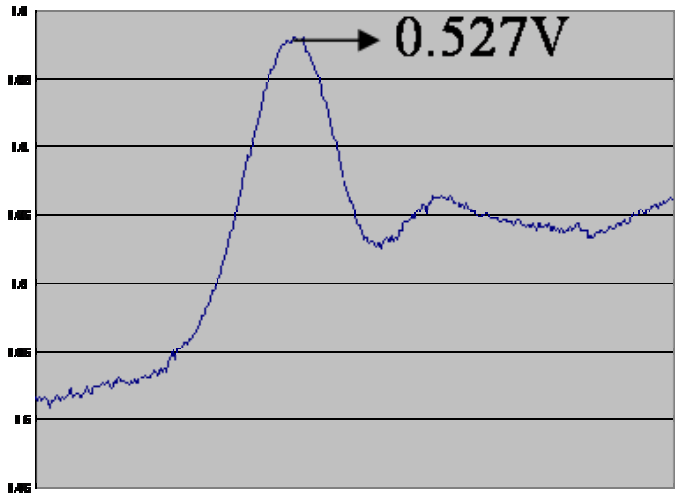


Figure 7-3. Equivalent circuit of via.

Although the via structure can be simply modeled as a lumped element circuit, this model will break down when the delay of the via is larger than one-tenth of the signal edge rate [2.7]. This means that the via needs to be modeled by full wave 3-D modeling tools when the signal edge rate becomes fast. If the series inductance and pad capacitances are inaccurately modeled, then the via will have a characteristic impedance different from anticipated which causes errors in estimate of signal reflections. If the signal edge rate is slow, the via model doesn't affect the signal waveform too much and is acceptable. The signal waveform shown in Figure 7-1 and Figure 7-2 had been generated by the GTL I/O test IC whose knee frequency was 4.5GHz. This range of frequency is high enough to include microwave effects. In order to generate accurate package electrical models in this frequency range, accurate via models should be obtained by simulating the package trace using a 3D field solver with all relevant metallization geometry modeled. In full-wave modeling, the electric and magnetic fields for via are typically solved in a volume and the vias are modeled by mesh elements.

When mutual coupling effects due to the mutual inductance and capacitance are incorrectly modeled, package electrical model has different peak amplitude in FEXT measured and modeled result comparisons. The magnitude and shape of the crosstalk noise depend heavily on the amount of coupling when aggressor and victim line has a specific load termination. FEXT can be either negative or positive depending on the relative magnitude of inductively and capacitive coupled components. Figure 7-4 shows a FEXT validation result for the CML I/O test IC. All the signal traces and coupling coefficients were modeled with a 3-D modeling tool and the maximum FEXT value from SPICE simulation is closely matched to the measurement result. However, the FEXT from the SPICE simulation has a lower peak amplitude than the measurement indicating that modeling tool overestimates mutual inductance or underestimates

mutual capacitance. Because the frequency dependent dielectric constant gives rise to different amounts of mutual capacitance, the modeling frequency should be increased to cover the effects of the non linear constant dielectric constant.



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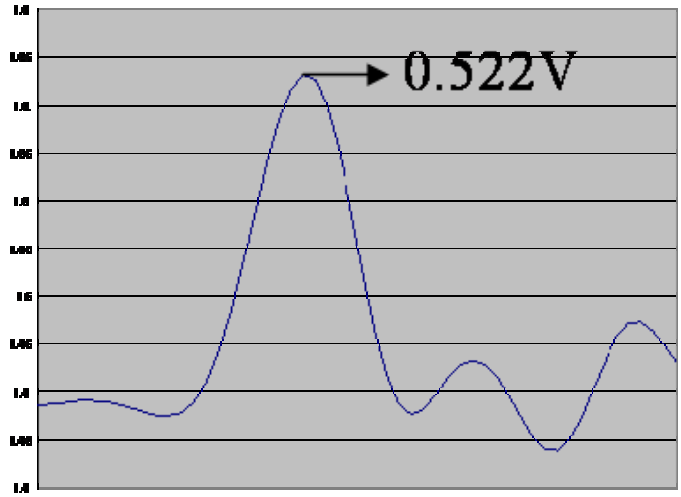


B

Figure 7-4. FEXT comparison result of CML I/O test IC. A) Measured FEXT. B) SPICE simulation result.

As explained in Chapter 5, a package electrical model showed different amounts of SSN when the package reference (power and ground) layer are incorrectly modeled. A package reference layer needs to be modeled by a meshed RLGC distributed circuit through the 3-D

modeling tools because of the many through-hole vias and complicated current and voltage distribution. Figure 7-5 shows the SSN comparison result for CML I/O test IC indicating that the peak value of the package ground noise from the SPICE simulation is closely matched to the measurement value. Although noise signal shapes are not exactly same as those from the measurement results, the peak amplitude is a much more important factor, especially in crosstalk and SSN.

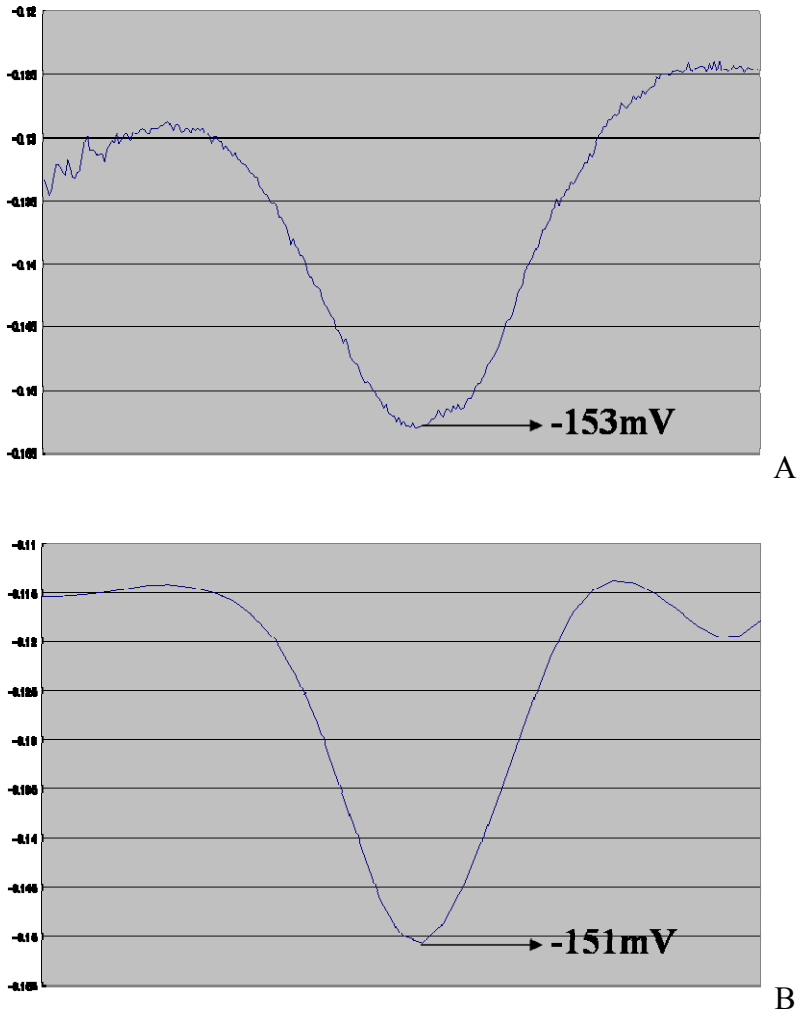


Figure 7-5. SSN comparison result for CML I/O test IC. A) Measured peak value. B) SPICE simulation result.

Full-wave modeling tools provide the better accuracy and become imperative for higher frequencies, but building and editing a 3-D model can be time consuming if package engineers

have no idea how many power and ground layers completely should be added to be accurate. If the target goal is set by the measurement results of the peak SSN, the package engineer can gradually increase the complexity of package power and ground layers until differences between the peak SSN values from SPICE simulations and measurement are within the margin specified by the application.

In summary, this chapter presented important criteria for determining the accuracy of package electrical model. The key features of package signal integrity were suggested as the potential criteria and the methodology on how to interpret the validation results was explained for signal trace effect, FEXT noise and SSN.

CHAPTER 8
SUMMARY AND FUTURE WORK

8.1 Summary

The important contributions of this work to the field of high-speed I/O chip-package systems are summarized in this chapter. The goal of this research was to develop a methodology that can effectively characterize the signal integrity performance of a high-speed I/O chip-package system and verify the package electrical model using the SPICE macro model. The increase in the higher performance electronic devices drives a faster data rate and a higher packaging density. This makes it essential to have accurate package electrical models before the chip is manufactured at production level. A possible solution for package model verification is with I/O test IC, which will minimize the discrepancies between the actual performance characterized with measurements and predictions derived from conventional modeling methods. This is proposed in Chapter 1. The major speed bottleneck in the high-speed I/O chip-package system is package signal integrity such as power/ground fluctuation due to the switching noise, cross talk, intersymbol interference (ISI) and these effects are explained in Chapter 2. The architecture and circuit design for I/O test ICs are described in Chapter 3 and Chapter 4. Three versions of I/O test ICs, each of which has push-pull I/O, CML differential I/O, and GTL I/O, have been designed with the IBM7WL 0.18um process and the TI 65nm CMOS process and each of them has unique functionality in order to characterize different types of packages. Chapter 5 describes the high impedance probing technique in detail used to create the IBIS macromodel of the I/O test IC. Time varying voltage sources measured at the chip bond pads include dynamic buffer impedance information and can create time varying current at all signal and return current paths. This makes it simple to create true signal integrity phenomena inside the package SPICE model and remove the discrepancy between simulation and measurement;

making it possible for the chip design engineer to use accurate package electrical models. Simulation results are shown to prove how IBIS macromodel can represent the I/O test IC response and how to validate or invalidate the package electrical model through the time domain signals showing their signal integrity performance. All the simulations have been performed with an Amkor lead frame package for demonstration purposes.

Finally, measurement results are shown in Chapter 6. All test ICs have been assembled with a TI GBGA package. First of all, each I/O test IC has been measured with a different measurement setup to prove the chip performance and functionality. Maximum bandwidth of the CML I/O and GTL I/O are reported using the signal rise time probed at the chip bond pad after removing the package; this is the maximum frequency that I/O test IC can validate package electrical models. After that, package validation for the TI GBGA packages are performed to show how test data is useful in developing, optimizing, verifying or invalidating existing commercial IC package interface models.

8.2 Suggested Future Work

8.2.1 Next Generation I/O Test IC Design

Increasing signal integrity problems make it necessary to characterize and validate the package signal integrity performance after conventional package modeling procedures. In this research, I/O test ICs have been developed to provide real operating conditions for validating package electrical models. High impedance probing techniques are used to capture on chip signals to generate IBIS macromodel of a I/O test IC. However, rapid advances in integrated circuit technology drive the I/O data rate to be faster and making it hard to capture the on-chip signals with commercial high impedance probes. Besides, launching high speed input and clock signals to the I/O test IC is increasingly difficult because of the limited bandwidth of package,

making it necessary to develop more sophisticated I/O test ICs. In order to solve the above mentioned problems, future I/O test ICs should have following additional circuits.

- On-chip high speed sampler for I/O signals.
- On-chip clean clock generator

On-Chip High Speed Sampler for I/O Signals: Probing the on-chip signal is really important for creating a IBIS macromodel and a high impedance probe has been used for this research. However, currently available high impedance probes are very expensive, especially for good high frequency performance. High speed on-chip samplers using sub sampling techniques has been already included in I/O test ICs; the sampled probe points were power and ground lines. If on-chip samplers are added to the output of an I/O driver, they can remove the necessity of an expensive high impedance probe and reduce the validation cost. Because on-chip samplers were designed such that their outputs are transmitted at low speed, they allow the use of a low performance real time oscilloscope or A/D; this will reduce the overall test cost. Besides, non ideal interconnect effects associated with package do not distort the signal waveform of sampler output since it is low speed.

On-Chip Clean Clock Generator: As explained in Chapter 3, different types of clock and data receivers were included in the I/O test ICs in order to reshape the high speed signals. But this technique will become major bottleneck of the I/O test IC performance because it's difficult to launch high speed input signals through the package and the PCB board. This is the same issue in current high speed I/O trends and this difficulty makes it necessary to use a more sophisticated method to allow high speed I/O chip-package characterization at higher speed. A phase locked loop (PLL) can be a possible solution for an on chip clean clock generator since it has a frequency multiplication capability. High speed input data can also be slower using a delay

locked loop (DLL) and some interface circuitry. Appendix C explains in detail about new approach to next generation I/O test IC design. By using these techniques, all input signals will become slow speed allowing the designer to use a low performance external stimulus system.

8.2.2 In-Situ Characterization of I/O Chip-Package-Socket Systems

If the silicon die is directly connected to the PCB board through a package, it wouldn't be interchangeable. In this case, a socket needs to be used to allow the package plug in or out from the PCB board. A good example for using a socket is when the CPU or memory card needs to be upgraded. Like the package, socket also affects to the overall signal integrity performance especially due to the pin inductance and the pin capacitance. The I/O test IC based characterization method can be effectively used to look at the socket effects on signal integrity. Figure 8-1 shows the socket soldered on a test board which has been used to select the functional packaged CML and GTL I/O test IC.

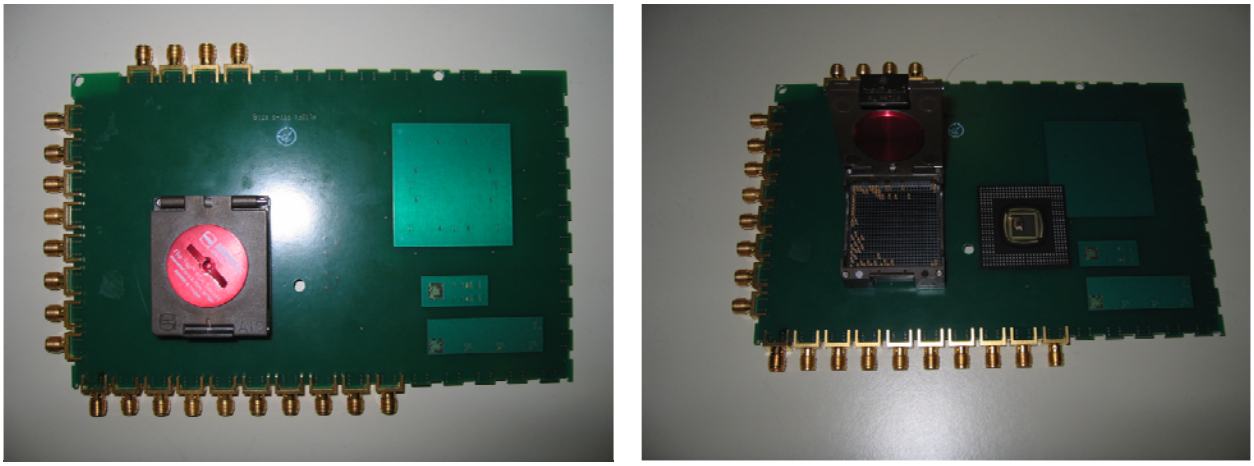


Figure 8-1. Test board having packaged IC and socket.

8.2.3 3-D Packaging Characterization

Three dimensional packaging is gaining wide attentions in the products that require high density and small space such as wireless products or consumer products. This attention comes from the fact that 3-D packaging technology allows multiple device types to be integrated into

the same space as a single die by stacking the silicon chips inside the same package. It has been reported that 40 to 50 times reduction in size and weight is achievable using 3-D stacking technology compared to conventional packaging [8.1]. As shown in Figure 8-2, one 3-D package could replace two or more single die packages; this would reduce the electrical trace length on the substrate and PCB which enhance the electrical performance significantly [8.2]. In spite of many advantages, there are several issues that need to be taken into account when using 3-D technology in package design. Because of the design and modeling complexity, the development time can be more than the time taken by 2-D packaging technology. This means a more robust signal integrity performance verification tool is crucial. This problem can be addressed by characterizing and validating 3-D package with the high speed I/O test IC.

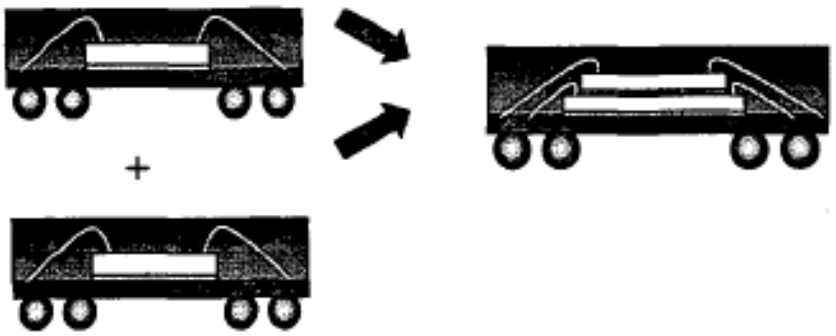


Figure 8-2. 3-D package replacing two single die packages.

APPENDIX A
HIGH-SPEED I/O STANDARDS

A.1 An Overview of I/O Signaling Standards and Techniques

There are versatile standards and techniques associated with I/O signaling. Many I/O standards incorporate a combination of different signaling categories and it makes it difficult to organize all the I/O standards. But we can characterize I/O standards in three groups.

1) I/O driver and receiver type
   - Single-ended vs. Differential
   - Voltage mode vs. current mode
2) Bus interface type
   - Point-to-multipoint : multi-drop bus
   - Point-to-point : point-to-point parallel link, point-to-point serial link
3) Timing method
   - Common clock timing
   - Source synchronous timing
   - Embedded timing
4) Signaling technologies
   - GTL, SSTL, HSTL, LVDS, CML, etc.

A.1.1 Single-Ended versus Differential

Single-Ended I/O: In single-ended I/O, signal transmission is performed on one signal line and this signal is compared to a reference voltage in receiver. The advantages are simple, low cost and low power consumption. But single ended I/O is susceptible to crosstalk and common mode noise. It also has simultaneous switching noise, huge ground and power noise,

Large EMI due to big loop inductance Figure A-1 shows signal and return current flow in single-ended and differential I/O.

Differential I/O: In differential I/O, the driver transmits two signals which are complimentary each other and receiver detects voltage difference between the inputs. In high-speed systems, the reason differential signaling is preferred is because it is relatively insensitive to symmetric discontinuities; that is, discontinuities that affect both members of the pair equally. The advantages of differential I/O over single ended I/O are the less ground and power noise, better noise performance, less cross talk noise, less electro-magnetic interference (EMI) noise and large signal swing. However, differential I/O consumes larger power and larger chip size than single ended I/O. Figure I-1 shows signal and return current flow in single-ended and differential I/O.

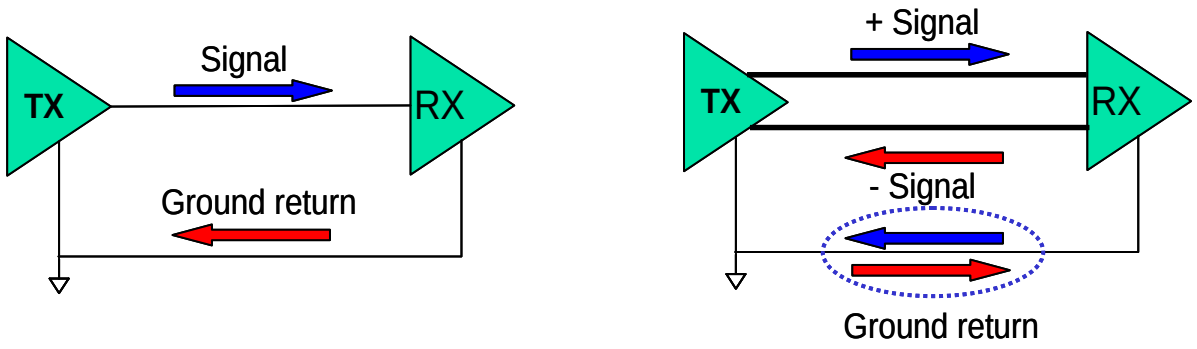


Figure A-1. Single-ended I/O versus differential I/O.

A.1.2 Voltage Mode versus Current Mode

From the driver perspective, if the driver has low impedance path to ground or VDD, then it is voltage mode driver. In contrast, a current mode driver has high impedance path to the ground or VDD. This high impedance path isolate the output node to ground or VDD, it is less susceptible to power and ground noise. From the receiver perspective, the input impedance of voltage mode receiver is high because it is a capacitive node. The current mode receiver has low

input impedance by using a resistive termination. Because of a smaller RC time constant, the current mode I/O is faster than voltage mode I/O since the signal swing is smaller.

A.1.3 Bus Interface

Multi-Drop Bus: Multi-drop bus topologies are commonly used in the front side bus on a computer motherboard that connects multiple processors and memory modules. The speed bottleneck of this bus interface mainly comes from the impedance mismatch at the stub nodes. A sharp edge data transition propagating down the bus will partially reflect off each stub. To avoid these reflections, the rise time of the signal on the bus must be significantly longer than the round-trip delay of the stub so that the stub acts as a lumped capacitance [2.3]. Figure A-2 illustrates how multi-drop bus is organized.

Parallel Bus: Parallel bus has been widely used in short distance applications when this link has explicit clock signal such as source synchronous interface. The major drawback of parallel interface is pin-to-pin cross talk. Figure A-3 shows point-to-point source synchronous parallel links.

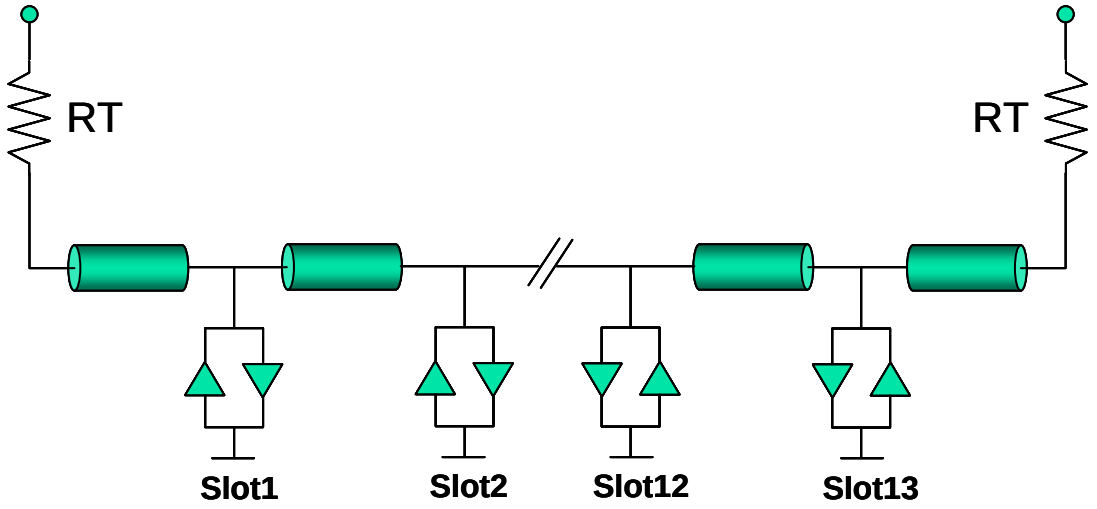


Figure A-2. Multi-drop bus topology.

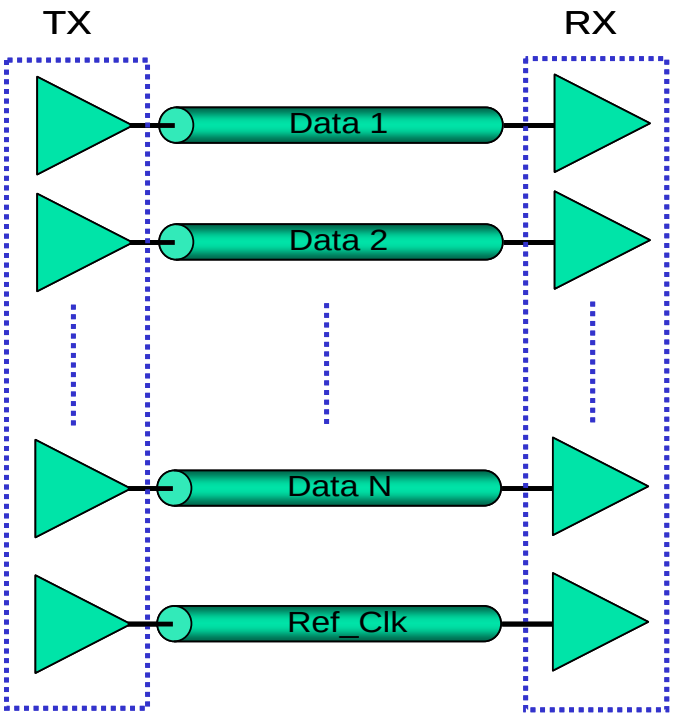


Figure A-3. Source synchronous parallel bus.

Point-to-Point Serial Bus: Point-to-point serial interface which is illustrated in figure A-4 is the current high speed I/O trend. In this bus interface, the data must first be converted to a serial data through the serializer. The serial data is then transmitted to the receiver, which deserializes the data back into the parallel data. Receiver generates its own clock using clock and data recovery circuit (CDR), removing the need for routing the clock signal on the board.

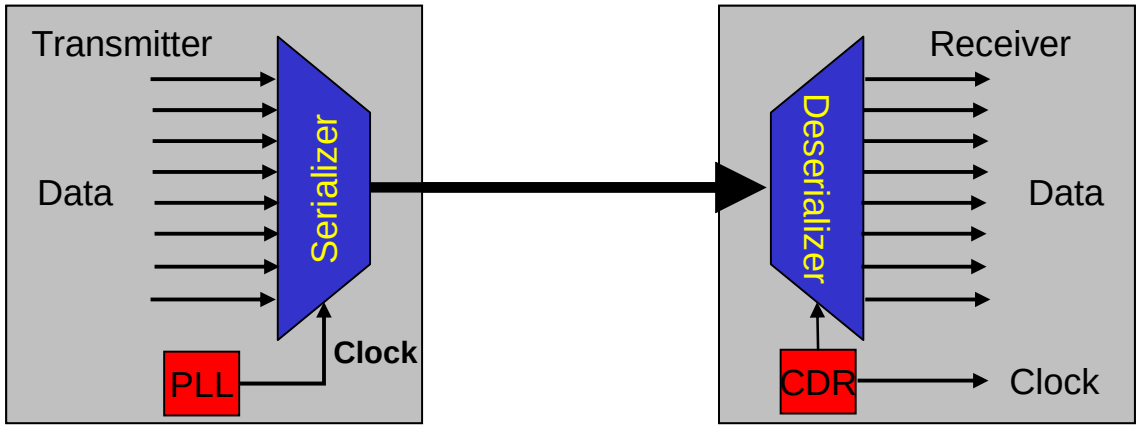


Figure A-4. Point-to-point serial interface.

A.1.4 Timing Topologies

Transmitter IC can send data to the receiver IC using clock signals and there are two timing methods. Common clock timing is timing scheme where single clock is shared by driver and receiver on a bus. This technique is generally adequate for medium speed buses with frequencies below 200 to 300MHz and this limitation stems from the total delay of the circuitry and the PCB traces, which much remain less than the delay of one clock cycle [2.7]. Second method is source synchronous timing, which is generally used in high speed microprocessor and memory interface. In contrast to the common clock timing, source synchronous timing is a technique where the strobe signal is sent from the driver chip instead of a separate clock source. Since the strobe and data signals are sent from the same driver, the design depends on the delay difference between the groups of strobes and the data, which is an easy design compared to a common clock bus as shown in Figure A-5 [A.1]

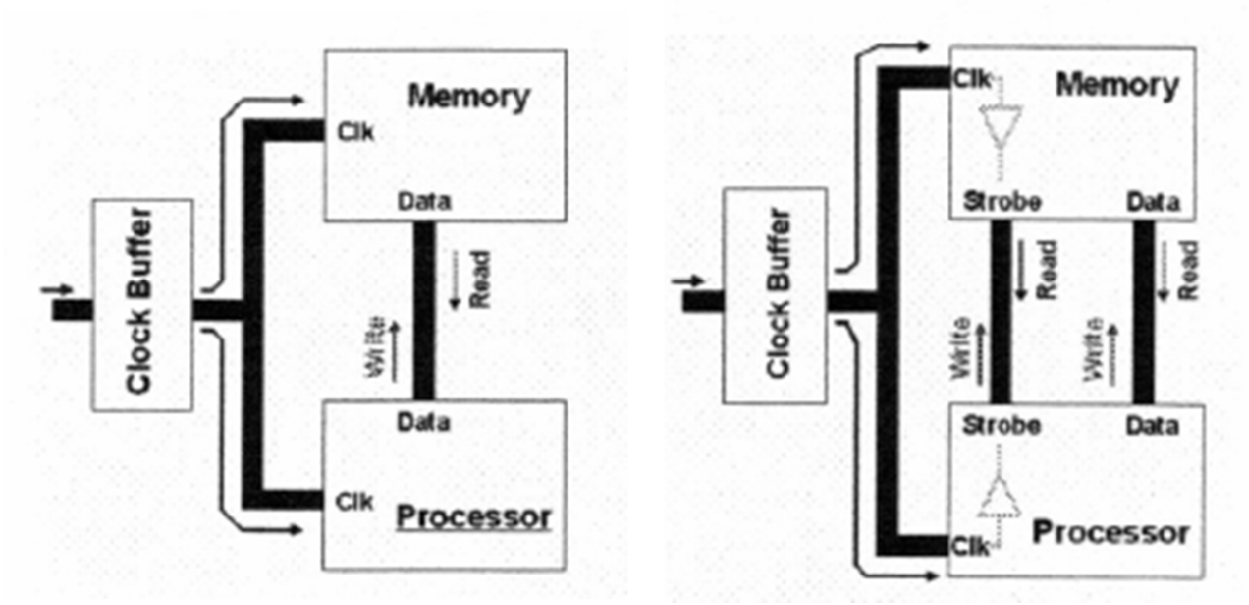


Figure A-5. Bus signaling techniques.

As the data rates continue to increase, it is becoming increasingly difficult to match the data and timing signal lines to eliminate timing skews. Furthermore, requiring a timing signal line to be routed along with the data line is costly in terms of board area and power. An attractive option is to remove the timing line and instead use a circuit on the receiving chip that requires only the data signal itself to determine when to sample the data signal to most reliably extract the data. Such a circuit is called a Clock-Data Recovery (CDR) circuit. Embedded timing is generally used in point-to-point serial interface.

A.2 Evolution of High-Speed I/O

The continuous improvement of the performance of PC and network server has made the I/O bandwidth the primary performance bottleneck of entire system. Figure A-6 shows the block diagrams of legacy and new trend personal computers [A.2].

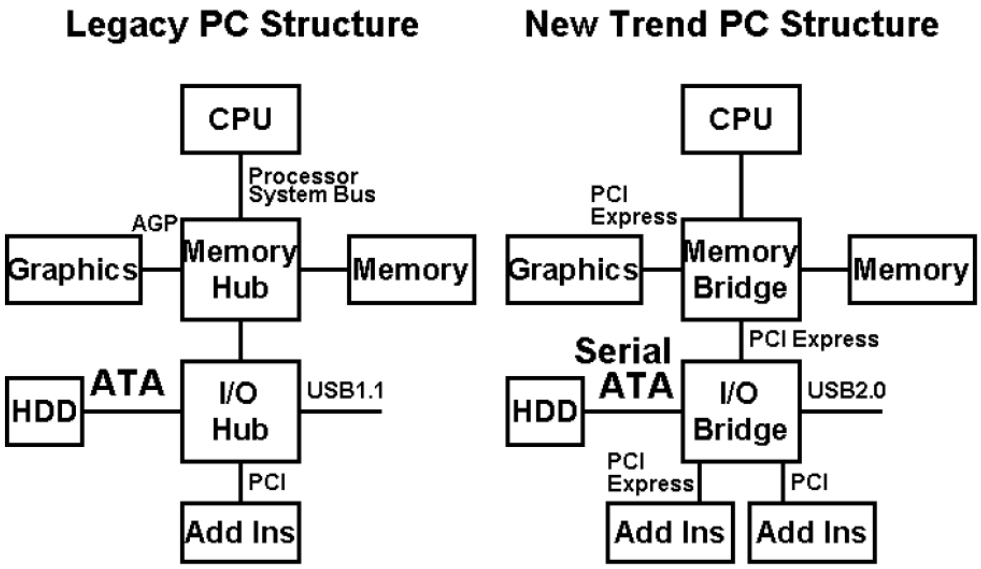


Figure A-6. New PC structure.

There are common characteristics in the evolution of high speed I/O, which is point-to-point serial interface which has embedded clocking through CDR. This dramatically reduces the

number of connections, the pin count and the cost. This also makes the board size smaller because the routing area is reduced. The features of high speed serial interface is

- Serializer and deserializer
- Low swing differential signaling
- Embedded clocking with CDR
- Channel equalization
- On-die termination

As system requirements grow over time, the parallel link employs serial link techniques like embedded clocking and serializer and deserializer. As a result, the distinctions between serial links and parallel links are blurred.

APPENDIX B
FREQUENCY-DOMAIN COMPONENTS IN DIGITAL SIGNAL

There are several ways to estimate the spectral envelope of a digital signal [2.7]. Widely used estimation technique approximates the frequency envelope by observing the fastest edge rate and equation B-1 is derived from equation B-2, which is the response of a step function into a network with a time constant.

$$f_{knee} = \frac{0.35}{t_r} \tag{B-1}$$

$$V = V_{input}(1 - e^{-t/\tau}) \tag{B-2}$$

Setting $V = 0.1V_{input}$ and $V = 0.9V_{input}$ allows the calculation of the 10-90% rise time in terms of the time constant. 10-90% rise time is $t_{10-90\%} = t_{90\%} - t_{10\%} = 2.3\tau - 0.105\tau = 2.195\tau$.

The frequency response of a 1 pole network is $F_{3dB} = \frac{1}{2\pi\tau} \rightarrow \tau = \frac{1}{2\pi F_{3dB}}$ and substituting this into the step response yields $t_{10-90\%} = \frac{1.09}{\pi F_{3dB}} = \frac{0.35}{F_{3dB}} \approx \frac{1}{\pi F_{3dB}} \rightarrow F_{3dB} = \frac{0.35}{t_{10-90\%}}$

APPENDIX C
10GB/S DIFFERENTIAL I/O TEST IC

C.1 Overall Block Diagram

As explained in chapter 3, it is fairly difficult to launch high speed clocks through measurement instruments without using an on-chip clean clock generator, especially with wire bond packages because of the L-C low pass filter due to the bond-wire inductance in combination with the on-chip capacitance. A high speed multiplexer also needs to be used in order to reduce the speed requirement of the programmable data register. Programmable data register consists of lots of CMOS flip-flops and the number of flip-flops can be more than 500 if there is a need to fire $2^7 - 1$ PRBS data across quad CML I/O. Therefore, the clock buffer chain is necessitated to drive huge capacitive nodes associated with the data register. The maximum data rate has a practical limit set by the on-chip clock period, which in turn is determined by the bandwidth of the clock buffer chain. Figure C-1 illustrates the reduction of the clock amplitude as the frequency is increased and in order to maintain a reasonable clock amplitude, the clock period is constrained to roughly 6FO-4 [C.1]. If we add N:1 multiplexer between I/O driver and data register, the speed requirement of data register is reduced by N. Even if we could solve the speed bottleneck through the multiplexer, clock buffer chain is still needed to drive a huge capacitive load for the data register. The clock buffer chain has large delay and this will cause timing error when multiplexer tries to capture the parallel data from data register. Therefore, to keep enough timing margin, a clock aligner such as a DLL is added to remove the clock skew. This also helps us to use different clock signals when the data register loads the serial data from measurement instrument. After the data register stores serial data from external test equipment, the DLL starts working and removes the clock skew so that the data register could use the same clock signal with the multiplexer. The biggest advantage of using different clocks is that we can

use very a slow speed of clock and data when the data registers load the serial data. This makes it possible to use a low cost stimulus system and achieve a low cost characterization methodology.

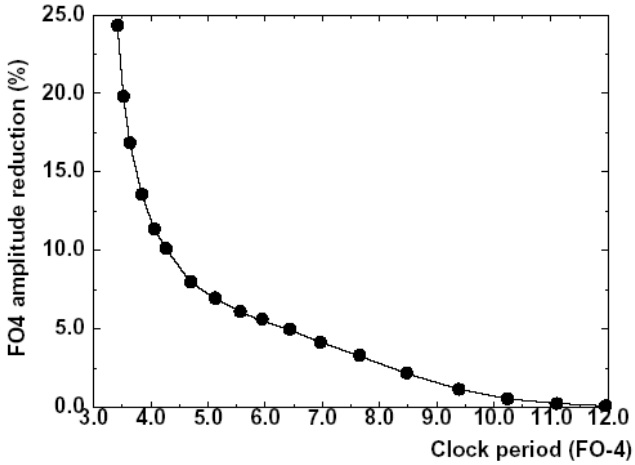


Figure C-1. Clock amplitude reduction (%) with clock period (in FO-4 delays).

The I/O drivers are designed such a way that they fires data which has the fastest edge rate. This will allow engineers to look at the worst case signal integrity of package and board and compare the performances of different types of package and board. Figure C-2 shows the overall block diagram for multi Gb/s differential I/O test IC.

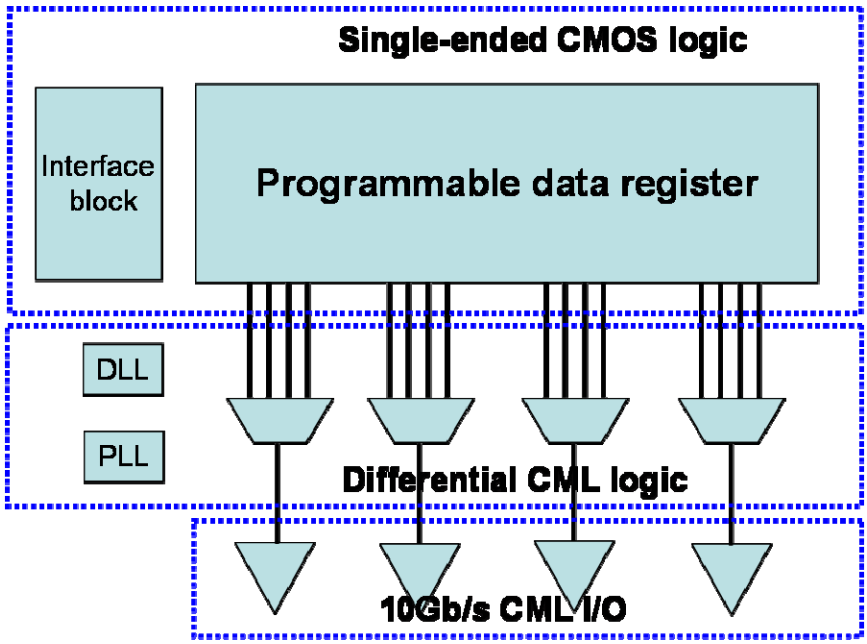


Figure C-2. Overall block diagram for 10 Gb/s differential I/O test IC.

C.2 Fully Differential High-Speed Multiplexer

The multiplexer style adopted in this design is a tree type architecture. Illustrated in Figure C-3, the tree structure 4:1 MUX is a natural extension of 2:1 MUX which consists of a master-slave flip-flop, master-slave-master flip-flop, and a selector. Current-mode logic (CML) gates are used for the flip-flops and the SEL gate to increase the system speed. In this architecture, Inter-stage timing design between 2:1 MUX M3 and the retimer flip-flop is critical for full rate clock operation [C.2]. An internal clock buffer CB1 is composed of multistage CML buffer and increases the timing margin of the final retiming flip-flop. 4:1 multiplexer was designed and simulated with TI65nm process, as shown in Figure C-4. All sub circuits were designed using differential CML logic. Figure C-4 (B) is the simulation results showing the 10 Gb/s output from the multiplexer. Serial-to-parallel converter can be used to generate 4 bit parallel data for 4:1 multiplexer and Figure C-5 illustrates the example of showing how 4:1 multiplexer combined with serial-to-parallel converter can generate serial data having 8 bits data depth.

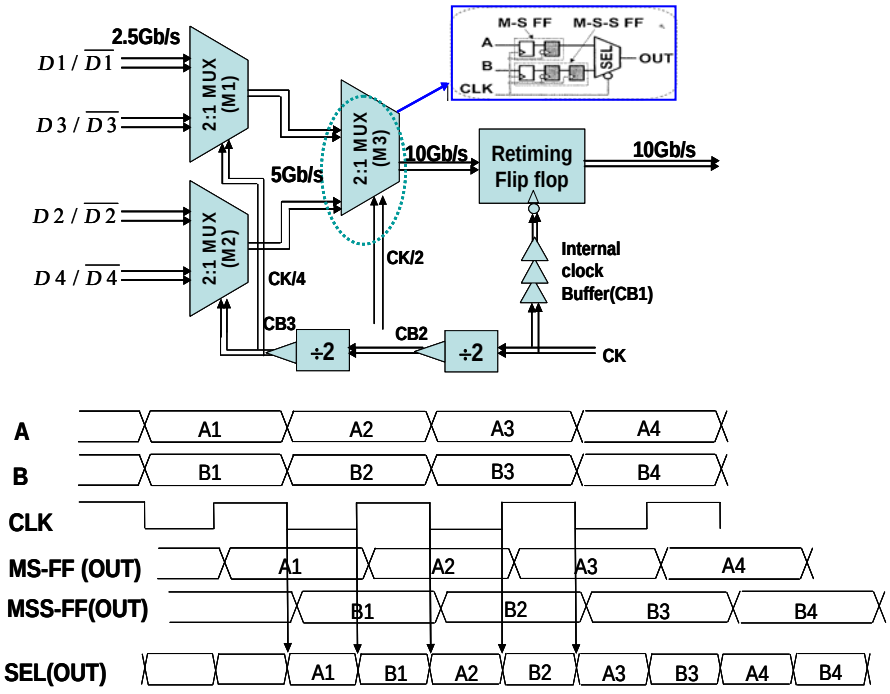


Figure C-3. Structure and timing diagram of 4:1 tree multiplexer.

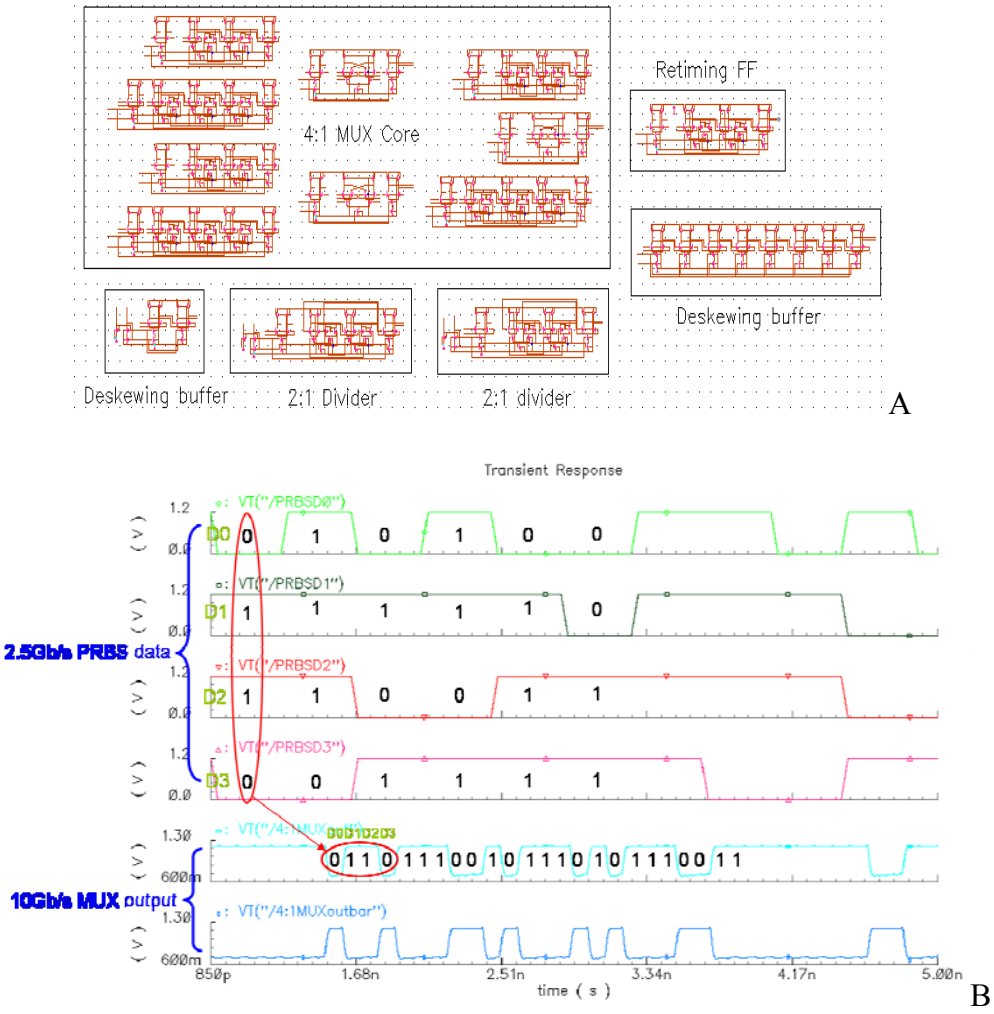


Figure C-4. 10Gb/s 4:1 multiplexer. A) Schematic. B) Simulation results.

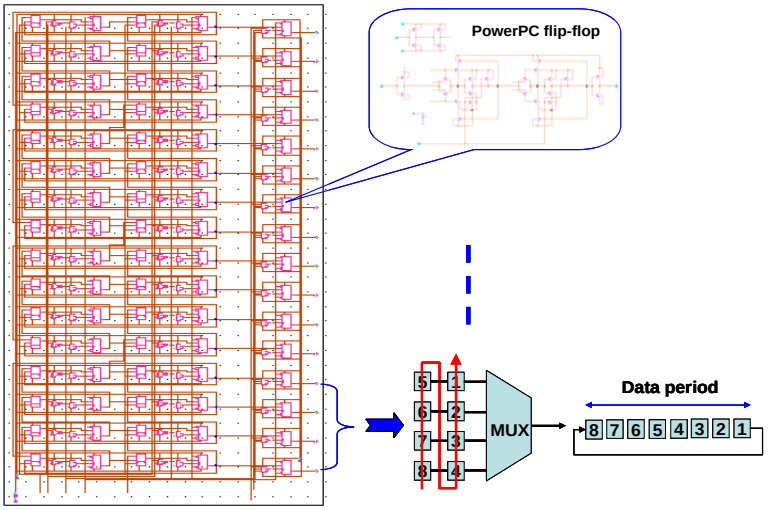


Figure C-5. Example of serial data having 8 bit data depth.

C.3 Timing Interface Circuit

As mentioned previously, the serial-to-parallel converter doesn't have to use a fast clock and data when it loads the serial data from the measurement instrument. After it is finished loading the data, the data register fires the parallel data to multiplexer with the fast clock which is synchronized to the multiplexer clock. In order to make this scheme behave reasonably, a clock aligner and interface circuitry was added which consists of a Schmitt trigger, retiming flip-flop and clock selector. The clock selector selects the external low speed clock when data register loads the data and switches to the fast clock after the DLL removes the clock skew. But between these two modes, this block needs some time period to get the DLL to achieve a lock condition and the data register turned off to prevent stored data from being removed. As shown in Figure C-6, time period B is generated by two control signals which are a clock selection signal and register select signal. The operation of the interface circuit is as follows. Clock multiplexer selects external low speed clock during the loading of data. After loading the data, data register is turned off for a while so that DLL has sufficient time to synchronize these two clocks. After DLL is locked, then clock multiplexer selects the fast on-chip clock to transfer the parallel data to the 4:1 multiplexer.

C.4 Delay-Locked Loop (DLL)

DLL aligns the phase of the output to match the input by delaying the input signal. It consists of phase frequency detector (PFD), charge pump and voltage controlled delay line (VCDL). PFD gives phase difference information to the charge pump and charge pump charges or discharges the current which is proportional to the phase difference and loop filter integrates this current through the capacitor to give the control voltage to the VCDL.

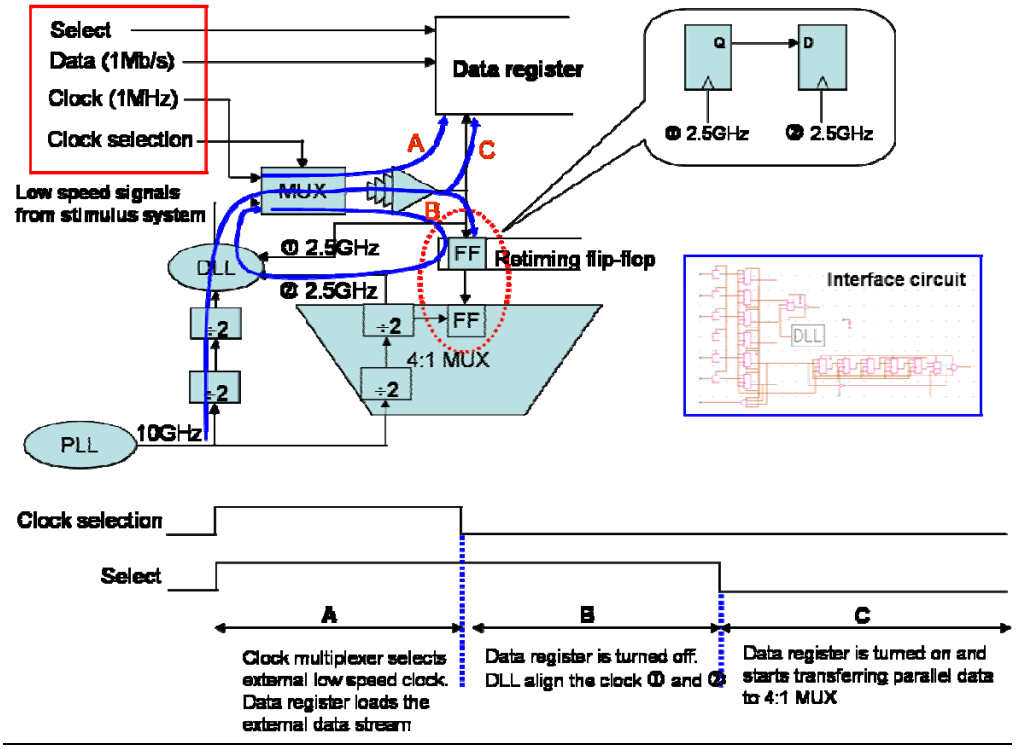


Figure C-6. Timing interface circuitry.

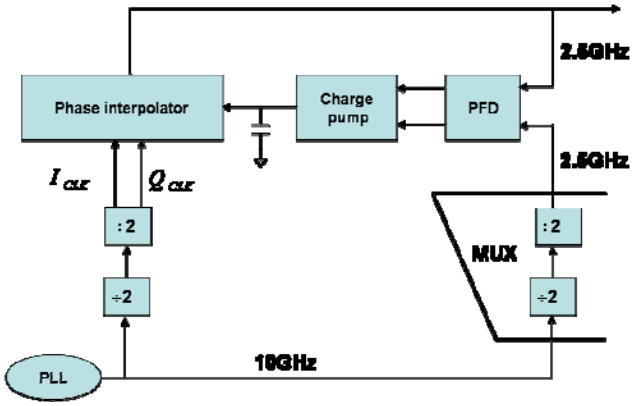


Figure C-7. DLL block diagram.

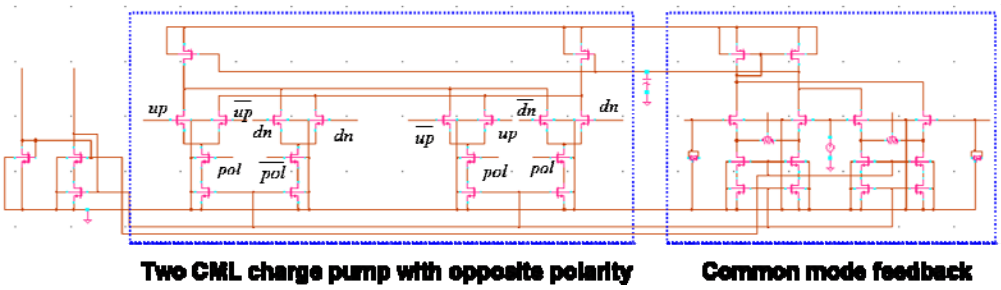


Figure C-8. CML charge pump and CMFB.

In this research, analog phase interpolator based DLL was chosen because of its infinite phase shift capability and Figure C-7 shows the DLL block diagram. Fully differential circuits were used for entire sub blocks to get a good CMRR and PSRR. The loop bandwidth was decided such that the ripple on the control voltage causes 1% jitter. A charge pump is realized by connecting two conventional CML charge pumps with opposite polarity in parallel, as shown in Figure C-8. Analog phase interpolator consists of quadrature clock mixer, constant transconductance boundary detector and finite state machine [C.3]. It provides infinite phase shift by using two quadrature clock signals from the frequency divider and Figure C-9 shows how phase interpolator can have infinite phase shift. A quadrant boundary detector constantly detects when a I or Q clock should flip over to I_bar or Q_bar and generate I_comp and Q_comp signal to the Finite-State-Machine (FSM) whose outputs generate the signals I_sel , Q _sel and pol_flip. Two parallel charge pumps are selected by the pol_flip signal such that the system constantly generates differential control voltages V_c^+ and V_c^-. Figure C-10 shows the schematic for DLL and phase interpolator simulation result.

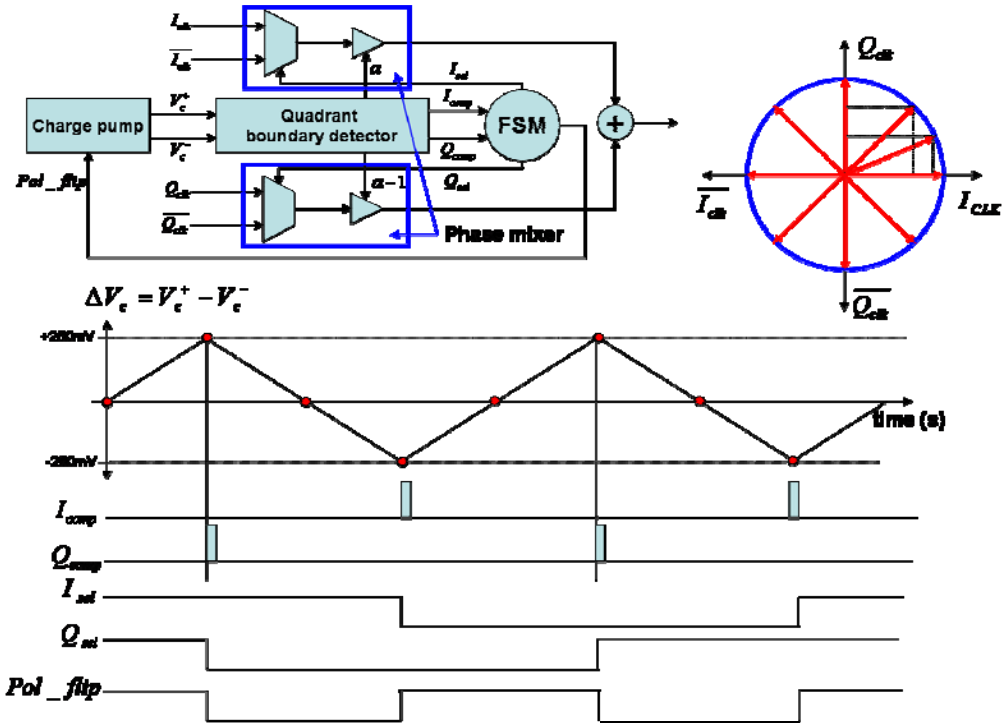


Figure C-9. Phase interpolator.

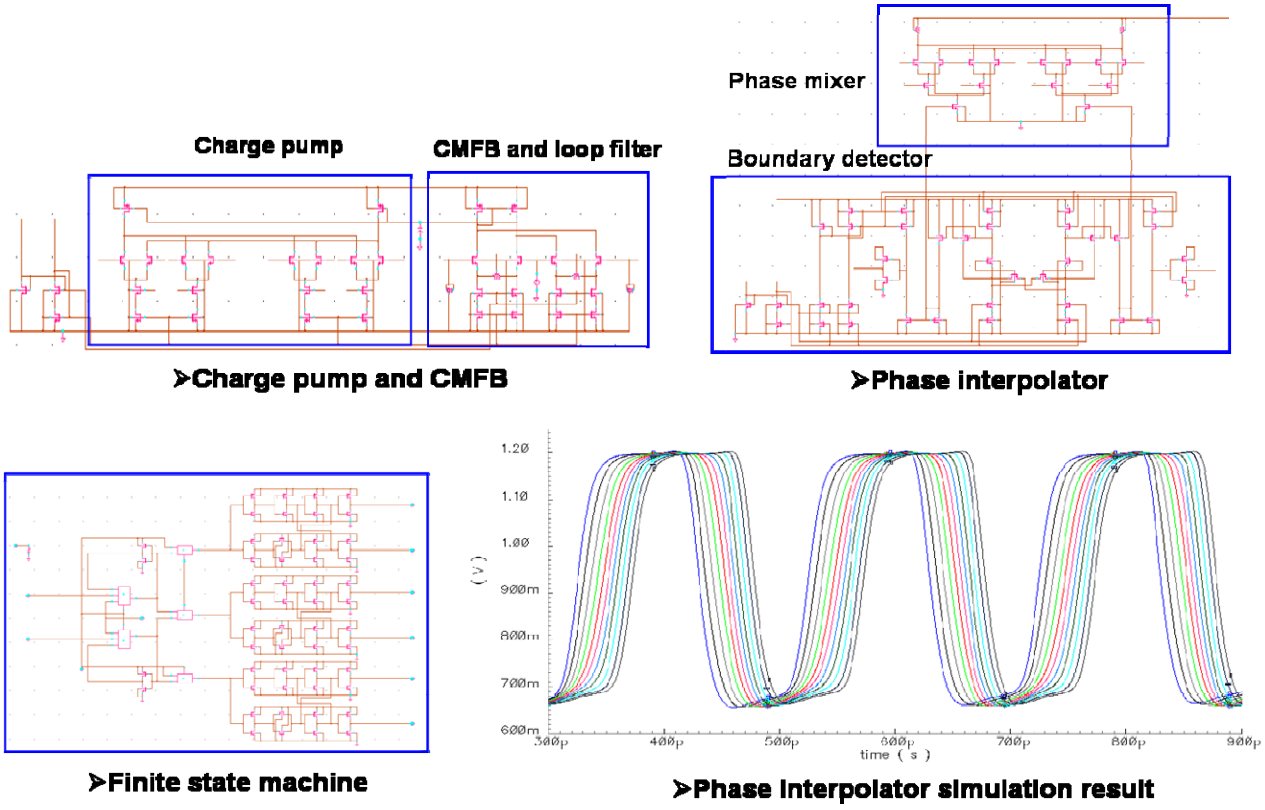
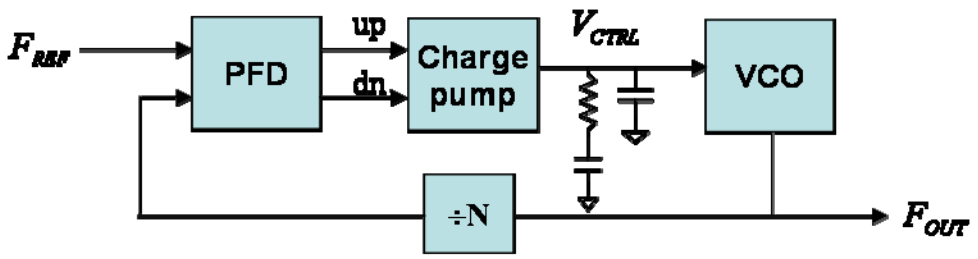


Figure C-10. DLL schematic and phase interpolator simulation result.

C.5 Wide Tuning Range Phase-Locked Loop (PLL)

The PLL is a phase feedback system that compares the output phase with the input phase. The main difference between PLL and DLL is that PLL can multiply the input frequency. Figure C-11 shows the divide by N PLL block diagram.



$$F_{OUT} = NF_{REF}$$

Figure C-11. Divide by N PLL.

One of the key requirement in high speed serial interface testing is to support multiple and simultaneous interfaces on a single device and to operate over a wide range of data rates [C.4]. The using of wide frequency tuning range PLL allows to characterize chip-package-board interface at different frequencies. It is possible to get high frequency clock signals directly from an external clock source, but it's very hard to keep the clock quality up to the die because of PCB and package. This is the same reason why transmitted signals get distorted as they go through the package and PCB. Therefore, it's better to generate an on-chip clean clock inside the die by using the clock multiplication property of a PLL since the PLL has jitter suppression capability. This also allows one to use low cost external clock sources and characterize multiple I/O interface standards with a single device. In order to generate multiple clock frequency through the PLL, there can be two possible choices, one of which is to use multiple VCOs and the other one is to use a wide tuning range VCO. In this research, the author decided to go with wide tuning range VCO because it reduces the area and power consumption. Low supply voltage such

as the one in this design causes the realizable control voltage range to shrink to a very small value and so the VCO gain has to be as high as a few tens of GHz/V. Keeping the VCO gain small is important for noise performance because high VCO gain is detrimental to jitter, as it accentuates the effects of the noise on the control voltage. In this design, the dual path approach [C.5] is used to meet those two requirements. The basic idea of dual path approach is to split up the loop filter in two paths, one of which is coarse tuning path and the second of which is fine tuning path. Figure C-12 shows the wide tuning range PLL which covers 2.5G, 5G and 10GHz on-chip clock.

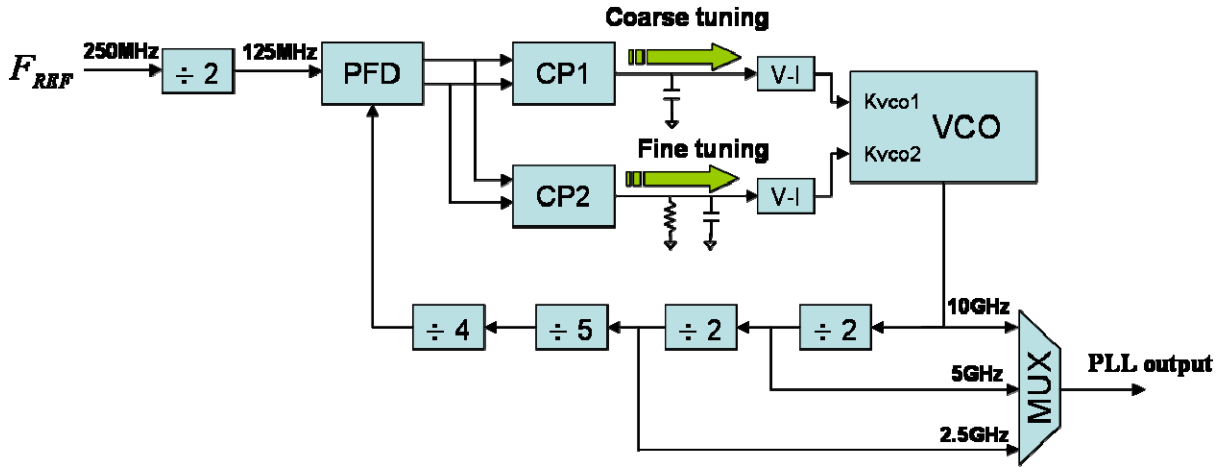


Figure C-12. Wide tuning range PLL.

A coarse tuning path provides the large tuning range, but the loop filter has one dc pole which means the bandwidth is extremely small. So, any high frequency noise cannot affect the VCO through this path even if VCO gain is high. In loop dynamic perspective, static phase offset $[\phi_{err}(S)]_{s=0}$ is locked through this path and dynamic phase offset $[\phi_{err}(S)]_{s\neq 0}$ is tracked by the fine tuning path. Therefore, the loop dynamics is totally determined by fine tuning path. The small VCO gain of fast path makes the VCO to be insensitive to the noise even if there is a large loop bandwidth. Another big advantage of dual path PLL is that it reduces loop filter component

size. The capacitance value in coarse tuning path is B times lower than conventional charge pump PLL. The principle is explained in Figure C-13. In conventional charge pump PLL, the passive loop filter consisting of R_z, C_z and C_p actually forms a pole at zero frequency, a zero at ω_z and another pole at ω_p. It is the capacitor creating the zero that has the largest size and hence poses difficulties in integration. In the dual path PLL, the same filter characteristic is achieved by combining two signals, which does not need an actual RC combination at zero frequency. The goal is to add two signals, which is called V_z and V_p. The first signal is integrated version of the input current. So it has a pole at zero frequency

$$V_z = \frac{1}{sC_z} I_{pump}$$

The other signal path has a low pass transfer function

$$V_p = \frac{1}{1 + sR_pC_p} BI_{pump}$$

These two signals are added to form the complete output signal. This results in

$$V_{out} = V_z + V_p = \frac{1}{sC_z} \frac{1 + s\tau_z}{1 + s\tau_p} I_{pump}$$

with $\tau_z = R_p(C_p + BC_z) \approx BR_pC_z$ and $\tau_p = R_pC_p$.

So a large time constant (or a low frequency) is realized for the filter zero without the requirement for a large capacitor, as τ_z profits from the multiplication by the factor B. Therefore, there are two advantages of dual path approach in contrast to the conventional charge pump, which is jitter suppression through the small VCO gain and component size relaxation of loop filter capacitor. Figure C-14 is the schematic of PLL. Ring oscillator based VCO has been chosen to get wide tuning range. The basic cell of VCO circuit is based on CML buffer stage

with variable negative resistance load [C.6]. The folded cascode V-I converter is used to maintain constant voltage swing for varying currents. Figure C-15 shows the VCO gain curves and loop filter components for fine control and coarse control path. In this design, loop band width was chosen to be 6.25MHz which is 1/20 of reference frequency. The dual path approach reduces the loop filter capacitor C_z by 12 times smaller than when conventional type 2 charge pump PLL is used.

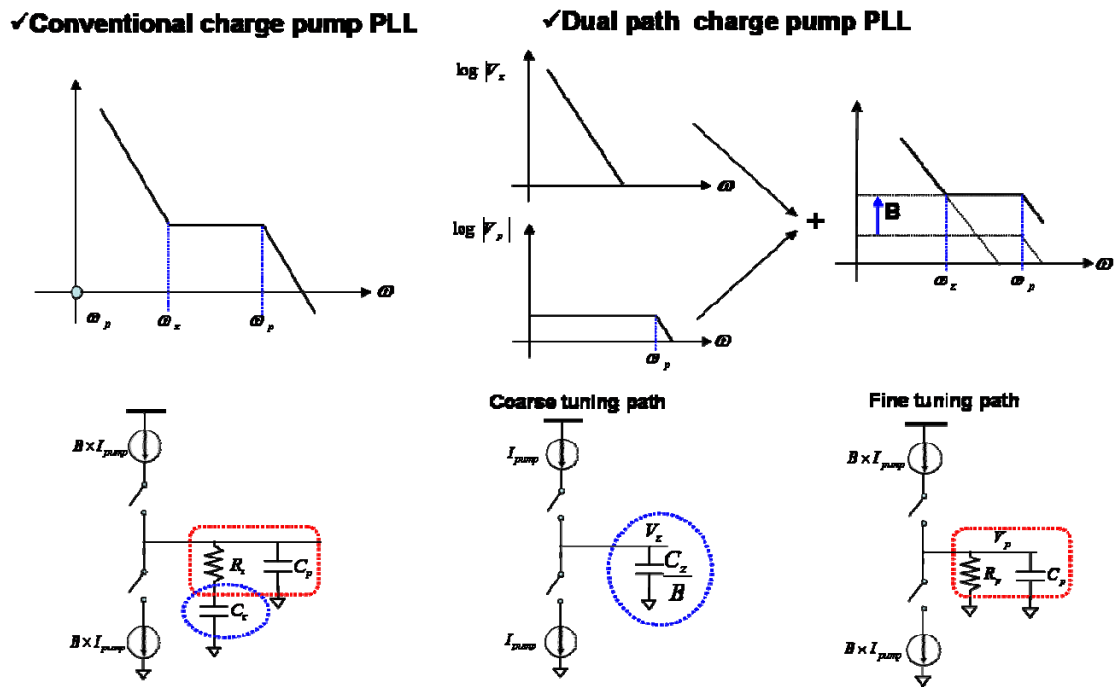


Figure C-13. The principle of dual path charge pump PLL.

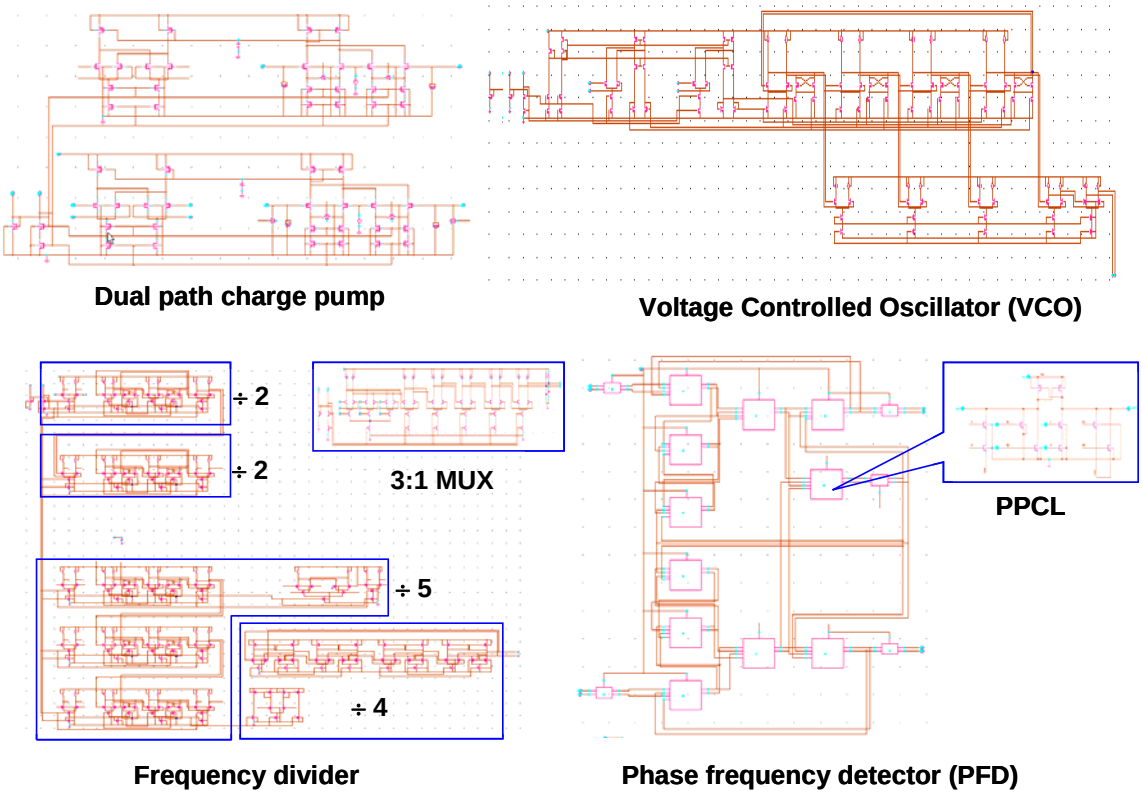


Figure C-14. Schematic of wide tuning range PLL.

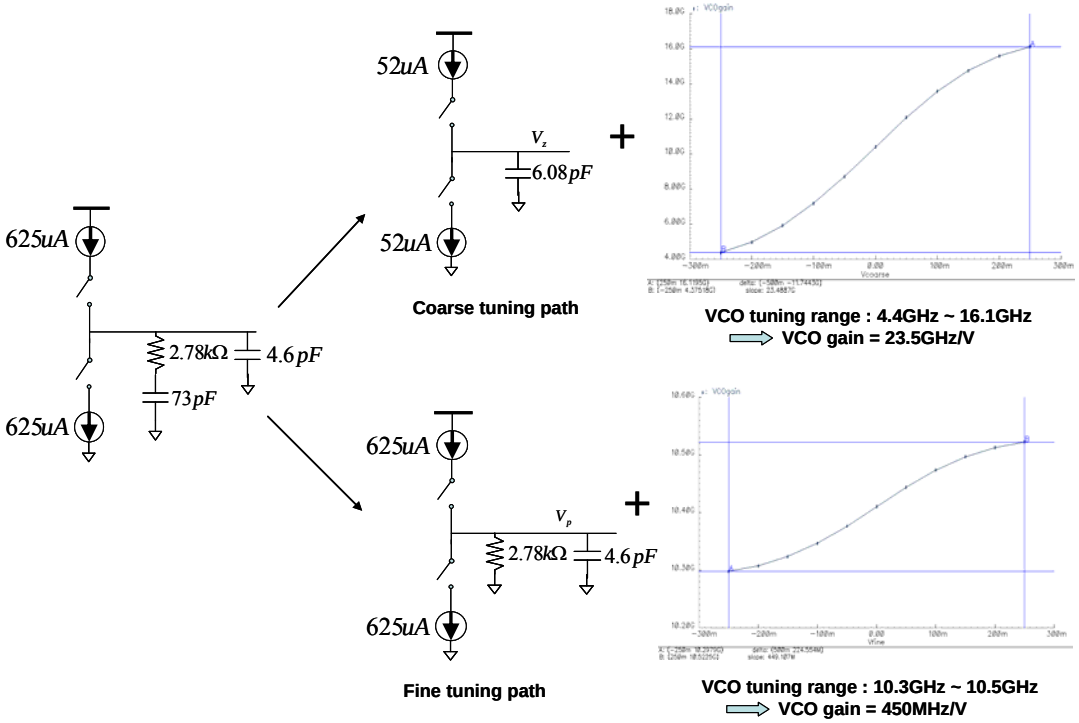


Figure C-15. VCO gain curves and loop filter components.

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