MOSFET PIEZORESISTANCE COEFFICIENTS ON (100) SILICON

By

NIDHI MOHTA

A THESIS PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE

UNIVERSITY OF FLORIDA

2006
ACKNOWLEDGMENTS

I would like to thank my advisor, Dr. Scott E. Thompson, for all the support, encouragement and assistance he has given me throughout my graduate studies, and for the opportunity to work with him in the SWAMP group. Despite being really busy, he always found time for his students to discuss research and other technical deliberations. I will always adore his innovative thinking and diligent commitment to research, which I tried to imbibe during my work tenure. I will be ever grateful to Dr. Thompson for encouraging me to take up an internship with the Process Technology team at Intel, while still working on my thesis. His advice has been valuable in helping my make a sound career decision. I am also very thankful to Dr. Toshikazu Nishida and Dr. William R. Eisenstadt for supporting my research activities and for their guidance and support as my supervisory committee.

I would like to thank the SWAMP group and all its members for their warm support during my research. I appreciate the efforts of Teresa Stevens for being an excellent program assistant. I thank Guangyu Sun for being a friend and source of inspiration when I first joined the group. I would like to thank Min Chu, Andrew Koehler, Umamaheshwari Aghoram, Sagar Suthram, Ji Song Lim, Xiaodong Yang, Youngsung Choi, Kehuey Wu, Xiaoliang Lu and Nirav Shah for all the research related discussions they’ve always found time for. We’ve spent many a long night in the lab trying to finish homework and prepare for quizzes, and getting into long discussions on research and life in general. I thank them for being good friends and for creating an enjoyable work environment over the years. I thank Ashok Verma for his love, support, patience, encouragement and his unwavering belief in me, like I believe in him. There has never been a single course or research related question of mine he has not tried to understand and answer to his best despite being so busy with his PhD research. My time at the university would not be
complete without Swasti Mishra, who has been an incredibly understanding roommate and
caring friend.

During my internship at Intel, I had an opportunity to work with state-of-the-art process
technologies and learn a lot of new, exciting things. I thank the Process Technology and
Collateral team in Folsom team and especially Kirupa Pushparaj for being a great industry
mentor and supporting me with my thesis writing while balancing a busy schedule at work. I
thank my loving parents, my brother Varun, and each member of my family, without whose
support and motivation, my achievements would have been incomplete. I owe by being here to
them. I would also like to thank all my friends, colleagues and teachers in the United States, and
back home, for their overwhelming love and trust in my efforts, and for making me believe in
myself.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACKNOWLEDGMENTS</td>
<td>3</td>
</tr>
<tr>
<td>LIST OF TABLES</td>
<td>7</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>8</td>
</tr>
<tr>
<td>ABSTRACT</td>
<td>11</td>
</tr>
<tr>
<td><strong>CHAPTER</strong></td>
<td></td>
</tr>
<tr>
<td><strong>1</strong> INTRODUCTION</td>
<td>13</td>
</tr>
<tr>
<td>Introduction</td>
<td>13</td>
</tr>
<tr>
<td>Stress and Strain</td>
<td>13</td>
</tr>
<tr>
<td>Future Scalability of Strain</td>
<td>17</td>
</tr>
<tr>
<td>Focus and Organization of the Thesis</td>
<td>18</td>
</tr>
<tr>
<td>Summary</td>
<td>20</td>
</tr>
<tr>
<td><strong>2</strong> STAINED SILICON MODELING AND PIEZORESISTANCE</td>
<td>23</td>
</tr>
<tr>
<td>Introduction</td>
<td>23</td>
</tr>
<tr>
<td>Strained Si Modeling and Need for Piezoresistance Coefficients</td>
<td>23</td>
</tr>
<tr>
<td>Definition of Piezoresistance Coefficients</td>
<td>24</td>
</tr>
<tr>
<td>Relation between Strained Silicon CMOS and Piezoresistance Effect</td>
<td>25</td>
</tr>
<tr>
<td>Graphical Representation of Piezoresistance Coefficients – Definition</td>
<td>27</td>
</tr>
<tr>
<td>Longitudinal and Transverse Piezoresistance Coefficients</td>
<td>28</td>
</tr>
<tr>
<td>Summary</td>
<td>28</td>
</tr>
<tr>
<td><strong>3</strong> STRAIN EFFECTS ON THE VALENCE AND CONDUCTION BAND</td>
<td>31</td>
</tr>
<tr>
<td>Physics of Strained Silicon</td>
<td>31</td>
</tr>
<tr>
<td>Electron Transport</td>
<td>31</td>
</tr>
<tr>
<td>Hole Transport</td>
<td>33</td>
</tr>
<tr>
<td>Importance of a Larger Out-of-Plane Mass for the Top versus Second Band</td>
<td>34</td>
</tr>
<tr>
<td>State-of-the-Art Strain Technologies</td>
<td>35</td>
</tr>
<tr>
<td>Summary</td>
<td>38</td>
</tr>
<tr>
<td><strong>4</strong> WAFER BENDING EXPERIMENT AND MOBILITY ENHANCEMENT EXTRACTION ON</td>
<td>44</td>
</tr>
<tr>
<td>STRAINED SILICON MOSFETS</td>
<td></td>
</tr>
<tr>
<td>Wafer Bending Experiments on MOSFETs</td>
<td>44</td>
</tr>
<tr>
<td>Uniaxial Stress: Four-Point Bending Apparatus Illustration</td>
<td>45</td>
</tr>
<tr>
<td>Biaxial Stress: Concentric-Ring Bending Apparatus</td>
<td>48</td>
</tr>
<tr>
<td>Error Analysis</td>
<td>49</td>
</tr>
</tbody>
</table>
# LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Elastic stiffness and compliance coefficients for Si.</td>
<td>21</td>
</tr>
<tr>
<td>5-1</td>
<td>Measured long channel p-MOSFET piezoresistance coefficients in this work (in blue) compared against other works and against Smith’s [Smi52] bulk data in units of 10^{-12} cm²/dyne. The data in blue refers to this work.</td>
<td>79</td>
</tr>
<tr>
<td>5-2</td>
<td>Measured long channel n-MOSFET piezoresistance coefficients in this work (in blue) compared against other works and against Smith’s [Smi52] bulk data in units of 10^{-12} cm²/dyne.</td>
<td>80</td>
</tr>
<tr>
<td>5-3</td>
<td>Measured long channel n-MOSFET piezoresistance coefficients along [100] channel compared against a) bulk pi-coefficients measured on an n-type resistor on the same process and b) against Smith’s [Smi52] bulk data in units of 10^{-12} cm²/dyne.</td>
<td>81</td>
</tr>
<tr>
<td>5-4</td>
<td>Measured stress types needed for enhancing n/pMOSFET currents.</td>
<td>81</td>
</tr>
</tbody>
</table>
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Stress components acting on an infinitesimal cubic element [Ran05].</td>
<td>22</td>
</tr>
<tr>
<td>2-1</td>
<td>Illustration of the definitions of longitudinal and transverse stress (Adopted from [Klo94])</td>
<td>30</td>
</tr>
<tr>
<td>3-1</td>
<td>MOSFET schematic device cross section (standard orientation)</td>
<td>39</td>
</tr>
<tr>
<td>3-2</td>
<td>Ellipsoids of constant electron energy in reciprocal (“k”) space each corresponding to one of the degenerate conduction band valleys. a) For this case, the four orange colored valleys are in the plane of the silicon and the two green colored valleys are out of the plane. b) Energy level at the bottom of the six conduction band valleys. Application of advantageous strain splits the energy level as shown, removing the degeneracy (i.e the equivalence in energy) between the $\Delta_2$ and $\Delta_4$ valleys.</td>
<td>39</td>
</tr>
<tr>
<td>3-3</td>
<td>Hole constant energy surfaces obtained from 6 band kp calculations for common types of stresses (a) unstressed, (b) longitudinal compression on (100) wafer, (c) longitudinal compression on (110) wafer, (d) biaxial tension.</td>
<td>40</td>
</tr>
<tr>
<td>3-4</td>
<td>Simplified schematic of the hole intervalley phonon scattering process. High stress and splitting larger than the optical phonon energy (60meV) are required to suppress scattering.</td>
<td>40</td>
</tr>
<tr>
<td>3-5</td>
<td>Simplified valence band energy vs. k diagram for strained silicon under longitudinal uniaxial compression and biaxial tension.</td>
<td>41</td>
</tr>
<tr>
<td>3-6</td>
<td>Simplified schematic of valence band splitting of strained Si as a function of gate overdrive.</td>
<td>41</td>
</tr>
<tr>
<td>3-7</td>
<td>Schematic diagram of the biaxially strained-Si MOSFET on relaxed Si$_{1-x}$Ge$_x$ layer. (Adopted from [Mey04])</td>
<td>42</td>
</tr>
<tr>
<td>3-8</td>
<td>Strained Si p-channel MOSFET a) process flow, b) TEM cross sectional view</td>
<td>42</td>
</tr>
<tr>
<td>3-9</td>
<td>Dual stress liner process architecture with tensile and compressive silicon nitride capping layers over NMOS and PMOS.</td>
<td>43</td>
</tr>
<tr>
<td>4-1</td>
<td>Illustration of Si channel orientation a) Si (001) surface, b) MOSFET schematic device cross section [100] channel orientation</td>
<td>55</td>
</tr>
<tr>
<td>4-2</td>
<td>The apparatus, jig, used to apply uniaxial stress to the substrate. (a) In this picture, uniaxial compressive and tensile stresses are generated on the upper and lower surfaces of the substrate respectively. (b) Illustration of calculating the uniaxial stress on a bent substrate. The substrate is simply supported. Four loads applied by cylinders are approximated by four point forces, $P$. The deflection at any point on the</td>
<td></td>
</tr>
</tbody>
</table>
upper surface is designated by \( y(x) \). (c) When the parallel ridges are closer on plate A, and farther apart on plate B uniaxial compression is applied. The reverse is true for uniaxial tension. .................................................................56

4-3 The apparatus, jig, used to apply biaxial stress to the substrate. In this picture, biaxial compressive and tensile stresses are generated on the upper and lower surfaces of the substrate respectively. Illustration of simulating biaxial stress on a bending plate (substrate). The plate (substrate) is simply supported. The deflection at any point on the upper surface is designated by \( w(r) \). ...........................................................................................................57

4-4 Finite element analysis simulation of the bending plate (substrate) [Kwu05]. (a) The radial stresses at the center of the top, middle, and bottom planes of the bending plate vs. the displacement of the smaller ring are shown. (b) Illustration of top, middle, and bottom planes of the plate. ..........................................................................................58

4-5 Snapshot of the \( I_{DS}-V_{GS} \) characteristic and threshold voltage/transconductance extraction from Keithley 4200SCS Semiconductor Parameter Analyzer........................................59

5-1 Si channel orientation, (001) surface and MOSFET schematic device cross section [100] channel orientation. .................................................................................................70

5-2 Mobility enhancement vs. stress for six kinds of stresses, biaxial tensile and compressive and uniaxial longitudinal and transverse, tensile and compressive along [110] channel direction. [Kwu05]. The mobility enhancements are extracted at 0.7MV/cm. The solid lines are the model predictions: blue: [Kwu05], orange: Wang et al. [Wan03]. The symbols are experimental data: blue circle: [Kwu05], green triangle: Thompson et al. [Tho04], orange diamond: Wang et al. [Wan04], and purple square: Gallon et al. [Gal04]...................................................................................71

5-3 \( \pi \) coefficient of p-MOSFETS vs. stress, including longitudinal and transverse \( \pi \) coefficients for [110] direction and transverse \( \pi \) coefficient for [001] direction from an earlier work[Kwu05]. The solid lines are the model predictions: blue: [Kwu05], orange: Wang et al. [Wan04]. The symbols are experimental data: blue circle: this work, green triangle: Smith [20], orange diamond: Wang et al. [Wan04], and purple square: Gallon et al. [Gal04]..............................................................................................72

5-4 Effect of Uniaxial Longitudinal Tensile stress on Bulk n-type resistor and NMOSFETs (indicated as surface tension) oriented along [100] direction on (001) Si ..................73

5-5 Effect of Uniaxial Transverse Tensile stress on Bulk n-type resistor and n-MOSFETs (indicated as surface tension) oriented along [100] direction on (001) Si ..................73

5-6 Effect of Biaxial Tensile and Compressive stress on and n-and p-MOSFETs oriented along [100] direction on (001) Si...............................................................74

5-7 (100) Surface Piezoresistance coefficient vs. bulk Piezoresistance coefficients (a) nMOSFET (b) pMOSFET. Thicker lines indicate the surface value and thinner lines denote the bulk value. Solid lines are longitudinal piezoresistance coefficients and
dashed lines are transverse piezoresistance coefficients. (Courtesy: Chu, Min)
[Tho06] ...................................................................................................................................75

5-8 Constant energy contour for bulk Hole constant-energy band surfaces for the top band obtained from six-band $k \cdot p$ calculations for common types of 1-GPa stresses: (a) unstressed, (b) biaxial tension, (c) longitudinal compression on (001) wafer, and (d) longitudinal compression on (110) wafer (note significant differences in stress induced band warping altering the effective mass). [Tho06] ........................................................................76

5-9 Illustration of mobility enhancement due to band shift for (100) / [100] NMOS under transverse tensile stress. ......................................................................................................................................77

5-10 Band shift for (100) / <110> longitudinal tensile stress. ..................................................................................................................78
Abstract of Thesis Presented to the Graduate School
of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Master of Science

MOSFET PIEZORESISTANCE COEFFICIENTS ON (100) SILICON

By
Nidhi Mohta

December 2006

Chair: Scott E. Thompson
Major Department: Electrical and Computer Engineering

Simple MOSFET geometric scaling has driven the industry to date but as the transistor
gate length drops to 35 nm and the gate oxide thickness to ~1 nm, physical limitations such as
off-state leakage current and power density make geometric scaling an increasingly challenging
task. In order to extend Moore’s law, process-induced strain has emerged as the new scaling
vector for industry. The strain effects are characterized by a combination of band structure
alteration, effective mass changes, band splitting, and hole repopulation. Piezoresistance
coefficients are used as a metric to explain the performance improvement of devices under stress.

This thesis is an experimental study of piezoresistance effects in both n and p-type silicon
and mobility enhancement in strained silicon Metal Oxide Semiconductor Field Effect
Transistors (MOSFETs). Four-point and concentric-ring wafer bending experiments are used to
apply external stresses to the MOSFET devices. Mobility enhancement and hence device-level
piezoresistance coefficients have been extracted by applying uniaxial and biaxial mechanical
stress on (100) MOSFETs to benchmark with conventional bulk piezoresistance coefficients,
where (100) denotes the substrate orientation of silicon. A study of piezoresistance coefficients
measured on different channel orientations and both (100) and (110) silicon surfaces is
presented. Piezoresistance measured on a (100) surface for MOSFETs oriented along the [100]
channel direction has been reported for the first time. The data in this study indicates that: (1) uniaxial transverse stress for nMOSFETs in the [100] direction results in increased mobility (2) an almost constant drive current is observed for pMOSFETs along a [100] channel direction on (100) wafer. (3) in the out-of-plane direction, compressive stress is a better for pMOSFETs current enhancement, rather than tensile stress. A simple qualitative argument for this difference is presented by investigating the effect of the surface electric field on carrier mobility under stress. It is shown that 2-D quantization in the inversion layer results in the MOSFET piezoresistance coefficients to be different from the bulk piezoresistance coefficients. These device-level piezoresistance coefficients study provides a guideline for performing aggressive strain engineering on MOSFETs.
Strain is today a widely accepted technique of enhancing transistor performance, especially when we are scaling down to nanometer dimensions. This thesis is a study of MOSFET piezoresistance coefficients which is an important parameter to quantify mobility enhancement due to strained silicon. For the past 4 decades, geometric scaling of silicon CMOS transistors has enabled not only an exponential increase in circuit integration density — Moore's Law — but also a corresponding enhancement in the transistor performance itself. Simple MOSFET geometric scaling has driven the industry to date but as the transistor gate length drops to 35 nm [Cha03], [Bai04], [Chi04] and the gate oxide thickness to ~1 nm, physical limitations such as off-state leakage current and power density make geometric scaling an increasingly challenging task. Also, thin oxide results in high electric field in the channel. This results in a reduction of carrier mobility together with high channel doping. In order to continue CMOS device scaling and historical performance improvement trends, the industry needs a new scaling vector. Starting at the 90 nm technology generation, mobility enhancement through uniaxial process induced strained silicon has emerged as the next scaling vector being widely adopted in logic technologies [Cha03], [Chi04], [Tho04]. The mobility enhancement results from strain fundamentally altering the electronic band structure of silicon.

**Stress and Strain**

Since the thesis is primarily concentrated around stress and strain in MOSFETs, it is essential to understand the basics of engineering mechanics like stress, strain and mechanical properties. When a force is applied on a fixed body, it deforms in its shape. If the deformation is small enough, it returns to its original shape once the applied force is removed. This is described
as the linear elastic behavior of the body and the deformation is considered to be within the elastic limit. Stress ($\sigma$) is defined as force per unit area $\Delta A$ acting on the surface of a solid. Its unit is Pascal (Pa).

$$\sigma = \lim_{A \to 0} \frac{F}{A} \quad (1-1)$$

Any stress on an isotropic solid body can be expressed as a stress matrix $\sigma$ in a cartesian coordinate system as a 3x3 matrix, (Equation 1-2)

$$\sigma = \begin{pmatrix}
\chi_{xx} & \kappa_{xy} & \kappa_{xz} \\
\kappa_{yx} & \chi_{yy} & \kappa_{yz} \\
\kappa_{zx} & \kappa_{zy} & \chi_{zz}
\end{pmatrix} \quad (1-2)$$

The stress matrix is symmetric with $\kappa_{xy} = \kappa_{yx}$ and the 3x3 matrix can be simplified into the 6 x 1 stress vector below:

$$\sigma = \begin{pmatrix}
\chi_{xx} \\
\chi_{yy} \\
\chi_{zz} \\
\kappa_{yz} \\
\kappa_{zx} \\
\kappa_{xy}
\end{pmatrix} \quad (1-3)$$

Stress is a vector which has two components: normal and shear component.

**Normal or Hydrostatic Stress**: Force per unit area, acting normal to the area is called the normal stress ‘$\chi$’.

**Shear Stress**: Force per unit area, acting tangential to area, i.e. along the plane of the surface, is called the shear stress ‘$\kappa$’. As a rule of thumb, tensile stresses are considered positive and compressive stresses as negative.
To understand the stresses and strains in depth, consider an infinitesimal cube as shown in Figure 1-1. The figure shows normal and shear stresses in x, y and z directions acting on different planes of the cube. The first subscript identifies the face on which the stress is acting, and the second subscript identifies the direction. The \( \chi_{ii} \) components are the normal stresses while the \( \kappa_{ij} \) components are the shear stresses.

Strain \( \varepsilon \) is defined as change in length of an object under force, compared to its original length. It is a unit less quantity. Normal strain is the relative lattice constant change.

\[
\varepsilon = \frac{a - a_0}{a_0}
\]  
(1-4)

where \( a_0 \) and \( a \) is the lattice constant before and after strain respectively.

Similar to stress, strain also can be represented as a 6x1 matrix, as is shown in Equation 1-5.

\[
\varepsilon = \begin{bmatrix}
\varepsilon_{xx} \\
\varepsilon_{yy} \\
\varepsilon_{zz} \\
2 \varepsilon_{yz} \\
2 \varepsilon_{zx} \\
2 \varepsilon_{xy}
\end{bmatrix}
\]  
(1-5)

Poisson ratio \( \nu \), one more important property of the material, is the ratio of lateral contraction strain to longitudinal extension strain in the direction of the tensile stress. Stress and strain are related to each other by the material property called Young’s Modulus ‘C’ as \( C = \frac{\sigma}{\varepsilon} \). Hence, the Young’s modulus defines the stiffness of the material. The relationship between stress and strain in terms of stiffness coefficients is shown in Equation 1-6.
\[
\begin{pmatrix}
\chi_{xx} \\
\chi_{yy} \\
\chi_{zz} \\
\kappa_{yz} \\
\kappa_{zx} \\
\kappa_{xy}
\end{pmatrix} = \begin{pmatrix}
C_{11} & C_{12} & C_{12} & 0 & 0 & 0 \\
C_{12} & C_{11} & C_{12} & 0 & 0 & 0 \\
C_{12} & C_{12} & C_{12} & 0 & 0 & 0 \\
0 & 0 & 0 & C_{44} & 0 & 0 \\
0 & 0 & 0 & 0 & C_{44} & 0 \\
0 & 0 & 0 & 0 & 0 & C_{44}
\end{pmatrix} \begin{pmatrix}
\varepsilon_{xx} \\
\varepsilon_{yy} \\
\varepsilon_{zz} \\
2\varepsilon_{yz} \\
2\varepsilon_{zx} \\
2\varepsilon_{xy}
\end{pmatrix}
\]

(1-6)

where the coefficients $C_{11}$, $C_{12}$ and $C_{44}$ are constant for a given material. Reversibly, the relation can be also be expressed as $S = \frac{\varepsilon}{\sigma}$, where $S$ gives the compliance coefficients of the given material. Table 1-1 shows the values of stiffness and compliance coefficients for silicon.

**Motivation**

Device level piezoresistance coefficients are of great value to device and process engineers in evaluating the types of process-induced stress than can contribute to mobility enhancement which in turn improves transistor performance. Different types of stress are required for device mobility enhancement as indicated from Si bulk piezoresistance coefficients [Smi52]. For channel direction [110], longitudinal tensile and out-of-plane compressive stress for nMOSFETs and longitudinal compressive stress for pMOSFETs are used [Tho04]. However, some characteristics of strained devices cannot be explained by the bulk piezoresistance coefficients. Also, there isn’t enough published data on the piezoresistance observed along strained [100] channel devices. In this work, upon application of uniaxial transverse stress on a [100] nMOSFET it is observed that surface and bulk piezoresistance values not only differ in magnitude but also in sign. However, based on the previous bulk Si piezoresistance coefficients [Smi52], there is actually mobility degradation observed on the nMOSFETs. Also this work reports the best-fit piezoresistance coefficient $\pi_L$ of nMOSFET from experiments as $38.55 \times 10^{-16}$.
11Pa-1, which is smaller than 102×10^{-11} Pa^{-1} [Smi52]. Surface longitudinal piezoresistance coefficient for [100] channel is much smaller than bulk value, which means that the <100> channel MOSFETs have smaller mobility enhancement than bulk Si. Therefore, the previously reported bulk piezoresistance coefficients should be modified for strained device engineering. In this work, device-level piezoresistance coefficients were directly extracted from Si n/pMOSFETs by applying uniaxial and biaxial stress in different channel direction on (100) surfaces.

**Future Scalability of Strain**

When pursuing performance features to extend Moore’s law, it is important to consider how the performance enhancement scales as the device feature size is reduced. The classical equations for MOSFET transport for long channel devices show that the drain current is inversely proportional to the channel length.

\[
I_{d(lin)} = \frac{\mu W C_{ox}}{L} \left( V_g - V_t - \frac{V_d}{2} \right) V_d
\]

\[
I_{d(sat)} = \frac{\mu W C_{ox}}{2L} \left( V_g - V_t \right)^2
\]

However as the MOSFET carrier transport becomes ballistic, the carrier transport can best be described by carrier injection at the source [Lun02]. The drain current in saturation, \( I_d \) is given by

\[
I_{d(sat)} = W C_{ox} < \nu(0) > \left( V_g - V_t \right)
\]

where \( < \nu(0) > \) is the average velocity of carriers at the source and \( C_{ox} \left( V_{gs} - V_t \right) \) is the charge density [Lun02]. In the limit where channel length goes to zero, \( < \nu(0) > \) is the unidirectional thermal velocity \( \nu_T \), since the velocity at the beginning of the channel is set by carriers injected from the thermal equilibrium source [Lun03], \( \nu_T \) is given by
\[ v_r = \sqrt{\frac{2k_BT_L}{e \hbar}} \]  

Thus in the nanoscale channel limit, the drain current becomes

\[ I_d = WC_{\alpha x} \sqrt{\frac{2k_BT_L}{e \hbar}} \left( V_g - V_i \right) \]

From Equation 1-11, it can be seen that strain-induced decrease in the effective mass will still enhance the drive current in ballistic MOSFETs which has been a historical concern for mobility enhancement techniques. This serves as the motivation for this work, as peizoresistivity will be shown as an important parameter in quantifying mobility enhancement through strain.

Furthermore, at higher strain levels than in state-of-the-art production today, reduction in effective mass continues due to increased repopulation of valleys/bands. This phenomenon is even more pronounced for holes. Also, when at higher strain the valence band splitting (~25meV at 100 MPa to ~55meV at 1 GPa) becomes greater than the optical phonon energy, the hole mobility will further be enhanced by a reduction in scattering rate. Experimental and theoretical work suggests much larger mobility enhancement is achievable at higher strain. Ratios of stressed to unstressed mobilities of 4 and 1.7 have been reported experimentally for holes and electrons [Hoy02], respectively. The problem of dislocations in the strained layer at higher levels of strain will have to be addressed by changing thermal cycles and controlling growth.

**Focus and Organization of the Thesis**

This thesis will mainly focus on reporting measured Piezoresistance coefficients of MOSFETS on (100) silicon wafer and oriented along two major crystal axes, [100] and [110] directions. The effect of surface electric field on stress has been explained and incorporated in the piezoresistance model for the first time and as a result, device level piezoresistance coefficients show sharp contrast with bulk piezoresistance first reported by Smith [Smi52].
comparative study will be made with all reported piezoresistance coefficients in literature which can be easily understood and provide quick, accurate predictions for the types of stress that contribute to mobility enhancement in strained-Si MOSFETs. Most of the experimental work has not studied the piezoresistance observed along the [100] direction of n and p type MOSFETs. A simple physical model is developed that provides insight into the physics of mobility enhancement under the combined influence of stress and surface electric field.

Chapter 1 begins with an introduction to the history of strain, definitions and relation between stress and strain. Future scalability of silicon into the ballistic regime is discussed. In chapter 2, a thorough understanding of piezoresistance coefficients is developed and the relationship between strained silicon CMOS and piezoresistance is outlined which serves as the basis for experimental results in the future chapters. In chapter 3, an explanation of the valence and conduction band physics under strain is given. The importance of a large out-of-plane mass for mobility enhancement is explained in detail. This is followed by a discussion of state-of-the-art strained technologies used today and why the industry is adopting uniaxial stress. In Chapter 4, experiments designed to measure piezoresistance are presented. The four-point and concentric-ring wafer bending experiments are used to apply the uniaxial and biaxial stresses respectively. The technique used to extract piezoresistance on bulk n-type silicon resistors has been described. This is followed by a brief discussion on uncertainty and error analysis. The main factor contributing to the linear drain current increase will be identified from analyzing the variables in the linear drain current equation. Chapter 5 discusses the experimental results obtained and the physics behind the observed piezoresistance in detail. The electron and hole mobility and the mobility enhancement are extracted from the drain current in the linear region ($I_{\text{dlin}}$). The mobility enhancement vs. stress will be plotted. The $\pi$ coefficients will then be
calculated from the mobility enhancement vs. stress. The reasoning behind the observed change in magnitude and even sign of the device level piezoresistance coefficients when compared to bulk piezoresistance values is stated. The effect of vertical electrical field on the carrier mobility and splitting in the energy-levels due to inversion layer confinement is explained. Finally, chapter 6 summarizes the thesis and provides recommendation for the future work.

Summary

In this chapter, strain is introduced as a vector to extend Moore’s law and to ensure continual MOSFET performance enhancement. The relation between stress and strain is outlined. This is followed by a discussion on the main motivation behind this work and the focus and organization of this thesis. In the following chapter, a thorough understanding of piezoresistance coefficients is developed and the relationship between strained silicon CMOS and piezoresistance is outlined. This will serves as the basis for experimental results in the future chapters.
Table 1-1. Elastic stiffness and compliance coefficients for Si.

<table>
<thead>
<tr>
<th>Compliance Coefficients (10^{11}N/cm^2)</th>
<th>( C_{11} )</th>
<th>( C_{12} )</th>
<th>( C_{44} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S_{11} )</td>
<td>1.657</td>
<td>0.659</td>
<td>0.7956</td>
</tr>
<tr>
<td>( S_{12} )</td>
<td>0.768</td>
<td>-0.214</td>
<td>1.250</td>
</tr>
<tr>
<td>( S_{44} )</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 1-1. Stress components acting on an infinitesimal cubic element [Ran05].
CHAPTER 2
STRAINED SILICON MODELING AND PIEZORESISTANCE

Introduction

The first section of this chapter introduces the relation between the piezoresistive effect and strained silicon MOSFET. This is followed by a discussion on the piezoresistance coefficients, their need, and relevance to understanding strain-enhanced electron and hole mobility for the industry. The piezoresistive effect arises because silicon is a cubic crystal with anisotropic material properties. As a consequence, stress applied along different directions/surface orientations of silicon results in making the piezoresistance coefficients to be a function of crystal direction and orientation. Appropriate numerical analysis of the effect of MOSFET carrier mobility under stress in terms of piezoresistance coefficients is provided. The technique of extraction of piezoresistance coefficients reported in this work from drive current and mobility enhancement is explained. Finally, the literature to-date on piezoresistance coefficients is briefly reviewed.

Strained Si Modeling and Need for Piezoresistance Coefficients

Many previous works [Wel94], [Nay94],[Fis96],[Tak96] have pointed out that the main factors that affect mobility are:

- the change in the averaged longitudinal effective mass due to relative carrier distribution on different valleys (NMOS) or bands (PMOS);
- the change in intervalley carrier scattering rate due to the energy splitting between different valleys or bands. (More details and insight into the physical mechanism responsible for this mobility enhancement is given in chapter

Historically, it has been difficult to model strain-enhanced mobility due to the uncertainty in the inversion layer scattering parameters [Fis02] [Fis03] [Tak96] and numerical complexity that forces many early approximations during the modeling process. It is possible that using
conventionally accepted scattering parameters, electron and hole mobility enhancements could be under or over predicted [Fis02] [Tak96]. Another example is the field dependence of hole mobility enhancement for uniaxial compression and biaxial tensile stress that was first observed experimentally [Tho04] but not predicted. Experimental data sometimes helps in gaining more insight into a complex physical mechanism than predictive modeling.

Because of these modeling difficulties, the most effective approach at predicting and understanding strain-enhanced electron and hole mobility for the industry has been the empirically measured piezoresistance coefficients [Tho06]. Piezoresistance coefficients are generally measured at low strain and low field, primarily due to the limits imposed by the existing wafer bending set-up which will be discussed later in chapter 4. Additionally, piezoresistance coefficients have the benefit of capturing mobility enhancement primarily resulting from changes in conductivity mass, which will be shown later in this chapter.

**Definition of Piezoresistance Coefficients**

Since C. S Smith [Smi53] first discovered the piezoresistance effect of semiconductors having anisotropic band structures such as silicon 50 years ago, the semiconductors have found applications in pressure and mechanical stress sensors [Kan91]. The piezoresistance effect in strained silicon is defined as the stress-induced resistance change. The exact definition of piezoresistance coefficients can be expressed as Equation 2-1:

\[ \pi = \frac{1}{\chi} \frac{R_\chi - R_0}{R_0} = \frac{1}{\chi} \frac{\Delta R}{R_0} \]  

(2-1)

where, \( R_0 \) and \( R_\chi \) are the unstressed and stressed resistances, \( \chi \) is the uniaxial stress and \( \Delta R \) is the change of resistance under certain stress. Thus, the value of \( \pi \) coefficient is determined by the value of \( \Delta R \) with stress [Klo94]. Since \( R = \rho A / L \) where \( \rho \) is the resistivity,
A is the cross-sectional area, and L is the length; the resistance change may either be due to a combination of resistivity change and/or change in geometry.

Furthermore, the work done in reference [Kan91] explains that the change of resistance is somewhat linearly dependent on stress within the range of our measurement (50-400MPa). The relative change in resistance is given by:

\[ \frac{\Delta R}{R} = \frac{\Delta l}{l} - \frac{\Delta w}{w} - \frac{\Delta t}{t} + \frac{\Delta \rho}{\rho} \]  

(2-2)

where, \( l, w, t \) and \( \rho \) represent the length, width, thickness and resistivity respectively. For a semiconductor, the dimensional change under stress can be neglected for the stresses of interest used in the experiments in this work (<500 MPa) compared to the change of resistivity [Kan91]. Thus, the change in resistance is mainly due to the change of resistivity. Next, we will establish the relation between this piezoresistive effect as seen in a semiconductor with the mobility enhancement resulting from strained silicon MOSFETS.

**Relation between Strained Silicon CMOS and Piezoresistance Effect**

The strain effects responsible for the transduction physics of micromachined piezoresistive sensors is closely related to mobility enhancement in strained silicon CMOS [Kwu05]. The strain effect on the valence and conduction band of silicon can be used to explain and quantify the piezoresistance effect in n and p-type strained silicon as well as the electron and hole mobility enhancement in strained-Si MOSFETs. The stress-strain relationship has been explored in chapter.

From equation (2-2), it follows that the \( \pi \) coefficient may be expressed in terms of resistivity change or conversely in terms of conductivity change as follows:

\[ \pi = \frac{1}{\chi} \frac{\Delta R}{R_0} = \frac{1}{\chi} \frac{\Delta \rho}{\rho_0} = -\frac{1}{\chi} \frac{\Delta \sigma}{\sigma_0} \]  

(2-3)
The resistivity of a semiconductor can be expressed as Equation 2-4:

\[
\rho = \frac{1}{q\mu_n n + q\mu_p p}
\]  

(2-4)

where, \(\rho\) and \(\sigma\) are the resistivity and conductivity respectively and \(q\), \(\mu_n\) and \(\mu_p\) are electron charge, electron mobility and hole mobility respectively. The electron and hole concentration are represented by \(n\) and \(p\) respectively. This conductivity change is directly related to mobility change since \(\sigma = q \mu p\) where \(q\) is the electronic charge, \(\mu_{n,p}\) is the electron and hole mobility, \(p\) is the hole concentration and \(n\) is the electron concentration. Hence, assuming that for a certain semiconductor under steady state \(n\) and \(p\) are constant, it can be concluded that piezoresistance coefficients are mainly determined by the change in carrier mobility with stress. The effect of mechanical stress on mobility can be developed by the following equations.

Under uniaxial stress, the normalized mobility variations reduce to [Bra01]

\[
\frac{\Delta \mu}{\mu} \parallel = \left( \frac{\Pi_5 + \Pi_{44}}{2} \right) \sigma
\]

(2-5)

\[
\frac{\Delta \mu}{\mu} \perp = \left( \frac{\Pi_5 - \Pi_{44}}{2} \right) \sigma
\]

(2-6)

where, \(\Pi_s = \Pi_{11} + \Pi_{12}\). Hence, we can reduce equations (2-5) and (2-6) to get an expression for mobility under stress as [Tho06]

\[
\frac{\Delta \mu}{\mu} \approx \left| \Pi_\parallel \sigma_\parallel + \Pi_\perp \sigma_\perp \right|
\]

(2-7)

where the subscripts \(\parallel\) and \(\perp\) refer to the directions parallel and transverse to the current flow in the plane of the MOSFETs, \(\frac{\Delta \mu}{\mu}\) is the fractional change in mobility, \(\sigma_\parallel\) and \(\sigma_\perp\) are the
longitudinal and transverse stresses and \( \pi \parallel \) and \( \pi \perp \) are the piezoresistance coefficients expressed in Pa\(^{-1}\) or 10\(^{-12}\) cm\(^2\)/dyne.

Two types of uniaxial stresses are defined in Figure 2-1 in order to distinguish the two kinds of \( \pi \) coefficients, longitudinal and transverse [Klo94]. Longitudinal stress implies it means that the uniaxial stress, electric field, and electric current are all in the same direction. Transverse stress implied that the electric field is parallel to the electric current but normal to the applied uniaxial stress. This is illustrated in more detail in Figure 2-1.

**Graphical Representation of Piezoresistance Coefficients – Definition of Surface Longitudinal and Transverse Piezoresistance Coefficients**

Yozo Kanda [Kan82] plotted the bulk longitudinal and transverse piezoresistance coefficients as a function of the crystal directions for orientations in the (100), (110), (211) planes. In this way, the value of piezoresistance coefficient for different channel directions can be seen clearly and can be compared directly. The method of generating surface piezoresistance coefficients is the same while the process is slight different from that introduced in [Kan82]. In crystal with cubic symmetry, such as Si and Ge, the bulk \( \pi \) coefficient tensor is given by

\[
\begin{bmatrix}
  \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\
  \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\
  \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\
  0 & 0 & 0 & \pi_{44} & 0 & 0 \\
  0 & 0 & 0 & 0 & \pi_{44} & 0 \\
  0 & 0 & 0 & 0 & 0 & \pi_{44} \\
\end{bmatrix}
\]  
(2-8)

The tensor is used to calculate the longitudinal and transverse piezoresistance coefficient for any arbitrary direction as shown below [Kan82]

\[
\pi_{\parallel} = \pi_{11} - 2(\pi_{11} - \pi_{12} - \pi_{44})(l_1^2m_1^2 + m_1^2n_1^2 + n_1^2l_1^2) 
\]  
(2-9)

\[
\pi_{\perp} = \pi_{12} + (\pi_{11} - \pi_{12} - \pi_{44})(l_1^2t_1^2 + m_1^2m_3^2 + n_1^2n_3^2) 
\]  
(2-10)
For the calculation of surface piezoresistance coefficient, the symmetrical 3-D tensor was not used, instead a 2-D form was used which is applicable to an inversion layer [Col68]

\[
\begin{bmatrix}
\pi_{11} & \pi_{12} & \pi_{14} \\
\pi_{21} & \pi_{22} & \pi_{24} \\
\pi_{41} & \pi_{42} & \pi_{44}
\end{bmatrix}
\]

As the tensor is symmetric, for both (100) and (110) surface of Si, the tensor reduces to [Col68]:

\[
\begin{bmatrix}
\pi_{11} & \pi_{12} & 0 \\
\pi_{21} & \pi_{22} & 0 \\
0 & 0 & \pi_{44}
\end{bmatrix}
\]

For (100) surface, \( \pi_{11} = \pi_{22} \) and \( \pi_{12} = \pi_{21} \)

Using coordinate transformation to find the longitudinal and tranverse piezoresistance coefficient in any arbitrary direction, the final result obtained is shown below

\[
\pi_\ell = \pi_{11} l_1^4 + \pi_{12} l_1^2 m_1^2 + \pi_{21} l_1^2 m_1^2 + \pi_{22} m_1^4 + 2\pi_{44} l_1^2 m_1^2
\]

\[
\pi_t = \pi_{11} l_2^2 l_2^2 + \pi_{12} l_1^2 m_2^2 + \pi_{21} l_1^2 m_2^2 + \pi_{22} m_1^2 m_2^2 + 2\pi_{44} l_1^2 m_1 m_2
\]

where \( \pi_\ell \) is the surface longitudinal piezoresistance coefficient and \( \pi_t \) is the surface transverse piezoresistance coefficient.

It is this difference in bulk and surface coefficients that will lead to some interesting physics about the mobility enhancement in a 2D quantized inversion-layer MOSFET to be presented with the results in chapter 5.

**Summary**

In this chapter, the relation between the piezoresistive effect and strained silicon MOSFET was elaborated, which will serve as a foundation for understanding the experimental results. This was followed by a discussion on the piezoresistance coefficients, their need, and relevance to
understanding strain-enhanced electron and hole mobility for the industry. Appropriate numerical analysis of the effect of MOSFET carrier mobility under stress in terms of piezoresistance coefficients was provided. The technique of extraction of piezoresistance coefficients reported in this work from drive current and mobility enhancement is explained. Finally, the literature to-date on piezoresistance coefficients is briefly reviewed. Chapter 3 discusses the physics of strained silicon, its implications and state-of-the-art strained technologies.
Figure 2-1 Illustration of the definitions of longitudinal and transverse stress (Adopted from [Klo94]).
CHAPTER 3
STRAIN EFFECTS ON THE VALENCE AND CONDUCTION BAND

Physics of Strained Silicon

Strained Si has been studied for 50 years but only recently have some of the subtleties of
carrier transport in a strained 2-dimensional MOSFET inversion layer been fully understood or
possibly appreciated [Wel94], [Nay94], [Tho03], [Fis96]. The carrier mobility is given by

\[ \mu = \frac{q \tau}{m^*} \]  

(3-1)

where \( \tau \) is the scattering rate and \( m^* \) is the conductivity effective mass. Strain achieves
mobility enhancement by the following two primary factors: (a) Reduction in the conductivity
effective mass and (b) Reduction in the scattering rate or (c) a combination of both.

For electrons, both mass and scattering changes are now generally accepted as important
for mobility enhancement [Yua01]. However, for holes, only mass change due to band warping
[Tho03] appears to play a significant role at today’s manufacturable (< 1GPa) stress levels
since strain induced valence band splitting is smaller than for the conduction band. Furthermore,
though there has been much focus on reduced in-plane mass to increase mobility, increasing the
out-of-plane mass for electrons and holes is now understood to be equally important for
maintaining the mobility enhancement at high vertical fields (see Figure 3-1 for definition of in
and out-of-plane). In the next section, electron transport in strained silicon is explained, which is
better understood. This is followed by a discussion on hole transport which until recently
[Tho03] was less understood, but which has some interesting physics with practical implications.

Electron Transport

For electron transport in bulk silicon at room temperature, the conduction band is
comprised of six degenerate valleys as shown in Figure 3-2a. These valleys are of equal energy
as shown by $\Delta 6$ in Figure 3-2b. The degeneracy reflects the cubic symmetry of the silicon lattice. The effective mass for any direction is the reciprocal of the curvature of the electron energy function in that direction. Consequently, the effective mass of each ellipsoid is anisotropic, with the transverse mass (perpendicular to the axis) given by $m_t = 0.19 m_o$ being significantly smaller than the longitudinal mass (parallel to the axis) given by $m_l = 0.98 m_o$, where $m_o$ is the free electron mass. For unstressed bulk silicon, the total electron conductivity mass, $m^*$, is obtained by adding the contributions of the six degenerate valleys and is given by Equation 3-2,

$$m^* = \left[ \frac{1}{6} \left( \frac{2}{m_t} + \frac{4}{m_l} \right) \right]^{-1}$$ \hspace{1cm} (3-2)

For MOSFETs on a (001) wafer, advantageous strain removes the degeneracy between the four in-plane valleys ($\Delta 4$) and the two out-of-plane valleys ($\Delta 2$) by splitting them in energy, as shown in Figure 3-2b. Due to the lower energy of the $\Delta 2$ valleys they are preferentially occupied by electrons. The electron mobility partly improves via a reduced in-plane and increased out-of-plane $m^*$ due to the favorable mass of the $\Delta 2$ valleys resulting in more electrons with an in-plane transverse effective mass ($m_t = 0.19 m_o$) and out-of-plane longitudinal mass ($m_l = 0.98 m_o$). For a given strain, quantifying the effective mass reduction and comparing it to the enhanced mobility shows that mass reduction gain alone explains only part of the mobility enhancement [Tak96]. Hence, electron scattering must also be reduced due to the conduction valleys splitting into two sets of energy levels, which lowers the rate of intervalley phonon scattering between the $\Delta 2$ and $\Delta 4$ valleys. Quantifying the improvement due to scattering has been difficult using acceptable scattering parameters but reduced scattering is still believed to account for the rest of the mobility enhancement [Yua01]. Many types of stress increase the electron mobility via increased
population in the Δ2 valley (in-plane biaxial and uniaxial tensile and out of plane uniaxial compressive stress are some examples).

**Hole Transport**

For holes, the valence band structure of silicon is more complex than the conduction band. It is this complex band structure and valence band warping under strain that results in much larger hole than electron mobility enhancement and the reason strained pMOSFETs are a key focus in advanced logic technologies. The band warping is also responsible for why different types of strain (namely the technologically important biaxial tensile and uniaxial compressive stress) behave differently. For unstrained silicon at room temperature, holes occupy the top two bands: heavy and light hole bands. The unstrained constant energy surfaces for the two bands are shown in Figure 3-3 and highlight the large heavy hole mass along the $<110>$ direction (common MOSFET channel orientation). With the application of strain, the hole effective masses become highly anisotropic due to band warping and the energy levels become mixtures of the pure heavy, light and split-off bands. Thus, the light and heavy hole bands lose their meaning and holes increasingly occupy the top band at higher strain due to the energy splitting. The warped valence bands are shown in Figure 3-3 for the three most common types of stresses studied by the industry (biaxial tensile and longitudinal uniaxial compressive stress on (100) and (110) wafers). To achieve high hole mobility, it is key for the top band to have a low in-plane conductivity mass (i.e. a narrow width to constant energy surface along $<110>$) since it is difficult at manufacturable stress levels to significantly enhanced hole mobility through reduced intervalley scattering. This is because valence band splitting under strain is small (as compared to the conduction band). Hole intervalley scattering is not significantly reduced for stress <
1GPa since the bands’ splitting needs to be comparable to the optical phonon energy (60meV) to appreciably suppress intervalley phonon scattering (see Figure 3-4).

Thus, the key to providing large hole mobility is favorable band warping in the top band and enough band splitting to primarily populate the top band. As seen in Figure 3-3, the narrower constant energy surface in the \( <110> \) direction for uniaxial compression on both (100) and (110) wafers creates a 40% smaller in-plane mass as compared to biaxial tensile stress. Also, as seen in Figure 3-3 for biaxial tensile stress, the out-of-plane mass (z / \(<001>\) direction) for the second band is larger then the top band (reverse is true for compressive stress). Figure 3-5 summarizes the key features for the top band in the simple 2-dimensional energy vs. \( k \) diagram. The light, top band, out-of-plane mass for biaxial tensile stress creates an interesting effect for carrier transport in the 2-dimensional MOSFET inversion layer that will be discussed in the next section and explains why biaxial tensile stress gives significant mobility enhancement at high stress but only to lose the mobility enhancement at high vertical fields.

**Importance of a Larger Out-of-Plane Mass for the Top versus Second Band**

In a MOSFET, 2-dimensional surface confinement in the inversion layer also shifts the valence bands and the conduction valleys. Whether the confinement induced shift adds to or reduces (cancels) the strain induced splitting simply depends on the magnitude of the out-of-plane masses (valence band splitting is more complicated but this simple model captures the essential physics). Bands or valleys with a “light” out of plane mass will have a larger energy level shift relative to bands with a “heavy” mass (similar to the increasing ground state energy of a quantum well as the particle mass decreases). Hence, when the top most occupied band (or valley) has a lower out-of-plane mass compared to the next occupied band, the splitting is reduced or lost with surface confinement. Figure 3-6 pictorially shows the energy level shift.
with confinement for both uniaxial and biaxial stress. Etop represents the top band with large out-of-plane mass for uniaxial stress and small for biaxial stress (relative to the second band). Hence, the top band will have a small shift in energy due to confinement from high vertical field for uniaxial stress but large shift for biaxial stress. Esecond represents the second band. As seen in the figure, the stress induced band splitting (Etop – E bottom) is increased for uniaxial stress but decreased for biaxial tensile stress. Thus, strain favors occupation of the top band for both types of stresses; however, confinement favors occupation of the top band for uniaxial compressive stress and second band for biaxial tensile stress. The net effect is strain and confinement is additive for uniaxial compressive stress but subtractive for biaxial tensile stress. The competing effects of strain and surface confinement on the band splitting is one of the reasons for the loss in mobility enhancement in biaxially strained silicon p-MOSFETs at high electric fields. However, in n-MOSFETs at high electric fields, the out-of-plane mass for the $\Delta 2$ valleys is high because in the out-of-plane direction, the mass is given by the longitudinal mass ($m_l = 0.98m_o$) Hence the band splitting for NMOS at high electric fields is preserved. The increased valence band splitting with confinement maintains the stress enhanced mobility at high vertical fields and is one of the key reasons uniaxial stress is being widely adopted [Wel94], [Zha05], [Gha03], [Gil04].

**State-of-the-Art Strain Technologies**

Two basic approaches of implementing strain on MOSFETS exist - A global approach where stress is introduced across the entire substrate and the other is a local approach where stress is engineered into the device by means of epitaxial layers and/or high stress nitride capping layers. Most of the pioneering work on strained silicon has focused on biaxial global stress using a wafer based approach of a thin strained silicon layer on a thick relaxed Si$_{1-x}$Ge$_x$ virtual
substrate to stretch the Si channel. High biaxial tensile stress can been shown to increase the hole mobility [Mey04]. Figure 3-7 [Kwu05], [Mey04] is a schematic diagram of the biaxial strained-Si MOSFET using relaxed Si$_{1-x}$Ge$_x$.

However, for the first and second generation strained silicon MOSFETs being adopted in all high performance logic technologies [Tho04], [Gha03], [Gil04] the industry is adopting process induced uniaxial stress, which will be the focus of this section. Although both biaxial tensile and uniaxial compressive stresses can improve the hole mobility, the efficacies of the two stresses are different. Uniaxial process induced stress (as opposed to biaxial) is being pursued since larger hole mobility enhancement can be achieved at low strain and because of significantly smaller stress induced n-channel MOSFET threshold voltage shift [Tho04].

For uniaxial compressive stress, about 50% hole mobility enhancement can be achieved with about 500MPa [Tho04b], [Tho04c]; however, biaxial tensile stress needs more than 1GPa to be able to increase the hole mobility. In fact, at low biaxial tensile stress, the hole mobility is actually degraded [Rim02], [Rim03], [Fis02], [Fis03], which is contradictory to the theoretical prediction made by Oberhuber et al. [Obe98]. Because of these and other differences between uniaxial and biaxial stress, the highest drive current enhancement on short channel devices for uniaxial stress (1.46mA/µm and 0.88mA/µm for n and p-channel devices, respectively) [Bai04] has already significantly surpassed biaxial stress (0.85 mA/µm and 0.45mA/µm for n and p-channel, respectively) [Wan03]. Three state-of-the-art techniques to introduce uniaxial strain in the Si channel will be described next.

In the first approach [Tho04] reported by Intel, Texas Instruments and Applied Materials Inc., a local epitaxial film is grown in the source and drain regions which introduces uniaxial stress into the silicon channel. The process flow consists of the following steps shown in Figure
First, the Si source and drain are etched creating a silicon recess. Next, SiGe (for p-channel) or SiC for n-channel is epitaxially grown in the source and drain. This creates primarily a uniaxial compressive or tensile stress respectively, in the channel of the MOSFET. For 17% Ge, 500 to 900 MPa of channel stress is created depending on the proximity of the SiGe to the channel. Impressive 60-90% drive current enhancements on short devices (~35 nm) have been demonstrated, which offers greater device performance than nearly any other Si device enhancement concepts.

A second lower cost technique to introduce strain in the MOSFET is with a tensile and/or compressive capping layer [Pid04], [Yan04] as shown in Figure 3-9. The capping films are introduced either as a permanent layer post salicide as discussed here or as a sacrificial layer before source and drain anneal to be discussed next. This dual capping layer approach has been recently enabled by the creation of very high compressive and tensile stress SiN. SiN layers with > 2.0 GPa of tensile stress and >2.5GPa of compressive stress have recently been developed by Applied Materials. IBM, AMD and Fujitsu [Pid04], [Yan04] have reported a CMOS architecture as shown in Figure 1-5 in which high tensile and high compressive silicon nitride layers are selectively deposited on NMOSFET and PMOSFET respectively. This Dual Stress Liner (DSL) architecture creates longitudinal uniaxial tensile and compressive stress in the silicon channel to simultaneously improve both n and p-channel transistors. The process flow consists of a uniform deposition of a high tensile Si3N4 liner post silicidation over the entire wafer followed by patterning and etching the film off p-channel transistors. Next, a highly compressive SiN layer is deposited and this film is patterned and etched from n-channel regions. High stress compressive films can induce channel stress comparable in magnitude to the first generation embedded SiGe in the source and drain. The advantages of dual stress liner flow over
epitaxial SiGe are reduced process complexity and integration issues. Capping layers can also introduce strain into the silicon channel via a stress memorization of the poly-Si gate [Hao04]. In this approach, a highly tensile nitride capping layer acts as a temporary stressor. The flow consists of the following steps: (i) poly-Si gate amorphization, (ii) deposition of a high stress SiN layer on top of the poly-Si gate, (iii) re-crystallization of the poly-Si gate during source/drain anneal, and (iv) removal of the SiN layer. After removal of the poly-Si capping layer some stress remains in the poly-Si gate and Si channel. N-channel transistor enhancement of > 10 % has been reported with this technique.

Summary
In this chapter, the physics of strained silicon was discussed in detail. Strain introduces advantageous anisotropy in silicon by altering the valence and conduction band structures and/or scattering rates. Favorable carrier repopulation and reduced inter-valley scattering result in higher mobility enhancement for uniaxial stress compared to biaxial stress, and this enhancement is maintained even at high vertical electric field. SiGe in the source and drain, dual stress liners and stress memorization techniques have been introduced into state-of-the-art MOSFETS. The next chapter discusses wafer bending techniques used in the experimental set-up of this work and explains the method of extraction of piezoresistance coefficients from the drive current enhancement.
Figure 3-1. MOSFET schematic device cross section (standard orientation)

Figure 3-2. Ellipsoids of constant electron energy in reciprocal (“k”) space each corresponding to one of the degenerate conduction band valleys. a) For this case, the four orange colored valleys are in the plane of the silicon and the two green colored valleys are out of the plane. b) Energy level at the bottom of the six conduction band valleys. Application of advantageous strain splits the energy level as shown, removing the degeneracy (i.e the equivalence in energy) between the $\Delta_2$ and $\Delta_4$ valleys.
Figure 3-3. Hole constant energy surfaces obtained from 6 band kp calculations for common types of stresses (a) unstressed, (b) longitudinal compression on (100) wafer, (c) longitudinal compression on (110) wafer, (d) biaxial tension.

Figure 3-4. Simplified schematic of the hole intervalley phonon scattering process. High stress and splitting larger than the optical phonon energy (60meV) are required to suppress scattering.
Figure 3-5. Simplified valence band energy vs. k diagram for strained silicon under longitudinal uniaxial compression and biaxial tension.

Figure 3-6. Simplified schematic of valence band splitting of strained Si as a function of gate overdrive.

Band splitting due to strain

Splitting (increases) / (decreases)

under confinement
Figure 3-7. Schematic diagram of the biaxially strained-Si MOSFET on relaxed Si$_{1-x}$Ge$_x$ layer. (Adopted from [Mey04])

Figure 3-8. Strained Si p-channel MOSFET, a) process flow, b) TEM cross sectional view
Figure 3-9. Dual stress liner process architecture with tensile and compressive silicon nitride capping layers over NMOS and PMOS.
CHAPTER 4
WAFER BENDING EXPERIMENT AND MOBILITY ENHANCEMENT EXTRACTION ON STRAINED SILICON MOSFETS

In this chapter, wafer bending experiments designed to measure Piezoresistance coefficients as described the in previous chapters are presented. The electron and hole mobility enhancement vs. stress is extracted and the $\pi$ coefficients of n and p-type silicon are subsequently calculated. Concentric-ring and four-point bending apparatus are used to apply six kinds of mechanical stress to the channels the MOSFETS under test. These are: Biaxial tensile, biaxial compressive, uniaxial longitudinal tensile and compressive and uniaxial transverse tensile and compressive stresses. The stress range used in these experiments is 50MPa to 350MPa. MOSFETs from 90nm technology [Tho04a], [Tho04b], [Tho02] with the channels oriented along [100] direction on (001) wafers are used in the experiments. Uniaxial Tension is also applied on n-type resistors on the same wafer belonging to 90 nm technology as well. This is done to measure and compare piezoresistance coefficients on bulk silicon where the effect of surface electric field is absent with device level coefficients.

First, the four-point bending apparatus used to apply uniaxial stress will be explained in detail and equations for calculating the uniaxial stress will be derived. For the concentric-ring bending jig used to apply biaxial stress, nonlinear bending relations are used. Methods used to extract threshold voltage and mobility under a given gate bias are explained. Finally, a brief discussion on error and uncertainty analysis associated with stress calibration is reviewed followed by a summary of the chapter.

Wafer Bending Experiments on MOSFETs

An illustration of a (001) silicon surface is shown in Figure 4-1(a). As seen in the figure, the [100] crystallographic direction is oriented at 45° from the wafer notch (which is oriented along [110] direction). Rectangular wafer strips with the n and p channel devices were prepared
by sawing the wafer using an optical-cleaver. Care was taken to ensure the edges were as smooth as possible and free of defects. Figure 4-1(b) shows the MOSFET cross-section with [100] being the channel direction and the [110] axis represented as the direction out-of-the-plane of silicon. In this work, uniaxial stress is applied along the [100] direction and a corresponding biaxial stress is also applied on the device that translates into an equivalent out-of-plane stress.

**Uniaxial Stress: Four-Point Bending Apparatus Illustration**

Uniaxial stress is applied to the channel of a MOSFET using four-point bending technique. Figure 4-2(a) and 4-2(b) are pictures of the apparatus used to bend the substrate and the illustrations of calculating the uniaxial stress. As shown in Figure 3-2(b), the upper and lower surfaces of the substrate will experience uniaxial compressive and tensile stress along [100] direction, respectively. Reference [Tim76] describes the equations used to quantify the applied stress on both the surfaces under the following assumptions:

(i) The substrate is simply supported.

(ii) Four loads applied by four cylinders are approximated by four point forces, $P$.

Using Figure 4-2(b), the deflection at any point on the upper surface is represented by $y(x)$ [Kwu05]. As there is no deflection at the end points, it can be assumed that $y(0)=0$ and $y(L)=0$. Using the above assumption the stress on the upper and lower surfaces at the center of the substrate are given by Equation 4-1 and Equation 4-2,

$$\sigma_{upper} = -\frac{EH}{2r} \quad (4-1)$$

$$\sigma_{lower} = \frac{EH}{2r} \quad (4-2)$$

where $E = 1.302 \times 10^{11} Pa$ [Bra72] is the Young’s modulus of crystalline silicon along the [100] direction on (001) substrate, $H$ is the substrate thickness, $r$ is the radius of curvature [Tim76], which is given by Equation 4-3,
\[ \frac{1}{r} = \frac{M}{EI_z} = \frac{Pa}{EI_z} \]  

(4-3)

where \( M = Pa \) is the moment for \( a \leq x \leq L/2 \), and \( I_z = bH^3/12 \) is the moment of inertia for a substrate with rectangular cross section and width of \( b \). Using Equation 4-1 and 4-2, equation 4-2 can be written as, [Tim76]

\[ \sigma_{upper} = -\frac{MH}{2I_z} = -\frac{PaH}{2I_z} \]  

(4-4)

\[ \sigma_{lower} = \frac{MH}{2I_z} = \frac{PaH}{2I_z} \]  

(4-5)

For \( 0 \leq x \leq a \), the moment \( M = Px \) and

\[ EI_z \frac{d^2y}{dx^2} = -M = -Px \]  

(4-6)

The solution for the second order differential equation is given by Equation 4-7,

\[ y = \frac{1}{EI_z} \left( -\frac{P}{6} x^3 + C_1x + C_2 \right) \]  

(4-7)

where \( C_1 \) and \( C_2 \) are integration constants. For \( a \leq x \leq L/2 \), the moment \( M = Px - P(x - a) = Pa \) and [Tim76]

\[ EI_z \frac{d^2y}{dx^2} = -M = -Pa \]  

(4-8)

Solving Equation 4-8, it can be written that

\[ y = \frac{1}{EI_z} \left( -\frac{Pa}{2} x^2 + C_3x + C_4 \right) \]  

(4-9)
where $C_3$ and $C_4$ are integration constants. The four integration constants can be determined from the boundary conditions [Tim76]: (i) the slope $dy/dx$ determined from Equations 3-7 and 3-9 should be equal at $x = a$, (ii) the slope $dy/dx = 0$ at $x = L/2$, i.e., at the center of the substrate, (iii) at $x = a$, $y$ determined from Equations 3-7 and 3-9 should be equal, and (iv) at $x = 0$, $y = 0$.

With these four boundary conditions, Equations 3-7 and 3-9 can be simplifies as Equations 4-10 and 4-11 respectively, [Tim76]

$$y = \frac{1}{EI_z} \left( -\frac{P}{6} x^3 + \frac{Pa(L-a)}{2} x \right) \quad 0 \leq x \leq a \quad (4-10)$$

$$y = \frac{1}{EI_z} \left( -\frac{Pa}{2} x^2 + \frac{PaL}{2} x - \frac{Pa^3}{6} \right) \quad a \leq x \leq L/2 \quad (4-11)$$

Using Equations 4-10 and 4-11, the deflection at $x = a$ and $x = L/2$ are represented as shown in Equation 4-12 and 4-13,

$$y_{x=a} = \frac{Pa^2}{EI_z} \left( \frac{L}{2} - \frac{2a}{3} \right) \quad (4-12)$$

$$y_{x=L/2} = \frac{Pa}{24EI_z} \left( 3L^2 - 4a^2 \right) \quad (4-13)$$

Measuring the deflection at $x = a$, $P/I_z$ can be obtained as

$$\frac{P}{I_z} = \frac{Ey_{x=a}}{a^2 \left( \frac{L}{2} - \frac{2a}{3} \right)} \quad (4-14)$$

Using above equations the stress on the upper and lower surfaces is given by,
\[
\sigma_{\text{upper}} = -\frac{EH_y y_{x=a}}{2a \left( L - \frac{2a}{3} \right)} 
\]  
\[
\sigma_{\text{lower}} = \frac{EH_y y_{x=a}}{2a \left( L - \frac{2a}{3} \right)} 
\]  

The radius of curvature can also be simplified as, (Equation 4-17),

\[
\frac{1}{r} = \frac{Pa}{EI_z} = \frac{y_{x=a}}{a \left( L - \frac{2a}{3} \right)} 
\]  

The assumptions used to obtain Equations 4-15 and 4-16 has been verified by FEM elsewhere [Kwu05] and it holds valid within the deflection range of 0.91mm, which is greater than the deflection used in the piezoresistive measurements in this work.

Figure 4-3 is a simple illustration of how tensile stress is generated on the lower surface and a compressive stress is simultaneously generated on the top one. The exact opposite holds when the positions of the force applying rods are changed as shown in Figure 4-3 i.e. compressive stress is generated on the lower surface and a tensile stress is simultaneously generated on the top one.

**Biaxial Stress: Concentric-Ring Bending Apparatus**

Biaxial stress is applied to the channel of the n and p channel MOSFETs using concentric-ring bending. Figure 4-3(a) and 4-3(b) are pictures of the apparatus used to bend the substrate and an illustration for simulating the biaxial stress. In the case of beams, for uniaxial stress state, even deflections comparable to the plate thickness produce large stresses in the middle plane and contribute to stress stiffing. Hence, one should use large deflection to calculate deflections and stresses in a plate [Kwu05]. This translates to a non-linear analysis unlike a linear displacement-
stress relationship associated with uniaxial stress. Finite element analysis (FEM) using ABAQUS that considers both the nonlinearity and orthotropic property of Si has been used from an earlier work [Kwu05] to calculate the biaxial stress from the measured deflections. The stress calibration is illustrated by a simulation of stresses on the top and bottom plates as shown in Figure 4-4. [Mul99] As shown in Figure 4-4, on the bottom plane of the substrate, the stress at the center is tensile as expected while, on the top plane, the center stress appears as compressive first, then gradually decreases and finally becomes tensile. This can be explained by the nonlinearity of bending plate with large deflection [Kwu05]. At small deflection (<< the thickness of substrate 0.77 mm), the stress on the top and bottom planes are of nearly the same magnitude but opposite sign, as shown in Figure 4-4. The magnitude of the tensile stress on the top plane is additive due to substrate stretching while the magnitude of the compressive stress is reduced by the additional tensile stress. The corresponding load is about 4500N or 1000lb when displacement reaches 0.89mm. The maximum deflection achieved in this work is about 0.46mm, corresponding to about 1100N or 250lb.

**Error Analysis**

In this subsection, the sources of uncertainty in the applied stress will be estimated. There are four major sources of uncertainty in applied uniaxial stress using the four-point bending jig shown in Figure 4-2. They are:

a) Uncertainty is the starting point of bending.

b) The second source of uncertainty is the micrometer for setting the displacement.

c) The third source is the variation of the substrate thickness. The typical thickness of a 12 inches (300mm) wafer is 775±20µ. The uncertainty in wafer thickness is 0.02mm.
d) The uncertainty associated with wafer alignment in the bending apparatus. The wide spread in piezoresistive coefficient values in p type silicon makes the parameter extraction process highly sensitive to measurement errors. The four point bending loading fixture has a number of sources of experimental error and five predominant sources of error can we summarized as [Bea92]

a) Weight Measurement Error

b) Length Measurement Error

c) Loading Symmetry Error

d) Beam Rotation Error due to wafer/substrate angle misalignment and

e) Probe Force Errors

It has been shown that \( \pi_{44} \) is smaller than \((\pi_{11} + \pi_{22})\) in n-type silicon [Bea92] and hence this small ratio of \((\pi_{11} + \pi_{22})/\pi_{44}\) should make calibration errors much less of a problem with Piezoresistance measurement on n-channel MOSFET. A detailed error analysis has been done by Beaty et al [Bea92] and is beyond the scope of this work.

An approach to reducing the errors in the measured values of \((\pi_{11} + \pi_{22})\) is to avoid trying to determine individual values of \(\Delta R/R\). The following recommendations could help in minimizing error in the measurement technique and more accurate stress calibration

a) Wheatstone bridge techniques that can directly measure the quantities \(\Delta R_x/R_x + \Delta R_y/R_y\) and \(\Delta R_y/R_x - \Delta R_y/R_y\).

b) Using four point probing technique instead of a two point probe technique to minimize contact resistance while measuring the Piezoresistance of n and p type resistors. It is often difficult or impossible to accurately measure the contact resistance of the pads when in contact with the probe tips and a four-point probing
technique is one of the most common methods for measuring resistivity [Sch90]. In the four point probing technique, current is injected into the material via the outer two electrodes. The resultant electric potential distribution is measured via the two inner electrodes. By using separate electrodes for the current injection and for the determination of the electric potential, the contact resistance between the metal electrodes and the material will not show up in the measured results. Because the contact resistance can be large and can strongly depend on the condition and materials of the electrodes, it is easier to interpret the data measured by the four-point probe technique than results gathered by two-point probe techniques. Hence, the resistance measured is more accurate and the source of error arising due to the contact resistance is eliminated.

c) Statistical data collection is often the primary solution to obtaining accurate values of piezoresistive coefficients in p-type silicon. [Bea92] Variation of Piezoresistive coefficients from die to die and wafer to wafer should be taken into account for greater confidence in the stress calibration method. Other factors such as temperature, humidity and room conditions are usually kept constant during the experiment and hence their effect on the measurement can be considered negligible. The bending apparatus and the microscopic/stage combination is always kept covered in a walled, closed probe station with no source of light in it and hence optical generation is also not considered as a significant factor to the changes in resistance.

**Extracting Mobility, Threshold Voltage and Electric Field from Drive Current**

In this section, the methods of extracting the $\pi$ coefficients from mobility enhancement will be described. The effective mobility will be extracted from the drain current in the linear
region (low drain bias) for a long-channel MOSFET. At low drain bias $V_{DS}$, the linear drain current of an ideal MOSFET can be approximated as

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS},$$

(4-18)

and the effective mobility $\mu_{eff}$ can then be expressed as

$$\mu_{eff} = \frac{I_{DS}}{C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}^2},$$

(4-19)

where $C_{ox}$ is the gate oxide capacitance, $W$ and $L$ are the channel width and length respectively, and $V_{GS}$ and $V_T$ are the gate bias voltage and threshold voltage respectively. The linear region threshold voltage is extracted by drawing a tangent line to the $I_{DS}-V_{GS}$ curve at the point where the slope is the largest and extending it to intercept the x axis. The gate voltage at the intercept is defined as the threshold voltage. ($V_{gs}=V_{t}$). This indicates the onset of inversion in the MOSFET channel. Figure 4-5 is a plot of the $I_{DS}-V_{GS}$ curve and threshold voltage extraction using the Keithley 4200SCS Semiconductor Parameter Analyzer. Also, an additional curve proportional to the gradient of the $I_{DS}-V_{GS}$ curve, $\partial I_{DS}/\partial V_{GS}$, defined as the transconductance, is also shown to help to determine the point with the largest slope on the $I_{DS}-V_{GS}$ curve.

Also, the effective vertical electric field $E_{eff}$ is expressed as [Tau98]

$$E_{eff} = \frac{Q_b + \eta Q_{inv}}{\varepsilon_s},$$

(4-20)

where $\eta$ is a fitting parameter and equal to 1/3 for holes, $Q_b$ is the bulk depletion charge, $Q_{inv} = C_{ox} (V_{GS} - V_T)$ is the inversion charge, and $\varepsilon_s$ is the dielectric constant of silicon. At the interface of gate oxide and silicon channel using the electric displacement continuity [Tau98]
equations and the expression for electric field at the surface, the effective vertical field $E_{\text{eff}}$ can then be obtained in terms of the depletion and inversion charge densities as

$$E_{\text{eff}} = \frac{E_{\text{ox}} e_{\text{ox}} - (1 - \eta) Q_{\text{inv}}}{e_s} = \frac{C_{\text{ox}} [V_{\text{GS}} - (1 - \eta)(V_{\text{GS}} - V_{\text{i}})]}{e_s},$$

(4-21)

where $E_{\text{ox}}$ is approximated by $V_{\text{GS}}/t_{\text{ox}}$, which is valid for $V_{\text{DS}}<<V_{\text{GS}}$ [Tau98], and $C_{\text{ox}}$ is the gate oxide capacitance.

**Extraction of Piezoresistance Coefficients from Drive Current**

In chapter 2, from equation (2-1), piezoresistance was defined as

$$\pi = \frac{1}{\chi} \frac{R_{\chi} - R_0}{R_0} = \frac{1}{\chi} \frac{\Delta R}{R_0},$$

(4-22)

However, it can also be shown that the change in resistance $\Delta R/R_0$ is proportional to change in drive current. From Ohm’s law $V = IR$

$$\Delta R_{\text{ch}} = \frac{V}{I_{\chi}} - \frac{V}{I_0}$$

(4-23)

where $I_{\chi}$ is the drain current of the MOSFET after application of stress and $I_0$ is the unstressed current.

$$\Delta R = \frac{VI_{\chi} - VI_0}{I_{\chi}I_0}$$

(4-24)

$$\Delta R = \frac{V \Delta I}{I_{\chi}I_0}$$

(4-25)

$$\Delta R = \frac{R_0 \Delta I}{I_{\chi}} \Rightarrow \Delta R = \frac{\Delta R}{R_0} = \frac{\Delta I}{I_{\chi}}$$

(4-26)

$$\frac{\Delta R}{R} = \frac{\Delta I}{I_0} = \frac{\Delta \sigma}{\sigma}$$

(4-27)
Of course, here it has been assumed that upon application of stress, the dimensional changes are negligible when compared to the change of resistivity. Hence, all other factors in the mobility expression in equation 4-19 are constant and get canceled out. This approach has been used in chapter 5 to extract device level piezoresistance coefficients on (100) wafer along the (100) channel direction.

Summary

In this chapter, the wafer bending experiments to generate uniaxial and biaxial mechanical strain was discussed in detail. The four-point bending and concentric ring bending techniques were elaborated upon with the relevant mathematical analysis and simulation results. This was followed by a discussion on uncertainty analysis associated with stress-calibration; the main factors contributing to the uncertainty were identified as starting point of bending, micrometer displacement, wafer misalignment and variation of substrate thickness. The technique used to extract mobility, threshold voltage and electric field from the drive current are described. And the approach used to extract piezoresistance from drive current enhancement in turn, is also described. Chapter 5 will discuss the experimental results obtained and build a physical insight/reasoning into the physics behind the observed piezoresistance coefficients.
Figure 4-1. Illustration of Si surface a) and b) MOSFET schematic device cross section [100] channel orientation.
Figure 4-2. The apparatus, jig, used to apply uniaxial stress to the substrate. (a) In this picture, uniaxial compressive and tensile stresses are generated on the upper and lower surfaces of the substrate respectively. (b) Illustration of calculating the uniaxial stress on a bent substrate. The substrate is simply supported. Four loads applied by cylinders are approximated by four point forces, $P$. The deflection at any point on the upper surface is designated by $y(x)$. (c) When the parallel ridges are closer on plate A, and farther apart on plate B uniaxial compression is applied. The reverse is true for uniaxial tension.
Figure 4-3 The apparatus, jig, used to apply biaxial stress to the substrate. In this picture, biaxial compressive and tensile stresses are generated on the upper and lower surfaces of the substrate respectively. Illustration of simulating biaxial stress on a bending plate (substrate). The plate (substrate) is simply supported. The deflection at any point on the upper surface is designated by w(r).
Figure 4-4. Finite element analysis simulation of the bending plate (substrate) [Kwu05]. (a) The radial stresses at the center of the top, middle, and bottom planes of the bending plate vs. the displacement of the smaller ring are shown. (b) Illustration of top, middle, and bottom planes of the plate.
Figure 4-5. Snapshot of the $I_{DS}-V_{GS}$ characteristic and threshold voltage/transconductance extraction from Kiethley 4200SCS Semiconductor Parameter Analyzer.
CHAPTER 5
EXPERIMENTAL RESULTS AND DISCUSSION

Introduction

In this chapter, piezoresistance coefficients are revisited. Experimental results from the wafer bending experiment in chapter 4 are discussed. Many previous works have reported piezoresistance coefficients and used them to analyze MOSFET performance under stress [Gal04], [Bra01], [Wan03]. However, most of those works use bulk piezoresistance coefficients directly and only a few of them [Dor73], [Fis03] investigate surface piezoresistance coefficients, which take into account the effect of 2-D inversion-layer confinement due to surface electric field. In this chapter, the measurements for both bulk Si and MOSFETs are presented. The results show that differences do exist between bulk and confined cases. This is followed by a simple qualitative picture in terms of carrier repopulation, band splitting and scattering rates to explain the differences between device level (MOSFET) and bulk piezoresistance. In order to investigate the piezoresistance effect due to the out-of-plane stress induced by capping layers, an equivalent in-plane biaxial stress has been used to investigate the piezoresistance coefficient of the out-of-plane direction.

It had been shown in chapter 2 that piezoresistance coefficients are mainly determined by the change in carrier mobility with stress. Since in-process strain is typically introduced longitudinal or perpendicular to the channel, the mechanical stress effect on mobility can be expressed by equation 2-7: \[ \frac{\Delta \mu}{\mu} \approx \left| \Pi \sigma_{||} + \Pi \sigma_{\perp} \right| \]

where the subscripts \( || \) and \( \perp \) refer to the directions parallel and transverse to the current flow in the plane of the MOSFETs, \( \frac{\Delta \mu}{\mu} \) is the fractional change in mobility, \( \sigma_{||} \) and \( \sigma_{\perp} \) are the longitudinal and transverse stresses and \( \Pi_{||} \) and \( \Pi_{\perp} \) are...
\( \pi \) are the piezoresistance coefficients expressed in Pa-1 or 10-12 cm2/dyne. They can be expressed in terms of the three fundamental cubic piezoresistance coefficients \( \pi_{11}, \pi_{12} \) and \( \pi_{44} \) for a (001) wafer and five coefficients for a (110) wafer. Under uniaxial stress, the normalized mobility variations reduce to [Bra01]

\[
\frac{\Delta \mu}{\mu} \parallel = \left( \frac{\Pi_s + \Pi_{44}}{2} \right) \sigma \\
\frac{\Delta \mu}{\mu} \perp = \left( \frac{\Pi_s - \Pi_{44}}{2} \right) \sigma
\]

where, \( \Pi_s = \Pi_{11} + \Pi_{12} \).

Many previous works [Wel94], [Nay94],[Fis96],[Tak96] have pointed out that the main factors that affect mobility are: (1) the change in the averaged longitudinal effective mass due to relative carrier distribution on different valleys (NMOS) or bands (PMOS); (2) the change in intervalley carrier scattering rate due to the energy splitting between different valleys or bands. The following section provides the measured results of the work done and the detailed explanation in terms of the factors mentioned above.

**Experimental Results**

**Description of devices measured**

The devices used in the experiment are from 90nm technology having 10\( \mu \)m channel length and 12\( \AA \) thin gate oxide thickness. Kiethley 4200SCS Semiconductor Parameter Analyzer is used to measure the \( I_{DS}-V_{GS} \) characteristics with gate voltage \( V_{GS} \) swept from 0 to 1.2V for n-channel MOSFETS and drain voltage \( V_{DS} \) fixed at 50mV. A similar negative bias is applied to p-channel devices. The experimental setup for applying stress using four-point bending to generate uniaxial loading [Bea92] and measuring the I-V curves was shown in chapter 4, Figure 4-2. The stress was applied by a standard four-point-bending method along Si channel direction. Figure 5-1(a) shows the simple schematic of a (001) surface and figure 5-1(b) illustrates a MOSFET cross-sectional view indicating the in-plane and out-of-plane directions. Concentric ring bending
apparatus as illustrated in chapter 4, Figure 4-3 was used to apply biaxial stress on the devices. Both p- and n-MOSFETS oriented along the [100] channel were measured. Figure 5-2 and Figure 5-3 show the results reported in an earlier work [Kwu05] for p-MOSFET Piezoresistance coefficients oriented along the [110] direction on a (001) surface. The corresponding values of piezoresistance are reported for comparison with the [100] data in table 5-1 and table 5-2. Figures 5-4 and 5-5 how the measured result for nMOSFET [100] channel under longitudinal and transverse uniaxial stress, respectively. These results are averages over 3 sets of measurements. The results of both nMOSFETS and pMOSFETS under in-plane biaxial stress are shown in Figure 5-4. All the measured devices had the same gate length of 10 μm. The stress range used in the experiments was < 350 MPa, beyond which the silicon strips failed due to edge defects.

The longitudinal and transverse piezoresistance coefficients of our work and other works for the (100) and (110) wafers oriented in the [100] and [110] channel directions are summarized in Table 5-1. For the case of uniaxial transverse stress on a [100] NMOS, surface and bulk values not only differ in magnitude, but also in sign. A qualitative explanation for this observation is explained in the next section. The experimental data also show an almost constant drive current for the case of [100] PMOSFETS on (100) wafer, which is indicated by the low values of their piezoresistance. (9.10 x 10-12 cm²/dyne and -6.19 cm²/dyne respectively).

Piezoresistance coefficients for bulk silicon were found using test 1 square ohm n-well resistors of W/L 46.7 μm. The values are reported in Table 5-3 and compared with the inversion layer piezoresistance coefficients. Figure 5-5 shows the effect of uniaxial longitudinal tension on a [100] n-well resistor measured on the same wafer as the MOSFETs.
Effect of surface electric field

In order to clarify the piezoresistance effect of MOSFET, not only the effect of external stress has to be investigated, but also the effect of surface electric field. When adding perpendicular electric field, the band structure of both conduction band and valence band will change. This is because on the application of vertical electrical field under certain types of stress there is strong coupling of the electric field with the wave function [Wang04][Tho06]. Neglecting spin orbit coupling [Cha72], it is seen that this energy change caused by electric field will enhance or sometimes compensate the effect of stress. Since MOSFETs are working under certain gate voltage, the bulk values of piezoresistance coefficients are not always precise. The effect of this gate field should be considered.

Experimental data from this work for nMOSFETs and pMOSFETs is plotted together with Smith’s bulk data in Figure 5-6a and Figure 5-6b, respectively. After coordinate transformation for an arbitrary channel direction, the values of surface longitudinal and bulk piezoresistance coefficients is shown below

\[ \pi_l = \pi_{11}l_1^4 + \pi_{12}l_1^2m_1^2 + \pi_{21}l_2^2m_1^2 + \pi_{22}m_1^4 + 2\pi_{44}l_2^2m_1^2 \]  \hspace{1cm} (5-7)

\[ \pi_t = \pi_{11}l_2^4 + \pi_{12}l_1^2m_2^2 + \pi_{21}l_2^2m_2^2 + \pi_{22}m_2^4 + 2\pi_{44}l_2m_1m_2 \]  \hspace{1cm} (5-8)

where \( \pi_l \) is the longitudinal piezoresistance coefficient and \( \pi_t \) is the transverse piezoresistance coefficient.

Surface piezoresistance coefficients of pMOSFETS in [100] direction

The experimental results showed negligible/very little drive current enhancement for pMOSFETS under longitudinal or transverse compressive stress and hence the low value of their piezoresistance, as see in Table 5-1. Table 5-1 also shows that for pMOSFET, the bulk Piezoresistance coefficient values [Smi52] and measured surface piezoresistance upon
application of both longitudinal and transverse stresses are very similar in value. This can be explained by the result of 6-band $k \cdot p$ calculation for valence band shown in Figure 5-7. From band calculations, we can find that the constant energy contour under strain for bulk Si and MOSFET are similar [Tho04]. The energy structure doesn’t change much from bulk to surface, and thus both the carrier repopulation and scattering rate are similar for bulk and surface cases, which indicates that the piezoresistance coefficients are also similar.

**Surface piezoresistance coefficients of nMOSFETS in [100] direction**

The experimental result in Figure 5-6 and Figure 5-7 shows that the bulk piezoresistance coefficients are quite different from their (100) surface counterparts for the case of uniaxial tension on nMOSFETS. The most obvious differences are: (1) Transverse piezoresistance coefficients have different sign for bulk case and surface case; (2) Surface longitudinal piezoresistance coefficient for [100] channel is much smaller than bulk value, which means that the [100] channel MOSFETs have smaller mobility enhancement than bulk Si.

**Transverse Tension**: A simple qualitative physical reasoning for (1) is developed below. In the case of bulk silicon, the calculation of band splitting caused by strain shows that valleys 1 and 2 have lower energy while valley 3 has higher energy (See Figure 5-8). Thus most electrons will favorably occupy the lower energy state and distribute on valleys 1 and 2. Since valley 2 has larger longitudinal effective mass, the mobility of bulk Si will decrease ($\tau_{\perp} = 53.4$). For MOSFET (Figure 4-4b), under the electric field, valley 1 will have lower energy because of its largest out-of-plane effective mass (this is explained in greater detail in chapter 3). However, when increasing the transverse tensile stress, band splitting calculations show that valley 1 will have even lower energy while valley 3 will have the highest energy. This will result in a different carrier repopulation scheme than bulk silicon Thus, most electrons will distribute on valley 1.
Thus, with increasing strain, the magnitude of band-splitting increases and valley 3 will move even higher while valley 1, 2 move even lower. This will make the electrons that used to be in valley 3 redistribute to valley 1 or 2. Bands or valleys with a “light” out-of-plane mass will shift more in energy relative to bands with a “heavy” mass. Since there are more electrons on valley 2 with strain, combined with the fact that valley 2 has the largest longitudinal effective mass, the mobility will decrease a little bit. (But not much since most of the electrons are already at valley 1.) However, with increasing strain, valley 3 and valley 1, 2 split further apart which will cause a reduction in scattering rate. The reduction in scattering rate compensates the larger effective mass and makes the mobility increase a little bit ($\pi_{\perp} = -12.77$).

From the discussion above, we can see that bulk value is not always working for the case of modern day MOSFET. The mobility enhancement largely depends on the crystal symmetry of the certain surface direction. Since piezoresistance coefficients are measured experimentally, we should use device-level MOSFET inversion-layer coefficients and not bulk silicon values.

### Effects of out-of-plane uniaxial stress

There are many ways to induce strain on MOSFETs, such as nitride capping layer, SiGe doped source and drain region or epitaxial SiGe layer. Among these methods, some of them affect the total channel mobility by introducing an out-of-plane uniaxial stress while some affect the mobility by introducing an in-plane uniaxial/biaxial stress. In this work, an in-plane biaxial stress is applied to analyze the effect of out-of-plane uniaxial stress. We know that the strain tensor can be equivalently decomposed into three matrices [Chu95], where

$$
E_{ij} = E_{ij}^{\text{trace}} + E_{ij}^{\text{shear-100}} + E_{ij}^{\text{shear-111}}
$$  \hfill (5-9)

$$
E_{ij}^{\text{trace}} = \frac{1}{3}
\begin{bmatrix}
E_{xx} + E_{yy} + E_{zz} & 0 & 0 \\
0 & E_{xx} + E_{yy} + E_{zz} & 0 \\
0 & 0 & E_{xx} + E_{yy} + E_{zz}
\end{bmatrix}
$$  \hfill (5-10)
represents the fractional change of the volume, while Equation 5-11,
\[
\frac{1}{3} \begin{bmatrix}
2\varepsilon_{xx} - (\varepsilon_{yy} + \varepsilon_{zz}) & 0 & 0 \\
0 & 2\varepsilon_{yy} - (\varepsilon_{xx} + \varepsilon_{zz}) & 0 \\
0 & 0 & 2\varepsilon_{zz} - (\varepsilon_{xx} + \varepsilon_{yy})
\end{bmatrix}
\begin{bmatrix}
0 & \varepsilon_{xy} & \varepsilon_{xz} \\
\varepsilon_{xy} & 0 & \varepsilon_{yz} \\
\varepsilon_{xz} & \varepsilon_{yz} & 0
\end{bmatrix}
\] (5-11)
represents the shear strain created by stress along [100] and [111], respectively.

It is important to identify which component of strain contributes to change in mobility. Since hydrostatic strain only shifts the energy position of the bands but does not cause band splitting, it doesn’t affect mobility much. In the case of shear strain, it removes symmetry and splits degenerate bands, thus cause the total mobility to change [Chu05]. As a result, when comparing the effects of in-plane biaxial stress and out-of-plane uniaxial stress, we only need to compare the shear strain matrix caused by the stress. It has been shown that [Kwu05] that the in-plane biaxial tensile stress \( \chi_{bi} \) can be represented by an equivalent out-of-plane uniaxial compressive stress \( \chi_{uni} \) of the same magnitude. The following analysis supports the statement above.

For out-of-plane uniaxial stress [Chu95] [Bra73]:
\[
\sigma_{zz} \neq 0 \quad \sigma_{xx} = \sigma_{yy} = 0
\]
\[
\begin{bmatrix}
\varepsilon_{xx} \\
\varepsilon_{yy} \\
\varepsilon_{zz} \\
\varepsilon_{xy} \\
\varepsilon_{yz} \\
\varepsilon_{xz}
\end{bmatrix}
= \begin{bmatrix}
S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\
S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\
S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\
0 & 0 & 0 & S_{44} & 0 & 0 \\
0 & 0 & 0 & 0 & S_{44} & 0 \\
0 & 0 & 0 & 0 & 0 & S_{44}
\end{bmatrix}
\begin{bmatrix}
0 \\
\sigma_{zz}
\end{bmatrix}
\] (5-13)
\[
\Rightarrow \varepsilon_{xx} = S_{12}\sigma_{zz}
\] (5-14)
\[
\Rightarrow \varepsilon_{yy} = S_{12}\sigma_{zz}
\] (5-15)
\[
\Rightarrow \varepsilon_{zz} = S_{11}\sigma_{zz}
\] (5-16)
\[
\therefore \varepsilon_{\text{shear-111}} = 0
\] (5-17)
\[
\varepsilon_{ij}^{\text{shear--100}} = \frac{1}{3} \begin{bmatrix}
(S_{12} - S_{11}) \sigma_{zz} & 0 & 0 \\
0 & (S_{12} - S_{11}) \sigma_{zz} & 0 \\
0 & 0 & 2(S_{11} - S_{12}) \sigma_{zz}
\end{bmatrix}
\] (5-18)

For in-plane biaxial stress, [Kwu05][Gua06]:

\[
\sigma_{zz} = 0 \quad \sigma_{xx} = \sigma_{yy} = \sigma
\] (5-19)

\[
\begin{bmatrix}
\varepsilon_{xx} \\
\varepsilon_{yy} \\
\varepsilon_{zz} \\
\varepsilon_{xy} \\
\varepsilon_{yz} \\
\varepsilon_{xz}
\end{bmatrix} = \begin{bmatrix}
S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\
S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\
S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\
0 & 0 & 0 & S_{44} & 0 & 0 \\
0 & 0 & 0 & 0 & S_{44} & 0 \\
0 & 0 & 0 & 0 & 0 & S_{44}
\end{bmatrix} \begin{bmatrix}
\sigma \\
\sigma \\
\sigma \\
\sigma \\
\sigma \\
\sigma
\end{bmatrix}
\] (5-20)

\[ \Rightarrow \varepsilon_{xx} = (S_{11} + S_{12}) \sigma \] (5-21)

\[ \Rightarrow \varepsilon_{yy} = (S_{11} + S_{12}) \sigma \] (5-22)

\[ \Rightarrow \varepsilon_{zz} = 2S_{12} \sigma \] (5-23)

\[ \therefore \varepsilon_{ij}^{\text{shear--111}} = 0 \] (5-24)

\[ \therefore \varepsilon_{ij}^{\text{shear--100}} = \frac{1}{3} \begin{bmatrix}
(S_{11} - S_{12}) \sigma & 0 & 0 \\
0 & (S_{11} - S_{12}) \sigma & 0 \\
0 & 0 & 2(S_{11} - S_{12}) \sigma
\end{bmatrix} \] (5-25)

Equations 5-18 and 5-25 show that under the same magnitude of stress, the shear strain caused by these two types of stress are the same in magnitude. This indicates that both stress split bands in the same way and cause the same mobility change.

It is worth mentioning that the above qualitative discussion uses bands and out-of-plane masses and is presented only to help understand the physics. Correct and more accurate physical treatment requires self-consistent solution to Schrodinger’s and Poisson’s equations to calculate the sub-band energy shifts in the confined MOSFET inversion layer. Quantum-mechanical
calculations and confinement induced band-splitting has been calculated with a single valley and many valley model with Schrodinger’s equation elsewhere [Ste72], [Fis03],[Cha92] which can be shown to be in agreement with this simple qualitative model that can indeed capture the correct physics.

Summary

This chapter presented the experimental results along with simple qualitative reasoning. The differences observed between the conventional bulk piezoresistance coefficients and those in the surface-inversion layer of the MOSFETs were reported. It was shown that is imperative to include the effect of vertical electric field and stress on the carrier mobility to develop insight into the reasons for mobility enhancement in the inversion-layer MOSFET. Results in this work indicate that (1) Transverse piezoresistance coefficients have different sign for bulk case and surface case; (2) Surface longitudinal piezoresistance coefficient for [100] channel is much smaller than bulk value, which means that the [100] channel MOSFETs have smaller mobility enhancement than bulk Si and (3) Uniaxial Compressive stress on pMOSFETS shows little or no change in drive current enhancement. A simple qualitative physical model in terms of carrier repopulation, out of plane masses, band-splitting and scattering was used to explain the mechanisms responsible. A more numerically intensive and accurate physical treatment requires self consistent solution to Schrodingers and Poisson’s equations to calculate the sub-band energy shifts in the confined MOSFET inversion layer for which the reader is referred elsewhere [Thp06][Fis04]. Finally, the effects of out-of-plane uniaxial stress were listed. An in-plane biaxial stress can be modeled by an equivalent out-of-plane uniaxial stress. It was shown that both split the bands in a similar way and hence cause the same mobility change. This fact is particularly useful in modeling process-induced strain applied on the gate of MOSFETS (on which an out-of-plane stress actually applies through a capping later etc.) by an equivalent in-
plane biaxial stress that can be measured using existing mechanical wafer-bending techniques.

The next chapter is a summary of the thesis and provides recommendations for future work.
Figure 5-1. Si channel orientation, (001) surface and MOSFET schematic device cross section [100] channel orientation.
Figure 5-2. Mobility enhancement vs. stress for six kinds of stresses, biaxial tensile and compressive and uniaxial longitudinal and transverse, tensile and compressive along [110] channel direction. [Kwu05]. The mobility enhancements are extracted at 0.7MV/cm. The solid lines are the model predictions: blue: [Kwu05], orange: Wang et al. [Wan03]. The symbols are experimental data: blue circle: [Kwu05], green triangle: Thompson et al. [Tho04], orange diamond: Wang et al. [Wan04], and purple square: Gallon et al. [Gal04].
Figure 5-3. $\pi$ coefficient of p-MOSFETS vs. stress, including longitudinal and transverse $\pi$ coefficients for [110] direction and transverse $\pi$ coefficient for [001] direction from an earlier work [Kwu05]. The solid lines are the model predictions: blue: [Kwu05], orange: Wang et al. [Wan04]. The symbols are experimental data: blue circle: this work, green triangle: Smith [20], orange diamond: Wang et al. [Wan04], and purple square: Gallon et al. [Gal04].
Figure 5-4. Effect of Uniaxial Longitudinal Tensile stress on Bulk n-type resistor and NMOSFETs (indicated as surface tension) oriented along [100] direction on (001) Si.

Figure 5-5. Effect of Uniaxial Transverse Tensile stress on Bulk n-type resistor and n-MOSFETs (indicated as surface tension) oriented along [100] direction on (001) Si.
Figure 5-6. Effect of Biaxial Tensile and Compressive stress on and n-and p-MOSFETs oriented along [100] direction on (001) Si.
Figure 5-7. (100) Surface Piezoresistance coefficient vs. bulk Piezoresistance coefficients (a) nMOSFET (b) pMOSFET. Thicker lines indicate the surface value and thinner lines denote the bulk value. Solid lines are longitudinal piezoresistance coefficients and dashed lines are transverse piezoresistance coefficients. (Courtesy: Chu, Min) [Tho06]
Figure 5-8 Constant energy contour for bulk Hole constant-energy band surfaces for the top band obtained from six-band $k \cdot p$ calculations for common types of 1-GPa stresses: (a) unstressed, (b) biaxial tension, (c) longitudinal compression on (001) wafer, and (d) longitudinal compression on (110) wafer (note significant differences in stress induced band warping altering the effective mass). [Tho06]
Figure 5-9. Illustration of mobility enhancement due to band shift for (100) / [100] NMOS under transverse tensile stress.
Figure 5-10. Band shift for (100) / <110> longitudinal tensile stress.
Table 5-1  Measured long channel p-MOSFET piezoresistance coefficients in this work (in blue) compared against other works and against Smith’s [Smi52] bulk data in units of 10^{-12} cm^2/dyne. The data in blue refers to this work.

<table>
<thead>
<tr>
<th>Channel</th>
<th>P-MOSFET</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\pi_L$</td>
<td>$\pi_T$</td>
</tr>
<tr>
<td></td>
<td>$\pi_{11}$</td>
<td>$\pi_{12}$</td>
</tr>
<tr>
<td>[100]</td>
<td>[Smi52] 6.6</td>
<td>[Smi52] -1.1</td>
</tr>
<tr>
<td></td>
<td>[Col68] -1</td>
<td>[Col68] 23.8</td>
</tr>
<tr>
<td></td>
<td>[Uch04] 14.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>[Pan06] -1</td>
<td>[Pan06] 25</td>
</tr>
<tr>
<td>[this work]</td>
<td>9.10</td>
<td>-6.19</td>
</tr>
<tr>
<td>[110]</td>
<td>[Smi52] -71.8</td>
<td>[Smi52] -66.3</td>
</tr>
<tr>
<td></td>
<td>[Bra01a] 50.0</td>
<td>[Bra01a] -45.0</td>
</tr>
<tr>
<td></td>
<td>[Bra01b] 41.5</td>
<td>[Bra01b] -38.5</td>
</tr>
<tr>
<td></td>
<td>[Bra01c] 60.0</td>
<td>[Bra01c] -40.0</td>
</tr>
<tr>
<td>[Uch04]</td>
<td>78.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>[Col68] 23.8</td>
<td>[Col68] -38.2</td>
</tr>
<tr>
<td>[Pan06]</td>
<td>118</td>
<td>[Pan06] -66</td>
</tr>
<tr>
<td>[this work]</td>
<td>71.7</td>
<td>-33.8</td>
</tr>
</tbody>
</table>
Table 5-2  Measured long channel n-MOSFET piezoresistance coefficients in this work (in blue) compared against other works and against Smith’s [Smi52] bulk data in units of $10^{-12}$ cm$^2$/dyne.

<table>
<thead>
<tr>
<th>Channel</th>
<th>N-MOSFET</th>
<th>( \frac{\pi_L}{(\pi_{11}+\pi_{12}+\pi_{44})/2} )</th>
<th>( \frac{\pi_I}{(\pi_{11}+\pi_{12}-\pi_{44})/2} )</th>
<th>Biaxial ( \pi_{12} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>[100]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Smi52]</td>
<td>-102</td>
<td>[Smi52] 53.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Uch04]</td>
<td>-53.1</td>
<td></td>
<td></td>
<td>[Ham91] -54.7</td>
</tr>
<tr>
<td>[Pan06]</td>
<td>-59</td>
<td>[Pan06] 10</td>
<td>[Pan06] -64</td>
<td></td>
</tr>
<tr>
<td>[this work]</td>
<td>-38.55</td>
<td>-18.7</td>
<td>-24.5</td>
<td></td>
</tr>
<tr>
<td>[110]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Smi52]</td>
<td>-31.6</td>
<td>[Smi52] -17.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Uch04]</td>
<td>-46.2</td>
<td></td>
<td>[Uch04] -74</td>
<td></td>
</tr>
<tr>
<td>[Bra01a]</td>
<td>-45.0</td>
<td>[Bra01a] -35.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Bra01b]</td>
<td>-32.0</td>
<td>[Bra01b] -25.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Bra01c]</td>
<td>-50.0</td>
<td>[Bra01c] -35.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Ir104]</td>
<td>-39.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Deg04]</td>
<td>-34.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Ham91]</td>
<td>-14.7</td>
<td>[Ham91] -8.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Pan06]</td>
<td>-67</td>
<td>[Pan06] -38</td>
<td>[Pan06] -68</td>
<td></td>
</tr>
<tr>
<td>[this work]</td>
<td>-35.5</td>
<td>-14.5</td>
<td>-21.4</td>
<td></td>
</tr>
</tbody>
</table>
Table 5-3  Measured long channel n-MOSFET piezoresistance coefficients along [100] channel compared against a) bulk pi-coefficients measured on an n-type resistor on the same process and b) against Smith’s [Smi52] bulk data in units of 10^-12 cm²/dyne.

<table>
<thead>
<tr>
<th>N-MOSFET</th>
<th>[100]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(\pi_L)</td>
</tr>
<tr>
<td>((\pi_{11} + \pi_{12} + \pi_{44}))/2</td>
<td>((\pi_{11} + \pi_{12} - \pi_{44}))/2</td>
</tr>
<tr>
<td>This Work (Surface)</td>
<td>-38.55</td>
</tr>
<tr>
<td>This Work (Bulk)</td>
<td>-24.5</td>
</tr>
<tr>
<td>[Smi52]</td>
<td>-102</td>
</tr>
</tbody>
</table>

Table 5-4  Measured stress types needed for enhancing n/pMOSFET currents.

<table>
<thead>
<tr>
<th>Device</th>
<th>PMOS</th>
<th>NMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel</td>
<td>[100]</td>
<td>[110]</td>
</tr>
<tr>
<td>Longitudinal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compressive</td>
<td>Tensile</td>
<td>Tensile</td>
</tr>
<tr>
<td>Neg. change</td>
<td>+++</td>
<td>+++</td>
</tr>
<tr>
<td>Transverse</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compressive</td>
<td>Tensile</td>
<td>Tensile</td>
</tr>
<tr>
<td>Neg. change</td>
<td>+++</td>
<td>++</td>
</tr>
</tbody>
</table>
Summary

The work presented in this thesis is motivated by the fact that strain is being adopted in all modern day logic technologies to achieve performance improvement in CMOS technologies and the need for empirical device level piezoresistance coefficients by industry to quantify mobility enhancement. In Chapter 1, strain is introduced as a vector to extend Moore’s law and continue historical MOSFET performance enhancement. The relation between stress and strain is also outlined. For isotropic solids strain is a linear function of stress. The two are related to each other through the elastic properties of Si.

The relation between the piezoresistive effect and strained silicon MOSFET was elaborated in chapter 2, which serves as a foundation for understanding the experimental results. This is followed by a discussion on the need of piezoresistance coefficients and their relevance to understand strain-enhanced electron and hole mobility is presented in chapter 2. Appropriate numerical analysis of the effect of MOSFET carrier mobility under stress in terms of piezoresistance coefficients is provided. In chapter 3, the underlying physics of strained silicon MOSFETs has been presented. In equilibrium state silicon is isotropic in nature and strain introduces advantageous anisotropy in silicon by altering the valence and conduction band structures and/or scattering rates. Favorable carrier repopulation and reduced inter-valley scattering result in higher mobility enhancement for uniaxial stress compared to biaxial stress, and this enhancement is maintained even at high vertical electric field. SiGe in the source and drain, dual stress liners and stress memorization techniques have been introduced into state-of-the-art MOSFETS.
Mechanical stress can be introduced in the channel of a device to measure the change in the performance of device i.e. mobility. A discussion of the wafer bending techniques used in the experimental set-up of this work has been provided in chapter 4. The four-point bending and concentric ring bending techniques are elaborated upon with the relevant mathematical analysis and simulation results. The method to extract piezoresistance coefficients from drive current enhancement is also presented. The change in mobility is studied for different kind of stress types namely Uniaxial and Biaxial. Discussion on uncertainty analysis associated with stress-calibration has been presented. The main factors contributing to the uncertainty are identified as starting point of bending, micrometer displacement, wafer misalignment and variation of substrate thickness.

Chapter 5 presented the experimental results along with simple qualitative reasoning. The differences observed between the conventional bulk piezoresistance coefficients and those in the surface-inversion layer of the MOSFETs were reported. It was shown that is imperative to include the effect of vertical electric field and stress on the carrier mobility to develop insight into the reasons for mobility enhancement in the inversion-layer MOSFET. Results in this work indicate that: (1) transverse piezoresistance coefficients have different sign for bulk case and surface case; (2) surface longitudinal piezoresistance coefficient for [100] channel is much smaller than bulk value, which means that the [100] channel MOSFETs have smaller mobility enhancement than bulk Si and (3) uniaxial compressive stress on pMOSFETS shows little or no change in drive current enhancement. A simple qualitative physical model in terms of carrier repopulation, out of plane masses, band-splitting and scattering was used to explain the mechanisms responsible. A more numerically intensive and accurate physical treatment requires self consistent solution to Schrodinger's and Poisson's equations to calculate the sub-band energy
shifts in the confined MOSFET inversion layer for which the reader is referred elsewhere [Thp06][Fis04]. Finally, the effects of out-of-plane uniaxial stress were listed. An in-plane biaxial stress can be modeled by an equivalent out-of-plane uniaxial stress. It was shown that both split the bands in a similar way and hence cause the same mobility change. This fact is particularly useful in modeling process-induced strain applied on the gate of MOSFETS (on which an out-of-plane stress actually applies through a capping later etc.) by an equivalent in-plane biaxial stress that can be measured using existing mechanical wafer-bending techniques.

Today strain is being adopted in all high performance logic technologies. SiGe in the source and drain, dual stress liners and stress memorization techniques have been introduced into state-of-the-art MOSFETS. Strain will continue to scale well into future logic technology generations as the MOSFET enters the ballistic regime.

**Future Work**

In Chapter 1, it was established that strain will continue to scale as the MOSFET enters into the ballistic regime. It will be interesting to investigate if it would be possible to break the performance limit even when mobility saturates, through other strain effects like band splitting and carrier repopulation.

The need for more accurate stress calibration, especially for biaxial stress is essential. A strain gage used to directly measure the surface strain instead of force could eliminate some calibration errors and it is recommended as future work. 4 point probing technique that eliminates contact resistance instead of the 2 point probing technique for resistors is also recommended. Also, it would interesting to investigate the piezoresistance effects as a function of temperature and doping concentration and it is recommended as future work.
LIST OF REFERENCES


BIOGRAPHICAL SKETCH

Nidhi Mohta was born on April 12, 1983, in Madhya Pradesh, India. She has loving parents, Deepali and Mahendra Mohta. She received her Bachelor of Electronics and Communication Engineering in 2004 at University of Madras, Chennai, India. Her hobbies include reading, dancing, and astronomy.

Nidhi Mohta joined the Master of Science program in the Electrical and Computer Engineering Department at University of Florida in fall 2004. She has been working as a research assistant with Dr. Scott Thompson and the SWAMP Center since 2005. She is currently interning with the Process Technology and Collateral Team in Intel Incorporation, Folsom, California.