HYSTERETIC MODULATION FOR POINT OF LOAD APPLICATION

By

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by

Santanu K. Mishra
To My Grandparents
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Advancement in semiconductor technology has enabled the modern communication and
data processing integrated circuits (ICs) to improve speed and integration density. The power
supply to these ICs is continually required to deliver power at lower voltage and with stringent
regulation requirements. Dynamic behavior of the power supply is normally improved by
feeding the dynamic variables, such as the inductor current and the output voltage of the
converter, into the pulse width modulator (PWM). Very fast dynamic response can be achieved
by using both the peak and valley of the output voltage ripple to determine the switching
instants, leading to the class of hysteretic modulators.

The requirement to have lower supply voltage for the ICs also tightens the output voltage
ripple requirement. In order to meet these requirements, capacitors with small equivalent series
resistance (ESR) are used. This makes the natural output voltage ripple of the supply very small
and corrupted for proper hysteretic operation. This dissertation describes a modulation scheme
for modulator carrier wave generation from converter voltages with added dynamic variables.
The resulting hysteretic modulator, identified here as the synthetic ripple modulator (SRM),
allows proper hysteretic operation even with very small and noisy output voltage ripple.
The steady-state operation of the SRM is derived and experimentally validated. Critical design parameters affecting the steady-state operation, such as the switching frequency, are quantified and validated. Small signal modeling technique is applied in order to characterize the dynamic behavior of the modulation scheme. Design equations are developed to device a comprehensive design technique for optimized transient response with minimum number of output capacitor. Average models are developed to help predict the steady-state and dynamic behavior of the modulator for faster simulation with minimal computational time.

A synchronous buck converter with a 10.5 V input and 1.8 V/15 A output rating is designed to verify the steady-state and dynamic equations. The response of the VRM to dynamic load transition is verified with a 15 A load current step at a slew rate of 15 A/µs. Transients results show a 65 mV step-down overshoot and a 37 mV step-up undershoot in output voltage, which matches very closely with the prediction. Results prove the superior response speed of the SRM without the inherent problems of the conventional hysteretic modulators.
CHAPTER 1
INTRODUCTION

Research Background

The ever-advancing field of data processing and communication poses new challenges for power supplies in these systems. The integrated circuit (IC) chips are continually powered by lower supply voltage. The low supply voltage not only increases the speed and integration density of the IC, but it also reduces the power consumption per clock cycle [1-4]. The increase in speed and integration density poses a high slew rate load for the power supply [5-10].

The fast dynamic characteristics and low supply voltage make the voltage regulation more difficult in a centralized power system in which power to the ICs and processors is supplied from a single supply far away from the load. In order to tightly regulate the output voltage under static and dynamic load conditions, dedicated power supplies of different voltage and current ratings are located near to the load. The impact of parasitic impedance between the power supply and the load on voltage regulation is reduced by this architecture [11-13].

For high-end computing and data communication applications, multiple processors are commonly used on one motherboard. Each processor demands very high current at a very low voltage. In order to efficiently supply power to this system, distributed power architecture (DPA) is used, as shown in Figure 1-1 [14-16]. This architecture is comprised of a number of isolated voltage regulator modules (VRMs) powered from a 48-V fully or quasi-regulated rail. Each microprocessor is powered from a fully regulated isolated VRM in proximity.

In order to reduce the cost and size of the power delivery system, intermediate bus architecture (IBA) is sometimes preferred, as shown in Figure 1-2. This system uses only one isolated power supply, which is known as the “bus converter”. Depending on the application, the bus converter can be unregulated, semi-regulated, or fully regulated [17-18]. Several non-
isolated point-of-load (POL) power supplies are powered from this bus converter and located near the load. The advantages of an IBA over a DPA can be summarized as follows:

- Lower overall cost
- Smaller board area
- Higher efficiency
- Higher reliability
- Faster transient response

Various topology choices are available for POL, as shown in Figure 1-3. A low drop-out regulator (LDO) can be used when the differential voltage between the input and output is small, and the output current requirement is below 6 A. The LDOs exhibit poor dynamic performance. With an increase in the power rating and voltage conversion ratio, switching regulators prove more efficient.

Apart from the location of the power supply with respect to the load, the choice of control strategy and number of output capacitor also have a significant effect on the dynamic performance of the POL [19-20]. As the real estate on a motherboard is limited and expensive, it has prompted a significant research effort on devising new control schemes which will require a lower output capacitor without compromising dynamic response. Ultimately, any control scheme and capacitor configuration need to adhere to the stringent requirements that the POL has to satisfy, which can be summarized as follows:

- High power density
- High current density
- Low output voltage deviation in both steady-state and transient load condition
- Very low output voltage ripple
- Small size
• Lightweight by using smaller filter inductor and capacitor
• Improved thermal performance and efficiency

**Unique Requirements for POL Converters**

Most POLs with output load demand above 6 A use the synchronous buck topology. The schematic and fundamental waveforms of this topology are shown in Figure 1-4. The output voltage is determined by the fraction of a switching cycle, \( DT_s \), for which the top switch is on. The bottom switch receives the complement of the top switching signal with some delays to avoid grounding of the supply.

The inductor and the capacitor form the low pass filter for this topology. As the power output increases, a single phase synchronous buck topology becomes highly inefficient due to increased losses, and it requires a large number of output capacitors to meet the dynamic requirements, which make it impractical [21-24].

The amount of output capacitor and filter size for a high output load can be minimized by employing the interleaving technique in a multi-phase architecture. The interleaving technique, as shown in Figure 1-5, is implemented by connecting many single phase converters in parallel and phase-shifting their switching. The primary advantage of this technique is the decreased magnitude and increased frequency of the output voltage ripple. Current sharing between phases is very important for this architecture in order to maximize the thermal performance and reduce the stress on any particular phase. The master control IC normally ensures equal current distribution and phase shifting of the phases. The overall power rating of the output load decides the number of interleaved phases [25-27].

**Different Control Options for POL Converters**

There are many control techniques to choose from for a POL, depending on the design requirements. The basic approach in any control technique is to vary the switching time of the
top switch in a synchronous buck converter in such a way that the output voltage follows a constant reference voltage. This section discusses some of these control techniques and their implications.

**Constant Switching Frequency Pulse-width Modulation**

The voltage mode control is the most common control technique for a switching converter. In this scheme, a constant frequency ramp is compared with a constant $V_{\text{cmd}}$ signal through an analog comparator to generate the switching pulses for the top switch. The fundamental waveforms and the expression for duty ratio are shown in Figure 1-6. The constant $V_{\text{cmd}}$ signal is the output of a high gain error amplifier, which has the output voltage and a constant reference as its input. This scheme is optimized for regulation of output voltage and is not the best in terms of dynamics [28-30].

In order to out-perform the conventional pulse-width modulation (PWM) approach in terms of speed, converter dynamic variables can be injected into the feedback loop. The average current mode control, as shown in Figure 1-7, is one such example. The inductor current is sensed and fed back to an error amplifier which compares this sensed current with a constant reference voltage. Similar to the conventional PWM, the output of the current error amplifier is compared to a constant frequency ramp.

Unlike conventional PWM controllers, the average current mode control has two feedback loops. The inner loop is the current feedback loop, known as the “modulation loop.” The outer loop is the voltage feedback loop, known as the “regulation loop” [31-33].

**Variable Switching Frequency Pulse-width Modulation**

The operating frequency is load-dependent for this class of PWM. At light load the reduction in switching frequency improves the efficiency. Other advantages include superior transient response, low audio susceptibility, and simpler dynamics [34].
Figure 1-8 shows the voltage hysteretic modulation scheme [35-36]. The basic idea is to use the output voltage ripple as a PWM ramp. The peak and valley of the ramp are used to generate the switching instants with the help of a hysteretic comparator. In order to make the switching immune to noise, a higher hysteretic window needs to be used, making the output voltage ripple bigger.

Unlike voltage hysteretic control, current hysteretic modulation uses the sensed inductor current as the PWM ramp, as shown in Figure 1-9. In a constant on-time control scheme, the on time of the upper switch is fixed and the off-time is decided by a constant reference and slope of the PWM signal [37-39].

Figure 1-10 shows the sensed current signal used as the ramp. The external ramp signal can also be used for this modulation scheme. Figure 1-11 describes the constant off-time control technique in which the off-time of the upper switch is constant and the on-time is varied according to a reference voltage.

The switching frequency, command-to-duty ratio, and the control law for the previously mentioned variable frequency modulators are delineated in Table 1-1. As the equations suggest, the switching frequency is a function of input voltage $V_{\text{in}}$ and output voltage $V_{o}$ for all these variable switching frequency schemes. It can also be seen that the output voltage has a linear dependence on the command signal $V_{\text{cmd}}$.

**V$^2$-control Scheme**

The V$^2$-control scheme uses a combination of an output voltage ripple and an external ramp to generate the triangular carrier waveform for the PWM [40-41]. Another modification of this scheme uses only the output voltage ripple in combination with a hysteretic comparator to generate the PWM signal for the buck switches. The basic circuit and operational waveform of this control technique are shown in Figure 1-12 and Figure 1-13. Since the output voltage is
affected by the load transient, the level of the ramp changes with load. A step change in the ramp signal affects the duty cycle immediately before the slow error amplifier can react.

**Enhanced V²-control Scheme**

As an enhancement to the V²-control technique, the enhanced V²-control technique uses the sensed inductor current instead of the external ramp signal [42]. The schematic of this scheme is shown in Figure 1-14. The slope of the inductor current is affected by the input voltage. Any variation in the input voltage therefore affects the duty cycle within one cycle as shown in Figure 1-15. The use of output voltage for the PWM ramp ensures an excellent transient performance, which is similar to the V²-control technique.

**Focus of This Dissertation**

As previously described, the next generation of POLs tends to use fewer output capacitors to save motherboard space. It also tends to use a capacitor with lower electrostatic resistance (ESR) to minimize output voltage ripple. In a power supply employing lower ESR capacitors, the output voltage ripple is not a triangular wave. Figure 1-16 shows the output voltage ripple of a power supply with a low ESR capacitor. The parabolic segments are created by the integration of triangular current by an ideal capacitor and jumps are created by equivalent series resistance (ESL). The peak and valley of the ripple therefore no longer coincide with the switching instants and with small peak-to-peak magnitude, the noise susceptibility increases.

This dissertation describes a modulation scheme for a modulator carrier wave generation from converter voltages with added dynamic variables. The resulting hysteretic modulator, identified here as the “synthetic ripple modulator” (SRM), allows a proper hysteretic operation even with a very small and noisy output voltage ripple.

The steady-state operation of the SRM is derived and experimentally validated. Critical design parameters affecting the steady-state operation, such as the switching frequency, are
quantified and validated. Small signal modeling technique is applied in order to characterize the
dynamic behavior of the modulation scheme. Design equations are developed to devise a
comprehensive design technique for an optimized transient response with a minimum number of
output capacitor. Average models are developed to help predict the steady-state and dynamic
behavior of the modulator for faster simulation with minimal computational time.

Chapter 2 describes the basic circuit and operation of the SRM. This section also
describes all the individual blocks to realize the SRM.

Chapter 3 discusses the design-oriented steady-state design equations for the SRM. The
command-to-duty transfer function and switching frequency are quantified. Average models are
developed and design methodology for this modulator is presented and verified using a 1.8 V/10
A prototype.

Chapter 4 quantifies the dynamic behavior of the SRM. The small signal command-to-
output, audio-susceptibility, and output impedance equations are developed. These equations are
used to design the feedback loop. The transient behavior of the SRM and its dependence on the
design factors are also described in this section.

Chapter 5 presents a comprehensive design solution for the modulator. A 1.8 V/ 15 A
prototype is used to verify the developed design equations. Experimental verification shows a
very good resemblance between the theory and practical results.
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<td>Voltage hysteresis</td>
<td>$f_s = \left(1 - \frac{V_o}{V_{in}}\right) \frac{V_o}{L} \frac{esr}{V_{hys}}$</td>
<td>$D = \frac{V_{cmd}}{V_{in}}$</td>
<td>$V_{cmd} = V_o$</td>
</tr>
<tr>
<td>Current Hysteresis</td>
<td>$f_s = \left(1 - \frac{V_o}{V_{in}}\right) \frac{V_o}{L} \frac{K_2}{V_{hys}}$</td>
<td>$D = \frac{V_{cmd} \ast R_o}{K_2 \ast V_{in}}$</td>
<td>$V_{cmd} = \left(\frac{K_2}{R_o}\right) \ast V_o$</td>
</tr>
<tr>
<td>Constant-on Time</td>
<td>$f_s = \frac{V_o}{V_{in}} \ast \frac{1}{T_{on}}$</td>
<td>$D = \frac{V_{cmd} + \frac{V_{in} \ast T_{on} \ast K_2}{2 \ast L}}{K_2 \ast V_{in} \ast \left(\frac{1}{R_o} + \frac{T_{on}}{2 \ast L}\right)}$</td>
<td>$V_{cmd} = \left(\frac{K_2}{R_o} - \frac{K_2 \ast D \ast T_{on}}{2 \ast L \ast D}\right) \ast V_o$</td>
</tr>
<tr>
<td>Constant-off Time</td>
<td>$f_s = \left(1 - \frac{V_o}{V_{in}}\right) \ast \frac{1}{T_{off}}$</td>
<td>$D = \frac{V_{cmd}}{K_2 \ast V_{in} \ast \left(\frac{1}{R_o} + \frac{T_{off}}{2 \ast L}\right)}$</td>
<td>$V_{cmd} = \left(\frac{K_2}{R_o} + \frac{K_2 \ast T_{off}}{2 \ast L}\right) \ast V_o$</td>
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Figure 1-1. Schematic of distributed power architecture.
Figure 1-2. Schematic of intermediate bus architecture

Figure 1-3. Power supply regulators and its application domain.
Figure 1-4. Single phase synchronous buck converter.

Figure 1-5. Interleaving of phases in a synchronous buck converter.
Figure 1-6. A conventional PWM.

\[
D = \frac{V_{cmd}}{V_{pk}}
\]

Figure 1-7. Average current mode control implementation as a conventional PWM.

Figure 1-8. Voltage hysteretic modulation and control waveforms.
Figure 1-9. Current hysteretic modulation and control waveforms.

Figure 1-10. Constant-on time modulation and control waveforms.

Figure 1-11. Constant-off time modulation and control waveforms.
Figure 1-12. $V^2$-control architecture.

Figure 1-13. Operational waveforms of the $V^2$-control architecture.
Figure 1-14. Enhanced V²-control architecture.

Figure 1-15. Impact of supply voltage variation on the enhanced V²-control architecture.
Figure 1-16. Output voltage ripple with a low ESR capacitor.
CHAPTER 2
CIRCUIT AND OPERATION

This chapter describes the fundamental operation and operational waveforms of the SRM driving a synchronous buck converter. The basic building blocks for the SRM are described, and the condition for proper operation of the modulator is analyzed.

Circuit Realization for the SRM

Figure 2-1 shows the schematic of a synchronous buck converter driven by the SRM. The gate-driver is fed from the output of the SRM. The gate-driver generates a complementary gate-drive signal that drives switches of the synchronous buck converter. As previously described, the basic idea is to generate an artificial ripple which enables proper hysteretic mode operation, even when the natural ripple of the output is small, corrupted, and buried under a lot of noise. The artificial ripple is synthesized by regenerating the voltage across the inductor with a definite gain and adding it to the output voltage. The regeneration of this voltage is performed by feeding the voltage across the inductor into a transconductance amplifier, the output of which is fed into a resistor capacitor network level shifted by the output voltage.

The main constituents of the SRM are a ripple synthesizer and a hysteretic compactor. In more general terms, the ripple synthesizer is essentially an integrator formed by a transconductance amplifier with gain $g_{m\text{Mod}}$ and a capacitor $C_{\text{mod}}$. The voltage across the $C_{\text{mod}}$ is the synthetic ripple being sought. This ripple is stacked on the output voltage $v_o$ to generate the modulating signal $v_{\text{mod}}$ for the hysteretic comparator. As shown in Chapter 1, the carrier waveform needs to be piece-wise linear in order to exhaust an ideal hysteretic PWM operation. As shown in Figure 2-2, the synthetic ripple is piece-wise linear and triangularly shaped compared to the natural output voltage ripple. This triangular modulation signal results in smooth single point intersection of the hysteretic limits and the carrier wave for proper commutation of
the power switches. The carrier magnitude can be controlled to have a much higher amplitude than the natural ripple.

Under ideal operating conditions, the hysteretic limits are placed symmetrically around the reference signal $V_{\text{cmd}}$ [43]. The rising edge of the synthetic ripple defines the on-time of the top switch UFET, whereas the falling edge defines the freewheeling interval during which the bottom switch LFET is on.

The resistor, $R_{\text{cmd}}$, absorbs the DC current generated by the trans-conductance amplifier from the DC voltage across the inductor. Thus, $R_{\text{cmd}}$ and inductor DC resistance $r_L$ provide the low frequency gain of the integrator. It will be shown later that the low frequency gain can be used to control the DC performance of the modulator.

Even though voltage across the inductor is used to generate the carrier wave for the ripple regulator, in general, any AC converter waveform can be used for this carrier wave generation. The AC converter waveform can also be bonded to virtually any variable that needs to be regulated to realize fast and linear dynamic response [44].

**Alternate Form of SRM Realization**

An alternate way of realizing the SRM is shown in Figure 2-3 [45]. Instead of sensing the voltage across the inductor, a pseudo buck converter is realized within the control circuit itself. When the PWM is high, the top field-effect transistor (FET) conducts. The control circuit imitates this behavior by having a differential voltage of $(V_{\text{in}}-V_o)$ across the transconductor, which creates the positive slope of $V_{\text{mod}}$. Similarly, when the bottom FET is turned on, the voltage across the transconductor is given by $(-V_o)$, which in turn creates the negative slope for $V_{\text{mod}}$. The advantage of this circuit is that no inductor current sensing is required. The operational waveforms are shown in Figure 2-4. It can also be noted that the lower hysteretic levels are
defined as the $V_{cmd}$, which is the output of the voltage error amplifier. The switching frequency can be varied by changes in the $V_{hys}$ signal.

One of the major drawbacks of the architecture is that the output voltage is not added to the synthetic ripple at the output of the transconductor. This eliminates the load current feed-forward mechanism, which is a major catalyst for good dynamic performance. Because the circuit does not use any high frequency signal from the converter, it is very easy to implement on a chip.

**Ripple Synthesizer**

The Howland current pump [46-47] is an extremely versatile way to realize a transconductance amplifier, as shown in Figure 2-5. The simplest scheme uses one Opamp and four resistors. The relationship between the output current and input voltages can be expressed as

$$I_{mod} = (V_1 - V_2) \times \left( \frac{1}{R} + \frac{1}{R_1} \right)$$  \hspace{1cm} (2.1)

Proper matching of external resistors is very important for this configuration to reduce feedback error. As shown in Figure 2-6, an extra Opamp can be used to minimize this feedback error. The expression for the output current in terms of the differential input voltage can be derived as

$$I_{mod} = (V_{phase} - V_o) \times \left( \frac{R_2}{R_2 + 2R_1} \right) \times \left( \frac{1}{R_m} \right)$$  \hspace{1cm} (2.2)

This circuit is used for the implementation of the ripple synthesizer. Few design criteria need to be followed while designing the transconductance amplifier for this application. The input voltage to the ripple synthesizer is a high frequency switching signal. The amplitude of this signal varies between the differential voltage ($V_{in} - V_o$) and $-V_o$ every switching cycle because
most of today’s POL applications use only one bias power supply, the following basic design rules must be followed for proper operation of the ripple regulator.

- At any given instant in a switching cycle, the voltage at the input and output nodes for the Opamps in the ripple regulator must be within the common mode input range and output voltage swing specification.

- The bandwidth of the Opamps must be sufficiently larger than the switching frequency of the buck converter. For example, a 1 MHz switching frequency buck regulator should use Opamps with bandwidth 30 MHz or above.

- The slew rate of the Opamp must be sufficient to support the high frequency input of the ripple regulator.

- The input bias currents $I_{\text{bias}}$ for the Opamps must be much smaller than the output current $I_{\text{mod}}$. This will ensure ideal operation of the ripple regulator.

Based on the characteristic and design criteria of the SRM either AD8065/8066 or AD8057/8058 is chosen as the Opamp for the ripple regulator. To reduce a mismatch error, precision 1% resistors are used. The important characteristics of the Opamp with a single 5 V bias are shown in Table 2-1.

**Hysteretic Comparator**

The hysteretic comparator for this application is implemented using a two-comparator circuit, as shown in Figure 2-7. The advantage of this circuit is that the hysteretic voltage $V_{\text{hys}}$ can be varied as per design requirements. The operational waveforms of this comparator are given in Figure 2-8. The adder and subtractor circuit generate the upper and lower hysteretic levels for the SRM, respectively. These levels are compared with $v_{\text{mod}}$ to generate the set and reset signal for the NAND flip-flop. The inputs of this flip-flop are inverted. The output of this flip-flop is the PWM signal for the gates of the synchronous buck converter. As with any comparator and digital circuit, there is a finite amount of delay from the modulation voltage $V_{\text{mod}}$.
to the PWM output $V_{\text{pwm}}$. This signal is fed into the gate-driver which has its own delay due to the large capacitive load posed by the input of the power FET.

**Sufficient Condition for Proper SRM Operation**

A sufficient condition for an ideal operation of the SRM is that the slope of $v_{\text{cmd}}$ should be much smaller than the slope of $v_{\text{mod}}$. This condition arises from the fact that the output voltage of the error amplifier $v_{\text{cmd}}$ could contain the amplified output voltage ripple. As a result, this signal may not be a purely DC signal, and it contains the switching frequency noise. If the noise is large enough, it will result in an undesired commutation of the power switches.

Figure 2-9 shows a condition where the slope of $v_{\text{cmd}}$ is more than that of $v_{\text{mod}}$. The sufficient condition for proper PWM operation for the SRM can therefore be identified as

$$\frac{dv_{\text{mod}}}{dt} \leq \frac{dv_{\text{cmd}}}{dt} \quad (2.3)$$

The condition of having the slope of $v_{\text{mod}}$ less than that of $v_{\text{cmd}}$ is useful when it is desired to prolong the on-time of any of the switches. It can be shown that the condition in (2.3) is satisfied when:

$$G_{\text{fEA}}(f_s) < \frac{g_{\text{mMod}} \cdot L}{C_{\text{mod}} \cdot \text{esr} C_o} \quad (2.4)$$

$$R_{\text{mod}} = \frac{g_{\text{mMod}} \cdot L}{C_{\text{mod}}} \quad (2.5)$$

$G_{\text{fEA}}(f_s) =$ Gain of the error amplifier at the switching frequency

$\text{esr} C_o =$ ESR of the filter capacitor for the power stage

$g_{\text{mMod}} =$ Transconductance of the ripple regulator

In summary, this chapter presents the basic building blocks of the SRM. The non-idealities of the blocks, that are critical to fundamental SRM operation, are delineated. Alternate
architecture to generate the synthetic ripple is presented. The design condition, for ideal PWM operation of the SRM, is described in form of a design equation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>AD8066</th>
<th>AD8057</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3db Bandwidth</td>
<td>155 MHz</td>
<td>325 MHz</td>
</tr>
<tr>
<td>Common mode Input Voltage range</td>
<td>0-2.4 V</td>
<td>0.9-3.4 V</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>5 pA</td>
<td>0.5 µA</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>0.03 V-4.95 V</td>
<td>0.9 V-4.1 V</td>
</tr>
<tr>
<td>Slew rate</td>
<td>160 V/us</td>
<td>700 V/us</td>
</tr>
</tbody>
</table>

Figure 2-1. Synchronous buck converter controlled by the SRM.
Figure 2-2. Operational waveforms for the SRM.

Figure 2-3. Alternate way to realize the synthetic ripple modulator.
Figure 2-4. Operational waveforms for the alternate synthetic ripple generator.

Figure 2-5. Simplified implementation of Rowland voltage controlled current source.
Figure 2-6. Rowland voltage controlled current source with reduced feedback error.

Figure 2-7. Implementation of hysteretic comparator.
Figure 2-8. The switching waveforms of the hysteretic comparator.

Figure 2-9. The SRM operating condition with \( (\frac{dV_{cmd}}{dt}) > (\frac{dV_{mod}}{dt}) \).
CHAPTER 3
STEADY-STATE ANALYSIS OF SRM

The analytical results for the steady-state operation of the SRM are derived in this section. The DC control law, command-to-duty transfer function, and switching frequency equations are derived in terms of the modulator design parameters ($g_{\text{mmod}}$, $V_{\text{hys}}$, $R_{\text{cmod}}$, $C_{\text{mod}}$) and converter parameters ($r_{\text{L}}$, $L$ etc.), assuming there is continuous conduction mode (CCM) operation of the synchronous buck converter.

Control Law

The control law for the SRM describes the relationship between the output voltage $V_o$ and the command signal $V_{\text{cmd}}$. Figure 3-1 shows the DC schematic of the SRM, which can be used to derive the steady-state performance of the modulator. In the last section, the steady-state waveforms of the SRM are described, assuming there is an ideal operation of the modulator. In practice, delays in the comparator, gate-drivers, and non-ideal switches result in operational waveforms shown in Figure 3-2. The time periods $t_1$ and $t_1'$ are the delays incurred by the non-ideal behavior of the circuit. As a result, $v_{\text{mod}}$ is no longer confined between $V_{\text{mod+}}$ and $V_{\text{mod-}}$ and has a new peak identified as $V_{\text{mod++}}$ and $V_{\text{mod--}}$. The differential ($V_{\text{mod++}}-V_{\text{mod+}}$) is larger than ($V_{\text{mod--}}-V_{\text{mod-}}$) for POL applications, where $V_o$ is much smaller than $V_{\text{in}}$. Effectively, $V_{\text{cmd}}$ changes to $V_{\text{cmdE}}$ and $V_{\text{hys}}$ changes to $V_{\text{hysE}}$.

By definition

$$V_{\text{cmdE}} = \frac{(V_{\text{mod++}} + V_{\text{mod--}})}{2} \quad (3.1)$$

$$V_{\text{hysE}} = V_{\text{mod++}} - V_{\text{mod--}} \quad (3.2)$$

Using Figure 3-2, the equations for the command and hysteresis signal are derived as
\[ V_{\text{cmdE}} = V_{\text{cmd}} + \frac{g_{\text{mod}}}{2 \cdot C_{\text{mod}}} ((V_{\text{in}} - V_o) \cdot t_1 - V_o \cdot t_1') \]  

(3.3)

\[ V_{\text{hysE}} = V_{\text{hys}} + \frac{g_{\text{mod}}}{C_{\text{mod}}} ((V_{\text{in}} - V_o) \cdot t_1 + V_o \cdot t_1') \]  

(3.4)

If the delays \( t_1 \) and \( t_1' \) are comparable, \( V_{\text{cmdE}} > V_{\text{cmd}} \) when \( V_{\text{in}} > 2V_o \), \( V_{\text{cmdE}} < V_{\text{cmd}} \) when \( V_{\text{in}} < 2V_o \). It can also be concluded from (3.4) that the overall hysteresis voltage is dependent on the input voltage \( V_{\text{in}} \), assuming a comparable delay of \( t_1 \) and \( t_1' \).

The DC control law can be derived by equating the DC value of \( V_{\text{mod}} \) and the DC value of \( V_{\text{cmdE}} \) and is given by:

\[ V_{\text{cmdE}} = V_o + I_o \times (r_L \cdot g_{\text{mod}} \cdot R_{\text{mod}}) \]  

(3.5)

The above equation identifies the droop resistance as

\[ R_{\text{droop}} = r_L \cdot g_{\text{mod}} \cdot R_{\text{mod}} \]  

(3.6)

Using (3-5) and (3-6), the relationship between \( V_o \) and \( V_{\text{cmd}} \) can be expressed as follows.

\[ V_o = \frac{V_{\text{cmdE}}}{1 + \frac{R_{\text{droop}}}{R_o}} \]  

(3.7)

It can be seen that \( V_o \) varies linearly with \( V_{\text{cmdE}} \) and is load dependent. As shown in (3.5), the SRM naturally implements droop control with \( R_{\text{droop}} \) being the droop resistance. The design of feedback loop is generally facilitated by the linear relationship between \( V_o \) and \( V_{\text{cmd}} \).

**Command-to-duty Transfer Function**

The command-to-duty transfer function describes the switching intervals for the synchronous buck converter in terms of the modulator parameters and input voltage. The minimum and maximum switching time that can be achieved by the modulator varies depending on the control circuit, non-idealities such as delay time, bandwidth limitation, common mode
range, and output swing for Opamps. The command-to-duty transfer function gives an insight into this switching period and helps the design around these extremes.

The basic relationship between the duty and output voltage for a synchronous buck converter is expressed as

\[
D = \frac{V_o}{V_{in}}
\] (3.8)

Using (3.7) and (3.8), the equation for the duty cycle can be expressed in terms of the command signal as follows:

\[
D = \frac{V_{cmdE}}{V_{in} \times \left(1 + \frac{R_{droop}}{R_o}\right)}
\] (3.9)

The duty cycle D is inversely proportional to the \(V_{in}\) and load current. If the switching frequency is fixed, this equation provides an insight into the extreme \(V_{in}\) and load current that can be supported by the modulator.

**Switching Frequency**

The switching frequency is inversely proportional to the switching time \(T_s\). Using Figure 3-2 it can be shown that

\[
T_s = t_{on} + t_{off} = \frac{V_{hySE}}{\frac{dv_{mod}}{dt}\bigg|_{t_{on}} - \frac{dv_{mod}}{dt}\bigg|_{t_{off}}}
\] (3.10)

where

\[
\frac{dv_{mod}}{dt}\bigg|_{t_{on}} = g_{mMod} \cdot \left(\frac{V_{in} - V_o}{C_{mod}}\right)
\] (3.11)

\[
\frac{dv_{mod}}{dt}\bigg|_{t_{off}} = -\frac{g_{mMod} \cdot V_o}{C_{mod}}
\] (3.12)
Substituting (3.11) and (3.12) into (3.10) yields the steady-state switching frequency expression as

$$f_s = \left[1 - \frac{V_o}{V_{in}}\right] \cdot \frac{V_o}{V_{hysE}} \cdot \frac{g_{mMod}}{C_{mod}}$$ (3.13)

The switching frequency is inversely proportional to the hysteresis voltage $V_{hysE}$ and the ripple regulator capacitor $C_{mod}$. The transconductance and input voltage have direct proportionality to switching frequency. Unlike $V^2$-control, the switching frequency is not dependent on the converter parameters. It can also be noted that the SRM is a variable frequency modulator and its switching frequency varies with the change in output voltage. This characteristic is of particular importance for POL application because the power supply generally encounters high slew transient load, which causes an instantaneous change in the output voltage during transient. Another important advantage of having a variable frequency modulation is that the switching frequency reduces at light load when the converter goes into the discontinuous conduction mode. This improves the light load efficiency and elongates the battery life.

**Steady-state Modeling of SRM**

The average models can result in a reduced computational time in simulation and enhance the design cycle speed. The average model for the SRM is shown in Figure 3-3. The model describes the modulator as a high gain Opamp, which forces its input to be at the same potential. The synchronous buck converter is modeled with the popular three-terminal model [48-49].

The output of the high gain Opamp essentially generates a voltage to make $V_{cmd}$ and $V_{mod}$ equal and is fed to the model of the converter. Figure 3-4 shows the comparison between the real-time model and the average model to a step change in $V_{cmd}$. The response of the average model to this step change in command signal $V_{cmd}$ is similar to the response of the real-time
model, but with a significant reduction in computation time. It is worth noting that the model is valid both under time and frequency domain which facilitates the real-time and AC analysis of the modulator.

**Design Example**

The theory derived in this chapter is verified using a design example. The designed modulator drives a synchronous buck converter. The design of the SRM starts with the assumption that the power converter has already been designed, and the discrete semiconductor components used to implement the control blocks are known. The discrete semiconductors used for the design are tabulated in Table 3-1.

As outlined in Table 3-2, \( V_{hys} \) is selected first. In this case for this example, the hysteresis voltage is chosen much larger than the steady-state output voltage ripple on \( V_o \), 20 mV. In order to verify the design equations, \( V_{hys} \) was swept between 150 mV and 1.1 V although 0.7 V is listed in Table 3-2 as a nominal value.

The transconductor is designed such that the output current is much larger than the bias current. For this example, the output of the transconductance amplifier has a minimum \( I_{mod} \) of 135 \( \mu A \), which is much larger than the sum of all the bias currents.

To demonstrate that the SRM could provide more droop resistance than the resistance of the inductor, 40 m\( \Omega \) is specified for \( R_{droop} \). The droop resistance is used to calculate the \( R_{cmod} \) using (3.6). The switching frequency was swept between 300 kHz and 1 MHz although 420 kHz is specified as a nominal value in Table 3-2. The total delay \( t_1 \) is approximated from the datasheet to be 100 ns. The experimental waveforms shown in Figure 3-5 confirm this delay term. Using (3.4) and (3.13), \( C_{mod} \) was found to be 270 pF. Finally, \( V_{cmd} \) is found from (3.3) and (3.5) to be 2.12 V. As will be shown later, this voltage will automatically be set by an error amplifier by comparing the output voltage to a DC reference voltage.
Figure 3-5 shows the switch node voltage in comparison to the control signals. When the top FET is turned on, the level of $V_{\text{phase}}$ equals the input voltage $V_{\text{in}}$, which is 9.5 V for this design. A 100ns delay is observed between the instant $V_{\text{mod}}$ intersects $V_{\text{mod,in}}$, and the rise of switching node as predicted in Table 3-2. The rising and falling slope of the $V_{\text{mod}}$ signal is observed to be 2.13 V/µs and 0.5 V/µs respectively, as predicted by (3-11) and (3-12). Apart from the high frequency noise due to parasitic impedances, the phenomena underlying the derivations of the design equations are indeed observed on the experimental waveforms.

Figure 3-6 shows the control signals and the gate-drive signals for the top and bottom FET of the synchronous buck converter, with a higher value of hysteresis voltage. The maximum value of the bottom FET gate signals equals the 5 V gate-drive voltage provided by the gate-driver. However, the maximum value of the top switch gate-drive is about 14.5 V, which is 5 V higher than the $V_{\text{in}}$. The level-shift for the top FET gate-drive is provided by a bootstrap circuit, which is comprised of a diode and a capacitor, and is part of the gate-driver design. The effect of reduced $V_{\text{hys}}$ on the switching frequency is shown in Figure 3-7. With a hysteretic voltage of 0.3 V ($V_{\text{hys,E}}=0.7$ V), the switching frequency increases to 585 kHz.

The relationship between the $V_{\text{cmd}}$ and $V_o$ is shown in Figure 3-8. As the command signal reduces, there seems to be a bias current mismatch in the ripple regulator which contributes to an increase in the transconductance. The overall error is less than 10 %, which confirms a good correlation between the experiment and the theory. The measured relationship between $f_s$ and $V_{\text{hys}}$ is compared with the theoretical one, as shown in Figure 3-9. As the hysteresis voltage reduces, the noise exhausts significant impact on the switching frequency making it slightly higher than the predicted value.
### Table 3-1. Semiconductor Components used for Fabrication

<table>
<thead>
<tr>
<th>Parts</th>
<th>Attributes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opamps</td>
<td>AD8057 (SR: 1000 V/µs, BW: 325 MHz; I\textsubscript{bias}=0.5 µA; Analog)</td>
</tr>
<tr>
<td>Comparator</td>
<td>LT1720 (Delay: 13 ns; I\textsubscript{bias}: -6 µA; Linear Tech.)</td>
</tr>
<tr>
<td>Flip-Flop</td>
<td>74 ACT11074 (Delay: 9 ns; Texas Instruments)</td>
</tr>
<tr>
<td>Gate-driver</td>
<td>HIP 6603B (Delay: 30 ns; Transition time: 50 ns; Intersil)</td>
</tr>
</tbody>
</table>

### Table 3-2. Design Procedure for Example 1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Design Method</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_0$</td>
<td>Specified</td>
<td>1.8 V</td>
</tr>
<tr>
<td>$V_{hs}$</td>
<td>$V_0$ \text{Ripple}&lt;&lt;V_{hs}&lt;&lt;V_0$ Transient</td>
<td>0.7</td>
</tr>
<tr>
<td>$g_{mMod}$</td>
<td>$g_{mMod}V_0$&gt;&gt;Total Bias Current</td>
<td>75 µs</td>
</tr>
<tr>
<td>$R_{drop}$</td>
<td>Specified</td>
<td>40 mΩ</td>
</tr>
<tr>
<td>$n_L$</td>
<td>Specified</td>
<td>5 mΩ, 1 µH</td>
</tr>
<tr>
<td>$R_{cmd}$</td>
<td>Using (3.6)</td>
<td>107 kΩ</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Specified</td>
<td>420 kHz</td>
</tr>
<tr>
<td>$V_R$</td>
<td>Specified</td>
<td>9.5 V</td>
</tr>
<tr>
<td>$t_1$</td>
<td>Datasheet and measurements</td>
<td>100 ns</td>
</tr>
<tr>
<td>$C_{cmd}$</td>
<td>From (3.4) and (3.13)</td>
<td>270 pF</td>
</tr>
<tr>
<td>$I_0$</td>
<td>Specified</td>
<td>10 A</td>
</tr>
<tr>
<td>$V_{cmd}$</td>
<td>From (3.3) and (3.5)</td>
<td>2.12 V</td>
</tr>
</tbody>
</table>
Figure 3-1. DC schematic of the SRM driving a synchronous buck converter.

Figure 3-2. Impact of delay on the control signal and switching frequency.
Figure 3-3. Average modeling of the SRM driven buck converter.

Figure 3-4. Step response comparison between average and real-time simulation.

Figure 3-5. Experimental validation of the SRM design in example 1.
Figure 3-6. The control and gate-drive signals with a higher hysteresis voltage.

Figure 3-7. Effect of reduced hysteretic window on the switching frequency.
Figure 3-8. Command-to-output transfer function with a 7 A load.

Figure 3-9. Switching frequency as a function of the hysteresis voltage.
CHAPTER 4
DYNAMIC ANALYSIS OF SRM

The SRM is required to maintain a tight load regulation even under high slew rate load transitions. This chapter describes the design parameters that affect the dynamic performance of the SRM. The chapter starts with the derivation of control-to-output transfer function, which is instrumental in the design of the feedback loop. The audio susceptibility of the modulator is analyzed and verified. The output impedance characteristics of the modulator in open loop and closed loop configuration are derived. These results are used to design the voltage loop for stable operation and a fast transient response. The large signal transient behavior of the modulator and the synchronous buck converter are described. The design factors affecting the dynamic response of the modulator are identified. An optimized design methodology to obtain a very fast transient response is also described.

Control-to-output Transfer Function

The control-to-output transfer function is the small signal relationship between the command signal and the output voltage [29, 50-52]. The control method for the SRM is dependent on the inductor current and output voltage. The inductive impedance responsible for the generation of inductor sense current is given by:

$$z_L(s) = r_L + s \cdot L$$  \hspace{1cm} (4.1)

The output impedance of the synchronous buck converter is given by:

$$z_o(s) = R_o \parallel \left( \frac{1}{s \cdot C_o + esrC_o} \right)$$  \hspace{1cm} (4.2)

The load current is represented by the load resistance $R_o$. The output capacitor is represented by the filter capacitance $C_o$ and the equivalent series resistance $esrC_o$. The output impedance of the transconductance amplifier is given by:
\[ z_{\text{mod}}(s) = R_{\text{mod}} \cdot \left( \frac{1}{s \cdot C_{\text{mod}}} \right) \]  \hspace{1cm} (4.3)

Referring to Figure 4-1, the small signal expression of the carrier wave \( v_{\text{mod}} \) is given by:

\[ \hat{v}_{\text{mod}} = \hat{v}_o + \hat{i}_L \cdot \left[ z_L(s) \cdot g_{m\text{mod}} \cdot z_{\text{mod}}(s) \right] \]  \hspace{1cm} (4.4)

For a synchronous buck converter, the relationship between the inductor current and the output voltage is given by:

\[ \hat{i}_L = \frac{\hat{v}_o}{z_o(s)} \]  \hspace{1cm} (4.5)

As the input voltage to the hysteretic comparator track each other it can be expressed as

\[ \hat{v}_{\text{mod}} = \hat{v}_{\text{cmd}} \]  \hspace{1cm} (4.6)

The expression is valid for frequency range much below the switching frequency, and it is unable to predict the sub-harmonic behavior. The modeling technique is therefore sufficient for loop design for the SRM. Using (4.4)-(4.6), the expression for the control-to-output transfer function is given by:

\[ G_c(s) = \frac{\hat{v}_o}{\hat{v}_{\text{cmd}}} = \frac{z_o(s)}{z_o(s) + z_L(s) \cdot g_{m\text{mod}} \cdot z_{\text{mod}}(s)} \]  \hspace{1cm} (4.7)

Assuming a minimum value of \( R_o \gg \text{esr} C_o \), the above expression for the control-to-output transfer function can be expressed as

\[ G_c(s) = G_{co} \cdot \left( 1 + \frac{s}{\omega_c} \right) \frac{1 + \frac{s}{\omega_{\text{mod}}}}{1 + \frac{s}{\omega_o} \cdot \frac{R_o + R_{\text{drop}}}{\omega_{\text{mod}} + \omega_{\text{drop}}} + \frac{s^2}{\omega_o \cdot \omega_{\text{mod}}}} \cdot \left( 1 + \frac{R_o + R_{\text{drop}}}{\omega_c \cdot \omega_{\text{mod}} + \omega_o \cdot \omega_{\text{drop}}} \right) \]  \hspace{1cm} (4.8)

where

\[ G_{co} = \frac{R_o}{R_o + R_{\text{drop}}} \]  \hspace{1cm} (4.9)
\[
\omega_{esr} = \frac{1}{esrC_o \cdot C_o}
\]  
(4.10)

\[
\omega_{droop} = \frac{r_L}{L}
\]  
(4.11)

\[
\omega_{mod} = \frac{1}{R_{Cmod}C_{mod}}
\]  
(4.12)

\[
\omega_o = \frac{1}{R_oC_o}
\]  
(4.13)

The two zeros for this transfer function originate from the filter capacitor and the ripple regulator. The zero originating from the filter capacitor is at a very high frequency due to very low ESR. Figure 4-2 shows the comparison between the theory and the experimental results with parameters of Table 3-2. The results show the cancellation of a pole and a zero resulting in an effective single pole response. Figure 4-3 shows the effect of the load on the transfer function. With an increase in the load, there is a reduction in the low frequency gain of the transfer function, as can be deduced from (4.9). The increase in the load also results in a reduction in the dominant pole frequency. Due to an effective single pole response for the control-to-output transfer function, the loop design becomes very simple for this modulator.

**Output Impedance**

The open loop and closed loop output impedance of the modulator are derived in this section. The open loop output impedance transfer function is derived by setting the command signal \(v_{cmd}\) to a DC voltage. The overall philosophy is to inject a small signal current into the output node and compare it with the output voltage variation, as shown in Figure 4-1. The output voltage expression is given by:

\[
\hat{v}_o = z_o(s) \cdot (\hat{i}_o + \hat{i}_L)
\]  
(4.14)
The expression for the inductor current can be obtained from (4.4) by setting the small signal variation of the command signal to zero.

\[
\dot{i}_L = \frac{-\dot{v}_o}{z_L(s) \cdot g_{\text{mod}} \cdot z_{\text{mod}}(s)} \tag{4.15}
\]

Replacing (4.15) into (4.14) the open loop output impedance is derived as

\[
Z_{\text{OL}}(s) = \frac{\dot{v}_o}{L_{\text{OL}}(s)} = Z_{\text{OL}0} \cdot \left( \frac{1 + \frac{s}{\omega_{\text{ee}}}}{1 + \frac{s}{\omega_{\text{ee}}} + \frac{s}{\omega_{\text{drop}}} + \frac{1}{R_o + R_{\text{drop}}}} \right)^2 \tag{4.16}
\]

where

\[
Z_{\text{OL}0} = \frac{R_o \cdot R_{\text{drop}}}{R_o + R_{\text{drop}}} \tag{4.17}
\]

The open loop droop resistance \( R_{\text{drop}} \) is defined in (3.6). Figure 4-4 shows the validation of the open loop impedance derived above. The circuit parameters are shown in Table 3-2. The low frequency characteristic of this equation is dictated by the parallel combination of load resistance \( R_o \) and droop resistance \( R_{\text{drop}} \), as shown in (4.17). The high frequency characteristic is dictated by the parallel combination of \( R_{\text{mod}} \) and ESR of the filter capacitor. A low frequency zero originates from the DC resistance (DCR) \( r_L \) and the inductance \( L \) of the filter inductor. The second zero results from the ESR and the filter capacitor \( C_o \) and is at a very high frequency due to very low ESR. The two poles are close to each other and make the overall open loop output impedance a single pole response. Ideally, the overall output impedance is expected to be resistive in order to facilitate that the modulator meets the adaptive voltage regulation requirements [53]. Figure 4-5 shows the impact of variation in filter capacitor on the open loop output impedance. With the increase in filter capacitor, the first zero moves to the left and the poles move to the right, and they help reduce the output impedance variation over frequency.
The closed loop output impedance can be derived by taking into account the frequency response of the voltage error amplifier (VEA) on the command signal \(v_{cmd}\). The relationship between the command and the output voltage is given by:

\[
\hat{v}_{cmd} = G_{fEA}(s) \cdot \hat{v}_o
\]  

(4.18)

For type 2 compensation, \(G_{fEA}(s)\) can be expressed as

\[
G_{fEA}(s) = G_{fEA0} \cdot \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}}
\]  

\[
\omega_z = \frac{1}{(R_2 \cdot C_2)}, \quad \omega_p = \frac{1}{(R_2 \cdot C_3)}\quad G_{fEA0} = \frac{-R_3}{R_1 \cdot C_3}\]  

(4.19)

The previous equation can be combined with (4.4) and (4.14) to find the expression for the closed loop output impedance as follows

\[
(z_{out}(s))_{CL} = \frac{\left(z_o \cdot z_L \cdot g_{mMod} \cdot z_{mod}\right)}{\left(z_L \cdot g_{mMod} \cdot z_{mod}\right) + z_o(1 - G_{fEA}(s))}
\]  

(4.20)

Combining (4.2), (4.3), and (4.20), the expression for the closed loop output impedance is found out as

\[
(z_{out}(s))_{CL} = \frac{R_o \cdot R_{droop} \cdot \left(1 + \frac{s}{\omega_{str}}\right) \cdot \left(1 + \frac{s}{\omega_{droop}}\right)}{R_{droop} \cdot \left(1 + \frac{s}{\omega_{droop}}\right) + R_o \cdot \left(1 + \frac{s}{\omega_{mod}}\right) \cdot \left(1 + \frac{s}{\omega_{str}}\right) \cdot [1 - G_{fEA}(s)]}
\]  

(4.21)

In the above equation, \(G_{fEA}\) is the compensator transfer function and it can be designed to achieve the requisite closed loop output impedance. Low frequency behavior is dictated by the droop resistance and the high frequency characteristics by the ESR of the filter capacitor. Figure 4-6 shows the comparison of open loop and closed loop output impedance. It also signifies the impact of compensation design on the closed loop impedance [54].

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**Audio Susceptibility**

The effect of input voltage variation on the output is minimal for the SRM due to the feed-forward of the input voltage through the inductor current. As shown in Figure 4-7, any change in the input voltage results in a change in the slope of $V_{\text{mod}}$ effectively changing the duty cycle. For example, if there is an instantaneous increase in the input voltage, the duty cycle is reduced within one switching cycle and minimizes the impact on output voltage.

Using (4.4) and (4.14), it can be shown that the audio susceptibility of this modulator is zero.

$$G_{\text{vg}}(s) = \frac{v_o}{v_g \mid \dot{e}_{\text{cmd}} = 0} = 0$$

(4.22)

Experimental verification proves the instantaneous response of the control circuit to a sudden change in input voltage, as shown in Figure 4-8. The injected input voltage noise consists of both low frequency and high frequency variations. The high frequency noise seems to impact the output voltage as it is much higher than the switching frequency and the converter is unable to respond to this kind of noise.

**Loop Gain**

The loop gain expression is determined by combining (4.8) and (4.19) as follows:

$$G_{\text{loop}}(s) = G_{\text{co}} \cdot \left( 1 + s \left( \frac{1}{R_o + R_{\text{droop}}} \cdot \frac{1}{\omega_{\text{co}} + \omega_{\text{mod}} + \omega_{\text{droop}} + \omega_2} \right) \cdot \frac{1 + s/\omega_{\text{co}}}{1 + s/\omega_{\text{mod}} \cdot G_{\text{FEA}}(s)} \right)$$

(4.23)

This expression is used to design a fast and stable feedback loop for the SRM, as shown in Figure 4-9. The basic philosophy is to design the compensation in such a way that the zero of the compensator cancels out the single pole posed by the control-to-output transfer function. This can be effectively done by a type 2 compensator, as shown in Figure 4-10. The small signal
model for this compensator is also shown. Because reference voltage $V_{ref}$ is the DC voltage desired at the output, it has little impact on the small signal response.

**Input Impedance**

The input impedance is an extremely important parameter for POL application. As delineated in Chapter 1, the output of the bus converter acts as a supply for a number of POLs. The input impedance of the POL therefore gives an understanding into the loading of the output bus converter. As the excitation for this impedance is same as the audio susceptibility, $v_o$ is a constant. The input impedance for the SRM can be derived from the power conservation equation.

$$v_{in} \cdot i_{in} = v_{out} \cdot i_{out}$$

The small signal perturbation of this equation can be expressed as follows:

$$V_{in} \cdot \hat{i}_{in} + I_{in} \cdot \hat{v}_{in} = 0$$

Therefore, the input impedance is derived as

$$\frac{\hat{v}_{in}}{\hat{i}_{in}} \bigg|_{I_{in} = 0} = -\frac{V_{in}}{I_{in}} = -\frac{V_{in}^2}{V_o \cdot I_o}$$

(4.24)

The above equation defines the input impedance of the SRM as a constant with an 180° phase shift. The impedance characteristic is load dependent. With a higher load, the input impedance reduces. The input impedance characteristics for the example presented in Chapter 3 is shown in Figure 4-11. With an increase in load current the input impedance reduces.

**SRM Design Criterion**

In Chapter 2, the sufficient condition for proper PWM operation of the SRM was identified. This condition is quantified in terms of the parameters of the modulator and the converter in this section.
The peak-to-peak ripple on the command signal is the magnified version of the output voltage ripple through the voltage error amplifier. This can be expressed as

\[ \Delta v_{cmd} = G_{fEA}(f_{sw}) \cdot \Delta v_{out} \quad (4.25) \]

\( G_{fEA}(f_{sw}) \) = Gain of the compensator at the switching frequency

\( \Delta v_{out} \) = Output voltage ripple

The peak-to-peak ripple on the output of the transconductance amplifier can be expressed in terms of the transconductor gain as

\[ \Delta v_{mod} = G_{mod}(f_{sw}) \cdot (\Delta i_L) \quad (4.26) \]

\( G_{mod}(f_{sw}) \) = Ripple regulator gain at the switching frequency

\( (\Delta i_L) \) = Inductor current ripple

As per the condition of proper PWM operation

\[ G_{fEA}(f_{sw}) \cdot \Delta v_{out} < G_{mod}(f_{sw}) \cdot (\Delta i_L) \quad (4.27) \]

Assuming the ripple output voltage ripple to be much smaller than the inductor current generated ripple at the output of the transconductance amplifier, the above expression can be expressed as follows

\[ G_{fEA}(f_{sw}) < G_{mod}(f_{sw}) \cdot \left( \frac{\Delta i_L}{e_{sr}C_o \times (\Delta i_L)} \right) \quad (4.28) \]

The gain of the transconductance amplifier at the switching frequency is expressed as

\[ G_{mod}(f_{sw}) = sL \times g_{mMod} \times \frac{1}{sC_{mod}} = R_{mod} \quad (4.29) \]

The above equation assumes that at the switching frequency \( sL >> r_L \) and \( (1/s.C_{mod}) << R_{cmod} \). Using (4.28) and (4.29), the condition for the SRM design is derived as

\[ G_{fEA}(f_{sw}) < \frac{R_{mod}}{e_{sr}C_o} \quad (4.30) \]
The output voltage ripple is assumed to be much smaller than the magnitude of the $V_{mod}$ signal. In fact, that is one of the most important design criteria for proper hysteresis operation and a significant factor in development of this class of modulators. This equation quantifies the condition for proper operation of the SRM. Modern POLs are required to use less real estate on a motherboard, which limits the number to buck output capacitors. In order to further reduce the $esrC_0$, high-quality ceramic capacitors can be placed in parallel to the buck capacitor.

**Transient Modeling of SRM**

In this section, the response of the SRM to a high slew rate transient is analyzed and quantified in terms of switching time and switching frequency variation.

During steady-state operation, the inductor current has an average component and a high frequency ripple component. The average component equals the output load current. Typically, the ESR of the capacitor is much smaller than the output load resistance. The high frequency ripple current in the inductor is therefore completely absorbed by the capacitor. This creates the output voltage ripple given by:

$$\Delta v_o = esrC_o \cdot \Delta i_L$$  \hspace{1cm} (4.31)

Because the current in the inductor cannot change instantaneously when a sudden load step is applied, the differential between the inductor and load current is absorbed by the filter capacitor. The impact of load step-down on the transient performance is shown Figure 4-12. When the load is step-down instantaneously, the differential DC current between the inductor and the load flows through the ESR of the filter capacitor, causing it to increase by $(esrC_0 \Delta I_o)$ [55]. This causes a sudden reduction in the turn-on time of the top FET, which has the effect to reduce the inductor current and reestablish the balance between the load and the inductor current. The change in one time is given by:
\[ \Delta t_{on} = t_{on} - t_{on1} \quad (4.32) \]

\[
K_t = \frac{\Delta t_{on}}{\Delta I_o} = \frac{t_{on}}{t_{on}} \cdot \frac{esr C_o}{V_{hys}} = \frac{t_{on}}{\Delta i_L} \left( \frac{esr C_o}{R_{mod} + esr C_o} \right) \quad (4.33)
\]

Note that the change in on-time for this modulator occurs even before the voltage error amplifier can respond. As the differential load current flow dictates the dynamic behavior of the SRM, it is referred to as the “load current feed-forward mechanism.” It should also be noted that there is a change in the switching frequency as a response to the load transient. A similar response is expected during load step-up.

**Transient Modeling of the Synchronous Buck Converter**

The design of the LC filter for the POL is often based on the load transient requirements and efficiency rather than the output voltage ripple. Assuming infinite bandwidth of the feedback loop and instantaneous transient response of the modulator, the synchronous buck converter can be modeled, as shown in Figure 4-13. Based on the models, the rate of change in the inductor current during step-up and step-down transient can be expressed as

\[
\left( \frac{di_L}{dt} \right)_{\text{stepup}} = \frac{(V_{in} - V_o)}{L} \quad (4.34)
\]

\[
\left( \frac{di_L}{dt} \right)_{\text{stepdown}} = -\frac{V_o}{L} \quad (4.35)
\]

The input voltage for the POL is much larger than the output voltage. The rate of the rise of inductor current during step-up is therefore much faster than that during step-down. Therefore, the step-down transient dictates the number of output capacitors for certain transient specification. Figure 4-14 shows the response of the synchronous buck converter to load transient. The transient response of the output voltage can be divided into two parts. The step change in output voltage is the result of the ESR of the filter capacitor. The relatively slow push
back to regulation is due to the output capacitor charge storage differential. The net change in output voltage change is expressed as

$$\Delta V_{o,\text{max}} = \Delta V_{\text{ocap}} + \left( \Delta I_o \cdot esr C_o \right)$$  \hspace{1cm} (4.36)

This equation can be used to estimate the output capacitance required to meet a specific load regulation requirement as derived below

$$C_o = \frac{1}{2} \cdot \frac{(\Delta I_o)^2 \cdot L}{(V_{in} - V_o) \cdot \Delta V_{ocap}}$$  \hspace{1cm} (4.37)

The amount of filter capacitance required is directly proportional to the load transient step and the inductor size. In order to reduce the effective filter inductor size, a number of modules can be operated in parallel and is known as “interleaving.” This improves the transient performance in a high current step system. It should also be noted that the capacitance requirement is the worst when the input voltage is minimum or the output voltage is maximum.

**Factors Affecting Transient Response**

Apart from choice of filter components of the synchronous buck converter, other factors can also affect the transient performance. The most important factor is the loop design.

**Loop Design**

The speed or the crossover frequency of the loop is one of the most important factors that affect the transient performance. Figure 4-15 shows the impact of this crossover frequency on the design in Table 3-2. When a 20 A transient is introduced, a 100 kHz crossover loop responds to it almost instantaneously and gets back the output voltage into regulation within 10 µs. When a 20 kHz crossover loop responds to the same transient, it has a much slower response leading to a higher voltage deviation from nominal, and it takes around 150 µs to get back to regulation.

Unlike voltage mode control, which has a two pole response, the SRM poses a single pole response. Therefore, the feedback loop design is much easier and can be achieved with a simple
compensation scheme. In order to achieve a fast dynamic response, the crossover frequency for the loop is set around one-fifth of the switching frequency. For example, if the switching frequency is set at 250 kHz, the crossover frequency of the feedback loop is designed to be about 50 kHz.

**Trace Impedance**

The trace impedance, which leads from the output of the converter to the load, affects the transient behavior and steady-state behavior of the system. Two types of voltage sensing are implemented in a power system, as shown in Figure 4-16. The choice of the type of sensing is dependent on this trace impedance. In general, the distribution voltage drop in output power train leads and host board plane can be compensated by using a differential remote sense technique. If local sensing is implemented with large trace impedance, the output will have a permanent DC error with respect to the constant reference voltage. Therefore, even when the POL is located near the load, voltage sensing is always done remotely. As shown in Figure 4-17, the transient response to a 20 A step is affected by this trace impedance, owing to the distribution drop. The converter was operated at a 400 kHz switching frequency. The parameters for the converter and the modulator are given in Table 3-2.

**Optimizing Dynamic Response for the SRM**

In the previous section, it is identified that the load release is the worst case transient for POL application due to slow discharge of inductor energy after the transient. For modern POLs, in order to improve efficiency, the output voltage is reduced by introducing some droop in the output. This creates a minimum and maximum voltage bound for the output voltage known as load line characteristics. In order to fully utilize this window of tolerance, the output voltage is strategically placed near the maximum limit at no load and minimum limit at full load. This technique is known as automatic voltage positioning (AVP), as shown in Figure 4-18. The
window helps to reduce the capacitor size required to meet the transient requirement. This section describes the design optimization of the modulator, in order to take full advantage of the AVP window and quickly get the converter back to regulation [56].

Figure 4-19 shows a close look at the buck converter response after a step-down transient strikes. The current differential between the inductor and the load charges the output filter capacitor and causes a rise in the output voltage. During this time period $t_f$ the modulator forces the bottom FET to be on. The optimum time for the converter to start switching again is just before the output voltage reaches the upper limit of the AVP, such that the current in the inductor will come back to zero as the output voltage reaches the AVP limit at $t_3$.

The current charging the capacitor is the differential between the load current and the inductor current and is given by:

$$i_c(t) = I_o - \frac{I_o}{t_1} \cdot t$$ (4.38)

Due to this charge current there is a voltage deviation at the output, which is given by:

$$v_o(t) = \frac{1}{C_o} \left[ I_o \cdot t - \frac{I_o}{t_1} \cdot \frac{t^2}{2} \right] + esrC_o \cdot \left[ I_o - \frac{I_o}{t_1} \cdot t \right]$$ (4.39)

The time period after with the output voltage resonates to maximum value can be found out as follows

$$\frac{dv_o(t)}{dt} = 0 \Rightarrow t = \left( t_1 - \frac{I_o}{esrC_o} \right)$$ (4.40)

In the above equation, time $t_1$ is a known quantity because the slope of inductor current and maximum current step is known. The equation also shows that, if the ESR is not neglected, the output voltage reaches the peak value prior to the inductor current reaching zero. The size of output capacitor can be calculated using (4.37) in order to meet certain maximum voltage specification $\Delta V_{\text{omax}}$. 
The instant at which the UFET can be turned on depends on two factors. The first one is the slew rate of the modulation signal $V_{\text{mod}}$ and it is given by (3.12). The second one is the response of the compensator to the output voltage overshoot. As the output voltage rises it injects a current given by $(V_o - V_{\text{ref}})/R_1$ into the feedback node $V_{\text{fb}}$. This current creates the drop in the command signal $V_{\text{cmd}}$. This drop can be approximated as the drop across the resistor $R_2$, as $C_2$ has very high impedance and $C_1$ has very low impedance at that frequency range. The simulation response of the compensator to a high slew rate load step is shown in Figure 4-20. The results show the comparison between the current through $C_3$ and $C_2$. It also shows the drop across $R_2$ and $C_2$, which confirm the above approximation. The change in $V_{\text{cmd}}$ can be approximated as

$$
\Delta V_{\text{cmd}} = \frac{v_o(t_2)}{R_1} \cdot R_2 
$$

(4.41)

As shown in Figure 4-18, the net change is $v_{\text{cmd}}$ and $v_{\text{mod}}$ signal is given by:

$$
\Delta V_{\text{mod}} = \Delta V_{\text{cmd}} + V_{\text{hys}} 
$$

(4.42)

This behavior can be used to design the compensator and the modulator, such that the UFET of the buck converter can be turned on right before the output voltage crosses the maximum AVP limit.

In summary, analysis that is critical to dynamic behavior of the SRM is described in this chapter. The small signal behavior is derived and validated. The design of the feedback loop, in order to obtain a fast and stable system, is described. Factors affecting the dynamic performance are quantified. The chapter concludes with a design philosophy for the modulator and the compensator, which ensures a fast dynamic response.
Figure 4-1. Small signal modeling of the SRM.

Figure 4-2. Control-to-output transfer functions of the SRM with design parameters in Table 3-2.
Figure 4-3. Control-to-output transfer functions with load variation.
Figure 4-4. Open loop output impedance of the SRM with parameters in Table 3-1.
Figure 4-5. Open loop output impedance variation with filter capacitor.

Figure 4-6. Closed loop output impedance can pose resistive output impedance. (Type 2 compensator: \( R_1=630 \), \( C_2=600\text{n} \), \( R_2=10 \text{ K} \), \( C_3=200 \text{ pF} \))
Figure 4-7. Impact of change in $V_{in}$ on the output voltage for the SRM.

Figure 4-8. Effect of low and high frequency input noise on the output voltage $V_o$. 
Figure 4-9. Basic philosophy of the loop design for faster transient response.

Figure 4-10. Type 2 compensator and its small signal model.
Figure 4-11. Input impedance characteristics of the SRM.
Figure 4-12: Large signal behavior of the SRM.

Figure 4-13. Response of synchronous buck converter to load transient.
Figure 4-14. Synchronous buck converter response to load transient.

Figure 4-15. Impact of crossover frequency on the load step response.
Figure 4-16. Output voltage sense options for a POL.

Figure 4-17. Impact of distribution impedance on load transient and voltage regulation.
Figure 4-18. Automatic voltage positioning of output voltage helps transient design.

Figure 4-19. Optimizing large signal response of the SRM.
Figure 4-20. Compensator design for optimum SRM dynamic response.
CHAPTER 5
EXPERIMENTAL VERIFICATION

This chapter presents two different design methodologies. The first design example is based on the design methodology presented in Chapter 3. The modulator is designed to meet critical parametric requirements. Based on the modulator, the feedback loop is designed to provide a stable and fast acting system. The second design example verifies the optimal transient theory developed in Chapter 4. The converter, modulator, and compensator are designed to meet a specific transient requirement with an optimal transient response. The optimal transient response helps the converter back into regulation in a minimum amount of time. The experimental verification shows a good co-relation between the theory and the experiment for both design examples.

SRM Design Based on Conventional Design Methodology

This section describes the SRM design based on the conventional design methodology without any attempt of optimizing the dynamic response. The SRM design is based on the design methodology in Chapter 3. The compensator is designed to meet the stability criteria of the feedback loop and to provide a fast response to the load transient.

Converter Design

The synchronous buck converter is designed to have an output of 1.8 V with a 15 A rating. The nominal input voltage is 10.5 V. As the module is designed to have a single phase, the inductor size is specified as 0.82 µH in order to reduce the peak-to-peak ripple current through it. The peak-to-peak current ripple results in degradation of converter efficiency due to excessive switching loss in the top FET. Based on these initial specifications, the filter capacitor, the modulator, and the feedback loop are designed. There are three important design and layout considerations for a synchronous buck converter design.
One of the most important considerations in designing a synchronous buck converter is to avoid a miller capacitor-induced \( \frac{dv}{dt} \) turn-on of the LFET \([57]\). Figure 5-1 shows the mechanism of this fault turn-on. The sharp rise in the \( V_{\text{phase}} \), during the UFET turn-on, is associated with an injection of charge into the gate of the LFET. Ideally, the gate-driver creates a low impedance node. However, during this high slew rate transient the interconnect inductance between the gate-drive output and the lower gate terminal results in high gate impedance. This results in an increase in the lower gate voltage \( V_{gL} \). If not designed properly, this voltage spike can result in the LFET turning on and causing a shoot-through between \( V_{in} \) and the ground. This fault turn-on can be avoided by a proper choice of the LFET device as follows:

\[
(C_{gs})_{LFET} \gg (C_{gd})_{LFET}
\]  

(5.1)

Therefore, IRF6678 is used as the LFET in this design which has \( C_{gs}=43 \) nC and \( C_{gd}=15 \) nC. This FET also has a very low on-resistance of \( 2.3 \) m\( \Omega \), which improves the overall efficiency.

The next most important consideration pertains to proper layout of the board, as shown in Figure 5-2. For example, if there is a presence of parasitic inductance between the gate-driver ground and source of the LFET, it results in a negative ringing on the phase node. The ringing is a result of trapped energy circulation in the loop formed by the gate charge capacitor, internal gate-drive device, parasitic inductor, and lower FET diode. The negative ringing can result in voltage across the bootstrap capacitor \( C_b \) to exceed above \( V_{cc} \) and leads to the failure of the gate-driver \([58]\).

Another important layout consideration is to have the input decoupling capacitor very close to the drain of the UFET and the source of the LFET in order to reduce the parasitic inductance. The parasitic inductance can result in heavy phase node ringing during the top FET
turn-on as shown in Figure 5-3. This ringing results in an increased switching loss and potential high frequency noise interference with other sensitive devices on the motherboard.

The bias supply consists of a linear regulator comprised of an NPN device and a 6 V zener diode. This scheme gives a flexible on-board circuit to generate a bias voltage using the input supply. The major load on this supply is the gate-driver current, which is typically about 30 mA with a 250 kHz switching frequency for IRF6678. The complete power converter, gate-driver, and its bias supply design are shown in Figure 5-4. The power converter is realized using power FETs IRF6678 for both the top and bottom switch. The ISL6605 gate-driver accepts the square wave output signal of the PWM circuit as input and generates the gate-drive signal for the top and bottom switch. The input gate capacitance is specified as 5 nF and is driven by the gate-driver with minimum delay. The rated overall transition delay for the gate-driver is specified within 30 ns for a 5 nF load.

The power filter is realized using a powder core inductor. Powder cores have the advantage of significantly less temperature de-rating at the expense of higher core loss compared to ferrite cores. This inductor has a DC resistance of 1.8 mΩ.

**Modulator Design**

Based on the converter specification, the modulator can be designed as delineated in Chapter 3 [59]. The design steps are outlined in Table 5-1 and are summarized below.

The hysteresis voltage $V_{\text{hys}}$ is selected first. For this example, the hysteresis voltage is chosen much larger than the steady-state output voltage ripple on $V_o$. Therefore, a 0.3 V hysteresis voltage is chosen.

The ripple regulator is designed such that the output current of the transconductance amplifier is much larger than the input bias current of the Opamp. For this example, the transconductance is specified as 55 µS. Therefore, the output current of the transconductance
amplifier has a minimum of 100 µA, which is much larger than the sum of all the bias currents. Note, the Opamp chosen for the design has a CMOS input stage and therefore has a very small input bias current in the Pico-ampere range.

The droop resistance $R_{\text{droop}}$ is chosen as 14 mΩ. The droop resistance is used to calculate the $R_{\text{cmod}}$ using (3.6). The switching frequency is specified as 250 kHz. The discrete semiconductors used for the design are tabulated in Table 5-2. The total delay $t_1$ is approximated from the datasheet to be 100 ns. Using (3.4) and (3.13), $C_{\text{mod}}$ can be calculated as 820 pF. The command voltage will automatically be set by the voltage error amplifier when the feedback loop is closed.

Figure 5-5 shows the experimental implementation of the transconductor. The Opamp AD8066 is a dual amplifier with similar characteristics as AD8057. The value of $R_m$ for the transconductor is calculated using (2.2). The input voltage to the ripple regulator is scaled down using an input resistive divider. The reduced input voltage helps the circuit to be within the input and output range of the Opamp. Figure 5-6 shows the implementation of the hysteresis voltage generator and it provides a low impedance supply for the hysteresis level generators. Figure 5-7 shows the implementation of the hysteresis level generator, which is fundamentally a combination of an analog adder and a subtractor. The adder is used to generate the upper level hysteresis $V_{\text{mod+}}$ and the subtractor is used to generate the lower level hysteresis $V_{\text{mod-}}$. The hysteresis comparators are realized using the dual LT7120 comparator. The output of these comparators is fed into an NAND-FF, which generates the PWM signal for the gate-driver. Table 5-2 summarizes all the components and its key parameters of specific importance to this design.

**Dynamic Design**

Most modern POLs are required to satisfy specific dynamic requirements under all load conditions. The worst case to maintain dynamic regulation is during a high slew rate step-down
transient, as identified in Chapter 4. This example explores the design of the filter capacitor and
the SRM under this load transient condition.

**Filter Capacitor Requirement for Transients**

The design meets the following example transient requirements [60]:

Load line=1.25 mΩ ± 19 mV (additional 50 mV during load release)

The no-load voltage of this design is 1.8 V. With a 15 A load step the required maximum
voltage deviation is quantified from the above specification as

$$
\Delta V_{\text{max, req}} = (15 \times 1.25 \text{mΩ}) + 38 \text{mV} = 56.75 \text{mV}
$$

Thus, the maximum output voltage deviation during load step-up and step-down equals
56.7 mV. Due to distribution impedance and component tolerances, a conservative target for this
voltage deviation is about 45 mV. Based on this result, the number of output capacitors can be
found.

Assuming a 2 mΩ ESR for the output capacitor, the net voltage deviation allowed by the
capacitor is given by (4.36) as follows:

$$
\Delta V_{\text{ocap}} = 45 \text{mV} - (15 \times 2 \text{mΩ}) = 15 \text{mV}
$$

Using (4.37), the output filter capacitor required is found out to be

$$
C_o = \frac{1}{2} \cdot \frac{(15)^2 \cdot 0.82 \mu(1 + 0.2)}{(10.5 - 1.8) \cdot 15 \text{mV}} = 862 \mu \text{F}
$$

The inductor used has a tolerance of 20% and is reflected in the previous filter capacitor
calculation. Therefore, three specialty polymer capacitors with a 330 µF specification are used
for the design. Nominal input voltage of 10.5 V and output voltage of 1.8 V is assumed to the
design.
Feedback Loop Design

The control-to-output transfer function for this design is calculated using (4.8). The experimental and theoretical comparison for this transfer function is shown in Figure 5-8. Results show a 4 kHz dominant pole for this design, which means the second pole is effectively canceled by the resultant zero from the modulator. The ESR zero is around 80 kHz and has little impact at low frequency. The transfer function gives a starting point for the design of the stable feedback loop and optimizing it for faster transient. The designed type 2 compensator is shown in Figure 5-9. The compensator is designed to have a zero at about 4 kHz and a pole at very high frequency. The theoretical verification and experimental verification of the loop gain are shown in Figure 5-10. The theoretical loop gain is predicted using (4.23). The crossover frequency is one-fifth the switching frequency of 250 kHz. The phase margin of the design is shown to be 55° and the gain margin to be 18 dB.

SRM Condition Check

This check is performed to make sure that the condition specified in (4.30) is satisfied. For this design, the gain of the compensator at switching frequency can be calculated using (4.19) and is estimated to be 4.8. The value of $R_{\text{mod}}$ for the design is calculated using (4.29) and Table 5-1 to be 55 mΩ. The ESR of the filter capacitor is specified as 2 mΩ. Using these parameters in (4.28)

$$G_{BEA} \left( f_{sw} \right) < \frac{R_{\text{mod}}}{esrC_o} \Rightarrow 4.8 < \left( \frac{55m\Omega}{2m\Omega} = 27.5 \right)$$ (5.4)

The equation suggests that the peak-to-peak ripple at the command signal is nearly four times smaller than the peak-to-peak ripple at the output of the ripple regulator. This ensures a proper PWM switching instant determination by the hysteretic comparator. The simulated ripple
is shown in Figure 5-11. The result shows a ripple of 300 mV at the output of the ripple regulator compared to a 65 mV ripple at the output of the voltage error amplifier.

**Simulation**

A simulation platform is developed using PSpice in order to predict the performance of the SRM as shown in Figure 5-12. The buck switches are realized using ideal switches. In order to simulate the turn-on delays an input capacitance of 3 nF is included to simulate the gate capacitance. The on-resistance is simulated with the help of a series resistor. All the Opamps, except the voltage EA, are simulated as an ideal voltage controlled voltage source. The voltage EA is modeled with a slew rate and bandwidth limit. A shoot-through protection circuit is included in the gate-driver to delay the gate signals and ensure that they are not high at the same time. A comprehensive filter capacitor model provided by the manufacturer is used to simulate the output filter capacitor.

The step-up and step-down transient responses are shown in Figure 5-13 and Figure 5-14. The load transient applied was a 15 A step with a rate of transition of 10 A/us. The simulation shows a voltage deviation of 55 mV for step-down and 40 mV during the step-up transient. Also plotted is the current output of the ripple regulator. The current is pulsed at switching frequency due to its pulse input voltage. The peak output current is about 350 µA and the valley current equals -80 µA.

**Prototype Design and Test Setup**

The designed prototype is shown in Figure 5-15. The prototype was laid-out using PCAD. In order to test this VRM, a test fixture was developed to simulate the host board of the POL. In order to simulate the extreme environment of the host board in a real application, only a 20 µF ceramic capacitor was used, which represents the bare minimum decoupling capacitor necessary for remote sensing. The test setup of the VRM and the test fixture is shown in Figure 5-16. An
electronic load with a 15 A/µs current transition capability is used to simulate the actual load on the host board.

**Experiment**

Figure 5-17 shows the steady-state operation of the design. The switching frequency matches the designed value of 250 kHz. The output voltage ripple is close to the approximated value of 20 mV. There seems to be some injected noise because of the measurement setup. In order to verify experimental data with the theoretical prediction, the peak-to-peak ripple at the $V_{mod}$ node is predicted to be about 0.4 V and matches very well the experimental results in Figure 5-17. The positive slope of $V_{mod}$ is predicted by (3.11) to be 0.5 V/µs, which is close to the experimental results. Similarly, the negative slope is given by 0.12 V/µs and matches closely with the predicted value.

The response of the circuit to a 15 A transient with a rate of transition of 15 A/µs is shown in Figure 5-18 and Figure 5-19. The step-up transient is about 65 mV and the step-down transient is around 37 mV. As predicted in the Chapter 4, the step-down transient is the worst edge as far as regulation is concerned. In practice, extra head room is provided in the specification for this transient. For example, VR 10.0 allows an extra 50 mV for 25 µs for this transient edge. During load release, the slope at which $V_{mod}$ responds is predicted by (3.12), and the experimental results confirm this prediction.

Figure 5-20 shows the response of the lower FET gate to the step-down transition. The lower gate voltage turns on to respond to this load release almost immediately, ignoring some delay in the control circuit. Similarly, the response to load step up is also very fast, as shown in Figure 5-21. It can be observed that the control responds by not only increasing the duty cycle but also by the increase in switching frequency. The overall drop in output voltage during this transient is below 40 mV. In order to make the fast transient response more evident, the response
of the hysteretic threshold limits are plotted with the $V_{\text{mod}}$ for both the load transient edges in Figure 5-22 and Figure 5-23.

**SRM Design with Optimizing Transient Response**

This design example presents an SRM design methodology for an optimized transient response. The basic philosophy is to meet the specified dynamic voltage regulation requirements and get the voltage back to regulation in a minimum number of switching cycles. The specifications for this design are described as follows:

**Specification:**

1. $V_{\text{in}}=10.5 \, \text{V}$, $V_{\text{o}}=1.8 \, \text{V}$, and $I_{\text{o}}=15 \, \text{A}$
2. Load line: $2 \, \text{mΩ} \pm 10 \, \text{mV}$ ($V_{\text{tol}}=20 \, \text{mV}$, $V_{\text{tolR}}=30 \, \text{mV}$ during load release)
3. $\Delta I_{\text{omax}}=15 \, \text{A}$

**Power Stage Design:**

Chapter 4 identifies the load release as the worst case in terms of dynamics. The LC can be designed so the output resonates between $V_{\text{omin}}$ to $V_{\text{omax}}$ as inductor current goes to zero. The inductor is chosen as $0.82 \, \mu\text{H}$ in order to reduce the inductor ripple and switching loss. For this example the specified maximum voltage deviation is given by:

$$\Delta V_{\text{omax, req}} = 2m\Omega \times 15 + 20mV = 50mV$$

Similar to the previous example, due to distribution impedance and component tolerance, maximum allowed deviation in the output voltage is approximated as $45 \, \text{mV}$. Using (4.36), the maximum voltage drop allowed across the filter capacitor is estimated as $15 \, \text{mV}$. The required filter capacitor $C_{\text{o}}$ required to meet this transient specification is calculated using equation (4.37) and is equal to $850 \, \mu\text{F}$. The 20% inductor tolerance is also taken into account for this calculation.
The same capacitor combination is therefore used as in the previous design example, which is three 330 µF capacitors in parallel.

**UFET Turn-on Instant:**

As described in the optimized design response in Chapter 4, after a load release transient, the UFET can be turned as the output voltage reaches the regulation limits. These regulation limits are defined by the load line. For this example, the regulation limits define a 30 mV droop in output voltage from full load to no-load. The output voltage is therefore allowed to resonate to nearly 30 mV before the UFET is turned on. This condition defines the time instant at which the UFET is turned on. The output voltage characteristic is defined by (4.39). The output voltage characteristics can be used to compute the UFET turn-on instant $t_2$. Figure 5-24 shows the Mathcad simulation of the output voltage characteristic after the load transient hits. The output voltage resonates to a maximum value after 5 µs of the load transient. This conclusion is the same as predicted by (4.40). Without the intervention of the voltage EA, the output voltage reaches 30 mV after 10 µs of the transient strike. The modulator and the compensator should be designed so that the $V_{\text{mod}}$ intersects the lower limit of the hysteretic signal $V_{tL}$ and 10 µs after the transient hits.

**Design of the Modulator:**

The hysteresis voltage is selected to avoid noise affecting the modulation signal. The no-load value of the command signal $V_{\text{cmd}}$ is equal to the output voltage. Because IR8057 is used as the error amplifier, the minimum output swing defines the lowest voltage to which $V_{\text{cmd}}$ can swing. As the lower limit of the output swing is 0.9 V, a 0.4 V can be safely allowed for $\Delta V_{\text{cmd}}$. The calculation means the $V_{\text{mod}}$ intersects the $V_{tL}$ at about 0.66 V below $V_{tH}$, given by (4.42). Based on this information, (3.12) can be used to find the optimal value of $g_{m\text{Mod}}/C_{\text{mod}}$, and is given by
30 kS/F. Selecting $C_{\text{mod}}=820$ pF, $g_{m\text{Mod}}$ can be calculated as 30 µS. This gives the switching frequency of the modulator equal to 210 kHz.

**Compensator Design**

The control-to-output transfer function is shown in Figure 5-25. The loop resistor $R_1$ is selected based on the current capability of the input pins of the voltage error amplifier. As explained in Chapter 4, the drop in the command $V_{\text{cmd}}$ after a high slew rate transient is approximated as the voltage drop across the feedback resistor $R_2$.

If $R_1$ is chosen as 630 Ω, $R_2$ can be calculated using (4.41) as approximately 10 kΩ. The loop response for this compensation is shown in Figure 5-26. The crossover frequency is 40 kHz with a phase margin of 55°. Table 5.3 summarizes the design presented in this section.

The response of the designed system to a 15 A load step-down at a rate of 10 A/µs is shown in Figure 5-27 and Figure 5-28. Figure 5-28 shows the response of the system without optimal design. It can be seen that the modulator takes about 8 to 10 cycles to get back to regulation. Figure 5-27 clearly shows the fast response and minimum cycle taken by the modulator to get back to regulation. The step down load response shows a predicted voltage overshoot of about 60 mV, which is reached after 5 µs of the load transient. The theory predicts the output reaching at 30 mV after 10 µs, and is confirmed by the experiment. Similarly, the Figure 5-29 shows the load step down response. The transient is within the specification and confirms the superior design.

This example confirms the superior dynamic response of the SRM with the optimized dynamic behavior. The modulator takes minimum time to get back to regulation.
### Table 5-1. Design Procedure for Example 2

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Design Method</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_o$</td>
<td>Specified</td>
<td>1.8 V</td>
</tr>
<tr>
<td>$V_{bgs}$</td>
<td>$V_o$Ripple&lt;&lt;$V_{bgs}$&lt;&lt;$V_o$ Transient</td>
<td>0.3</td>
</tr>
<tr>
<td>$g_{mMod}$</td>
<td>$g_{mMod}V_o$&gt;&gt;Total Bias Current</td>
<td>55 µS</td>
</tr>
<tr>
<td>$R_{drop}$</td>
<td>Specified</td>
<td>14 mΩ</td>
</tr>
<tr>
<td>$n_sL$</td>
<td>Specified</td>
<td>1.8 mΩ, 0.82 µH</td>
</tr>
<tr>
<td>$R_{mod}$</td>
<td>Using (3.6)</td>
<td>137 kΩ</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Specified</td>
<td>250 kHz</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>Specified</td>
<td>10.5 V</td>
</tr>
<tr>
<td>$t_1$</td>
<td>Datasheet and measurements</td>
<td>100 ns</td>
</tr>
<tr>
<td>$C_{mod}$</td>
<td>From (3.4) and (3.13)</td>
<td>820 pF</td>
</tr>
<tr>
<td>$I_o$</td>
<td>Specified</td>
<td>15 A</td>
</tr>
</tbody>
</table>

### Table 5-2. Part Specification for Design Example 2

<table>
<thead>
<tr>
<th>Parts</th>
<th>Attributes</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>FETs</td>
<td>IRF6678 ($R_{dson}=1.7$ mΩ, $Q_g=43$ nC, $Q_{gd}=15$ nC)</td>
<td>International Rectifier</td>
</tr>
<tr>
<td>Opamps</td>
<td>AD8066 (SR: 160 V/µs, BW: 155 MHz; $I_{bias}=1$ pA)</td>
<td>Analog Devices</td>
</tr>
<tr>
<td>Comparator</td>
<td>LT1720 (Delay: 13 ns; $I_{bias}=-6$ µA; Linear Tech.)</td>
<td>Linear Tech.</td>
</tr>
<tr>
<td>Flip-Flop</td>
<td>74 ACT11074 (Delay: 9 ns; Texas Instruments)</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>Gate-driver</td>
<td>HIP 6605B (Delay: 10 ns; Transition time: 10 ns;</td>
<td>Intersil</td>
</tr>
<tr>
<td>Filter Cap</td>
<td>3 X 330 µF/ 7 mΩ SP-Capacitor</td>
<td>Panasonic</td>
</tr>
<tr>
<td>Inductor</td>
<td>IHLP-5050EZ, (0.82 µH, 2 mΩ, Vishay)</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>Load</td>
<td>120 A output, 15 A/us (Max. Slew)</td>
<td>Croma</td>
</tr>
</tbody>
</table>
Table 5.3. SRM Design Example for Optimal Transient Behavior

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Equation</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΔV_{omax,eq}</td>
<td>Specified</td>
<td>50 mV</td>
<td>Selected based on specifications</td>
</tr>
<tr>
<td>V_{in}</td>
<td>Specified</td>
<td>10.5 V</td>
<td></td>
</tr>
<tr>
<td>L, r_L</td>
<td>Select</td>
<td>0.82 µH, 1.8 mΩ</td>
<td>Selected to minimize switching loss</td>
</tr>
<tr>
<td>ΔV_{ocap}</td>
<td>(4.36)</td>
<td>20 mV</td>
<td></td>
</tr>
<tr>
<td>C_0</td>
<td>(4.37)</td>
<td>850 µF</td>
<td>3 X 330 µF is selected for the design</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Modulator Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_f</td>
</tr>
<tr>
<td>V_{hs}</td>
</tr>
<tr>
<td>ΔV_{omd}</td>
</tr>
<tr>
<td>ΔV_{mod}</td>
</tr>
<tr>
<td>g_{nMod}/C_{mod}</td>
</tr>
<tr>
<td>C_{mod}</td>
</tr>
<tr>
<td>g_{nMod}</td>
</tr>
<tr>
<td>f_s</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Compensator Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_1</td>
</tr>
<tr>
<td>R_2</td>
</tr>
<tr>
<td>C_2, C_3</td>
</tr>
</tbody>
</table>
Figure 5-1. Miller injected turn-on mechanism in a synchronous buck converter.

Figure 5-2. Carefully gate-drive layout reduces the negative spike on the V_{phase}.

Figure 5-3. Tight decoupling of the buck converter is essential to reducing noise on the V_{phase}.

Sensitivity: 5 V/div and 500 ns/div.
Figure 5-4. The power converter design with gate-driver supply.

Figure 5-5. Transconductance amplifier implementation.
Figure 5-6. Hysteresis voltage generator.

Figure 5-7. Hysteretic level generator, comparator, and PWM latch circuit.
Figure 5-8. Control-to-output transfer function for the system in Table 5.1.

Figure 5-9. The compensator design for the SRM in Table 5-1.
Figure 5-10. Loop response of the design.
Figure 5-11. The ripple voltage on $V_o$, $V_{mod}$, and $V_{cmd}$ for the designed system.

Figure 5-12. Implementation of SRM driven synchronous buck using PSpice.
Figure 5-13. Step-down transient simulation of SRM.

Figure 5-14. Step-up transient simulation of the SRM.
Figure 5-15. Prototype of the VRM with synchronous buck converter driven by the SRM.

Figure 5-16. Prototype test fixture for the VRM.
Figure 5-17. Steady-state performance for design example 2.

Figure 5-18. Load release response of the SRM.
Figure 5-19. Load step-up response of the SRM.

Figure 5-20. Fast response of the lower FET with the SRM to load release.
Figure 5-21. Fast response of the upper FET with the SRM to load step-up.

Figure 5-22. $V_{\text{mod}}$ response to load step-up.
Figure 5-23. $V_{\text{mod}}$ response to load release.

Figure 5-24. Computation of output voltage characteristics to load release.
Figure 5-25. The control-to-output transfer function of the optimized design.

Figure 5-26. Loop design for the optimized design.
Figure 5-27. Step-down response of the optimized design.

Figure 5-28. Step-down response without the optimized design.
Figure 5-29. Step-up response of the optimized design.
CHAPTER 6
SUMMARY AND FUTURE WORK

Point-of-load DC-DC converters and voltage regulator modules for the next generation of integrated circuits, which power communication and computing applications, are required to meet very strict dynamic requirements and challenging specifications that include a small size, being lightweight, and having higher efficiency. A very fast transient response has been realized by using hysteretic modulation with a minimum number of filter capacitors. As the supply voltage to the IC becomes smaller, the ripple requirements also go down. The output voltage ripple therefore becomes small and corrupted for proper hysteretic operation.

This dissertation describes a modulation scheme that synthesizes an artificial ripple by filtering the converter waveforms and adding it to the output voltage in order to achieve a fast dynamic response. The circuit implementation of the modulator and design parameters are described.

The steady-state operation of the SRM is derived and experimentally validated. Critical design parameters affecting the steady-state operation, such as the switching frequency, are quantified and validated. The dynamic behavior of the modulator is analyzed, and design equations to optimize the transient behavior of the modulator are identified. Average models are developed to help predict the steady-state and dynamic behavior of the modulator with minimal computational time.

A synchronous buck converter with a 10.5 V input and 1.8 V/15 A output rating is designed to verify the steady-state and dynamic equations. The response of the VRM to dynamic load transition is tested with a 15 A load current step at a slew rate of 15 A/μs. Results prove the superior response speed of the modulator to load transients and show a 65 mV step-down
overshoot and a 37 mV step-up undershoot in output voltage, which matches very closely with the perdition.

The research presented in this dissertation has made significant headway in understanding and implementing hysteretic control for POL application. Further research can focus on large signal characterization of the control scheme. One such example is the variable switching frequency response to large signal transient loads.

Apart from the application presented herein, this control scheme can be applied to class-D audio applications. Unconditional open loop stability of the control scheme means the voltage loop can be eliminated and a purely open loop power supply with desired droop can be devised. This control scheme can also be implemented digitally and a fully digital solution of the control architecture can be obtained.
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BIOGRAPHICAL SKETCH

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