DEVELOPMENT OF DRIE CMOS-MEMS PROCESS AND INTEGRATED ACCELEROMETERS

By

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2006

This thesis is dedicated to my wife Chen Chen, and my daughters Wendy and Angela.

ACKNOWLEDGMENTS

I would like first to thank my advisor, Dr. Huikai Xie, for his continuous encouragement, expert advice, guidance and support of my thesis research. His profound knowledge and expertise in MEMS and other engineering fields are sources I can always rely on.

I would like also to express my appreciation to my Ph.D. committee members, Dr. Toshikazu Nishida, Dr. David Arnold and Dr. Mark Davidson, for their advice, suggestion and time on my research and thesis. I am grateful to Dr. Arnold for his comments and corrections of my thesis manuscript. I am also benefited from the discussions with Dr. Mark Sheplak on fabrication process and characterization of the accelerometers developed in this thesis work.

I would like to acknowledge Drs. David Johnson and Chris Constantine at Unaxis in St. Petersburg for beneficial discussions on the plasma etch of thick SiO_2; Dr. Rauf Shahid at Freescale for help on physical models in plasma etch.

I appreciate the helps from my group members at the Biophotonics and Microsystems Lab (BML). My special thanks go to my project mate, Dr. Deyou Fang, for his excellent circuit design and help in device tests. The days and nights we spent together in the labs are just memorable. I enjoy my time with Dr. Ankur Jain and Shane Todd at BML. Dr. Jain's advices on my device fabrication are valuable. He is also an export on optical instruments and is always a reliable support to all BML members. Shane's work on the modeling of optical MEMS devices helps me in a better

understanding of these devices. Mingliang Wang, Lei Wu, Kemiao Jia and Xiaoxing Feng offer me many helps in device fabrication and characterization.

My thanks also go to the fellow members at the Interdisciplinary Microsystems Group (IMG) of the University of Florida. I benefited from the good research environment in IMG and helps from many IMG members including, but not limited to, Jian Liu, Anurag Kasyap, Stephen Horowitz, Robert Dieme, Yawei Li, David Martin, Benjamin Griffin and Chris Bohr.

The fabrication of the devices was mostly carried out at the University of Florida Nano Fabrication facilities (UFNF). Thanks go to Al Ogdan, Bill Lewis and Dr. Ivan Kravchenko at UFNF for the maintenance of the facility and support in the fabrication.

I also thank Shannon Chillingworth, the departmental graduate coordinator, for her outstanding work in my graduate study. Thanks go to Joyce White and Kathy Thomson for their support in my research.

Finally, I am grateful to my family and friends for their constant support and encouragement. I am indebted to my wife Chen Chen for her endless love and support. Without her support, this thesis work is impossible. My love to my daughters, Wendy and Angela, is the propellant in achieving this thesis research. I owe my parents and parents-in-law for their endless love and support for my study in USA. I am in debt to my sister, Hongpei Qu, who takes care of my parents when I study abroad. I would like to thank my friends - James Zhang, Jiandi Zhang, Michael Liu and their families - for their friendship and help. I want also thank Vicky Liu and Huanyu Yue for their valuable advices on my Ph.D. study.

This research work was partially supported by NASA UF/UCF Space Research Initiative and the device fabrication was supported by MOSIS through its Educational Program.

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DEVELOPMENT OF DRIE CMOS-MEMS PROCESS AND INTEGRATED ACCELEROMETERS

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August 2006

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Major Department: Electrical and Computer Engineering

Plasma etch based CMOS MEMS technologies have the advantage of monolithic integration of sensors and conditioning electronics, which yields small size, low noise and low cost of the devices. In this thesis work, a new deep reactive-ion-etch (DRIE) based post-CMOS MEMS microfabrication technology was developed, and single-axis and 3-axis integrated accelerometers were fabricated using the new microfabrication technology. Compared to the previous CMOS-MEMS technological approaches, the new microfabrication technology features the capability of monolithic integration for high performance MEMS sensors. The integrated accelerometers demonstrate small size, high sensitivity and high resolution with low power consumption. They can be used in a large spectrum of applications including human activity monitoring, engineering measurement, security, and portable electronics.

Detailed post-CMOS microfabrication processes are presented. Reactive-ion-etch (RIE) and DRIE tools and processes are tuned to satisfy the technological requirements

of the device fabrication. Some general design rules are extracted based on the systematic characterization of the etching tools. Special techniques were developed for aluminum wet etch and electrical isolation etch. The thermal issues in the device fabrication were identified and an alternate fabrication process was developed to avoid the device damage due to the overheat in the plasma processes. Wafer-level fabrication processes are also proposed.

Detailed design of 3-axis and single-axis accelerometers is presented. Device performance is predicted based on the calculations and finite-element analysis (FEA) using Coventor, a commercial FEA tool. The Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm technology is used for the CMOS fabrication.

With power consumption of 1 mW in each axis, the fabricated 3-axis accelerometer achieves sensitivities of 560 mV/g and 320 mV/g in the lateral and z axes, with noise floors of 12 μg/√Hz and 110 μg/√Hz, respectively. The single-axis accelerometer achieves a sensitivity of 90.1 mV/g with a noise floor of 60.7 μg/√Hz. The non-linearity in all lateral axes is less than 0.35%.

CHAPTER 1
INTRODUCTION

The last couple of decades have been seeing the emergence and prevalence of Micro-Electro-Mechanical Systems (MEMS) technology. Many MEMS products, from the first generation of pressure sensors to newly developed integrated MEMS accelerometers and gyroscopes[1-4] , have been commercialized at a fraction of the cost and size of conventional devices. Manufacturing technologies have been developed specifically for MEMS, and some MEMS foundry services such as MUMPS® and MEMS-Exchange are now available commercially [5-7] to MEMS community. However, these fabrication technologies are more research oriented and often incompatible with mainstream Complementary Metal-Oxide Semiconductor (CMOS) technology. The requirement of separate signal-conditioning circuitry, which in turn requires multi-chip assembly, makes the packaging of MEMS devices complicated and expensive.

Small size, multi-function and low cost are the ultimate goals of commodity MEMS devices. One way to achieve these goals is the monolithic integration of MEMS technology with the standard integrated circuit (IC) technology. In fact, the crossover of the conventional IC industry and the fast-growing MEMS technology has led to many newborn technologies in the past years.

Much effort has been made and large capital has been invested into CMOS-compatible MEMS technology, or CMOS-MEMS. With assorted approaches, MEMS

devices have been directly integrated with CMOS circuits, allowing smaller device sizes and higher performance.

In this thesis research, a new post-CMOS MEMS technology is developed, and two integrated devices - a 3-axis and a single-axis accelerometer - are demonstrated based on this deep reactive-ion etch (DRIE) CMOS-MEMS technology. Device microfabrication processes are investigated in detail. Device design is described and the characterization of the fabricated devices is presented.

This chapter summarizes the related CMOS-MEMS technologies and previous work on MEMS accelerometers. The organization of the thesis is given at the end of the chapter.

1.1 CMOS-MEMS Technology

The integration of MEMS technology with the mainstream CMOS technology is referred to as CMOS-MEMS technology. This approach can be classified in three categories: pre-CMOS, inter-CMOS and post-CMOS technology [8], determined by when the MEMS processing is performed relative to the CMOS processing.

1.1.1 Pre- and Inter-CMOS MEMS Technology

In the pre-CMOS technology represented by iMEMS® developed by Sandia National Laboratory, MEMS structures are pre-defined before CMOS processes [9]. Post-CMOS release processes are still required in device fabrication. Analog Device, Inc (ADI) adapted Sandia's approach and developed a MEMS technology based on its BiCMOS process. This iMEMS technology, originally dedicated to CMOS-MEMS accelerometer and gyroscope fabrication, is an intermediate-CMOS MEMS, or inter-CMOS MEMS technology, in which LPCVD polysilicon deposition and annealing are inserted into CMOS process steps for the formation of inertial sensor micor structures

[10, 11]. Infinion's pressure sensor is also fabricated using this type of inter-CMOS MEMS technology [12]. To reduce the residual stress in structural polysilicon, high temperature annealing of polysilicon is normally required in inter-CMOS MEMS, which could pose a potential risk to previous CMOS layers. Contamination caused by the process switch between microfabrication of MEMS structure and normal CMOS steps would be another serious problem. Therefore, usually a dedicated foundry is required for inter-CMOS MEMS technology.

Since most pre- and inter- CMOS MEMS technologies were developed for surface micromachining with polysilicon as the structural material, they suffer from some limitations as the following [13]:

- Mechanical performance of polysilicon is not as good as that of single crystal silicon (SCS). The structure size is limited by the residual stress of thin-film structures. The smaller mass will result in higher thermo-mechanical noise in devices such as accelerometers where a large proof mass is required for high resolution.

- The curling of thin-film structures due to residual stress will severely reduce both the mechanical and electrical performance of MEMS devices. The temperature dependence and robustness of the device will be degraded as well.

- In the electrical domain, the parasitics between the polysilicon structures and the substrate underneath will reduce the output signal dramatically. In a surface micromachined polysilicon accelerometer, depending on the polysilicon wiring path, the parasitic capacitance can be as high as the order of pF [14], which could be several times larger than the sensing capacitance. This will lower the resolution and sensitivity of the device.

- Many thin-film polysilicon MEMS structures are fabricated using wet release in which the sacrificial SiO_2 layer is etched by HF. Although vapor phase etch can be employed, stiction problems become severe when the feature size of a device is reduced to a few microns.

- The processes need to meet very stringent criteria to eliminate the potential contamination to the following CMOS process steps.

- The limited foundry availability, especially for inter-CMOS MEMS foundries, makes the overall cost of MEMS devices relatively high.

1.1.2 Post-CMOS MEMS Technologies

Post-CMOS MEMS technology has a potential to overcome the above-mentioned drawbacks by providing robust and sensitive detecting structures. In contrast to both pre-CMOS MEMS and inter-CMOS MEMS, in post-CMOS MEMS technology, the fabrication of the CMOS circuitry and MEMS structures are performed independently. This makes it possible to integrate high performance mechanical structures made of bulk materials with high performance electronics.

There are mainly two integration methods for post-CMOS micromachining. The first one is to add MEMS structures on the CMOS substrate, leaving the CMOS layers un-etched during the structure microfabrication. The second is to form the MEMS structures by performing micromachining directly in the CMOS thin film layers and/or substrate. These two processing methods are addressed as the following.

1.1.2.1 Additional MEMS structures on CMOS substrate

By adding additional layers onto a CMOS substrate, both metal, dielectric and other semiconductor materials with desired mechanical properties can be used to form MEMS structures. Because of its low process temperature, electroplating is frequently employed in the formation of metal micro structure [15]. In Texas Instruments' popular digital micromirror devices (DMD^{TM}), a sputtered metal is used as the mirror structural material and deep-UV hardened photoresist is used as the sacrificial layer [16]. A research group at UC-Berkeley developed a modularly integrated MEMS technology (MOD-MEMS) in which both polysilicon and poly-SiGe can be used as structural materials. However, when polysilicon was used as the structural material in this MOD-MEMS technology, the aluminum interconnection in standard CMOS technology must be replaced with refractory metals such as tungsten to satisfy the high temperature

requirement for polysilicon annealing [17]. Moreover, a TiN_4 barrier layer should also be added to prevent the reaction between silicon and tungsten. These metallization steps are non-standard CMOS processes and can introduce further residual stresses in polysilicon structural layers. A low temperature process in which SiGe is used as the MEMS structural material was developed recently by the same group at Berkeley and a SiGe resonator was demonstrated [18] using this process. In this MOD-MEMS technology, in-situ p-doped polycrystalline SiGe was deposited at approximately 450°C using low pressure chemical vapor deposition (LPCVD) and etched with conventional reactive ion etch (RIE). Germanium was used as sacrificial layer since it could be easily etched using H_2O_2, with a high selectivity over oxide, poly SiGe (if Ge concentration is less than 70%) and metal. Unfortunately, due to the low deposition temperature, the mechanical properties of poly SiGe were not as good as those of polysilicon. Moreover, the laser melting annealing (ablation) needed in this process also introduces stress gradient in poly SiGe thin films. Therefore, currently this material is not suitable for MEMS devices such as MEMS accelerometers.

Accelerometers made of electroplated copper on silicon substrate have also been demonstrated [19]. Potentially, the integration of electroplated MEMS structures with CMOS substrate is achievable, although the contamination of heavy metal ions to the CMOS circuit is possible.

In addition to the formation of MEMS structures on top of CMOS substrate by thin film deposition, wafer bonding provides another method to directly integrate the wafers containing MEMS structures on CMOS substrate wafer. This approach is exemplified by the fabrication process of a polysilicon thin film accelerometer [20]. In this

accelerometer, the prefabricated polysilicon capacitive acceleration sensor was bonded to the substrate wafer on which electrodes and CMOS read-out electronics were also prefabricated separately. In another wafer-bonded piezoresistive accelerometer, the micromachined bulk silicon proof mass was sandwiched by a bottom glass cap and a top CMOS chip in which the conditioning circuit was pre-fabricated [21].

1.1.2.2 Formation of MEMS in CMOS substrate

In the second type of post-CMOS MEMS, the CMOS surface layers and silicon substrate can be used to create surface and bulk MEMS structures. A high-Q RF MEMS filter with inter-metal dielectric layer as the structural material was reported by IBM [22]. A medical tactile sensor array was also reported in which the aluminum sacrificial layer was etched from the backside of the wafer after the CMOS substrate was etched completely [23]. A research group at ETH in Switzerland processes bulk silicon substrate of CMOS wafer with anisotropic wet etch to obtain thin film and bulk MEMS devices [24]. For thermal sensors in which membranes consisting of dielectric layers are needed for thermal isolation, substrate silicon can be etched completely to obtain the suspended dielectric membranes [25]. The silicon dioxide membrane acts as an intrinsic etch stop layer in a backside silicon anisotropic wet etch using KOH or TMAH solution. Using this anisotropic wet etch based post-CMOS process, 256-pixel thermal imager arrays and multifunctional chemical sensors have been developed [26, 27]. Recently, a monolithic CO gas sensor with an integrated hotplate was reported from the same group [28]. By combining the electrochemical stop techniques with KOH anisotropic etch, silicon membranes with n-well islands can be obtained. In this auto-stop technique, the anisotropic etch stops at the pn junction [29]. This process can be specifically used in the fabrication of highly sensitive pressure and force sensors [30]. By combing silicon

anisotropic wet etch with deep reactive ion etch (DRIE), some sophisticated surface and bulk MEMS structures such as bridges and cantilever arrays can be created. A multisensor system was demonstrated using the combined etch processes [31].

The main challenge in the wet post-CMOS MEMS technology is the protection of the CMOS structures. When etch stop is required for silicon diaphragm formation, the preparation for electrochemical process also increases the complexity of the process. Also, in most cases, precise double-side alignment is required in the fabrication of silicon islands using wet etch.

The technological approaches developed by Carnegie Mellon University differ from those described above in that only dry etch steps are used to create both surface and bulk MEMS structures [32, 33]. Dielectric layers and bulk silicon substrate are etched by isotropic/anisotropic RIE and DRIE respectively, avoiding the potential stiction problem that is common to wet release processes. This dry technology shows another particular advantage in that it is a maskless process, where CMOS metal layers act as masks in the dry etch steps. The MEMS structures are pre-defined by the proper arrangement of metal layers; thus no lithography is needed in this post-CMOS micromachining process. Moreover, multi metal layers (normally 3~6 layers from different CMOS technologies and foundries) make the wiring of the devices flexible which in turn reduces the parasitic effects and improves the electrical performance.

This approach was originally developed for thin film MEMS structures in which mainly surface micromachining was involved [34]. A device based on a copper CMOS technology was also reported [35]. The size of the MEMS structures fabricated using this post-CMOS surface micromachining was strictly limited due to the large curling of thin-

film structures caused by residual stresses. The maximum device size achieved was about 400μm×400μm. Meanwhile, the strong temperature dependence of the thin-film MEMS structures caused by the mismatch of the temperature coefficient of expansion (TCE) of the materials in the thin films also limited their reliable application. Figure 1-1 shows the SEM image of a single-axis accelerometer fabricated using the thin film CMOS-MEMS technology [36].

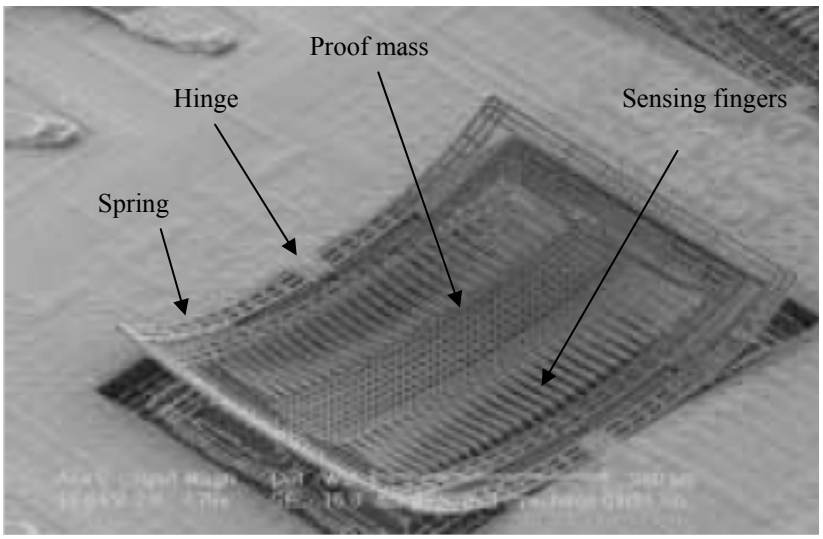


Figure 1-1. A lateral accelerometer fabricated using the thin film CMOS-MEMS technology. Device size is limited due to the large curling of the thin film structures. After Luo, with permission [36].

A DRIE CMOS-MEMS process was developed later based on the surface micromachining described above. In this DRIE CMOS-MEMS technology, single crystal silicon (SCS) was etched using DRIE to form bulk MEMS structures [33]. This DRIE CMOS-MEMS technology has shown great advantages in the fabrication of relatively large MEMS devices such as micromirrors [37]. A large flat mirror can be obtained with bulk silicon existing underneath the aluminum mirror surface. However, when fine structures such as comb drives are fabricated through this process, the isotropic undercut

needed for the formation of electrical isolation structures will have some severe effects on MEMS structures. Figure 1-2 shows the SEM images of sensing comb fingers in a CMOS-MEMS integrated accelerometer fabricated using the previous DRIE CMOS-MEM process [38]. The SCS underneath the comb fingers was severely undercut when isotropic etch was performed to undercut the end of the fingers where the isolation beams are located.

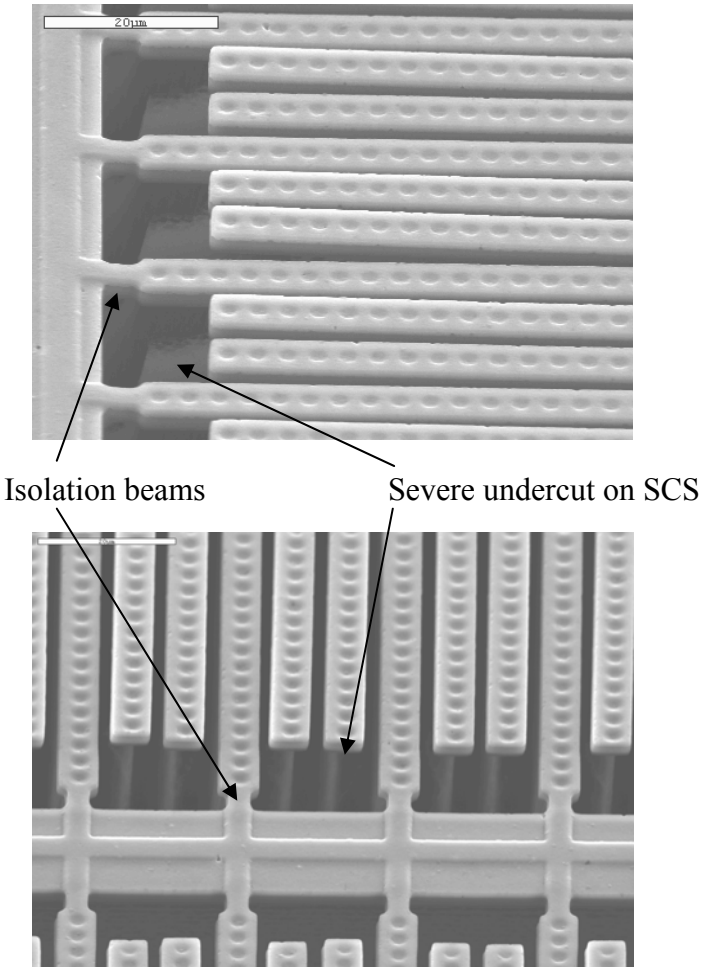


Figure 1-2. SEM images of some sensing comb fingers in an integrated accelerometer fabricated using the previous DRIE CMOS-MEMS process. SCS underneath the fingers was severely undercut when isotropic etch was performed for isolation beam undercut. Images were taken at orthogonal angles.

In this thesis work, a new process is developed to overcome the drawbacks of the previous DRIE post-CMOS technology. As a demonstration of the new process, an integrated 3-axis accelerometer and a single-axis accelerometer are designed and fabricated using the developed new technology.

1.2 MEMS Accelerometers

The accelerometer is one of the first devices demonstrated using MEMS technology. Since the early 1990's, MEMS accelerometers have been dominating the fast-growing market of inertial sensors. Analog Devices is one of the major MEMS accelerometer suppliers. After it shipped its first iMEMS™ accelerometer in the year of 1994, it took about 10 years for the market to grow to 100 million units. As accelerometers have found enormous applications beyond its original business of air-bags in automotives, ADI will ship its second 100 million MEMS accelerometers in only two and half years [39].

The wide spectrum of applications for MEMS accelerometers is attributed to their small size, high sensitivity and low cost due to the large product volume. The conventional applications for accelerometers include automotive safety, inertial navigation and guidance, seismetic and engineering monitoring, explosion measurement in oil drilling, etc. Newer applications of MEMS accelerometers relate to the intelligent data carrier systems, in which data logging/transfer is used between monitoring accelerometers and the data processing center. Wireless communication is essential in many of these data carrier systems. Other typical applications include management of rental vehicles, monitoring and tracking of cargo or goods in logistics systems, working condition and health monitoring. Figure 1-3 illustrates the typical applications and performance requirements for accelerometers in these applications[40]. To date, the

fastest growth of MEMS accelerometers is in the consumer electronics industry. The prevalence of portable electronics and personal communication tools have tremendously boosted the need for small-sized MEMS accelerometers and gyroscopes. Several models of cellular phones and personal data assistants (PDA) have been reported to perform certain functions using just specific hand motions in different directions [41]. Computer and game peripheral manufactures are increasingly integrating MEMS accelerometers in their products. The handheld electronics market is expected to exceed 600 million units in 2005, in which MEMS inertial sensors are expected to play a major role by enabling new functionalities and ease of operation.

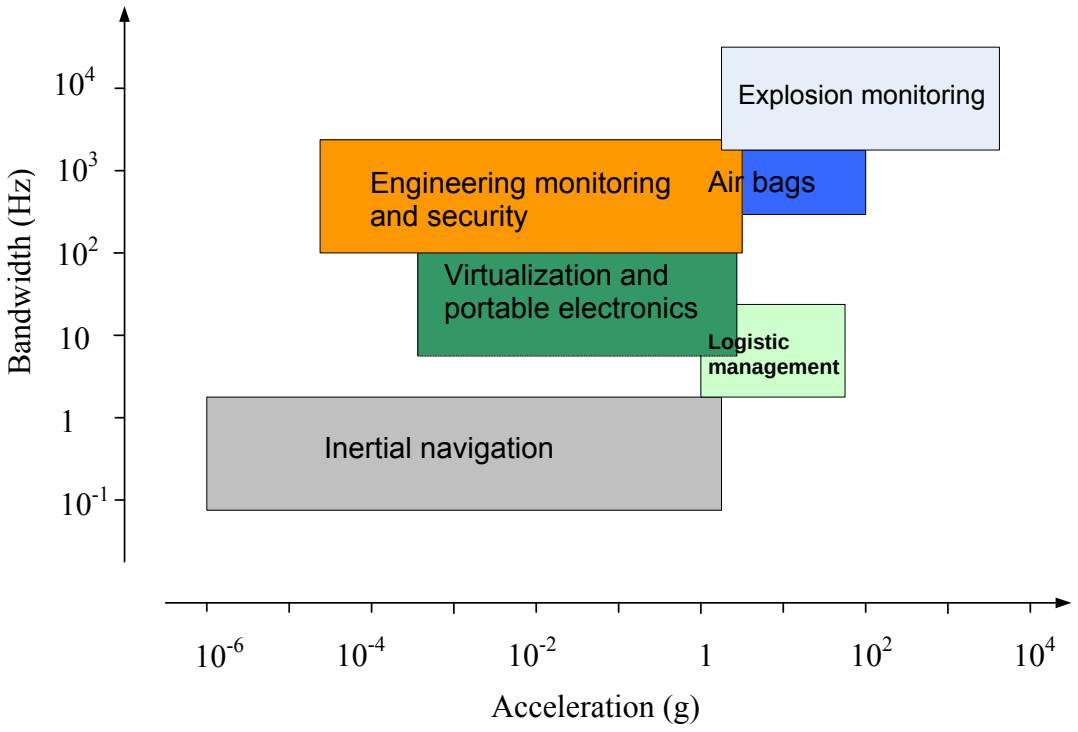


Figure 1-3. Typical applications and performance requirements of accelerometers.

1.2.1 Sensing Mechanisms of MEMS Accelerometers

In principle, many physical effects can be used for acceleration or position sensing. The first micromachined accelerometer commercialized by NovaSensor was piezoresistive [42]. The main advantages of piezoresistive accelerometers are the simplicity of their structures and fabrication processes as well as the read-out circuits. However, piezoresistive devices have some critical drawbacks such as low sensitivity and large temperature dependence. Complex temperature compensation circuits are often needed and a very large proof mass is essential for an acceptable sensitivity.

The capacitive sensing mechanism is dominant in MEMS accelerometers for several reasons. Both surface and bulk micromachining can be used to fabricate a variety of capacitive accelerometers with performance ranging from the low-end automotive application grade to the high-precision inertial navigation grade. Compared to piezoresistive accelerometers, capacitive accelerometers have high sensitivity, low power consumption, low noise level, stable dc characteristics and less temperature dependence. Their simple structures and fabrication processes make the integration of conditioning circuits with sensing elements more straightforward. Due to these advantages, integrated capacitive accelerometers are the primary focus for the booming portable electronics industry.

While capacitive and piezoresistive sensing are two of the most common sensing mechanisms, other physical mechanisms such as resonant frequency shift, thermal transfer and quantum electron tunneling have been exploited as well for the acceleration and motion sensing. A micromachined vibrating beam accelerometer and a vacuum packaged resonant accelerometer have been reported respectively [43, 44]. In both resonant accelerometers, the force generated by the external acceleration on the specially

designed proof mass changes its resonant frequency. Therefore, the acceleration is measured in terms of a shifted resonant frequency of the resonant device. The apparent advantage of the resonant accelerometer is its direct digital output. Thermal accelerometers have also been developed based on the principle of convection heat transfer [45, 46]. Since there are no movable elements in this thermal accelerometer and the manufacturing variations do not influence the thermal performance of the device, these thermal accelerometers demonstrate very good robustness and good batch reproducibility. To achieve high sensitivity, current tunneling effects have also been exploited for sensing acceleration. [47-49]. These accelerometers measure the displacement operating on the principle of quantum electron tunneling, which has very high position sensitivity. A resolution of 20 $ng/\sqrt{Hz}$ has been accomplished by the reported micromachined tunneling accelerometer [50]. This particular accelerometer requires very specific technological processes. The complexity of the fabrication and strict conditioning circuit design make it very difficult for this tunneling accelerometer to be commercialized.

Other accelerometers using optical, piezoelectric and electromagnetic sensing mechanisms have been demonstrated [51-54]. However, the integration of these accelerometers with CMOS technology is a challenge.

1.2.2 Capacitive MEMS Accelerometers

Due to their prevalence, capacitive MEMS accelerometers are discussed in more detail in this section.

Technologically, MEMS capacitive accelerometers can be categorized into three types: thin-film accelerometers fabricated using surface micromachining; bulk

accelerometers fabricated using bulk micromachining and/or wafer bonding technology; and other accelerometers fabricated using more exotic processes. Surface micromachined accelerometers, e.g., polysilicon thin film capacitive accelerometers, have been commercialized for more than ten years. They are available in large volume at very low unit price [1]. However, due to their small proof mass, typically they can only achieve several tens to several hundreds of $\mu g / \sqrt{Hz}$ noise floor [55-57]. This constrains their applications to only middle and low end devices and systems. Today, many high-end inertial sensors are still dominated by very expensive non-MEMS or piezoelectric devices.

In capacitive sensing, normally micro-g resolution can only be realized by bulk accelerometers with large proof masses. Many of the reported high-performance capacitive accelerometers use multi-wafer bonding or SOI technology to form a large, thick proof mass [58-61]. Some special processes such as wafer dissolving, double-side process and thick Epi-SOI are also utilized in the fabrication of bulk micromachined capacitive accelerometers [62-64]. Recently a high-sensitivity bulk silicon capacitive accelerometer with a mechanical noise floor of $0.18\,\mu g / \sqrt{Hz}$ was reported [65]. All these reported bulk micromachined capacitive accelerometers employed wet etches to form the large proof masses. The special techniques such as wafer bonding and automatic stop in wet etching complicates the fabrication. If glass is used in wafer bonding to form silicon-on-glass (SOG) accelerometers [66], the temperature performance of the devices could be degraded due to the mismatch of the thermal expansion coefficients between the glass substrate and the sensing element. SOI technology makes the fabrication and further

monolithic integration of the accelerometer very costly. The previous works on bulk micromachined capacitive accelerometers are summarized in Table 1-1.

Table 1-1 Summary of previous work on bulk micromachined capacitive accelerometers.

Contributors	**Published year**	**Structure and/or process used**	**Accelerometer performance (noise floor)**
Rudolf et al [58]	1990	Sandwiched silicon-glass	$1.0\ \mu g/\sqrt{Hz}$
Henrion et al [59]	1990	Sandwiched silicon-glass, Multi-step wet etch	$120\ dBg/\sqrt{Hz}$ 260 Hz bandwidth
Warren [60]	1994	SIMOX	N/A
Bernstein et al [61]	1999	Silicon-glass bonding Dual chips Combination of wet and dry etch Automatic wet etch stop	$1.0\ \mu g/\sqrt{Hz}$ 1 kHz bandwidth
Yazdi, et al [63]	2000	Combination of bulk and surface micromachining Wet release	$0.23\ \mu g/\sqrt{Hz}$
Yazdi et al [65]	2003	Combination of bulk and surface micromachining Wet release	$0.18\ \mu g/\sqrt{Hz}$
Chae et al [62]	2005	SOG structure Silicon-glass bonding Silicon thinning by CMP Dry release	$79\ \mu g/\sqrt{Hz}$

Other non-mainstream technologies were reported for fabrication of specific capacitive accelerometers as well [67-69]. These technologies require some unique processes and equipments which are currently cost-prohibitive for commercialization.

The DRIE post-CMOS MEMS technology can be used in bulk micromachining for in-plane or out-of-plane capacitive sensing devices. It has the capability of creating thick structures with pure dry etch, which avoids the problems in wet release. An in-plane driving, out-of-plane Coriolis acceleration sensing gyroscope has been demonstrated using this bulk DRIE post-CMOS MEMS technology [70].

The achievable device performances versus device sizes with different technological approaches mentioned above are further illustrated in Figure 1-4. DRIE CMOS-MEMS technology has advantages of monolithic integration of bulk MEMS structures and interface circuits fabricated using mainstream CMOS technologies, allowing MEMS devices with overall higher system performance.

In this work, 3-axis and single-axis single-crystal silicon (SCS) accelerometers are designed and fabricated using an improved DRIE post-CMOS MEMS technology [71].

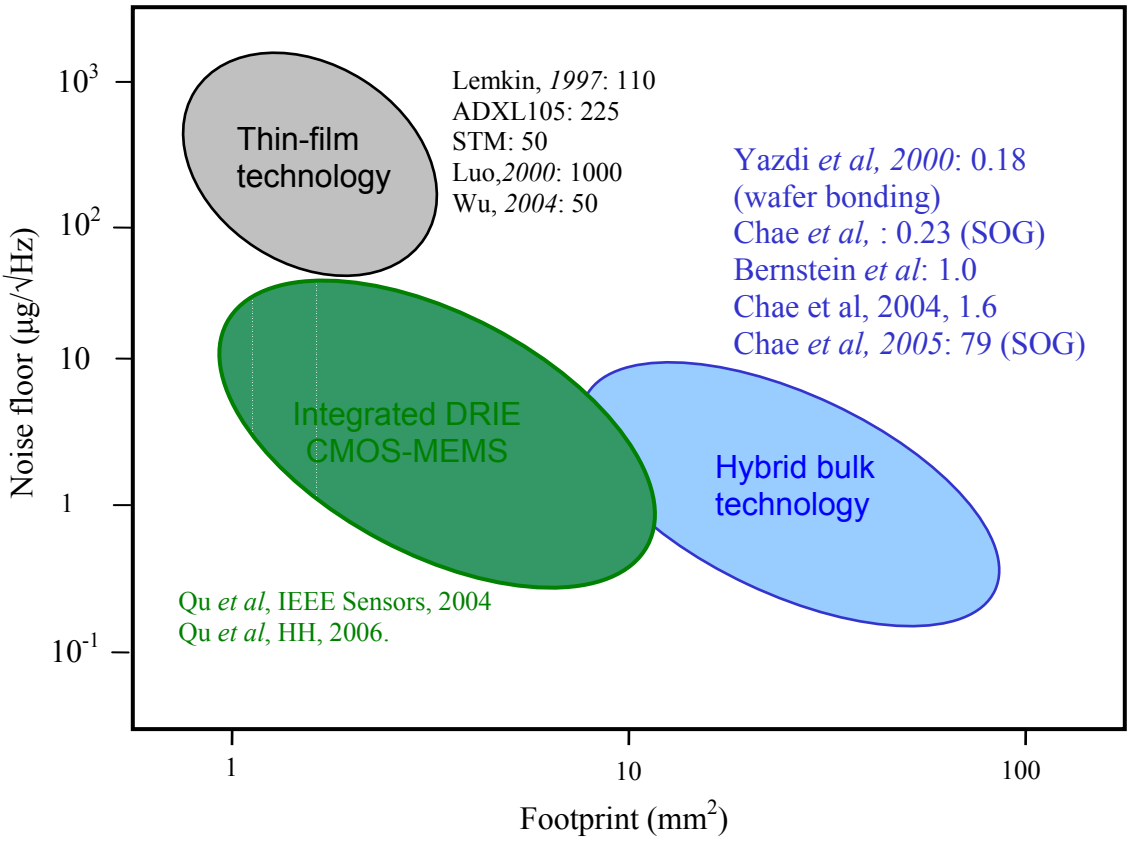


Figure 1-4. Achievable device performance versus device size with different technological approaches shows the advantage of the DRIE CMOS-MEMS technology.

1.3 3-Axis CMOS-MEMS Accelerometers

Millions of portable personal electronics require smaller inertial sensors for easier operation and more functionality. Integrated dual- or tri-axis accelerometers are advantageous for these portable devices in terms of compact size and multi-axis sensing.

The first monolithic single-axis accelerometer was industrialized by ADI [72]. Later on, dual-axis monolithic accelerometers were also commercialized. Recently tri-axis integrated accelerometers have been released by a few industrial companies [3, 4, 73, 74]. The majority of multi-axis accelerometers in the market are hybrid, where single-axis sensing elements and conditioning circuits are assembled together and packaged in the same enclosure. There is a tradeoff between the monolithic integration and hybrid approaches. The advantages of monolithic integration are smaller device size and better signal conditioning. But these advantages are attained at the cost of more complicated fabrication processes. The hybrid solution, on the other hand, allows optimized mechanical structures and signal processing circuits to be realized by dedicated and well-established fabrication processes. The drawbacks include the relatively large package sizes and large parasitics caused by the wiring and bonding between the sensing elements and the signal processing application-specific IC (ASIC). Some high performance hybrid capacitive accelerometers were reported from both industry and academic institutes [62, 66, 75, 76].

Multi-axis accelerometers employing other sensing mechanisms are also available. With proper design of the suspending beams and the configuration of piezoresistive bridge, 3-axis piezoresistive accelerometers with a single proof mass can be easily achieved using SCS or SOI [21, 77]. Some 3-axis piezoresistive accelerometers are already available as volume products [78, 79].

However, in most of the reported monolithic dual-axis or tri-axis accelerometers, separated in-plane and out-of-plane proof masses are used. Or, at least the out-of-plane element for z-axis sensing is separated from the lateral element where x, y-axis sensing parts share the same proof mass [80]. The advantage of the separated proof masses is usually the reduced cross-talk between the sensing axes. Yet it is self-evident that the electrical performance is degraded by the larger parasitic effects. In addition, this approach is less economical due to the large device size, especially for middle to low end capacitive accelerometers used in consumer electronics where small size and low cost are the main concern.

The lack of 3-axis monolithic capacitive accelerometers with a single proof mass is due to the difficulty in the realization of vertical out-of-plane and lateral in-plane sensing using a shared proof mass. Z-axis sensing has two primary challenges. The first is how to use horizontal electrodes to sense out-of-plane displacements with the presence of large parasitic capacitances to the substrate, especially when differential sensing is needed. The second is how to realize large capacitance changes in the z-axis using vertically-oriented electrodes. In most of the reported z-axis capacitive accelerometers where the z-axis proof mass moves vertically, polysilicon is used as the lower electrode of a horizontally-oriented sensing parallel plate capacitor. A fixed reference capacitor is also typically fabricated on the substrate. Therefore, it is difficult to have a fully differential output from the sensor node [14, 81].

Recently a z-axis sensing torsional accelerometer with horizontal capacitors and differential output was reported [82]. Due to the asymmetric arrangement of the sensing capacitors, the satisfactory linearity of the accelerometer is only limited to 1g. Moreover,

the sensitivity of the accelerometer is extremely constrained by the process performed on a costly SOI substrate. The process is less controllable in that the formation of the horizontal gap for vertical sensing is greatly affected by the later processes. Only a minimum of 4μm vertical gap can be achieved due to the influence of the damping hole etch on the pre-defined z-sensing gap. In another torsional z-axis accelerometer fabricated using dissolved wafer process (DWP), acceleration in z-axis is detected by vertically-oriented interdigitated capacitors [83]. The change of the capacitance between stators and rotors are caused by the variation of their common area instead of the change of the gap between them. A linearity of 0.2% in an acceleration range of -4 ~ 3g and a mechanical noise of $0.28\,mg/\sqrt{Hz}$ was achieved. No differential output can be realized from the sensor node due to its mechanism. Thus, this accelerometer can not detect the direction of the acceleration in z direction.

If fully-differential z sensing can be properly realized, the cross-talk among three axes can be greatly eliminated and the sharing of the same proof mass for 3-axis sensing will be feasible with proper mechanical design. More recently, fully differential z-axis accelerometers using sidewall capacitance formed by CMOS metal layers were reported [84, 85]. Due to the thin film mechanical springs employed in these accelerometers, these devices still suffer the constrains of thin film devices.

This thesis work targets an integrated 3-axis capacitive accelerometer with a shared, bulk silicon proof mass scheme [86]. With a unique z-axis sensing mechanism, fully differential sensing will be achieved in all three axes. The developed DRIE post-CMOS MEMS technology will be employed in the fabrication of this compact tri-axis accelerometer.

1.4 Thesis Goals and Organization

In this thesis work, a novel DRIE post-CMOS MEMS technology is developed, and two devices - a 3-axis and a single-axis integrated accelerometer - are designed and fabricated based on the new fabrication process.

In the improved DRIE post-CMOS MEMS, details of dry etch based micromachining of the designed MEMS devices with fine structures are explored. In particular, some physical effects that arise from the plasma etching and affect both the mechanical and electrical performance of suspended MEMS structures are investigated. These detailed fabrication studies are directed towards creating general design rules and optimizing the design and fabrication of MEMS devices. An integrated 3-axis and a single-axis accelerometer are designed and fabricated to demonstrate the features of the improved DRIE post-CMOS MEMS technology. Device design details are presented.

Chapter 1 introduces the background of CMOS MEMS technologies. Particularly, the evolution of post-CMOS MEMS technology is presented and the prior works on a variety of non-CMOS, CMOS-MEMS capacitive accelerometers are reviewed.

Chapter 2 is a technological introduction of plasma etch processes. Basic processing tools used in the developed post-CMOS technology are introduced. Electron cyclotron resonance (ECR) and inductively-coupled plasma (ICP) etchers for anisotropic SiO_2 etch and silicon DRIE are introduced. Etching system configurations are described, and the system characterizations are detailed based on the particular microfabrication requirements for accelerometers.

Chapter 3 illustrates the DRIE post-CMOS MEMS technology and its potential applications. For comparison, thin-film post-CMOS MEMS process and other previously investigated DRIE CMOS-MEMS process are also addressed.

Chapter 4 focuses on the device design of the accelerometers. The mechanism of fully differential z-axis sensing is detailed in addition to the lateral-axis accelerometer design. Mechanical design and modeling of the single and 3-axis accelerometer are given, and performance of the devices is predicted.

Chapter 5 discusses some specific practical issues in the fabrication of the devices. Contaminations of the surface and sidewalls of the sample during plasma processes, and their impact on the successful device release are addressed. Thermal effects on MEMS structures in the DRIE release step are investigated. To have a better control of the etch process, especially the release step, a simplified model is created to estimate the temperature rising on the suspended MEMS structures during the plasma etch. This model helps in understanding and eliminating of the structure damage caused by the thermal effect mentioned above. Based on these observations in the microfabrication, MEMS device design rules and optimization considerations are discussed.

In Chapter 6, the characterizations of the fabricated devices are detailed. The experimental setups are introduced followed by test results. Discussions on the performance of the devices are addressed.

Chapter 7 concludes the thesis work and proposes some future work including the wafer-level microfabrication processes for CMOS-MEMS devices.

CHAPTER 2
DRY POST-CMOS MICROFABRICATION AND TOOLS

To improve the performance of MEMS devices, a new DRIE post-CMOS MEMS technology has been developed in this thesis work. This post-CMOS micromachining consists of multiple plasma etch steps of SiO_2 layer and Si substrate. Therefore, in the development of the new technology, individual plasma dry etch process should be optimized. As part of this thesis work, thick SiO_2 anisotropic RIE etch and Si DRIE used in the new technology were investigated and optimized. Test structures were designed for the purpose of individual process calibration and the extraction of critical technology-based device design rules.

In this chapter, plasma etch technologies involved in the developed DRIE post-CMOS technology are introduced and the relevant etching systems are calibrated using the test structures. The choice of the processes for the new technology is based on the availability of the qualified equipments locally on campus at the University of Florida.

2.1 Plasma Etch

In MEMS structure release, plasma dry etch method has advantages over wet etch in structure profile control, stiction prevention and etch efficiency. The DRIE post-CMOS MEMS technology developed in this work is completely based on the plasma dry etch of SiO_2 and silicon. Therefore, the control of these plasma etch processes is a critical issue to the fabrication and the final performance of the MEMS devices. The dielectric etch is used to open the patterns of MEMS structures, therefore anisotropic profiles are needed. For silicon etch, both isotropic and anisotropic processing are used. Normally, in

terms of the feature size and etching depth, plasma etch in MEMS microfabrication differs from that in VLSI and ULSI. Their differences can be summarized in Table 2-1.

Table 2-1 Comparison of plasma etch in IC and MEMS

Plasma Etching Parameters	**In ICs**	**In MEMS Devices**
Feature size	Small	Relatively large
Depth	Small	Large
Aspect ratio	Small to middle	Middle to large
Structure refill	Yes	Normally No
Etching time	Short	Long
Etch induced structure damage	Less	More
Etched surface contamination	Less	More

There are many kinds of plasma-based etch technologies in which both chemical and physical processes are employed for the etch [87]. Plasma can be described as an electrically neutral gas that contains equal numbers of positive and negative charges in addition to neutral atoms, radicals or molecules and photons emitted from the excited species [88]. Positively charged carriers are mostly ionized atoms, radicals, or molecules created by the impact of particles with electrons. The majority of negative charges are electrons. However, when some of positive carriers capture electrons from the plasma, they can also convert themselves into negative charges. Neutral atoms, radicals and molecules can be in their ground states or excited states. When species in an excited state lose their energy via spontaneous transitions to resume their lower energy levels, photons are emitted and a plasma glow is observed. Many external parameters, such as chamber pressure, reactor geometry and residence time in the reactor, affect the composition and relative concentration of individual carriers. Radicals and neutrals are main reactive species in the plasma etch. Radicals are much more abundant in a glow discharge (plasma) than ions because of their lower excited energy state and longer life time. However, the relative fluxes of radicals and neutral atoms are compatible. This is due to

the following two factors. On one hand, ions move faster than radicals as a result of kinetic energy gained from the applied electric field. On the other hand, heavier radicals move toward the substrate mainly by diffusion. Radicals have a larger tendency to be absorbed on the reacting surface due to their unfilled outer electron shell.

The etch process in plasma can be categorized into seven steps, as shown in Figure 2-1.

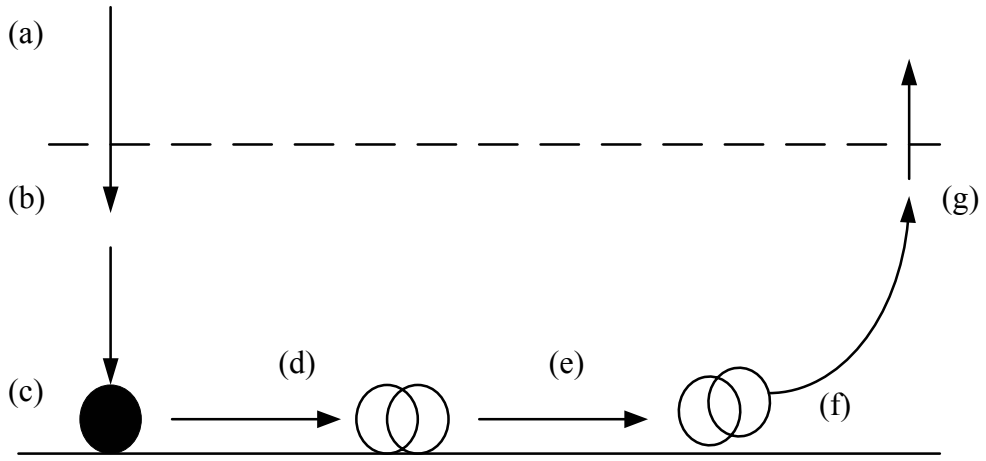


Figure 2-1. Seven steps of the etch process. (a) Dissociation and ionization of the reactive species. (b) Diffusion of the reactive radicals. (c) Absorption of radicals on surface. (d) Radical surface diffusion. (e) Chemical reaction. (f) Desorption of the by-products. (g) By-product diffusion to the chamber.

Reactive species (radicals, ions, etc.) are generated by excitation, dissociation or ionization in the glow discharge. By diffusion or acceleration due to the external electric field, these particles reach the substrate. Radicals are absorbed on the substrate surface, while ions, with their momentum, may disintegrate upon impact to the substrate and penetrate into the surface for a certain depth. With the help of surface diffusion, the reactions may happen locally on the landing site of the carriers, or somewhere in the

diffusion path of the carrier on the substrate surface. Finally, the reaction products leave the substrate surface, either by desorption if the by-products are volatile, or by ion-activated processes, and diffuse back into the plasma [87].

There are four basic etching mechanisms which contribute unequally to the etch process. They are illustrated in Figure 2-2 and their impacts on the etched materials are summarized as the following.

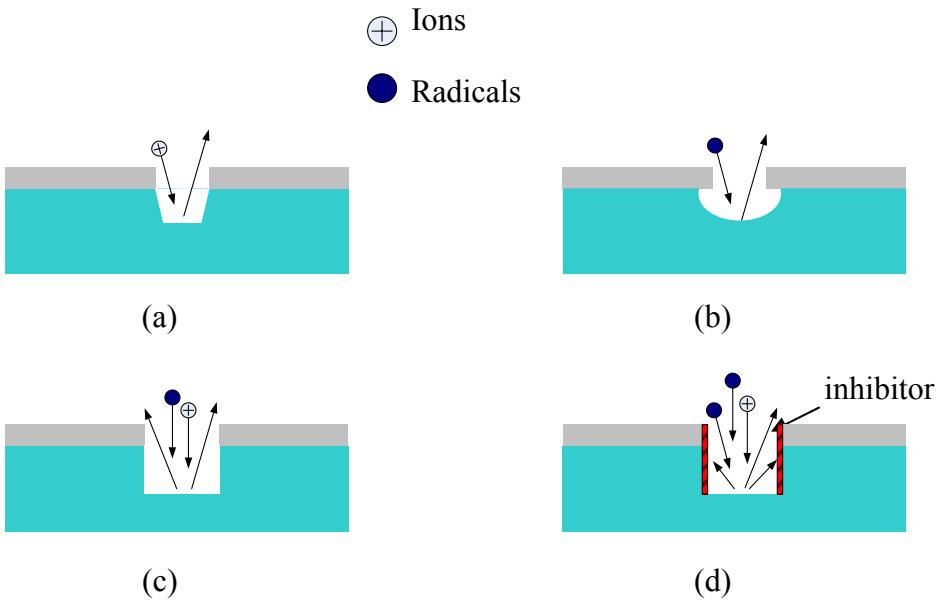


Figure 2-2. Four basic etch mechanisms. (a) Physical sputtering. (b) Chemical reaction by neutral radicals. (c) Ion enhanced chemical reaction. (d) Ion enhanced inhibitors.

Physical sputtering. The interaction of the impinging ions with substrate surface is a purely physical process in which momentum transfer is involved. The substrate atoms are mechanically ejected by ions with kinetic energy typically higher than 200 eV. This results in very anisotropic profiles, rough surface morphology, trenching effect and poor selectivity. The high energy ion bombardment always causes damages to the substrate.

Due to its physical nature, the etching rate of sputtering is very slow, lowing the efficiency of this etch method.

Chemical reaction. This etch is dominated by the chemical reaction between the neutral reactive species and the substrate, which results in volatile by-products. The chemical reactions rely on the formation of the reactive species and their absorption on the surface of the substrate. However, the main requirement for the chemical etch is the volatility of the by-product from the reaction. Good etch rate and high selectivity can be obtained from chemical etch, and the plasma induced damage can be minimized. With less physical enhancement, chemical etch demonstrates isotropy which is unwanted for the formation of vertical profile.

Energetic ion-enhanced chemical reaction. The neutral radicals slightly interact with the surface of substrate. The impinging ions alter the substrate or product layer, so that chemical reactions can take place more efficiently at the interface and the by-products can be delivered more easily into the plasma. This process offers highly anisotropic features since sidewalls receive minimal ion flux.

Ion-enhanced inhibitor. The inhibitor species form a polymer like thin film on sidewalls, which excludes the impinging neutral etchant. This process prevents the sidewall from being etched and thus leads to an increased anisotropy. It differs from the energetic ion-enhanced reaction in that the chemical etching can take place without the presence of impinging ions. Neutral etchant species spontaneously gasify the substrate material, and ions play a role by interacting with another component instead of substrate material and reaction by-product. That component is the protective inhibitor film. The ion flux breaks down the protective inhibitor film on the horizontal surface which is at a right

angle to the flux, allows the chemical etch to proceed anisotropically. Meanwhile, the protective film is not removed from the vertical sidewalls because these surfaces only intercept few ions scattered from other directions. The protective inhibitor may originate both from the involatile etch by-product or from film-forming precursors that absorbed on the surface of substrate during the etching process.

The last two ion-assisted plasma etch mechanisms dominate in most dry etching techniques that are widely used in VLSI and MEMS manufacturing and microfabricating. Reactive ion etch (RIE) is widely used in dielectric etch because of its high etch rate, high selectivity and easy control of the etching profile. Deep RIE provides an effective method for deep trench etch in silicon substrate to achieve bulk MEMS devices.

Several energy coupling methods have been developed in the configuration of plasma reactors [88]. Of them electron cyclotron resonance (ECR) and inductive coupled plasma (ICP) are most widely used due to their high plasma density thus effective etch. Both of them can work at lower pressure and provide higher aspect ratio etching. The long mean free path (MFP) of gas molecules and ions due to the low system pressure can reduce the scattering collision, enabling very directional etch along the direction of biasing electric field. More power can be coupled into plasma due to the high ion density sources, resulting in greater dissociation of etch species.

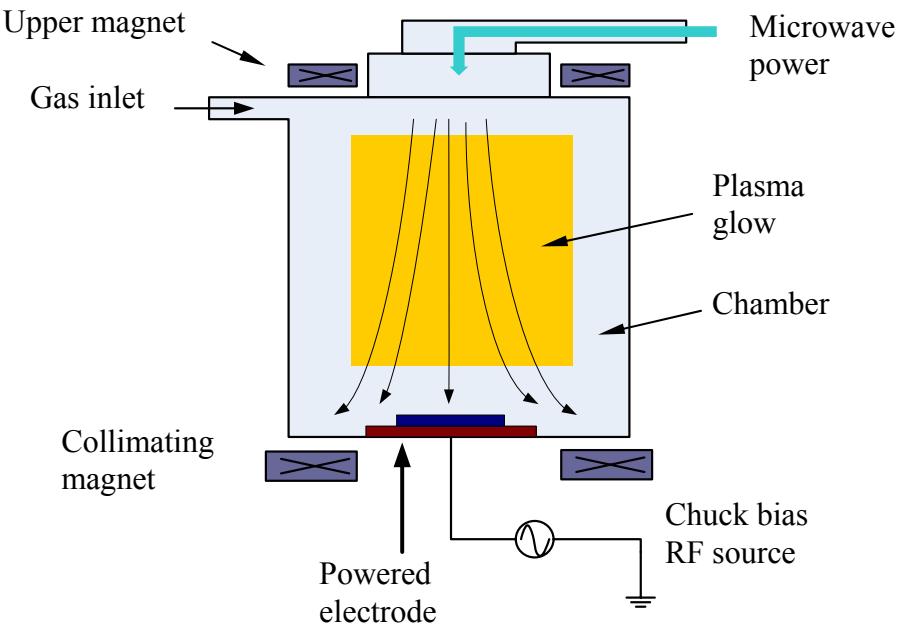
The main difference between an ECR and ICP system lies in the method to shape and sustain the plasma. An ECR reactor employs an external magnetic field to shape and contain the plasma; while an ICP reactor uses an inductively coupled RF bias to sustain high density ions in the discharge [88]. The configurations of these two systems are illustrated in Figure 2-3.

In an ECR reactor, microwave energy is coupled to the natural resonant frequency of the electron in the presence of a static magnetic filed. The resonance of electrons in plasma occurs when the microwave excitation frequency reaches the electron cyclotron frequency which is given by

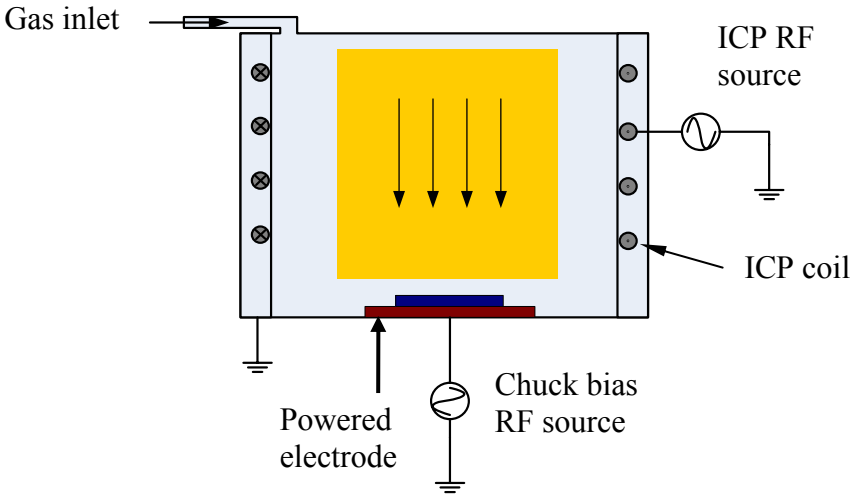
$$\omega_e = \frac{eB}{m_e} \qquad (2.1)$$

where e is the unit charge of an electron, B is the strength of the static magnetic field and m_e is the electron mass. In practice, this requirement can be satisfied in a discharge by adjusting the strength of the magnetic field. By presenting an electric field that is perpendicular to the magnetic field, as shown in Figure 2-3, the electrons are accelerated in the ECR volume to ionize and excite the neutral species. The result is a low pressure, low collision plasma that can be tuned from a weakly to a highly ionized discharge by changing pressure, gas flow and input microwave power. The advantage of the ECR setup is the easy and cheap microwave power coupling, non-electrode in the system and, low heating effect resulted from the electron collisions and, ultimately, the high density ions and radicals in the plasma. ECR has gained great attractions in many plasma processing applications.

On the contrary, an ICP reactor uses a radio frequency (RF) current applying to three coils in opposite directions to generate and alternating magnetic field in the upward and downward directions. It is the change rate of this magnetic field that induces a RF electric field which confines and accelerates electrons in a circular path. This inductive coupling is very efficient and leads to a high plasma density, normally one order higher than ECR coupling. Since the electrons are trapped in a circular path, they have little chance of reaching the sample chuck to lower the dc self-bias.



(a)



(b)

Figure 2-3. Configurations of ECR and ICP system. (a) ECR etcher, (b) ICP etcher.

Due to the well confined electrons, another RF source, driven at 13.56 MHz, is applied to the chuck which can control the dc bias separately. This configuration allows nearly independent control of ion flux (ICP power to the coils) and ion energy (RF power to the chuck), making the tuning of the etching easier. The etch rate of ICP reactor is much larger than other plasma etching tools due to the high concentration of the dissociated radicals and ions. In addition, since the electrons are relatively confined, fewer of them are lost to the chamber walls and electrodes compared to ECR, resulting in lower dc bias and less ion damage on the sample. High density plasma can operate at lower pressure, which increases the MFP of the radicals and ions and consequently increases the anisotropy of the etching profile.

No matter what kind of etcher is used, the basic requirements for the dielectric or silicon etching in MEMS technology remain the same. Relatively high etching rate, good uniformity and profile control, high aspect ratio and high selectivity are the main criteria for a good etching.

According to the availability of the reactors around, in this thesis work, an modified PlasmaTherm ECR etcher (SLR-770) was used for the SiO_2 etch and an ICP reactor from STS was employed for deep silicon etch in the development of DRIE post-CMOS MEMS technology. The etching system characterization was conducted before the device fabrication.

2.2 Characterization Methodology

Test structures were included on the same chips of the designed MEMS devices for the purposes of in-situ process monitoring and etching characterization. They were designed for the system characterization on assorted effects in SiO_2 RIE and silicon DRIE, which will be detailed in the following sections. Some layouts of the test

structures are given in Appendix A. In SiO_2 etch characterization, rectangular bars (cantilever beams after being etched) with permuted metal layer(s) were designed to characterize the etch rate and profiles. These cantilever beams were designed to have fixed length and width. This is to exclude the effects of process variations. In silicon DRIE characterization, similar cantilever beams with different spacing were designed to characterize the aspect-ratio dependent etching (ARDE) effect and the etching ratio.

A Dektak II step profilometer with accuracy of 10 nm was used in the depth measurement for etch system characterization [89]. In the developed DRIE CMOS-MEMS technology, the top aluminum layer acts as the etching mask in the etching steps of the front side process. Therefore, aluminum etching (mainly physical milling) rate was first characterized to define the reference plane in the measurement of etching rate in both SiO_2 and Si etch. After the glass passivation layer is etched and fresh top aluminum layer is exposed, part of the spare region on the chip surface is covered by photoresist or Kapton tape, which has very good thermal and chemical stability. As the SiO_2 RIE or Si DRIE proceeds, the uncovered aluminum area will be milled with a small rate. After certain etching time duration, a small step will be formed between the covered and uncovered aluminum area. By measuring the height of the step after the removal of the photoresist or Kapton® tape, and dividing it by the etching time, aluminum milling rate r_{al} is obtained.

Then, after an etching time of t in the following SiO_2 RIE or Si DRIE, the etching rate can be calculated as,

$$r = \frac{h + r_{al} \cdot t}{t} \qquad (2.2)$$

where *h* is the height of the measured step between the exposed top aluminum surface and the surface of etching front.

Since normally aluminum milling rate is much smaller than SiO_2 and Si etching rate, the second term from the Al milling in the numerator can be neglected.

A Joel 6400 scanning electron microscope (SEM) and a FEI Strata DB 235 focused ion beam (FIB) SEM were used for the etch profile observation and measurement.

2.3 SiO_2 Etch

In the development of DRIE post-CMOS MEMS technology, RIE SiO_2 etch is used to open the patterns of microstructures. After the SiO_2 etch, the top metal on the CMOS stacks with alternate metal and SiO_2 layers acts as the mask in the following Si DRIE. Thus the SiO_2 etch quality will directly affect the final microstructures. The SiO_2 RIE is a complex system in which many process variables have impacts on the etch results. In many cases, the influences of the process parameters are non-linear and co-related. Therefore, design on experiment (DOE) is needed for the device/process design and optimization.

2.2.1 Challenges in Anisotropic SiO_2 RIE

Figure 2-4 shows the multiple responses of a SiO_2 RIE system as a function of multiple system input parameters. The output of the RIE has some specific influences on MEMS structures due to the essential difference between the MEMS microfabrication and the standard IC processes. Compared to the requirements of the normal IC process, RIE used in MEMS technology has some special challenges.

The survival of the top metal layer and its profile. The SiO_2 layer that needs to be etched in a MEMS device is usually much thicker than that in the standard IC devices. This is due to the use of CMOS stacks that are consisted of alternate metal and SiO_2

layers. These CMOS stacks also act as masks in Si DRIE. The depth of the trench between the mask stacks measures from the surface of top metal to the interface of SiO_2/Si, ranging from a couple of μm to as high as ~ 12 μm depending on the different CMOS technologies employed. During the longer time SiO_2 etch, the top metal layer is exposed to the radicals and accelerated ions all the time, being milled physically or etched very slightly. The edges of the patterned top metal will be rounded and the microstructures will lose their critical dimensions.

The survival of interconnect vias and electrical connection of the MEMS device. The electrical connection failure of MEMS devices, mostly the failure of interconnect vias, may result from the SiO_2 RIE. There are two mechanisms of the electrical connection failure. The first is the milling of the top metal layer at the corners of the vias, leaving an open circuit due to the broken via corner. This is a physical process in which the ion bombardment damages via edges. The second failure mechanism is the lateral etch of the barrier layer (normally TiN) above or underneath each Al layer. On the fine microstructures with stacked CMOS layers, after the long SiO_2 RIE, the barrier layer could be chemically etched through in the lateral directions on each side of the thin structures, leaving the structure lose their electric connection. This lateral etch of the barrier layer can also cause the delamination of aluminum layers in the MEMS structures.

To satisfy the above and other more general requirements of the SiO_2 RIE, etching system should be very carefully characterized and design rules should be extracted from the characterization for the successful future designs.

2.2.2 System Characterization

A PlasmaTherm SLR 770 RIE reactor was used in the SiO_2 etch with CHF_3/O_2 as the etching chemicals. The output etch results were characterized as the functions of the system variables in Figure 2-4. Since the output parameters are correlated to more than one input variable, some tradeoffs should be made to have an optimal etch results. DOE experiments were performed by sweeping individual system parameter with other parameters fixed.

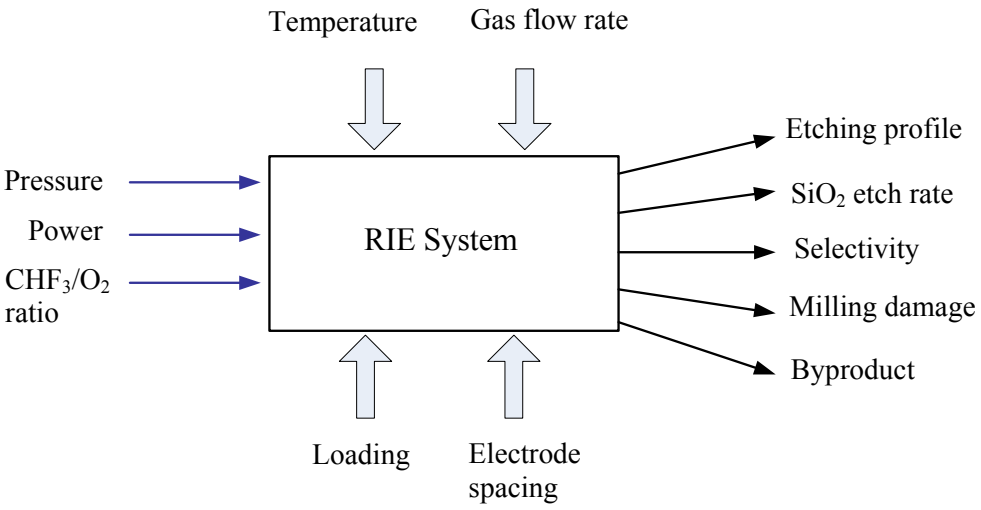


Figure 2-4. System response of the input parameters in a SiO_2 RIE system.

The correlation of the etch results with input variables can be qualitatively summarized as in Table 2-2.

Table 2-2. Influences of etching parameters on RIE etch results

Output / **Input**	**Etch rate**	**Top metal layer milling**	**Sidewall profile**	**Inhibitor polymers**
Microwave power ↑	↑	↓	↑	Varies
CHF_3 gas flow rate ↑	Varies	↓	Varies	Varies
Chamber pressure ↑	↓	↓	↓	↑
O_2/CHF_3 ratio ↑	Varies	Varies	Varies	↑
Dc bias of the sample ↑	↑	↑	↑	varies

2.2.2.1 Etching rate

To reduce the total etch time, an appropriate etch rate should be attained. Higher chemical etch rate helps to eliminate the ion milling of the top metal layer caused by the long time physical bombardment. The etch rate and milling effect should be balanced by adjusting the microwave power, chamber pressure and dc bias on the sample chuck (RF power applied on the chuck). Figure 2-5(a) shows etch rate as the function of the coupled microwave power. There is a steep section in the plot showing a critical value of the coupled microwave power (about 700W) for sufficient concentration of dissociated reactive radicals.

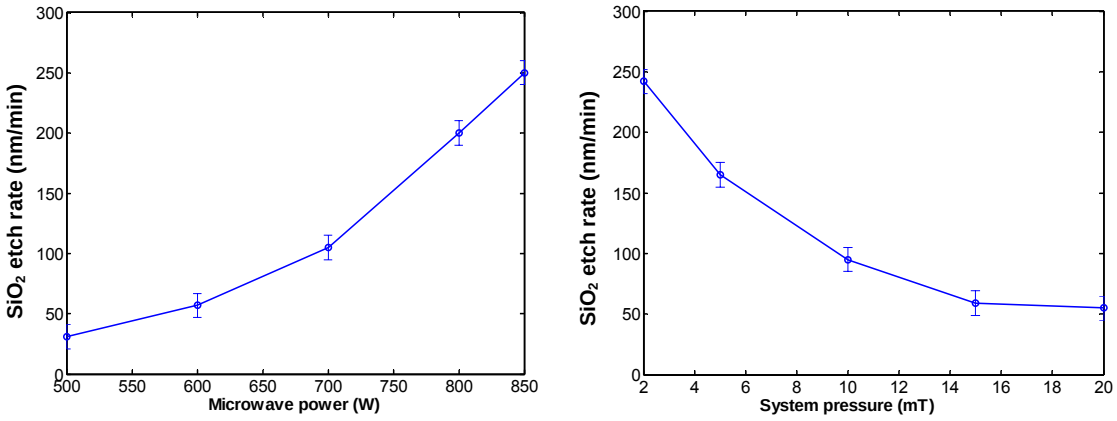


Figure 2-5. SiO_2 etch rate as functions of system parameters. (a) plot of the etch rate as the function of microwave power; (b) etch rate versus system pressure.

The coupled microwave power was selected as to be around 850W for an effective etch. Too high microwave power can result in the top layer metal damage. The chamber pressure dependence of the etching rate, as shown in Figure 2-11(b), reflects the ion assistance in the chemical etch. Lower pressure allows longer MFP thus higher kinetic

energy of the ions, which benefit the etching by bombarding the surface SiO_2 atoms, providing a fresh reaction front and easing the delivery of the byproduct.

2.2.2.2 Top metal layer milling

For long-time RIE of thick SiO_2 layers in CMOS stacks, the etch selectivity of SiO_2 over Al is critical for the survival of the top Al layer and vias. It is observed that aluminum etch during the SiO_2 etch is actually due to the physical ion milling effect on the aluminum layer. Therefore, the most significant influence on Al damage is from the chuck bias at a given chamber pressure. Figure 2-6(a) shows part of a capacitive sensing finger with milled top Al layer after 80 minutes of SiO_2 etch. The microwave power used in the etch was 700W at a system pressure of 5 mT. With a dc bias of 345V resulted from a 75W RF power, the top Al layer was milled to approximately 0.3 μm, which is only half of its original thickness.

If sidewall capacitance is used for vertical position sensing, as in the z-axis sensing of the 3-axis accelerometer, which will be addressed in Chapter 4, the milled Al layer will greatly reduce the sensing capacitance formed by Al sidewalls. In extreme case, damage to the MEMS devices will arise in the subsequent etch processes if the top Al layer, which acts as the mask for other etch steps, is completely milled away in the SiO_2 etch. Under a similar etch condition, the corner of an interconnection via on a bonding pad of a micromirror was etched away, resulting in an open circuit of the actuation polysilicon heater, as shown in Figure 2-6(b). A lower chamber pressure increases the MFP of the ions, allowing higher kinetic energy of the ions, which in turn reduces the selectivity of SiO_2/Al and deteriorates the damage on the top metal. This trend is shown in Figure 2-6(c).

In practice, the microwave power was increased to 850W and the dc bias was reduced to 140~150V. This results in a proper etch rate between 0.25 μm/min and 0.33 μm/min with a low aluminum milling rate. A selectivity of SiO_2/Al as high as 50 has been achieved.

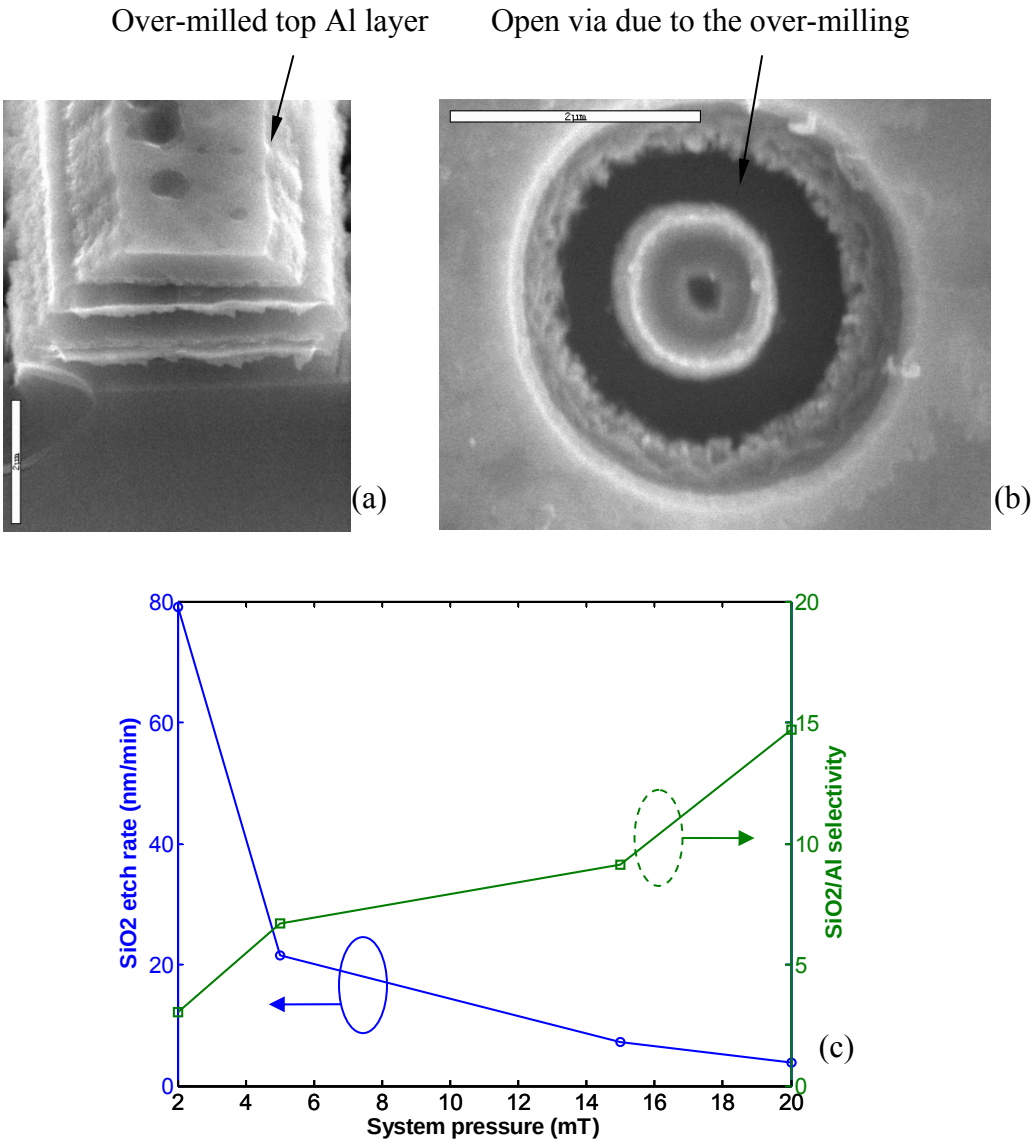
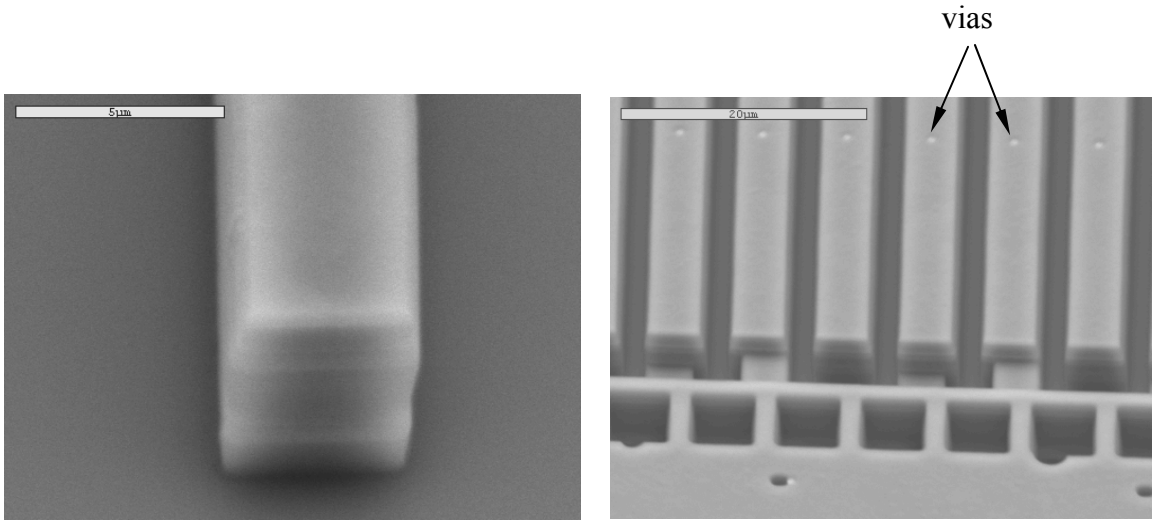


Figure 2-6. Impact of the SiO_2 etch on the top Al layer. (a) over-milling of the top Al layer on a comb finger of the fabricated accelerometer, (b) open via in an electrothermal micromirror. (c) SiO_2 etch rate and etch selectivity as the function of system pressure.

2.2.2.3 Sidewall profile of the SiO_2 layers and CMOS stacks

The main system variable which affects the sidewall profile of SiO_2 layer is the chamber pressure. With higher chamber pressures, the MFP of the ions and radicals reduces, resulting in more random collisions among the radicals. The deflected ions and radicals attack and react with the SiO_2 on the sidewall, consequently resulting in a more isotropic profile. For CMOS stacks with multiple layers of Al, it is prone to have an undercut on the SiO_2 between metal layers at a high chamber pressure. After optimization, a 10 mT system pressure was selected for an adequate etching rate and a reasonable SiO_2 profile.



(a) (b)

Figure 2-7. Profiles of the CMOS stack at different process stages. (a) after the first SiO_2 etch; (b) after the second SiO_2 etch. SiO_2 etch was performed with a system pressure of 10 mT.

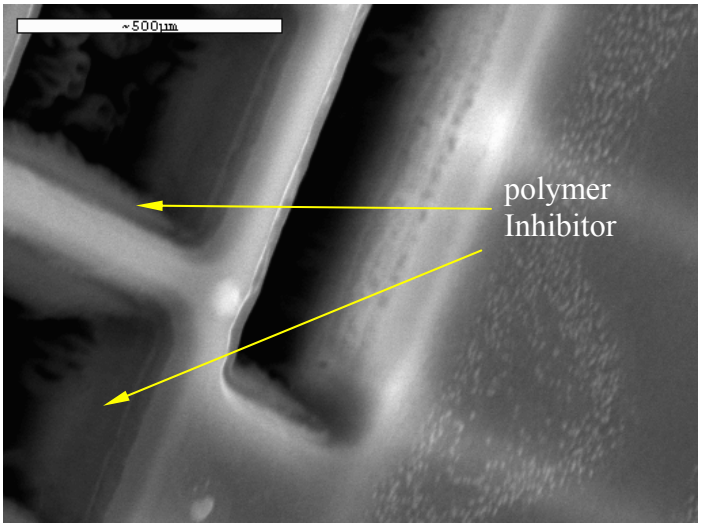
Note there are two SiO_2 RIE steps in the developed DRIE post-CMOS MEMS process. The first SiO_2 etch is to open the pattern of electrical isolation structures; while the second is for other structures. Figure 2-7(a) and (b) show the sidewall profiles of CMOS stacks after the first and second SiO_2 etch respectively. It can be seen that a

straight vertical SiO_2 profile has been obtained and the vias have been nicely kept in shape after the second SiO_2 etch, as shown in Figure 2-7(b).

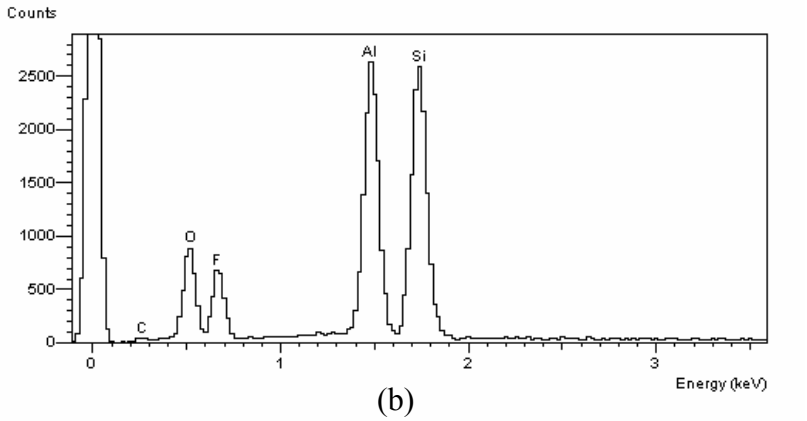
2.2.2.4 The inhibitor polymer redeposition on the sidewall

As one of the RIE mechanisms, inhibitors generated in the SiO_2 etch provide a protection layer to the sidewall, making the etch more anisotropic. However, if the feature size of the MEMS structure is small, or, if the inhibitors redeposited on the sidewall are too thick, they will affect the feature size. This is due to the micromask effect of the inhibitor film in the following SiO_2 RIE and Si DRIE. In addition to the etching system variables (e.g. chamber pressure, microwave power and biasing RF power), the oxygen concentration in the CHF_3/O_2 etching chemical plays an important role in the formation of the inhibitor polymers.

The SEM image in Figure 2-8(a) shows the thick inhibitor film formed on the sidewall of the SiO_2. The energy dispersive spectroscopy (EDS) compositional analysis result is also shown in Figure 2-8(b). The analysis was obtained by using the EDS system integrated in a Joel 6400 SEM system. The presence of elements F, C and O in the film indicates the polymer nature of the inhibitor. The existence of aluminum in the redeposition layer is the evidence of the ion milling of the top Al layer. The milled Al atoms collide with the downward ions from the plasma bulk and are swept to the CMOS stack trench. They are then scattered to the sidewall by the reflected ions from the bottom of the etched trench. The contamination of the sidewall with inhibitor film containing Al will cause some problems in the silicon etch for the release of the MEMS structures. This particular issue is addressed in Chapter 5.



(a)



(b)

Figure 2-8. Inhibitor polymer formation in SiO_2 etch. (a) Thick polymer layer on the sidewall of isolation holes. (b) EDS spectrum of the inhibitor polymer.

Experimental results show that not only does oxygen concentration in the etching gas affect the etch rate, but it also has impact on the formation of the inhibitor polymer film in the etching. Figures 2-9 shows the SiO_2 RIE etch rate as the function of the oxygen concentration in the CHF_3/O_2 etching chemicals. The etching rate peaks at the O_2 concentration of about 5% ~ 10%. It is widely accepted that in a certain concentration range, the additive oxygen helps in dissociating more F radicals which is the main etchant

in the SiO_2 etch [90]. When the O_2 concentration is higher than 15%, Teflon-like $(CF_2)_x$ inhibitor will form, and the SiO_2 etching rate reduces. On the other hand, if O_2 ratio is too low, it does not help the dissociation of the CHF_3. The plot agrees with the reported ECR RIE of SiO_2 [91]. Figure 2-10 shows the polymer formed on the sidewall of CMOS stacks after the final Si etch is performed. In Figure 2-10(a), thick polymer is present with a higher oxygen concentration of 40%. In Figure 2-10(b), the redeposition of the polymer is greatly reduced by lowering the oxygen concentration to 6.7%. The clean CMOS stack sidewall is highly desired in the subsequent Si etch, especially when alternate SiO_2 and Si etch are required in the micromachining processes.

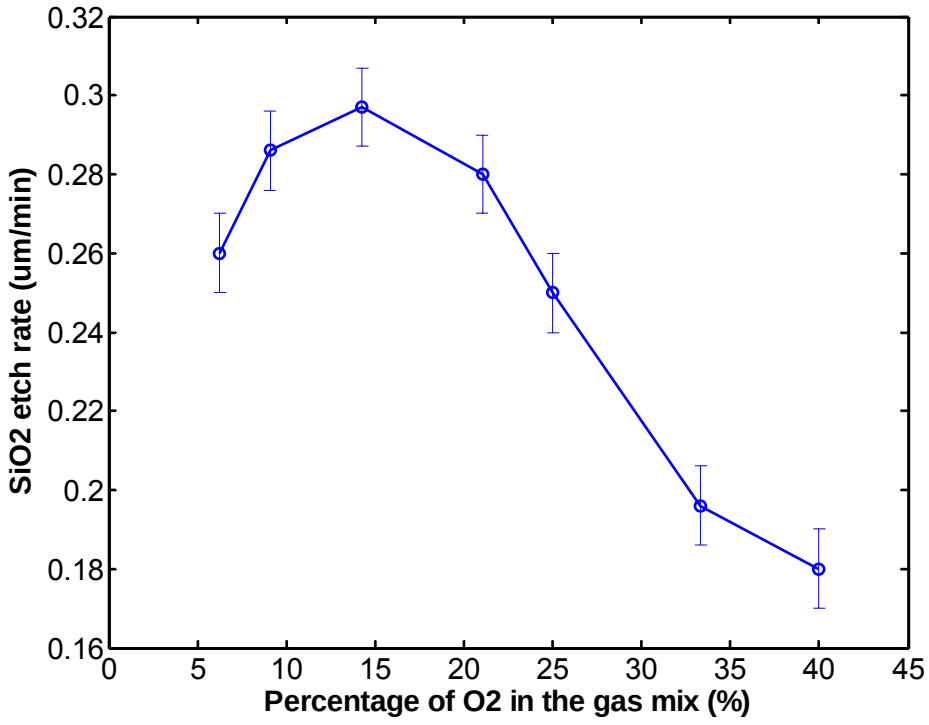


Figure 2-9. SiO_2 etching rate as the function of oxygen concentration in the CHF_3/O_2 gas mix.

The oxygen concentration in the gas flow also has affects the etch selectivity of SiO_2 over Si. A lower oxygen concentration increases the SiO_2/Si etching ratio by reducing the Si etching rate. In our experiment, the etch selectivity of SiO_2/Si increases from 1.67 at a 40% oxygen concentration to 4.1 at 3.3% of oxygen concentration.

The final recipe for the SiO_2 etch is listed in Table 2-3.

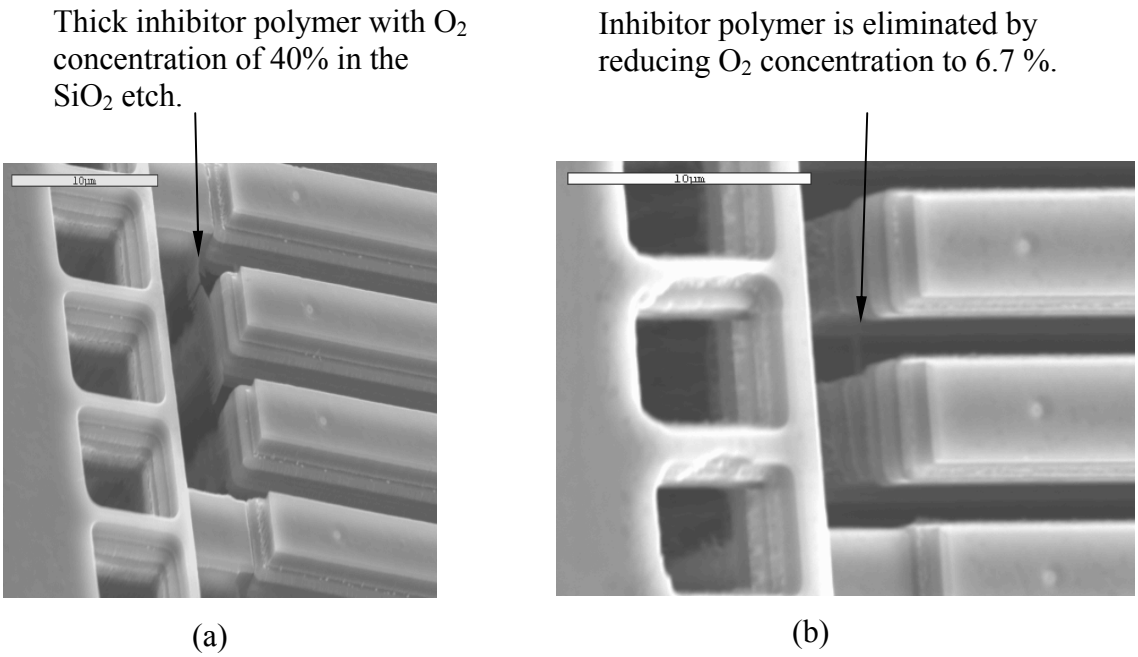


Figure 2-10. Inhibitor polymer formation as the function of oxygen concentration in the CHF_3/O_2 mixture. (a) Thick inhibitor polymer with O_2 concentration of 40% in the SiO_2 etch. (b) Inhibitor polymer is reduced by reducing O_2 concentration to 6.7 %.

Table 2-3. Anisotropic SiO_2 etch recipe on the PlasmaTherm SLR770 ECR RIE system

Parameters	**Settings**
CHF_3 flow	30 sccm
O_2 flow	3~5 sccm
RF2 power	850W
RF1 power (platen)	40W~50W (140~150V bias)
Chamber pressure	10 mT

2.4 Advanced Silicon Etch by STS ICP DRIE

Silicon DRIE is now a standard process for both bulk and surface micromachining in MEMS fabrication due to its capability of high-aspect-ratio etch and high selectivity over photoresist and SiO_2. It is common in an advanced silicon etch (ASE) system to achieve an aspect-ratio (AR) of over 30, with selectivities over PR and SiO_2 being higher than 50 and 100 respectively [92]. In the fabrication of many MEMS devices, silicon DRIE is the final dry release step. Since the normal etch time of a silicon DRIE step is relatively long, especially when a thick MEMS structure is fabricated, a number of geometry-related effects also play very significant roles in the final structure formation. These effects should be considered at both the device design and fabrication stages as additional design rules which are of equal importance as the basic process requirements [93, 94]. According to the fabrication level, the geometry-depended effects and other process variations can be categorized into inter-die effects and intra-die effects. The inter-die effects include spatial cross-wafer etch rate variations induced by the chamber geometry, and the macroloading effect caused by a global variation of etching species. The intra-die effects consist of aspect ratio dependent etching (ARDE) and microloading effect.

There is a difference between ARDE and microloading effect. ARDE is an effect in which the etch rate decreases as a result of the reduced transport of reactive species in deep and narrow structures. Whereas in microloading effect, the etch rate reduction is caused by a local depletion of reactive species.

In the improved DRIE post-CMOS MEMS technology, which is detailed in Chapter 3, three silicon DRIE steps are used in the fabrication of the accelerometers. The first is the backside etch by which the chip or wafer is thinned to the desired thickness.

The second step is the etch-through of the isolation trenches. The third is the etch-through of the structures to release the device. If necessary, more DRIE can be conducted in between the above two steps to form some particular structures. For example, one more silicon DRIE and isotropic silicon undercut is needed to create the isolation structure in the developed capacitive accelerometer.

In this section, the characterization of the DRIE etcher and some geometry-depended effects in the silicon DRIE are addressed. The silicon DRIE in the developed post-CMOS MEMS technology was conducted using an ICP etcher from Surface Technology Systems (STS), LLC.

2.3.1 ICP Silicon DRIE System Configuration

The system configuration of the STS ICP etcher is shown in Figure 2-11. As described in the previous sections, the key feature of the ICP system is the separation of the two RF powers in the system, i.e., the RF power for the generation of etching radicals and the other RF power for the sample bias. The RF coil at the top of the ceramic chamber supplies the power to dissociate the species and generate radicals; and the RF power applied to the bottom electrode provides power for directional etch. It is this power applied on the bottom electrode that generates a dc bias for the self-bias of the carrier wafer on which the sample to be etched sits. This configuration allows independent power tuning for species dissociation and sample bias. More power can be delivered to the top coil without affecting the self dc bias. As described in the previous section, compared to a RIE system, the ions in an ICP system are more confined in the plasma bulk due to the alternate magnetic field generated by the RF power on the coil, resulting in more collisions of ions with molecules and consequently higher plasma density in the system. For a processing pressure somewhere between 1 mT and 100 mT, the plasma

density is between $1\times10^{11}/cm^2$ and $1\times10^{12}/cm^2$, which is two orders of magnitude higher than in a traditional RIE system. Because of the high density of ion flux onto the sample chunk, the wafer in the process has to be cooled by helium flow running underneath the backside of the sample chunk. An effective vacuum system is required to reduce the residual time of numerous etch by-products in the chamber.

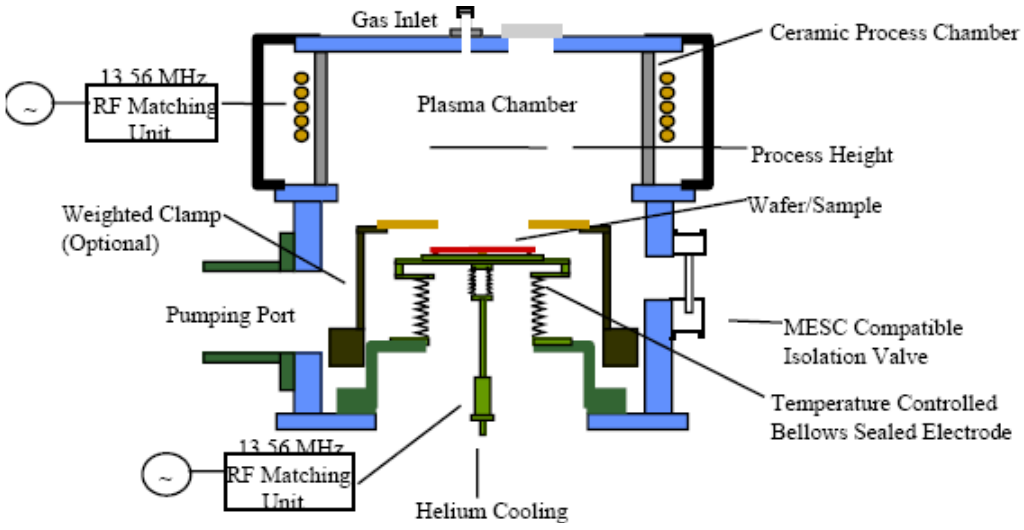


Figure 2-11. Configuration of the STS ICP ASE system. (Adapted from STS webside.)

2.3.2 Silicon Anisotropic Etch

ASE employs Bosch process to achieve anisotropic etch [95]. The essence of the Bosch Process is the alternate etch and passivation steps in the whole process duration, as shown in Figure 2-12.

The etching cycle utilizes SF_6/O_2 mix gas flow to etch exposed silicon. C_4F_8 flow is used for the passivation of sidewalls of the etched structures. The preference of SF_6 to pure F_2 as the reactive gas is due to its lower toxicity. SF_6 is dissociated into the reactive F radical and unsaturated fluorosulfur (S_xF_y) in the plasma. The added oxygen in the

reactive gas SF_6 has two functions in facilitating the silicon etch. The first is to oxidize the surface of silicon, making the passivated oxide layer on Si surface easier to be removed by the impinging ions, subsequently allowing more fresh silicon surface exposed to reactive atomic F. The second function of additional oxygen is to react with the unsaturated S_xF_y, enabling more reactive atomic F while depleting polymer-forming species. In the etching cycle of Bosch Process, three processes - the passivation of silicon surface by O_2, the passivation layer removal and the etching of silicon - happen simultaneously. Therefore, the silicon etch by SF_6 is isotropic. In a high-aspect-ratio structural etch, a relatively high dc bias on the sample chunk is necessary to completely remove the SiO_x passivation layer, especially from the bottom of the structure.

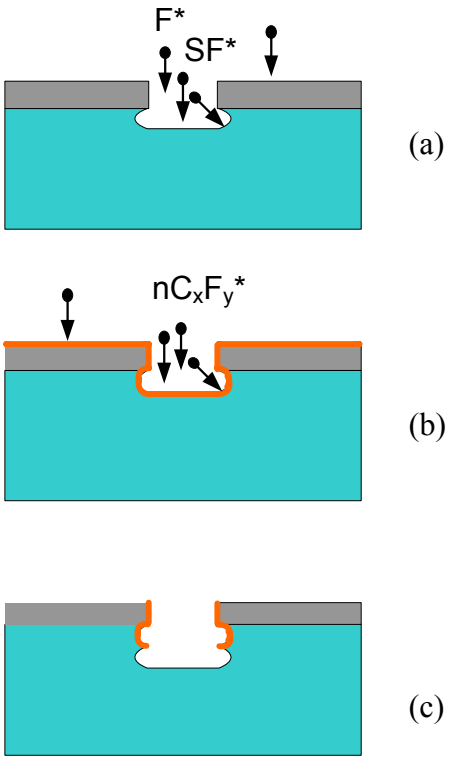


Figure 2-12. Alternate etching and passivation in Bosch process. (a) Etch step. (b) Passivation step. (c) The next etch step.

In order to achieve the anisotropic silicon etch, sidewall passivation of the etched structure must be performed to protect the sidewall from being etched in the etching cycle. C_4F_8 is used in STS ASE process as the passivating chemical. It is dissociated in the plasma and forms ions and radical species. These species undergo polymerization reactions and result in the deposition of a polymeric layer consisting of $n(-C_4-F_2-)$ molecular chains. This polymer layer is deposited uniformly on the surface of mask, sidewall of the etched structures and the bottom of the etched trenches. In the following etching cycle, aided by the ion bombardment, radicals dissociated from SF_6 preferentially remove the surface passivation layer, leaving the polymer on the sidewall of the etched structures unetched. The anisotropic silicon can be achieved by alternately performing the SF_6 etch and C_4F_8 passivation continuously. As a result of the periodic etching and passivation, scallops on the sidewall of etched structures are observed, as shown in Figure 2-13.

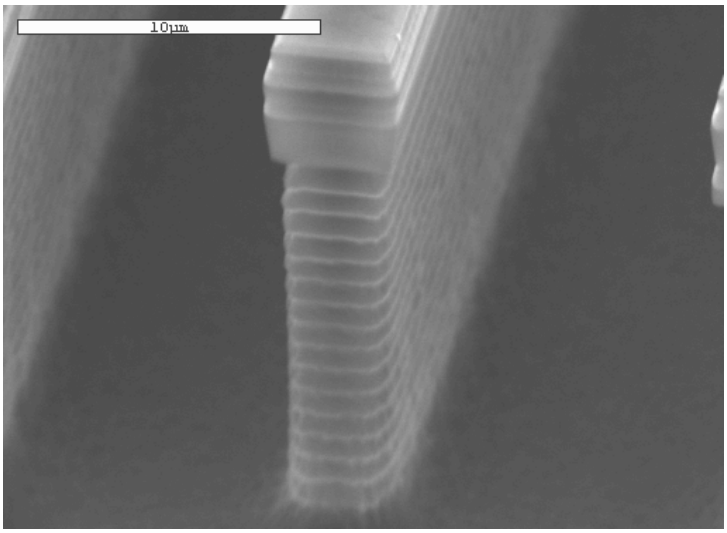


Figure 2-13. Scallops formed on the sidewall of the etched structures showing the alternate etching and passivation cycles in Bosch process.

By adjusting the etching and passivation duration and their ratio, different scallop depth and spacing can be achieved. More directional etch and smoother sidewall can be obtained at the expense of smaller etch rate and longer process time duration.

2.3.3 Silicon DRIE Characterization

Due to the alternate etching and passivation cycles, more input parameters are involved in the silicon DRIE than in a traditional RIE system. While the common multiple input parameters of DRIE have the similar effects on the etching outputs as in RIE, as shown in Figure 2-4, great attention should be paid to some other variables specifically existing in an ASE system. For example, the time duration and the ratio of etching and passivation cycles play important roles in the etching rate tuning and profile control. In order to control the silicon anisotropic etch more effectively, after some optimal experiments on the input parameters, we fixed most input parameters, only leaving the etching/passivation ratio and platen dc bias tunable for the etch of different structures. The basic silicon ASE recipe is shown in Table 2-4.

Table 2-4. Input parameters in the silicon ASE on STS ICP DRIE system.

Parameters	Settings
Coil power	600W
Platen power	Tunable
Etching pressure	40 mT (APC position: 84%)
Passivation pressure	~20~25 mT
SF_6 flow	130 sccm
O_2 flow	30 sccm
C_4F_8 flow	85 sccm
Etching time/cycle	Varies
Passivation time/cycle	Varies

In the backside etch in the developed DRIE CMOS MEMS technology, the main concern is the surface and thickness uniformity in the etched cavity on the backside. In an open area as large as 2 mm by 2 mm, the intra-die thickness uniformity can be controlled

within 2.5% and the surface roughness is less than 0.2μm [92]. This satisfies the thickness uniformity requirement for the accelerometers developed in this thesis work.

2.3.3.1 Etch rate and profile tuning

With other process parameters fixed, the etching rate can also be tuned by etch-passivation duration and their ratio. The duration of the etch period determines the general etch rate, and the passivation duration controls the lateral etch on the sidewall of the structure. Figure 2-14 shows the etching rate as the function of the time duration of the etching cycle. Other system parameters are fixed as in Table 2-4.

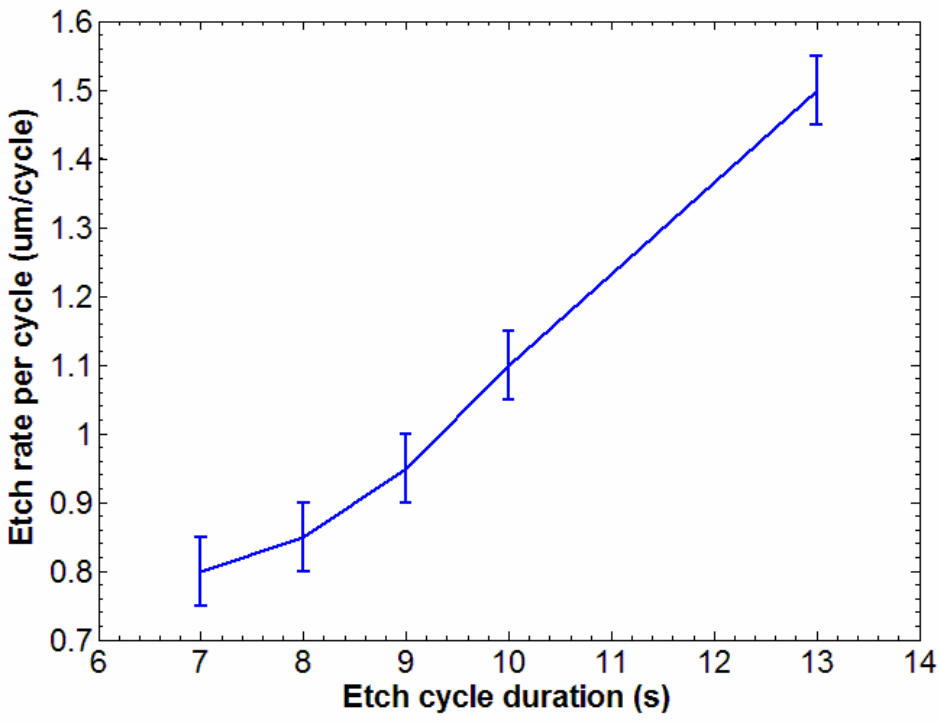


Figure 2-14. Etch rate per cycle using the recipe in Table 2-4 with varying etch duration.

By reducing the etch time and balancing the passivation duration, very small scallops can be achieved and consequently smooth sidewall can be obtained. Figure 2-15 shows a side view of a test structure. Smooth sidewall with scallops of 189nm in depth

and 620nm in spacing has been achieved. These achievements are similar to the typical results reported [96]. They are achieved with a lower etching rate of 2.5 μm/min.

In the process, we tune the etch cycle duration from 7.0 seconds to 13.0 seconds according to the requirement of different etching rate and sidewall profile. For microstructures in the accelerometers, a maximum etching rate of 4.5μm/min can be used with an etch/passivation ratio of 13/7 under the other conditions listed in Table 2-4.

The tuning of the platen dc bias also influences the etching rate by changing the momentum of the impinging ions, which is extremely useful in the etch of structures with high aspect ratio. For deeper trenches, in addition to the above methods, the etching rate can be increased further by increasing the gas flow rate of SF_6.

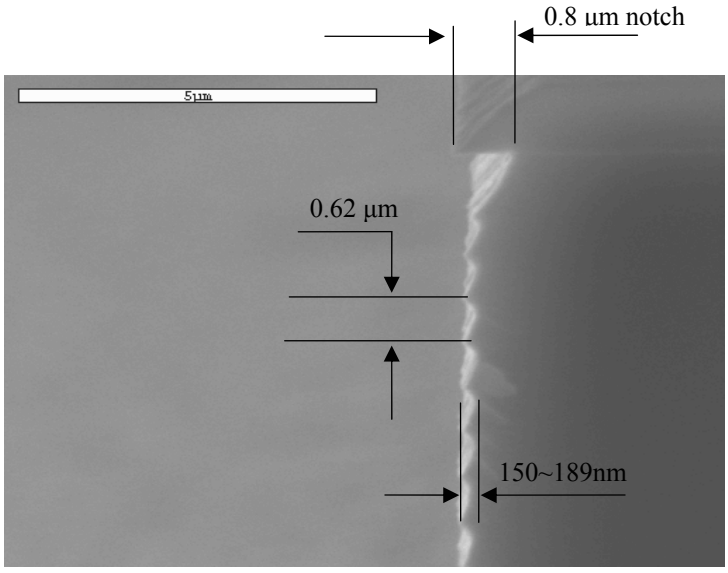


Figure 2-15. Smooth sidewall in Si DRIE achieved with a lower etch rate.

Obviously, by changing the etch/passivation time ratio, the sidewall profile can be tuned. Higher etch/passivation ratio turns out a more negative trench angle; while lower ratio produces a positive one. Figure 2-16 shows schematically the trends of the sidewall

angle evolution; and photographs of the actual comb fingers after the release etch with different etch/passivation ratios. The tuning effect is obvious. In the fabricated CMOS-MEMS accelerometers in this thesis work, the gap between the 4.5 μm-wide comb fingers is 2.1 μm. The aspect ratio of the gap trench ranges from 20 to 25 with the thickness of the structure being 40 ~ 50 μm. A nearly 90° profile angle can be obtained by tuning the etch/passivation ratio between 9/5 to 10/5. Figure 2-17 shows the sidewall profiles of test structures and the finished comb fingers. The SEM pictures of the test structures were taken after 15 cycles of etching and passivation, as show in Figure 2-16(a). The thickness of the etched comb finger in Figure 2-17(b) is approximately 45 μm. The undercut on each side of the finger sidewall is less than 0.4 μm.

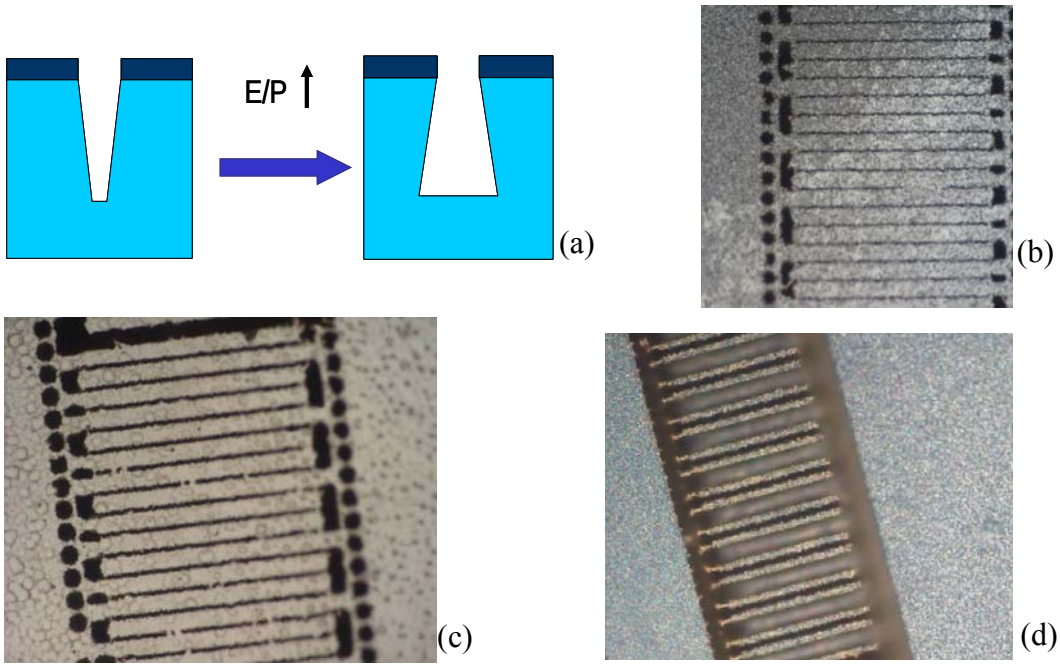
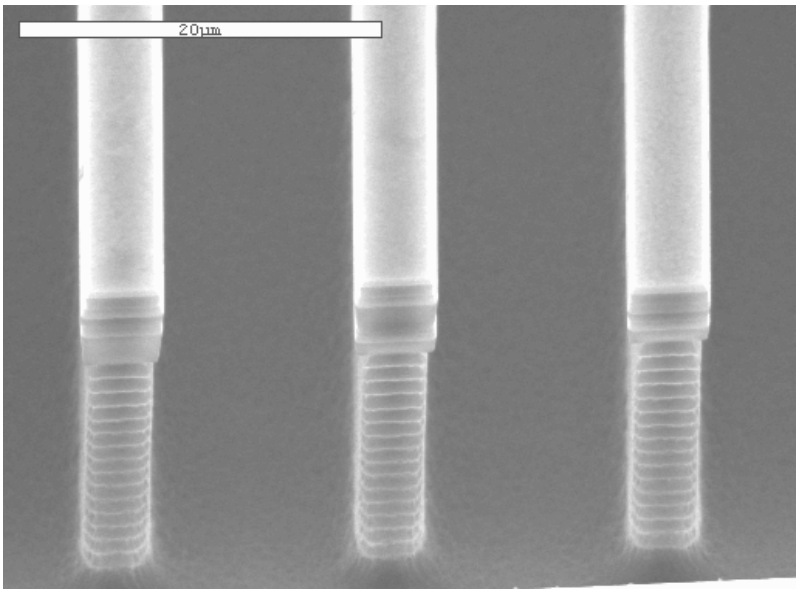
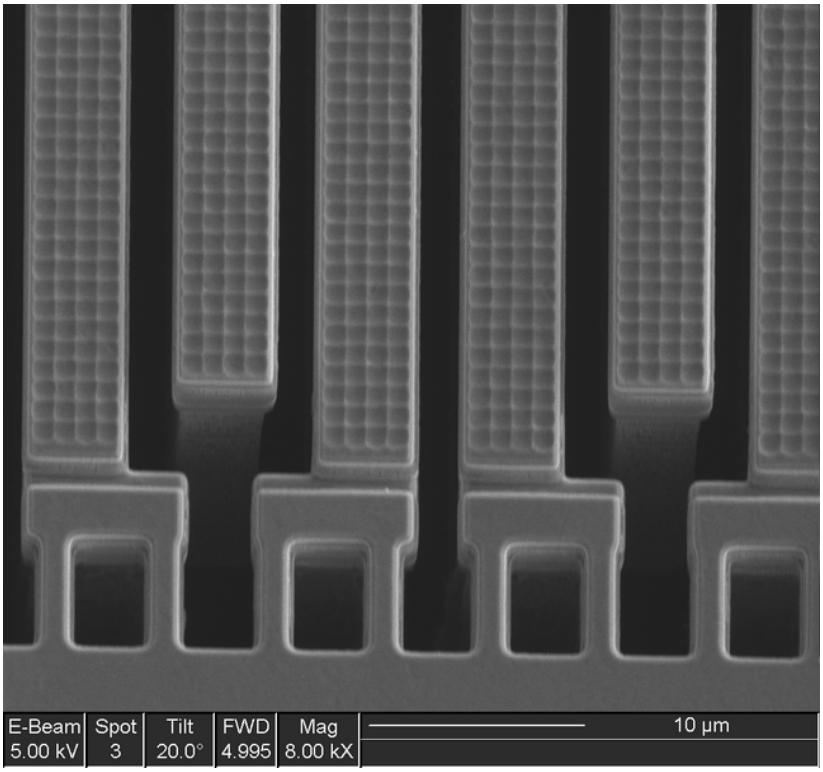


Figure 2-16. The tuning of etch profile by changing the etch/passivation ratio. (a) Schematic tuning effect. (b) image of the comb fingers after the release etch with 7:5 E/P ratio, (c) after the release etch with 8:5 E/P ratio, (d) after the release etch with 13:7 E/P ratio.



(a)



(b)

Figure 2-17. Sidewall profiles of the comb fingers. (a) test comb fingers after 15 cycles of etching, (b) the actual comb fingers after device release.

2.3.3.2 Microloading and ARDE effect

As mentioned previously, the geometry-dependent effects in the ASE mainly include macroloading effect, microloading effect and aspect ratio dependent etch (ARDE). Macroloading effect is characterized by the faster etching rates on the largest open area. It is also observed that in the whole wafer etching, the patterns on the wafer edge experience larger etching rate than the same patterns at the center of the wafer. Apparently this macroloading effect, or called isotropic loading effect, is ascribed to diffusion-limited chemical reactions in confined spaces [97].

For a through-wafer etch of a 500μm thick silicon wafer with same patterns uniformly distributed through the whole wafer, after hours of etch, the difference of the depth of the etched patterns can be as high as tens of microns. This implies that extra measurements should be taken to prevent the effects caused by the over-etch on the fast-etched patterns. For through-wafer etch without carrier wafer, large features on the wafer edge are etched through first, causing helium gas, which is used to maintain the substrate temperature in the plasma etch, to leak through these features to the chamber and cause the system to shut down. Therefore, this macroloading effect is one of the main obstacle in achieving the wafer level fabrication and package for MEMS devices. In the silicon ASE in this work, chips of MEMS devices are glued on a 4 inch silicon carrier wafer. To avoid the macroloading effect, chips are distributed symmetrically in the center area of the carrier wafer. The rest area of the carrier wafer is covered by photoresist or Kapton® tape which demonstrates good thermal and chemical stability. With very small open area of silicon on the chips, this approach can reduce the depletion of the reactive radicals in

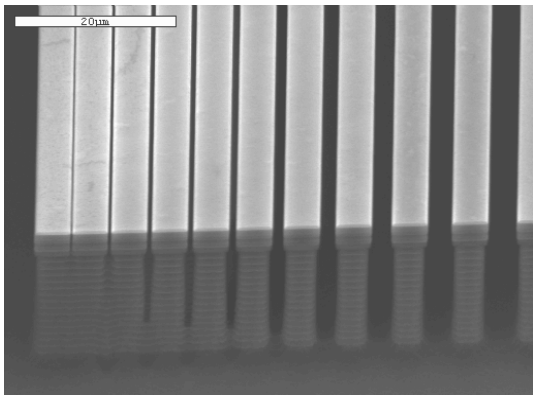
the sheath region, resulting a relatively uniform etch in the center area where device are attached.

Microloading effect and ARDE are more related to both RIE and DRIE of smaller patterns. In general, they refer to the phenomenon that the etching rate scales not only to the absolute feature size, but also to the aspect ratio of the structure being etched. Sometimes they are used in ambiguous ways since in both of them the etching rate is a function of the mask geometry. Although they are based on some similar physical and chemical principles in terms of affecting the etching rate and trench profile in different geometrical structures, they differ from each other subtly [98].

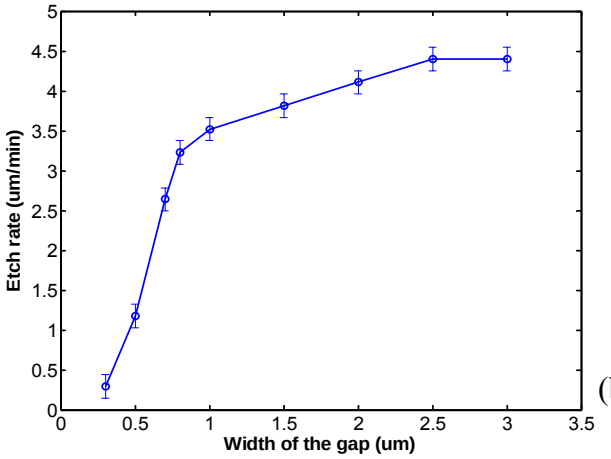
Microloading effect is related to the lower etching rate that occurs on high pattern density regions, which is mainly due to the local depletion of etchant as a result of excessive load of the etching surface. It can be considered as a micro scale isotropic loading effect that applies to both anisotropic and isotropic etches. This means that similar features close together etch slower than a single isolated feature of the same size. Meanwhile, this also means that when considering uniformly distributed features, big features etch slower than small ones, due to the higher local density of the exposed surface thus less supply of etchant. Elaborately designed experiments have been conducted to detail the effects of microloading effect on the etching rate for different pattern shape and pattern density [99]. In practice, microloading effect is often considered together with the ARDE effect in the MEMS device pattern design.

The ARDE effect is the most problematic effect in the fabrication of MEMS devices with fine mechanical structures. Thus, it is one of the most important parameters in MEMS design rules. In this effect, the etching rate is purely dependent geometrically

on the aspect ratio of the trenches or holes being etched. Moreover, not only does it affect silicon etching rate in DRIE, but also causes specific sidewall profile defects like bowing, bottling and microtrenching [98]. Figure 2-18(a) shows the SEM photography of the etched trenches on a test structure. The width of the trenches varies from 0.3μm to 30μm. The experiment was carried out using the same etching recipe as in the actual device fabrication. Top metal layer of the CMOS composite layers acts as the mask in silicon ASE. The plot in Figure 2-18(b) shows the silicon etching rate as the function of the trench width. The sharp slope indicates the higher the aspect ratio, the lower the etch rate. If the trench is too narrow, the etch process even can not proceed.



(a)



(b)

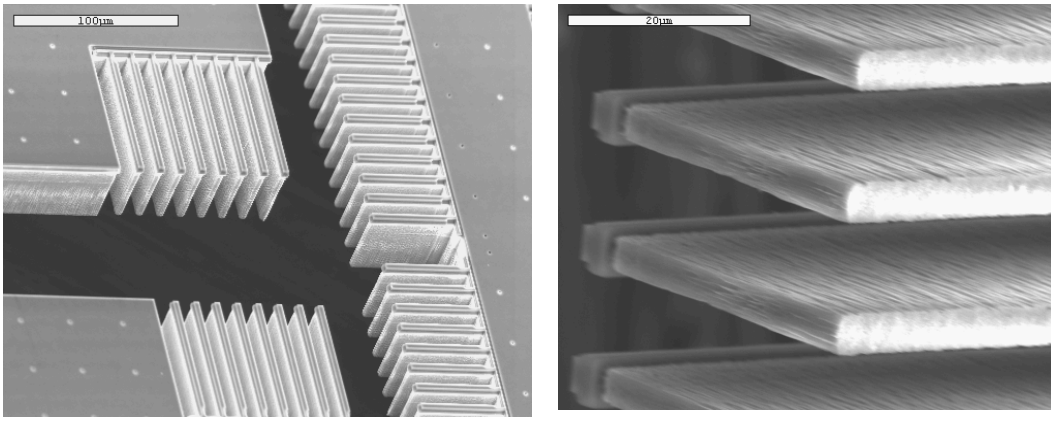
Figure 2-18. ARDE effect and its influence on the trench profile and etching rate. (a) Sidewall profile of trenches with various gaps. (b) etch rate as a function of gap width.

A large quantity of research works show that the ARDE effect is ascribed to a variety of mechanisms in RIE and DRIE. These mechanisms include ion shadowing, differential charging, neutral shadowing, and Knedsen transport of neutrals in which the diffusion of the neutrals is limited by the geometry [100-102]. To describe these mechanisms in a simpler way, the conductance of the trench is reduced by the high aspect ratio, impeding both the transport of the etching species to the bottom of the trench, and the removal of the etching by-product from the trench. Moreover, the induced charges on the extruding mask at the trench entrance will also shield the etch-aiding ions from entering and arriving the bottom of the trench.

Microloading and ARDE effect play extremely important roles in MEMS design rules. They directly determine the maximum thickness the MEMS device can achieve once the smallest feature of the device is set. Or, in other words, for a MEMS device with certain thickness, there exists the limit of the minimum feature size. In capacitive accelerometers, high sensitivity can be achieved by either reducing the gap between the sensing comb fingers, or increasing the structure thickness which consequently increase the proof mass. These two approaches are all limited by the ARDE effect that is intrinsically determined by the configuration of the ASE system. In practice, the ARDE effect can be reduced by lowering the chamber pressure. Lower pressure is also helpful in reducing the bowing effect and the etching notch which happens to the trench sidewall just underneath the mask. However, lower pressure means the longer MFP and higher kinetic energy of the ions which is the main cause of the rough surface [103]. The thermal effect caused by the bombardment of high-energy ions can result in over etch on

fine structures in the lateral direction, especially when the structure is suspended. This thermal effect will be discussed in Chapter 5.

In the accelerometer design, the gap between the comb fingers should be carefully chosen based on the ARDE characteristics of the available system for silicon DRIE. According to the sidewall profile of the test comb fingers the ICP DRIE etcher can accomplish, as shown in Figure 2-18, we choose the gap of the comb finger as 2.1μm to avoid the apparent bowing and other ARDE caused sidewall deterioration. For comb fingers of 50μm thick, the final gap of 2.1μm can be achieved with 90±1° sidewall, as shown in Figure 2-19 where only stator comb drives are shown.



(a) (b)

Figure 2-19. Etching profile of the sensing comb fingers. (a) Stator comb drives after the device is released. (b) Backside closed-up view of the comb fingers.

2.5 Summary

In this chapter, basic plasma etch technologies are introduced with exemplified PlasmaTherm SLR770 ECR and STS ICP ASE system. Some physical and chemical effects in the plasma etches, which are critical to the MEMS device design and fabrication, are also addressed with experimental results. The design rules for CMOS-

MEMS accelerometers with structure thickness of 50 μm are extracted, which are tabulated in Table 2-5.

Table 2-5. CMOS-MEMS accelerometer design rules extracted from the experimental results

Structural/process Parameters	**Design rules**
Highest aspect ratio	30
Comb finger gap	≥ 2.0 μm
Undercut on suspended structures	0.2~0.3 μm
Width of dummy pattern for ARDE reduction	3.0 μm
Selectivity in SiO_2 etch (SiO_2/Si)	3.0~4.0
Selectivity in SiO_2 etch (SiO_2/Al)	≥ 50.0
Selectivity in Si DRIE (Si/SiO_2)	≥ 150
Selectivity in Si DRIE (Si/Al)	500~600

CHAPTER 3
IMPROVED DRIE POST-CMOS MEMS TECHNOLOGY

This chapter details the new DRIE post-CMOS MEMS process developed for the fabrication of CMOS-MEMS integrated accelerometers. As a technological background, the previous plasma etch based post-CMOS MEMS approaches, including the thin-film and DRIE approaches, are introduced first. As a practice, a single-axis accelerometer and a thermally-actuated micromirror were fabricated using the previous DRIE post-CMOS technology. When used in the fabrication of capacitive accelerometers, the critical drawback of the previous DRIE CMOS-MEMS process (compared to the improved process developed in this thesis work) is the simultaneous undercut of the whole structure when the undercut on isolation beams are performed. This universal undercut enlarges the comb finger gap and thins the mechanical springs, lowering both the electrical and mechanical performance of the accelerometers. It is concluded that although the previous DRIE process is effective in the fabrication of thermal micromirrors where the feature sizes are as large as 10μm, it is not a good choice in the micromachining of MEMS devices with much smaller features.

The new DRIE post-CMOS MEMS process was developed to overcome the shortcomings of the previous technology. It is specifically designed for the fabrication of capacitive inertial MEMS sensors where the sensing and driving comb fingers are required to be electrically isolated from each other and from the substrate. Using the new process, the electrical isolation structures and the functional MEMS structures can be processed independently, allowing separate control of the fabrication parameters.

3.1 Dry Post-CMOS MEMS: Background

There are two types of dry post-CMOS MEMS technologies: thin-film surface micromachining technology and DRIE bulk micromachining technology. Both of them are CMOS-compatible because the CMOS circuitry can be completely protected by the top metal layer during the post-CMOS micromachining, which consists of dielectric and silicon plasma etches. Meanwhile, the MEMS structures are defined by the pattern of the top metal layer, which acts as a mask in the dry etch steps. Therefore, both approaches are maskless, and no photolithography is needed for front side process. This greatly simplifies the micromachining and makes the prototyping development cycle much shorter. In addition to the convenience of the fabrication, the multiple interconnect metal layers make the wiring of MEMS structures and integrated circuits very flexible. The fully-integrated metal wiring also helps in reducing the parasitics, allowing high overall device performance.

3.1.1 Thin-film Post-CMOS MEMS Technology [32]

The process flow of thin-film CMOS-MEMS process with 4 metal layers is shown in Figure 3-1.

The CMOS circuit region is designed to be covered by the top metal layer. MEMS structures are pre-defined by the top metal layer or the other interconnect metal layers. Figure 3-1(a) shows the cross-section of the original chip after CMOS foundry fabrication, with a passivation layer on top. Two processing steps are performed only on the front side of the chip. First, the pre-defined MEMS structure is exposed by etching the SiO_2 stack between the interconnect layers, as shown in Figure 3-1(b). This is done by an anisotropic SiO_2 plasma etch using an ECR RIE system with CHF_3/O_2 gases, as detailed in Section 2.2. Next, a silicon DRIE is performed using an ASE technology,

followed by an isotropic silicon etch, which releases the MEMS structures by undercutting the silicon beneath the MEMS structures. The depth of the anisotropic etch into silicon controls the gap between the released structure and the silicon substrate. This gap should be large enough to eliminate the parasitic capacitance between the MEMS structures and the silicon substrate. In practice, it is normally on the order of 30μm [104].

A lateral accelerometer with 1 $mg/\sqrt{Hz}$ noise floor exemplifies the types of MEMS devices fabricated using this technology [34, 84, 105]. This simple fabrication process yields much smaller parasitic effects as compared to the MUMPs polysilicon process, and it provides flexible wiring by using the multiple metal layers. However, there are some drawbacks in this technology, which limit the performance of the fabricated accelerometer.

First, there is large vertical curling of the suspended MEMS structure caused by the residual stress gradient existing in the composite SiO_2/Al layers, as shown in the example device in Figure 1-1. For both in-plane and out-of-plane sensing or actuation, this large vertical curling will result in the reduction or complete loss of the engagement between comb fingers or other capacitive MEMS structures. Additionally, due to different thermal expansion coefficients (TEC) of Al and SiO_2, the curled MEMS devices exhibit a strong temperature dependence, which limits their utility. Although particular compensation technology was employed to reduce the structure mismatch by using a specially designed frame, the device fabricated using this thin film process still has a stringent size limit [106, 107].

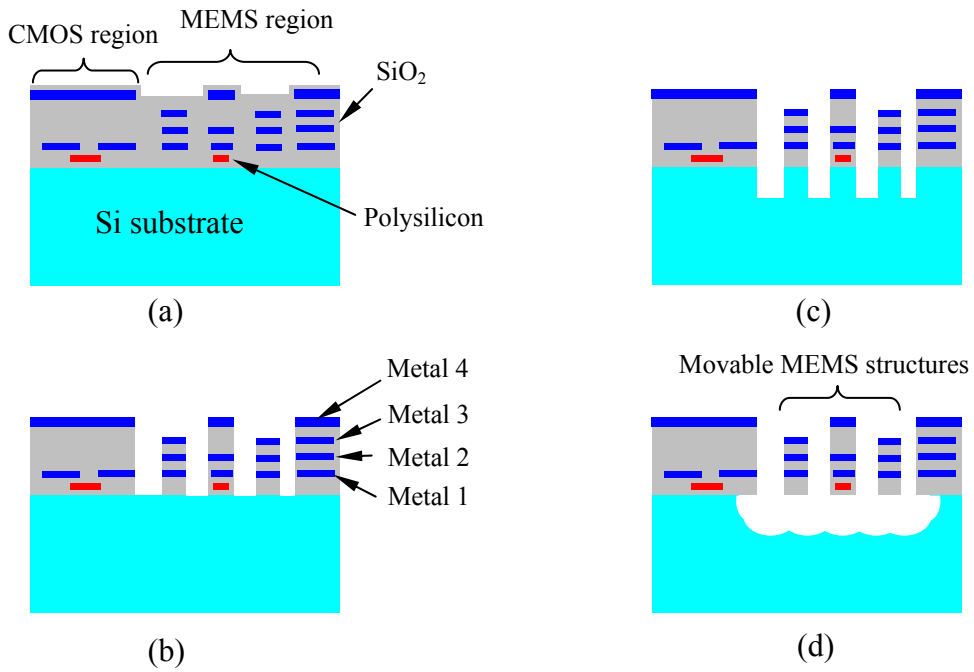


Figure 3-1. Cross-sectional view of the thin-film CMOS-MEMS process. (a) Before the micromachining. CMOS region is shielded by top metal layer. (b) SiO_2 anisotropic etch. (c) Anisotropic of Si (DRIE). (d) Isotropic etch of Si for structure release.

Second, for inertial sensors fabricated using this technology, the requirement of release holes on the proof mass reduces the mass of the proof mass, resulting in a lower mechanical sensitivity of the sensors. To achieve a capacitance change large enough for the conditioning circuit to detect, the dimension of the accelerometer may need to be considerably large, which is in conflict with the dimension limit by the structure curling.

Third, in-plane curling of the thin film structures due to fabrication variations also limits the maximum size of the device. Although there are some specific processes designed for low residual stress thin films [108], normally CMOS foundries have very few, if any, considerations to meet the particular requirements for MEMS devices. The curling of the MEMS structures can only be compensated to a limited degree by proper

design of both the MEMS and compensating structures. In addition to the collection of technological data directly from the employed CMOS foundries, systematic post-CMOS process calibration must be conducted to characterize the process variations and their effect on the MEMS devices.

Lastly, since the last release step is an isotropic etch, it undercuts the silicon close to the circuit and structure anchors. The ratio of the vertical and lateral etching rate is approximately 2:1 [109]. To protect the silicon underneath the circuit region from being etched away during the structure release, the CMOS circuitry must be placed far away from the microstructures, especially when a large separation between the microstructures and substrate is needed. As a result, significant chip area is wasted due to the protection margin around the MEMS structures. Since the silicon underneath the mechanical anchors of the MEMS structures is also etched away, the suspension of the mechanical structures is softened, which results in a lower mechanical performance and less robustness of the device.

3.1.2 DRIE Post-CMOS MEMS Technology [33]

To overcome the drawbacks of the above thin-film post-CMOS MEMS process, DRIE post-CMOS MEMS technology was developed to incorporate bulk, single-crystal silicon (SCS) into the MEMS structures. By taking advantage of the ASE technology, high aspect ratio CMOS-MEMS structures have been demonstrated.

The maximum aspect-ratio a DRIE system can achieve is an important factor in the MEMS structure design. It determines the dimensional limit of the structures fabricated using that DRIE system. Once a lateral feature to be etched is fixed, the maximum thickness is uniquely defined. Similarly, for a structure with certain thickness, the smallest gap that can be created between adjacent structures is also uniquely defined.

The DRIE post-CMOS MEMS technology stems from the thin film technology described in last section. By taking advantage of both the flexible wiring with multiple metal layers in CMOS technology and the capability of high aspect ratio etching, DRIE CMOS-MEMS provides an approach to implement thick and flat MEMS structures with better mechanical performance and device robustness.

Figure 3-2 shows the process flow of the DRIE post-CMOS MEMS technology. The process starts with a backside silicon DRIE to define the MEMS structure thickness, as shown in Figure 3-2(a). As described above, the maximum thickness of this structure is limited by the smallest etching pattern on the front side of the MEMS structure and the maximum etch aspect-ratio. Next, as in the thin film process, an anisotropic SiO_2 etch is performed on the front side of the wafer (chip) to define the MEMS structures (Figure 3-2(b)). The following step differs from the thin film process in that an anisotropic DRIE, instead of isotropic Si etch, finalize the structure release by etching through the remaining SCS diaphragm, as shown in Figure 3-2(c). With SCS incorporated underneath the CMOS interconnect layers, large and flat MEMS structures can be obtained because the residual stresses in the SiO_2/Al thin-films are mitigated by the thick SCS, leading to very little out-of-plane curling. If necessary, an optional time-controlled isotropic silicon etch can be added to create compliant mechanical structures which only consist of CMOS thin films (Figure 3-2(d)). In the accelerometers developed in this thesis work, the fully-undercut CMOS thin-film layers are employed as the electrical isolation between the sensing fingers and silicon substrate.

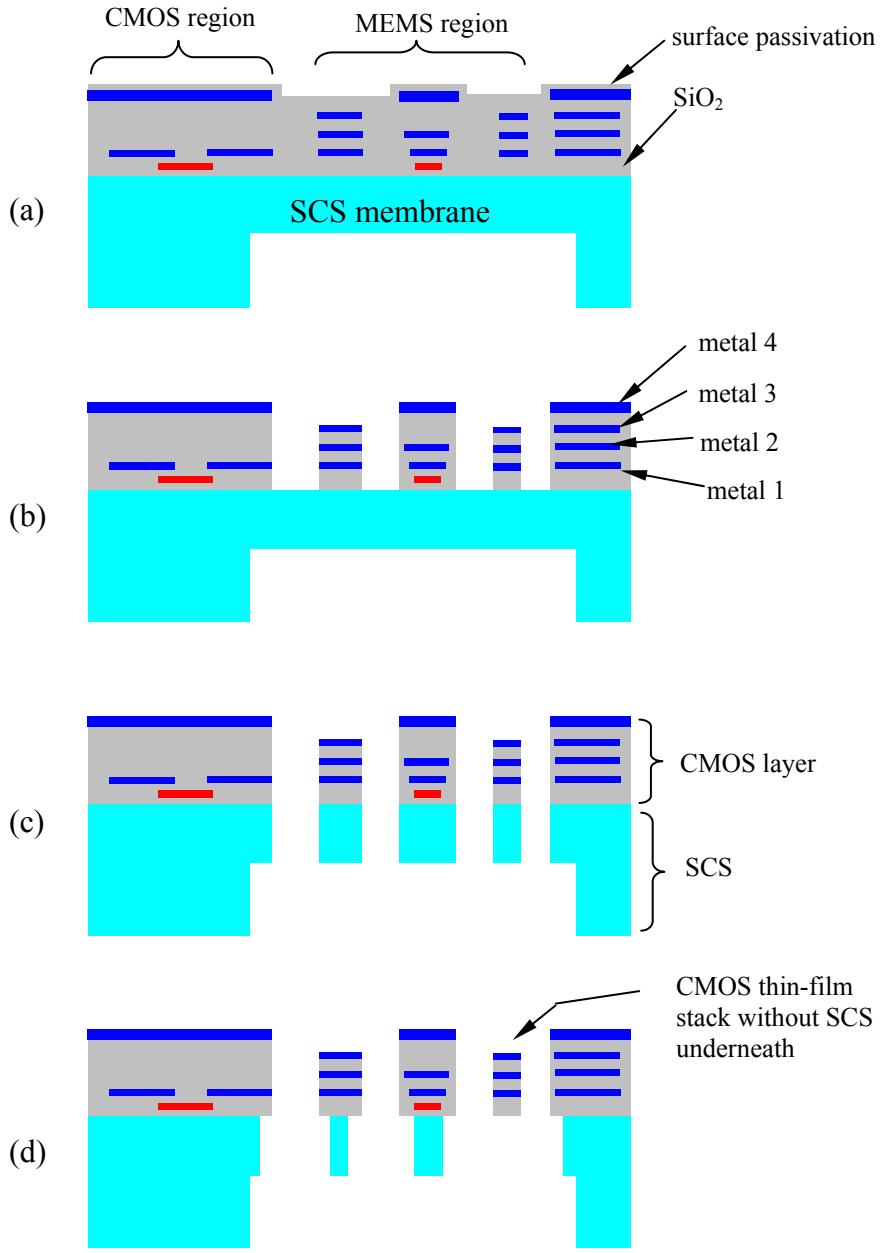


Figure 3-2. Cross-sectional view of the process flow of DRIE post-CMOS MEMS technology. (a) Backside silicon DRIE. (b) Anisotropic SiO_2 etch. (c) Silicon DRIE for structure release. (d) Optional silicon isotropic etch to create thin film structures.

It should be pointed out that in the backside DRIE step to define the thickness of the MEMS structures, double side alignment is required. However, since normally the remaining silicon for bulk MEMS structures is on the order of tens of microns, there is no apparent circuit performance degradation caused by the substrate thinning. Therefore, there is no strict requirement for alignment in the backside etch.

With the flat MEMS microstructures enabled by the DRIE CMOS MEMS technology introduced above, reliable sensing and actuation can be achieved. A lateral-axis angular rate gyroscope with a noise floor of $0.02°/s/\sqrt{Hz}$ has been fabricated using this technology [70]. In particular, this technology is very suitable for the fabrication of thermally actuated micromirrors where bimorphs are used to elevate the mirror plate. Several electrothermal micromirrors have been demonstrated using this technology [37, 110, 111].

3.1.2.1 Example device I: electrothermal micromirror

As a process practice and comparison, two MEMS devices were fabricated using the above mentioned DRIE post-MEMS technology: a micromirror and a lateral-axis accelerometer. In the first device, the fabricated electrothermal micromirror can provide large vertical displacement (LVD) by employing a tilting-angle compensation between the mirror plate and the actuating frame where the mirror plate is attached.

Figure 3-3 shows a fabricated electrothermal micromirror with LVD actuation in which the flat mirror with a large area allows high resolution, easy alignment and reliable scanning in an optical system [111]. In fabrication, when isotropic silicon etching is performed to remove the SCS underneath the bimorphs, the same amount of lateral

undercut simultaneously applies to both the mirror frame and mirror plate, as shown in the process flow of Figure 3-2(d). The undercut is shown in the inset of Figure 3-3.

For large structures such as the mirror plate with a dimension of 1mm by 1mm, the undercut is on the order of several microns, which has negligible effect on the structure integrity. However, for fine microstructures, this undercut could be disastrous! Thus, because of this simultaneous undercut, there will be a minimum structure size limit in MEMS device design if this DRIE post-CMOS MEMS technology is employed.

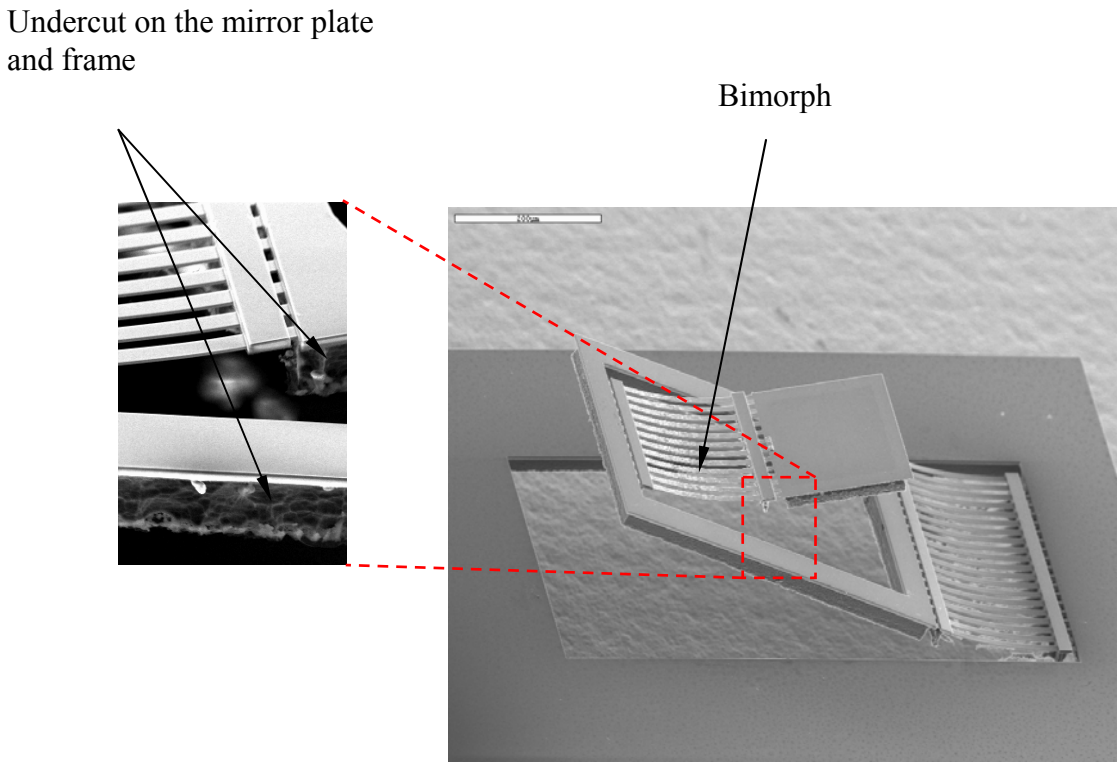


Figure 3-3. LVD electrothermal micromirror fabricated using DRIE post-CMOS MEMS technology. The inset shows the undercut on the mirror plate and actuation frame, which is caused by the undercut of bimorphs.

3.1.2.2 Example device II: single axis accelerometer

The second device fabricated using the previous DRIE CMOS-MEMS technology is a single-axis accelerometer. Without densely distributed release holes, large proof masses have been realized for better overall performance. The drawback of this process is revealed by the accelerometer fabrication, in which severe problems caused by the simultaneous undercut have been observed.

Figure 3-4(a) shows the lateral accelerometer fabricated using the previous DRIE post-CMOS MEMS technology. The CMOS technology used was the AMI Semiconductor (AMIS) 0.5μm process. The electrical isolation between the silicon underneath the sensing fingers and the bulk silicon substrate was realized by a CMOS interconnect stack of 2.4μm width, as shown in Figure 3-4(b). The designed critical dimensions of the fabricated accelerometer are tabulated in Table 3-1.

Table 3-1. Dimensions of the microstructures in the test accelerometer

Structures	**Dimension (μm)**
Overlapped sensing finger length (L)	100.0
Sensing finger width (w)	4.0
Gap between sensing fingers (g)	2.4
Width of the isolation beam (w_i)	2.4
Length of the isolation beam (L_i)	4.0
Width of the spring (w_s)	3.2
Length of the spring (single fold)	240.0
Thickness of the structure (t)	50.0

When the isotropic etch was performed to undercut the SCS underneath the isolation beam, at least 1.2 μm on each side should be etched to completely remove the SCS. This amount of undercut took place on the sensing fingers and the mechanical springs at the same time, resulting in an enlarged gap between the comb drives. As a result, compared with the actual dimensions in Table 3-1, the capacitance formed

between a rotor finger and stator finger is reduced by half according to the following equation,

$$C = \frac{\varepsilon_0 L h}{g} \qquad (3.1)$$

where ε_0 is the dielectric constant of the air and other parameters are defined in Table 3-1. This reduction of the sensing capacitance caused a lower sensitivity of the accelerometer. The impendence at the input node of the circuit will increase.

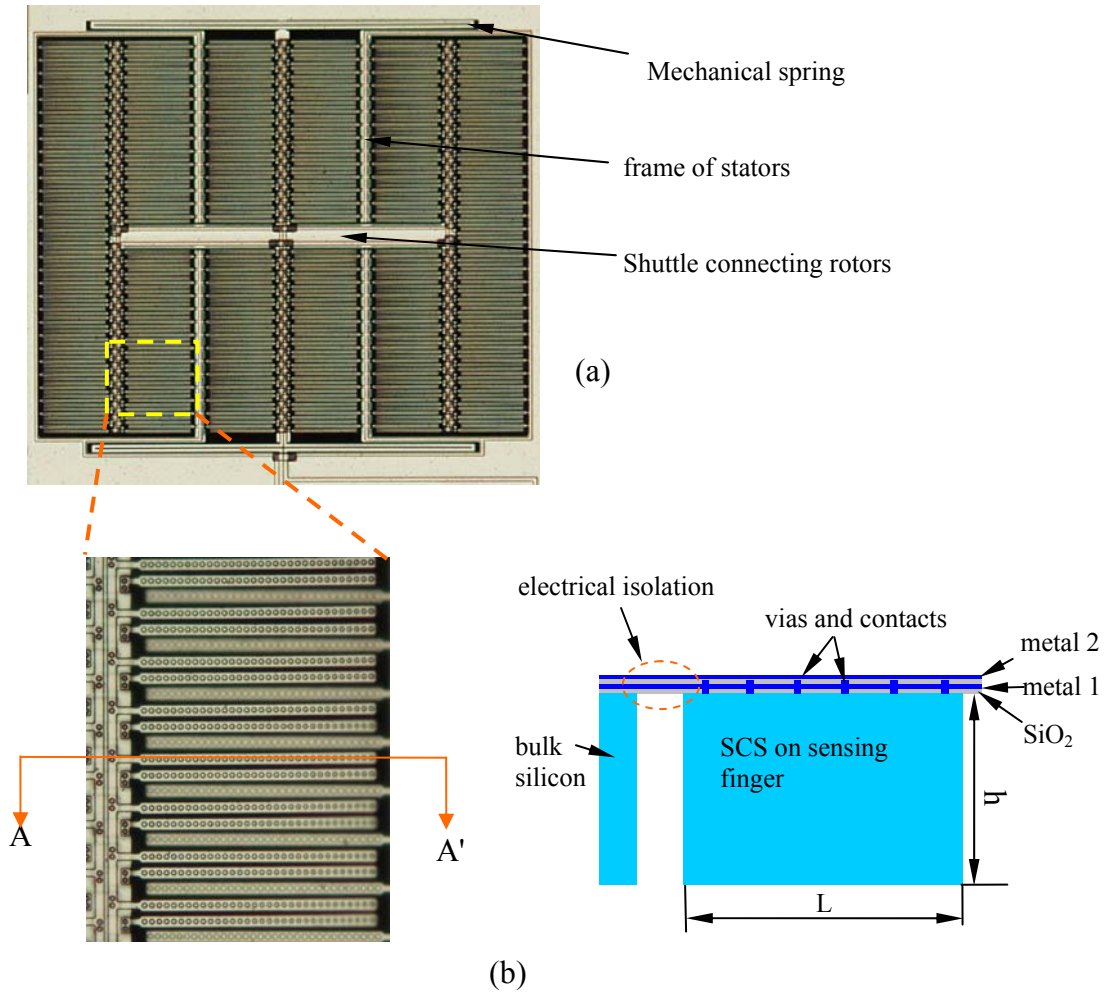


Figure 3-4. Fabricated lateral accelerometer using previous DRIE CMOS MEMS process. (a) Topology of the device. (b) Top view of the enlarged sensing fingers and the illustrated cross-sectional view of the sensing finger seen from A-A'.

Additionally, the mechanical performance of the accelerometer will also be affected dramatically by the silicon undercut on the mechanical springs. The spring constant of one turn clamped spring in the response direction is given by [112]

$$k_y = Eh(\frac{w_s}{L_s})^3 \qquad (3.2)$$

where E is the Young's modulus of SCS. By undercutting 1.2 μm on each side of SCS spring, the actual spring width will reduce to 0.8 μm, which is only 1/3 of its original design value. According to Equation 3-2, the spring of the accelerometer will be softened to only 3.7% of the designed value.

3.2 Improved DRIE post-CMOS MEMS Technology

As can be seen from last section, the anisotropic etch of the last step in Figure 3-3 has a significant impact on both electrical and mechanical performance of MEMS device. For the fabrication of MEMS devices in which capacitive sensing and actuation is employed, the isotropic undercut for electrical isolation increases the minimum gap of comb fingers. It can even completely damage the mechanical structures if the etching time is not well controlled.

The main task of this thesis work is to develop a microfabrication process to overcome the drawbacks caused by the last isotropic etch in the previous DRIE CMOS MEMS process. To avoid the unwanted undercut on other MEMS structures, the electrical isolation etch should be performed independently to the structure release process. To realize this idea, we perform the isolation structure etch prior to the device release step. Another metal layer is used as the mask for the isolation structure etch.

The process flow of the new DRIE post-CMOS MEMS technology developed in this thesis work is shown in Figure 3-5. A CMOS-MEMS accelerometer is exemplified in

the fabrication. TSMC 0.35μm technology with 4 metal layers was used for CMOS foundry fabrication. The process starts with the backside etching to define the structure thickness (Figure 3-5(a)), which is same as the previous DRIE CMOS MEMS technology. Then, anisotropic SiO_2 etching is performed to expose the regions for electrical isolation of silicon only (Figure 3-5(b)). Note here top metal layer M4 covers all other regions on the device except for the isolation structure. An aluminum etch is then performed to remove the top metal layer M4 (Figure 3-5(c)). Next, a deep anisotropic silicon etch, followed by an isotropic silicon etch, is performed to undercut the silicon beneath the isolation beams (Figure 3-5(d)). These beams isolate the sensing fingers from the silicon substrate. Next, the second anisotropic SiO_2 etch is performed to open the patterns of comb fingers, mechanical springs and other structures (Figure 3-5(e)). In this step, M3 is used to protect circuit region. Finally, a deep silicon etch is performed again to etch through and release the accelerometer (Figure 3-5(f)).

For accelerometer fabrication, compared to the previous DRIE CMOS MEMS process shown in Figure 3-2, in which isolation beams and comb fingers were undercut by the isotropic silicon etch at the same time, the new process performs the etch steps for isolation and other structures separately. Therefore minimal undercut of comb fingers can be achieved, which will greatly increase the sense capacitance and device sensitivity. This is realized by simply sacrificing the top metal layer M4. It should be pointed out that this process can be further adapted for the fabrication of MEMS devices in which independent processes should be performed for different structures.

In this thesis work, two accelerometers have been designed and fabricated using the above improved DRIE CMOS MEMS technology. The device designs are detailed in

Chapter 4. In the 3-axis accelerometer, with a z-axis accelerometer embedded in the proof mass of a dual axis lateral accelerometer, small size and robust structures are achieved.

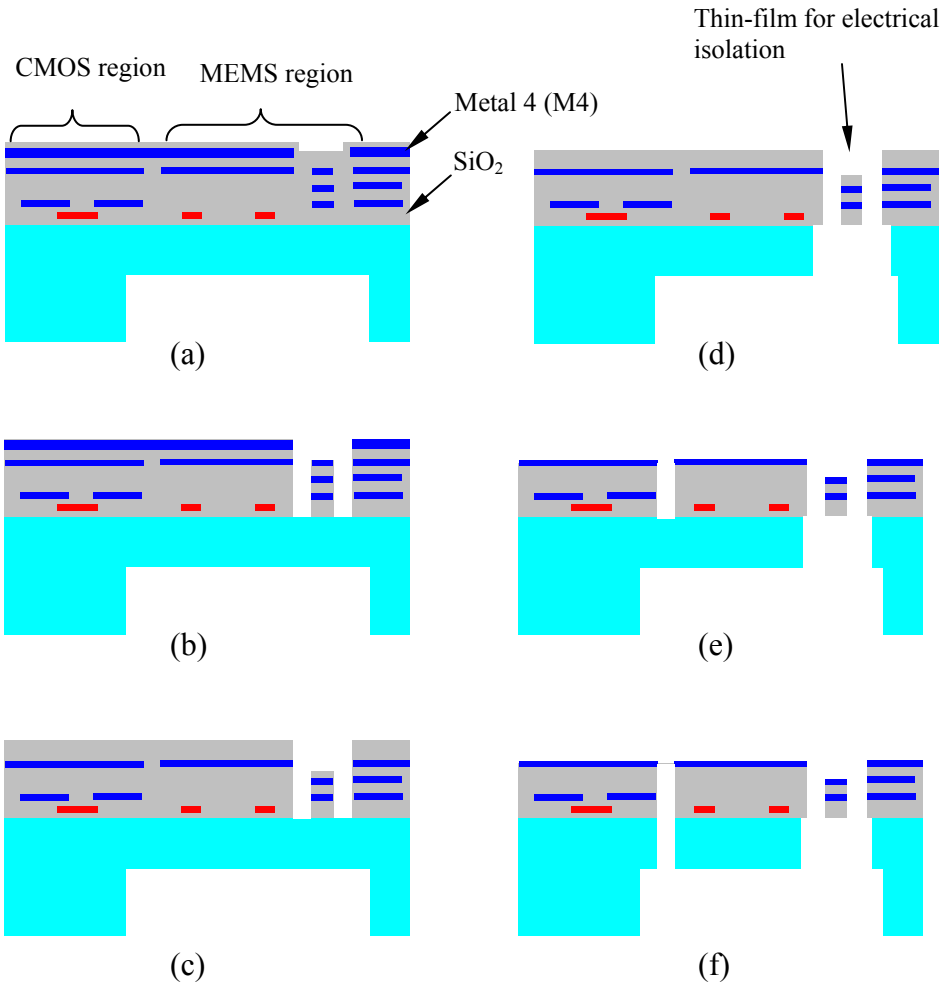


Figure 3-5. The improved process flow of new DRIE post CMOS MEMS technology. (a) Backside etch. (b) Anisotropic SiO_2 etch and deep Si etch followed by Si undercut. (c) Top Al etch. (d) Anisotropic SiO_2 etch followed by deep Si etch and Si undercut. (e) SiO_2 etch to open microstructure region. (f) DRIE to release the device.

3.3 Summary

In this chapter, thin-film and the previous DRIE post-CMOS MEMS technologies are introduced followed by two example MEMS devices showing the drawbacks and limitations of these two processes. A new DRIE CMOS-MEMS process is developed. It features the independent control of the etch steps for isolation thin films and other mechanical structures. It is particularly suitable for the fabrication of capacitive inertial sensors in which sensing and driving comb fingers are isolated from each other and from the silicon substrate. In general, the new process is applicable to other MEMS devices where independent processes are required for different functional structures.

CHAPTER 4
DESIGN OF THE INTEGRATED ACCELEROMETERS

Two CMOS MEMS devices have been developed to demonstrate the improved post-CMOS MEMS technology described in Chapter 3. These devices are a 3-axis and a single-axis CMOS MEMS accelerometer. For these capacitive inertial sensors, the improvements of the new DRIE post-CMOS MEMS technology allows comb drives with larger engaged area and smaller gap, enabling high sensitivities.

In this chapter, the performance goals for the devices are outlined first. Then, the mechanical and electrical designs of these devices are addressed in detail. The dimensions of the mechanical structures are determined according to the device performances, which are predicted based on simulation results. The CMOS technology used in this work is the Taiwan Semiconductor Manufacturing Company (TSMC) 0.35μm 4-metal, 2-poly CMOS technology. Low-power, low-noise, open-loop, capacitive amplifiers are used as interface circuits for the lateral and 3-axis accelerometers. The interface circuit design is a separate work and can be found in [113].

4.1 Applications of the Designed Devices

The features of the designed accelerometers are their small size and monolithic integration enabled by CMOS-MEMS technology. What is more important, the improved DRIE post-CMOS MEMS technology developed in this work allows thick and robust sensor structures by incorporating SCS in the mechanical structures. These are essential for the fabrication of high performance capacitive sensors.

Monolithic accelerometers with small size and 3-axis sensing capability are focused on human body motion sensing for applications in human activity/physiological monitoring, athletic/sports monitoring, and the motion-triggered functions in portable electronics. In these applications, the typical acceleration human can generate is less than 1.5 g [114, 115]. In sports, the highest acceleration an athlete can generate is less than 5g, and the muscle frequency is less than 200 Hz [116]. The minimum acceleration the human body generates in normal activities is on the order of tens of milli-g. If an accelerometer with a 3 g full sensing range and 200 Hz bandwidth is used to sense a 30 mg motion, from the following relation,

$$a_{\min} = \sqrt{\overline{a}_n^{\,2}} \cdot \sqrt{BW} \qquad (4.1)$$

where a_{min} is the resolution of the detection, a_n is the noise floor of the accelerometer and BW is the bandwidth, the noise floor required from the accelerometer is $2.12\, mg/\sqrt{Hz}$. This is a noise floor that even the second generation of commercial MEMS accelerometer can achieve. Therefore, the human physiological and physical activity monitoring only requires very low end of MEMS accelerometers.

Much higher performance can be achieved using the improved DRIE CMOS MEMS technology due to its capability of producing a sensing structure with a large proof mass. We are pushing the developed integrated CMOS MEMS accelerometers into higher end applications by targeting a noise floor of tens of $\mu g/\sqrt{Hz}$ with a bandwidth of a few hundred Hertz. With this improved performance, as tabulated in Table 4.1, the applications of the designed CMOS-MEMS accelerometers can be expanded to engineering monitoring, seismic monitoring, instrumentation and robotics. By optimizing the structural design, inertial navigation grade performance could be achievable.

Table 4.1. The major specifications of the designed single and 3-axis accelerometers

Parameters (unit)	Notation	Value
Power supply (V)	V_{dd}	3.3
Modulation signal (V)	V_m	1.5
Power consumption per axis (W)	P	1×10^{-3}
Full scale of acceleration sensing (g)		± 2
Bandwidth of the accelerometer (Hz)	BW	500
Overall sensitivity (mV/g)	S	200
Noise floor for z-axis ($\mu g/\sqrt{Hz}$)	N_z	200
Noise floor for lateral axes ($\mu g/\sqrt{Hz}$)	N_l	50
Dynamic range of z-axis (dB)		60
Dynamic range of lateral axes (dB)		70

4.2 Single-axis Lateral Accelerometer

In the single-axis accelerometer, the external acceleration is sensed by the vertically parallel electrodes attached to the proof mass, which is anchored to the silicon substrate through SCS springs. The springs suspending the proof mass are designed in such a way that they are primarily compliant in one in-plane direction. Compared to the accelerometer fabricated with the thin film CMOS-MEMS technology [57], the performance and the robustness of the proposed accelerometer are greatly improved by the virtue of the SCS incorporated on the proof mass and the sensing fingers and mechanical springs.

4.1.1 Device Design

The single-axis accelerometer can be simplified as the lumped model shown in Figure 4-1[112]. The governing equation of the system is [117]

$$m\frac{d^2x}{dt^2}+b\frac{dx}{dt}+kx=ma_{ext} \qquad (4.2)$$

which results in the transfer function of

$$H(s)=\frac{X(s)}{A(s)}=\frac{1}{s^2+\frac{b}{m}s+\frac{k}{m}}=\frac{1}{s^2+\frac{\omega}{Q}s+\omega^2} \qquad (4.3)$$

where b is the damping coefficient of the proof mass, ω is the resonant frequency and Q is the quality factor defined by $Q=\frac{m\omega}{b}$. For accelerometers working at a frequency lower than the system resonant frequency, the mechanical sensitivity can be expressed by dropping the first two terms in the denominator in Equation (4.3), which gives

$$\frac{x}{a_{in}}=\frac{1}{\omega^2}=\frac{m}{k} \qquad (4.4)$$

This is the mechanical sensitivity of the accelerometer. It is interesting to note that the mechanical sensitivity is inversely proportional to the square of the resonant frequency.

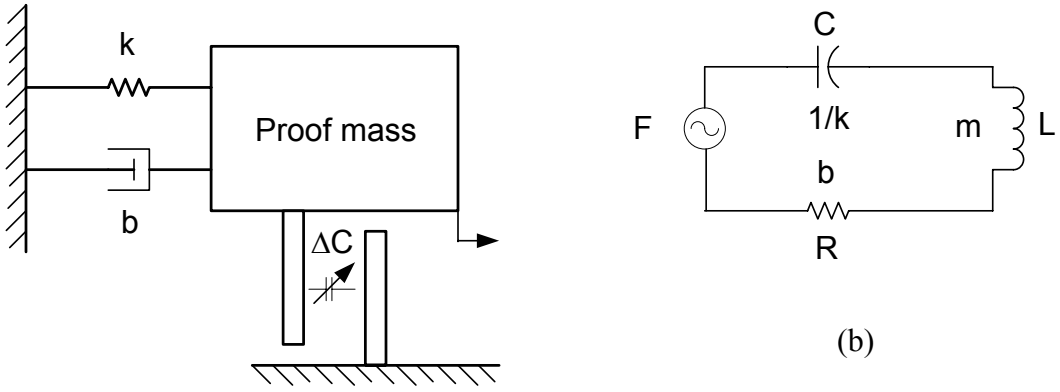


Figure 4-1. Lumped model and equivalent electrical circuit of the single axis capacitive accelerometer. (a) schematic model, (b) lumped circuit model.

A fully differential configuration of the capacitive sensing is employed to reject the common mode noise. The sensing bridge is formed by wiring the comb fingers in a common-centroid way, as shown in Figure 4-2. The sensitivity in electrical domain can be derived as

$$\frac{V_s}{a_{in}} = \frac{4C_s}{2C_s + C_p} \cdot \frac{V_m}{x_0} \cdot \frac{1}{\omega^2} \qquad (4.5)$$

where $V_s = V_{out+} - V_{out-}$ is the differential output of the capacitive sensing bridge, $\boldsymbol{x_0}$ is the original gap between the sensing comb fingers. C_s and C_p are the sensing capacitance and parasitic capacitance in the system respectively. In Figure 4-2, C_s=C_1=C_2=C_3=C_4, and C_p is the parasitic capacitance from the sensing node to the ground.

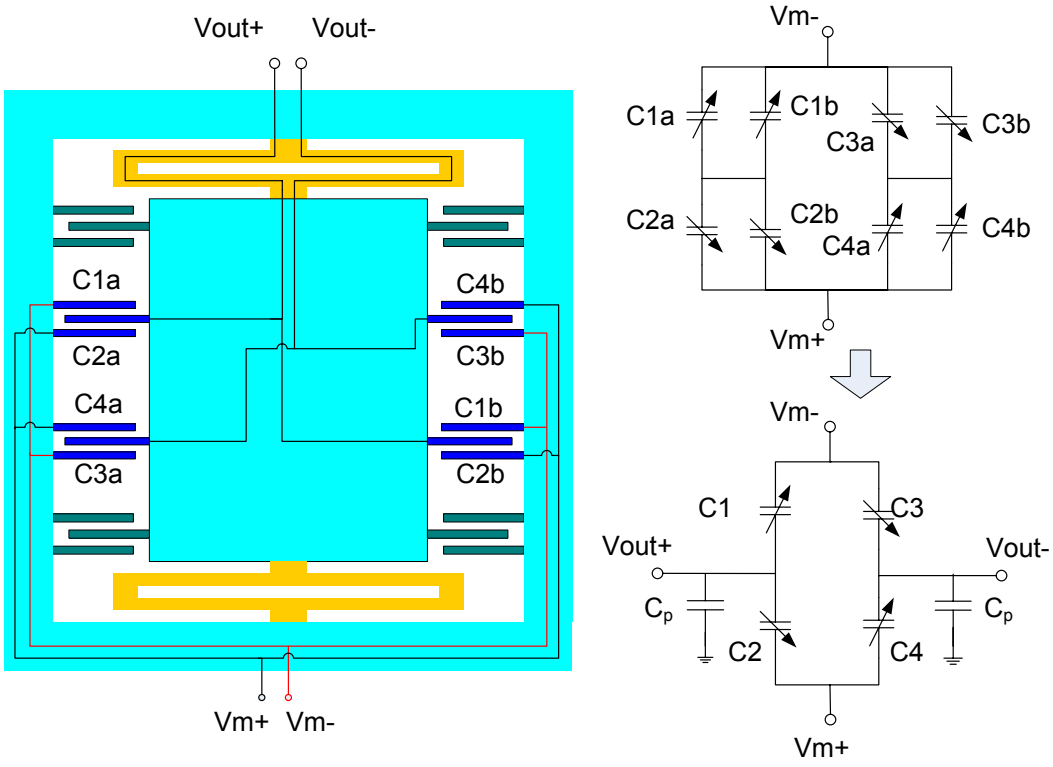


Figure 4-2. Fully differential configuration of the lateral accelerometer.

Figure 4-3 shows the schematic 3-D model of the single-axis accelerometer. The configurations of mechanical spring and the sensing comb fingers are also given. The 3-D model was created using CoventorWare [118], a commercial FEM simulator. The dimensions of the structures are tabulated in Table 4-2.

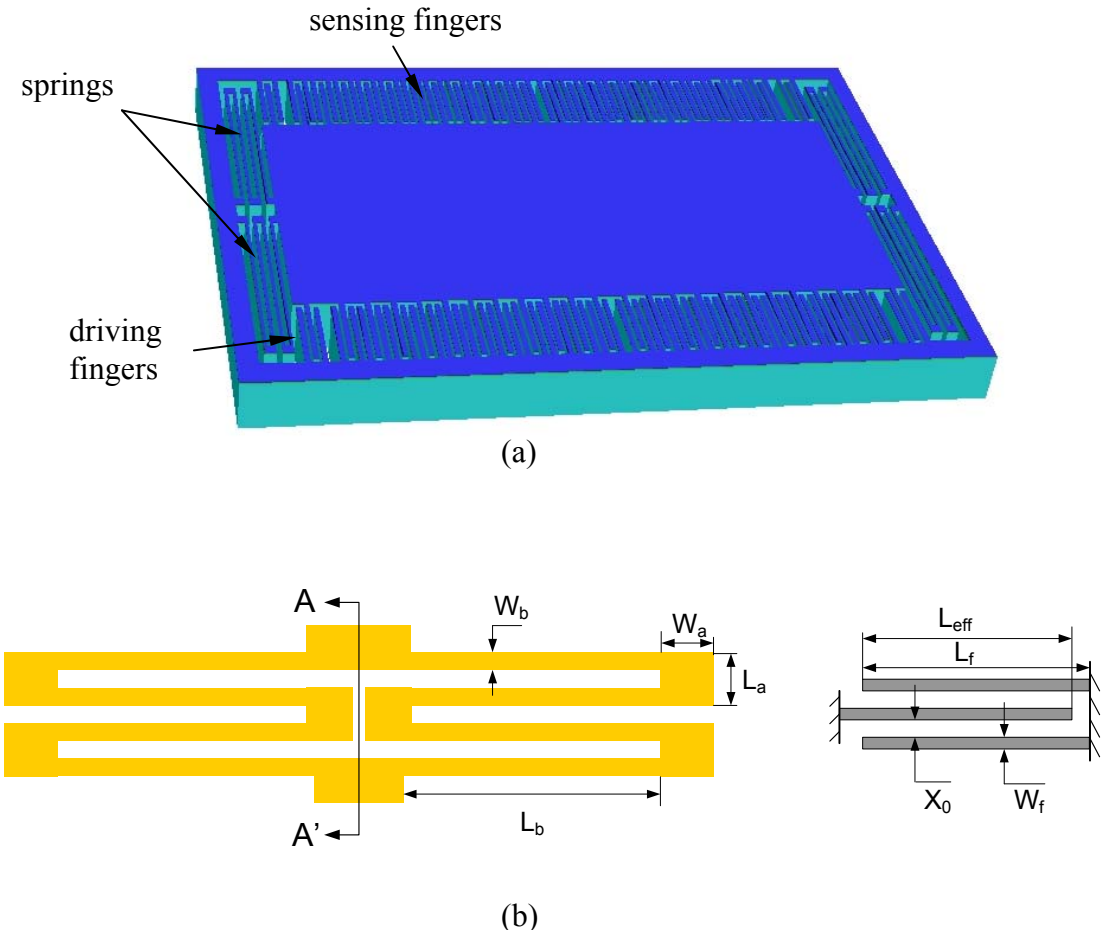


Figure 4-3. Schematic 3D model and mechanical spring configuration of the single-axis accelerometer. (a) 3D model of the device, (b) spring configuration.

Due to the large ratio of L_a/W_a in the configuration, the spring constant of half of the serpentine mechanical springs, as seen from AA' in Figure 4-3(b), can be simplified as [119]:

$$k_{quat} = \frac{1}{(n-1)^3} \cdot E(\frac{W_b}{2L_b})^3 t \qquad (4.6)$$

where n is the number of turns of the mechanical springs, E is the Young's Modulus of silicon, t is the thickness of the springs. Since there are two sets of the springs on each end of the proof mass, the overall spring constant k should be the double of what is in Equation 4.6.

The mechanical resonant frequency of the sensor is then

$$f = \frac{1}{2\pi}\sqrt{\frac{k}{m}} \qquad (4.7)$$

where m is the mass of the proof mass.

Table 4-2 Dimensions of the lateral accelerometer

Parts (unit)	**Notation**	**Dimensions**
Proof mass area (μm^2)	A	300*600
Length of single turn spring (μm)	L_b	200
Width of single turn spring (μm)	W_b	4
Length of meander (μm)	L_a	13
Width of meander (μm)	W_a	10
Length of comb finger (μm)	L_f	85
Length of effective comb finger (μm)	L_{eff}	80
Width of comb fingers (μm)	W_f	4.8
Gap of the fingers (μm)	x_0	2.1
Thickness of all the structure (μm)	t	50
Number of sensing comb finger pairs	N	56

4.1.2 Device Simulation Using Finite Elements Method (FEM)

The mechanical performance of the accelerometer was simulated with CoventorWare. Folded mechanical springs are employed to reduce the device size. They suspend the proof mass symmetrically.

The simulated resonant frequency of the lateral accelerometer is 6.05 kHz, which is within 10% of the value calculated using Equations 4.6 and 4.7. The calculated parasitic

wiring capacitance is less than 60 fF, according to the technical data of TSMC 0.35μm process provided by TSMC and the actual layout. While the mechanical thermal-elastic damping effects are neglected in this system, squeeze-film damping must be considered for the designed structure with large number of lateral sensing comb fingers. The squeeze-film damping coefficient of a single pair of the comb fingers is given by [120]

$$b = 7.2N\mu t(\frac{l_{eff}}{x_0})^3 \qquad (4.8)$$

where N is the number of comb fingers; μ=1.54×10^{-6} *kg/m/s* is the viscosity of the air under atmospheric pressure at 20°C [112]. l_{eff} is the engaged length of the comb fingers. In the designed lateral-axis accelerometer, 4 groups of comb finger arrays, each consisting of 14 pairs of fingers are used to achieve large sensing capacitance. There are also 4 groups of driving comb fingers, each consisting of 2 pairs of fingers with the same dimension as the sensing comb fingers. Therefore, in Equation 4.8, N=(14+2)×4=64.. The dimensions of the structures in the designed accelerometer are listed in Table 3-1. The equivalent Brownian noise a_m can then be expressed as [121]

$$a_m = \frac{\sqrt{4k_BTb}}{9.8m} \quad (g/\sqrt{Hz}) \qquad (4.9)$$

where k_B is the Boltzman's constant (1.38×10^{-23} J/K), T is the absolute temperature of the working ambiance and m=12.6 μg, is the proof mass of the accelerometer.

The snap-in voltage can be calculated based on the electrostatic spring softening effect by balancing the electrostatic spring constant and the mechanical spring constant [117], this yields

$$V_{snap} = \sqrt{\frac{8k_m x_0^{\,2}}{27C_0}} \qquad (4.10)$$

where the mechanical spring constant k_m is approximately $30\ N \cdot m$.

The designed accelerometer has 13×4 pairs of sensing fingers, wired in a common-centroid configuration as in Figure 4-2. The modulating voltage is designed as 1.5 V. The proof mass is assumed as approximately 23 μg, attributed to the incorporated SCS. The performance of the designed accelerometer can be predicted based on the above equations, as tabulated in Table 4-3.

Table 4-3. Predicted performance of the designed single axis accelerometer

Parameters	**Units**	**Calculated value**
Total sensing capacitance	fF	440
Device sensitivity (without amplification)	mV/g	2.3
Brownian noise of the sensor	$\mu g / \sqrt{Hz}$	38.9
Resonant frequency	kHz	6.05
Snap-in voltage of the sensing comb drive	V_{si}	15.5
Quality factor		1.1

With a designed 40 dB on-chip amplification, the output sensitivity of the device can be expected as high as $0.23 V / g$. The noise floor of the interface circuit is about $10 nV / \sqrt{Hz}$ [113]. This single-axis accelerometer is integrated with the 3-axis accelerometer. Their layout will be shown in later section.

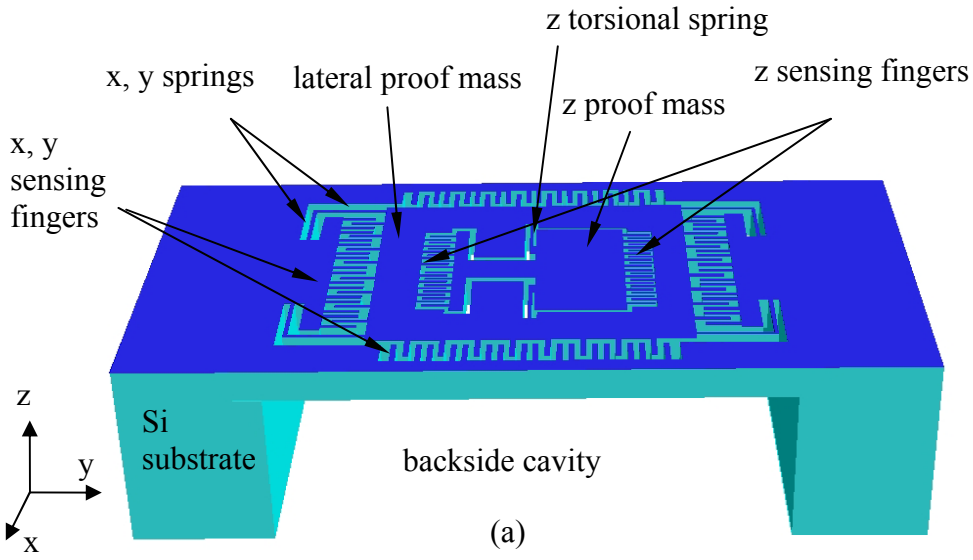
4.3 Tri-axial Accelerometer

A unique 3-axis accelerometer is the primary device developed using the proposed post-CMOS MEMS technology [86]. The independent silicon DRIE steps for electrical isolation structure formation and device release allow a precise control of the structure dimensions and critical profiles. By incorporating SCS in the mechanical spring, robust devices are accomplished.

As introduced in Chapter 1, there are normally two topologies for dual or 3-axis accelerometers. The hybrid topology has the advantage of better mechanical performance

due to the optimized mechanical structure. The monolithic integrated approach has much lower parasitics. In this thesis work, the monolithic integration approach is used for the design of a 3-axis accelerometer. Moreover, in order to further reduce the device size and parasitic effects caused by the long wiring path, the z-axis sensing element is embedded in the proof mass of the lateral accelerometer, as schematically shown in Figure 4-4(a). As a first-order approximation, the dual-axis lateral accelerometer can be considered as a regular lateral accelerometer with a solid proof mass. In each sensing direction, i.e. x-axis and y-axis, it consists of four groups of symmetric sensing and actuation comb fingers along the two opposite sides of the proof mass. The sensing comb fingers are wired the same way as in the single-axis accelerometer described in the last section for common mode rejection. The proof mass is anchored to the silicon substrate through four symmetric crab-leg SCS springs. The crab-leg springs permit displacement in both lateral directions, enabling the lateral sensing by the comb fingers on the proof mass.

This compact configuration can improve the circuit performance by reducing the parasitics at a slight cost of possible cross-axis mechanical coupling. The simulated results, as presented in the following section, show that the mechanical coupling is acceptable for this kind of small-sized device designed for portable electronics and engineering monitoring. Figure 4-4(b) shows the layout of the single and 3-axis accelerometer, along with other test structures. The dimensions of the designed 3-axis accelerometer are tabulated in Table 4-4.



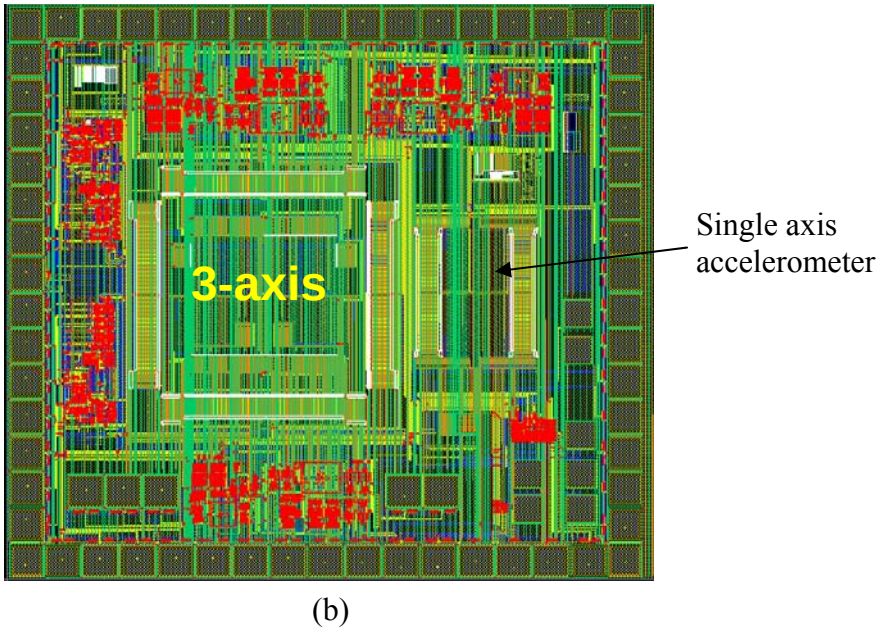


Figure 4-4. Schematic 3D model of the 3-axis accelerometer and layout of devices designed. (a) Schematic 3D model showing the configuration of the sensing elements. (b) Layout of the integrated single and 3-axis accelerometer chip with circuit blocks.

Table 4-4. Structural dimensions of the designed 3-axis accelerometer.

Structures	**Dimension**
Lateral proof mass (μm×μm)	1000×1000
Torsional plate (μm×μm)	700×300
Structure Thickness (μm)	50
Lateral sensing finger length (μm)	90 (80 engaged)
Z sensing fingers length (μm)	80
All finger gaps (μm)	2.1
Lateral springs ($l \times w$) (μm×μm)	320×5
Z torsional springs ($l \times w$) (μm×μm)	400×5
Number of lateral sensing fingers	18×4
Number of z-sensing comb fingers	25×4

4.2.1 Z-axis Sensing

One of the main challenges for achieving monolithic 3-axis capacitive accelerometers is how to realize z-axis sensing. The difficulty of z-axis sensing lies in the fabrication of horizontal electrodes to sense out-of-plane displacement in the presence of large parasitic capacitance to the substrate, especially when differential sensing is needed. Z-axis capacitive sensing with an imbalanced proof mass and torsional springs have been demonstrated [83, 122], but they suffer from either non-differential sensing or complicated fabrication processes. In the torsional structure described in [122], glass-silicon bonding, wet etching and chemical mechanical polishing (CMP) were required, which complicates the fabrication process. Recently, a bulk-silicon, integrated, 3-axis CMOS-MEMS accelerometer was demonstrated [123]. However, it has two drawbacks. First, although most of the sensing structure is made of single-crystal silicon (SCS), the z-axis sensing employs Al/SiO_2 thin-film spring beams, which have large out-of-plane curling and poor temperature performance. Second, the silicon undercut for electrical isolation of substrate silicon also undercuts the silicon underneath comb fingers, which increases the comb-finger gap and in turn reduces the sensitivity.

As described in Chapter 1, the purpose of the improved DRIE post-CMOS MEMS technology developed in this thesis work is to solve the problem of the simultaneous undercut on the isolation structure, comb fingers and mechanical springs, thus overcome the drawback of the device in [123]. Torsional sensing is one method to achieve out-of-plane sensing in the z-axis without sacrificing the robustness of the device. In this 3-axis accelerometer design, a torsional z-axis sensing element is employed that uses the sidewall capacitance of the embedded metal layers for differential capacitive sensing. The z-axis accelerometer is embedded in the dual-axes sensing proof mass by suspending the imbalanced z-axis proof mass to the lateral sensing proof mass with a pair of SCS incorporated torsional springs, as shown in Figure 4-4(a).

The concept of the z-axis sensing is illustrated in Figure 4-5. The z-axis sensing element consists of an imbalanced proof mass, a torsional spring beam and comb fingers on both ends of the proof mass. If there exists an external acceleration in z-axis, a net torque is generated about the torsional spring due to the mass difference on two sides of the imbalanced proof mass. Thus, one end of the proof mass moves down and the other end moves up with the same displacement. This symmetry is due to the same distance (L) from the both ends of the imbalanced proof mass to the torsional spring, as shown in Figure 4-5(a). The out-of-plane displacement is capacitively sensed by the capacitors formed among the metal layers in the CMOS thin-film stacks.

Note that the SCS underneath the metal/SiO_2 multilayer stacks is not shown in Figure 4-5(b). SCS in the z-axis sensing comb fingers is used only as a mechanical support to maintain the flatness of the comb fingers. It is grounded to the substrate

through the SCS on the torsional springs in z-element and crab-leg springs on lateral proof mass.

The wiring configuration is shown in Figure 4-5(b), where all three metal layers in the stators are electrically connected, while the rotors have only two metal layers which are electrically isolated. Therefore, four sidewall capacitors, C_{1a}, C_{1b}, C_{2a} and C_{2b}, are formed. The pair C_{1a}/C_{1b} changes values oppositely when there is a z-axis acceleration induced rotation; so does the other pair C_{2a}/C_{2b}. Note that C_{ia} and C_{ib} $(i=1, 2)$ are not equal even at the rest position. This is due to two factors. First, the top metal layer M3 will be slightly thinner than the bottom metal layer M1 because of the ion-milling effect during the etching of SiO_2 during the post-CMOS fabrication. Second, there is a SiO_2 layer and supporting SCS structure underneath M1 but nothing on top of M3. This results in an asymmetric electric field along the z axis. Therefore, there will be a large d.c. offset if a capacitive half bridge is formed by only one pair of C_{ia} /C_{ib}. However, note that C_{1a} changes value the same way as C_{2b} which is on the other side of proof mass; so does C_{1b} with C_{2a}. With this observation, the large d.c. offset can be compensated by constructing a half capacitive bridge with the wiring as illustrated in Figure 4-5(b). This connection forms a differential capacitive bridge with two pairs of capacitors, i.e., $C_{1a}+C_{2b}$ $(=C_2)$ and $C_{2a}+C_{1b}$ $(=C_1)$. The equivalent circuit is shown in Figure 4-5(c). In this configuration, $C_1 = C_2$ at the rest position.

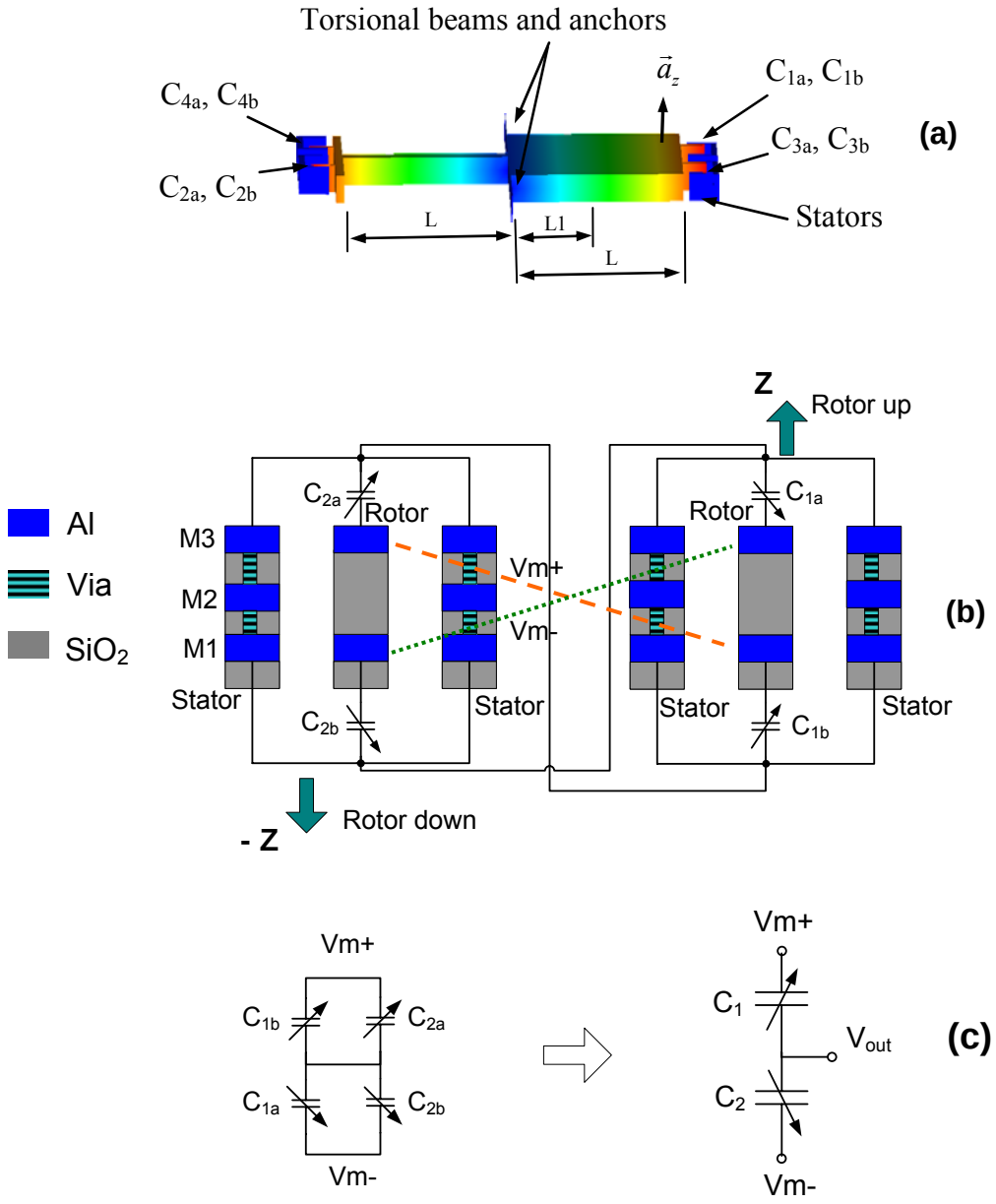


Figure 4-5. Differential connection of the sidewall capacitors in z-axis sensing element. (a). Torsional block motion in z direction and the capacitor arrangement. (b). Common-centroid configuration of the capacitance. (c). Formation of the half sensing bridge.

For the half capacitive bridge in Figure 4-5(c), at the presence of a z-axis acceleration a_z, the output voltage V_{out} is given by [84]

$$V_{out} \approx \frac{d}{dz}\left[\frac{C_1(z)-C_2(z)}{C_1(z)+C_2(z)}\right]\cdot\frac{m_z a_z L_1 L}{k_t}\cdot V_m \qquad (4.11)$$

where m_z is the net mass of the Z sensing block, L_1 is the distance from the mass center of the z-axis proof mass to the torsional beam, L is the distance from the torsional beam to the end of the proof mass and V_m is the modulation voltage. A small-angle approximation is used for deriving the above equation and the mass of the sensing fingers is neglected.

k_t is the torsional stiffness of the torsional beam, which is given by [124]:

$$k_t = \frac{2Gw_b^{\,3}t}{3l_b} \qquad (4.12)$$

where l_b is the length of the torsional spring beams, t is the thickness of the beam, w_b is the width of the torsional beam and G is the shear modulus of the beam (silicon).

Then, the resonant frequency of the torsional z sensing element is then,

$$f_z = \frac{1}{2\pi}\sqrt{\frac{k_t}{I}} \qquad (4.13)$$

where I is the overall moment of inertia of the z proof mass about the torsional spring and is given by:

$$I = \sum_n I_n = \frac{1}{3} m_z L_1^{\,2} \qquad (4.14)$$

where n stands for the different rectangular plate on the z-axis proof mass, and L_1 is the distance from the mass center to the torsional springs.

Due to the complexity of the fringe capacitance formation, only FEM simulation was performed to predict the capacitance change versus the external acceleration.

Figure 4-6 shows the CoventorWare™ simulation results of the capacitance change as a function of z acceleration ranging from -50g to +50g. Two stators and two rotors on each end of the sensing block are used in the simulation for simplicity. This simulation is based on the actual dimension of the designed device listed in Table 4-4. Due to the large difference in dielectric constant of the SiO_2 thin film and the air, it is apparent that C_{1a} differs from C_{1b} in value at the rest position. In value, C_{1b} is almost the double of C_{1a}. However, after swapping the counterpart capacitors in the opposite side of the proof mass, C_1 and C_2 are equal when the z sensing block is flat and they change their value oppositely under the external acceleration.

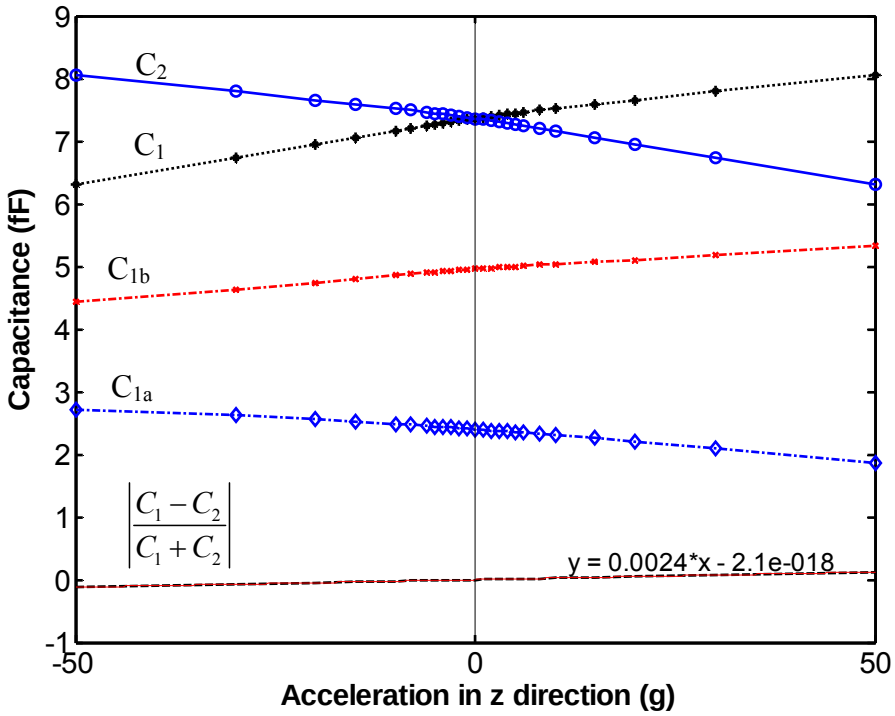


Figure 4-6. Capacitance change in the range of -50*g* to +50*g* in z direction shows a good linearity.

Due to both the small displacement in the z-axis and the rotational angle about the torsional spring, a good linear sensing output can be achieved because of the linearity of the term $\left|\frac{C_1 - C_2}{C_1 + C_2}\right|$. The fitted curve of this term is shown in the figure as well.

A fully differential capacitive bridge can be formed when the other two groups, C_3 and C_4, are connected in the same configuration. With this fully differential topology, the sensor offset caused by the fabrication variations and the cross-axis coupling can be greatly reduced. In addition, bidirectional sensing in z axis is achieved.

Based on the calculation above, the sensitivity of the lateral and z elements can be expected as 4.5*mV/g* and 2.4*mV/g*, with approximately a total capacitance of 600 *fF* and 86 *fF,* respectively. The noise floor of the lateral sensing element is 0.35 $\mu V / \sqrt{Hz}$. Since the z sensing element has a Couette damping instead of squeeze-film damping between comb fingers, which has a much lower damping coefficient, as shown in Equation 4.15.

$$b_z = N_z l_z \frac{t_z}{g_z} \qquad (4.15)$$

where N_z is the number of the z-axis sensing fingers, l_z, t_z, are the length, thickness of the z-axis sensing comb fingers and g_z is the gap between z comb fingers.

Compared to lateral axes, the damping coefficient in z-axis is much smaller according to Equation 4.15. However, due to the smaller z-axis proof mass, the noise floor of the z sensing element calculated using Equation 4.9 is considerably large. The z quality factor is larger than those in lateral axes due also to the smaller proof mass. The predicted performance of the 3-axis accelerometer is summarized in Table 4-5.

Table 4-5. Predicted performance of the designed 3-axis accelerometer

Parameters	**Unit**	**Value**
Total lateral sensing capacitance	fF	400
Total z-axis sensing capacitance	fF	86
Sensitivity in lateral axes	mV/g	4.5
Sensitivity in z-axis	mV/g	2.4
Quality factor in lateral axes		1.1
Quality factor in z-axis		3.6
Brownian noise of the lateral axes	$\mu g / \sqrt{Hz}$	5.5
Brownian noise of the z-axis	$\mu g / \sqrt{Hz}$	27.0

4.2.2 Analysis of the Cross-axis Coupling

The simulated resonant frequencies of the first three modes of the 3-axis accelerometer are respectively 1.70 *kHz*, 3.23 *kHz* and 3.51 *kHz*, corresponding to the rotation about the torsional spring of the z sensing element, the in-plane transversal motion of the whole structure along x direction and the in-plane longitudinal motion along y direction, respectively. The accelerometer is designed to work in a bandwidth of 0 ~ 500*Hz* in frequency, as shown in Table 4-1. Therefore other modes at higher frequencies can be neglected. One of the most significant features of the designed 3-axis accelerometer is the fully differential configuration in all the three sensing elements by a common-centroid wiring. It is capable of canceling most cross-talk caused by orthogonal mechanical coupling. Simulation results conclude that the cross-talk between x and y axis is negligible by the virtue of the symmetric mechanical geometry and common-centroid electrical wiring in both directions. Moreover, since the lateral crab-leg springs are rigid in z direction, the influence of the motion of embedded z proof mass on lateral structure can be neglected.

In this analysis, only the coupling of z sensing element from lateral motion will be addressed. By analyzing the force applied on the torsional beam, starting from the equation

$$T = G \cdot I \cdot \theta_l \qquad (4.16)$$

where T is the torque generated by the imbalanced proof mass. I is the moment of inertia, and θ_l is the rotational angle per length along the torsional beam. The rotational angle on the proof mass θ can then be calculated as [124],

$$\theta = \frac{m l_1 l_b}{2\alpha G t w_b^{\,3}} a_z \qquad (4.17)$$

where α is an adjusting constant defined by the ratio of t/w_b, l_1 is the distance from the center of the z proof mass to the torsional beam, as the L_1 in Equation 4.11.

For our structure, the α in (1.5) is 0.32~0.33 for the ratio of $t/w_b = 50/3$ [124].

Even though an analytical model can be created to reveal the motion of the z element in the mechanical domain, it is complex to predict the fringe capacitance change in the presence of the external vertical acceleration, especially when a torsional structure is involved. Therefore, only FEM analysis is carried out using the CoSolver tool in CoventorWare by including iterations in the mechanical and electrical domains simultaneously. For the coupling evaluation, the z capacitance change responding to z acceleration was swept in the presence of either x or y acceleration. The z acceleration was swept from negative 10 *g* (pointing down) to positive 10 *g* (pointing up), with a lateral acceleration of 1 *g* or 3 *g* applied to the device at same time. These values were then compared with the capacitance values under pure z acceleration without any lateral coupling.

Figure 4-7 shows both the capacitance change in z acceleration with and without the coupled acceleration from lateral axes. Figure 4-7(a) is the capacitance response to z-axis acceleration with and without 1g coupled from lateral axes. The right figure, 4-7(b) shows the zoomed portion where the cross of C_1 and C_2 happens. Figure 4-7(c) is the same as Figure 4-7(a) except that the coupled lateral accelerations are changed to 3g both in x and y axis. Figure 4-7(d) is the zoomed portion of 4-7(c).

It is observed that the larger coupling effect to z-axis comes from in y direction, as shown in Figure 4-7(a) and (c). However, this kind of coupling is very small. From calculation based on the data in the both plots, the maximum capacitance change caused by y direction coupling is on the order of 10^{-4} of the original value without coupling. Therefore, the coupling effects from both lateral axes to z sensing element are negligible.

It should be pointed out that the simulation conducted above is reliable. Under two randomly selected conditions, i.e., -5*g* and -10*g* acceleration in z axis, the simulation result as a function of the number of meshing elements is plotted as Figure 4-8. The number of elements in the mesh ranges from 1820 to 20312. After the number reaches 5600, the simulation results vary within 5.5%, which means a confidence of 89%. To simulate effectively for the z acceleration sweep, the z sensing element was meshed with 5600 volume elements.

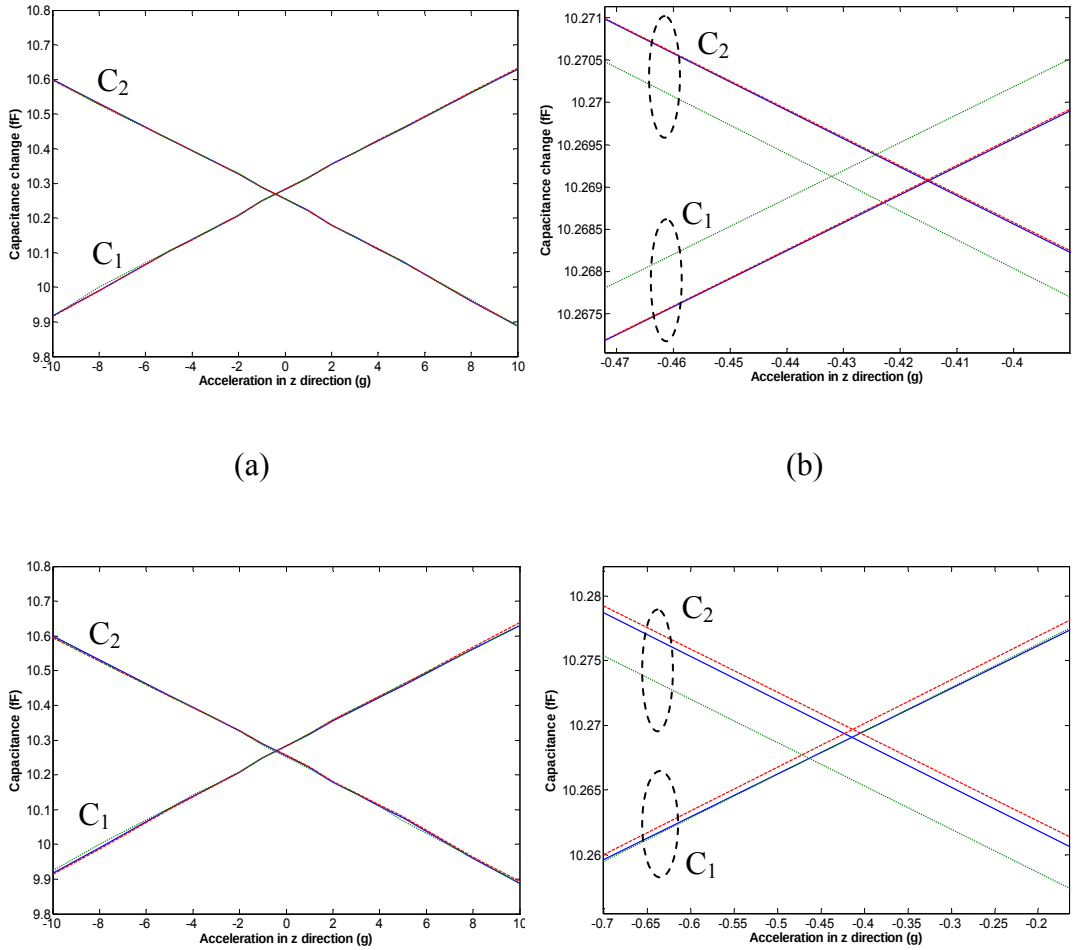


Figure 4-7. Z capacitance coupling from the lateral motion. (a) Z capacitance change with and without 1g coupling from both x and y direction. (b) Portion of zoomed (a). (c) Same as (a), lateral acceleration is 3g in both x and y direction. (d) Portion of zoomed (c).

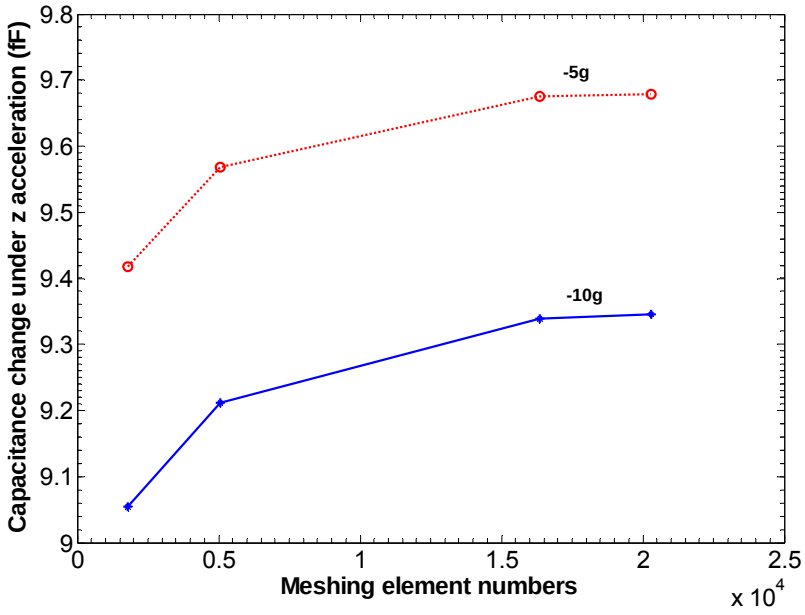


Figure 4-8. The relation between capacitance change and the number of volume elements in mesh shows a convergent trend, indicating the reliability of the simulation.

4.4 Summary

Two CMOS MEMS accelerometers, including one single-axis and one 3-axis integrated accelerometer, have been designed and their performances are predicted in this chapter. These devices are designed to have applications in engineering monitoring and human activity monitoring and sensing, in which small size, robust structures and low noise floor are required. The devices are intended to be fabricated using the proposed new post-CMOS MEMS technology. Due to the SCS incorporated in the sensing comb fingers, large sensing capacitance and high sensitivity can be achieved for in-plane lateral acceleration. The independent etching processes for the electrical isolation and comb fingers and other mechanical structures enables less undercut on the comb fingers, which further increases the sensitivity by reducing the gap between the fingers. In the 3-axis accelerometer, the torsional z sensing element is embedded in the proof mass of a dual-

axis in-plane lateral accelerometer. Sidewall and fringe capacitance of the CMOS metal layers is employed in the z-axis sensing. By swapping the symmetrically distributed sidewall capacitors, fully differential sensing is accomplished in z sensing as well as the lateral sensing.

CHAPTER 5
SOME ISSUES IN THE DEVICE FABRICATION

In the fabrication of the designed devices, especially that of the 3-axis accelerometer, which has over five hundred sensing and driving comb fingers, some issues particularly relating to the improved DRIE CMOS-MEMS process were observed. These issues include: problems in the top metal layer removal, isolation trench contamination caused by subsequent etching steps, and comb finger undercut due to the thermal effects in the plasma processes. In this chapter, these specific practical issues observed in the device fabrication are addressed, and solutions to these issues are presented. Not only are these solutions valid to the fabricated accelerometers, but also to other MEMS devices with similar suspended structures fabricated using dry plasma etching. In particular, these fabrication methods can be used in the post-CMOS microfabrication of MEMS gyroscopes, in which both suspended driving and sensing structures exist [70]. In addition to the general design rules generated from the ordinary etching system characterization, as described in Chapter 2, some other significant MEMS design rules can be extracted from these observations for the design and optimization of the similar MEMS devices.

5.1 Top Aluminum Layer Removal

When the improved DRIE post-CMOS MEMS technology is employed in the microfabrication of the designed CMOS-MEMS accelerometers, the top metal layer on the devices are only used to define the electrical isolation structures, which isolate the comb fingers from the substrates, as shown in Figure 3-4(b). After the formation of the

electrical isolation structures, the top metal layers are removed to expose the other mechanical structures on the accelerometers. In practice, this step is performed after the first SiO_2 etch, as shown in Figure 3-5(c). Cl_2-based plasma aluminum anisotropic etch can be used in the top metal layer removal. Normally Cl_2 is mixed with BCl_3, which plays an important role in removing the local native Al_2O_3 layer and scavenging water vapor absorbed on the Al surface [87]. Due to the unavailability of BCl_3, the aluminum dry etch was only tested using Cl_2/Ar gas mix. After experiments, it is shown that the residues on the chip surface after the Cl_2/Ar plasma etch pose a severe risk to the later processes. Without BCl_3, some big clusters of involatile byproducts remain on the device surface, forming micro masks in the later etching processes. Figure 5-1 shows a cluster of these residues. The typical size of the individual residue is approximately 4 μm×3 μm.

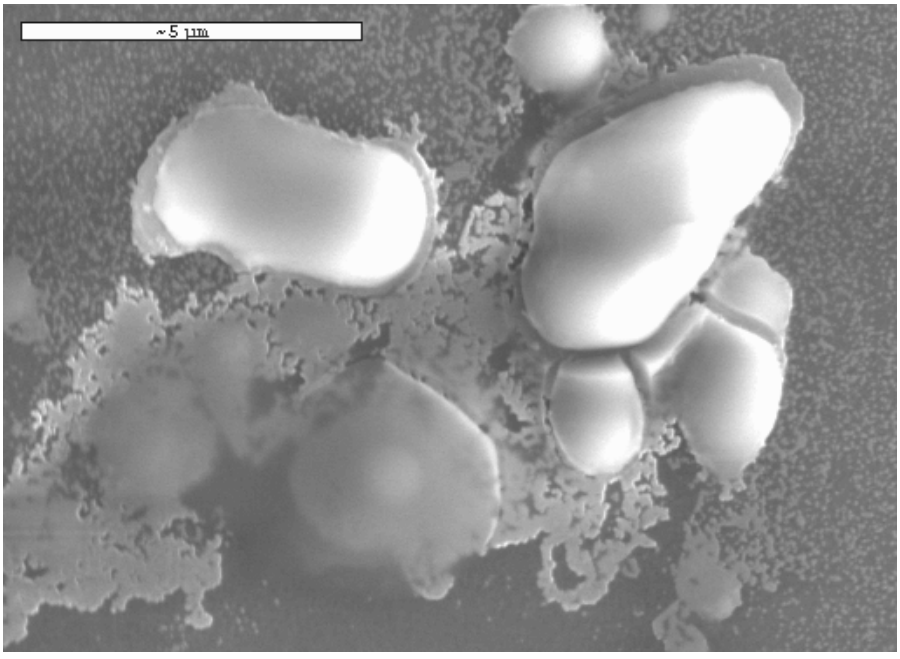


Figure 5-1. A cluster of the residual byproduct formed in the aluminum plasma etch using Cl_2/Ar chemicals.

A special low-cost and clean wet Al etch process was developed to avoid the potential micromasking effect of the residues in the Cl_2 plasma etch described above. In order to protect the sidewalls of the metal layers other than top layer, which form the isolation beam, a polymer layer is deposited over the whole device using the passivation cycle of the Bosch process. Then, a regular deep silicon etch follows to remove the polymer on the top surface of the device and the bottom in the isolation trenches. Note the polymer layer remains on the sidewalls of the isolation trenches in this etch step, as shown schematically in Figure 5-2(a). Next, the standard Ashland aluminum etchant (Phosphoric acid: nitric acid: acetic acid: de-ionized water = 16:1:1:2) is used to etch the exposed top Al layer at 40°C. The top Al layer (about 0.8μm in thickness) is etched away in approximately two minutes and ten seconds. No apparent aluminum undercut was observed on the sidewalls of the isolation beams due to the protection of the remaining fluoride polymer. Figure 5-2(b) and (c) show the isolation beam wetly etched using the aluminum etchant with and without the passivation layer protection on the sidewall. It is clear that the sidewall of aluminum layers in the isolation beams has been greatly improved with the polymer layer protection.

Although this polymer passivation method is effective for the aluminum sidewall protection, it introduces one more process step and increases the fabrication cost. One easier way to avoid this extra step is to protect the aluminum in the isolation beams with SiO_2 layer. This can be easily realized in the design step. Figure 5-3 illustrates the cross section view of the designed isolation beam structure before and after the SiO_2 etch. M2 and M3 beams are designed slightly narrower than M4 beam. Thin vertical SiO_2 spacers

will be left on both sides of the stack after the SiO_2 etch, which act as protection to the inner aluminum beams in the following wet Al etch.

In practice, the first SiO_2 etch can stop anywhere between M1 and M3 before the top M4 removal. This also can effectively reduce the chance of M2 and M3 exposure due to the undercut on SiO_2 spacers in the long plasma etch.

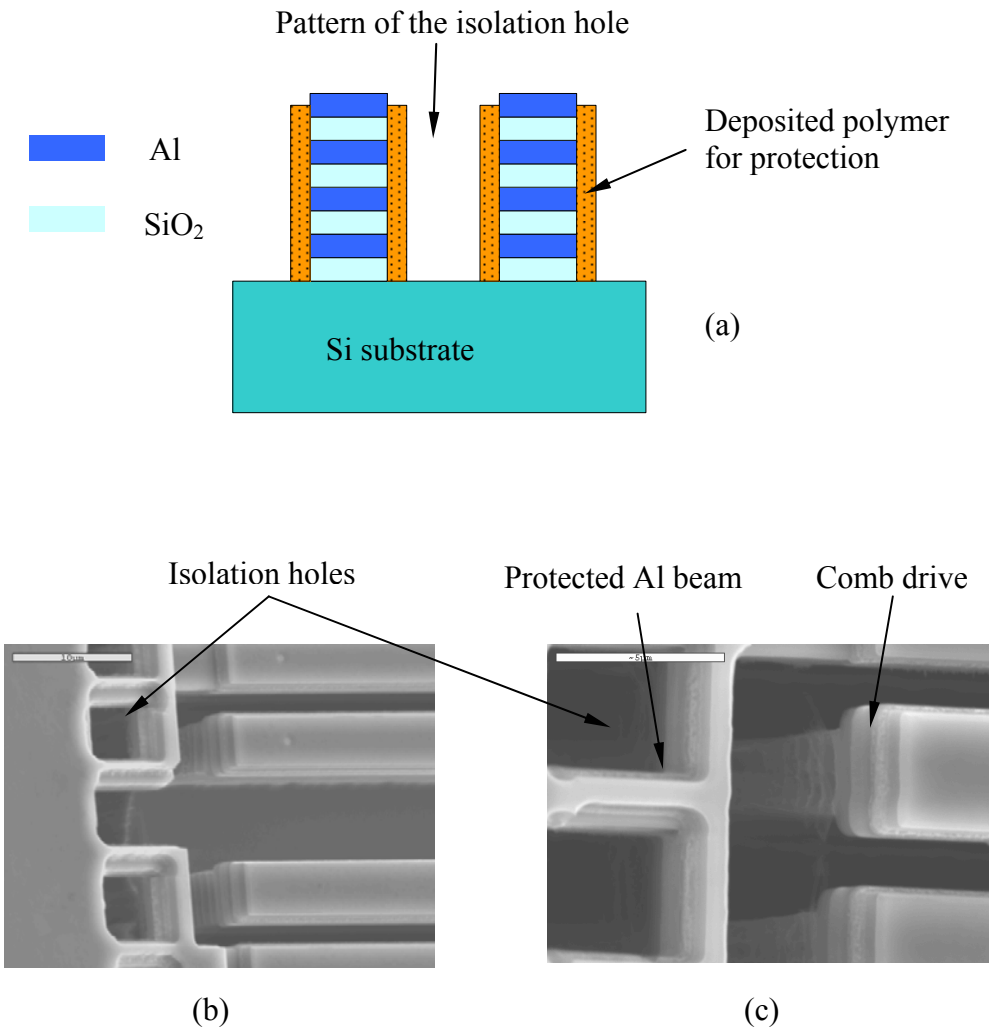


Figure 5-2. The mechanism and result of the sidewall protection in the aluminum wet etch. (a) schematic of the polymer protection; (b) isolation beams after the wet etch of the top aluminum layer without polymer protection; (c) same structures after the aluminum wet etch with polymer protection.

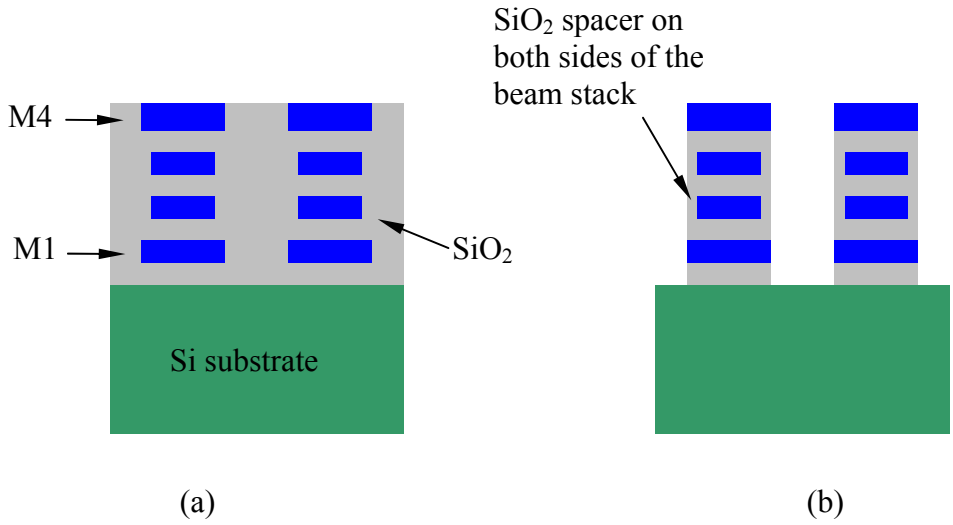


Figure 5-3. Formation of the Al sidewall protection spacers on the isolation beams. (a) before SiO_2 etch; (b) after SiO_2 etch.

5.2 Dry Etch Caused Device Contamination

Sidewall and surface contamination of the device during the process is a very common phenomenon in the dry plasma etches and has been investigated intensively [125-132]. The reported research efforts mainly focused on the physical and chemical principles of the contamination formation from a metallurgical point of view. The samples used in these research efforts had only simple patterns and the process time was relatively short. In MEMS devices, the dry etch process caused device contamination is more severe because of the complexity of MEMS structures in all three dimensions and the longer etching time. If multiple plasma process steps are required in the microfabrication of a MEMS device, the microfabrication would be even more challenging due to the cross contamination. In the microfabrication of the designed 3-axis accelerometers using the improved DRIE post-CMOS MEMS technology, the cross contaminations caused by the alternate SiO_2 RIE and Si DRIE plasma etch steps are identified as the major reason for the failure of device release. The main contamination

occurs on the sidewalls of the isolation trenches. In particular, the additional isolation trench etching specifically needed in the developed DRIE CMOS MEMS technology introduces more potential device contamination. The involatile contaminants on the sidewalls act as micro masks in the following plasma etch steps, leaving some tiny connections between the movable and fixed structures after all the etching processes are completed.

Figure 5-4 shows the SEM photos of the etched-through comb fingers in a fabricated 3-axis accelerometer. As observed from the backside of the device, all other regions on the comb fingers were etched through except for the narrow connections along the both ends of the fingers. In many case, this connection line causes the failure of the device release. In this section, the sources of the contamination are investigated and corresponding methods to avoid or overcome the contaminations are presented.

5.2.1 The Sources of Contamination

The contamination sources in the device fabrication include debris and residues generated in the dry etch steps which fell onto the front surface; the inhibitor and sputtered particles on the sidewall of the structures; and the additional contamination layer on the sidewalls of the isolation trenches and on the backside surface of the device which is caused by the backside scattering of the ions. The mechanism of the contamination formation are schematically illustrated in Figure 5-5. The contaminants originate from a variety of sources and have particular impacts on the mechanical structure formation in the accelerometers. They are detailed as the following.

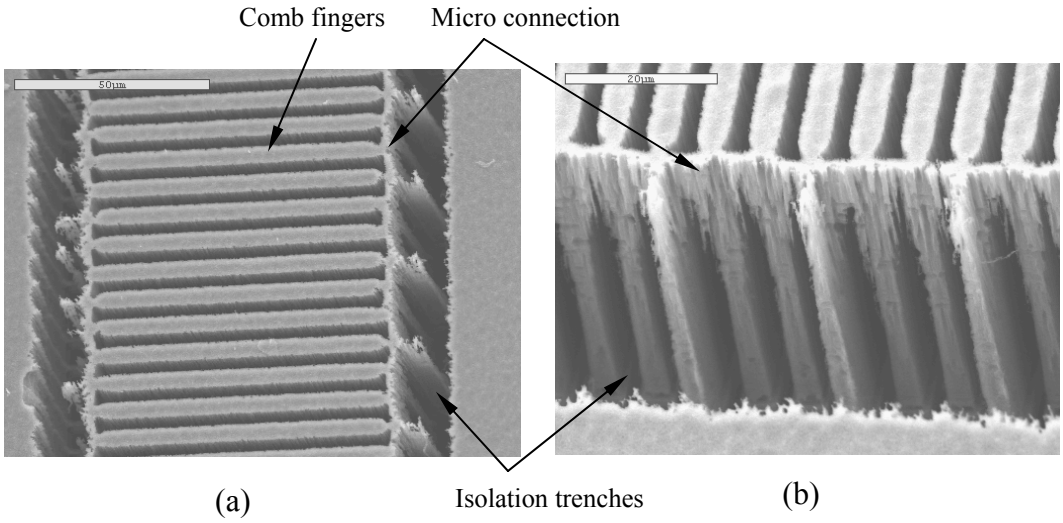


Figure 5-4. SEM photographs of the etched-through comb fingers. The narrow connections along the ends of the comb fingers are caused by the micromasking effect of the contaminant on the sidewall of isolation trenches. (a) top view from the backside of device, (b) side view by rotating the sample for 90°.

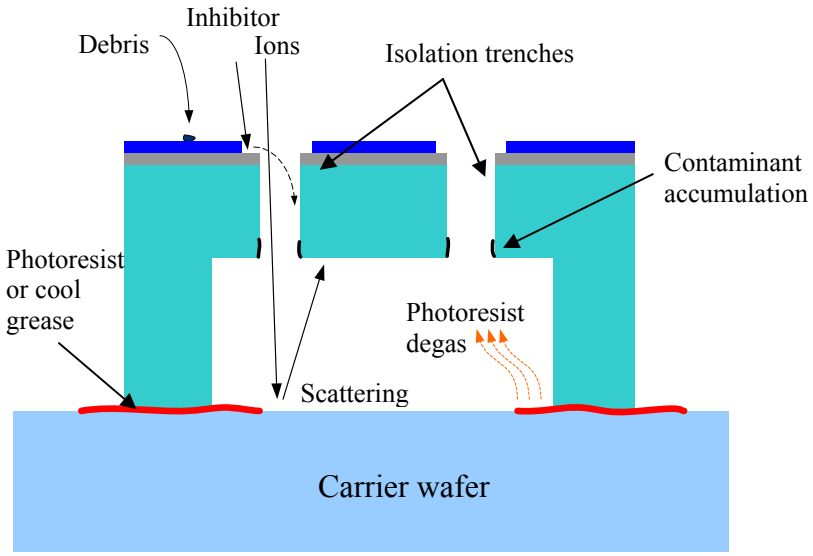


Figure 5-5. Schematic of the contamination in the plasma etch.

5.2.1.1 Front surface contaminants

The contaminants on the front side of the device include the debris generated physically during the etching process and the residues of the involatile byproducts after a chemical etching process. Note that the involatile by-products here differ from the inhibitors in SiO_2 etch. By optimizing an etching recipe, the chemical byproducts can be controlled very well. The sources of the debris, which consequently are mainly the physical contaminants, include the accumulated polymers on the chamber walls of the etcher and the sputtered or milled movable particles from the neighboring materials.

Figure 5-6 shows the contamination on the front side of the device observed at the interval of etching processes. In Figure 5-6(a), the debris found after the first SiO_2 etch turned out to be a tiny piece of photoresist bombarded from the coating resist layer on the carrier wafer on which the chip being processed was glued. Whereas in Figure 5-6(b), the source of the movable debris on the surface is believed to be a piece of polymer falling from the chamber walls of the etcher.

Once these photoresist and/or polymer debris fell onto the surface where the structure pattern is located, they would play a role of etching mask and the SiO_2 or SCS underneath them would not be removed after the dry etch. The movable structure would remain electrically and/or mechanically connected to the substrate if these debris particles happen to be on the top of the corresponding patterns. Figure 5-7 is a top view of a few z element sensing finger observed from the back side after the device release. Due to the existence of a piece of contaminant on the front side during the processes, one spot connecting a rotor finger and its neighboring stator comb finger was formed. This single connection just causes the failure of the device release.

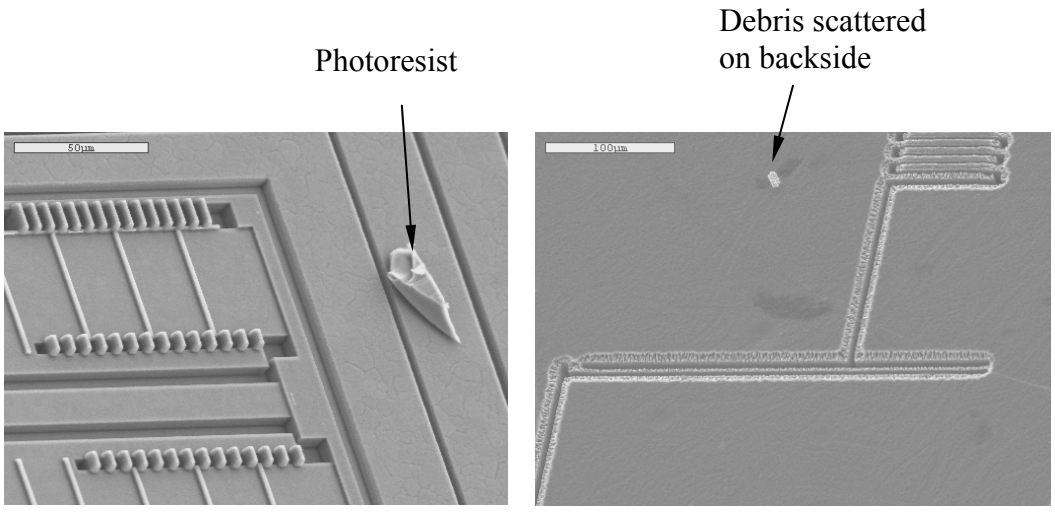


Figure 5-6. Front side surface contamination caused by the physical process in the plasma etching. (a) a small piece of photoresist was sputtered from the carrier wafer. (b) a piece of polymer scattered to the backside of a device.

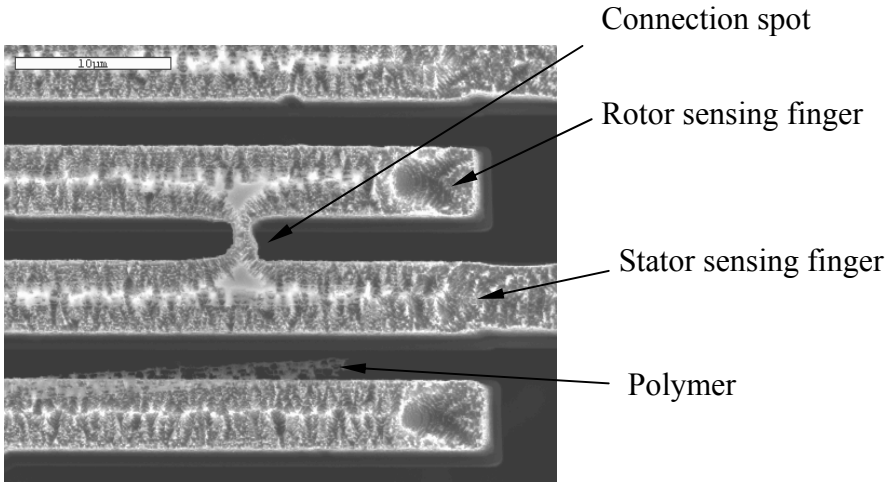


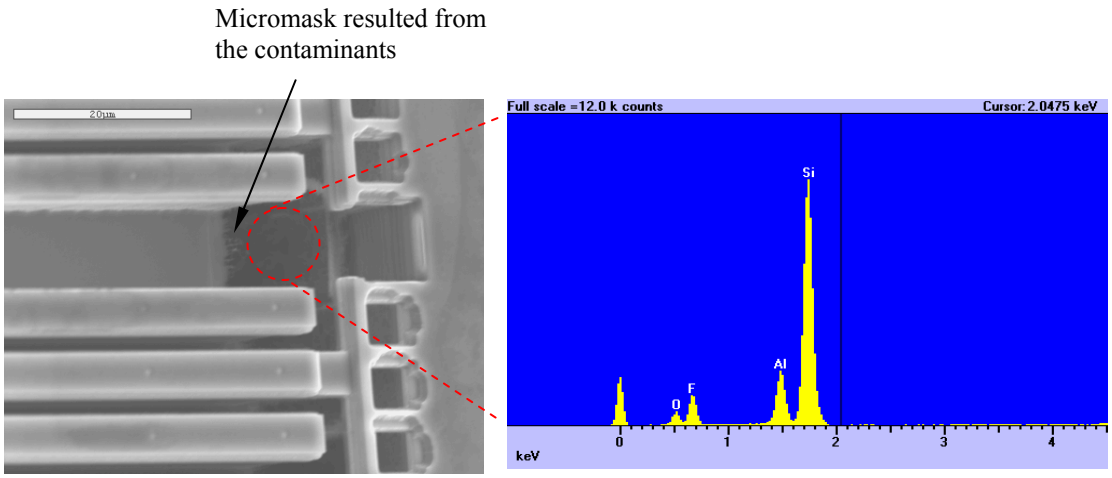
Figure 5-7. Structure connection caused by the debris on the front surface generated in the plasma etch.

5.2.1.2 Isolation trench sidewall contamination

The most severe process contamination hindering the successful release of the accelerometers is the contamination of the sidewalls of the isolation trenches. The sources of this contamination come from the plasma etching steps after the isolation trench etch. As illustrated in Figure 3-5 of the process flow the improved DRIE CMOS-MEMS process, there are still two plasma etching steps after the formation of the isolation trench, i.e. the SiO_2 etch to open the pattern of other MEMS structures and the Si DRIE for the final device release. It has been proven that the second SiO_2 etch after the trench etch contributes most of contamination on the sidewall of the isolation trenches. Figure 5-8 shows the SEM photograph of part of an isolation trench and the energy dispersive spectroscope (EDS) analysis of the composition on the sidewall of the isolation trench. The SEM image and EDS were taken after 10 cycles of Si DRIE in the last release step. The spectrum was obtained by scanning the circled region on the sidewall of the isolation trench.

The compositional analysis clearly indicates that the contaminants on the trench sidewall mainly originate from the SiO_2 etch in which the shown elements, F, O, and C (very small peak) were involved in the etching chemical of CHF_3 and O_2. These contaminants are actually the inhibitors formed in the SiO_2 etch. Since both ends of the trenches between adjacent sensing fingers are open in the SiO_2 etch, the inhibitors, mainly involatile oxide and fluoride, will fall into the isolation trenches and deposit on their rough sidewalls, as illustrated in Figure 5-5. Another possible source of the contaminants is the fluoride polymer generated in the passivation cycle of Si DRIE. The passivation polymer can stay on the rough trench sidewall, hiding in the micro caves caused by the ion scattering during the isolation trench etch. Since aluminum is present in

the compositional spectrum as well, it is believed that Al atoms are also sputtered directly from the device surface where the top aluminum layer covers everywhere.



(a) (b)

Figure 5-8. SEM image and EDS spectrum of part of an isolation trench and peripheral structures. (a) SEM photograph, (b) EDS spectrum of the circled region on the trench sidewall.

It was observed that the contaminants on the sidewalls of the isolation trenches described above tend to accumulate on the bottom region which is close to the back surface of the structure, as shown in Figure 5-5. This is easy to be understood. During the anisotropic etch of SiO_2 and SCS after the formation of the isolation trench, the impinging energetic ions hit the contaminants and eventually sweep them to the bottom region in the trench. It is from there that they act as a micromask in the following Si DRIE, leaving a connection line along the ends of the comb fingers next to the isolation trenches, as shown exactly in Figure 5-4. Since the isolation trenches were formed by performing an isotropic undercut after the anisotropic DRIE which etched through the isolation holes, the profile of the isolation trenches would not be straight on the sidewall due to the screening effect of the isolation beams in the silicon DRIE.

Figure 5-9(a) shows a broken structure with exposed sidewall of an isolation trench. The sidewall has a positive angle with respect to the plane of the back surface. This profile narrows down the isolation trenches in the bottom region, making the contaminants prone to accumulate there. A bowed profile has the same trend to collect contaminants there at the trench bottom, as shown in Figure 5-9(b).

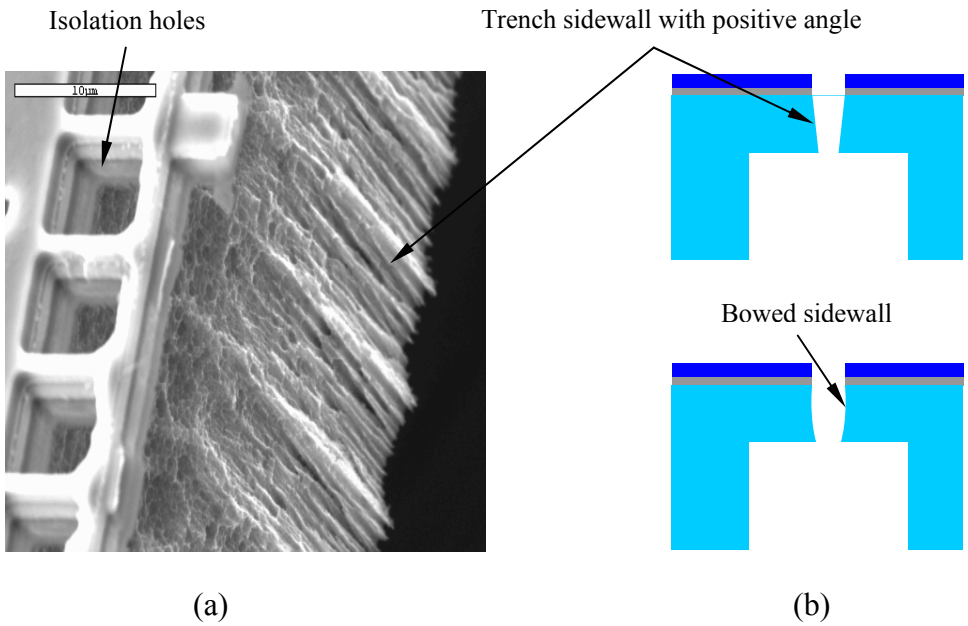


Figure 5-9. SEM image and schematic profile of an isolation trench sidewall with rough surface. (a) SEM photograph, (b) schematic profiles of the positive and bowed isolation trench.

5.2.1.3 Back surface contamination

Another type of contamination takes place on the backside of the thinned substrate diaphragm, as shown in Figure 5-5. The formation of this contamination can be classified into two categories with different mechanisms. The first is the redeposition of the particles onto the back surface of the device by backside scattering of the impingent ions. Since the isolation trenches are already open during the second SiO_2 and the last Si DRIE

step, particles are sputtered from either the front surface or the trench sidewalls, falling onto the surface of the carrier wafer just beneath the isolation trenches. Scattered by the impinging ions through isolation trenches, some of these micro particles can redeposit onto the back surface of the device diaphragm. The second mechanism is the degassing of the photoresist that is used to glue the device chip on the carrier wafer. During the soft bake of the photoresist at 95°C, or, even during the anisotropic SiO_2 etch and Si DRIE in which the chip temperature can be over 100°C due to the energy radiation from the plasma and the ion bombardment, the photoresist experiences a degassing process. In the enclosed backside cavity, organic compounds evaporate from the photoresist and deposit on the back surface of the diaphragm to form a thin resist layer.

These contaminants on the backside of the device, although not as severe as that on the sidewall of the isolation trenches, also play negative roles in the release of the device. After the SCS is etched through in the final release step, the contaminant layer still keeps the movable part of the device connecting the stators mechanically, resulting in an unfunctional device.

5.2.2 Solutions to the Device Release with Contamination

Some processes, especially physical processes such as sputtering and sputtering-induced particle redeposition, are inevitable in plasma processes. Therefore, in the fabrication of the devices, in addition to the optimization of the etching recipe to have a better control over the physical and chemical reactions, the procedure of the processes should also be arranged appropriately. In this section, efforts are made not only to tune the etching recipes for the reaction control, but also to create some additional processes to

minimize or avoid the contaminations on the device surfaces. These solutions to the contaminations are addressed in the sequence corresponding to that in the last section.

5.2.2.1 Surface debris prevention

As described in the last section, the sources of debris on the front surface include the dirty chamber wall and the exotic materials around the device chip, mainly photoresist in this device fabrication. The polymer accumulated on the chamber wall not only affects the etching process by changing the composition of the chemical gases, but also generates dusts in the etching that fall onto the front surface of the device, forming the debris mentioned above [133]. When the etcher has multiple users, the different chemicals used by each user just make the contamination worse. Therefore, a clean etcher chamber must be maintained in any plasma etch. Due to the heavy load of the facility usage in this research work, the chamber of the SiO_2 etcher should be physically cleaned with acetone every two weeks. Moreover, before and after each etching run, additional oxygen plasma cleaning of the chamber helps to scavenge the micro polymer dusks in the chamber. Before the sample is loaded, running a dummy sample with the actual recipe is an effective method to get some particles pinned in their original positions.

5.2.2.2 Sidewall contamination control

As described in last section, the main obstacle to the successful release of the device is the sidewall contamination of the isolation trenches. Both chemical and physical measurements have been taken to minimize or remove this type of contamination which mainly originate from the anisotropic SiO_2 etch.

As shown in Figure 2-8(a), the thick inhibitor film left from the SiO_2 etch also acts as a mask in the final comb finger etch. It has a screening effect on the SCS underneath the film. The chemical method includes mainly the SiO_2 etching recipe tuning to reduce

the fluoride polymer inhibitor generated on the sidewall of isolation holes. By optimizing the flow rate ratio of CHF_3 and O_2, both acceptable etching rate and minimum inhibitor generation can be achieved. This effort has already been shown in Figure 2-8.

It is difficult from the front side to chemically remove the contaminants accumulated on the sidewall at the bottom of deep isolation trenches. An additional Si anisotropic etching step is added to remove the contaminated area from the backside. To do so, the silicon diaphragm should be left thicker than the intended thickness in the first backside Si DRIE as shown in Figure 3-5. Since the accumulated contaminants normally exist at the lower part of the isolation trench with a few microns from the backside of the device, to keep the final structure thickness as 50μm, approximately 60μm diaphragm should be left after the first backside silicon etch. Right before the last DRIE step for the final release of the device, the chip is flipped over and glued on a clean carrier wafer with tiny amount of photoresist. The surface of the substrate frame is protected with photoresist after the device backside is cleaned in an ashing oven. Normal Si DRIE using Bosch process is then performed on the back side to etch a few microns of the diaphragm. During this additional etch step, most of the fluoride polymer accumulated close to the back side surface on the sidewall of isolation trenches is removed. The very small amount of remaining aluminum compound is sputtered by the ions to distribute through the backside surface, losing the function as micromask. In addition, due to the larger exposure area, the edges of the isolation trenches are cut and a V shape groove is formed at the entrance of an isolation trench from back side. This V shape profile is beneficial to the final release of the device from the front side. Figure 5-10 illustrates the additional Si DRIE process on the back side and the comb fingers after the final release etching step.

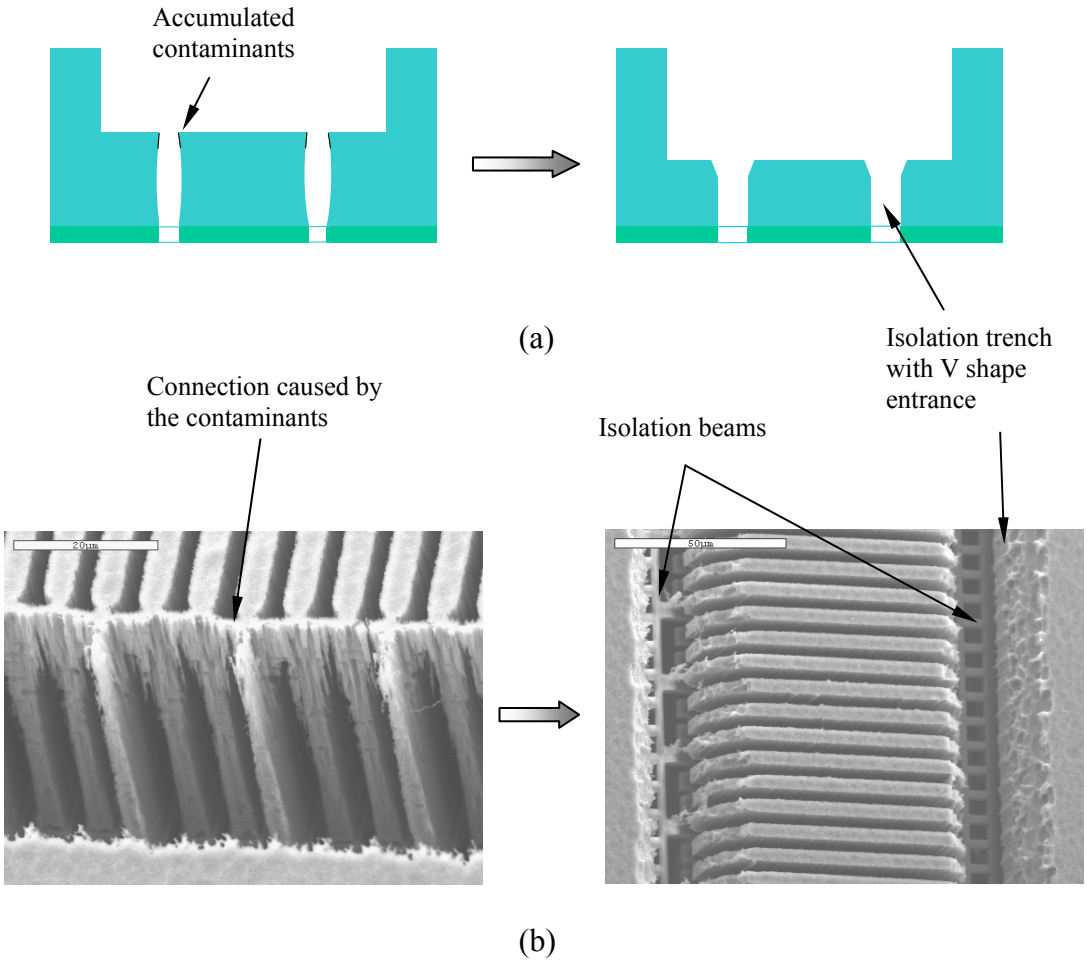


Figure 5-10. Fabrication method using additional etch on backside. (a) schematic of the function of the additional backside Si DRIE, (b) comb fingers released without and with the additional backside etch.

With the additional backside Si DRIE, the contaminants are removed and the chance of the successful device release is increased greatly. This is achieved at an expense of the reduced electrode area of the parallel capacitors due to the formation of the V shape isolation trench, which cuts the comb finger ends close to the back surface. According to the device dimensions, it is estimated that the total capacitance will reduced

by 3% due to the corner cut. For the lateral sensing element in the 3-axis accelerometer, the total capacitance for each lateral axis is as high as 400 fF, a 3% reduction of the sensing capacitance only causes very limited performance drop.

5.2.2.3 Backside surface contaminant removal

As mentioned in the last section, the additional Si DRIE performed on the backside of the device right before the final release step also helps to provide a clean back surface. Before this Si DRIE, the back surface can be pre-cleaned in an oxygen plasmas asher to remove most of the organic compounds degassed from photoresist. The following DRIE process removes the other micro particles. Since the particle contaminants generated by the ion back scattering are relatively small, even though they can not be etched, they will lose the function as a mechanical connection after the final device release.

5.3 Thermal Effect in the Device Release

With a different mechanism, there exists another physical effect – thermal effect, which frequently causes the release failure of the 3-axis accelerometer. It is observed that normally this severe effect takes place on the suspended MEMS structures during the silicon DRIE of the final device release, more exactly, during the overetch period after the etch reaches the ‘ending point’. The result of the effect is the severe lateral undercut on narrow suspending structures, which consequently results in device failure. Through extensive experiments, it has been unveiled that this lateral undercut is different in mechanism from the one tuned by changing the etching/passivation ratio in regular silicon DRIE described in Chapter 2. Since this thermally-caused failure mechanism on suspended MEMS devices is prevalent, great attention must be paid to it in the creation of related MEMS design rules. In this section, the mechanism of this overheat caused lateral undercut on suspended MEMS devices is discussed and an effective fabrication technique

has been developed to avoid this damaging thermal effect. A simplified lumped model has been created to estimate the temperature rise on the suspended z-sensing block, which is the real reason for the larger undercut.

5.3.1 Mechanism of the Undercut Caused by Thermal Effect

Figure 5-11(a) shows the severe undercut on a torsional spring of z sensing element after the device is released. The 3μm-wide torsional spring of the z sensing element was undercut approximately by 0.85μm on each side, leaving the width of the SCS on the spring only less than 1/3 of the designed value. This undercut on the torsional springs changes the mechanical performance of the device dramatically. What is worse, in many cases with only seconds of more overetch, the SCS on the springs was undercut completely, resulting in a broken thin-film beam. A similar phenomenon was also observed on the electrically isolated rotor sensing fingers of the lateral sensing elements. In another experiment, after an overetch period of 30 seconds with the standard SCS DRIE recipe described in Chapter 2, the lateral rotor fingers connecting to the proof mass of the lateral sensing element are completely etched away, as in Figure 5-11(b).

As mentioned above, this lateral undercut is different in mechanism from the normal undercut caused by the large etching/passivation ratio in Bosch process. The evidence is that under the same etching condition, the right part in Figure 5-11(a), which is the proof mass of the lateral element where the z element is embedded, has no apparent undercut on the sidewalls. Similarly, the stator fingers in Figure 5-11(b) keep in good shape after the overetch while the rotor fingers are completely etched.

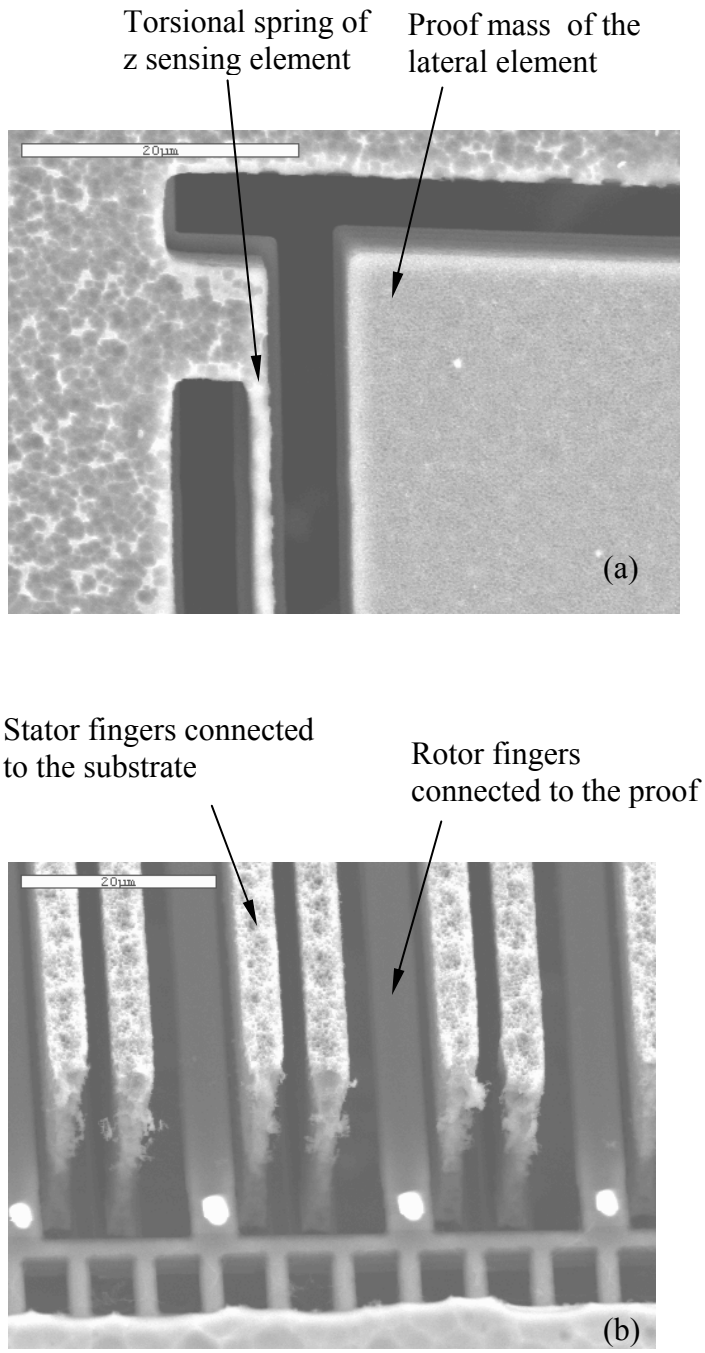


Figure 5-11. Undercut caused by the overheating of the structure. (a) undercut of part of a z-axis torsional spring, (b) rotor sensing fingers of a x-axis sensing element. SEM images were taken from the back side of the device.

The direct reason for the large undercut rate is the elevated temperature on the suspended MEMS device during the overetch period, which results in increased etching rate. Assuming that in the silicon DRIE of the device release step, the etching rate is determined by the surface reaction rate rather than the reactive radical flux to the etching surface. The general relationship between the reaction rate and surface temperature at the reaction spot is given by the Arrhenius Equation, which reads [134],

$$r = A\exp(-\frac{E}{RT}) \qquad (5\text{-}1)$$

where r is the general reaction rate of a chemical process, E is the surface activation energy, R is the molar gas constant with positive value and A is the frequency constant in the reaction.

Qualitatively, there is a positive feedback among the heat generated in the reaction, the temperature rise of the structure being etched and the etching rate. Once the equilibrium in either step is broken, consequently the reaction rate will increase dramatically. The etching rate as a function of the substrate temperature has been investigated with other materials based on empirical results [135].

To estimate more quantitatively the undercut etch rate increase caused by the temperature rise, a plasma energy transfer mechanism should be investigated to bridge the etching process parameters and the etching rate. To achieve this, it is necessary to have an estimation of the temperature difference between the suspended structures and the substrate during the overetch time.

In a ICP chamber where collisonless Bohm sheath exists, the ion power density $\boldsymbol{P}$, in the unit of W/m^2, can be expressed as [136],

$$P = n_s (\frac{eT_e}{M})^{\frac{1}{2}} \cdot qV_{bias} \qquad (5\text{-}2)$$

where n_s is the ion density, e is the electron charge, T_e is the electron temperature measured in eV (2 ~ 3eV for normal ICP system), V_{bias} is the DC bias on the sheath and M is the mass of the reaction ion.

Here the z sensing element, in which the undercut happens on the torsional springs frequently, is exemplified. Assuming all the kinetic energy of the impingent ions converts into heat which rises the temperature of the z proof mass and the temperature on the proof mass is uniform. The structure is shown in Figure 5-12(a), with dimensions in Table 5-1. The simplified lumped model as shown in Figure 5-12(b) can be used to evaluate the temperature rise. Suppose T is the temperature on the proof mass, T_0 is the temperature on lateral proof mass in which the z proof mass is embedded.

The heat capacitance of the z proof mass can be calculated as

$$C = \rho C_m V \qquad (5\text{-}3)$$

where V is the total volume of the z element. ρ and C_m are density and specific heat of silicon respectively and their values are given in Table 5-1. The thermal resistance of the torsional springs is,

$$R = \frac{1}{2k}\frac{L}{wt} \qquad (5\text{-}4)$$

where L , t and w are the length, thickness and width of the torsional spring, respectively. k is the thermal conductivity of silicon and its value is listed in Table 5-1. The factor of 2 is due to the fact that there are two torsional spring on the z-axis sensing element. It is clear the two torsional springs contribute most of the thermal resistance. Plugging in the

dimension of the z block, the thermal time constant of the system $\tau = RC$ can be calculated as 0.183 second.

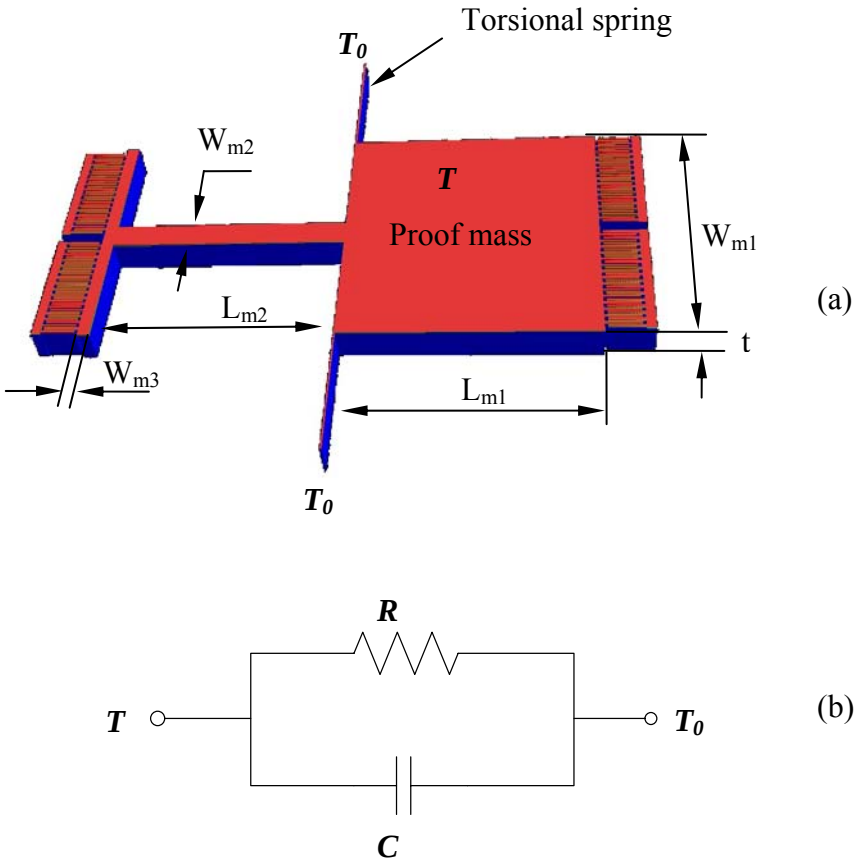


Figure 5-12. Model of the z sensing element for temperature rise estimation. (a) 3D model of the z proof mass, (b) the simplified thermal model.

Table 5-1. Dimensions of the z element and the parameters used in the analysis.

Dimensions or parameters	**Values**
Thickness of the structure (t)	50μm
Torsional spring ($L_s \times W_s$)	400μm×5μm
Proof mass 1 ($L_{m1} \times W_{m1}$)	300μm×700μm
Proof mass 2 ($L_{m2} \times W_{m2}$)	260μm×80μm
Proof mass 3($W_{m1} \times W_{m3}$)	300μm×40μm
Thermal conductivity of silicon (k)	98.9 W/(K.m)
Specific heat of silicon (C_m)	712 J/(kg.K)
Density of silicon (ρ)	2330 kg/m^3

With this short time constant, the system will rapidly reach the steady state once the structure is released. The following equation can be obtained for the thermal current running from the z proof mass to the lateral proof mass through the two torsional springs.

$$\frac{dQ}{dt} = P \cdot A = C\frac{d}{dt}(T(t) - T_0) + \frac{d}{dt}(\frac{T(t) - T_0}{R}t) \qquad (5\text{-}5)$$

Then, the temperature on z proof mass can be expressed as,

$$T(t) = T_0 + P \cdot A \cdot R \cdot (1 - \exp(-\frac{t}{RC})) \qquad (5\text{-}6)$$

Figure 5-13 shows the plot of the temperature change on the z proof mass with respective to the lateral proof mass, where the temperature is set to 50°C due to the backside helium cooling. After the system reaches its equilibrium state once the overetch starts, the temperature difference between the z proof mass and the lateral proof mass can be as high as 148.3°C. This explains why the large undercut was observed on the z sensing block.

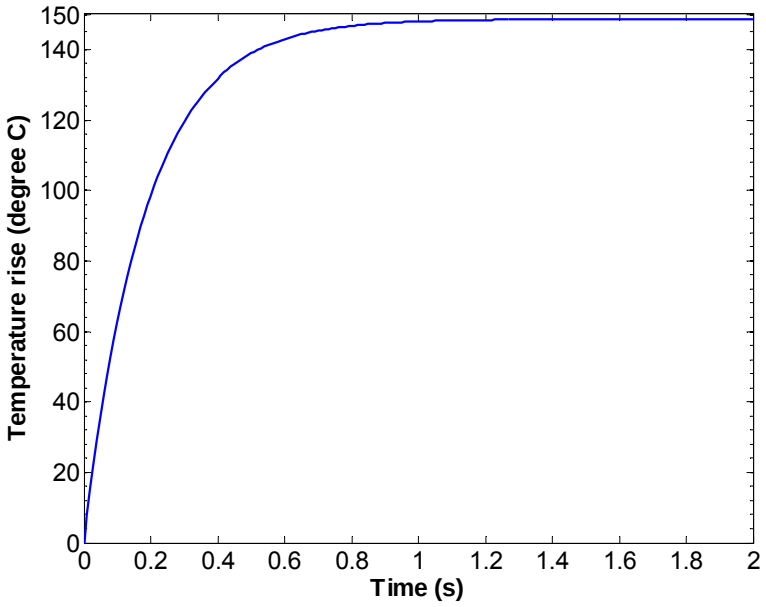


Figure 5-13. Calculated temperature rise on z proof mass.

It should be noted that the abrupt temperature rise on the suspended accelerometer structures only takes place in the overetch period after the structures are released. Before the 'ending point' of etch-through, movable structures are still connected to the substrate through the remaining silicon at the bottom of the silicon diaphragm, which provides a good heat path to prevent the abrupt temperature rising on the structures being etched. Due to the microloading effect and ARDE, structures with different trenches have different etching rates, resulting in their different release points. Structures with wider trenches are etched through earlier than those with narrower trenches. After they reach the ending point first, these structures start to experience an overetch during the remaining etch time for those with narrower trenches. Since the heat path provided by the connecting SCS does not exist any more, the released structures are thermally isolated from the substrate. Therefore, it is in this overetch period that the temperature of the suspended structure rises rapidly, resulting in the fast lateral undercut on all the suspended z proof mass. Figure 5-14 shows another SEM image of the z sensing fingers after the overetch in the release step. More undercut can be found on rotor sensing fingers than on the stators. The reason is that the lateral proof mass, where the stator fingers are connected, has larger thermal conductance to substrate and thus has lower temperature than the z proof mass connecting the rotor fingers. The higher temperature on the z proof mass also increases the etching caused by the radicals back scattered from the carrier wafer, deteriorating the back surface of the suspended z block.

Similarly, on the lateral sensing element in the 3-axis accelerometers fabricated using the proposed new DRIE CMOS MEMS technology, the electrical isolation trenches are first etched. After the sensing fingers are etched through in the final release step, the

silicon on the comb fingers are only connected to the proof mass or substrate through the electrical isolation beams which consist of only thin films of CMOS stacks. The low thermal conductance of the narrow composite CMOS stack also causes the temperature rise on the lateral comb fingers, giving rise to the unique undercut on these fine fingers, as shown in Figure 5-11(b).

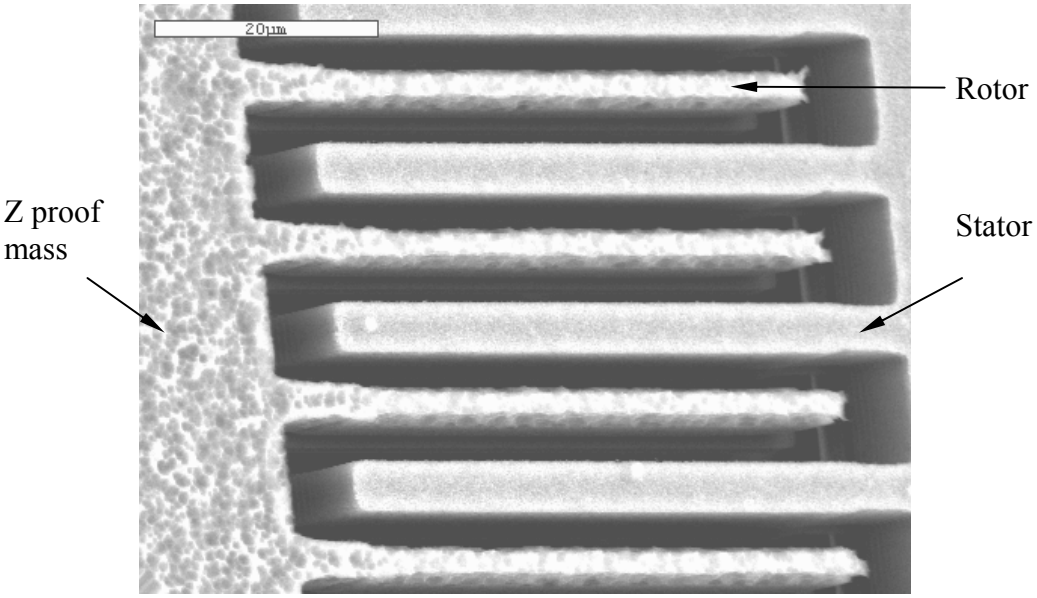


Figure 5-14. Lateral undercut on the rotor sensing finger of z element. The back surface of the z block is also deteriorated due the higher temperature on the block.

5.3.2 Fabrication Method for the Suspended MEMS Devices

The key factor that causes the large undercut on the fine structures of suspended devices is the reduced heat paths from the suspended MEMS structures to the substrate once the device is released. The ultimate solution for this overetch-caused structure damage includes two aspects. The first is the design issue. Microloading and ARDE effect should be very carefully considered in the design stage to assure a proper device release sequence for different types of structures. The suspended fine structures should be

released lastly to avoid the temperature rise on them. The second aspect involves the process monitoring. In device fabrication, if the etching 'ending point' in the release step could be precisely detected, the process could be terminated immediately after the final point was reached to avoid the thermal effect caused device damage. However, the in-situ detection of the ending point requires specific monitoring systems which are unavailable to this research.

The alternate method to overcome the thermally caused device damage described above is to provide additional thermal path for the suspended structures during the short overetch period.

A couple of materials can be used to provide the external thermal path. For instance, a thin layer of metal with good thermal conductivity can be sputtered to the backside of the silicon diaphragm. During the final release step, the sputtered metal layer provides an extra heat path from the suspended structures to the solid substrate. A layer of PECVD SiO_2, even with lower thermal conductivity, can also function as the heat path. However, these additional layers will introduce extra processes and must be removed finally, which complicates the release of the device in another way.

In practical fabrication, hard baked photoresist was employed to provide the external thermal path in the device release. To keep the back surface clean, the photoresist was applied to the backside of the silicon diaphragm right after the first backside DRIE. To withstand the temperature rise in the plasma processes, the photoresist should also be hard baked to avoid any reflow during the processes. After all the fabrication processes are finished, the photoresist can be ashed away in an oxygen plasma asher and simultaneously, the device is released. Figure 5-15 shows the modified

process flow of the 3-axis accelerometer fabrication. It is the same as Figure 3-5 except for the photoresist application after the backside etch in Figure 3-5(a) and the photoresist ashing step in Figure 5-15(f). The photoresist used for backside coating was AZ9260. After the application, it was soft-baked at 90°C in oven for 30 minute and then hard baked at 120°C for 1 hour 30 minutes.

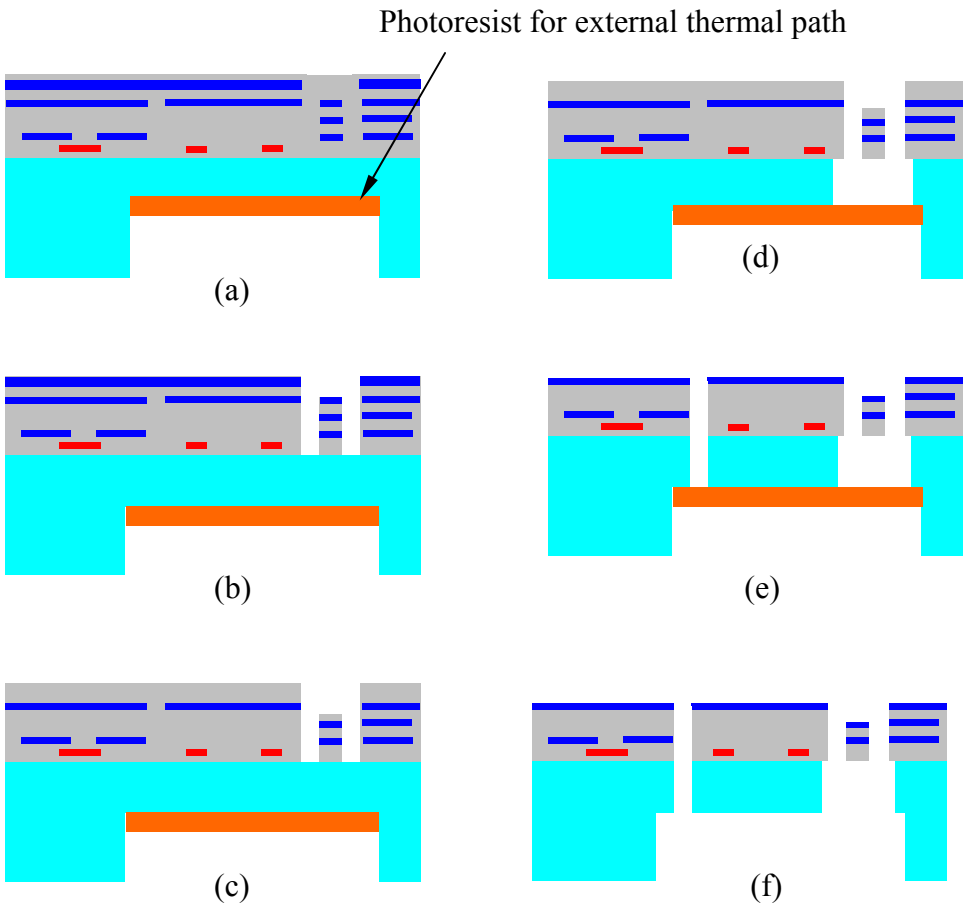


Figure 5-15. Modified accelerometer fabrication process with photoresist coating on backside.

Figure 5-16 shows the backside image of the device after the final Si DRIE. The comb fingers and lateral mechanical springs can be seen through the coated photoresist. It

can also be found that cracks were developed in some area of the photoresist layer. That is due to the relative large thickness of the resist required for enough conductance.

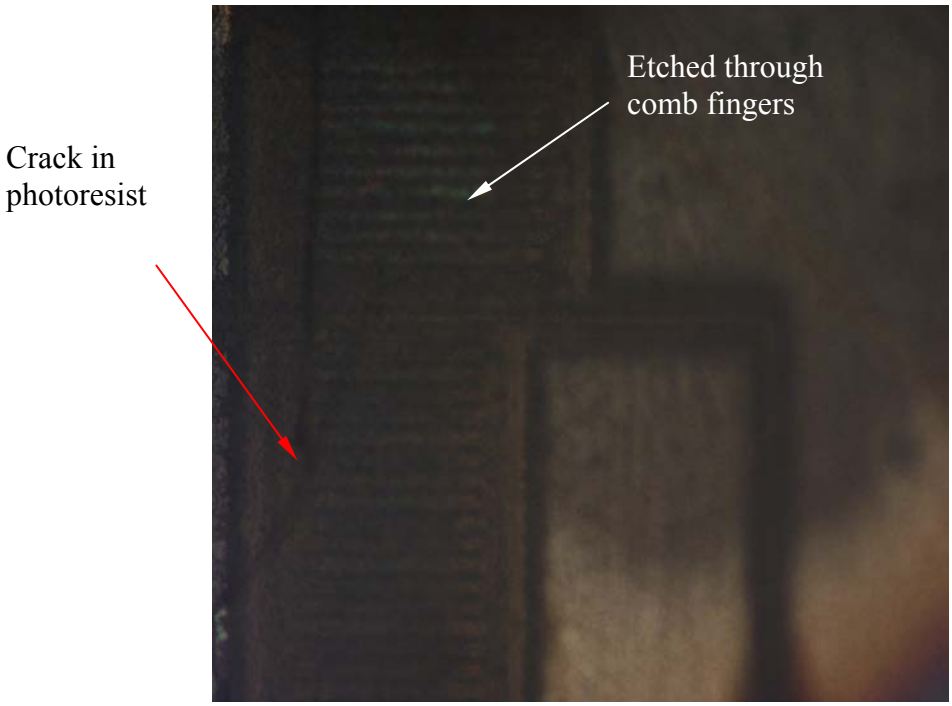


Figure 5-16. Etched-through structures observed through photoresist coated on the backside of the device.

Figure 5-17 is the top view of a fabricated device observed from the backside. The removal of the photoresist completes the fabrication process. Comb fingers and mechanical springs are etched through without apparent undercut, as shown in the insets. The good release result suggests that this fabrication method with backside photoresist coating is effective to avoid the severe undercut on the suspended MEMS structures during the overetch for device release.

It is noted that due to the footing effect caused by the ion scattering at the interface of the coated photoresist and the silicon on the diaphragm, part of the SCS at the bottom of the structures is etched, leaving a sloped shape on the bottom of the structures. This

can be observed in the insets of Figure 5-17 as well. This effect is similar to the entrance enlargement described in section 5.2 to remove the contamination. Therefore, with backside photoresist coating, the profile of the electrical isolation trenches can also be tuned by ion scattering inside the trenches. This makes the release even easier by redistributing, if not completely removing, the contaminants generated during the multiple etching steps.

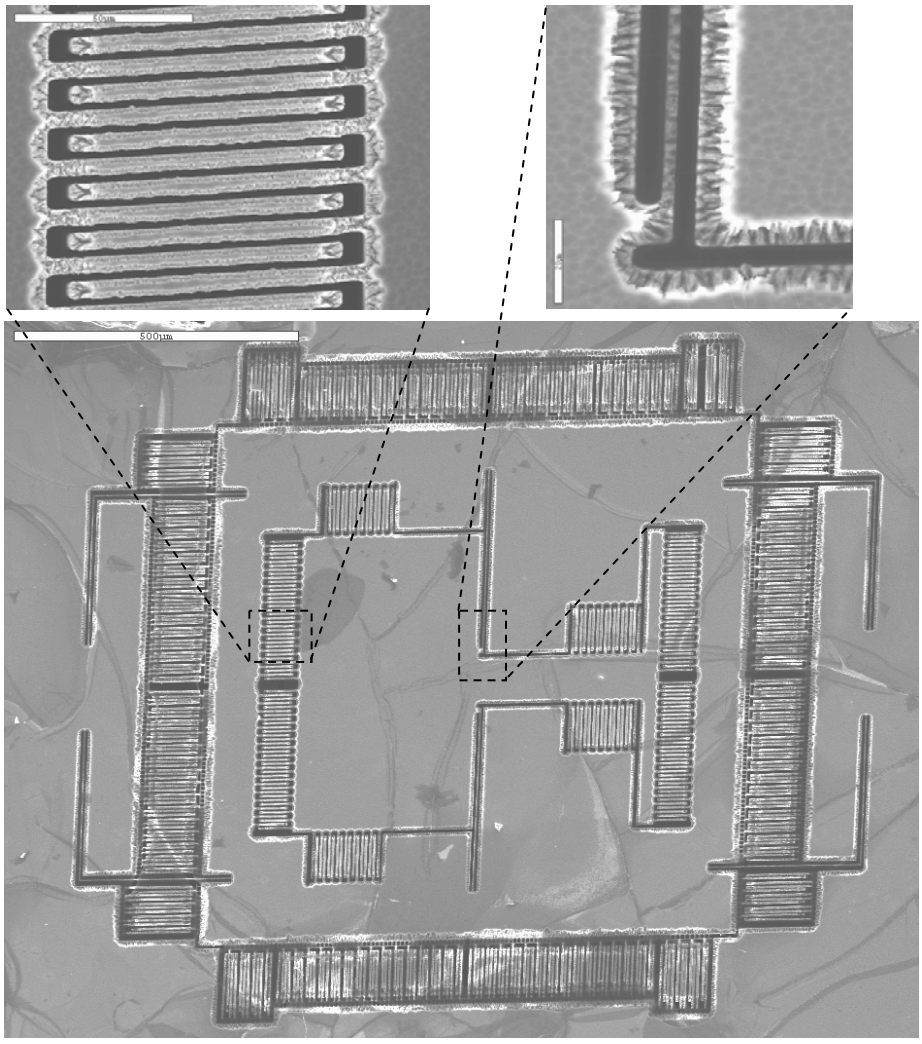


Figure 5-17. Fabricated device with most structures released. The structure damage caused by the thermal effect is avoided by coating photoresist on the backside of the device.

Since photoresist itself is not a good thermal conductor, other materials with higher thermal conductivity are highly desired. To be used as an additional thermal path in the specific process for the suspended MEMS device release, these materials should also be easily removed without any damage to the MEMS structures after the etch processes. Some thermal conducting polymers could meet this requirement.

5.4 Summary

In this chapter, some practical issues in the fabrication of the accelerometers using the new DRIE CMOS-MEMS process are addressed. These issues include both the common phenomena in plasma etch and the specific problems caused by the particular process steps in the new DRIE CMOS MEMS technology developed. By arranging the process sequence or adding some easy process steps, the device release yield has been greatly increased. The proposed methods to overcome the contamination on the sidewall of the isolation trenches were proven effective. The additional thermal path method is also valid for the fabrication of other suspended MEMS devices that are released by dry etch.

CHAPTER 6
DEVICE CHARACTERIZATION

Both the 3-axis and single-axis integrated CMOS-MEMS accelerometers have been fabricated successfully using the improved DRIE post-CMOS MEMS microfabrication process described in previous chapters. These devices have been tested intensively. In this chapter, the experimental methods are introduced, followed by detailed test results of the 3-axis and single-axis CMOS-MEMS accelerometers. All the tests were conducted in open air. The dynamic tests were performed on a vibration-isolated optical table to eliminate the spurious environmental mechanical vibrations. In total, nine 3-axis accelerometers were characterized. The test results reported in this thesis are from different devices.

6.1 Device Package

To reduce the size of the test boards and minimize the mechanical modes of the boards, the fabricated devices are packaged in 52-pin ceramic leaded chip carriers (CLCC). Accelerometer chips are hand-aligned and glued in the carrier cavities using silver epoxy with minimal misalignment with regard to the package. In chip gluing, it is important to press the solid part of the die uniformly to ensure a flat assembly and help reduce the output offset. Figure 6-1 shows the photographs of one packaged 3-axis accelerometer and the bonded die in which the locations of the accelerometers and other structures are labeled. The die pin-outs and the bonding configuration are given in Appendix B.

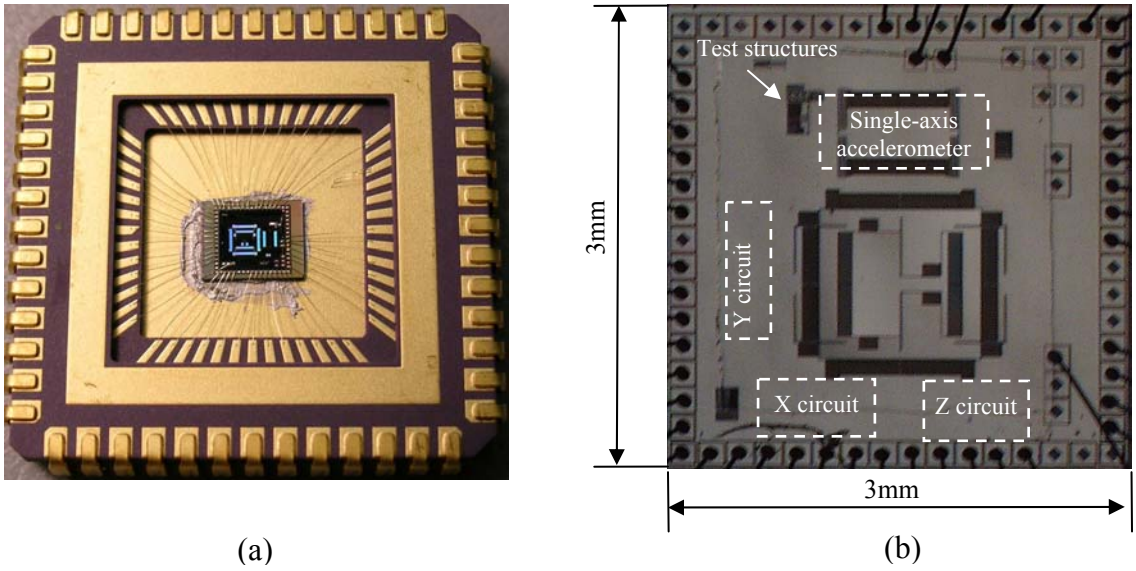


Figure 6-1. Photographs of the packaged device. (a) Device packed in CLCC-52 carrier, (b) bonded die showing the locations of the devices.

The packaged devices are mounted on a test printed circuit board (PCB) through a 52-pin plastic leaded chip carrier (PLCC) socket. To further reduce the mechanical modes, the test PCB board is split into a mounting board and a supporting board. They are connected to each other by detachable soft parallel wires, as shown in Figure 6-2.

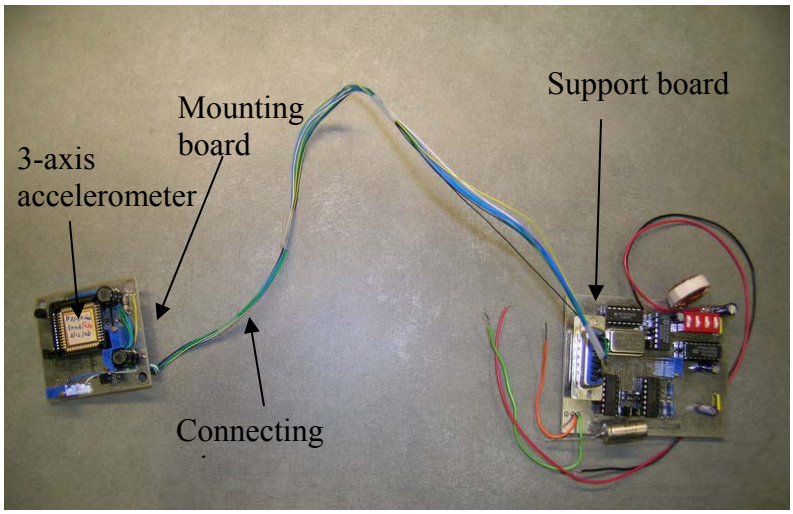


Figure 6-2. 3-axis accelerometer test PCB board.

6.2 Test Setups

The facilities and instruments used in the comprehensive tests of the fabricated CMOS-MEMS accelerometers include a rotary table, a vibratory shaker and their controllers; network spectrum analyzer for noise measurement; and other general bench-top instruments for electrical measurement. A Polytec laser vibrometer is employed for the mechanical test (resonant frequency) of the z-axis accelerometer. Commercial reference accelerometers are used for the purpose of device calibration. The motion generation devices and electrical instruments used in the accelerometer characterization are tabulated in Table 6.1.

6.3 3-Axis Accelerometer Test Results

The characterization of the fabricated devices can be categorized into quasi-static test, dynamic test, noise measurement, mechanical test (resonant frequency), temperature test and process verification. In this section, the 3-axis accelerometers test results are presented separately before the summary of the device performance. Due to the process variations, the fabricated devices have slight dimensional variations as compared to the designed values described in Chapter 3. The tested devices come from the same fabrication batch. There was approximately 0.2 μm undercut on the sensing comb fingers and mechanical springs. The thickness of the sensor was about 37±2 μm. These process variations were considered in the calculation of theoretical device performance. Other microstructure dimensions are listed in Table 4-4.

Figure 6-3 shows some microstructures on a released 3-axis accelerometer, with typical process variations described above.

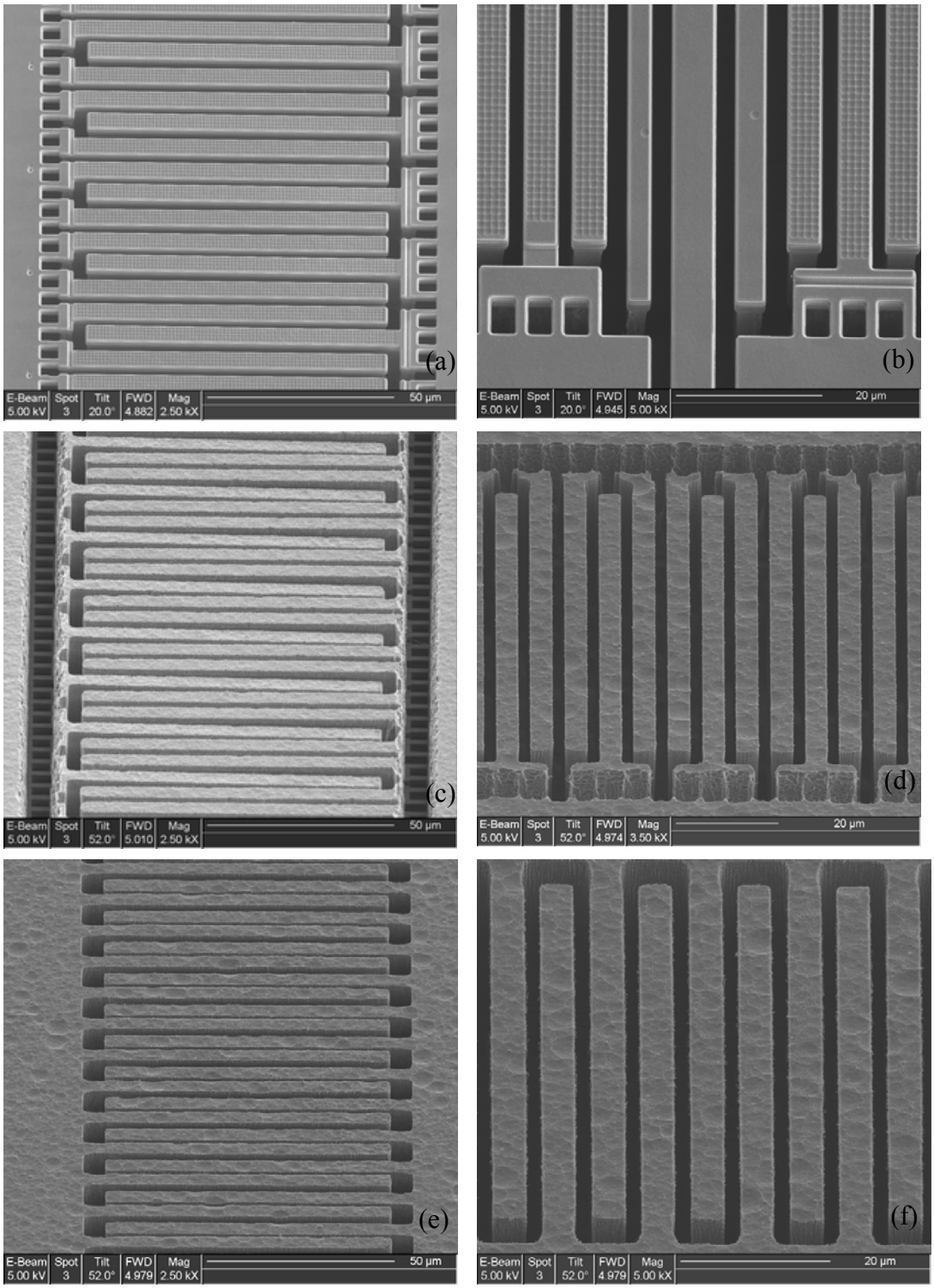


Figure 6-3. Sensing comb fingers on a 3-axis accelerometer. (a) and (b), Front side view of the lateral fingers with a 52° tilting angle; (c) and (d), Backside view of the lateral fingers with a 52° tilting angle; (e) and (f), Backside view of z-axis fingers with a 52° tilting angle.

Table 6.1. Instruments and setups for the characterization of fabricated accelerometers.

Item Name	**Maker and Model**	**Specifications**
Rotary Table and Controller	Klinger Scientific, CC1.1	Resolution: 0.002°
Vibratory Table + Power Amplifier	Ling Dynamic Systems, V408 + PE 100	Frequency range: 5 Hz ~ 9 kHz; Maximum acceleration: 50 g.
Vibratory Table + Power Amplifier	Bruel & Kjaer, Mini shaker Type 4801 + Amplifier Type 2718	Frequency range: DC ~ 18 kHz; Maximum acceleration: 550 m/s^2 (~55g).
Hand-held Shaker	PCB Piezoelectronics, 394C06	1 g acceleration at 159.2 Hz.
Network Spectrum Analyzer	Stanford Research Systems, SR785	Dual-channel; Bandwidth: DC~102.4 kHz; Dynamic range: 90 dB.
Oscilloscope	Tektronics, TDS-2014	4-channel; Bandwidth: 100 MHz; Sampling rate: 1GHz/sec.
Reference Accelerometers + coupler	Kistler, Accelerometer: 8638B5; 8702B50; Coupler: Type 5118B2	8638B5 Acceleration range: ±5g; Nominal Sensitivity: 979mV/g; Resonant frequency: 9.0 kHz, Accuracy: 1.0%. 8702B50 Acceleration range: ±50g; Nominal Sensitivity: 100.4mV/g; Resonant frequency: 54.0 kHz, Accuracy: 1.7%.
Laser Vibrometer	Polytec, OFV3001 Scanner control: MSV-Z-040	Displacement resolution (out-plane,) 8 nm.

6.3.1. Mechanical Test Results

The mechanical test of the fabricated accelerometer was performed mainly to identify the resonant frequencies of the device in all three axes. Four methods can be used for the resonant frequency measurement. The first and most convenient one is to use the on-chip self-test unit in which comb drives are designed to drive the accelerometer structures electrostaticly by applying an external driving signal. The resonant frequency

can be directly obtained by sweeping the frequency of driving signal while monitoring the sensor output. In the second method, the structure is electrostaticly driven by external signal as in the first method. But the resonant frequency is obtained by the displacement or velocity measurement, normally accomplished by optical interferometry measurement. The third one is to apply external acceleration directly on the accelerometer, normally by mounting the device on a shaker table, and by sweeping the frequency of the acceleration, resonant frequency can be obtained through the device output. The last one is to apply external acceleration on the microstructure and measure the velocity and displacement response using optical methods.

Although driving comb fingers are designed on the proof mass for the self-test in all three axes, due to the complex and crowded global wiring on the integrated accelerometer chip, driving signal feed-through was observed in the sensor output, which resulted in unreliable frequency response. The mounting board in Figure 6-2 has some unidentified mechanical modes, which prevent method three in last paragraph from being used in the frequency test. We use method two and method four for the resonant frequency measurement.

A Polytec OFV3001S scanning laser Doppler vibrometer is used to measure the velocity and acceleration response of the mechanically driven devices. This model of laser vibrometer is only capable of out-of-plane velocity measurement. Therefore only the resonant frequency in the z-axis is obtained.

Figure 6-4 is the block diagram of the setup for z-axis resonant frequency measurement. To remove the other mechanical modes in the system, a released device chip was directly glued on the end of the mini shaker shaft, as shown in the inset. The

mini shaker (Bruel & Kjaer Type 4810), separately placed on the isolated optical table, was driven through the power amplifier (B&K Type 2718) by the signal generated by the scanner controller MSV-Z-040.

A chirp driving signal with frequencies ranging from 100 Hz to 5 kHz was used to drive the mini shaker. The fiber interferometer OFV-511 generates the input laser beam and receives the optical signal reflected from the sample surface, which contains the motion information of the detected area on the sample. The resulting optical signal is converted to an electrical signal by the laser diode in the interferometer and consequently decoded by the interferometer controller OFV-3001S to obtain the velocity of the sample. With further computation based on the system configuration, other motion signals such as acceleration can be obtained.

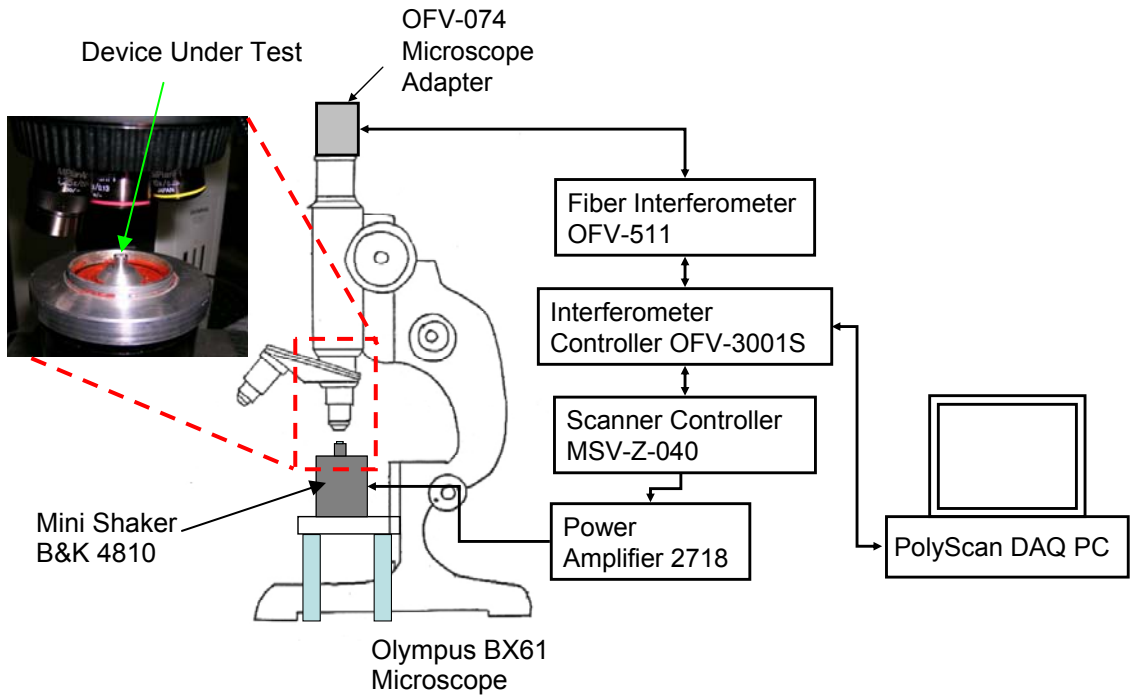


Figure 6-4. Block diagram of the Scanning Laser Doppler Vibrometer setup for z-axis resonant frequency test.

Figure 6-5 shows the scanning area on the z-axis proof mass and the detected acceleration of the proof mass versus the driving frequency. The scanning area consists of totally 66 scanning spots. At each spot, 50 samplings were performed to obtain the average value.

To obtain some more system information, part of the raw data from the above measurement is re-plotted in Figure 6-6, with the detected acceleration expressed in dB. With the resonant frequency of 1497 Hz, the quality factor of the z-axis sensing element is extracted as approximately 11, which indicates a low damping coefficient. This is exactly the case in the z-axis sensing structure where Couette damping of the vertical comb fingers has a smaller damping coefficient compared to the squeeze-film damping in lateral sensing elements.

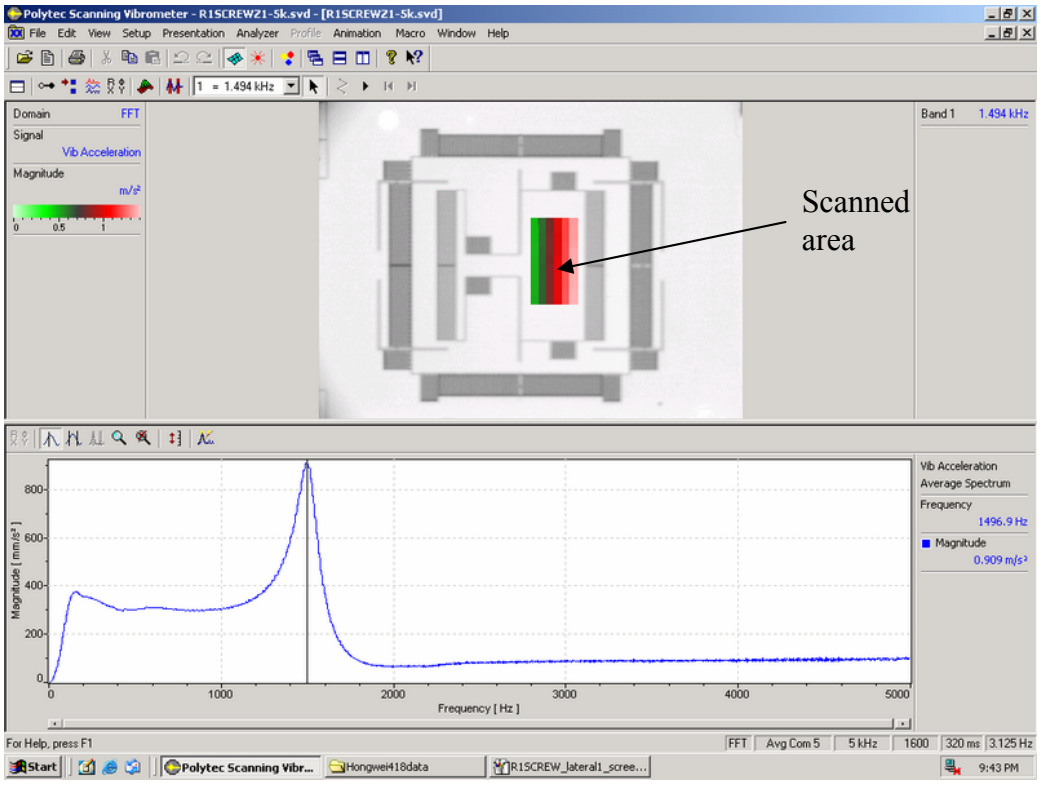


Figure 6-5. The scanning area on the z-axis proof mass and the frequency response of the motion in the scanned area.

Since no in-plane displacement measurement facility was available locally, the resonant frequencies in lateral axes were not performed.

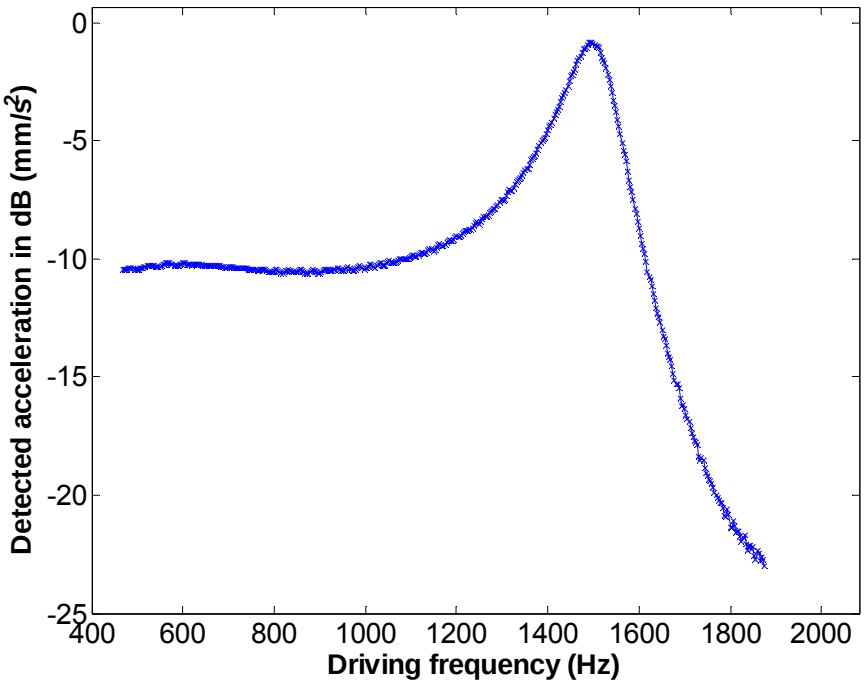


Figure 6-6. The detected acceleration versus driving frequency around the z-axis accelerometer resonant frequency.

6.3.2. On-Chip Circuit Test[137]

A replica of the two-stage, dual-chopper amplifier used for on-chip signal amplification was integrated on the same chip for the purpose of sole circuit characterization. This circuit was tested without the sensor release. With a 3.3V power supply voltage of 3.3V, it dissipates 300μA current, resulting in a power consumption of 1 mW. The measured gain of the on-chip amplifier is 44.5 dB, and a load capacitor of 1 nF is employed to form a low pass filter. The tested 3-dB bandwidth is 1.5 kHz. The noise performance of the circuit is addressed in Section 6.3.4.

6.3.3. Quasi-Static Response

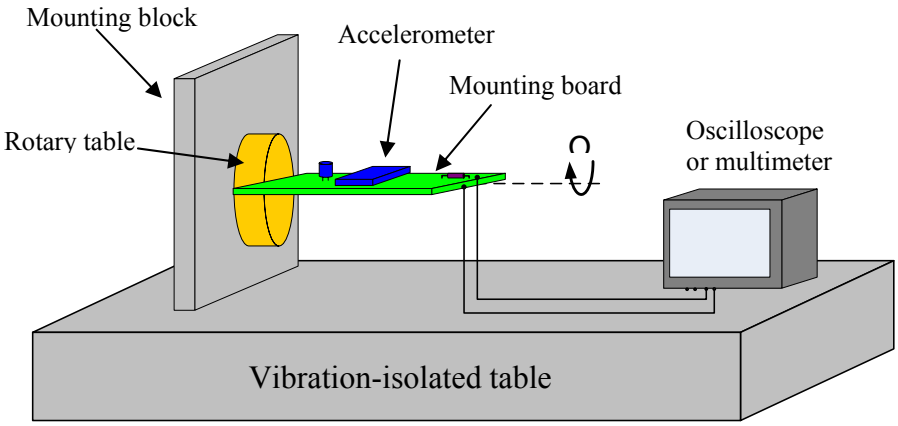
By rotating the device under test (DUT) 180° about certain axis, ±1g gravitational acceleration in the orthogonal axis will be applied to the DUT. For instance, suppose the DUT is rotated about the x-axis, if the rotation starts from y-plane, by rotating the DUT 180°, ±1 g acceleration in the y-axis can be applied to the device. The linearity and sensitivity of an accelerometer can be examined by performing the device rotation which generates ±1 g gravitational acceleration. It is a quasi-static process in which the sensor outputs are recorded at uniformly distributed rotation angles.

Figure 6-7 shows the diagram and photograph of the quasi-static test setup. The device mounting plate is perpendicular to the rotation plate attached to the rotary table, which is vertically mounted on a rack perpendicular to the surface of the vibration-isolated optical table. The rotary table has an angular resolution of 0.001°, corresponding to approximately 17μg of acceleration resolution.

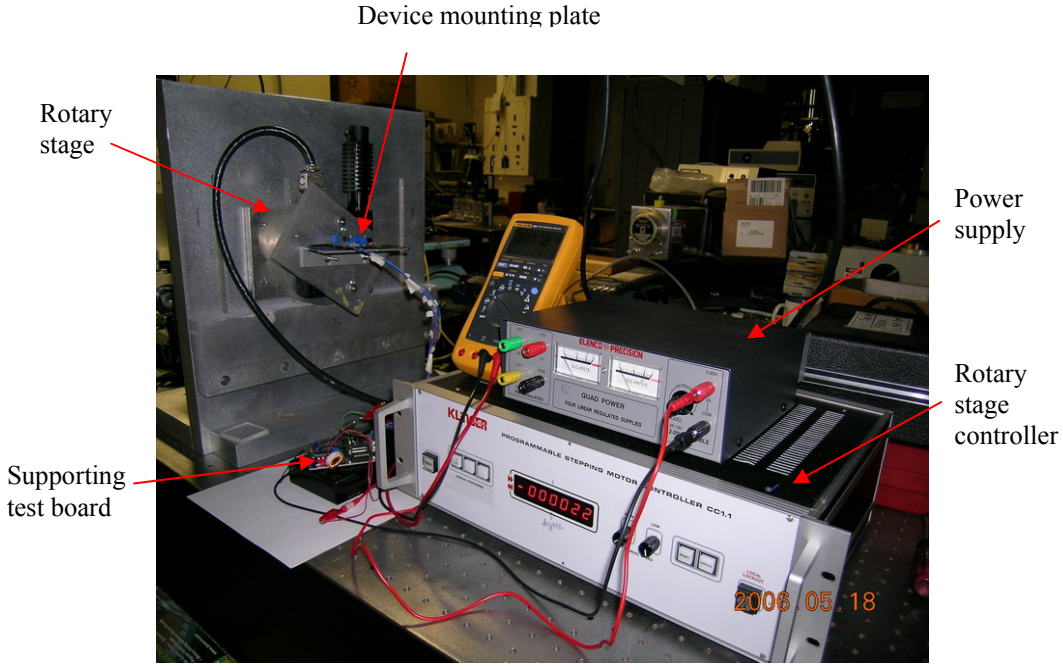
The plots in Figure 6-8 show the quasi-static response of the tri-axis accelerometer in all three axes. With a 1.5V modulation voltage, 560, 460 and 320 mV/g sensitivities are achieved in the y-, x- and z-axis, respectively.

Two versions of circuits were designed for the 3-axis accelerometer [137]. One was used for y-axis sensing and the other was for x-axis and z-axis. The gains of the two circuits are slightly different due to the different configurations of the first and second stage amplifier. In addition to the gain difference between the two versions of interface circuits used for the x- and y-axis, the different mechanical modes between the two sensing elements also contribute to the sensitivity variation. The crab-leg x- and y-axis springs in Figure 4-4 are completely symmetric in both axes. However, due to the

different modes of the embedded z-axis sensing element in lateral directions, which is caused by the imbalanced z proof mass, there is a slight difference in resonant frequencies for the x- and y-axis, which also results in the different sensitivity in these two axes. Less than 0.35% of non-linearity is achieved in both lateral axes.



(a)



(b)

Figure 6-7. Quasi-static test setup. (a) Block diagram of the system, (b) photograph of the setup.

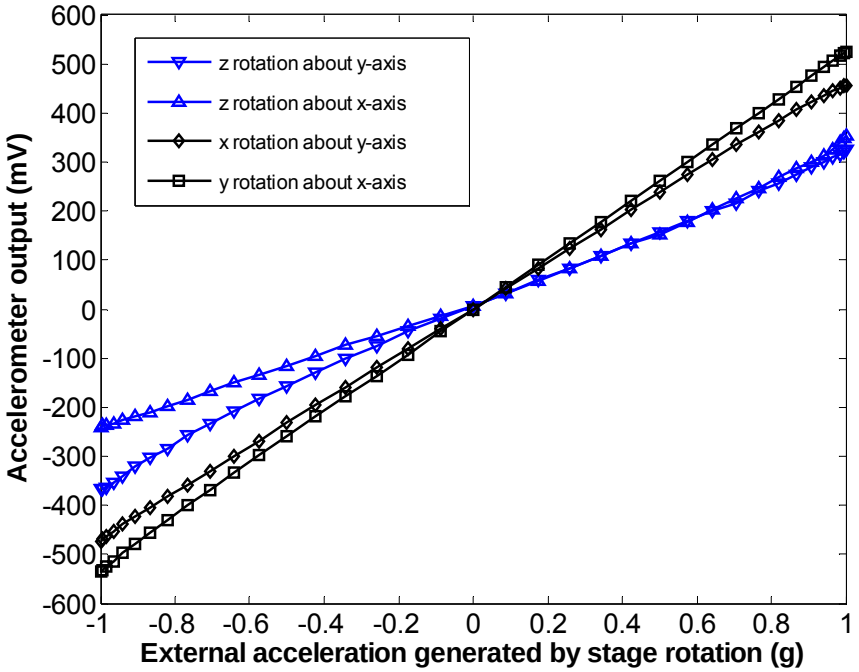


Figure 6-8. Responses of the 3-axis accelerometer to ±1g acceleration.

The device demonstrates different non-linearities in z-axis when rotated about x- and y-axis, as shown in Figure 6-8. The non-linearity is 2.1% when rotated about x axis and 4.7% about y-axis. This non-linearity in z-axis can also be considered as the cross-talk coupling from x- and y-axis when the device is working in an acceleration range of ±1g. Again, this is due to the asymmetry of the z sensing block. The larger value about y-axis is due to the fact that the z torsional spring can also be bent in y direction, which results in the non-linear capacitance change in the z-axis. This trend coincides with the simulated results shown in Figure 4-7.

6.3.4. Noise Measurement

The noise floor of the accelerometer in unit of $g/\sqrt{Hz}$ determines the minimum acceleration the device can detect. It consists of the thermo-mechanical noise of the sensor and the electrical noise from the interface circuit, as shown in Equation 6.1

$$a_n = \sqrt{a_m^{\,2} + a_e^{\,2}} = \sqrt{a_m^{\,2} + (\frac{V_e}{S})^2} \qquad (6.1)$$

where a_n, a_m, a_e are the overall noise floor, thermo-mechanical noise and circuit noise respectively. S is the sensitivity of the accelerometer in unit of V/g and V_e is the input-referred circuit noise measured in the unit of $V/\sqrt{Hz}$. With a dummy self-test circuit designed on chip, the circuit noise and the overall noise can be measured independently. Then the thermo-mechanical noise (Brownian noise) can be calculated using Equation 6.1. The theoretical value of the mechanical noise is expressed in Equation 4.9.

The noise performance of the device was characterized using a SR-785 network spectrum analyzer from Stanford Research Systems. First, the electronic noise from the interface circuit was identified. This was accomplished by measuring the noise floor of the dummy amplifier without a sensor connected. The performance of the 3-axis accelerometer in both x-axis and y-axis was characterized respectively. However, the x-axis and y-axis sensing element have different interface circuits, and only a replica of the y-axis sensing interface circuit was integrated on the chip for the purpose of pure circuit characterization. In the following sections, only the characteristics of the y-axis accelerometer are presented to represent the device performance in both lateral axes.

The noise density measured from the output node of the dummy self-test circuit was 2.7μV/√Hz, as shown in Figure 6-9. With the measured 44.5 dB gain of the on-chip amplifier and a unit gain of an amplifier (AD623 from Analog Device, Inc., used as a buffer), the input-referred noise floor was 16.08 nV/√Hz. For a sensitivity of 560 mV/g, the input-referred electronic noise in y-axis is 4.82 μg/√Hz. With the measured sensitivities in Section 6.3.2, the overall noise floor of the y-axis is 12μg/√Hz at 200 Hz.

The z-axis sensing element has a noise floor of 110μg/√Hz at 200 Hz. Their spectra are shown in Figure 6-10 and Figure 6-11, respectively. As a comparison, the spectrum of the noise floor measured without acceleration input is presented in Figure 6-12. The spectrum was obtained from the same device with a modified sensitivity of 260 mV/g. The same acceleration-referred noise floor was observed compared to that in Figure 6-10.

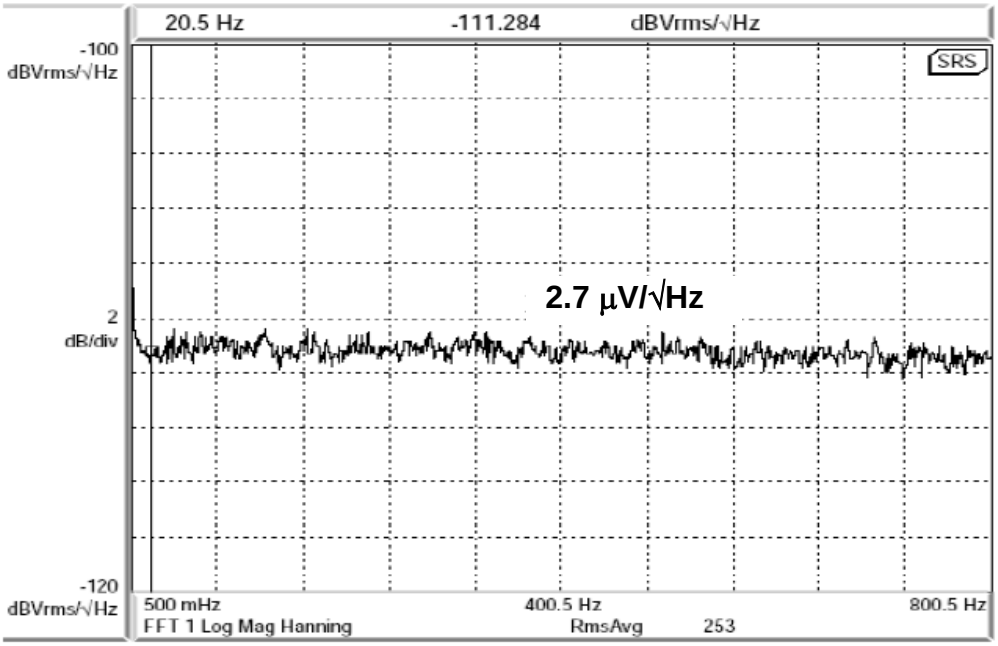


Figure 6-9. Electronic noise density of y-axis interface circuit which has an overall gain of 44.5 dB[137].

From Equation 6-1, the Brownian noise for the y-axis can be estimated as 10.98 μg/√Hz. This noise level is larger than the calculated value of 5.6 μg/√Hz. The reason for the difference is that in the practical accelerometer devices, in addition to the squeeze damping of the comb fingers, material damping and joint damping in the micro structures, especially in the crab-leg mechanical springs, also contribute to the overall damping coefficient, which consequently increase the Brownian noise floor of the device

[138]. Quantitative analysis of these two damping mechanisms is out of the scope of this thesis work.

The dominant damping of z-sensing comb fingers is Couette damping which has much smaller damping coefficient, as described in Section 6.3.1. However, the sensor has much larger noise floor in z-axis. This is mainly due to the much smaller sensing capacitance and the larger electronic noise floor of the interface circuit used in the z-axis sensor.

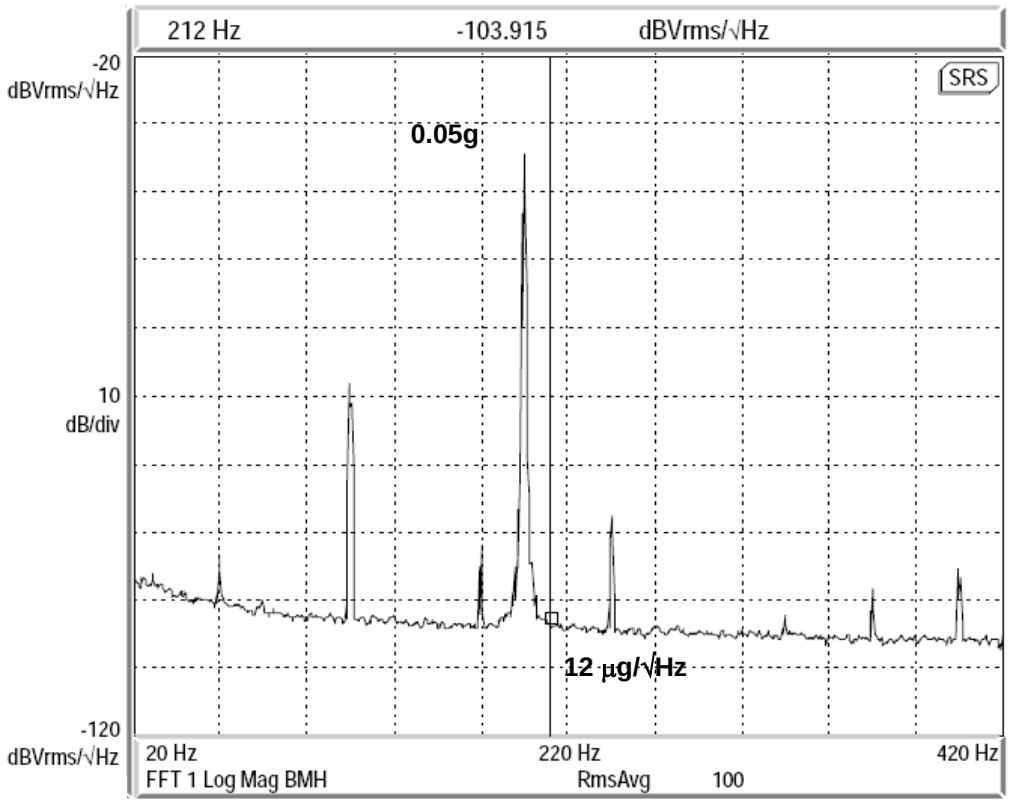


Figure 6-10. The output spectrum of y-axis accelerometer at 200 Hz under 0.05g of sinusoidal acceleration. The sensitivity was 560 mV/g.

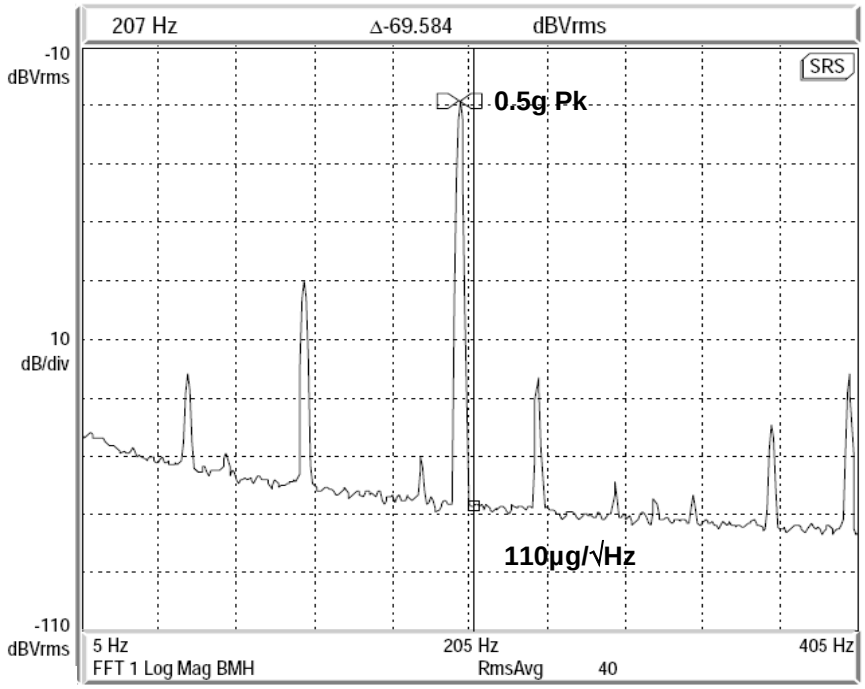


Figure 6-11. The output spectrum of z-axis accelerometer at 200 Hz under 0.5g of sinusoidal acceleration. The sensitivity was 320 mV/g.

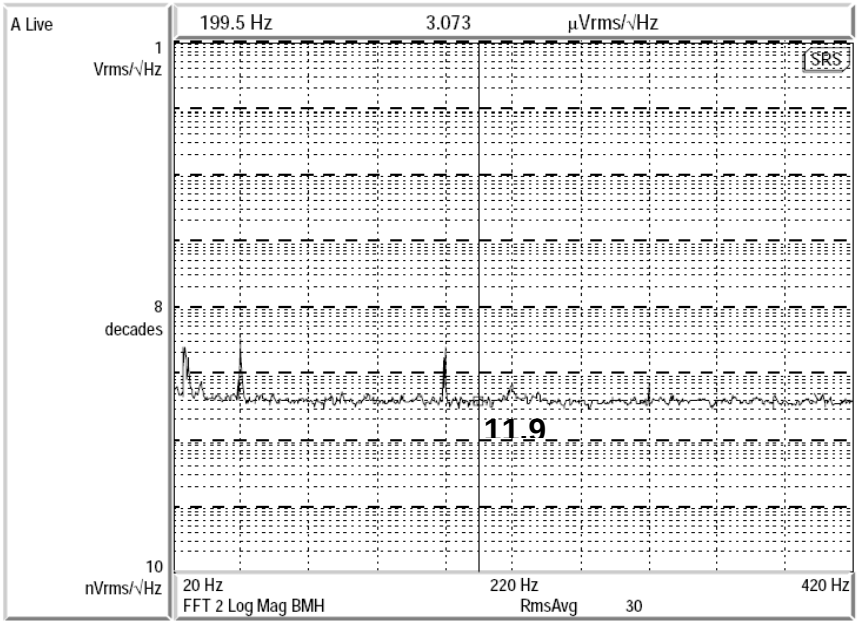


Figure 6-12. The output spectrum of y-axis accelerometer at 200 Hz without acceleration input. The sensitivity tested was 260 mV/g.

The minimum detectable acceleration can be readily derived once the noise floor and bandwidth of the device are determined, as expressed in Equation 6-2.

$$a_{\min} = a_{noise} \cdot \sqrt{BW} \qquad (6.2)$$

With a 1.5 kHz bandwidth, the minimum detectable accelerations in the lateral axis and z-axis are 0.46 mg and 4.26 mg, respectively. If the detectable range is limited by the circuit output swing of 1.65V, the maximum acceleration is about ± 3g. Thus, the theoretical dynamic ranges of the lateral and z-axis can be derived as 76.8 dB and 61.4 dB for a bandwidth of 1.5 kHz. With this noise performance, the 3-axis accelerometers developed in this thesis work can be readily used in physiological monitoring, infrastructure monitoring in civil engineering and security monitoring. If narrower bandwidth is satisfactory, the device can achieve higher resolution.

It is also worthy to examine how sensitive the designed accelerometer is if it is used for displacement detection. Take the lateral sensing element as an example. The lateral sensing element has a proof mass of approximately 86.2 μg. With the simulated resonant frequency of 3.23 kHz, as in Section 4.3.2, the spring constant is derived as 35.5 N·m from Equation 6.3.

$$k = m \cdot (2\pi f_r)^2 \qquad (6.3)$$

Then the minimum detectable displacement can be approximately estimated as Equation 6.4, which gives a value of 1.1×10^{-12} m.

$$\Delta x_{\min} = \frac{m \cdot a_{\min}}{k} \qquad (6.4)$$

This means that the lateral sensing element can detect an extreme tiny displacement of 0.011 angstrom! With the sensing capacitance of 400 fF, from Equation 6.5, the sensor achieves a capacitance resolution of 1.78×10^{-19} F.

$$\frac{\Delta x_{\min}}{x_0} = \frac{\Delta C_{\min}}{C_0} \tag{6.5}$$

With a modulation voltage of 1.5V, the minimum detectable charge will be 2.68×10^{-19} Coulomb. This quantity is merely less than the charges of two electrons!

The above explanation helps in understanding why capacitive sensing has extremely high sensitivity and is widely employed in the design of various sensors.

6.3.5. Dynamic Test

The dynamic test of the 3-axis accelerometers was performed on a LDS shaker table. The tested items include waveform observation, linear response of the device to the swept sinusoidal input acceleration and the inter-axis coupling at 1g orthogonal acceleration. The accelerometer output was measured by a SRS-785 spectrum analyzer, Tektronics 2014 oscilloscope and/or multimeters. Two commercial accelerometers from Kistler, with full sensing range of ±5 g and ±50 g respectively, were used for reference. Before each test, the reference accelerometer was calibrated on-site by a Piezoelectronics 394C06 hand-held shaker, which generates 1g standard acceleration at frequency of 159.2 Hz. An aluminum mounting block was designed to connect the mounting board in Figure 6-2 to the shaker. By mounting the test board on different plane of the mounting block, the accelerometer can be characterized in different axis. Figure 6-13 is the photograph of the mounting block on which both a reference accelerometer and the test board with a 3-axis accelerometer are mounted for the x-axis test.

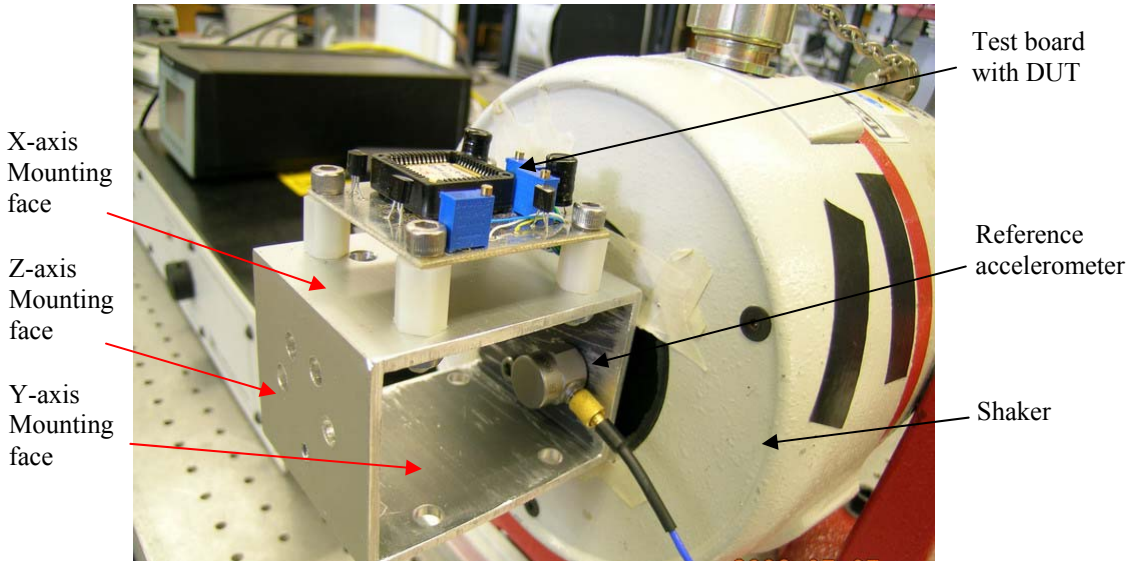


Figure 6-13. Mounting method of the test board and reference accelerometer on shaker table.

6.3.5.1 Waveforms

A waveform is exemplified to show the typical dynamic output of the 3-axis accelerometer. Figure 6-14 shows a waveform of the z-axis response to 1g acceleration at 160 Hz. As a comparison, the waveform of a Kistler 8638B5 reference accelerometer is also included. Clean output waveforms were obtained from the test board.

6.3.5.2 Dynamic ranges

The goal of the dynamic range test is to determine the upper limit of the linear response of the accelerometers. The dynamic range can be obtained once the highest acceleration and the minimum detectable acceleration are known. It should be noted that the upper linear response of the device can either be limited by the circuit or by the mechanical structures in the sensor. As described in Section 6.3.4, with power supply of 3.3V, the circuit has a swing limit of 1.65V. With sensitivities of 560 mV/g and

320 mV/g for lateral and z-axis, the device has upper limit of detectable acceleration of about 3g and 5g. This does not mean that the mechanical structures of the sensor can not response to higher acceleration. In this experiment, by reducing the modulation signal, the sensitivity of the sensor is reduced to allow the sensing of higher acceleration. The upper detectable acceleration limit is determined when the total harmonic distortion reaches 5%.

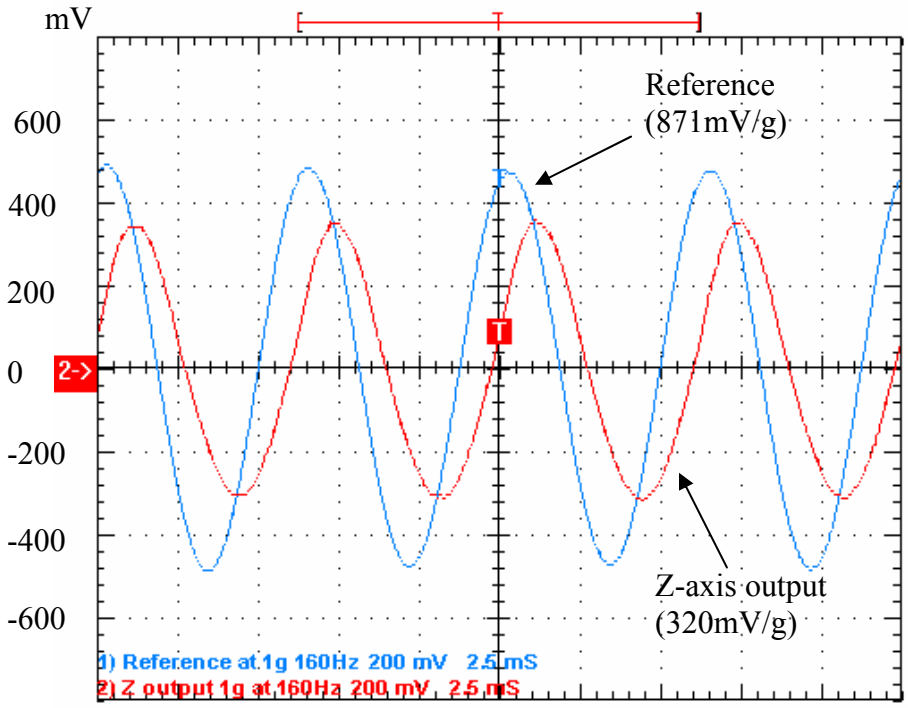


Figure 6-14. Output waveform of a z-axis accelerometer under 1g acceleration at 160 Hz. One grid in the lateral axis stands for 2.5 ms.

Figure 6-15 shows the dynamic response of the accelerometer z-axis. The 50 Hz acceleration generated by shaker table was measured by the reference accelerometer. Due to the stability of the test board mounting, the highest acceleration detected only reached to 34 g. The output still demonstrates an acceptable linearity of 2.1%, which indicates that the mechanical limit for the sensing should be at least 34 g.

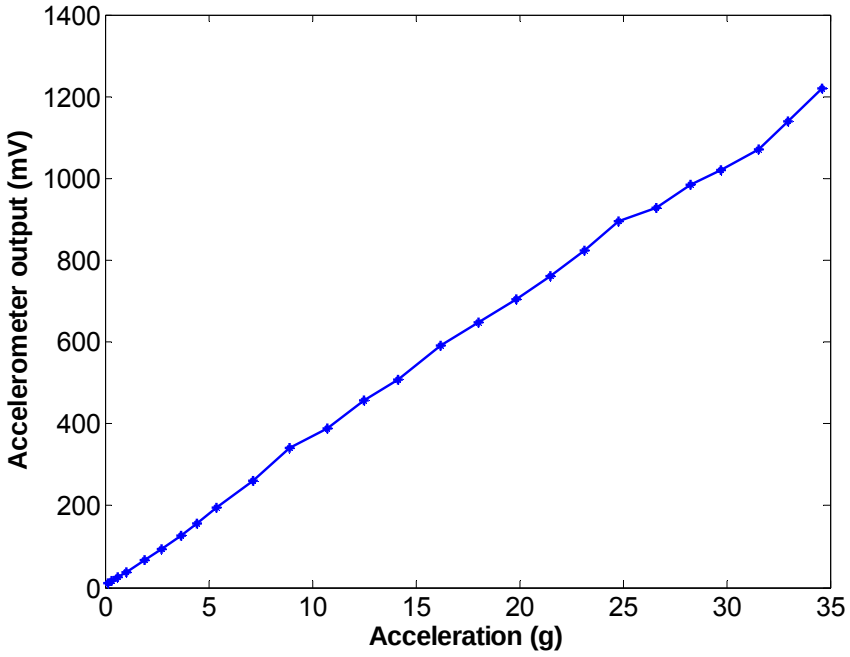


Figure 6-15. Dynamic response of z-axis to 50 Hz sinusoidal acceleration.

In a similar test, by reducing the sensitivity, the lateral axis achieved about 8 g of highest detectable acceleration, which is limited by the amplifier saturation. From the above experiment, it is clear that with the device sensitivity in Section 6.3.4, the upper detectable acceleration is limited by the circuit output swing.

Normally 100 Hz bandwidth is used for the calculation of dynamic range. For the tested device with sensitivities of 560 mV/g and 320 mV/g for lateral and z-axis, the dynamic ranges are then 87.9 dB and 73.4 dB.

6.3.5.3 Inter-axis coupling

Inter-axis coupling between two lateral axes was examined individually by observing the sensor output while a 1g orthogonal acceleration was applied. This was carried out by monitoring the output of reference accelerometer (with a sensitivity of 871 mV/g) and the sensor output simultaneously using the spectrum analyzer.

In Figure 6-16, Window A shows the spectrum of the sensor output in y-axis when 1 g acceleration of 160 Hz is applied to x-axis. The sensitivity in y-axis was calibrated as 158 mV/g. Window B is the spectrum of the reference accelerometer showing the applied 1g acceleration in x-axis. The coupling from x-axis to y-axis can be readily calculated as 2.26%. The same measurement was conducted for the cross-talk from y- to x-axis, resulting in a coupling of 2.38%.

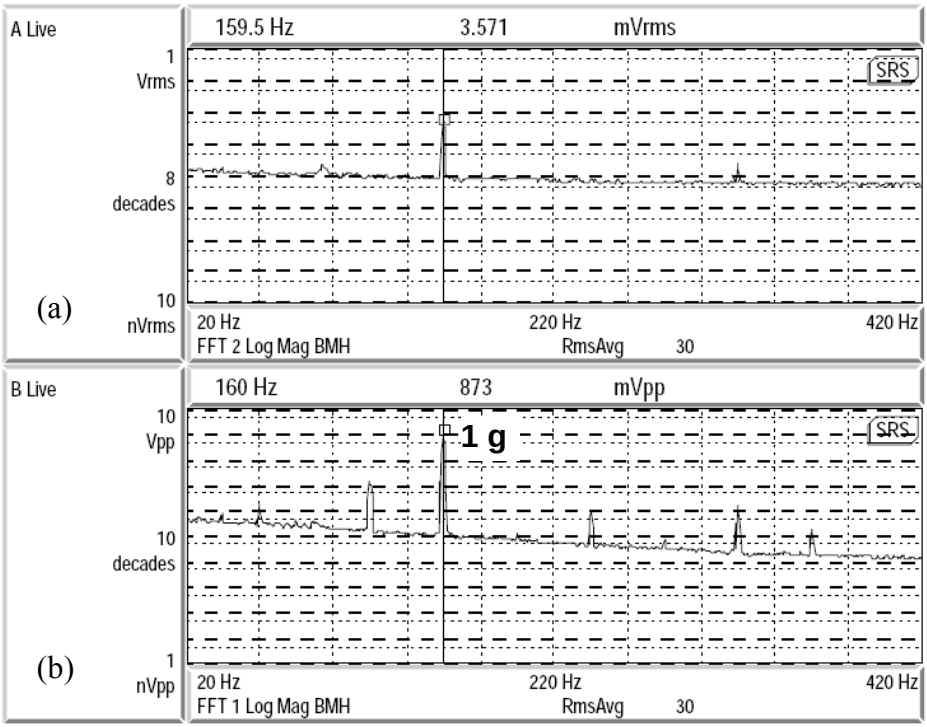


Figure 6-16. Spectrums obtained in the cross-talk test. (a) shows the y-axis output responding to 1g acceleration from x-axis; (b) is the spectrum of the reference accelerometer showing 1g acceleration at 160 Hz in the x-axis.

As introduced in Section 6.3.3, in the static test of z-axis response, 1g acceleration from either lateral axis is coupled to z-axis when the device is rotated about the other lateral axis. Therefore, the coupling of lateral axes to z-axis can be derived from Figure 6-8. They are 2.11% from x-axis and 4.73% from y-axis, respectively.

The measured inter-axis coupling is summarized in Table 6-2.

Table 6-2. Summary of the inter-axis coupling of the 3-axis accelerometer.

	x	y	z
x		2.38%	<0.35%
y	2.26%		<0.35%
z	2.11%	4.73%	

6.3.6. Stability and Temperature Performance

6.3.6.1. Offset drift

Only offset stability in y-axis was observed to evaluate the device stability. The experiment was conducted at room temperature for 48 hours. Figure 6-17 shows the recorded offset drift during the observation, indicating a large unidirectional drift of 54 mV.

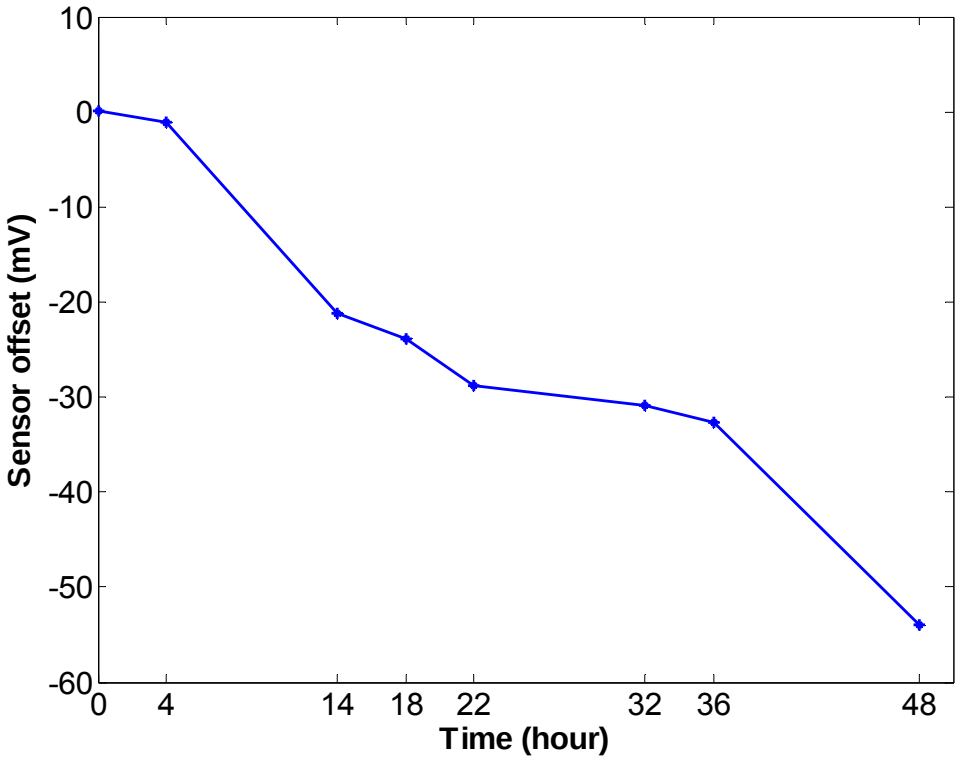


Figure 6-17. Y-axis offset drift observed in duration of 48 hours.

The reasons for the unidirectional drift include the material relaxation in the sensor microstructures, circuit gain drift, power supply drift and environmental variations. Since the package of the device is non-hermetic, the humidity in Florida could most likely be the main reason for the offset drift. To further identify the reasons for the offset drift, hermetic package and strict test environment are need, which is part of the future work on the accelerometers developed.

6.3.6.2. Temperature performance test

A large overall temperature coefficient of sensitivity (TCS) in the lateral axis sensing element was observed. The acceleration sensitivity experienced a 23% reduction when the device was heated from the room temperature (21°C) to 96°C, resulting in a TCS of 3.07×10^{-3}/°C. Simulation of the temperature dependence of the interface circuit and temperature test on sensor structures were performed independently to identify the source of the large TCS. In the circuit simulation, a negative open-loop gain drift of over 10% was observed, which contributes most of the TCS reduction [137].

In addition to the examination of temperature drift of the circuit, the impact of temperature on the sensor microstructures was investigated separately. Due to the thermal expansion coefficient difference and the residual stress, CMOS thin film structures curl up or down with temperature changes. As described in Chapter 3 and Chapter 5, the only thin film structures in the 3-axis accelerometer are the electrical isolation beams in the lateral accelerometers, which connect the sensing comb fingers to the substrate or lateral proof mass, as shown in Figure 6-3(a). These isolation beams have certain temperature coefficients. Once environmental temperature changes, the isolation beams will curl up or down, making the comb fingers that connect to the isolation beams change their positions

in vertical direction. This will directly result in the sensing capacitance change. This is one of the reasons that cause the temperature sensitivity of the accelerometer.

The comb finger curling caused by the temperature variation was investigated by observing the vertical position change of the comb fingers using a surface profilometer. The packaged device was heated to designated temperature points on an isolated stage. The profiles of the fingers were obtained by scanning the surface at these temperature points. Figure 6-18 shows the setup for this temperature experiment.

Four sets of data were acquired at four temperature points: 21°C, 54°C, 71°C and 96°C. Comb fingers from lateral-axes and z-axis sensing elements, including stator and rotor fingers and scanned. Figure 6-18 show the surface profiles of lateral comb fingers on a working device, simultaneously obtained by using a Wyko NT-1000 surface profilometer when the device was heated to 71°C. Figure 6-19(a) shows the curling of a rotor finger and Figure 6-19(b) gives the profile of a stator finger.

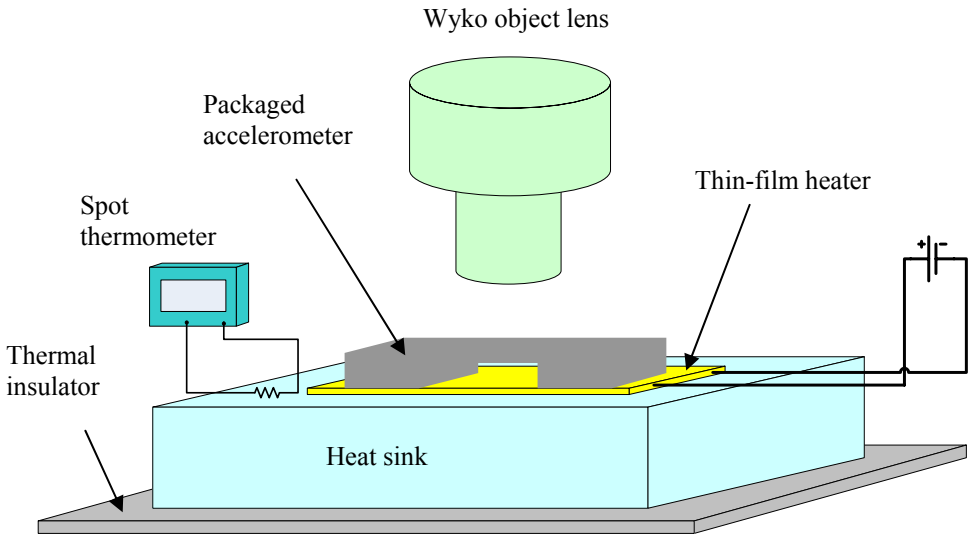


Figure 6-18. Experimental setup for the comb drive curling calibration.

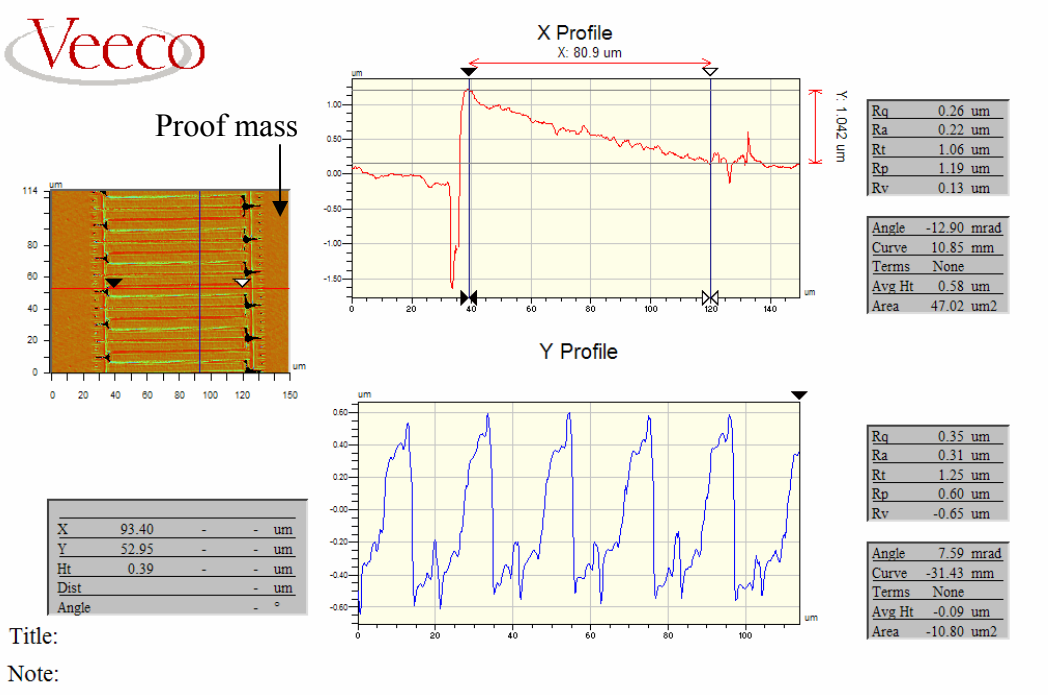
Figure 6-20 shows the plots of curling displacements on lateral and z-axis comb fingers as the function of device temperature. In total, 0.533 μm and 0.065 μm net curling was observed on lateral rotor and stator fingers, respectively.

It is obvious that the rotor fingers have larger curling than the stator fingers. The reason for the difference can be explained as the following. First, in design, the rotor and stator isolation thin films have different patterns, as shown in Figure 6-3(a), resulting in the different temperature dependence of the thin film bending. Second, there is possible large undercut at the end of the rotor comb finger on the proof mass side during the device release. As described in Chapter 5, the undercut difference between the rotors and stators is due to the temperature rise on the proof mass during the overetch in the release process.

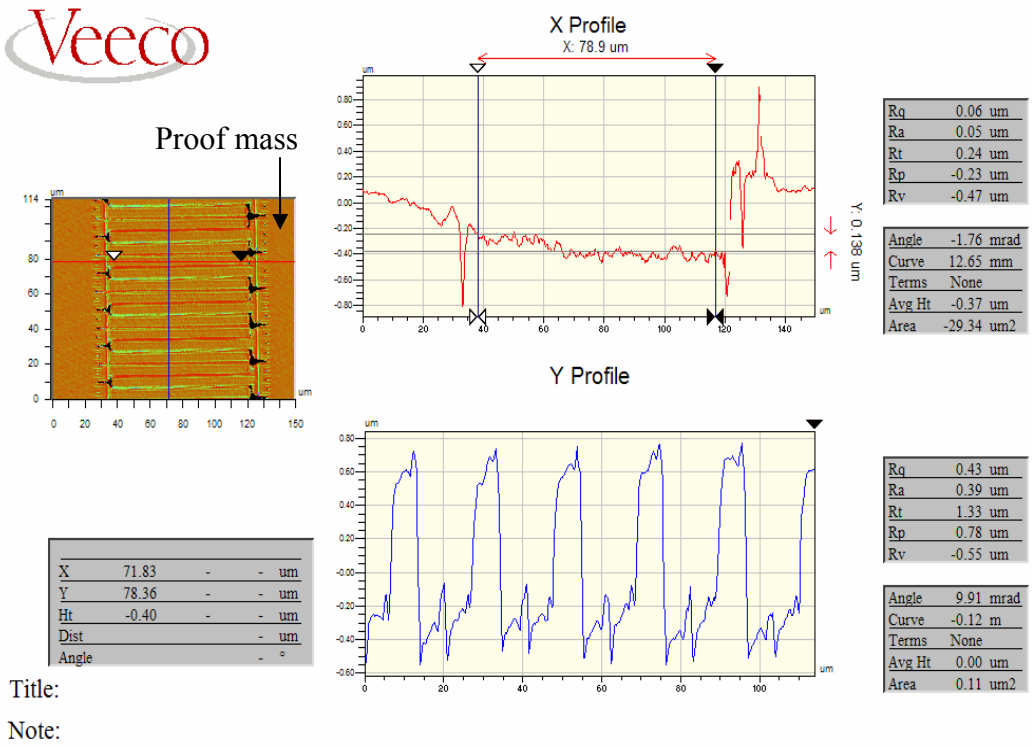
The temperature dependence of the comb finger curling causes the temperature dependence of the sensing capacitance, thus the TCS of the accelerometer. The comb finger curling changes the sensing capacitance by changing the common area of the lateral sensing capacitors. By neglecting the temperature-caused curling of the stator finger, with the comb finger thickness of 37 μm, as given early in this chapter, a positive temperature coefficient of sensing capacitance (TCC) of 9.73×10^{-5}/°C can be derived. The following equations hold.

$$S(T) \propto \frac{\Delta C_s(T)}{C_s(T)} = \frac{C_0 \cdot \alpha T}{C_0(1+\alpha T)} = \frac{\alpha T}{1+\alpha T} \tag{6.6}$$

$$\frac{dS(T)}{dT} = -\frac{\alpha(1-\alpha T)}{(1+\alpha T)^2} \approx -\alpha \tag{6.7}$$



(a) Surface profile of the lateral rotor comb finger.



(b) Surface profile of the lateral stator comb finger.

Figure 6-19. Surface profiles of lateral sensing comb fingers. (a) rotor comb finger, (b) stator finger. The test temperature was 71°C.

where S is the sensitivity of the accelerometer; C_s is the sensing capacitance; C_0 is the sensing capacitance at room temperature; α is the TCC of the sensing capacitance, 9.73×10^{-5}/°C, as given above; and A is a normalized constant. The validation of Equation (6.7) is due to the very small quantity of α in the given temperature range.

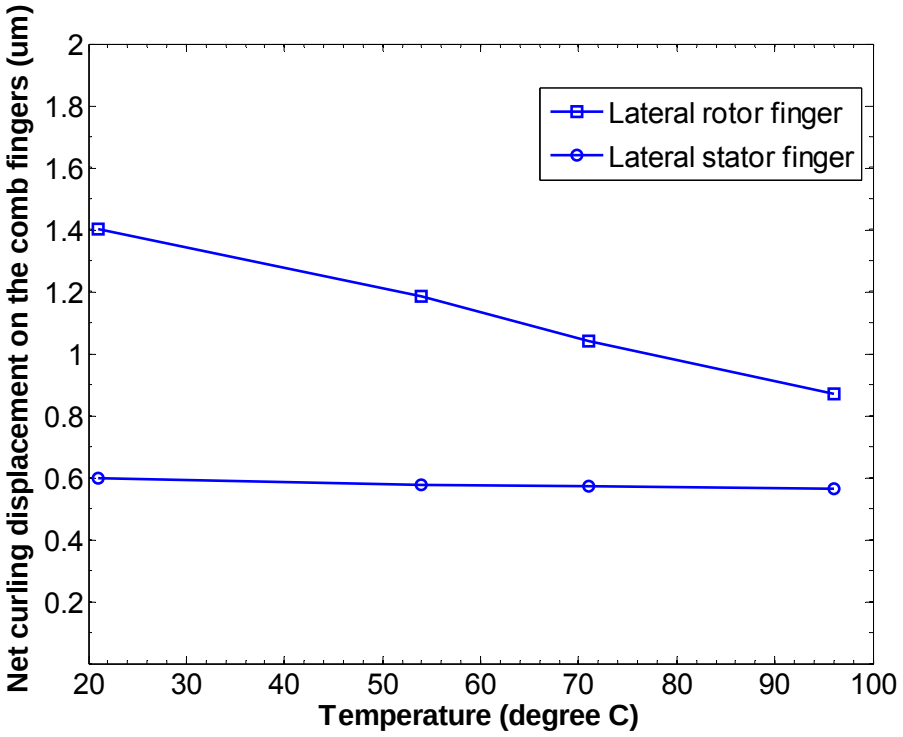


Figure 6-20. Net curling displacements on lateral comb fingers as the function of temperature.

From Equation (6.7), the TCS resulted from the sensing comb finger curling has a small value of -9.73×10^{-5}/°C, which is two orders smaller than the simulated TCS that caused by the temperature-caused open-loop gain drift. Therefore, it can be concluded that the main reason for the large TCS is the large temperature dependence of the open-loop gain in the first stage of the capacitive amplifier.

Since no thin film structure exists in the z-sensing element, in the same experiment, no apparent temperature dependence of out-plane displacement was observed on the z-

axis rotor comb fingers. Therefore, the TCS of the z-axis acceleration is also mainly caused by the gain drift of the interface circuit.

6.3.7. 3-Axis Accelerometer Performance Summary

The main performance of the fabricated 3-axis accelerometer is summarized in Table 6-3. The designed and tested parameters are listed, showing the good agreement between them. As a comparison, the corresponding performance parameters of a mean stream commercial integrated 3-axis accelerometer, ADXL330 from Analog Device, Inc, are also listed [139].

Table 6-3. Performance summary of the fabricated 3-axis accelerometer and a comparison between the this device and the ADXL330 from Analog Device.

Parameter (Unit)	**Designed Value**	**Tested Result**	**ADXL330**
Chip size (mm×mm)	3×3	-	4×4 (with package)
Power consumption (mW)	1.0	0.9~1.0	0.6 ~ 1.15
Lateral-axis mechanical sensitivity (mV/g)	4.5	3.54	-
Z-axis mechanical sensitivity (mV/g)	2.4	2.02	-
Lateral-axis overall sensitivity (mV/g)	450	560	270~330
Z-axis overall sensitivity (mV/g)	240	320	270~330
Lateral-axis noise floor (μg/√Hz)	7.97	12.0	280
Z-axis noise floor (μg/√Hz)	-	110.0	350
Linearity (%)	0.1	0.35 (lateral) 2.11~4.71 (z)	0.3
Bandwidth (kHz)	1.5 (lateral) 0.5 (z)	1.5 (lateral) 1.5(z)	1.6 (lateral) 0.6 (z)
Dynamic range (dB) BW=100Hz		87.9(lateral) 73.4 (z)	-
TCS (%/°C)		-0.307	±0.01
TCO (mg/°C)	-	7.03	±1
Inter-axis coupling (%)		2.26~2.38 (lateral) 2.11~4.71 (z)	±1

The designed and test value on sensitivity and noise floor in lateral axes have good agreement with each other. Except for the temperature performance and inter-axis coupling, the 3-axis in this thesis work has higher sensitivity and resolution than the only monolithic integrated 3-axis MEMS accelerometer available on the market. The large temperature dependence of the fabricated CMOS-MEMS 3-axis accelerometer is mainly due to the high temperature sensitivity of the open-loop gain in the first stage of the interface amplifier.

6.4 Test on The Single-Axis Accelerometer

In addition to the above tests on the 3-axis accelerometer, the single-axis accelerometer integrated on the same chip was tested using the same test setup and method. The quasi-static response and the noise spectrum are shown in Figure 6-21 and Figure 6-22, respectively.

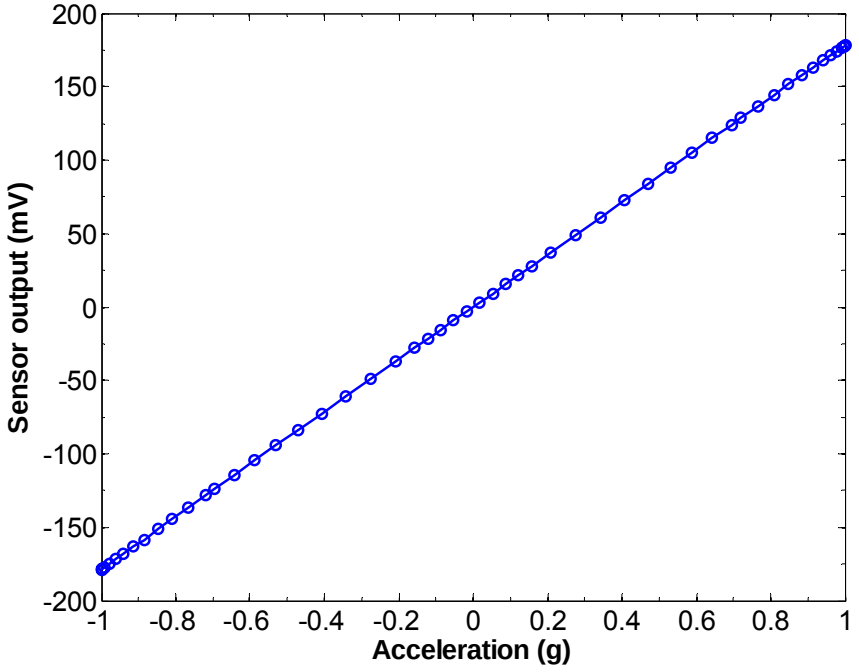


Figure 6-21. Quasi-static response of the single-axis accelerometer. The output instrumental amplifier (INA) on the test board has a gain of 2.

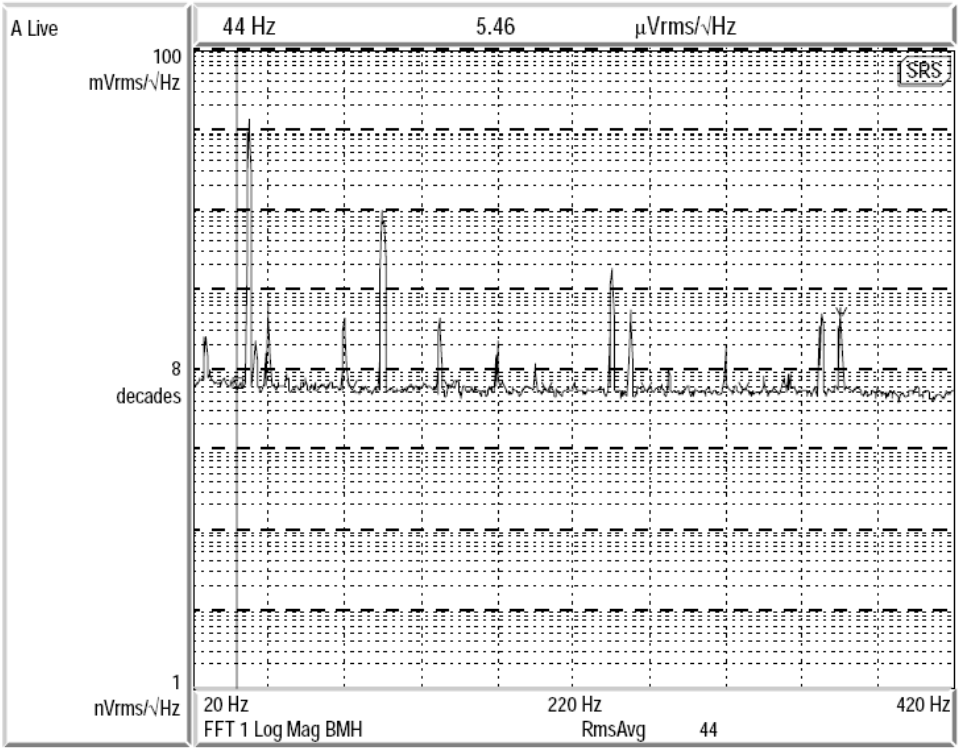


Figure 6-22. Measured noise density of the single-axis accelerometer with a small acceleration input at 50 Hz. A gain of 2 was used in the output INA.

The major parameters of device performance are listed in Table 6-4. The less sensitivity of the device is due to the larger sensing capacitor gap caused by the backside release.

Table 6-4. Performance summary of the single-axis accelerometer.

Parameters	Unit	Designed Value	Tested Value
Sensitivity	mV/g	210	90.1
Linearity	%	-	0.22
Noise floor	µg/√Hz	38.9	60.7
Linear range	g	± 5	± 16
Dynamic range (BW=100Hz)	dB	85.8	88.5
Power consumption	mW	1	1

6.5 Summary

In this section, the experimental setups for the test of the fabricated 3-axis and single-axis accelerometers are introduced and the detailed test results of these two devices are presented. The main performance parameters of the devices have good agreement with the designed specifications. The monolithic integrated CMOS-MEMS 3-axis accelerometer demonstrates small size, high sensitivity, high resolution and good linearity. It has advantages over the mainstream integrated MEMS 3-axis accelerometers in low noise floor, low power consumption and high sensitivity. These features make the 3-axis accelerometer developed in this work a highly desired device in the applications such as physiological/athletic monitoring, engineering monitoring, security and portable electronics.

CHAPTER 7
CONCLUSION AND FUTURE WORK

7.1 Summary and Conclusion

A CMOS-MEMS microfabrication technology has been successfully demonstrated in this thesis work with the accomplishment of both monolithic integrated 3-axis and single-axis accelerometers. The silicon-DRIE based technological process developed in this work can be widely used in the fabrication of sensors and actuators where comb drives are used for capacitive sensing or electrostatic actuation. The 3-axis and single-axis CMOS-MEMS accelerometers fabricated using the developed technology have numerous applications in physical monitoring, engineering monitoring, and most significantly, in portable electronics where low-power and high resolution are required.

Individual process steps in the fabrication technology were tuned to achieve the optimal profile for the micro structures in the accelerometers. Process parameters were extracted as design rules for the design and fabrication of these and other MEMS devices. In the fabrication of CMOS-MEMS accelerometers, by performing the dry etch of electrical isolation structures and the etch-through step for other sensor structures separately, the undercut on comb drives and mechanical springs is minimized, allowing large capacitance for sensing and actuating. This is achieved by using the top metal layer on the device to define the isolation etch holes.

Two device release processes were demonstrated to overcome the inter-process contamination and the over-heating problem to the suspended single-crystal silicon micro structures. In the first release method, the electrical isolation trenches are etched to a

tapered shape from the backside right before the final structure release step. This allows the removal of the contaminants on the sidewall of the isolation trenches for the complete device release. In the other method, a thick photoresist layer is applied to the backside of the structure right after the backside silicon etch. This photoresist layer provides additional thermal paths, allowing the heat generated on the micro structures in the plasma etch transferring to the substrate. The over-heat of the micro structures in the overetch period of the device release step is largely reduced; and the device structure damage resulted from the uncontrollable rapid undercut at high temperature is eliminated.

The CMOS-MEMS 3-axis accelerometer and single-axis accelerometer developed in this work have features of small size, robust structure with single-crystal silicon, high sensitivity and resolution. In the 3-axis accelerometer, the z-sensing element is embedded in the lateral proof mass. This greatly reduces the overall sensor size. 560 mV/g and 320 mV/g sensitivities are achieved for lateral and z-axis axes, with noise floors of 12 μg/√Hz and 110 μg/√Hz, respectively. For a bandwidth of 100 Hz, dynamic ranges for lateral and z-axis are 87.9 dB and 73.4 dB. The single-axis accelerometer achieves a sensitivity of 90.1 mV/g with noise floor of 60.7 μg/√Hz. The non-linearity in all lateral axes is less than 0.35%. A slightly large non-linearity has been observed due to the inevitable inter-axis coupling in the z-axis response. The interface circuit in each axis consumes 1 mW power. Most of the test results demonstrate good agreement with the designed specifications. With these performances and a die size of 3 mm×3 mm, the CMOS-MEMS accelerometers in this work can be widely used in portable electronics and wireless applications for human activity monitoring, engineering monitoring and public

security. An evaluation prototype is under test by a commercial company for security applications.

7.2 Future Work

The future work of this project involves the sensor improvement and process development for large volume fabrication. The sensor improvement includes the circuit improvement, integration of advanced function blocks and mechanical structure design optimization. The current interface circuit has a draw back of large temperature dependence due to the different types of the input transistors in the first stage of amplifier. The modification of the input stage should be the first task to improve the temperature performance of the sensors. A new circuit has been proposed by the circuit designer [137]. For high performance standalone wireless applications of inertial measurement unit (IMU), analog-digital converter (ADC), control and wireless blocks should be integrated on the chip. The mechanical structure design optimization includes mechanical spring optimization to reduce the inter-axis coupling; creation of precise analytical models for the prediction of device performance in all three axes.

No device optimization can be realized without a proper fabrication process. In the current CMOS-MEMS process used for accelerometer fabrication in this project, the separation of etch steps for isolation trench and device release causes the contamination and the overheating problem, which both hinder the devices from being successfully released. Other materials with better electrical and thermal conductivity than photoresist should be investigated for use as the thermal path on the backside in the device release. The isolation trench should be refilled with insulating materials for really robust sensor structures.

In commercialization of any devices, cost is a dominant design constraint. Based on the CMOS-MEMS DRIE process in this work, two wafer-level microfabrication processes are proposed as the future work for volume fabrication of the accelerometers. The process flows are presented in Appendix C with brief descriptions. The main challenges in wafer-level plasma etch processes for MEMS devices include the loading effect caused nonuniformity in etch; wafer handling in process transfer; and device separation after the processes. Wafer-level vacuum package for high performance devices is even more challenging. It requires some additional particular processes such as wafer bonding, through-wafer interconnect and double-side precise alignment. Some steps should be finished in vacuum with remote handling. For successful device development, these issues must be solved in the future.

APPENDIX A
LAYOUTS OF TEST STRUCTURES FOR PROCESS CHARACTERIZATION

The layouts of some on-chip test structures are given in this appendix section. Other individual test structures are not included.

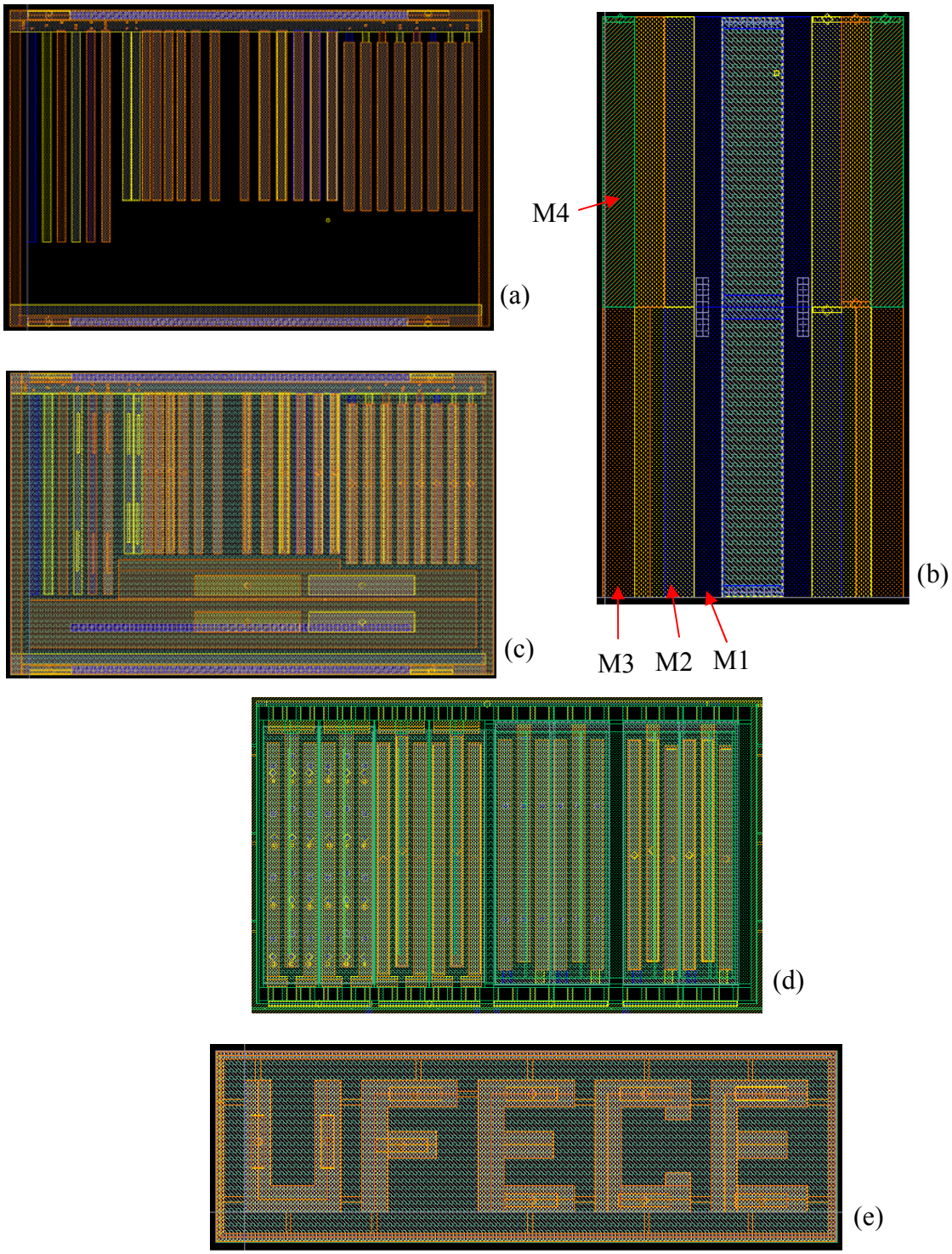


Figure A-1. Layouts of on-chip test structures. (a) ARDE test structure #1, (b) etching rate test structure, (c) ARDE test structure #2, (d) comb fingers with different patterns, (e) UFECE logo.

APPENDIX B
PIN-OUT OF ACCELEOMETERS AND BONDING PAD CONFIGURATION

For convenience of test, the wire bonding configuration for the 3-axis accelerometer is fixed. The die pin-out is given in Figure B-1 with the label of PLCC-52 pin numbers. PCB test boards were made based on this configuration.

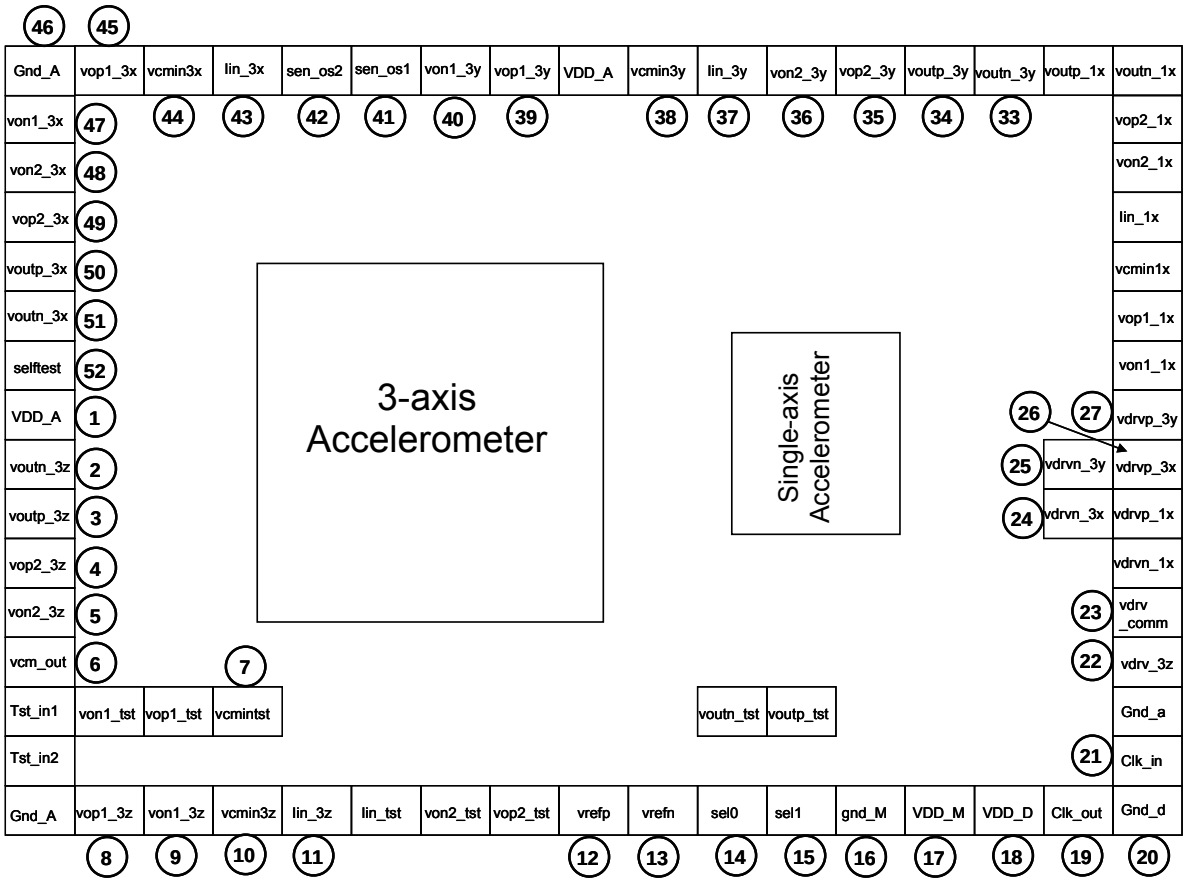


Figure B-1. Pad configuration and PLCC pin-out

APPENDIX C
PROPOSED WAFER-LEVEL FABRICATRION PROCESSES

Wafer Level Process I

In this process, the isolation trenches are formed completely from the backside etch. Two masks are needed. One is used to pattern the isolation trenches and device separation trenches. The other is to pattern the MEMS structure region.

The backside is first deposited with SiO_2 using low-temperature PECVD. The SiO_2 layer is patterned to define the MEMS structure region and device separation lines, as shown in Figure C-1(a). Then another photoresist layer is patterned to define the isolation trenches, see Figure C-1(b). In this step, double side alignment is need. Next, DRIE is performed to etch isolation trenches and separation trenches to certain depth, Figure C-1(c) before photoresist is removed to expose the SiO_2 patterns that define the MEMS structure regions, as in Figure C-1(d). The last DRIE step continues the etch in isolation and separation trenches until the etch front reaches the first SiO_2 layer on front side. In the meantime, the newly opened area is etched to define the structure thickness, as shown in Figure C-1(e). Finally, the wafer will be flipped over to perform the front side etch. Only one step of SiO_2 is needed before the final DRIE from front side to release the device.

It can be predicted that the profile of the isolation trenches will be tapered to the shape as shown in Figure C-1(e). As described in Chapter 5, this helps the complete release of the MEMS structures.

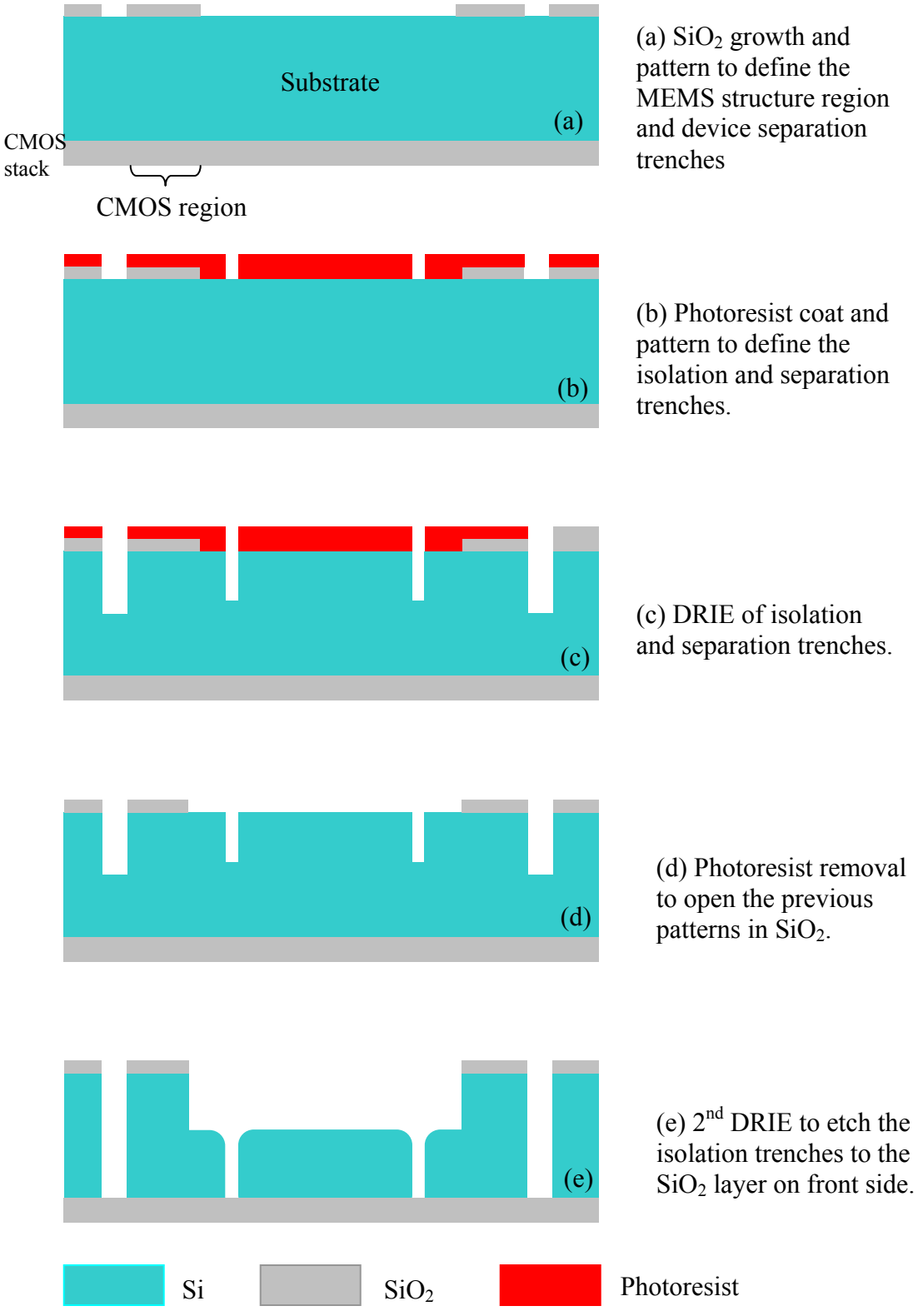


Figure C-1. Proposed wafer-level process flow for backside etch steps.

In this proposed process, we can take advantage of microloading effect to get an optimal timing ratio of the two DRIE steps to balance the isolation trench profile and the device thickness. Another merit of this process involves the comb drive design. Since no undercut etch from the front side is required, the comb drive fingers have no limit in shape at the connecting ends. Wider and robust comb drives with normal shape can be employed to realize the overall device robustness.

Wafer Level Process II

As described in Chapter 5, the isolation trench sidewalls are prone to be contaminated with etch byproduct and particles milled from sample surface. This complicates the device release due to the micro mask effect of the contaminants. Additionally, the existence of the thin film isolation beams makes the sensor structures less robust and more temperature dependent. For the above reason, it is highly desired to replace the isolation trenches with other solid structures that still have the function of electrical isolation. Another wafer-level fabrication process is proposed as the following. It employs a trench-refilling technique in which SiO_2 and poly silicon-germanium (Poly SiGe) low temperature deposition and CMP are involved. PECVD SiO_2 and LPCVD poly SiGe can all be deposited at a temperature below 425°C, which is proven safe to CMOS circuits [140]. Since the CMOS circuits are completely protected by metal layers, CMP should not affect the electrical performance of the circuits.

To ease the trench etch, the CMOS fabricated wafers will be thinned approximately to 100 μm. This thickness is constrained by the achievable aspect ratio for isolation trench etch, and more practically, the wafer thickness limit for safe handling. Double-side alignment is needed to define the isolation trench, followed by DRIE trench etch, as

shown in Figure C-2(a). Low-temperature PECVD (~350°C substrate temperature) is performed to deposit a 1~2 μm SiO_2 layer on trench bottom and sidewalls for isolation. LPCVD poly SiGe deposition at about 425°C follows to refill the trench partially, see Figure C-2(b). RIE or surface polish is followed to remove the SiO_2 and polysilicon on the surface, as shown in Figure C-2(c). In the meanwhile, a separate silicon bare wafer (substrate wafer) is prepared for low-temperature Si-Si wafer bonding. 1~2 μm SiO_2 layer is deposited and patterned followed by silicon DRIE for cavity etch in the substrate wafer. Then, after alignment, the CMOS wafer and substrate wafer are bonded together, see Figure C-2(d). Before front side etch process on CMOS wafer, the bonded wafers are attached to another carrier wafer and diced into device elements, as in Figure C-2(e). Finally, anisotropic SiO_2 etch and silicon DRIE finish the MEMS sensor release, which is followed by the chip separation by photoresist ashing, as in Figure C-2(f).

It should be noted that between the carrier wafer and substrate wafer in Figure C-2(e), a reliable adhesion should be formed for physical attachment and thermal conduction. The sensor elements should also be easily removed from the carrier wafer after the final process. Photoresist can be used as this adhesion layer. After the device release, it can be ashed away to allow the separation of sensor element from carrier wafer.

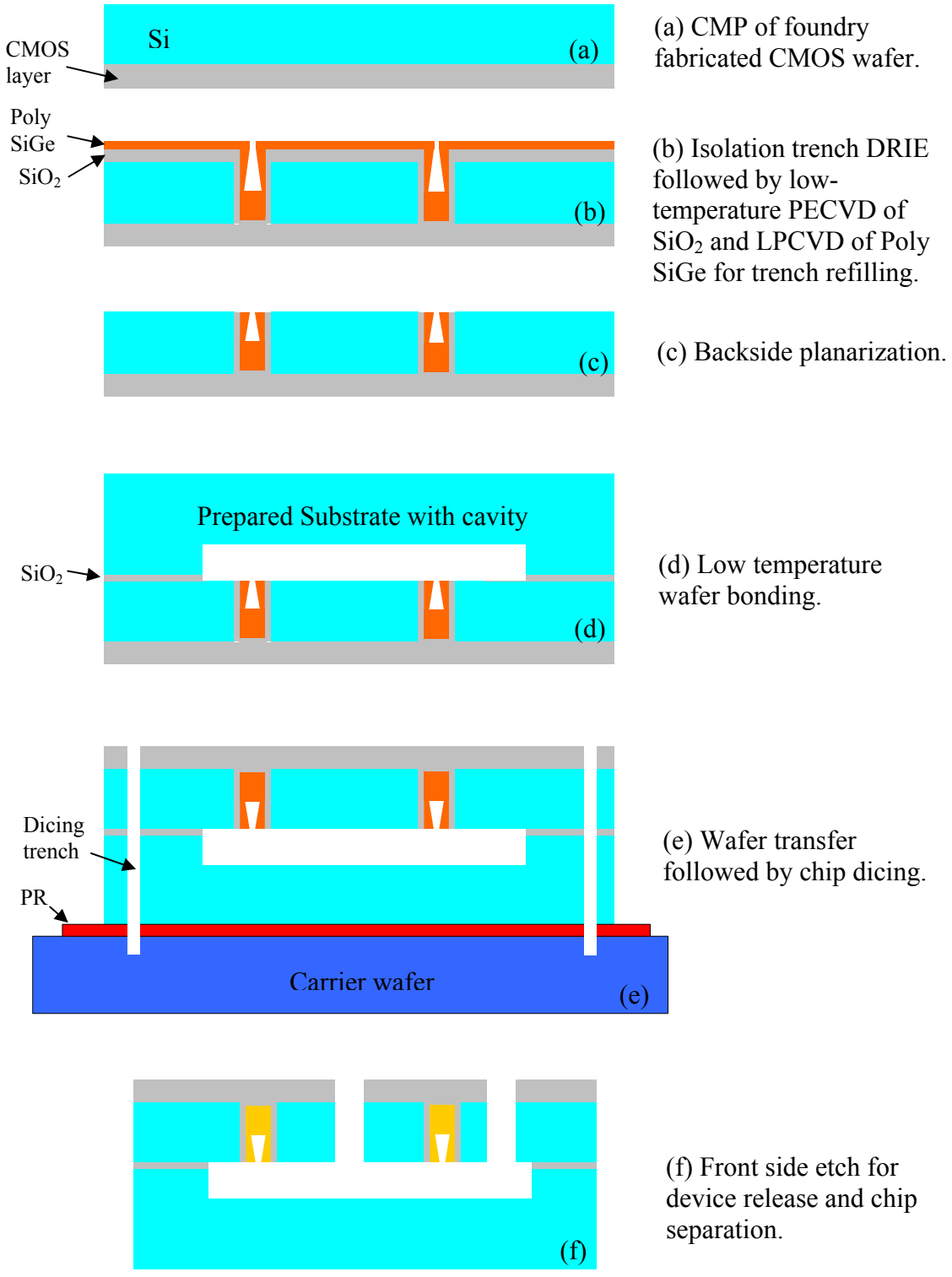


Figure C-2. Wafer level process with isolation trench refilling and wafer-bonding.

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BIOGRAPHICAL SKETCH

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