A 24-GHZ FULLY-INTEGRATED CMOS TRANSMITTER WITH ON-CHIP ANTENNA

By

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Chair: Kenneth K. O
Major Department: Electrical and Computer Engineering

The ever-increasing demand for low-cost portable devices has motivated the research on high frequency CMOS communication integrated circuits. We designed and implemented a transmitter chain that will be part of a single-chip 24-GHz CMOS radio for sensor network applications. The radio includes a RF transceiver, an on-chip antenna, a baseband processor, a sensor, and eventually a battery. The integration of an antenna on the same chip greatly simplifies the package, lowers the device cost to less than $1, and makes the radio easy to use.

The transmitter includes a minimum shift key (MSK) modulator, IF amplifiers, an up-conversion mixer, drivers and a power amplifier. A discrete approximation of the MSK using phase interpolation simplifies the modulator design and lowers the power consumption. A mode locking technique using positive feedback is also proposed to improve the power added efficiency (PAE) of power amplifier to 23.5%. The transmitter chain implemented in the UMC 0.13-μm CMOS provides 8-dBm output power to a 50-Ω

load and 7.7% rms error vector magnitude (EVM) while dissipating 100 mW. The signal transmitted by the chain with an on-chip antenna was picked up 5 meters away using an on-chip antenna, and 95 meters away using a horn antenna with 20-dBi gain. These demonstrations prove that short-range wireless communications using a single-chip radio with an on-chip antenna are possible.

Frequency sources for future millimeter-wave applications are also demonstrated. The transistors, varactors, and inductors are optimized to reduce the parasitic loss and capacitances. The components are used to realize wide tuning range 60-GHz voltage-controlled oscillators (VCO's) in UMC 0.13-μm CMOS and VCO's around 140 GHz in UMC 90-nm CMOS processes. We also used push-push architecture obtain an operation frequency of 192 GHz in 0.13-μm CMOS. This is the highest operating frequency for any silicon-based circuit. Our study also showed that the lumped element approach can be used even for circuits operating well above 100 GHz. A PLL tunable from 45.9 to 50.5 GHz was also implemented in 0.13-μm CMOS process. The power consumption was reduced to 57 mW by using an LC-oscillator based injection locked frequency divider (ILFD) while the operating frequency range is increased by tracking the VCO and ILFD self oscillation frequencies. These results indicate the feasibility of implementing millimeter-wave applications using low-cost CMOS technology. With more advanced CMOS processes, it should be possible to extend the frequency to sub-millimeter or THz range.

CHAPTER 1
INTRODUCTION

Over the past 10 years, the wireless communication industry has grown explosively and radio frequency integrated circuit (RFIC) research has received great attention. Ever-increasing demand for monolithic, low-cost, and low-power portable devices has motivated much research on a single-chip radio [1]. Since the baseband digital signal processors (DSP) are being implemented exclusively using CMOS technologies, CMOS technology offers highest level of integration and lowest cost in volume product.

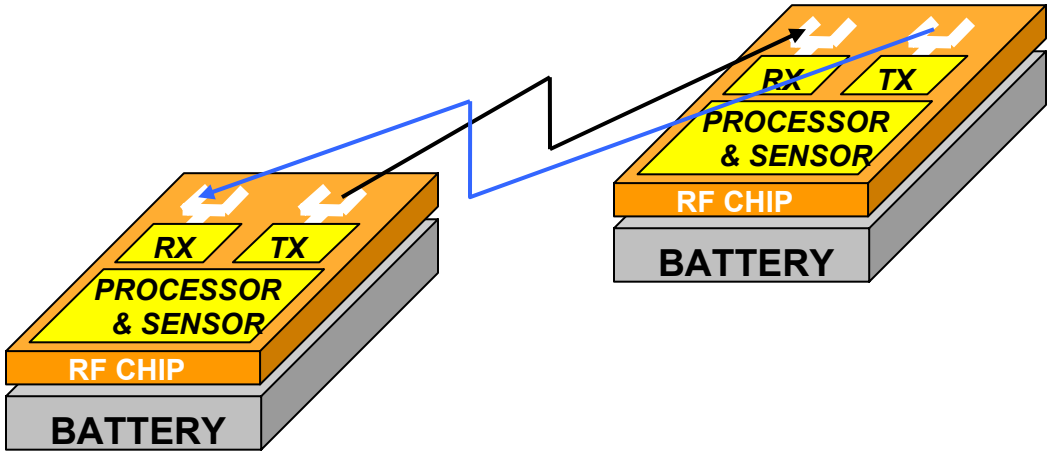


Figure 1-1 Conceptual μNode system

A μNode is a true single-chip radio incorporating an on-chip antenna, a transceiver, a digital baseband processor, a sensor, and potentially even a battery. Including of small antennas in an integrated circuit keeps the μNode size small, greatly simplifies their use, and eliminates the need for external transmission line connections and sophisticated packaging, which can radically reduce cost of wireless systems operating above 10 GHz [2]-[4]. Figure 1-1 shows a conceptual diagram of a μNode. The size of μNode device is

limited by the battery. Currently, a version with the size of an m&m® (Figure 1-2) is being developed.

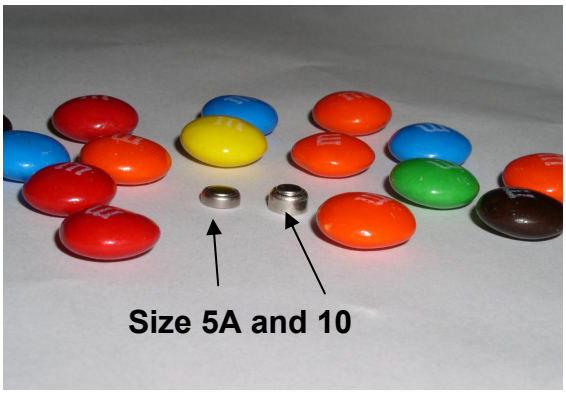


Figure 1-2 Typical μNode device size

The version being developed using standard CMOS technology costs less than $1, and is capable of wireless transmission and reception at 24 GHz ISM band over short distances. The communication range is typically 1 to 5 meters, and the range can be extended to around 30 meters at the cost of increased transmitted power and battery size. To keep the battery small and thus the over all form factor small, power consumption must be low. This rugged system on a chip could be so small that it is practically difficult to be detected, and so inexpensive that it can be distributed in large numbers. Groups of active μNodes can form self-organizing wireless communication networks. The μNode system can be viewed as a modified Zigbee radio operated at 24 GHz.

Our study focuses on design and characterization of a 24-GHz fully-integrated CMOS transmitter chain. The primary goal is to integrate all components including the antenna onto a single-chip while achieving low power consumption. The feasibility of implementing circuits for future millimeter-wave radios and sensor networks using CMOS technology are also studied.

Chapter 2 reviews the architecture of integrated transmitter chain and discusses their advantages and drawbacks. The two step transmitter architecture is used in the μNode system, to mitigate the VCO pulling issue in a fully integrated radio.

Chapter 3 discusses the design and characterization of the building blocks in the transmitter chain, including a static frequency divider, an MSK-like modulator, IF amplifiers, an up-conversion mixer, RF drivers and a power amplifier. A discrete approximation of the MSK using phase interpolation greatly simplifies the modulator design. The efficiency of PA is crucial because it is the most power hungry block in the transceiver. Since a constant envelope modulation scheme is used, a high efficiency non-linear class-E PA is utilized. A mode locking technique using positive feedback is proposed to improve the efficiency of the PA.

Chapter 4 presents wireless communications using on-chip antennas. The characteristics of on-chip antenna are reviewed briefly and an up-converter with an on-chip antenna is used to demonstrate the feasibility of using on-chip antennas pair for 5 meters short range communications. Then, the fully-integrated transmitter chain is described. The transmitter is first characterized using a 50-Ω load. It provides 8-dBm output power and 7.7% rms error vector magnitude (EVM, Appendix A) while consuming 100-mW power. The signal transmitted by the transmitter with on-chip antenna has been picked up 95 meters away using a horn antenna with 20-dBi gain. This uplink demonstration proves that communication between a base station and an integrated circuit with on-chip antenna over a distance of 100 meters is possible.

Chapter 5 describes the design of CMOS millimeter-wave voltage controlled oscillators. The high frequency characteristics of MOS transistor are discussed. The

transistor, varactor and inductor designs are optimized to reduce the parasitic capacitances and loss. An investigation of trade-off between quality factor and tuning range for MOS varactors at 24 GHz has shown that the polysilicon gate lengths between 0.18 and 0.24 μm result in both good quality factor and tuning ratio in the 0.13-μm CMOS process. The components were utilized to realize a wide tuning range 60-GHz VCO as well as oscillators operating above 140-GHz. A push-push architecture is utilized to obtain frequency close to 200-GHz. The lumped element approach can be used even for oscillators operating above 100-GHz and it results in a smaller circuit area.

Chapter 6 presents a 50-GHz phase-locked loop design. This fully integrated PLL manufactured in the 0.13-μm logic CMOS process is tunable from 45.9 to 50.5 GHz. It consumes less than one-tenth of the power for the SiGe PLL's using static frequency dividers, while achieving comparable phase noise performance. The power consumption is reduced using an LC-oscillator based injection locked frequency divider (ILFD). The operating frequency range is increased using a combination of an ILFD with an increased input frequency range, and tracking the VCO and ILFD self oscillation frequencies.

Finally, this research work is briefly summarized and possible future works are suggested in Chapter 7.

CHAPTER 2
RADIO FREQUENCY TRANSMITTER ARCHITECTURE

2.1 Introduction

Single chip radio implementation requires proper selection of radio architecture. A RF transmitter performs modulation, up-conversion, and power amplification, with the first two combined in some cases [5]-[7]. This chapter reviews the architectures of a RF transmitter with an emphasis on those issues particularly challenging when attempting to integrate all the functionalities onto a single chip. Sections 2.2 and 2.3 describe the two-steps and direct-conversion architecture and discuss their advantages and drawbacks. Chapter 2.4 presents the transceiver used in μNode system.

2.2 Two-Steps Transmitter

Figure 2-1 shows the block diagram of the two-steps transmitter architecture, which is similar to the heterodyne receiver architecture. First, the baseband I and Q channels undergo qudrature modulation at intermediate frequency of ω_1. Then, the result is up-converted to $\omega_1+\omega_2$ by mixing and bandpass filtering. The first bandpass filter suppresses the harmonics of the IF signal, while the second one removes the unwanted sideband, called image, centered around $\omega_1-\omega_2$.

In a two-step conversion architecture, since quadrature modulation is performed at lower frequencies, I and Q matching is superior, leading to less cross-talk between the two bit streams. Also, a channel filter may be used at IF to limit the transmitter noise and spurs in adjacent channels. The difficulty in two-steps transmitters is that the bandpass

filter following the second upconversion mixer must reject the unwanted image signal and LO leakage by a large factor, which could be more difficult when all the components are integrated on a single chip.

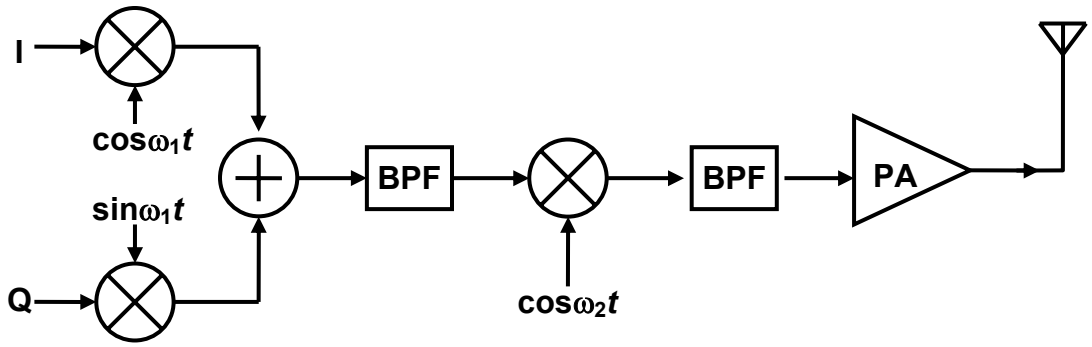


Figure 2-1 Two-step conversion transmitter

2.3 Direction-Conversion Transmitter

If the transmitted carrier frequency is equal to the local oscillator frequency, the architecture is called "direction conversion." In this case, the modulation and upconversion occur in the same circuit. Figure 2-2 shows the block diagram of a direct-conversion transmitter.

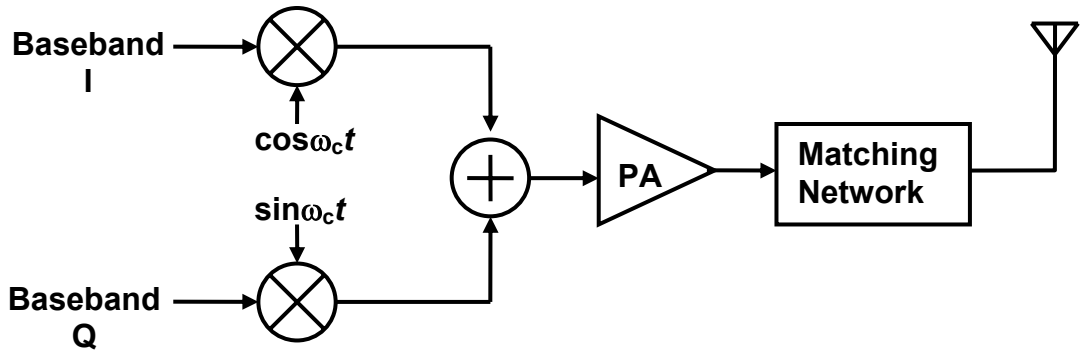


Figure 2-2 Direct-conversion transmitter

The direct-conversion transmitter in Figure 2-2 provides the highest integration level and lowest system cost, however it suffers from an important drawback called injection pulling, that is, the transmitter local oscillator is disturbed by the output of

power amplifier (Figure 2-3). This issue arises because the PA output is a modulated waveform with high power and a spectrum centered around the LO frequency [7]-[8]. Despite various shielding technique employed to isolate the VCO, the strong output of PA still corrupts the oscillator spectrum. In μNodes, a PA is integrated along with an antenna in the same chip as an oscillator and the PA is turned on and off periodically to save power. This problem is expected to be even more severe.

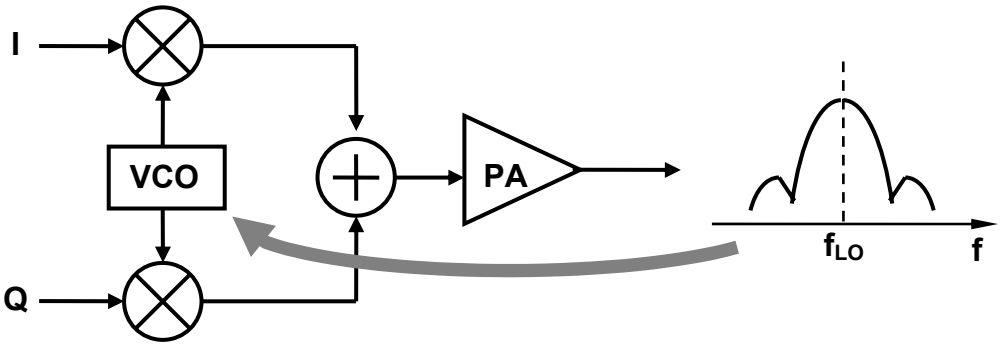


Figure 2-3 Disturbance of the local oscillator by PA leakage

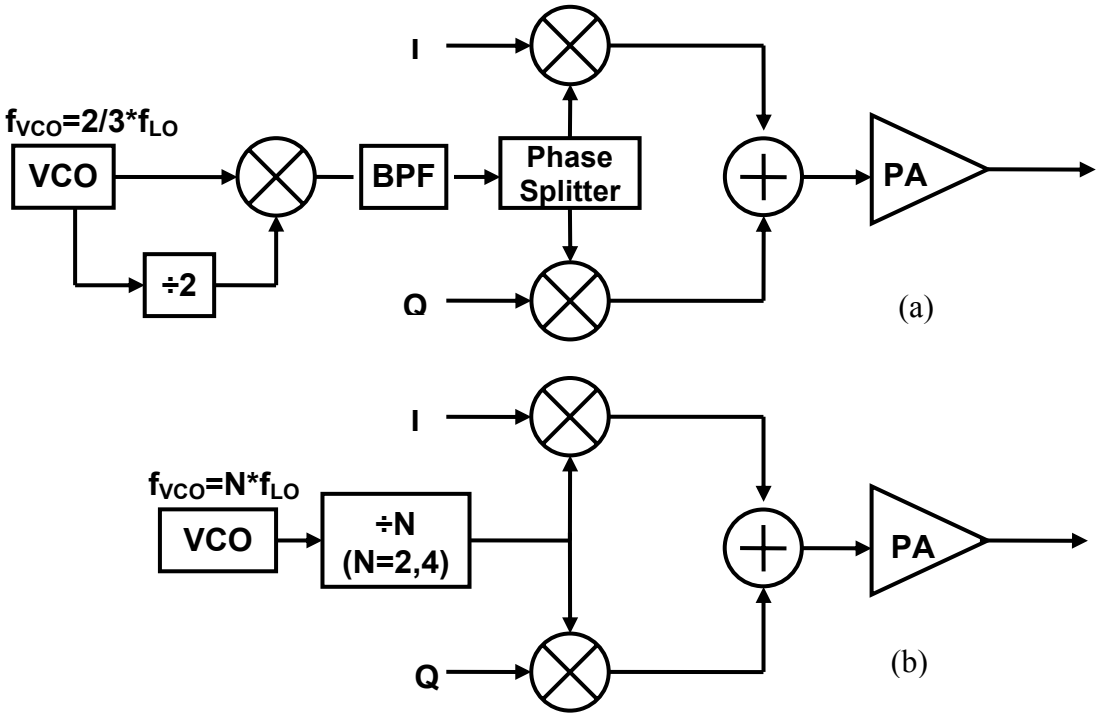


Figure 2-4 Direct-conversion transmitters with an offset LO

The phenomenon of LO pulling is alleviated if the PA output frequencies are sufficient higher or lower than the oscillator frequency. For a quadrature modulation scheme in Figure 2-2, this can be accomplished by offsetting the LO frequency. In Figure 2-4 (a), the output of VCO is first divided by 2. Then, the VCO and divider output are mixed and the result is filtered. Therefore, the VCO frequency is 2/3 of the LO frequency. In Figure 2-4 (b), the VCO output is divided by 2 or 4, and the frequency divider naturally generates quadrature LO signals.

2.4 Overview of the μNode Transceiver

2.4.1 Radio Frequency Subsystem Specifications

The μNode system operates at in the ISM band between 24 and 24.25 GHz. The data rate is 100 kbps. Since a direct sequence spread spectrum (DSSS) technique is used, it leads to 50 or 100 Mega chips per second. To have a low bit errors rates (BER) and good tolerance to LO frequency drifting, the required E_b/N_o is larger than 18 dB. Assuming the receiver noise figure (NF) is around 8 dB, the received signal must be larger than -98 dBm. The power gain between a pair of on-chip 3-mm zigzag antennas with 5-meters separation is around -99 dB. To have sufficient link margin, the transmitter output power is required to be higher than 10 dBm. Table 2-1 summarizes the key specifications of the RF subsystem. The link margin of the system is 9 dB. The antenna pair gain is expected to increase by about 10 dB when the substrate is thinned to ~100 μm [9], thus, the link margin can be as high as 19 dB.

2.4.2 Radio Frequency Transceiver Architecture

Both the two-steps and direct-conversion transmitter architecture could be used for the μNode system. Because the PA and antenna are integrated on the same chip as the

local oscillator, the VCO pulling issue becomes worse. Thus, the two-steps transmitter architecture is easier to implement and its performance requirements are relaxed.

Table 2-1 Link budget of the μNode system.

Frequency Band	24 to 24.25 GHz ISM band
TX Output Power	10 dBm
Communication Range	5 m
Antenna Pair Gain	-99 dB
Received Power	-89 dBm
Thermal Noise	-174 dBm/Hz
Date Rate (100 kb/s)	50 dB
SNR	18 dB
RX Noise Figure	8 dB
Receiver Sensitivity	-98 dBm
Link Margin	9 dB

Figure 2-5 shows the two-step or heterodyne architecture of the RF subsystem. The frequency synthesizer provides a 21.4-GHz LO signal. The intermediate frequency is 2.7 GHz, which is exactly 1/8 of the LO frequency, thus, IF signal could be generated using a frequency divider and only one synthesizer is required. The transmitter includes a multi-phase generator (8:1 frequency divider), an MSK-like modulator, IF amplifiers, an up-conversion mixer, drivers and a power amplifier. The 8:1 frequency divider generates quadrature signals for the modulator. The serial baseband digital data are directly up-converted to IF by the modulator and the IF I/Q mixers are not needed any more. The signal at IF is amplified and fed into a double-balanced Gilbert cell up-conversion mixer. The RF signal is amplified by a 3-stage driver and fed to a class-E power amplifier (PA). Finally, the PA drives a 3-mm on-chip zigzag dipole antenna.

The receiver includes a low noise amplifier (LNA), a RF-to-IF down-conversion mixer, IF amplifiers, an IF-to-baseband mixer, an automatic gain control (AGC) unit, a low pass filter (LPF), and an analog to digital converter (ADC).

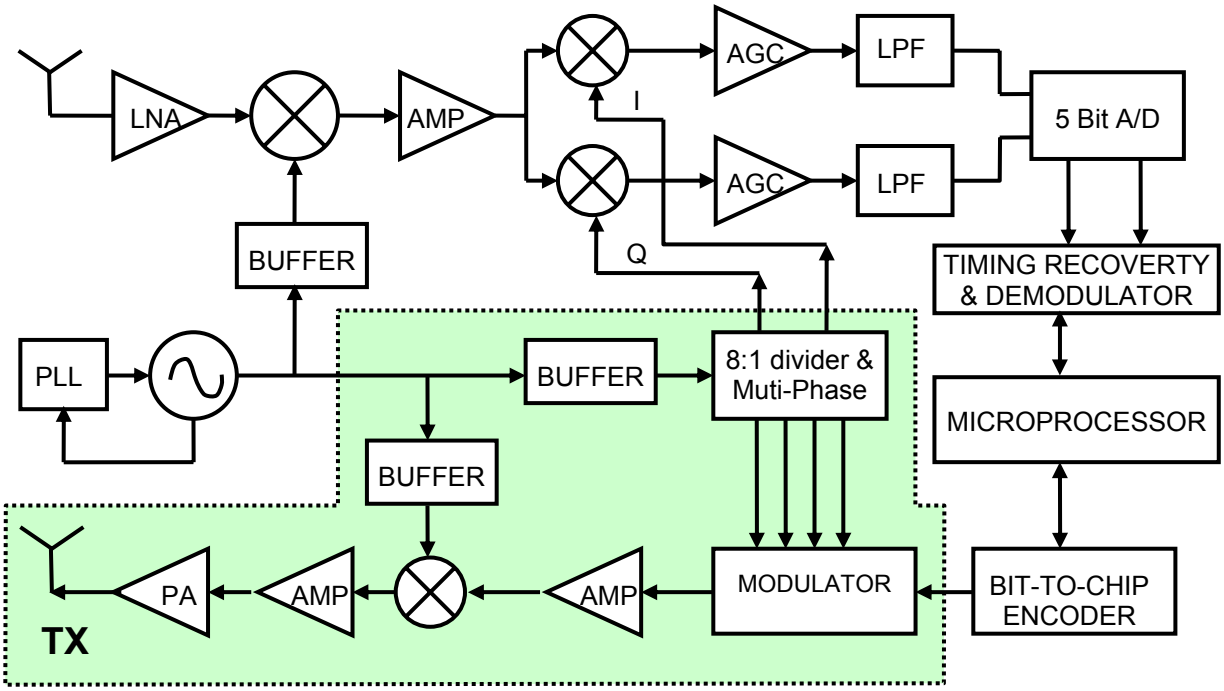


Figure 2-5 Block diagram of simplified μNode RF subsystem using two-step conversion architecture

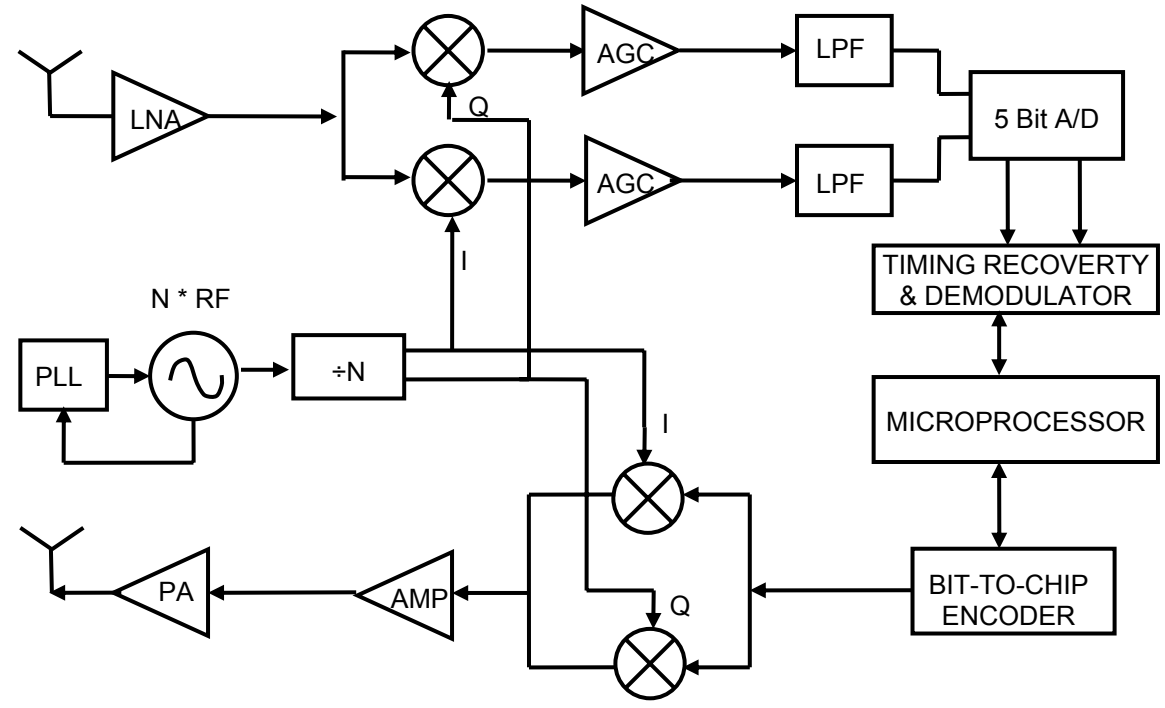


Figure 2-6 Direct-conversion architecture for μNode

The direct conversion architecture can also be used for the μNode system. Both of the architectures in Figure 2-4 could be used. Because it is difficult to design a good phase shifter around 24 GHz, the architecture using a frequency divider in Figure 2-4(b) is easier to implement. Therefore, a synthesizer running around 48 or 96 GHz is required. The feasibility of implementing oscillators and a synthesizer at this frequency band will be discussed in Chapter 5 and 6.

CHAPTER 3
KEY BLOCKS OF THE TRANSMITTER

3.1 Introduction

As described in Chapter 1, the key requirement for μNode is the low power consumption. In the design, each block must consume as low current as possible. Another requirement for the transmitter is that the output power must be sufficient high and it must be power sufficient. In this chapter, the design and measurement results of each block of the transmitter are described. A power efficient 26-GHz static frequency divider is presented in Section 3.2. A low power wide bandwidth MSK-like modulator is discussed in Section 3.3. The IF amplifier and up conversion mixer are described briefly in Section 3.4 and 3.5. Section 3.6 proposes a high efficiency class E power amplifier using the mode locking technique.

3.2 Power Efficient 26-GHz 32:1 Static Frequency Divider

3.2.1 Circuit Architecture

High speed frequency dividers are critical in a variety of applications from frequency syntheses in wireless communications to broadband optical fiber communication systems. As shown in Figure 2-5, in the transmitter a 21.4 GHz frequency divided-by-8 circuit is required for I/Q modulation. These applications require high speed, low power, high sensitivity and monolithic integration.

To date, the highest operating frequencies for frequency divider have been achieved with bipolar and III-V technologies, though their power consumptions are high [10], [11].

Compared to the bipolar and III-V dividers, CMOS ones usually operate at lower frequencies. To increase the operating frequency at given power consumption, several techniques are used, such as injection locking [12], dynamic circuit [13] and improved Miller divider [14]. Compare with them, a static one has a much wider operating range and moderate operating frequency and power consumption. CMOS static frequency dividers operating around 20 GHz have been recently reported [15]-[19], but the power consumption is too high (usually higher than 25 mW for 25-GHz operation).

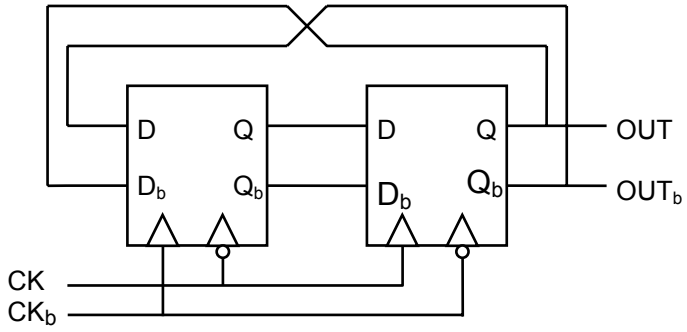


Figure 3-1 Block diagram of the 2:1 static frequency divider

Figure 3-1 shows the block diagram of 2:1 current mode logic (also known as source-coupled logic) static frequency divider [20]. The divider is based on the classical master-slave D-type flip-flop in which the inverted slave outputs are connected to the master inputs. The differential nature reduces the switching noise and provides sufficient noise margin. The divider inputs (CK and CK_b) are usually also terminated with 50-Ω resistors (not shown) to make the amplitude of input signals more predictable. As shown in Figure 3-2, each master-slave flip-flop is implemented using CML. The master and slave stages consist of an evaluate stage ($M_{1,3,4}$) and a latch stage ($M_{2,5,6}$). The current sources in conventional CML latches are omitted [15] for low voltage operation. This causes the total current flowing through the evaluation and latch stages to fluctuate in

time, which may potentially generate larger switching noise. However, at high frequencies, there is big overlap when both the evaluation and latch stages are turned on, which makes the supply current relatively constant. Therefore, the switching noise is limited. That is also verified by the simulation.

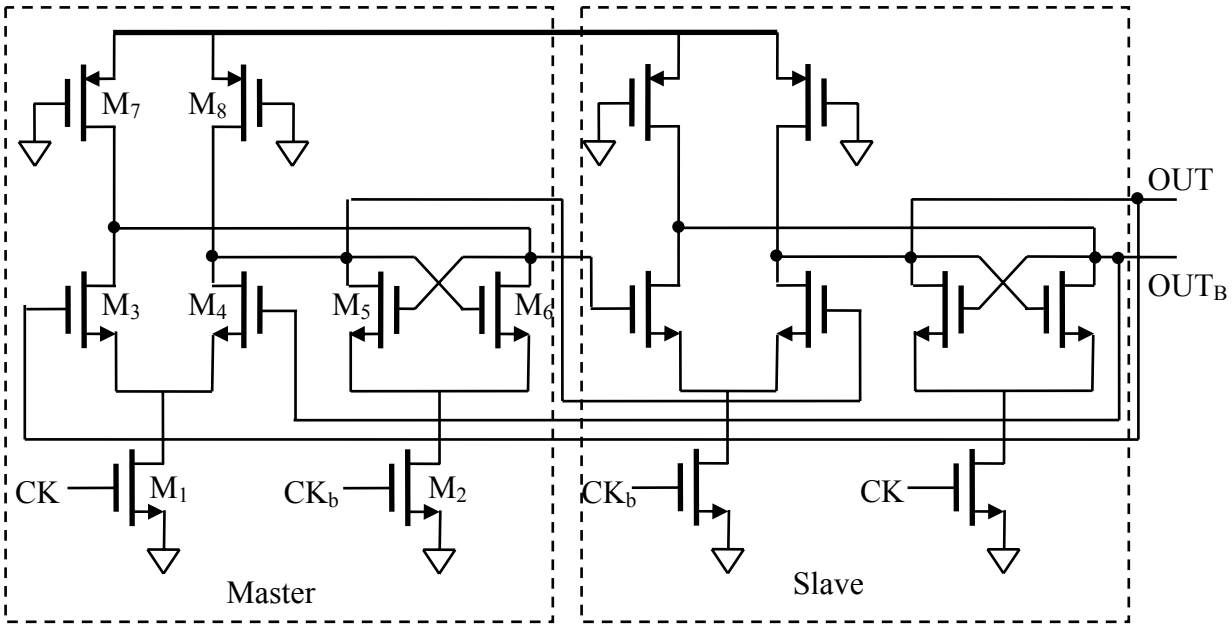


Figure 3-2 Schematic of the 2:1 static frequency divider

When CK and CK_b are equal to the common mode value and there is no input clock signal, both the master and slave latches are semi-transparent, allowing signals to propagate through both the latches. This makes the circuit work as a ring oscillator. If the delay from the gate to drain of M_3 is τ_{pd}, then the oscillation period is equal to $4\tau_{pd}$. Thus, the circuit oscillates at $1/(4\tau_{pd})$ and the signal at the drain of M_3 lags the signal at the gate of M_3 by 90°. In the small signal model, the propagation delay, τ_{pd}, is proportional to the R_LC_L constant at the output node. However, the voltage swing in this circuit can be large and the operation of the oscillator becomes nonlinear [21]. This makes R_LC_L only an approximate estimate and large signal characteristic also need to be considered to estimate the real oscillation frequency.

Usually, the higher self-oscillation frequency leads to higher operating frequency of divider. Meanwhile, the oscillation frequency strongly depends on the transistors size. Figure 3-3 shows the simulated oscillation frequency as function of the width of latch transistors ($M_{5,6}$) for varying widths of PMOS loads ($M_{7,8}$). In the simulation, the widths of $M_{3,4}$ are fixed at 5 μm and $M_{1,2}$ are fixed at 8 μm. As can be seen, smaller load transistors lead to lower oscillation frequency, because the R_L increases with smaller loads. Though the capacitance C_L also decreases a little, it decreases slower than the increase of R_L. Furthermore, with given load transistors, wider latch transistors lead to lower frequency. From the simulation, the output voltage swing (OUT, OUT_B) increases as the latch transistor size increases, because of the larger negative resistance from the cross-coupled transistors. Meanwhile the maximum charge/discharge current is also limited by M_1. This leads to the longer charging and discharging time, which in turn results in larger τ_{pd} and smaller oscillation frequency [22]. Additionally, when the widths of PMOS loads are less than 1.8 μm and latch transistors are less than 1 μm, the circuit stops oscillating because the PMOS transistors are too small to pull-up sufficiently fast [23].

To lower power consumption, the PMOS loads and latch transistors should be small, while avoiding the region where the circuit fails to oscillate. Sufficient voltage swing is also required to drive the subsequent stage. In the final design, the widths of the drive transistors ($M_{3,4}$), PMOS loads ($M_{7,8}$) and latch transistors ($M_{5,6}$) are chosen as 5 μm, 2.6 μm and 1.6 μm, respectively. There is greater flexibility for sizing input transistors ($M_{1,2}$). It should be sufficiently large that the voltage drop across the transistors is not too high and the gate capacitance is sufficiently low that the power

consumption for driving their gates is not high. The widths of $M_{1,2}$ are chosen to be 8 μm. For the following four stages, the frequency is lower, thus, smaller transistors are used and the power consumption is much lower than that of the first stage.

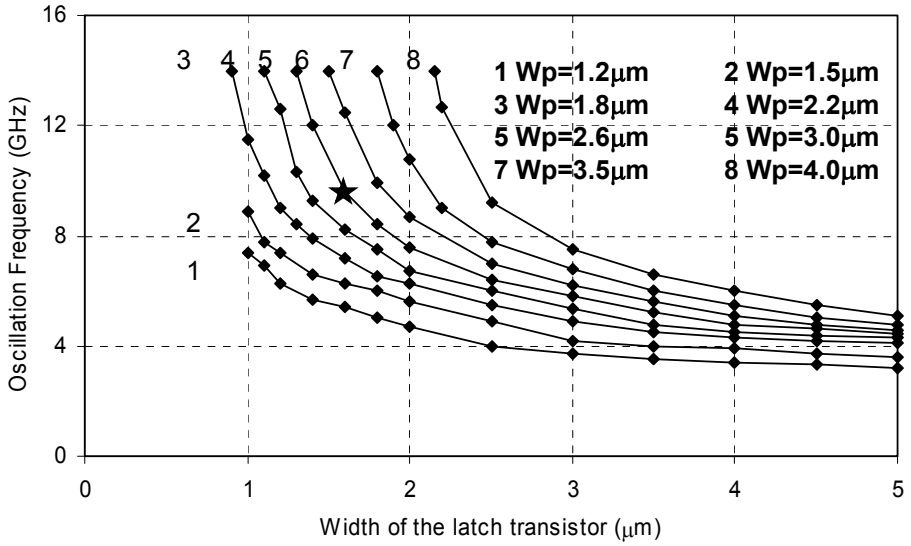


Figure 3-3 Oscillation frequencies versus the width of the latch transistors with different PMOS load

Further, extracting from the layout of divider, the interconnect capacitance does not change much with different sizes of the transistors. Therefore, as the sizes of all the transistors are scaled up, the impact of interconnect parasitic capacitance becomes less important and the self-oscillation frequency is increased. This, however, also increases the power consumption. Figure 3-4 shows the power consumption, maximum and minimum operating frequencies as function of the drive transistor ($M_{1,2}$) width. In this simulation, for both the master and slave stages, the widths of $M_{1,2}$, $M_{5,6}$ and $M_{7,8}$ are approximately 1.6 times, one third (1.6/5), and one half (2.6/5) of the width of $M_{3,4}$ respectively. As expected, the power consumption increases almost linearly with the transistor sizes, however, the operating frequency levels off when the drive transistor is larger than 5μm. This shows that the choice of 5 μm for $M_{3,4}$ is almost optimal.

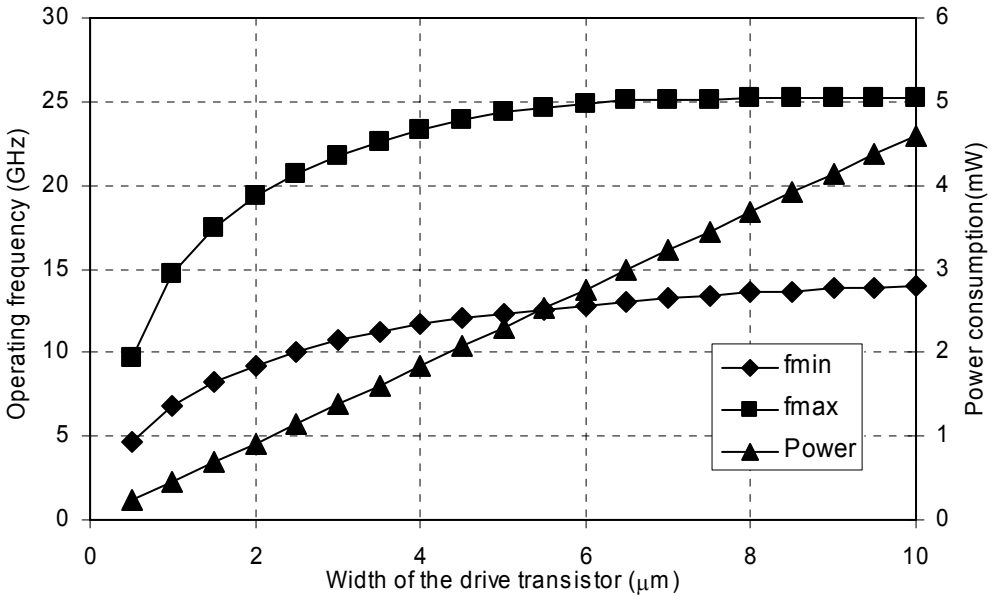


Figure 3-4 The operating frequencies and power consumption versus the drive transistor width

3.2.2 Experiment Results

To make the measurements easier and more realistic, a 32:1 circuit consisting of 5 stages of 2:1 divider is implemented. The circuit is fabricated in the UMC 0.13-μm CMOS logic process with eight-layer copper metallization. The die micrograph of circuit is shown in Figure 3-5. The chip size is 0.38 mm x 0.53 mm, which is mainly determined by the pad frame, while the active area is only about 20 μm x 80 μm.

The divider starts to work at supply voltage of 0.53 V with 4.2 GHz maximum operating frequency and only 56 μW power consumption of the first 2:1 stage. This is only ~12 μW higher than the divider architecture specially designed for low voltage and power operation [24]. Figure 3-6 shows the input sensitivity measured at three different supply voltages of 0.7, 1.2 and 1.5 V. The maximum operating frequencies are 10, 22.5 and 26 GHz respectively and the power consumption of the first 2:1 stage is 228 μW, 1.86 mW and 3.88 mW, respectively. The power consumption of the whole 32:1 circuit

including buffers (with high impedance output load) is 551 μW, 4.68 mW and 8.97 mW, respectively. With 50 Ω output load, the power consumption is about 1/3 higher due to larger current in the buffers. As can be seen, the first stage consumes about 45% of total power. The output waveform is measured with Agilent Infiniium 86100B oscilloscope. Figure 3-7 shows the output waveform with 26 GHz input signal. Since the buffers work at low frequency, the output is close to square.

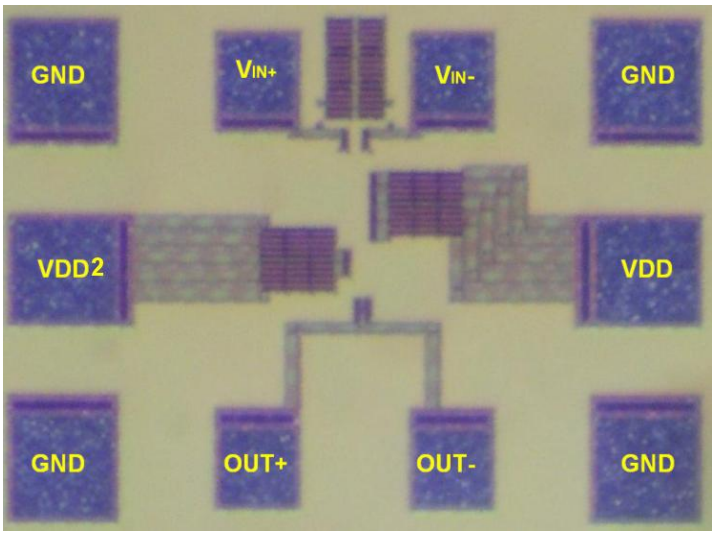


Figure 3-5 Micrograph of the 32:1 frequency divider

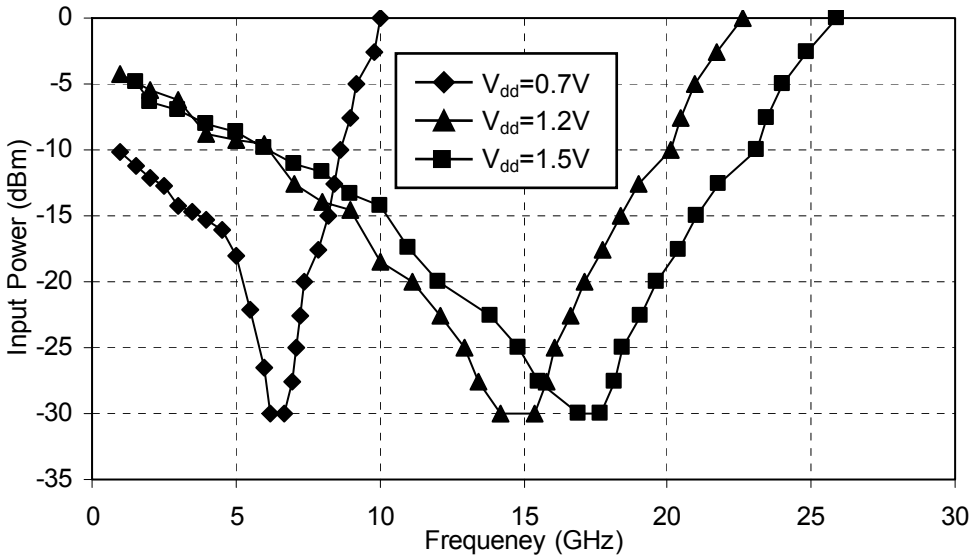


Figure 3-6 Measured input sensitivity at different supply voltages

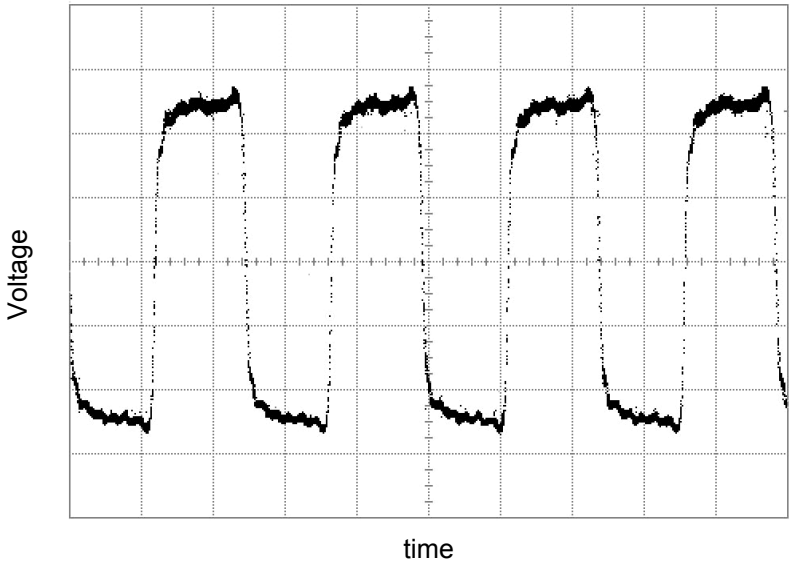


Figure 3-7 Output waveform with 26GHz, 0-dBm input (Time 500ps/div, voltage 100mV/div, offset -5.1mV, AC coupled, 50Ω output load, V_{dd}=1.5V)

Table 3-1 summaries the power consumption and the maximum operating frequency for several previously reported 2:1 CMOS static frequency dividers above 20 GHz. The 3.88-mW power consumption at 26 GHz is much less than those of all the bulk CMOS dividers [16]-[18] and is close to that of the SOI CMOS frequency divider [19].

Table 3-1 Power consumption and maximum operating frequency for several recently published 2:1 CMOS static frequency dividers

Ref	V_{dd} [V]	Power [mW]	Input Power [dBm]	Max. Freq. [GHz]	Technology
[16]	1.5	60.9*	9	25	120-nm CMOS
[17]	1.5	45*	10	27	120-nm CMOS
[18]	1.5	66*	0	18.5	120-nm CMOS
[19]	1.0	2.7	-7	25	120-nm SOI CMOS
	1.5	7.66	-7	28.6	
This work	1.2	1.86	0	22.5	0.13-μm CMOS
	1.5	3.88	0	26	

* Including the power consumption of output buffers, which is about 1/3 of the total power consumption

By optimizing the transistors sizes in D-flip-flops, a power efficient and high sensitivity 32:1 static frequency divider in a 0.13-μm CMOS process is demonstrated. The first 2:1 stage can work up to 26 GHz with only 3.88 mW power consumption at 1.5 V supply. This is the most power efficient bulk CMOS static frequency divider operating above 20 GHz.

3.3 Low Power Wide Bandwidth Constant Envelope Modulator

3.3.1 Minimum Shift Key and Constant Envelope Modulation

Minimum shift key (MSK) modulation can be considered as a special offset quadrature phase shift key (OQPSK), as shows in Figure 3-8. Like other quadrature modulation schemes, every two consecutive bits are impressed on quadrature phase of a carrier. Suppose, we use half sinusoids, rather than rectangular pulses (which is used in OQPSK), to represent the levels that are multiplied by the carrier. More specifically, as shown in Figure 3-9, let us multiply the levels in the upper arm by $\cos\omega_1 t$ and those in the lower arm by $\sin\omega_1 t$, where $\omega_1 = \pi/(2T_b)$ and T_b is the data period. Thus, the output of the modulator is

$$x(t) = a_m \cos\omega_1 t \cos\omega_c t - a_{m+1} \sin\omega_1 t \sin\omega_c t . \tag{3-1}$$

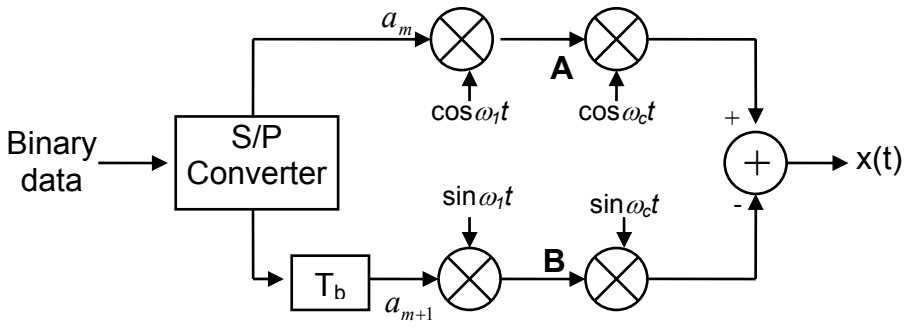


Figure 3-8 Block diagram of the MSK modulation

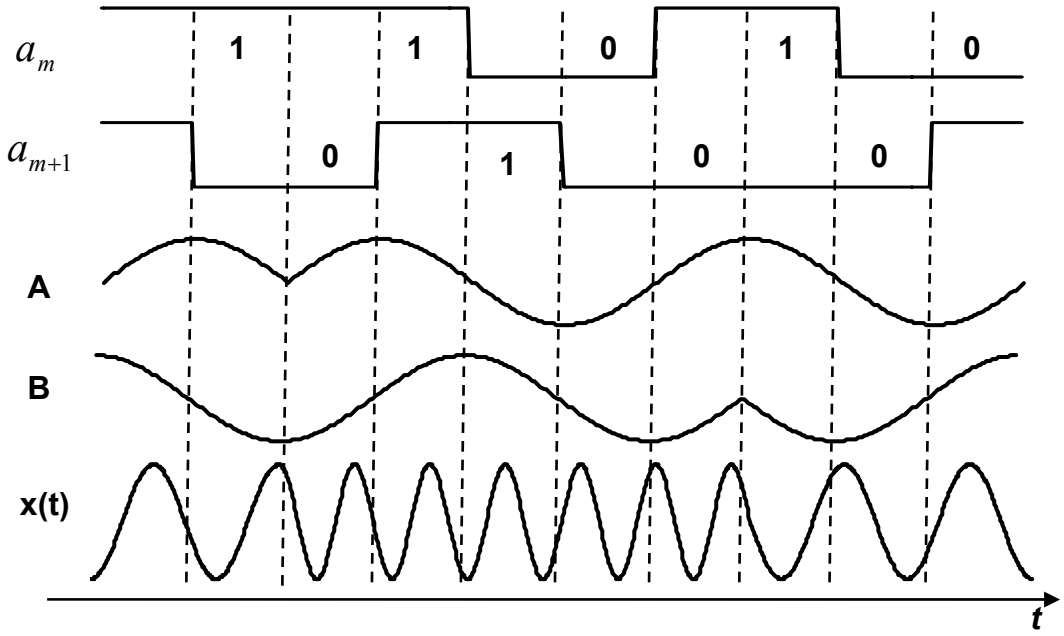


Figure 3-9 Signals in the MSK modulation

The resulted output signal of a MSK modulation is constant envelope. As a matter of factor, MSK should eventually be viewed as a type of frequency shift key (FSK). The MSK modulation can also be seen in the constellation of a phase modulated signal. The signal vector, or phasor, changes its angle according to the transmitted bits while the magnitude of the vector is kept the same. This results in a point moving on a constant–radius circle and changing direction from time to time, as illustrated in Figure 3-10, which shows an MSK modulation and its constellation for 8 bit intervals. The baseband I/Q channel data bits are shaped into sinusoidal pulses and respectively modulated onto two carriers with quadrature phases. Then the resulting signals of the two channels are summed up, and the modulated signal becomes a constant envelope carrier with changing phases. It can be seen that on the resulting constellation the phasor moves on a circle and changes directions based on the I/Q bit pattern. It goes over a quadrant in a bit interval.

In order to simplify the circuit architecture without significantly compromising the performance of modulator, the possible output states are limited to 16 discrete steps. Therefore, the phase change over any bit interval, which corresponds to a quadrant on the constellation, was implemented in a limited number of 4 discrete steps. The output of modulator should generate a constellation as shown in Figure 3-11, where the modulated signal moves sequentially on the circle and changes direction only on the I or Q axis points. Theoretically, if infinite steps are used, i.e., these steps are continuous, it implements standard MSK modulation [25], [26]. The modulator implements an MSK-based constant envelope phase-shift scheme, so that a high efficiency non-linear power amplifier can be used.

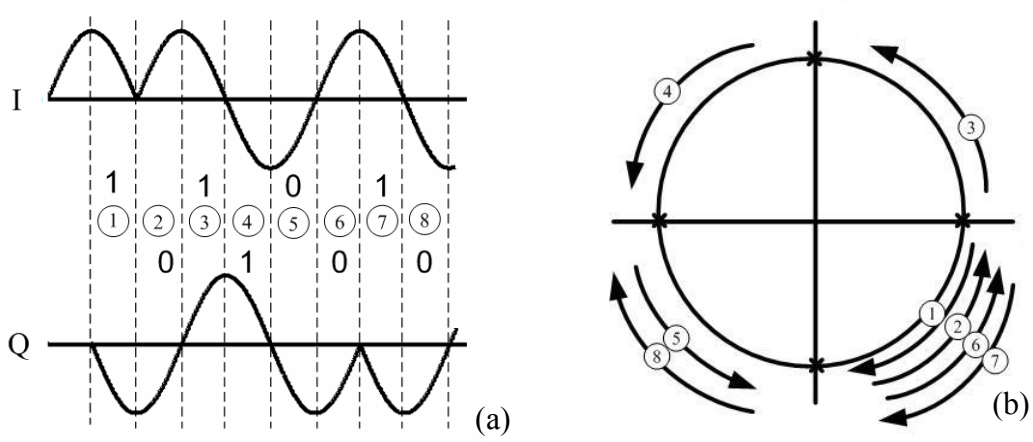


Figure 3-10 An MSK modulation example and the modulated signal's constellation
(a) MSK modulation is I-Q modulation with half sinusoidal pulse shaping
(b) The modulation generates a constant envelope constellation

In order to simplify the circuit architecture without significantly compromising the performance of modulator, the possible output states are limited to 16 discrete steps. Therefore, the phase change over any bit interval, which corresponds to a quadrant on the constellation, was implemented in a limited number of 4 discrete steps. The output of modulator should generate a constellation as shown in Figure 3-11, where the modulated

signal moves sequentially on the circle and changes direction only on the I or Q axis points. Theoretically, if infinite steps are used, i.e., these steps are continuous, it implements standard MSK modulation, and if one step per quadrant is used, its spectrum is the same as standard offset QPSK [25], [26].

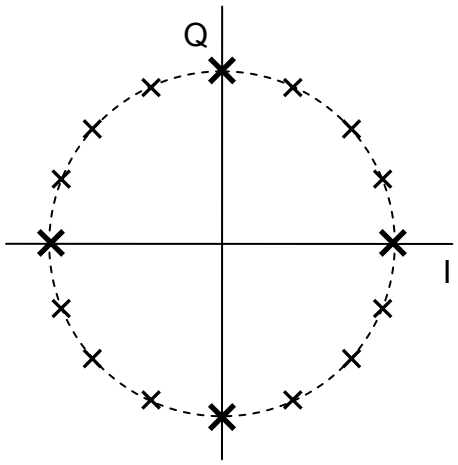


Figure 3-11 Ideal constellation of modulator output

Figure 3-12 shows the simulated output spectrum of this modulator, as well as standard MSK and offset QPSK. Because of the limited steps is used, the modulation sidelobes are higher than those for MSK. In particular, these are at frequency offset equal to multiples of four times the data rate are higher. They are about -26 dB lower than the mainlobe. However, compared to the offset QPSK, these peak sidelobes are lower and occur at higher frequencies. This makes the filtering of the sidelobe easier.

3.3.2 Implementation of Constant Envelope Modulator

Figure 3-13 illustrates how, in a particular quadrant, constant envelope and different phases can be generated from two quadratures of a carrier. By maneuvering the values of a and b, which can be seen as the weights of two quadratures, θ can be changed while maintaining the constant envelope, r. By choosing pairs of quadratures of different phases according to the actual data, the correct quadrant can be chosen.

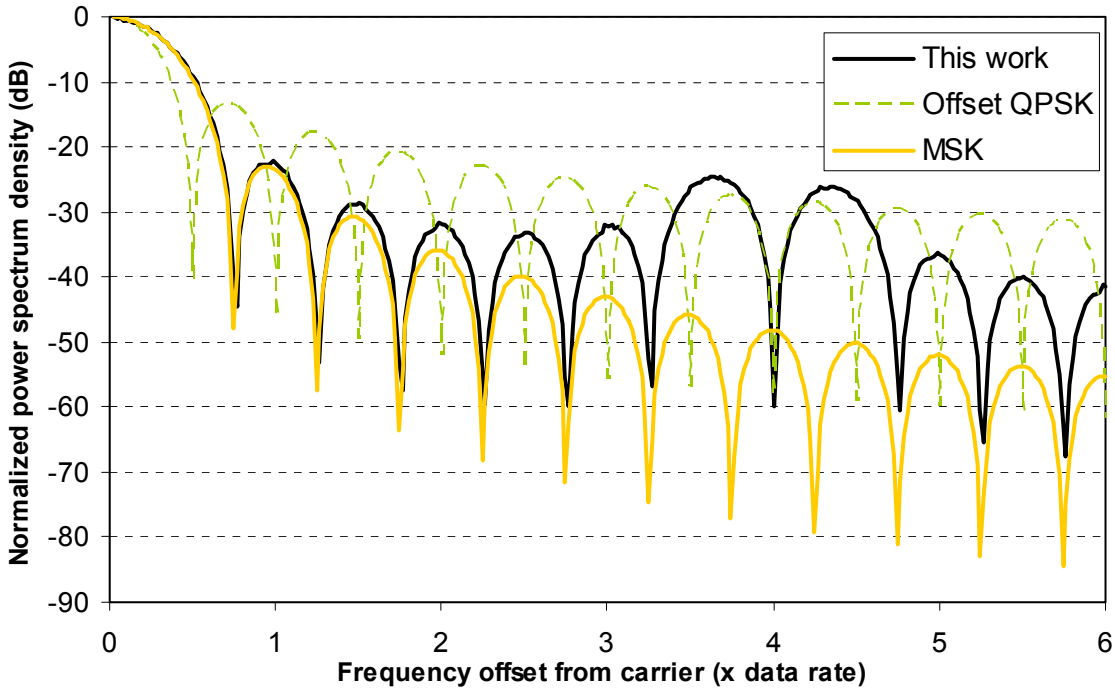


Figure 3-12 Simulated power spectra of the modulator output, standard MSK, and offset QPSK

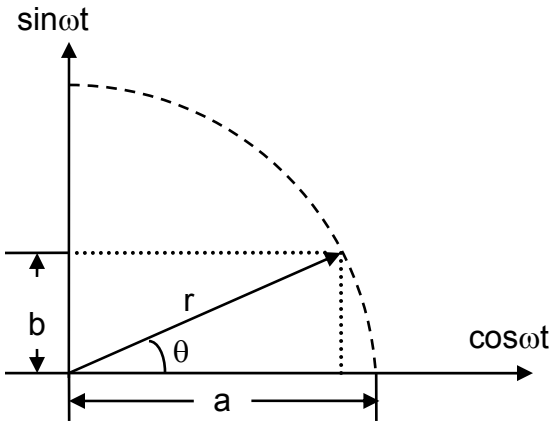


Figure 3-13 Illustration of how a phasor can be generated from two phasors in quadrature

The approach of generating an in-between phasor from two phasors in quadrature can be realized by a phasor combining circuit, or a summing circuit, whose conceptual schematic is presented in Figure 3-14 [25], [26]. In this circuit, the two input LO signals, V1 and V2, are at carrier frequency and have 90 degree difference in phase, while the

values of I1 and I2 determine the weights of the two LO's. Using the long channel small signal transistor model,

$$a = g_{m1}V = \sqrt{2\beta I_1}V \text{ , where } \beta = \mu C_{ox}W / L \tag{3-2}$$

$$b = g_{m2}V = \sqrt{2\beta I_2}V \tag{3-3}$$

From Figure 3-13,

$$r = \sqrt{a^2 + b^2} = \sqrt{2\beta(I_1 + I_2)}V \text{ .} \tag{3-4}$$

To ensure the constant envelope, the summation of I_1 and I_2 should be constant. The input signal swing must be limited and the longer gates need to be used, so that, the model is valid. However, to achieve ~2.7 GHz operating frequency, the gate lengths should also be kept as short as possible. In the final design, the transistor length is chosen as 0.3 μm. The input and output voltage swing must also be limited to valid the linear small signal transistor model.

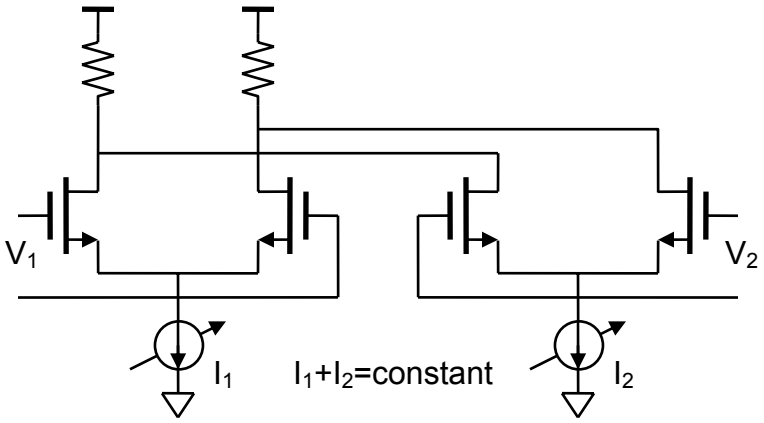


Figure 3-14 Conceptual schematic of a summing circuit

3.3.3 Circuit Description

Figure 3-15 shows the block diagram of the modulator. The circuit mainly consists of two 4:1 differential multiplexers, a phasor summing circuit, output buffers, and a logic

circuit to control the two 4:1 multiplexers. The logic circuit is not included in Figure 3-15, for the purpose of clarifying the modulator circuit's main architecture. The input I/Q data determine the control signals of the multiplexers. The four input quadrature signals are the outputs of an 8:1 static divider similar to that described in Section 3.2

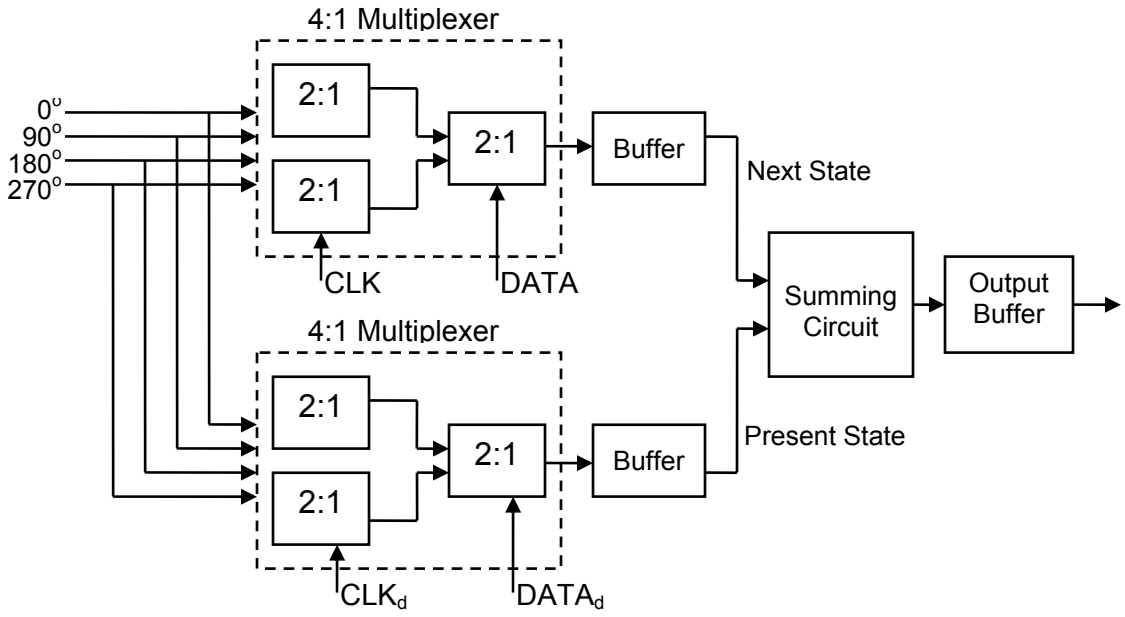


Figure 3-15 Block diagram of the constant envelope phase shift modulator

Figure 3-16 shows the schematic of the phasor combing circuit. The size of the summing transistors ($M_{1\text{-}4}$) is 8 μm/0.3 μm and the load resistor is about 1.6 KΩ. The variable currents (I1 and I2 in Figure 3-14) are implemented by switching current source ($M_{10\text{-}13}$) to left branch ($M_{1,2}$) or right branch ($M_{3,4}$). In each period, the value of I1 decreases as $4I_0$, $3I_0$, $2I_0$, and I_0, while the value of I2 increases as 0, I_0, $2I_0$, and $3I_0$. This topology ensures the total current of the two branches are always constant. The width of $M_{8,9}$ is twice of $M_{5\text{-}7}$, so that they have the same voltage drop. The width of switches ($M_{5\text{-}9}$) and current sources are made sufficient large, so the voltage drops across these transistors are not too high, which is important for the low voltage operation.

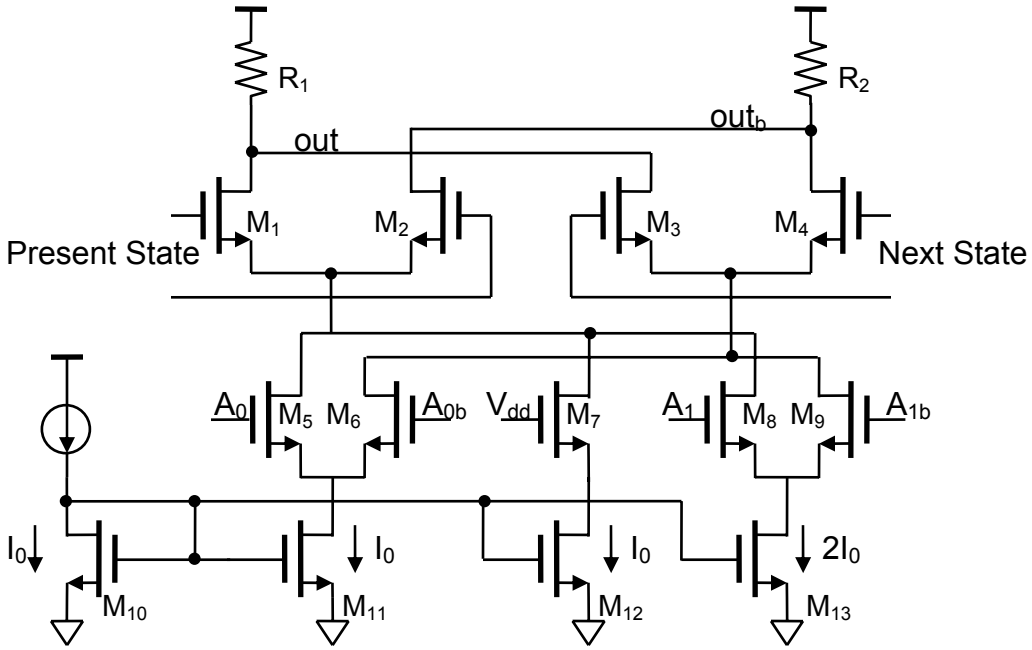


Figure 3-16 Schematic of the phasor combining circuit

3.4 Intermediate Frequency Amplifier

The IF amplifier is implemented using the cascode topology. The schematic of the IF amplifier is shown in Figure 3-17. Two cascode stages are used to provide sufficient power gain. The size of the transistors in first stage ($M_{1\text{-}4}$) is 60 μm/0.12 μm and that of the second stage ($M_{6\text{-}9}$) is 180 μm/0.12 μm. From simulations, the two stages provide 20 dB power gain, while consuming 4 mA from 1.5 V supply voltage. The simulated output P_{1dB} is higher than 0 dBm.

3.5 Up-Conversion Mixer

Figure 3-18 shows a circuit schematic of the up conversion mixer. A double balanced Gilbert cell active mixer is used to get higher gain and output power. From the measurement results of [27], the gain of mixer is about 1 dB and the output P_{1dB} is about -11 dBm, while consuming 4.5 mA from 1.5-V supply voltage. In order to deliver 10 dBm to the antenna, the following RF amplifiers must provide at 20 dB power gain.

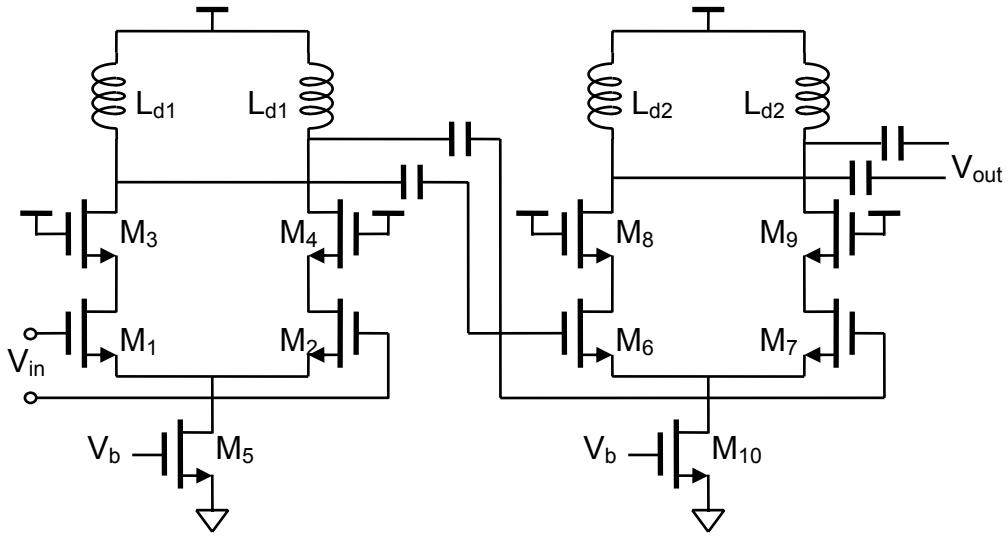


Figure 3-17 Schematic of the IF amplifier

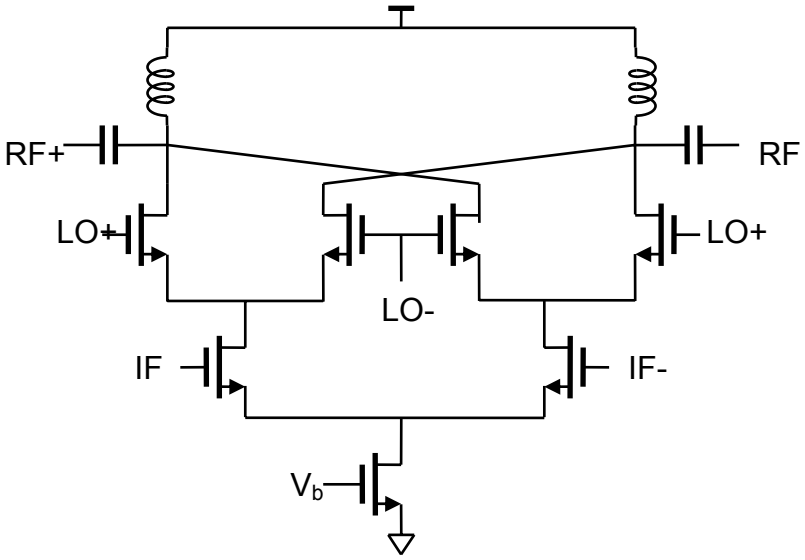


Figure 3-18 Schematic of the up conversion mixer

3.6 High Efficiency Power Amplifier

3.6.1 Introduction to CMOS Power Amplifier

The power amplifier is the most difficult RF block in the transmitter. The PA is typically the most power-hungry building block, which makes the PA efficiency crucial. Compared to the transistors in III-V technology, the MOS transistor is slower, which makes it more difficult to get high efficiency, especially around 20 GHz. The continuous

scaling down of supply voltage due to the lower breakdown voltage of MOS transistors also limits the output power.

The efficiency of power amplifier is defined by two metrics [28], [29]. The drain efficiency, η, is equal to the power delivered to the load (usually at the first harmonic) divided by the power drawn from the supply. The power-added efficiency (PAE) is the difference between the input and output powers divided by the supply power. If the PA has a relatively large power gain, the drain efficiency is equal to PAE. In addition, the output spurs and harmonics of the PA in the μNode system must also satisfy the wireless standards and FCC rules.

Figure 3-19 shows a simplified schematic of a typical common-source PA. The RF chock (RFC) ideally has no voltage drop, thus, it will not affect the voltage swing at the drain node. The matching network provides bandpass filtering at the fundamental frequency. More importantly, it transforms the 50-Ω load to lower impedance. For the common-source configuration, the voltage at the drain node can only swing from 0 to $2V_{DD}$, thus the maximum power delivered is VDD2/2RL. By transform the load to a lower value, higher output level can be achieved. It should also be noted that the output stage of PA generally includes only one transistor instead of the cascode, because the large current would introduce more loss with more active devices in the signal path [29]. However, for the single-transistor amplifier in Figure 3-19, the gate and drain nodes have anti-phase voltage stresses to the gate oxide. The gate to drain breakdown is becoming more and more severe limitation in CMOS, because the thinner gate oxide thickness in shorter channel length device. Thus, some circuits [30], [31] have utilized the cascode structure instead of the classical topology in Figure 3-19.

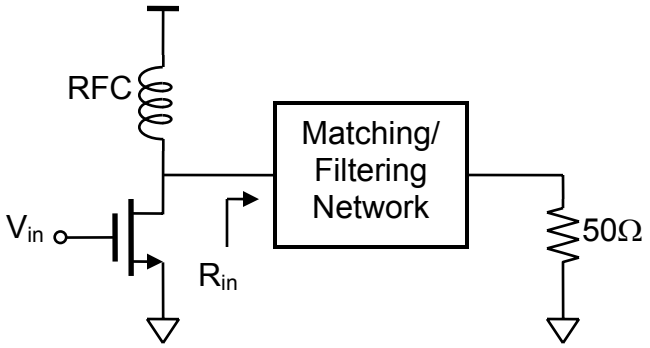


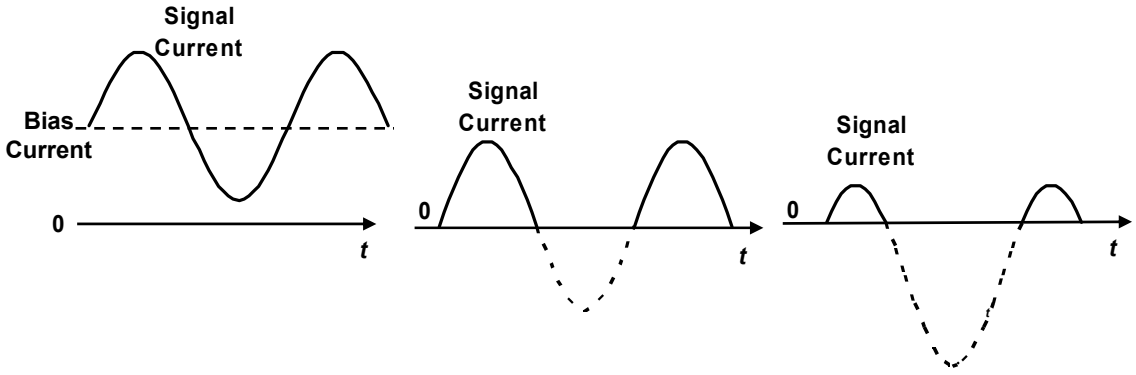
Figure 3-19 Simplified schematic of the power amplifier

3.6.2 Class A, B, AB, and C Power Amplifier

The power amplifiers are traditionally categorized by classes: A, B, C, D, E, F, etc. In class A, B, and C power amplifiers, the output transistor current and voltage waveforms are sinusoidal, and they are similar to the standard small signal amplifier. However, the signal current in a PA is a substantial fraction of the bias level, and one would therefore expect potentially serious distortion. In narrowband operation, the high-Q matching and filtering network solve the distortion problem, so that, overall linear operation prevails. These PAs are primarily distinguished by bias conditions. In a class A amplifier, the transistor operates linearly across the full input and output range; in a class B amplifier, the transistor conducts for half of the carrier period, while in a class C amplifier, the transistor is on for less than a half of the cycle. They can also be classified using the conduction angle, θ. Figure 3-20 shows the signal current in these three amplifiers.

In a class A power amplifier, if the drain voltage in Figure 3-19 is a sinusoid having a peak-to-peak voltage of approximately $2V_{DD}$, then the maximum power delivered to the matching network is equal to $V_{DD}^2/(2R_{in})$. For the drain voltage to reach $2V_{DD}$, the RFC must provide current of V_{DD}/R_{in}. Since the RFC current is relatively constant, the power

drawn from the supply equal to V_{DD}^2/R_{in}. Therefore, the maximum drain efficiency is equal to 50%.



(a) Class A (b) Class B (c) Class C

Figure 3-20 Transistor currents for class A, B, and C power amplifiers.

In a class B power amplifier, since the transistor only conducts half of the carrier period, the maximum power delivered to the load is only a half of class A amplifier, or $V_{DD}^2/(4R_{in})$. The average current drawn from V_{DD} is given by

$$I_{DD,avg} = \frac{1}{T}\int_0^{T/2} V_{DD}/R_{in} \sin \omega t = V_{DD}/(\pi R_{in}) \tag{3-5}$$

The maximum efficiency is therefore equal to $\pi/4 \approx 79\%$. In audio systems, class AB power amplifiers operating between class A and B are widely used. In these amplifiers, the transistors conduct slightly more than a half of period. A push-pull configuration makes sure that at least one transistor is on during an entire cycle. The class AB shows good efficiency, high output power as well as good linearity.

In a class C stage, the conduction angle, θ, is less than 180^o. As θ decrease, the transistor is on for a smaller fraction of the period, thus dissipating less power. For the same reason, however, the power delivered to the load also decreases. If the current drawn by the transistor is assumed to be a piece of a sinusoid and the output voltage is a

sinusoid with a peak voltage equal to V_{DD}, then the efficiency can be calculated as a function of θ. As described in [28], [29], the efficiency is given by

$$\eta = \frac{1}{4}\frac{\theta - \sin\theta}{\sin(\theta/2) - \theta/2\cos(\theta/2)} \tag{3-6}$$

varying from 50% for $\theta = 360^{o}$ (class A) to 79% for $\theta = 180^{o}$ (class B) to 100% for $\theta = 0^{o}$. Though the class C stage could provide a maximum efficiency as high as 100%, the actual power delivered to the load is

$$P_{out} \propto \frac{\theta - \sin\theta}{1 - \cos(\theta/2)} \tag{3-7}$$

The quantity drops to zero as the conduction angle vanishes. For this reason, a true class C power amplifier is not suitable to some portable transceivers, where the output power is also a great concern.

3.6.3 High Efficiency Class E Power Amplifier

The main premise in class A, B and C amplifiers has been that output voltage and current waveforms are sinusoid (or a section of a sinusoid), thus limiting the efficiency of the class A and B and the output power of class C [28]. In these amplifiers, the output matching network is designed with the assumption that the transistor operates as a current source. While in class D, E and F stages [32], [33], the transistor operates as an ideal switch, rather than a voltage-controlled current source. They are nonlinear amplifiers that achieve efficiencies approaching 100% while delivering full power.

Figure 3-21 shows a schematic of a class E power amplifier [32]. It consists of an output transistor M_1, a grounded capacitor C_1, and a series network C_2 and L_1. The RFC has high impedance at the frequency of operation and C_1 includes the drain junction capacitance of M_1. To ensure 100% power efficiency, the power consumption of the

transistor M_1 must be zero, i.e. the drain voltage V_X and transistor current I_{D1} cannot be non-zero at the same time. Therefore, the values of C_1, C_2, L_1, and R_L are chosen such that the drain voltage of M_1, V_X, satisfies three conditions [32]:

(1) As the switch turns off, V_X remains low long enough for the current to drop to zero.

(2) V_X reaches zero just before the switch turns on.

(3) dV_X/dt is also near zero when the switch turns on.

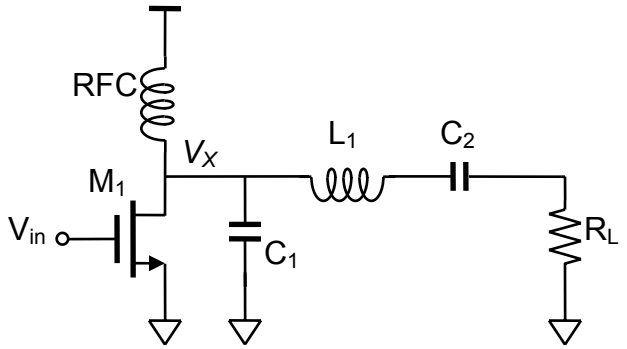


Figure 3-21 Class E power amplifier

Figure 3-22 shows the simplified model of the class E stage. The transistor can be modeled as a switch with small resistance. When the switch is on, a near linearly increasing current is built up through the inductor. As the turn-on resistance of the transistor is nearly zero, the voltage drop across the transistor is nearly zero and there is no power consumption. At the moment the switch is turned off, this current is steered into the capacitor, causing the voltage across the switch to rise. The tuned network is designed such that in steady state, V_X returns to zero with a zero slope, immediately before the switch is turned on. The bandpass filter then selectively passes the fundamental component to the load, creating a sinusoidal output.

From [32], the value of the inductor and capacitors can be chosen as follows:

$$L = \frac{QR}{\omega} \tag{3-8}$$

$$C_1 = \frac{1}{\omega R(\pi^2 + 1)(\pi / 2)} \approx \frac{1}{5.447\omega R} \tag{3-9}$$

$$C_2 = C_1(\frac{5.447}{Q})(1 + \frac{1.42}{Q - 2.08}) = \frac{1}{\omega QR}(1 + \frac{1.42}{Q - 2.08}) \tag{3-10}$$

The Q should be as high as possible while satisfying the bandwidth requirement. Once the Q is chosen, the PA can be designed in a straightforward manner, using the equations given.

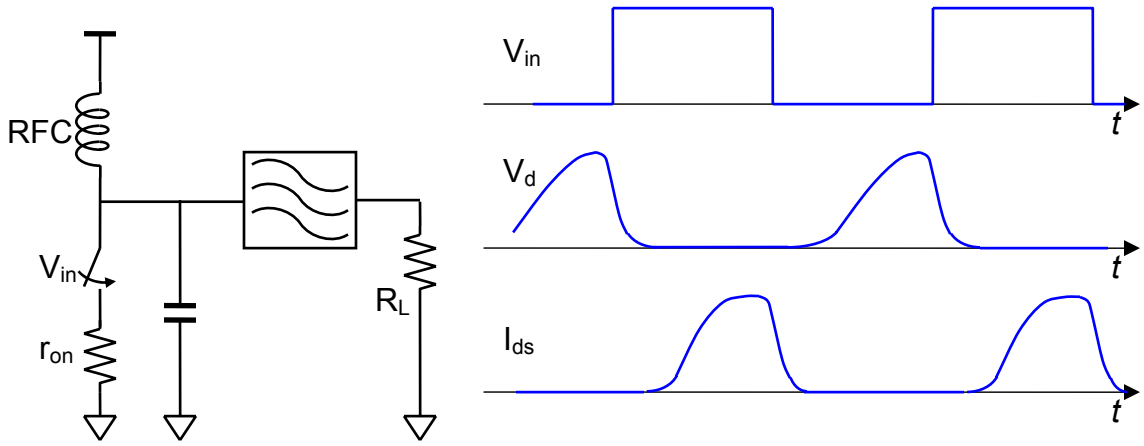


Figure 3-22 Simplified class E stage model and its voltage and current waveform

However, an ideal RFC and switch is not available in integrated circuits. A technique using the relative low Q on-chip inductors and slow transistor is described in [34]. A real class E power amplifier also includes an impedance transferring network [32], as shown in Figure 3-23. The two series inductors are also usually merged as one. It should also be noted that 100% efficiency is never possible because the transistor and matching network always have loss. The non-zero turned-on resistance and non-zero switch time limits the efficiency. The transistor is further away from an ideal switch

when the operating frequency is higher. In a practical circuit, PAE of 40-50% is usually expected.

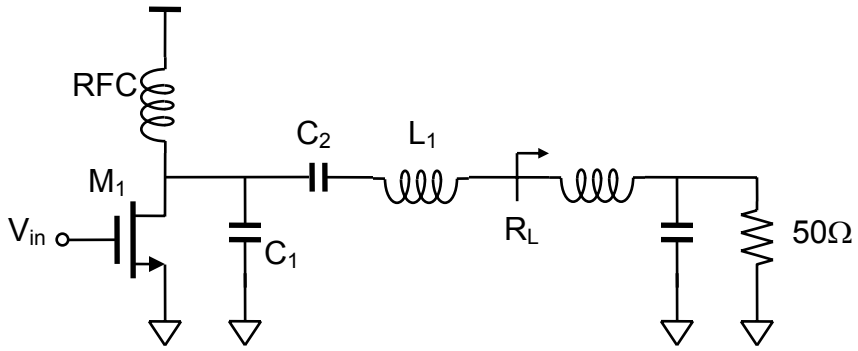


Figure 3-23 Class-E power amplifier with impedance transformation network

A drawback of class E power amplifier is the large peak voltage that the switch sustains in the off state, which is about $3.56V_{DD}$ in an ideal case, which demands high transistor breakdown voltage. However, in real case, especially at higher frequencies, the transistor is not a perfect switch, thus the maximum drain voltage is lower than the theoretical value.

Compared with linear power amplifiers, which are usually optimized for maximum gain and linearity, the switching class-E power amplifiers provide much higher efficiency. They are particularly well suited for modern communication systems using a constant envelope modulation, such as the Zigbee wireless personal area networks (WPAN'S) and GSM cellular networks, as well as the constant envelope MSK-like modulation used in the μNode.

3.6.4 Circuit Description

Figure 3-24 shows the schematic of fully-integrated CMOS power amplifier designed using the UMC 0.13-μm process. It consists of a two-stage cascode amplifier, a common source driver, and an output stage. Due to the limited voltage headroom,

common-source amplifiers are used in the last two stages. The sizes of transistors in these four stages are 14, 24, 40, and 100 μm, respectively. The cascode amplifiers are used to provide sufficient gain, good input matching and isolation from the last two stages which potentially could oscillate.

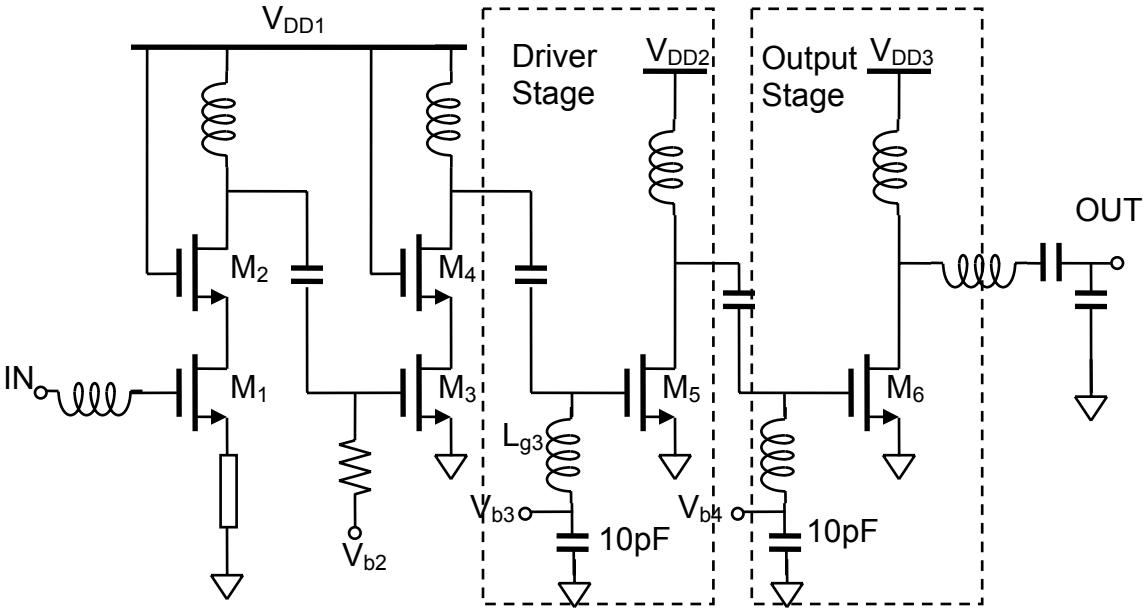


Figure 3-24 Schematic of the fully-integrated CMOS power amplifier

Figure 3-25 shows the schematic of the output stage. The matching network components, L_1, L_2, C_1, and C_2, have to be properly selected as described above. The shunt capacitor at the drain of the transistor is omitted because the capacitance from the drain of the transistor is already large enough. To lower the matching network loss, the inductors L_1 and L_2 are formed with the top two copper layers, which results an effective thickness of 1.6 μm. The metal traces are 3.6-μm wide and 4-μm above the polysilicon patterned ground shield. The effective series resistance of two inductors is about 5 Ω. The shunt capacitor C_2 transfers the 50 Ω load to around 40 Ω at 20 GHz. In the layout, C_2 is formed by absorbing the pad capacitance (~48 fF) and shunt parasitic of the C_1 (~32 fF). A shunt inductor (L_g) is placed at the gate of output transistor to tune out the gate

capacitance, which reduces the value of the coupling capacitor, but as will be discussed below, also makes the circuit more potentially unstable.

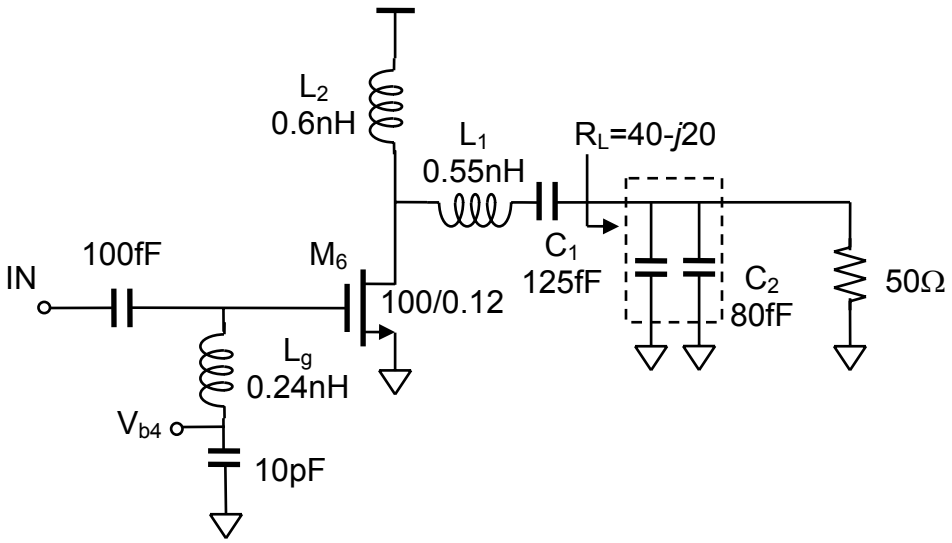


Figure 3-25 Schematic of output stage

3.6.5 Mode Locking Technique

Near 20 GHz, the common source driver stage is potentially unstable due to the feedback through C_{gd}, which is one of the reasons of the wide use of cascode amplifiers. Figure 3-26 shows the simplified small signal model of the common-source amplifier, which includes a transconductor and two resonant networks connected by C_{gd}.

Due to C_{gd}, the output of the amplifier is fed back to the input. The open loop gain of this circuit can be written as,

$$T(s) = \left(-g_m \left(Z_d \,//\left(Z_g + \frac{1}{sC_{gd}} \right) \right) \right) \bullet \left(\frac{Z_g}{Z_g + 1/(sC_{gd})} \right) \tag{3-11}$$

This expression consists of two parts: the gain from the gate to drain and voltage divider for the feedback path. To start oscillation, the loop gain should be larger than 1 and the phase change must be 360 degree. For the network at the gate node, below its resonant

frequency, the network is inductive with an equivalent inductor $L_{g,equ}$ and a series resistor $R_{g,Eq.}$ The transfer function of voltage divider between C_{gd} and the network is

$$\frac{Z_g}{Z_g + 1/(sC_{gd})} = \frac{j\omega L_{g,equ} + R_{g,equ}}{j\omega L_{g,equ} + R_{g,equ} + 1/(j\omega C_{gd})} = \frac{-\omega^2 L_{g,equ} C_{gd} + j\omega C_{gd} R_{g,equ}}{1 - \omega^2 L_{g,equ} C_{gd} + j\omega C_{gd} R_{g,equ}} \tag{3-12}$$

When $\omega L_{g,equ} >> R_{g,equ}$ or Q is high, at frequencies below $1/\sqrt{L_{g,equ} C_{gd}}$, this voltage divider provides a phase shift close to 180°. Meanwhile, when $\omega L_{g,equ} << R_{g,equ}$, it gives a phase shift of 0 to 90°. To satisfy the oscillation condition, the first term in Eq. (2.10) needs to provide 180° phase shift or the tank at drain node must resonate at the oscillation frequency, and the second term must provide another 180° phase shift. Therefore, the resonant frequency of $L_{g,equ}$-C_{gd} circuit is set higher than the oscillation frequency and the high Q inductive load at the gate node is used.

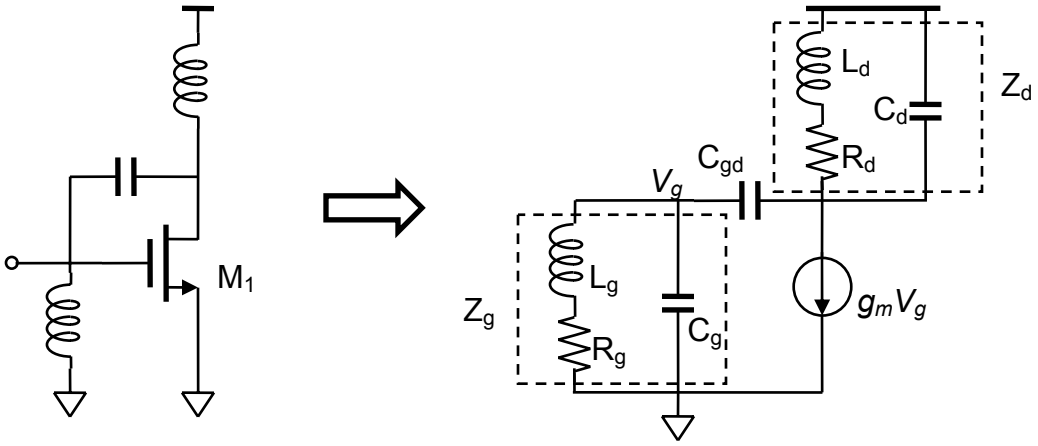


Figure 3-26 Small signal model of the common source amplifier

The output stage is designed to drive 50-Ω load, so the voltage gain is not high. On the other hand, the driver stage is designed to achieve high voltage gain. Because of this, it is easier to make the driver stage oscillate. To provide good input matching, two stage

cascode amplifiers are used at the input. The gates of the common-gate transistors are connected to a bypass capacitor right beside the transistors to make the cascode stage stable.

The instability is generally not desirable in power amplifiers. However, if the self-oscillation can be locked by the input, the instability actually increases the gain of the circuit and reduces the drive requirement for switching the output transistor. This is called mode-locking (also known as injection-locking) and has been previously utilized in power amplifiers [35], [36]. Usually, cross-coupled transistors are used to provide the positive feedback (or negative resistance). Since the driver in this work is unstable, additional positive feedback is not included. To study the benefits of mode-locking, a power amplifier without mode-locking is also implemented. This is accomplished by removing the gate inductor of the driver stage (L_{g3} in Figure 3-24). In addition, a 3-kΩ resistor is added for dc biasing.

3.6.6 Experiment Results

The power amplifier was fabricated in the UMC 0.13-μm logic CMOS process with eight copper layers and a substrate resistivity of 20 Ω·cm. Another PA without using mode locking is fabricated for comparison. Figure 3-27 shows the die photograph of the two single-ended power amplifiers. The two amplifiers together occupy an area of 0.92 mm x 0.85 mm including bond pads.

The large signal measurements were performed using the setup shown in Figure 3-28. The output is connected to a power meter with an HP8485A 50MHz-26.5GHz power sensor. The losses of measurement setup are de-embedded using a thru-measurement. The loss at the output end (from the probe and short SMA cable) of ~0.7

dB at 18 GHz was measured with a network analyzer. An Agilent E4448A 50-GHz spectrum analyzer is also used to monitor the output spectrum of power amplifier.

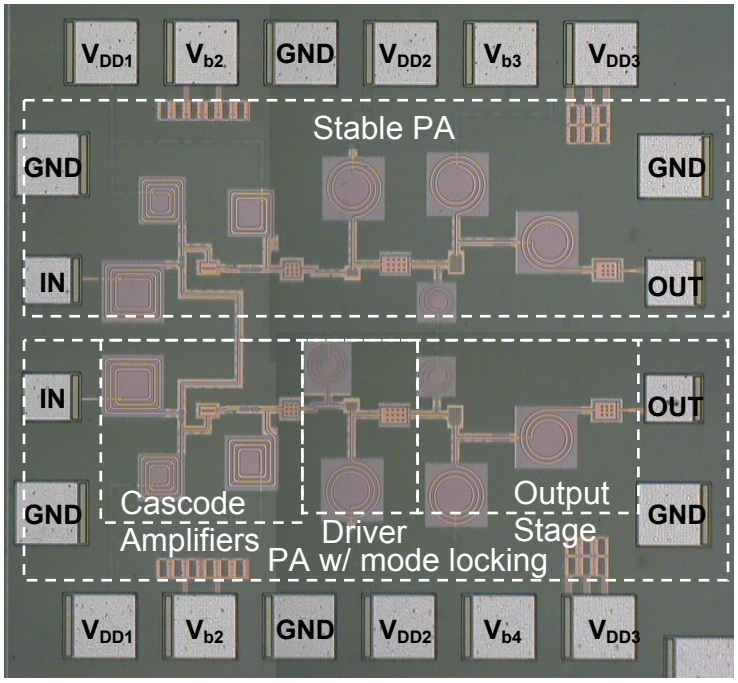


Figure 3-27 Die photograph of the chip containing two single-ended power amplifiers

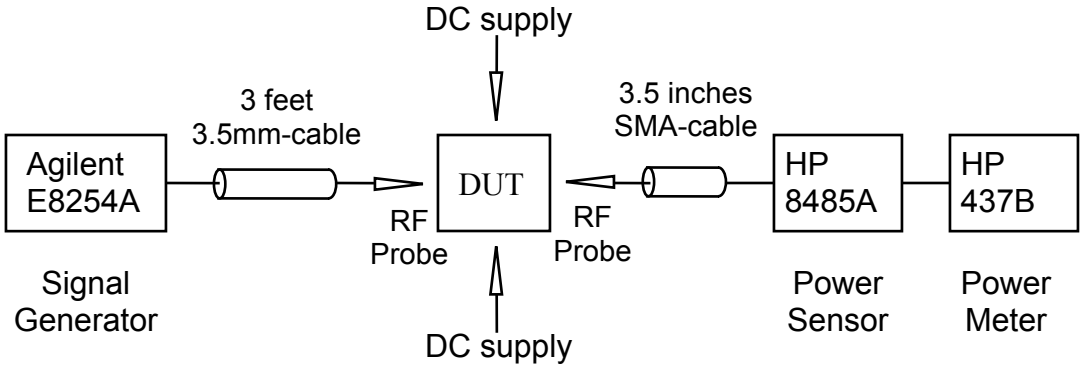


Figure 3-28 PA measurement setup

With 1.5-V supply voltage and proper gate bias (0.5~0.7 V), the power amplifier shows self-oscillation with ~1-dBm peak power near 17.4 GHz. The self-oscillation is lower than designed frequency of 20 GHz probably because the gate to drain capacitance (C_{gd}) is larger than expected. As the input signal level applied at the 'IN' node in Figure 3-24 is increased, the self-oscillation becomes weaker until finally the circuit is forced to

oscillate at the same frequency as the input. Figure 3-29 shows the output spectrum with 17.6 GHz input. With -42-dBm input power level, the self-oscillation cannot be locked, and the self-oscillation peak and inter-modulation products are shown beside the main peak. At -36-dBm input power, the circuit locks to the input signal. Figure 3-29(b) shows that the output power is more than 10dBm when input power is -10dBm. When the input frequency is farther away from the self-oscillation frequency, the circuit becomes more

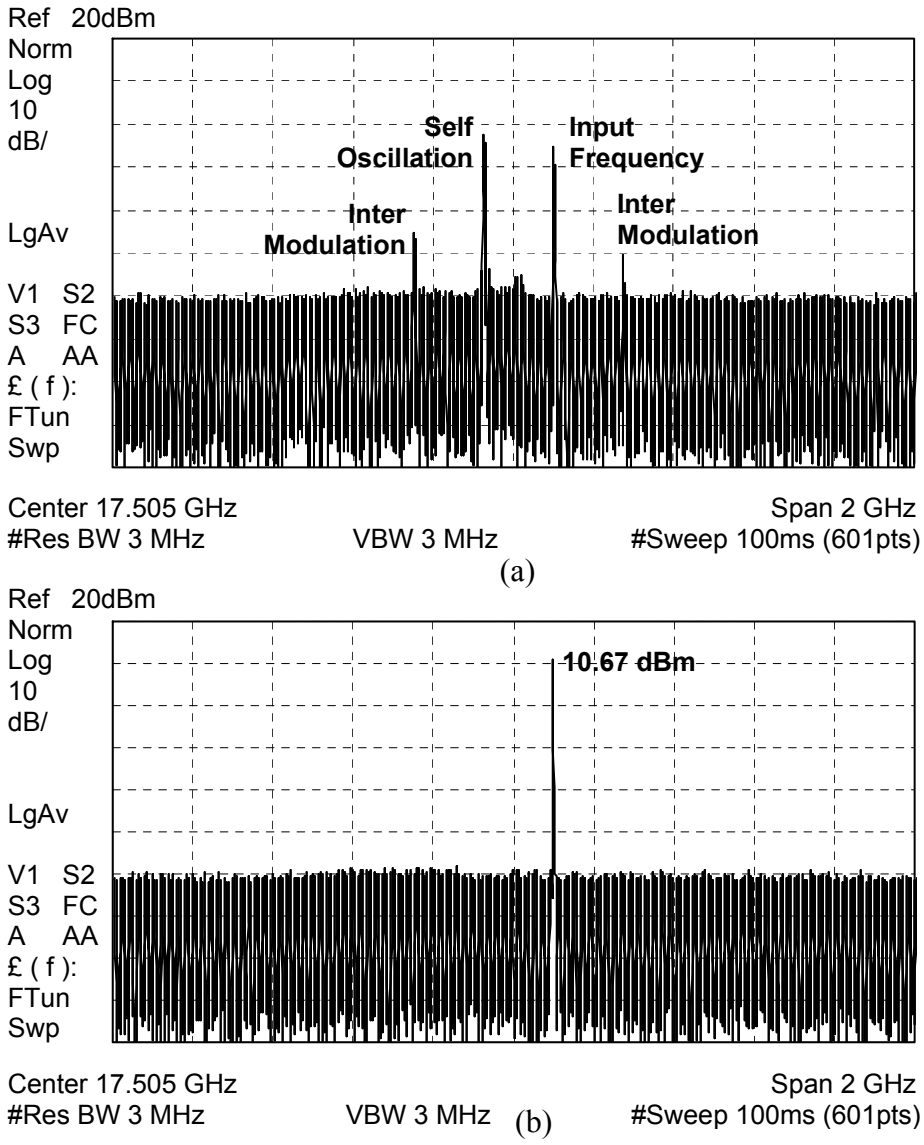


Figure 3-29 Output spectrum (a) unlocked, input:-42dBm (b) locked, input: -10dBm. (Losses from the cable and connector have been de-embedded)

difficult to be locked. At -10-dBm input power level, the circuit can be locked from 15.5 to 21.4 GHz. In addition, when a 20-GHz -10-dBm FM signal with 16-MHz maximum frequency deviation and 1 kbps to 1 Mbps data rate is used as input, the PA locked to the input, while preserving the shape of spectrum. A drawback of the circuit is that the minimum output power level is above 2 dBm when the PA is locked. If an output level below this is desired, the bias voltage can be lowered, making the oscillator easier to lock or stop the oscillation. The self-oscillation disappears when the gate bias of the driver stage is below 0.45 V.

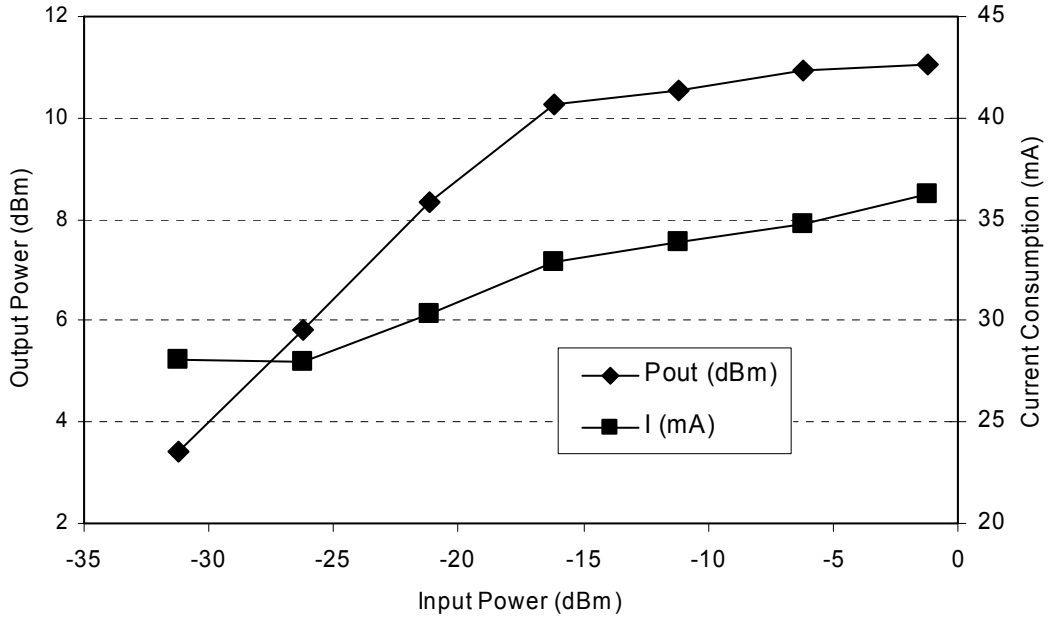


Figure 3-30 Output power and current consumption as function of the input power for the 18 GHz power amplifier. (Supply voltage: 1.5 V)

Figure 3-30 shows the output power and current consumption as function of the input power for the PA with mode-locking. At 18 GHz, with -5-dBm input power, a single-ended output power of 10.9 dBm is obtained while drawing 35 mA from a 1.5-V supply. The maximum power added efficiency including all the amplifiers and driver is 23.5% (Figure 3-31). Because all the four stages are integrated together, the power at the

gate of the last stage cannot be measured. Here the current consumptions of all stages are included in the calculation of the PAE. The last stage consumes 22 mA and drain

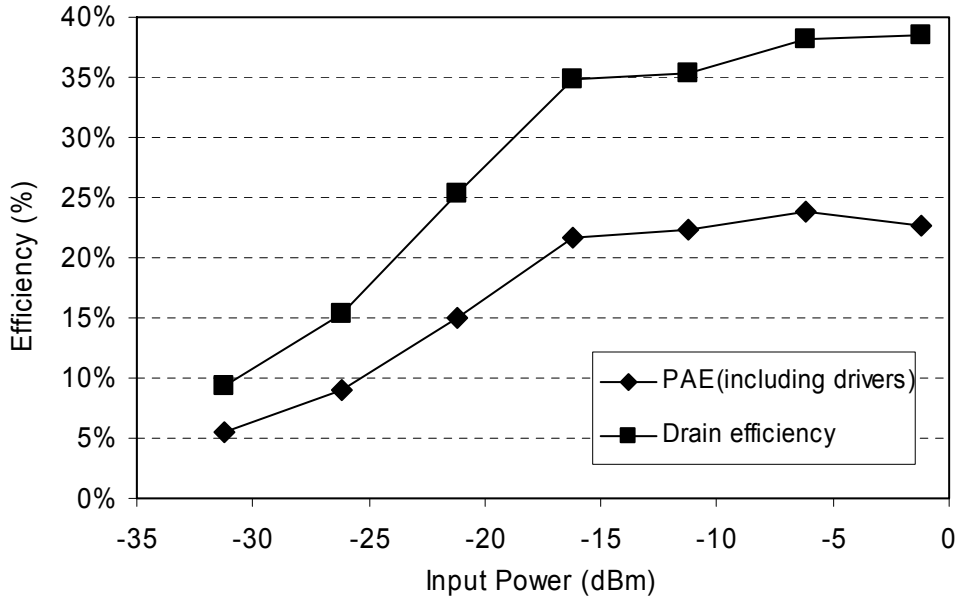


Figure 3-31 PAE and drain efficiencies as a function of the input power of the 18-GHz power amplifier (Supply voltage: 1.5 V)

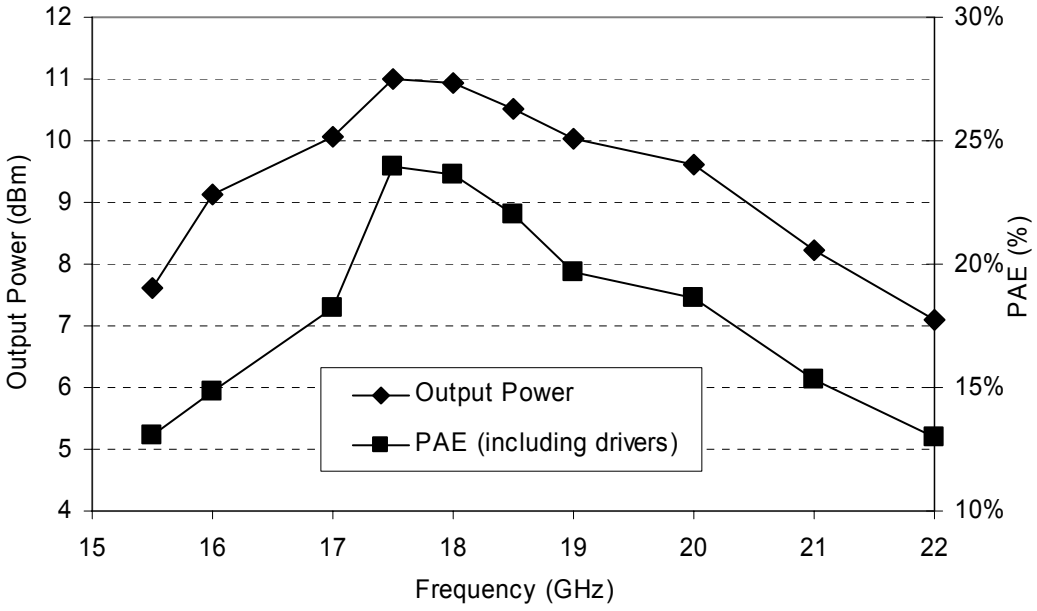


Figure 3-32 Output power and PAE as a function of the frequency of the 18-GHz power amplifier. (Supply voltage: 1.5 V)

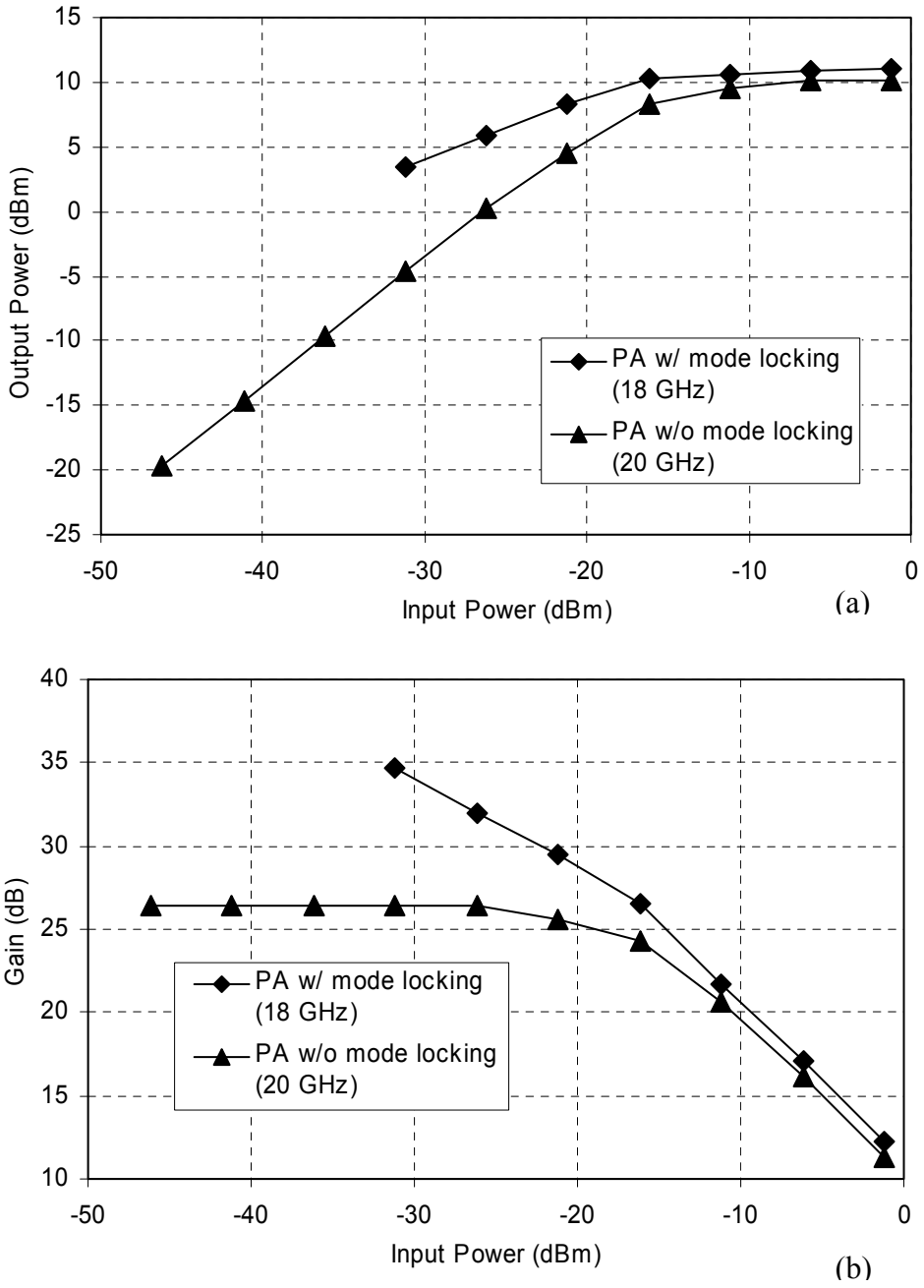


Figure 3-33 Output power and gain as function of the input power for the two power amplifiers.

efficiency of the last stage is about 38%. Further increase the input power leads to slightly higher output, but larger current consumption and lower efficiency. At 1.2 V supply, the PA provides 7.5-dBm saturated output power and 18.6% maximum PAE,

while drawing 24.5 mA current. Figure 3-32 shows the saturated output power and PAE from 15.5 to 23 GHz at 1.5 V supply. The PA with mode-locking provides more than 8-dBm saturated output power over a 5-GHz band.

The result for the PA without mode-locking is compared in Figure 3-33. This PA achieves 10.2 dBm peak output power and 20.5% maximum PAE at 20 GHz. Because the gain is lower, it requires 6-8 dB higher input power to get the same output level. The use of mode-locking technique leads to slightly larger saturated output power and efficiency. More importantly, it reduces the input power requirement of class-E amplifier.

3.6.7 Summary and Conclusions

An 18-GHz 10.9-dBm class-E power amplifier with 23.5% maximum PAE is demonstrated in the UMC 0.13-μm CMOS technology. The mode-locking technique is used to force the oscillating driver to follow the input signal. The performance of power amplifier in this work is compared to that of the previously reported power amplifiers operating near 20 GHz in Table 3-2. The PA presented in this work shows significantly higher efficiency and lower input requirement than that for the previously reported CMOS PA operating near 20 GHz. This work suggests CMOS technology is a viable candidate for building a fully-integrated transmitter operating near 20 GHz.

Table 3-2 Comparisons of power amplifiers operating near 20 GHz

Ref.	Freq. [GHz]	Vdd [V]	Small Signal Gain [dB]	Pout [dBm]	Output	PAE	Technology
This work	18	1.5	34	10.9	Single-ended	23.5%	0.13-μm CMOS
	20	1.5	26	10.2	Single-ended	20.5%	0.13-μm CMOS
[31]	24	2.8	7	14.5	Single-ended	~6%	0.18-μm CMOS
[37]	24	N/A	N/A	18	Differential	26%	0.13-μm GaAs

3.7 Summary

In this chapter, the key RF blocks of the transmitter implemented in the UMC 0.13-μm CMOS technology were presented. These blocks were a quardrature generator (frequency divider), a constant envelope modulator, an IF amplifier, an up-conversion mixer, and a high efficiency power amplifier. A complete transmitter chain could be built by integrating these blocks.

CHAPTER 4
WIRELESS COMMUNICATIONS USING ON-CHIP ANTENNAS

4.1 Review of On-Chip Antennas

4.1.1 Introduction to On-Chip Antennas

The research on antennas fabricated on semi-conducting substrates dates back to late 1980's [38]. An on-chip antenna integrated with a 95-GHz IMPATT diode oscillator on a high resistively silicon substrate and an on-chip antenna integrated with a 43.4-GHz IMPATT diode oscillator on a GaAs substrate [39] have been reported in 1986 and 1988, respectively. High resistivity silicon substrates have also been used to fabricate MEMS based antennas operating at 90 to 802 GHz [40]. However, use of IMPATT diode circuits limits the types of radios that can be built. Furthermore, the substrates are not compatible with the low cost mainstream silicon process technologies.

For on-chip antennas, the antenna size is limited by the size of the chip. Therefore, to achieve usable antenna efficiency while limiting the physical size of the antenna requires operation at higher frequencies (e.g., > 15 GHz), with corresponding to smaller wavelengths. As discussed in the preceding chapters, the speed improvement of silicon devices has made implementation of silicon integrated circuits operating at 20 GHz and higher feasible. At 24-GHz, a quarter wave dipole antenna needs to be only 3.2 and ~1.5 mm in free space and silicon, respectively, making integration of an antenna for wireless communication possible.

An on-chip antenna could potentially be used to relieve the bottleneck associated with global signal distribution inside integrated circuits. The first proposed uses of on-

chip antenna fabricated in conventional foundry process are clock distribution [41] and data communication [41], [42]. Clock transmitter and receiver with on-chip antennas for intra-chip [42]-[45] and inter-chip [46] wireless connection have been demonstrated. Using one of the clock receivers, a 14.3-GHz 20-dBm signal from a 2-mm long zigzag dipole transmitting antenna 40 cm away has been successfully picked up [44]. An 18-GHz clock transceiver circuits with start-up initialization and programmable delays successfully demonstrated the wireless clock distribution using an on-chip antenna pair [45]. A signal from a transmitter incorporating a 10-GHz VCO, buffer and antenna fabricated in a BiCMOS technology [47] has also been picked up by an external horn antenna. These suggest the potential to communicate over free space using CMOS and BiCMOS radios with on-chip antennas.

4.1.2 Measured Performance of On-Chip Dipole Antenna

Figure 4-1 shows a micrograph of an on-chip antenna. The antenna is a 3-mm long zigzag dipole with a bend angle of 30º similar to that reported in [3], [9]. Compare to a linear dipole antenna, the zigzag one possesses higher efficiency [48]. The 3-mm length corresponds to around λ/4 in free space at 24 GHz. The antenna is formed by shunting all eight metal layers. The metal width is 24 μm. Figure 4-2 shows the input refection coefficient, $|S_{11}|$, of the on-chip antenna between 20 and 26 GHz. $|S_{11}|$ is below -10 dB over this frequency range. The measured input impedance is $75 - j23\Omega$ at 24 GHz.

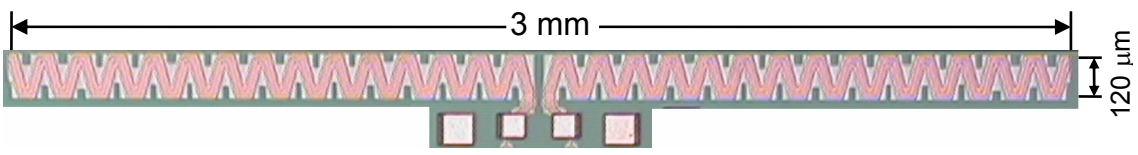


Figure 4-1 Photograph of an on-chip antenna

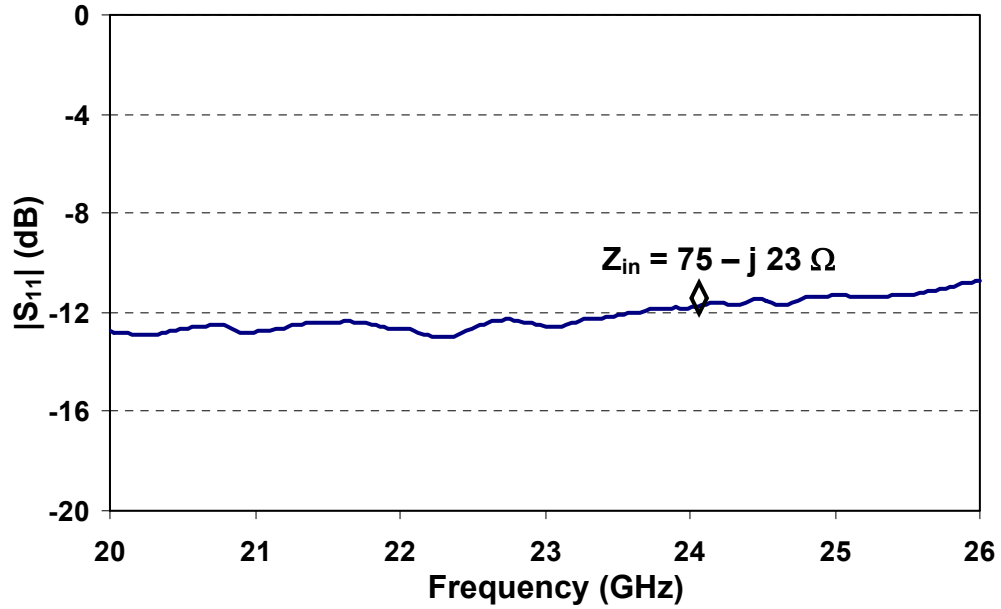


Figure 4-2 Input reflection coefficient of a 3-mm zigzag on-chip antenna

The power gain of an on-chip antennas pair is measured in real environments using mobile probe stations [9]. Figure 4-3 shows a measurement environment. A signal generator provides a 24-GHz signal to the transmitting on-chip antenna and the signal is picked up using another on-chip antenna at different locations. The received signal power level is measured using a spectrum analyzer. By de-embedding the cable and probe loss, the power gain of an antenna pairs can be obtained. Figure 4-4 shows the measured antenna pair gain in the lobby as a function of the distance with different height to the ground. The antenna pair gain, G_a, for the 5 meters separation is between –93 and –104 dB, depending on the height to the ground.

By using the Friis transmission equation, the free space path loss is

$$\frac{P_r}{P_t} = \left(\frac{\lambda}{4\pi R}\right)^2 G_t G_r \,, \tag{4-1}$$

where λ is the wavelength in free space, R is the distance between an antenna pair, and G_t and G_r are the transmitting and receiving antenna gains. If isotropic antennas with unity

gain are used, the path loss at 24 GHz can be calculated as -74 dB with 5-m spacing. Therefore, the power gain of the on-chip antennas pair is -30 to -20 dB lower, or each of the on-chip antenna's gain is between -15 and -10 dBi in the lobby environment. This lower power gain is mainly due to the lossy silicon. Referring back to system link budget in Table 2-1, the on-chip antenna despite the loss associated with the conductive substrate should be sufficient for the μNode application with –98-dBm sensitivity [3], [9]. The antennas pair gain is increased by about 10 dB when the substrate is thinned to from 700 μm to 100 μm [9].

Figure 4-3 Antennas pair measurement environment (lobby)

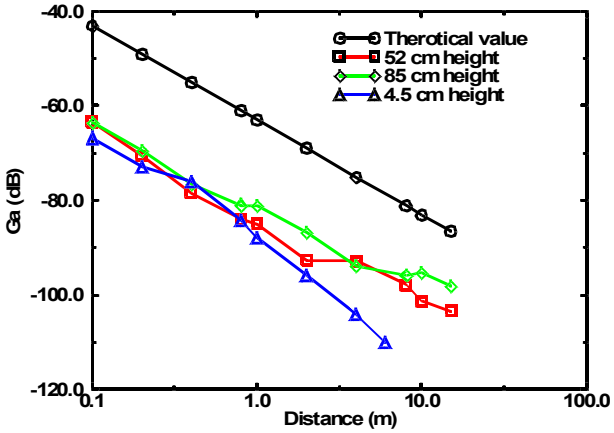


Figure 4-4 Antenna pair gain vs. distance in the lab for 3-mm zigzag antennas on a 20 Ω·cm, 670-μm thick substrate with a 3-μm oxide layer. The measurement frequency is 24 GHz [9].

4.2 Test Transmitter with an On-Chip Antenna

4.2.1 Circuit Architecture

In order to demonstrate the feasibility of using an on-chip antenna for wireless communications, a test transmitter was fabricated and tested. Figure 4-5 shows a block diagram of the chip. The circuit includes an IF amplifier, an up-conversion mixer, two-stages RF amplifiers, and an on-chip antenna. The IF and RF amplifiers utilize the cascade topology, and the mixer utilizes the double balanced Gilbert cell, as described in Chapter 3.

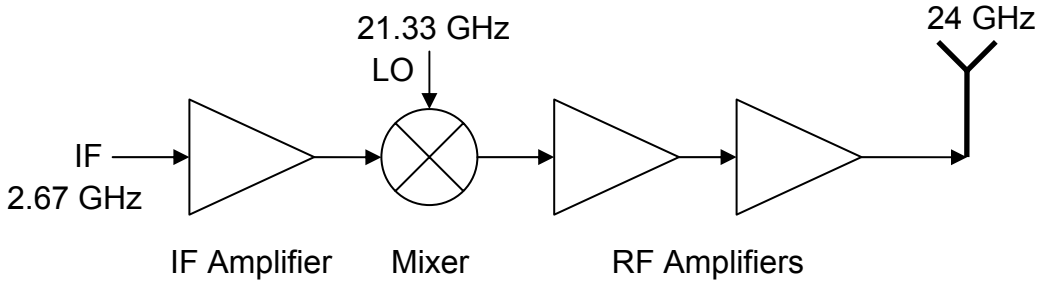


Figure 4-5 Block diagram of the test chip with an on-chip antenna

4.2.2 Experiment Results

The chip was fabricated in the UMC 0.13-μm logic CMOS process. Figure 4-6 shows the micrograph of test chip. The antenna occupies 3.0 mm x 0.12 mm and the other part occupies 1.1 mm x 0.85 mm including bond pads. The zigzag antenna is formed using all 8 metal layers available and the width of the metal trace is 24 μm.

The chip is first characterized on-wafer without the antenna. Figure 4-7 shows the input and output matching of the circuit. The $|S_{11}|$ is lower than -10 dB from 2.5 to 3 GHz and $|S_{22}|$ is lower than -10 dB from 22.5 to 25.5 GHz. Figure 4-8 shows the measured output power as function of input power. The LO signal power is about 3 dBm. The conversion gain from these four stages is about 20 dB. The circuit provides an output P_{1dB}

of around -4 dBm and a saturated output power of around -1.5 dBm, while consuming 15 mA from a 1.2-V supply. The current consumptions of IF amplifier, mixer, and RF amplifiers are 1.8 mA, 4.8 mA, and 8.4 mA, respectively. With a 1.5-V supply, the saturated output power is about 0 dBm and the current consumption is 28 mA.

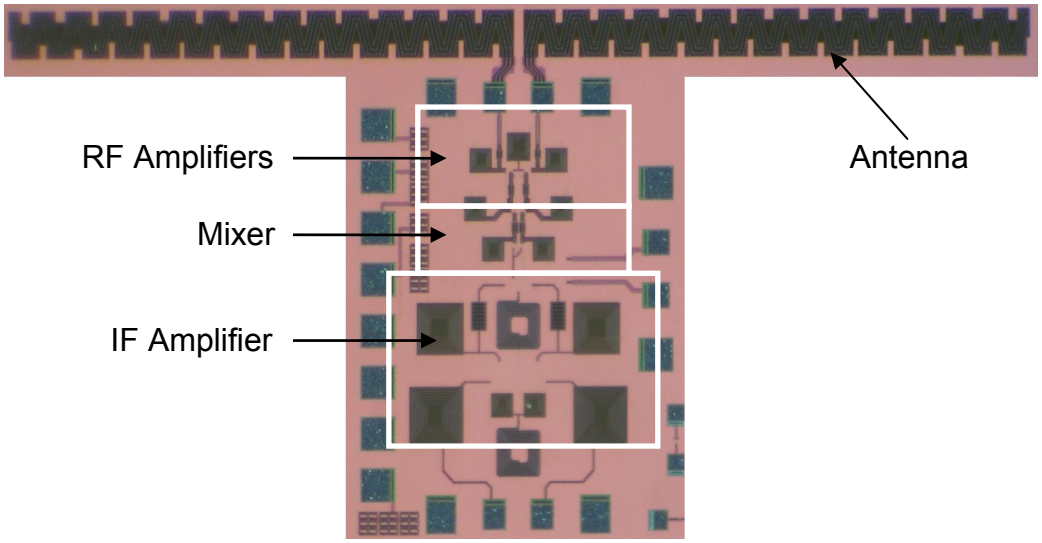


Figure 4-6 Micrograph of the test transmitter with an on-chip antenna

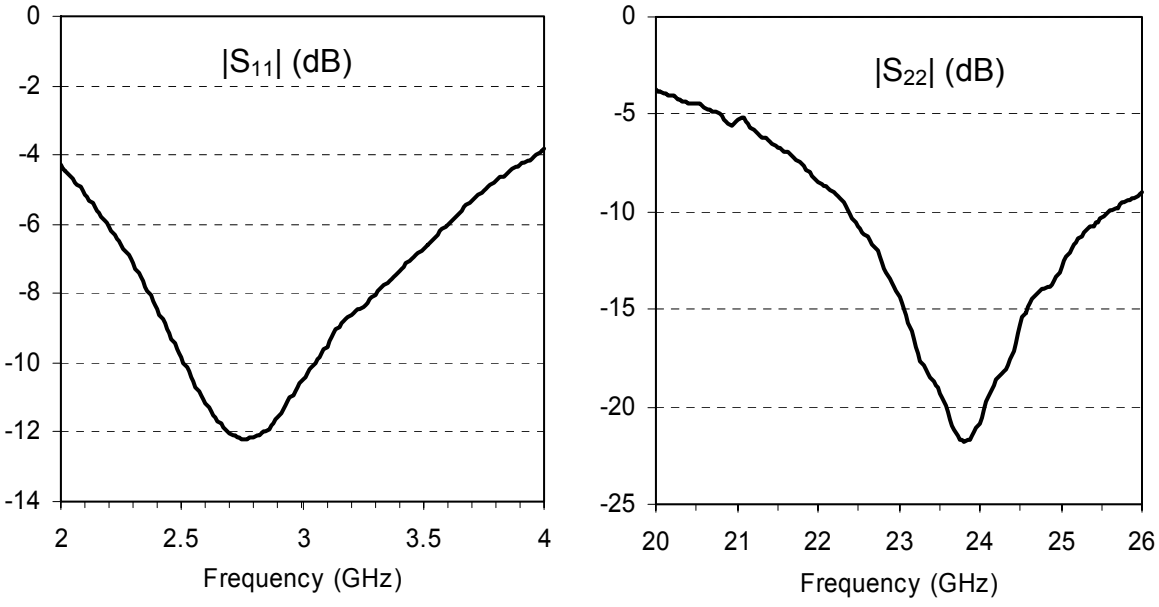


Figure 4-7 Input and output matching of the test transmitter

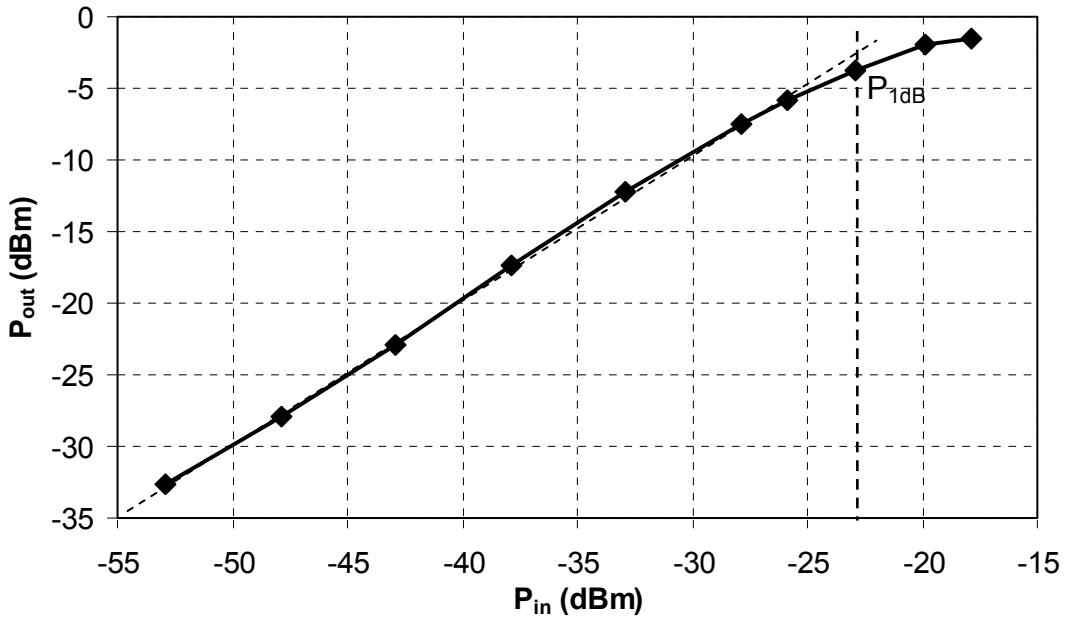


Figure 4-8 Output power as function of input power

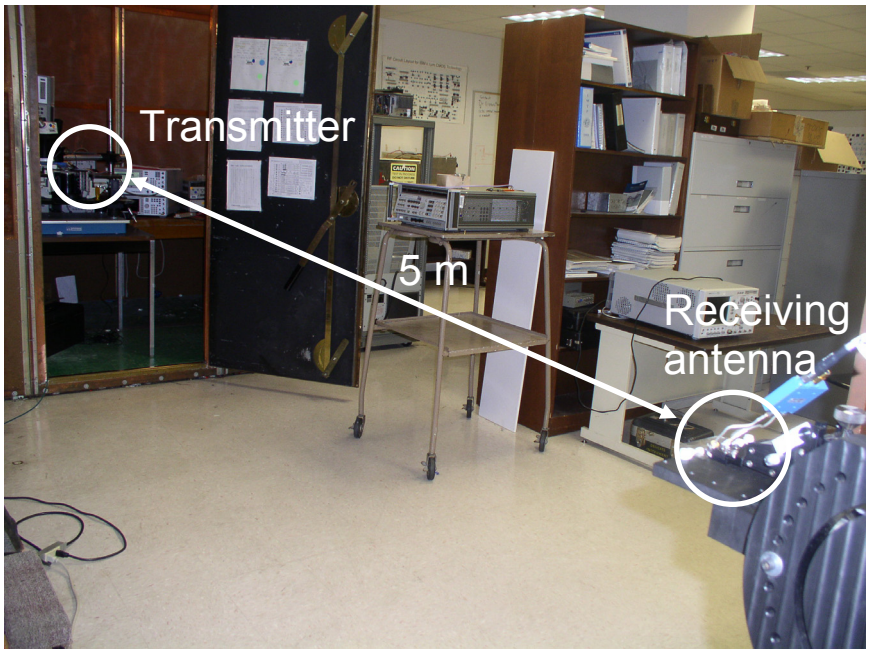


Figure 4-9 Measurement setup of the 5-m wireless communication using an on-chip antennas pair

To demonstrate the feasibility of using an on-chip antenna for wireless communication, an amplitude modulation (AM) signal with 50% modulation depth was provided to the IF input of the test transmitter chain, so that, the transmitter delivered a

24-GHz, 0-dBm AM signal to the on-chip antenna. The measurement setup and environment are shown in Figure 4-9. The distance between the transmitter and the receiving antenna pair is 5 meters. The transmitter is located on a probe station while the receiving antenna is placed on a mobile probe station. The received signal is measured using an HP 8563E spectrum analyzer. The signal received at 5 m is about -102 dBm. Considering there is about 3 dB loss from the probe and cable, the gain between the on-chip antennas pair is estimated to be about -99 dB. Figure 4-10 shows the AM signal picked up by the on-chip receiving antenna.

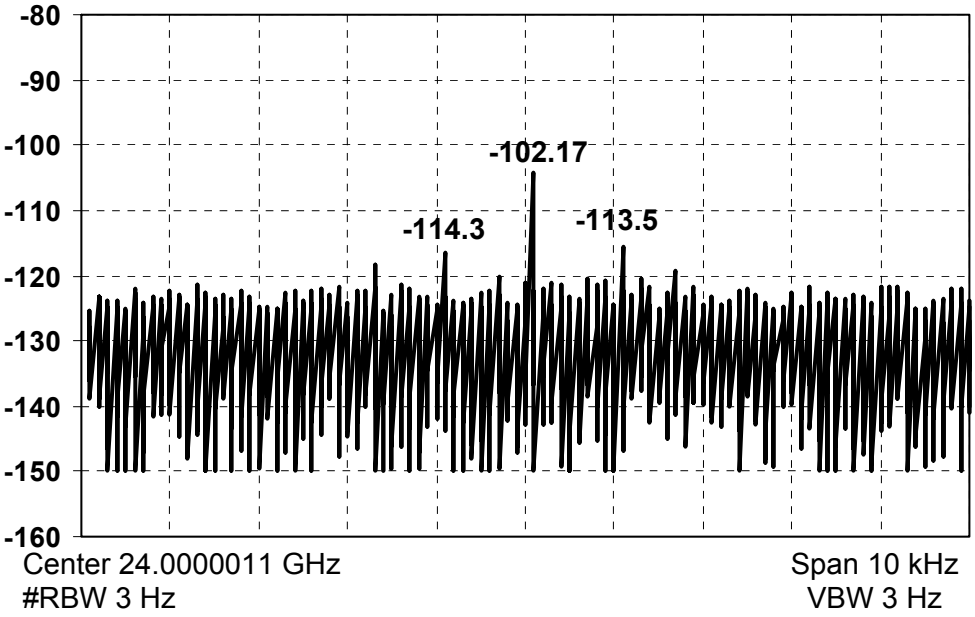


Figure 4-10 Received signal using an on-chip antenna located 5 m away

4.3 Fully Integrated Transmitter with On-Chip Antenna

4.3.1 Transmitter Chain Overview

Figure 4-11 shows the transmitter chain. As mentioned before, the transmitter includes a frequency divider, a MSK-like modulator, IF amplifiers, an up-conversion mixer, RF drivers, a power amplifier and an on-chip dipole antenna. The 8:1 frequency divider generates quadrature signals for the modulator. The serial baseband digital data

are up-converted to IF by the modulator. The signal at IF is amplified and fed into a double-balanced Gilbert cell up-conversion mixer. The RF signal is amplified by a 3-stage driver and fed to a class-E power amplifier (PA). Finally, the PA drives a 3-mm long on-chip zigzag dipole antenna. To provide sufficient LO power level, two buffers for LO signals are also included on the same chip.

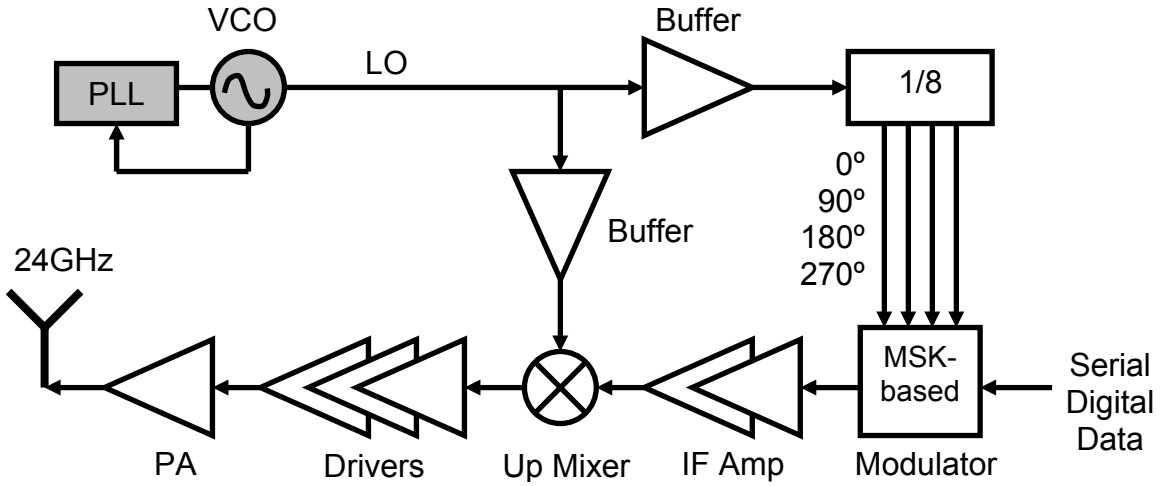


Figure 4-11 Transmitter chain architecture

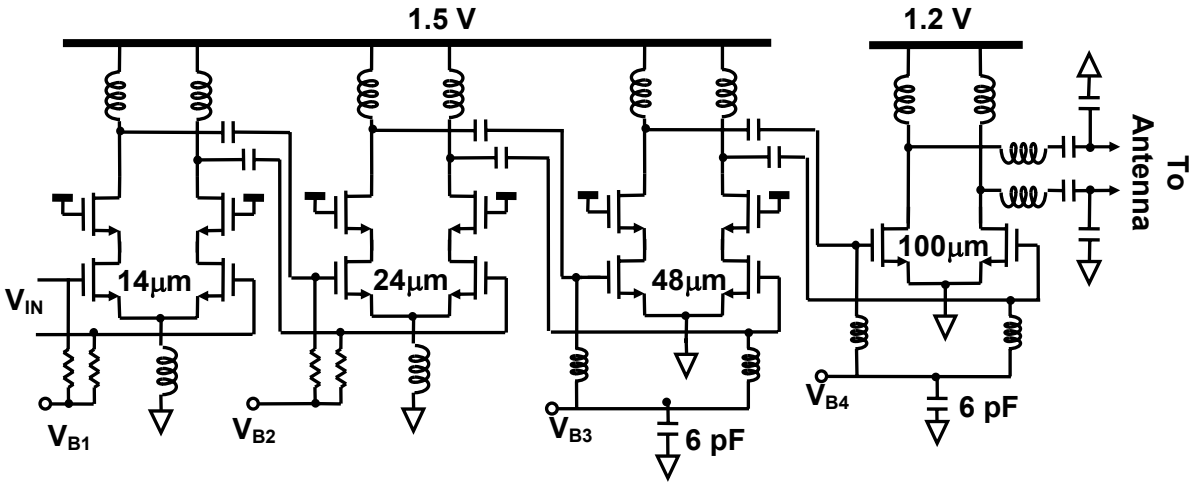


Figure 4-12 Schematic of the RF drivers and power amplifier

The 1-dB compression point of the upconversion mixer is only -10 dBm [27], so that, more than 20 dB power gain must be provided by the following RF stages. Too

much gain at IF stage is just a waste. Meanwhile, to achieve a lower error vector magnitude (EVM, Appendix A), the output voltage swing of the modulator is intentionally limited (Chapter 3.3) and a moderate IF stage gain is required. In this design, a two-stage IF amplifier provides about 18 dB power gain. The four-stage RF amplifiers including PA provide about 25 dB small signal gain. It should also be noted the mixer output power level could be improved by using alternate architecture [49]. However, it provides lower gain and requires higher power consumption.

Figure 4-12 shows the schematic of differential RF drivers and power amplifier. All the circuits in the signal path are fully-differential, which should improve the rejection of common-mode noise from the digital circuits which will eventually be integrated on the same chip. This also allows the connection to the dipole antenna to be made without a balun. To deliver sufficient power level to the antenna, the widths of transistors are chosen as 14, 24, 48 and 100 μm, respectively. Because the self-oscillation of drivers could be mistuned, to improve the chance for proper frequency tuning of the transmitter, the mode locking technique is not used in this version. Instead, all the three driver stages utilized the cascode topology. In the first two driver stages, the current sources at the common-mode nodes are replaced by inductors to increase the voltage headroom. Shunt inductors are placed at the gates of transistors in the last two stages, so that, the AC coupling capacitor can be smaller. Here, a lower supply voltage of 1.2 V is used for PA to have larger reliability margins.

4.3.2 Experiment Results and Discussions

The chip was once again fabricated using the UMC 0.13-μm 1P8M CMOS process. Figure 4-13 shows the die micrograph. The active area occupied by the transmitter is 1.8

mm^2 including the antenna and bond pads. An integer-N frequency synthesizer is also integrated to study the VCO pulling issue. The size of the synthesizer is 0.7 mm^2.

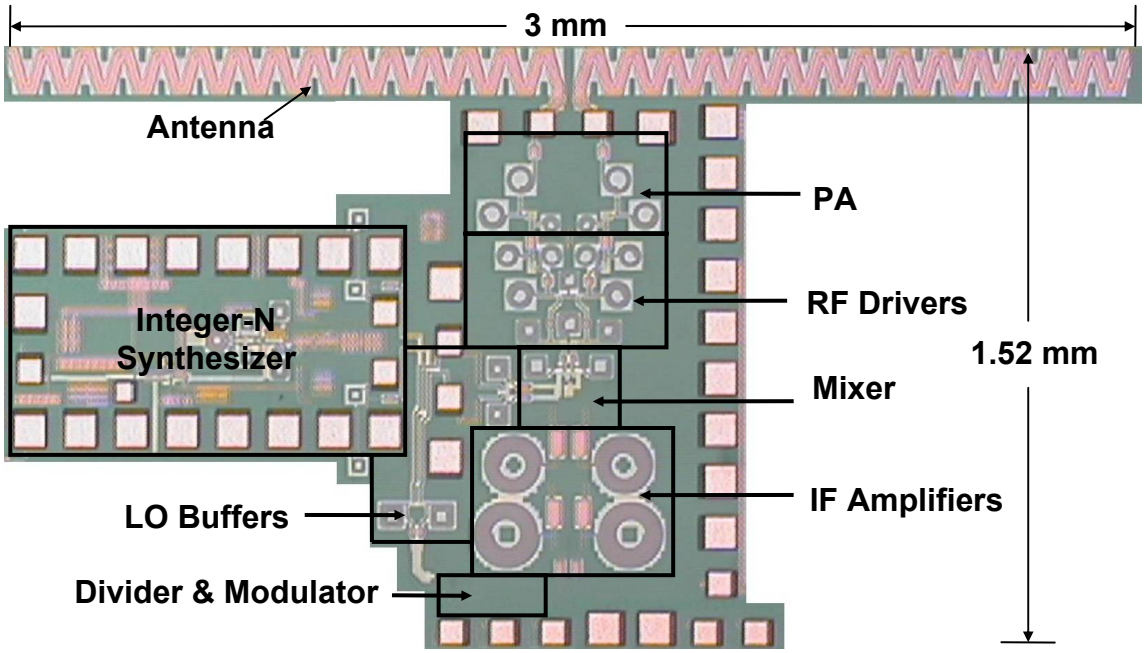


Figure 4-13 Photograph of the fully-integrated transmitter and frequency synthesizer

The transmitter is first characterized on-wafer without the antenna. The output spectrum is measured using an Agilent E4448A spectrum analyzer and the output power level is measured using a power meter. The transmitter including the divider and LO buffers consumes 100.2 mW. The supply voltage of the PA is 1.2 V and supply voltage of other circuits is 1.5 V to achieve higher power gain. Figure 4-14 shows percentage of power dissipation in each block. As can be seen, the 24-GHz RF drivers and PA contribute more than 60% of the power consumption, which is why the efficiency of drivers and power amplifier is so critical in the design.

The transmitter can deliver 8-dBm output power to a 50-Ω load near 24 GHz. The 3-dB bandwidth is 3 GHz. The PA should be able to deliver saturated output power of 10 dBm at 1.2-V V_{DD} if a larger voltage swing were provided by the driver. Figure 4-15

shows the output power level between 21 and 26 GHz. The differential LO signal is provided using an external signal generator and the minimum required power is -5 dBm.

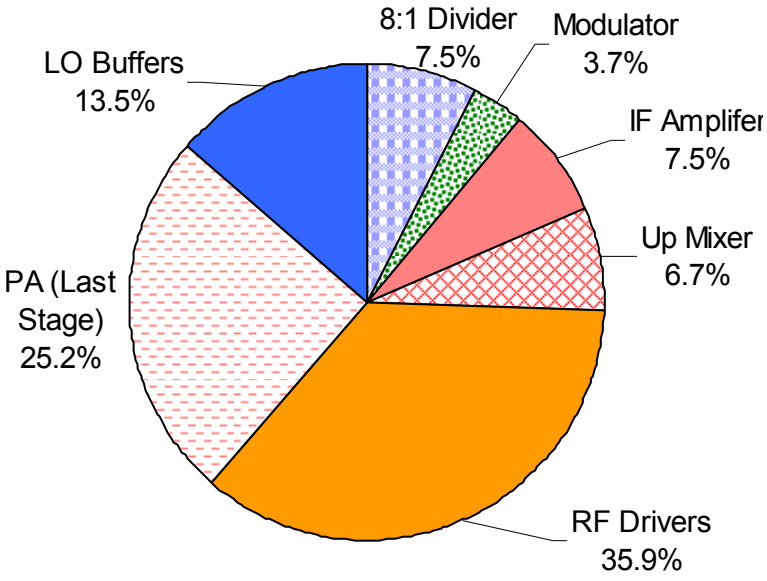


Figure 4-14 Power consumption distribution in the transmitter chain

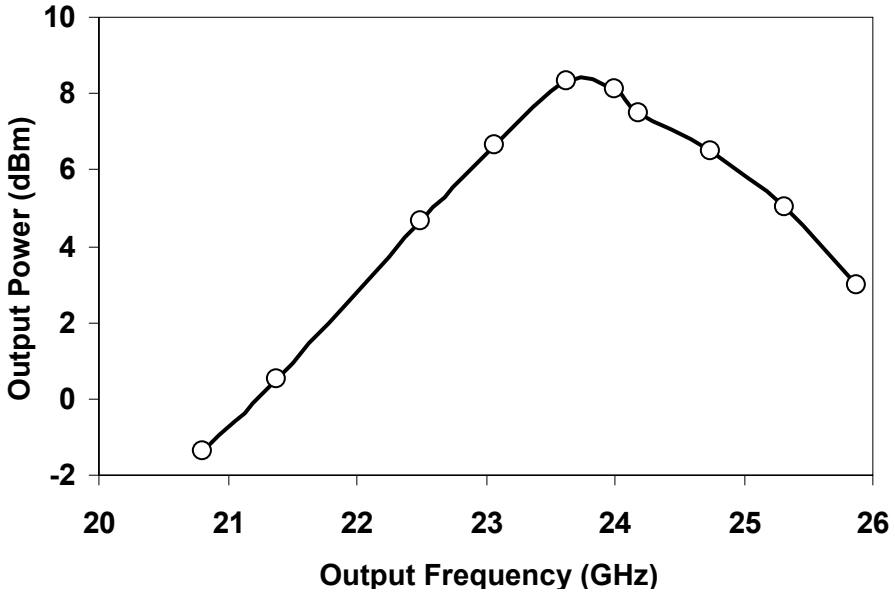


Figure 4-15 Transmitter output power versus frequency

Figure 4-16 shows the measured output power spectrum density (PSD) for 100-Mb/s pseudo random digital input. The random data are provided by an Agilent N4906

serial Bit Error Rate Test (BERT) instrument. The measured main lobe bandwidth is about 1.5 times the data rate and contains nearly all the output power as expected for MSK modulation. Outside the 24-24.25 GHz ISM band, the peak PSD is -36 dBm/MHz, or 5 dB higher than the equivalent isotropic radiation power (EIRP) of -41.25 dBm (measured with 1-MHz resolution bandwidth) required by F.C.C. If the antenna gain of -10 to -8 dBi is included, the emission easily satisfies the requirement. However, the radio itself should satisfy the requirement, so that it can be used for a wider variety of applications. The higher sidelobes are partially due to the IF amplifiers being slightly mistuned to higher frequency. In addition, the modulation steps should be increased to 8 (Chapter 4.4), so that, the peak sidelobes are around 3 dB lower and occur at 800-MHz offset, so that, the IF amplifier could provide better suppression.

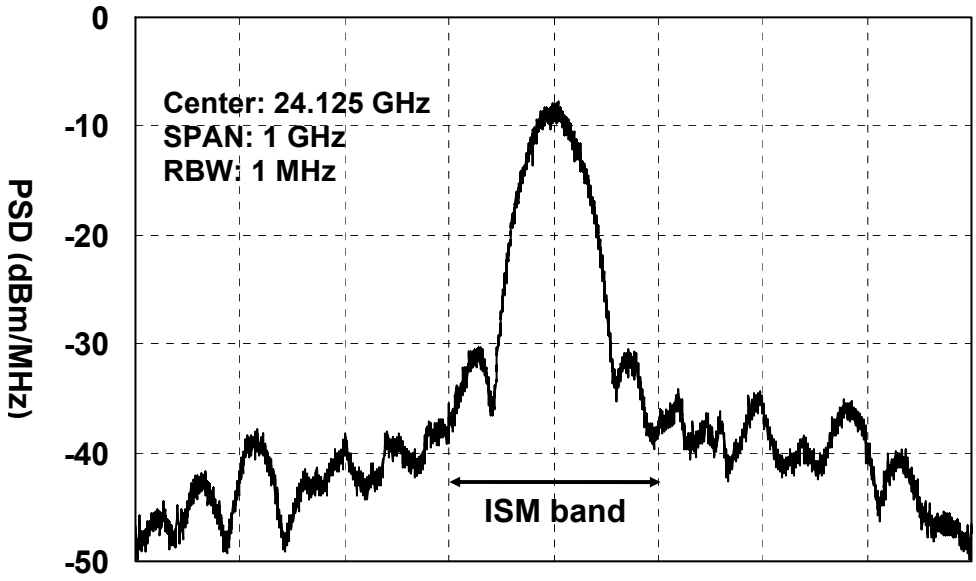


Figure 4-16 Measured output power spectra of the transmitter around 24-GHz

The output of transmitter for pseudo random input is down-converted to 1 GHz and the constellation is obtained using an Agilent 89600 vector spectrum analyzer (VSA). The measured rms and peak EVM's are 7.7% and 16.8% (Figure 4-17). A lower data rate

of 12 Mb/s is used due to the bandwidth limit of VSA. The measured rms magnitude error is 4.4% and the average phase error is 3.8 degrees.

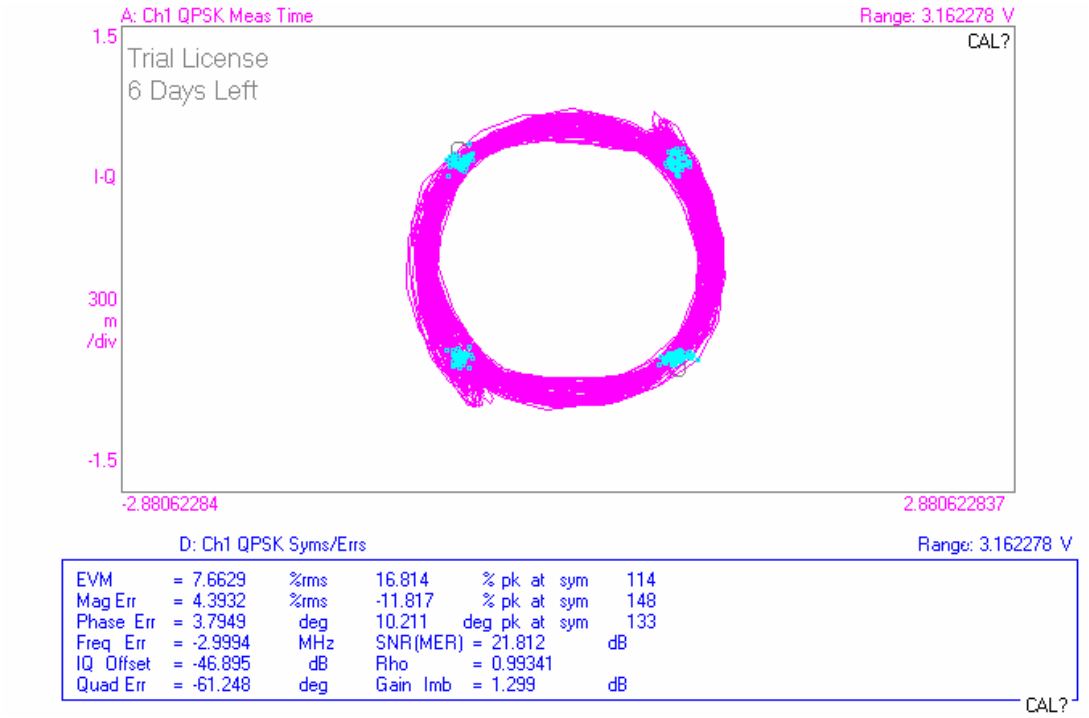


Figure 4-17 Measured transmitter output constellation with a 12-Mb/s data rate

Figure 4-18 shows the measured spectrum with constant data input. The span is 24-GHz, so most of the harmonic spurs can be observed. As mentioned, the F.C.C requires the EIRP of harmonic emission to be lower than -41.25 dBm/MHz. The image signal at 18.76 GHz is around -24 dBm or 32 dB lower than the in-band output. When a random input is used, the power will spread to the entire frequency band and the power spectrum density will be no higher than -42 dBm/MHz. Therefore, the harmonic emission due to the image satisfies the F.C.C requirements.

The LO leakage is about -27 dBm or 35 dB lower than the in-band carrier. The LO leakage is about 14 dB higher than the F.C.C requirement and its power level does not change when random data are used. To reduce this below the F.C.C. limit, notch filters

must be added in the transmitter. More symmetric layout should also be used so that the LO leakage can be better rejected by the circuit.

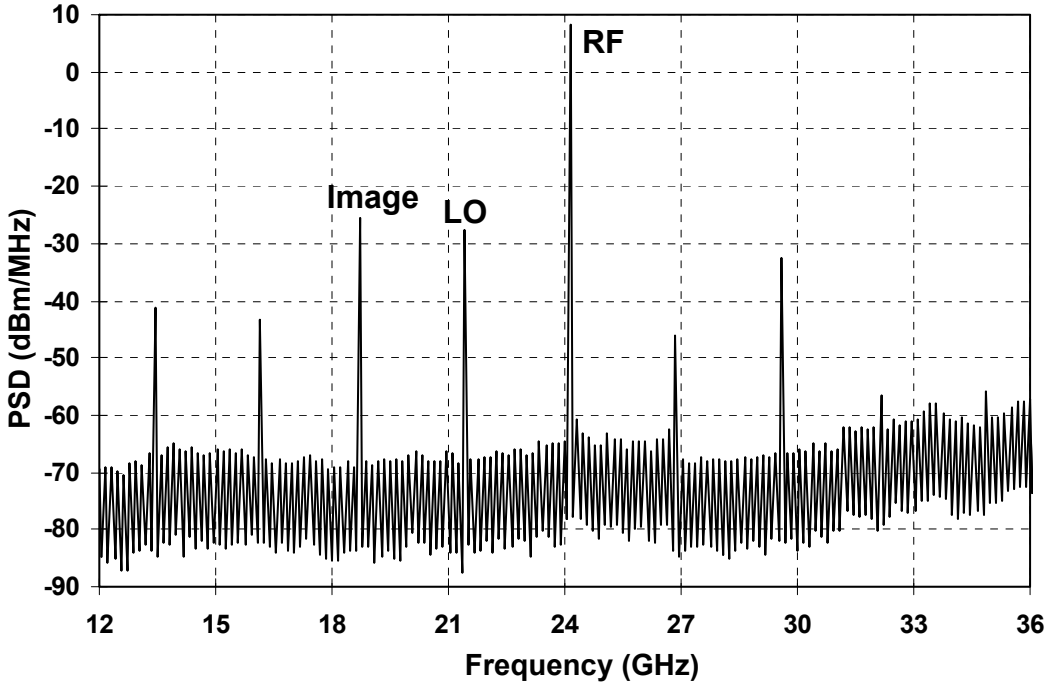


Figure 4-18 Measured output power spectrum with 24-GHz span

Table 4-1 Summary of the 24-GHz transmitter performance

Frequency band	24 - 24.25 GHz ISM band
Modulation	constant envelope MSK-like
Data rate	Up to 200 Mb/s
Output power	8 dBm
PA saturated output	10 dBm (V_{dd}=1.2 V)
Power dissipation	100.2 mW PA: 21 mA x 1.2 V Others: 50 mA x 1.5 V
EVM	7.7% rms (data rate:12 Mb/s)
LO leakage	-35 dBc (req. -49 dBc)
Chip area	1.8 mm^2

The integer-N synthesizer beside the transmitter chain operates from 20.05 to 20.95 GHz, while consuming 24 mA from a 1.5-V supply. However, due to the mis-tuning of buffers, the output power was not sufficiently. Nevertheless, the transmitter is functional

when driven from the synthesizer although the transmitted power is about 10 dB lower. The measured performance of the transmitter is summarized in Table 4-1.

4.3.3 Up-Link Demonstration Using an On-chip Antenna

The communications between a transmitter with an on-chip antenna and a base station is demonstrated by transmitting a 24-GHz single tone (with constant digital input) and picking up the signal using a horn antenna with 20 dBi nominal gain. The horn antenna was located at an entrance of a building and the transmitter is placed on a mobile probe station located at a parking lot 95 meters away in a humid morning (Figure 4-19). The horn could be considered as the antenna of a base station. The received signal is -97 dBm or the antenna pair gain is about -105 dB. These suggest that communication between a base station and an integrated circuit with an on-chip antenna over a distance of 100 meters is possible.

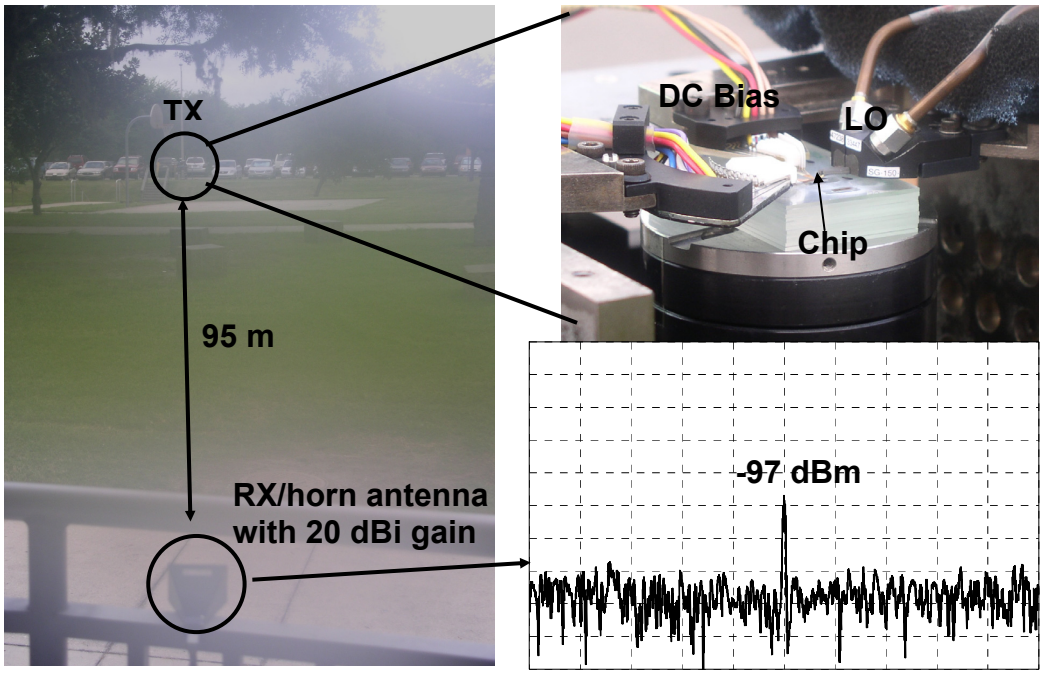


Figure 4-19 Reception of the signal from a transmitter IC with an on-chip antenna using a 20-dBi gain horn antenna located 95m away

4.4 Improved Transmitter Chain Design

As discussed, it is required by F.C.C that the spurious emission must be less than -41.25 dBm when measured with 1-MHz resolution bandwidth. The transmitter chain however presently can not satisfy this. The problems come from two parts. First, the peak sidelobe power spectrum density is around -35 dBm/MHz. Secondly, the LO leakage is about -27 dBm, or 14 dB higher than required. These two problems can be solved using improved modulator and amplifiers design.

4.4.1 Improved Modulation Scheme

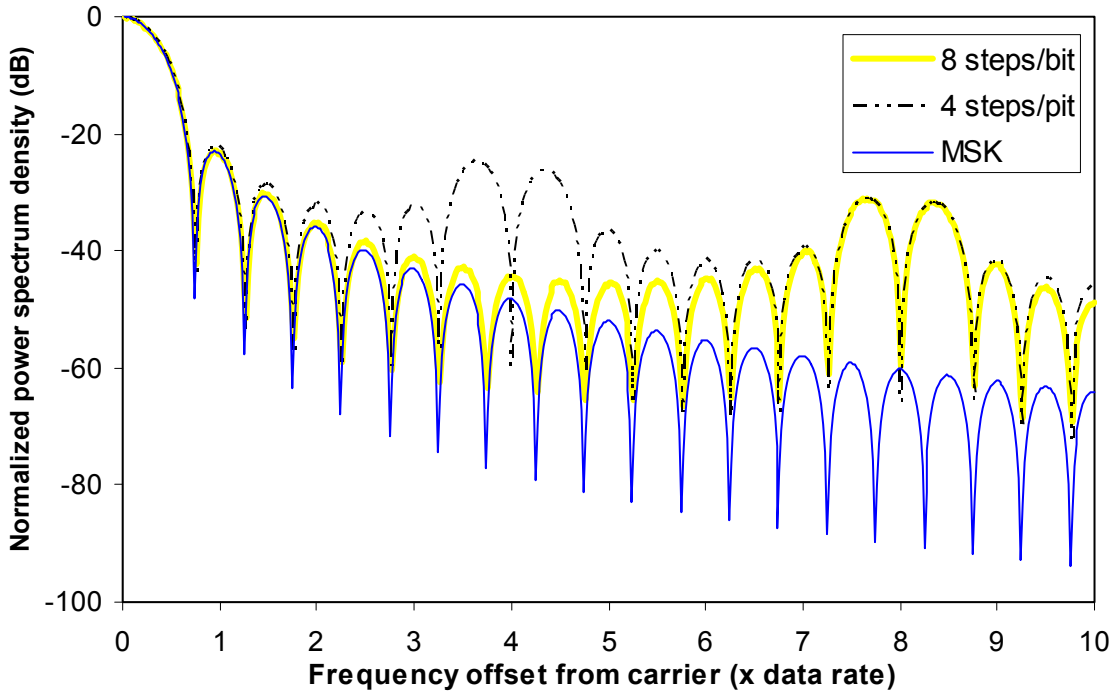


Figure 4-20 Modulator output spectra with different modulation steps per bit

The sidelobes in Figure 4-16 come form the modulator. To achieve higher level integration, no filters are used in the transmitter and IF amplifier is the only component which can suppress these sidelobes. To provide better rejection to these sidelobes, more IF amplifier stages can be used, which however results in higher power consumption and

larger silicon area. A better way is to move these sidelobes to higher frequency offset. Because only 4 discrete steps per bit are used, the peak sidelobes appear around 4 times of the data rate. If more steps per bit are used, the sidelobes will move to higher frequency offset. Figure 4-20 shows the modulator output spectra with 4 and 8 steps per bit scheme. As a matter of fact, the MSK modulation has infinite steps per bit. In the improved modulator, 8 steps per bit are used. This also requires the control circuit running at higher frequency and the control signals better matched to reduce the clock feed-through. The IF amplifiers is also re-tuned, so that, its center frequency is around 2.7 GHz.

4.4.2 Improved Transmitter Front-End with Notch Filters

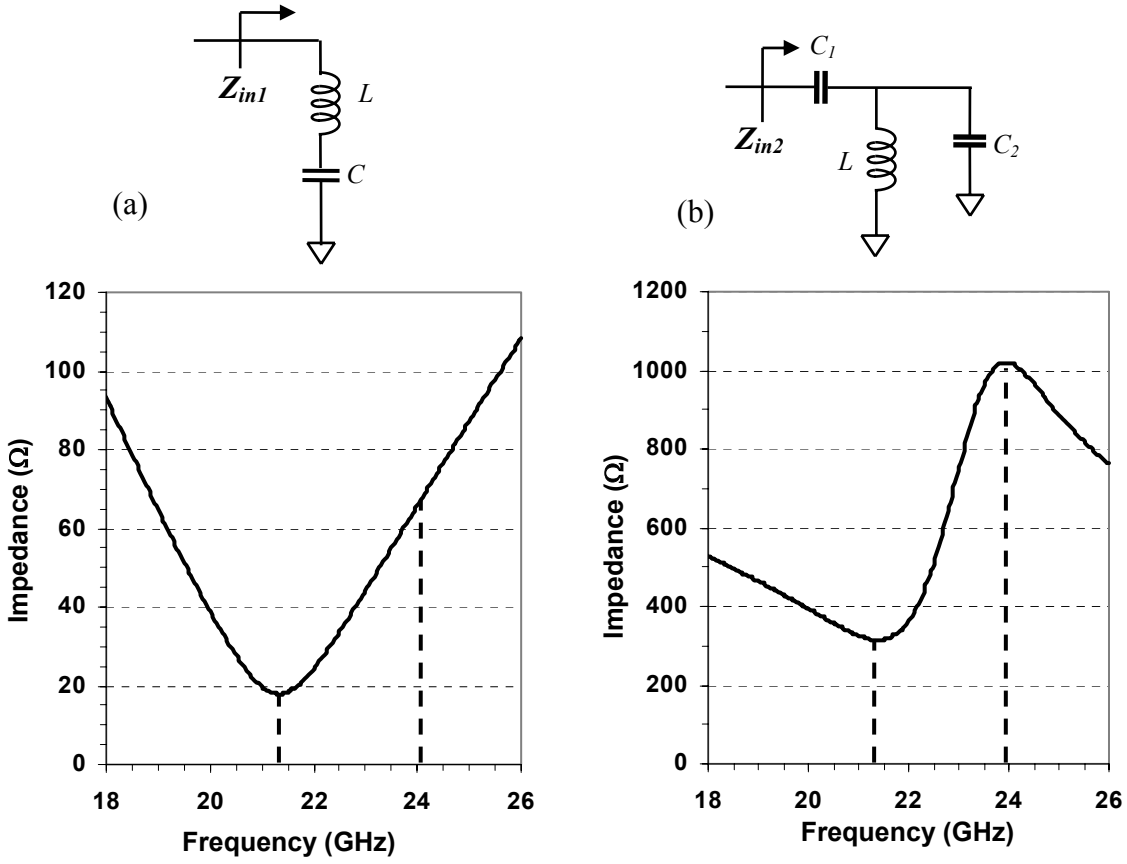


Figure 4-21 Second and third order notch filters and their characteristics

The LO leakage most likely comes from the active circuitry. Because the bandwidth of the RF amplifiers is wide due to low-Q passive components, the RF amplifiers cannot provide sufficient suppression of LO leakage from the up-conversion mixer. To solve this, notch filters at LO frequency can be inserted. Two notch filters structures can be used. Figure 4-21 shows the schematic and the simulated characteristics of the second and third order notch filters. The Q of the inductor is assumed as 20 and that of the capacitor is 50 at 24-GHz. The inductor value is limited to less than 1 nH, and the capacitance is less than 100 fF. The gain difference at RF and LO frequency can be estimated as the ratio of impedance at these two frequencies. Therefore, both notch filters could provide about 10 dB suppression to the LO signal. In fact, the LO suppression only depends on the Q of the inductors and capacitors, if the filters are tuned well.

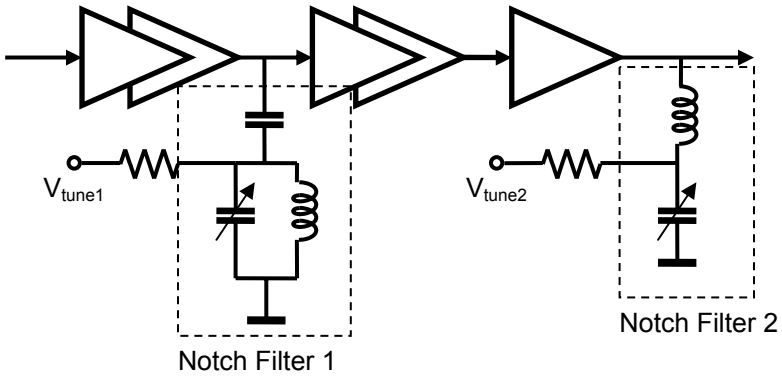


Figure 4-22 Improved transmitter RF front-end with notch filters

To provide more than 14-dB rejection, two notch filters should be added to the circuit. From simulation, these notch filters also have nearly 2-dB in-band insertion loss. To compensate this, additional driver stage is also included. Figure 4-22 shows the improved transmitter RF front-end. The impedance of second order filter is small, typically less than 100 Ω, thus, it cannot be added to a node where the impedance is high; otherwise the in-band gain will be significantly degraded. On the other hand, the third

order notch filter cannot be added to a node where the impedance is low, because it almost has no effect on the gain at either the LO or RF frequencies. Therefore, a third order notch filter is inserted between the second and third driver stages, while a second-order filter is added to the output of the power amplifier. The capacitors in these filters are formed using a combination of a metal capacitor and a MOS capacitor/varactor, so that the operating frequency of the filter can be tuned, while maintaining relatively high Q for the capacitor.

4.5 Fully-Integrated Transceiver

Since the transceiver of a μNode device is time division duplex (TDD), which means only one chain is active at one time, one antenna can be used. This will make the design more flexible and decrease the silicon area. Generally, a T/R switch is required to control the connection between the receiver, transmitter and the antenna. However, it is difficult to implement single-pole double-throw (SPDT) switches with low insertion loss at 24-GHz using the 0.13-μm CMOS process. For example, switches implemented in the 0.13-μm CMOS process achieve 1.8-dB insertion loss at 15 GHz [50]. From simulations, insertion loss of a switch operating at 24 GHz can easily go higher than 2.5 dB. Therefore, at transmitting mode, nearly 50% of the transmitted power will be dissipated in the switch. While in the receiving mode, the high insertion loss will degrade the input SNR or increase the noise figure of receiver chain.

For the μNode transceiver, instead of using a T/R switch, the switching function is merged into the PA and receiver [51], as shown in Figure 4-23. In the transmitting mode, *RxEn* is set to low voltage level (around 0.4 V in simulation). The series $L_{sw}C_{sw}$-tank works as a notch filter for LO signal. At the same time, *TxEn* is set to V_{DD} to turn on

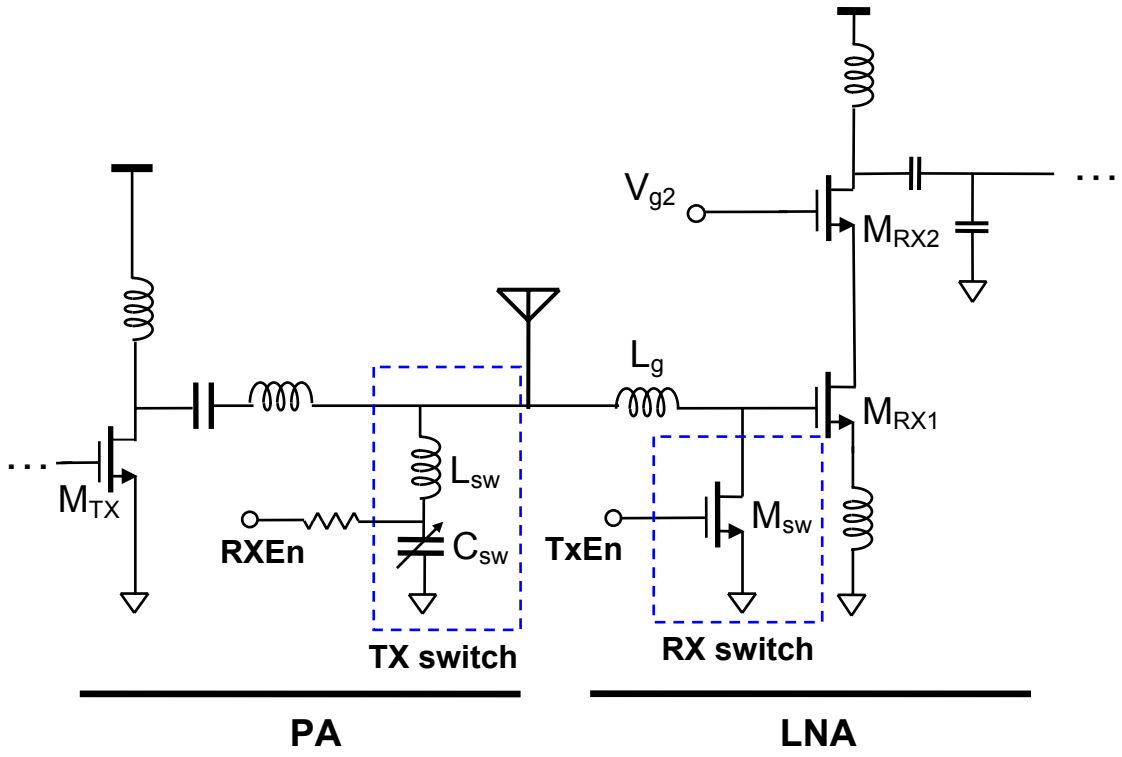


Figure 4-23 Integrated transmitter and receiver RF front-end with distributed T/R switches

transistor M_{sw}. The gate of M_{RX1} is shorted to ground and this avoids high voltage swing at M_{RX1} gate. The impedance looking into the receiver will be $j\omega L_g$ which is around 150 $j\Omega$. This high impedance assures the impedance matching between the antenna and PA output to deliver maximum power while protecting the LNA. While in the receiving mode, *TxEn* is ground to turn off M_{sw}. *RxEn* is set to high voltage (V_{DD}), so that C_{sw} is tuned to its maximum capacitance value. The resonant frequency of the L_{sw}-C_{sw} series tank moves to 13.5 GHz and it provides an inductive impedance of 100 $j\Omega$ at 24 GHz. In simulation, this distributed switches scheme increase the noise figure for the receiver by 1.3 dB and decreases output power of the PA by 0.8 dB, which are much better than the SPDT T/R switch. The synthesizer provides the 21.4-GHz LO signals to the receiver and the transmitter. To assure sufficient LO drive, buffers have been inserted between the

synthesizer and each mixer and divider in the receiver and the transmitter. Figure 4-24 shows the PLL output to different buffers. The PLL output buffer consumes 4-mA DC current from a 1.5-V supply. It provides around 800-mV peak-to-peak voltage swing at the TX and RX buffer inputs.

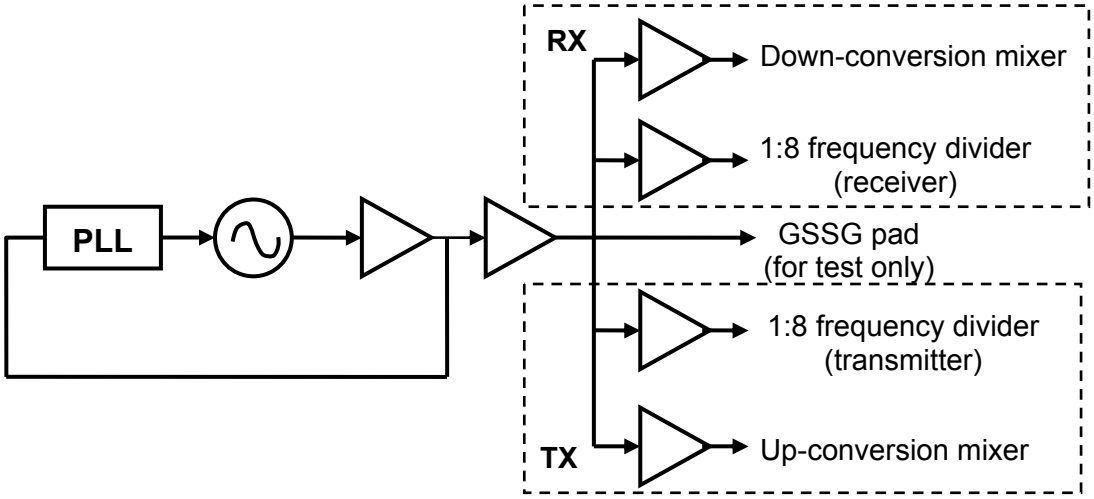


Figure 4-24 Integration of the frequency synthesizer, transmitter and receiver

4.6 Summary

In this chapter, the design and measured results of a fully integrated 24-GHz transmitter chain are presented. The signal transmitted by the circuit with an on-chip antenna can be picked up by an on-chip antenna 5 meters away or a horn antenna 95 meters away. The communication between a transmitting antenna and a receiver with an on-chip antenna separated by 5 m was also demonstrated in [3]. These works demonstrated that it is feasible to build a wireless transceiver with on-chip antennas for short range communications. An integrated RF transceiver with a frequency synthesizer has been implemented.

CHAPTER 5
MILLIMETER-WAVE VOLTAGE CONTROLLED OSCILLATORS

5.1 Overview of the Millimeter-Wave Oscillators

For direct conversion architecture, a voltage controlled oscillator operating at either 50 or 100 GHz is needed. With the rapid advance of high frequency capability for CMOS technology, it is becoming possible to make CMOS circuits operating in the millimeter-wave frequencies [52]-[70], which once were only possible to be realized using GaAs and InP technologies. These millimeter wave CMOS integrated circuits can be used to satisfy the ever-increasing demand for bandwidth in communication (broadband WLAN at 59-64 GHz ISM band) as well as the emerging needs for RF sensor systems such as automotive cruise control at 76-77 GHz and imagers at 94 GHz. The MMIC solutions can provide the size, weight and performance advantages. Implementing millimeter-wave systems using the low cost CMOS technology will lead to lower cost and higher integration levels, and help to turn the relatively small volume applications mentioned above as well as others into main stream high volume consumer applications.

Over the past five years, the maximum operating frequency of VCO's fabricated in silicon technology has almost quadrupled from 25.9 to 117.2 GHz [52]-[56], [60]-[64]. Push-push VCO's using the second harmonic operating between 63 and 131 GHz [59], [65], [67] have also been demonstrated in silicon technology. However, among these, the bulk CMOS fundamental VCO's operating around or above 50 GHz usually show poor phase noise, limited frequency range or large power consumption. In this chapter, the design trade-offs and optimization techniques for high frequency LC-resonator based

VCO's are described. These techniques are utilized to realize a 59-GHz VCO with a tuning range of around 5.8 GHz, a 140-GHz fundamental mode VCO, as well as a 192-GHz push-push VCO using CMOS technology. This work also shows that even at 100 GHz, lumped element approach can be used to implement VCO's. As a matter of fact, the circuit sizes can be reduced using the lumped elements instead of that based on transmission lines.

A key to achieving oscillation in an LC oscillator is providing sufficient negative resistance to cancel the losses in the resonant LC tank. This is particularly difficult at high frequencies, because the core transistors cannot be large due to the capacitances they add to the tank. To accommodate core transistors with a sufficient width, the parasitic capacitances connected to the tank, including those of transistors, must be minimized. At given operating frequency, the reduced parasitic capacitances also allow inclusion of larger varactors for wider tuning range. The transistor size limitation can also be alleviated by increasing the quality factor (Q) of tank to lower the loss. Therefore, low parasitic and high-Q resonator, as well as low parasitic and high gain transistor design is needed.

Section 5.2 describes the transistor model in the millimeter-wave frequency range and discusses the operating frequency of the oscillators. Sections 5.3 and 5.4 discuss the performance of passive components (varactor and inductor). The trade-off between the quality factor (Q) and tuning range of varactor is studied in detail. Section 5.5 proposes a low parasitic and high gain transistor design, while section 5.6 describes the architecture of these millimeter wave oscillators. The measured results of the fundamental VCO's between 59 and 140 GHz are presented in Sections 5.7 to 5.9. The performance of 192-

GHz push-push VCO is discussed in Section 5.10. Finally, the design method of millimeter wave VCO's is summarized.

5.2 MOSFET Modeling for Millimeter-Wave Design

5.2.1 Gate Resistance and Non-Quasi Static Effect

Two figures of merit for quantifying the higher frequency performance of transistors are popular. These are f_T (or ω_T) and f_{max} (or ω_{max}), which are the frequencies at which the extrapolated current and power gain are unity. For a VCO, in order to sustain oscillation, the transistor must provide a power gain larger than one. Therefore, the unity power gain frequency, f_{max}, is closely related to the maximum operating frequency of an oscillator.

It has been well known that the gate resistance reduces f_{max}. The gate resistance is usually just considered as the ohmic sheet resistance of polysilicon. To reduce the gate resistance, the gate can be contacted on both ends and folded into multiple fingers. Therefore, the gate resistance can be expressed as,

$$R_g = \frac{1}{4} \times \frac{1}{N} \times \frac{1}{3} \frac{W/N}{L} R_{\square,poly} = \frac{1}{12} \times \frac{1}{N^2} \times \frac{W}{L} \times R_{\square,poly}, \tag{5-1}$$

where, W and L are the width and length of the transistor, $R_{\square,poly}$ is the sheet resistance of the polysilicon, N is the number of fingers, 1/3 accounts for the distributed gate resistance, and 1/4 accounts for the two-ends connection.

This gate resistance is a bias-independent component at DC and low frequencies. There is another gate resistance component with bias dependence at high frequency, which is due to the distributed transmission line effect of the gate. To reduce this, a multi-finger device with a narrow finger width should be used. The other effect is distributed

channel resistance, arising from the non-quasi static (NQS) effect. At frequencies NQS effects cannot be neglected, an additional resistance is needed to account for the NQS effect. From [71], [72], the equivalent channel resistance can be expressed as $1/(5g_m)$.

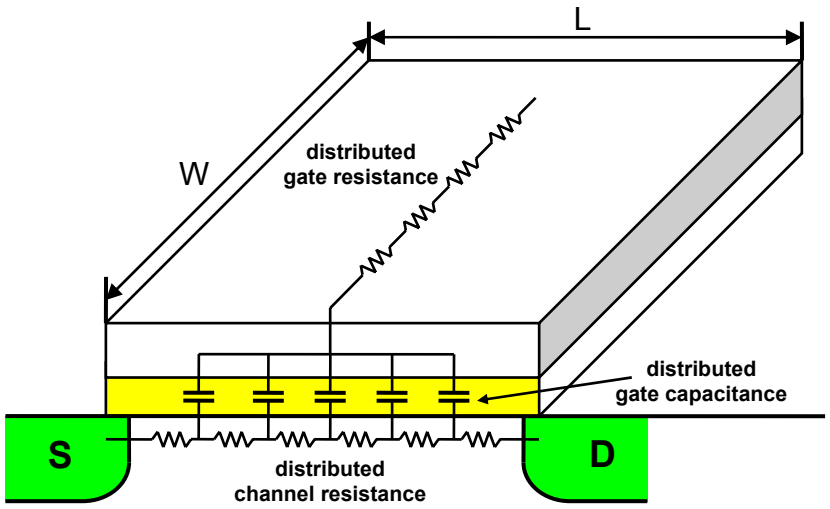


Figure 5-1 Equivalent gate resistance model including distributed ploy-silicon resistance and distributed channel resistance

5.2.2 Unity Gain Frequencies

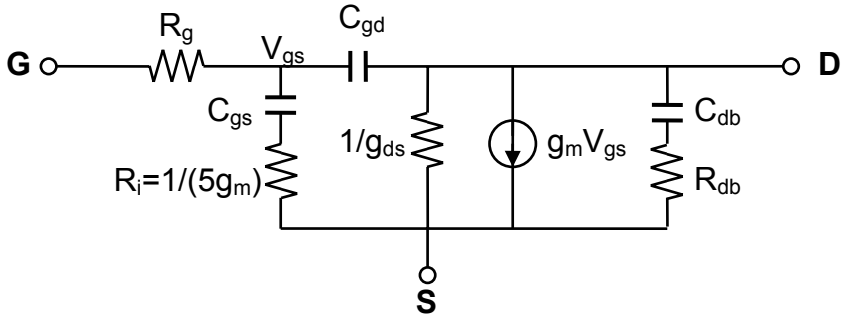


Figure 5-2 Equivalent MOS transistor model including the gate resistance

Using the equivalent transistor model in Figure 5-2, the unity current and power gain frequencies can be derived. A transistor can be considered as a two-port network. The gate terminal is the input port, while the drain terminal is the output port. The source terminal is connected to ground. The expression for ω_T assumes the drain is terminated as

short while the gate is driven by an ideal current source. In addition, the gate-to-drain capacitance is considered only in the computation of the input impedance, while its feed-forward contribution to the output current is neglected. With these assumptions, the ratio of drain current to gate current is

$$\left|\frac{i_d}{i_{in}}\right| \approx \left|\frac{g_m V_{gs}}{j\omega(C_{gs}+C_{gd})V_{gs}}\right| = \frac{g_m}{\omega(C_{gs}+C_{gd})}, \tag{5-2}$$

which has a value of unity at the frequency of

$$\omega_T = 2\pi f_T = g_m/(C_{gs}+C_{gd}) \tag{5-3}$$

Though the unity current gain of frequency, ω_T, is widely used, it dose not include the effects of several components. As a consequence of the shorted termination, ω_T does not include the drain-bulk capacitance C_{db} or output impedance $1/g_{ds}$. The current source drive also takes out the series gate resistance term. Therefore, unity power gain frequency, ω_{max}, which include these terms, is more relevant for high frequency oscillator design. The computation of ω_{max} is generally difficult, so several simplifying assumptions are used to make an approximate derivation possible (Appendix B) and it can be expressed as

$$\omega_{\max} = 2\pi f_{\max} = \frac{\omega_T}{2\sqrt{(R_g + 1/(5g_m))(g_{ds} + \omega_T C_{gd})}} \tag{5-4}$$

Figure 5-3 shows the unity current gain frequency and unity power gain frequency, versus the transistor gate length. For the transistor in 0.13-μm and 90-nm processes, f_{max} higher than 100 GHz has been reported. Therefore, it should be possible to build a CMOS circuit running above 100 GHz. However, with device scaling, the contact/via area decreases and these resistances increase very fast. For instance, the typical contact resistances are 7 Ω, 15 Ω, and 45 Ω in the 0.13-μm, 90-nm and 65-nm process,

respectively. The higher contact resistance increases the gate resistance and slower the increase of f_{max} of the transistor with scaling.

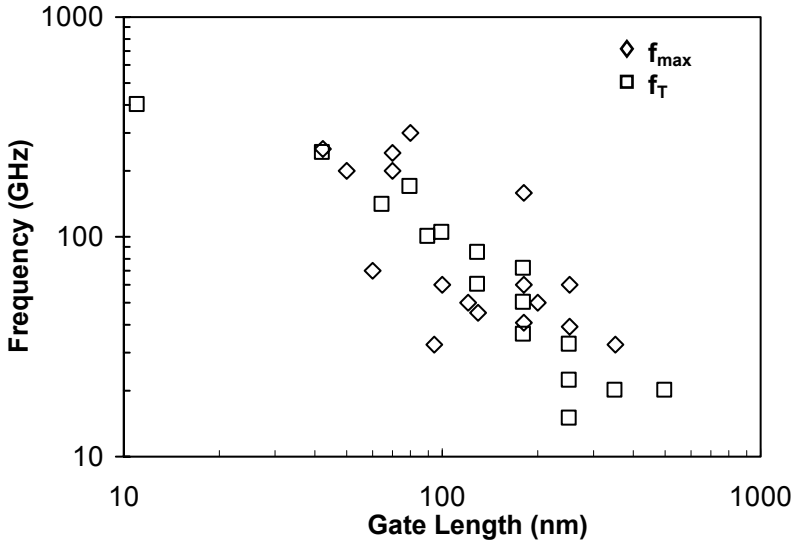


Figure 5-3 Unity current frequency, f_T, and unit power gain frequency, f_{max}, versus gate length

5.2.3 MOSFET Radio Frequency Model

Including the parasitic capacitors and resistors at the drain, gate, source and substrate, a complete RF subcircuit model for a NMOS transistor is shown in as Figure 5-4 [71], [73], [74]. R_s and R_d are the source/drain resistances due to the resistive n^+ active region. C_{gsp} and C_{gdp} are the parasitic gate-to-source/drain capacitances, mostly from metal interconnections. C_{sb} and C_{db} are the source/drain junction capacitances, while, R_{sb} and R_{db} are the series resistances of junction capacitances. The parasitic capacitances at the gate and drain terminals will directly contribute to the LC-tank of the VCO and lower the oscillation frequency.

The influence of substrate resistance, R_{sub}, is usually ignored for digital circuit simulation at low frequency. However, at high frequencies, the signal at drain couples to the source and bulk terminals through source/drain junction capacitance and the substrate

resistance. The substrate resistance influences mainly the output characteristics, and it can lower the output impedance as much as 30% in 0.13-μm CMOS process. The C_{gb}-R_{sub} network also increases the noise figure of LNA.

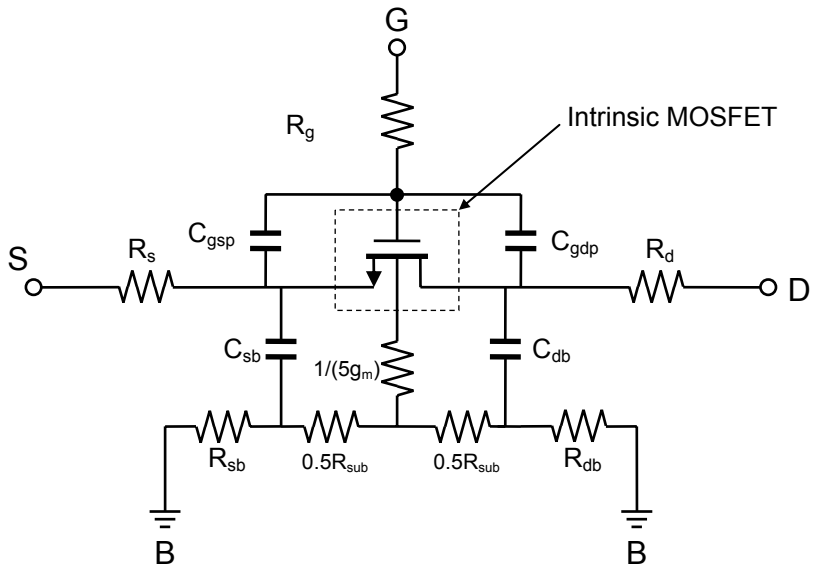


Figure 5-4 RF model of an NMOS transistor with intrinsic and extrinsic components

5.3 MOS Varactor

Usually, at frequencies lower than 10 GHz, the Q of LC resonator is limited by inductor loss. This is no longer the case at millimeter-wave frequencies. Because the Q of capacitors ($Q_C \sim 1/(\omega RC)$) decreases with frequency, while that of inductor ($Q_L \sim \omega L/R$) increases with frequency, the tank Q is limited by the Q's of capacitors at the millimeter-wave frequencies. The optimization of layout and an accurate model for the MOS capacitor/varactor are more critical at the millimeter-wave frequencies oscillators design.

5.3.1 MOS Varactor Structure

Figure 5-5 shows the top-view and cross-section of a MOS varactor. The top and bottom plates are formed by silicided n^+ polysilicon and n-well, which are separated by a gate oxide layer. The thickness of gate oxide is only about 3 nm, which leads to high

capacitance density of 11 fF/μm^2 in the accumulation region. The poly gate is connected at two ends to reduce the resistance. To increase the tuning range, the parasitic capacitance must be minimized. In advanced CMOS technologies, where the minimum metal-to-metal and contact-to-polysilicon spacing can be very small, the parasitic interconnect capacitance can be large. To decrease the parasitic capacitance, the metal contacts for n-well are placed 0.4 μm from the polysilicon gate. Since the n-well is usually AC-grounded, the increased n-well to substrate junction capacitance can be tolerated. The metal interconnection of n-well is formed by only metal1 and 2 layers, and the gates are connected together using the metal7 and 8 layers. For comparison, a varactor structure using the minimum spacing and a ploy gate dimension of 0.12 μm x 0.28 μm was also fabricated. The metal connection for n-well was formed by stacking metal1 through metal6. The measured parasitic capacitance, which is mainly due to the poly and metal interconnections, is about 3 times that of the gate oxide. This makes the tuning range of the varactor close to zero.

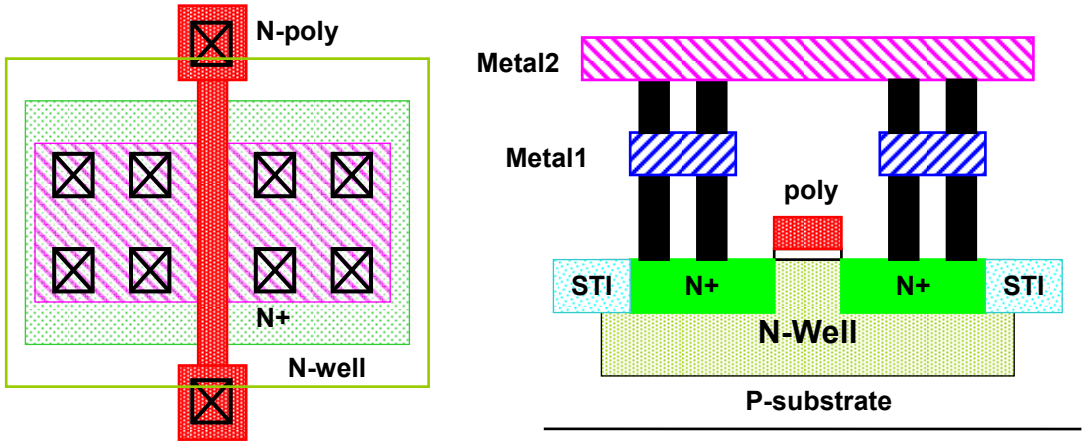


Figure 5-5 Top view and cross section of the MOS varactor

5.3.2 Equivalent Model

A simplified MOS varactor model including a series L_s-R_s-C network is shown in Figure 5-6. In the equivalent model, C_{var} is the variable MOS capacitance and C_{par} is the fixed parasitic capacitance due to the metal and polysilicon gate parasitic. R_{gate} is the resistances of poly gate, R_{well} is the resistance associated with n-well/channel under the gate, and R_{metal} is those associated with the contacts, vias and metal interconnects at the gate and n-well side, respectively. Other effects, such as n-well to substrate capacitance, and substrate loss, are not included in the simplified model. More complete varactor models are discussed in [74]-[75].

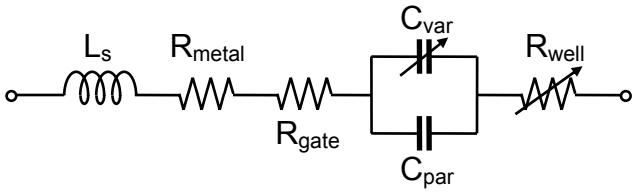


Figure 5-6 Simplified MOS varactor model

As described in [76], the series resistance is

$$R_s \cong \frac{1}{N}\left(\frac{1}{12\times W\times L}\left(R_{\square,nw}\times L^2 + R_{\square,poly}\times W^2\right) + R_{metal,unit}\right), \tag{5-5}$$

where, W and L are the width and length of each finger, $R_{\square,nw}$ and $R_{\square,poly}$ are the sheet resistance of n-well and poly gate, N is the number of fingers. The factor of 12 in the denominator accounts for the double sided n-well and poly gates contacts. $R_{metal,unit}$ is the resistance from contacts, vias and metal interconnect in each finger. Because it decreases with more contacts and vias, their numbers are increased to as many as allowed.

As also described in [76], if only the capacitors from gate oxide and resistance from poly gate and channel are considered, the quality factor of this simplified model network is,

$$Q \cong \frac{1}{\omega R_s C} = \frac{12}{\omega C_{ox}(R_{\square,nw}L^2 + R_{\square,poly}W^2 + R_{metal,unit}WL)}, \quad (5\text{-}6)$$

where ω is the frequency and C_{ox} is the gate-oxide capacitance per unit area. To increase Q, smaller W and L should be used. However, the penalty is larger parasitic capacitance due to more metal interconnections, which decreases the tuning range. Since $R_{\square,nw}$ is more than 50 times the $R_{\square,poly}$, L should be made smaller, while W of a finger can be made larger to reduce the parasitic capacitances. With the continuing scaling in CMOS technology, the Q of varactor should increase with smaller gate length and lower n-well sheet resistance. However, this increase will be tempered by the increases in the contact and via resistances.

5.3.3 Experiment Results and Discussions

To experimentally examine these, structures with varying gate lengths were fabricated in the UMC 0.13-μm CMOS process. The average capacitances of structures are kept approximately the same. The effects of pads are de-embedded using the open structure formed by disconnecting the gate connection from the pad as discussed in [76], [77]. One-port S-parameters of the test and open structures were collected using an HP8510C 26.5-GHz network analyzer. Figure 5-7 shows the measured capacitance, series resistance, and quality factor of a MOS varactor. The finger length (L) is 0.24 μm and width (W) is 0.64 μm and there are 20 fingers. Figure 5-8 shows the C-V and Q-V curves measured at 24 GHz for three varactors with different dimensions. The minimum gate length of 0.12 μm is used for structure (a), thus, it gives nearly the highest available Q. A minimum Q of 24 is achieved at 24 GHz, which is close to the Q reported in [52]. When extrapolated using Q=1/(ωRC), Q is about 9 and 6 at 60 and 100 GHz, respectively.

However, the tuning range is limited (C_{max}/C_{min}=1.75), though larger than 1.2 reported in [52]. In structure (c) with a gate length of 1 μm, the tuning range (C_{max}/C_{min}) is ~7. As

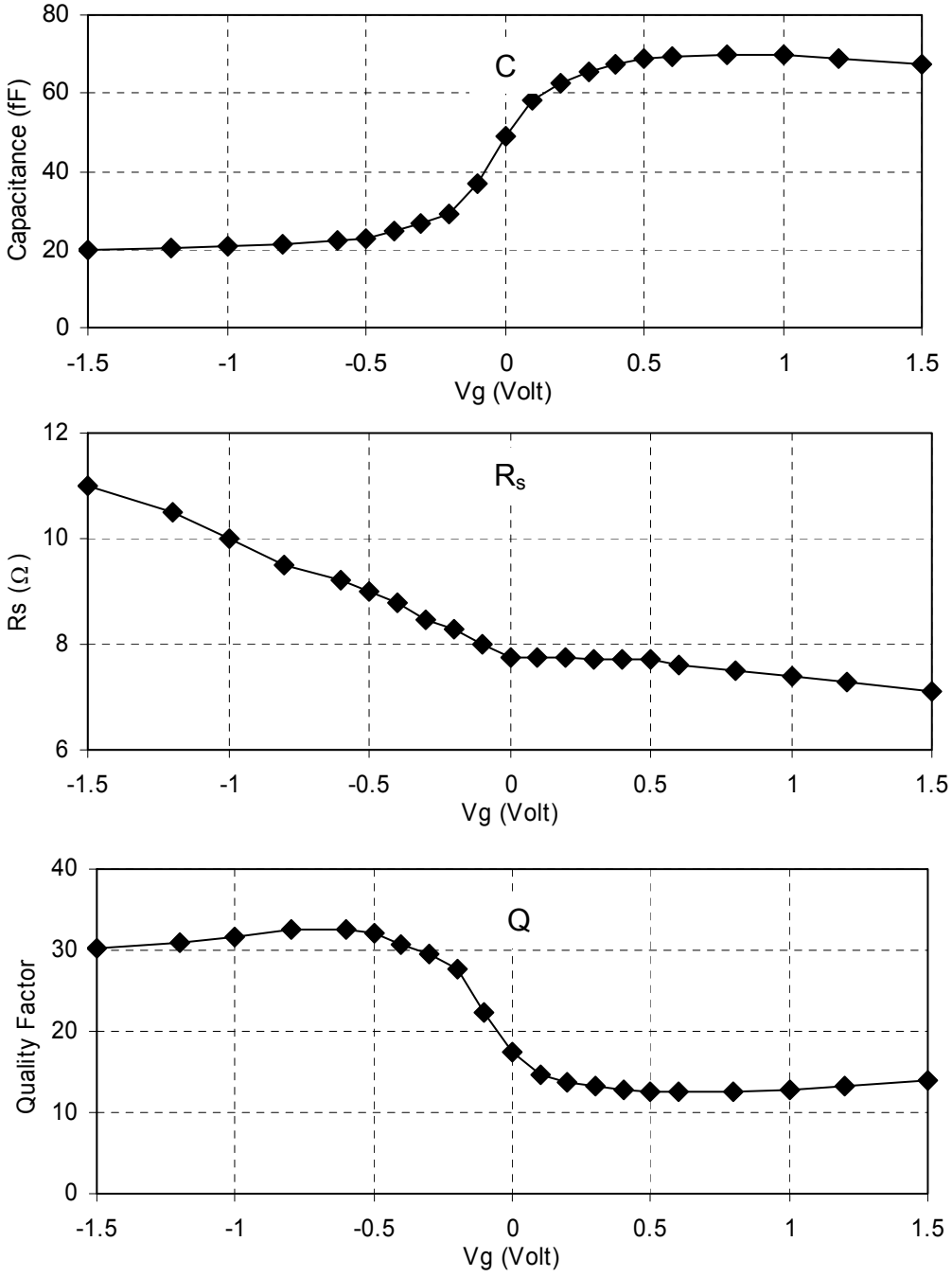


Figure 5-7 Measured MOS varactor capacitance, series resistance and quality factor at 24 GHz for a varactor with 0.64-μm width, 0.24-μm length and 20 fingers

expected, the penalty is lower Q of ~2.5 in the accumulation region. A medium gate length of 0.24 μm is used in structure (b), which has moderate Q at 24 GHz of 12.5 and an excellent C_{max}/C_{min} ratio of 3.5.

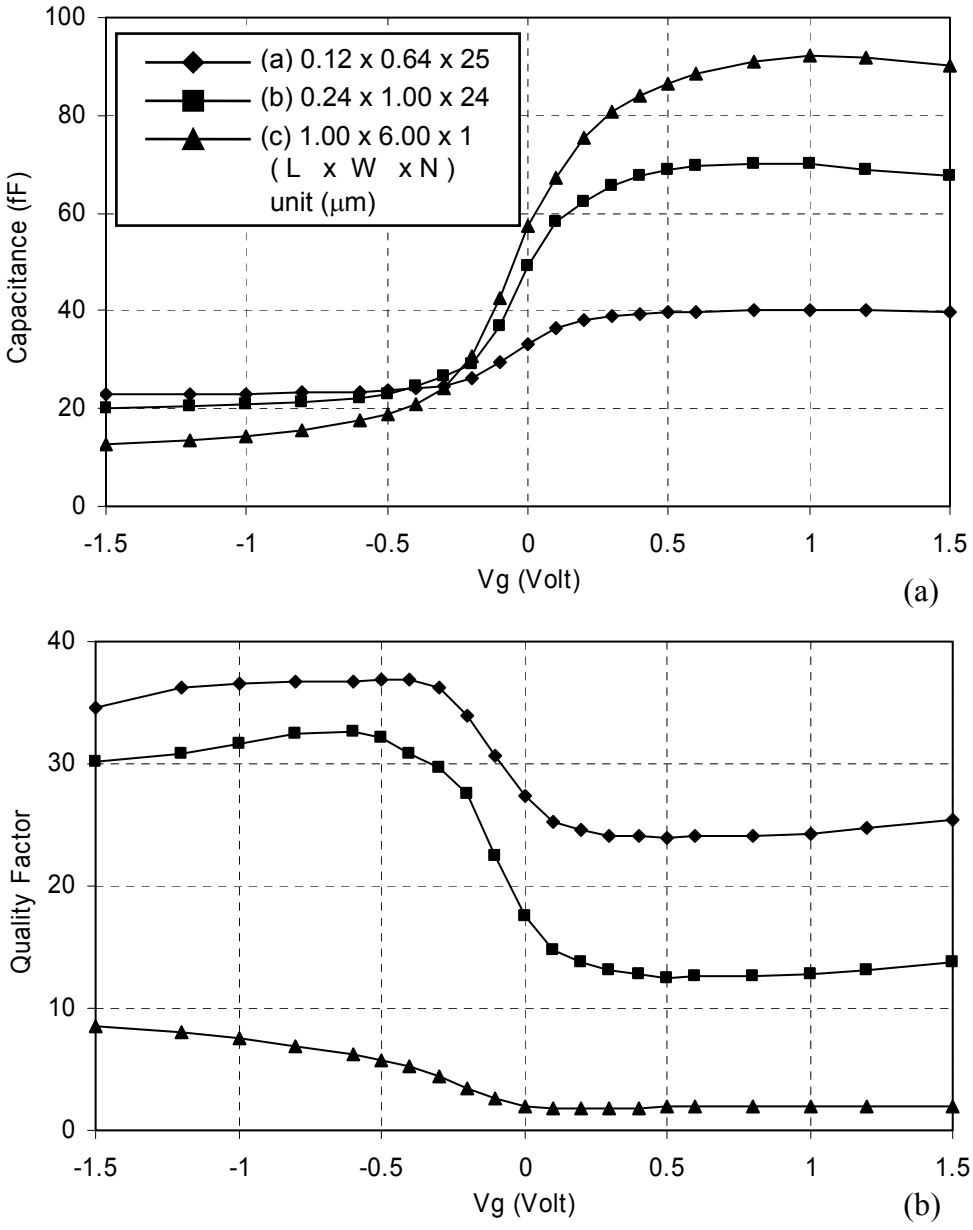


Figure 5-8 C-V and Q-V characteristics of the MOS varactors with different gate dimensions

Figure 5-9 shows the measured minimum Q and C_{max}/C_{min} ratio of varactors with varying gate lengths. The minimum Q decreases with the gate length, while the tuning

ratio increases. Depending on the operating frequency, phase noise, power consumption and tuning range requirements for the VCO, a suitable varactor structure can be chosen using a plot like this. For the 0.13-μm CMOS process, the gate lengths between 0.18 to 0.24 μm result good tuning and Q.

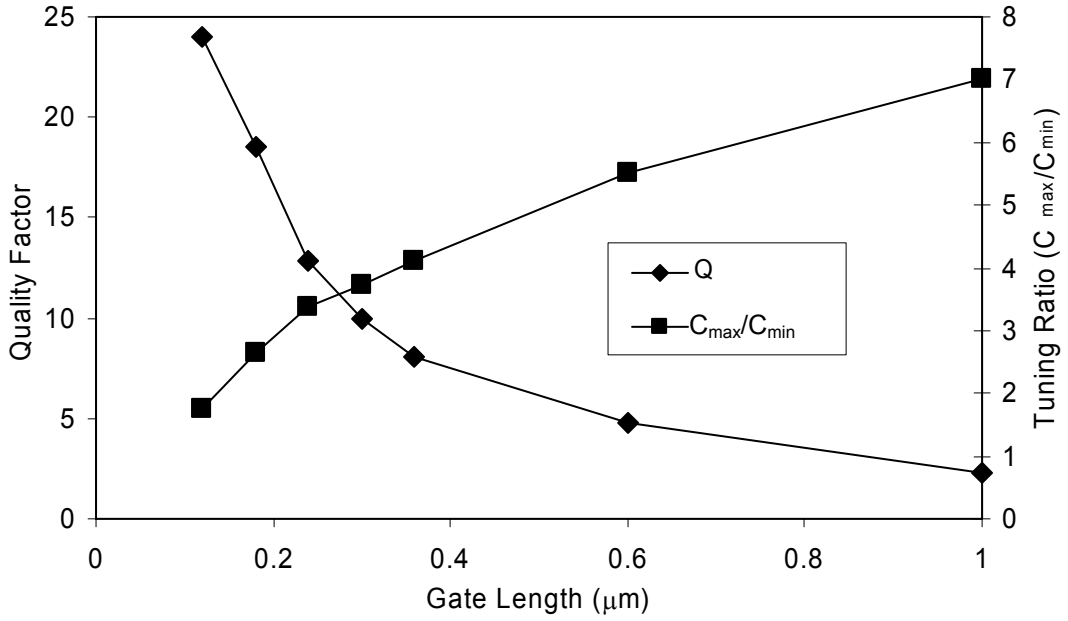


Figure 5-9 Minimum varactor Q and C_{max}/C_{min} ratio at 24 GHz as a function of gate length

5.4 High Performance On-Chip Inductor

Figure 5-10 shows the layout of differential circular inductor used in the 105-GHz VCO. To reduce the capacitance to substrate, only the top metal 8 layer is used. The metal 8 layer is 0.8 μm thick and ~5 μm above the silicon substrate. The metal width is 3.6 μm. Since the skin depth of copper at 105 GHz is ~0.20 μm, the metal width of inductor can be as narrow as ~6 x 0.20 = ~1.2 μm. The patterned ground shield is formed using the polysilicon layer and each finger is perpendicular to the metal trace. The spacing between polysilicon shields is set to ~4 μm to reduce the parasitic capacitance

without degrading the quality factor [78]. A lumped inductor model [79], [80], including a series resistor, shunt capacitors, and substrate resistors, is used for the design. The model parameters are extracted using Agilent Momentum, a 2.5-D EM field simulator. The simulations show the inductance of loop with a diameter of 57 μm is ~ 90 pH and Q_{bw} [81] is ~50 at 105 GHz. For the 59-GHz VCO, the inductor diameter is 89.6 μm and the trace width is 4.8 μm. The inductance is ~200 pH and Q_{bw} is ~35 at 60 GHz. Lastly, the interconnections carrying signals at the millimeter-wave frequencies have also been modeled using the lumped inductor model.

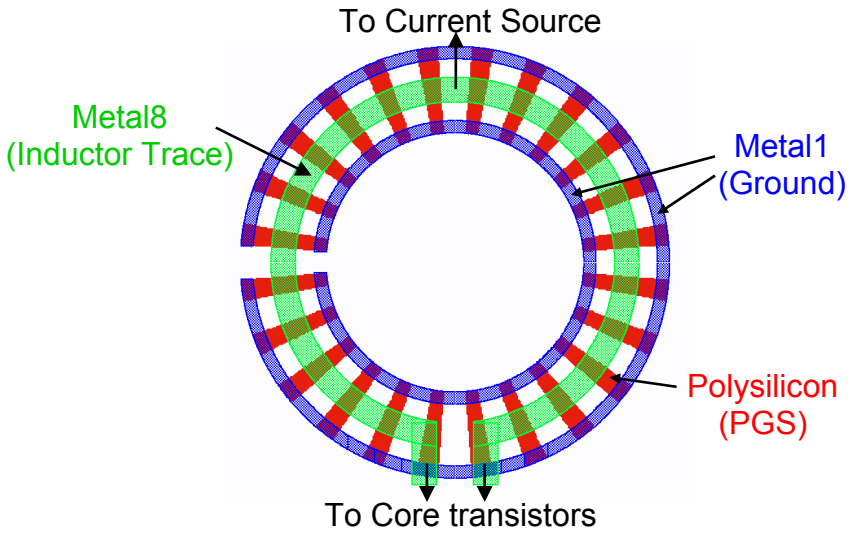


Figure 5-10 Differential inductor layout

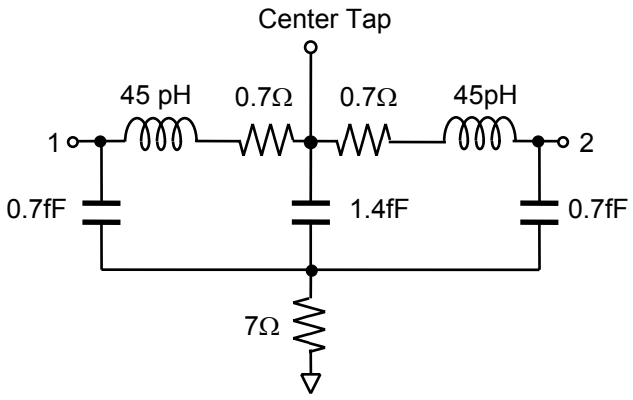


Figure 5-11 Lumped inductor model of differential inductor

5.5 Transistor Layout

As mentioned, to increase the oscillation frequency, the parasitic capacitance connected to the tank must be minimized. For the VCO's operating near 60 and 100 GHz, the capacitance of transistors in the 0.13-µm technology is comparable or larger than that from the varactors. Therefore, the parasitic capacitance of transistors must also be minimized. Figure 5-12 shows the top view of cross-coupled transistors, which is similar to that used in [82]. It consists of a top part (M_1) and a bottom part (M_2) that are directly cross connected from the drain to gate. This makes the metal interconnect between the two transistors shorter which lowers the loss and parasitic capacitance of the interconnections. The drains of fingers are connected together by metal6 lines. The finger width of transistors needs to be kept small to lower the gate resistance. This however increases the gate to body/substrate capacitance. Because of these two competing effects, there should be an optimal finger width. The final finger width of 0.64 µm is chosen to maximize f_{max} [82]. From the measured results in [58], f_{max} is expected to be ~120 GHz.

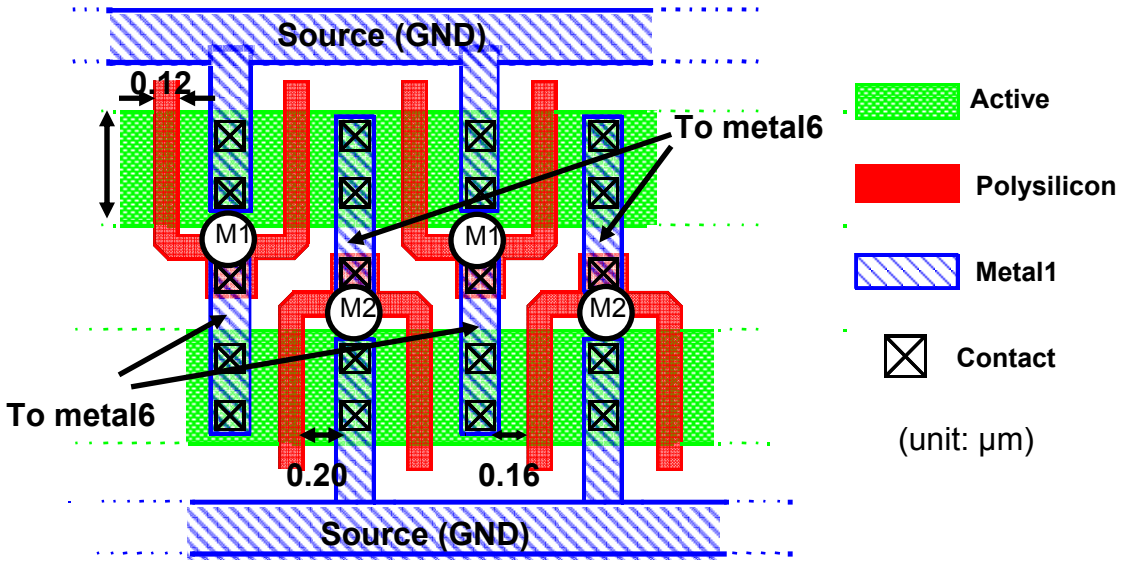


Figure 5-12 Cross-coupled transistor layout

As was done for the varactor, the metal spacing is intentionally increased. The spacing of source contact to gate is made 0.20 μm, so that the parasitic gate and drain to source capacitances are reduced at the expense of slightly larger source series resistance. The increased source-to-body capacitance has negligible impact on VCO operation since the source nodes are virtual grounds. The drain is usually made as small as allowed by design rules to reduce C_{db}. However, in the VCO, the gate to drain capacitors (C_{gd}) of two core transistors are connected to the anti-phase nodes. As shown in Figure 5-13, due to the Miller effect, the gate-to-drain overlap capacitance contribution to the tank is $2(C_{gd1}+C_{gd2})$. Thus, the effective transistor capacitance at the drain node is actually $C_{db}+4C_{gd}$.

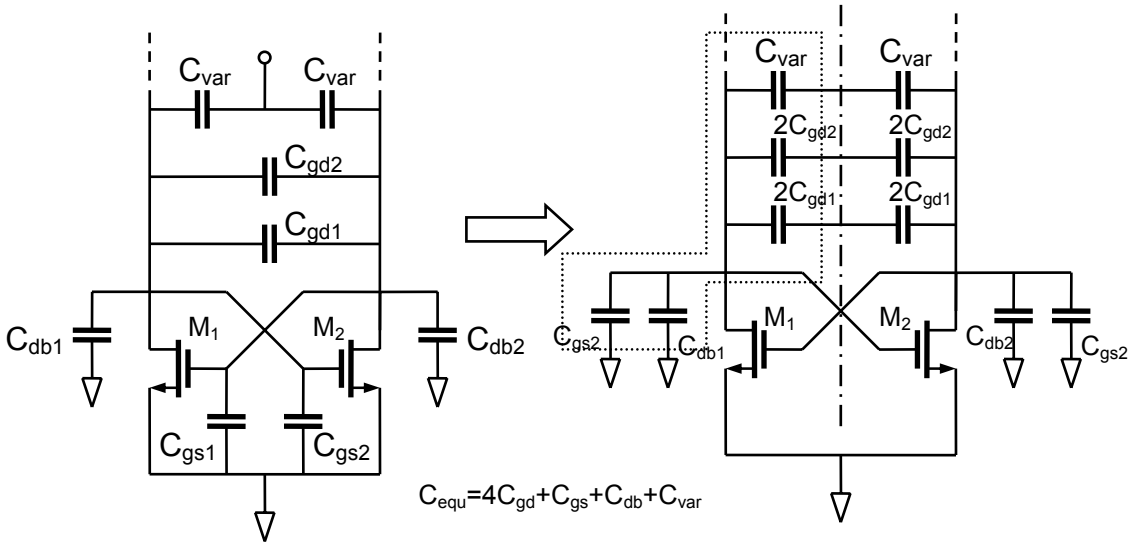


Figure 5-13 Capacitors in the VCO

Increasing the spacing between drain contact and gate decreases C_{gd} and increases C_{db}. Simulations show that the drain contact to gate spacing of ~0.16 μm minimizes the effective capacitance added to the tanks. As stated earlier, the capacitance of transistors is comparable or larger than that from the varactor. Because of this, the Q of LC-tank strongly depends on the transistor. For the 100-GHz VCO's, since the capacitance of

transistors is much larger than that of the varactors, the transistor capacitance is expected to determine the Q of the LC-tank.

5.6 Circuit Architecture

The VCO employs the NMOS cross-coupled topology and is shown in Figure 5-14. The resonator consists of a single-loop circular inductor and an accumulation mode MOS capacitor. The bias current is injected in the middle of the inductor by a PMOS transistor, M7. This enables the modulation of V_{drain} node by changing the V_{bias} voltage. As will be described, unlike other VCO's, this is the main mechanism used to tune the VCO frequency around 100 GHz. In addition, the buffer for driving the 50-Ω load utilizes two tapered stages to lower the capacitance added to the LC tanks.

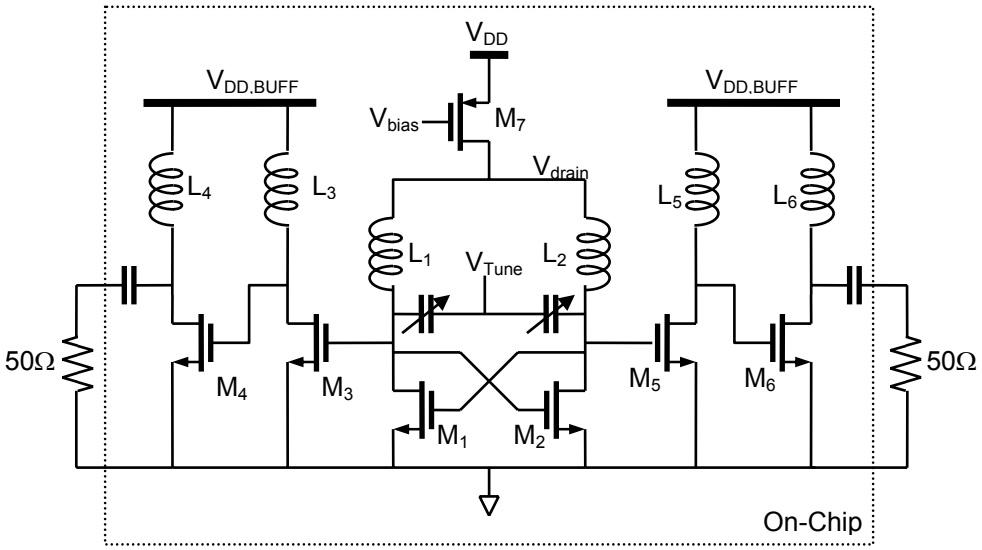


Figure 5-14 Schematic of the proposed VCO

The PMOS current source is used to utilize the full range of the varactor without requiring tuning voltages above V_{dd} or below zero. The varactor shows the best tuning around zero gate bias. For the VCO in Figure 5-14, the top plate (gate) voltage of varactor is set to ~$V_{DD}/2$ by using the PMOS current source on the top. When the bias

voltage on the bottom plate of varactor is varied between 0 and V_{DD}, the voltage across the varactor varies from $-V_{DD}/2$ to $V_{DD}/2$. Figure 5-8 also shows that the C-V curve is not monotonic due to the poly gate depletion when the gate bias is higher than 1 V. This may lead to a locking problem in the phase-locked loop [52]. Since V_{DD} is usually 1.2-1.5 V for the circuits built using this process, by limiting the gate to bulk voltage from $-V_{DD}/2$ to $V_{DD}/2$, the bias range affected by the poly gate depletion region is avoided.

5.7 60-GHz Wide Tuning Oscillators

5.7.1 Design Considerations

The 60-GHz WLAN band spans the frequencies between 59 and 64 GHz. The VCO for this application must have a tuning range greater than 5 GHz. However, the recently published CMOS VCO's operating near 40-60 GHz have tuning ranges significantly less than 5 GHz [53], [54], [62], except those fabricated using SOI processes due to lower parasitic capacitances in the SOI processes [55], [60]. A wider tuning range in bulk CMOS is also possible when the parasitic capacitances from the varactor, transistor and inductor are minimized as discussed above. The varactor value should be maximized and varactors with a larger tuning ratio should be used. This however, can degrade phase noise because of an increase of VCO gain and a decrease of varactor Q. To evaluate this trade-off for VCO's operating in the millimeter-wave frequency range, two VCO's with different varactor structures are fabricated. In the first VCO, varactors with twenty 0.12 μm (L) x 0.64 μm (W) fingers are used. In the second one, varactors with ten 0.24 μm (L) x 1 μm (W) fingers are used. The two varactor structures have nearly the same capacitance value in accumulation region. The core transistor width is chosen to be 14.72 μm. It is more than twice the minimum size required to sustain oscillation.

5.7.2 Experiment Results and Discussions

Figure 5-15 shows a micrograph of the 60-GHz VCO. Both VCO's start to oscillate with about 3.5 mA current from a 0.9-V supply when the varactors are biased in the depletion region (V_{tune} = 1.5 V). To achieve good phase noise performance and output power greater than -10 dBm, the measurements are made at 6.5-mA bias current and 1.5-V V_{DD}. The output buffer consumes about 10 mA from a 0.8-V supply. Figure 5-16 shows the output spectrum of the VCO. Figure 5-17 shows the measured carrier frequency vs. the tuning voltage for these two VCO's. For the VCO using 0.12-μm gate length varactors, the tuning range is 3.8 GHz, while for the second VCO using the varactors with 0.24-μm gate length, the tuning range is 5.8 GHz. This difference is due to the larger tuning from the varactors with a longer channel length. Figure 5-18 shows phase noise at 10 MHz offset vs. the tuning voltage for these two VCO's. The phase noise peaks around 0.5~1.0-V tuning voltage due to larger VCO gain resulting

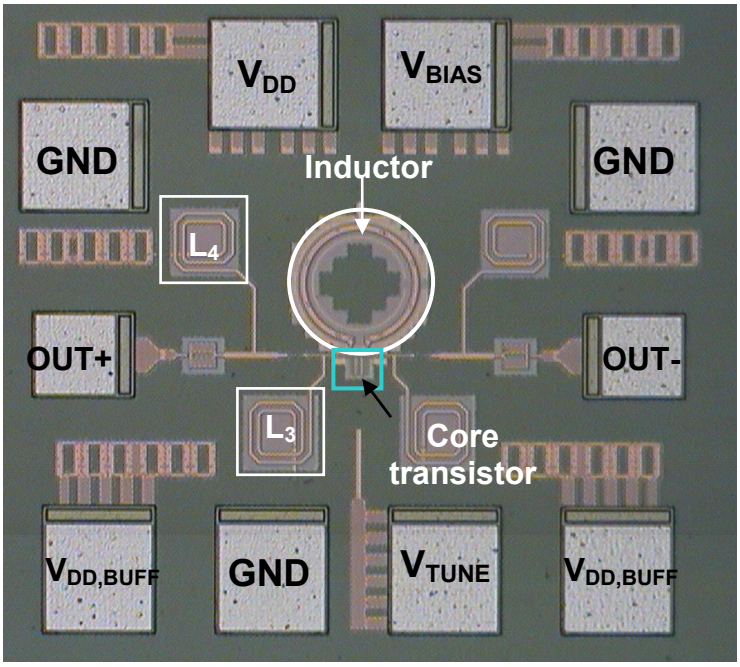


Figure 5-15 Micrograph of the 60-GHz VCO

from a higher rate of change of varactor capacitance. When the varactors are biased in the depletion region (V_{tune} = 1.5 V) and accumulation region (V_{tune} = 0 V), the VCO using varactors with a shorter finger length has phase noise of -89 dBc/Hz (not shown) and

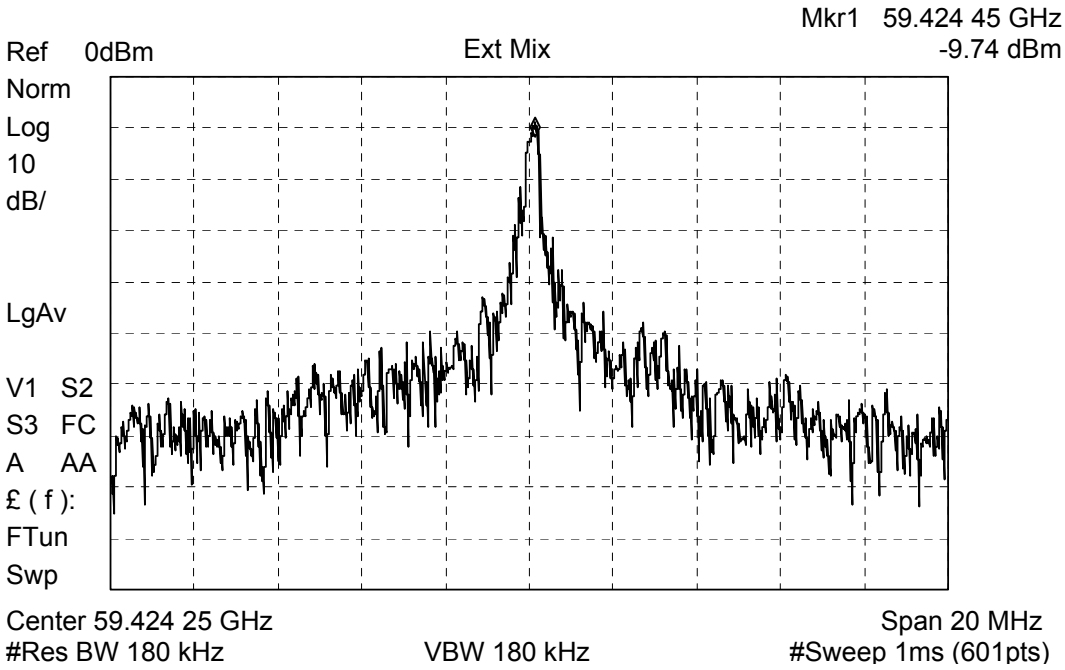


Figure 5-16 Output spectrum of the 59-GHz VCO (V_{DD} = 1.5V, V_{tune}= 1.5V)

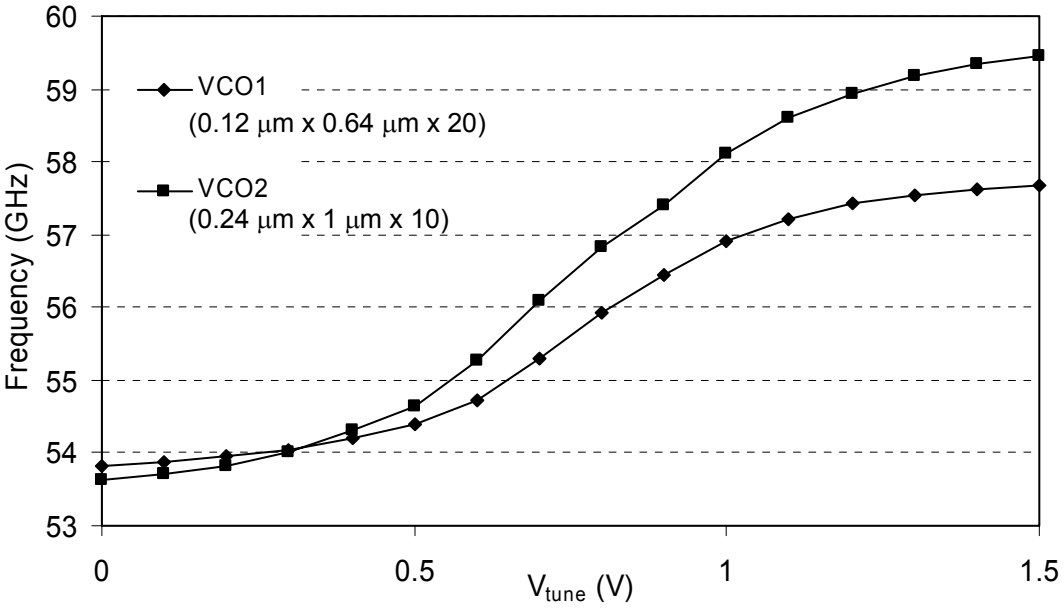


Figure 5-17 Frequency range of two different VCO's using different varactor structures

-108 dBc/Hz at 1-MHz and 10-MHz offsets, respectively, which are ~ 1 dB lower than that of the second VCO. When the varactors are biased in the transition region, the VCO using the longer gates shows 2-3 dB higher phase noise. The differences are attributed to the 50% lower Q of the longer channel varactor as well as the larger VCO gain resulting from the ~60% larger tuning range.

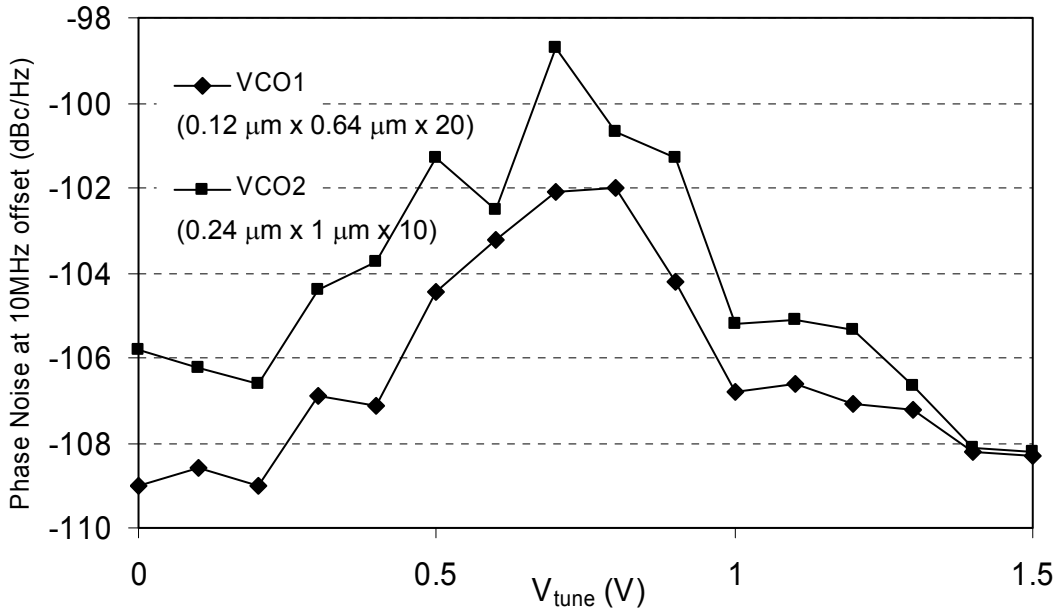


Figure 5-18 Phase noise of the two different VCO's as function of the tuning voltage

5.8 100-GHz Oscillators in 0.13-μm CMOS

5.8.1 Design Considerations

Since the f_{max} of NMOS transistors in the 0.13-μm CMOS process is higher than 100 GHz, so it should be possible to implement a VCO operating near 100 GHz. By applying the low parasitic, low loss design techniques discussed above, VCO's operating between 90 to 105 GHz were designed. To explore the frequency limit of this process, the core transistor sizes varying from 12.16 to 8.32 μm are used to tune the center frequencies of VCO's. For the varactors, the minimum gate length is not used. Instead,

one 0.24 μm x 0.9 μm finger with a larger tuning ratio is used. For the cross-coupled transistors, the finger width is 0.64 μm. The number of fingers is changed from 19 to 13.

Transmission lines have been used for matching and tuning in the circuits operating at frequencies from 60 to 100 GHz [56]-[58]. However, a quarter-wavelength is still about 600 and 375 μm at 60 and 100 GHz, respectively. The relatively long transmission line will increase the circuit size, as well as increasing the loss. The dimensions of components in the 105 GHz VCO are less than 90 μm or ~6% of a wavelength. This makes the lumped element analysis still applicable for these components even at 105 GHz. In the design, the lumped model of varactor was extracted from the measurement at 24 GHz and the inductor model was constructed using Agilent Momentum. The simulated carrier frequencies and tuning range are within 5% of the measurements.

5.8.2 Millimeter-Wave Spectrum Measurement Setup

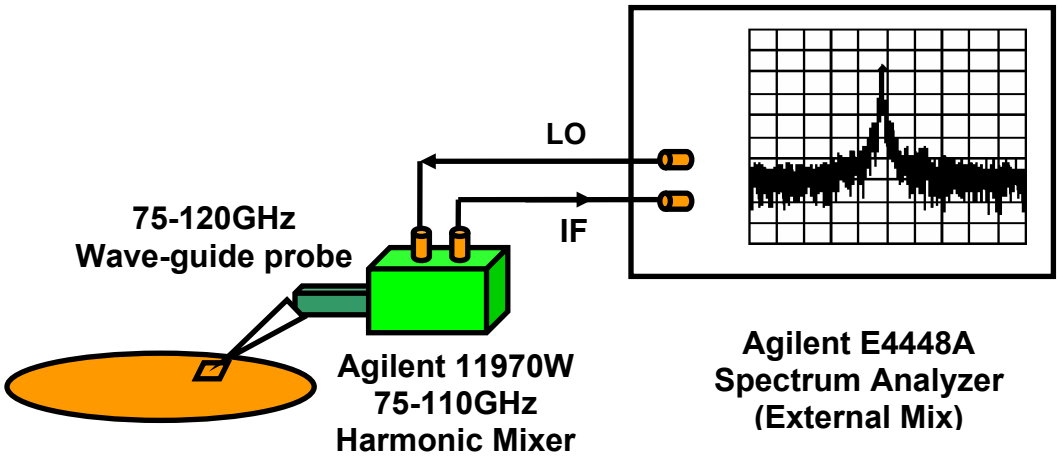


Figure 5-19 100-GHz VCO measurement setup

Making spectrum measurements at millimeter-wave frequencies gets progressively more difficult as the frequencies get higher. Figure 5-19 shows the setup to measure a frequency source around 100 GHz. The VCO's were measured on-wafer with an Agilent

E4448A spectrum analyzer and an Agilent 11970W 75-110 GHz harmonic mixer. The harmonic mixer down-converts the VCO output to 321.4 MHz [83], [84]. A 75-120 GHz W-band wave-guide probe is used to measure the VCO's operating near 100 GHz.

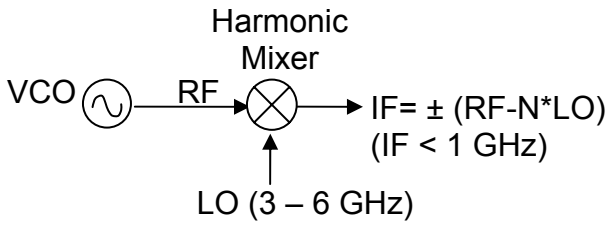


Figure 5-20 Simplified block diagram of measurement setup

The most common architecture for spectrum analysis uses fundamental mixing, i.e. IF = ± (RF - LO). However, this technique is less desirable for measurements at higher microwave and millimeter-wave frequencies due to the need for a high performance local oscillator with a very high and very wide frequency range. Instead, using a harmonic of the local oscillator provides several benefits. These benefits depend on whether the first mixer is located inside the spectrum analyzer (internal mixing) or outside (external mixing) of the analyzer. Figure 5-20 shows the simplified block diagram of the measurement setup. The frequency relationship can be expressed as IF = ± (RF – N x LO). The RF frequency can be obtained using RF = N x LO ± IF and the correct harmonic number can be automatically found using the signal identification function in spectrum analysis [83], [84]. The harmonic number N ranges from 6 to 54, and the LO frequency is around 3 to 6 GHz. Presently, the harmonic mixers which can cover up to 325 GHz are commercially available.

The main benefit of harmonic mixing is the ability to analyze higher frequencies by using the same local oscillator and most of the same IF structures that are also employed to analyze signals at lower frequencies. With harmonic mixing, the local oscillator need

not have a signal source with frequency near the frequency of signals being measured. The LO only needs to have a harmonic (with sufficient energy to drive a mixer) at near the frequency of signal being measured. However, there are also drawbacks and performance limitations including reduced frequency accuracy and stability, increased phase noise, undesired and unidentified mixer products, reduced amplitude sensitivity, and reduced amplitude accuracy.

The VCO frequency can be obtained using the signal identification function. This works well for the VCO measurements below 100 GHz. However, sometimes this function fails for oscillators operating around or above 100 GHz, most likely due to the signal not being sufficiently stable. Instead, to obtain the value of N, the LO frequency is changed by Δf, which changes IF by $\pm N \times \Delta f$. Then, the output frequency of VCO can be calculated using $RF = N \times LO \pm IF$. The sign depends on whether IF increases or decreases with the LO frequency change. Actually, this procedure is similar to that used by the built-in signal identification function, where the LO frequency is also changed by some amount depending on the harmonic number [84].

5.8.3 99-GHz Voltage-Controlled Oscillator

The 99-GHz VCO using 9.6-μm wide cross-coupled transistors starts to oscillate at the bias current and supply voltage of 3.4 mA and 1.0 V. Once again, for more stable oscillation and larger output power, the measurements are made at higher bias current of 6 mA and V_{DD} of 1.5 V. An amplifier with 20-dB gain and 4.5-dB noise figure is added between the mixer output and spectrum analyzer to reduce the impact of background noise from the analyzer. The measured output spectrum is shown in Figure 5-21. The external amplifier gain, ~40-dB conversion loss of mixer and ~3-dB loss from probe and

cable were de-embedded. The measured phase noise is about -103 dBc/Hz at 10-MHz offset from the carrier.

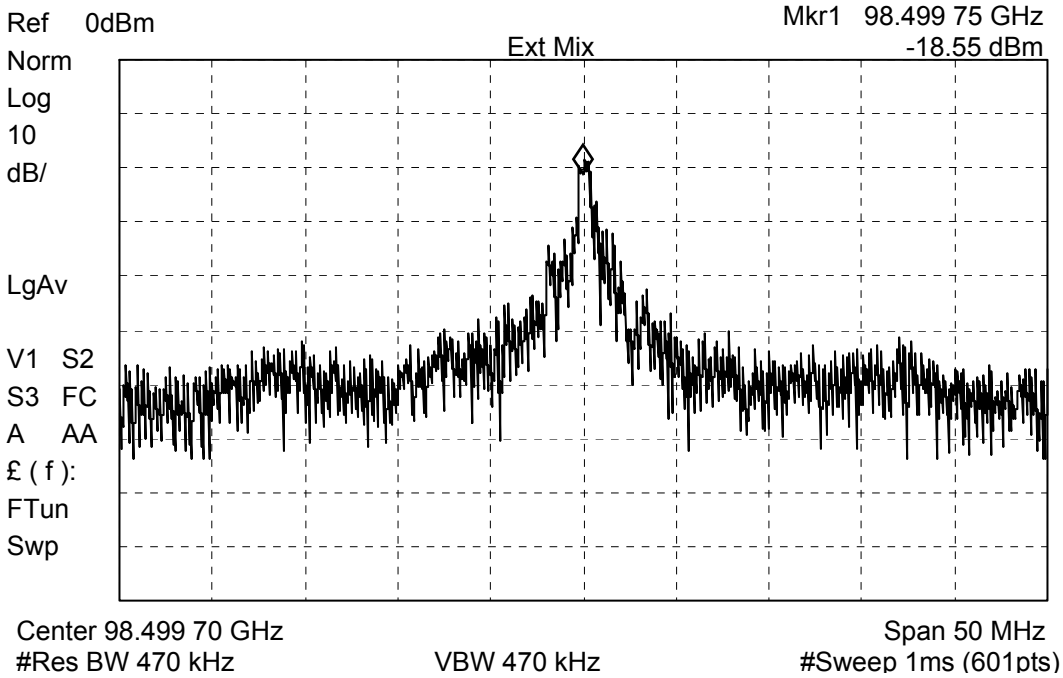


Figure 5-21 Output spectrum of the 99-GHz VCO

Since the transistor capacitance is the dominant contributor to the LC-tank capacitance and the transistor capacitance depends on the bias conditions, the transistor capacitance can be tuned to increase the tuning range. In fact, several authors have suggested changing supply voltage to increase the tuning range of VCO's [54], [56]. However, varying supply voltage is not practical. A simple way to vary the DC bias of transistors is to change the gate bias of the tail transistor (M_7 in Figure 5-14). By limiting the current range, it is possible to limit the variations of output power and phase noise over the tuning range. In this implementation, the V_{bias} is used for fine tuning and the varactors are used for coarse tuning. Since the varactors are biased in either strong accumulation or depletion, where the VCO gain due to the varactors is smaller, this helps to keep the phase noise low. Figure 5-23 shows the tuning characteristics of VCO. By

varying V_{bias} from 0 to 0.59 V when V_{tune} is 1.5 V, the bias current can be changed from 4.5 to 10 mA and the VCO can be tuned between 97.8 and 99.2 GHz. By biasing the MOS varactor in the accumulation region (V_{tune} = 0 V), the output frequency can be varied between 96.7 to 98 GHz. Over the tuning range, the phase noise at 10-MHz offset varies from -99.5 to -102.7 dBc/Hz and output power varies from -22 to -18 dBm. The total tuning range is 2.5 GHz or ~ 2.5%. The best phase noise is measured at 6-mA bias current instead of the largest current. If larger output power level variations and higher phase noise can be tolerated, the tuning range can be increased to ~3 GHz.

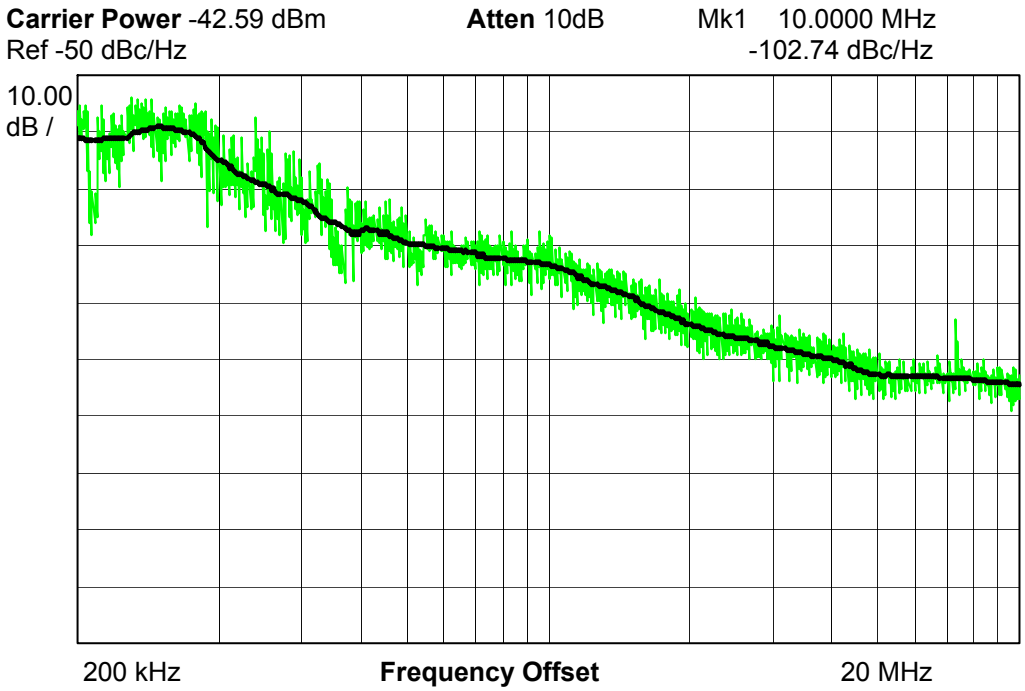


Figure 5-22 Measured phase noise plot of the 99-GHz VCO

5.8.4 105-GHz Voltage-Controlled Oscillator

By reducing the core transistor width to 8.32 m, a VCO operating from 105.1 to 105.3 GHz is demonstrated. Figure 5-24 shows a micrograph of the VCO. The VCO consumes 6 mA from a 1.2-V supply. Figure 5-25 shows the measured output spectrum. When it was reported, this was the highest fundamental frequency CMOS circuit up to

that time. The tuning range is only 200 MHz. The circuit stops oscillation when the varactors are biased in the accumulation region or the bias current is reduced below 5 mA. This also suggests the oscillation frequency of 105 GHz is very close to the limit of 0.13-μm CMOS process. The VCO achieves phase noise of -97.5 dBc/Hz at 10-MHz offset. Because the signal is week and unstable, the phase noise plot like Figure 5-22could not be obtained.

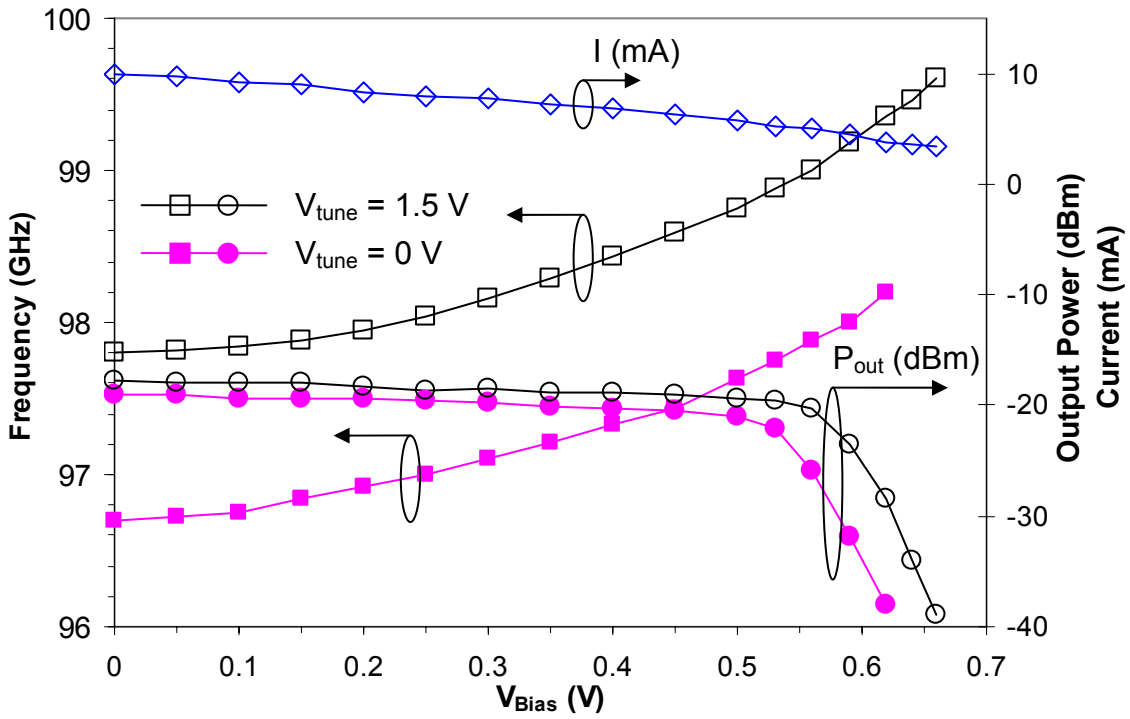


Figure 5-23 Frequency tuning, current consumption and phase noise of the 99-GHz VCO at 1.5 V V_{DD}.

5.9 Oscillators Operating above 100 GHz in 90-nm CMOS

The 90-nm CMOS process offers a unity power gain frequency, f_{max}, of around 200 GHz [71], therefore, it should be feasible to build oscillators operating well above 100 GHz. In this section, F-band (90–140GHz) VCO's fabricated in the UMC 90-nm CMOS [70] process is discussed. The architecture of the VCO's is the same as the 100-GHz VCO's

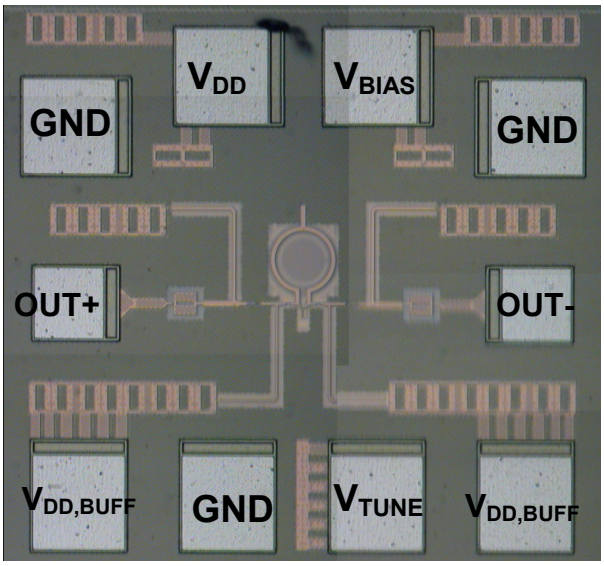


Figure 5-24 Micrograph of the 105-GHz VCO

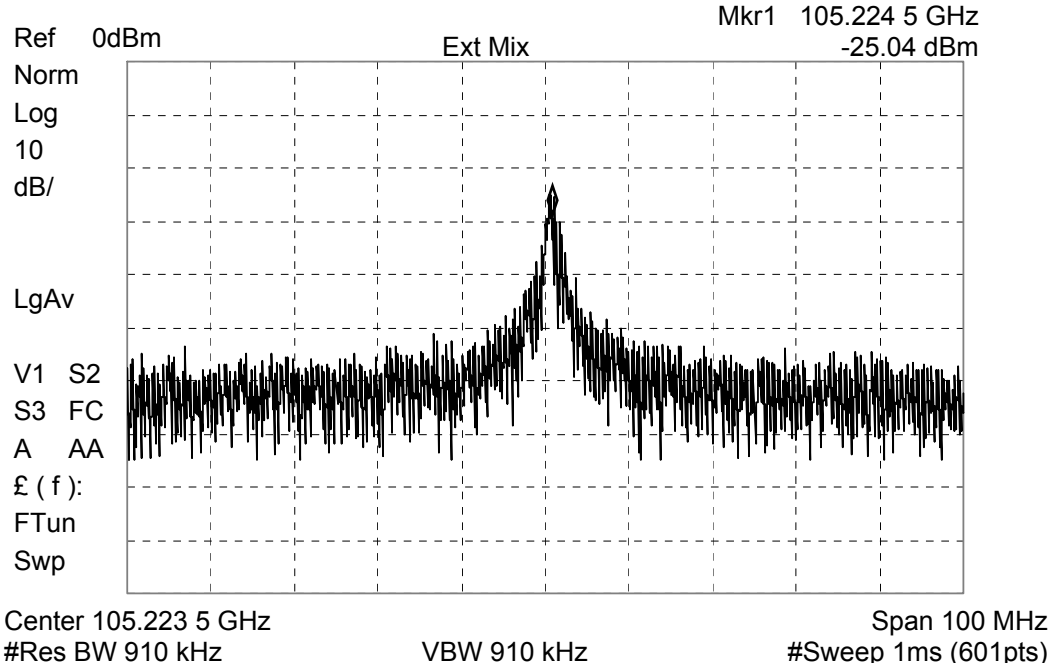


Figure 5-25 Output spectrum of the 105-GHz VCO

discussed above. Figure 5-26 shows the micrograph of a 140-GHz VCO. Each VCO occupies 540 x 360 μm^2 including bond pads. The cross-coupled transistors are 8.36 μm wide with the minimum gate length. They consist of 11 fingers, whose width is 0.76 μm. The varactors are formed by two 0.5 μm x 0.18 μm fingers with contacts on both sides of

the gate finger. The inductor trace was formed using the top metal 9 (copper) layer with a thickness of 0.8 μm. The trace width is chosen to be 2 μm. To explore the frequency limit of this process, three VCO's with varying inductor size are fabricated while keeping the transistors and varactors the same. The diameters of the circular inductors are 53, 40.8 and 31.6 μm, respectively. The inductance is estimated to be between 80 and 50 pH.

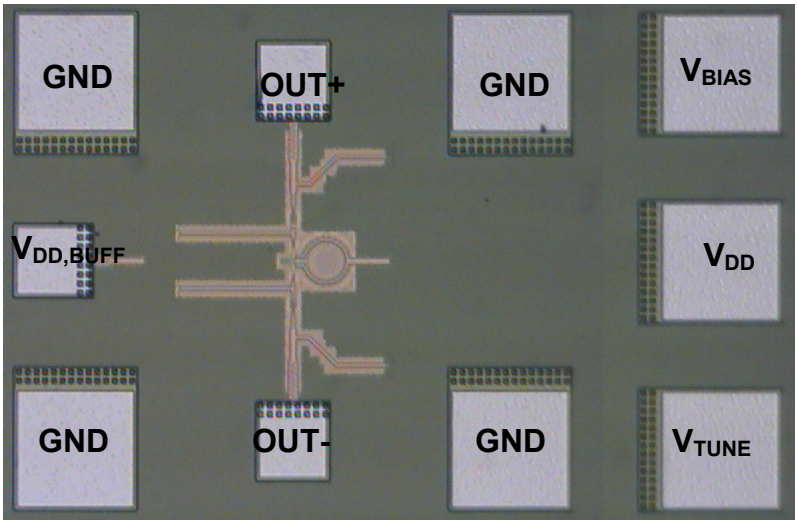


Figure 5-26 Photograph of the 140-GHz VCO

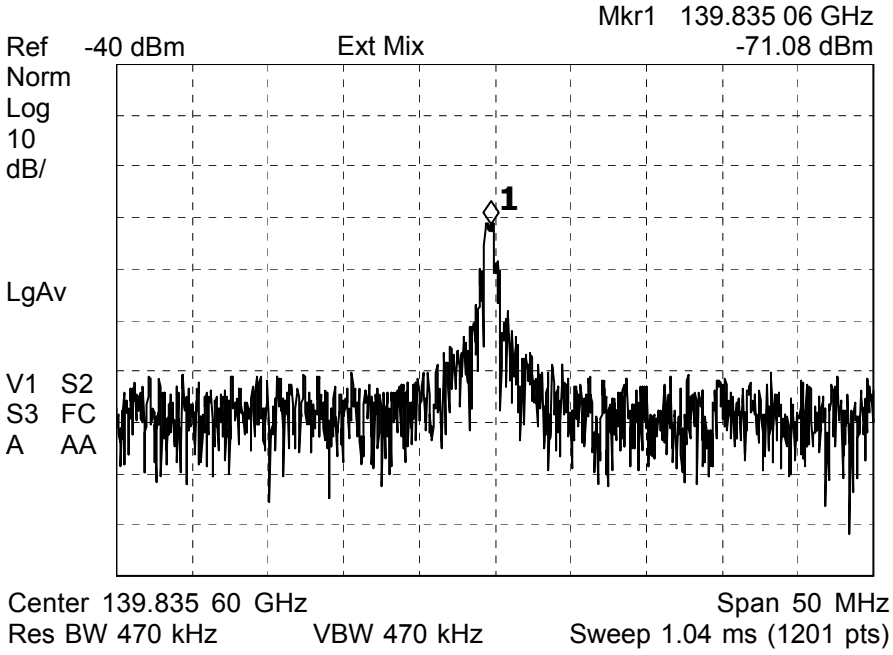


Figure 5-27 Output spectrum of the 140-GHz VCO

The 140-GHz VCO starts to oscillate at a bias current of 4.5 mA with V_{DD} = 1 V. For more stable oscillation and larger output power, the measurements are made at a bias current of 8 mA and V_{DD} = 1.2 V. Figure 5-27 shows the output spectrum. The conversion loss of harmonic mixer is about 50 dB and the insertion loss of probe is about 2 dB at 140 GHz. Thus, the output is estimated to be somewhere around -19 dBm. Figure 5-28 shows the measured free running VCO phase noise plot. The phase noise plot is noisy especially at low offset frequencies due to the frequency drift. The phase noise is about -85 dBc/Hz at 2-MHz offset from the carrier.

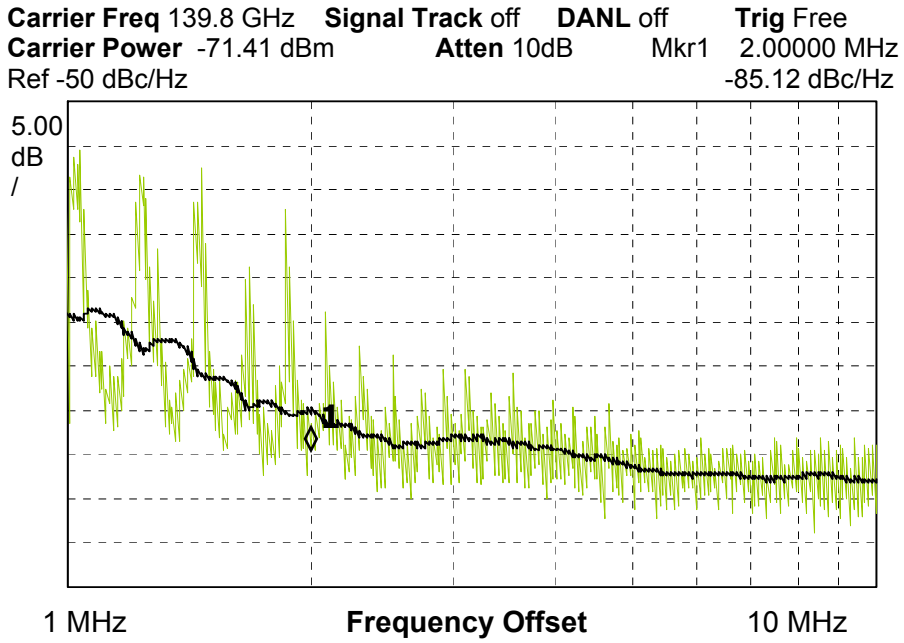


Figure 5-28 Phase noise plot of the 140-GHz VCO

Figure 5-29 shows the output frequency versus tuning voltage (V_{tune}) at 1.2-V V_{DD}. At bias current of 8 mA, the output frequency can be tuned from 139 to 139.8 GHz by changing the varactor voltage. As mentioned before, the operating frequency of VCO can also be tuned by the bias current. The output frequency can be tuned from 139 to 140.2 GHz if both the bias current and varactor are varied. In order to keep the output power

within 3 dB of the maximum, V_{bias} is kept lower than 0.56 V or the bias current is kept higher than 6.4 mA. If larger output power variation can be tolerated, the operating frequency can be increased to as high as 140.5 GHz. For this VCO, the bias current is used for coarse tuning and the varactor for fining tuning. The tuning curves for V_{bias}'s of 0 and 0.56 V overlap by ~ 500 MHz.

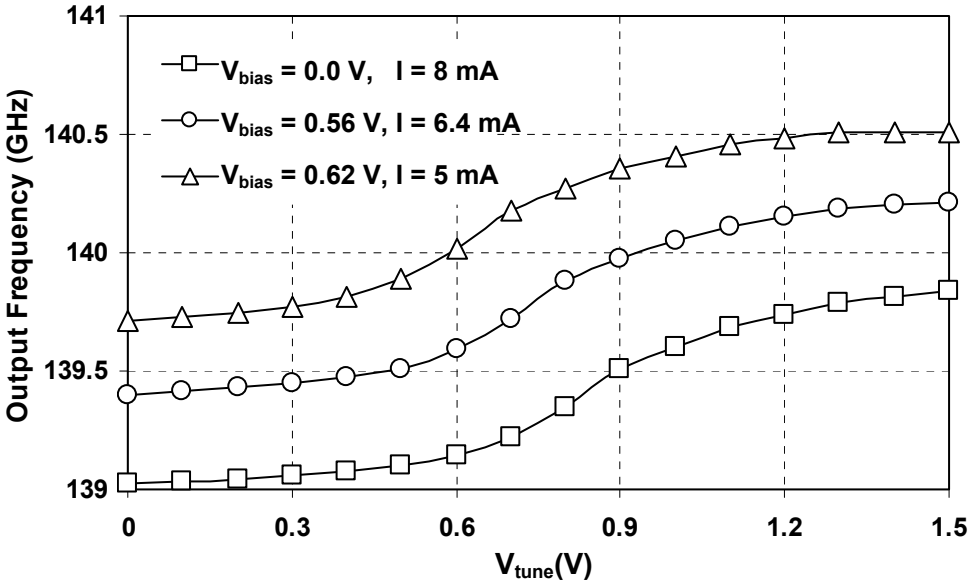


Figure 5-29 Output frequency versus the tuning voltage

The operating frequency decreases monotonically with the increase of bias current or supply voltage for the oscillators in the 0.13-μm process (Figure 5-23). However, this is not the case for the VCO's fabricated in this process. Figure 5-30 shows the output frequency versus supply voltage for the 140-GHz VCO when both V_{bias} and V_{tune} are grounded. The minimum operating frequency is achieved around 1.2 V. The VCO stops oscillation when the supply voltage is lower than 1.0 V or higher than 1.5 V. For the 110-GHz and 123-GHz oscillators, the minimum operating frequencies are achieved at 1.5 V and 1.35 V, respectively. These minima are most likely due to the enhanced polysilicon gate depletion effect in the transistors with a thinner gate oxide (~2 nm) layer. The supply

voltages for 90-nm processes are less than 1.2 V, and this phenomenon should in general not matter.

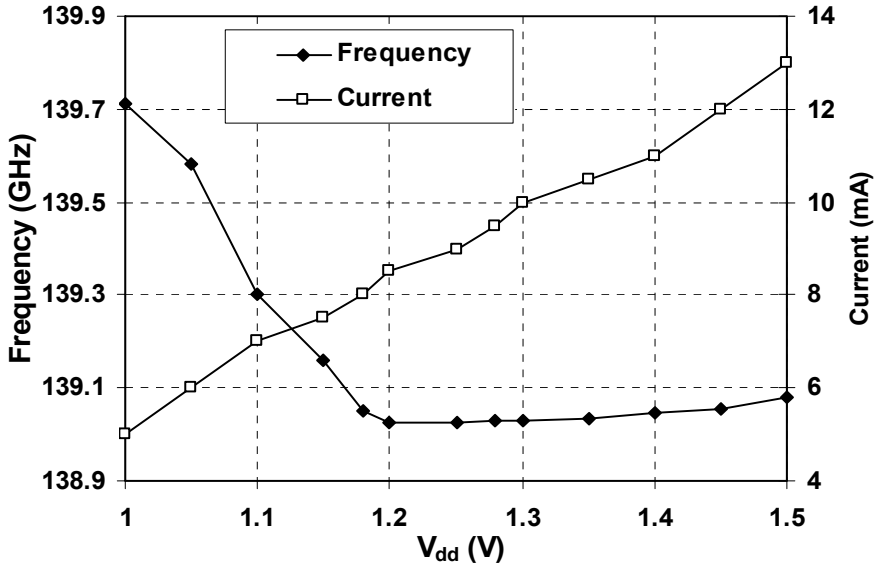


Figure 5-30 Output frequency versus V_{DD} for the 110-GHz VCO

Table 5-1 Summary of the measured VCO performance

Version	109	123	140
V_{DD} [V]	1.2	1.2	1.2
Current [mA]	8	8	8
Output Power [dBm]	-10	-14[1]	-19[1]
Freq.Range[GHz] (varactor only)	108.3 – 109.2	122.1 – 122.95	139 – 139.8
Freq. Range[2] [GHz] (varactor + current)	107.95 – 110.4[3]	122 – 123.6[4]	139 – 140.2
2-MHz offset	-88.2[3]	-86.4[4]	-85.1
10-MHz offset	-105.2[3]	-100.2[4]	-93
Technology	UMC 90-nm logic CMOS		
Chip Area	540 μm x 360 μm		

[1] Accurate conversion loss of the harmonic mixer is not available, and the output power estimation is only approximate.
[2] Output power levels are kept within 3dB of the maximum.
[3] V_{DD} = 1.5 V. Phase noise is measured at 12 mA bias current.
[4] V_{DD} = 1.35 V. Phase noise is measured at 10 mA bias current.

Table 5-1 summarizes the measured VCO performance. With increasing oscillation frequency, output power drops and phase noise increases. The phase noise for 109, 123

and 140-GHz VCO's were measured at V_{DD} of 1.5, 1.35, and 1.2 V, respectively. These are the points at which the output frequency versus V_{DD} plots have the minima, and the supply pushing is minimized. At these bias conditions, the VCO's become sufficiently stable to attempt the phase noise measurements. An interesting possibility for exploration is reducing the supply pushing by making the flat portion in Figure 5-30 to be centered around V_{DD} for the circuit.

5.10 192-GHz Push-Push Oscillator

5.10.1 Circuit Design

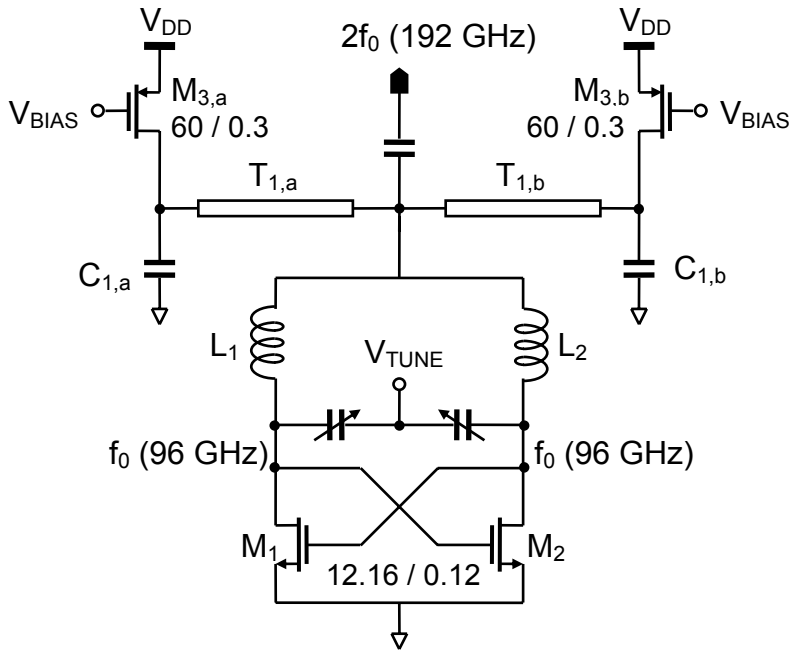


Figure 5-31 Schematic of the push-push VCO

Figure 5-31 shows the schematic of push-push VCO. It is based on the fundamental mode VCO discussed above. Cross-coupled transistors M_1 and M_2 form the VCO core. The width of the transistors is 12.16 μm. Inductors, L_1 and L_2 (~45 pH), accumulation mode MOS capacitors, and the capacitances associated with M_1 and M_2 form the LC resonant tank. At the virtual ground (or common mode) nodes, the anti-phase

fundamental signals cancel out and the second harmonic signal can be extracted. The middle point of inductors L_1 and L_2 has the lowest parasitic capacitance to ground among the common-mode nodes. This makes the impedance at resonant frequency the highest and the best port to extract the push-push output. A quarter wavelength transmission line tuned for the second harmonic frequency is usually used to increase the amplitude of second harmonic while suppressing the fundamental signal. In this design, the transmission line and the current source transistor are broken into two parts to make the layout symmetric, which better suppresses the fundamental signal at the common mode nodes.

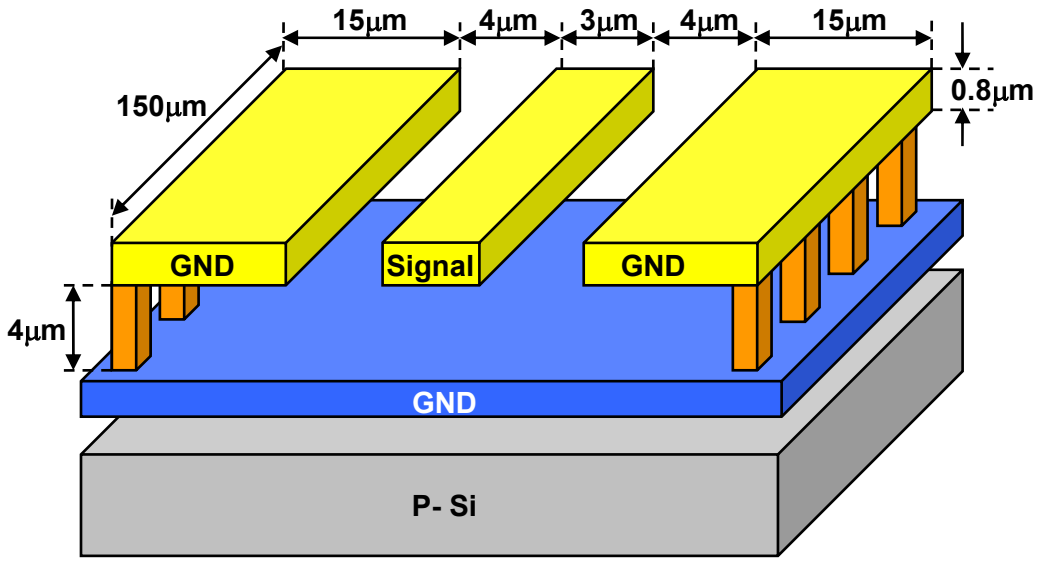


Figure 5-32 Grounded coplanar waveguide transmission line

The transmission line structure is shown in Figure 5-32 and is formed using the grounded coplanar waveguide (CPW) structure [31], [85]. Compared to the conventional CPW, the ground plane isolates the line from the lossy silicon substrate and reduces the insertion loss. The lines are formed using the top metal 8 layer and the ground plane is formed by metal 1. The transmission line width and gap are 3 and 4 μm, respectively.

The characteristic impedance of the line is about 65 Ω. The length of lines is 150 μm. This length is slightly shorter than λ/4, so that the impedance looking into the transmission line is inductive to resonate the capacitances from the pad and other metal interconnections. The 2-pF bypass capacitors ($C_{1,a}$, $C_{1,b}$ in Figure 5-31) serve as short around 190 GHz. They are formed using the parasitic capacitance between adjacent metal layers [50]. The metal 8, 6, 4 and 2 layers form the top plate, and metal 7, 5, 3 and 1 layers form the bottom plate. The capacitance density is 0.55 fF/μm^2. The transmission lines and bypass capacitors are simulated using the Ansoft HFSS, a 3D EM simulator.

5.10.2 Experiment Results

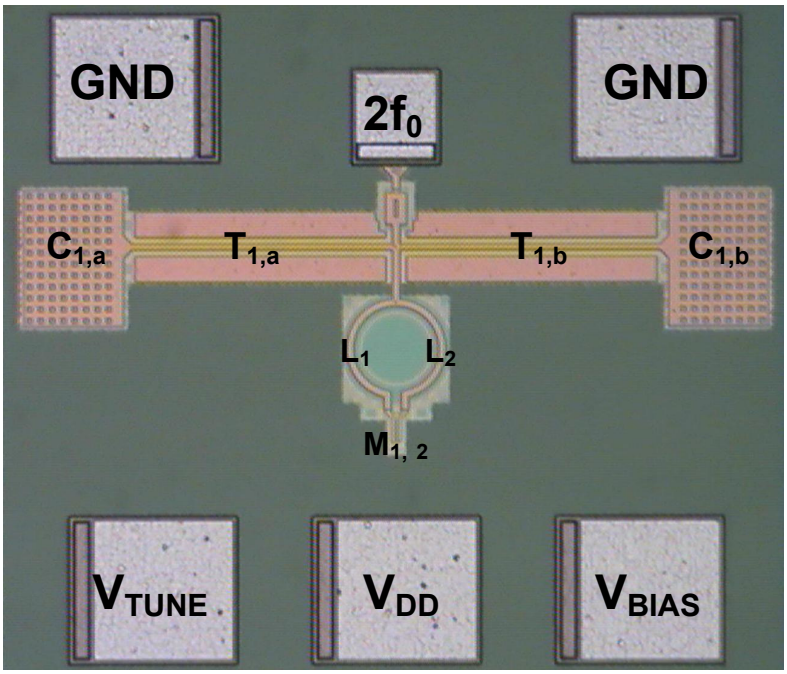


Figure 5-33 Micrograph of the 192-GHz push-push VCO

Two VCO's are implemented in the UMC 0.13-μm CMOS. In the first version, to achieve higher oscillation frequency, the output buffers and bond pads for the fundamental output were not included. The chip occupies 450 μm x 390 μm including the bond pads. A micrograph is shown in Figure 5-33. The second VCO including the buffers

for the fundamental port was also fabricated. Due to the capacitance from output buffers, the measured fundamental oscillation frequency is about 4 GHz lower.

The chip was measured on-wafer as illustrated in Figure 5-19 using a GGB WR-5 (140 to 220 GHz) waveguide probe. The cut-off frequency of the TE_{10} mode in WR-5 waveguide is 115.7 GHz, which attenuates the fundamental signal entering the waveguide probe. The VCO output spectrum is measured using an OML M05HWD (140 to 220 GHz) harmonic mixer and an Agilent E4448A 50-GHz spectrum analyzer. An Agilent 11970W (75 to 110 GHz) harmonic mixer has also been used to evaluate the fundamental output.

The circuit starts to oscillate at 3.2-mA bias current. However, no signal was detected at the push-push port until the bias current is increased to above 8 mA due to the detection limit of the measurement setup. To obtain higher output level, the circuit is measured with 11 mA bias current from a 1.5-V supply. Figure 5-34 shows the output spectrum and the measured signal level is -82 dBm. The conversion loss of harmonic mixer is around 60 dB at 190 GHz. The insertion loss of probe is about 2 dB. Thus, the signal is estimated to be about -20 dBm. The oscillation frequency can be tuned from 191.4 to 192.7 GHz by changing V_{tune} from 0 to 1.8 V. 192-GHz is the highest operating frequency for any silicon based circuits. Because the output of harmonic mixer is weak, the phase noise could not be directly measured. The phase noise of fundamental output is -106 dBc/Hz at 10-MHz offset for the VCO with the output buffer. The phase noise at the push-push port is expected to be 6 dB higher. Due to the coupling through the substrate and metal interconnection, the fundamental signal also appears at the push-push port. The measured fundamental signal is about -30 to -25 dBm at the push-push port after

calibrating the losses. As expected, the frequency tuning range of fundamental signal is exactly one half of the second harmonic.

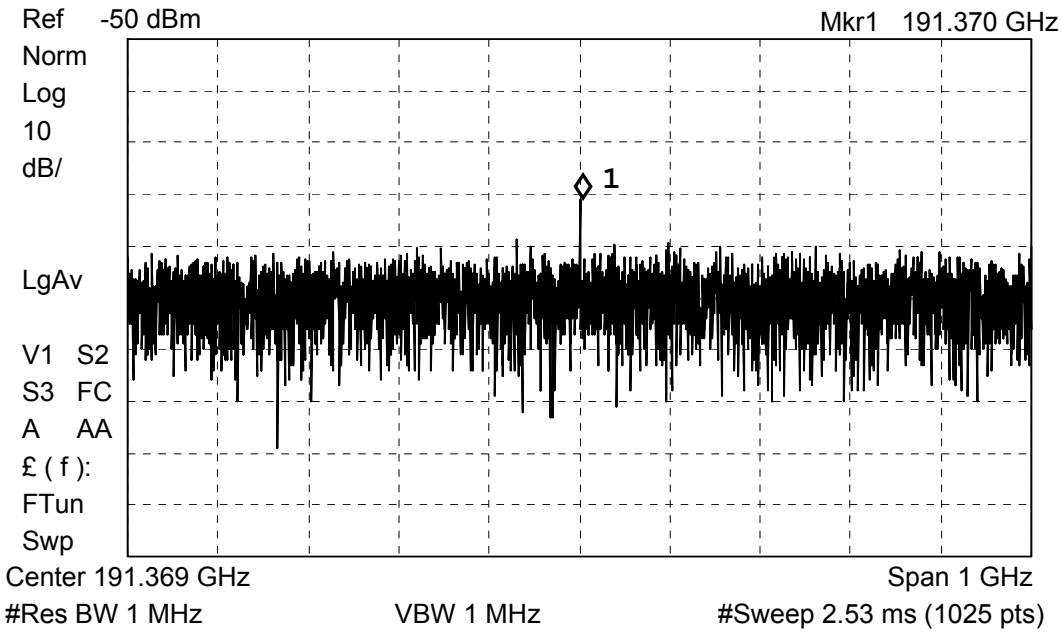


Figure 5-34 Measured VCO output spectrum

5.11 Summary and Discussions

Millimeter-wave VCO's operating between 60 and 192 GHz are presented. Reducing the metal parasitic capacitances of varactors, inductor and transistors is the key for achieving the wide tuning range at 60 GHz and operation close to 200 GHz using a 0.13-μm bulk CMOS process. The 192-GHz operating frequency is the highest for any silicon based circuits, while 140-GHz is the highest fundamental frequency in silicon. Using push-push architecture, a 280-GHz VCO in 90-nm CMOS should be possible. Given that the state of art is 65-nm, generation of THz signals using CMOS technology cannot be far in the future.

Table 5-2 compares the characteristics of recently published millimeter-wave fundamental VCO's implemented using silicon technologies. The 59-GHz VCO

implemented in the 0.13-μm bulk CMOS process has almost comparable phase noise and tuning range as that implemented in a 90-nm SOI CMOS process [60]. This work also shows that with optimized design, a much higher VCO operating frequency can be attained. As a matter of fact, the 105-GHz VCO in 0.13-μm CMOS has a higher operating frequency than the one fabricated in a 90-nm technology [56]. This work has also shown that even at 100 GHz, lumped elements which should occupy a smaller area than the components based on transmission lines can be used.

Table 5-2 Comparison with recently reported high speed fundamental mode VCO's in silicon technologies.

Ref	Freq.	Phase Noise	V_{dd}	P_{dc}	Tuning	Technology
This work	59	-89@1MHz	1.5	9.8	5.8	0.13-μm CMOS
	90	-104@10MHz	1.5	7.5~16	2.2[a]	
	98.5	-102.7@10MHz	1.5	7~15	2.5[a]	
	105.2	-97.5@10MHz	1.2	7.2	0.2	
	110	-105.2@10MHz	1.5	18	2.4[a]	90-nm CMOS
	123	-100.2@10MHz	1.35	13.5	1.6[a]	
	140	-93@10MHz	1.2	9.6	1.2[a]	
[53]	50	-100@1MHz	1.3	13	1.0	0.25-μm CMOS
[54]	51	-85@1MHz	1.0	1	1.0[a,b]	0.12-μm CMOS
[55]	40.7	-89@1MHz	1.8	11.3	6.0	0.13-μm SOI
[56]	103.9	-85@10MHz	1.5	45	N/A	90-nm CMOS
		-94@10MHz	1.5	180	N/A	
[60]	60.6	-90@1MHz	1.5	21	8.3[b]	90-nm SOI
[61]	85.8	-97.5@1MHz	3	25.8	2.3	0.12-μm SiGe
[62]	43	-91@1MHz	1.0	7	1.7	0.13-μm CMOS
[63]	117.2	N/A	2.5	25-70	3.7[a]	0.25-μm SiGe
	114.5	N/A	2.5	N/A	8.7	
[64]	80.6	-97@1MHz	N/A	1200[c]	6.7	0.35-μm SiGe
	100.2	-90@1MHz	N/A	N/A	6.2	

[a] The bias conditions of the transistors are changed to increase tuning range.
[b] The tuning voltage is higher than supply voltage.
[c] Higher power consumption is due to the powerful output buffer and large output power level.

CHAPTER 6
50-GHz CMOS PHASE-LOCKED LOOP

6.1 Introduction

Millimeter-wave band VCO's have been demonstrated in CMOS. However, no CMOS phase-locked loops (PLL's) operating in the millimeter-wave band have been reported. The existing PLL's operating at frequencies above 50 GHz are based on III-V [86] or SiGe bipolar technologies [87]-[89]. Besides the VCO, the other challenging circuit block in the PLL is the high speed frequency divider. The dynamic frequency divider [13] could potentially be faster than the static divider. However, dynamic divider usually consumes much more power, which makes it not attractive. To obtain high speed with low power consumption, an LC-resonator based injection locked frequency divider (ILFD) is proposed [90], [91]. However, the ILFD usually shows much narrower operating frequency range compared with other dividers. To utilize an ILFD in a PLL, the operating frequency range must be extended and the method to accomplish this is presented in this chapter.

In addition, a 50-GHz phase-locked loop implemented in the UMC 0.13-μm CMOS process is presented. The PLL can be locked from 45.9 to 50.5 GHz and output power level is around -10 dBm. The circuit including buffers consumes 57 mW from 1.5/0.8 V supplies. The phase noise at 50 kHz, 1 MHz and 10 MHz offset from the carrier is -63.5, -72, and -99 dBc/Hz, respectively. The PLL also outputs -22-dBm second order harmonic frequencies between 91.8 and 101 GHz. Section 6.2 describes the fundamental theory of

the charge-pump PLL. Section 6.3 discusses the high frequency ILFD design. The measured results of 50-GHz PLL are presented in Section 6.4.

6.2 Fundamental of Phase-Locked Loop

6.2.1 Basic Phase-Locked Loop

A phase-locked loop is a feedback control system that operates on the excess phase instead of the voltage of the output signal. Shown in Figure 6-1 is a simple PLL, which consists of a phase detector (PD), a loop-filter, a VCO and a frequency divider (1/N) [92]-[94]. The PD detects the phase difference between feedback signal and input single, and the feedback loop minimizes this difference. The loop is considered "locked" if the phase difference is constant with time. During the locked condition, the phase detector produces an output proportional to phase difference $\Delta\phi$. The loop filter is a low-pass filter that suppresses high-frequency component in the PD output and allows the DC value to pass and control the VCO frequency. The input reference frequency and the divider output frequency are equal and the PLL output frequency is exactly N times of the input frequency.

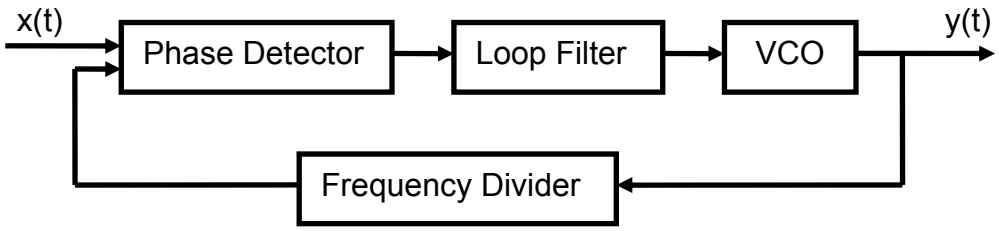


Figure 6-1 Basic phase-locked loop

The most popular phase-detector is a charge-pump phase-frequency detector (PFD). The PFD can detect both phase and frequency differences. It provides a frequency-sensitive signal to aid acquisition when the loop is out of lock. The charge pump is so

named because it delivers charge to the loop filter with the amount of charge proportional to the phase error.

6.2.2 Phase Frequency Detector and Charge Pump

Figure 6-2 shows a block diagram of the PFD. The circuit consists of two D flip-flops with reset control. Both the D inputs of flip-flops are connected to logic ONE. Signals A and B are two clock inputs. When $Q_A = Q_B = 0$, a rising edge on A causes $Q_A = 1$. A subsequent rising edge on A does not affect Q_A, until a rising edge on B sets $Q_B = 1$ and resets both flip-flops through an AND gate. $Q_A = Q_B = 1$ for a short period of time which is the total delay of the AND gate and reset path. Figure 6-2 shows the input and output waveforms of the PFD. If the frequency of input A is higher than B, then the PFD generates positive pulses at Q_A, and vice versa. If the frequencies are equal, PFD generates pulses at either Q_A or Q_B with a pulse width equal to the phase difference of two inputs. Figure 6-3 shows the input-output characteristic of the PFD. The linear operating range is 4π radians.

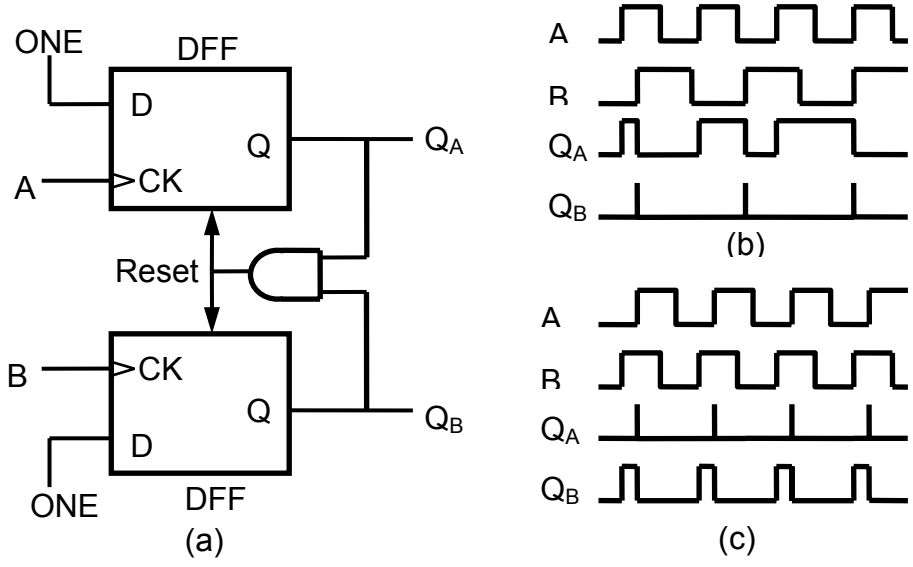


Figure 6-2 (a) Phase frequency detector block diagram and PFD input/output waveform with (b) $f_A > f_B$, (c) A lagging B

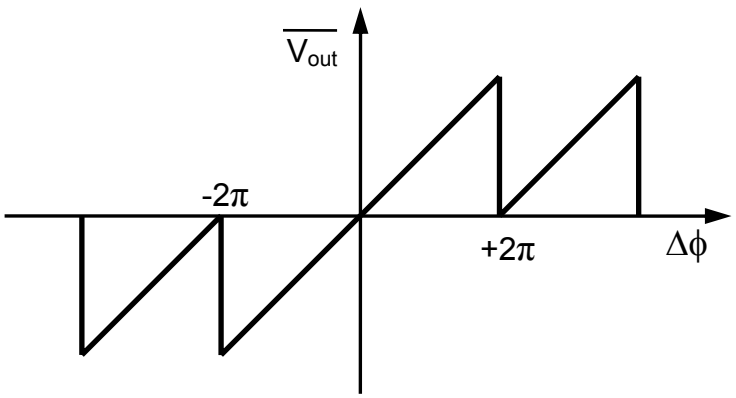


Figure 6-3 PFD transfer function

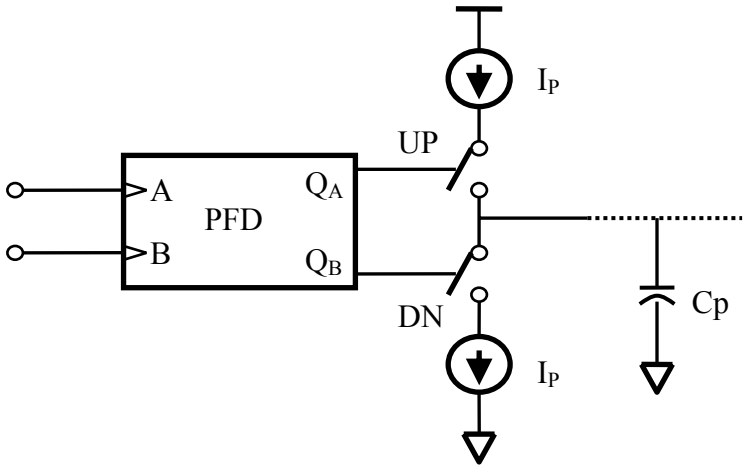


Figure 6-4 Charge pump with phase/frequency detector

The PFD outputs drive a three-state charge pump as shown in Figure 6-4. The charge pump consists of two current sources and two switches. The switches are controlled by the two PFD outputs. If $\phi_A > \phi_B$ or A leads B, positive pulse on Q_A turns on the UP switch to deliver charges to C_p with the amount of charge equals to the charge pump current I_p times the Q_A pulse width. If $\phi_A < \phi_B$ or A lags B, the positive pulse on Q_B turns on the DN switch to removes charges from C_p. In the third state, when $Q_A = Q_B = 0$, both UP and DN switch are open, the charge pump output remains high impedance and the charges on the capacitance C_p are kept constant.

6.2.3 Linear Model

Figure 6-5 shows the block diagram of charge-pump PLL. Because of the switching operations of charge-pump, the PFD and charge-pump work as discrete-time circuits and the whole PLL is a time-varying system. A simple transfer function analysis is not directly applicable to this system. However, if the loop bandwidth is much smaller than the reference frequency, the VCO control voltage changes by a very small account during each cycle of the reference signal. The changes in a single cycle becomes unimportant, while the average behavior over many cycles is of relevance and the linear analysis using transfer functions can be applied as in the continuous-time systems.

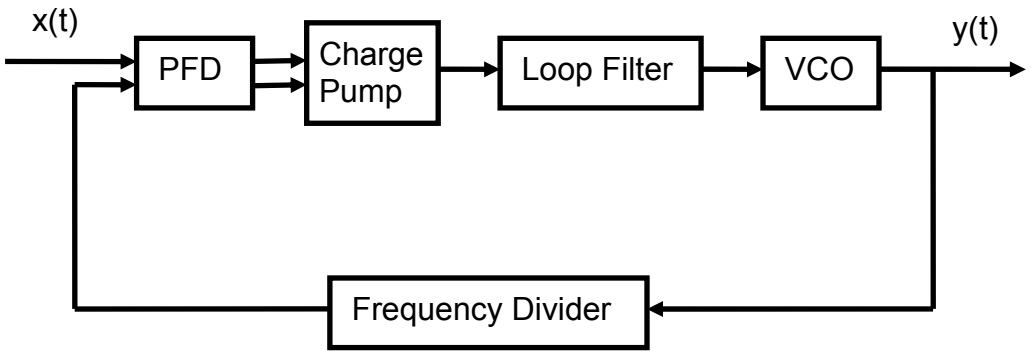


Figure 6-5 Charge-pump PFD PLL block diagram

Figure 6-6 shows a block diagram of PLL with *s*-domain transfer functions for each block. For an ideal VCO, the output frequency is a linear function of control voltage V_{ctrl},

$$\omega_{out} = \omega_{FR} + K_{VCO} V_{ctrl} \tag{6-1}$$

where K_{VCO} is called the VCO gain. Treating a VCO as a linear time-invariant system, with the control voltage as input and excess phase $\Phi_{out}(t) = K_{VCO} \int V_{ctrl} dt$ as output, the VCO transfer function is

$$\frac{\Phi_{out}}{V_{ctrl}}(s) = \frac{K_{VCO}}{s} \tag{6-2}$$

Using the continuous-time approximation, the charge pump average error current over a reference cycle is

$$i_d = I_p \cdot t_p / T = I_p \cdot \phi_e / 2\pi \tag{6-3}$$

where I_p is the charge pump current, t_p is the charge pump current pulse width due to a phase error ϕ_e between reference and divider output. The charge pump gain can be expressed as

$$i_d / \phi_e = I_p / 2\pi \tag{6-4}$$

$Z_F(s)$ is the transfer function of loop filter and it will be discussed in the next part. Since frequency divider divides the phase by N, its transfer function is 1/N, which can be considered as the feedback coefficient.

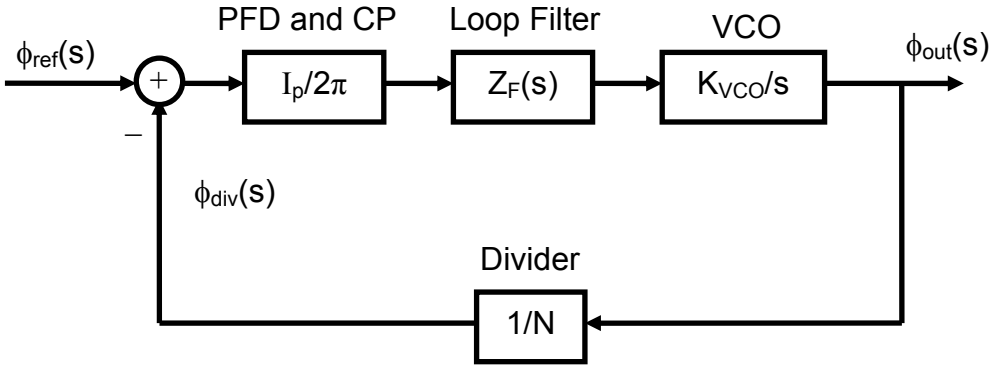


Figure 6-6 Linear model of charge-pump PFD PLL

From the linear model in Figure 6-6, the open-loop and close-loop transfer functions of PLL can be expressed as,

$$H_{OL}(s) = \frac{I_p}{2\pi} \cdot Z_F(s) \cdot \frac{K_{VCO}}{s} \tag{6-5}$$

$$H_{CL}(s)=\frac{H_{OL}(s)}{1+\frac{1}{N}H_{OL}(s)}=\frac{\frac{I_p}{2\pi}\cdot Z_F(s)\cdot\frac{K_{VCO}}{s}}{1+\frac{I_p}{2\pi}\cdot Z_F(s)\cdot\frac{K_{VCO}}{s}\cdot\frac{1}{N}} \tag{6-6}$$

The loop transfer function is

$$T(s)=\frac{1}{N}H_{OL}(s)=\frac{1}{N}\frac{I_p}{2\pi}\cdot Z_F(s)\cdot\frac{K_{VCO}}{s} \tag{6-7}$$

6.2.4 Loop Filter and Frequency Response

A passive second-order loop filter that can be used in a PLL is shown in Figure 6-7. The loop filter input is the charge pump current I_p and the output voltage V_{ctrl} is connected to VCO control voltage. For the second order loop filter in Figure 6-7, the transfer function is

$$Z_F(s)=\frac{V_{ctrl}(s)}{I_p(s)}=\left(\frac{1}{sC_p}\right)//\left(R_z+\frac{1}{sC_z}\right)=\frac{1+sR_zC_z}{s\left(sR_zC_zC_p+C_z+C_p\right)} \tag{6-8}$$

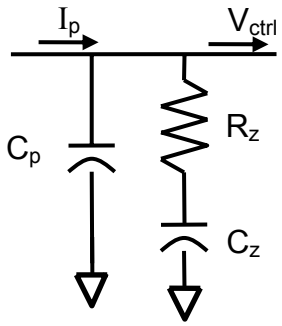


Figure 6-7 Second-order passive loop filter

Inserting Equation (6-8) into Equation (6-7), the PLL loop transfer is

$$T(s)=\frac{I_p}{2\pi}\cdot\frac{K_{VCO}}{s}\cdot\frac{1}{N}\cdot\frac{1+sR_zC_z}{s\left(sR_zC_zC_p+C_z+C_p\right)} \tag{6-9}$$

The open loop transfer function has two poles at the origin, which indicates the charge-pump PLL with a second-order loop filter is a third-order type II loop [28]. Figure 6-8

shows the bode plot of a third-order charge pump PLL loop transfer function. As an indicator for the stability of a negative feedback system, the phase margin is defined as the phase difference between -180º and the actual phase angle of the loop transfer function at unity gain frequency, ω_t, as shown in Figure 6-8. Like most feedback systems, phase margin of 60º or more is preferred.

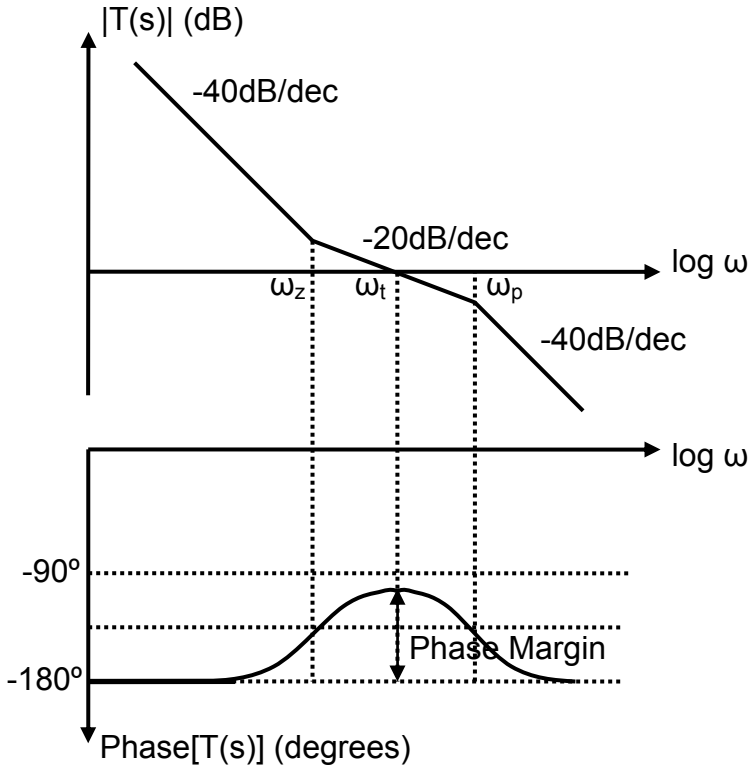


Figure 6-8 Bode plot of third-order charge pump PLL

6.2.5 Phase Noise in the Loop

The phase noise at the PLL output comes from the reference, VCO, frequency divider, PFD, charge pump and loop filter, as shown in Figure 6-9. The PLL operates as a low-pass filter for the noises from PFD, CP and divider, a band-pass filter for the noise from loop filter, and a high-pass filter for the noise from VCO. Therefore, for a third-order charge pump PLL, the phase noise spectrum has a shape similar to Figure 6-10.

Within the loop bandwidth, the phase noises from reference and frequency divider are dominant and outside the loop bandwidth, the noise from VCO is dominant. More discussions on the noise contribution of the each component in a PLL can be found in [28], [94].

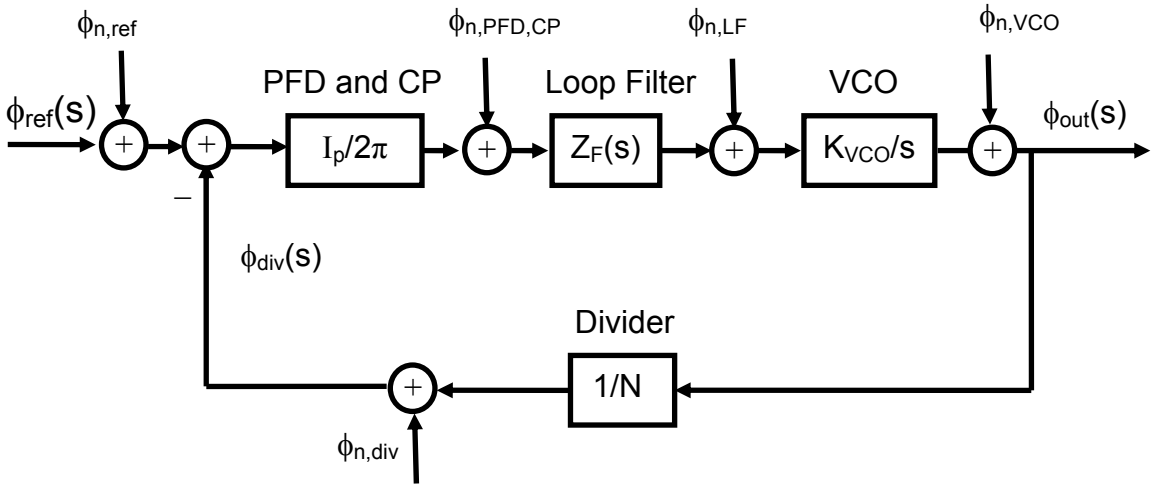


Figure 6-9 PLL block diagram with noise sources

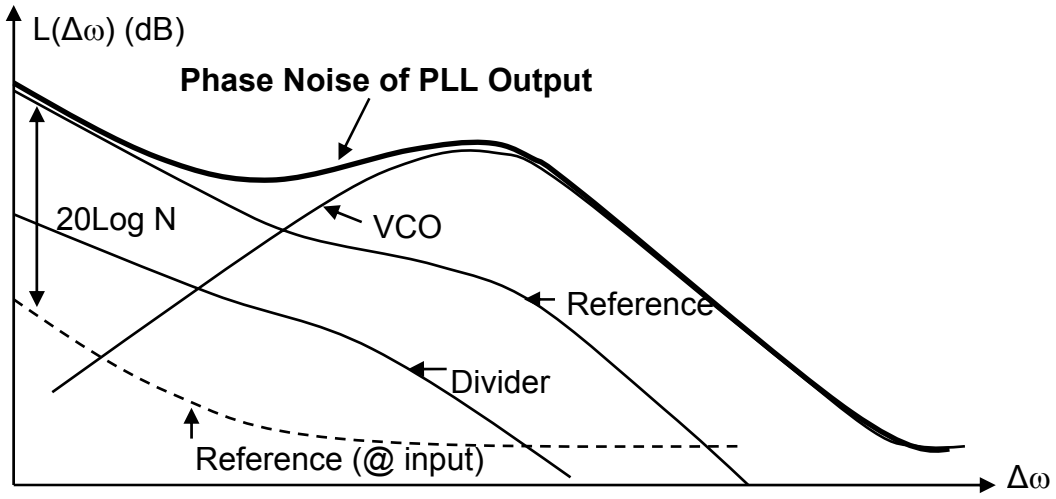


Figure 6-10 Output phase noise plot of a third order charge pump PLL

6.3 High Frequency Injection-Locked Frequency Divider

The VCO output frequency will be pulled away if a continuous wave signal at a different frequency is nearby. This phenomenon is called VCO injection pulling.

Injection pulling is especially an undesired effect in direct conversion transceiver, where the PA is running at the same frequency as the VCO. However, it can be exploited to realize an ILFD.

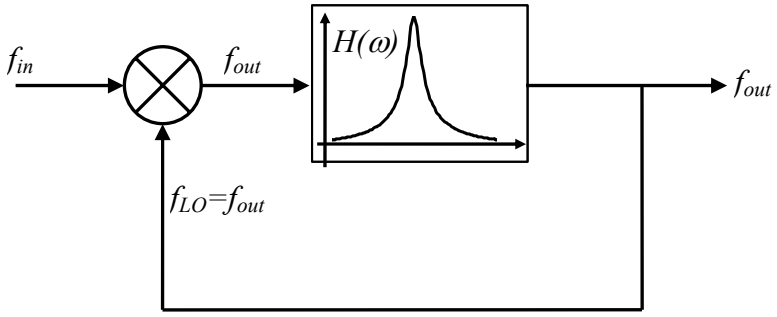


Figure 6-11 Simplified model of the injection-locked frequency divider

An LC oscillator based injection-locked frequency divider can be modeled as shown in Figure 6-11. From the basic mixer theory, $f_{out} = f_{in} - f_{LO} = f_{in} - f_{out}$, so that, $f_{out} = \frac{1}{2} f_{in}$, i.e. the input is divided by half. The bandpass filter is needed to reject all the undesired spurious outputs of the mixer. It should also be noted that by carefully controlling which harmonic is generated, higher divider ratio can be achieved. For instance, the mixer may generate the third or higher order inter-modulation product, i.e. $f_{out} = f_{in} - 3f_{LO} = f_{in} - 3f_{out}$, so that $f_{in} = 4f_{out}$. This way a divided-by-4 operation is accomplished.

The LC oscillator based ILFD was first proposed as that in Figure 6-12 and used in a 5-GHz frequency synthesizer [90], [91]. In this divider, the transistors, M_1 and M_2, serve as the mixer. The signal is injected to the mixer input node (sources of M_1 and M_2) from the tail current transistor. The LC tank serves as the bandpass filter. However, this topology is not suitable for high frequency operation because the sources of cross-coupled transistors and the drain of tail current transistor contribute relative large

capacitance (C_p in Figure 6-12). Thus, at high frequencies, most of the AC current flows to this capacitor instead of the oscillator core. From [95], a 50-GHz divider like this only achieves an 80-MHz input frequency range.

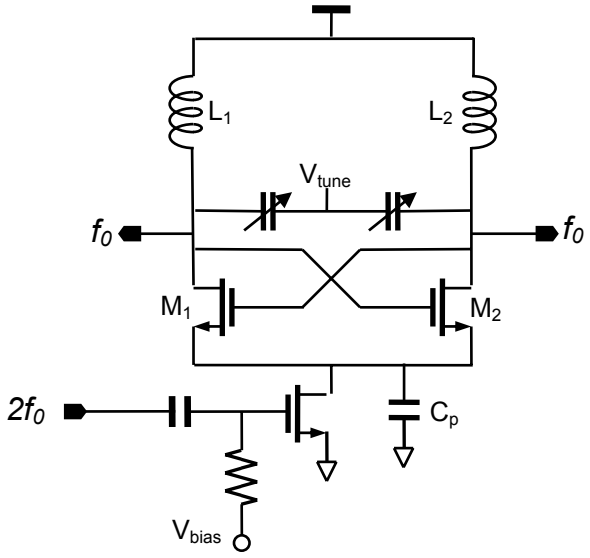


Figure 6-12 Schematic of the ILFD with signal injected from the tail current transistor

To obtain a wider frequency range, it should be better to inject the signal directly into the LC-tank. Figure 6-13 shows the topology of this kind of divider, where the signal is injected to the gate of M_3, which is connected to the VCO core. This input signal is summed with the oscillating outputs of injection-locked divider. The nonlinearities of M_1 and M_2 generate inter-modulation products which allow sustained oscillation at a fraction of the input frequency. The measured frequency range of a 55-GHz ILFD is about 3.3 GHz [96], which is more than 40 times of the one in [95].

Compared to D-flip-flop based static frequency dividers, the LC resonator based injection-locked frequency divider can operate at much higher frequencies. However, even using the topology in Figure 6-13, an ILFD still has a much narrower operating frequency range compared to static frequency dividers, whose range could be more than 80% of the maximum operating frequency. In order to further extend the locking range,

the ILFD is designed so that its tank resonant frequency tracks that of the VCO. As shown in Figure 6-14, MOS varactors are used to tune the ILFD's self-oscillation frequency. Its control voltage (V_{tune} in Figure 6-14) is tied to the VCO control voltage. Thus, the self-oscillation frequency of ILFD tracks that of the VCO [91]. The self-oscillation frequency of ILFD should be around half of the VCO frequency. If for some values of V_{tune}, the self-oscillation frequency of ILFD were too far away from the half of VCO frequency, then the VCO will fail to lock the ILFD and the loop will fail to lock.

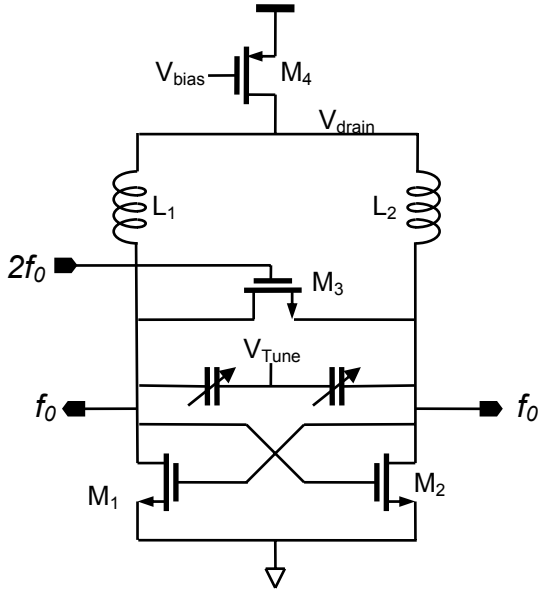


Figure 6-13 Schematic of the injection-locked frequency divider with the input signal directly injected to the core transistor

The output frequency of injection-locked divider is around 25 GHz. At this frequency range, a static frequency divider can be used. In addition to the much wider frequency range, it occupies a much smaller area. A 1/512 static frequency divider is built using the D-flip-flop architecture discussed in Section 3.2. It consists of 9 divide-by-2 stages. To have sufficient margins, the transistors widths in the first divided-by-2 stage are increased by 50% and it consumes about 40% more power than that described in Section 3.2.

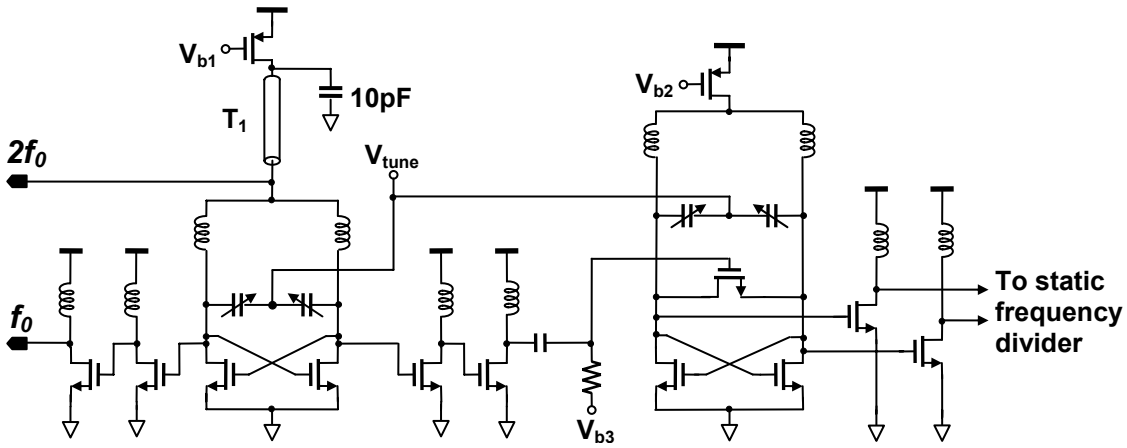


Figure 6-14 Schematic of the VCO and ILFD in the 50-GHz PLL

6.4 50-GHz Phase-Locked Loop

6.4.1 Loop Overview

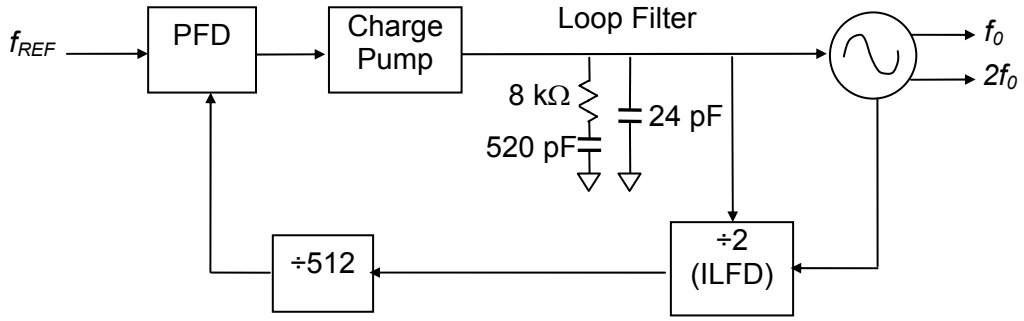


Figure 6-15 Block diagram of the 50-GHz phase-locked loop

Figure 6-15 shows the block diagram of a 50-GHz PLL. It includes a 50-GHz VCO, an ILFD, a 1/512 static frequency divider, a phase frequency detector (PFD), a charge pump (CP), and a low pass filter (LPF). The reference frequency for the PLL is between 45 and 49 MHz. To achieve even higher operating frequency, the 50-GHz VCO also provides a second harmonic around 100 GHz. The loop bandwidth is around 500 kHz. The resistor in the LPF is formed using non-silicided polysilicon and the capacitors are formed using MOS capacitors.

6.4.2 Measurement Results

The chip was fabricated in the UMC 0.13-μm logic CMOS process with eight metal layers. Figure 6-16 shows the micrograph of the chip. The chip size is 1.16 x 0.75 mm^2 including bond pads. The PLL was tested on-wafer and the output was measured using an Agilent E4448A 50-GHz spectrum analyzer. An Agilent E8254A signal generator is used to provide a -10-dBm sine-wave frequency reference signal around 50 MHz. The second order harmonic near 100 GHz is measured using an Agilent 11970W harmonic mixer.

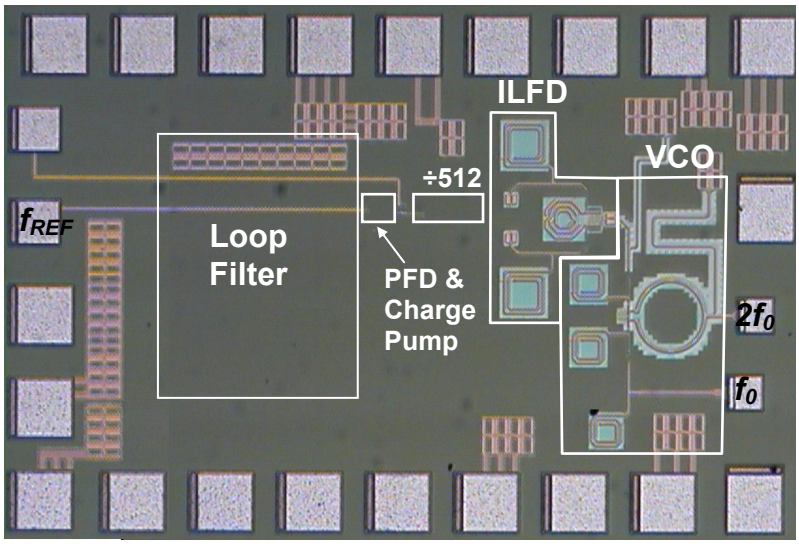


Figure 6-16 Micrograph of the 50-GHz PLL

The VCO is biased at 1.5-V V_{DD} and 12-mA bias current. Figure 6-17 shows the output frequency range of VCO. The VCO can be tuned over 4.75 GHz from 45.85 to 50.6 GHz. The output power level is about -10 dBm and phase noise of free running VCO is about -90 and -109 dBc/Hz at 1-MHz and 10-MHz offsets from the carrier, respectively.

The ILFD is measured at 1.5-V V_{DD} and 10-mA bias current. The self-oscillation frequency of ILFD varies from 23 to 25.1 GHz, which is slightly less than a half of the

tuning range of VCO. If the tank is not tuned, the measured input locking range of ILFD is 1.8 GHz when driven by the VCO on the same chip. By tuning the ILFD along with the VCO, the ILFD can be made to operate over the entire tuning range of VCO. Figure 6-17 also shows the minimum and maximum input frequencies to lock the ILFD. It should also be noted that the frequencies of VCO and ILFD are slightly affected by the bias current. The bias conditions mentioned above are chosen to maximize the input frequency range. The tuning range of ILFD should be increased to the half of VCO tuning range in future designs, in order to increase the margin. The static frequency divider is powered by a 1.5-V supply and all the buffers are powered using a 0.8-V supply.

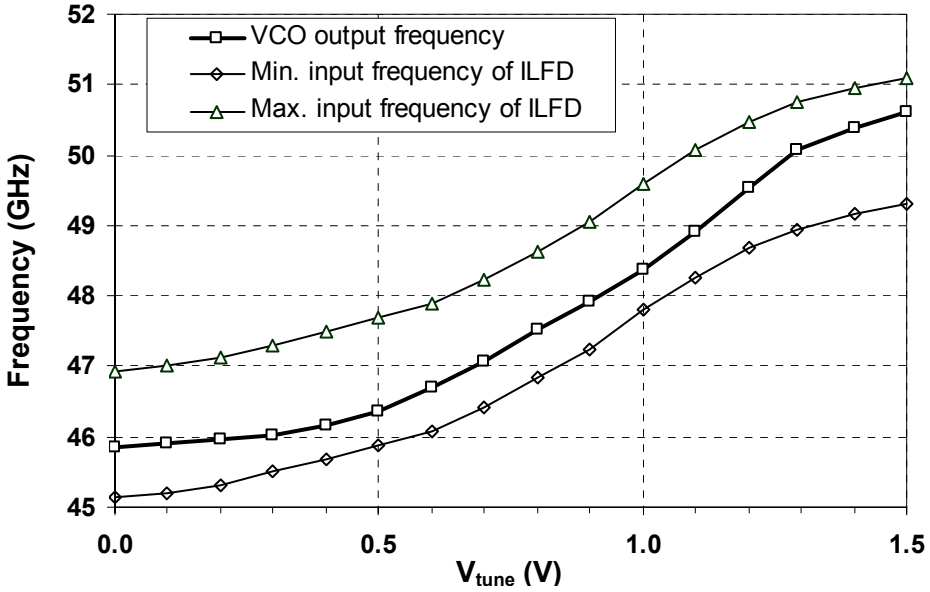


Figure 6-17 Frequency range of VCO and locking range of ILFD

The PLL can be locked from 45.9 to 50.5 GHz while consuming 57 mW from 1.5/0.8 V supply. The frequency range can be extended to 51 GHz, if the supply voltage for charge pump is increased. Figure 6-18 shows the measured output spectrum at 46.2 GHz, after the cable and probe losses are de-embedded. The loop bandwidth is around 500 kHz. Figure 6-19 shows the phase noise plot of the PLL from 2 kHz to 20 MHz. The

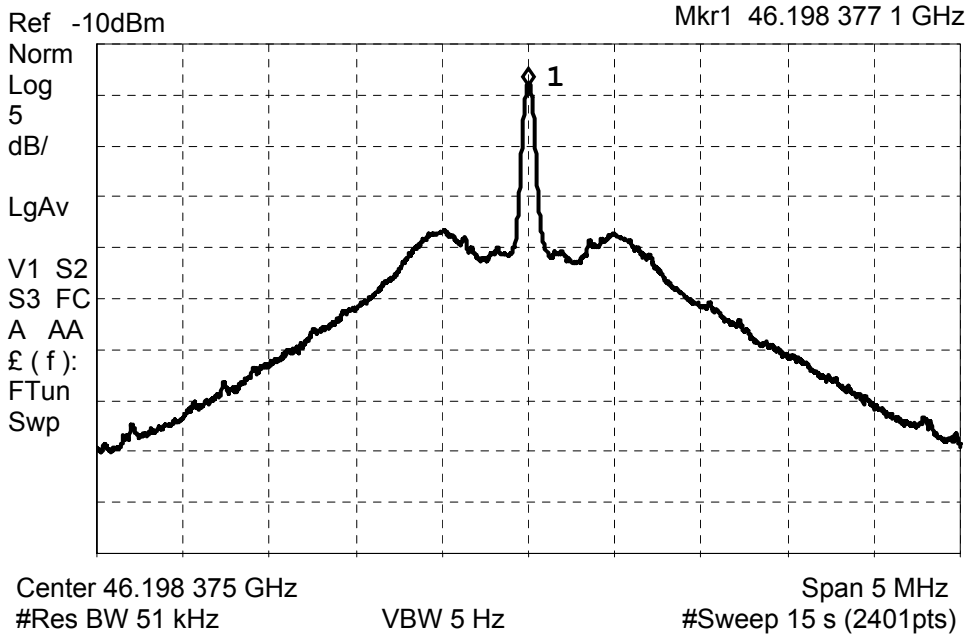


Figure 6-18 Close-in output spectrum of the PLL

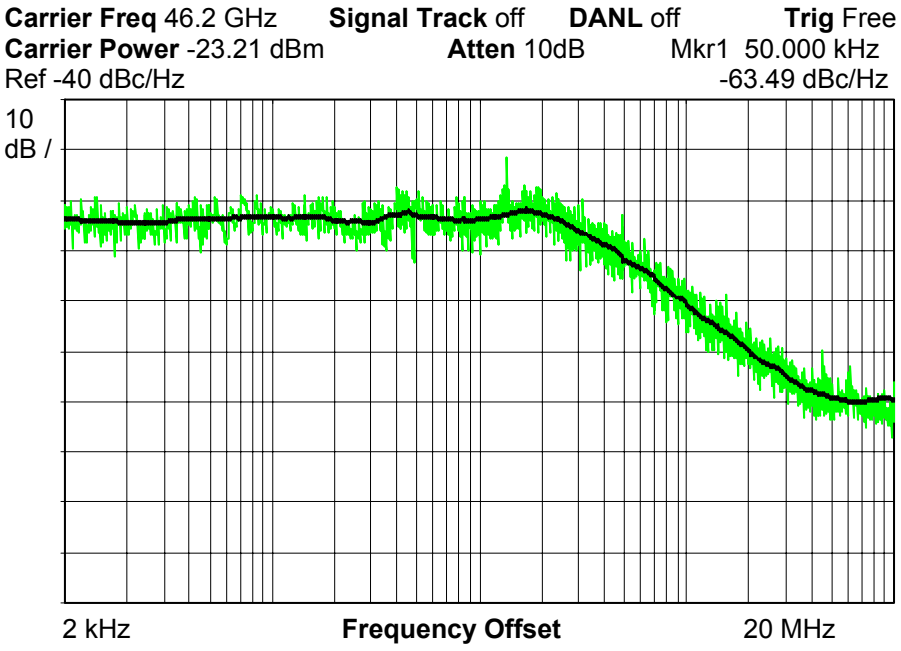


Figure 6-19 Phase noise plot of the PLL

phase noise at 50-kHz, 1-MHz and 10-MHz offset from the carrier is about -63.5, -72 and -99 dBc/Hz, respectively. The output spectrum with 200-MHz span is also shown in Figure 6-20. The spurs are about 40 dB below the carrier. At 50.5-GHz output frequency,

where the VCO gain is higher, the spurs become stronger and they are only about 27 dB below the carrier. Figure 6-17 shows the control voltage of VCO when the reference signal frequency is changed from 45 to 49 MHz, while the PLL output frequency is changed from 46 to 50 GHz. The measured settling time of PLL is about 40 μs.

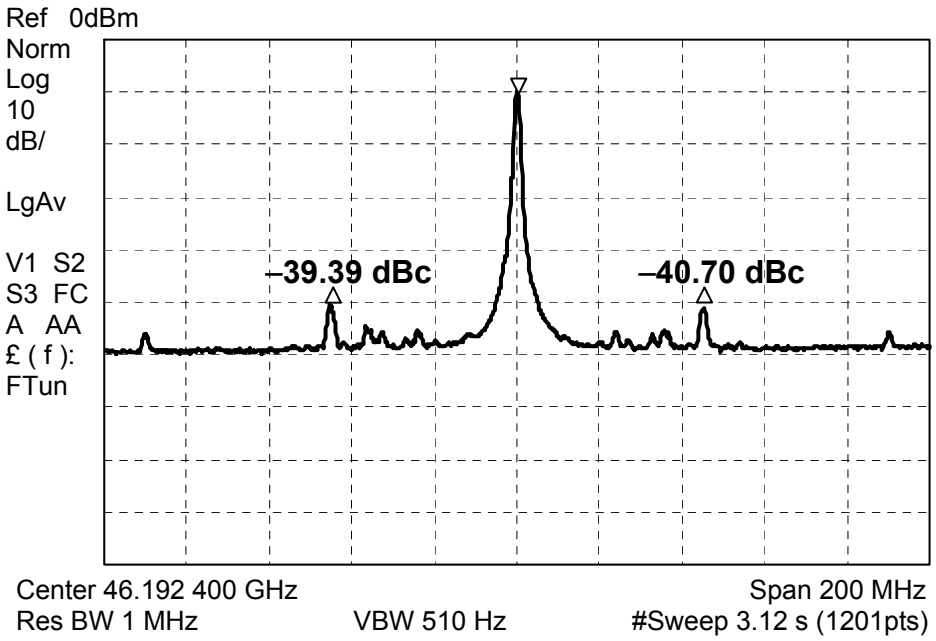


Figure 6-20 output spectrum of the PLL with 200-MHz span

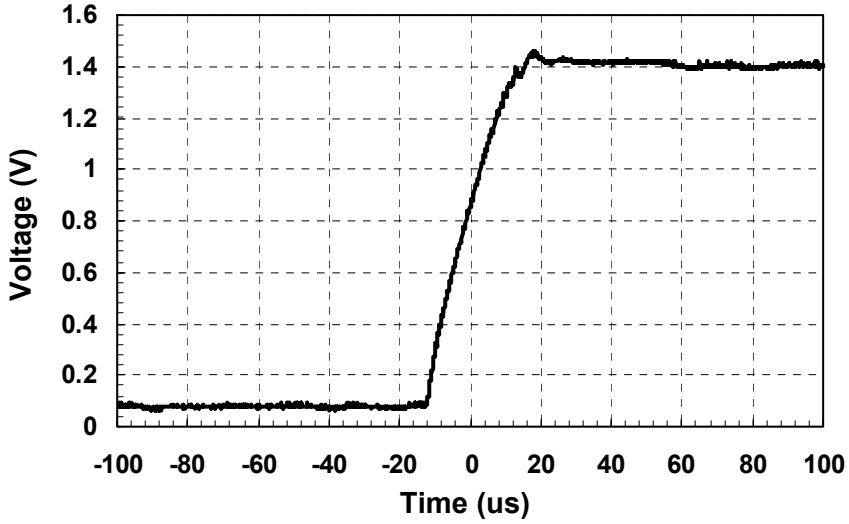


Figure 6-21 The PLL settling time is around 40 μs for a 4-MHz reference frequency step

The second order harmonic output frequency varies from 91.8 to 101 GHz. The measured output power is about -22 dBm at 101 GHz after all the losses in the measurement setup are de-embedded. Figure 6-22 shows the spectrum of push-push output at 101 GHz. The center frequency is exactly 2^{11} times of input reference frequency. The output power is about 5 dB lower at 92 GHz. This frequency dependence is probably due to the frequency response of transmission line matching network at the push-push node.

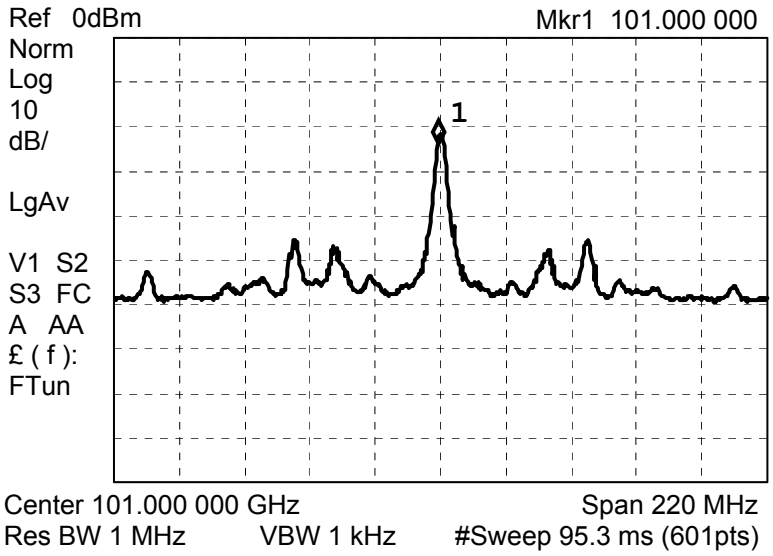


Figure 6-22 The output spectrum of push-push node at 101 GHz.

6.5 Summary

A 50-GHz phase-locked loop is demonstrated using the UMC 0.13- m CMOS. The operating frequency range of injection locked divider is extended by tracking the VCO output frequency. The loop can be locked from 45.9 to 50.5 GHz, and the power consumption is 57 mW. This PLL also outputs ~-22-dBm second order harmonic at frequencies between 91.8 and 101 GHz.

Table 6-2 compares the performance of this PLL with those of the previously reported SiGe PLL's using static frequency dividers, as well as that using an ILFD [89].

Table 6-1 Summary of the PLL Performance

Locked frequencies	45.9 – 50.5 GHz (fundamental) 91.8 – 101 GHz (second harmonic)
Phase noise	-63.5 dBc/Hz @ 50 kHz offset -72 dBc/Hz @ 1 MHz offset -99 dBc/Hz @ 10 MHz offset
Output Ppower	-10 dBm (fundamental) -27 to -22 dBm (second harmonic)
Settling time	< 40 μs
Spurs	-40 to -27 dBc
Supply voltage	1.5/0.8 V
Power dissipation	57 mW
VCO	12 mA x 1.5 V
ILFD	10 mA x 1.5 V
Static divider	8 mA x 1.5 V
PFD & CP	< 1 mW
Buffers	14 mA x 0.8 V
Die area	1.16 x 0.75 mm^2
Technology	UMC 0.13-μm logic CMOS

Table 6-2 Comparison to the previously reported SiGe HBT PLL's

	This work	[87][1]	[88]	[89]
Technology	0.13-μm CMOS	0.4-μm SiGe	0.25-μm SiGe	0.12-μm SiGe
Freq. [GHz]	45.9 – 50.5	36 – 45.5	54.5 – 57.8	51.4 – 54.5
P_{out} [dBm]	-10	-16 to -12	> 0	N/A
Power consumption	57 mW	650 mW	650 mW	N/A
Spurs [dBc]	-27 to -40	N/A	< -50	N/A
Settling time	40 μS	< 300 μS	N/A	N/A
50 kHz offset	-63.5	N/A	-58	-58
1MHz offset	-72	-79.5[1]	-72[2]	-80

[1] 20-GHz fundamental frequency, not all parts integrated on-chip, phase noise is for a free running VCO with a frequency doubler.

[2] 750 kHz offset from the carrier.

It achieves similar phase noise performance as the SiGe bipolar PLL's. The SiGe PLL's using static frequency dividers consume 650 mW [87], [88], which is more than ten times that of the CMOS PLL. The SiGe PLL using an ILFD [89] also consumes significantly lower power than those using static frequency dividers. Unfortunately, the accurate

power consumption number is not available for comparison. The maximum operating frequency of PLL proposed in this work is limited essentially by the maximum operating frequency of the oscillator that can be built. Given that a 192-GHz VCO can be built in the 0.13-μm CMOS, CMOS PLL's operating in 100's of GHz should be possible.

CHAPTER 7
SUMMARY AND FUTURE WORK

7.1 Summary

The ever increasing demand for low-cost portable devices has motivated the research on high frequency integrated CMOS communication circuits. This research work demonstrated a prototype of 24-GHz single chip radio for sensor network applications. The integration of an antenna on the same chip greatly simplifies the package, lowers the device cost, and makes the radio easy to use. Our work also has shown that it is possible to implement millimeter-wave applications with reasonable performance and power consumption using CMOS technology. These millimeter-wave integrated circuits can be used for high data rate communications, THz detection, and others.

The transmitter chain includes an MSK-like modulator, an IF amplifier, an up-conversion mixer, drivers and a power amplifier. A discrete approximation of the MSK using phase interpolation simplifies the modulator design and lowers the power consumption. A mode locking technique using positive feedback is also proposed to improve the efficiency of power amplifier. The transmitter chain implemented in the UMC 0.13-μm CMOS provides 8-dBm output power to a 50-Ω load and 7.7% rms EVM at 12-Mb/s data rate, while dissipating 100 mW power. The signal transmitted by the chip with an on-chip antenna was picked up 5 meters away using an on-chip antenna, and 95 meters away using a horn antenna. These demonstrations indicate that wireless communications over air using on-chip antennas is possible.

Frequency sources for future millimeter-wave applications are also studied in this dissertation. The transistors, varactors, and inductors are optimized to reduce the parasitic capacitances. The components were utilized to realize wide tuning range 60-GHz oscillators as well as VCO's operating around 140-GHz in the UMC 90-nm process. Push-push architecture is utilized to obtain an operation frequency of 192 GHz in the UMC 0.13-μm CMOS. This is the highest operating frequency for any silicon based circuits. With more advanced CMOS processes, it should be easy to extend the operation frequency into the sub-millimeter or THz range. A PLL tunable from 45.9 to 50.5 GHz is also implemented in the UMC 0.13-μm CMOS process. The power consumption is reduced to 57 mW by using an LC-oscillator based injection locked frequency divider (ILFD). These results indicate the feasibility of implementing millimeter-wave systems using low cost CMOS technology.

7.2 Suggested Future Work

A transmitter chain and millimeter wave circuits have been implemented in this work. The main challenge beyond this is improving the circuit performance to meet real system requirements. Suggested future work includes the following.

Evaluation of the improved transmitter chain and integrated transceiver. The biggest concern for the transmitter chain is the harmonic emissions are higher than F.C.C requirements. An improved transmitter chain with notch filters and better modulation scheme has been designed and submitted for fabrication. A frequency synthesizer is also integrated on the same chip. The VCO pulling issue due to the on-chip power amplifier also needs to be carefully investigated.

Improving operating frequency of millimeter-wave circuits and building oscillators in THz range. In this work, a fundamental mode oscillator around 140-GHz and a push-push oscillator close to 200-GHz have been successfully demonstrated. The frequency limit of the oscillators has been studied. With the continuous MOS transistor scaling, as well as improved design, it should possible to build oscillators at higher operating frequencies. For instance, it should be possible to build a fundamental oscillator above 200-GHz or a push-push VCO operating above 400-GHz using a 65-nm CMOS process. However, with device scaling, the contact/via area decreases and the resistance increases very fast. For instance, the typical contact resistances are 7 Ω, 15 Ω, and 45 Ω in 0.13-μm, 90-nm and 65-nm process, respectively. The higher contact resistance increases the gate resistance and lowers f_{max} of the transistor, thus limiting the maximum operating frequency of oscillators.

Improve the performance of the millimeter-wave frequency sources. Millimeter-wave oscillators and phase-locked loop have been successfully demonstrated in this work. However, the performance may not be acceptable in real applications. For instance, the output power of oscillators around 100-GHz is much lower than those implemented in III-V and SiGe bipolar processes. The phase noise of the oscillators and the phase-locked loop also should be improved.

APPENDIX A
DEFINITION OF ERROR VECTOR MAGNITUDE

Error vector magnitude (EVM) is often used to specify the modulation accuracy of transmitted signals in the presence of impairments. In the vector modulation, digital bits are transferred onto an RF carrier by varying the carrier's magnitude and phase such that, at each data clock transition, the carrier occupies any one of several specific locations on the I/Q plane. Each location encodes a specific data symbol, which consists of one or more data bits. The EVM is a measure of the difference between the ideal location and the measured results.

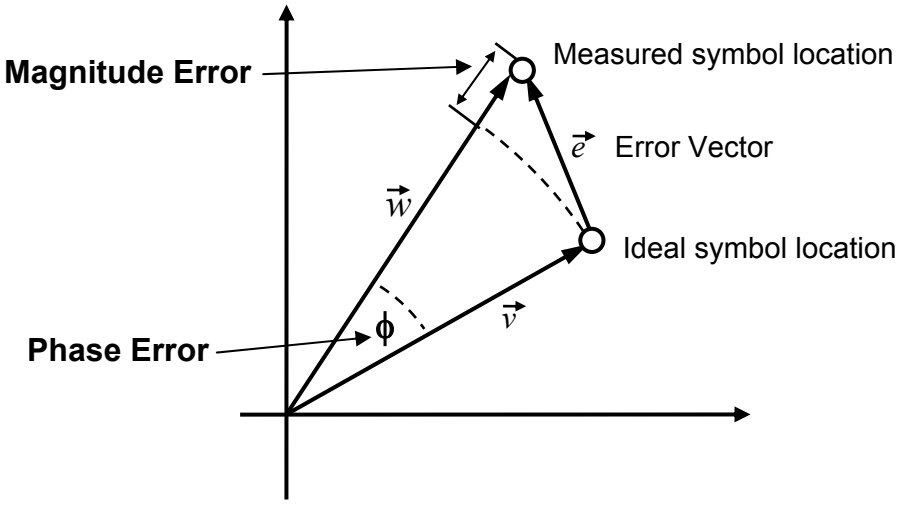


Figure A-1 Error vector magnitude and related quantities.

Figure A-1 shows EVM and several related terms. The rms EVM, rms magnitude error and average phase error are defined as

$$EVM = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left|\frac{\vec{e}_i}{\vec{v}_i}\right|^2} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left|\frac{\vec{w}_i - \vec{v}_i}{\vec{v}_i}\right|^2} \qquad \text{(A-1)}$$

$$Magnitude \quad Error = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\frac{|\vec{w}_i| - |\vec{v}_i|}{|\vec{v}_i|}\right)^2} \tag{A-2}$$

$$Phase \quad Error = \frac{1}{N}\sum_{i=1}^{N}\left|\angle\vec{w}_i - \angle\vec{v}_i\right| \tag{A-3}$$

Where, $\vec{w}_i$, $\vec{v}_i$, and $\vec{e}_i$ are the measured vector, ideal vector and error vector in the I/Q constellation plane. EVM is the scalar distance between the end points of actual and intended phasor. The error vector, $\vec{e}_i$, consists of anything that causes a displacement of the symbol from the intended state, thus it can also be treated like the noise. Since, SNR is the ratio of signal power and noise power, SNR can be approximated from EVM by

$$SNR = -20\log EVM \ . \tag{A-4}$$

APPENDIX B
DERIVATION OF UNITY POWER GAIN FREQUENCY

The unity power gain frequency, f_{max}, was first explicitly defined by P. R. Drouilhet in 1955 as a figure of merit of transistor [97]. Later, Thornton and Glasser [99]-[102] proved that "no such network, regardless how cleverly constructed, can have pure sinusoidal natural frequencies of oscillation above f_{max}" [100]. The computation of the unity power gain frequency, f_{max}, is generally difficult, so several simplifying assumptions are used to make an approximate derivation possible [29]. Figure B-1 shows the simplified transistor models using in the calculation of f_{max}.

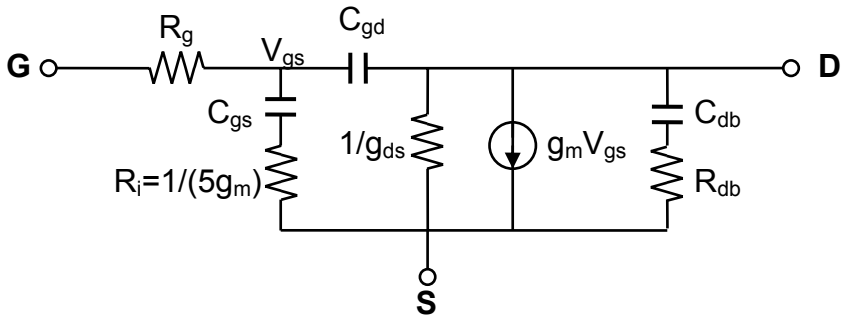


Figure B-1 Simplified transistor model

The power delivered to the input is

$$P_{in} = i_{in}^2\left(R_g + 1/(5g_m)\right), \tag{B-1}$$

where the current consumption of $1/g_{ds}$ through C_{gd} is not included. As, Eq. 5-2, the magnitude of short circuit current can be obtained by the same expression used for the computation of ω_T:

$$\left|\frac{i_d}{i_{in}}\right| \approx \frac{\omega_T}{\omega}. \tag{B-2}$$

The output impedance can be calculated by applying a voltage source (V_x) at the drain of the transistor, as shown in Figure B-2. Due the voltage divider network of C_{gd} and C_{gs}, the voltage across the gate-to-source is

$$V_{gs} = \frac{C_{gd}}{C_{gs} + C_{gd}} V_x . \tag{B-3}$$

Here the gate resistor and channel resistor are not included for simple expression. Therefore, the input current is

$$\begin{aligned} I_x &= g_m C_{gs} + g_{ds} V_x + \frac{V_x}{1/(j\omega C_{gs}) + 1/(j\omega C_{gd})} \\ &= \left(g_m \frac{C_{gd}}{C_{gs} + C_{gd}} + g_{gs} + \frac{1}{j\omega} \frac{C_{gs} C_{gd}}{(C_{gs} + C_{gd})} \right) V_x \end{aligned} . \tag{B-4}$$

It is straight forward to show that output impedance is

$$g_{out} = \frac{I_x}{V_x} = g_m \frac{C_{gd}}{C_{gs} + C_{gd}} + g_{gs} + \frac{1}{j\omega} \frac{C_{gs} C_{gd}}{(C_{gs} + C_{gd})} , \tag{B-5}$$

and its resistive part of output impedance is roughly

$$\mathrm{Re}(g_{out}) \approx g_m \bullet \frac{C_{gd}}{C_{gd} + C_{gs}} + g_{ds} = \omega_T C_{gd} + g_{ds} . \tag{B-6}$$

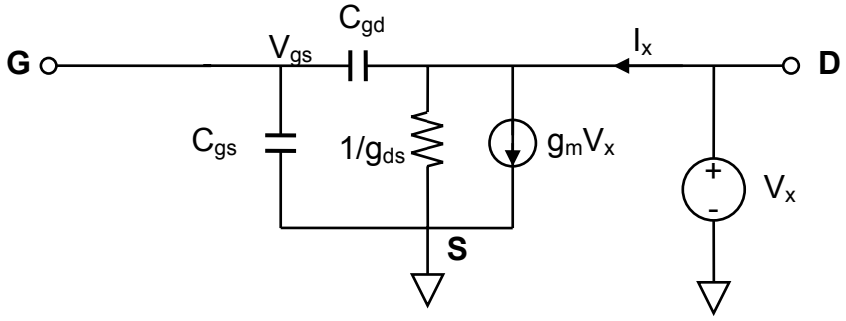


Figure B-2 Calculation of the output impedance of MOS transistor

Here, the effects of gate resistance and the series resistance of C_{db} are not included. In Figure B-3, if the conjugate termination has a conductance of this value then the power gain will be maximized, with half of the short circuit current going into the conductance of the termination. Thus, the maximum power delivered is

$$\frac{P_L}{P_{in}} = \frac{1}{4} i_d{}^2 \left(\frac{1}{\mathrm{Re}(g_{out})} \right) = \frac{1}{4} \left(\frac{\omega_T}{\omega} i_{in} \right)^2 \frac{1}{(\omega_T C_{gd} + g_{ds})}. \tag{B-7}$$

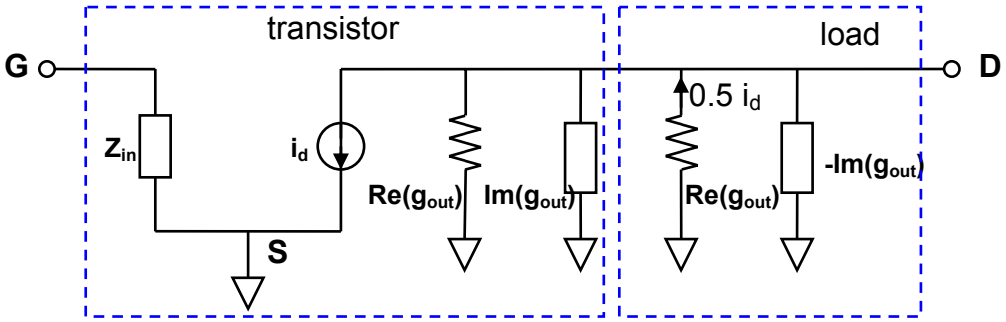


Figure B-3 Maximum power delivery using complex conjugate termination

Then, the maximum power gain is,

$$\frac{P_L}{P_{in}} = \frac{\frac{1}{4} i_d{}^2 \left(\frac{1}{\mathrm{Re}(g_{out})} \right)}{i_{in}^2 \left((R_g + 1/(5g_m)) \right)} = \frac{\frac{1}{4} \left(\frac{\omega_T}{\omega} i_{in} \right)^2 \frac{1}{(\omega_T C_{gd} + g_{ds})}}{i_{in}^2 \left((R_g + 1/(5g_m)) \right)} = \frac{\omega_T^2}{4\omega^2 \left((R_g + 1/(5g_m)) \right) (\omega_T C_{gd} + g_{ds})}. \tag{B-8}$$

This power gain has a value of unity at the frequency given by

$$\omega_{\max} = 2\pi f_{\max} = \frac{\omega_T}{2\sqrt{\left((R_g + 1/(5g_m)) \right) (g_{ds} + \omega_T C_{gd})}} \tag{B-9}$$

It is clear that ω_{max} depends on the gate resistance, so it is more comprehensive in this regard than ω_T. Because a good layout can reduce gate resistance to a small value, ω_{max} can be considerably larger than ω_T, especially in deep submicron CMOS processes. The

output capacitance C_{db} has no effect on ω_{max}, because its series resistor R_{db} is not included in our derivation, so that, C_{db} can be tuned out with a lossless inductance. If R_{db} is considered, the resistive part of the output impedance is

$$\begin{aligned} \mathrm{Re}(g_{out}) &\approx g_m \bullet \frac{C_{gd}}{C_{gd}+C_{gs}} + g_{ds} + \mathrm{Re}\left(\frac{1}{R_{db}+1/(j\omega C_{db})}\right) \\ &= \omega_T C_{gd} + g_{ds} + \frac{\omega^2 R_{db} C_{db}^2}{1+\left(\omega R_{db} C_{db}\right)^2} \end{aligned} \tag{B-10}$$

and the maximum power gain becomes smaller,

$$\frac{P_L}{P_{in}} = \frac{\omega_T^2}{4\omega^2\left((R_g+1/(5g_m)\right)\left(\omega_T C_{gd} + g_{ds} + \frac{\omega^2 R_{db} C_{db}^2}{1+(\omega R_{db} C_{db})^2}\right)} \tag{B-11}$$

As a consequence, the unity power gain frequency will be lower than Eq. B-9.

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