APPLICATIONS OF STRESS FROM BORON DOPING AND OTHER CHALLENGES IN SILICON TECHNOLOGY

By

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This document is dedicated to my mom, dad, and brother Aaron.

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Semiconductor device performance has been improving at a dramatic rate due to scaling to nanometer dimensions. Strain engineering of the substrate has also proven to increase drive currents in MOSFETS and other advanced devices. An active area of research and development is focused on intentionally straining the channel of MOSFETS to enhance mobility. However, increased scaling can also magnify the mechanical forces that arise during IC fabrication.

Multiple material layers with differing thermal expansion coefficients and deposited stress levels become closer in proximity to one another and to the device channel. Shallow trench isolation (STI) can create large stresses due to thermal mismatch, oxide growth, and trench fill, and the sharp corners at the top and bottom of the trenches are major contributors to the stress behavior. Stress will influence dopant and defect behavior in unexpected ways. It has been predicted that the proper stress can double the solubility of dopants such as boron in silicon. Thus, accurate process models

need to be developed to incorporate both the intentional and unintentional stress sources in order to maximize device performance. This work focuses on the unintentional stress source from dopant incorporation.

The model that FLorida Object Oriented Device and Process Simulator (FLOOPS) currently utilizes to compute stress and strain was developed for LOCOS processes, which are largely no longer employed. In addition, these computations are decoupled from the solution of the diffusion equations. Most of the materials used in silicon processing can be modeled as simple elastic materials, which makes process modeling easier. New models must be developed to more accurately calculate the stresses in the silicon substrate.

To achieve this goal, new software operators were developed in FLOOPS to calculate the displacements and stresses in the silicon substrate due to boron doping. This elastic stress solver was integrated into the Alagator scripting language, and the simulation results provide a more accurate description of the stress evolution. Part of the future work is to enable the elastic stress solver to be coupled to defect and dopant evolution.

CHAPTER 1
INTRODUCTION

Strain engineering has become a key component of emerging technologies, however due to the great complexity and cost in IC fabrication, it is difficult to physically develop new processes. Technology Computer Aided Design (TCAD) tools are invaluable for shortening new technology development and for optimizing existing processes [Cea96]. Front-end process modeling of stress effects from oxidation, thermal mismatch, and intrinsic stress have been demonstrated over the last 15 years, beginning with 2D and 3D modeling of oxide growth for viscous and viscoelastic materials [Cea96]. Recently stress simulations for strained silicon have been performed to understand the effects of strain on device mobility and drive current enhancements, and threshold voltage shifts [Lim04, Tho04a, Tho04c, Uch04].

While applying the proper strain has clearly demonstrated enhancements in transistor performance, the effects of mechanical stress can also degrade device characteristics. In the front-end process, shallow trench isolation (STI) is a major source of stress in the MOSFET channel. The proximity and amount of the stress in the silicon substrate limits the density of ICs, and when the too much stress is exerted in the silicon, it will yield by releasing dislocations that lead to leakage currents and degraded device performance. Thus, having an in depth understanding of how stress affects the semiconductor fabrication processes is critical.

As we enter the nanometer regime, stress from standard process steps such as source/drain doping introduce significant stress in the channel of MOSFETs. In PMOS

devices, the tensile stress generated in the channel from source/drain boron doping is nearing values large enough to compensate the engineered strain engineered intended for performance enhancement.

This focus of this chapter is to provide a survey of the existing literature on stress applications in silicon technology. Section 1.1 provides a brief history of the transistor and discusses scaling trends over the past 50 years. Section 1.2 presents work that explored the effects of stress on defect evolution and regrowth velocities in patterned structures. Section 1.3 discusses mechanically induced channel stress from shallow trench isolation structures (STI). Section 1.4 introduces strained silicon and demonstrates various methods of applying stress to enhance device performance. Section 1.5 will provide a brief summary of each chapter of the thesis.

1.1 Motivation

The semiconductor industry is on an eternal hunt for methods to continue Moore's Law. Since the invention of the transistor in 1947 by William Shockley, John Bardeen, and Walter Brattain, and the fabrication of the first Metal Oxide Semiconductor Field Effect Transistor (MOSFET) at Bell Labs in 1960, much innovation in the forms of transistor scaling and new materials has led to the recent MOSFET [Tho04a,Tho05]. In 1965, Gordon Moore proposed that the number of transistors on an integrated circuit (IC) will approximately double every 2 years [Moo65]. Since then, much work in the area of transistor scaling has been accomplished. The goal of technology scaling is to create faster, denser, low power circuits per chip for the same amount of money. For long channel devices, dimensions and supply voltages scaled by the same factor in order to maintain a constant electric field. The next trend in scaling was to maintain a fixed supply voltage and scale only device dimensions. Modern short channel devices scale both the

supply voltage and device dimensions by different factors. Moore's prediction has held over the last 4 decades and will continue as long as the price of a transistor continues to drop in price [Tho04a]. The scaling of minimum feature size over the years and the evolution of the transistor is illustrated in Figures 1-1 and 1-2.

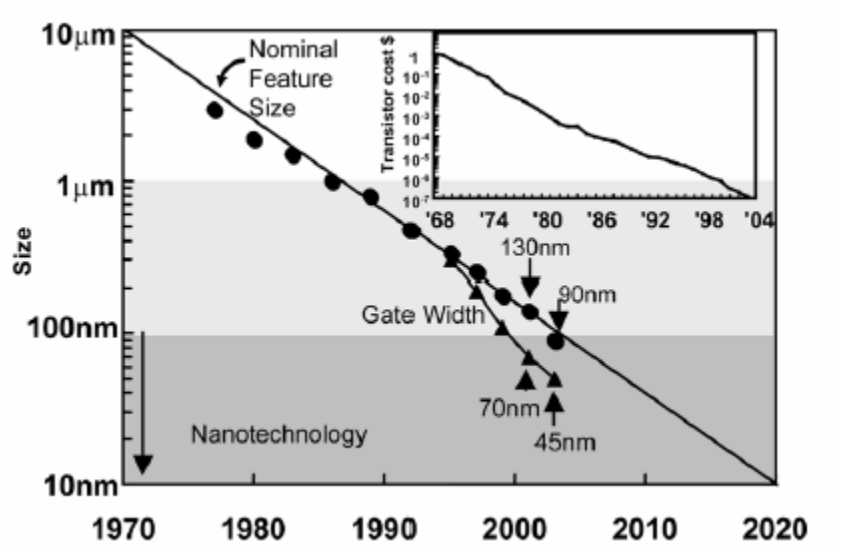

Figure 1-1: Evolution of transistor minimum feature size and transistor cost vs. year [Tho04a]

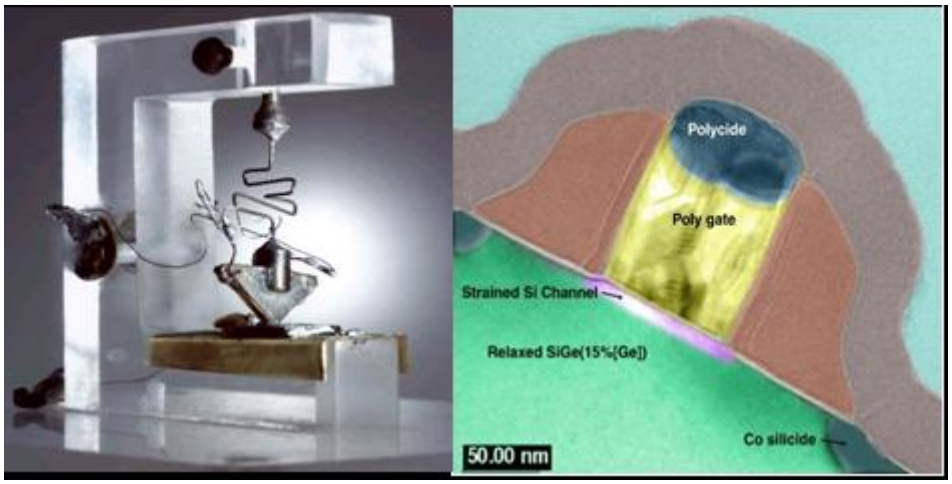

Figure 1-2: Evolution of the MOSFET from 1947 to 2002 [Pbs47].

1.2 Stress Induced Defects in Patterned Structures

Thin films such as silicon nitride, silicon dioxide, and polysilicon are frequently encountered in device fabrication; these films contain intrinsic stresses as a result of the deposition process. Continuous films deposited over the entire silicon substrate produce low levels of stress in the silicon because the substrate is generally a few orders of magnitude thicker than the film. Large stresses occur when films are not planar or have discontinuities, and silicon substrate yields by forming dislocations.

In MOSFET fabrication, high dose ion-implantation is used to accurately dope the source/drain regions to desired junction depths. The implanted region becomes amorphized and upon subsequent annealing dislocations form at the original amorphous-crystalline interface. Dislocations have been known to affect dopant redistribution during thermal cycling by capturing and emitting point defects, leading to variations in junction depths. Calculations of the stress around a dislocation loop with observed density and size shows that the pressure around the loop layer can locally be on the order of 10^9 dyne/cm^2. This value is comparable to stresses induced from patterned nitride films and isolation structures [Par95]. Thus, the control and understanding of dislocation loops formation is critical.

The effect of multiple nitride stripes on stress and dislocation loop formation was investigated by Chaudhry. His work demonstrated that the stress in the silicon substrate is a strong function of the nitride stripe thickness and width. Narrow stripes resulted in higher levels of stress than significantly wider stripes. Large shear stresses developed at the nitride/silicon interface which can lead to slip in silicon. Hu reported the critical shear stress slip in silicon to be $3x10^7$ dyne/cm^2. These dislocations lie on the {111} plane and glide in the [110] direction [Fah92]. Dislocations in regions of shear stress

higher than this value will glide. Placing the nitride stripes in closer proximity offset the shear stress components. The tensile component of one strip offset the compressive component of the adjacent strip [Cha96].

Ross demonstrated the effect of stress on defect formation at the mask edge of patterned structures and on the regrowth velocity [Ros03, Ros04]. Line and square structures were formed by depositing 80Å of SiO_2 and 1540Å of nitride on silicon. An amorphizing silicon implant with a dose of $1x10^{15}$ atoms/cm^2 at 40keV was performed after patterning the wafer, and samples were anneals between 550°C and 750°C. Cross-sectional Transmission Electron Microscopy (XTEM) samples were prepared at different stages of the solid-phase epitaxial regrowth process to observe the formation of half-loop dislocations at the mask edge. The defects only occurred around the line edges and not the square edges. When the square structures were etched and re-annealed, defects formed around the mask edge. Dislocation loops migrate to regions of tension to relieve stress, and FLOOPS simulations confirmed a tensile pocket at the nitride/silicon interface where the defects formed. It was concluded that the stress from the nitride square structure suppressed the defect formation.

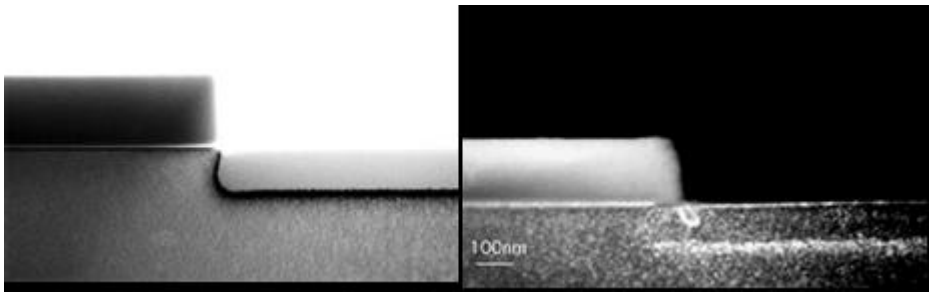

Figure 1-3: Dislocation formation at the edge of a nitride strip after solid-phase epitaxial regrowth (left) before annealing and (right) after annealing.

Low defects densities are required in the areas where devices are fabricated on wafers because they lead to leakage current and performance degradation. In a study performed by Phen [Phe04], a wafer bending study was performed in which the patterned wafers aforementioned were bent to a stress of 86 MPa of tension and annealed at 750°C for five minutes. Transmission electron microscopy micrographs confirmed that the tensile mechanically-induced stress removed defects from the samples. This is further proof that suggests stress affects defect formation and is worthwhile investigating.

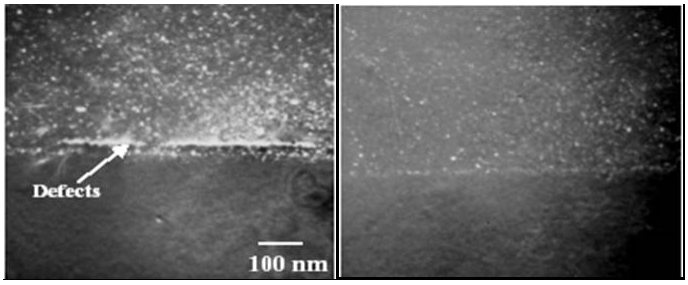

Figure 1-4: Application of stress to patterned wafers prevented line defects from forming [Phe04].

Isolation structures such as deep and shallow trench isolation are also known to generate dislocations. After the formation of isolation structures, residual stresses are present in the silicon and trench area; however they are not significant enough to generate dislocations. These stresses will be addressed in Chapter III. After processing steps such as ion implantation, point defects are introduced into the silicon and can serve as nuclei for dislocation formation. Once the dislocations form, the stress in the silicon from the trench formation can cause the dislocations to glide. The energy for dislocation glide is much less than the energy for dislocation formation, thus the glide process can even occur in materials with moderate stress [Fah92].

Fahey et al. observed the formation of dislocations in a deep trench isolation structure filled with poly for a bipolar process. A phosphorus implant was performed to

make contact with the deep subcollector. After annealing to activate the dopant, defects formed near the corners of the structure. The defects did not form in similar patterned structures that did not receive the implant. In addition, no defects formed in unpatterned wafers that received identical implantation implants and anneals. This phenomenon was further investigated for a DRAM trench capacitor process, in which a deep trench filled with poly, is fabricated next to a PMOS device. The source and drain are doped with boron, and after the annealing step, gliding dislocations formed next to the trench on the {111} plane and glided in the [110] direction towards the PMOS transistor. Again, the defects did not form in identical structures with no implantation. This study concluded that the ion implantation can reduce the stress in silicon because it provides nuclei for dislocations, and the dislocations glide due to the stress from forming the isolation structures. However, if the dislocations glide out of the implanted area, they could become deleterious to device performance [Fah92].

1.3 Mechanically Induced Channel Stress from Shallow Trench Isolation (STI)

Experimental data and simulations show that while the stress introduced by the STI formation enhances PMOS drive current, it also demonstrates sensitivity to layout for NMOS transistors [Jeo03, Gal04, Sco99, She05]. The STI process introduces a compressive stress in the channel direction, which enhances hole mobility. The physics behind this improvement in carrier mobility are discussed in Section 1.4. Scott et al. observed a mobility reduction in NMOS devices due to stress from isolation trenches. The proximity of the gate to the trench edge and the active area were critical factors that made NMOS devices sensitive to layout. Linear current was reduced by as much as 13% for diffusion lengths less than 2 um, and the extracted mobilities agreed with piezoresistance calculations [Sco99]. Current reduction was also observed as the width

of the NMOS devices were decreased from 20 um to 0.5 um, where PMOS devices were relatively insensitive to the width variation. Jeon et al. investigated the effects of mechanical stress from STI formation on silicon-on-insulator wafers for a silicon thickness of 50 nm and 90 nm. For the 50 nm wafers, he observed a 13.5% current degradation in NMOS and a 23% current increase in PMOS current as the gate-edge-to-STI distances were decreased from 2.69 um to 0.26 um [Jeo03]. Thus, it is critical to compute the stresses throughout the IC fabrication process, and use those values as parameters to for future technology development.

Gallon et al. performed wafer bending experiments to investigate the effect of STI mechanical stress on 0.13 um bulk and SOI transistors. For both bulk and SOI devices, an increase in PMOS and reduction in NMOS current was observed as the gate-to-STI distance was decreased from 10 um to 0.34 um, which was in accordance with the findings of both Scott and Jeon. For small stresses ranging from |0-130| MPa, a linear change in mobility enhancement/reduction was observed for NMOS and PMOS bulk devices.

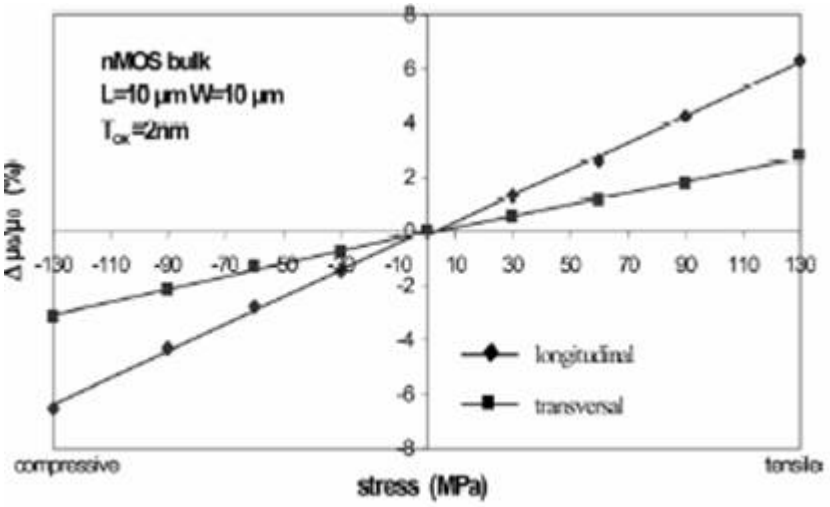

Figure 1-5: Linear variation of mobility enhancement for a bulk NMOS transistors [Gal04].

Lower values of stress were applied because silicon yields for a mechanical stress between 175-220 MPa. The modeling of silicon in the plastic regime will be addressed in the future work Chapter IV. For both NMOS and PMOS devices, higher stresses were observed in SOI vs. bulk transistors. This is because the silicon can reoxidize at the buried-oxide/silicon interface at the STI edge, and the bending of the silicon adds to the compressive stress in the channel from the STI formation [Gal04].

Gallon et al proposed that the enhanced performance for SOI PMOS and decreased performance for NMOS devices is a result of the implantation, amorphization, recrystallization process rather than from bandgap effects and reduction in conductivity effective masses. Amorphous silicon relaxes by viscous flow under compressive stress with a temperature dependence, which is driven by a decrease in concentration of defects [Wit93]. When fabricating NMOS transistors, an arsenic implant of $2x10^{15}/cm^2$ created an amorphous layer approximately 50 nm below the surface. Simulations demonstrated that due to the compressive stress from the STI, the amorphous layer was able to relax, causing a reduction of internal stress from -1650 GPa to -750 MPa [Gal04]. The boron implant for PMOS transistors however was non-amorphizing, and no initial stress relaxation occurred. Bulk devices on the contrary did not show significant relaxation after recrystallization because the stress from the STI formation is not large enough to relax the amorphous layer (~400 MPa). As a result, bulk NMOS and PMOS transistors retain their initial stress levels.

Strain relaxation of a SiGe layer upon regrowth was also observed by Crosby [Cro04]. Fifty nm of strained silicon was grown on top of a graded SiGe buffer layer up to 30% germanium incorporation. High Resolution X-ray Rocking Curves confirmed

that the strain varied from 0-2.4% throughout the structure. Low energy implants of 12 keV, creating at 30 nm amorphous layer, and high energy implants of 60 keV, creating a 100 nm amorphous layer were implanted with $1x10^{15}/cm^2$ Si^+ into the SiGe structure. Both structures were annealed at 600°C and 675°C for up to 30 minutes. Similar to and STI structure, SiGe creates a compressive stress due to the increased lattice constant of germanium compared to silicon. For germanium contents exceeding a critical thickness, the strained silicon layer will relax by emitting misfit dislocations at the Si/SiGe interface. This will be described in more detail in Section 1.4. The strain relaxation occurred in the structures for both implant conditions, but did not occur in unimplanted samples. These finding further support the work of Gallon et al. suggesting that compressive stress causes stress relaxation after amorphous regrowth.

Cowern et al. developed an Arrhenius relationship for dopant diffusion in a biaxially strained SiGe layer to be [Cow94]:

$$D_S = D_I \exp[\frac{-sQ'}{kT}] \qquad (1\text{-}1)$$

where D_S is the dopant diffusivity under strain, D_I is the dopant diffusivity without strain, s is the biaxial strain in the plane of the SiGe layer, and Q' is the activation energy per strain. Similar to this relationship, Sheu et al. developed a sophisticated stress-dependent dopant diffusivity model to calculate the mechanical stress from STI formation. The model was calibrated to account for implant damage, dopant-point defect pairing diffusion, silicon-oxide dopant segregation, oxidation-enhanced diffusion models, dopant clustering models, dopant-defect clustering models, and intrinsic diffusion models. The relationship for dopant diffusivity due to STI mechanical stress is [She05]:

$$D_S(T,x,y) = D_I(T)\exp[-\frac{\Delta E_S \varepsilon_t(T,x,y)}{kT}] \quad (1\text{-}2)$$

where D_S is the dopant diffusivity under strain, D_I is the dopant diffusivity without strain, and ΔE_S is the activation energy per volume change ratio (V_{CR}) depending on dopant species and temperature (T). The V_{CR} is the volume change ratio due to stress, and for small applied stresses, the V_{CR} can be approximated as [She05]:

$$V_{CR}(T,x,y) \cong \varepsilon_t(T,x,y) \equiv \varepsilon_{xx}(T,x,y) + \varepsilon_{yy}(T,x,y) + \varepsilon_{zz} \quad (1\text{-}3)$$

where ε_{xx} is the strain in the direction of the channel, ε_{yy} is the strain perpendicular to the channel, and ε_{zz} is the strain in the channel width direction. For simulations, a wide width was chosen, so ε_{zz} is zero. Stress simulations involved the STI and other main process steps, and the model was tested for MOSFETS with varying gate and active lengths. Unsurprisingly, the compressive stress in the channel direction increased as the active area decreased. Tensile stress was also observed in the bulk direction with magnitudes significantly less than in the channel direction. For active areas = 0.6 um, the stress and strain magnitudes were simulated to be $-5\text{x}10^9$ dyne/cm^2 and -0.4% respectively, which is equated to the strain from incorporating 10% germanium in silicon [Cow94, Gal04]. It was concluded that the dopant distributions were properly computed in the operating region of the device because device simulations matched subthreshold NMOS I-V experimental data curves. Boron, a known interstitial diffuser, exhibited retarded diffusion as a result of the compressive STI stress.

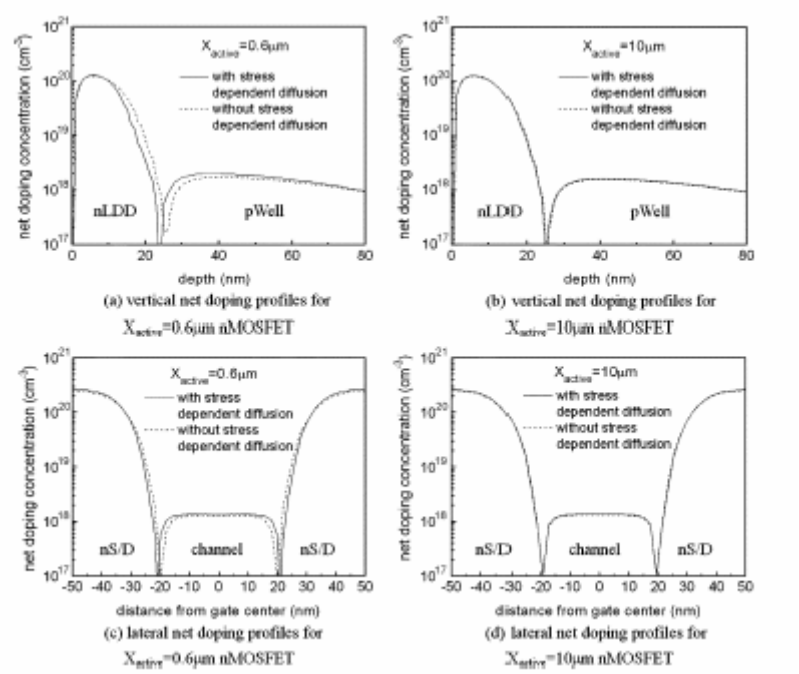

Figure 1-6: Dopant profiles, vertical profiles are taken at the gate edge and lateral profiles are taken 15 nm below the device surface [She05].

Threshold voltage increased with decreasing NMOS active areas, while PMOS exhibited negligible voltage shift to the decreasing active area, which was also verified by experimental data. This will be further explored in Section 1.4.

1.4 Strained Silicon

Two main factors that control the switching speed of an ideal transistor are the channel length and the speed at which carriers move through the semiconductor material. In this section, the speed of the carrier through the semiconductor material is discussed, and is described by the strained silicon concept. Strained silicon can be applied biaxially or uniaxially to improve the drive currents in MOSFETs and other advanced devices through mobility enhancements. An important and promising feature of strained silicon for future technology nodes is that it increases device performance without decreasing the channel length or increasing the off-state leakage current. This is done by increasing the

carrier mobility through the channel by reducing the conductivity effective mass, and/or scattering rate [Moh04].

1.4.1 Strained Silicon Physics

Carrier mobility (μ) in semiconductors can be expressed as a linear relationship between the velocity (v) and the external electric field (E) [Cro04]:

$$v = \mu \cdot E \tag{1-1}$$

The mobility is also function of transport scattering time (τ) and effective mass (m^*):

$$\mu = \frac{e}{m^*} \cdot \tau \tag{1-2}$$

where e is the electron charge. Both effective mass and scattering reductions have demonstrated mobility enhancements for electrons, while only effective mass reduction is necessary for hole mobility enhancement. This is because the valence band splits less than the conduction band under strain [Moh04].

For electron transport, the conduction band of silicon is sixfold degenerate. When strain is applied, the degeneracy is lifted and lowest energy level of the band is split. Two states drop to a lower energy level and the remaining four states occupy a higher energy level. As a result of the band splitting, electron scattering is reduced, and the average velocity in the conduction direction increases. The combination of increasing the average distance an electron travels before it is knocked off course, and reducing the effective mass results in electron mobility enhancements [Lim04, Tho04a, Tho05, Tho04c]

Hole mobility transport is more complex. The valence band consists of three bands that are all centered at the gamma point, and from lowest to highest energies are the heavy-hole, light-hole, and spin-orbit bands. When strain is applied, the degeneracy is

lifted between the light and heavy hole bands, and holes fill the “light hole”-like band, thus reducing the effective mass and increasing hole mobility [Moh04]. Under no strain, the bands have mirror symmetry about the k=0 point. Applying a uniaxial or biaxial strain in the [110] direction results in severe band warping. For biaxial tensile strain, the warping remains symmetrical; meaning that the electrons repopulate the lowest energy levels equally. However for uniaxial strain, the warpage is no longer mirror symmetrical and the holes will still repopulate the lowest energy states first. The breaking of the symmetry is caused by a shear stress component that does not affect the conduction band and is not present for biaxial stress [Gha04].

A key advantage to uniaxial compressive strain for PMOS devices is that the hole mobility enhancements do not degrade at high vertical fields. This is because the large out-of-plane mass causes further band splitting with confinement in the inversion layer of a MOSFET [Fis03]. On the contrary, biaxial stress does not maintain the hole mobility enhancements at higher vertical fields because unlike uniaxial stress, at high fields the bands splitting reduces because of the lighter out-of-plane mass. At approximately 1 MV/cm, the mobility decreases to that of the universal hole mobility, and all gains from straining are lost [Gha05, Tho04a, Tho05, Tho04c]. The mobility vs. effective field data for biaxial and different applications of uniaxial stress are shown below. Note that only the uniaxial stress applied by silicon germanium in the source/drain region resulted in mobility enhancements at high vertical fields.

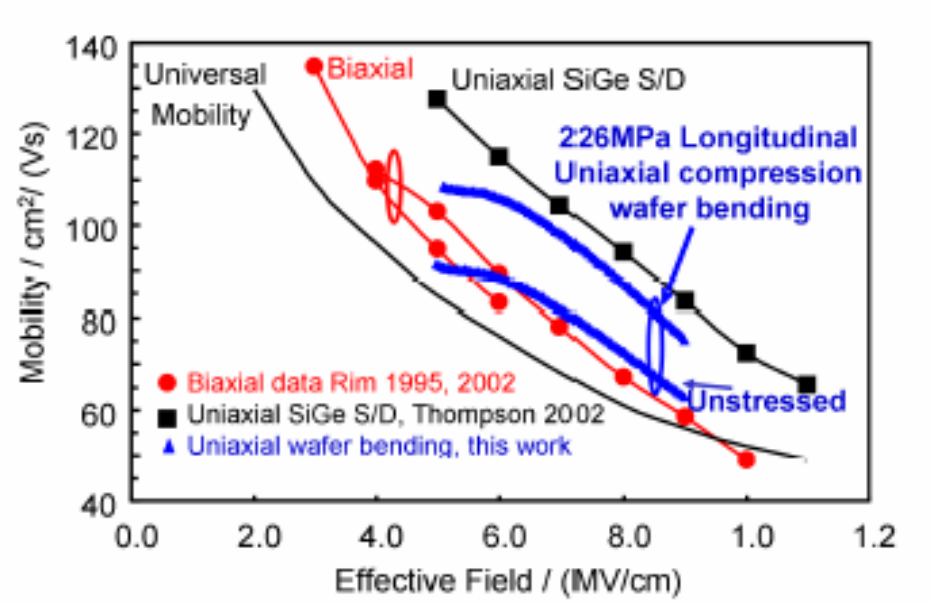

Figure 1-7: Strained silicon hole mobility enhancement vs. vertical electric field (wafer bending, SiGe S/D, biaxial substrate stress [Tho04c].

1.4.1.1 Biaxially Strained MOSFETS

Applying stress in the channel region of a device allows for higher carrier mobility. Tensile strain increases the interatomic distances in the silicon crystal, thus increasing the mobility of electrons. The same effect is observed with holes and compressive strain. Although this method of introducing strain enhances both hole and electron mobility, a large mobility loss is evident at high vertical fields [Tho05].

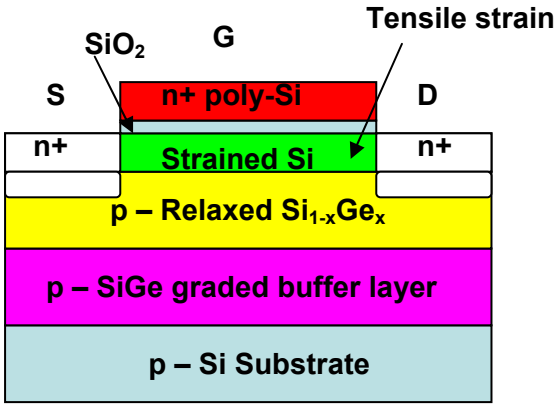

Figure 1-8: Formation of biaxially strained NMOS transistor

Biaxial strain occurs in both the x and y directions of the deposited silicon layer. The formation of biaxially strained NMOS transistors begins with a silicon wafer and a grown SiGe graded buffer layer. The buffer layer is formed by linearly increasing the Ge content as the layer thickness is increased. As the Ge content becomes larger, relaxation occurs in the layer by generating misfit dislocations. When a lattice constant approximately 1% greater than that of silicon is formed, a relaxed $Si_{1-x}Ge_x$ is grown on top of the graded layer to set the lattice constant of the material [Tho04a]. Finally, a defect-free thin silicon layer is grown on top of the relaxed structure and the layer remains strained as long as the thickness is below a critical value [Cro04, Peo85]. The critical thickness decreases as the lattice mismatch (% Ge) increases. This is illustrated in Figure 1-9 below.

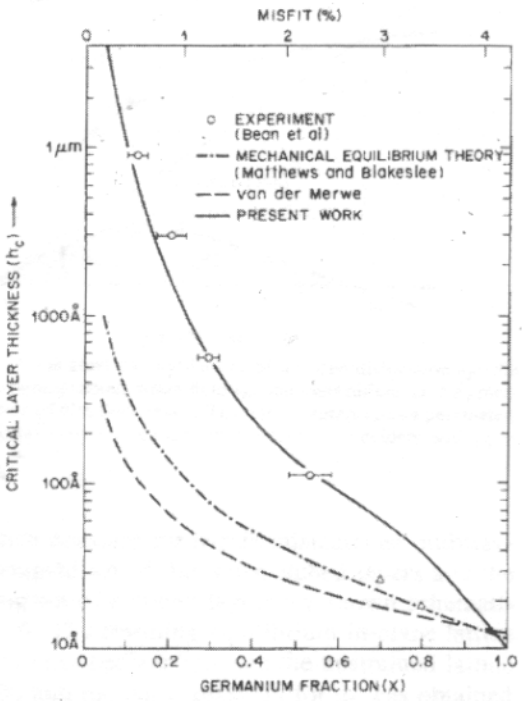

Figure 1-9: Critical thickness as a function of Ge composition for SiGe on Si [Peo85].

Fiorenza et al. studied strained silicon MOSFETS with silicon thicknesses below and above the critical thickness value to understand the effects of exceeding the critical

thickness on device performance [Fio04]. Although increasing the strained silicon thickness far beyond its critical value had little effect on mobility loss, a significant off-state leakage current was observed, which is deleterious to device performance. The leakage current was attributed to misfit dislocations that form at the silicon/SiGe interface and can cross between the MOSFET source and drain. The increased leakage was only observed when transistor gate lengths were less than the diffusion lengths.

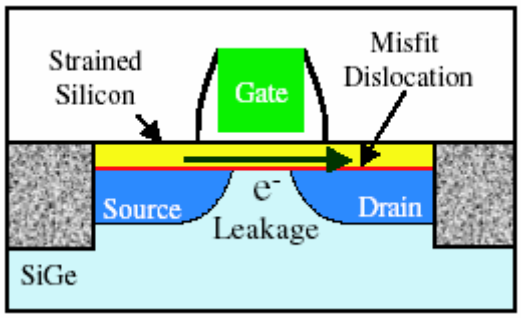

Figure 1-10: Drain current leakage mechanism in strained silicon films with misfit dislocations [Fio04].

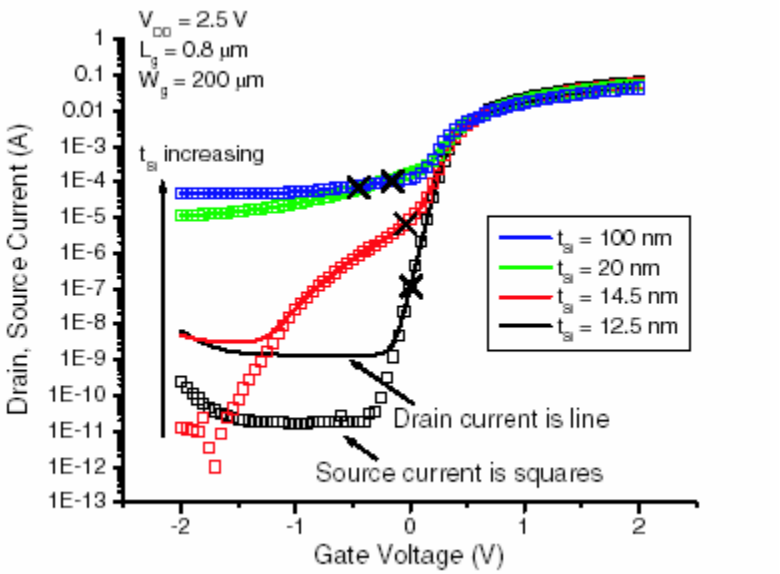

Figure 1-11: Subthreshold characteristics of strained silicon MOSFETS with strained silicon thicknesses above the critical thickness. Devices above the critical thickness (14.5 nm, 20 nm, and 100 nm) show increased off-state leakage current [Fio04].

1.4.1.2 Uniaxially Strained MOSFETS

The Intel Corporation recently developed a process flow that uses two different approaches to introduce uniaxial channel strain in both NMOS and PMOS devices. With this new process, strain is independently introduced into the channel of both devices with minimal integration challenges or major increased in manufacturing cost. NMOS devices are fabricated with the standard process flow, and at the end of the process, a highly tensile nitride capping layer is deposited over the source, gate and drain regions. The high tensile stress, approximately $1.8x10^{10}$ dyne/cm^2, in the capping layer creates compressive stress in the source and drain regions, which in turn induces longitudinal tensile stress and out of plane compressive stress in the channel area. [Tho04a].

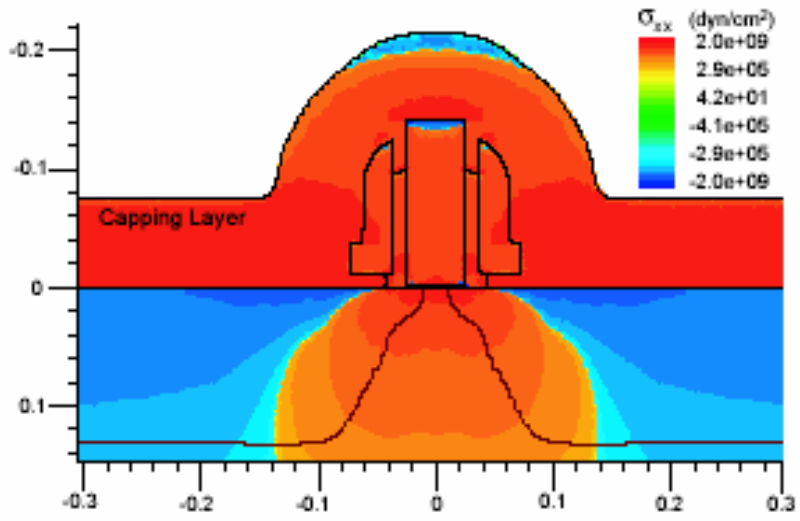

Figure 1-12: Stress along the channel in a strained silicon NMOS transistor [ISE04]

Uniaxial strain is introduced into PMOS transistors by depositing $Si_{1-x}Ge_x$ in a recessed etched trench (source and drain regions) on each side of the channel. Boron has a higher solid solubility limit in silicon germanium, thus allowing for higher boron activation [Sad02]. Since the $Si_{1-x}Ge_x$ has a larger lattice constant than Si, it compresses

the channel from both sides and induces compressive stress in the channel region. For a PMOS device of $Si_{0.83}Ge_{0.17}$ source/drain regions, 1.4 GPa of compressive stress simulation results show approximately 500 MPa of uniaxial compression in the channel [Tho05]. This technique of applying strain in the channel however is only applicable for nanometer channel lengths; in longer devices the compressive force would not have penetrated far enough to strain the entire channel. A large benefit to introducing strain in this technique is that integration issues are kept to a minimum because the strain is applied late in the process flow. Because the $Si_{1-x}Ge_x$ is confined to the source/drain regions, self-heating and leakage currents are not observed [ISE04]. Compressive stress from is shallow trench isolation structures has also demonstrated enhancements in PMOS device performance, which was discussed above in Section 1.3.

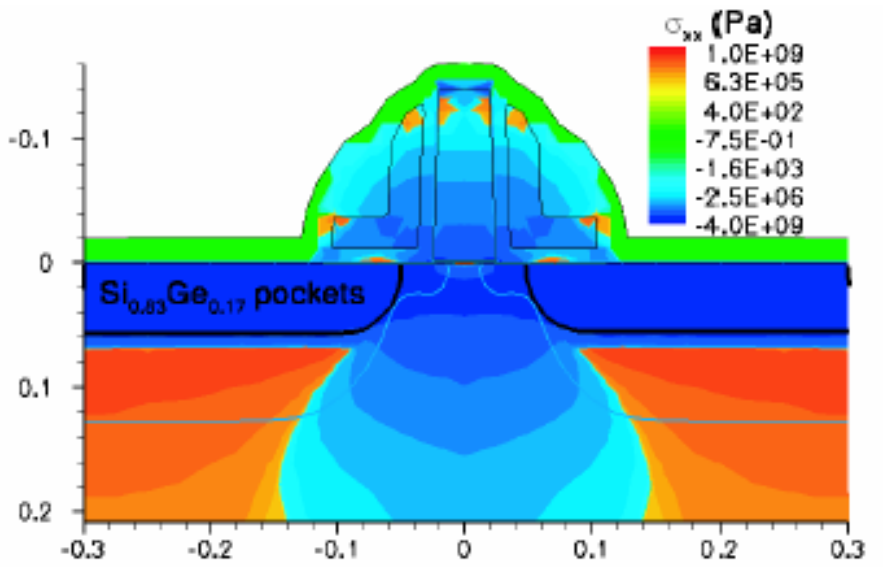

Figure 1-13: Stress along the channel in a strained silicon PMOS transistor [ISE04]

1.4.2 Stress effects on electrical characteristics

In 1954, Charles S. Smith discovered that bulk silicon and germanium demonstrate a change in electrical resistance with strain [Smi54]. This is known as the piezoresistive effect, and it can be used as a strain measurement tool for in strained silicon devices.

Since there is a lack of data for many thin film materials used in semiconductor processing, the bulk coefficients are used for simplicity. For small strains, piezoresistance varies linearly with stress, and by analyzing the piezoresistive coefficients, it was observed that the most effective stress for PMOS devices is longitudinal compressive stress, but is longitudinal tensile and out-of-plane compressive for NMOS devices [Tho04a].

Thompson et al. studied mobility enhancements in MOSFETs at low strain and high vertical electric field [Tho04a]. For PMOS devices, the piezoresistance coefficients predicted that for 500 MPa of stress, a 40% increase in hole mobility for uniaxial compressive stress, and a 5% decrease in hole mobility for biaxial tensile stress resulted. Longitudinal uniaxial compressive strain introduced by $Si_{0.83}Ge_{0.17}$ in the source/drain of a PMOS increased the hole mobility by 50% for a 45 nm gate length, and the NMOS devices showed a 10% mobility enhancement from a 75 nm capping layer [Tho04a]. The electron mobility enhancement is less than the PMOS because the strain induced from the nitride capping layer is less than the strain from growing $Si_{0.83}Ge_{0.17}$ into the source/drain regions. However, the strain from the capping layer increases as the nitride capping layer is increased.

Wafer bending techniques performed by Uchida et al. investigated the hole and electron mobility enhancement in biaxial and uniaxial stressed bulk and SOI MOSFETs. For both carriers, the appropriate uniaxial stress showed the largest enhancements in the [110] direction at high vertical fields. For 3.5 nm SOI NMOS devices, the electron mobility enhancements under biaxial and uniaxial strains were almost equivalent. In

addition, the electron mobility enhancement in the [110] direction under uniaxial tensile strain was comparable in both SOI and bulk devices.

Lim et al. and Thompson et al. demonstrated through wafer bending, a favorably small threshold voltage shift was found for uniaxially strained NMOS devices. Biaxially strained NMOS devices exhibited a four times greater threshold voltage shift than uniaxially strained silicon NMOS transistors. Simulations show that when correcting for the large biaxial threshold voltage shift, much of the performance gain is lost [Lim04]. The small threshold shift for uniaxial strain, however, is a result of lower bandgap narrowing and the strain of the n+ poly gate [Tho04c].

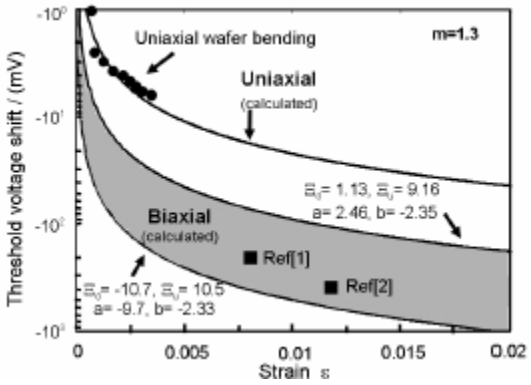

Figure 1-14: Calculated and measured threshold voltage shift for NMOS under biaxial and uniaxial stress (4x shift for biaxial stress) [Lim04, Tho04c].

1.5 Organization

The purpose of this work is to understand the unintentional stress sources that arise during integrated circuit (IC) fabrication process and provide more accurate process models. By understanding how the stresses affect device operation, the stresses and strains can be engineered to improve device performance and avoid high leakage currents. In this work, C++ code was implemented in Florida Object Oriented Processing Simulator (FLOOPS) to study stress in the silicon substrate due to boron doping and

nitride deposition. Simulations were performed for software validation and results were presented.

This chapter provided a literature review describing many applications of stress in silicon technology. In the first section, stress induced dislocations were discussed for various structures. Next, the effects of STI stress on device performance were addressed. In the following section, the strained silicon concept was introduced and the effects of the advantageous and unintentional stresses on device performance were presented. In Chapter II, the concepts of stress and strain are defined, examples of the normal and shear components are given, and a stress-strain relationship for linear elastic materials also described. In Chapter III, various stress and strain sources that arise during the semiconductor fabrication process are addressed, including sources from LOCOS, STI, thin film deposition, and dopant induced strains. Chapter IV focuses on the software implementation in FLOOPS to calculate the displacement and stress in the silicon substrate due to boron doping and nitride deposition. Chapter V provides applications and results of the displacements and stresses computed from beam bending, nitride deposition, and PMOS-like structure simulations. Chapter VI provides a summary and recommendations for future work.

CHAPTER 2
LINEAR ELASTICITY, STRESS, AND STRAIN

2.1 Linear Elastic Materials

Linear elasticity is a property that all materials possess to an extent. Solids respond to externally applied loads by developing internal forces, and stress is the distribution of those forces over a unit area. A solid deforms from its natural state due to stress, and if the deformation is small enough, the solid will return to its original shape once the load has been removed. The relationship between stress and strain for linear elastic materials is shown in Figure 2-1.

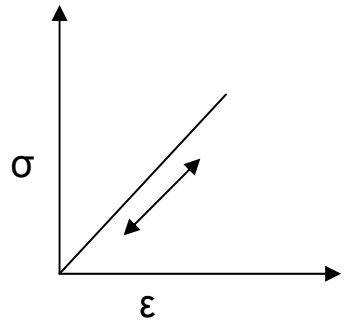

Figure 2-1: Linear elastic deformation

A simple example to illustrate linear elasticity is an ideal spring. One end of the spring is fixed and the other end is free to move.

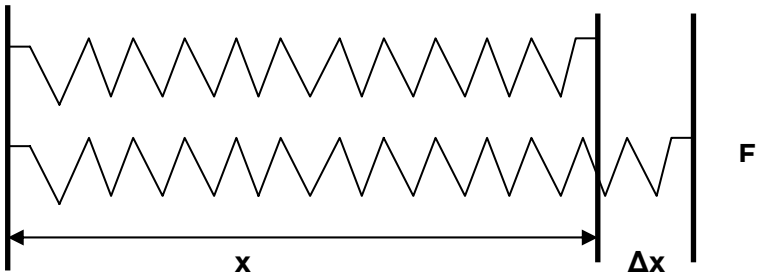

Figure 2-2: Deformation of a spring with an applied force

When an external force is applied to the spring, an equal but opposite counter force is generated. A deformation Δx, or strain results due to the force applied. The internal force and deformation is related by $f = kx$, where f is the force, x is the length of the spring, and k is the stiffness of the spring. Stiffness is a measure of how resistant the body is to external forces. If too much stress is applied, the spring will not return to its original position and will become plastically deformed. A measure of how much stress can be applied before plastic deformation occurs is called the yield strength.

Under the temperatures ranges and processing conditions that will be considered in this work, silicon acts as a linear elastic material. Understanding how stress affects the fabrication process is very important because proper strain engineering can enhance device performance, while unintentional strain can be deleterious. In this section, stress, strain, plane stress, plane strain, and the stress-strain relationship will be discussed.

2.2 The Stress Tensor

Stress (σ) is defined as the force per unit area acting on the surface of a solid.

$$\sigma = \lim_{\Delta A \to 0} \frac{\Delta F}{\Delta A} \tag{2-1}$$

Stresses have two components, normal and shear forces. Normal forces act perpendicular to a face and tend to stretch or compress a body, while shear forces (τ) act along the face of a body and exhibit a "tearing" motion. Tensile forces are positive, while compressive forces are negative. An example illustrating a normal force is a weight hanging from the bottom of a cube by a string. The force of the weight acts perpendicular to the bottom of the cube and pulls the box downward to create a tensile force. To illustrate shear stress imagine a metal rod permanently attached by a bolt to a sheet of metal. If the rod was pushed parallel to the metal sheet, the ripping forces that develop in the bolt represent the shear stresses.

To illustrate all of the stress components, consider an infinitesimal cube with normal (σ_{ij}) and shear (τ_{ij}) stress components stress components in the *x*, *y*, and *z* directions. The first subscript identifies the face on which the stress is acting, and the second subscript identifies the direction.

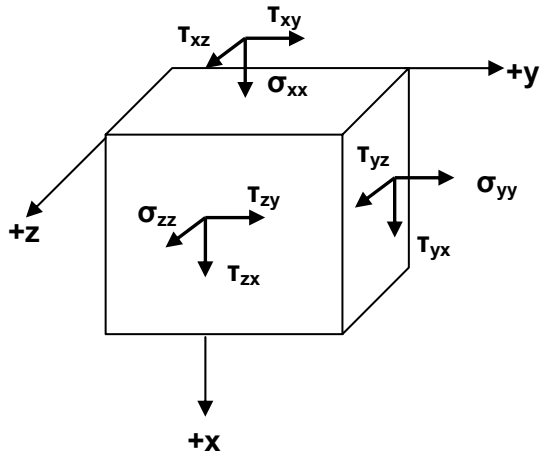

Figure 2-3: Stress components of an infinitesimal cubic element.

For example, to evaluate the stress acting on the y-plane of the cube in figure 2-3, with area $\Delta A_y = \Delta x \Delta z$, the stress vector T on that plane is:

$$T = \tau_{yx} \cdot \mathbf{x} + \sigma_{yy} \cdot \mathbf{y} + \tau_{yz} \cdot \mathbf{z}\,, \tag{2-2}$$

where **x, y,** and **z** are unit vectors in the *x*, *y*, and *z* directions, and the normal and shear stress components acting on the y-plane are:

$$\tau_{yx} = \lim_{\Delta A_y \to 0} \frac{\Delta F_x}{\Delta A_x} \tag{2-3}$$

$$\sigma_{yy} = \lim_{\Delta A_y \to 0} \frac{\Delta F_y}{\Delta A_y} \tag{2-4}$$

$$\tau_{yz} = \lim_{\Delta A_y \to 0} \frac{\Delta F_z}{\Delta A_y} \tag{2-5}$$

Nine stress components from three planes are needed to describe the stress state at an arbitrary point on the continuous body. The grouping of these terms in matrix form is called the stress tensor σij:

$$\sigma_{ij} = \begin{bmatrix} \sigma_{xx} & \tau_{xy} & \tau_{xz} \\ \tau_{yx} & \sigma_{yy} & \tau_{yz} \\ \tau_{zx} & \tau_{zy} & \sigma_{zz} \end{bmatrix} \tag{2-6}$$

In static equilibrium, some of the shear stresses are equal τxy= τyx, τyz= τzy, and τxz= τzx, and by symmetry, the stress matrix can be reduced to six components:

$$\sigma_{total} = \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \tau_{xy} \\ \tau_{yz} \\ \tau_{zx} \end{bmatrix} \tag{2-7}$$

2.3 The Strain Tensor

When forces are applied to a solid body it will deform. Strain (ε) is a unitless parameter that quantifies the amount of deformation, and is equal to a change in length in a given direction divided by the initial length. To illustrate normal strain, consider an infinitesimal element with possible displacements *u(x,y,z), v(x,y.z),* and *w(x,y,z).* The variables *u, v, and w* are the displacements in the *x*, *y*, and *z* directions respectively. Assume the element in figure 2-4 experiences deformation in all three directions, and the dashed lines represent the element after deformation. The change in length in the *x* and *z*

directions are negative, which represents a compressive, or negative strain. The change in length in the y direction is positive, which represents a tensile or positive strain.

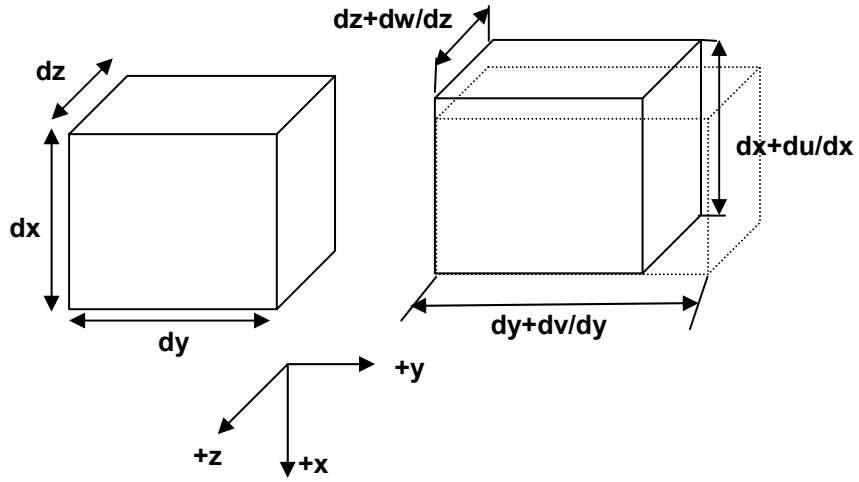

Figure 2-4: Normal strain in the x, y, and z directions. du/dx<0, dv/dy>0, and dw/dz<0

Silicon, like all linear elastic materials, becomes narrower in the cross section when it is stretched. A measure of the transverse to longitudinal strain is know as Poisson's ratio, υ, where a positive ratio is considered tensile and a negative ratio is considered compressive.

$$\upsilon = \frac{\varepsilon_{transverse}}{\varepsilon_{longitudinal}} \tag{2-8}$$

Shear strain (γ) is the displacement in *x* direction with respect to a change in the length of *y*, plus the displacement in the *y* direction with respect to a change in length of *x*:

$$\gamma_{xy} = (\frac{\Delta u_x}{\Delta y} + \frac{\Delta u_y}{\Delta x}) = (\frac{\partial u_x}{\partial y} + \frac{\partial u_y}{\partial x}) \tag{2-9}$$

To illustrate shear strain, consider the differential element experiencing deformation in the *x* and *y* directions where $\theta_1$and θ_2 are the change in angle from the original shape, and Δu_x and Δu_y are the direction of the displacements.

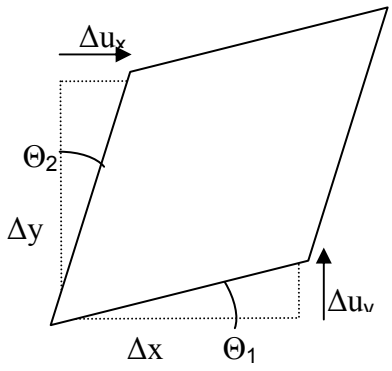

Figure 2-5: Example of shear strain in the x-y direction

For small displacements, referred to as micro-strain (με), the shear strain can be approximated as the angle itself, tan θ ~ θ and the total strain is equal to the sum of the angles θ_1 and θ_2. [Sen01] To illustrate the strain components, consider the cube from figure 2-4. There are nine normal and shear strain components that are related to the displacements by:

$$\begin{array}{lll} \varepsilon_{xx} = \dfrac{\partial u}{\partial x} & \gamma_{xy} = \dfrac{\partial v}{\partial x} + \dfrac{\partial u}{\partial y} & \gamma_{xz} = \dfrac{\partial w}{\partial x} + \dfrac{\partial u}{\partial z} \\ : \ \gamma_{yx} = \dfrac{\partial u}{\partial y} + \dfrac{\partial v}{\partial x} & \varepsilon_{yy} = \dfrac{\partial v}{\partial y} & \gamma_{yz} = \dfrac{\partial w}{\partial y} + \dfrac{\partial v}{\partial z} \\ \gamma_{zx} = \dfrac{\partial u}{\partial z} + \dfrac{\partial w}{\partial x} & \gamma_{zy} = \dfrac{\partial v}{\partial z} + \dfrac{\partial w}{\partial y} & \varepsilon_{zz} = \dfrac{\partial w}{\partial z} \end{array} \tag{2-10}$$

Combining these terms in matrix is called the strain tensor, εij:

$$\varepsilon_{ij} = \begin{bmatrix} \varepsilon_{xx} & \gamma_{xy} & \gamma_{xz} \\ \gamma_{yx} & \varepsilon_{yy} & \gamma_{yz} \\ \gamma_{zx} & \gamma_{zy} & \varepsilon_{zz} \end{bmatrix} \tag{2-11}$$

In static equilibrium, the shear components are equal:

$$\gamma_{xy} = \gamma_{yx} = \frac{1}{2}\left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}\right), \gamma_{yz} = \gamma_{zy} = \frac{1}{2}\left(\frac{\partial v}{\partial z} + \frac{\partial w}{\partial y}\right), \gamma_{xz} = \gamma_{zx} = \frac{1}{2}\left(\frac{\partial u}{\partial z} + \frac{\partial w}{\partial x}\right) \tag{2-12}$$

By symmetry of the matrix, the strain tensor can be condensed into six components:

$$\varepsilon_{total} = \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \gamma_{xy} \\ \gamma_{yz} \\ \gamma_{xz} \end{bmatrix} \tag{2-13}$$

2.4 Plane Stress

Plane stress is defined as a state of stress in which the normal stress and shear stresses directed perpendicular to the plane are assumed to be zero: $\sigma_z = \tau_{xz} = \tau_{yz} = 0$. Thin films exhibit plane stress because the *z* direction dimension is very small in comparison to the *x* and *y* dimensions, and the forces only act in the *xy* plane. A significant source of plane stress in thin films arises from the deposition process. Stress from thin films will be discussed in more detail in Chapter III.

Consider a thin film attached to a substrate to illustrate plane stress. The regions of the plane that are about three times the film thickness from the edge exhibit plane stress because the top surface is stress free. The behavior in the edge regions is more complex, and is dominated by peel forces that tend to detach the film from the substrate. [Sen01]

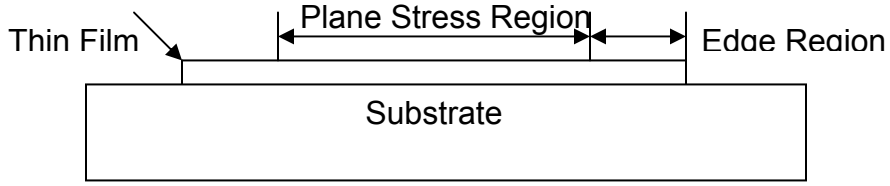

Figure 2-6: Plane stress in a thin film

For an isotropic linear solid under plane stress, the in-plane strain (ε) and shear strain (γ) values are defined as:

$$\varepsilon_x = \frac{1}{E}(\sigma_x - \upsilon\sigma_{y)} \tag{2-14}$$

$$\varepsilon_y = \frac{1}{E}(\sigma_y - \upsilon\sigma_x) \tag{2-15}$$

$$\gamma_{xy} = \frac{2(1+\upsilon)}{E}\sigma_{xy} \tag{2-16}$$

The only non-zero out of plane strain is:

$$\varepsilon_z = \frac{-\upsilon}{E}(\sigma_x + \sigma_y)\,. \tag{2-17}$$

2.5 Plane Strain

Plane strain is defined as a state of strain in which the normal strain ε_z and shear strains γ_{xz} and $\gamma_{yz} = 0$:

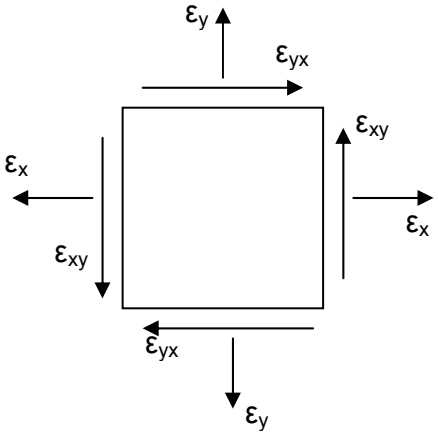

Figure 2-7: Example of plane strain in the x-y direction

The plane strain assumption is used for long bodies with constant cross-sectional area whose forces only acts in the *xy* plane, and used when the strain in the *z* direction is significantly less than in the other two orthogonal directions. Under this assumption, $\varepsilon_{xy} = \varepsilon_{yx}$ and the strain matrix reduces to:

$$\varepsilon_{xy} = \begin{bmatrix} \varepsilon_{xx} & \gamma_{xy} \\ \gamma_{yx} & \varepsilon_{yy} \end{bmatrix} \tag{2-18}$$

2.6 The Stress-Strain Relationship

The relationship between stress and strain is described by Hooke's Law, and it is used to calculate the deformation in a material due to stress. The ratio of stress to strain is known as Young's Modulus of Elasticity, *E*, and the ratio of shear stress to shear strain is known as the Shear Modulus of Elasticity, *G*. For a linearly elastic material, the normal stress is linearly proportional to normal strain by:

$$\sigma = E \cdot \varepsilon \tag{2-19}$$

and the normal forces are resisted by the body's bulk modulus, which determines how much a solid will compress under external pressure:

$$K = \frac{E}{3(1-2\nu)} \tag{2-20}$$

Shear stress is linearly proportional to shear strain by:

$$\tau = G\gamma \tag{2-21},$$

and shear forces are resisted by the body's shear modulus:

$$G = \frac{E}{2(1+\nu)} \tag{2-25}$$

The Hookean Model

For linear elastic materials stress is linearly proportional to the strain and is described by:

$$\sigma_{ij} = C_{ijkl}\varepsilon_{ij} \tag{2-26}$$

where Cijkk is the fourth order elastic stiffness tensor of 81 material constants, σij is the equilibrium stress values from (2-7) , and εij is the equilibrium strain from (2-13).Silicon is an anisotropic material with diamond cubic crystal symmetry and the C_{ijkl} matrix reduces to 36 components with three elastic constants c11, c12, and c44:

$$C_{ijkl} = \begin{vmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44} \end{vmatrix} \tag{6-2}$$

C11 = 166 GPa, C12 = 64 GPa and C44 = 80 GPa [Str05]. Although silicon is an anisotropic material, it can be approximated with isotropic elastic properties for simplicity, meaning that the elastic properties in all directions are equal. For isotropic material, the elastic constants c11, c12, and c44 are [Sen01, Zie89]

$$c_{11} = \frac{E(1-\nu)}{(1+\nu)(1-2\cdot\nu)} \tag{6-3}$$

$$c_{12} = \frac{E\cdot\nu}{(1+\nu)(1-2\cdot\nu)} \tag{6-4}$$

$$c_{44} = \frac{E}{(1+\nu)} \tag{6-5}$$

The elasticity constants for the crystal directions are E[100] = 129 GPa, E[110] = 168 GPa, and E[111] = 186 GPa [Str05].

Hooke's Law states that strain can exist without stress. To illustrate this, consider an elastic band that experiences a force in the *y* direction, creating a stress in the *y* direction. The strain in the *x* direction however is not equal to zero. As the rubber band is pulled outward in the *y* direction, it moves inward in the *x* direction to fill the original space. The *x* plane does not have any external forces acting upon it, but a change in length is experienced. This demonstrates that strain can exist in a particular plane without any stresses present. When the forces are removed, the elastic band returns to its original shape.

2.7 Summary

This chapter discusses the mechanics behind linear elastic materials and definitions of stress and strain. First, linear elastic materials are defined as materials that return to their original form after an applied force is removed, and a spring is used to demonstrate this behavior. When to much force is applied, the spring will leave the elastic regime and experience plastic deformation. Next the stress and strain tensors are defined by the normal and shear components. Stress is the force per unit area, and strain is the change in length divided by the original length. In static equilibrium, both the stress and strain tensors can be reduced to six components compared to nine because the shear stresses and shear strains are equal. Next, the two-dimensional plane stress and plane strain assumptions are discussed. Finally, the stress-strain relationship is described by Hooke's Laws, which relates Young's Modulus, the Shear Modulus and the Bulk Modulus to stress and strain, and the laws explain how strain can exist without stress.

In Chapter III, stress and strain sources that arise during the IC fabrication process will be discussed in detail. Different sources of stress and strain that will be explored are: non-planar oxidation, thin film deposition, STI formation, and dopant induced strains.

CHAPTER 3
STRAIN SOURCES

While scaling devices to nanometer dimensions improves performance, it also strongly magnifies the mechanical forces that arise during fabrication. Stress and strain are unintentionally introduced into the silicon substrate after various stages of the fabrication process, and are becoming increasingly difficult and expensive to cope with. Stress from thermal expansion mismatch, ion implantation and lattice mismatch can all result in thin film stress. This chapter will discuss the main factors influencing stress and strain from the IC fabrication process and measures to control them. Oxidation induced stress, thin film stresses, STI stress, and dopant induced strains will be discussed. Finally, a brief discussion of boron diffusion in silicon and silicon germanium (SiGe) will be provided.

3.1 Oxidation Induced Stress

Silicon dioxide (SiO_2) formation is a critical process step for device fabrication, and exposing a silicon wafer to oxygen at high temperatures forms an excellent electrical isolator. In addition to its isolation properties, SiO_2 also acts as a barrier to impurities during deposition and implantation. [Jae02] During thermal oxidation, Si-Si bonds are broken to accommodate the oxygen atoms, and the oxide reacts with the Si at the Si-SiO_2 interface. The forming oxide consumes the silicon as it expands upwards at a rate of 2.2 times the volume of oxidized silicon. The interface moves into the Si bulk and leaves behind a compressively stressed region. The coefficient of thermal expansion for SiO_2 is less than that of Si, resulting in a negative strain value. In non-planar regions, the

behavior is more complex because the oxide can no longer freely expand upward. On convex surfaces such as the top corner of an isolation trench, the oxide becomes stretched around the corner in tension. On concave surfaces such as the bottom corner of an isolation trench, the growing oxide squeezes together and becomes compressed. The stress from oxide growth relaxes depending on the oxide viscosity and as the temperature increases, the oxide flow increases and permits faster relaxation of the structural strains. [Yen00, Yen01] Oxide viscosity determines the oxide growth on shaped surfaces, and is described by:

$$\eta(stress) = \eta(T)\frac{\sigma_s Vc / 2kT}{\sinh(\sigma_s Vc / 2kT)} \tag{2-1}$$

where $\eta(T)$ is the stress free temperature dependent oxide viscosity, σs is the shear stress in the oxide, and Vc is a fitting parameter [Yen00, Yen01].

Yen et al [Yen01] showed that external mechanical stress affects the kinetics of silicon thermal oxidation. It had been previously understood that the oxidation rate constants were only temperature dependent, but recent studies show that stress also plays a large role in the rate. In the experiment conducted, two wafers were bent, one in tension and the other in compression and the oxide thickness and stress distribution across the wafer was observed over time. The tensile wafer exhibited an increase in oxide growth, while the wafer in compression showed little to no effect. The increase in oxide growth can be explained by the enlarged atom spacing of the silicon wafer under tensile stress.

LOCOS Formation

Local Oxidation of Silicon (LOCOS) is an obsolete technique used to isolate active regions of ICs. Selected areas of the wafer are oxidized by masking the non-oxidized

region with silicon nitride (Si3N4). Beginning with a clean wafer, a uniformly thin layer of SiO2 is grown, and a layer of Si3N4 is deposited. The thin SiO2 layer is present to alleviate the mismatch stress between the silicon and the nitride layer. After the nitride is patterned, the wafer is exposed and all areas not covered by the nitride form a thick layer of SiO2. Compared to a planar surface, the stress from LOCOS formation is significantly higher because the volume expansion is dimensionally confined. [Sar04] The main forces that arise in the formation of LOCOS structures are illustrated in Figure 3-1: F1 represents the intrinsic stresses from the pad oxide and nitride layer, F2 represents the tensile bending stresses from the nitride deposition, F3 represents the compressive stresses from the non-planar field oxide growth into confined areas, and F4 represents the thermal expansion mismatch stress from the difference in thermal expansion coefficients between Si and SiO_2.

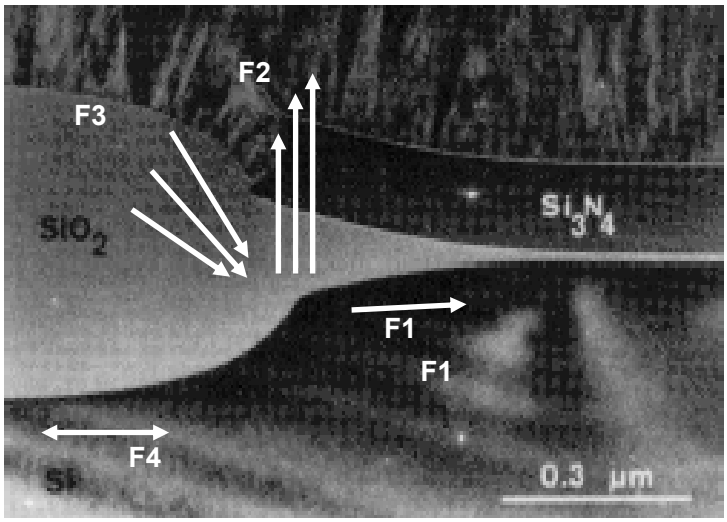

Figure 3-1: Forces present in LOCOS formation [Sar04]

Due to the high stresses encountered in LOCOS formation, alternate isolation techniques such as shallow and deep trench isolation were developed.

3.2 Thin Film Stress

Thin films are a layer with high surface-to-volume ratio and are commonly used in IC fabrication for masking, passivation, isolation, and conduction [Hu91]. All stresses present in thin films after deposition are referred to as residual stresses and can be broken down into two components: 1) thermal mismatch stress and 2) intrinsic stresses. Thin films can be deposited or thermally grown, but depending on the deposition process, temperatures, and dopant concentration, tensile or compressive residual stresses will be obtained [Hu91]. The regions of highest intrinsic stress in thin films are at the film edges or in non-planar regions. Residual stresses will cause device failure due to instability and buckling if the deposition process is not properly controlled.

3.2.1 Thermal Mismatch Stress

Thermal mismatch stress occurs when two materials with different coefficients of thermal expansion are heated and expand at different rates. During thermal processing, thin film materials such as polysilicon, SiO_2, and Si_3N_4 expand when exposed to high temperatures and contract when cooled to lower temperatures according to their coefficient of thermal expansion. The thermal expansion coefficient for small strains such as those encountered in IC processing is defined as the rate of change of strain with temperature and is measured in microstrain/Kelvin (με/K) [Sen01]:

$$\alpha_T = \frac{d\varepsilon}{dT} \tag{2-2}$$

Although α_T is temperature dependent, it can be treated as a constant over a wide range of temperatures. For example, Si ~ polysilicon has an α_T ranging from 2.6-4.5 με over the temperature ranges of 20-900°C [Fre03] and SiO_2 has an α_T of 0.5 με .

Consider the strain when a thin Si_3N_4 layer is deposited onto a Si wafer at temperature T_d and cooled to room temperature T_r and ΔT =. T_d- T_r. The thermal mismatch strain of the substrate is [Sen01]:

$$\varepsilon_{sub} = -\alpha_{Tsub}\Delta T \quad (2\text{-}3)$$

If the film was not attached to the substrate, it would experience a thermal strain:

$$\varepsilon_{f} = -\alpha_{Tf}\Delta T \quad (2\text{-}4),$$

Thin films that are attached to a substrate experience more complex behavior. Given that the Si wafer is much thicker than the Si_3N_4 layer, the nitride will contract according to the Si substrate and the thermal mismatch strain that results is [Fre03]:

$$\varepsilon_{f,mismatch} = (\alpha_{Tf} - \alpha_{Ts}) \cdot \Delta T \quad (2\text{-}5)$$

where αTf and αTs are the thermal expansion coefficients of the film and substrate respectively. Positive strain is denoted as tensile and negative strain as compressive. Thermal mismatch stress and strain are related through Young's modulus E, and Poisson's ratio, ν by:

$$\sigma_{f,mismatch} = (\frac{E_f}{1-\upsilon}) \cdot \varepsilon_{f,mismatch} \quad (2\text{-}6)$$

where Ef is Young's Modulus for the film, and εf, mismatch is the thermal mismatch strain described in (2-5).

3.2.2 Intrinsic Stress

Intrinsic stress is the component of residual stress due to variations in the deposition process and is dependent on factors such as: deposition rate, thickness and temperature. It is important to minimize the intrinsic stresses generated because their magnitudes can amount to stresses greater than those of thermal mismatch. After a thin

film is deposited, it will lie in either tension or compression. Tensile intrinsic stress is the result of a film wanting to be "smaller" than the substrate because it was "stretched" to fit it. Compressive stress results when a film wants to be "larger" than the substrate because it was "compressed" to fit.

A technique commonly used to quantify the intrinsic stress is measuring the substrate curvature. In 1909 Stoney observed that a metal film deposited on a substrate was in tension or compression when no external loads were applied to it [Fre03]. Through this observation, Stoney created a simple analysis to relate the stress in the film to the amount of substrate curvature. This is known as the Stoney formula [Fre03]:

$$\sigma_f = \frac{E_{si}}{6 \cdot (1 - \nu_{Si}) \cdot R} \cdot \frac{h_{si}}{h_f} \tag{2-7}$$

where ESi and, νSi are Young's Modulus and Poisson's Ratio for Si, hf and hSi are the film and Si thicknesses, and R is the radius of curvature of the substrate.

Annealing can be performed to alter the residual stresses in thin films, however the large thermal budgets necessary to achieve stress relaxation is inconvenient for standard silicon processing. Zhang et al. [Zha98] showed that compared to conventional heat treatments, high temperature rapid thermal annealing (RTA) can effectively reduce the residual stress within a few seconds.

3.3 Stress from STI

Shallow trench isolation (STI) is a technique used to electrically isolate transistors. While allowing a higher packing density, STI structures are becoming major contributors to the mechanical stresses present in the silicon substrate. To create an STI structure a trench is etched into the silicon using reactive ion etching (RIE). Next the trench walls are lined with a thin layer of SiO_2 by thermal oxidation. The trench is then filled with

chemical vapor deposition (CVD) SiO_2, another CVD dielectric or CVD polysilicon. Finally, the structure is chemical mechanical polished (CMP), and a planar STI structure is created [Chi91].

The stress that results from this process comes from three areas: 1) thermal oxidation of a non-planar surface, 2) thermal mismatch stress from the different materials, and 3) intrinsic stress from the CVD fill deposition. For SOI devices, the silicon can re-oxidize at the buried oxide/Si interface at the STI edge which bends the silicon and adds an additional compressive stress component in the channel of the transistor [Gal04]. These stress sources act cumulatively and result in increased stress levels in the silicon substrate. If the stress levels become significant enough device failure is likely to occur.

Thermal oxidation of non-planar surfaces leaves a compressive stress in the silicon substrate. After etching a trench in the silicon a SiO_2 sidewall liner is thermally grown which creates a large stress in the trench corners due to the oxide growth. In the top corners of the trench, the stress is tensile in the oxide and compressive in the silicon, and in the bottom corners of the trench, the silicon is in tension while the oxide is in compression [Law03]. This corner-induced stress is relaxed by the viscous flow of oxide which was described in section 2.1.

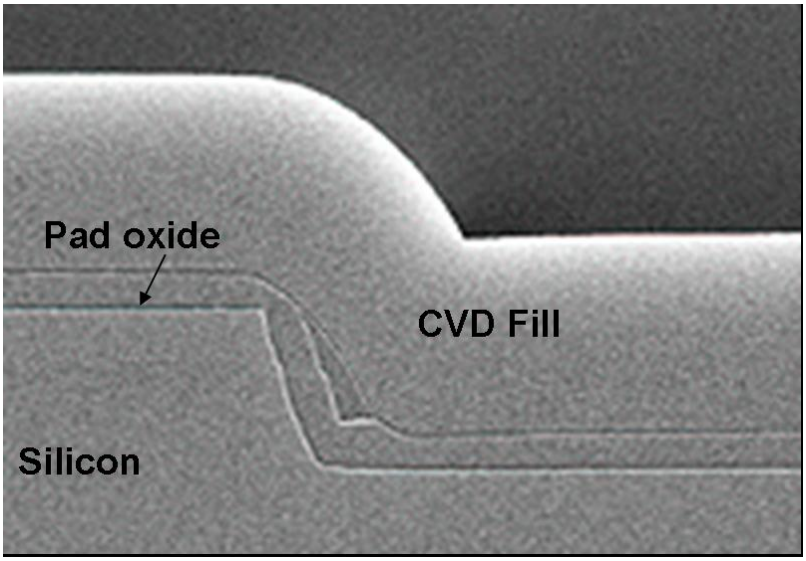

Figure 3-2: Top corner of an STI structure

The second source of stress is the thermal mismatch that arises during the STI process. Before thermal oxidation occurs, the silicon is considered to be in a zero-stress state. After thermally growing the oxide, the wafer is cooled from the oxidation temperature to an intermediate temperature causing a thermal mismatch stress between the Si and SiO_2. Since the coefficients of thermal expansion are almost equivalent for Si and polysilicon, no thermal mismatch strain results for any change in temperature [Chi91].

The final source of stress is a result of the intrinsic stress of CVD fill deposition. Depending on the fill material used and the process conditions, the thin film can have a tensile or compressive intrinsic stress [Chi91]. Films of this nature exhibit biaxial stress, however, when considering an entire trench structure, the biaxial plane changes around the rounded corners of the trench.

Hu performed many isolation trench studies to investigate the effects of varying trench geometry on the stress distribution. His studies showed that for an oxide-filled trench, a compressive stress existed perpendicular to the trench sidewall, localized near

the bottom of the trench and at the surface. In addition, there was a tensile component parallel to the trench near the center of the side wall. The shear stresses were dominant near the trench ends, but vanished at the mid-length of the trench. [Chi91, Hu91].

Stress cancellation can be desirable for increasing the density of transistors on a wafer. For NMOS devices, where compressive channel stress degrades device performance, stress reducing techniques can be employed to return the substrate to a zero stress state. Some mechanisms to alleviate the stress generated during the STI process are counter doping and corner rounding. Boron introduces a local tensile strain into the silicon substrate when it sits in a substitutional lattice site. In areas of larger compression, boron can be introduced by ion implantation or diffusion to even out stresses. By altering the processing conditions, different magnitudes of stress can be achieved to cancel out stresses of opposite magnitudes. Oxide growth stress is significant in the corner regions of isolation trenches and can be reduced by corner rounding. After an oxide is grown it is isotropically etched and the new oxide regrows around a more rounded corner, lowering the total stress from the growth process.

3.4 Dopant Induced Stress

It is well known that introducing dopants into silicon will induce a mechanical stress in the substrate and change the lattice structure. As dopants are introduced in silicon through ion implantation or diffusion, a local lattice expansion or contraction will occur due to the varying atomic sizes and bond lengths of the dopants. Boron is smaller in size than silicon and when it sits on a substitutional lattice site, a local lattice contraction occurs because the bond length for Si-B is shorter than for Si-Si. Horn et al [Hor55] discovered that a single boron atom exerts a 0.0141Å lattice contraction per atomic percentage of boron in silicon at room temperature. Germanium on the other

hand is larger than silicon and when it sits on a substitutional lattice site, a local lattice expansion occurs. At high concentrations significant strain values can result due to a lattice mismatch between the silicon substrate and the dopants [Avc02]. The lattice contraction and expansion for boron and germanium are illustrated in figure 3-3.

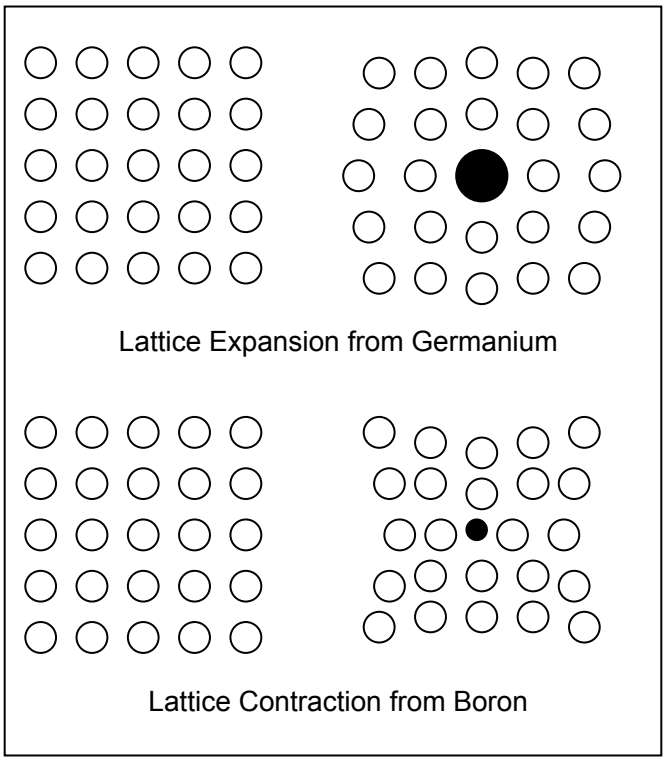

Figure 3-3: Lattice contraction due to boron atom, and lattice expansion due to germanium atom

Stress has demonstrated enhancements in the solid solubility limit of boron in silicon. As we move towards smaller, faster transistors, higher concentrations of dopants have to be packed into smaller regions of the silicon substrate [Sad02]. A critical threat to the future development of ICs is that the electrical solubility limit of boron is being reached. For operational devices, dopants must be electrically activated by annealing to repair the crystal damage from ion-implantation, allowing dopants to sit on substitutional lattice sites. It is important to investigate methods to enhance the solubility of boron in

silicon because it is the most commonly used p-type dopants. Sadigh et al. suggested from calculations that the proper stresses can double the solubility of dopants such as boron in silicon at an annealing temperature of 1000°C for 1% biaxial compressive strain [Sad02]. He observed that negatively charged dopants, such as boron become more soluble under compressive stress, and positively charged dopants such as arsenic prefer tensile stress. The size mismatch of the dopant compared to silicon also plays a large role in the solubility enhancement. The maximum solubility enhancement occurs when the charge and size mismatch with silicon favor the same type of strain.

Stress from Dislocation Loops

Dislocations are a break in the regular lattice spacing, and when too much stress is applied, the silicon substrate will yield by generating dislocations to relax the stress in the material. The presence of many dislocations forms loops, and the growth rate of these loops is dependent on point defect concentration. When combined with ion implantation or oxidation, dislocation loops will nucleate below the substrate's yielding point [Avc02]. The regions of highest stress typically exist on non-planar topologies and at film edges. During several process steps in the fabrication process, a nitride layer is used to mask the oxidation of silicon in active regions. A high shear stress develops at the nitride edge and if the stress becomes too significant, dislocation loops are generated and can glide [Avc02]. To alleviate some of the stress around the nitride edge, a pad oxide can be inserted between the nitride edge and the substrate. Dislocation loops are also generated from STI formation. Fahey et al. [Fah92] demonstrated that minimizing the stress from the STI process such by changing the nitride thickness or using different fill materials

with less intrinsic stress, will help reduce the dislocation density in the substrate. A more in depth explanation of stress from dislocation loops can be found in Chapter I.

3.5 Dopant Diffusion in Silicon and Silicon Germanium (SiGe)

As we move towards the next technology node in the ITRS Roadmap, shallow source/drain junctions requiring high concentrations of active dopants are packed into smaller regions of the substrate. Achieving shallow junctions with active dopants is becoming increasingly difficult due to excessive dopant diffusion. Phosphorus, boron and indium are considered "fast" diffusers, where arsenic and antimony are "slow" diffusers. Arsenic has been the dopant of choice to fabricate NMOS transistors, however PMOS transistors encounter more problems because boron is the only dopant with a high enough solid solubility for the processing temperatures required. Effects such as transient enhanced diffusion (TED) cause the dopant profile to move significantly during annealing, resulting in deeper junction regions.

Ion implantation is used to introduce dopants into the substrate but it creates significant crystal damage. Annealing is used to remove the damage from the implant, return the silicon lattice to a crystalline configuration, and place dopants on substitutional sites to become electrically active. During the early stages of the annealing process, excess interstitials react with dopants resulting in TED; boron is a dopant that strongly exhibits this behavior. Boron interacts with excess interstitials to form BI pairs and they diffuse by breaking atomic bonds and moving the BI pair throughout the lattice. At lower temperatures the damage is not repaired and enhances the dopant diffusion, while at higher temperatures the damage annihilates faster and a transient diffusion is not as significant [Plu00].

Fick's Laws describe dopant diffusion, and the first law relates dopant diffusion to the concentration gradient by [Plu00]:

$$F = -D\frac{\partial C}{\partial x} \tag{2-8}$$

where F is the flux, D is the diffusivity, and $\frac{\partial C}{\partial x}$ is the concentration gradient. Fick's second law of diffusion states that the rate of change of concentration is proportional to the second derivative of the concentration:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} = \nabla \cdot F = \nabla \cdot (D\nabla C) \tag{2-9}$$

In a zero stress-state, dopants diffusivity is characterized by:

$$D = D^0 \exp(\frac{-E_A}{kT}) \tag{2-10}$$

where D is the diffusivity, D^0 is the exponential prefactor, E_A is the activation energy, *k* is Boltzman's constant, and T is the temperature. When compressive and tensile strain is introduced, dopants diffusivities change. Boron for example has an enhanced diffusivity under tensile stress, and a decreased diffusivity under compressive stress. Thus, compressive stress is applied to retard boron diffusion when forming shallow junctions. Boron is a known interstitial diffuser, and the diffusion coefficient is composed of two parts: the neutral and positive charged state of the interstitial [Zan03]:

$$D^B = D^{B^-I^0} + D^{B^-I^+}(\frac{p}{n_i}) \tag{2-11}$$

where ni is the intrinsic carrier concentration and p is the hole concentration. In equilibrium, ni=p. The DBI terms can be expressed in Arrhenius form as:

$$D^{BI} = D_0{}^{BI} \exp(-Q_{BI}/kT) \tag{2-12}$$

where D_0^{BI} is the prefactor and Q_{BI} is the enthalpy.

Diffusion in alloys such as $Si_{1-x}Ge_x$ is different that in pure silicon due to a lattice mismatch between the two materials. There is a 4.2% difference in the lattice constants of Si and Ge; Si has a lattice constant of ~ 5.43Å while Ge has a lattice constant of ~ 5.65Å. When a layer of $Si_{1-x}Ge_x$ is grown on top of Si, it has a bulk relaxed lattice constant which is larger than Si. Layers grown below the critical thickness become strained, but once the critical thickness is exceeded, misfit dislocations are released to relieve the strain of the layer.

Impurity diffusion in SiGe is a debated topic, and many researchers have observed the diffusivity of boron in SiGe. Aziz et al [Raj03] looked at diffusion under biaxial strain with a strain-induced activation enthalpy term. Kuo et al found that increasing Ge content from 0-60% decreased B diffusion and that strain was not a significant factor. He attributed the decrease in B diffusion to the binding between B and Ge atoms which immobilized the B [Kou95]. Rajendran et al found results similar to Kuo and modeled the diffusion of B in Si1-xGex as a result of GeB- clusters. This behavior can be attributed to the fact that B creates a local tensile strain around a B atom, and Ge provides a local compressive strain around a Ge atom. The positive and negative strains are attracted to each other and form a complex to release the stress energy. The total strain from Ge incorporation is [Raj03]:

$$S_{Ge} = (a_{Si-Ge} - a_{Si}) / a_{Si} \tag{2-13}$$

$$a_{Si-Ge} = a_{Si} + (a_{Ge} - a_{Si}) \cdot x \tag{2-14}$$

where a is the lattice constant and x is the atomic fractions of Ge, and substitution the in the lattice constants for Ge and Si gives the strain $S = 0.0425x$.

The boron diffusivity is modeled as (2-10) in silicon. However, in SiGe the incorporation of Ge atoms changes the overall B diffusivity to [Raj03]:

$$D_B^{eff} = D_{B0} \exp(-E/kT) \exp(-QS/kT) \quad (2\text{-}15)$$

where S is the local strain from Ge, and Q is the rate of change of activation energy per unit strain.

3.6 Summary

This chapter discussed the multiple stress and strain sources that arise during the fabrication process . Oxidation-induced stress was described and issues such as the oxidation of non-planar surfaces were addressed. To go into more depth, stress from LOCOS formation such as intrinsic stresses, bending stresses, non-planar oxidation stresses, and thermal expansion stresses between the Si and SiO2 were discussed. In the next section, thin film stresses were described. Thin films exhibit residual stresses and are composed of two components: thermal mismatch strains as a result of materials having different thermal expansion coefficients, and intrinsic stresses as a result of varying conditions during the deposition process. The next section introduced stress from STI structures. The formation of an STI was described and the stress as a result of non-planar oxidation, thermal mismatch strain, and intrinsic stresses were explained. When accounting for stress from an STI, all of the sources are necessary and none can be ignored in computations. Methods to alleviate STI stress such as strain compensation and corner rounding were also touched on. The next section discussed dopant induced stress due to lattice mismatch between different dopants and stress from dislocation loops. Finally, boron diffusion in silicon and silicon germanium under was explored. Chapter IV

focuses on the software implementation in the process simulator FLOOPS, and their applications for boron doping and nitride deposition.

CHAPTER 4
SOFTWARE ENHANCEMENTS TO FLOOPS

Mechanical stresses from process steps such as trench isolation, doping, and epitaxial regrowth play a large role in the scaling of semiconductor devices. Understanding how these stresses affect phenomenon such as dopant diffusion and defect evolution is critical for understanding the limitations of each process technology. Continuum mechanics, which is a branch of mechanics that deals with continuous matter, is used to study these behaviors. More specifically, solid mechanics is the study of the physics of continuous solids. Differential equations are used to solve problems in continuum mechanics, and the equations are specific to the materials under investigation. For example linear elasticity in silicon is described using the constitutive equation known as Hooke's Law that was described in Chapter II. Most of the materials used in silicon processing are modeled as simple elastic materials which make process modeling simpler.

This chapter focuses on the software implementation in the process simulator, FLOOPS (Florida Object Oriented Process Simulator). The "elastic", "bodyforce", "stress" and "strain" operators were developed in FLOOPS to calculate the displacement and stress in the silicon substrate due to boron doping and nitride deposition. The Finite Element Method was implemented using the 2-D plane strain approximation to discretize the region and solve the equations. Simulations were performed to verify the software functionality. The model that FLOOPS currently utilizes to compute stress is a viscoelastic model that was developed for LOCOS; an outdated process. This model

utilizes nonlinear and stress dependent viscosities to describe the behavior of the material, which is no longer an accurate assumption. First, the viscous flow of the oxide is computed in response to the growth forces and then changing forces are calculated as a result of the growth rate [Sim04].

For current fabrication processes, however, the material model that most accurately describes the behavior of materials is the linear elastic model. Unlike the current viscoelastic model that is used, the linear elastic model will couple the mechanical equations with the diffusion solution. In addition, the operators listed above were integrated with the property database and process commands [Law02].

As discussed in Chapter III, the introduction of different dopants into the silicon substrate causes change in the mechanical state of the lattice. Dopants come in a variety of sizes and cause a local tensile or compressive strain in the lattice due to the size mismatch between the dopants and silicon. Boron is a substitutional dopant that is smaller than silicon, and it introduces a local tensile strain in the lattice. Chu et al., Rueda et al., and Yang et al. demonstrated that bending occurs in boron doped cantilever beams, and the amount and direction of bending are dependent on the beam length, width, and doping profile into the depth of the beam [Chu93, Rue98, Yan95]. The strain from boron doping was used to calculate the deflection of the cantilever beam, and results were compared with those of Rueda. Other structures such as a strip of nitride on silicon, and silicon doped with boron source/drain regions were simulated and the stresses were observed. The results will be discussed in Section Chapter V.

4.1 FLOOPS Background

FLOOPS is a C^{++} based simulation program which uses physical models to describe various process steps such as ion implantation, oxidation and diffusion.

Furthermore, FLOOPS uses the Alagator scripting language to define partial differential equations to solve these models by reading in material properties from the parameter database. To arrive at a solution, the program solves a series of differential equations and utilizes matrix mathematics to generate a solution. An internal Newtonian solver is used to converge to a solution. Newton's Method is defined as [Adl04]:

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)} \tag{4-1}$$

Equation 4-1 states that the next solution is equal to the previous solution minus the value of the function at the previous solution divided by the value of the function's derivative at the previous solution.

Operators such as gradients and time derivatives are needed when solving partial differential equations. FLOOPS currently has five operators "ddt", "grad", "sgrad", "diff", and "trans". The "elastic," "bodyforce," "stress," and "strain" are the new operators created in this work. The "ddt" operator computes time derivatives and the "grad" and "sgrad" operators take spatial derivatives. These operators are necessary when performing a diffusion simulation. The "diff" and "trans" operators can be used to compute the parallel and perpendicular electric field components needed to evaluate device mobility [Law02]. The "elastic", "bodyforce", "stress" and "strain" operators calculate the stiffness, displacement, stress and strain in the silicon substrate respectively, and will be used to couple the mechanical stress equations with the diffusion process step.

4.2 The Finite Element Method

The Finite Element Method (FEM) is a numerical technique used for solving differential equations that describes a variety of problems, such as the solution to

displacement in an elastic continuum . The principle of this method allows a complicated region to be sub-divided into elements in a process called discretization. By solving the differential equations of each region, the behavior of the complete domain is determined. First, the geometry of the solid was identified as a three-noded triangle and a 2-D finite element mesh was generated. Each node in the mesh was assigned a number and a set of coordinates (x, y) which specified the position of the node, and as forces were applied, nodes of the solid moves accordingly.

Lets revisit the mechanical equation to be solved is $f=kx$, where f is the force applied, k is the material stiffness, and x is the unknown, displacement. For this notation, the "*f"* term (and any force discussed from here on) is referred to as the "right hand side," and the "*k"* term, or stiffness, is referred to as the "left hand side."

The first step in solving the mechanical problem is finding the element stiffness matrix (left hand side), which describes the how each element will respond to forces. The element stiffness matrix for each element is then assembled into a global stiffness matrix that describes the behavior of the entire material region. Next, the "right hand side" needs to be constructed, which consists of the force, specifically the force from boron doping. Reflecting boundary conditions were applied and the unknown was solved for, in this case, displacement. From the calculated displacements, other parameters of interest such as stress were computed. Silicon was modeled as an isotropic elastic material and the two-dimensional plane strain approximation was used to implement the operators into FLOOPS.

4.2.1 Constructing FEM Elements for the Elastic, Bodyforce, Stress, and Strain Operators

Consider a three-noded triangle *e,* defined by nodes *i, j,* and *k* numbered in the counter-clockwise direction with an area Δ and displacements in the x and y directions.

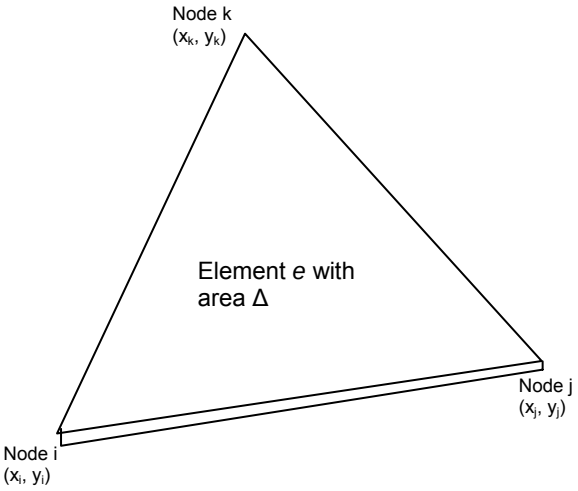

Figure 4-1: Triangular element in coordinate system

There are two degrees of freedom (*x, y*) for each node and three nodes per triangle, creating six degrees of freedom per element. The stiffness of a finite element describes how the element responds to external forces. The stiffer a material, the less deformation it will experience, whereas a flexible material will deform more. Under mechanical equilibrium, all of the nodal forces are equal to zero, $q^e = 0$. Integrating over the triangular element gives the stiffness matrix:

$$k^e = \int B^T \cdot D \cdot B \cdot d(vol) \tag{4-2}$$

or in discretized form [Zie89]:

$$k^e = B^T \cdot D \cdot B \cdot \Delta \tag{4-3}$$

where *k* is the element stiffness, Δ is the element area in two dimensions, and the element volume in three dimensions. The B matrix is a constant matrix dependent on nodal coordinates and [Zie89]:

$$B = \frac{1}{2 \cdot \Delta} \begin{vmatrix} y_{j-}y_k & 0 & y_k - y_i & 0 & y_i - y_j & 0 \\ 0 & x_k - x_j & 0 & x_i - x_k & 0 & x_j - x_i \\ x_k - x_j & y_j - y_k & x_i - x_k & y_k - y_i & x_j - x_i & y_i - y_j \end{vmatrix} \quad (4\text{-}4)$$

where $2 \cdot \Delta$ is twice the area of the triangle and is equal to:

$$2 \cdot \Delta = [(x_j y_k - x_k y_j) - (x_i y_k - x_k y_i) + (x_i y_j - x_j y_i)] \quad (4\text{-}5)$$

The B matrix is used to relate the strain to the displacements, which will be discussed more in Section 4.2.2. The D matrix contains the material properties *E* and *v*. For plane strain, the D matrix is equal to:

$$D = \frac{E \cdot (1-\nu)}{(1+\nu) \cdot (1-2\nu)} \begin{vmatrix} 1 & \frac{\nu}{1-\nu} & 0 \\ \frac{\nu}{1-\nu} & 1 & 0 \\ 0 & 0 & \frac{(1-2\nu)}{2 \cdot (1-\nu)} \end{vmatrix} \quad (4\text{-}6)$$

To find the displacements due to external forces, a matrix mathematics solver called UMF is used to solve the equation *Ax=b,* where A represents the stiffness, b represents the external forces, and x represents the nodal displacements. Below is a portion of the code developed to build the stiffness matrix for a single element.

The B matrix routine takes the six coordinates of a triangle as arguments (three nodes * two displacements *x, y* per node) and returns the [3x6] matrix that was illustrated in (4-4). From the B matrix, the transpose of the B matrix is easily obtained. The D matrix contains the material properties such as Young's Modulus and Poisson's Ratio and returns a [3x3] matrix. As illustrated in (4-4), the stiffness routine multiplies the B

matrix, transpose of the B matrix, and the D matrix together and returns the [6x6] stiffness matrix for a single element.

```
B_Matrix( Bmatrix, x[0], y[0], x[1], y[1], x[2], y[2] );
BT_Matrix(Bmatrix, BTmatrix);
D_Matrix(Dmatrix, E, nu);
Stiffness(BTmatrix, Dmatrix, Bmatrix, C, stiffness);
```

The sum of all element stiffness matrices is known as the global stiffness matrix, which determines the stiffness of the each material region in the mesh. The flowchart below in figure 4-2 demonstrates the step-by-step procedure to create the stiffness matrix for an element.

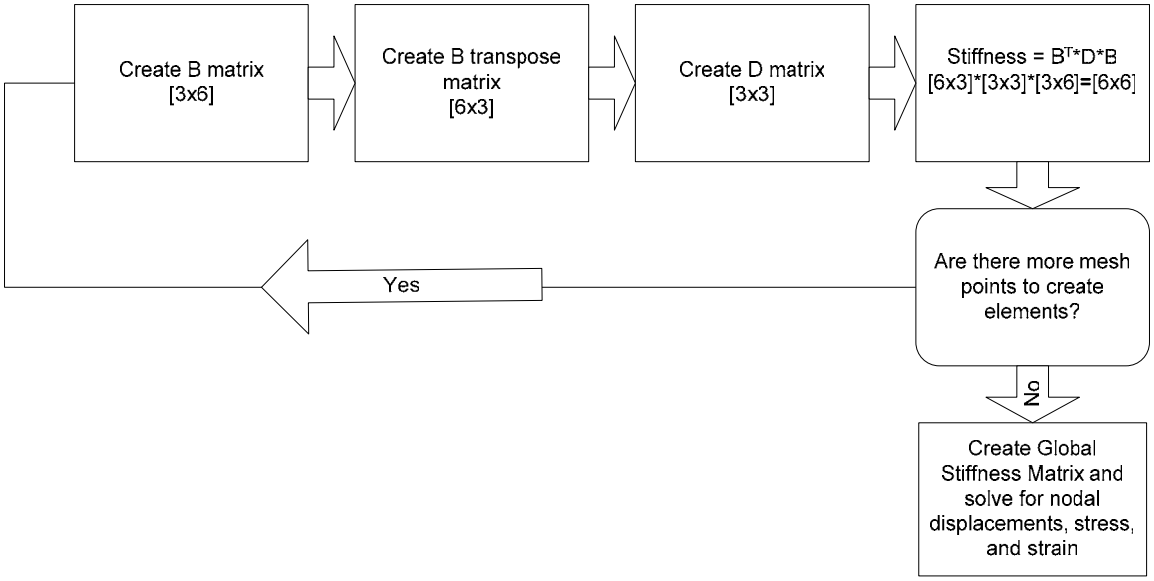

Figure 4-2: Flowchart to create element stiffness matrix

4.2.1.1 Plane Strain Assumption

The plane strain approximation assumes that $\varepsilon_{xz} = \varepsilon_{yz} = \varepsilon_{zz} = 0$; however stress in the z-direction is not equal to zero. This assumption can be used to solve problems with infinitely long dimensions in the z-direction; therefore the strain in the z-direction will approach zero [Rue97]. A problem with the plane strain assumption arises with dopant

and thermal mismatch strain because both dopant and thermal mismatch strains have stress components in the z-direction. To compensate for the 3-D behavior in a 2-D domain, the 2-D strain must be multiplied by a factor of (1+v):

$$\varepsilon = \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \end{bmatrix} = (1+\nu) \begin{bmatrix} \varepsilon \\ \varepsilon \\ 0 \end{bmatrix} \tag{4-7}$$

4.2.1.2 Boundary Conditions

Reflecting boundaries require that the normal component of the velocity and displacement field is set to zero across the interface, which corresponds to a mirror-reflected symmetry across the boundary [Rue97]. To verify the boundary conditions was working, simple simulations were performed that fixed one side of the mesh to zero with the boundary condition, and displaced the other side to a specified distance. The proper displacements were observed across the mesh, verifying the boundary functioned correctly.

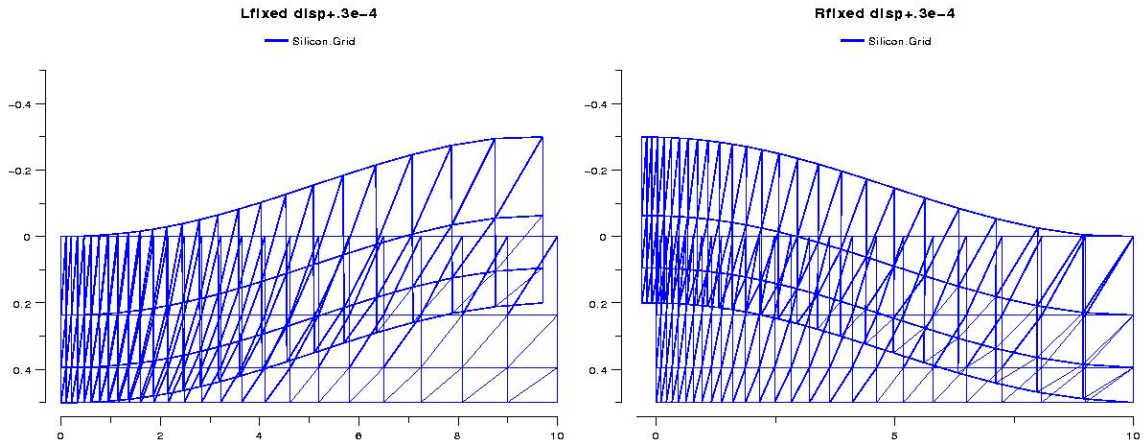

Figure 4-3: Verification of boundary conditions –displacements due to external forces

4.2.2 Forces from Boron Doping

The equivalent nodal force $q_i^{\ e}$ at node *i* due to element *e* must have the same number of components as the nodal displacements, six values – two for each node. This force is described by:

$$q^e = \int_{V^e} B^T \cdot \sigma \cdot d(vol) - f_b^{\ e} \tag{4-8}$$

where B^T is the transpose of the vector relating strain to nodal displacements, f_b is the distributed body forces of the element, and σ is the stress tensor. The "bodyforce" operator was created to model the force from boron and is modeled by [Zie89]

$$f^e{}_b = \int_{V^e} B^T \cdot D \cdot \varepsilon_B^{\ e} \cdot d(vol) \tag{4-9}$$

Integrating over the volume of the element gives the body force in discretized form:

$$f^e{}_b = B^T \cdot D \cdot \varepsilon^e{}_B \cdot \Delta \tag{4-10}$$

The general stress-strain relationship of linear elastic materials is given by:

$$\sigma = D(\varepsilon - \varepsilon_0) + \sigma_0 \tag{4-11}$$

where D is the elasticity matrix, and σ_0 and ε_0 and are the initial stress and strain tensors. The elemental strain is related to the elemental displacements by:

$$\varepsilon^e = B \cdot a^e \tag{4-12}$$

where *a* is the displacements and *B* is the constant matrix given in (4-4). By substituting equation (4-11) into (4-8), the expression for nodal forces becomes:

$$q^e = \int_{V^e} B^T \cdot D \cdot \varepsilon^e \cdot d(vol) - \int_{V^e} B^T \cdot D \cdot \varepsilon_0^{\ e} \cdot d(vol) + \int_{V^e} B^T \cdot D \cdot \sigma_0^{\ e} \cdot d(vol) - f_b^{\ e} \tag{4-13}$$

The "bodyforce" operator was developed to model the elemental strain (ε_B) from boron doping, and is modeled by [Cha96, Rue97]:

$$\varepsilon_B^{\ e} = \frac{\delta_B}{A_{Si}} \cdot \frac{C_{Boron}}{C_{Si}} \cdot (100) \tag{4-14}$$

Where δ_B is the lattice contraction parameter for boron in silicon, C_{Boron} is the boron concentration, (C_{Si} =5x10^{22}cm^{-3}) is the atomic density of silicon, and (A_{Si} =5.4295Å) is the lattice constant of silicon. Horn et al found that the silicon lattice contracts 0.0141Å per atomic percentage of boron concentration [Hor55]. Since the boron concentration is a nodal quantity, the elemental boron concentration must be calculated from the nodal concentrations. To obtain the elemental values of boron strain from the nodal values, the boron concentration is first divided by the atomic density of silicon ($\frac{C_{Boron}}{C_{Si}}$). The lattice displacement is equal to ($\frac{C_{Boron}}{C_{Si}}$) times the lattice contraction parameter (δ_B). Then the strain is computed by dividing the lattice displacement by the lattice constant of silicon (A_{Si}) [Rue98]. The average elemental strain is then computed as the average of the strain value at each of the nodes. Below is part of the code to calculate the nodal displacements and a flowchart for the procedure:

```
double s1 = a.Val(0).get(k); //evaluate the strain at each node
double s2 = a.Val(2).get(k);
double s3 = a.Val(4).get(k);

//compute the average elemental strain by taking the average of all
nodal values.

Strain[0] = sqrt(2.0) * (s1+s2+s3) / 6.0;
strain[1] = sqrt(2.0) * (s1+s2+s3) / 6.0;

//assume no shear component for dopant-induced stress
strain[2] = 0.0;

B_Matrix( Bmatrix, x[0], y[0], x[1], y[1], x[2], y[2] );
BT_Matrix(Bmatrix, Btmatrix); //create B transpose from B matrix
D_Matrix(Dmatrix, E, nu);  //create D matrix
BTMultD(Btmatrix, Dmatrix, C); //multiply B transpose[6x3]
       *D[3x3]=C [6x3]
MultBtDBF(C, strain, fx); //multiply C [6x3] * elemental strain
          [3x1]= nodal displacements [6x1]
```

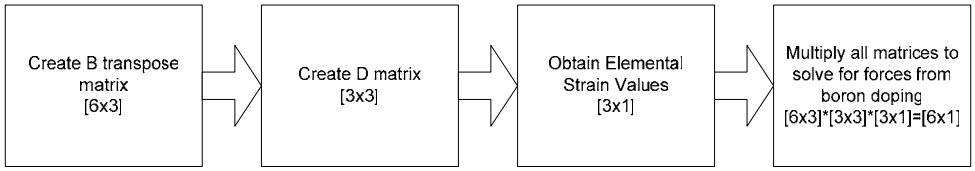

Figure 4-4: Flowchart to solve for forces from boron doping

4.2.3 Strain and Stress Computation

The strains and stresses were calculated from the displacements described in section 4.2.2. The strain is related to the nodal displacements by (4-12) and is equal to the B matrix times the nodal displacements that were calculated in 4.2.2. The strain is a [3x1] column vector containing the normal ***xx, yy*** and the shear ***xy*** values:

$$\varepsilon = \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{xy} \end{bmatrix} \tag{4-15}$$

The stress is related to the strain by the D matrix as defined in (4-11), and by multiplying the strain values above by the D matrix, another [3x1] column vector of the stresses is obtained:

$$\sigma = D \cdot \varepsilon = \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{xy} \end{bmatrix} \tag{4-16}$$

Once the displacements in the silicon were solved for, the function on the command line to solve for stress or strain is: *select z= "Stress/Strain(xx/yy/xy, displacement)",* which calls the stress or strain operators and calculates their values based on the displacements. The ***xx, yy,*** or ***xy*** stress or strain values can be obtained with this function. As noted in (4-15) and (4-16), the column array of stress and strain represent

the ***xx, yy,*** and ***xy*** directions respectively; all of the strain or stress components are initially solved for, and additional code will determine which direction of stress is desired. Contours of the stress fields were plotted, and will be illustrated in chapter V. Below is part of the code and the flowchart to calculate the strains and stresses from the nodal displacements:

```
B_Matrix( Bmatrix, x[0], y[0], x[1], y[1], x[2], y[2] );

//multiply [3x6]B*[6x1]displacement=elestrain[3x1] - strain[xx, yy, xy]
MultiplyStrain(Bmatrix, elestrain, displacement);

// find tt to determine if want xx, yy, or xy direction
if (tt==Dir_XX) val = elestrain[0];

else if (tt==Dir_YY) val = elestrain[1];
else val = elestrain[2];

//now calculate the stresses from the strains
MultiplyStress(Dmatrix, elestrain, stress); //elestrain
   [3x1]*Dmatrix[3x3]=stress[3x1]
```

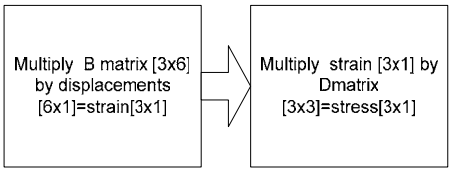

Figure 4-5: Flowchart to calculate strain and stress

4.3 Summary

This chapter began by introducing continuum mechanics and the finite element method. Large areas were sub-divided into smaller regions in a process called discretization to create elements. The stiffness of a region describes how it responds to external forces, and the procedure to create the stiffness matrix for a single element was described. Next, the bodyforce operator defined as representing the forces due to boron doping. The mechanical equation $f=kx$ was solved for, and from the calculated displacements, the stresses in the silicon substrate were calculated. In the next chapter,

applications such as beam bending, nitride deposition, and channel stress from boron doping will be explored.

CHAPTER 5
APPLICATIONS AND COMPARISONS OF TWO-DIMENSIONAL SIMULATIONS

As device channel lengths are scaled into the deep submicron realm, stress components that once could be ignored are now significant. A few examples of how stress is introduced during different process steps is by creating STI structures, doping the source and drain regions, and depositing thin films. At channel lengths as short as 0.1 um, these stress sources can create enough undesirable stress in the channel to alter the carrier mobility and decrease overall device performance. Methods to either suppress the undesirable stress, or enhance the advantageous stress are under research. The software operators, discussed in Chapter IV, were used to calculate stress from various process steps, and the results were compared with experiments from literature and simulations from the commercial version of ISE FLOOPS for software validation.

This chapter presents finite element based models that calculate the residual stresses in various structures. To illustrate the effect of strain from boron doping, a silicon cantilever beam was simulated and the beam length, width, and concentration gradient were varied to observe the bending behavior from a particular boron diffusion process. Next, the stress caused by depositing a strip of nitride on silicon was simulated, and the stress around the corner of the nitride/silicon interface was compared with the values simulated from the ISE version of FLOOPS. Lastly, the stress from doping the source drain regions with boron was observed, and the effects of scaling the channel length, source/drain length, and boron concentration were quantified.

5.1 Boron-Doped Beam Bending

Cantilever beams are used in silicon fabrication technology to create sensors and other MEMS devices. Beam structures are fabricated by thermally diffusing or implanting boron on one side of the silicon wafer, and etching through a mask on the other side of the wafer. sing etchants such as KOH, silicon layers with boron concentrations greater than $7x10^{19}$ cm^{-3} (p^+ Si) show significant slower etching rates than compared to undoped silicon [Yan95]. Since boron is a substitutional atom in silicon, the silicon lattice will contract in the boron diffused layer, and layers with different concentrations of boron will be subjected to different tensile stresses. The wafers bend up or downwards after the cantilever beams are released due to the stress gradient through the depth of the beam [Jae02, Nin96, Rue98,Yan95]. Yang and Chu et al. demonstrated that as-implanted cantilever beams with tensile residual stresses bend upwards to maintain equilibrium. However, subsequent processing steps such as oxidation or annealing can change the residual stress state from tensile to compressive [Yan95]. The results of these experiments however are not comparable because of the difference in experimental conditions.

For a cantilever beam made of linear elastic material such as silicon, the beam deflection is [Nin96]

$$v_{def} = -\frac{Ml^2}{2EI} \tag{5-1}$$

where M is the bending moment, I is the moment of inertia of the beam, and E is Young's Modulus. For cantilever beams of different lengths, but identical *M, E,* and *I,* the deflection curves are the same.

Beams with a uniform dopant profile, or a profile that is symmetric to the center of the beam, do not exhibit bending due to equal distribution of forces from boron through the thickness of the beam.

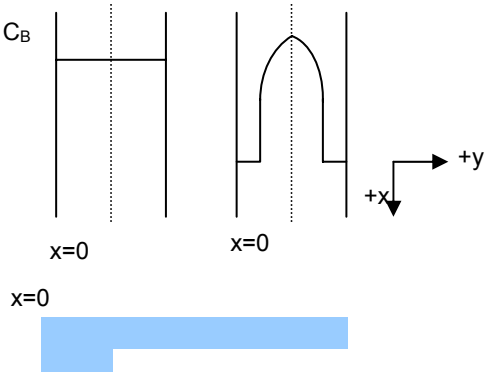

Figure 5-1: A uniform or symmetric doping profile about the center of the cantilever beam thickness results in no bending

However, under a concentration gradient, the beam will bend towards the more heavily doped boron side with respect to the center of the beam thickness to relieve the tension. This is a similar concept to applying a nitride strip on top of silicon, and it will be explored in the next section. For example, a doping profile located near the surface of the beam will bend upwards, while a profile located towards the bottom of the beam will bend downwards.

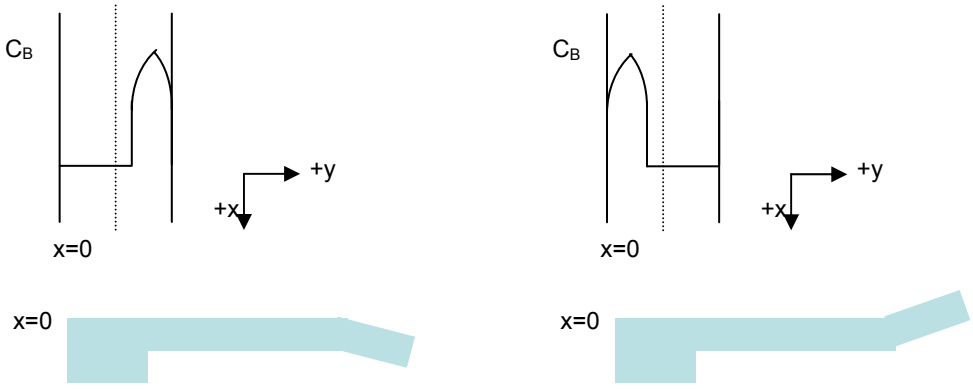

Figure 5-2: The strain from boron causes bending towards the more heavily doped boron side of the beam (a) downwards bending (b) upwards bending

5.1.1 Beam Bending Simulation Results

Simulations in FLOOPS were performed to observe how varying the length, width, and concentration gradient affected the deflection of the cantilever beam. The experimental conditions of Rueda et al. [Rue98] were replicated to obtain accurate results. A boron profile with a peak concentration of $8x10^{19}$ cm^{-3} was implanted into silicon. The initial beam dimensions were 50um long by 0.6um thick. The grid spacing was 0.05 um in the x-direction to resolve the boron profile, and 0.5um in the y-direction. The material properties used for silicon were: Young's Modulus =$1.22x10^{12}$ dyn/cm^2 and Poisson's Ratio=0.3 [Rue98]. The boundary condition requirement for cantilever beams is the displacement and the first derivative of the displacement (velocity) is equal to zero. To achieve this, the left side of the boundary was fixed.

5.1.2 Effect of Varying Beam Length

Figure 5-3 demonstrates the beam deflection versus beam lengths for a 0.6 um thick beam. As stated in equation (5-1), a beam with identical material properties will follow the same deflection curve. As the beam length was increased from 25 um to 50 um, the deflection increased accordingly and fit a parabolic curve. These results agree with those of Rueda et al. and Chu et al.

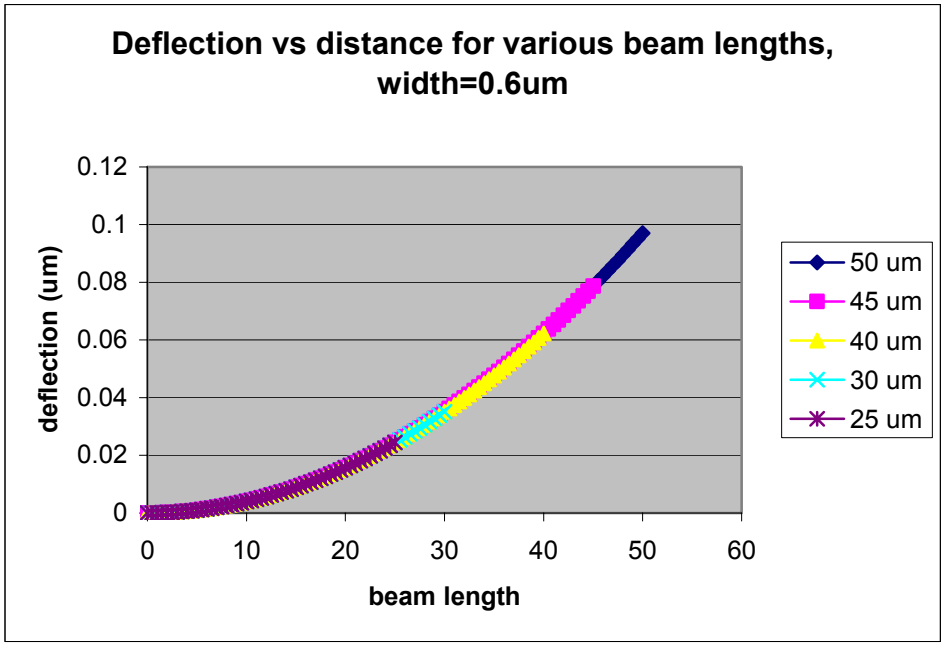

Figure 5-3: Beam deflection vs. beam length

5.1.3 Effect of Varying Beam Width

The next figure illustrates the effect of varying the beam width on the beam deflection. Notice the cantilever beams deflect in the negative-x direction, equating to an upwards bending as in Figure 5-2 (b). The beam width is varied from 0.6 um to 1.15 um and the deflection is observed. As anticipated, narrower beams deflect more than thicker beams. The deflections observed were in agreement with those of Rueda et al.

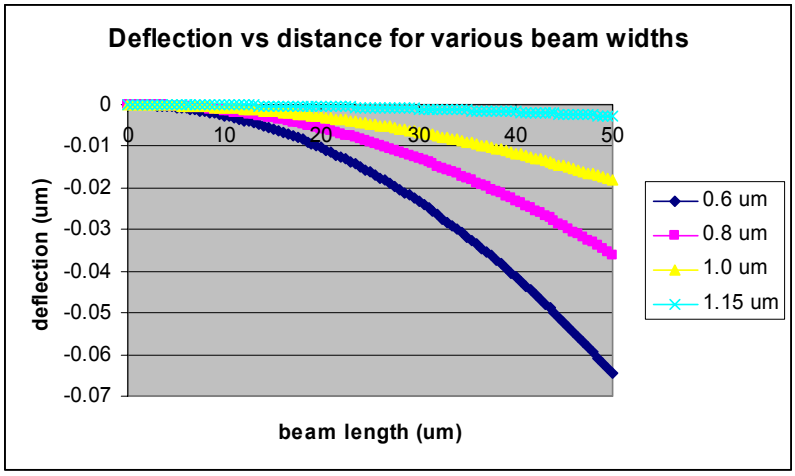

Figure 5-4: Beam deflection vs. beam length for varying beam widths

5.1.4 Effect of Varying Dopant Profile

The diffusion of boron in silicon is concentration dependent and is modeled by [Jae02]:

$$N(x,t) = N_p \exp-(\frac{x}{2\sqrt{Dt}})^2 \quad (5\text{-}2)$$

where N_p is the peak concentration in cm^{-3}, x is the distance in cm into the bulk of the wafer, D is the diffusivity of boron in silicon in cm^2/sec, and t is the time in seconds. The effect of varying the concentration gradient on beam deflection is shown below in Figure 5-5. For simulation purposes, the Dt factor was varied and the deflection of the beam was observed for a beam length of 50 um and width of 0.6 um. The beam with a larger boron distribution resulted in greater beam deflection.

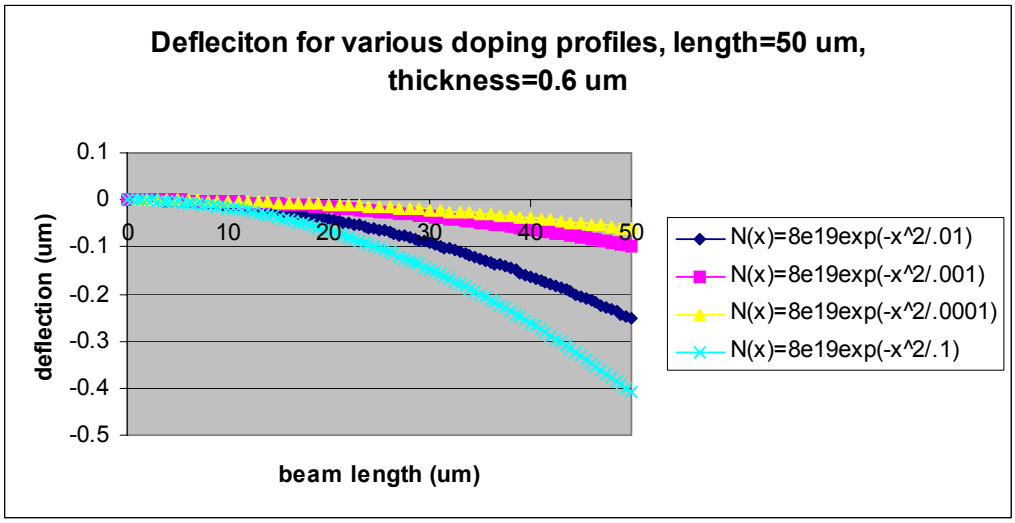

Figure 5-5: Beam deflection vs. beam length for varying doping profiles

5.2 Multiple Material Layer Bending Simulations

Due to its excellent mechanical properties, silicon nitride can be used for a variety of applications such as: a structural material to fabricate MEMS devices, isolation layers between transistors, masks for diffusion and etching, and recently, to induce uniaxial

tensile strain in the channel of NMOS transistors. Nitride is deposited by chemical vapor deposition typically around 700°C, and has a higher thermal expansion coefficient than silicon. If the resulting stress is below a certain threshold, the structure relaxes by distorting, and above the threshold it will generate dislocations. In equilibrium, the forces and moments between the silicon and silicon nitride must balance, creating a bending in the materials. The tensile residual stress in the nitride causes it to curl up at the edges, creating a pocket of tension near the edges of the silicon nitride/silicon interface, and compressive stress underneath the nitride. The bending behavior is illustrated in Figure 5-6 below:

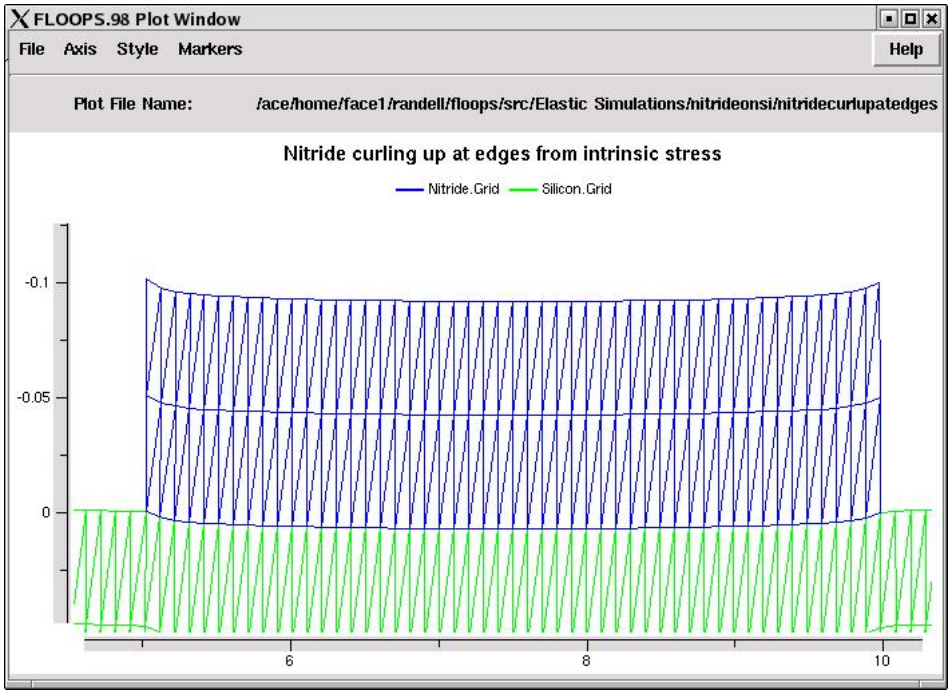

Figure 5-6: Nitride curling up at edges due to tensile residual stress

A functionality test was performed to ensure the multiple material layer structure behaved as expected. In FLOOPS, a region of silicon nitride was defined on top of a silicon region. The material properties used for each material were [Jae02]:

Table 1: Material parameters used for nitride on silicon simulations

	Young's Modulus	**Poisson's Ratio**
Silicon Nitride	$3x10^{12}$ dyn/cm^2	.25
Silicon	$1.22x10^{12}$	.3

In the first set of simulations, the nitride thickness was varied while the silicon thickness was kept constant at 10 um. Fixed boundary conditions were set at the bottom of the wafer, so a relatively thick substrate was selected to ensure that a small structure would not interfere with the bottom boundary. An intrinsic stress, approximately $1.6x10^{10}$ dyn/cm^2, was defined in the ***yy*** (channel direction) direction of the nitride. The bodyforce operator, discussed in Chapter IV, was used to provide the intrinsic stress in the nitride. By varying the elemental strain in the silicon nitride layer, an approximate value of the intrinsic stress can be computed. These stress values were compared with results from the ISE version of FLOOPS for the same simulation. When the stresses were equal, the elemental strain in the nitride was approximately equal to the intrinsic stress of $1.6x10^{10}$ dyn/cm^2. This is an unpractical way to provide intrinsic stress in a material layer and is discussed in the future work section of Chapter VI. The effect of varying the nitride thickness, while maintaining a constant silicon thickness, on wafer bending is illustrated in Figure 5-7. As the nitride thickness is increased, the structure curls up more appreciably due to a greater constant force distributed through the nitride layer.

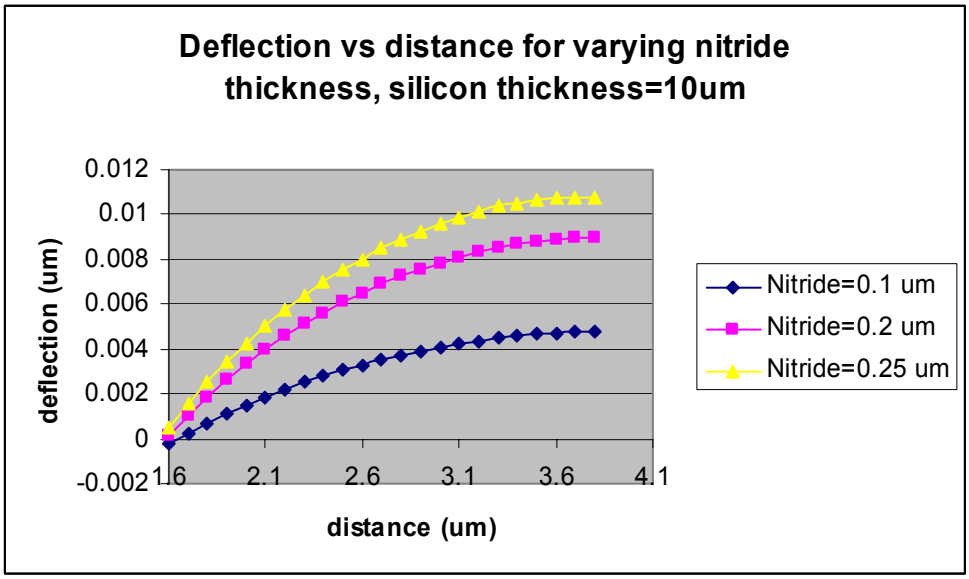

Figure 5-7: Deflection vs. distance for varying nitride thicknesses

Next, the effect of varying the silicon substrate thickness on wafer bending was observed. The nitride thickness was kept constant at 0.1 um, while the silicon thickness was varied. As the silicon thickness was decreased from 15 to 5 um, an increase in wafer curvature was observed as expected.

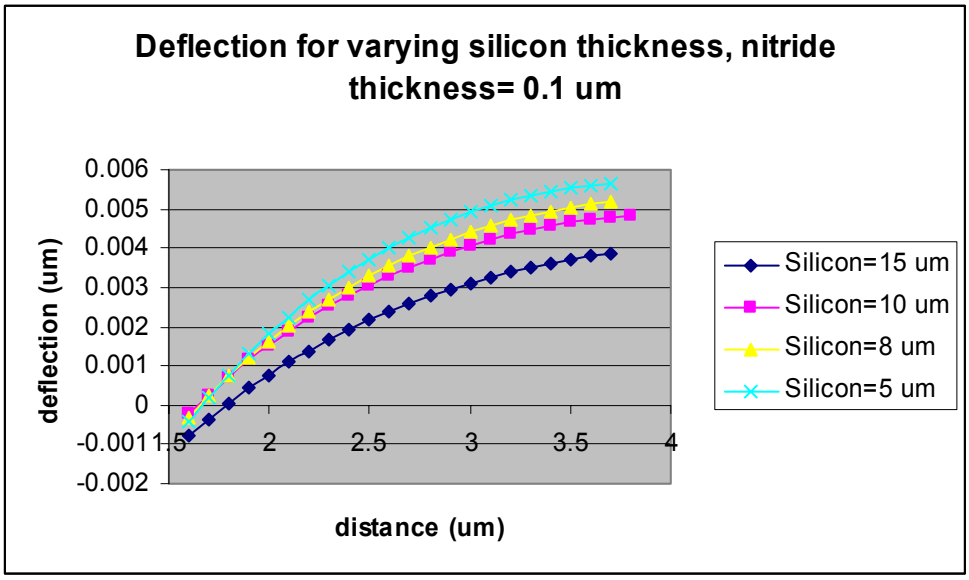

Figure 5-8: Deflection vs. distance for varying silicon thicknesses

The stress fields from the structure in Figure 5-6 are illustrated in Figures 5-9, 5-10, and 5-11. The lateral edges are not constrained and bottom boundary condition is used. The substrate is 20 um thick and the nitride is 0.1 um thick. The deposited nitride is assumed to be in tension. If the nitride extends over the entire substrate, minimal stress in the substrate would result since the substrate several orders of magnitude larger than the nitride. However the nitride is patterned and large stresses are generated in regions close to the edge, which is known as the "lift-off" effect, causing the edges to go into tension [Sen01]. The region below the nitride is pushed down in compression. The stress in the ***yy*** (channel) direction is larger than the ***xx*** (bulk) direction because the intrinsic stress in the nitride is defined in the ***yy*** direction. These results are in accordance with a similar simulation performed by Chaudhry [Cha96].

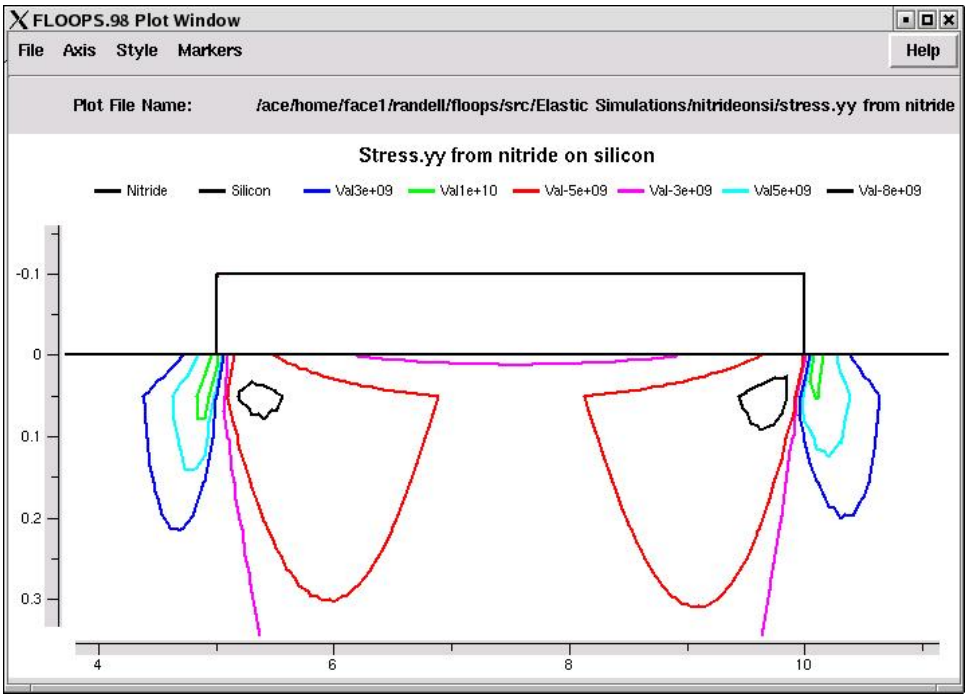

Figure 5-9: Stress.yy from silicon nitride on silicon

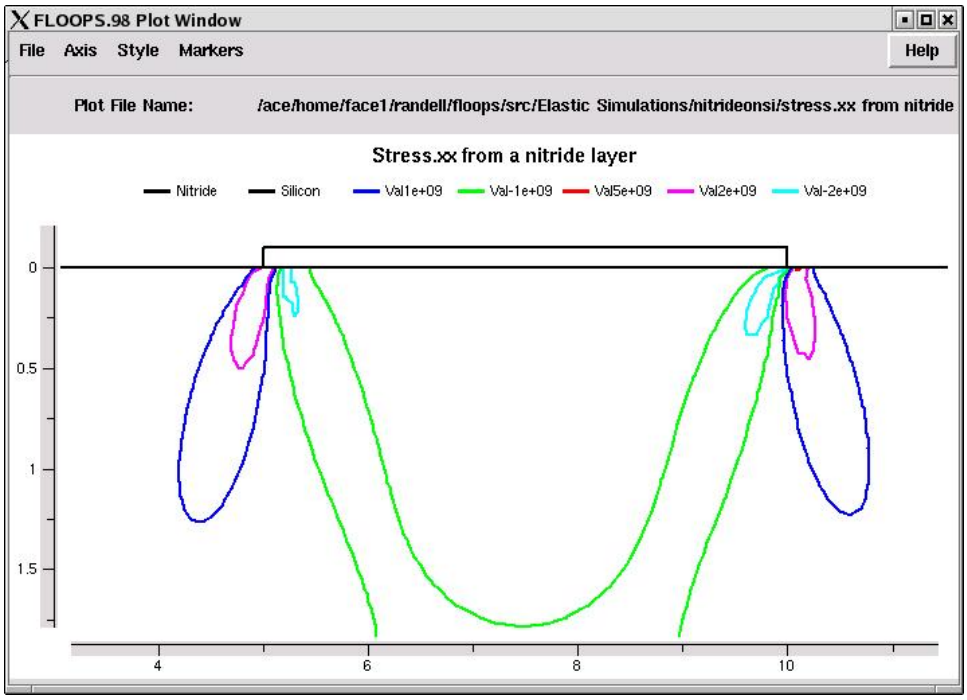

Figure 5-10: Stress.xx from silicon nitride on silicon

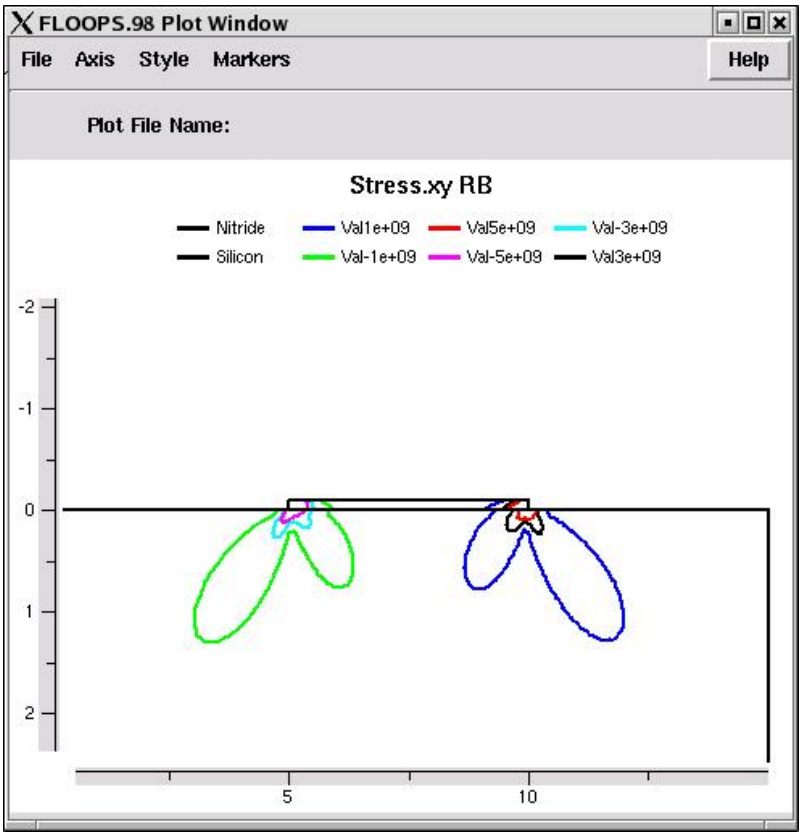

Figure 5-11: Stress.xy from silicon nitride on silicon

The shear components of stress have implications on bulk processing (dislocation loop glide and substrate yielding), thus it is of use to explore these stresses. The slip pattern in silicon for the <111> plane is the [110] direction, which corresponds to shear stresses. The contours of the ***xy*** simulations indicate that the shear stress lobes peak at approximately 45° and represent the area for dislocation loop glide. The contour is a double lobe because the shear stress is related to the polar coordinates as [Cha96]:

$$\sigma_z = (\sigma_r - \sigma_\theta)\sin 2\theta + \sigma_{r\theta}\cos 2\theta \cong \sigma_r \sin 2\theta \qquad (5\text{-}3)$$

In the experiments performed by Ross, dislocation loops from a nitride strip on silicon formed in the same region indicated by the stress contours. In simulation, Chaudhry also found lobes of the same shape to form on nitride strips in silicon.

Effect of Boundary Conditions on Stress Fields

Two different reflecting boundary conditions were simulated for the nitride on silicon structure to observe the overall shape of the stress contours. The reflecting bottom boundary condition and reflecting left and reflecting right boundary conditions were applied and the stress in the ***xx, yy,*** and ***xy*** directions are illustrated:

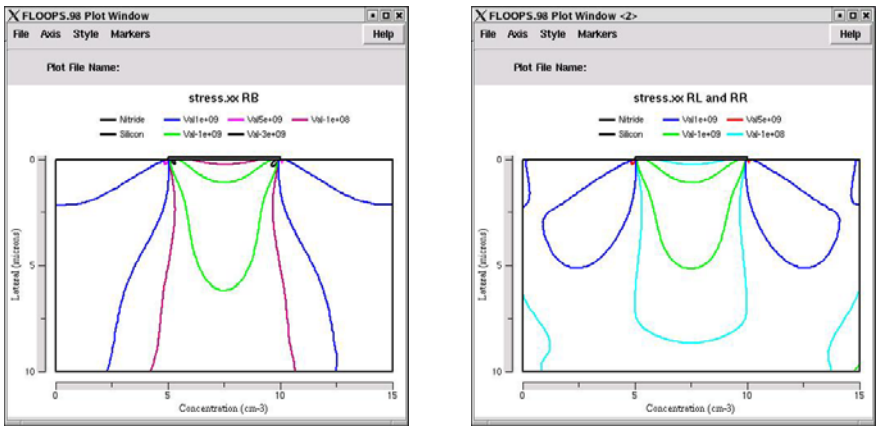

Figure 5-12: Stress xx for reflecting bottom (left) and reflecting left and right (right) boundary conditions

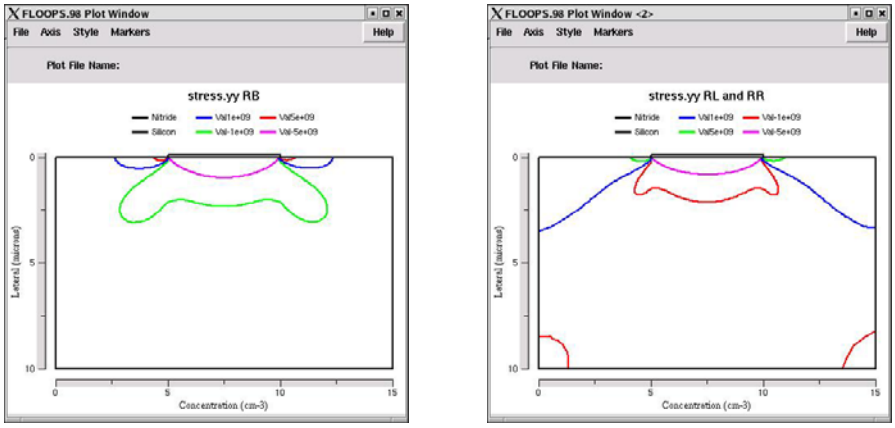

Figure 5-13: Stress yy for reflecting bottom (left) and reflecting left and right (right) boundary conditions

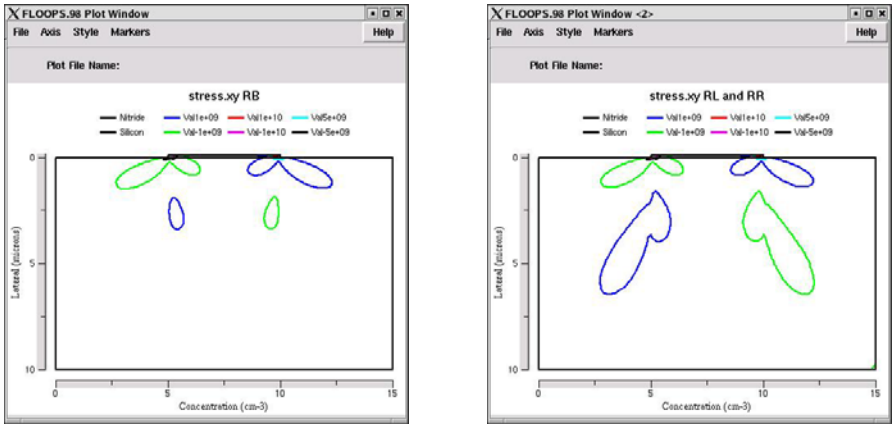

Figure 5-14: Stress xy for reflecting bottom (left) and reflecting left and right (right) boundary conditions

For the ***xx*** and ***yy*** stress simulations, stresses build up near the edges for the reflecting left and right boundary conditions. This would be expected because the left and right hand sides are fixed and there is no free surface for the stresses to relax. For the reflecting bottom ***xx*** and ***yy*** simulations, the compressive region underneath the nitride extends slightly lower than for the reflecting left and right boundary conditions. Overall, although the stress distribution for each simulation varies somewhat throughout the complete structure, the local stresses around the nitride/silicon interface are well-represented.

5.3 Channel Stress from Boron Source/Drain Doping

As discussed in Chapter IV and demonstrated in Section 5.1, boron doping introduces a local tensile strain in the substrate due to its size mismatch with silicon. The strain from the boron doping causes the silicon to warp and the deformations are used to calculate the resulting stresses in the substrate. While this phenomenon is beneficial for fabricating MEMS devices such as sensors and membranes, it can be deleterious to device operation as channel lengths are decreased below 100 nm.

Stress in the channel from doping the source and drain regions was a relatively insignificant factor until CMOS transistor channel lengths entered the nanometer realm. Consider a PMOS transistor doped with boron source drains. Boron is the p-type dopant of choice due to its high solubility limit in silicon; at 1100°C, boron has a solubility limit in silicon of $3.3 \times 10^{20}/cm^{-3}$ [Jae02]. Negatively charged dopants, such as boron, become more soluble under compressive stress, but the tensile stress induced from boron doping can counteract the desired compressive channel stress applied to increase hole mobility [Sad02]. For PMOS devices, tensile stress from boron incorporation as low as 100 MPa can compensate the intentional compressive stress engineered into the channel, resulting in a net close to zero stress. This example could be applicable for the compressive stress introduced from STI structures.

The bending behavior of a boron-doped silicon beam was properly calculated and compared with experimental data in Section 5.1. This technique is taken one step further and applied to a PMOS-like device; a silicon substrate and source/drain regions doped with boron. To observe the channel stress under varying process parameters, the stress at the center of the channel from boron doping in the source/drain region was observed. The channel length, source drain length, and boron concentration were varied to observe

scaling trends for different technology nodes. The finite element structure showing the parameters to be varied is illustrated in Figure 5-15.

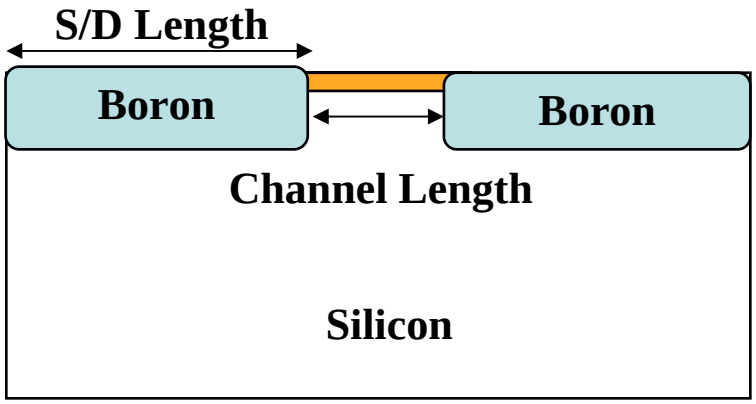

Figure 5-15: Silicon doped with boron source drain regions – general structure

5.3.1 Effects of Channel Length Scaling

The channel is used for carrier conduction and is defined as the region between the source and the drain; approximately 100 Å below the surface. The first structure simulated had a peak boron concentration of $2x10^{20}/cm^3$ in the source/drain regions, source/drain lengths of 1 um, and a junction depth of 0.12um. As the channel lengths were varied from 1 um to 45 nm, the stress at the center of the channel was observed. The results illustrate that as channel lengths decreased, the increased stress in the center of the channel approached exponentially. At a 45 nm channel length, approximately 80 MPa of stress exists from source drain doping alone. Due to the free surface at the top of the structure, the structure relaxes and deformed more than if a realistic PMOS device with a gate and spacers were present.

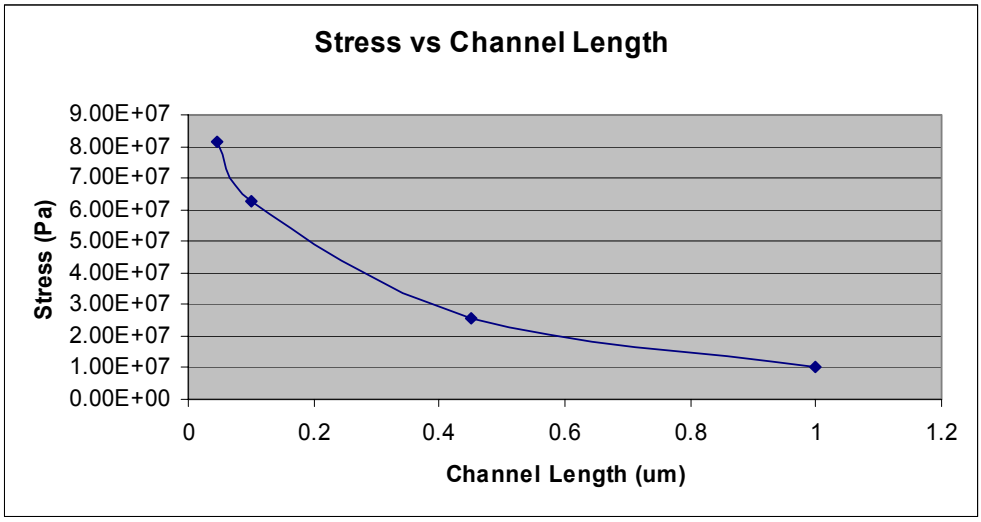

Figure 5-16: The effect of scaling channel length on stress from boron doping

5.3.2 Effect of Source/Drain Length Scaling

The length of the source and drain is determined by design rules specific to each technology, and is equal to 6 lambda, where lambda is half of the minimum feature size. The simulated structure had a peak boron concentration of $2x10^{20}/cm^3$ in the source/drain regions and a junction depth of 0.12um. As the source/drain lengths were varied from 0.3 um to 1 um, the stress at the center of the channel was observed. This was performed for both 45 nm and 100 nm channel lengths. For longer source/drain lengths, larger amounts of boron are available to pull on the channel, thus increasing the stress. This trend is shown in Figure 5-17.

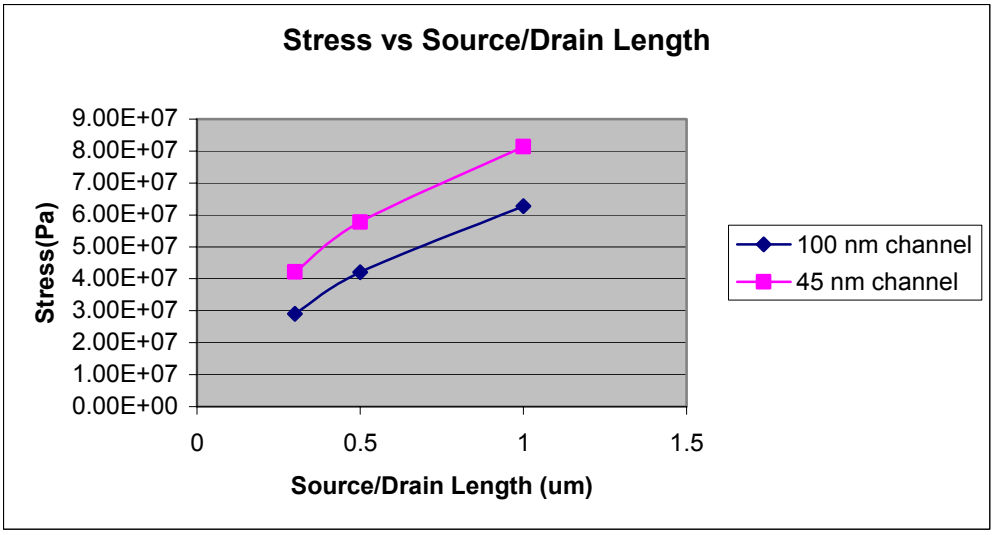

Figure 5-17: The effect of scaling the source/drain length on channel stress for 100 nm and 45 nm channel lengths

5.3.3 Effect of Boron Concentration Scaling

The effect of varying the boron concentration in the source/drain regions on channel stress was explored. Of all the factors affecting the stress in the channel, the boron concentration appears to have the largest influence on the channel stress. The simulated structure had a source/drain length of 1 um and a junction depth at 0.12 um. The boron concentration was varied from $6x10^{19}$ to $5x10^{20}/cm^3$, and the stress at the center of the channel was observed. Although boron is soluble in silicon up to approximately ~$3.3x10^{20}/cm^3$, it is soluble at larger concentrations in silicon germanium. For 45 nm and 100 nm devices, the stress in the channel approaches 100 MPa at concentrations above $2.5x10^{20}/cm^3$ and $3x10^{20}/cm^3$ respectively.

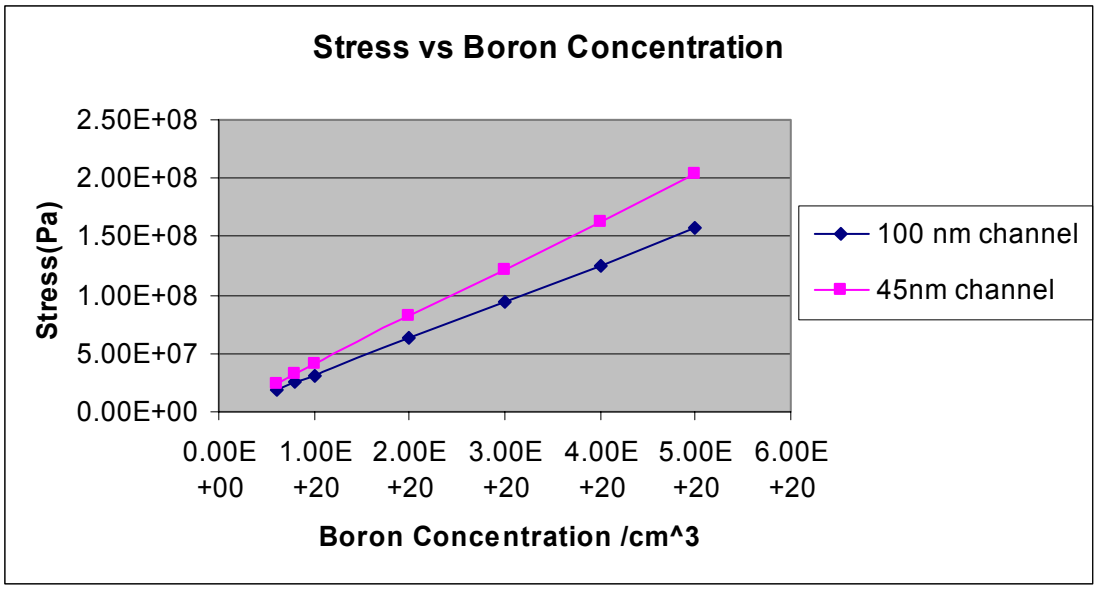

Figure 5-18: The effect of scaling the source/drain length on channel stress for 100 nm and 45 nm channel lengths

5.4 Summary

As the semiconductor industry enters the nanometer realm, stress from sources that were given little recognition in the past are becoming significant such as: stresses from STI structures, film deposition, and dopants. This chapter provided results regarding the stress from boron doping and the stress from nitride deposition. Boron is the main dopant for PMOS transistors due to it high solid solubility limit in silicon, however at large concentrations and small device dimensions, the presence of boron can alter intentional stress placed in the channel for carrier mobility enhancement, as well as introducing unintentional stress in the wafer.

Boron-doped cantilever beams were simulated to demonstrate the effect of boron doping on beam deflection that resulted from a non-uniform doping profile. The simulation setup was identical to that of Rueda et al., and the bending behavior results were in accordance. The beam length and width dictated the amount of beam deflection. Shorter, thicker beams deflected less than longer, thinner beams with identical boron

diffusion profiles. Beams with larger boron concentrations or wider diffusion profiles deflected more than beams with lower concentrations, or steeper diffusion profiles.

Next, the stress from depositing a strip of nitride on silicon was observed. The intrinsic stress of approximately $1.6x10^{10}$ dyn/cm^2 in the longitudinal direction is the main source of stress in nitride. As the edge regions of the nitride curl up, the silicon to curls up as well. This known behavior creates significant stress in the [110] direction. Tensile lobes are observed at the silicon nitride/silicon interface, and large compressive stresses are observed underneath the nitride film. Different boundary conditions were also simulated to investigate how the stress distributions differ throughout the structure. Although the stress distribution throughout the entire structure varied slightly, the local stresses around the nitride on silicon structure were approximately equal. Stresses built up more along the sides of the structure with fixed left and right hand side boundary conditions, as expected.

Table 2: Results summarizing the effect of boron doping on channel stress

Parameters varied	**Effect on Stress**
Channel Length	As channel length decreased, stress in the center of the channel increased
Source/Drain Length	As source/drain length decreased, stress in the center of the channel decreased
Boron Concentration	As the boron concentration increased, the stress in the center of the channel increased

Lastly, the effect of stress in the channel from boron doping was examined. The channel length, source/drain length, and boron concentration were varied and the stress at the center of the channel was quantified. Above is a table summarizing the results:

Increasing the boron concentration appeared to have the most significant effect on increasing the stress in the channel. For concentrations greater than $2.5x10^{20}/cm^3$ for 45 nm channel lengths and $3x10^{20}/cm^3$ for 100 nm channel lengths, the stress in the channel was greater than 100 MPa. In chapter IV, a summary of each chapter will be presented, and future work will be discussed.

CHAPTER 6
SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Summary and Conclusions

In this thesis, many important sources of stress in silicon technology have been investigated. Finite element code was implemented in FLOOPS to develop a two-dimensional model for dopant induced stress in the silicon substrate. The model was verified with experimental data when possible, and was compared to simulation data otherwise.

In Chapter I, a survey of existing literature on stress applications in silicon technology and driving motivations for studying stress was discussed. Stress-induced defect formation from patterned structures was quantified by experimentation and through simulation. Next, strained silicon was introduced because this work will have many future implications in this area of research. Applications of how the advantageous stress enhances device performance and how the unintentional stress hinders device performance were exemplified.

Chapter II introduced the concepts of stress, strain, and linear elasticity. Examples of normal and shear stresses were presented. Stress from patterned films are commonly encountered in IC fabrication, and understanding the stresses generated as a result of deposition are important. Examples are provided to describe the plane stress that results due to a thin film on a thick substrate.

Chapter III discusses various unintentional stress sources that arise during semiconductor fabrication processes such as STI formation, film deposition, and dopant

induced stresses. Non-planar oxidation, thermal mismatch, and intrinsic stresses all accumulate in and around the STI structure to contribute to the total stresses. In addition to STI formation, variations in the deposition process of thin films can affect the magnitude and amount of residual stress in the film and substrate.

Next, stress from dopants and dislocation loops, and stress assisted diffusion was discussed. Since boron is smaller than silicon, it contracts the silicon lattice and creates a local tensile region. Germanium, on the other hand, is larger than silicon and creates a lattice expansion. Due to dopant incorporation, the silicon will distort to relax the stress. This was demonstrated in Chapter V in the beam bending simulations. If the stress in the substrate is too high, it will yield by generating dislocations. Dislocation loops form as a result of high shear stresses in the {111} plane and can glide in the [110] plane if the critical glide stress is exceeded. Lastly, stress assisted diffusion of boron in silicon and silicon germanium was discussed. A possible explanation to boron diffusion retardation in silicon germanium is attributed to the boron-germanium binding.

Chapter IV focuses on the software enhancements in FLOOPS to calculate the displacements and stresses in the silicon substrate due to boron doping. The finite element method was implemented using the 2-D plane strain equation to create the "elastic", "bodyforce", "strain", and "stress" operators. The equation to be solved is essentially f=kx, where f is the force from the dopants, k is the stiffness, and x is the resulting displacements. The "elastic" operator was developed to find the stiffness (k) of the silicon mesh, and the "bodyforce" operator equated the strain from boron doping into an elemental force (f). The matrix equation was solved, and the resulting displacements were transformed into strains and stresses through the "strain" and "stress" operators.

The linear elastic model was also integrated with the property database and process commands.

Chapter V provided applications and results to the beam bending, nitride deposition, and PMOS-like structure simulations. A beam bending experiment was performed to observe the effect of strain from boron doping. The beam length, thickness, and doping profile were adjusted independently and the bending behavior was observed. Due to the non-uniform boron doping profile in the beam, the beam will bend upwards towards the tensile region to relieve the stress. Larger deflections resulted from longer beam lengths, thinner beams, and wider diffusion profiles. The simulation values agreed with those of Rueda.

Next the stress from a nitride deposition was simulated by applying a constant force to the nitride layer and equating the force to an intrinsic stress. Stress contours were compared with ISE FLOOPS, and when the substrate stresses were equivalent, the proper intrinsic stress of 1.6x1010 dyne/cm2 was defined in the nitride. These results were comparable to the simulation of Chaudhry as well. Two different boundary conditions reflecting bottom, and reflecting left and right were simulated to observe the xx, yy, and xy stress in the silicon substrate from nitride deposition. Although the stress contours varied slightly throughout the structure, the local stresses around the nitride/silicon interface were approximately equal for both boundary conditions. It was concluded that the different boundary conditions did not have significant effect on the stress simulation results.

Finally, the stress in the center of the channel due to boron doping in the source drain was investigated. Since the boron atom is smaller than the silicon atom, it exerts a

local tensile stress in the substrate which is transferred to the channel. In PMOS transistors, where boron is used as the source/drain dopant, enough tensile stress could counteract the advantageous compressive stress that is engineered into the channel for mobility and overall performance enhancements. To calculate these stresses from boron doping, a PMOS-like structure that consisted of bulk silicon with boron source/drain regions was simulated. Factors such as channel length, source/drain length, and boron concentration were varied to assess the channel stress. The results showed that decreasing the channel length, increasing the source/drain length, and increasing the boron concentration all resulted in larger stresses in the channel region. Increasing the boron concentration appeared have the largest effect in generating larger stresses. In a real device however, the resulting stress most likely will be larger due to all factors scaling together.

6.2 Recommendations of Future Work

Some of the important sources of stress in semiconductor fabrication technology have been analyzed and modeled as part of this thesis. The emphasis of this work was to develop a more accurate method to calculate stresses in the silicon substrate due to dopant incorporation using software, and to demonstrate functionality through simulations. As each technology node demands smaller feature sizes, very precise models will be necessary to predict device behavior. The work described below provides recommendations that will further enhance the capabilities that were implemented into FLOOPS.

6.2.1 Additions to Software

The software operators that were implemented into FLOOPS accurately simulate the stress from dopant incorporation. However, to quantify the total stress in a CMOS

structure, multiple stress sources must be accounted for. After the stress sources are properly modeled, boundary conditions need to be optimized for each stress source. The first work to be completed is to link the mechanical stress code with the solution to the diffusion equation. To solve the diffusion equation, derivatives with respect to the solution (displacement) must be computed. This entails developing code to calculate the derivatives of the "bodyforce," "strain," and "stress" operators.

Next, stress sources such as stress from dislocation loops, thin film deposition, thermal mismatch, oxide growth, and STI stress must be taken into account. These additional stress sources are right hand side components, like the stress from boron doping and represent the force components (f) in the elastic equation f=kx. Since each type of stress is unique, an operator to compute each stress source is required. After the operators are developed, adding the stress sources together to calculate the total stress of the system can be performed using tcl scripts.

The stress from dislocation loops should be relatively easy to incorporate because it is the same principle used in the stress from boron doping. The dislocation loops are treated as a strain induced by a change in the lattice parameter from introducing extra atoms into the lattice. The relationship describing the depth dependent number of atoms due to loops of radius, R, is [Cha96]:

$$N_{ALL}(x) = 2 \cdot D_{110} \cdot \int_{X}^{R_{\max}} f_D(R) \cdot \sqrt{R^2 - X^2}\, dX \qquad (6\text{-}1)$$

where D110 is the density of silicon atoms in the {110} plane and X is the distance from the center of the loops. The finite element method computes the strain due to the loops as:

$$\varepsilon_{xx0} = \frac{N_{All}(x)}{5.02x10^{22}} \tag{6-2}$$

This strain is converted into a force, and subsequently into a stress using the same method performed from boron doping in silicon.

In Chapter V, the stress from a thin strip of nitride deposited on a thick silicon substrate was calculated and the stress contours were compared with simulation values from ISE FLOOPS. However, the intrinsic stress in the nitride was modeled by applying a constant strain using the "bodyforce" operator, which converts a strain (application was for strain from boron doping), into a force. Next the "stress" operators converted the constant force into a constant stress value (the intrinsic stress of nitride). Though it provided the correct solution, it was a complicated method to model the intrinsic stress. The main purpose of this simulation was to further verify that the software had the ability to accurately calculate stress from a force.

For an initial implementation, only the yy stress component will be included. For planar thin films, intrinsic stress is specified at the nodes parallel to the deposition direction. However over non-planar surfaces, simulating the deposition process is more complicated, which makes calculating stresses more difficult. Around the non-planar surface, the stresses are translated from the planar system axis to the axis perpendicular to the normal of the growing film. The stresses at the non-planar nodes then must be averaged with their neighboring elements [Rue97]. This is illustrated below in Figure 6-1.

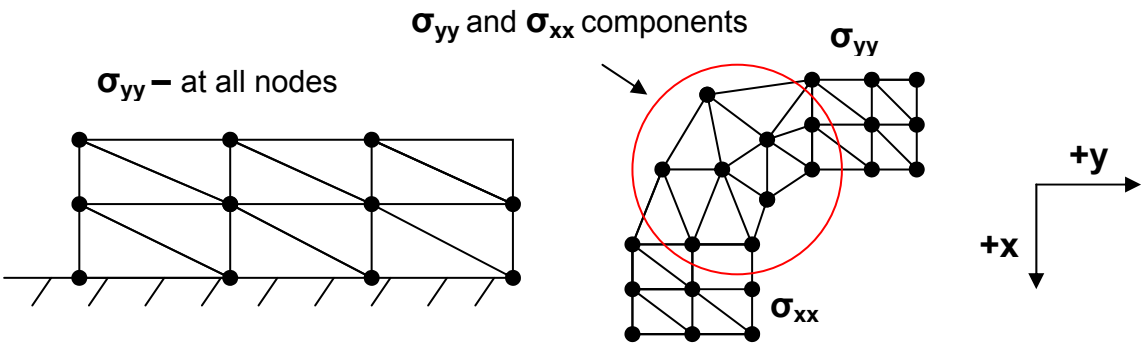

Figure 6-1: Intrinsic stresses are oriented parallel to the interface on which the film is grown or deposited (left) planar film, (middle) non-planar film [Rue97].

Computing the thermal mismatch stress can be invoked on the command line, or using tcl scripts. The thermal mismatch stress is calculated by multiplying the difference in thermal expansion coefficients of the two materials by the temperature difference (i.e., deposition temperature and room temperature).

Oxide growth is currently treated as a viscoelastic material that flows at high stresses and temperatures. This is valid for large amounts or long oxide growth steps, which are typically not employed for current fabrication processes. Large oxide growth was once important for LOCOS formation, but trench isolation has taken over due to the lower stresses generated. For process steps such as trench isolation, oxide is typically deposited in thin layers, and acts more like an elastic material. Adding this stress source is not as straight forward because the growth kinetics of oxide under stress is different than in an unstressed material. In addition, computing the oxide growth forces in non-planar topology must be accounted for.

Boundary conditions are defined on the external edges of each material, and different boundary conditions will finite element simulations. Chaudhry demonstrated the effect of different boundary conditions on dislocation loop stress [Cha96]. In the work presented in this thesis, reflecting boundary conditions were implemented to

investigate the effect of fixing the left and right, or bottom side of the finite element mesh. A reflecting boundary simulates mirror symmetry by setting the normal velocity and displacement field equal to zero at the boundary. Reflecting boundary conditions are illustrated in Figure 6-2 for all edges except for the top surface which is free to relax.

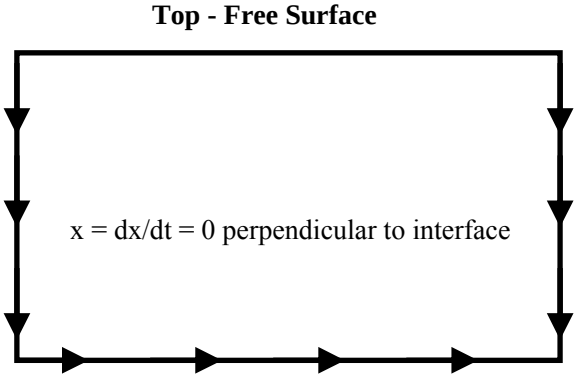

Figure 6-2: Reflecting boundary condition – displacement and velocity perpendicular to the interface is set to zero, but can have vertical movement. Top surface is free to relax.

For a diffusion simulation, this would imply that no diffusion can occur across the interface, or for a stress simulation, the forces across the interface are equal to zero. In this work the displacement solution is two-dimensional, having x and y displacement values. Currently, when a reflecting boundary condition is applied, both the x and y values are simultaneously fixed at the same node. Future enhancements could include decoupling the x and y coordinates by allowing one coordinate to deform while the other remains fixed. Other boundary conditions, such as Dirichlet and periodic boundary conditions can be tested to obtain more accurate stress simulation results. The Dirichlet boundary conditions states that the value of the solution is defined on the boundary of the solution domain. The periodic boundary condition is similar to the reflecting boundary condition in that one lateral edge demonstrates mirror symmetry by setting the normal component of the displacement and velocity to zero along the boundary, while the other

lateral edge is allowed to move by a constant distance, thus restricting all nodes to the same value of normal displacement [Cha96].

Before simulating an entire transistor structure, stresses after each process step need to be calibrated with experimental data and model parameter fitting. In conjunction with properly modeling all of the stress sources, optimization of boundary conditions will allow for more accurate MOSFETs models in the future.

6.2.2 Stress-Dependent Diffusivity Model

SiGe and strained silicon have been identified as alternative materials to help extend Moore's Law for years to come. To update and incorporate new models, knowledge of how stress will affect dopant diffusion is essential. It is known that boron diffusion is enhanced under tensile stress and retarded under compressive stress. The exact mechanisms governing boron diffusion in SiGe have been speculated, but are still unknown. Zangenbeg et al. confirmed that macroscopic strain does contribute to dopant diffusion. His studies showed that boron diffusion was enhanced by a factor of 2 in strained silicon, and decreased by a factor of 2 in Si0.88Ge.12 and by a factor of 4 in Si0.76Ge0.24 [Zan03]. Another theory of retarded boron diffusion in SiGe is the Ge-B pairing. The local tensile strain from boron and local compressive strain from Ge will attract one another to relieve the stress [Cro04, Kuo95]. The diffusivity enhancement and retardation of boron under relaxed, tensile, compressive stress is shown in Figure 6-3.

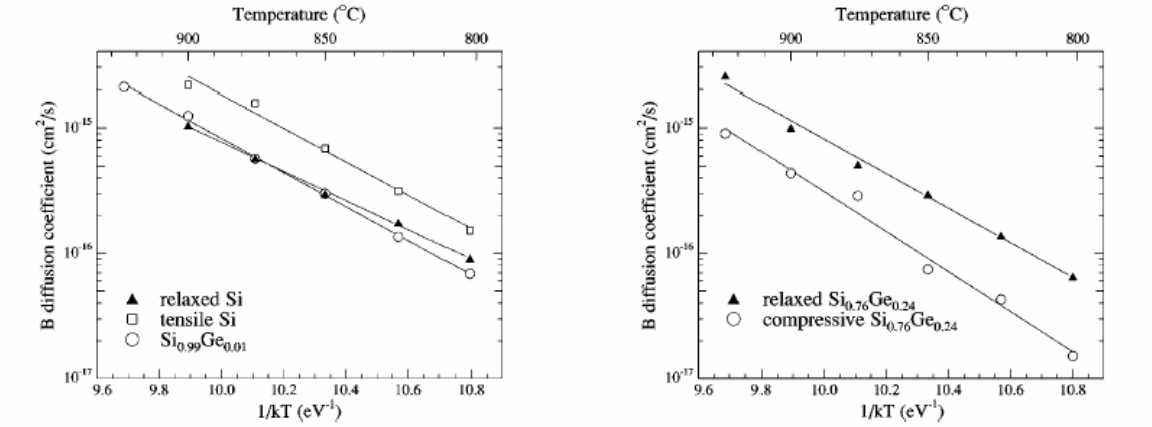

Figure 6-3: Diffusion of B in (left) relaxed Si, tensile Si, and $Si_{0.99}Ge_{0.01}$ and (right) diffusion of B in strained and relaxed $Si_{0.76}Ge_{0.24}$ [Zan03].

6.2.3 STI Induced Stress Modeling

As channel lengths decrease, stress sources such as STI have demonstrated a uniaxial compressive stress in the [110], or channel direction of MOSFETs. As a result, scaling devices introduces another method of channel engineering without having to modify the existing fabrication process. However, the source/drain regions are also in closer proximity to the channel, and for bulk silicon PMOS devices, the tensile strain from boron (without SiGe source/drains) can counteract the advantageous compressive stress from the STI, reducing the performance enhancement. It was demonstrated in Chapter V through simulation, that the strain from boron doping in silicon is significant enough to affect the channel stress for both 100 nm and 45 nm channel lengths.

The STI-induced stress can be tailored by the geometry of the structure. Shah demonstrated through simulation the effect of transverse stress on STI width, depth, active area width, and STI topology. Wider trenches for the same active area length exhibited higher channel stress. For STI depth, he observed that there was an optimal depth at which the maximum compressive stress in the channel could be achieved. Depths greater or shallower than this critical value resulted in a sharper roll-off of the

stress in the channel. Raised STI structures demonstrated larger stresses than recessed structures due to the enhanced stresses associated with non-planar surface topology. A caveat with these finding is that the STI stress was only defined in the transverse region, however the intrinsic stress is defined in both the transverse {1-10} and out-of-plane {001} regions. Though simulations need to be performed which take into account the intrinsic stress in both directions, these results are very promising to bringing us one step closer in understanding STI stress affects at nanometer channel lengths.

It has been long known that longitudinal uniaxial compressive stress enhances hole mobility, but degrades electron mobility, whereas transverse tensile stress improves both types [Smi54, Tho04a]. A technique that is currently being explored to improve CMOS devices is the HARP STI process. After a standard STI is fabricated, the HARP process densifies the trench structure, creating a moderate to high transverse tensile stress [Tho05b]. The mechanisms governing the stress magnification are not completely understood, thus methods to properly model this behavior would enable a more fundamental understanding of this phenomenon. An example application would be to investigate the effect of stress superposition for enhanced device performance. A tensile nitride capping that induces a uniaxial tensile stress in the channel is incorporated into NMOS devices to increase electron mobility. Intel uses SiGe source/drains and IBM uses compressive nitride capping layers to induce a uniaxial compressive stress in the channel to increase hole mobility. Could the transverse tensile stress induced from the HARP process that enhances mobility in both devices be added to the advantageous longitudinal stresses to enhance device performance further [Tho05b]?

6.2.4 Modeling Silicon at the Elastic/Plastic Limit

As we continue to decrease the physical dimensions of semiconductor devices, many different processing techniques are being explored to meet the requirements of the International Technology Roadmap for Semiconductors (ITRS). An area of active research is how stress affects material properties and device performance. Phen investigated this phenomenon with a wafer bending experiment by placing ultra-thin silicon wafers preamorphized with Ge and implanted with boron in tension, compression, and under no stress. The samples were annealed and the activation and defect densities were observed under each condition. Hall measurements indicated there was little difference in activation at low temperatures, and TEM indicated larger defect densities for the compressed layers [Phe04]. However, to successfully conduct theses studies, it is critical that the stress at the surface of the samples is below the yield strength of silicon to avoid plastic deformation.

Yield strength of a material is dependent on the amount of stress applied, the processing temperature, and the amount of time the sample is stressed. Thus, to increase the stress that a sample is subjected to, one of the other parameters will have to be decreased to avoid deforming the material by slip.

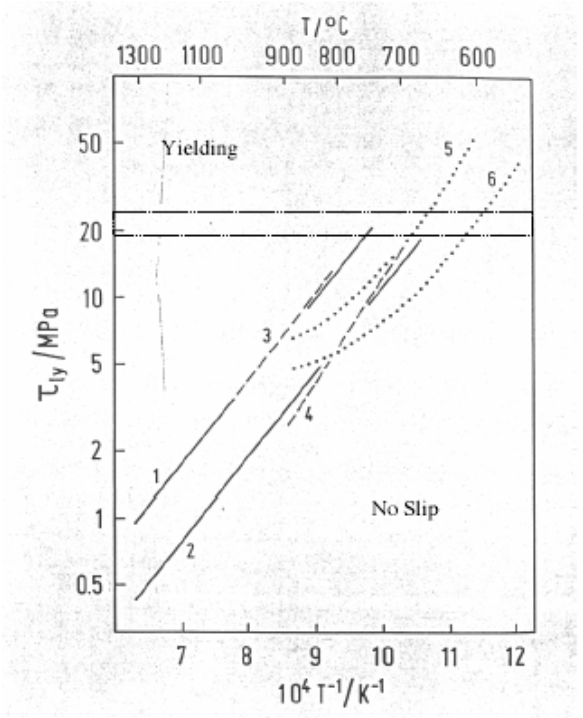

Figure 6-4: Yield point reduction as a function of temperature.

The yield strength of silicon is over 100 MPa at 500°C, but drops to approximately 10 MPa at 1000°C. Rabier et al. found the limit of elasticity in silicon is limited by a thermal budget of 750°C for 10 min at a stress of 100 MPa [Rab00]. This creates large challenge for performing high temperature studies below the plastic deformation limit. Phen's results of the elastic/plastic limit for silicon under various temperatures are illustrated in Figure 6-5.

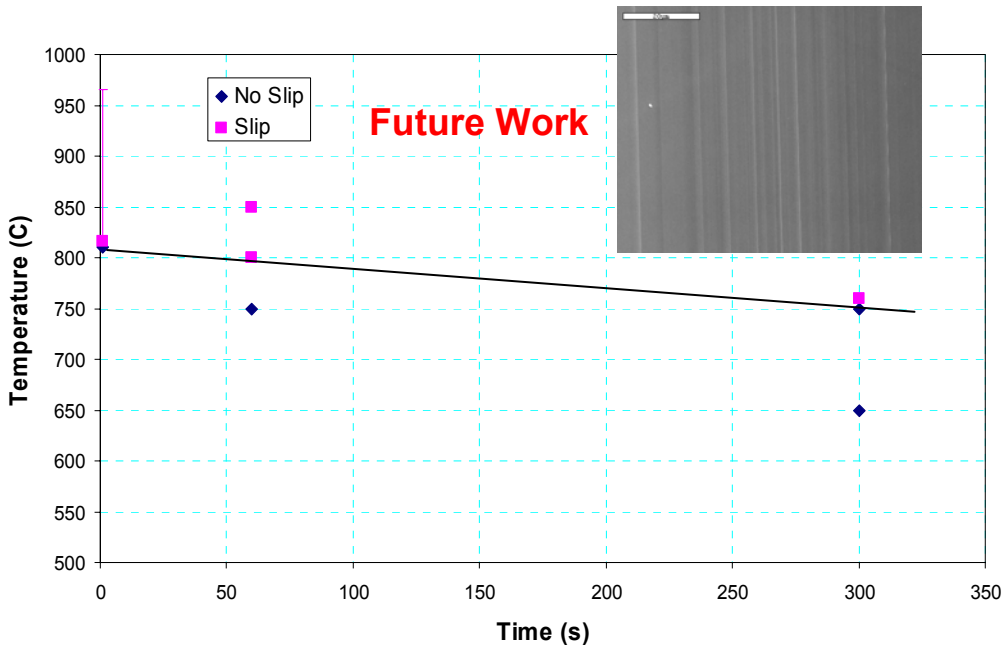

Figure 6-5: Regime of elastic/plastic deformation of silicon for various temperatures and times under 110 MPa stress [Phe04].

The work presented in this thesis allows silicon to be modeled in the elastic regime, but the elasticity of silicon ceases to exist at higher temperatures under a given stress, as described above. Thus, modeling silicon in the non-linear plastic regime would be beneficial because it will cut down on the technology development time and cost of running many experiments. In addition, experimental data for silicon that has undergone plastic deformation is readily available for instant calibration.

APPENDIX A
CODE APPENDIX

The code in this appendix was either modified from its original author, Dr. Mark E. Law, or written by Heather E. Randell. Each file will specify if the code was written or modified.

EleInfo.h

The Nind and Sind functions are used to access the node numbers (0-2) and the solution number (0-1) respectively For the Sind function 0 represents the x solutions, while 1 represents the y solution. Each function takes in an integer (0-5) to represent 3 nodes * 2 positions per node. The output of Nind and Sind are shown below.

Node Number	Nind	Sind
0	0	0
1	0	1
2	1	0
3	1	1
4	2	0
5	2	1

```
int Nind(const int i) const { return i / ns; }
int Sind(const int i) const { return i % ns; }
```

Expr.cc

The Expr class is the base class for all types of expressions. A few examples are: SumExpr which performs the addition and subtraction function, PrdExpr which performs the multiply and divide function, SolExpr which is a solution reference, PowExpr which handles exponents, and DiscExpr which handles discritizable functions. The functions below are defined for many of the expressions, in addition to the expressions listed above. They will be defined in more detail in Spatial.cc, where the body of the function originates. After the function is evaluated in Spatial.cc, if the values of the stiffness matrix are not already stored, it is passed in as an argument and the location of its values are stored.

```
StaticColumn &Expr::EleEvaluate( ElementInfo &ev ) {
int i, k;
if ( !nodestore ) FLPS_panic("retrieving cached answers when they are   unavailable");
        int cached = this->Column0Cached(ev);
        if ( !cached && nodestore ) {
                for(i = 0; i < ev.Size(); i++) {
                        VectorStatic &v0( se0->Val(i) );
                        for(int k = 0; k < ev.VecLen(); k++)
                                v0[k] = v[ev.node(i,k)->Index()];
```

```
                                                    }
                                                }
                                            return *se0;
                                    }
StaticColumn &Expr::EleInside( ElementInfo &ev ) {
int i, k;
if ( !nodestore ) FLPS_panic("retrieving cached answers when they are unavailable");
   int cached = this->Column1Cached(ev);
   if ( !cached && nodestore ) {
         for(i = 0; i < ev.Size(); i++) {
                  VectorStatic &v0( se1->Val(i) );
                  for(int k = 0; k < ev.VecLen(); k++)
                           v0[k] = v[ev.node(i,k)->Index()];
                                                    }
                                            }
                           return *se1;
                           }

StaticMatrix &Expr::EleDeriv( ElementInfo &ev ) {
int i,j,k;
FLPS_panic("retrieving cached answers when they are unavailable");
int cached = this->MatrixCached(ev);
if ( !cached && nodestore ) {
         for(i = 0; i < ev.Size(); i++) {
            for(j = 0; j < ev.Size(); j++) {
                  VectorStatic &v0( sd->Val(i,j) );
                  if ( i == j )
                     for(int k = 0; k < ev.VecLen(); k++)
                           v0[k] = v[ev.node(i,k)->Index()];
                           else
                           v0 = 0.0;
                                                    }
                                                }
                                            }
                           return *sd;
                  }
```

Genpde.cc

Genpde.cc contains the routines that allocate space, and numbers the nodes for the multidimensional displacement solution. This code was modified from its original Author, Dr. Mark E. Law.

```
void GenericPDE::SetEqnMap( ElementInfo &ev, EqnMap &stf ) {
if ( sid->isDimension() ) ev.SetSolDim( m->dimension() );
//get and set equation numbers....
IntData &e = sol->EqnNum();
IntBlock e1;
e1.ReSize(ev.VecLen());
//for each node, initialize the equation numbers
for(int j = 0; j < ev.Size(); j++) {
        ev.SetCur(j);
         for(int i = 0; i < ev.VecLen(); i++)
                e1[i] = sol->EqnNum( ev.Sind(j) ).get(
                *ev.node(j,i) );
                 stf.SetIntRow( off, j, e1 );
                                        }
                                }

void GenericPDE::VectorElement( ElementInfo &ev, EqnMap &stf ){
int i, j;
if ( sid->isDimension() ){
        ev.SetSolDim( m->dimension() );
        else ev.SetSolDim(1);
                }
if ( ev.type() == NODE ) {
        FLPS_panic("GenericPDE::VectorEdge called with non-edges");
   }
if ( Eeq->IsEmpty() ) return;
stf.SetSteady();
StaticColumn &r = Eeq->EleEvaluate( ev );
for(i = 0; i < ev.Size(); i++){
        stf.Sumrhs( off, i, r.Val(i) );
        }

//get derivatives...
ExprIter ei( Eder );
while( ei++ ) {
int oa = ei.cursign();
StaticMatrix &r = ei.current().EleDeriv( ev );
for(i = 0; i < ev.Size(); i++) {
        for( j= 0;  j< ev.Size(); j++) {
                stf.SumBlock( r.Val(i,j), off, oa, i, j );
                VectorStatic &ref = r.Val(i,j);

                                }
                        }
                 }
```

```
        }

int GenericPDE::NumberNode( Node &n, const int ne ) {
int i;
int length = 1;
int nodecount=0;
if ( sid->isDimension() ) {
        length = m->fieldserver().dimension();
        }

int assign = ne;
for( i = 0; i < length; i++ ) {
        if ( sol->EqnNum(i).get(n) != 0 ) continue;
        assign += 1;
        NodeIter ni( n.location().nodes() );
        while( ni++ ) {
                if ( sid->isContinuous() ){
                sol->EqnNum(i).set( ni.current(), assign );
                } //sets equation number at each node

                if ( ni.current().mesh().mater() == m->mater() ){
                sol->EqnNum(i).set( ni.current(), assign );
                } //sets equation number at each node
        }
Coordinate &c=n.location();
cout << "Node location" << " "<<"x=" << c.x() << " " <<"y=" << c.y() <<" " <<
"equation number = " << sol-
EqnNum(i).get(n) <<  endl;
                }
return assign;
}
```

Spatial.cc

The file contains the routines for the “elastic,” “bodyforce,” “stress,” and “strain” computations to compute the displacements and stress due to boron doping. This code was developed by Heather E. Randell. DiscExpr::ElasticEval computes the stiffness matrix of an element. DiscExpr::BodyForceEval computes the forces from boron doping. DiscExpr::StrainEval converts the forces from boron doping into strain values, and DiscExpr::StressEval converts the forces strains into a stress component.

```
void DiscExpr::ElasticEval( ElementInfo &ev ) {
double x0;
double y0;
double x1;
double y1;
double x2;
double y2;
double C[6][3];
double stiffness[6][6];
double Bmatrix[3][6];
double BTmatrix[6][3];
double Dmatrix[3][3];
double fx[6];
double displacement[6];
double x[3];
double y[3];

if ( oar != NULL ) FLPS_panic("fubar");
        StaticColumn &a = arg->EleInside(ev);
        for (int k=0; k<ev.VecLen(); k++) { //loop over all faces
                for (int i=0; i<6; i++) displacement[i]=0;
                        for (int i=0; i<6; i++){
                                VectorStatic &av = a.Val(i);
                                displacement[i] = av[k];
                                cout <<"Displacement = " << " " <<
                                        displacement[i] <<endl;
                                                }

for (int l=0; l<6; l+=2) {
//loop over 3 nodes of each face NOTE:should be less than ev.Size() for an arbitrary
//element, but triangles is 3
        Coordinate &chead = ev.node(l,k)->location(); //find location of //nodes
        x[ev.Nind(l)]=chead.x();
        y[ev.Nind(l)]=chead.y();
                } //finishes NodeLen for loop

B_Matrix( Bmatrix, x[0], y[0], x[1], y[1], x[2], y[2] );
```

```
BT_Matrix(Bmatrix, BTmatrix);
D_Matrix(Dmatrix, E, nu);
Stiffness(BTmatrix, Dmatrix, Bmatrix, C, stiffness);
//multiply stiffness matrix by column vector
Multiply(stiffness, displacement, fx);
for (int i=0; i<6; i++){  //store info at Val(i)
        VectorStatic &v = se0->Val(i);
        v[k] = fx[i];
        cout << "fx = " << " " << v[k] << endl;
                        }
                }//finishes VecLen for loop
        }

StaticColumn &DiscExpr::EleInside( ElementInfo &ev ) {
FLPS_panic("DiscExpr inside another discexpr")
}

void DiscExpr::ElasticDeriv( ElementInfo &ev) {
double x0;
double y0;
double x1;
double y1;
double x2;
double y2;
double C[6][3];
double stiffness[6][6];
double Bmatrix[3][6];
double BTmatrix[6][3];
double Dmatrix[3][3];
double fx[6];
double displacement[6];

//Print out nodes of all faces & create storage for the nodes
double x[3];
double y[3];

for (int k=0; k<ev.VecLen(); k++) { //loop over all faces
        for (int l=0; l<6; l+=2) {
//loop over 3 nodes of each face //NOTE: should be less than ev.Size for an arbitrary
//element, but  triangles is 3
//print node x and y values
                Coordinate &chead = ev.node(l,k)->location(); //find //location of nodes
                cout << "x = " <<chead.x()<< " " << "y = " << chead.y() << endl;
                x[ev.Nind(l)]=chead.x();
                y[ev.Nind(l)]=chead.y();
                        } //finishes NodeLen for loop
```

```
        B_Matrix( Bmatrix, x[0], y[0], x[1], y[1], x[2], y[2] );
        BT_Matrix(Bmatrix, BTmatrix);
        D_Matrix(Dmatrix, E, nu);
        Stiffness(BTmatrix, Dmatrix, Bmatrix, C, stiffness);

        for (int i=0; i<6; i++){
                for (int j=0; j<6; j++){
                        VectorStatic &v = sd->Val(i,j);
                        v[k] = stiffness[i][j];
                                }
                        }
                }//finishes VecLen for loop
}

//This function calculates the strain from boron doping
void DiscExpr::BodyForceEval( ElementInfo &ev ) {
double x0;
double y0;
double x1;
double y1;
double x2;
double y2;
double C[6][3];
double stiffness[6][6];
double Bmatrix[3][6];
double BTmatrix[6][3];
double Dmatrix[3][3];
double fx[6];
double displacement[6];
double x[3];
double y[3];
double strain[3];

if ( oar != NULL ) FLPS_panic("fubar");
StaticColumn &a = arg->EleInside(ev);
for (int k=0; k<ev.VecLen(); k++) { //loop over all faces
        for (int i=0; i<3; i++) strain[i]=0;
        //strain source at each node
        double s1 = a.Val(0).get(k);
        double s2 = a.Val(2).get(k);
        double s3 = a.Val(4).get(k);

//assume the strain is hydrostatic - isotropic in direction and //magnitude equals the
//average
```

```
        strain[0] = sqrt(2.0) * (s1+s2+s3) / 6.0;

        strain[1] = sqrt(2.0) * (s1+s2+s3) / 6.0;
        //assume no shear component
        strain[2] = 0.0;

        for (int l=0; l<6; l+=2) {
//loop over 3 nodes of each face NOTE:should be less than ev.Size() for an arbitrary
//element, but triangles is 3
                Coordinate &chead = ev.node(l,k)->location(); //find //location of nodes
                x[ev.Nind(l)]=chead.x();
                y[ev.Nind(l)]=chead.y();
                        } //finishes NodeLen for loop

        B_Matrix( Bmatrix, x[0], y[0], x[1], y[1], x[2], y[2] );
        BT_Matrix(Bmatrix, BTmatrix);
        D_Matrix(Dmatrix, E, nu);
        BTMultD(BTmatrix, Dmatrix, C);
        //multiply [6x3]C*nodal //strain[3x1]=(displacements) - forces [6x1]
        MultBtDBF(C, strain, fx);
        for (int i=0; i<6; i++){  //store info at Val(i)
                VectorStatic &v = se0->Val(i);
                v[k] = fx[i]; //store away the displacements
                cout << "fx = " << " " << v[k] << endl;
                        }
        }//finishes VecLen for loop
}

void DiscExpr::BodyForceDeriv( ElementInfo &ev ) {

   for (int k=0; k<ev.VecLen(); k++) {
        for (int i=0; i<6; i++){
                for (int j=0; j<6; j++){
                        VectorStatic &v = sd->Val(i,j);
                        v[k] = 0.0;
                                }
                        }
                }//finishes VecLen for loop
                } //this is not general
```

```
void DiscExpr::StrainEval( TensorType tt, ElementInfo &ev ) {
double x0;
double y0;
double x1;
double y1;
double x2;
double y2;
double C[6][3];
double stiffness[6][6];
double Bmatrix[3][6];
double BTmatrix[6][3];
double Dmatrix[3][3];
double fx[6];
double displacement[6];
double x[3];
double y[3];
double strain[3];
double elestrain[3];
double val;

if ( oar != NULL ) FLPS_panic("fubar");
StaticColumn &a = arg->EleInside(ev);
for (int k=0; k<ev.VecLen(); k++) { //loop over all faces
        for (int i=0; i<6; i++) displacement[i]=0;
                for (int i=0; i<6; i++){

//fill in the displacement vector to compute the strain
                        VectorStatic &av = a.Val(i);
                        displacement[i] = av[k];
                      cout << "displacement = " << " " << displacement[i] << endl;
                        }


for (int l=0; l<6; l+=2) { //loop over 3 nodes of each face NOTE: .
        Coordinate &chead = ev.node(l,k)->location(); //find location of //nodes
        x[ev.Nind(l)]=chead.x();
        y[ev.Nind(l)]=chead.y();
                } //finishes NodeLen for loop

        B_Matrix( Bmatrix, x[0], y[0], x[1], y[1], x[2], y[2] );
        //multiply //3x6]B*[6x1]=elestrain[3x1] - strain[xx, yy, xy]
        MultiplyStrain(Bmatrix, elestrain, displacement);
        // find tt to determine if //want strain_xx, strain_yy, or strain_xy
        if (tt==Dir_XX) val = elestrain[0];     else if (tt==Dir_YY) val = elestrain[1];
        else val = elestrain[2];
```

```
        for (int i=0; i<3; i++){  //store info at Val(i)
//store away the elemental strain values at //each node (strain_xx, yy, or xy)
                VectorStatic &v = se0->Val(i);
                v[k] = val;
                cout << "strain = " << " " << v[k] << endl;
                }
        }//finishes VecLen for loop
}

void DiscExpr::StrainDeriv(TensorType tt,  ElementInfo &ev ) {FLPS_panic("Calling
StrainEval");
}

void DiscExpr::StressEval( TensorType tt, ElementInfo &ev )
{
double x0;
double y0;
double x1;
double y1;
double x2;
double y2;
double C[6][3];
double stiffness[6][6];
double Bmatrix[3][6];
double BTmatrix[6][3];
double Dmatrix[3][3];
double fx[6];
double displacement[6];
double x[3];
double y[3];
double strain[3];
double elestrain[3];
double stress[3];
double val;

if ( oar != NULL ) FLPS_panic("fubar");
StaticColumn &a = arg->EleInside(ev);
for (int k=0; k<ev.VecLen(); k++) { //loop over all faces
        for (int i=0; i<6; i++) displacement[i]=0;
                for (int i=0; i<6; i++){ //fill in the displacement //vector to compute strain
                VectorStatic &av = a.Val(i);
                displacement[i] = av[k];
                        }
                cout << "displacement = " << " " << displacement << endl;

for (int l=0; l<6; l+=2) { //loop over 3 nodes of each face
```

```
        Coordinate &chead = ev.node(l,k)->location(); //find location of //nodes
        x[ev.Nind(l)]=chead.x();
        y[ev.Nind(l)]=chead.y();
                } //finishes NodeLen for loop

        B_Matrix( Bmatrix, x[0], y[0], x[1], y[1], x[2], y[2] );
        D_Matrix(Dmatrix, E, nu);
        //multiply [3x6]B*[6x1]=elestrain[3x1] - strain[xx, yy, xy]
        MultiplyStrain(Bmatrix, elestrain, displacement);
        MultiplyStress(Dmatrix, elestrain, stress);

       // find tt to determine if want //strain_xx, strain_yy, or strain_xy
        if (tt==Dir_XX) val = stress[0];
        else if (tt==Dir_YY) val = stress[1];
        else val = stress[2];

        for (int i=0; i<ev.Size(); i++){  //store info at Val(i)
                VectorStatic &v = se0->Val(i);
                v[k] = val; //store away the stress values at each node //(xx, yy, or xy)
                cout << "stress = " << " " << v[k] << endl;
                        }
                }//finishes VecLen for loop
        }


void DiscExpr::StressDeriv(TensorType tt,  ElementInfo &ev ) {FLPS_panic("Calling
StressEval");}

double Delta (double x0, double y0, double x1, double y1, double x2, double y2)
{
double ans = (((x1*y2) - (x2*y1)) - ((x0*y2) - (x2*y0)) + ((x0*y1) - (x1*y0)));
cout << "two_delta =" << ans << "\n";
return ans;
}

//BT*D*B=stiffness matrix, start here with B matrix
void B_Matrix( double Bmatrix[3][6], double x0, double y0, double x1, double y1,
double x2, double y2 )
{
Bmatrix[0][0] = y1 - y2;
Bmatrix[1][0] = 0;
Bmatrix[2][0] = x2 - x1;

Bmatrix[0][1] = 0;
Bmatrix[1][1] = x2 - x1;
Bmatrix[2][1] = y1 - y2;
```

```
Bmatrix[0][2] = y2 - y0;
Bmatrix[1][2] = 0;
Bmatrix[2][2] = x0 - x2;

Bmatrix[0][3] = 0;
Bmatrix[1][3] = x0 - x2;
Bmatrix[2][3] = y2 - y0;

Bmatrix[0][4] = y0 - y1;
Bmatrix[1][4] = 0;
Bmatrix[2][4] = x1 - x0;

Bmatrix[0][5] = 0;
Bmatrix[1][5] = x1 - x0;
Bmatrix[2][5] = y0 - y1;

double two_delta = Delta (x0, y0, x1, y1, x2, y2);
cout <<"Bmatrix is...\n";
for (int i=0;i<3; i++) {
        for (int j=0; j<6; j++) {
        Bmatrix[i][j] = (Bmatrix[i][j] / two_delta);
          cout << Bmatrix[i][j]<< ",";
                }
              cout<< "\n\n\n";
         }
}

//Compute BT matrix
void BT_Matrix (double Bmatrix[3][6], double BTmatrix[6][3])
{
for (int i=0;i<6; i++) {
        for (int j=0; j<3; j++) {
                BTmatrix[i][j]=Bmatrix[j][i];
                 }
        }
 }

 //Compute D matrix
 void D_Matrix (double Dmatrix[3][3], double E, double nu)
{
  /*    Dmatrix[0][0] = 1;      //This is the plane stress approximation
        Dmatrix[1][0] = nu;
        Dmatrix[2][0] = 0;

        Dmatrix[0][1] = nu;
        Dmatrix[1][1] = 1;
```

```
	Dmatrix[2][1] = 0;

	Dmatrix[0][2] = 0;
	Dmatrix[1][2] = 0;
	Dmatrix[2][2] = (1-nu)*0.5;

	cout << "Dmatrix is...\n";
	for (int i=0;i<3; i++) {
		for(int j=0;j<3; j++) {
		Dmatrix[i][j] = Dmatrix[i][j] * (E/(1-(nu*nu)));
		cout << Dmatrix[i][j]<< ",";
		}
		cout<< "\n\n\n";
		   }
	*/

	Dmatrix[0][0] = 1;	//This is the plane strain approximation
	Dmatrix[1][0] = (nu/(1-nu));
	Dmatrix[2][0] = 0;

	Dmatrix[0][1] = (nu/(1-nu));
	Dmatrix[1][1] = 1;
	Dmatrix[2][1] = 0;

	Dmatrix[0][2] = 0;
	Dmatrix[1][2] = 0;
	Dmatrix[2][2] = ((1-(2*nu))/(2*(1-nu)));

	cout << "Dmatrix is...\n";
	for (int i=0;i<3; i++) {
		for(int j=0;j<3; j++) {
		Dmatrix[i][j] = Dmatrix[i][j] * ((E*(1-nu))/((1+nu)*(1-(2*nu))));
		cout << Dmatrix[i][j]<< ",";
		}
		cout<< "\n\n\n";
			}
			 }

//multiply BT*D*B to get a 6 by 6 stiffness matrix
void Stiffness(double BTmatrix[6][3], double Dmatrix[3][3], double Bmatrix[3][6],
double C[6][3], double stiffness[6][6])
 {
for (int i=0;i<6; i++) {
	for (int j=0; j<3; j++) {
		C[i][j]=0;
	  for (int z=0; z<3; z++){
```

```
                        C[i][j] += BTmatrix[i][z] * Dmatrix[z][j];
                        }
                }
        }

        //multiply stiffness = C*B
        for (int i=0;i<6; i++) {
        for (int j=0; j<6; j++) {
                stiffness[i][j]=0;
                for (int z=0; z<3; z++){
                        stiffness[i][j] += C[i][z] * Bmatrix[z][j];
                                }
                                }
                        }
                        }

 //multiply BT* D to compute body forces
void BTMultD(double BTmatrix[6][3], double Dmatrix[3][3], double C[6][3])
 {
for (int i=0;i<6; i++) {
        for (int j=0; j<3; j++) {
        C[i][j]=0;
           for (int z=0; z<3; z++){
                C[i][j] += BTmatrix[i][z] * Dmatrix[z][j];
                        }
                }
        }
 }


 //multiply stiffness (derivative matrix) * fx
void Multiply(double stiffness[6][6], double displacement[6], double fx[6])
 {
for (int i=0; i<6; i++){
        fx[i]=0;
        for(int j=0; j<6; j++){
                fx[i] += stiffness[i][j] * displacement[j];
                                }
                        }
                }

void MultBtDBF(double C[6][3], double strain[3], double fx[6]) //f[x] is the 6
displacement values
 {
for (int i=0; i<6; i++){
        fx[i]=0;
```

```
        for(int j=0; j<3; j++){
                fx[i] += C[i][j] * strain[j];
                                }
                }
}
```

APPENDIX B
SIMULATION FILES

This appendix contains the simulation files for the results presented in Chapter 5.

```
#This simulation computes the displacement in the silicon beam due to boron doping.
#The grid is adjusted in the x and y directions to accommodate changes in the length and
#width. The doping profile is adjusted by commenting out the line “profile name=Bar
#infile=bartop1p4u.prof,” and uncommenting the line “sel z=8.0e19*exp(-x*x/0.01)
#name=Bar.”

math diffuse dim=2 umf none col !scale
solution name=Potential nosolve

pdbSetBoolean Silicon displacement Negative 1
pdbSetBoolean ReflectLeft displacement Negative 1
pdbSetDouble Silicon displacement Abs.Error 1.0e-8
pdbSetDouble ReflectLeft displacement Abs.Error 1.0e-8


#Set up grid
line x loc=0.2 tag=top spa=0.05
line x loc=1.4 tag=bot spa=0.05
line y loc=0.0 tag=left spa=0.5
line y loc=50 tag=right spa=.5

#Define silicon region
region silicon xlo=top xhi=bot ylo=left yhi=right

init

#Import doping profile, uncomment the second line to adjust the doping # profile
profile name=Bar infile=bartop1p4u.prof

#Set up solution for displacement
solution name = displacement add solve dim continuous
solution name = Temp const val = 1000 add solve

#Fix left boundary
pdbSetBoolean ReflectLeft displacement Fixed 1
pdbSetString ReflectLeft displacement Equation "displacement"
```

```
#Set Young's Modulus and Poisson's Ratio
pdbSetDouble Silicon YoungsModulus 1.80E12
pdbSetDouble Silicon PoissonRatio 0.28


#Evaluate the equation – the argument of the bodyforce operator is the strain from boron
doping
pdbSetString Silicon displacement Equation "elastic(displacement)-
BodyForce((1+.3)*5.19e-24*Bar)"

#Initiate Alagator
diffuse time = 1e-6 temp=1000 init=1.0e-5
plot.2d grid pos=displacement

#Solve for Stress/Strain in the xx, yy, or xy directions
select z = "Stress(xy, displacement)"


#This simulation computes the displacement and stress in the silicon due to an intrinsic
#force (stress) in the nitride layer. NOTE: This is an unpractical method to apply an
#intrinsic stress in a nitride layer.

math diffuse dim=2 umf none col !scale
solution name=Potential nosolve

pdbSetBoolean Silicon displacement Negative 1
pdbSetBoolean ReflectLeft displacement Negative 1
pdbSetDouble Silicon displacement Abs.Error 1.0e-8
pdbSetDouble ReflectLeft displacement Abs.Error 1.0e-8

pdbSetBoolean nitride displacement Negative 1
pdbSetBoolean ReflectLeft displacement Negative 1
pdbSetDouble nitride displacement Abs.Error 1.0e-8
pdbSetDouble ReflectLeft displacement Abs.Error 1.0e-8

#Set Young's Modulus and Poisson's Ratio
pdbSetDouble Silicon YoungsModulus 1.22e12
pdbSetDouble Silicon PoissonRatio 0.3
pdbSetDouble nitride YoungsModulus 3e12
pdbSetDouble nitride PoissonRatio 0.25

#Set up grid
line x loc=-0.02 tag=nit spa=0.05
line x loc=0.0 tag=top spa=0.05
line x loc=10 tag=bot spa=0.5
line y loc=0.0 tag=left spa=0.5
```

```
line y loc=5 tag=side   spa=.1
line y loc=10 tag=mid   spa=.1
line y loc=15 tag=right spa=.5

#Define silicon, nitride, and gas region
region gas xlo=nit xhi=top ylo=left yhi=side
region gas xlo=nit xhi=top ylo=mid yhi=right
region nitride xlo=nit xhi=top ylo=side yhi=mid
region silicon xlo=top xhi=bot ylo=left yhi=right

init

# Apply a constant force (intrinsic stress) in the nitride material
select z=0.6e20*(Material(nitride)) name=Bar

#Set up solution for displacement
solution name = displacement add solve dim continuous
solution name = Temp const val = 1000 add solve

#Fix left boundary
pdbSetBoolean ReflectBottom displacement Fixed 1
pdbSetString ReflectBottom displacement Equation "displacement"



#Evaluate the matrix
pdbSetString Silicon displacement Equation "elastic(displacement)"
pdbSetString nitride displacement Equation
"elastic(displacement)+BodyForce(Bar*5.19e-22)"

#Initiate Alagator
diffuse time = 1e-6 temp=1000 init=1.0e-5
plot.2d grid pos=displacement

#Solve for Stress/Strain in the xx, yy, or xy directions
select z = "Stress(xy, displacement)"


#This simulation computes the stress in the silicon due to boron doping. The channel
length and source/drain length can be adjusted in the grid. The boron concentration can
be manually adjusted on the “sel z=2e20*exp(-x*x/0.0013)*((y<1.0)||(y>1.1))
name=Bar” line

math diffuse dim=2 umf none col !scale
solution name=Potential nosolve
```

```
pdbSetBoolean Silicon displacement Negative 1
pdbSetDouble Silicon displacement Abs.Error 1.0e-8
pdbSetBoolean nitride displacement Negative 1
pdbSetDouble nitride displacement Abs.Error 1.0e-8

pdbSetBoolean ReflectBottom displacement Negative 1
pdbSetDouble ReflectBottom displacement Abs.Error 1.0e-8

#Fix bottom boundary
pdbSetBoolean ReflectBottom displacement Fixed 1
pdbSetString ReflectBottom displacement Equation "displacement"

#Set Young's Modulus and Poisson's Ratio
pdbSetDouble Silicon YoungsModulus  1.80E12
pdbSetDouble Silicon PoissonRatio 0.28
pdbSetDouble nitride YoungsModulus  3E12
pdbSetDouble nitride PoissonRatio 0.25

#Set up Grid
line x loc=  0.0   tag=SiTop       spacing=0.01
line x loc = 0.12  tag=BorBottom   spacing=0.005
line x loc = 0.5                   spacing=0.1
line x loc=5.0     tag=SiBottom    spacing=0.2
line y loc=0.0     tag=Mid         spac=0.01
line y loc=1.0     tag=BorRight    spac=0.05
line y loc=1.1     tag=BorLeft     spac=0.05
line y loc=2.1     tag=Right       spac=0.01

#Define silicon region
region silicon xlo=SiTop xhi=SiBottom ylo=Mid yhi=Right

init


#Set up solution for displacement
solution name = displacement add solve dim continuous
solution name = Temp const val = 1000 add solve

#Selectively implant the channel region with species Bar (boron)
sel z=2e20*exp(-x*x/0.0013)*((y<1.0)||(y>1.1)) name=Bar

#Evaluate the matrix
pdbSetString Silicon displacement Equation
"elastic(displacement)+bodyforce((1+.28)*Bar*5.19e-24)"

#Initiate Alagator
```

```
diffuse time = 1.0e-6 temp=1000 init=1.0e-5

#Solve for Stress/Strain in the xx, yy, or xy directions
select z= "Stress(yy, displacement)"
print.1d x=.01
```

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BIOGRAPHICAL SKETCH

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