A 10 GIGABIT PER SECOND LIMITING AMPLIFIER WITH 42dB GAIN AND 7 GHz BANDWIDTH FOR SONET OC-192 APPLICATIONS

By

STEPHEN E. COVE

A THESIS PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
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This document is dedicated to my wife Dee Dee and sons Ethan and Kyle.

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of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Master of Science

A 10 GIGABIT PER SECOND LIMITING AMPLIFIER WITH 40dB GAIN AND 7 GHz BANDWIDTH FOR SONET OC-192 APPLICATIONS

By

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Major Department: Electrical and Computer Engineering

Traditionally high speed RF and serial I/O multi-gigahertz circuits have been built in expensive processes such as Silicon Germanium. This has kept cost up for systems requiring these types of circuits. Now that CMOS processes have shrunk minimum gate sizes to deep sub-micron lengths of 0.13um and beyond, it has become possible to attempt these designs in this less expensive and widely available technology. Doing so allows IC designers to begin to combine the custom analog portion of a system onto the same die as the digital circuitry.

This paper documents the design and testing of a 10gigabit per second limiting amplifier (LIA) for an OC-192 SONET serializer/deserializer (SERDES) chipset. It was fabricated in UMC's 0.13 micron Mixed Mode/RFCMOS technology. The design required the use of a modified Cherry-Hooper amplifier stage and incorporated active inductors to extend the bandwidth. To improve sensitivity, two types of offset

correction/cancellation were incorporated; one automatic and one manual controlled by an off-chip potentiometer.

The goal of the design was to exceed 7GHz of bandwidth and 42dB of gain to deliver a data eye with less than 10pS jitter and 1.2VPP differential amplitude. Simulations demonstrated that greater than 6.5GHz bandwidth would be possible over the majority of process, temperature, and voltage variation but that the strain of high temperature and low voltage combined closed the data eye significantly.

Because the LIA was incorporated in a full deserializer IC, its output could not be accessed directly. Instead the system performance with a large clean input signal was used as a benchmark and then the input amplitude decreased to determine LIA performance. Test results showed that the LIA did achieve an absolute sensitivity of 14mVPP differential and a bandwidth wide enough to achieve error-free performance at 9.95GHz. However, the sensitivity was decreased as low voltage and high temperature extremes were applied.

Overall, the design was found to be acceptable for use in SONET systems where power was a factor as the LIA and other parts of this SERDES system were very power efficient for the performance achieved.

CHAPTER 1
INTRODUCTION

In the ever-growing internet economy, the requirements for bandwidth are becoming exponentially greater. Businesses are connecting sites around the globe and more homes are using the World Wide Web. To keep up with this demand, telecommunications companies are striving to provide systems that move data at extremely high speeds. Some of the fastest of today's systems are based on the Sonet OC-192 standard. This standard defines serial data transfer at approximately 10Gigabits/second.

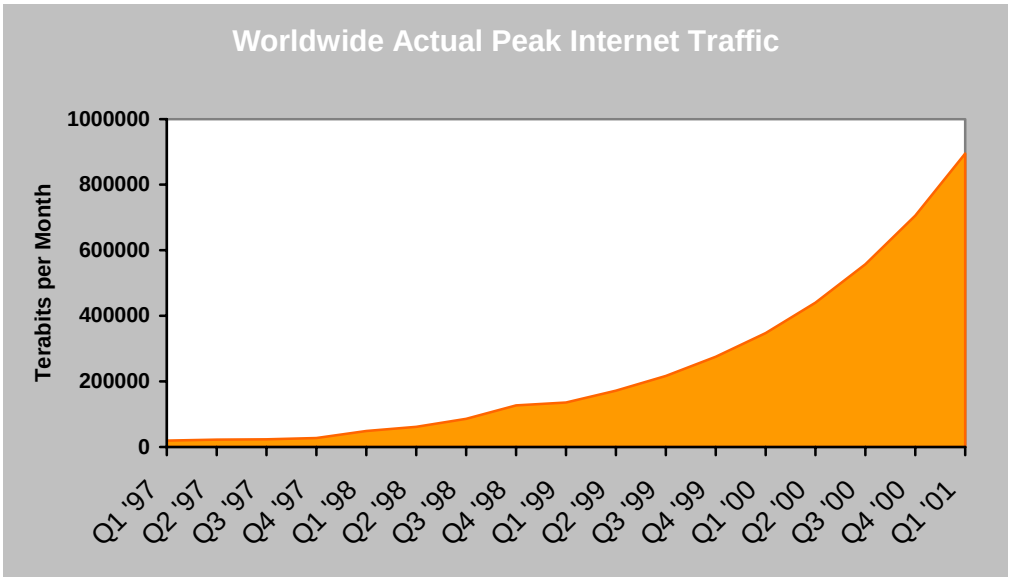


Figure 1-1. Growth of internet traffic [1]

Historically, telecom companies have used copper to connect systems. However, optical fiber has a much higher bandwidth than copper and the signal is not distorted

nearly as much from electromagnetic interference or other noise. Because of this, optical fiber is the preferred medium for data transmission over distances greater than a kilometer at rates in excess of 100 megabits [2].

In optical fiber, information is transmitted as light. Since data manipulation systems (computers, telephone switches, etc.) operate using electrical signals, the data must be converted between the two media. To do this, lasers are driven by electrical binary data patterns. The laser turns on and off according to the value of the input pattern and this pulsating light is transmitted along the optical fiber.

At the far end of the fiber, a device called a photodiode is used to convert the light back into electrical pulses. Photodiodes change conductivity based on the presence of light, conducting more when exposed to the light energy. A simple diagram of this system is shown below.

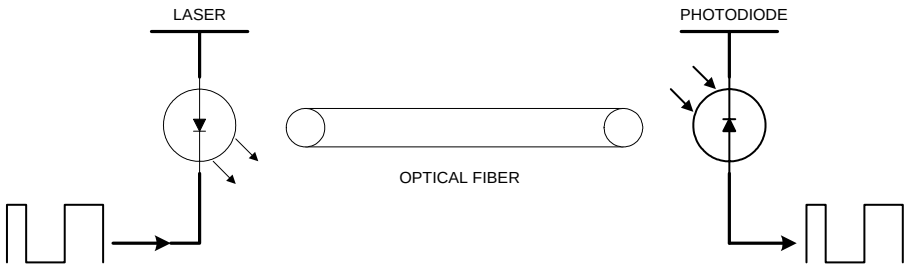


Figure 1-2. Simplified diagram of an optical system [3]

While lasers, fiber optic cable and photo-diodes allow the transmission of high-speed serial data, it is not yet possible to build standard CMOS logic processing circuitry that operates at 10GHz. Today's fastest microprocessors using 90nm technology have clock speeds of approximately 4GHz.

To take advantage of the bandwidth available over a high-speed link, custom high speed I/O circuitry is used to multiplex several low speed parallel digital inputs for

transmission. At the receiving end the data is de-multiplexed by more high speed I/O circuitry into the original parallel streams which can be processed by economical digital ICs. These analog circuits are called serializer/deserializers or SERDES.

The limiting amplifier described in this paper is part of a commercial SERDES product developed to meet the needs of this market. It was designed in UMC's 0.13 micron Mixed Mode/RFCMOS technology. It was specified to operate within the OC-192 Sonet specification with a stretch goal of achieving up to 11.1 gigabits per second. Chapter two describes the system architecture of a SERDES system and the general requirements of a limiting amplifier. Chapter three details the design and function of each block of the limiting amplifier. In Chapter four, the layout is discussed. Chapter five presents the simulation results and summarizes a BSIM3 modeling issue that was discovered during the simulation phase. Chapter six lists the measurement results from silicon and chapter seven summarizes the work.

CHAPTER 2
SYSTEM ARCHITECTURE AND LIMITING AMPLIFIER INTRODUCTION

SERDES System Architecture

A common SERDES architecture is shown in figure 2-1.

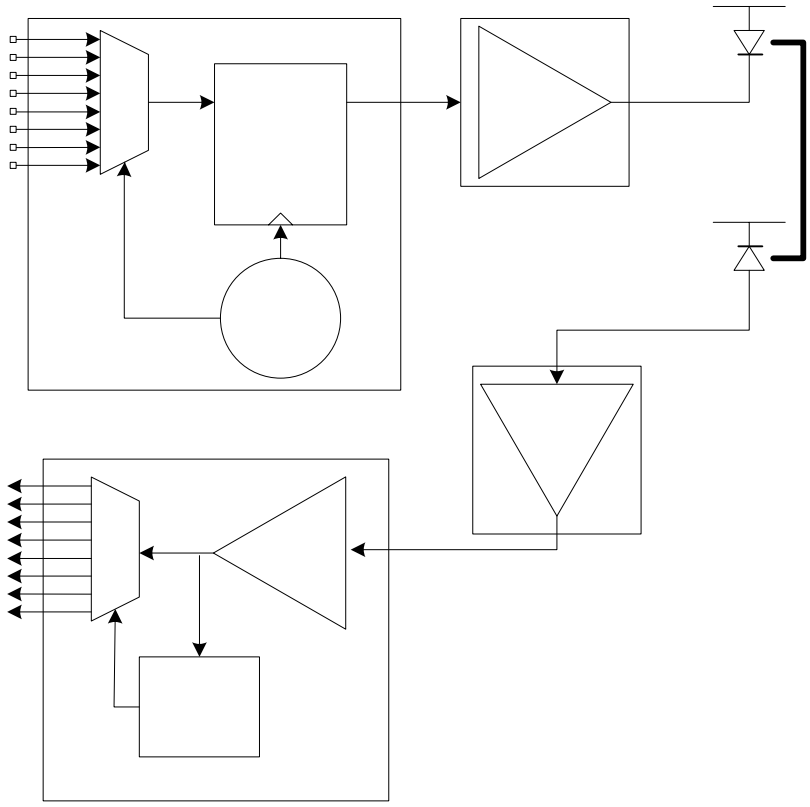


Figure 2-1. A typical SERDES system

To transmit, several parallel data streams are fed into the serializer's multiplexer or MUX. Since digital processors often work with 8 bit data words (bytes), this parallel input is often a multiple of 8. For a digital block with a clock frequency of 311 MHz, 32 channels could be multiplexed together to achieve a serial stream of 9.95 GHz. Once multiplexed, the serial data can be fed through a retimer, which is a high speed flip-flop

clocked by the transmitter's Voltage Controlled Oscillator (VCO.) This step reduces the jitter that can be generated by the previous stages. The data is then sent to the laser for transformation to an optical signal as described previously.

At the receiver, the photo-detector feeds a Transimpedance Amplifier (TIA) the recovered serial stream. The output of the TIA can be a very low amplitude signal, as small as 10mV. To boost this small signal, a Limiting Amplifier (LIA) is employed. Once the LIA has restored the signal to a reasonable level (on the order of 1V differential) it is sent to both the decision circuit and the clock recovery circuit. Recovery of the clock is necessary as no separate reference is transmitted with the high speed data. The recovered clock provides timing for the decision circuit and the following demultiplexer (DEMUX) which restores the data to its original parallel form.

While traditionally the SERDES system consisted of several separate ICs utilizing exotic technologies, designs are emerging that combine several blocks and use CMOS technology. By using CMOS processes, the SERDES can be included on the same die as the digital circuitry; very desirable from a cost standpoint. Care must be taken to ensure good isolation for critical circuits since digital switching and multiple oscillators can easily create too much noise.

General Requirements of the LIA

All limiting amplifiers must somehow overcome the following issues to transfer the data from the external trans-impedance amplifier IC to the clock recovery and demultiplexing circuitry of the system.

- Gain—as mentioned previously, the output of the TIA can be as low as 10mV, while the CML logic of the deserializer requires signals on the order of 1VPP differential. This translates to a gain of ~40dB.

- Bandwidth—Depending on the standard, the passband for an LIA must be very wide. As low as 50MHz (determined by the maximum run length of the bit patterns) and greater than 7GHz for acceptable ISI.
- Sensitivity—must be able to detect the small signal above any noise.
- Jitter—the system has a maximum jitter budget that combines VCO, LIA, and other block jitter. There must be sufficient eye opening to allow the clock to sample at a time when the data can be read with confidence.
- Input impedance matching—The LIA must minimize reflections at the input pins to maximize performance.

Bandwidth Limitations of Cascaded Stages

Imagine an LIA is comprised of *N* identical single pole stages with gain A_0 and an output resistance *R* driving a load *C*. If ω_0 is used to represent the time constant 1/RC, the total gain of the circuit is

$$H(s) = \left(\frac{A_0}{1 + \frac{s}{\omega_o}} \right)^N \qquad \text{eq. 2-1}$$

If it is assumed that the -3dB point is the minimum LIA bandwidth required to pass a signal with acceptable ISI, the following equality can be written:

$$\left(\frac{A_0}{\sqrt{1^2 + \left(\frac{\omega_{-3db}}{\omega_o} \right)^2}} \right)^N = \frac{A_0{}^N}{\sqrt{2}} \qquad \text{eq. 2-2}$$

Solving for w-3db results in

$$\omega_{-3dB} = \omega_0 \sqrt{\sqrt[N]{2} - 1} \qquad \text{eq. 2-3}$$

For N > than 2, this is often approximated as

$$\omega_{-3dB} = \omega_0 \frac{0.9}{\sqrt{N}} \qquad \text{eq. 2-4}$$

This equation shows that the number of stages *N* increases, the bandwidth ω_0 of each stage must increase to maintain a given overall -3dB bandwidth. More stages relax the gain requirement but increase the bandwidth requirement. Also, lower gain per stage increases the effect of circuit noise in the later stages. To control input referred noise, most high gain limiting amplifiers do not exceed five stages [3].

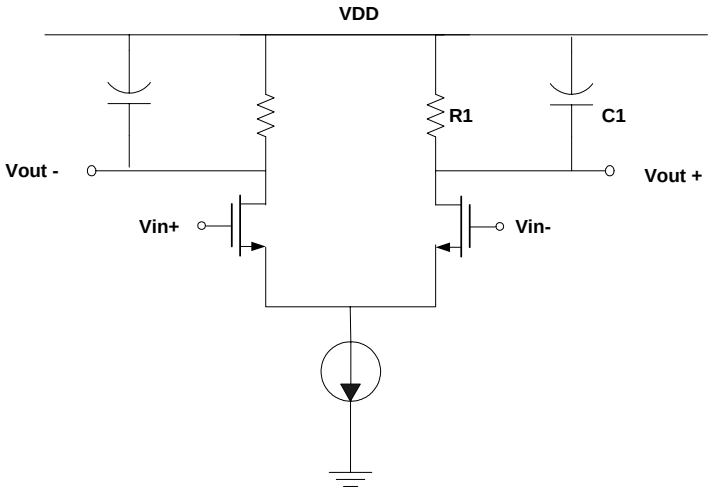


Figure 2-2. Simple gain stage

To achieve a gain of 100 (40dB), a 10G-bit three-stage limiting amplifier would require that each stage had a gain of 4.65V/V and a bandwidth of over 19GHz. However, because the latter stages of the amplifier work in large-signal mode, the bandwidth estimate derived from equation 2-4 is conservative. A description of the speed limitations of large signal operation from Razavi [3] is given below.

Assume the circuit in figure 2-2 has an input pair with a large transconductance. A sufficiently large signal Vin applied to the gates would drive all of the available current

through one side of the differential pair in less time than it takes for the input to transition from its high to low value. As the current moves through the resistor and capacitor, the output voltage changes at the rate of $\tau = R_1C_1$. Therefore the speed of the system in this large signal mode is limited only by the time constant at the output.

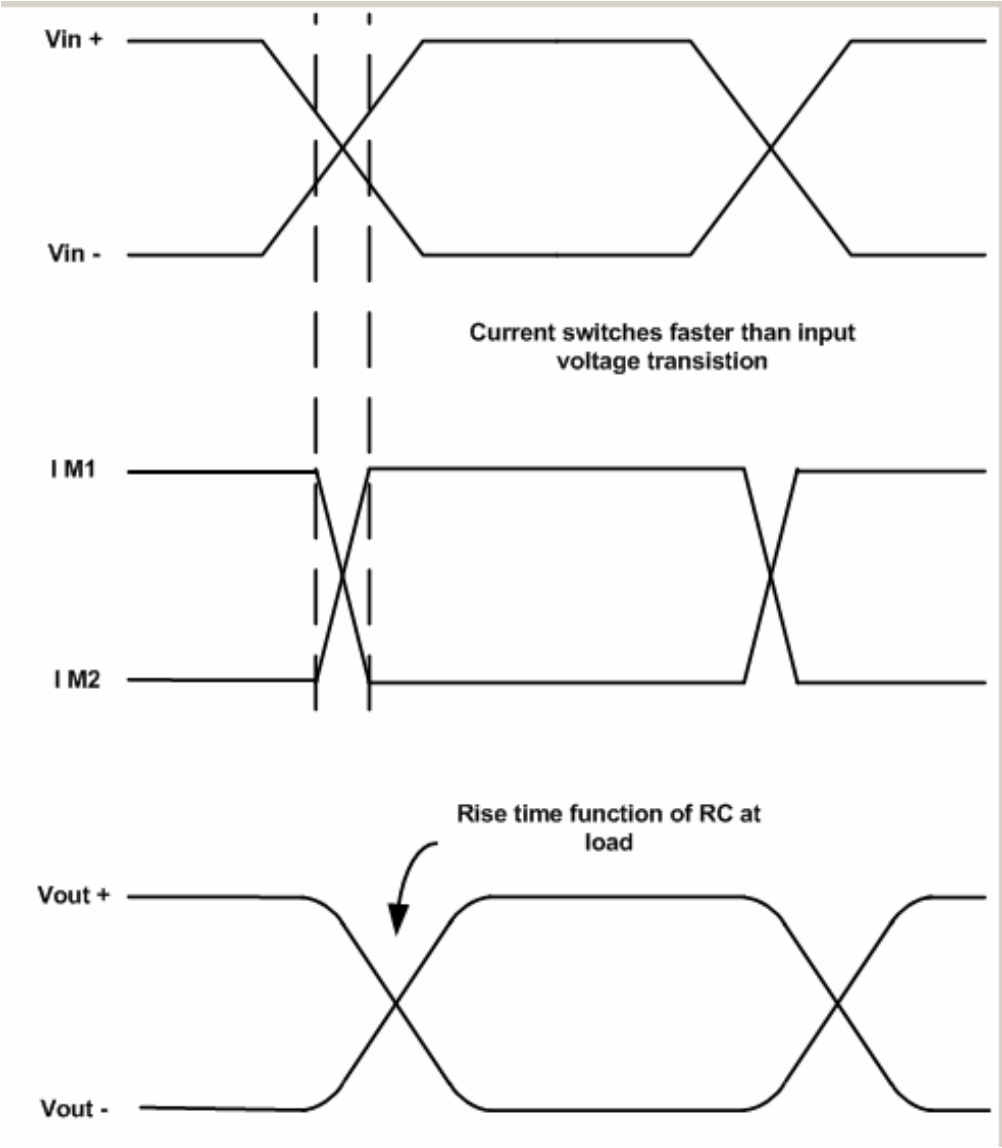


Figure 2-3. Voltage and current waveforms through simple amplifier stage

LIA Design Specifications

The following tables list the design requirement for the limiting amplifier.

Table 2-1. DC characteristics

DC Symbol	Characteristics	Conditions	Min	Nom	Max	Unit
VDD	Supply voltage		1.71	1.8	1.89	V
IDD	Supply current			60	81	mA
Vin	Input level	AC coupled	n/a	n/a	n/a	V
Vout	Output voltage	Std cell definition		600		mV
DTC	Input decision threshold control	Open inputs, DC	-100		100	mV
Rin	Input termination	Differential	90	100	110	Ohm

Table 2-2. AC characteristics

Symbol	Characteristics	Conditions	Min	Nom	Max	Unit
F	Operating line rate				10.71	Gbps
Vi	Input sensitivity, differential	BER=$1x10^{-9}$			10	mVpp
BW	Bandwidth	small signal fanout 2	7	8		GHz
Gain	Gain	small signal fanout 2	42			dB
S11	Input reflection coefficient	Over bandwidth		-15	-10	dB
J	Output cross jitter in eye diagram				10	ps

CHAPTER 3
DESIGN

Top Level Block Description

The top level of the LIA consists of an input stage, three gain stages, an output buffer, a low pass filter for DC offset cancellation, and a bias circuit. The architecture is shown below:

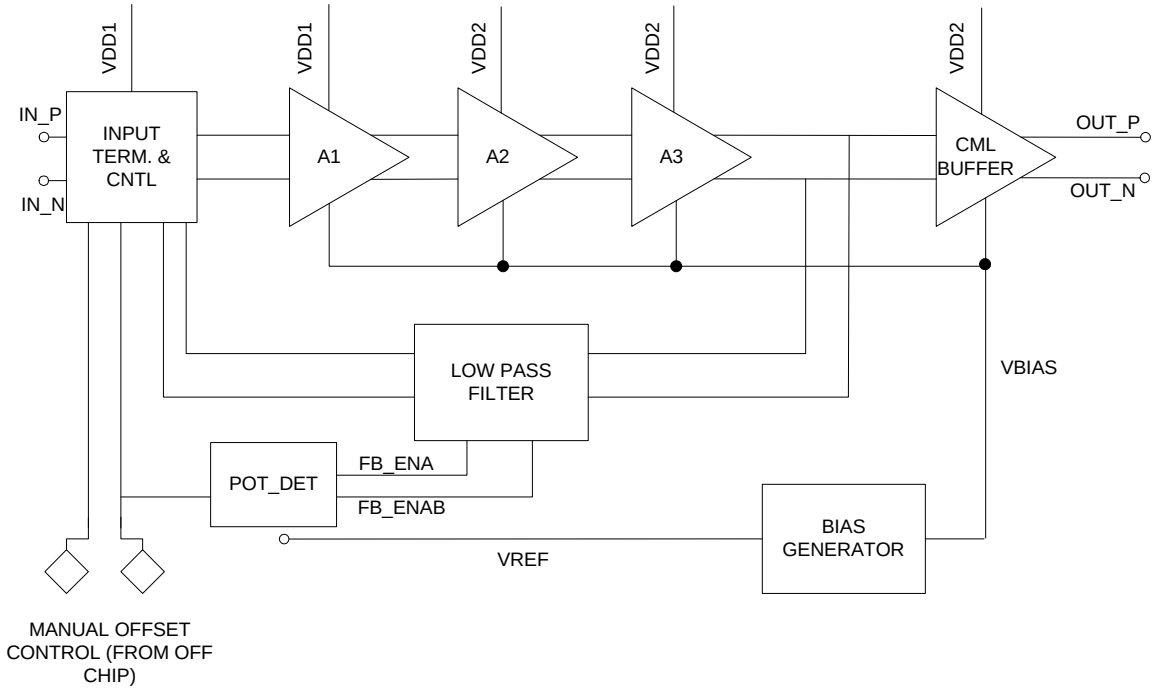


Figure 3-1. Limiting amplifier top level

Input Stage

There are two main purposes for the input stage. It must provide a 50 ohm termination for the input signal and it performs offset cancellation to maximize the circuit sensitivity. This stage was designed to allow two different methods of offset cancellation. The first method is accomplished by closing a negative feedback loop that

returns the output of the third gain stage. If the circuit offsets are evenly distributed and the input signal is symmetrical, this method should be sufficient. However, because mismatches in the first stages of an amplifier affect the input the most, canceling the complete forward path noise can result in less than optimal performance (the first stage offset is not likely equal to the overall input referred forward path offset.) In addition, if the TIA does not produce a perfectly symmetrical waveform, it sensitivity may be improved by shifting the decision threshold to a value other than the middle of the input eye.

Because the output of this stage is DC coupled to the differential pair of the first gain stage, the common mode voltage of the output must be controlled. This requires that the input to this block be AC coupled.

Referring to figure 3-2, the circuit operates in the following manner. A minimum 10mVPP differential signal is applied at pins Vin_P, Vin_N. The connection to these pins is through a 50 ohm transmission line. The return path for this signal is through R3, R4, MIM capacitor C1 and device capacitor M7. These capacitors were required because 50 ohms to VDD would require three times the current to set the DC bias point for the output, and the current is already quite large at 4mA typical through each leg to set a common mode of 1.2V. Because the impedance of these devices must be minimal at the transmission line frequencies, they are very large. Furthermore, the system specification required that the return path could be tied to either VDD or Ground. When the signal return is through VDD, the voltage across device capacitor M7 would be well below its Vt of 600mV. Therefore a much larger device was necessary to maintain a minimum of

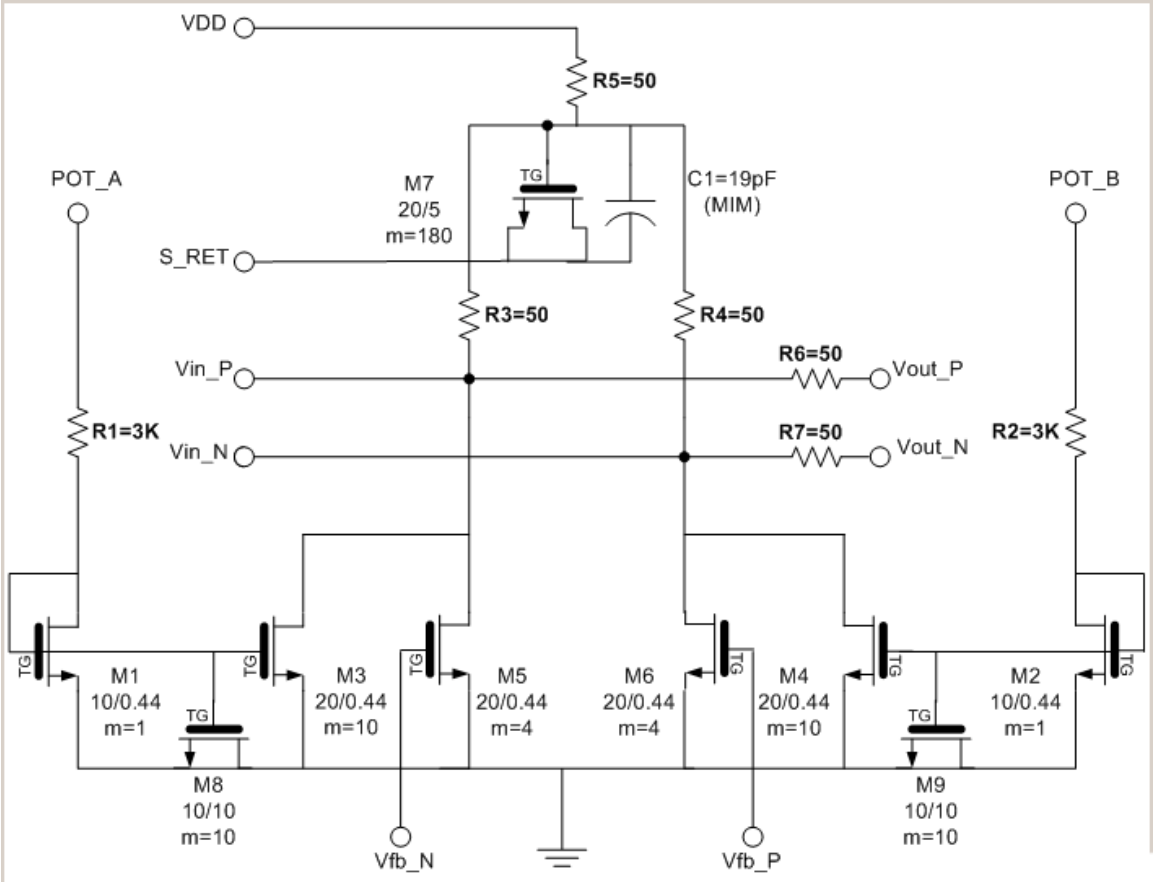


Figure 3-2. Input termination and control

40pF in this configuration. The impedance of the capacitors is given by 1/2πfC and is equal to just under 4 ohms at 1GHz and 0.8 ohms at 5GHz. With a 50 ohm transmission line, this would yield a return loss of -28dB at 1GHz, well below the specification of -10dB. Note that the 50 ohm resistor between VDD and the top of the capacitor is a parallel impedance, but is much greater than the 4 ohms of the capacitor and therefore has been ignored in the calculations.

When the return path is tied to ground, the total capacitance is 100pF. This results in an impedance of 1.6 ohms and a return loss of -36dB at 1GHz. The capacitance curves for device M7 when the source/drain node is tied to ground and VDD are shown in the following figures.

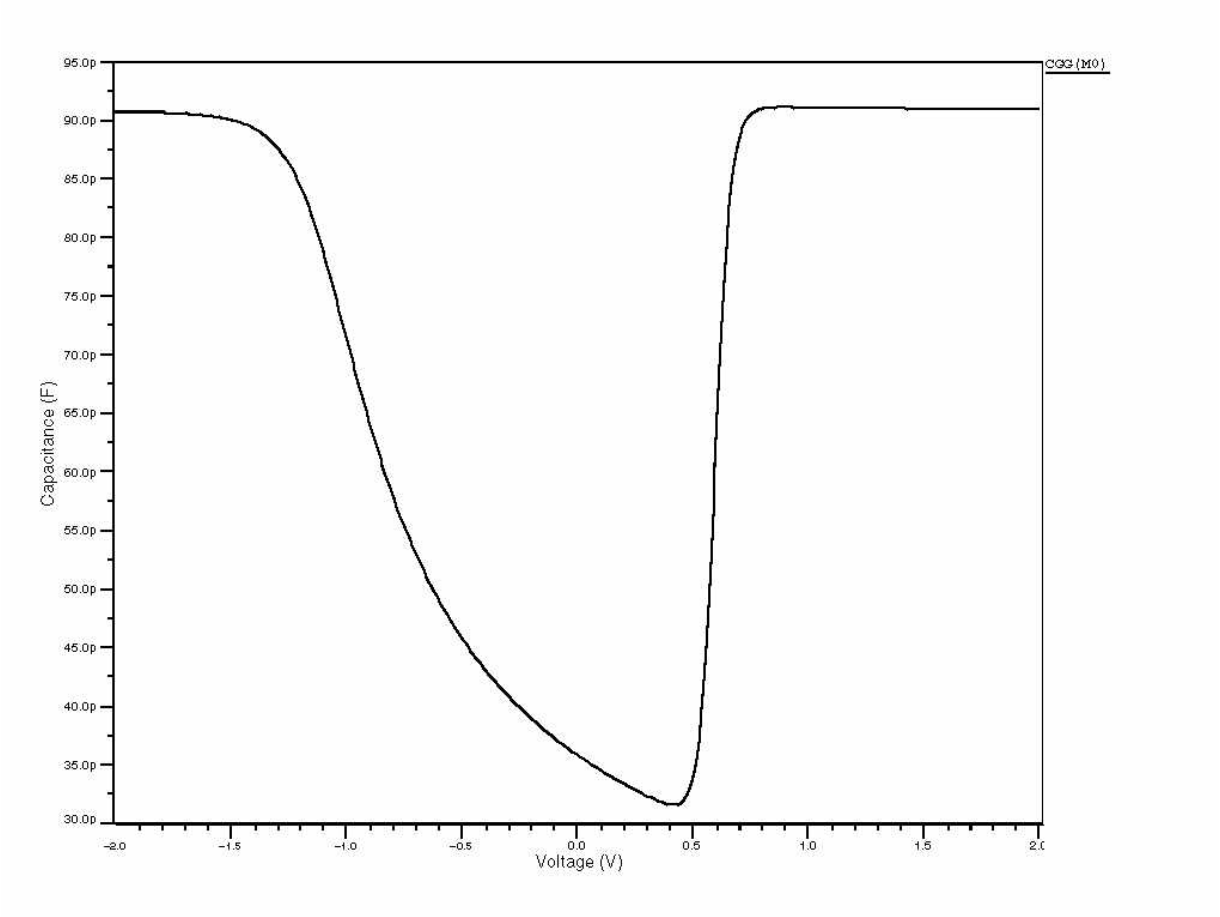


Figure 3-3. Gate capacitance for input termination device cap M7 with source/drain equal to Vbulk. (Vt=599mV)

Resistors R6 and R7 are for ESD purposes. Adding these in series with the gate capacitance of the next stage protects against oxide breakdown if there is an ESD event on the input pad. The drawback is an increased time constant at the differential pair, but because the time constant formed by these 50 ohm resistors and the 34fF gate capacitance of the next stage is 1.7E-12 seconds, there is little impact on signals in the 5GHz range. Alternatively, it can be thought of as a low pass filter with a pole at $1/2\pi RC \approx 90GHz$. This is more than a decade above the required bandwidth.

As mentioned previously, the offset correction can be accomplished in two ways. In “automatic offset cancellation” mode, transistors M1, M2, M3 and M4 are off due to a

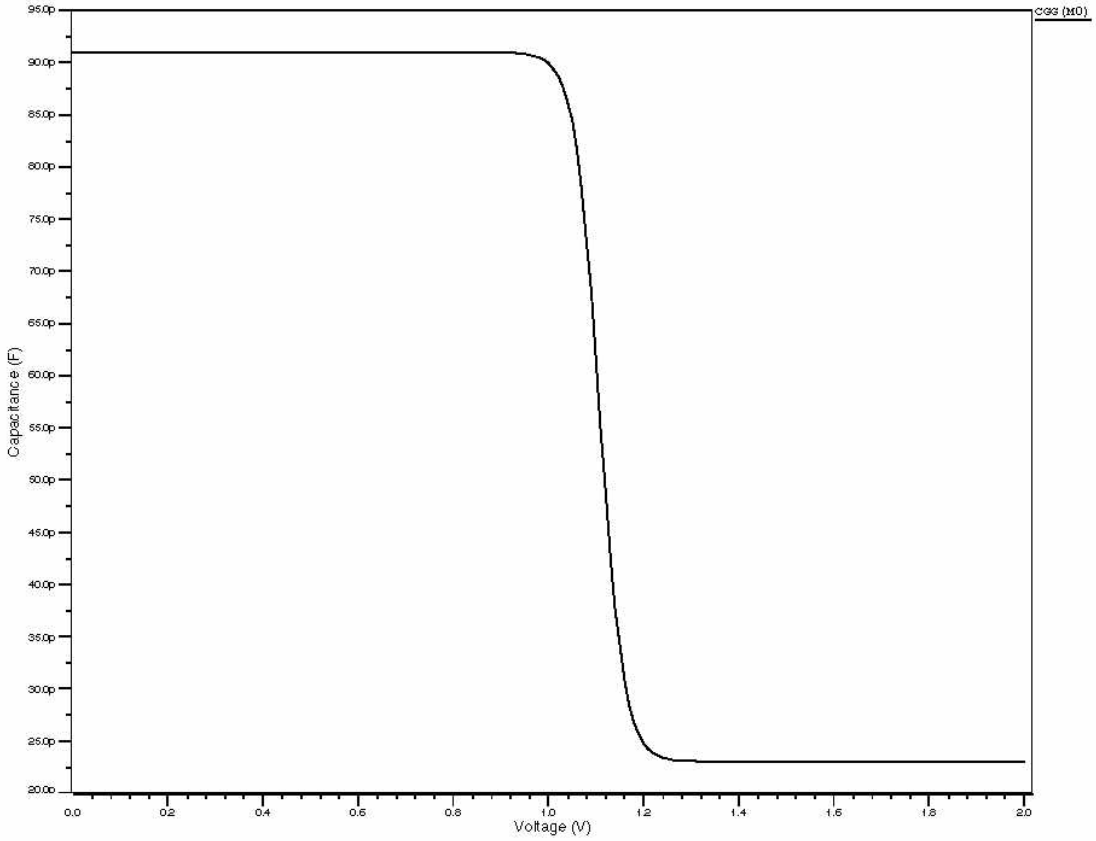


Figure 3-4. Gate capacitance for input termination device cap M7 with source/drain swept from 0 to 2V (Vbulk =0, Vgate=2V.)

ground applied to pins POT_A and POT_B through the POT_DET block (described later.) Transistors M5 and M6 have a gate voltage equal to the common mode output level of the last amplifier stage (see figure 3-1.) They have been sized to draw 4mA through the termination resistors to provide a DC level of 1.2V at the input of the first gain stage.

The negative feedback providing Vgs also generates the opposite voltage of the input referred noise, effectively canceling the device mismatches of the forward path.

This feedback is supplied through a low pass filter to hold the offset cancellation to low frequencies as it would also cancel the input signal if its speed was not controlled.

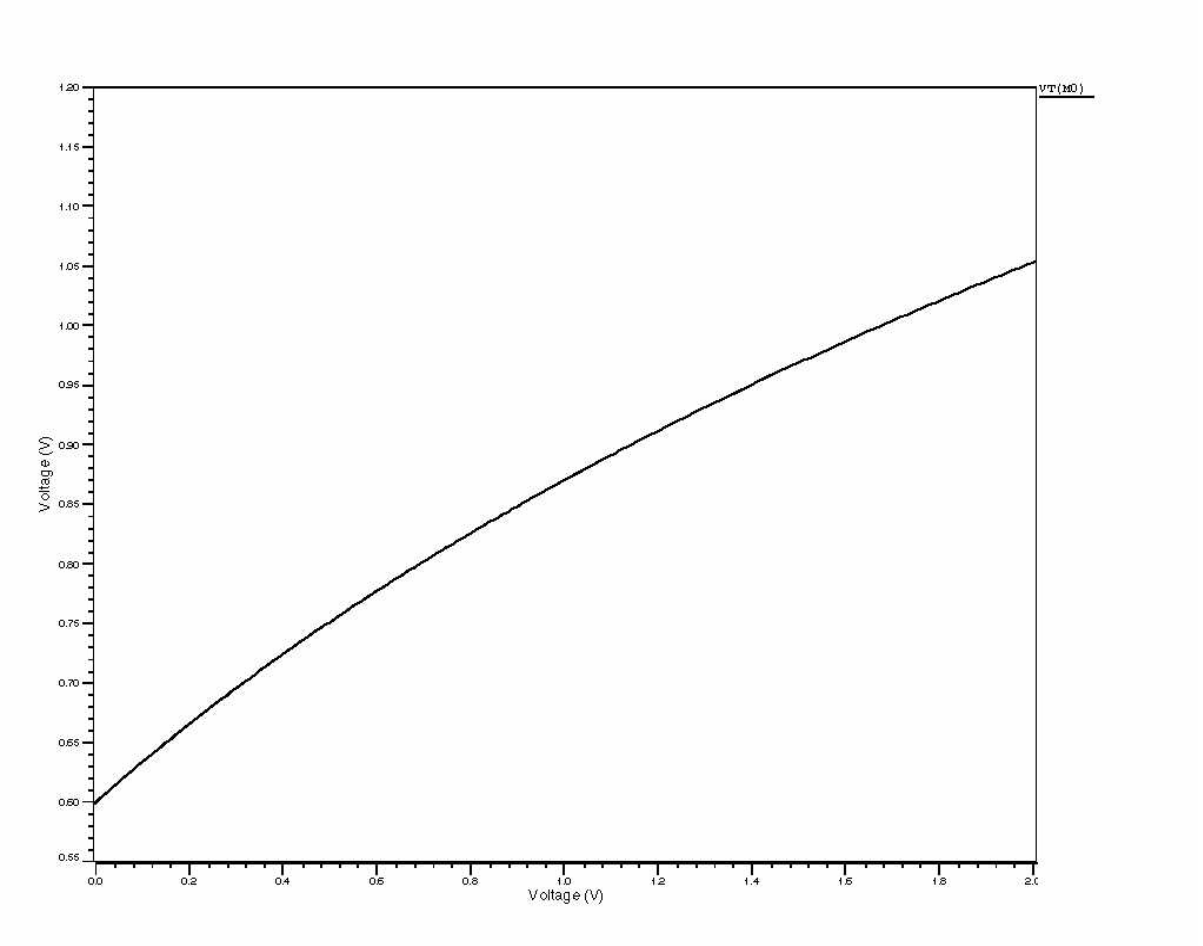


Figure 3-5. Vt as a function of Vsb on device capacitor M7

To further increase circuit sensitivity, it is helpful to have the option to manually set the offset voltage at the input. This IC allows the board designer to add an off-chip 5K ohm potentiometer connected to pins POT_A and POT_B. When this potentiometer is present, the POT_DET circuit will ground the output of the low pass filter and turn off transistors M5 and M6. By tying the wiper arm of this potentiometer to VDD, Vgs of M1 and M2 are skewed to create offsets in each device's current. This current mismatch is mirrored to M3 and M4 where it develops a DC offset voltage at the input of up to +/- 100mV. The optimum level of this offset is found by trial and error during system setup and would be adjusted during installation of the circuit board in the larger system.

First and Second Gain Stages

To achieve the high gain and bandwidth needed from the LIA, a modification of the classic Cherry-Hooper amplifier [4] was used. The original CMOS adaptation of a Cherry-Hooper amplifier uses a transconductance stage to feed a transimpedance stage. The transconductance stage has a high output impedance and the transimpedance stage has a low input impedance due to negative feedback. The cascading of these stages

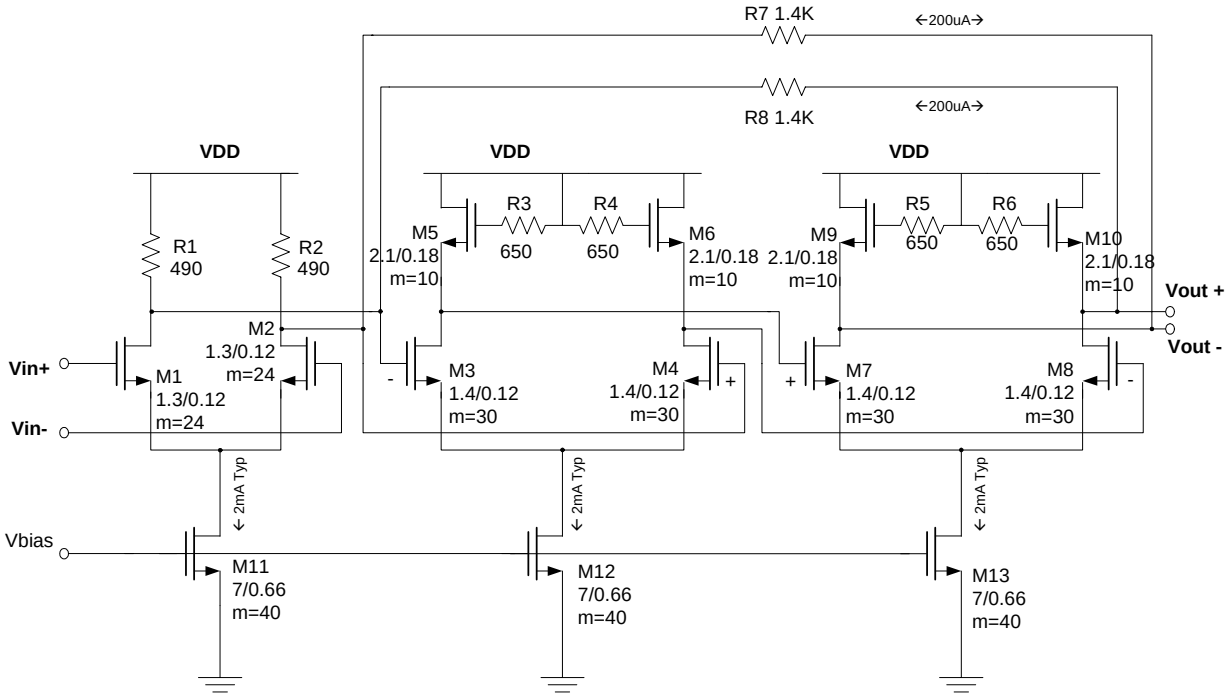


Figure 3-6. LIA gain stage using active inductors

allows for maximum performance because the impedance mismatch results in virtually no effect on the transfer function of one by the other.

In the paper "Front-End CMOS Chipset for Fiber-Based Gigabit Ethernet" [5] it is shown that by putting two forward gain stages inside the feedback loop of the transimpedance amplifier stage, the bandwidth can be increased by 50% for a given gain.

This added bandwidth can be traded for increased gain and reduce the number of stages needed to achieve the desired amplification.

For the transconductance amplifier, the gain is simply defined as

$$A \equiv \frac{i_{out}}{v_{in}} = gm_1 \qquad \text{eq. 3-1}$$

To derive the gain for the transimpedance amplifier, the method of Sedra & Smith's Microelectronic circuits [6] is employed. First, an equivalent circuit representation is created as described in the above reference where Rs is the output impedance of the transconductance stage, R11 is the resistance looking into the feedback network from the input port with the far end of the feedback network shorted, and R22 is the resistance looking into the feedback network from the output port with the feedback terminals at the input shorted.

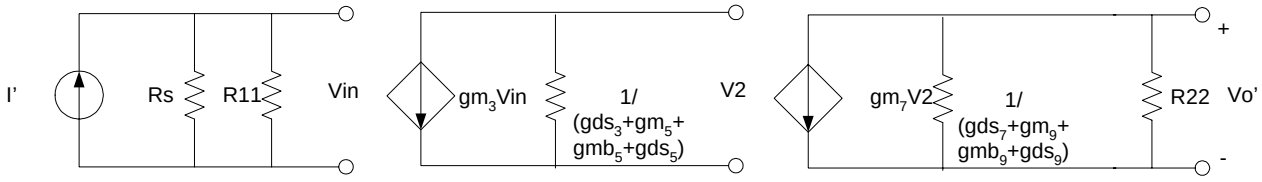


Figure 3-7. Transimpedance stage circuit for finding A

Normally the gds values would be ignored as they are traditionally much lower (high ro) than the other conductances, but in this circumstance they are significant enough to include. Ignoring gmb for the NMOS load devices is also a source of significant error (about 12% per stage) and therefore was also included as needed. Using typical models at room temperature the following values are found from DC simulation:

gm_2=12.8mA/v

Rs=282 ohms

(Rs→gds_2=1.5mA/v || R2=490 ohms)

R_{11}=1.4K

gm_3=14.4mA/v

gds_3=1.8mA/v

gm_5=7.9mA/v

gmb_5=0.7mA/v

gds_5=0.4mA/v

gm_7=14.6mA/v

gds_7=1.8mA/v

gm_9=7.6mA/v

gmb_9=0.7mA/v

gds_9=0.4mA/v

R_{22}=1.4K ohms

The gain A for the transimpedance amplifier is then

$$\frac{v_o'}{i_{in}'} = Rs \,||\, R11\left(\frac{gm3}{gds3+gm5+gmb5+gds5}\right)\left(\frac{gm7}{gds7+gm9+gmb9+gds9+1/R22}\right) = 407\Omega$$

eq. 3-2

The feedback factor β is defined as

$$\beta = \frac{I_f'}{v_o'}\Big|_{v1=0}$$ eq. 3-3

where v1 is the voltage across the input side of the feedback network. In this circuit, this is equal to 1/R22 or 0.714mA/v. The closed loop gain of the transimpedance amplifier is then

$$A_{cl} = \frac{A}{1+A\beta} = 315\Omega$$ eq. 3-4

The total voltage gain through the cell is then

$$A_v = gm_1 * A_{cl} = 12.8mA/v * 315\Omega = 4v/v$$ eq. 3-5

To extend the bandwidth, the NMOS loads in the transimpedance amplifier were configured as active inductors. This is accomplished by placing a resistor in the gate

circuit. Refer to figure 3-8 during the derivation of the impedance transfer function for this device.

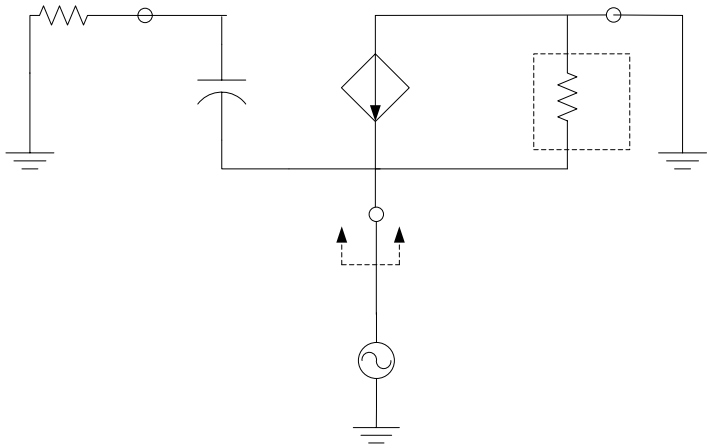


Figure 3-8. Small signal model of NMOS load configured as an active inductor

The impedance looking into the source is derived defined as

$$z_{in} = \frac{v_s}{i_{in}} \qquad \text{eq.3-6}$$

If r_{ds} is ignored, the input current can be written as

$$-i_{in} = i_{gs} + gmv_{gs} \qquad \text{eq.3-7}$$

$$i_{gs} = \frac{0 - v_s}{R_g + \frac{1}{sC_{gs}}} \qquad \text{eq.3-8}$$

$$v_{gs} = \frac{i_{gs}}{sC_{gs}} \qquad \text{eq. 3-9}$$

Substituting eq. 3-8 and eq. 3-9 into eq. 3-7

$$-i_{in} = \frac{-v_s}{R_g + \frac{1}{sC_{gs}}} + gm\frac{\frac{-v_s}{R_g + 1/sC_{gs}}}{sC_{gs}} \qquad \text{eq.3-10}$$

$$\frac{i_{in}}{v_s} = \frac{sC_{gs}}{sC_{gs}R_g + 1} + \frac{gm}{sC_{gs}R_g + 1} \qquad \text{eq.3-11}$$

$$\frac{i_{in}}{v_s} = \frac{gm(\frac{sC_{gs}}{gm} + 1)}{sC_{gs}R_g + 1} \qquad \text{eq.3-12}$$

and finally

$$\frac{v_s}{i_{in}} = \frac{sC_{gs}R_g + 1}{gm(\frac{sC_{gs}}{gm} + 1)} \qquad \text{eq.3-13}$$

This transfer function shows that at low frequencies the impedance looking into the source is 1/gm as expected. At a frequency of 1/(2πRgCgs) a zero is introduced. A pole levels off the impedance again at a frequency of gm/2πCgs. Between the zero and the pole the impedance is sCgsRg/gm. Recalling that the s domain impedance of an inductor is sL, it follows that the impedance looks like an inductor L=RgCgs/gm between the zero and the pole.

To achieve this effect, care must be taken in sizing the NMOS loads to ensure gm/Cgs is greater than 1/RgCgs. Another drawback to the use of a zero is that it adds a frequency dependent phase shift which translates to time domain jitter on the eye pattern.

Third Gain Stage

The third gain stage differs from the previous two only at the output—the loading there is resistive instead of an active inductor NMOS. This was done to add enough gain at the low corners to get by with a three-stage amplifier. (Additional stages decrease the overall bandwidth and increase the corner variation, which was significant in this design.)

By changing the output load to resistors, the gain of this stage was increased to 6.3v/v at the expense of bandwidth.

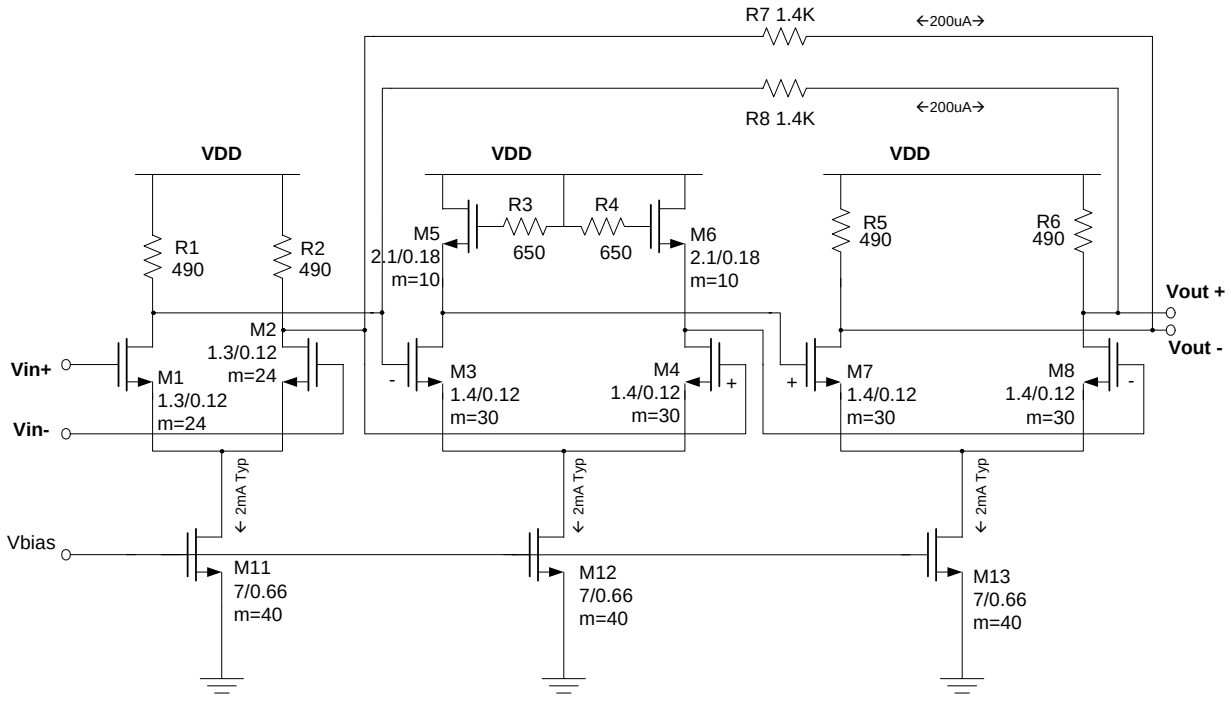


Figure 3-9. Modified gain stage used for third stage

LIA Output Buffer

The output buffer is a Current Mode Logic (CML) buffer. It provides a final gain boost as well as shifting the output to CML signal levels (1.2VPP differential in this design.)

The operation is straightforward. The input signal is expected to be large enough to completely steer the 1.5mA current to one leg of the amplifier. This will result in an output swing from VDD to VDD-IR (1.8-400*1.5m=1.2V at typical.) The bandwidth of this cell is limited by the discharge time of C_{load} through R5 or R6. Therefore it is simply $1/2\pi RC_L$. For 10 gigabit operation, this cell can drive up to approximately 60fF. The phase frequency detector following the LIA has an input load of 20fF. The physical

placement of the LIA is very close to the PFD to minimize parasitic routing capacitance and preserve the margin.

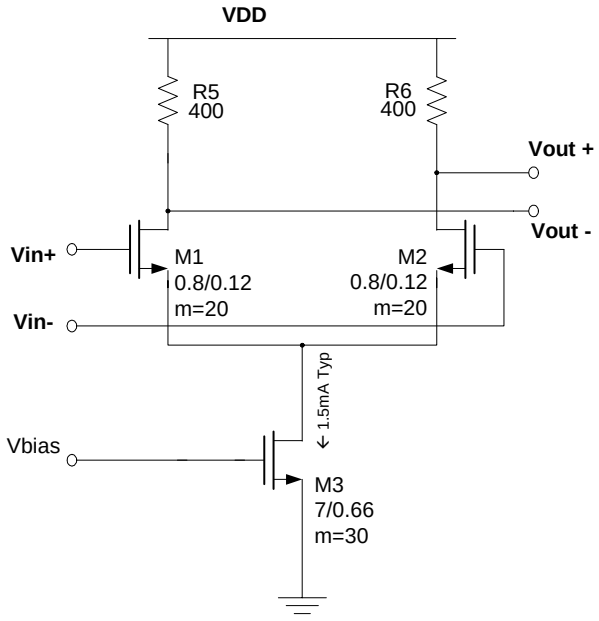


Figure 3-10. LIA output buffer

Low Pass Filter

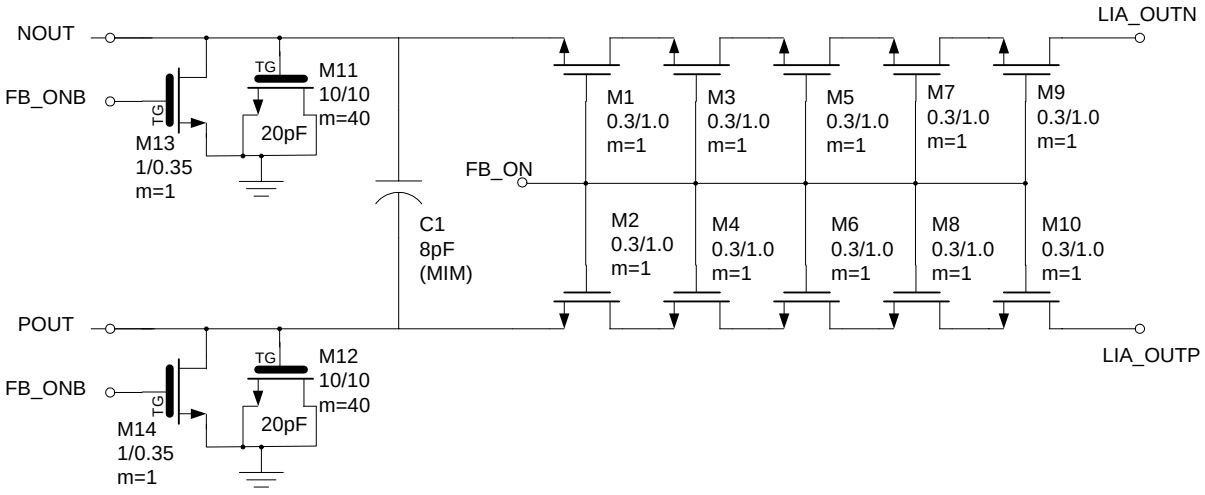


Figure 3-11. Feedback path low pass filter

The LIA's automatic offset cancellation mode requires the feedback be limited to low frequency to avoid canceling the input data. This is accomplished using a single pole

RC filter. Because the actual value of the pole is not critical as long as it is well below the lowest frequency of the data, triode transistors were used. This was a significant space savings over the use of resistors at the expense of a much greater variation over process.

The low frequency limit of the LIA was specified at 50MHz. With 40dB of gain in the forward path, and one pole in the feedback loop, the pole must be more than 2 decades down from this low frequency operating limit, or less than 500kHz. The filter has five NMOS devices in series that are biased in the linear region. This configures them as voltage controlled resistors with a resistance defined as [7]

$$r_{ds} = \frac{1}{u_n C_{ox}\left(\frac{W}{L}\right)\left(v_{gs} - v_t\right)} \qquad \text{eq. 3-14}$$

At typical conditions, each device has an r_{ds} equal to about 110KΩ.

The capacitor at the output node is a combination of thick gate NMOS devices and metal-insulator-metal (MIM) capacitors. The MIM capacitors are created using plates of routing metal high in the routing stack. This allows them to be placed directly over the device capacitors and utilize otherwise wasted space. Additionally, the MIM capacitor is connected differentially, which doubles its effective value. The MIM cap contributes ~45% of the total capacitance and therefore reduced the total area used for this capacitance by an equivalent amount. The total effective capacitance for each path is ~36pF. This results in a pole of about 10KHz. This value is sufficiently far from the area of concern that variations over process and temperature should not affect circuit performance.

To disable the feedback loop, the gates of M1 through M10 are pulled low by the Potentiometer Detector block. Additionally, M13 and M14 are turned on pulling the output nodes low.

Potentiometer Detector

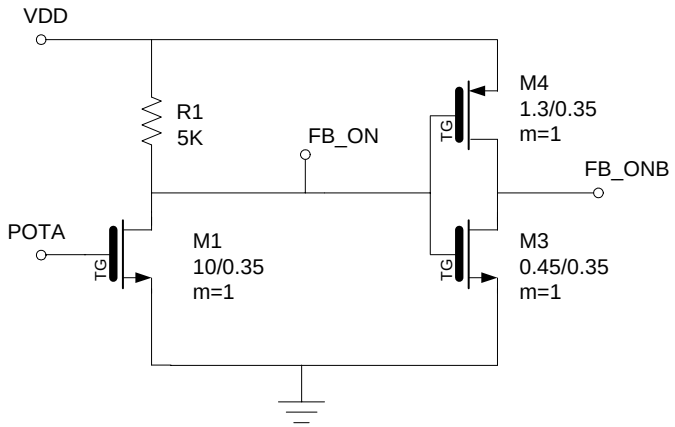


Figure 3-12. Potentiometer detect circuit

This block's function is to determine whether the LIA offset is being controlled by an external potentiometer as described earlier and if so, disable the feedback path. If a potentiometer is connected to the offset correction pads, a voltage of around 1 volt will be present on the POT_A and POT_B nodes. When there is no potentiometer, the nodes will be pulled low by the diode connected devices in the LIA front end. By connecting an NMOS to one of these nodes, an enable signal can be generated. When there is no potentiometer, transistor M1 is off and node FB_ON is pulled to VDD through resistor R1. An inverter consisting of devices M4 and M5 creates a complimentary low and each is sent to the feedback block. When node POTA goes high due to the presence of an external potentiometer, current flows through M1 and the voltage on node FB_ON is set by I_{M1}*R1. M1 is an NMV3 device which is 3.3V tolerant but has a lower Vt than the

standard thick gate transistors at 375mV. This lower Vt ensures M1 is on hard enough to pull FB_ON close to zero volts under all conditions.

Biasing

The bias circuit for this limiting amplifier was not part of this design but done as another portion of the IC and re-used by each block designer. Because this bias block is designed to track and minimize the process variation of the on-chip resistors, its function is described here.

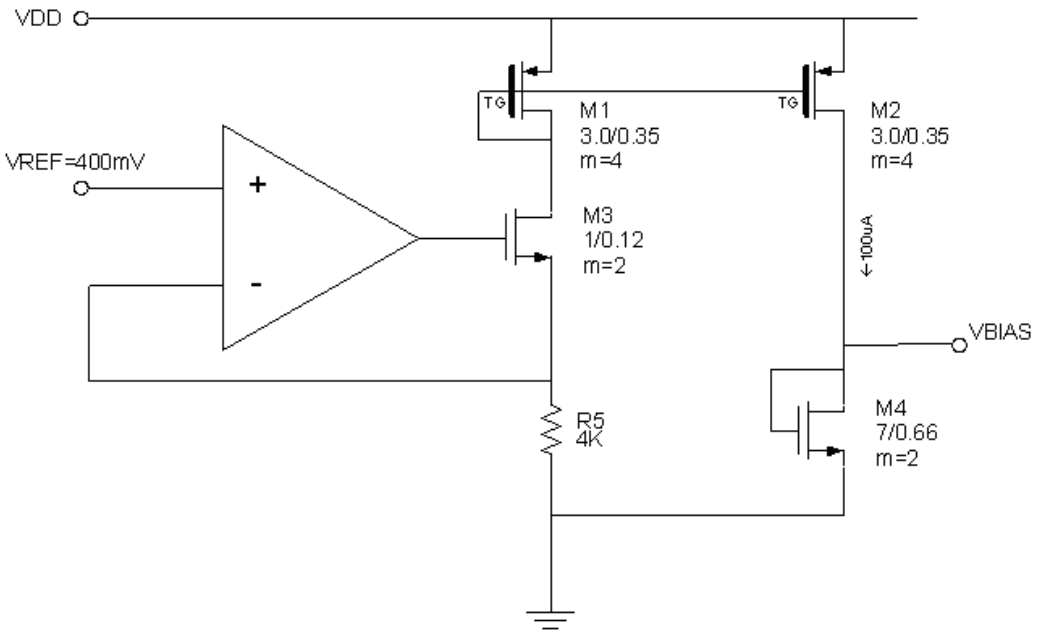


Figure 3-13. LIA bias circuit

A reference voltage of 400mV is generated through a voltage divider and applied to a terminal of an op-amp. The output of the op-amp drives an NMOS source follower that pushes a current through a reference resistor. The voltage generated by this current is fed back to the other op-amp terminal. The loop forces an IR product equal to 400mV independent of the resistor variation. The current forced through the reference resistor is pulled from a diode connected PMOS. This device is half of a current mirror that drives

the equivalent current through a diode connected NMOS equal in dimension to the current sources in the LIA (and other blocks on the chip.) The result is a constant DC common mode voltage at the output of all stages that are resistively loaded.

CHAPTER 4
LAYOUT

Top Level

For a circuit to operate in the GHz frequency range, attention to layout parasitics is critical. Also, symmetry must be maintained to minimize any offsets to preserve the sensitivity of the LIA. Figure 4-1 is a screen capture showing the complete circuit with applicable pads. The main LIA is the section between the two blocks labeled "cap." Every attempt was made to balance the layout on each side of a vertical line through the center of this block. Pads for VDD and the signal return were reserved on each side so that the routing would be identical with respect to the data in pads DIN_P and DIN_N. Pin limitations prohibited symmetrical Ground pads, but Ground was supplied through a

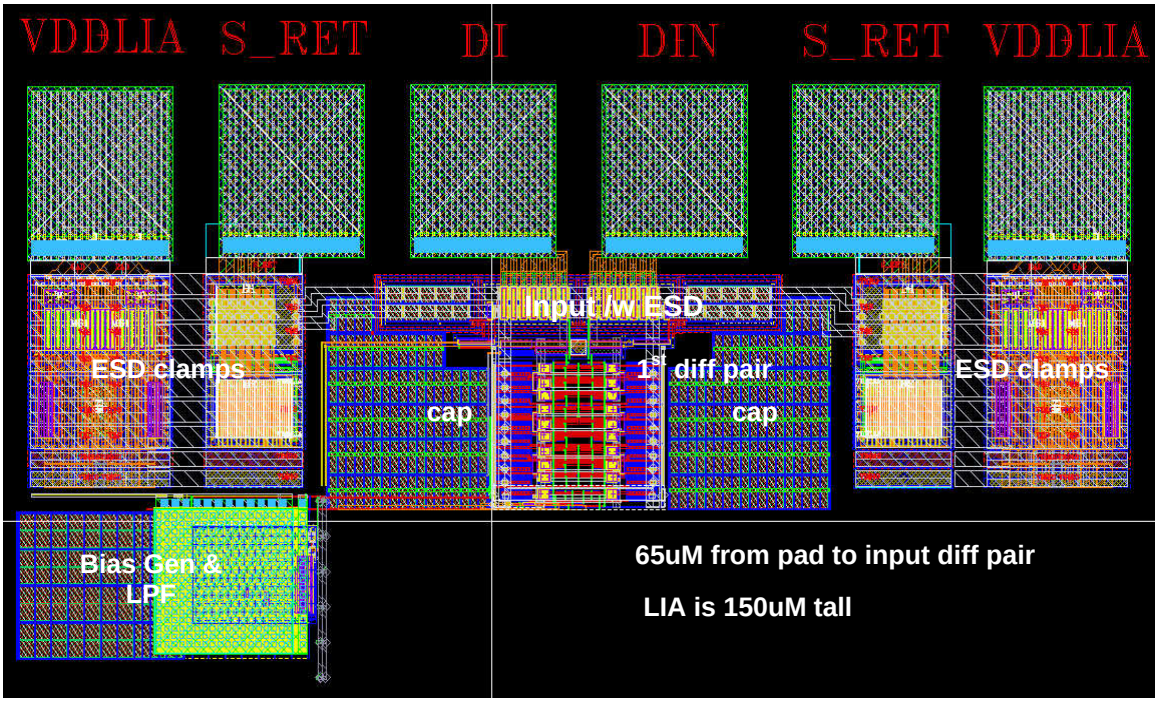


Figure 4-1. Layout of limiting amplifier with pads, biasing, and ESD.

pad ring and symmetrically connected on each side of the block. The input routing resistance was kept low by using 10um lines for the connection between the pad and the input block. Maximum via connections were made between metal layers, also to minimize resistance.

Input Stage

The input block was floor planned as a short wide block so that the differential pair of the first gain stage is as close to the pads as possible—this path still measured 65um. The large capacitors from the input stage were placed along the sides of the forward path because of the area required for these devices.

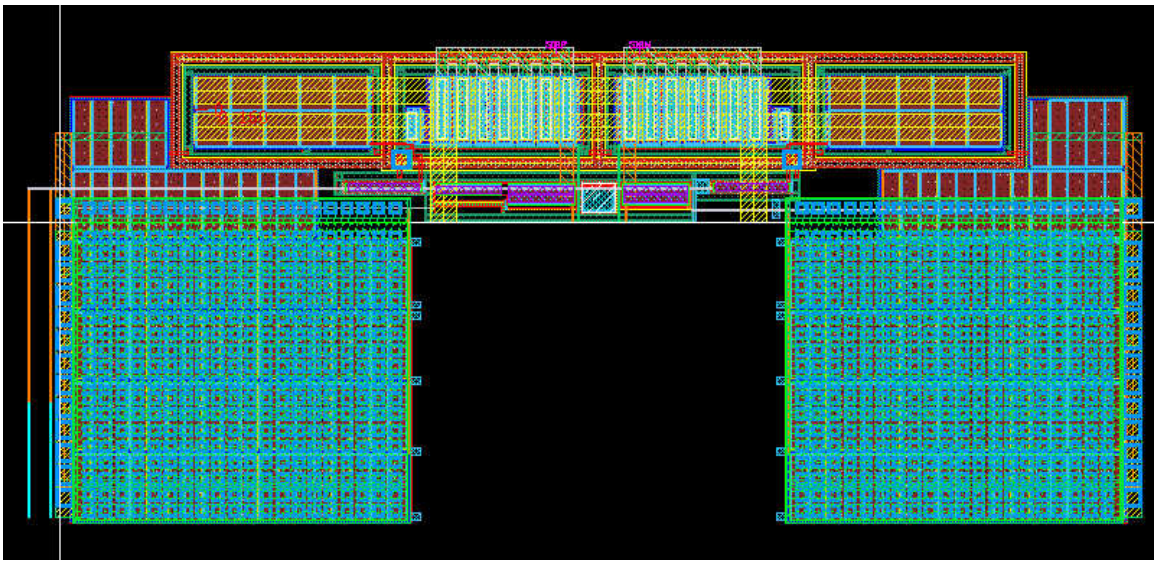


Figure 4-2. Input stage with termination capacitors

Gain Stage

Figure 4-3 shows the gain stage layout. To minimize parasitics for these stages, the current source was divided in two and placed at the outer edges of the block. This allowed the shortest distance between stages. The three differential pairs and NMOS loads are visible in the center with the resistors placed just to the outside of the transistors. Ground buses are along both outside edges and VDD was routed over the

resistors to keep any parasitic capacitance and noise away from the high speed signal path.

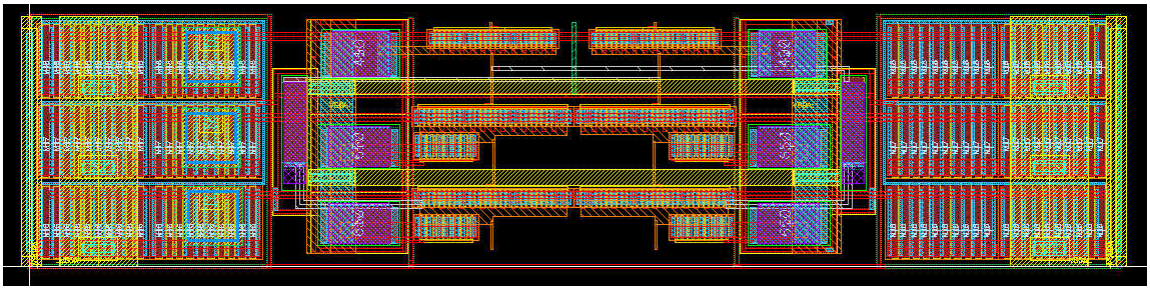


Figure 4-3. LIA gain stage layout

Matching efforts were limited to keeping the differential pairs as close as possible to each other. Interdigitation and common centroid methods were considered, but the additional routing required for those topologies was excessive and determined to be too detrimental to the bandwidth.

Output Buffer

The layout of the output buffer followed the strategy of the gain stages; it has the differential pair in the center, then the load resistors, and finally the current source split in two on the outside edges.

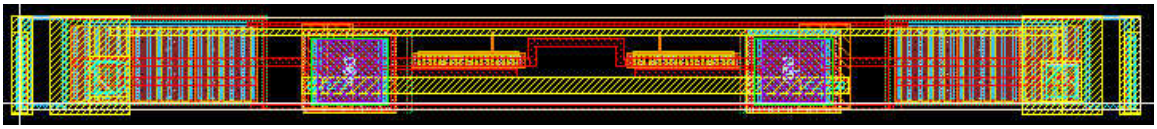


Figure 4-4. Output buffer

Low Pass Filter

The low pass filter contains the triode NMOS devices and a large device/MIM capacitor array. The cell was floorplanned so that the NMOS were tight to the output of the third gain stage to minimize routing to this block. These devices are located at the top center of the horizontal stripe at right in figure 4-5 (small red rectangle.) However, after

tapping the forward path signal, routing is not an issue and the capacitor was placed where space was available far to the left.

Figure 4-5. Low pass filter

Routing Capacitance

The post-layout capacitance was extracted using STAR. The output of this program is an extensive netlist that reports capacitances between all nets in a design. This netlist is included in the Eldo input file for all transient and AC simulations. The output also contains a summary of total capacitance for each net. The total capacitances from this summary for the signal path are reported in table 4-1.

Table 4-1. Parasitic capacitances along signal path

Node	C value	Location
INP	0.153pF	input including bond pad
INM	0.144pF	
PIN	12.0fF	1st stage input node
NIN	11.1fF	
XI47.SIG1P	25.1fF	1st stage gm output
XI47.SIG1M	24.9fF	
XI47.SIG2P	25.4fF	1st stage source of 1st active inductors
XI47.SIG2M	24.5fF	
ST1P	27.2fF	1st stage output/2nd stage input node
ST1M	26.8fF	
ST2P	25.5fF	2nd stage gm output
ST2M	25.2fF	
XI73.SIG1P	26.8fF	2nd stage source of 1st active inductors
XI73.SIG1M	24.9fF	
XI73.SIG2P	25.9fF	2nd stage output/3rd stage input node
XI73.SIG2M	27.1fF	
XI48.SIG1P	24.0fF	3rd stage gm output
XI48.SIG1M	24.5fF	
XI48.SIG2P	25.1fF	3rd stage source of 1st active inductors
XI48.SIG2M	25.6fF	
LIA_OUTP	21.5fF	3rd stage output/buffer stage input node
LIA_OUTM	21.9fF	
LATCH_INP	9.13fF	buffer stage output node (not loaded)
LATCH_INM	8.56fF	

CHAPTER 5
SIMULATION RESULTS AND MODELING ISSUES

Simulation Tools and Methodology

All simulations were run using ELDO by Mentor. This is a simulator that is very similar to HSPICE. It also has a transient noise feature that produces transient waveforms while including the effects of 1/f and thermal noise for devices.

The Synopsis tool STAR was used to extract node capacitance values from the layout. These capacitances were then included in the netlist for transient and AC simulations to verify bandwidth performance.

Simulations for the Limiting Amplifier were performed over 17 parameter combinations represented by a 4 letter acronym defined as

<M><R><T><V>

where M is the transistor speed, R is the resistor value, T is temperature and V is the supply voltage. Table 5-1 defines the process corners simulated on this design.

The following simulations were performed to verify operation of the limiting amplifier. They were performed at all corners unless otherwise noted:

DC Operating point simulations

- Ensure all transistors are in saturation at above corners with >200 mV Vds above Vd_{sat}.
- Record maximum supply current.
- Make sure Vgs or Vgd is < 1.8V at all times, and does not exceed 1.2V during normal operation.

Table 5-1. Simulation corners

Corner	Transistors	P+Poly Resistors	Temp ºC	VDD
FHCH	fast	high	0	1.935 V
FHCL	fast	high	0	1.665 V
FHHH	fast	high	100	1.935 V
FHHL	fast	high	100	1.665 V
FLCH	fast	low	0	1.935 V
FLCL	fast	low	0	1.665 V
FLHH	fast	low	100	1.935 V
FLHL	fast	low	100	1.665 V
SHCH	slow	high	0	1.935 V
SHCL	slow	high	0	1.665 V
SHHH	slow	high	100	1.935 V
SHHL	slow	high	100	1.665 V
SLCH	slow	low	0	1.935 V
SLCL	slow	low	0	1.665 V
SLHH	slow	low	100	1.935 V
SLHL	slow	low	100	1.665 V
TTTT	typ	typ	25	1.8 V

DC Transient simulations

- With extracted layout parasitic capacitances, verify output of LIA is 1.2VPP differential when a 10mV differential input is applied.
- Generate eye diagram using different data patterns (010101 to 011111101111110…) at minimum and maximum input values and record zero crossing jitter.
- Run Eldo .NOISETRAN simulations and record zero crossing jitter.

  **This will be run only at suspected worst-case corners of gain and pattern-dependent jitter.

AC simulations

- Verify small signal Gain and Bandwidth greater than 42dB and 7 GHz

- Verify phase margin of feedback loop in gain stage is >50 degrees.

Other

- Monte Carlo simulations (typical only)

Simulation Results

DC Operating Point

All transistors were checked for saturation and overdrive across the input common mode range. All devices exceeded the 200mV over Vd_{sat} at corners with the following exceptions:

- Current source M13 in all three gain stages: 100mV over Vd_{sat} at SLHL
- Current source M11 in 2^{nd} and 3^{rd} stages: 100mV over Vd_{sat} at SLHL

The worst-case current draw was 33mA for the block at 1.935 volts—63.9mW of power. The typical current draw is 25mA consuming 45mW.

DC Transient Simulations and AC Gain/Bandwidth

The block was run at all 17 corners with a 10mV differential input and the pattern dependent jitter, eye opening, gain, and high/low 3dB bandwidth were recorded. The numerical results are shown in table 5-2. Additional transient simulations were run with larger input signals; all results were equal or better to those in table 5-2.

Table 5-2. AC and transient simulation results

CORNER	GAIN	$3dB_L$	$3dB_H$	JITTER	EYE
FHCH	55.7dB	1.9M	6.7G	8.7 pS	1.41 V
SHCH	53.2dB	0.3M	6.6G	9.6 pS	1.31 V
FHCL	53.0dB	1.0M	6.3G	11.0 pS	1.25 V
SHCL	50.4dB	0.1M	6.3G	11.0 pS	1.13 V
FHHH	50.2dB	0.7M	5.9G	11.6 pS	1.38 V
SHHH	47.7dB	0.2M	5.9G	10.8 pS	1.24 V
FHHL	47.3dB	0.4M	5.6G	12.6 pS	1.10 V
SHHL	44.7dB	0.1M	5.6G	11.0 pS	1.03 V
FLCH	48.1dB	1.0M	7.8G	1.8 pS	1.41 V
SLCH	44.9dB	0.1M	7.8G	0.8 pS	1.25 V
FLCL	45.7 dB	0.5M	7.5G	2.2 pS	1.22 V

Table 5-2. Continued

CORNER	GAIN	$3dB_L$	$3dB_H$	JITTER	EYE
SLCL	42.3dB	0.1M	7.5G	1.4 pS	1.02 V
FLHH	41.7dB	0.3M	6.9G	2.6 pS	1.02 V
SLHH	38.3dB	0.6M	6.9G	3.5 pS	738 mV
FLHL	39.1dB	0.2M	6.6G	2.9 pS	798 mV
SLHL	35.7dB	0.1M	6.5G	3.0 pS	561 mV
TTTT	48.5dB	0.3M	6.9G	6.7 pS	1.27 V

Worst-Case Corners .NOISETRAN Simulations

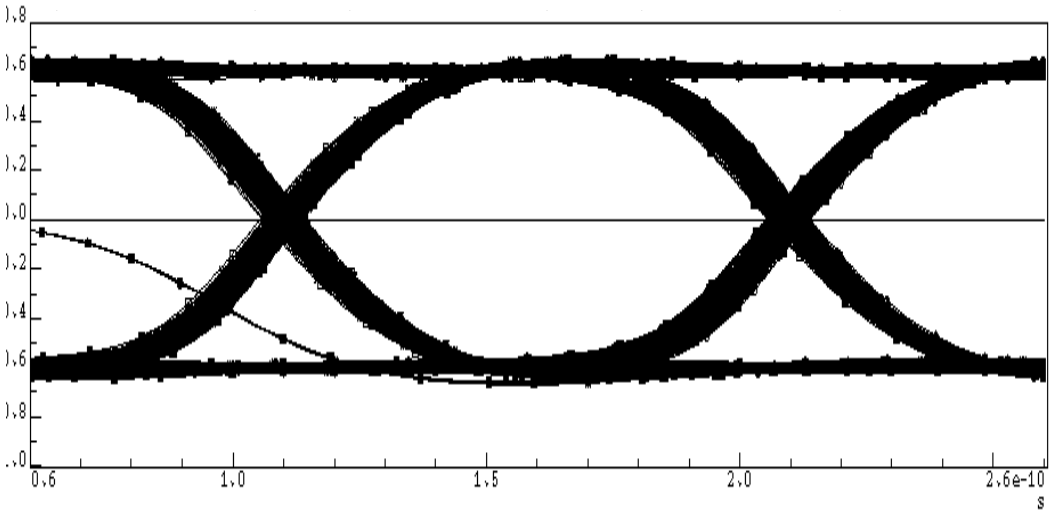


Figure 5-1. Typical case eye with 10mV differential input (8.6pS peak to peak jitter)

To examine the effects of noise on the eye diagram, a high gain corner (FHCH), low gain corner (SLHL), and high jitter corner (FHHL) were selected to be run in Eldo with device noise included. A typical case was also run with 10mV differential and 30mV differential inputs to compare with the above.

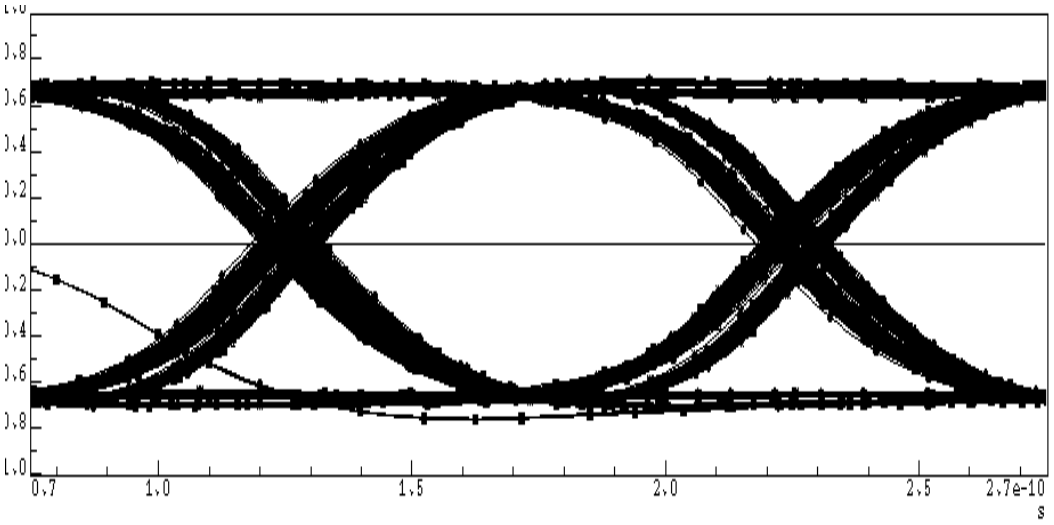


Figure 5-2. FHCH corner with 10mV differential input (13.5pS peak to peak jitter)

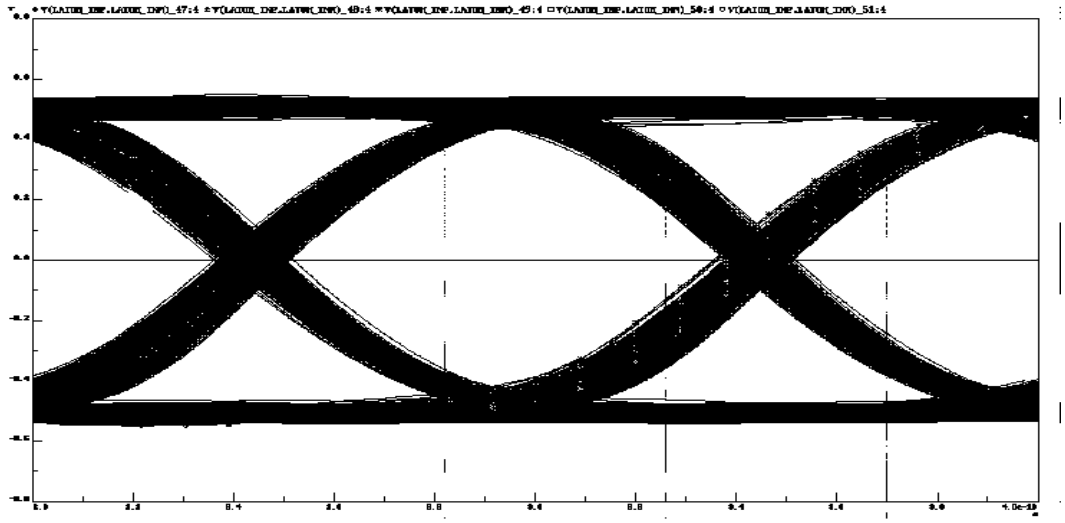


Figure 5-3. FHHL corner eye with 10mV differential input (15.8pS peak to peak jitter)

The Eldo .NOISETRAN simulation allows a selected number of consecutive transient simulations to be run with a different 1/f and thermal noise figure randomly selected for each device from the noise models. The resulting set of output waves gives an accurate portrayal of the total output waveform if enough simulations are run. For the recorded eye diagrams, 50 transient simulations were run with a wideband input data stream to incorporate the pattern dependent jitter.

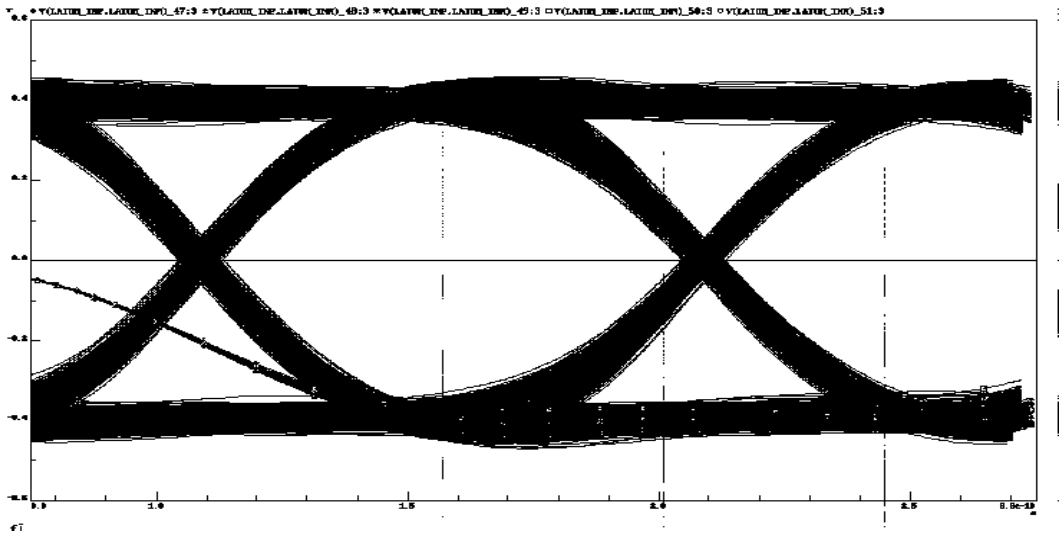


Figure 5-4. SLHL corner eye with 10mV differential input (9.1pS peak to peak jitter)

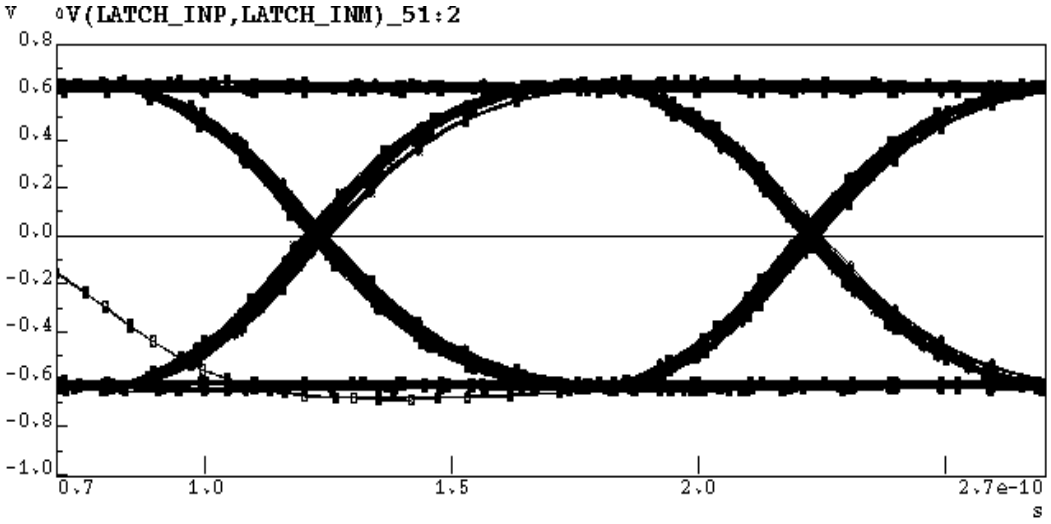


Figure 5-5. Typical eye with 30mV differential input (5.2pS peak to peak jitter)

AC Stability Simulations

There are four separate feedback loops in this block—the outer differential offset correction loop, and the three resistive feedback loops in each of the gain stages. The outer offset correction loop is very stable due to a low pass filter pole at ~10KHz and a

resulting phase margin of 90° at all corners. A Bode plot of the gain and phase of this loop is shown in figure 5-6.

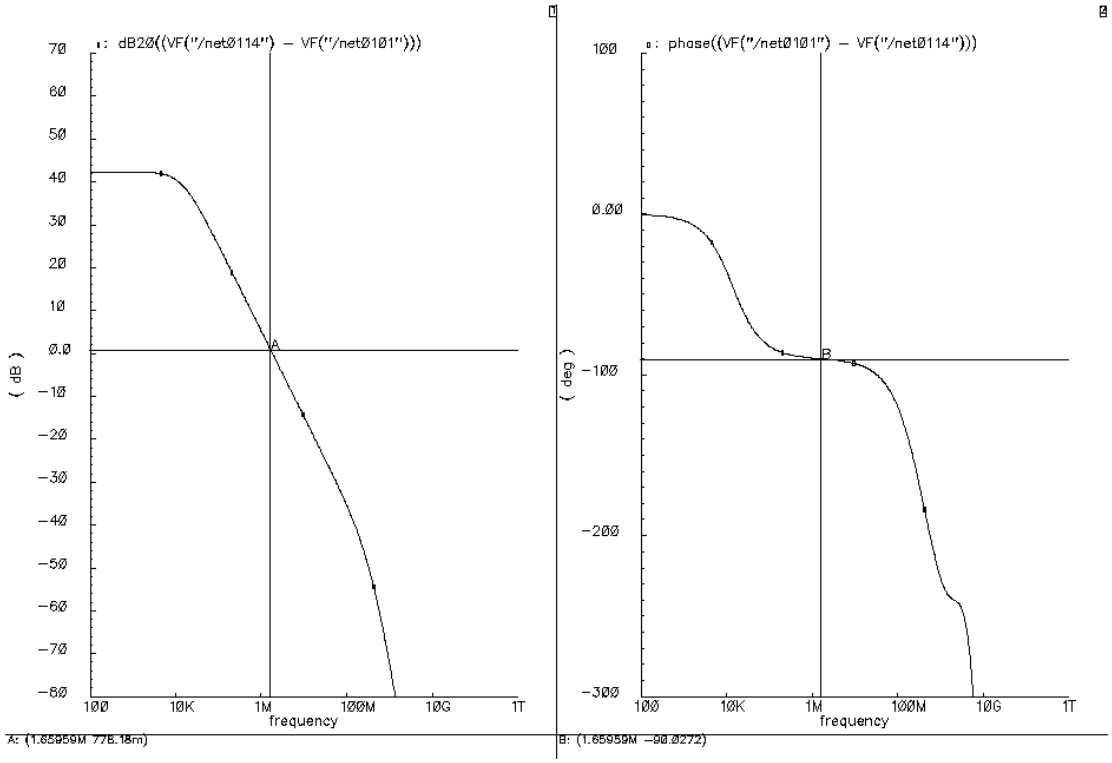


Figure 5-6. Bode plot of differential offset correction feedback loop

The three resistive feedback loops in the gain stages are similar to each other; the major difference being the increased loop gain in the last stage with resistive output load. They all have an open loop gain of less than one across the complete frequency band due to the relatively low forward path gain and the feedback factor of ~0.2. For example under typical conditions the forward path has a gain of 4.6dB, or 1.7V/V. (Note this gain excludes the input trans-conductance stage gain which is not in the loop.) Multiplying this by the feedback factor 0.16, the DC loop gain is about 0.28V/V or –11dB. Even with

the inductive peaking of 3-4dB, the open loop gain never goes positive. An example Bode plot is shown in figure 5-7.

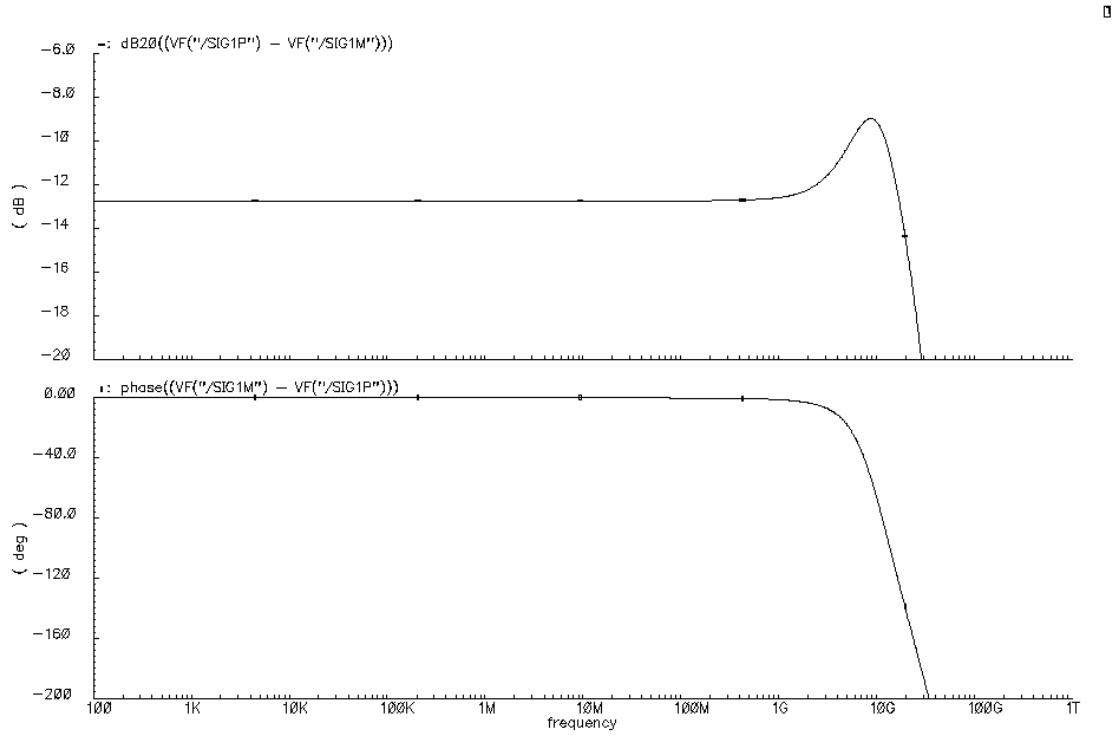


Figure 5-7. Gain stage Bode plot

Other Simulation Results

Monte Carlo simulations were run by creating mismatch in the circuit netlist. No appreciable difference in AC response or the eye diagram was recorded.

Performance Summary

GAIN: 56dB-36dB

BANDWIDTH: 7.8GHz-5.6GHz

TOTAL JITTER (PP): 8.6pS typical; 15.8pS worst-case (10mV differential input)

EYE OPENING: 1.2V differential typical; 561mV worst-case

Modeling Issues

During the design of the offset cancellation loop, a modeling issue was discovered. As the devices M5 and M6 in the input termination and control block were being sized, AC sweep simulations revealed that v_o/v_i was increasing at high frequency. This is in opposition to the known behavior of gain rolling off as a transistor reaches the limits of its operating frequency. This frequency where the transistor gain is reduced to unity is referred to as f_T and is defined as [7]

$$f_T = \frac{gm}{2\pi(C_{gs} + C_{gd})} \qquad \text{eq. 5-1}$$

In high-speed circuit design transistors would normally be sized to maximize ft. For this UMC process, a device f_T can be over 100GHz.

Because the feedback path for offset cancellation was to operate at only low frequency, this was not a requirement for devices M5 and M6. Since these devices had to source a particular current and had a pre-determined Vgs set by the DC common mode output of the third gain stage, gm through adjustment of W and L was the tunable variable.

During AC sweeps of the feedback path, it was noted that the voltage gain apparently increased at frequencies somewhere over a 1 GHz. To isolate the cause the circuit was methodically simplified until a single transistor with a resistive load remained as shown in figure 5-8.

Measuring the voltage gain of this circuit over frequency produced the plot shown in figure 5-9. The low frequency gain is correct at about 1v/v, but the circuit gain begins

to increase in the low GHz range and settles out with a gain of about 4v/v at very high frequency.

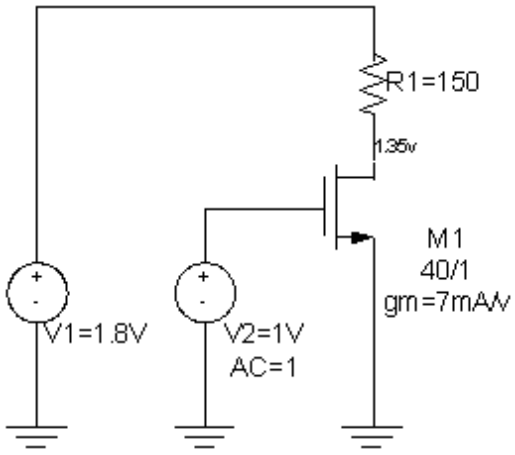


Figure 5-8. Test circuit for incorrect gain behavior

To determine the explanation, an investigation into the models was done. It was found that the default setting in the BSIM3 models calculate the transconductance of the voltage controlled current source such that it increases with frequency [8]. This model parameter is not the device transconductance gm defined as $\partial I_d/\partial V_{ds}$ but a transconductance given as

$$gm^{+} = gm - j\omega(C_{dg} - C_{gd}) \qquad \text{eq. 5-1}$$

where gm, C_{dg}, and C_{gd} are independent of frequency. This equation results from an assumption that the transistors are operating in a quasi-static state. This is true when the frequencies of operation are far from the device f_T. However, in the test case, the device f_T was somewhat low at ~3GHz due to its sizing. Therefore as the AC sweep approaches 3GHz, the model breaks down.

To partially correct this error, a model flag called XPART can be modified. XPART controls the charge partition between the drain and the source. For XPART=0, the charge is partitioned 60% and 40% respectively. XPART=1 puts 100% of the charge

at the source. This results in a C_{dg}-C_{gd} value of zero and removes the frequency dependency of gm^{+}.

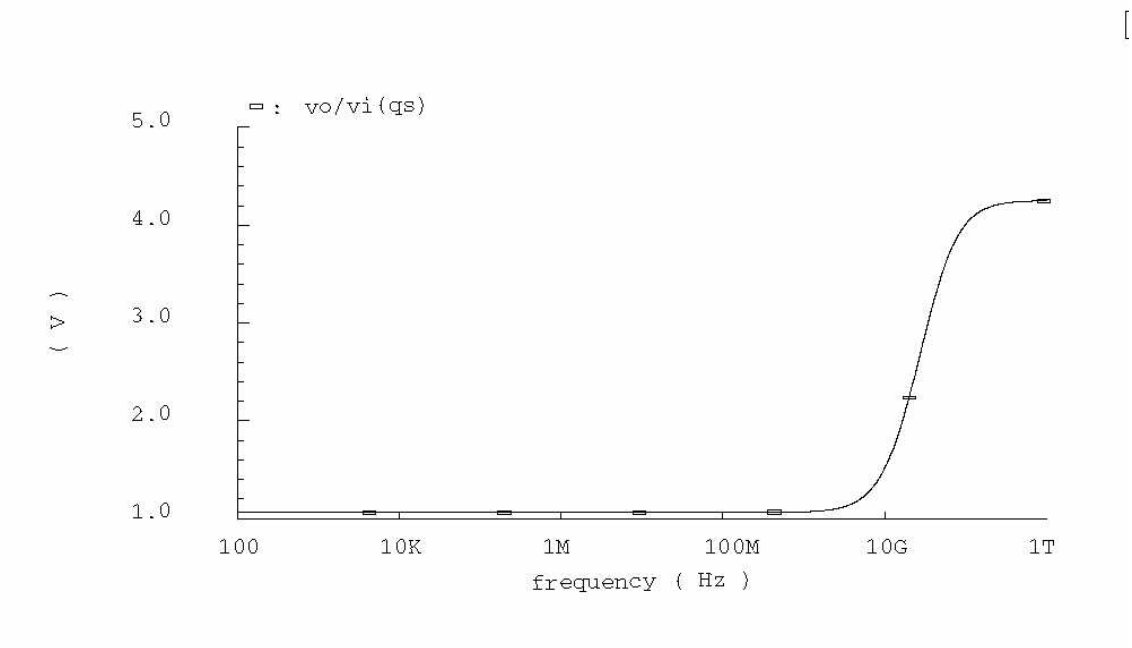


Figure 5-9. Test circuit gain plot

This is still not an accurate modeling of the device behavior. It is useful only in that it restores a qualitatively correct gain behavior at frequencies above a device f_T. Since most circuits will operate below this region, it is not recommended to routinely simulate with XPART=1.

A plot showing the resulting voltage gain with XPART=1 is overlaid on the original in figure 5-10.

According to [8], BSIM3 has a flag called NQSMOD which can be used to turn on non-quasi-static modeling, but it is not recommended for AC simulations. BSIM4 has improved the non-quasi-static shortcomings of BSIM3 by including the flag ACNQSMOD. Setting this to 1 will invoke equations for gm, C_{dg}, and C_{gd} that are

frequency dependent and result in a gm^+ reduction with frequency. Since BSIM4 models were not available, this was not tested.

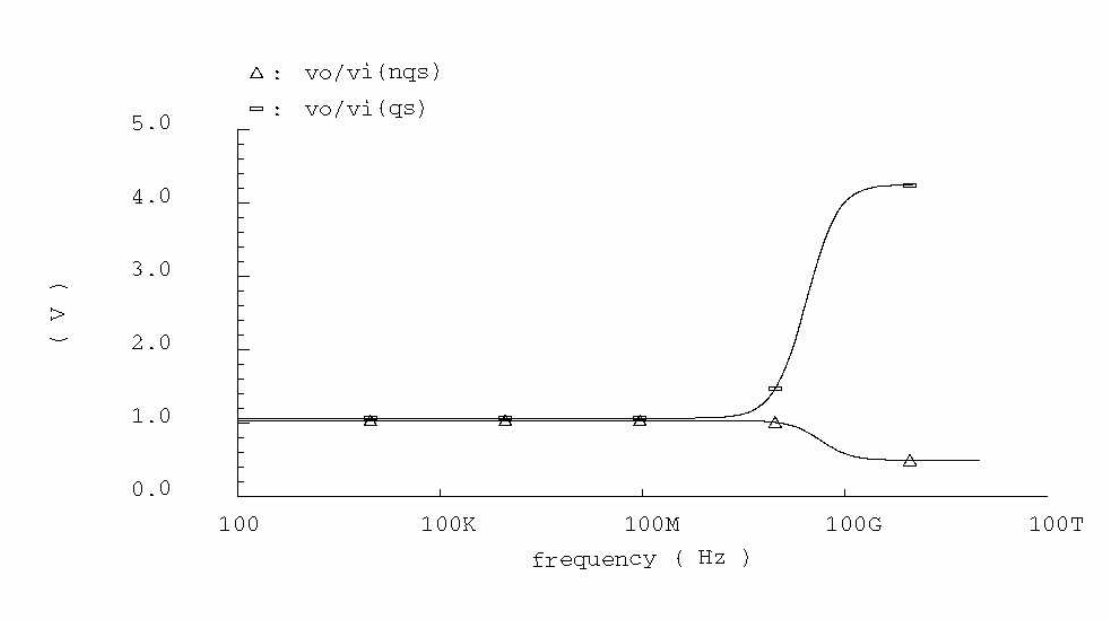


Figure 5-10. Gain plots with XPART=0 and XPART=1

CHAPTER 6
MEASUREMENT RESULTS

Testing Strategy

Because the limiting amplifier is part of a full deserializer IC, the output of the block cannot be accessed directly. This means that all testing must be done on an output that has passed through not only the LIA, but the demultiplexer and output buffering at a minimum. If access to the LIA output was available, conformance to specifications could be checked directly. For bandwidth, an AC signal could be applied to the input and the frequency increased until attenuation is observed. Similarly for gain, a small amplitude input would be applied and the output measured to extract the gain.

Because the blocks following the LIA are CML cells, in the absence of an input, the output of these later blocks will tend to switch fully to one logic level or the other based on circuit mismatches just as standard CMOS logic will. Therefore as frequency is increased and the LIA begins to lose gain, no reduction in the output signal will be measured. Instead the output will no longer follow the input value. For example, if a sine wave is considered a data string, it is the equivalent of a 101010 pattern. Applying this to the input of the deserializer the expected output would be a demultiplexed 101010 pattern. Once the output of the LIA begins to attenuate, the demultiplexed pattern would maintain its amplitude, but noise would begin to corrupt the signal in the demultiplexer and the output would no longer be 101010. It might begin to look something like 111010.

A similar effect would be seen as the input amplitude falls below the minimum level that the LIA can amplify to the needed CML voltage swing. The eye diagram driving the demultiplexer would close becoming more susceptible to noise and errors in the bit pattern would appear more frequently. Examples of the effect of gain and bandwidth limitations on the data eye are shown in figure 6-1.

These mismatches in the pattern are called bit errors. The lower the amplitude of the LIA output, the greater the number of bit errors. Counting the number of errors that occur over a period of time is referred to as measuring the bit error rate (BER.) Because noise is considered Gaussian, there will always be some statistical probability that noise will be great enough to corrupt a signal and cause an error. Therefore the rate will never go to zero. For this IC an error rate of less than one error every billion bits ($1x10^{-9}$) was set as the threshold for consideration as "error free" operation.

Since the only output that can be measured is a bit value of "1" or "0", a method to characterize the LIA using the bit error rate must be employed. Ideally, the output of the LIA should have characteristics uncorrelated to the input down to the sensitivity threshold. Therefore, to find the gain, a known data pattern can be applied to the input of the LIA and the output from the demultiplexer checked for errors. When BER rises above $1x10^{-9}$ the part is no longer passing data error free and it can be concluded that the LIA is not producing an output of full CML amplitude. Since this is known to be $1.2VPP_{diff}$ independent of process and temperature, dividing 1.2 by the differential input amplitude at which a BER of $1x10^{-9}$ was exceeded will reveal the gain. This should be done at a relatively low frequency so that bandwidth is not a factor in the result.

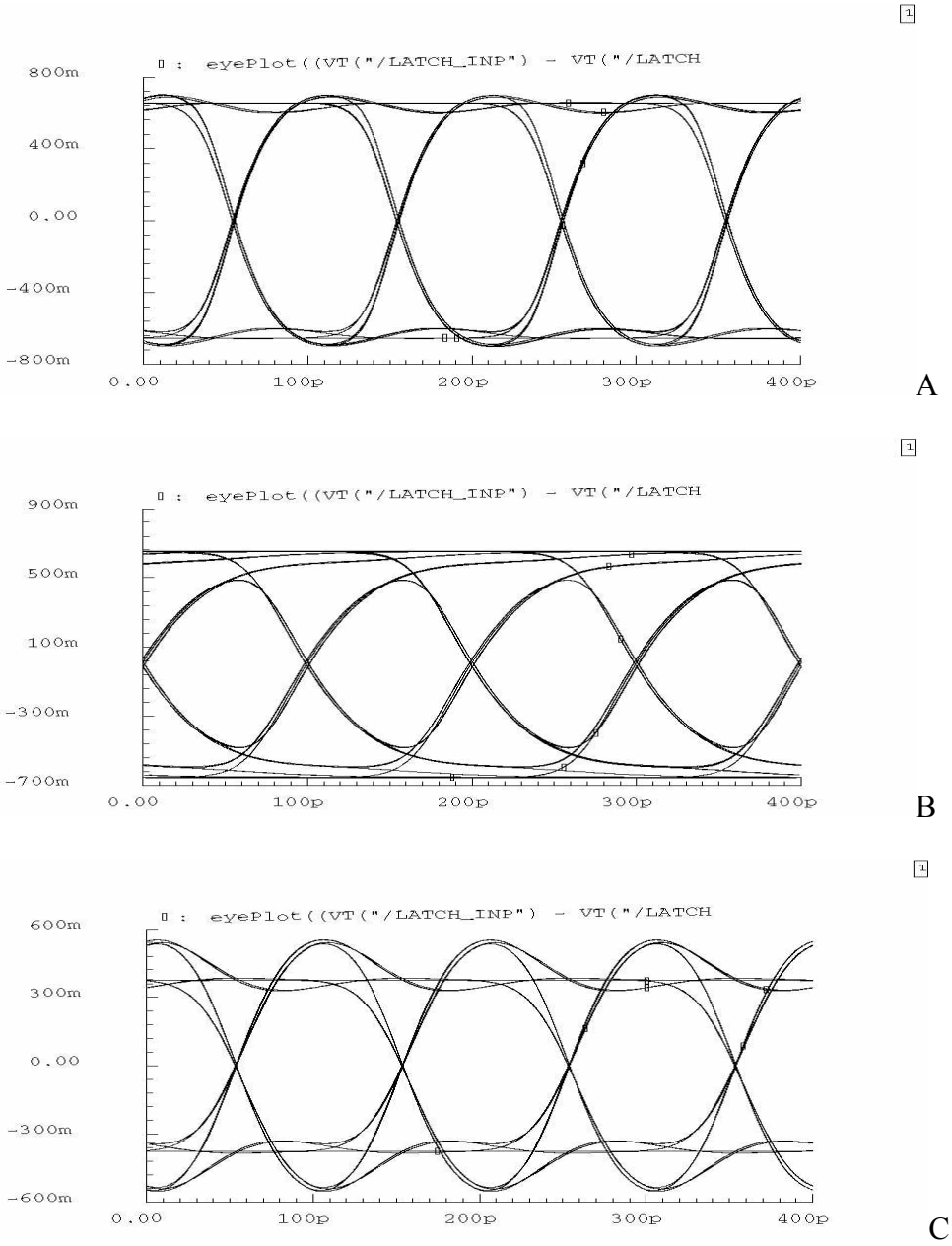


Figure 6-1. Effect of bandwidth and gain limitations on eye diagram. A) Good eye B) Eye closure due to bandwidth limitation C) Amplitude degradation due to low gain (note inductive peaking still drives edges to 600mV)

BER can also be used to roughly determine the LIA bandwidth. As stated above, the output of the LIA should not change as a function of input amplitude. This should hold true over the operational bandwidth. As the bandwidth of the complete deserializer is reached, the BER will increase. If increasing the input signal amplitude improves the

bit error rate at a specific frequency, then the LIA must be responsible for the bandwidth limitation. This can be concluded because if the LIA is not attenuating due to bandwidth limitations, increasing the amplitude would have no effect on the signal leaving the LIA and therefore no change in BER would be observed.

Test Setup

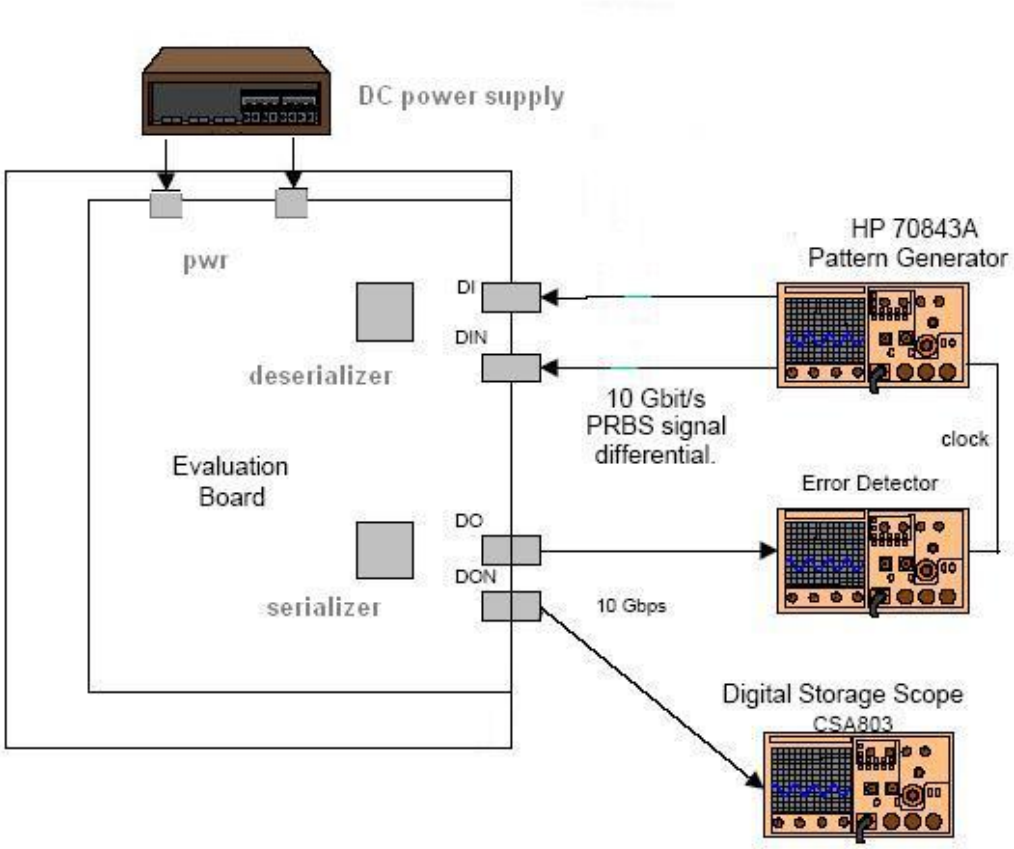


Figure 6-2. Test setup for SERDES chipset

The following test equipment was used to conduct the characterization:

HP 70843A pattern generator/error detector

Agilent 86100A Digital Sampling Oscilloscope

HP 8510 vector network analyzer

1.8V DC Power supply

Hand held Fluke multi-meter

100nF dc block capacitors

Phase matched hi frequency coaxial cable

Temperature chamber

For the following measurements, the test part was soldered to the evaluation board. The HP 70843A was connected to the data input and one of the output terminals using the dc block capacitors and phase matched cables. The oscilloscope was connected to the 2nd output terminal for monitoring purposes only.

Manual Offset and Cancellation Adjustment

To verify the manual offset cancellation, no input was required to the part. DC power was applied and the Fluke meter placed across the input terminals. The measured offset was 12mV with the internal loop active. Next the 5K ohm external potentiometer (on the evaluation board) was enabled and swept through its range. The offset at the input pins varied from -108mV to +105mV.

Absolute Input Sensitivity

For the mid-band absolute input sensitivity testing, the Hewlett-Packard 70843A pattern generator was used to provide a noise-free bit string to the evaluation board, but at half the rate of 9.95Gb/s. This is done by doubling the period of each bit effectively halving the operating frequency. The amplitude of the input signal was then lowered until the BER exceeded $1x10^{-9}$—the threshold for "error free" operation given in table 2-2. At low frequency, nominal power and temperature, the sensitivity was measured to be 11mVPP differential. As explained in the previous section, dividing 1.2 by $11x10^{-3}$ results indicates an LIA gain of 109v/v or 41dB. This is ~7dB below the simulated mid-

band frequency gain under nominal conditions, and 1dB below the specified gain of 42dB. Table 6-1 shows the mid-band sensitivity and calculated gain results over various supply and temperature settings.

Table 6-1. Measured mid-band sensitivity and calculated gain

Temp (ºC)	VDD (V)	Sensitivity ($mVPP_{diff}$)	CML amplitude (V)	Calculated gain (dB)
0	1.7	10.5	1.13	41
0	1.9	9	1.27	43
27	1.8	11	1.2	41
45	1.8	12	1.2	40
70	1.7	16	1.13	37
70	1.9	13	1.27	40

To test the part at speed, the HP 70843A was reset to provide a 2^{31}-1 psuedo-random pattern at 9.95Gb/S to the deserializer. If operating within specifications, the part should properly deserialize (BER<$1x10^{-9}$) data with an input amplitude of greater than 10mVPP up to a bit rate of 10.7 Gb/s.

Figure 6-3 shows the measured BER vs. input amplitude at the frequencies of operation for OC-192 Sonet (9.95G without and 10.3125G with forward Error Correction.) Two additional bit rates of 10.7G and 11.1G were also tested for possible implementation in other systems. For this test, the supply was kept at 1.8 volts, but the temperature increased to 45C.

The plot shows that the sensitivity was 19mVPP differential at 9.95GHz and rose to 28mVPP differential with a frequency of 11.3GHz.

Since the BER is decreasing as a function of input amplitude, the output of the LIA must be varying accordingly. As the low frequency test demonstrated that the mid-band

sensitivity was 12mVPP, the need for greater input amplitude indicates that the LIA is attenuating the high frequency components.

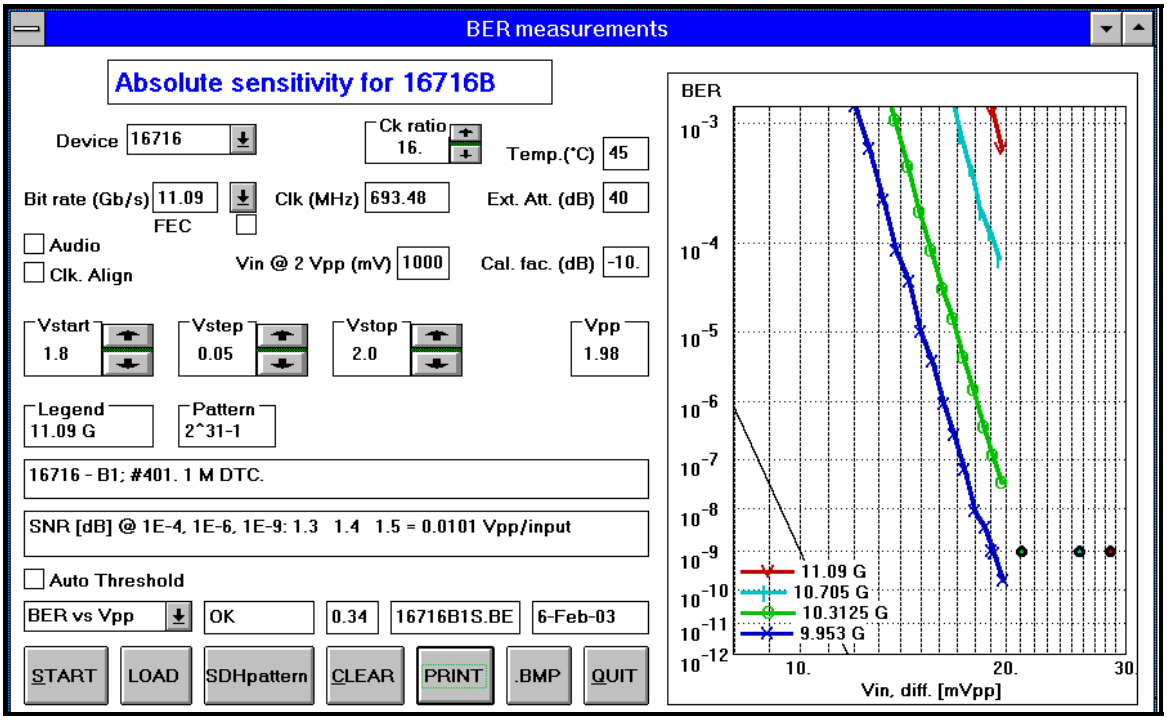


Figure 6-3. Absolute input sensitivity with 2^{31}-1 PRBS input, 9.95GHz-11.1GHz

A second test was conducted to determine the performance over temperature and supply extremes. BER vs. input amplitude was recorded at temperatures of 0C and 70C; the supply voltage was also varied between 1.7V and 1.9V. The frequency was held at 9.95GHz. The screen capture of this test is shown in figure 6-4.

The best performance was recorded at VDD=1.9V, 0C with an error-free input amplitude of 14mVPP differential. Decreasing the supply to VDD=1.7V degraded the sensitivity to 16mVPP differential. A stronger dependence on temperature was measured as the sensitivity increased significantly to 24mVPP differential for VDD=1.9V and almost 30mVPP differential with VDD=1.7V.

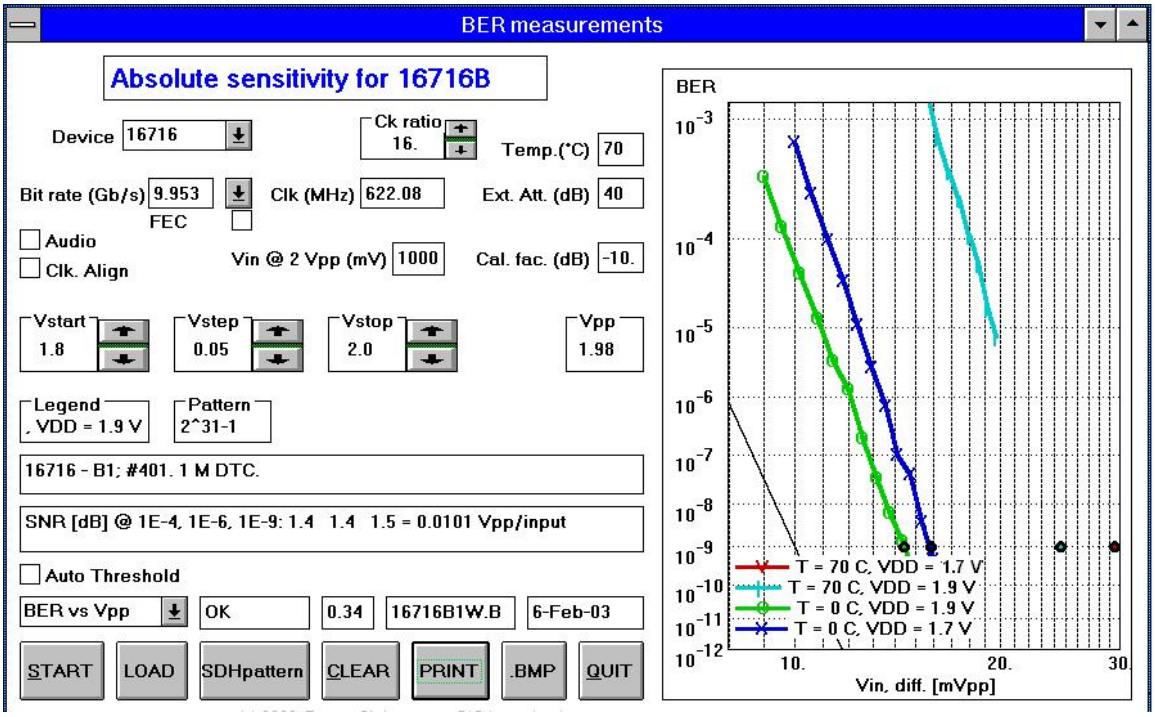


Figure 6-4. Sensitivity as a function of supply and temperature

Bandwidth Estimation

To get a picture of the effective bandwidth of the LIA, sensitivity at BER equal to $1x10^{-9}$ vs. frequency from the above figure can be plotted. If the mid-band sensitivity is considered the equivalent of passband gain in a Bode plot, connecting the data points recorded from the high frequency sensitivity and continuing the line until it intersects the mid-band sensitivity value will result in a rough upside-down Bode plot for the LIA. It is not an indicator or the -3dB point, but does infer the frequency limit of successful operation. (Inter-symbol interference will begin to degrade the data eye before the -3db point.) Figure 6-5 plots the data shown in Figure 6-3.

From the figure, it can be seen that the limit of maximum sensitivity operation is about 9.2Gb/s. The LIA was targeted for a maximum of 10.7Gb/s. This is 14% low. At

typical conditions, the LIA bandwidth was simulated to be 6.7GHz. A 14% reduction in simulated bandwidth infers an actual bandwidth on the order of 5.8GHz.

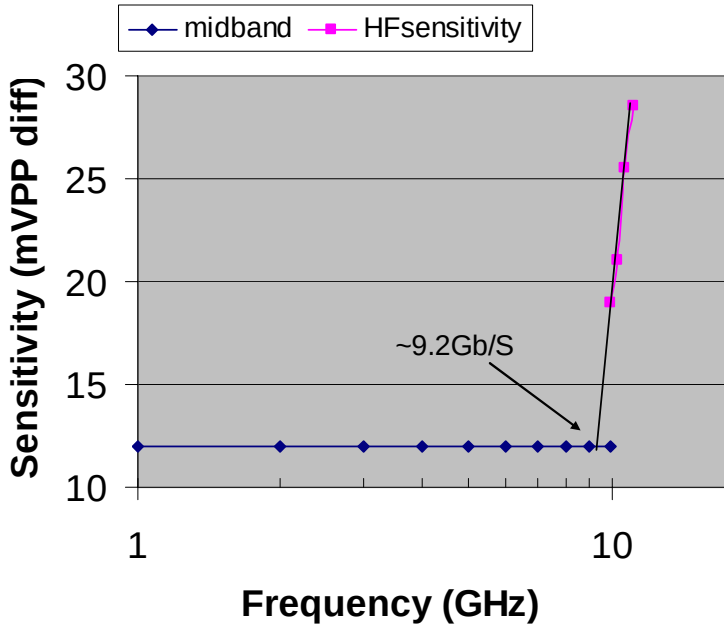


Figure 6-5. LIA sensitivity vs. frequency

Input Termination and Return Loss

The DC value of the input termination was measured form each pin to VDD and from DIN_P to DIN_N. The results are shown in table 6-2.

Table 6-2. DC input resistance

	VDD	DIN_P	DIN_N
DIN_P to	114	X	102
DIN_N to	119	102	X

S11 was measured to be better than -10dB up to 3GHz. It peaked at -6.5dB at just past 5GHz. Figure 6-6 is a test equipment screen capture of S11.

During design, the return loss was calculated based on a 50 ohm resistor in series with a large capacitor. As inspection of the circuit showed no other low impedance path to ground or VDD, this method was assumed to be sufficient. Because the measurement

did not return the expected results, a more detailed simulation was run to investigate the disparity.

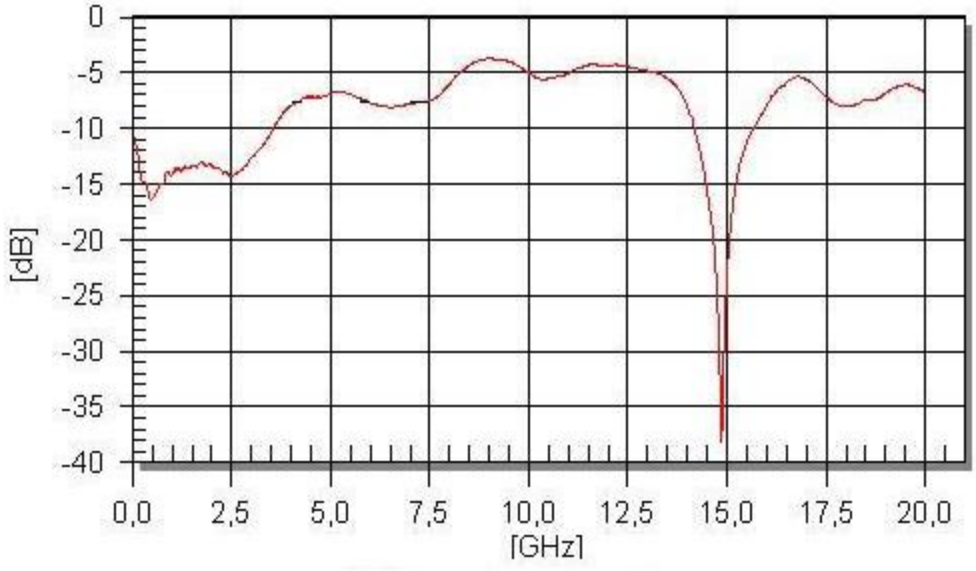
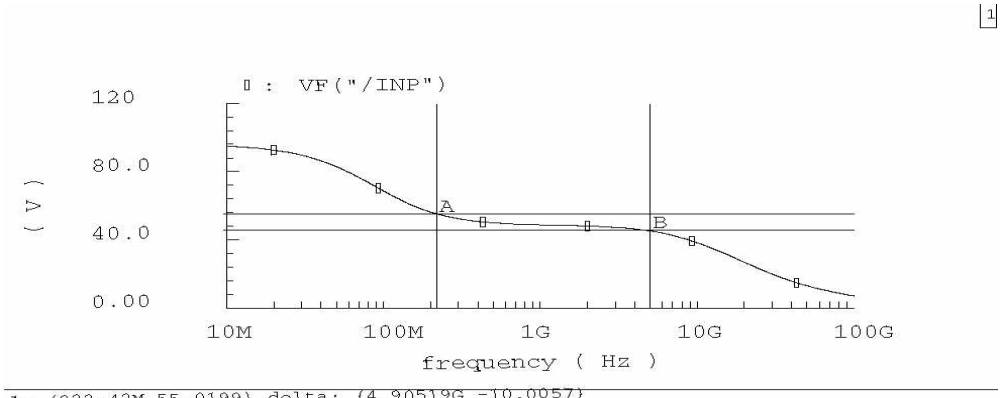


Figure 6-6. S11 measurement for LIA input

An AC current source with magnitude 1 was connected to the input of the LIA and an AC sweep performed. The voltage at the output of the current source is equal to the AC impedance (Ohm's law with I=1.) The plot is shown in figure 6-7.

The results show that the S11 curve should be below the specification up to 10GHz. During the simulation phase, no pad model was available despite attempts to obtain one. However, a pad model was available after silicon was produced. The model was added to the simulation and the two plots regenerated. The results are shown in Figure 6-8. While the S11 plot still shows better than -10dB return loss across the bandwidth, it is clear from the impedance plot that pad inductance is becoming a factor at about 2GHz. It is likely that the modeled values are optimistic and the pad inductance became a factor at a lower frequency than simulated.



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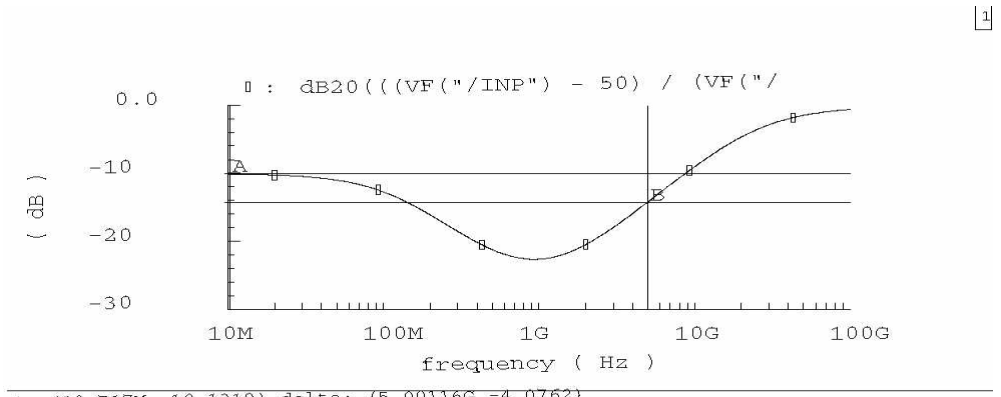

B

Figure 6-7. Simulated input impedance and S11 A) Zin B) S11

Measurement Summary

The above measurements are summarized and compared to the specifications in table 6-3 below.

Table 6-3. Measurement results vs. specifications

Parameter	Specification	Measured
Gain	42dB	37dB-43dB
Bandwidth	7GHz	5.8GHz (apparent)
Maximum Rate	10.7GHz	10.7GHz (with 25mVPP$_{diff}$)
Sensitivity	10mVPP$_{diff}$	9-16mVPP$_{diff}$ (low bit rates) 14mVPP$_{diff}$ 9.95GHz
Rin	100 ohms$_{diff}$	102 ohms$_{diff}$
S11	-10dB	-6.5dB

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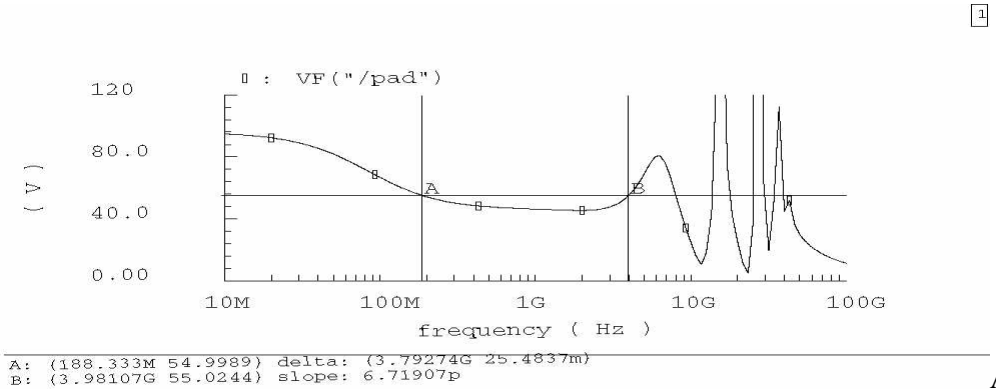

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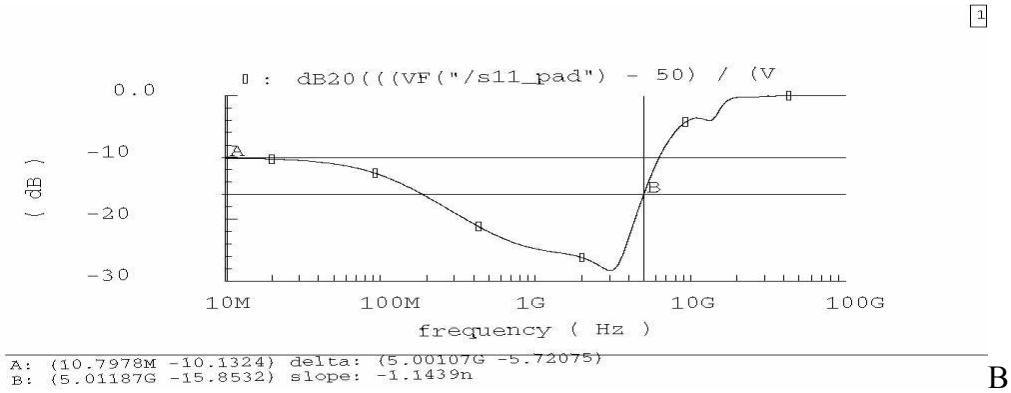

B

Figure 6-8. Simulated input impedance and S11 with pad model A) Zin B) S11

CHAPTER 7
CONCLUSIONS

This paper has described the design and testing of a limiting amplifier for OC-192 SONET applications in a CMOS process. Until recently, this was only possible in expensive processes. By utilizing a modified Cherry-Hooper amplifier architecture with active inductors to extend the bandwidth, a design with greater than 6.5GHz bandwidth and 40dB of gain over most PVT variations was achieved in simulation.

Silicon testing revealed that the goal of 10mVPP differential sensitivity was not reached, but error-free operation at 9.95Gb/s was demonstrated with a differential input of 14mVPP under good conditions and even at low voltage-high temperature error-free operation was possible with an input of less than 30mVPP.

Testing confirmed simulation results showing performance was reduced with low voltage and high temperature. This combination resulted in bandwidths below 6.5GHz and transient eye diagrams that were significantly closed. To overcome this, the block needs to be redesigned for greater bandwidth. A first possible improvement would be to reduce the operating point requirement of greater than 200mV above Vd_{sat} for the drain to source voltage. This would allow the differential pairs' W/L ratio to be reduced resulting in decreased capacitance along the signal path. The risk is that the current sources are closer to triode and if the models are off, this could affect performance through increased noise injection.

To address the sensitivity, the return loss should be improved. The specification was to have better than -10dB across the bandwidth, but rose above the threshold at about

4GHz, where it is most critical. While the LIA input stage should have good matching at the upper frequencies, the packaging and additional ESD measures extraneous to the block are sure to have an effect on this parameter. Unfortunately, no package model was available for simulation during the design phase. When a package model did become available and the S11 performance rechecked, a rise above -10dB was noted between 5GHz and 10GHz. It is very likely that model inaccuracies show this rise at a higher frequency than occurred in the silicon and that the package is a factor in the poor return loss at high frequency.

While the design needs improvement to meet all the initial specifications, it was still functional at speed and useable in systems where the input amplitude would be above 30mVPP differential. While not a focus of this paper, the system containing the LIA was designed for less than 1W of power consumption, and this was achieved. Overall, the less than desired sensitivity was deemed acceptable in exchange for the low power operation of the block. Previous bipolar products had demonstrated the extreme sensitivity targeted, but at more than twice the power. Therefore, no further improvement was deemed necessary.

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BIOGRAPHICAL SKETCH

Stephen Cove was born in Worcester, Massachusetts, and grew up in northern New England. After graduating from public high school, he joined the United States Navy as an avionics technician. He was stationed all over the world including three years in Keflavik, Iceland, and served during the first Gulf War.

After being honorably discharged, Stephen began his college education at Florida Community College Jacksonville while working various jobs. He graduated with high honors in 1996 and continued on to the University of Florida where he was accepted into the College of Engineering. He received a BSEE with honors in May, 1999, and began a career in design engineering at Intel Corporation in Folsom, CA. He continued to pursue his Master of Science from the University of Florida while working and is expected to complete it in the spring of 2005.