

PRACTICAL FORMATION OF EMPTY-SPACE SILICON VOIDS IN A
NON-EXPLOSIVE SEMI-HYDROGEN AMBIENT

By

WILLIAM S. HARRISON, III

A THESIS PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE

UNIVERSITY OF FLORIDA

2004

Copyright 2004

by

William S. Harrison, III

This thesis is dedicated to Lizandra Williams.

ACKNOWLEDGMENTS

The author would like to acknowledge all those who helped get this thesis to fruition. Special thanks (for patience and wealth of insight) go to Dr. Kevin Jones, Dr. Mark Law, and Dr. Stephen Pearton. Special thanks are also given to Dr. Holloway for insight dealing with vacuum science. All members of the swamp group (with special attention to Dian Hickey, Erik Kuryliw, and Mark Clark) are also acknowledged.

Most of all this could never have been completed without the help and support of William Harrison II, Joyce Harrison, Lizandra William, Lisa Harrison, Bruce Harrison, Ross Harrison, Peter Harrison, Alex Hargraves, Kim Hargraves, Kim Harrison, Lyn Harrison, Lance Reynolds, Collin Dunham, Heather Cameron, and the entire Harrison family.

TABLE OF CONTENTS

| | <u>Page</u> |
|---|-------------|
| ACKNOWLEDGMENTS | iv |
| LIST OF FIGURES | vii |
| ABSTRACT | ix |
| CHAPTER | |
| 1 INTRODUCTION | 1 |
| 1.1 Motivation..... | 1 |
| 1.1.1 Microphone..... | 2 |
| 1.1.1.1 General microphone overview | 2 |
| 1.1.1.2 Previous work..... | 3 |
| 1.1.2 Cooling Network | 5 |
| 1.2 Background..... | 6 |
| 1.3 Process Discription | 10 |
| 1.4 Thesis Scope and Approach..... | 11 |
| 2 PROCESS DEVELOPMENT..... | 13 |
| 2.1 Patterning Method | 13 |
| 2.1.1 Optical Lithography..... | 13 |
| 2.1.2 SEM Lithography | 16 |
| 2.1.3 Focused Ion Beam | 19 |
| 2.2 Etching..... | 19 |
| 2.2.1 Wet Etch | 19 |
| 2.2.2 RIE and DRIE..... | 20 |
| 2.2.3 Focused Ion Beam | 23 |
| 2.3 Annealing Gas | 24 |
| 2.4 Furnace Development..... | 26 |
| 3 EXPERIMENTAL..... | 35 |
| 3.1 Oxide Experiment..... | 35 |
| 3.1.1 Experiment 1 | 36 |
| 3.1.2 Experiment 2 | 37 |
| 3.1.3 Experiment 3 | 38 |
| 3.1.4 Experiment 4 | 39 |

| | |
|---|----|
| 3.1.5 Experiment 5 | 41 |
| 3.2 ESSV Experiments | 42 |
| 4 DISCUSSION | 43 |
| 4.1 Individual Experiment Discussion | 43 |
| 4.1.1 Discussion of Experiment 1 | 43 |
| 4.1.2 Discussion of Experiment 2 | 43 |
| 4.1.3 Discussion of Experiment 3 | 44 |
| 4.1.4 Discussion of Experiment 4 | 44 |
| 4.1.5 Discussion of Experiment 5 | 44 |
| 4.2 Discussion of Pitting | 45 |
| 4.3 Discussion of Overall Oxide Experiments | 48 |
| 4.4 Discussion of ESSV | 50 |
| 5 CONCLUSIONS AND FUTURE WORK | 52 |
| 5.1 Conclusion | 52 |
| 5.2 Future Work | 52 |
| LIST OF REFERENCES | 54 |
| BIOGRAPHICAL SKETCH | 57 |

LIST OF FIGURES

| <u>Figure</u> | <u>page</u> |
|---|-------------|
| 1-1. Heat flux due to subsequent increases in processor speed | 5 |
| 1-2. Graph showing depth vs. number of holes where R_R is the radius of the trench hole and L is the depth of the trench. | 7 |
| 1-3. Pipe fabrication..... | 7 |
| 1-4. TEM image of the migrated region. | 8 |
| 1-5. Above view of Fugi Electrics trench formation. | 8 |
| 1-6. SEM pictures. | 9 |
| 1-7. SEM images of anneal at 1100°C for 3 min... .. | 9 |
| 2-1. Flow chart of how a sample is processed in lithography..... | 14 |
| 2-2. Original array presented to Photonics | 15 |
| 2-3. Progression during a DRIE etch | 17 |
| 2-4. Silicon sample that has been over wet etched | 18 |
| 2-5. SEM picture taken of scalloping on a sample processed with DRIE | 21 |
| 2-6. Example of what is possible with SEM lithography using the software created by J. C. Nability. | 21 |
| 2-7. SEM picture taken of an array of holes over etched in the DRIE | 22 |
| 2-8. DRIE Recipes A, B, and C show three different sidewall profiles | 22 |
| 2-9. SEM picture taken of trenches created with recipe 3 | 23 |
| 2-10. SEM picture of a structure made with the FIB..... | 24 |
| 2-11. Original furnace setup not including the flow meter | 27 |
| 2-13. Original boat and rod..... | 28 |

| | |
|--|----|
| 2-14. Schematic of the turn and release boat system | 29 |
| 2-15. Newly designed boat | 30 |
| 2-17. Furnace schematic of sample boat outside of furnace hot zone | 31 |
| 2-18. Gas flow schematic of the amended system..... | 31 |
| 2-19. Pictures of the boat showing the holes that were put in to control oxidation..... | 34 |
| 3-1. Oxide thickness results from Experiment 1 | 37 |
| 3-2. Oxide thickness results from Experiment 2..... | 38 |
| 3-3. Oxide thickness results from Experiment 3..... | 39 |
| 3-4. Oxide thickness results from Experiment 4..... | 40 |
| 3-5. Oxide thickness results from Experiment 5..... | 41 |
| 3-6. SEM picture of a trench before and after 15 min anneal..... | 42 |
| 4-2. SEM picture showing the pitting phenomena at 150 x 0 tilt, 150 x 52°, and 10000 x 52° respectively. | 46 |
| 4-3. Simulations of oxide-capped Si-nanoprotrusions and elliptical etching pits. | 47 |
| 4-4. Ellingham diagrams of general oxides and SiO ₂ | 50 |

Abstract of Thesis Presented to the Graduate School
of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Master of Science

PRACTICAL FORMATION OF EMPTY-SPACE SILICON VOIDS IN A
NON-EXPLOSIVE SEMI-HYDROGEN AMBIENT

By

William S. Harrison, III

August 2004

Chair: Kevin Jones

Major Department: Materials Science and Engineering

In today's society, there is a growing need for smaller and faster devices. This can be seen in nearly all scientific fields. Among these fields and perhaps one of the largest, is the semiconductor industry, which largely caters to computer technology.

The need for faster devices has driven technology to new advances. One such advance is the formation of empty-space silicon voids (ESSV). Toshiba Corporation developed this process in 1999. In this process, small voids are formed just under the silicon surface, by way of silicon-surface self-diffusion. Toshiba's intent is to use the voids as oxide semiconductor devices in place of silicon on insulator structures. Along with that application, Dr. Kevin Jones and Dr. Mark Law hypothesize that ESSVs can be used to make sensors, and maybe even very small cooling networks used in computer transistors. In both cases, the ESSVs could possibly surpass the current industry standard.

Empty space silicon voids could have better functionality than those currently in its category. The ESSVs have a single crystal reverberating membrane with few defects. Their physical properties could also result in a more robust microphone design. Along with the possible performance benefits, one gains practical benefits by having such an extremely small receiver.

The focus of our study was to develop a condition in which the surface diffusion that creates ESSVs can take place. Specific aims were to develop the method, and to test the method.

The developmental experiments focus on trying to prohibit oxide growth. Surface diffusion cannot happen if there is an oxide on the surface. Results showed that the only way to create a non-oxidizing chamber condition is to anneal at positive pressure with an argon-hydrogen gas mixture.

Samples were annealed at 1000° C and 1100° C for 15 min under positive flow of 96% argon and 4% hydrogen. After annealing the samples showed no evidence of surface diffusion.

The method's inability to induce surface diffusion undoubtedly lies in the oxidation of the surface. The decomposition pressure is 5×10^{-22} Torr, and the actual partial pressure is only measured at about 1 Torr. This is far above the threshold at which oxidation can be prohibited.

CHAPTER 1 INTRODUCTION

1.1 Motivation

In today's society, there is a growing need for smaller and faster devices. This can be seen in nearly all scientific fields. Among these fields and perhaps one of the largest, is the semiconductor industry, which largely caters to computer technology. When information can mean saving lives, having information from many places, as quickly as possible, is very important.

The need for faster devices has driven technology to new advances. One such advance is the formation of empty space silicon voids (ESSV). This process was developed by Toshiba Corporation [1] in 1999. In this process, small voids are formed just under the silicon surface by way of silicon surface self-diffusion. Toshiba's intent is to use them as oxide semiconductor devices in place of silicon on insulator structures. Along with that application, Dr. Kevin Jones and Dr. Mark Law hypothesize that ESSVs can be used to make sensors, and maybe even very small cooling networks used in computer transistors. In both cases, the empty space silicon voids could possibly surpass the current industry standard.

Empty space silicon voids could have better functionality than those currently in its category. The ESSVs have a single crystal reverberating membrane with few defects [1]. Along with the possible performance benefits one gains practical benefits by having such an extremely small receiver.

1.1.1 Microphone

1.1.1.1 General microphone overview

Microphones can be found in many places. some are intended to be noticed, while some are not. For both uses there are growing needs for small microphones; whether the application is for omnidirectional surveillance, or for hybrid directional acoustic arrays. The small microphones are already being developed for hearing aids [2] and wind tunnels [3].

In general, all microphones work the same. They consist of some kind of membrane that moves in response to miniscule changes in pressure. This is even true of the human ear, which can sense pressure differences down to 0.02 mPa [4]. The audible range is roughly 20 Hz to 20 kHz, so any recording device that is meant to have the same range as the human ear hears must pick up at least this frequency range [4]. There are many types of microphones despite their general similarities. The difference is mostly in what the membrane is made of and how and what it translates the signal to. The average microphone translates the pressure differences into changes in current or voltage. The human ear is even a member of this category; while it does use mechanical and acoustic means for amplification, the end signal is an electrical impulse.

Crystal and condenser microphones will be discussed in this section. These two are selected because both can be fabricated with the silicon process developed in this thesis. A crystal microphone records sound by using a reverberating membrane that changes electrical properties during excitation. This has been studied using piezoelectric crystals [5].

Condenser microphones use a process based on capacitance. A condenser microphone consists of a cavity with an empty space enclosed by a reverberating

membrane and a back-plate. A charge is put on either the back plate or the membrane. When the membrane moves the cavity space the capacitance changes, thus converting sound to electrical signal.

1.1.1.2 Previous work

Extensive research has been Done on both silicon piezoresistive microphones and silicon condenser microphones. Currently most research involves condenser microphones, because of their mass reproducibility [6-8]. Depending on the application certain aspects of the microphone are more important. Frequency response is one example. If one desires to pick up audible sound then it must be in the audible range. To pick up some other sound a different range may be desired. Sensitivity and signal-to-noise ratio, however, are common qualities that are always preferred. These qualities are strongly influenced by the surface area of the membrane, the thickness of the membrane, and the size of the air gap behind the membrane [13-16]. Depending on the designer they focus may be on the particular aspect most important to given design constraints.

There are two main types of silicon membrane: single crystal or polycrystalline. Single crystal silicon is very robust. It has a high tensile strength, and good thermal resistance [9]. Silicon has a tensile strength 15 times that of steel [7]. Another reason single crystal silicon membranes are better is that they have very little residual tensile stress. An increased amount of tensile stress in a microphone causes a decrease in sensitivity [6]. Chemical vapor deposition-grown poly-silicon can have large residual stress [10,11].

Microtronics has successfully fabricated poly-silicon microphones [8]. They use two silicon materials to satisfy the residual stress issue. Silicon-rich nitride (which has 380 MPa of residual tensile stress) is layered with B⁺⁺ poly-crystalline, which has 40

MPa of compressive residual stress. Varying the thickness of each of these layers allows the designers to control the stress in the membrane. Here they achieve an ending residual stress of 45 MPa. This is the best achievable value because any mixture that produces less stress than 45MPa does not make a strong enough membrane to withstand any type of sound-induced excitation.

Results from Microtronics are comparable to results from other small condenser microphones. Microtronics measured a frequency response from 20 Hz to 10 kHz. Transound Electronics sells the typical small condenser microphone with a frequency response from 50 Hz to 15 kHz. Depending on the use, this difference may not be restrictive. The sensitivity for Microtronic's microphones is considerably higher-measured at 13 mV/Pa. Transound's sensitivity is calculated to be about 0.1 mV/Pa.

NHK Science and Technical Research Laboratories has successfully built a high-performance ultra-small single crystalline silicon microphone [7]. Because it is single crystal, they do not have the problems associated with residual stress. This is observed in their sensitivity, which is calculated to be about 20 mV/Pa. This is probably due to the lack of residual stress in the silicon membrane. The frequency range is 75 Hz to 24 kHz, which is wider than both the industry example and the poly-crystalline silicon example.

Silicon microphones demonstrate the ability to keep up with and surpass the current industry standard. They can exhibit better sensitivities and wider frequency response ranges. These advantages go even further when single crystal silicon is used in place of poly-crystalline silicon.

The small size of silicon microphones enables them to be put in arrays quite easily. They have been studied for wind tunnels and hearing aids [5,2]. Acoustic arrays give

more information about the sound source in that they can give information about location. Putting microphones in an array can also improve the signal to noise ratio and cancel feedback [2,5].

1.1.2 Cooling Network

Computer processor technology is forever changing. Computers are constantly getting faster and along with that they are also getting hotter. If advancement keeps up with Moor's law which predicts a doubling of the number of transistors every 18 months, a new method to cool computer chips will have to be developed. Figure 1-2 shows how heat flux has grown with processor speed.

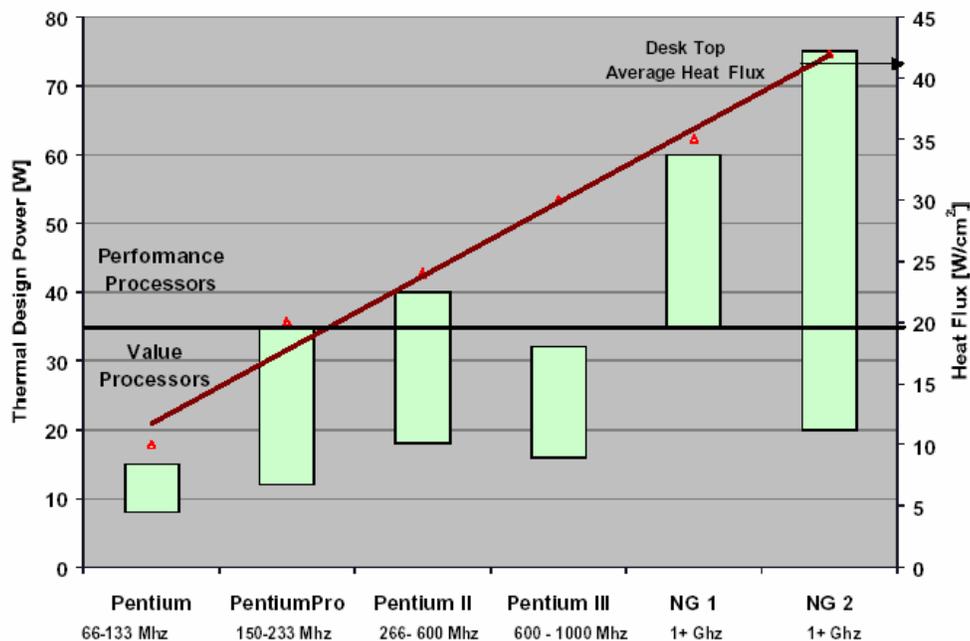


Figure 1-1. Heat flux due to subsequent increases in processor speed [17]

If heat increases with out heat dissipation, transistor reliability and speed decline [3].

ESSVs could be used to create cooling channels integrated into transistors.

Heat sinks are currently used in computers for cooling. There is a big difference in the heat transfer coefficient of gas and liquid forced convection. If air flows over a 1m

flat plate at 30 m/s, the heat flow coefficient is 80 W/m²K. If water flows over a 60 mm plate at 2 m/s, the heat flow coefficient is 590 W/m²K. The coefficient for forced water convection is much larger than that of air. This difference is compounded by the fact that the gas coefficient was at a 70°C difference in temperature and the water coefficient is at a 15° difference in temperature.

Currently, there is a technology created by Jiang et al. that is composed of small components that fit onto the back of a computer chip. Their new development is capable of actively cooling the chip by using what they call an electroosmotic pump [16]. However, even their technology is restricted by convection of heat between their cooling plate and the actual chip itself. The ESSV process could be used to cool individual transistors actively, drastically increasing the amount of heat that can be removed. The drastic increase would be from the integration of cooling pipes in individual transistors. This would considerably increase the exposed area and eliminate the convection between the cooling plate and the chip.

1.2 Background

Toshiba's process starts by etching deep holes in the surface of silicon [1]. These holes are then annealed at 1100°C in hydrogen for 180 seconds. They chose 1100°C because they need the surface kinetics associated with surface diffusion. The 1100°C annealing temperature is less than the 1400°C natural melting point of silicon, causing surface self diffusion to be driven by the minimization of surface energy. Their experiments showed, both the shape and the number of holes created are based on their radius, depth and spacing as indicated in Figure 1-2. From Figure 1-2 it is possible to see how multiple layered structures can be created with just a change in depth. This figure

also shows the range of radii that Toshiba studied. This will later serve as the reason for the range chosen in our study.

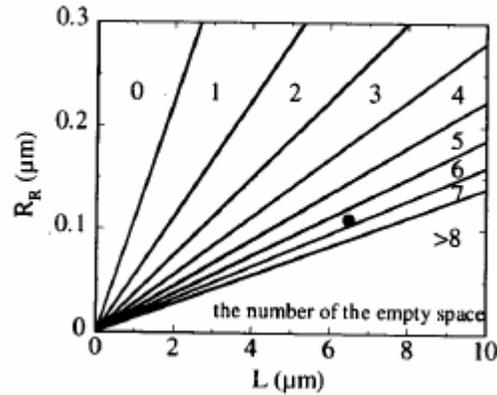


Figure 1-2. Graph showing depth vs. number of holes where R_R is the radius of the trench hole and L is the depth of the trench [1].

Different shapes can be formed beneath the surface of the holes depending on how close the holes are placed and the shape in which they are arranged. If the holes are put close enough together in a row, they can form a pipe beneath the surface. If consecutive pipes are placed side by side close enough, they can then form a plate.

Figure 1-3 is an example of how a row of holes can be placed to form a pipe.

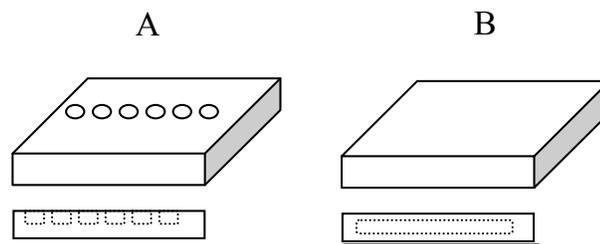


Figure 1-3. Pipe fabrication. A) before the anneal. B) after the anneal.

The holes will coalesce if they obey Equation 1-1 [1]. The shape parameters of the pipe and plate are described by Equations 1-2 and 1-3 respectively [1].

$$D_{NT} < 3.76 R_R \quad (1-1)$$

$$R_p = \left(\frac{8.86 r^3}{D_{NT}} \right)^{\frac{1}{2}} \quad (1-2)$$

$$T_p = \frac{27.83 R_r^3}{D_{NT}^2} \quad (1-3)$$

Toshiba's results show that there were no defects in the newly migrated silicon membrane, as seen in Figure 1-4. The amorphous layer is a result of Transmission Electron Microscopy (TEM) sample preparation.



Figure 1-4. TEM image of the migrated region [1]

Fuji Electric takes the research a bit farther exploring the conditions in which silicon surface diffusion or curvature reduction can take place. Instead of using dot arrays of holes, Fuji Electric uses long trenches (Figure 1-5) to observe diffusion. They determined that you can observe surface diffusion at 1000°C as well as 1100°C.

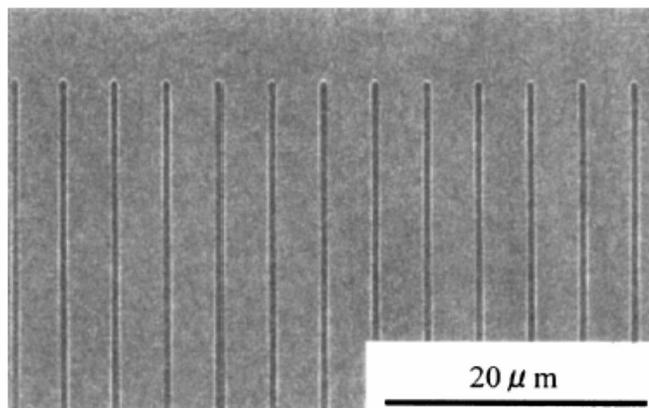


Figure 1-5. Above view of Fuji Electric's trench formation [19].

Fugi Electric determined that the diffusion is not nearly as far along at 1000°C as it is at 1100°C for the same annealing time as indicated in Figure 1-6.

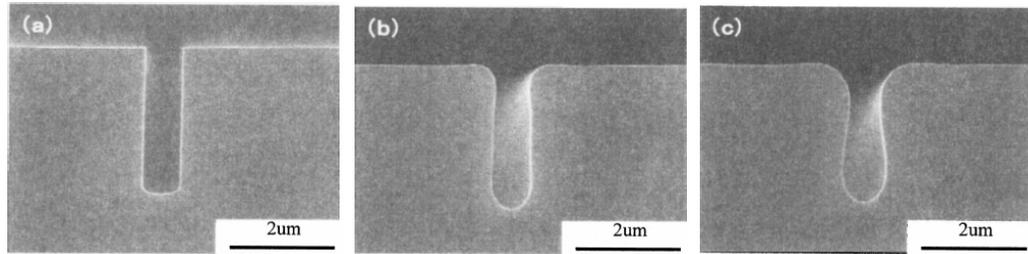


Figure 1-6. SEM pictures. A) before anneal. B) at 1000°C. C) at 1100°C [19].

This is what is kinetically expected since the diffusion equation is exponentially dependant on temperature. The temperature dependence can be seen in

$$D = D_o \exp\left(-\frac{Q_d}{RT}\right) \quad (1-4)$$

where D is diffusion, D_o is a constant, Q_d is the activation energy for diffusion, R is the gas constant, and T is the absolute temperature [21].

Fugi Electric also conducted studies concerning the pressure at which you could achieve surface migration. They found curvature to decrease at 300torr, 100torr and 40torr as illustrated in Figure 1-8. They also found however that diffusion increased with decreasing pressure. The activation energy for diffusion was estimated to be about 3.5 eV [19] which is higher than the 1.1 and 0.67 eV [20] observed at UHV. They speculate that the increase in the activation energy is due to the H_2 atoms absorbed on the surface.

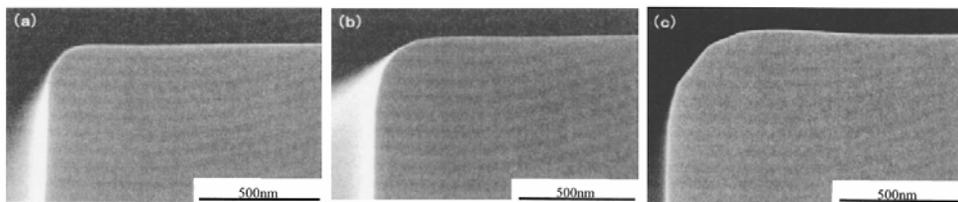


Figure 1-7. SEM images of anneal at 1100°C for 3 min. A) At 300torr. B) At 100 Torr. C) At 40 Torr.

The Toshiba cooperation has proven that their ESSV method is both controllable and reproducible. Fugi Electric Corporate Research and Development, Limited, Device Technology Laboratory has further proved that this process is reproducible. Fugi Electric has also proven that the parameters used by Toshiba are not necessarily the only ones that will result in voids being formed.

Toshiba's process consisted of a 100% hydrogen ambient at 10 Torr. Using pure hydrogen gas can be very dangerous and therefore is expensive to use safely. Using pure hydrogen makes the scalability of the process much more complicated as well. Along with the cost associated with the volatility of the gas is the temperature at which it is annealed. Toshiba used an annealing temperature of 1100°C. The temperature is important because the higher the temperature the higher the current and therefore the higher the cost of annealing. This is not an issue in a singular furnace, however if this process is scaled up the cost of heating the chamber could drastically increase with small changes in annealing temperature. Fugi Electric proved that you could get the ESSV phenomena with out going to 1100°C. They were able to recreate the same type of self diffusion at 1000°C. Figure 1-7 illustrates that the process takes longer with lower temperatures , which is what you would expect kinetically, considering equation 1-4.

If the process is ever utilized in a industrial means, one must assume that it will be profit driven. Currently the Toshiba process includes parameters that would be costly to scale up in a high throughput-processing scheme.

1.3 Process Discription

The ESSV process as developed by Toshiba and followed by Fugi Electric has three main parts: patterning etching annealing. Each part can be performed in various

different ways with various different types of equipment. Depending on the equipment, it may be possible to combine steps but all steps must be accomplished to achieve ESSVs.

In order to create a silicon topography that will result in ESSVs you must first drill or etch small holes in the surface of the silicon. Fugi Electric used reactive ion etching (RIE) to create the holes. If RIE is used, the usual method of patterning uses an ultraviolet aligner. There are alternatives to RIE that may result in more accurate and reliable patterns, as well as giving the process more freedom in the types of end products possible. A deep reactive ion etching machine (DRIE) has the same capabilities as a RIE, however a DRIE can create deeper features with a 30:1 aspect ratio [22]. Both the DRIE and the RIE require a patterned mask prior, from SEM or UV lithography. A Focused Ion Beam (FIB) can be used to both write and etch the pattern because it writes directly on the silicon. This thesis will explore the different types of patterning and etching methods one could use to achieve ESSVs.

The last portion of the process consists of annealing which is where the actual surface diffusion occurs. There is a kinetic driving force to decrease the amount of curvature in topography seen in

$$k = \frac{1}{r} \quad (1-6)$$

where k is curvature and r is radius. This driving force causes the corners to round and the whole corners begin to approach one another due to the motion of silicon atoms.

1.4 Thesis Scope and Approach

The scope of this thesis is two fold. The first section is process development, which covers the advantages and disadvantages to each step and piece of equipment. It

will cover all the process and equipment changes that were made during the evolution of the process. This section will cover the three main parts of trying to create ESSVs:

Patterning, Etching, Annealing

The second part is experimental which is divided into two parts. The first part covers the experiments designed to create a method that does not grow oxide. The second part covers experiments designed to test whether the developed process is successful. The overall objective is to explore the most scaleable way to recreate ESSVs in a non-explosive semi-hydrogen ambient.

CHAPTER 2 PROCESS DEVELOPMENT

There are three main aspects in the creation of ESSVs. They include the following:

1. Patterning Method
2. Annealing Chamber Ambient
3. Annealing Apparatus

2.1 Patterning Method

2.1.1 Optical Lithography

Fuji Electric's and possibly Toshiba's process includes typical wafer patterning techniques. Currently the industry standard is to use a mask to imprint patterns on photoresists. Optical lithography is a widely used method for wafer patterning. Optical lithography is the process by which a pattern is imprinted on a thin light sensitive film that has been spin coated onto a wafer [32]. The pattern then acts like a stencil only allowing particular parts of the wafer to be etched.

E-beam lithography has the same basic concept as optical lithography, only it does not use a mask and the resist is electron beam sensitive instead of photon sensitive. A typical wafer starts by having photoresist or an e-beam resist spun onto it. Photoresist is a photosensitive chemical that changes its chemical makeup when exposed to a particular type of light (in this case, ultra- violet). E-beam resists behave in the same way, only its sensitivity is to electrons. The thickness is controlled by the spin speed of the coater during the application of the resists. The resist on the wafer is then baked for a predetermined time dependent on the type of resist used (negative or positive). Baking is then followed by exposure to UV light or an electron beam. When the resist is exposed,

it breaks cross-links becoming soluble in a developer or vice versa for negative resist.

The wafer is dipped into a developing chemical that allows either the exposed or the unexposed portion to dissolve. Figure 2-1 shows these steps.

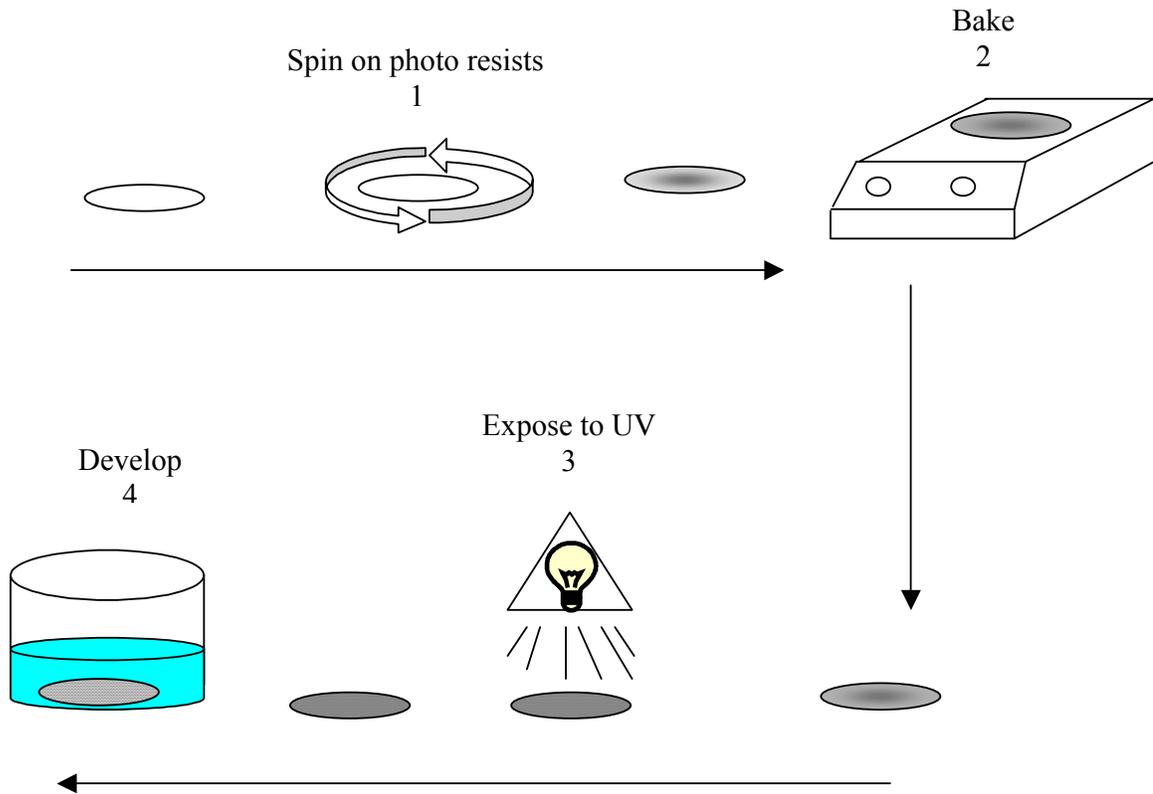


Figure 2-1. Flow chart of how a sample is processed in lithography

After the development, a copy of the pattern is left on the wafer in the photoresist. The resist then acts to protect parts of the wafer during an etching phase. Both optical lithography and scanning electron microscopic lithography use resists to transfer the pattern. Focused ion beam however does not use a resist because it directly writes the pattern on the silicon sample.

Optical lithography is most widely used in industry and thus is easily scalable to higher process throughputs. Because it usually involves only ultraviolet light a pattern can be made as large as the mask that imprints it. Aside from using a larger mask, it is

possible to utilize a step and repeat process to increase process throughput. In a step and repeat process, the pattern is repeated by moving the mask to different parts of the wafer. The scalability as well its common use made it an obvious first choice for this process development.

Photronics, a mask building company was found to be the most promising in the fabrication of a mask with the desired features. Toshiba's research had covered whole radii ranging from 0.1 μm to 0.3 μm . There were no other companies who would attempt making features so small. The matrix below (Figure 2-2) is the original desired pattern to be imprinted on the mask.

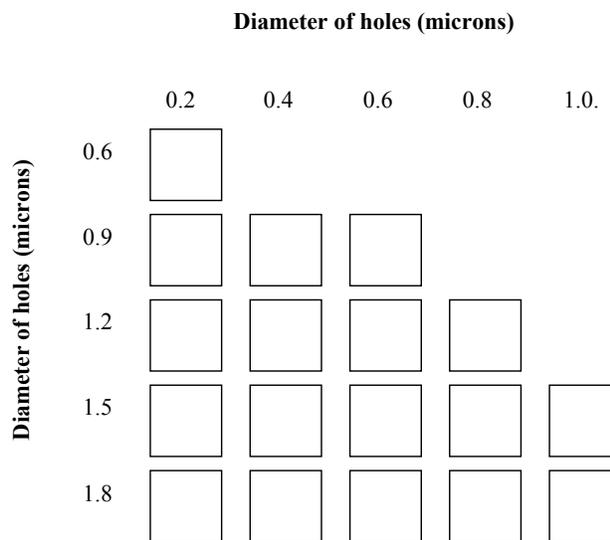


Figure 2-2. Original array presented to Photronics

There were some key problems that fundamentally plagued the method. Photronics required a computer aided design program to develop a mask with the specific parameters. As seen in Figure 2-2, the number of holes in the pattern is quite large. This was not thought to be a problem in transferring the pattern to the silicon, because the matrix of holes is transferred at one time. This would mean that the number of holes on a mask is independent of the process time to transfer them. This large magnitude of holes

however created a large problem in the file size of the CAD pattern. This would eventually cause a problem with file transport and would ultimately make the pattern too memory heavy to make changes to. Along with this memory problem, Photronics was unable to accommodate 100x100 hole arrays due to the write time associated with them. They recommended the dimension be dropped to 10x10, which would result in significantly fewer holes.

The feature size also proved to be a problem. Though they said a 0.2 μm diameter feature sizes was possible, they could not create these with the spacing required. Unfortunately they were only able to create 0.5 μm diameters, and with this, the diameters could be off by as much as 0.1 μm . Toshiba's research only covered holes up to 0.3 μm , 0.5 μm is outside of the tested range. Part of the experiments set up here will try to recreate the holes with the same diameters tested by Toshiba. Photronic's inability to create our desired feature size meant that they would not be a feasible option for a mask maker.

After further searching it became obvious that optical lithography would not be a very viable solution to patterning wafers. The size and dimensions required were too small for current optical standards.

2.1.2 SEM Lithography

The next choice was determined to be scanning electron microscopic (SEM) lithography. Though SEM lithography does not have the throughput capability that UV lithography has, it has no problem creating the 0.2 μm diameter holes that we desired. SEM lithography is actually capable of creating feature sizes much smaller than the ones required.

SEM lithography still requires a resist but it is a special resist used for electron beam exposure called poly(methyl-methacrylate) or PMMA. PMMA has a high resolution, which is why it is good for small features.

Originally it was thought that the pattern transferred to the resist would then be transferred to a SiO₂ layer on top of the silicon. However, a deep reactive ion-etching machine to etch the holes in the surface was selected instead. It was thought that the PMMA would not stand up to the ion beam directly, so by knowing the relative etch rates of SiO₂ and silicon one can grow the correct thickness of SiO₂ to get the depth of features desired.

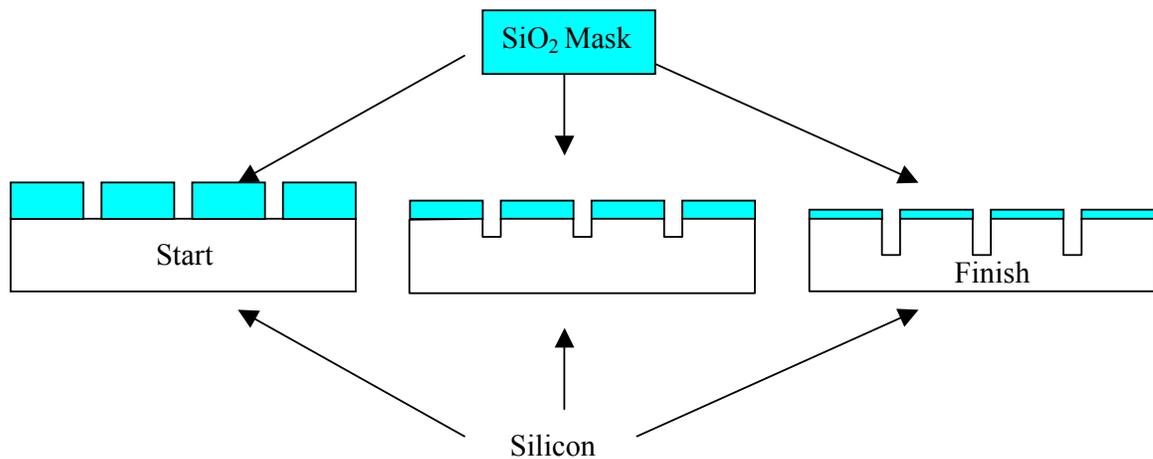


Figure 2-3. Progression during a DRIE etch

A wet etch was used to transfer the pattern from the resists to the SiO₂. A 6:1 buffered oxide etch (BOE) was used to open the holes in the SiO₂. BOE is used because hydrofluoric acid has no effect on PMMA. The etch rate of BOE on SiO₂ was measured at 18Å/sec, and the relative etch rate of Si to SiO₂ is about 100:1. The objective was to grow 0.15 μm of SiO₂ as a mask, and then etch 15 μm into the silicon. It was discovered however that timing a wet etch precisely is not trivial. Over etching was a definite

problem with each attempt. Figure 2-4 depicts a silicon sample that has been over wet etched.

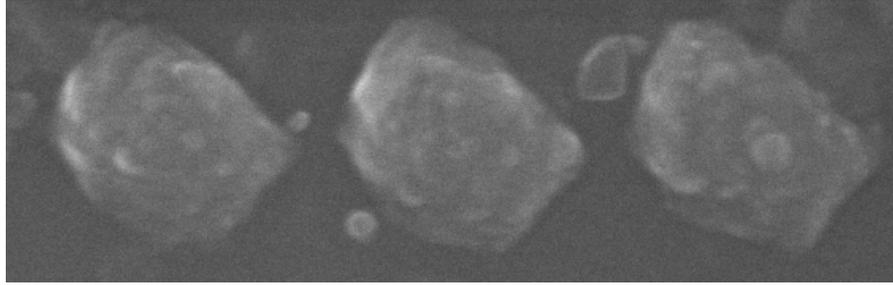


Figure 2-4. Silicon sample that has been over wet etched

Along with the over etching issue is the problem associated with using an isotropic etch. An isotropic etch, like BOE, etches in all directions all at once. As can be seen in Figure 2-4 this can cause undercutting beneath the PMMA cover. Figure 2-4 shows how the holes etched so much they undercut and only left the SiO₂ that had been between the holes. Through much further iterations it may have been possible to develop a dipping scheme that may have given close to desirable results. However, it is unlikely that vertically straight sidewall holes would be created. We learned nevertheless that it might be possible to directly pattern the silicon using the PMMA, bypassing the SiO₂ stage completely. The PMMA proved to be a very viable mask for the e-beam lithography although other problems still ensued. Getting the current dosage correct proved to be a problem. If the PMMA is underexposed the pattern will not transfer all the way down to the bulk silicon. This means during etching the pattern will not be the desired depth or it may not imprint at all. Though tedious, through trial and error a correct dosage was discovered for a particular thickness. There is unfortunately a variation in thickness depending on the distance from center. The center tends to be thicker because it travels

at a slower speed than the edges, therefore making the needed dosage dependent on where the sample comes from on the original wafer.

2.1.3 Focused Ion Beam

The focused ion beam (FIB) has the writing portion embedded in the software. Using the FIB would mean that the spin coating, baking, and pattern processing steps are all condensed into one. When using the FIB, all you have to do is design your pattern on the drawing software and the pattern writing is complete. Further explanation of the FIB's etching capability will be handled in the etching section.

2.2 Etching

Etching is the process by which material is removed. Etching is used in this process to make the small holes and trenches in the silicon to create the topography in which silicon surface diffusion can occur. There are three types of etching described here. The first is wet etch which is chosen for its ease of use and high throughput capability. The second and third are reactive ion etching and deep reactive ion etching, chosen because of their anisotropic nature.

2.2.1 Wet Etch

Wet etch is the first to consider because of its wide use and easy scalability. One could envision an automated assembly line where wafers are pulled through an acid-dipping bath at a particular speed keeping them submerged for a specific amount of time. The draw back to a wet etch is that it is largely an isotropic etch, meaning that it etches in all directions at once. As described earlier with trying to transfer patterns to SiO₂, wet etch can cause undercutting and can ultimately give you a bad aspect ratio which is a terminal problem in our case. An anisotropic etch is possible but it is dependant on the planes of the crystal [33]. It turns out that if you use a strong base the {111} plane etches

a lot slower than the $\{110\}$ and $\{100\}$. This has to do with the number of bonds faced into the crystal and the number of dangling bonds faced outward. Though this is an anisotropic etch it has no real value in this application.

2.2.2 RIE and DRIE

RIE and DRIE both use ions to etch into the material. In both cases an etchant like SF_6 is used. Etching occurs by directing SF_6 ions toward the sample to cause ion milling in one direction, which is known as a physical etch. While this is going on, there is also a chemical etch that comes from the vapor in the chamber. The chemical etch is an isotropic etch. The process is designed so the anisotropic etch rate will be higher than the isotropic etch rate. There must be a balance however, because if the anisotropic etch rate is too high it will obliterate the mask which creates the pattern.

The DRIE differs from the RIE in that it has a way to combat the tendency for the chemical etch to eat away at the side walls. The DRIE has two main steps, a passivation step and an etching step. The passivation step uses a compound like C_4F_8 to coat the sides so they are partially protected during the etching step. C_4F_8 is a polymeric coating that is deposited during the passivation step. The bottom of a hole or trench has both the chemical and the physical etch to contend with while the sidewalls only really have the chemical etch, causing the bottom of the hole to etch faster than the sidewalls. However, the polymeric coating does etch so it must be cycled with the etching step. The DRIE software can typically control the etching and passivation times. The amount of time you spend at each step is dependant on the type of structure you are making. Because the sidewalls do experience some etching the side profile of the hole or trench will have something called scalloping (Figure 2-5).

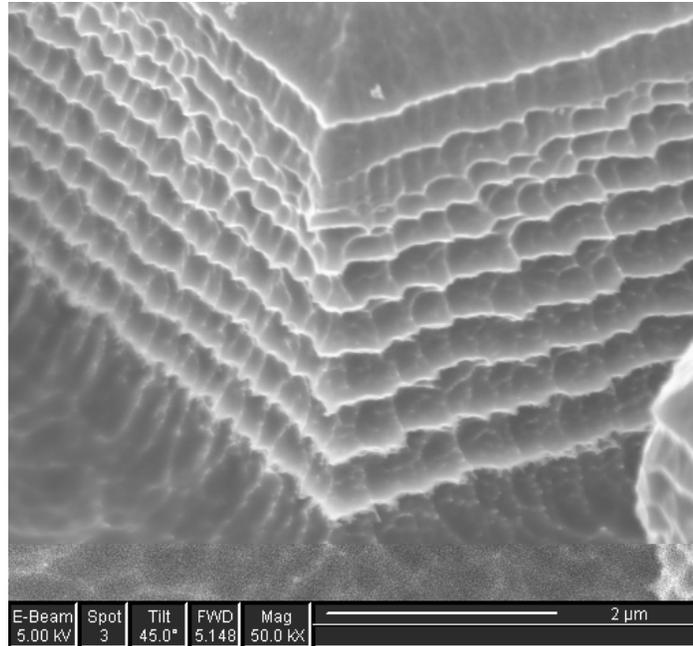


Figure 2-5. SEM picture taken of scalloping on a sample processed with DRIE

Functionally, the DRIE is capable of the feature sizes needed. SEM lithography used with DRIE is very versatile and capable of many different shapes and patterns.

Figure 2-6 shows examples of the different possible shapes.

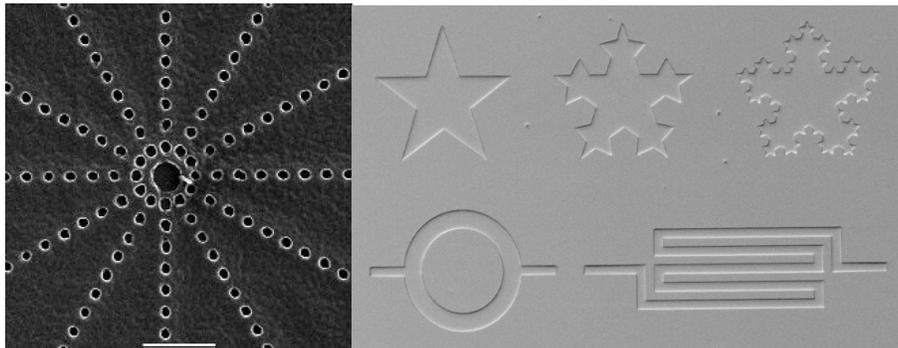


Figure 2-6. Example of what is possible with SEM lithography using the software created by J. C. Nabity.

It is possible to make the array of holes desired but finding the correct passivation and etch time is not a trivial task. If an array of holes positioned close together experiences scalloping, the scallops can etch into the adjacent hole and cause a three dimensional mesh of sorts (Figure 2-7).

It is possible to create hole arrays that are not over etched due to scalloping. The nature of the sidewall profile can vary drastically depending on the nature of the etch and passivation. The figures below illustrate three different recipes resulting in three different sidewall profiles.

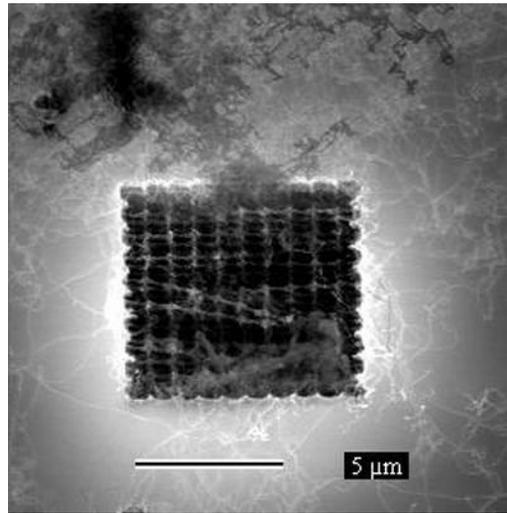


Figure 2-7. SEM picture taken of an array of holes over etched in the DRIE

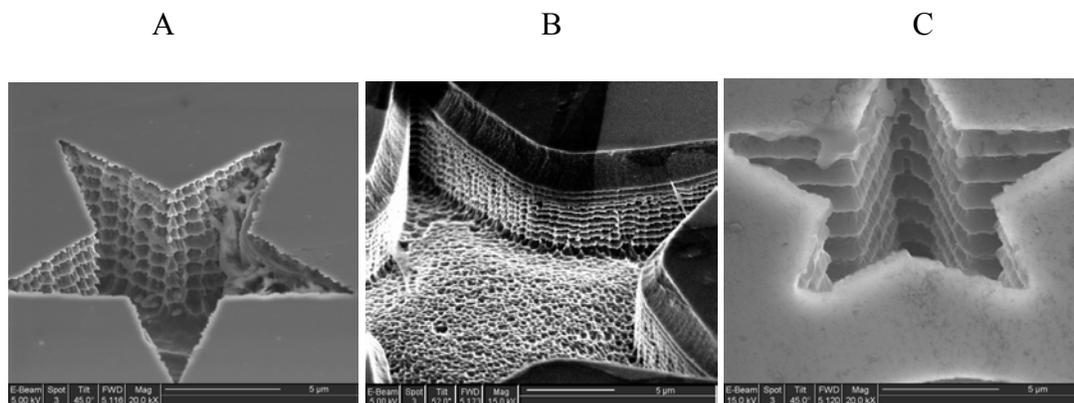


Figure 2-8. DRIE Recipes A, B, and C show three different sidewall profiles

After even more iterations and trial runs with different recipes Figure 2-9 was achieved.

Though Figure 2-9 has very straight sidewalls it does not have the necessary depth. This is because the PMMA mask does not stand up long enough to mill deeper.

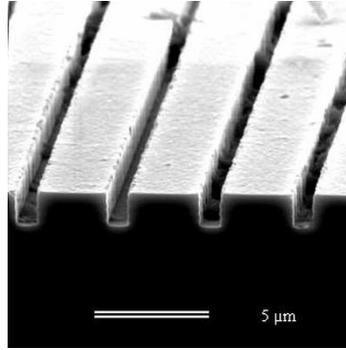


Figure 2-9. SEM picture taken of trenches created with recipe 3

Though DRIE does require a patterned PMMA mask prior to sample introduction, it can process as many patterned samples as can fit in the chamber. DRIE is a definite possibility for the ultimate upscale of the process. The iterations to achieve the optimal processing parameters are time intensive. They may also need to be redone if certain aspects of the desired end structure are changed. After the process has been characterized however, processing time may not be an issue. It takes about 3 minutes for a 5 μm hole depth. This is independent of the number of samples in the chamber.

2.2.3 Focused Ion Beam

The focused ion beam (FIB) uses ions as well, only it can focus them onto an area small enough to create the desired features. The ability to focus is the reason that it does not need a mask like the DRIE. The FIB can simply write a pattern as if it were a pencil on paper. The FIB can not completely separate images written at the same time, it can only write with less current. This creates light tracks between images. It can however deposit atoms from the ion source as well as damage some of the crystallographic order of the surface. This could be a problem but the surface should recrystallize very quickly relative to the annealing times used in the experiments. The implanted atoms should not be numerous enough to inhibit the silicon surface diffusion.

Though the FIB may cause some reversible crystallographic damage, its topological product is impeccable (Figure 2-10). It has the ability to create very straight sidewalls.

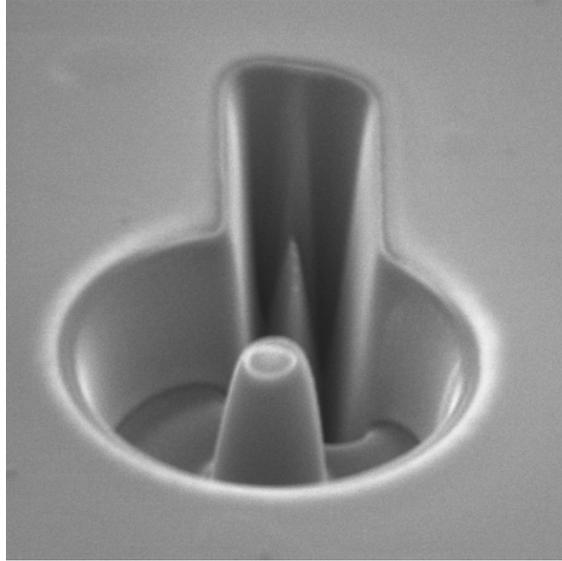


Figure 2-10. SEM picture of a structure made with the FIB

2.3 Annealing Gas

The annealing portion of the process is important because there in lies the actual surface diffusion phenomena. Silicon surface diffusion cannot occur if there is an oxide on the surface. Both Toshiba and Fugii Electric performed their experiments in 100% hydrogen ambient. This is the best annealing gas for the inhibition of SiO₂ growth on the surface. There are three main reactions happening in the furnace chamber that affect the silicon sample.



The gases discussed here are nitrogen, an argon hydrogen mix and pure hydrogen. The primary focus of this thesis is to initiate silicon surface diffusion with out using an explosive amount of hydrogen. That being said pure hydrogen is a reference reaction used to compare other ambient gases.

Nitrogen was chosen because it is both inert and plentiful. Nitrogen is probably one of the most commonly used gases in industry behind compressed air. It is also the most abundant gas in air so there is little concern when considering leaks. The actual nitrogen would not aid in the oxidation of the surface itself, however a nitrogen ambient is not reducing and would not drive equation 2-1 to the left. It is not possible to attain a pure nitrogen tank, even high purity nitrogen will have some fraction of impurities.

Annealing in pure nitrogen resulted in pitting and oxide growth on the surface. The pitting was not extensive but the oxide thickness was measured to be 80 Å higher than the unannealed control. This means that a nitrogen ambient is not an acceptable option.

The argon hydrogen mix is composed of 4% hydrogen and 96% argon. This composition is considered noncombustible, anything higher than that would require special safety concerns that would cause the cost of the annealing equipment to skyrocket. After considering nitrogen, the argon hydrogen mix was the next logical choice because it most resembled a pure hydrogen chamber ambient. Further testing of the use of argon and hydrogen will be covered in the experimental and discussion sections of this thesis.

2.4 Furnace Development

The furnace is among the most important pieces of equipment in this study. It controls all of the parameters that determine whether the surface diffusion can take place. It includes the following in its make up.

- Heat generator
- Quartz tube
- Entry chamber
- Load lock
- Vacuum
- Cooling system
- Sample boat
- Flow meter
- Gas flow system

Each of these pieces plays a key role in the chamber controls and has a crucial effect on the method in which each sample can be annealed. The design focus was to build something easily scaled. This was attempted by trying to make the furnace design as simple as feasibly possible. A system with simple parts is more likely to have linearly scalable characteristics. There exist systems capable of achieving better ambient conditions but it would be unrealistic to scale up such intricate designs. A chemical vapor deposition chamber, for example has the capability of producing the conditions needed. Such a chamber would prove to be very costly to scale up. For this reason focus is kept on parts that in theory could be scaled up linearly. The vacuum pump, chamber, and gas tanks all can be made stronger and bigger to accommodate more samples.

From its conception the furnace went through an evolution of sorts starting with a basic design. Here the furnace evolution is covered in detail. The furnace first started with the components shown in Figure 2-11. Figure 2-12 has the original gas flow and cooling network schematic.

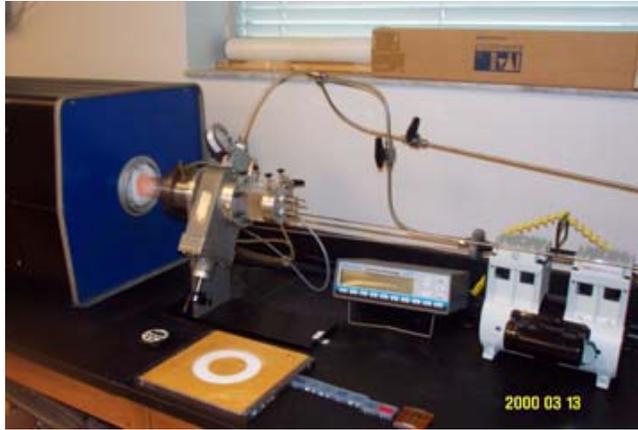


Figure 2-11. Original furnace setup not including the flow meter

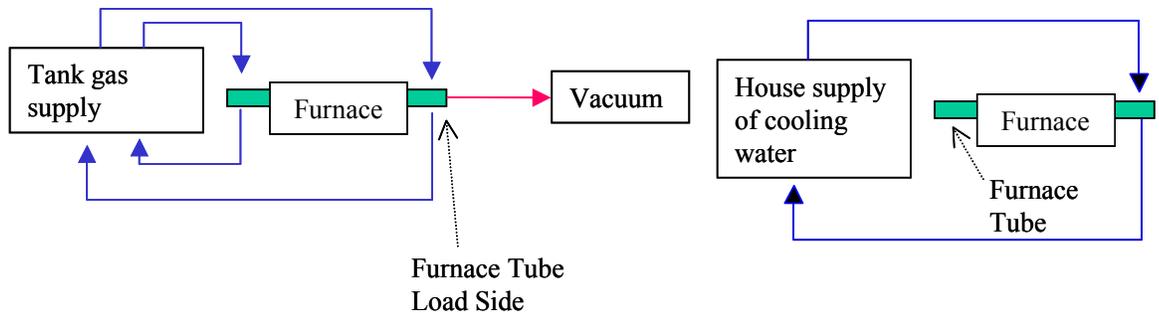


Figure 2-12. Flow diagram of the gas system on the left and the cooling system on right

The first problems originated from the entry rod used to put the sample into the chamber (Figure 2-13). The rod is made of a long thin piece of quartz that breaks easily and was broken many times. Introducing the sample under positive argon hydrogen pressure and vacuum was tried, which resulted in easy breakage of the rod. There was also an issue with sample introduction into the chamber. Opening the entire chamber to ambient conditions meant the chamber gas was getting into or out of the tube during sample transfer. This is detrimental to the sample and unsafe to the lab users depending on the desired chamber gas and conditions. Even if the sample was introduced under air and then purged the sample would see oxygen and vapor at heightened temperatures, which would mean oxide growth at exponential rates. This is a problem impossible to solve with an introductory method like the one described above. In most vacuum

chambers where a sample cannot be exposed to air at elevated temperatures, the sample is moved with a magnet on the out side.

The second problem originates from the loading portion of the chamber. The loading chamber is not made to maintain the vacuum. In order to inhibit leakage the load lock should be used to isolate the system from the load chamber. This is impossible as long as the rod and the boat are one piece.

A



B



Figure 2-13. Original boat and rod

Consideration was given to getting a thicker quartz rod to help make the introductory and extraction process more robust. Thick quartz however is very expensive and Pyrex would not sustain the 1100°C temperatures reached during testing.

To combat the load lock issue a boat was designed that could detach from the rod that introduced it (Figure 2-14).



Figure 2-14. Schematic of the turn and release boat system

With this design the sample boat had a hook that connected to the entry rod. The rod now pushed the boat forward into the chamber and at the desired location the hook could be turned and disconnected from the boat where it could then be retracted. At this point the load lock could be closed and the chamber could be purged.

The sample's introduction in air is still a relevant problem at this point, however it was thought that the chamber conditions could possibly reduce whatever oxide is grown during entry. After further testing, oxide was still measured at well over 100 Å on all samples regardless of chamber conditions. Another problem became obvious with this measured oxide. If the argon hydrogen mix does drive the oxidation reaction backwards to reduction, the sample could still be growing oxide when it is pulled out of the heated region. Upon sample extraction from the hot zone the boat and the sample are red hot and at this temperature any exposure to air would cause extremely high oxidization rates. This implies the oxide measured may or may not be from the anneal. It is possible to extract the sample under positive pressure conditions but this limits the system to only gases that can be intentionally leaked to the lab's atmosphere.

The problems with oxide thus far meant that something had to be devised to prohibit the sample's exposure to air at elevated temperatures. In addition to sample exposure, making sure there was never a time that the chamber gas was intentionally

leaked to atmosphere was very important as well. To combat both of these problems the sample boat and rod were completely redesigned to the structure in Figure 2-15.



Figure 2-15. Newly designed boat

The new design has the sample carrier and the rod as one piece. This new design means that the entire boat is made to exit the chamber for sample loading and unloading. This design change allows the sample to be loaded into the chamber and then sealed off before the sample is ever introduced to the hot zone. The boat also now has a holding cup on its rear for a magnet. The magnet is used to move the sample into and out of the hot zone. The length of the boat is made such that the magnet will never enter the hot zone.

To combat the problem of oxide growth during cooling, the furnace tube is made longer by about 2.5 feet. The sample can now be pulled sufficiently out of the hot zone to cool while still being in the chamber's gas (Figures 2-16, 2-17). Figure 2-16 B shows the longer tube, the boat would sit on the left side of the chamber tube far enough away from the hot zone to cool. Figure 2-17 shows exactly how this would look after a typical anneal.

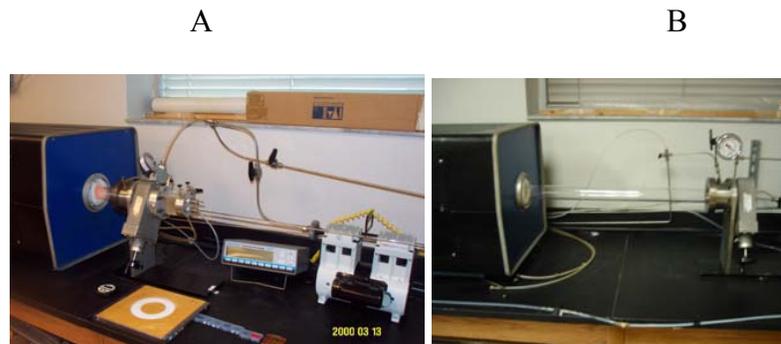


Figure 2-16. Furnace elongation where A is before and B is after

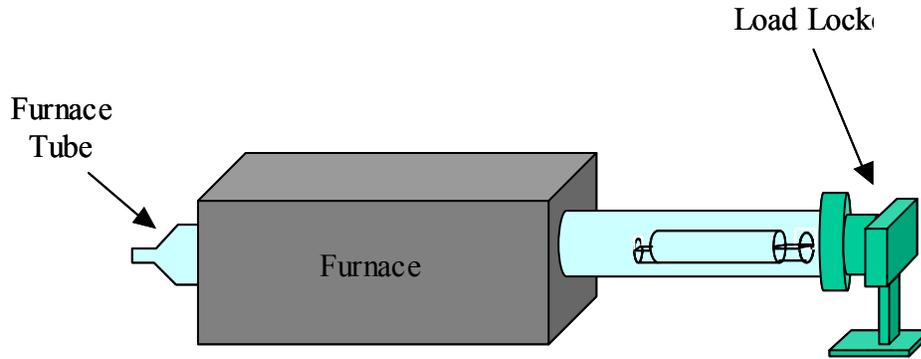


Figure 2-17. Furnace schematic of sample boat outside of furnace hot zone

Breakage is no longer an issue due to the boats new more robust design. The chambers new length and the use of a magnet will mean the sample is never exposed to air at temperatures far above room temperature. All these changes do not enable us to use a combustible gas like pure hydrogen, but it does make the chamber more versatile for future changes.

The heating of the gas as it travels through the quartz tube was the next problem. Originally as seen in the gas flow diagram in Figure 2-12, the gas is pulled from the sample entry side. When the vacuum pump is initially turned on the gas flow rate through the system is relatively high and the gas temperature is very hot. The vacuum pump however is not designed to sustain hot gas temperatures. To alleviate this problem the exhaust was put on the opposite side of the pump as seen below in Figure 2-17.

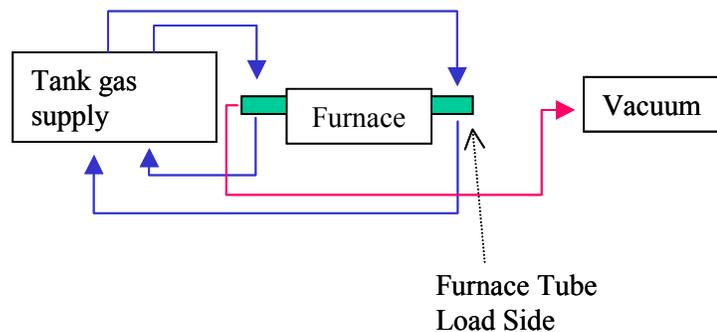


Figure 2-18. Gas flow schematic of the amended system

Now the gas must flow through a longer stainless steel section before it reaches the pump. Succeeding the above change, discoloration was observed on the exit portion of the stainless steel tube. Further heat extraction was achieved by both using a refrigerating water circulator external from the building, and cooling the exit and entry portions of the tube. Use of the external water circulator was also advantageous because if the water circulation sprung a leak, only the gallon of water present in the circulators reservoir would be lost. This would mean that the lab would never be in danger of flooding if such an event did occur.

The entry portion of the chamber had been water cooled in the original design however the opposite end had no such capability. To outfit this side with cooling ability a copper tube was wound around the tip of the tube and put in series with the cooling portion already installed.

At this juncture all of the intuitive problems with the system had been solved. This did leave however the functional problems that were not considered earlier. Among the most important aspects of the actual furnace tube was its ability to prohibit the growth of SiO_2 . SiO_2 could come from a leak in the chamber or it could be residual if proper purging techniques are not utilized.

Leakage was originally determined to be a problem. Its evidence could be observed both in the amount of oxide grown and the loss of vacuum during anneals without an active pumping vacuum. Making sure all sections of tubing prior to the exhaust were stainless steel with swagelock fittings solved the problem. In addition to the stainless steel, all portions of the system that were not essential during anneal were isolated. The isolation included the vacuum gauge, the gas flow entry point, and the

vacuum pump itself. The flow meter was completely bypassed to guard against possible leaks. At any time in an anneal all of those components can be isolated from the system using an on off 2-way flow valve.

After implementing all of the above changes, samples run in the chamber where still observed to grow oxide. This oxide was thought to come from residual gas present in the tube after loading. The typical rule is that there must be at least 20 volume changes when trying to purge a system. There were two problems with this method of purging. Since the flow meter was completely bypassed, measuring volume change was not possible. The second problem came from the design of the boat. The boat shaft is hollow inside and because of this, a hole was put in the shaft so gas expansion would not be a problem. This means however that the air that has diffused into the sample boat shaft during sample loading diffuses out of the shaft into the furnace tube during annealing. Even if purging was done for 20 volume changes, it would not purge the shaft of the boat because the shaft cavity only has one opening making it a stagnant point orifice. To see if this was the cause of the oxidation a vacuum and purge (VP) method was devised. After the tube has gone through some amount of normal purging a vacuum is pulled down to about 40 Torr and then alleviated with the argon hydrogen mix. This VP process is done 12 times to insure that air is being evacuated from all parts of the system. When practiced this resulted in a 20 Å reduction in oxide growth. The VP process is good for purging the furnace tube and the sample boat tube however it has diminishing returns.

To alleviate the problem from the sample boat decisively, holes were put in the boats sides so gas could easily flow into and out of them.

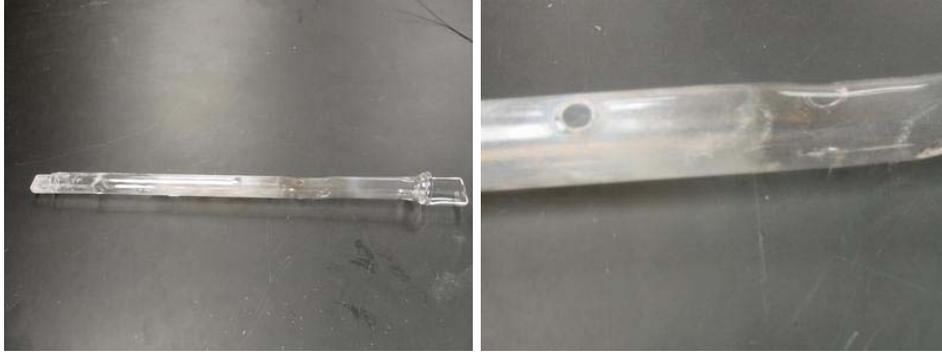


Figure 2-19. Pictures of the boat showing the holes that were put in to control oxidation.

The final place that an oxidizing gas could be coming from is the water that may be on the inside of the entry side of the tube. Since the tube is now cooled on both sides, the one farthest from the heating zone can get very cold. Raising the temperature of the water was not an option because the opposite end still needed to be cooled. To combat this problem the entry portion of the tube was taken out of the cooling circulation. This meant that it did heat up, but it was not hot enough to cause any problems in the annealing process.

The current furnace is now believed to be capable of creating the environment that will possibly induce ESSV or at least silicon surface diffusion within reasonable cost and scalability limits.

CHAPTER 3 EXPERIMENTAL

The experimental section of this thesis will cover both the experiments designed to develop a method for processing, and the experiments to test their result. The first section consists of the oxide experiments designed to find the best method for prohibiting oxide growth prior to and during sample annealing. The second portion covers the method testing, which will indicate if this process is successful in forming ESSVs.

3.1 Oxide Experiment

After all the changes made to the equipment, oxide was still observed to grow on all processed samples. The focus of this set of experiments is to find a chamber gas condition and method that will yield no oxide when compared to an unannealed control. The process variables below are what can be changed to develop the method.

1. Cooling Time
2. Purge Time
3. Number of VPs
4. Pressure

Each of these variables will result in a superposition of oxide thickness, meaning if all others are held constant, varying one can yield distinguishable differences.

By nature variables 1-3 are not optimizable variables. This means that there is no single value for which the experiment will work best. The processing quality increases with each of these variables and, if done to excess would not hurt the process or cause more oxide growth. That being said there is a diminishing return for each of them. There is a point at which increasing the amount will have no discernible effect on the process.

This parabolic nature makes their testing far more simplistic than a variable that has one particular optimal value.

It should be noted that process variables 1-3 will all be done at 10torr in an argon hydrogen mix because those are the conditions which best match Toshiba's experiments. A 10torr anneal in the furnace system will mean that the pump is kept on and no flow is permitted during the anneal.

Cooling time is the only post process variable among the four. The cooling time's optimal value does not affect the best circumstance for silicon surface diffusion, but it is necessary that we minimize its effect in order to test the other three preprocess variables. Oxide growth has a parabolic nature in that it grows exponentially at first and then the growth rate diminishes. If the oxide grown during cool down is so thick oxygen can not diffuse to the silicon surface, any changes made to the other process variables will go undetected.

3.1.1 Experiment 1

This experiment is designed to see if cooling time has an effect on oxide growth. Cooling time in specific is the time the sample spends inside the chamber still in argon hydrogen but outside of the hot zone. If the sample has not had enough cooling time it will still be hot when exposed to atmosphere and will result in exponential oxide growth. To test whether this is so, the following were done to three samples.

1. All three samples were put in a buffered oxide etch for 2 min. The etching rate was calculated to be 18 Å/sec so 2 min is far more than necessary to ensure that the 20Å of native oxide is consumed.
2. Sample 1 is put aside as the control. It will not be used in any other part of the experiment. Sample 1 is only for an oxide comparison of the processed samples.
3. Sample 2 is put in the chamber and sealed 10 min after the etch. It then goes through a 10 min purge followed by its introduction to the hot zone. Sample 2 is

annealed for 15min where it is then taken out of the hot zone and allowed to cool with argon hydrogen flow for 13 min.

4. Sample 3 goes through the same process as Sample 2 except Sample 3 is pulled to the cooling part of the tube, the hot zone is deactivated and the sample is allowed to cool for 14 hours. The deactivation of the hot zone means that the sample was never exposed to air at anything even minutely above room temperature.

The elipsometer results are listed below in Figure 3-1.

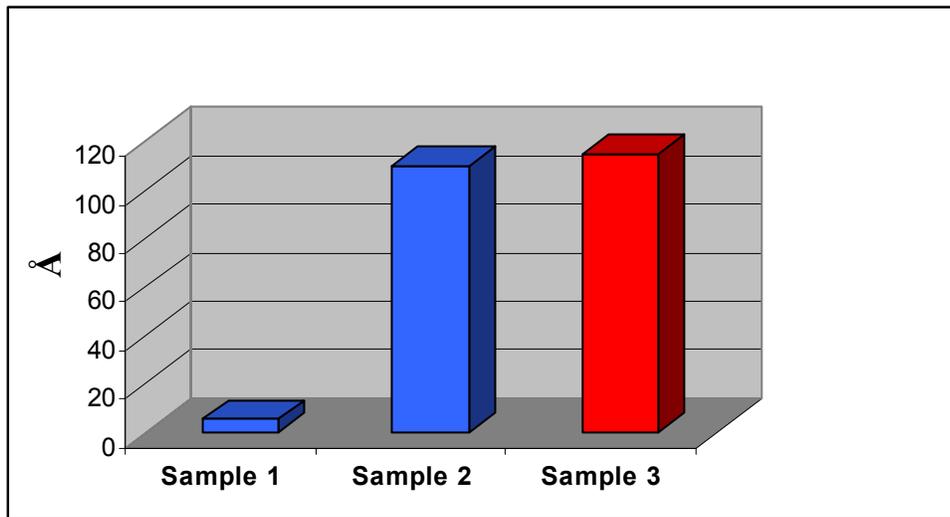


Figure 3-1. Oxide thickness results from Experiment 1

The results show that there is no real difference between Samples 2 and 3. The sample allowed to cool 14 hours in the argon hydrogen mix grew approximately the same amount of oxide as the sample that cooled for 13 min.

3.1.2 Experiment 2

Experiment 2 is designed to see if the purge time is causing the oxide problem. Purge time is defined as the amount of time gas is flowed through the tube purging all air from the chamber. The purging process is done to get rid of all residual oxygen or water vapor in the system.

- 1 All three samples were put in a buffered oxide etch for 2 min
- 2 Sample 1 is designated as the control. It will not be used in any other part of the experiment. Sample 1 is only for an oxide comparison of the processed samples.
- 3 Sample 2 is put in the chamber and sealed 10 min after the etch. It then goes through a 10 min purge followed by its introduction to the hot zone. Sample 2 is annealed for 15 min where it is then taken out of the hot zone and allowed to cool with argon hydrogen flow for 13 min.
- 4 Sample 3 goes through the same process as Sample 2 except Sample 3 is purged for twice as long.

The ellipsometry results for Experiment 2 are shown in Figure 3-2.

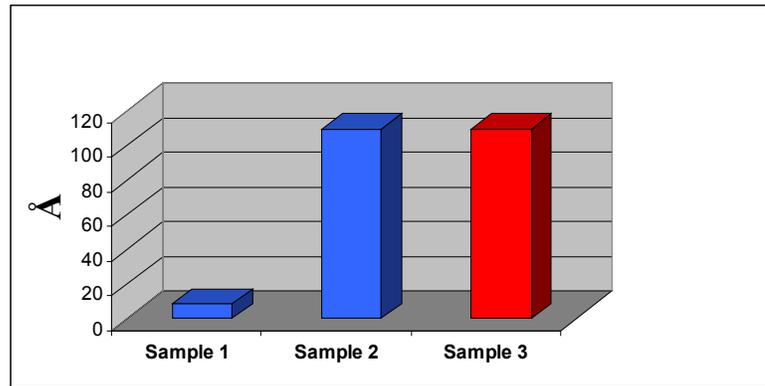


Figure 3-2. Oxide thickness results from Experiment 2

There is no discernable difference in the oxide thickness of the two annealed samples. The 20 min purge did no better than the 10 min purge.

3.1.3 Experiment 3

Experiment 3 is designed to see if successive vacuum and purge (VP) steps could affect the amount of oxide grown. A VP cycle is defined as a vacuuming step where the chamber pressure is pulled down to 40torr and then alleviated up to atmosphere with the argon hydrogen mix. One evacuation with one purge is 1 cycle of VP.

1. All three samples were put in a buffered oxide etch for 2 min.

2. Sample 1 is designated as the control. It will not be used in any other part of the experiment. Sample 1 is only for an oxide comparison of the processed samples.
3. Sample 2 is put in the chamber and sealed 10 min after the etch. It then goes through a 10 min purge followed by its introduction to the hot zone. Sample 2 is annealed for 15 min where it is then taken out of the hot zone and allowed to cool with argon hydrogen flow for 13 min.
4. Sample 3 goes through the same process as Sample 2 except 6 VPs are done just prior to introduction in to the hot zone.
5. Sample 4 goes through the same process as Sample 2 except 12 VPs are done just prior to introduction in to the hot zone.

The results from Experiment 3 can be seen in Figure 3-3. There is a difference in the oxide thickness between the samples with and without VPs. There is however no discernable difference between the sample with 6 VPs and the one with 12.

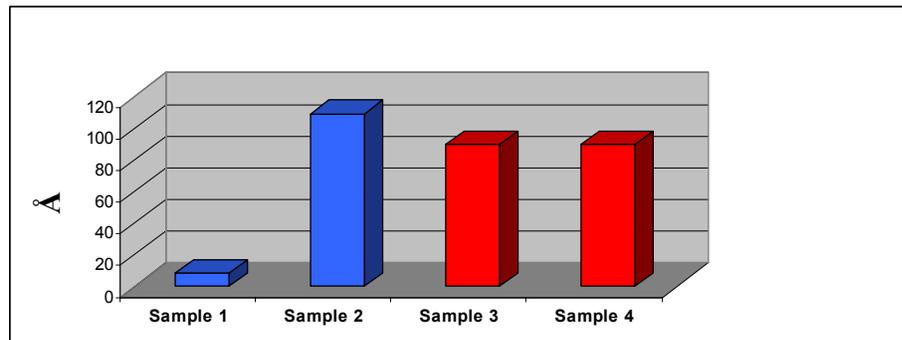


Figure 3-3. Oxide thickness results from Experiment 3

3.1.4 Experiment 4

Experiment 4 is design to see if there is an optimal pressure for annealing that will yield the least amount of oxide growth. It also should be noted that chamber pressure is regulated through argon hydrogen flow during annealing. This fact means that having a flow meter yields no extra information if the chamber pressure is monitored. It should also be noted that in this particular experiment each sample run is actually composed of two pieces of silicon run at the same time through the same conditions. Here each set of

samples shall be referred to with a single sample number. Two silicon pieces were used to make sure the elipsometer was not giving contradictory information on the same sample run. It is a well-known fact that the elipsometer has high precision on the same sample however the precision within the same run is also important.

1. All five were put in a buffered oxide etch for 2 min.
2. Sample 1 is designated as the control. It will not be used in any other part of the experiment. Sample 1 is only for an oxide comparison of the processed samples.
3. Sample 2 is put in the chamber and sealed 10 min after the etch. It then goes through a 10 min purge followed by its introduction to the hot zone. Sample 2 is annealed for 15 min where it is then taken out of the hot zone and allowed to cool with argon hydrogen flow for 13 min.
4. Sample 3 goes through the same process as Sample 2 except the chamber pressure during the anneal was adjusted to 40 Torr. This was done by changing the pressure regulator on the argon hydrogen tank until the chamber pressure was measured as 40 Torr.
5. Sample 4 goes through the same process as Sample 2 except during the anneal the chamber pressure was atmospheric with no flow.
6. Sample 5 goes through the same process as Sample 2 except during the anneal the chamber pressure was atmospheric with flow. The flow was adjusted to be the same regulator pressure that was used during the 40 Torr anneal.

Figure 3-4 shows the outcome of each sample. Here it can be observed that the thinnest oxide comes from the samples with positive flow and no vacuum (Sample 5).

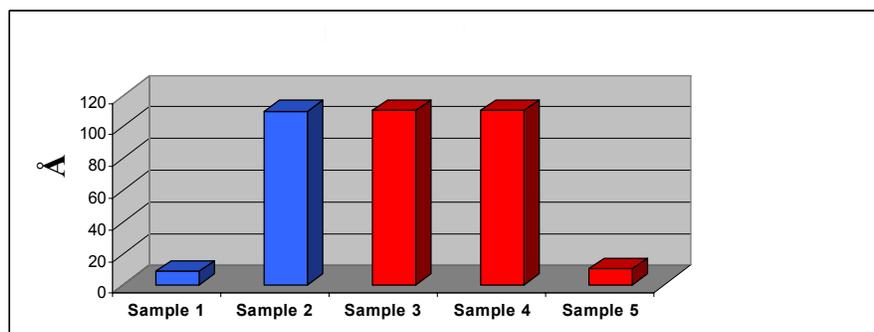


Figure 3-4. Oxide thickness results from Experiment 4.

It should be noted that a pitting phenomena was observed on all samples that where exposed to a flowing gas. Though this did occur in every flowing sample run it did not occur on all parts of all samples. Because there where two silicon pieces in each run, in some cases there were small portions of overlapping silicon. In every case the overlapped silicon never exhibited the pitting phenomena.

The elipsometer on both pieces of silicon always read the same within about 8%. This is the same deviation recorded on samples that did not overlap and samples that did not experience the flowing conditions.

3.1.5 Experiment 5

Experiment 5 is designed to see if oxide can be consumed by reducing the surface.

1. Two samples were used, each having about 500 Å of oxide on them.
2. Sample 1 is designated as the control. It will not be used in any other part of the experiment. Sample 1 is only for an oxide comparison of the processed samples.
3. Sample 2 is put in the chamber and sealed 10 min after the etch. It then goes through a 10 min purge followed by its introduction to the hot zone. Sample 2 is annealed for 15 min with no vacuum and a constant flow of argon hydrogen. It is then taken out of the hot zone and allowed to cool with argon hydrogen flow for 13 min.

As seen in Figure 3-5 the anneal had no effect on oxide thickness. This demonstrates that the oxide cannot be reduced in this condition.

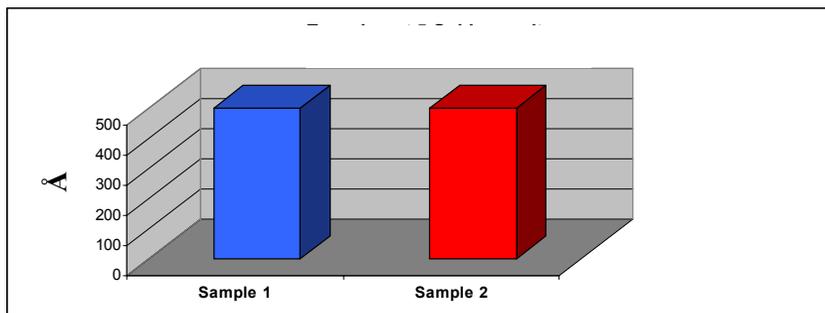


Figure 3-5. Oxide thickness results from Experiment 5.

3.2 ESSV Experiments

Originally the test conditions for creating ESSVs were to be done at two temperatures, four pressures, and four different annealing times. After the oxide experiments described above, it became obvious that none of these sub matrixes would even have a chance to induce surface migration.

Experiment 4 proved the only condition to be capable of not growing oxide is positive pressure. The pitting will be bypassed by covering the sample with a BOE etched piece of silicon. This will hopefully not only prohibit pitting but will also inhibit oxide growth due to two surfaces competing for oxidation.

This matrix is performed in approximately the same method as experiment three's Sample 4. It will however, have positive flow during the anneal. It is thought that this method is the best for creating conditions that will be successful in producing ESSVs.

Figure 3-6 shows the before and after pictures of a trench structure. These trenches are $0.3\mu\text{m}$ wide and $5\mu\text{m}$ deep. Only the 15 min anneal is displayed below because it is the most likely to have any evidence of surface diffusion. All the other runs at 1100°C and 1000°C showed the same results.

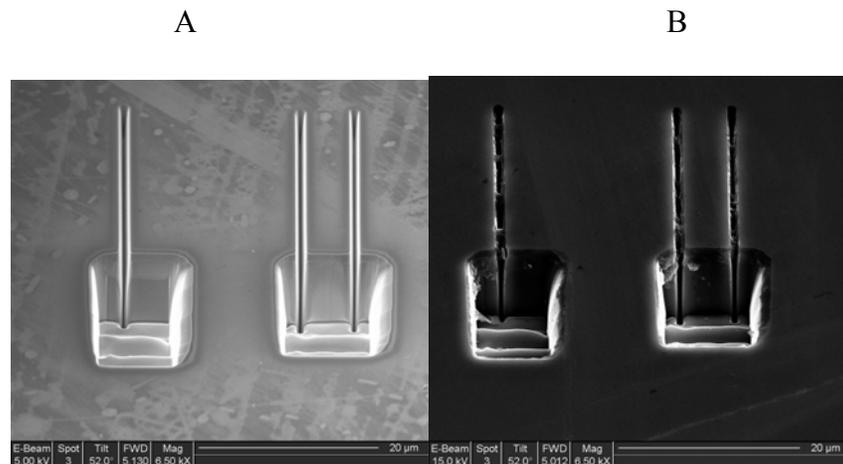


Figure 3-6. SEM picture of a trench (A) before and (B) after 15 min anneal.

CHAPTER 4 DISCUSSION

4.1 Individual Experiment Discussion

4.1.1 Discussion of Experiment 1

Experiment 1 proves that the cooling time is not a factor in contributing to oxide growth. If cooling time was a factor, Sample 3 would have grown less oxide than Sample 2.

Sample 2 and 3 both have considerably more oxide than the control. They have the same amount of oxide shown in succeeding experiments. This evidence suggests that a cooling time of 13 min had no effect on oxide growth.

4.1.2 Discussion of Experiment 2

Experiment 2 was designed to see if purge time was a factor in oxide growth. It should be noted that there is no flow meter on the argon hydrogen tank. The regulator on the argon hydrogen tank controls the flow. The same pressure is used for Sample 2 and Sample 3. This means that while the precise flow rate is unknown, it is however constant between the two runs making them comparable.

The results here show that doubling the purge time has no effect on the oxide growth. The effects of purging are assumed to be diminishing with increased purging time, so if doubling purging time has no effect, then it can also be assumed that tripling or quadrupling purge time would have no effect.

4.1.3 Discussion of Experiment 3

Experiment 3 was designed to see if VP cycles were a factor in oxide growth. VPs did show an effect on oxide growth. 6 VPs resulted in 20Å less of oxide while 12 VPs show no change from 6.

While VP cycles do have an effect on the oxide growth, they do not substantially affect the outcome.

4.1.4 Discussion of Experiment 4

Experiment 4 was designed to see if there is an optimal pressure for annealing that will yield the least amount of oxide growth. The experiment shows that there might be an oxygen or water vapor source somewhere in the system. Sample 5 (positive flow during anneal) has approximately the same amount of oxide as the control. This implies that there may be a leak in the system that allows enough oxygen to grow oxide.

4.1.5 Discussion of Experiment 5

Experiment 5 is designed to see if it is possible to reduce the surface by having a positive pressure of argon hydrogen. Equation 2.3.1 is naturally driven toward SiO₂. If the chamber contains enough hydrogen, there will be more constituents for the reverse reaction, and reduction may be possible. This is a simplification based completely on collision theory and does not take the energetics into account. The results suggest that a purely collisional assumption is an over simplification that does not describe the events accurately. Experiment 4 proved oxide growth could be inhibited. Unfortunately experiment 5 proved that the system has no other way to prohibit oxidation.

The original assumption is that if oxide can be reduced at some pressure, there is some process condition at which oxide is about to be formed and about to be reduced all at the same time. At this point process annealing can take place. There would be a pre-

process anneal at one pressure used to reduce native oxide grown in transition, followed by an anneal run at a lower pressure to induce surface migration (Figure 4-1).

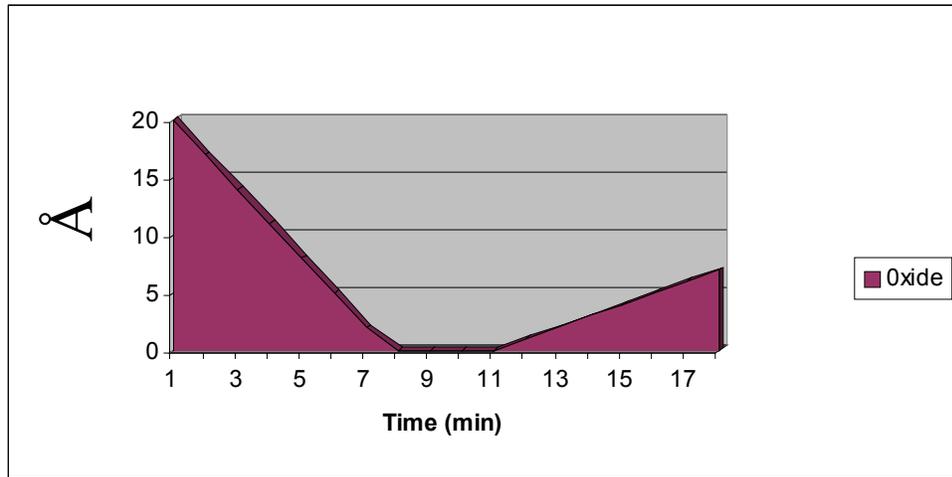


Figure 4-1. Graph showing the desired effect of experiment 5.

4.2 Discussion of Pitting

Pitting was observed to happen on all samples that experienced argon hydrogen flow during their anneal. Two facts suggest that this phenomenon is a result of the active movement of hydrogen over the surface. The first is that the pitting only happened on the top sample. Only the top sample would actually experience active movement. The next logical thought is that the chamber gas never got to the surface of the bottom sample however, the second fact is that the oxide was equal on both samples. This suggests that the top sample experiences the same gas mixture as the bottom. The only real difference between them is the active flow over the top sample. One can be reasonably certain that the hydrogen is the main constituent causing pitting. This is corroborated by a sample run in pure hydrogen (Figure 4-2). This sample is run in 99% hydrogen for 30 min. at 1130°C. This same pitting is seen at 1100°C.

It is likely that Toshiba did not flow hydrogen at as high of a rate. If they ran their 10 Torr experiments the same as Experiments 1-4, they had no flow and pulled vacuum continuously. The driving force of the pitting could either be oxygen or hydrogen. Hydrogen is definitely in the system because of the premixed chamber gas. It is unlikely that oxygen is the main cause of pitting because any mix with hydrogen should form water vapor. It may also be a mixture of the two. Oxygen and hydrogen etching are possible so both will be discussed.

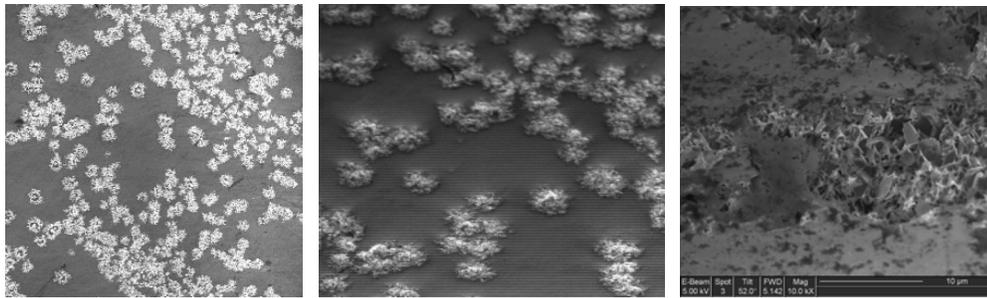


Figure 4-2. SEM picture showing the pitting phenomena at 150x 0 tilt, 150x 52°, and 10000x 52° respectively.

During normal oxide growth SiO_2 is formed however sometimes a more volatile SiO is formed [23,24]. The formation of SiO leads to a desorption from the surface causing etching. This has been observed to occur at high temperatures and low oxygen pressures [25]. Though etching is the loss of surface material and oxidation is the gain, simultaneous oxidation and etching is documented [23]. The mechanism by which the simultaneous interaction takes place is disputed. There are those who have done modeling of etch and oxidation reactions with one oxygen species like Hanon et al [26,27]. There are also those that model it with two oxygen species consisting of an O_α and an O_β like Engel and associates [29-30].

The phenomena described by the literature [25] suggest that if this was oxygen etching the features observed would be on the order of a few monolayers deep, and the

oxide capped Si-nanoprotusions 10\AA to 30\AA high. This is not consistent with the observed etch pits and Si protrusions. They are observed to be at least 4 orders of magnitude larger. The difference in size could be attributed to the annealing conditions used in the paper. Albao's temperature [25] was only 870K held for a time long enough to get a monolayer of depth in etching. The conditions covered here are 503K higher possibly resulting in exaggerated features. Simulations of what this phenomena looks like at 870K are illustrated in Figure 4-3 [25]. Figure 4-3 (a) is a $3000\text{\AA} \times 3000\text{\AA}$ area and Figure 4-3 (b) is a $780\text{\AA} \times 780\text{\AA}$ area, which is far smaller than the $20\mu\text{m} \times 20\mu\text{m}$ area in the highest magnification of Figure 4-2.

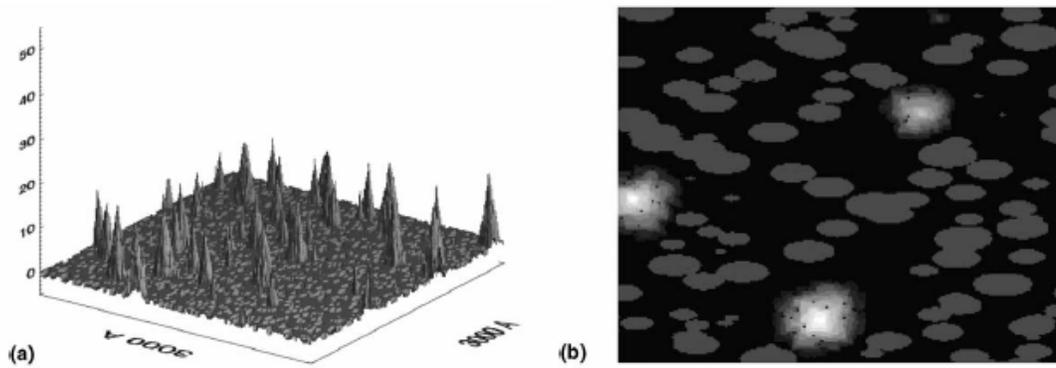


Figure 4-3. Simulations of oxide-capped Si-nanoprotusions (a) and elliptical etching pits (b).

Their evidence suggests that this phenomena may be taking place however it should not be the primary driving force of pitting. The presence of hydrogen and the lack of oxygen as a primary chamber gas support this. There is however insufficient evidence to rule out oxygen etching since we do know there is oxygen in the chamber from the measured oxidation thickness.

Hydrogen etching can occur in the chamber due to the 4% hydrogen source tank. The pitting was only observed with anneals that had an active flow. The hydrogen more

likely causes pitting because the flow rate of the source gas is the only thing that changes when the samples were annealed at different pressures. If the pitting was caused by an oxygen leak, the same pitting would have been observed at 10torr. That pressure has no flow but does have an active vacuum pull. The previous assumes that the oxygen comes from a leak in the chamber system and not an oxygen source near the source tanks. A leak near the source tanks would also explain the lack of oxygen etching in the 10torr anneal.

Hydrogen etching happens when silane or SiH_4 is formed [31]. This happens with the progression of equation 4.1 and 4.2 given below [31].



Silane is a very volatile gas that will leave the surface immediately after it is formed. Boland suggests that silane is formed if a high enough flux of hydrogen is used [31], which would explain the pitting only occurring during active flow.

Hydrogen etching appears to be a viable explanation for the etching phenomena. A mixture of both oxygen and hydrogen etching is unlikely due to their interaction before oxygen could collide with the sample. This does not rule out however that it is possible. With the knowledge of the two phenomena the pits are at least understood. In the future achieving higher pressures without increased flow would alleviate this problem.

4.3 Discussion of Overall Oxide Experiments

The oxide experiments prove that the system is incapable of creating the process conditions originally desired. The system cannot pull a 10torr vacuum and anneal samples without growing considerable oxide. It can be said however that there is a process condition at the desired 1100°C that does not grow oxide. Though this reduces

the amount of tests performed in the next phase of experiments, it does have some advantage. If surface diffusion is achieved it will mean that not only is the pure hydrogen gas mixture not necessary, the vacuum pressure is also not necessary. This will mean a lot in the focus of this thesis. If neither the chamber gas nor the chamber pressure is vital, scalability will be orders of magnitude easier.

Further analysis of the situation's energetics reveal the most probable reason for the process oxide growth. Figure 4-4 A below is an Ellingham diagram and Figure 4-4 B is specifically the portion that illustrates SiO_2 . From this chart the threshold partial pressure of formation at 1100°C is observed to be 5×10^{-22} torr. This means that the partial pressure of oxygen would have to be lower than 5×10^{-22} torr to reduce the oxide. Further insight comes from the threshold $\text{H}_2:\text{H}_2\text{O}$ ratio which is 3.65×10^5 . The purity of the sources gas is 99%, which is not sufficient to reach the threshold with only 4% hydrogen. The ratio calculated by the gas law equations suggests it's around 13.98. The calculated ratio is three orders of magnitude smaller than that needed to create a reducing ambient.

The amount of oxide grown ($100\text{\AA}/15$ min) begs the question of how much oxygen is in the system. Based on the purity there could be as many as 1.46×10^{16} oxygen molecules in the chamber. The amount that covers the sample to give the oxide thickness recorded is about 5×10^{10} molecules. There are six orders of magnitude more than the needed amount to grow the recorded oxide thickness.

The Deal Grove equations predict 490\AA of oxide thickness at 1100°C with 15 min of annealing in dry oxygen. The measured 100\AA amount seems high but could be possible once the parabolic nature of oxidation is taken into account. These

approximations do not suggest necessarily that there is a leak or another source of oxygen.

This unfortunately means that with the process equipment and materials it will be impossible to reduce oxide, or definitively not grow oxide.

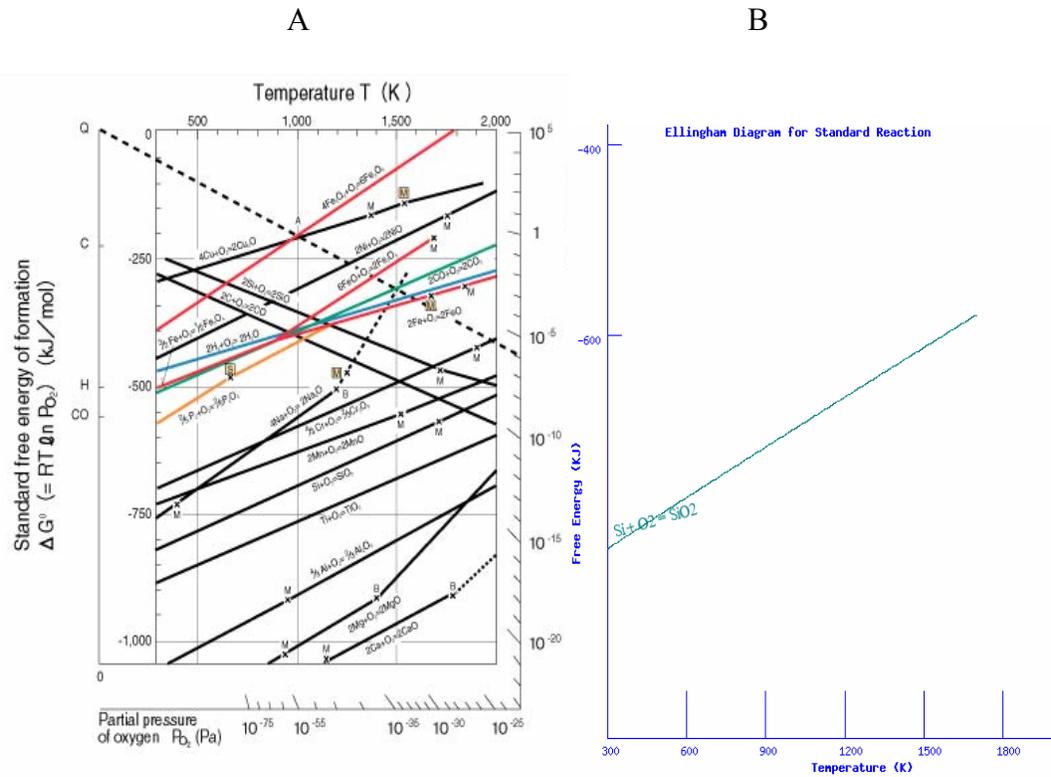


Figure 4-4. Ellingham diagrams of (A) general oxides and (B) SiO_2

4.4 Discussion of ESSV

The ESSV experiments were designed to test the success of the developed process. The results show that this process does not create ESSVs. The answer to this undoubtedly lies within the energetics of oxide growth. It was proven that the sample could be annealed without growing more oxide than the control. It was not proven that the oxide could be reduced. The Ellingham diagram shows a particular threshold at which a min change in pressure can cause oxidation or reduction. It is clear that with

these materials that this process is above the threshold at all possible process conditions and methods.

CHAPTER 5 CONCLUSIONS AND FUTURE WORK

5.1 Conclusion

Though the scalability of this process would have been a lot easier if successful, the vacuum quality and chamber gas purity have proven to be indispensable conditions that must be satisfied in order to form ESSVs. Unfortunately there does not exist a 4% Argon- Hydrogen mixed gas with high enough purity to satisfy the ratio needed to inhibit oxidation at the tested pressures.

To solve the problem of oxidation a greater amount of hydrogen is needed to satisfy the $H_2:H_2O$ ratio (3.65×10^5), or a partial pressure of oxygen below the 5×10^{-22} Torr calculated from the Ellingham diagram. If neither of these criteria is met, oxidation is inevitable.

5.2 Future Work

A gettering material can be used to control the gas localized to the region close to the sample. Using a material that has an oxide with a lower chemical potential will help control the amount of oxygen and possibly create an environment that will prohibit oxide growth.

A stronger pump capable of pulling lower vacuum pressures could also control oxide formation. Going to a pressure below 5×10^{-22} Torr may not be a practical solution but going to pressures lower than the 10 Torr reached could possibly work. There is no way to calculate the amount of oxygen in this system, therefore calculating the partial pressure is not possible here. This means that for this system there is no way to

figure out how far the partial pressure of oxygen is from its decompositional value. The oxygen partial pressure may not be as high as the argon- hydrogen partial pressure. It may be possible to pull a total chamber vacuum pressure considerably greater than the decompositional partial pressure of oxygen and still achieve a partial pressure equal to or below the decompositional pressure.

LIST OF REFERENCES

1. T. Sato, I. Mizushima, Y. Tsunashima, and N. Aoki, "A New Substrate Engineering for the formation of Empty Space in Silicon (ESS) Induced by Silicon Surface Migration," *Technical. Digest. - International Electron Devices Meet*, pp. 517, 1999.
2. B. Widrow and F.-L. Luo, "Microphones arrays for hearing aids: An overview," *Speech Communications*, vol. 2, pp. 139-146, 2003.
3. D. P. Arnold, T. Nishida, L. N. Cattafesta, and M. Sheplak, "A directional acoustic array using silicon micromachined piezoresistive microphones," *J. Acoust. Soc. Am.*, vol. 113, pp. 289-298, 2003.
4. F. H. Netter, *Atlas of Human Anatomy*, 3rd ed. Teterboro, N.J: Icon Learning Systems, 2003.
5. D. P. Arnold, S. Bhardwaj, S. Gururaj, T. Nishida, and M. Sheplak, "A piezoresistive microphone for aeroacoustic measurements," presented at Proceedings of ASME IMECE 2001, New York, NY, 2001.
6. J. Miao, R. Lin, L. Chin, Q. Zou, S. Y. Lim, and S. H. Seah, "Design considerations in micromachined silicon microphones," *Microelectronics Journal*, vol. 33, pp. 21-28, 2002.
7. T. Tajima, T. Nishiguchi, S. Chiba, A. Morita, M. Abe, K. Tanioka, N. Saito, and M. Esashi, "High-performance ultra-small single crystalline silicon microphone of an integrated structure," *Microelectronic Engineering*, vol. 76-68, pp. 508-519, 2003.
8. P. Rombach, M. Mullenborn, U. Klein, and K. Rasmussen, "The first low voltage, low noise differential silicon microphone, technology development and measurement results," *Sensors and Actuators A*, vol. 95, pp. 196-201, 2002.
9. M. Esashi, H. Fujita, I. Igarashi, and S. Sugiyama, *Micromachining and Micromechatronics*: Baifukan, 1992.
10. H. Guckel, T. Randazzo, and D. W. Burns, "A simple technique for the determination of mechanical strain in thin films with application to polysilicon," *Journal of Applied Physics*, vol. 57, pp. 1667-1675, 1985.

11. H. Guckel, T. Randazzo, and D. W. Burns, "Fine-grained polysilicon films with built-in tensile strain," *IEEE Transaction Electric Division*, vol. ED-35, pp. 800-801, 1988.
12. S. Chiba, A. Morita, K. Shoda, T. Tajima, and F. Ando, "Construction of a microphone consisting of an electro-acoustic conversion element on a silicon chip," presented at Proceedings of the Acoustic Society of Japan, 1999.
13. S. Chiba, A. Morita, K. Shoda, and T. Tajima, "Consideration on the sensitivity of silicon microphones," presented at Proceedings of the Acoustic Society of Japan, 1999.
14. A. Mizoguchi, "Design of a small directional condenser microphone," *Journal of the Acoustic Society of Japan*, vol. 31, pp. 593-601, 1975.
15. J. H. Jerman, "The fabrication and use of micro-machined corrugated silicon diaphragms," *Sensors Actuators*, vol. A21-A23, pp. 988-992, 1990.
16. A. Mizoguchi, "Doctoral Thesis," Aichi, Japan: Nagoya University, 1977.
17. R. Viswanath, V. Wakharkar, A. Watwe, and V. Lebonheur, "Thermal Performance Challenges from Silicon to System," *Intel Technology Journal*, pp. 1-15, 2000.
18. L. Jiang, J. Mikkelsen, J.-M. Koo, D. Huber, Shuhuai, L. Zhang, P. Zhou, J. G. Maveety, R. Prasher, J. G. Santiago, T. W. Kenny, and K. E. Goodson, "Closed-Loop Electroosmotic Microchannel Cooling System for VLSI Circuits," *IEEE Transaction on Components and Packaging Technologies*, vol. 25, pp. 347-355, 2002.
19. H. Kuribayashi, R. Hiruta, R. Shimizu, K. Sudoh, and H. Iwasaki, "Shape transformation of silicon trenches during hydrogen annealing," *J. Vac. Sci. Technol.*, vol. 21, pp. 1279-1283, 2003.
20. Y. Yang, E. S. Fu, and E. D. Williams, "An STM study of current-induced step bunching on Si(111)," *Surface Science*, vol. 356, pp. 101-111, 1996.
21. J. William D. Callister, *Materials Science and Engineering An Introduction*, 5th ed. New York: John Wiley & Sons, Inc, 2000.
22. J. Bhardwaj, H. Ashraf, and A. McQuarrie, "Dry Silicon etching for MEMS," presented at Proceedings of Symposium on Microstructures and Micro-fabrication Systems at the Annual Meeting of the Electrochemical Society, Quebec, Canada, 1997.
23. Y. Wei, Y. Hong, and I. S. T. Tsong, "Oxygen etching of the Si(100)-(2x1) surface," *Applied Surface Science*, vol. 92, pp. 491-496, 1996.

24. M. A. Albao, D.-J. Liu, C. H. Choi, and M. S. Gordon, "Atomistic modeling of morphological evolution during simultaneous etching and oxidation of Si(100)," *Surface Science*, vol. 555, pp. 51-67, 2004.
25. J. J. Lander and J. Morrison, "Low voltage electron diffraction study of oxidation and reduction of silicon," *Journal of Applied Physics*, vol. 33, pp. 2089, 1962.
26. J. B. Hannon, M. C. Bartelt, N. C. Bartelt, and G. L. Kellogg, "Etching of the Si(100) surface with molecular oxygen," *Physics Review Letter*, vol. 81, pp. 4676-4679, 1998.
27. M. C. Bartelt, J. B. Hannon, A. K. Schmid, C. R. Stoldt, and J. W. Evans, "Island formation during deposition or etching," *Journal of Colloid Surface A*, vol. 165, pp. 373, 2000.
28. T. Engel, "The interaction of molecular and atomic oxygen with Si(100) and Si(111)," *Surface Science Report*, vol. 18, pp. 91-144, 1993.
29. J. R. Engstrom, D. J. Bonser, M. N. Nelson, and T. Engel, "The reaction of atomic oxygen with Si(100) and Si(111).1. oxide decomposition, active oxidation and the transition to passive oxidation," *Journal of Surface Science*, vol. 256, pp. 317-343, 1998.
30. J. R. Engstrom and T. Engel, "Atomoc versus molecular reactivity at the gas-solid interface - the adsorption and reaction of atomic oxygen on the Si(100) surface," *Physics Review B*, vol. 41, pp. 1038-1041, 1990.
31. D. R. Olander, M. Balooch, J. Abrefah, and W. J. Siekhaus, "Modulated molecular-ebeam studies of the surface-chemistry of silicon reaction with reactive gases," *Journal of Vacuum Science*, vol. 1404, pp. 3302-3310, 1987.
32. J. J. Boland, "Role of Bodn-strain in the chemistry of hydrogen on the Si(100) surface," *Surface Science*, vol. 261, pp. 17-28, 1992.
33. S. D. Senturia, *Microsystem Design*, 3rd ed. Norwell, Massachusetts: Kluwer Academic Publishers, 2001.

BIOGRAPHICAL SKETCH

William Harrison was born in Greensboro, North Carolina, in 1979. He attended high school at Dudley Science and Math Academy. He received a Bachelor of Science degree in mechanical engineering from the University of Michigan. He earned his master's degree at the University of Florida, in materials science and engineering.