

FABRICATION AND CHARACTERIZATION OF COMPOUND SEMICONDUCTOR
DEVICES AND THEIR ELECTRICAL AND THERMAL SIMULATION

By

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by

Rishabh Mehandru

This document is dedicated to my parents; to my sister Ritu and her husband Ish; and to my fiancée Bharati, who has always stood by my side, through thick and thin.

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Scandium Oxide (Sc_2O_3) and Magnesium Oxide (MgO) were demonstrated as promising gate dielectrics for GaN-based Metal Oxide Semiconductor High Electron Mobility Transistors (MOSHEMTs) and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) along with being very good passivation layers for GaN/AlGaN HEMTs. I-V and C-V, G-V measurements were used to characterize the interface between oxide and GaN. Interface state density and breakdown field were extracted from these measurements (experimental data). These results of MOS diodes led to the first demonstration of GaN/AlGaN MOSHEMT using Sc_2O_3 as gate dielectric. The MOSHEMTs showed ~ 40% more saturation drain-source current than that of HEMTs and gate of MOSHEMTs can be biased to +6 V as compared to max +2 V for HEMT. Use of Sc_2O_3 and MgO as surface passivation layer enhanced RF and microwave performance of these devices.

Temperature simulations on bulk GaN power diodes were performed using Finite Element analysis to compare the junction temperature of power diodes packaged with conventional wire bonding and flip-chip bonding technology. Superior heat dissipation was obtained for the flip chip bonded device. Finite difference thermal analysis of 850 nm VCSELs was carried out by writing a code in MATLAB. Thermal characteristics of 1550 nm VCSEL were also studied by using finite element analysis software called FlexPDE.

W-based Schottky contacts on GaN are attractive for applications requiring long-term thermal stability, such as combustion gas monitoring. The effect of deposition conditions on the electrical properties of W/Pt/Au Schottky contacts on n-GaN was studied.

CHAPTER 1 INTRODUCTION

The Gallium Nitride (GaN) and its related alloys based semiconductor materials have been attracting attention because of their large bandgap and their ability to operate at high power, high temperature, and high speed. Such qualities have led to investigation of these material systems for various devices including High Electron Mobility Transistors (HEMTs), Heterojunction Bipolar Transistors (HBTs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), photodiodes, and photodetectors. Tremendous commercial applications await any successful and desirable demonstration of these devices. Radio Frequency (RF) power amplification is one example where GaN/AlGaN HEMTs are sought after [9-10].

For research to sustain itself, it must be fruitful in a manner that benefits society in the long run. The subject of our study is a material (GaN) that has stormed compound semiconductor research and industries with innumerable options. It has already proved useful for traffic signals (Automotive Interior Lighting) and CD-ROMs using blue Lasers (to provide manifold increase in storage capacity). Many commercial and military wireless systems use traveling wave tubes that require high voltages (more than 2000 V), which often result in reliability problems and preclude the implementation of satellites with multiple independently targeted simultaneous beams. The greater transmitting power and higher efficiencies supplied by gallium nitride materials mean that a smaller number of higher-orbiting, multiple-beam satellites can do the same job as a larger number of low-orbiting satellites. Nitride materials will also boost the power of transmitting towers,

giving them more coverage and versatility, thus reducing the need and expense of installing more towers. In addition, the higher "linearity" and dynamic range of these gallium-nitride amplifiers mean that more signals can broadcast simultaneously without undesirable cross talk or distortion. Thus the most important use of GaN transistors will be the amplifiers for advanced military and commercial applications.

AlGaN/GaN HEMTs have been the most researched among all devices fabricated in the GaN material system. However, there are many milestones to be achieved and the work in this field is far from complete. Cheap lattice-matched substrates (a SiC 3%, Sapphire 13% lattice mismatch is currently popular) are being studied to reduce dislocation density, which degrades the device performance. Good lattice match would result in higher RF power levels in such devices, when combined with innovative designs, such as flip-chip bonded structures for better heat dissipation. Strong piezoelectric polarization in III-V materials induces a two dimensional electron gas (2DEG) at AlGaN/GaN interface, which is the basis of the carrier generation of HEMTs. The piezoelectric polarization also results in charged surface states and charged states within the device. Surface states are considered responsible for DC to RF current collapse or dispersion. This is an undesirable effect that must be controlled and minimized. These electron traps act as a negatively charged virtual gate, and limit maximum current available during microwave operation. Good (lattice-matched or otherwise) oxide can passivate these surface states, and also reduce gate leakage.

The power-utility industry can appreciably profit from the development of wide band-gap power devices. Increasing numbers of transactions on the power grid in the US will take place with the deregulation of electrical power industry. Different companies

would buy and sell power so as to obtain economically viable distribution. Electrical power distribution comprises the primary distribution system (100~2000 kW) and subsidiary transmission systems (1~50 MW). Both the primary and subsidiary distribution systems suffer from momentary voltage sags in the power grid, which ultimately affect motor drives, computers, and digital controls. If a system can eliminate power sags and switching transients, it will dramatically improve power quality. Power outage and voltage sags usually cost a fortune to the computer centers.

Hybrid vehicles and future electric vehicles need semiconductor switches that can operate at high voltage and high currents. Wide-bandgap semiconductors like GaN have an untapped potential in such applications where they would inherently have a very good figure of merit (FOM) when compared with Si, GaAs, or Ge. Electric cars, although limited by their need for batteries, offer zero tailpipe emissions, which helps limit environmental pollution. Hybrid car designs use various strategies to combine both an engine and electrical elements to gain advantages of both [1]. In both cases, inverters and DC-DC converters rated for many kilowatts serve as primary energy-control blocks.

The basic devices that form the building blocks of power electronics system are diodes, MOSFETs, gate turn-off thyristors (GTOs), MOS-controlled thyristors (MCT) or insulated-gate bipolar transistors (IGBTs). These are combined with appropriate packaging and thermal-management techniques to make subsystems of switches, rectifiers, or adjustable-speed devices. Finally they integrate to form a system such as Flexible AC Transmissions (FACTS) [164-166]. Some examples of power-electronics systems inserted between the incoming power and the electrical load are uninterruptible power supplies (UPS), advanced motors, adjustable speed drives and motor controls,

switching power supplies, solid-state circuit breakers and power conditioning equipment. Motors consume about 50% of the electricity in the US [167]. Motor repairs also cost ~US\$ 5 billion each year, which could be dramatically reduced by high-power electronic devices with smoother switching and control [2]. Moreover, the control electronics could dramatically improve motor efficiency. Other end uses of the power applications include lighting, computers, heating, and air conditioning.

Some desirable attributes of next generation, wide-bandgap power electronics include the ability to

- Withstand currents in excess of 5 kA and voltages in excess of 50 kV
- Provide rapid switching, maintain good thermal stability while operating at temperatures above 250°C
- Have small size and light-weight
- Be able to function without bulky heat-dissipating systems

For these reasons, there is a strong development effort on wide-bandgap power devices, predominantly SiC, with lesser efforts in GaN and diamond for the applications that Si-based or electromechanical power electronics cannot attain. The higher standoff voltages should eliminate the need for series stacking of devices and the associated packaging difficulties. In addition these wide-bandgap devices should have a higher switching frequency in pulse-width-modulated rectifiers and inverters.

The absence of Si devices capable for the applications in 13.8 kV distribution lines (a common primary-distribution mode) opens a major opportunity for wide-bandgap electronics. However, cost will be an issue, with values of US\$ 200~2000 per kW necessary to have an impact. It is virtually certain that SiC switches will become commercially available within 3~5 years, and begin to be applied to the 13.8 kV lines. The MOS turn-off-thyristors using a SiC GTO and SiC MOSFET are a promising

approach [2]. An inverter module can be constructed from an MOS turn-off thyristor (MTO) and a SiC power diode.

Long-distance telecommunication applications require a material system with 1.3 μm /1.55 μm capabilities, where the dispersion and attenuation of the traveling wave is minimized. Because of its low energy bandgap and high detection sensitivity at these wavelengths, InGaAs is very well suited for use in optoelectronic integrated circuits (particularly in high-speed photodetectors). Laser detection and ranging (LADAR) is another area where 1.55 μm Lasers and photodetectors find application. Laser-based detection systems can allow military aircrafts to identify enemy ground vehicles accurately in battle zones, and permit spacecraft and robotic vehicles to navigate safely through unfamiliar terrain. Face recognition and archeological surveying are nonmilitary uses of LADAR systems (Figure 1-1). Highly sensitive optical detectors that measure minute amounts of reflected laser light are used in LADAR systems that do three-dimensional modeling of scanned objects. Advances in computer technology and miniaturization have made it possible to process the gathered information very fast; which, when combined with Lasers and detectors, allows 3-D imaging of stationary and moving objects.

InGaAs MSMs would allow LADAR operation at eye-safe wavelengths. Unfortunately, the Schottky barrier height on InGaAs is quite low ($\sim 0.1\text{-}0.2$ eV) [3], leading to high dark current and, hence, to a low signal-to-noise ratio. To reduce dark current, various methods of “enhancing” the Schottky barrier are used. The most common method uses a high-bandgap lattice-matched InP [4] or InAlAs [5, 6] Schottky

enhancement layer (SEL). Detectors using SELs yield low dark current, high responsivity, and high bandwidths.

To better understand the mechanism of current transport and the effect of the InAlAs SEL in the MSM photodetector and OE mixer, 2-D opto-electric modeling was performed [138]. The 2-D helped explain two slope (dI/dV) changes (knee) in the photo I-V characteristics of the MSMPD.

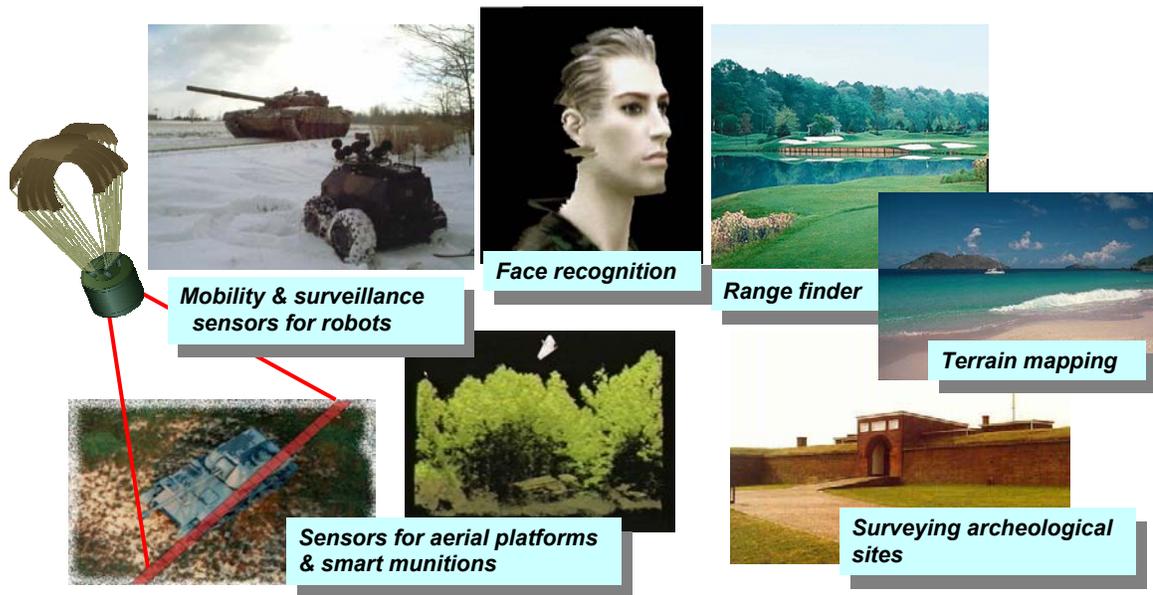


Figure 1-1. Applications of InAlAs/InGaAs OE mixer using conventional FPA and ROIC technology

Thermal management is important for device-level applications. By studying thermal characteristics, better heat-dissipation schemes can be developed resulting in longer life and enhanced efficiency of semiconductor devices. Tremendous progress has been achieved in the development of vertical-cavity surface-emitting lasers (VCSELs) for high-speed optical interconnects in high bit-rate data-transmission systems [3-8]. For local network applications, GaAs/AlGaAs based 850 nm VCSELs have already proved to be the laser of choice for short-wavelength transmissions. However, the laser

transmission distance was shown to become less than 1 km for an 850 nm VCSEL operating at 10 Gb/s. [7-8]. The low-loss window of optical fiber for 1.3 and 1.55 μm provides an opportunity for VCSEL technology to extend the transmission distance of optical fiber to more than 40 kilometers. This would be a major benefit for communications technology. Development of the long-wavelength VCSEL, however, has been slower than that of short-wavelength VCSELs (850/980 nm). Good thermal dissipation for the device design is a prerequisite for high-speed performance. A record-low thermal-resistance flip-chip bonding technique has been demonstrated with a 16×16 array of top $\text{TiO}_2/\text{SiO}_2$ mirror, implanted-apertures, and lateral current injected 980 nm VCSELs. However, there is no detailed study performed for this kind of flip-chip bonded VCSEL to confirm the temperature distribution in the active layer. Finite difference and finite element analyses were used to characterize 850 nm and 1550 nm VCSELs, respectively.

A novel flip-chip design was also studied to see the effects of enhanced heat dissipation. The temperature rise in the active region can be maintained below 16°C at 1 mW output power, with 10mA current bias for 1550 nm VCSELs. Flip-chip bonding will reduce the shift of the wavelength, peak power, threshold current, and slope efficiency during VCSEL operations.

CHAPTER 2 MOS DIODES AND INTERFACE STATE DENSITY EXTRACTION

Introduction

GaN is regarded as having tremendous potential for applications in high-temperature, high-power and high-speed electronic devices [9, 10]. Though it has a large bandgap, the device performance degrades at higher temperature due to high gate leakage resulting from a limited Schottky barrier height. Many insulators (such as Ga_2O_3 (Gd_2O_3), AlN , SiO_2 and Si_3N_4) have been proposed for use in GaN-based metal-oxide semiconductor field-effect transistor (MOSFET) structures [10-21]. Some are known to have a very high breakdown field, but they all have a large lattice mismatch to GaN, resulting in a relatively high interface state density for crystalline oxides. For example Gd_2O_3 (which has a bandgap of 5.3eV) has a large lattice mismatch of ~20% to GaN. Sc_2O_3 has a similar bixbyite structure but it also has a larger bandgap of 6.3 eV and a smaller lattice mismatch (~9.2%). Low-temperature grown oxide is typically amorphous or polycrystalline as compared to the oxide grown at higher temperatures, which is polycrystalline or single crystal. Because of less strain at the interface for amorphous oxide, the interface trap density is expected to be considerably less.

Scandium Oxide (Sc_2O_3) deposited as a gate insulator on GaN at 100°C was investigated. Transmission electron microscopy showed the resulting interface to be smooth. MOS diodes were fabricated and characterized with current-voltage (I-V), capacitance-voltage (C-V) and conductance-voltage (G-V) measurements. C-V

measurements under ultraviolet light and at higher temperature were also conducted to study the $\text{Sc}_2\text{O}_3/\text{GaN}$ MOS diodes.

Sc_2O_3 was deposited on (0001) GaN in a molecular beam epitaxy system (MBE) using elemental Sc and an electron cyclotron resonance (ECR) oxygen plasma. All oxide growths were performed in a modified RIBER 2300 MBE equipped with reflection high-energy electron diffraction (RHEED) system. Oxygen was supplied from a Wavemat MPDR 610 ECR plasma source (2.54 GHz) with 200 Watt forward power at 1×10^{-4} Torr Oxygen pressure. A standard effusion cell operating at 1130 to 1170°C was used for the evaporation of the scandium. The oxide was either dry etched in an inductively coupled plasma (ICP) system, or wet etched using hot H_2SO_4 based solutions before depositing Ti/Al/Pt/Au (200 Å /700 Å /400 Å/1000 Å) ohmic contact. Pt/Au (200 Å/1000 Å) was deposited as the gate contact.

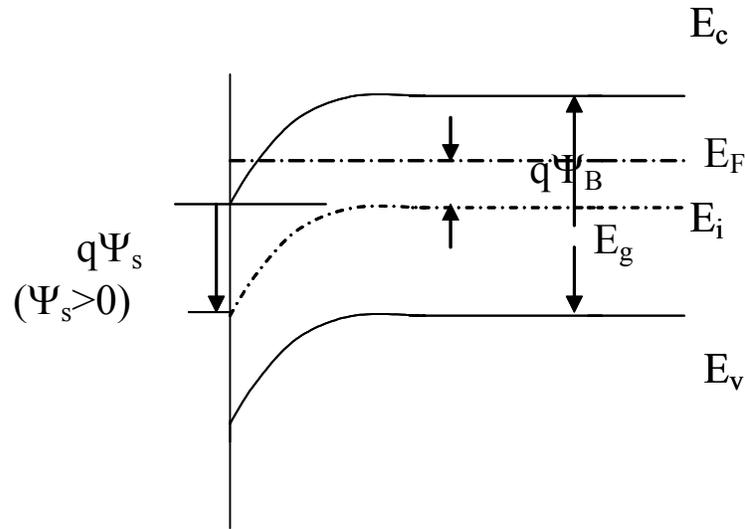


Figure 2-1. Energy band diagram at the surface of a n-type semiconductor. The potential Ψ is measured with respect to intrinsic Fermi level E_i . The surface potential Ψ_s is +ve as shown. (a) Accumulation (of majority carriers) occurs when $\Psi_s > 0$, (b) Depletion occurs when $\Psi_b < \Psi_s < 0$, (c) Inversion occurs when $\Psi_s < \Psi_b$.

An HP 4145 parameter analyzer was used to measure current-voltage characteristics of 100 μm size diodes. Capacitance and conductance were measured with an HP 4284 LCR meter. A Wentworth Labs TC100 heated chuck was used for high-temperature measurements.

Interface State Density Extraction

Terman Method

Figure 2-1 shows an energy band diagram for ideal MOS diodes with no interface states for an n-type semiconductor. The electron and hole concentrations as a function of surface potential ψ , are given by $n_n = n_{n0} \exp(q\psi/kT)$, $p_n = p_{n0} \exp(-q\psi/kT)$, where n_n and p_n are hole and electron concentration, Ψ is the band bending, k is the Boltzmann constant, and T is the temperature in Kelvin. This along with Poisson's equation,

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\epsilon_s}, \quad (2-1)$$

where ϵ_s is the permittivity of semiconductor. $\rho(x)$ is the total space charge density given by

$$\rho(x) = q(N_D^+ - N_A^- + p_n - n_n), \quad (2-2)$$

which can be solved with given the electric field, inside and on the surface of the semiconductor. Finally the charge at semiconductor surface, Q_s , is given by $Q_s = -\epsilon_s E_s$, where E_s is the electric field at the surface.

Differential Semiconductor Capacitance, C_s , can hence be calculated by

$$C_s = \frac{\partial Q_s}{\partial \psi_s}. \quad (2-3)$$

We can measure differential capacitance using an LCR meter. The capacitance-voltage method for estimating interface state density at high frequency (Terman Method) entails sweeping the DC voltage from + bias voltage (accumulation region for n-type) to – voltage (depletion region for n-type). A small ac signal is superimposed on the DC bias at all times. When the frequency of ac signal is small, the traps (at the Ψ_s corresponding to DC bias) fill and empty with ac signal, hence contributing to differential capacitance. But at higher frequency, the traps are too slow (their time constant depends exponentially on depth from conduction-band edge) to respond, so their contribution to differential capacitance is negligible. For an ideal MOS diode, we can calculate C_s for each Ψ_s , and the total capacitance is given by parallel combination of oxide and semiconductor capacitance.

Hence,

$$C_{hf} = \frac{C_s C_{ox}}{C_s + C_{ox}}, \quad (2-4)$$

$$\text{where } C_{ox} = \frac{A \epsilon_0 \epsilon_s}{d_{ox}}, \quad (2-5)$$

A is the diode area and ϵ_s is the permittivity of semiconductor. Plotting a theoretical C-V plot along with the measured one produces a ψ_s vs. V_g plot, which can then be used to determine $E_c - E_t$ at each V_g using

$$E_c - E_t = E_g / 2 - \psi_S - \psi_B \quad (2-6)$$

where E_c is conduction band edge, and E_t is trap energy level. The slope of ψ_s vs. V_g

gives the interface state density [18] by $D_{it} = C_{it}/qA$, where

$$C_{it} = \left[\left(\left(\frac{d\psi_s}{dV_g} \right)^{-1} - 1 \right) C_{ox} - C_s \right] \quad (2-7)$$

The AC Conductance Method

The interface state density calculated from Terman Method is generally an underestimate and its value is accurate only between 0.2-0.4 eV below the conduction-band edge. The AC conductance method [22] is usually used to look deep into the energy band gap and to accurately predict interface state density. The LCR meter measures impedance in the form of G_m (measured conductance) and C_m (measured capacitance), which could be used to extract the internal G_p and C_p values if R_s and C_{ox} are known (Figure 2-3). The C_{ox} is the saturation capacitance (of a C-V plot) and R_s , series resistance, can be determined from transition line method (TLM) measurements which give sheet resistance as $R_s = (\text{Sheet resistance}/2\pi) \ln(r_2/r_1)$, where r_2 is the inner radii of ohmic contact and r_1 is the radii of Schottky contact (Figure 2-2).

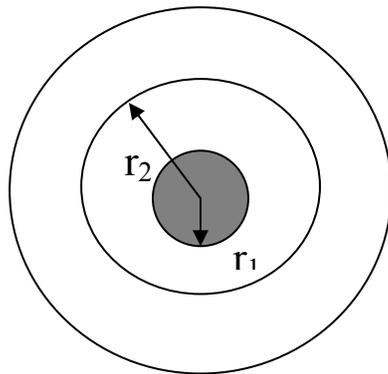


Figure 2-2. Top view of a MOS diode. Outer ring is the ohmic contact, the inner circle is the Schottky contact.

Solving the equivalent circuits shown in Figure 2-3, we get

$$C_p = \frac{-C_{ox}[(C_m^2 - C_m C_{ox})\omega^2 + G_m^2]}{\omega^4 C_m^2 C_{ox}^2 R_s^2 + \omega^2 (C_{ox}^2 R_s^2 G_m^2 + C_m^2 + C_{ox}^2 - 2C_{ox}^2 R_s G_m - 2C_m C_{ox}) + G_m^2} \quad (2-7)$$

$$\text{and } \frac{G_p}{\omega} = \frac{-\omega C_{ox}^2 (R_s C_m^2 \omega^2 + R_s G_m^2 - G_m)}{\omega^4 C_m^2 C_{ox}^2 R_s^2 + \omega^2 (C_{ox}^2 R_s^2 G_m^2 + C_m^2 + C_{ox}^2 - 2C_{ox}^2 R_s G_m - 2C_m C_{ox}) + G_m^2} \quad (2-8)$$

where ω is the angular frequency.

G_p/ω is also equal to $C_{it}\omega\tau/(1+\omega^2\tau^2)$. C_{it} and τ can be obtained by fitting curves to extracted G_p/ω (obtained above) vs ω . The value of G_p/ω at the maximum is $C_{it}/2$, and it is maximum at $\omega\tau = 1$. And $D_{it} = C_{it}/qA$. Thus D_{it} can be obtained [22].

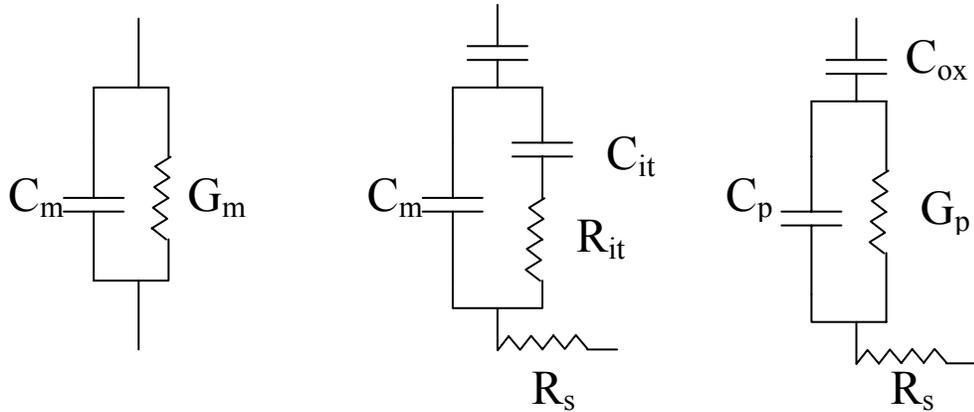


Figure 2-3. Model of MOS diode used to extract trap parameters from the experiment

Sc₂O₃/GaN Interface Characterization

Figure 2-4 shows the typical I-V characteristics of a 100 μm diameter Sc₂O₃/GaN diode. The reverse breakdown and the forward turn-on voltage were -14 and 7 V, respectively. The oxide thickness was ~ 40 nm, and the corresponding oxide breakdown field was 1.75 MV/cm at a current density of 1 mA/cm².

Room temperature high-frequency C-V characteristics are shown in Figure 2-5. Capacitance is measured as a function of gate bias, which is composed of a high-

frequency ac signal superimposed on a slowly changing (0.05 V/s) DC bias. By changing the bias on the gate, the surface potential could be varied either to accumulate carriers on the surface or to deplete them. Clear modulation from accumulation to depletion was observed. The voltage was swept from +4V (accumulation) to -1V (depletion). On further sweeping the voltage to -6V, a deep depletion region was observed. The deep depletion feature with no inversion capacitance is typical for wide-bandgap semiconductor MIS or MOS structures, because of the slow generation rate of the minority carrier at room temperature [20, 23]. Using the relation, $C_{ox} = \epsilon_0 \epsilon_{ox} A / T_{ox}$, (where ϵ_0 is the permittivity in a vacuum, C_{ox} is the oxide capacitance, A is the cross-

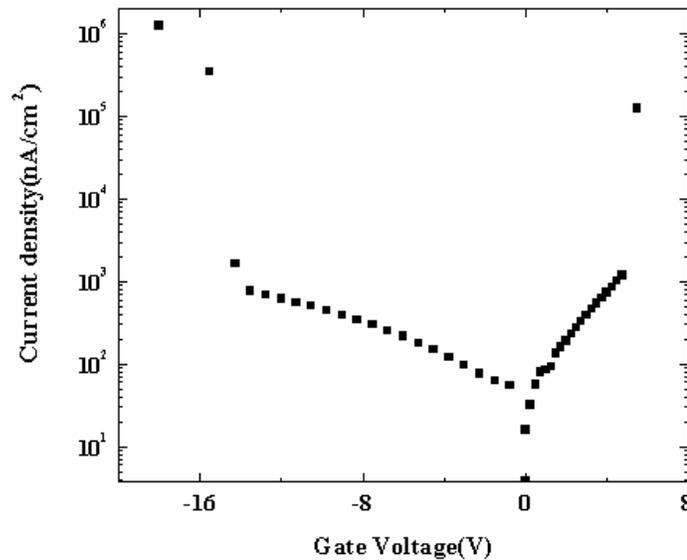


Figure 2-4. Typical current-voltage characteristics of a 100 μm diameter $\text{Sc}_2\text{O}_3/\text{GaN}$ diode

sectional area of oxide, and T_{ox} is the oxide thickness), the dielectric constant of the oxide, ϵ_{ox} , was calculated to be 14.2, a value that is in agreement with the tabulated value for Sc_2O_3 (14.5). From our preliminary results, the flat-band voltage shift is indeed considerably reduced.

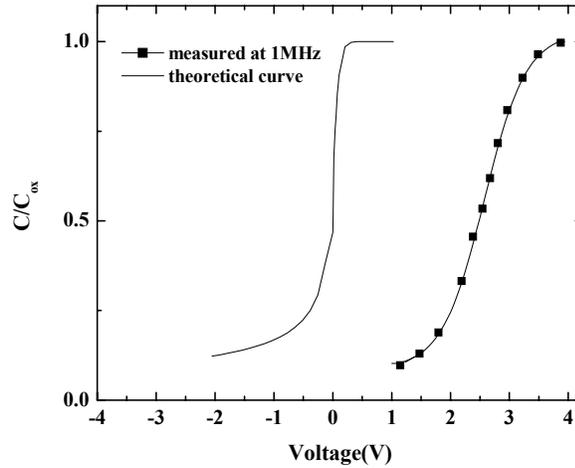


Figure 2-5. Room temperature C-V characteristics of a 100 μm diameter $\text{Sc}_2\text{O}_3/\text{GaN}$ diode measured at 1 MHz and at a sweep rate of 30 mV/s.

The interface state density was calculated using the Terman method [22, 23]. In this method, capacitance is measured as a function of gate bias at high enough frequency such that interface traps do not respond. Although interface traps do not follow the ac gate voltage in a high-frequency measurement, they do follow very slow changes in gate bias as the MOS capacitor is swept from accumulation to depletion. The doping density was calculated to be $5 \times 10^{15} \text{ cm}^{-3}$ from the slope of $1/C^2$ vs. gate bias curve. Using this doping density and closed-form approximation of the high frequency capacitance, the theoretical C-V curve was obtained (as discussed earlier, in the section dealing with Interface state density extraction using Terman Method) [22, 23]. The plot of D_{it} vs. $E_c - E_t$ is shown in Figure 2-6. Interface state density determined from this method is $5 \times 10^{11} / \text{eV} \cdot \text{cm}^2$ at $E_c - E_t = 0.2 \text{ eV}$. The Terman method provided a rough evaluation of the $\text{Sc}_2\text{O}_3/\text{GaN}$ interface trap density, and in general, underestimate of the trap density is expected [20]. AC conductance measurements were also conducted at 300 $^\circ\text{C}$ and an interface state density of $1.11 \times 10^{12} / \text{eV} \cdot \text{cm}^2$ at $E_c - E_t = 0.42 \text{ eV}$ was obtained (Figure 2-6)

[22, 24]. Though the Terman method underestimates interface state density, its value is much more reasonable near the conduction-band edge.

The C-V measurement under UV illumination (Figure 2-7) showed the presence of interface states between mid-gap and the valance-band edge. The voltage was swept from +6V to -4V and was held constant at -4V under UV illumination for 100 seconds. Then the voltage was swept back from -4V to +6V (without light). A sweep rate of 0.05V/s and a sweep frequency of 10 kHz were used. The increase in capacitance to a saturation value was observed due to the generation of minority carriers (holes) by UV light, but capacitance fell when UV illumination was removed. This might be explained by the presence of hole traps between the mid-gap and the valance-band edge. The capacitance value fell as soon as light was removed since the number of holes present at the semiconductor surface decreased because of hole capture by these traps. On the reverse sweep, for any given change in capacitance value to be achieved, the hole traps must be emptied in addition to changing the surface capacitance. Therefore, a larger decrease in bias was expected, and this resulted in “stretching” of the C-V curve, (Figure 2-7), during the reverse sweep.

Measurements performed at high temperature showed the presence of slow states. Slow states were buried deep in conduction-band and did not empty or fill at low temperatures. The time constant for electron emission is given by

$$\tau_e = (\sigma_n \bar{v} M_c)^{-1} \exp\left(\frac{E_T}{kT}\right), \quad (2-11)$$

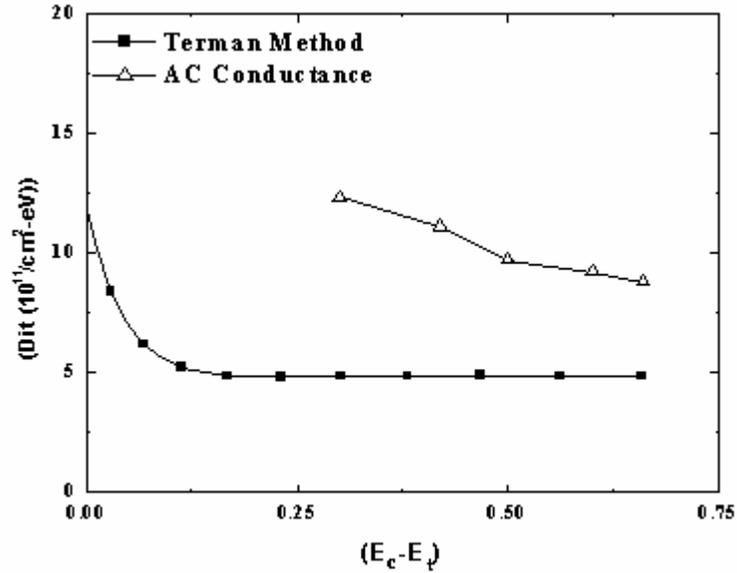


Figure 2-6. Interface trap-level distribution close to the GaN conductance band on n-type GaN MOS structures measured by the Terman method and by the conductance technique (300 °C)

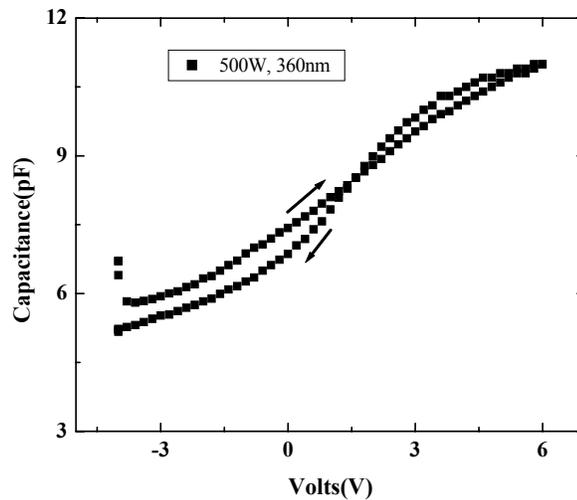


Figure 2-7. C-V characteristics of a typical diode measured at 10 KHz under UV illumination. Voltage was swept from accumulation to depletion, and kept constant for some time. Meanwhile light was not shined while voltage was swept back to accumulation

where E_T is the interface trap energy level measured from the band edge, σ_n is the capture cross section for electrons, \bar{v} is the thermal velocity of the electrons, and M_c is the

effective conduction-band density of states [22, 25]. These states could not fill and empty on changing DC bias and did not contribute to capacitance in any manner at the room temperature and high-frequency measurement. However, at higher temperature, these states contributed a non-equilibrium capacitance, since their long emission times were reduced to a moderate value. However, the emission times were not low enough to reach the equilibrium capacitance value. These interface traps could not emit electrons rapidly enough to maintain equilibrium when the gate bias was swept from accumulation toward inversion in the n-type semiconductor. During the forward sweep, insufficient electrons were emitted from interface traps. The charge on the metal has to be balanced at all times by a sum of opposite charges on the semiconductor and the interface. Since the interface traps did not emit carriers fast enough, the charges on the semiconductor must decrease. As a result, the capacitance value dropped below its steady-state value when gate bias was swept from accumulation toward depletion.

During the reverse sweep, hysteresis occurred, because interface traps continued to emit carriers during the forward sweep, so the effective potential seen by the semiconductor surface was higher (due to absence of -ve trapped charge), leading to an effective flat band shift in the C-V curve (Figure 2-8). At a certain applied bias (during reverse sweep), because of the absence of trapped negative charge, the potential experienced by the semiconductor surface was higher than its steady state value, which explained the higher semiconductor capacitance observed during the reverse sweep. The upper limit on time constants of the interface states that responded to high frequency C-V measurements was around 500 ms (20s/V times kT) [25]. From conductance-voltage measurements (at 300°C), the time constant of traps 0.4 eV below the conduction-band

edge was found to be around 0.5 ms. We assume that traps with a time constant of 1 s at 300 °C are contributing a non-equilibrium capacitance. Their location below the conduction-band edge at 0.73 eV was determined using the above formula. Though we could not pinpoint the exact location of such traps, this provided us a rough idea of where the traps might occur.

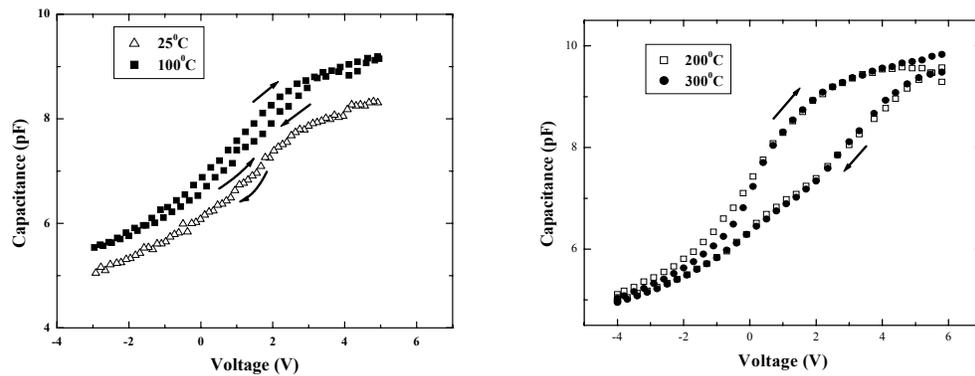


Figure 2-8. C-V measurement performed at 1MHz for different temperatures

Summary

Scandium oxide was deposited on GaN and electrically characterized. The interface state density was calculated using the Terman and AC conductance methods. Low leakage current showed scandium oxide to be an excellent candidate as the gate dielectric for FETs and HEMTs. UV illuminating measurements indicated the presence of hole traps. High temperature measurements suggested presence of slow states buried in band gap at the interface.

CHAPTER 3
ALGAN/GAN MOSHEMT, SURFACE PASSIVATION, LIQUID SENSOR AND W-
BASED SCHOTTKY METAL CONTACT ON GAN

Introduction

AlGaIn/GaN high electron mobility transistors (HEMTs) show great promise for applications such as high frequency wireless base stations and broad-band links, commercial and military radar and satellite communications [34, 52, 87-91]. One problem commonly observed in these devices is the so-called “current collapse” (as mentioned before) in which the application of a high drain-source voltage leads to a decrease of the drain current and increase in the knee voltage [34, 57, 60]. This phenomenon can also be observed by a current dispersion between DC and pulsed test conditions or a degraded rf output power. The use of dielectrics to produce metal-oxide-semiconductor (MOS) or metal-insulator-semiconductor (MIS) gate structures has shown marked improvements in reducing gate leakage [16, 35-56]. Simin *et. al.* have shown that the gate leakage of a MOSHEMT was approximately four orders of magnitude lower at 300 °C than that of conventional HEMTs [43]. Dielectrics are also capable of effective passivation of the surface states that are generally the major cause of the current collapse problem. It is obviously attractive if the same dielectric can be used both as a gate insulator and as the surface passivation layer.

The most commonly used dielectrics are SiO₂ and SiN_x. Sc₂O₃ or MgO deposited by Molecular Beam Epitaxy produce significant improvement over the conventional dielectrics. Sc₂O₃ exists in the bixbyite structure, has a bandgap of 6.3 eV and dielectric

constant of 14. In spite of the large lattice mismatch to GaN, 9.2%, the presence of a single crystal oxide at the oxide/semiconductor interface has been indicated by in-situ RHEED analysis and ex-situ XRD [21, 63, 64, 68-69].

AlGaIn/GaN high electron mobility transistors (HEMTs) have shown great promise for broadband wireless communication systems and advanced radar [10, 34, 57, 64, 70–79]. More recently these same structures have demonstrated the ability to perform as combustion gas sensors, strain sensors and also chemical detectors [80–86]. In most cases, the application of some external change in surface conditions changes the piezoelectric-induced carrier density in the channel of the HEMT, which in turn alters the drain–source or gate current. Ambacher and co-workers [80–86] have shown the strong sensitivity of AlGaIn/GaN heterostructures to ions, polar liquids, hydrogen gas and even biological materials. In particular they have shown that it is possible to distinguish liquid with different polarities. The sensitivity of ungated AlGaIn/GaN heterostructures to different polar liquids will be discussed in this chapter.

There is great current interest in developing schottky and ohmic contacts for n-GaN with improved thermal stability over the existing common metallurgy schemes (e.g. Ti/Al/Pt/Au for Ohmic, Pt/Au and Ni/Au for Schottky) [90, 182-209] for rectifying contacts. W based (W, WSi_x) [192-195, 208] metallurgy shows some promise of improved thermal characteristics, while for Ohmic contacts Ti/Al/Mo/Au and V/Al/Pt/Au show excellent stability at elevated temperatures. Clearly it is worth understanding how the parameters such as surface pre-cleaning and deposition conditions affect the electrical properties of these newer contact metallurgies. In particular, W-based schemes have been used for both rectifying (W/Ti/Au; WSi_x/Ti/Au) [192-195, 208] and ohmic (Ti/Al/Pt/

W/Ti/Au) [209] contacts on GaN rectifier and high electron mobility transition structures. Since sputtering is typically used for these contacts, there is a need to minimize the ion-induced damage for the GaN surface through optimization of the deposition rate and incident ion energy.

A discussion on $\text{Sc}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS-HEMT is followed by the effect of surface passivation on AlGaIn/GaN HEMTs. SiN_x , MgO and Sc_2O_3 passivation layers on AlGaIn/GaN HEMTs with different layer structures (GaN vs AlGaIn cap layer) is discussed along with the long-term (5 month) stability of the MgO and Sc_2O_3 passivation. In the second part DC and power characteristics of AlGaIn/GaN MOS-HEMTs and conventional metal-gate HEMTs employing Sc_2O_3 as the gate dielectric or surface passivation layer is discussed. The last two sections would discuss the use of AlGaIn/GaN HEMTs as fluid sensor and W based Schottky contacts on GaN.

AlGaIn/GaN MOSHEMT

Device Physics

Piezoelectric charges are induced at the interface due to lattice mismatch between AlGaIn and GaN layers. Additional charges are also produced by spontaneous polarization at the interface [26]. Figure 3-1 shows the conduction-band edge for HEMT structure with and without polarization fields, between AlGaIn-GaN interface. A net positive charge is thus produced at the AlGaIn/GaN interface. Electrons are attracted by this positive charge and remain confined in the triangular well (Figure 3-2) resulting in a 2 DEG. Hence charged carriers are free to flow only in a two-dimensional plane parallel to the AlGaIn/GaN interface.

When source and drain metallization contact to the 2D channel, current can flow from drain to source as shown in Figure. 3-2. This forms the basis of a depletion mode

device, which is normally on. The device can be pinched off ($I_{DS} \approx 0$) by applying a negative voltage on the gate and the electrons in 2 DEG are pushed out of the triangular well due to the negative gate bias.

Usually a thin undoped AlGaIn layer is inserted between highly doped AlGaIn layer and GaN layer to prevent any charged donor atoms (dopant atoms like Si^+) near the 2 DEG. Any fixed positive charged atoms near electron gas can scatter the electrons and reduce their mobility.

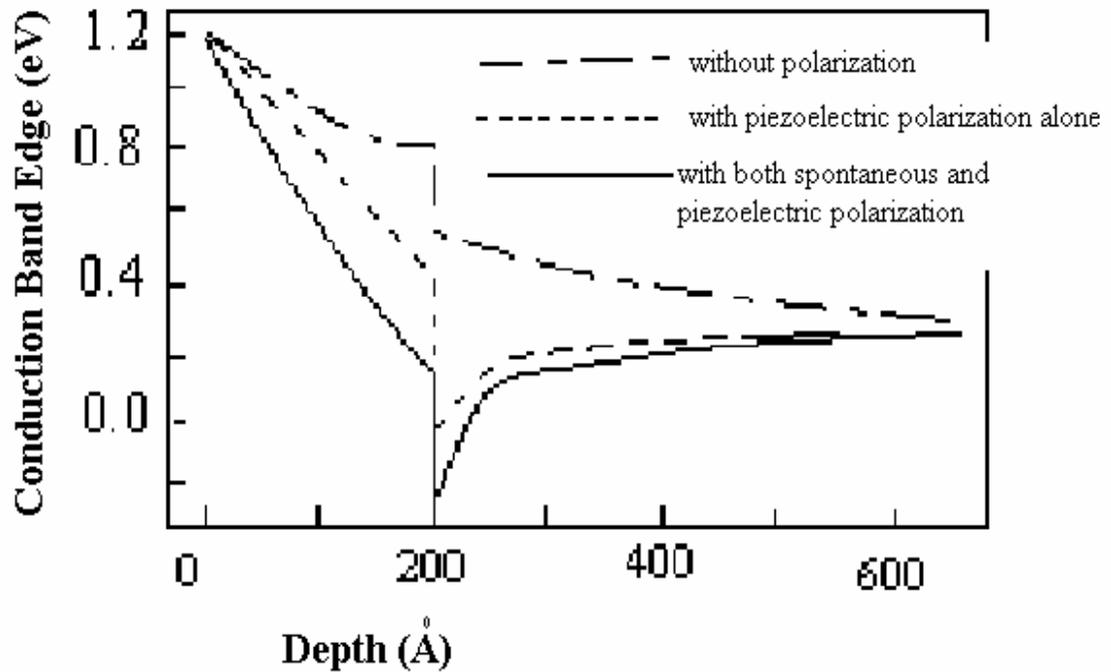


Figure 3-1. Conduction-band edge for the HEMT structure for $V_G = 0$

Effect of Surface States

In spite of excellent I-V characteristics and record high output power densities at microwave frequencies being achieved [27], nitride HEMTs still suffer from the current collapse during high frequency operations. Drain current collapse occurs due to a second virtual gate locating in the gate drain access region and increasing the device resistance

(Figure 3-5). When large bias voltages are applied on devices (as during microwave power measurement), surface states in the vicinity of the gate trap electrons, thus acting as negatively charged virtual gate.

Spontaneous and piezoelectric polarization effects lead to charge sheets of opposite polarity at the top and the bottom surfaces of the AlGa_xN_{1-x} layer in AlGa_xN_{1-x}/Ga_{1-x}N_x heterostructure [28, 29]. It has been shown that a positive sheet charge at free AlGa_xN_{1-x} surface must exist along with polarization dipole for 2DEG in the Ga_{1-x}N_x channel. Surface

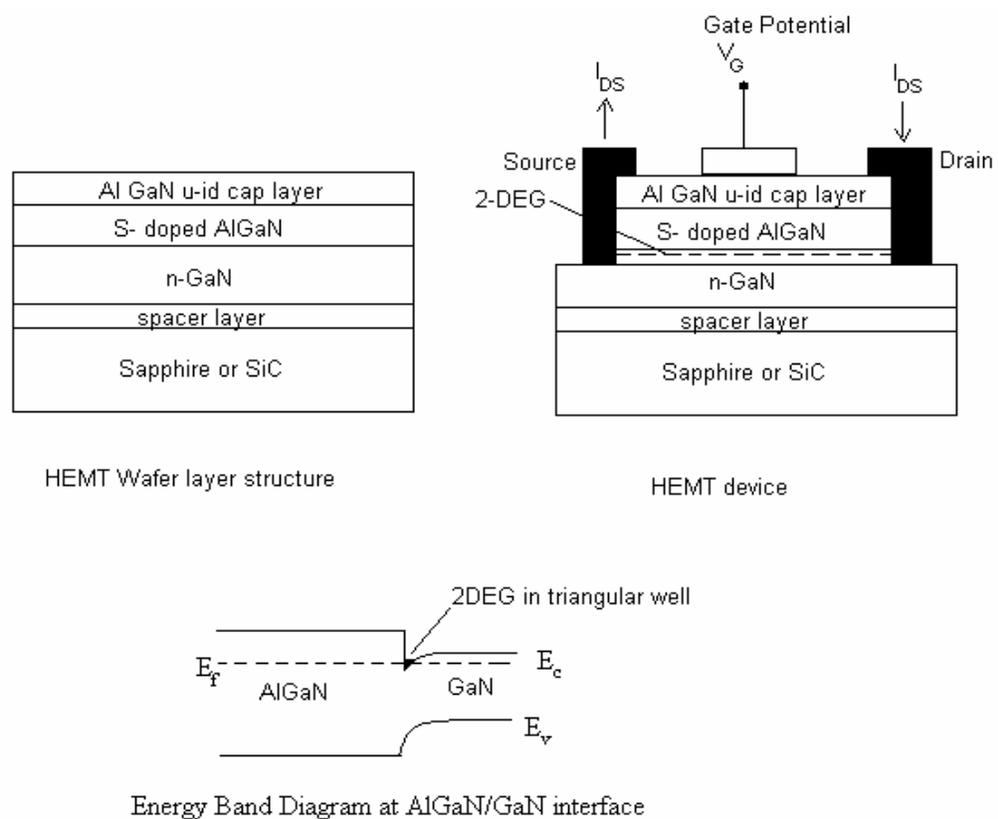


Figure 3-2. The HEMT structure, HEMT device and 2 DEG at AlGa_xN/GaN interface

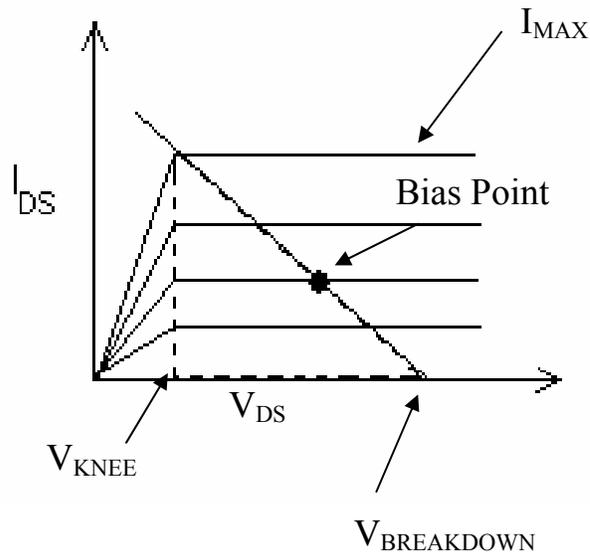


Figure 3-3. Ideal I-V characteristics showing load line drawn to maximize the area of the power triangle shown by dotted lines

donor states can give rise to such a positive charge [30-32]. This positive charge is not enough to completely neutralize the AlGa_N polarization, resulting in a depletion of 2 DEG proportional to the charge imbalance on the surface. If there exist a negative charge on the AlGa_N surface, the surface potential will become more negative. This depletes the channel of electrons and adds an extension of gate depletion region (Figure 3-4) [33].

Figure 3-3 shows ideal (I-V) characteristics of an ideal HEMT. When a HEMT is operated as an amplifier, the maximum output power is given by $P = (\Delta I \times \Delta V) / 8$, where, ΔI is the maximum current swing and ΔV is the maximum voltage swing, given by $(V_{\text{BREAKDOWN}} - V_{\text{KNEE}})$. Experiments show that the observed output power measured at frequencies of 14-18 GHz is well below the calculated one using equation above. The

output power reduction is due to decrease of drain current and increase of knee voltage, which is caused by presence of traps in the device structure [33].

During RF measurements, the voltage is swung to sufficiently large bias along the load line, to drive the device to the limits of I_{MAX} and $V_{BREAKDOWN}$. Associated with every point on the I-V plane, there exist certain amounts of trapped surface charges and hence a value of V_{VG} (voltage at virtual gate), established as a result of the bias applied to the device. The virtual gate is in series with the main gate (Figure 3-5), thus the output current is a function of the potential on the main gate V_G and the potential on the virtual gate, V_{VG} [33]. Due to large time constant associated with the charging and discharging of the traps, V_{VG} cannot change as rapidly as the applied bias swing. This results in a difference between the actual gate bias being applied to the 2 DEG channel and the V_{VG} , thus the drain current decays. It must be noted that there is a time constant associated with establishing the steady state value of V_{VG} associated with the quiescent bias point. Hence any measurement of the frequency dependence of the output drain current must be made after steady state is reached [33].

Gate Oxides

Depositing oxide or an insulator layer on top of AlGaN layer would quench the surface traps. This would not only help to decrease the drain current dispersion but also help to decrease gate leakage current. Though AlGaN/GaN material system has large band gap, the performance at higher temperature degrades due to thermionic emission over Schottky barrier at elevated temperatures. Many insulators, such as Ga_2O_3 (Gd_2O_3), AlN, SiO_2 , and Si_3N_4 , have been used to passivate AlGaN/GaN HEMTs [10-16, 34]. With the proper passivation, the extent of current collapse is much smaller and the surface passivation layer prevents the formation of a virtual gate, or pacifies the surface states.

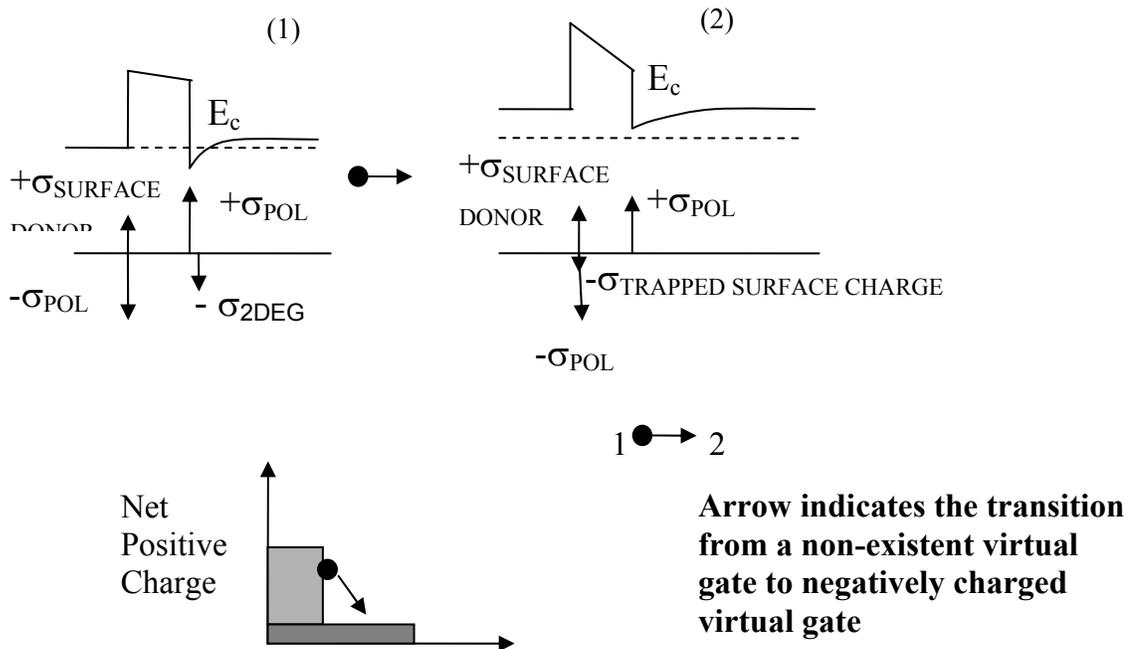


Figure 3-4. Band diagram of AlGaIn/GaN heterostructure showing the transition from a non-existent virtual gate to the negatively charged virtual gate. The surface negative charge reduces the effective donor density leading to an extension of the depletion region as shown

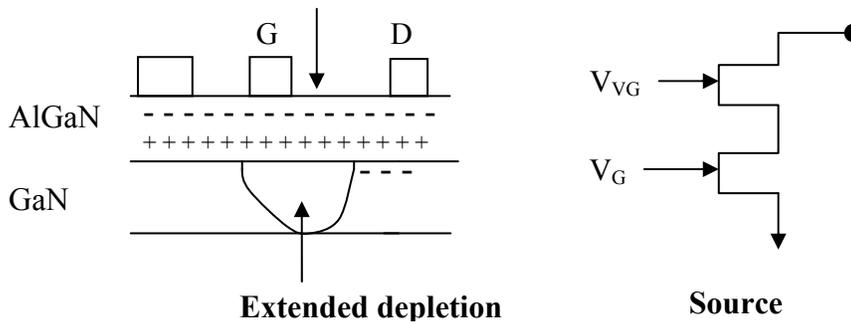


Figure 3-5. Model of the device showing the location of the virtual gate and schematic representation of the device including the virtual gate

It was found that Scandium Oxide (Sc_2O_3) and Magnesium Oxide (MgO) are promising passivation dielectrics for AlGaIn/GaN HEMTs [93, 94, 208, 210]. MOS structures grown on GaN were used to study the effectiveness of the passivation by

obtaining interface state density. Besides passivating the surface, the oxide also reduces gate leakage current, which is exponentially dependent on Schottky barrier height by

$$J_0 = A^* T^2 \exp\left(\frac{-\phi_{bn}}{kT}\right), \quad (3-1)$$

where J_0 is the dark current density, A^* is the effective Richardson constant, T is the Temperature in Kelvin, ϕ_{bn} is the effective barrier height and k is the Boltzmann constant. Schottky barrier height is enhanced by inclusion of an insulator between gate and the semiconductor. Very low leakage currents were obtained for MOS diodes employing Scandium Oxide (Sc_2O_3) and Magnesium Oxide (MgO) as gate dielectrics [210, 211]

Epitaxial Growth and Fabrication of AlGaN/GaN MOSHEMT

The AlGaN/GaN HEMT structures were grown with a Metal Organic Chemical Vapor Deposition (MOCVD) on c-plane Al_2O_3 substrates. The layer structures consisted of a 3 μm thick GaN buffer, 3 nm unintentionally doped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layer, 25 nm thick n-type ($5 \times 10^{18} \text{ cm}^{-3}$) $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ donor layer and 5 nm thick, undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ cap layer. The device fabrication started with device isolation. A based Cl_2/Ar discharge in an Inductively Coupled Plasma (ICP) system was used to define the mesa. Ohmic metallization consisted of e-beam deposited Ti/Al/Pt/Au (200 Å /700 Å /400 Å /1000 Å) subsequently annealed at 850 °C for 30 sec under a N_2 ambient. The wafer was divided in two pieces and 400 Å of Sc_2O_3 grown on one piece by rf plasma-accelerated MBE at 300 °C using elemental Sc and O_2 derived from a 13.56 MHz plasma source[62]. The ICP system was employed to open the Sc_2O_3 window for final metal deposition. The HEMT and MOSHEMT characteristics were measured in both DC mode and pulsed mode using an Agilent 4156 C parameter analyzer for DC mode and a pulse generator, DC power supply and oscilloscope for the pulsed measurements.

DC Characteristics of Sc₂O₃/AlGa_N/Ga_N MOSHEMT

Figure 3-6 shows the gate voltage dependence of the drain current for the identical geometry HEMTs and MOSHEMTs. The drain current is ~ 40 % higher for the MOS – HEMTs reaching a maximum value of over 0.8 A/mm, and the threshold voltage is higher because of the larger gate to channel separation, as reported previously for Si₃N₄ (10) and SiO₂ (2) gate devices. The experimental threshold voltage for both HEMTs and MOS – HEMTs were in good agreement with the values obtained from the relation [55]

$$V_{Th} = \frac{en_s}{C_b}, \quad (3-2)$$

where e is the electronic charge, n_s is the sheet electron density and C_b is the total unit area capacitance of the barrier layer and dielectric. This agreement is a good indicator of low surface state density at the Sc₂O₃/AlGa_N interface as discussed elsewhere [62].

The MOSHEMT output curves are shown in Figure 3-7 for a measurement temperature of 25 °C. The device can be modulated to + 6 V of gate Voltage. The maximum saturation source-drain current is about 860 mA/mm at $V_{DS} = 6$ V and the maximum transconductance was ~ 125 mS/mm. These results are comparable to MOS gate HEMTs reported in the literature [52, 56, 65]. There is no indication of negative resistance effects and thus self-heating does not appear to be a problem under the biasing conditions employed here. All of these results suggest that the Sc₂O₃ is an effective gate dielectric for AlGa_N/Ga_N transistors.

To investigate the effectiveness of the Sc₂O₃ for the surface passivation in these structures, we employed gate lag measurements. Figure 3-8 shows the drain current response of a Sc₂O₃/AlGa_N/Ga_N MOS – HEMT to a pulsed gate – source voltage for both DC and pulsed measurements. In this figure, V_G was pulsed from -7 to -0 at

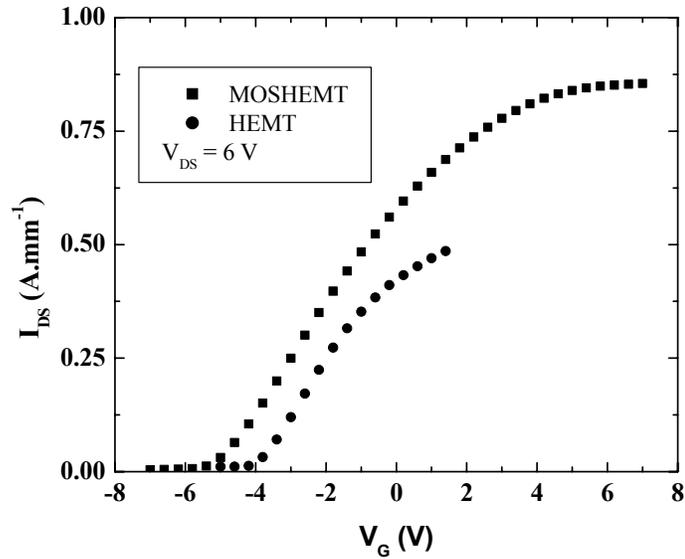


Figure 3-6. Comparison of drain current for MOSHEMT and HEMT as a function of gate voltage

0.1 MHz with a 10% duty cycle. There is less than 10% decrease in drain source current. This is our typical Sc_2O_3 passivation results [68, 69] as compared to 50% decrease for unpassivated HEMTs. This is clear evidence that the Sc_2O_3 retains its effectiveness in mitigating the surface state – induced current collapse. This is inferred by

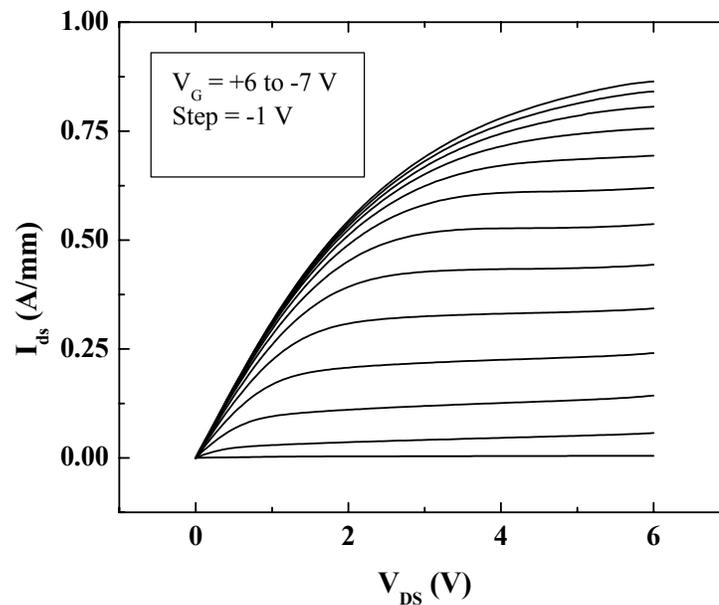


Figure 3-7. Drain I-V characteristics of a typical AlGaIn/GaN MOSHEMT

the data of Figure 3-9, which shows the drain – source current when the gate voltage is switched from -7 V to the value shown on the x-axis with V_{DS} held at a low enough value (6 V) to avoid any complications from device self – heating. Once again the fact that there is around less than 10% decrease in I_{DS} under pulsed conditions relative to DC conditions shows that the Sc_2O_3 minimizes the effect of surface traps in the gate – drain region that otherwise would create a depletion region and reduce the drain – source current.

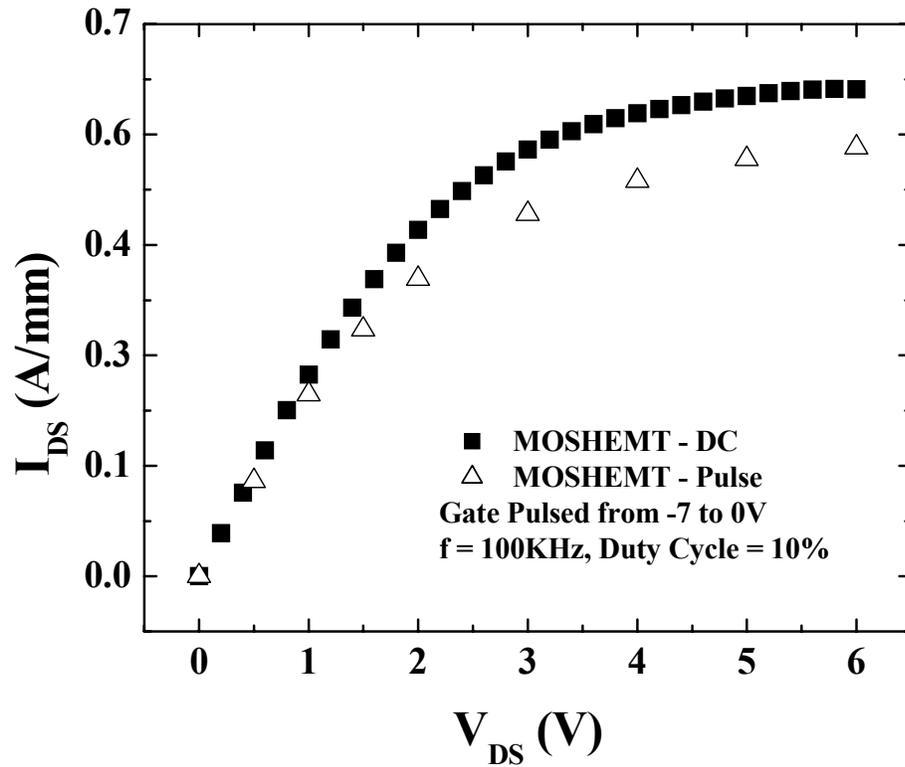


Figure 3-8. Gate lag measurement of a AlGa_N/Ga_N MOSHEMT with gate voltage pulsed from -7 V to 0 V

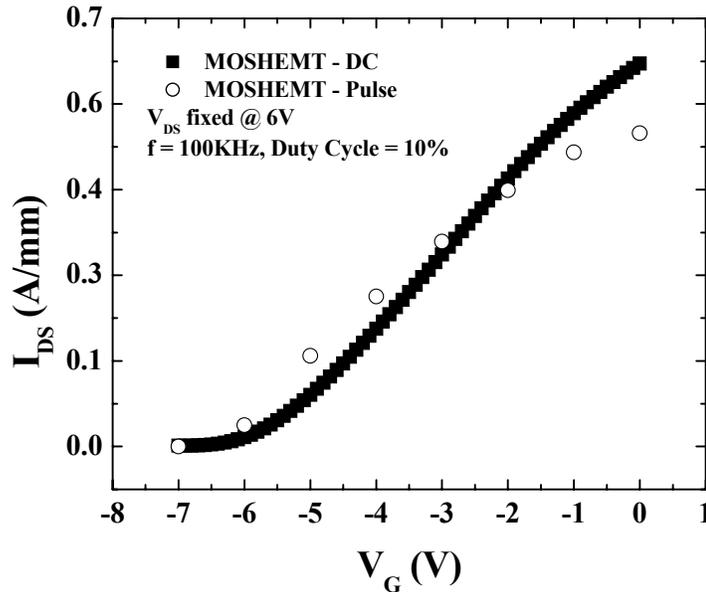


Figure 3-9. Gate lag measurement of a AlGaIn/GaN MOSHEMT with gate voltage pulsed from -7 V to the value shown on the x-axis

Surface Passivation

Two different HEMT structures were used in our studies as shown in Figure 3-10. The first employed an undoped GaN-cap layer on top of an undoped $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ layer. Both Al_2O_3 and SiC substrates were used. The second type of HEMT employed an undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ -cap layer on top of a doped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ donor layer. Around 100 \AA thick dielectric layers, MgO, Sc_2O_3 , or SiN_x , were deposited on completed devices using either Molecular Beam Epitaxy (MBE) for the oxides or PECVD for the SiN_x , with deposition temperatures of $100 \text{ }^\circ\text{C}$ in the oxide case and $250 \text{ }^\circ\text{C}$ for the SiN_x case. The SiN_x films were deposited with either $\text{SiH}_4 + \text{NH}_3$ or $\text{SiD}_4 + \text{ND}_3$ to examine the effect of deuterated precursors. The HEMT DC parameters were measured in DC and pulsed mode at $25 \text{ }^\circ\text{C}$, using a parameter analyzer for the DC measurements and pulse generator, DC power supply and oscilloscope for the pulsed measurements. For the gate lag

measurements, the gate voltage V_G was pulsed from -5 V to 0 V at different frequencies with a 10% duty cycle.

Figure 3-11 (a) shows typical gate lag data for $0.5 \times 100 \mu\text{m}^2$ GaN-cap HEMT grown on sapphire substrates. The decrease in drain-source current becomes more pronounced at high frequencies. The degradation in current was less significant when these same structures were grown on SiC substrates. The defect density will be lower in the latter case due to the closer lattice match between GaN and SiC. This suggests that at least some of the surface traps are related to dislocations threading to the surface. The effects of both substrate type and HEMT gate length on the change in drain-source current are shown in Figure 3-11 (b). The shorter the gate length, more pronounced the degradation observed in current due to larger surface area and higher electric field in the channel between gate and drain (the source-to-drain distance was fixed in all devices).

The I_{DS} - V_{DS} characteristics before and after SiN_X passivation using either hydrogenated or deuterated precursors are illustrated in Figure 3-12. The inset shows the complete set of I-V curves for the as-fabricated HEMT and the main figure shows only the uppermost curves for clarity. The I_{DS} increases after passivation with either type of SiN_X , which indicates that the passivation of the semiconductor is improved.

Similarly, the transconductance (g_m) increases after SiN_X deposition, which also suggests a decrease in surface trap density (Figure 3-12 (b)). The unity current gain frequency (f_T) and maximum frequency of oscillation (f_{MAX}) data before and after passivation are shown in Figure 3-13 (b). There is a slight increase in both parameters, in contrast to previous reports [96]. There were no systematic differences between the results of hydrogenated and deuterated precursor SiN_X , even though the latter typically

produce slightly denser films when deposited under the same PECVD conditions. The gate-lag measurement for MgO-passivated HEMTs immediately after MgO deposition and after 5 months aging without bias on the devices under room conditions are shown in Figure 3-14. The I_{DS} increases $\sim 20\%$ upon passivation and there is almost complete mitigation of the degradation in I_{DS} immediately after MgO deposition. However, after 5 months aging, there is a clear difference between the DC and pulsed data, indicating that the MgO passivation has lost some of its effectiveness.

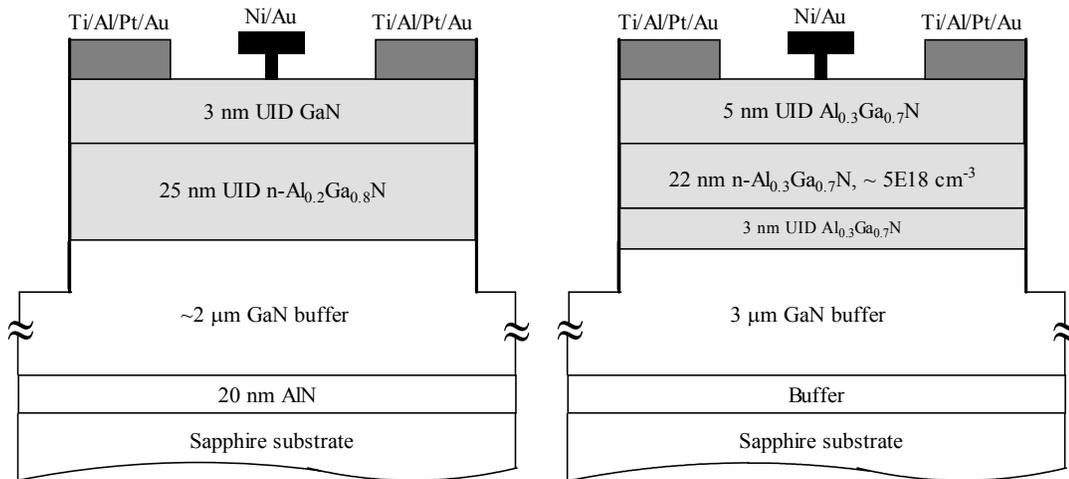


Figure 3-10. Cross-sections of a) GaN-cap b) and AlGaN-cap HEMT structures

Similar data is shown in Figure 3-15 for Sc_2O_3 -passivated HEMTs. In this case, the I_{DS} also increases upon deposition of the oxide and there is also essentially complete mitigation of the degradation in drain-source current.

On the contrary, Sc_2O_3 passivation after 5 months of ageing shows no significant change in the device characteristics. This indicates that Sc_2O_3 provides more stable passivation than that of MgO. We have noticed in separate experiments that the

MgO/GaN interface deteriorates over time. A higher interface state trap densities of GaN MOS diodes were observed, if MgO surface left uncapped for a while before diode metal is deposited. However, if the MgO is immediately covered with the diode gate metal, the lower interface state densities were observed. The MgO degradation may be easily resolved by depositing another dielectric such as SiN_x , since thicker dielectric film will be needed for capacitors or insulated layer between metal layers during the fabrication of power amplifiers or integrated circuits. However, further work is needed to establish the

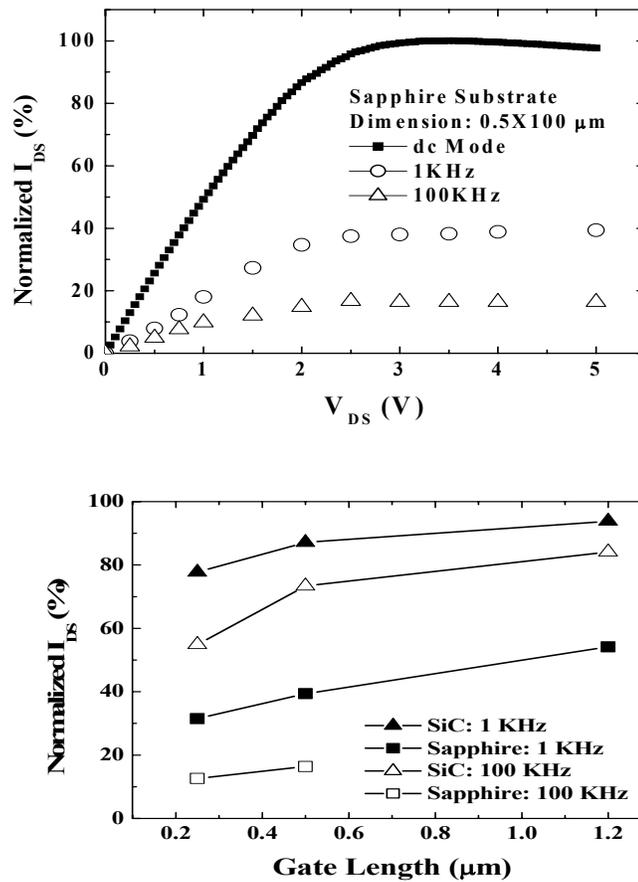


Figure 3-11. Gate lag measurements on unpassivated $0.5 \mu\text{m}$ gate length. a) GaN-cap HEMTs grown on sapphire. b) Normalized I_{DS} as a function of both gate length and substrate type for GaN-cap HEMTs at pulse frequency of 1 KHz and 100 KHz

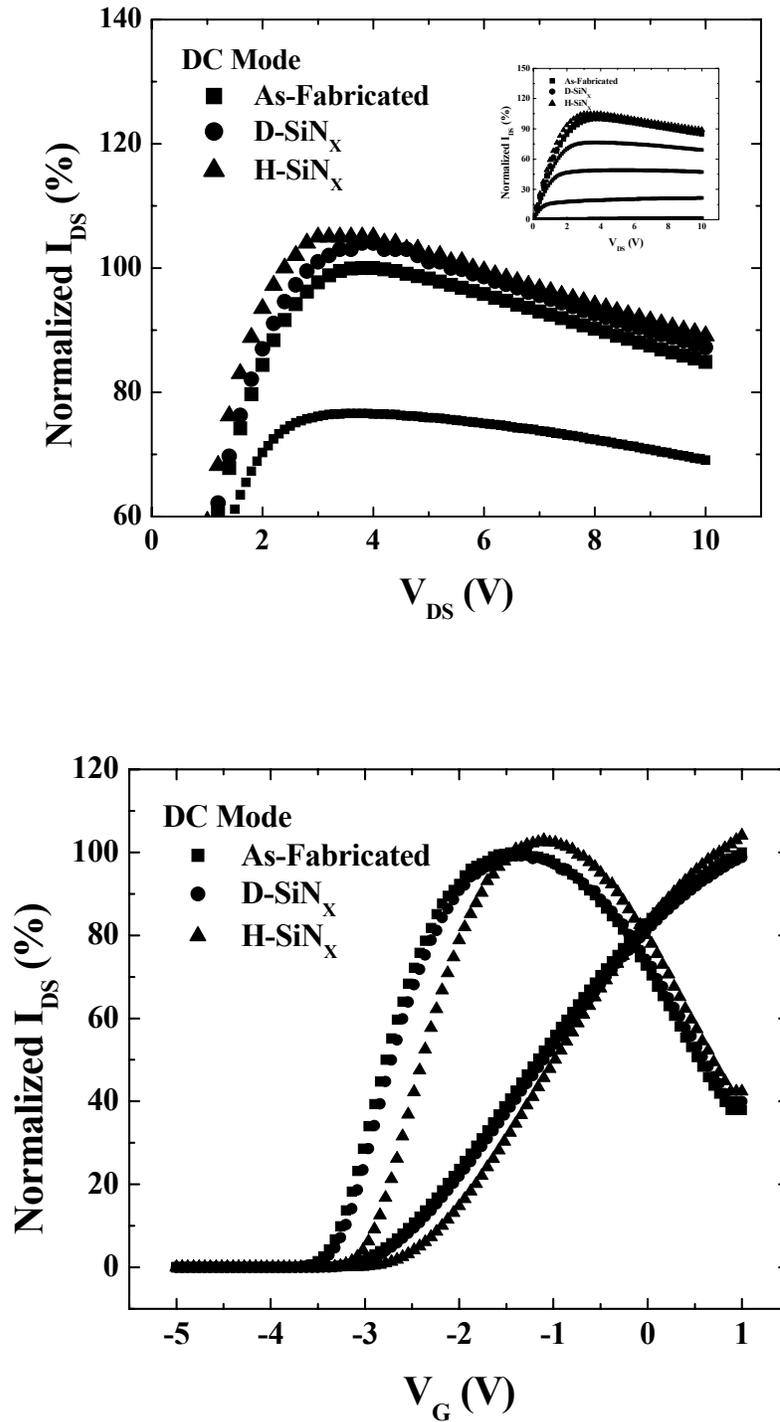


Figure 3-12. GaN-cap HEMTs before and after SiN_x passivation using either hydrogenated or deuterated precursors. a) Normalized I_{DS} versus V_{DS} . b) Normalised I_{DS} versus V_G for $1.2 \times 100 \mu\text{m}^2$

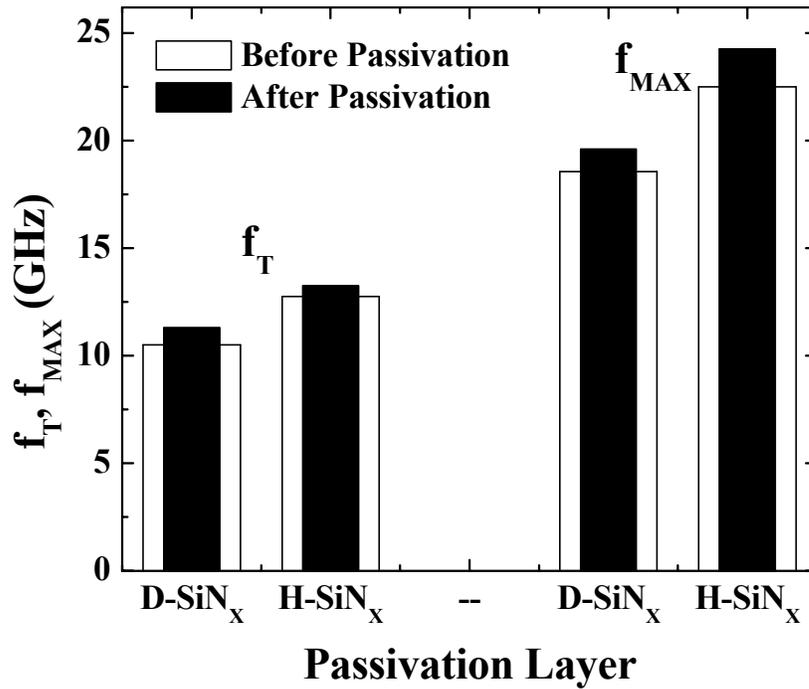
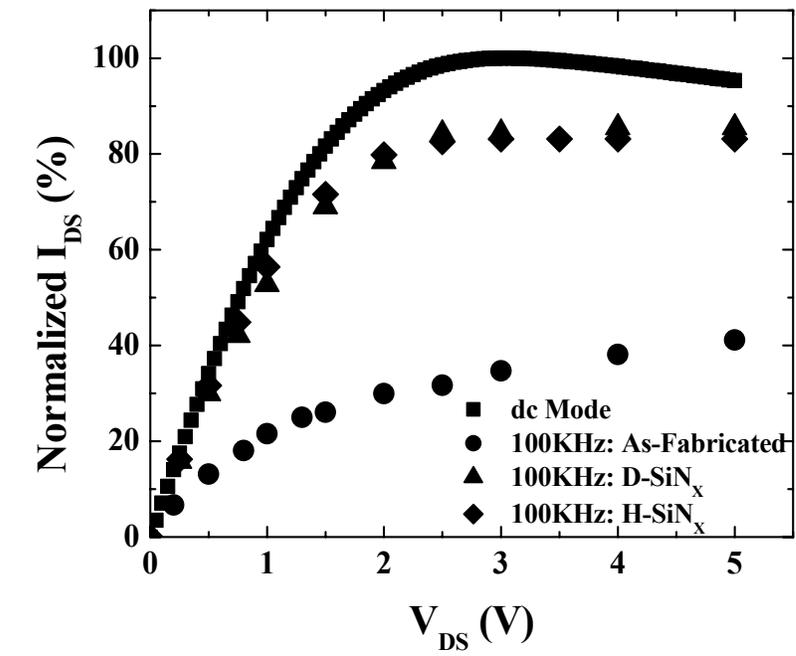


Figure 3-13. SiN_x passivation. A) Gate-lag measurements before and after SiN_x passivation of $1.2 \times 100 \mu\text{m}^2$. b) GaN-cap HEMTs f_T and f_{MAX} before and after

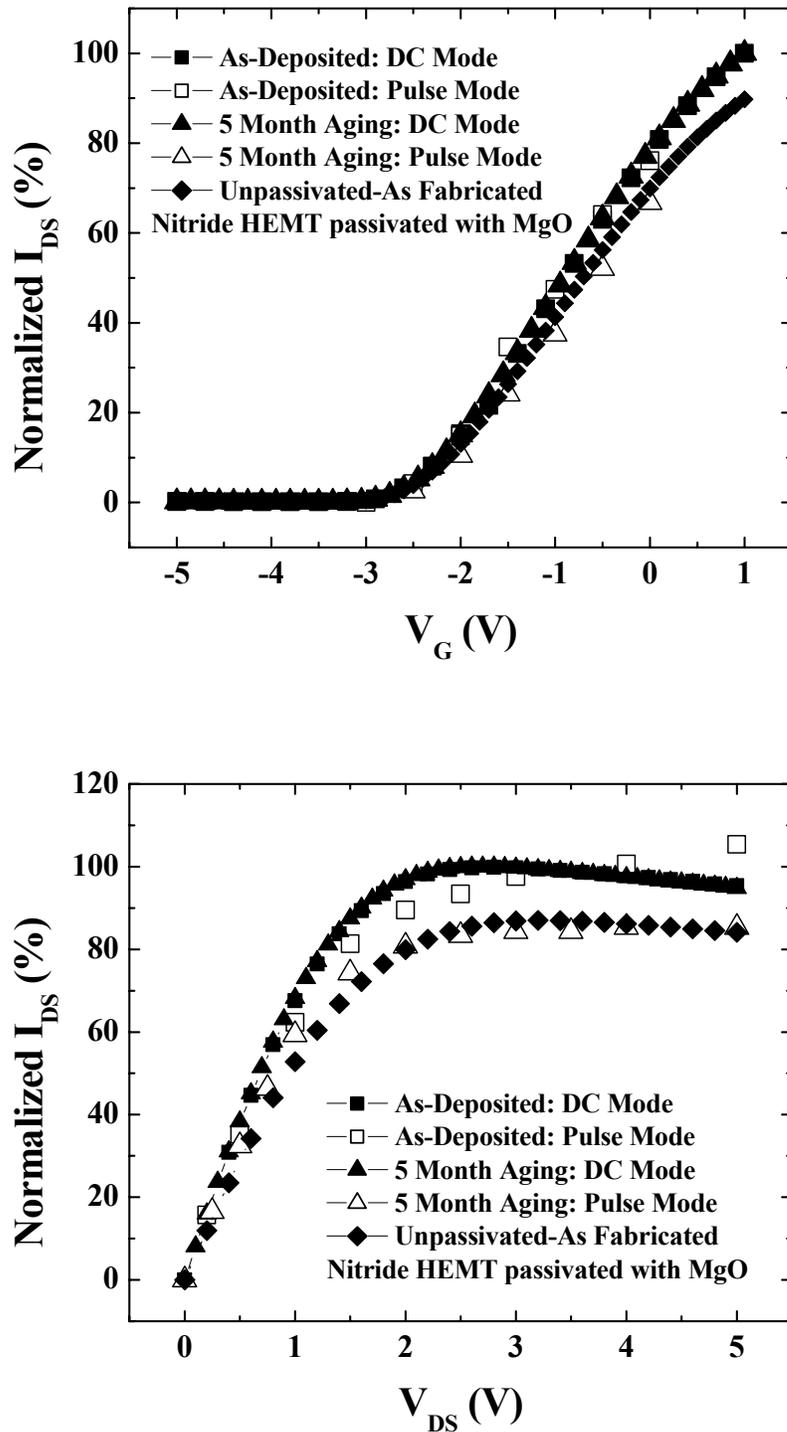


Figure 3-14. Gate lag measurements before and after MgO passivation and following 5 months aging of $1.2 \times 100 \mu\text{m}^2$, GaN-cap HEMTs. At left V_G was switched from -5 to 0 V, while at right it was switched from -5 V to the value shown on the X-axis

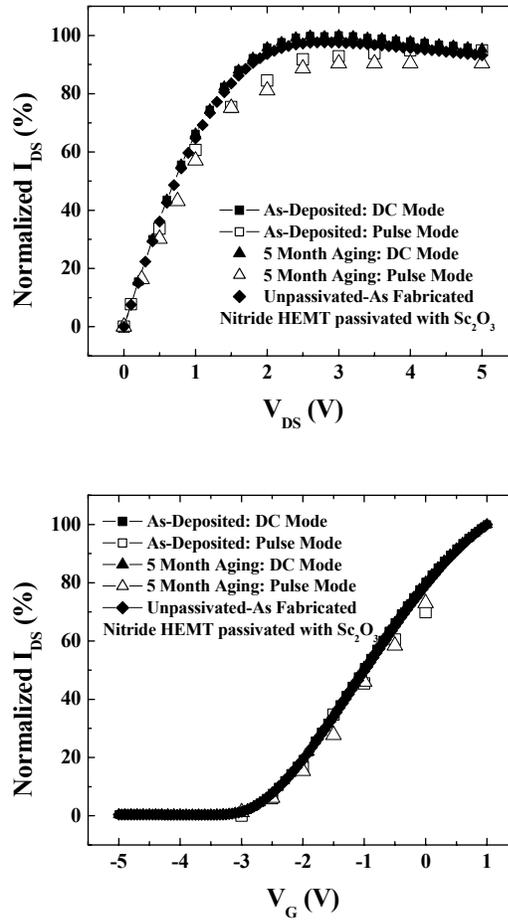


Figure 3-15. Gate lag measurements before and after Sc_2O_3 passivation and following 5 months aging of $1.2 \times 100 \mu m^2$, GaN-cap HEMTs. At left V_G was switched from -5 to 0 V, while at right it was switched from -5 V to the value shown on the X-axis

long-term reliability of Sc_2O_3 and MgO passivation, but the preliminary data with Sc_2O_3 looks very promising.

The cap layer of AlGaIn/GaN HEMT also plays an important role for the passivation. The gate lag data for the HEMT structures with $Al_{0.3}Ga_{0.7}N$ as the top layer as illustrated in Figure 3-10 (b), shows less recovery of drain current as compared to that of GaN capped HMET. Figure 5-7 shows typical gate-lag data from a Sc_2O_3 passivated AlGaIn-cap HEMT. The Sc_2O_3 passivated HEMTs were typically able to restore 80-90% of the drain current loss relative to DC measurement conditions.

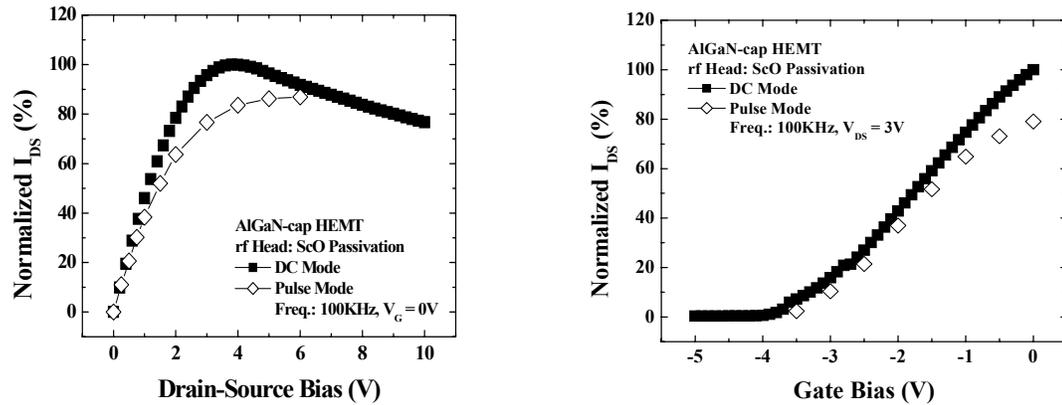


Figure 3-16. Gate lag measurements before and after Sc₂O₃ passivation of $0.5 \times 100 \mu\text{m}^2$, AlGaIn-cap HEMTs. At left V_G was switched from -5 to 0 V, while at right it was switched from -5 V to the value shown on the X-axis

Similar results were obtained for MgO passivation, as shown in Figure 3-17. This may be attributed to the in-situ cleaning procedure prior to deposition of oxides in the MBE chamber is not able to completely remove the native oxide from the AlGaIn surface. The native oxides limit the effectiveness of the resulting passivation and account for the more variable results we observe for the AlGaIn-cap devices.

DC and Power Performance Comparison

SiNx Structure

The HEMT structures consisted of $3 \mu\text{m}$ thick, undoped GaN buffer was followed by a 30 \AA thick, undoped Al_{0.3}Ga_{0.7}N spacer, a 220 \AA thick, Si-doped ($n \sim 5 \times 10^{18} \text{ cm}^{-3}$) Al_{0.3}Ga_{0.7}N donor layer and a 50 \AA thick, undoped Al_{0.3}Ga_{0.7}N cap layer on Al₂O₃. Device isolation was performed by Cl₂/Ar Inductively Coupled Plasma mesa etching. The e-beam evaporated Ni(200 \AA) / Au(2000 \AA) gate metallization was also patterned by lift-off.

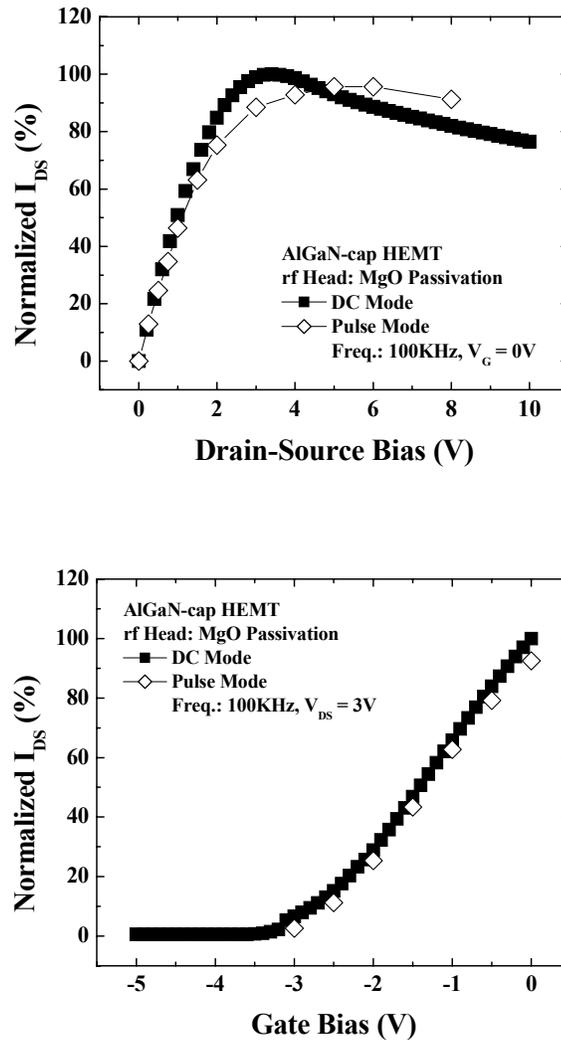


Figure 3-17. Gate lag measurements before and after MgO passivation of $0.5 \times 100 \mu\text{m}^2$, AlGaIn-cap HEMTs. At top V_G was switched from -5 to 0 V, while at bottom

The 1700 \AA thick SiN_x passivation layers were deposited on completed devices using plasma-enhanced chemical vapor deposition in a Unaxis 790 system. The deposition was performed with 13.56 MHz rf power at 40 W, pressure of 800 mTorr with 200 sccm Nitrogen, 600 sccm He, 4 sccm NH_4 , and 167 sccm of 3% Silane in Helium, with a deposition temperature of $300 \text{ }^\circ\text{C}$. The 100 \AA thick Sc_2O_3 or MgO layers were deposited at $100 \text{ }^\circ\text{C}$ using rf plasma-assisted MBE as discussed previously.

MOSHEMT and Passivated HEMT Structures

HEMT layer structures were grown on C-plane Al_2O_3 substrates by Metal Organic Chemical Vapor Deposition (MOCVD) in a rotating disk reactor. The layer structure included an initial 2 μm thick undoped GaN buffer followed by a 35 nm thick unintentionally doped $\text{Al}_{0.28}\text{Ga}_{0.72}\text{N}$ layer. The sheet carrier concentration was $\sim 1 \times 10^{13} \text{ cm}^{-2}$ with a mobility of 980 $\text{cm}^2/\text{V}\cdot\text{s}$ at room temperature. Two different types of experiments were performed. In the first, one of the wafers was divided in half and on one piece 400 Å Sc_2O_3 was deposited as a gate dielectric. Before oxide deposition, the wafer was exposed to ozone for 25 minutes. It was then rinsed in a 1:1 ratio of BOE: H_2O treatment for 1 min followed by in-situ 650 °C cleaning for 10 min. inside the growth chamber. The Sc_2O_3 was deposited by rf plasma-activated MBE at 100 °C. The purpose of this experiment was to compare the performance of the conventional metal-gate HEMTs with the Sc_2O_3 MOS-HEMTs and device fabrication was similar to MOSHEMT device discussed earlier.

In the second experiment, another wafer was fabricated as conventional metal-gate HEMTs by the same process as described previously. In addition, on half of the samples, Sc_2O_3 was deposited as a surface passivation layer at 100 °C. In this case, the pre- Sc_2O_3 -deposition treatment consisted of ozone exposure for 25 min. followed by an in-situ thermal treatment at 300 °C. The purpose of this experiment was to examine the effectiveness of the Sc_2O_3 as a passivation layer. Our preliminary reports previously have shown improved DC and gate lag characteristics after Sc_2O_3 deposition and increased output power [62-64, 68-69].

Device Performance Comparison

Maps of the saturated drain-source current, I_{DSS} , are shown in Figure 3-18 for devices either with or without Sc_2O_3 passivation. The average I_{DSS} increased slightly upon deposition of the Sc_2O_3 from 366 mA/mm in unpassivated devices to 388 mA/mm after Sc_2O_3 deposition. Comparable increases were observed with both SiN_x and MgO passivation. As reported previously, this is consistent with passivation of surface states, which leads to a decrease in surface depletion [34]. The SiN_x produced ~70-75% recovery of the drain-source current during gate lag measurement, while the Sc_2O_3 and MgO were more effective in reducing current dispersion, with 85% and 94% recovery, respectively.

Typical load-pull data for HEMTs before and after SiN_x passivation are shown in Figure 3-19 for a measurement frequency of 4 GHz. In all cases, the drain voltage, V_D , was held at 10 V, while the gate voltage V_G was -2 V. The wafer measurements employed mechanical tuners for matching and there was no harmonic termination under class A operation. The devices were matched for the power testing prior to passivation and were tested under these same conditions after SiN_x deposition. The difference in output power before and after SiN_x passivation is also shown in Figure 3-19 and is < 2 dB in all cases.

Similar data for HEMTs before and after Sc_2O_3 passivation are shown in Figure 3-20. Note the increased power output compared to typical SiN_x -passivated devices. This is consistent with the higher percentage recovery of I_{DS} during the gate lag measurements with Sc_2O_3 passivation. We believe that the Sc_2O_3 process can be better optimized with respect to the pre-deposition cleaning procedure. The SiN_x deposition has the advantage of a high flux of atomic hydrogen radicals that have proven effective in surface cleaning

of other III-V compounds and which can remove native oxide and surface hydrocarbons through formation of volatile reaction products. The Sc_2O_3 passivation has shown

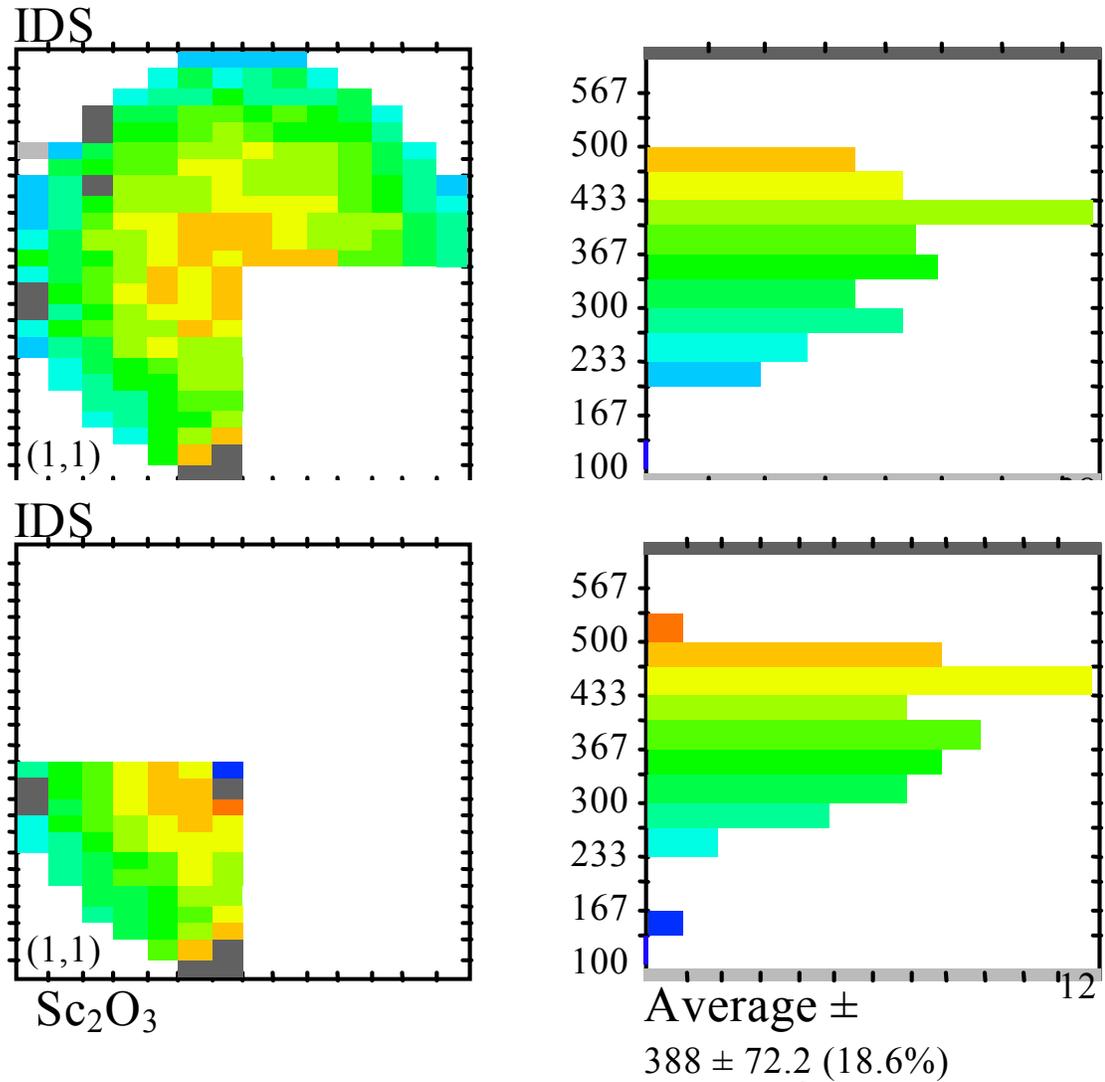


Figure 3-18. Wafer-map measurements of I_{DSS} for $0.5 \times 100 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation. The data is shown in histogram form at right

excellent aging characteristics when measured under DC test conditions, with no change in HEMT performance over a period of > 5 months.

The power measurement data for unpassivated and MgO deposited devices is shown in Figure 3-21. The output power increases are again significantly larger than for

SiN_x passivation of similar devices and the gain remained linear over a wider input power range. A drawback with MgO passivation is that we have observed deterioration

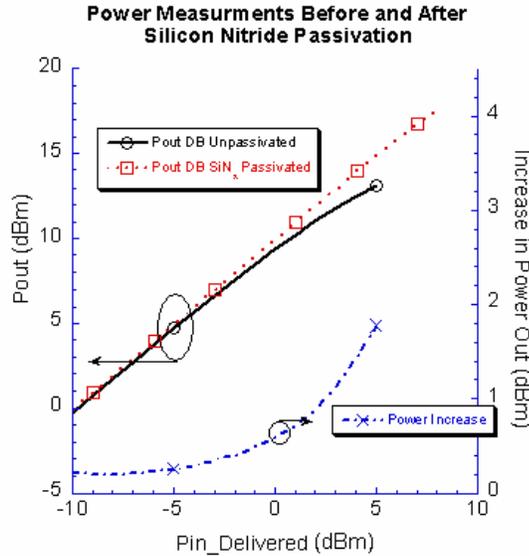


Figure 3-19. Output power characteristics before and after SiN_x passivation of $0.5 \times 100 \mu\text{m}^2$ devices measured at 4 GHz and a bias point of $V_D = 10 \text{ V}$, $V_G = -2 \text{ V}$

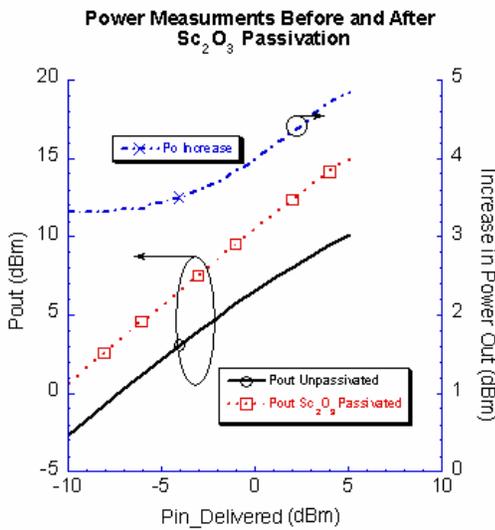


Figure 3-20. Output power characteristics before and after Sc₂O₃ passivation of $0.5 \times 100 \mu\text{m}^2$ devices measured at 4 GHz and a bias point of $V_D = 10 \text{ V}$, $V_G = -2 \text{ V}$

of the MgO over a period of months if left uncapped. The MgO reacts with water vapor in the ambient to form volatile MgOH species and we observe increases in interface state densities in MgO/GaN diodes on which the metal is deposited after a long storage period. By contrast, these changes are not observed in diodes that are immediately metallized after MgO deposition. For the case of using MgO as a passivation layer, we expect it will be necessary to provide an additional encapsulation layer to preserve MgO stability. Since both Sc_2O_3 and MgO are also promising as gate dielectrics for GaN-based devices, one can envision AlGaN/GaN MISFETs that employ these oxides both for gate oxides and for surface passivation. Hu et. al. have used SiN_x in a similar role in GaN-based HFETs [103].

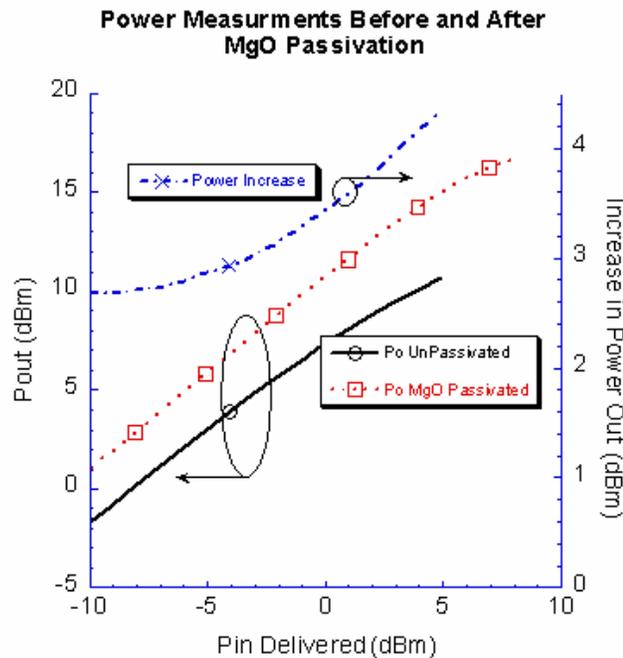


Figure 3-21. Output power characteristics before and after MgO passivation of $0.5 \times 100 \mu\text{m}^2$ devices measured at 4 GHz and a bias point of $V_D = 10 \text{ V}$, $V_G = -2 \text{ V}$

The DC characteristics of all of the devices from room temperature measurements were measured on an Agilent 4156 C parameter analyzer. The on-wafer power measurements were performed on a load-pull system using mechanical tuners for network matching and there was no harmonic termination under class A operation. The passivated devices were matched for the power testing prior to passivation and were tested under these same conditions after Sc₂O₃ deposition.

MOS-HEMT versus HEMT Devices

Figure 3-22 shows the transfer characteristics for both HEMTs and Sc₂O₃ MOS-HEMTs. The threshold voltage of the MOS-HEMTs shifted to more negative values relative to the HEMTs because of the longer gate-to-channel separation with additional Sc₂O₃ under the gate contact. Note that the drain current is increased from ~0.6 A/mm to ~0.75 A/mm. The threshold voltage for the two types of devices was in good agreement with the values expected from the equation 3-2.

The drain I-V characteristics of devices are shown in Figure 3-23. The MOS-HEMTs show a slightly better knee voltage and higher output conductance. The MOS-HEMT clearly showed much better gate modulation to +2 V as compared to that of conventional Schottky gate on the conventional HEMTs. Figure 3-24 shows typical load-pull data for the two types of devices at a measurement frequency of 4 GHz in both cases. The drain voltage was held at 10 V with a gate voltage of -3 V. The MOS-HEMT has higher output power and associated gain over the entire input power range investigated. The power-added efficiency, as illustrated in Figure 3-25, was also significantly improved (~27%) relative to the HEMT (~5%). In the latter case the unpassivated surface leads to severe reductions in output power and power-added efficiency due to the current collapse problem.

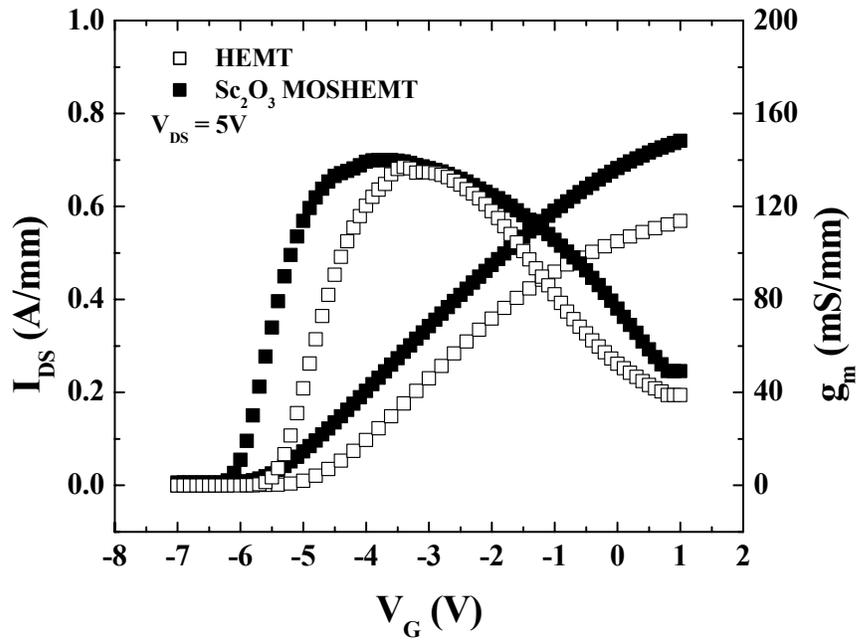


Figure 3-22. Transfer characteristics for MOS-HEMTs and HEMTs fabricated on the same wafer. The drain-source voltage was 5 V

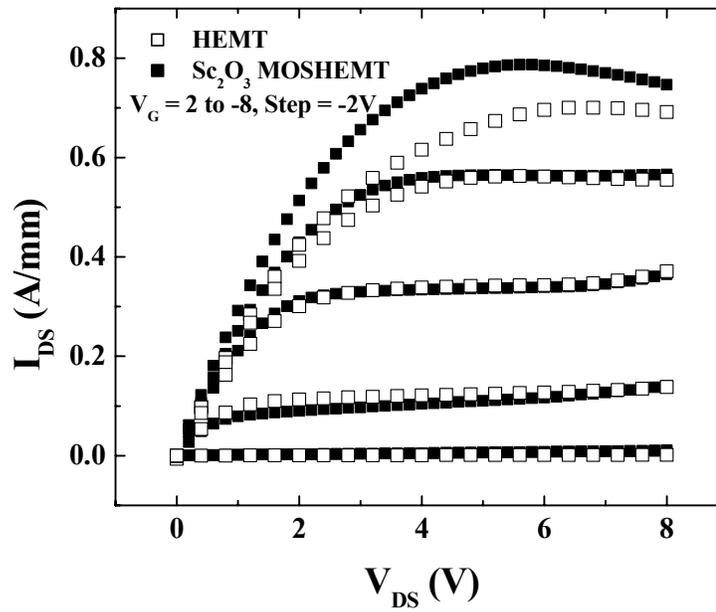


Figure 3-23. IDS-VDS characteristics for $1 \times 60 \mu\text{m}^2$ MOS-HEMTs and HEMTs fabricated on the same wafer. The gate voltage was varied from 2 to -8 V in steps of -2 V

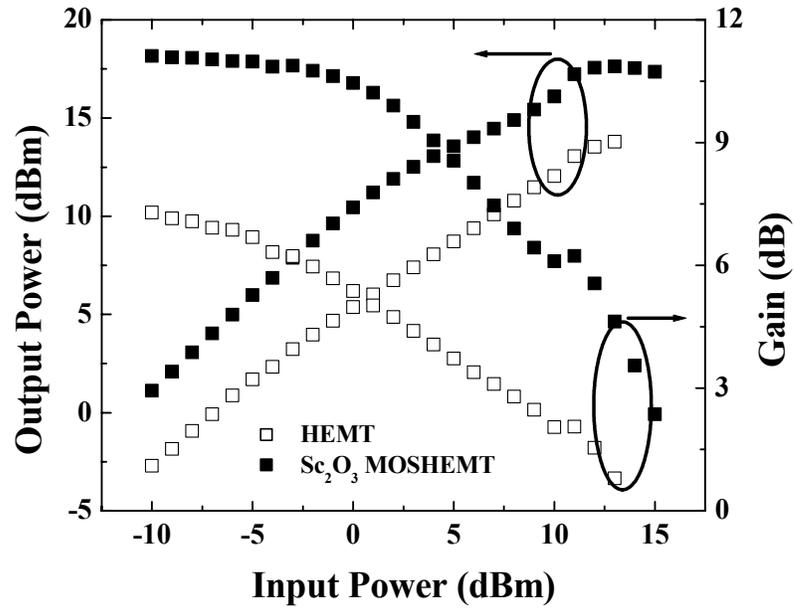


Figure 3-24. Output power and gain vs input power at 4 GHz of $1 \times 60 \mu\text{m}^2$ MOS-HEMTs and HEMTs fabricated on the same wafer

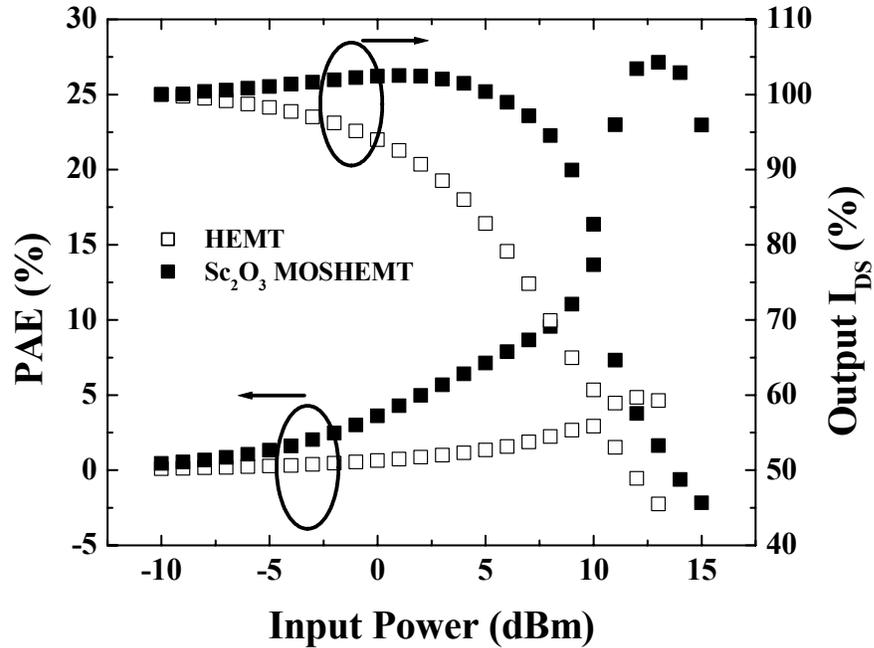


Figure 3-25. Power-added efficiency at 4 GHz of $1 \times 60 \mu\text{m}^2$ MOS-HEMT and HEMTs fabricated on the same wafer

HEMT versus Sc_2O_3 Passivated HEMT

Even without a MOS-gate, the HEMT performance is significantly improved by the presence of the Sc_2O_3 surface passivation layer. Figure 3-26 shows the output curves of metal-gate HEMTs with and without Sc_2O_3 passivation. Once again the drain current improves due to a reduction in the carrier depletion effects of the surface. Similar conclusions are drawn from the transfer characteristics in Figure 3-27. The saturation drain-source current increases from 0.55 A/mm to 0.75 A/mm with deposition of the Sc_2O_3 passivation layer and the threshold voltage shifts to more negative values because of the increase in effective channel carrier density.

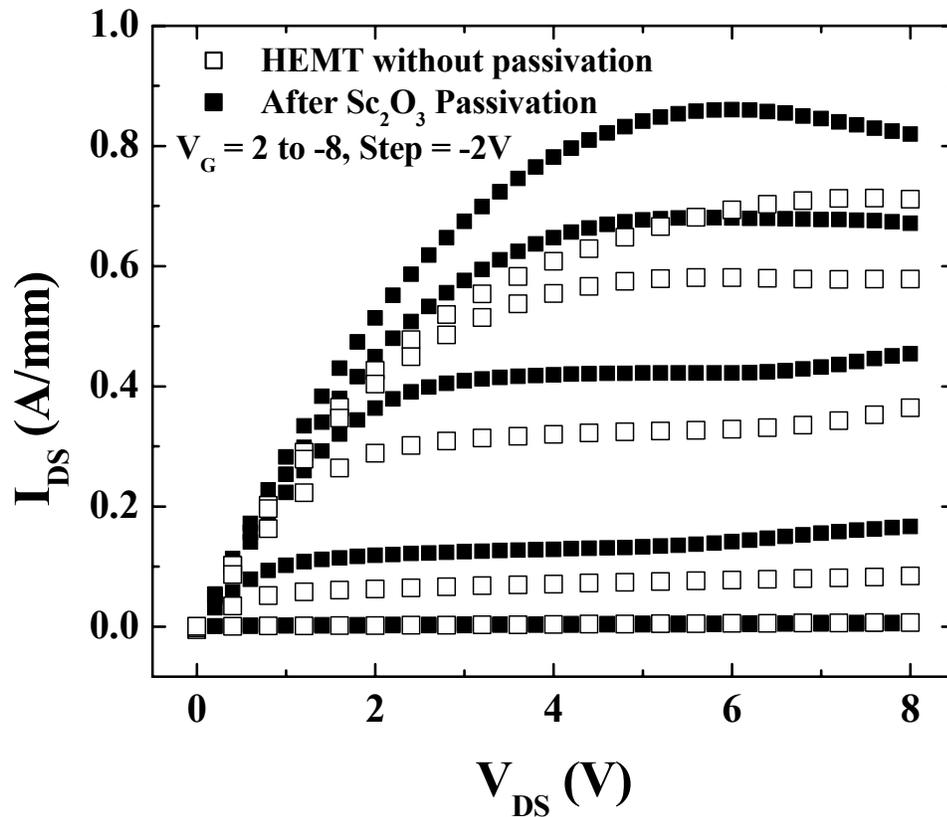


Figure 3-26. I_{DS} - V_{DS} characteristics for $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation. The gate voltage was varied from 2 to -8 V in steps of -2 V

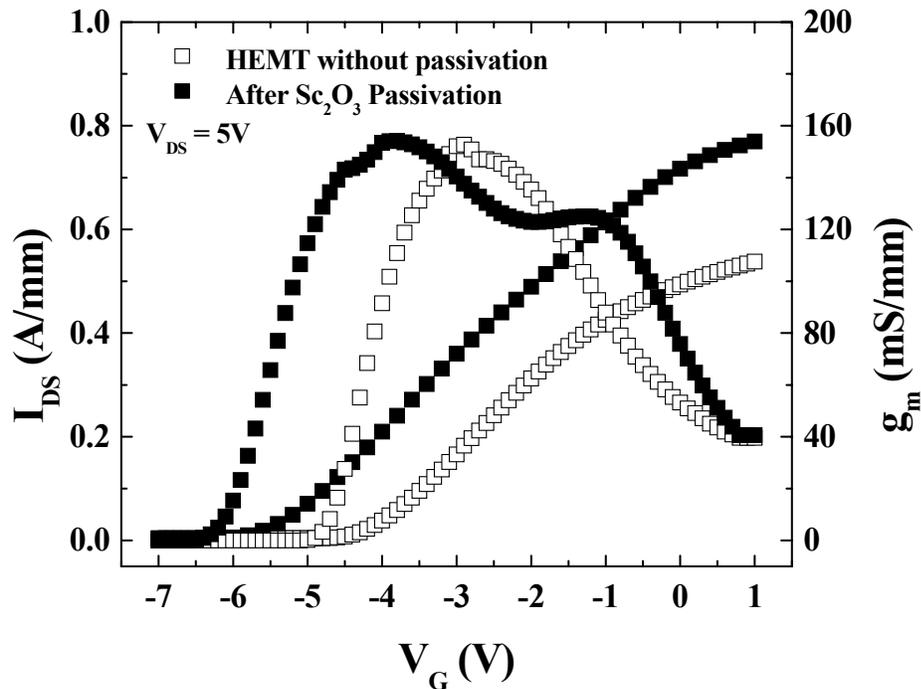


Figure 3-27. Transfer characteristics for $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation. The drain voltage was -5 V

The reduction in forward and reverse leakage was quite evident on the passivated HEMTs, as shown in Figure 3-28. This is consistent with a reduction in surface recombination center density and the series resistance of the HEMT is reduced due to the reduction in surface depletion effects on the channel carrier density. This same effect leads to an increase in reverse breakdown voltage. In addition, we observed an increase in the three-terminal breakdown voltage as seen in the $I_{\text{DS}}\text{-}V_{\text{DS}}$ curves at -9 V of gate bias voltage of Figure 3-29. This is the first report of an increase in three-terminal drain breakdown voltage of an AlGaIn/GaN HEMT after any form of surface passivation. The output power characteristics of the Sc_2O_3 -passivation HEMTs were significantly better than those of the comparison, unpassivated devices from the same wafer. Figure 3-30

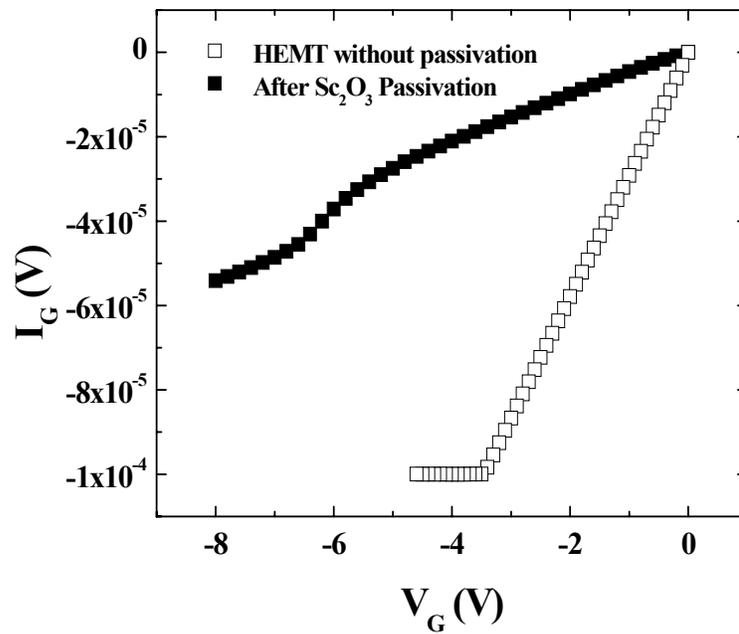
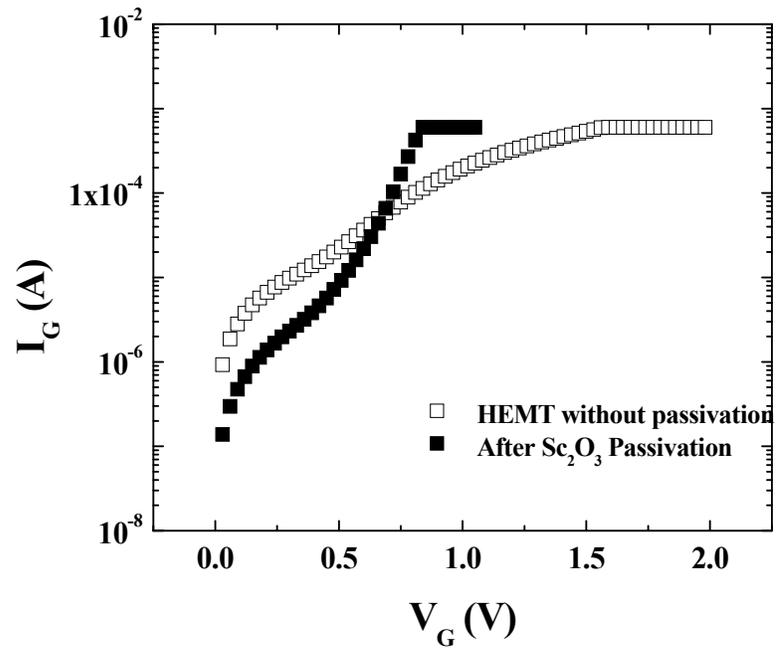


Figure 3-28. Forward a) and reverse b) I-V characteristics from $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation

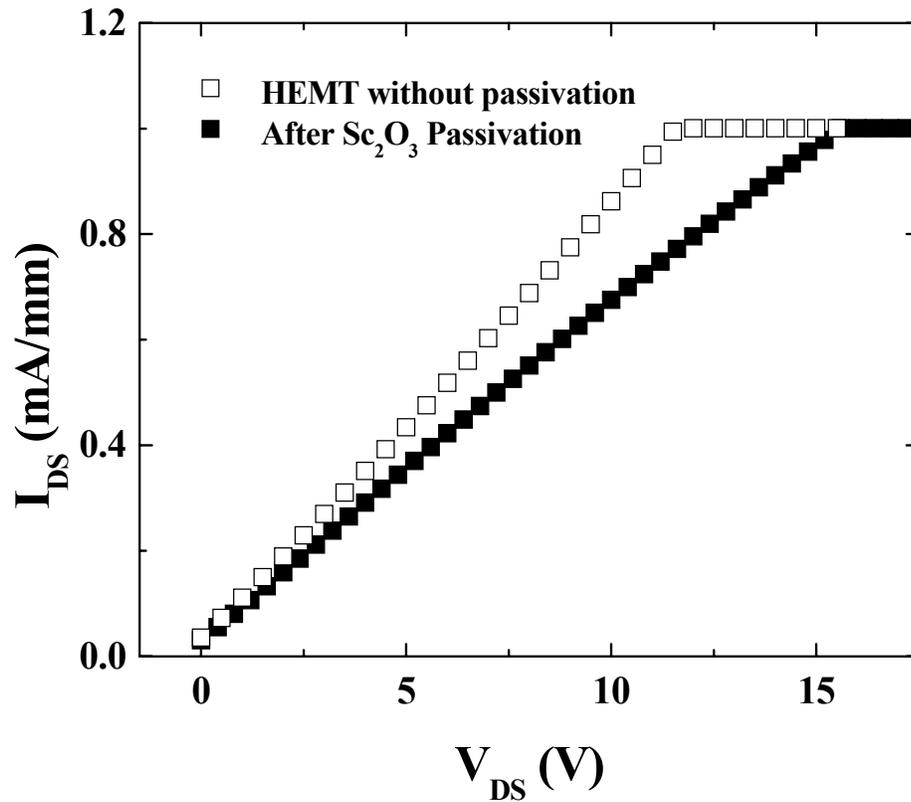


Figure 3-29. Forward I_{DS} - V_{DS} characteristics from $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation

shows the power sweep curves at 4 GHz under class A conditions for passivated and unpassivated HEMTs. The power-added efficiency also shows a major improvement from $\sim 5\%$ to 12% as a result of the passivation (Figure 3-31). The low PAE of the unpassivated HEMT is most likely due to the presence of surface states that decrease the output current. The PAE is calculated from the equation:

$$\text{PAE} = (\text{Pout_delivered} - \text{Pin_delivered}) / (\text{DC Power}) \quad (3-3)$$

In the case of the MOS-HEMT, PAE is high because the output power remains high even as output current decreases. Figure 3-32 shows I_{DS} - V_{DS} sweep characteristics for an unpassivated HEMT. There is an obvious decrease in the I_{DS} around the knee voltage

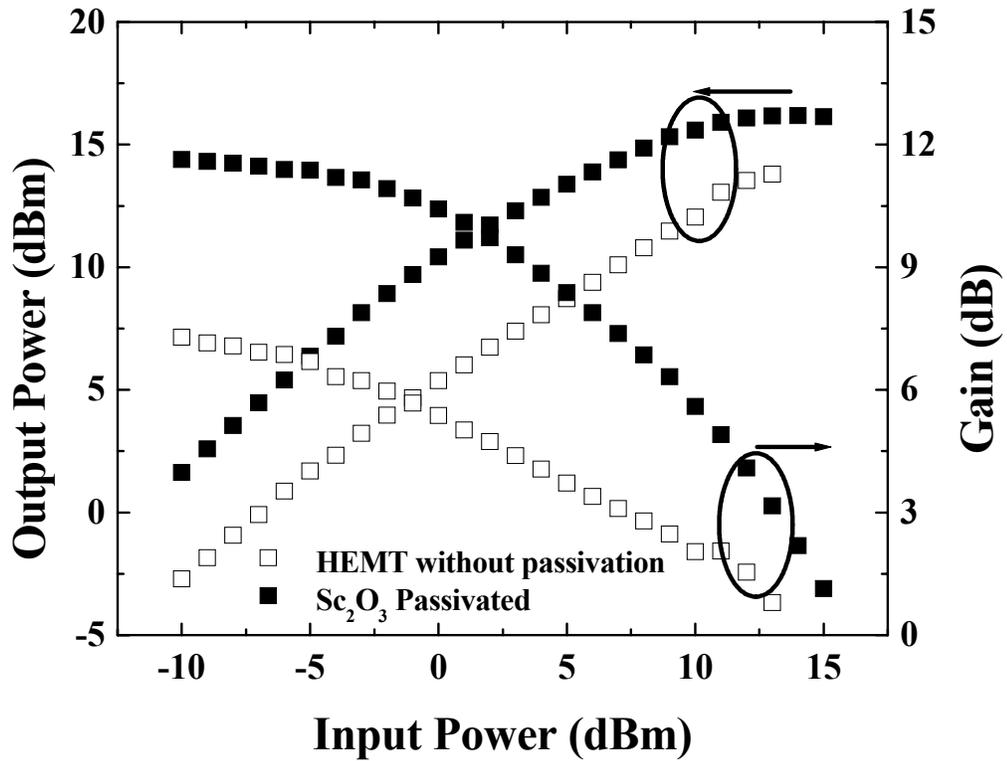


Figure 3-30. Output power and gain vs input power at 4 GHz of $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation

as the measurements are repeated. This phenomenon was not observed on the passivated HEMTs or on the MOS-HEMTs and suggests the low PAE of the unpassivated device is due to the presence of surface states. A summary of the PAE data is shown in Table 3-I

Table 3-1. Power-added efficiency of unpassivated, Sc_2O_3 passivated and Sc_2O_3 MOS-HEMT as a function of V_{DS}

V_{DS} Bias Voltage	Power-added Efficiency (PAE)		
	Unpassivated HEMT	Sc_2O_3 Passivated HEMT	Sc_2O_3 MOS-HEMT
5V	3.5%	6.4%	24.5%
10V	4.8%	12%	27.1%
15V	3.6%	13.2%	18.6%

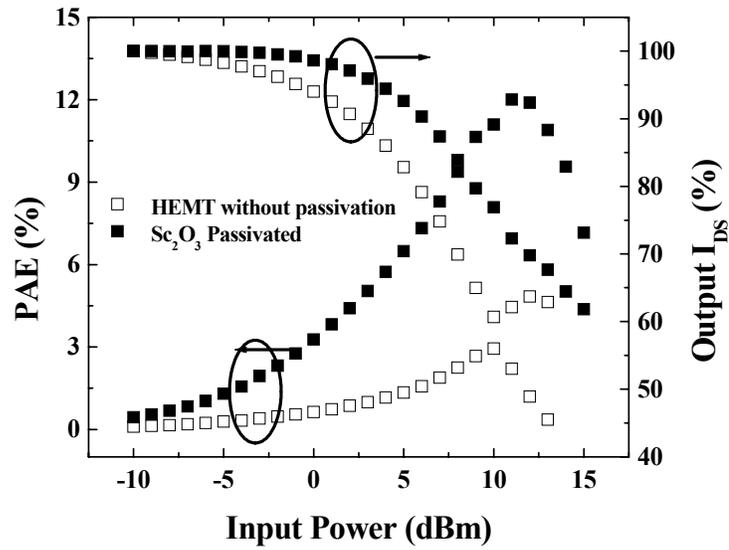


Figure 3-31. Power-added efficiency at 4 GHz of $1 \times 60 \mu\text{m}^2$ HEMTs with and without Sc_2O_3 passivation

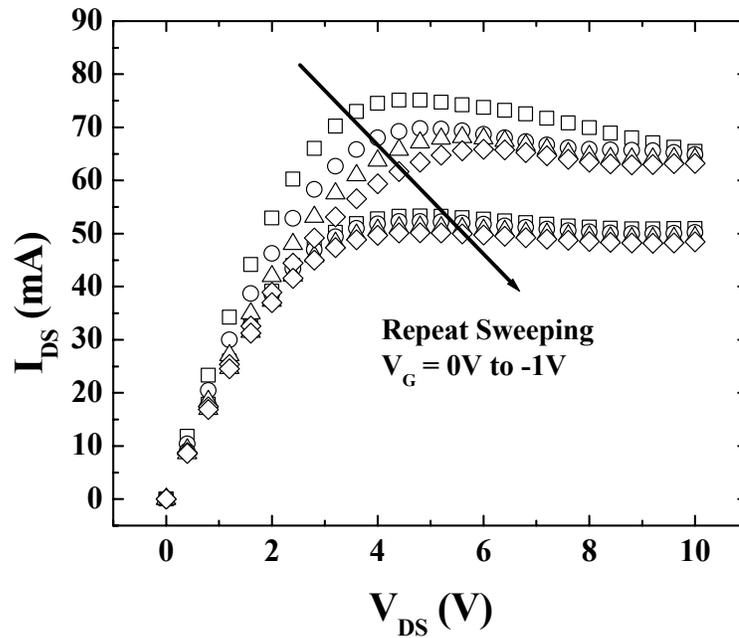


Figure 3-32. $I_{\text{DS}}-V_{\text{DS}}$ sweep measurements of unpassivated HEMT. The V_{DS} is swept from 0 V to 10 V, with $V_{\text{G}} = 0$ to -1 V in -1 V step. This phenomenon is not observed on passivated HEMTs or on MOS-HEMTs

AlGaN/GaN HEMT as Fluid Sensors

The HEMT structures were grown by metal organic chemical vapor deposition at 1040 °C on C-plane Al₂O₃ substrates. The layer structure consisted of a low temperature GaN nucleation layer, a 3 μm undoped GaN buffer and a 30 nm Al_{0.3}Ga_{0.7}N undoped layer. The sheet carrier density in the channel was $8 \times 10^{12} \text{ cm}^{-2}$ with a 300 K electron mobility of 900 cm²/V s. The ungated HEMT was fabricated using Cl₂ /Ar inductively coupled plasma etching for mesa isolation and lift-off of e-beam deposited Ti/Al/Pt/Au subsequently annealed at 850 °C for 30 s to lower the Ohmic contact resistance. Silicon Nitride was used to encapsulate the source/drain regions, with only the gate region open to allow the polar liquids to reach across the surface. A cross-section of the device is shown in Figure 3-33, while a plan view of the device layout is shown in Figure 3-34. The source–drain current–voltage characteristics were measured at 25 °C using an Agilent 4156 C parameter analyzer with the gate region exposed either to air, or 3 mm² of water, 50% or 75% acetone or 5–10% HCl.

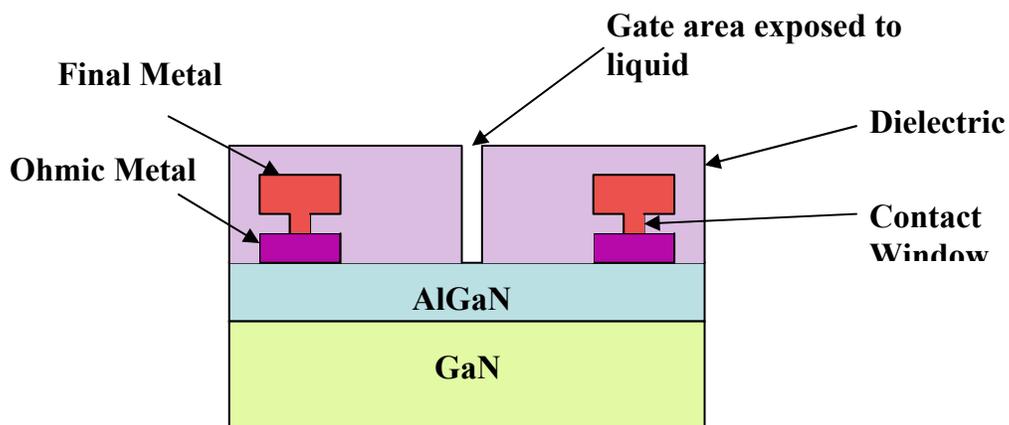


Figure 3-33. Cross – section of ungated AlGaN/GaN HEMT for liquid sensing

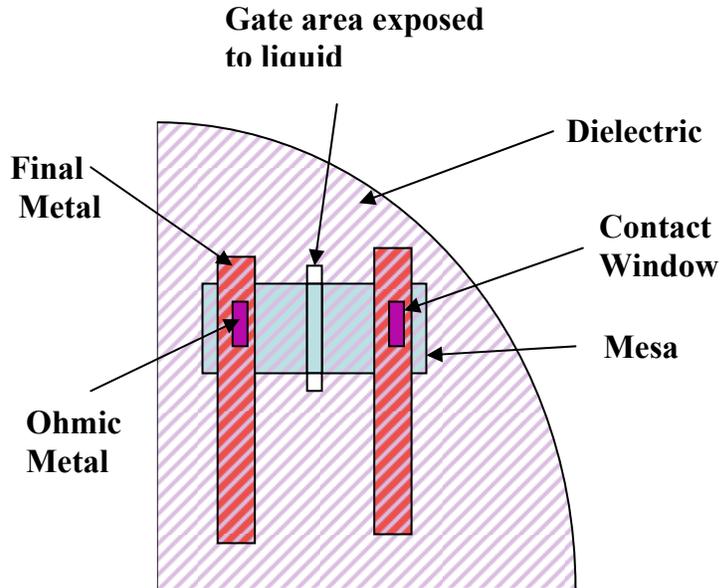


Figure 3-34. Plan view of the device layout of ungated AlGaIn/GaN HEMT for liquid sensing

Figure 3-35 shows the I–V characteristic from HEMTs exposed to air, H₂O or 50% and 75% acetone. The results are similar to those reported previously by Neuberger et al. [81]. The current is significantly reduced upon exposure to any of the polar liquids relative to the value in air. As seen previously, acetone has the largest effect [81], which correlates with its high dipole moment (2.7 Dy). The data in Figure 4-3 also shows that the HEMT sensor is sensitive to the concentration of polar liquid and therefore could be used to differentiate between liquids into which a small amount of leakage of another substance has occurred.

Fig. 3-36 shows the I–V characteristics of HEMTs in either air or 5% or 10% HCl. At a bias of 30 V, there is a difference in current of 8 mA for exposure to 5% versus 10% HCl, showing the remarkable sensitivity of the HEMT to relatively small changes in concentration of the liquid. There is still much to understand about the mechanism of the current reduction in relation to the adsorption of the polar liquid molecules on the

AlGaN/GaN surface. It is clear that these molecules are bonded by Van der-Waals type interactions and that they screen surface charge that is induced by polarization in the AlGaN/GaN heterostructure. This leads to changes in the induced electron density in the two dimensional electron gas that resides just below the AlGaN/GaN interface. Different chemicals are likely to exhibit different degrees of interaction with the AlGaN surface. Steinhoff et al [83] found a linear response to changes in the pH range 2–12 for ungated GaN-based transistor structures and suggested that the native metal oxide in the semiconductor surface is responsible.

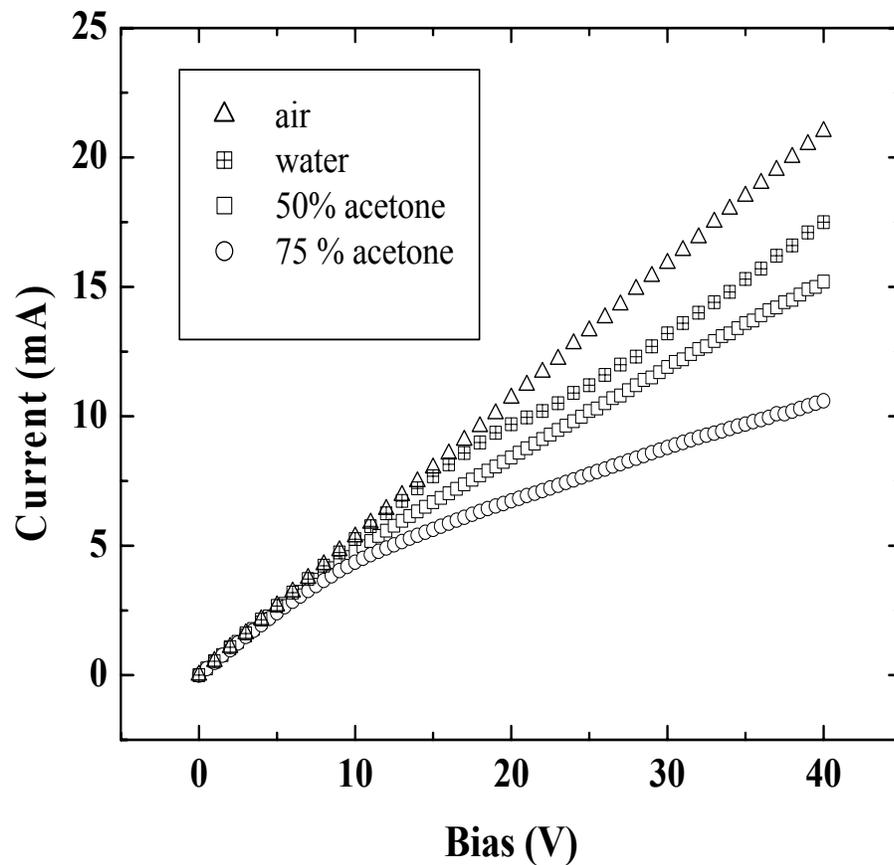


Figure 3-35. Drain-source I - V characteristics of ungated AlGaN/GaN HEMTs exposed to various concentrations of acetone in gate region

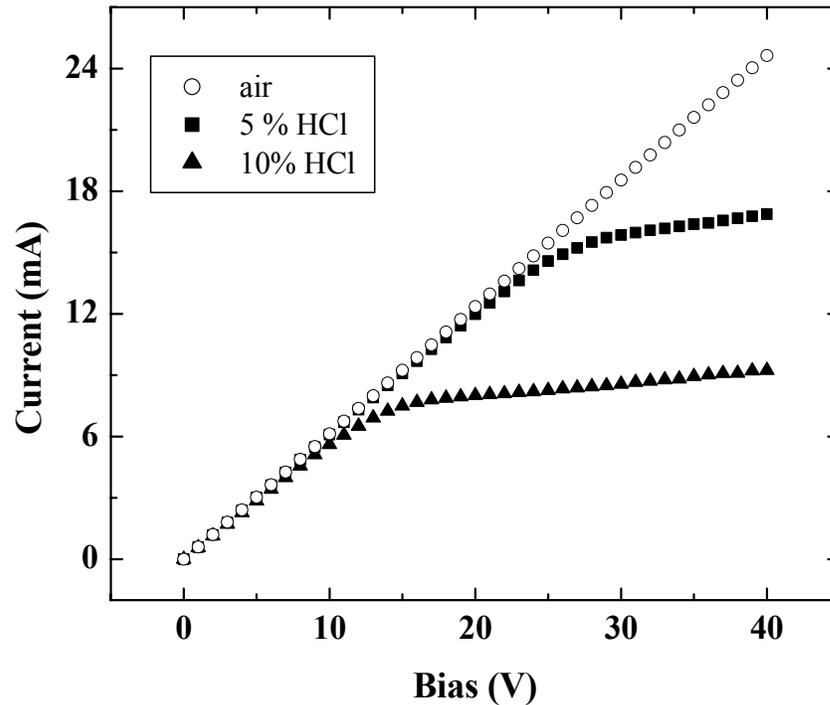


Figure 3-36. Drain-source I - V characteristics of ungated AlGaIn/GaN HEMTs exposed to air or various concentrations of HCl in gate region

Effect of Deposition Conditions and Annealing on W Schottky Contacts on n-GaN

The starting samples were $\sim 2 \mu\text{m}$ of n-type ($2 \times 10^{17} \text{ cm}^{-3}$) GaN grown on Al_2O_3 substrates by Metal Organic Chemical Vapor Deposition. For all samples, Ti/Al/Pt/W/Ti/Au deposited by e-beam evaporation and sputtering, patterned by lift-off and annealed at 850°C , 45 sec under a flowing N_2 ambient was used for ohmic contacts. Ti (200 Å)/ Al (1000 Å)/ Pt (400 Å) structure was e-beam deposited, followed by 500 Å W deposited by Ar plasma-assisted RF sputtering. After W sputtering, the samples were rinsed in buffered oxide etchant (BOE) to remove tungsten oxide and the 200 Å Ti/800 Å Au overlayer was deposited by e-beam evaporation. The W was sputtered to a thickness of 700 Å using Ar plasma-assisted deposition at pressures of 15-40 mTorr and

RF (13.56 MHz) powers of 200-250 W. A bilayer of Pt (200 Å)/Au (800 Å) was deposited by sputtering (RF sputtering for Pt and DC sputtering for Au) in the same chamber to reduce the contact sheet resistance. For comparison with conventional Schottky contacts on n-GaN, we also fabricated devices with Ni (200 Å)/Au (800 Å) metallization deposited by e-beam evaporation. The current-voltage (I-V) characteristics were recorded at 25 °C using an Agilent 4156 C parameter analyzer.

Comparison of Sputtered W Schottky Contacts with “Conventional” Ni/Au Contacts

Figure 3-37 shows the specific resistance of the W contact without any Pt/Au overlayer and the W sputter rate and DC self bias as a function of cathode power during the sputter deposition. The sputtering rate increases with power and the DC bias on the cathode also increases. This resistance was measured by a four-point probe and is determined only by the properties of the metal and not of the underlying GaN. The mechanism may be a more compact film at high sputtering powers.

Figure 3-38 shows the specific contact resistance and DC self-bias as a function of process pressure during sputtering of the W at fixed power of 200 W. The specific contact resistance is minimized at low pressures. The sputtering rate decreased with increasing pressure and the film most likely incorporates Ar gas under these conditions. Figure 3-39 shows the forward and reverse I-V characteristics of the W/Pt/Au diodes before and after annealing at both 500 and 600 °C and also from evaporated Ni/Au contacted diodes. We fit the forward I-V characteristics to the relation for the thermionic emission over a barrier as,

$$J_F = A^* T^2 \exp\left(-\frac{e\phi_b}{kT}\right) \exp\left(\frac{eV}{nkT}\right) \quad (3-4)$$

where J is the current density, ϕ_b the barrier height, n the ideality factor and V the applied voltage. From the data, ϕ_b was obtained as 0.80 eV for the as-deposited W

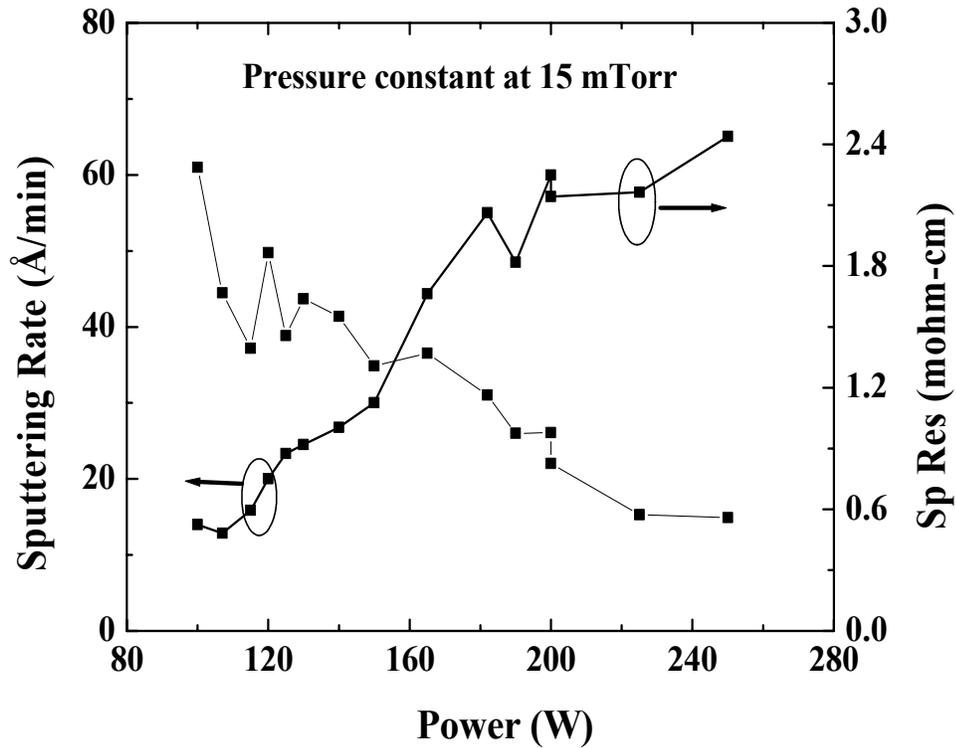


Figure 3-37. Dependence of specific resistance and sputter rate of W contacts deposited at 15 mTorr on GaN and DC self-bias b) on RF power during deposition

(similar to the value for evaporated Ni) and ~ 0.4 eV after 600 °C annealing (Table 3-II).

The forward I-V characteristics in each case showed the ideality factor was > 1.1 - 1.3 , suggesting transport mechanisms other than thermionic emission, such as recombination.

For anneals at ≥ 700 °C, the rectifying nature of the W-based contacts was significantly degraded due to the formation of β -phase W_2N , as expected previously [192, 193].

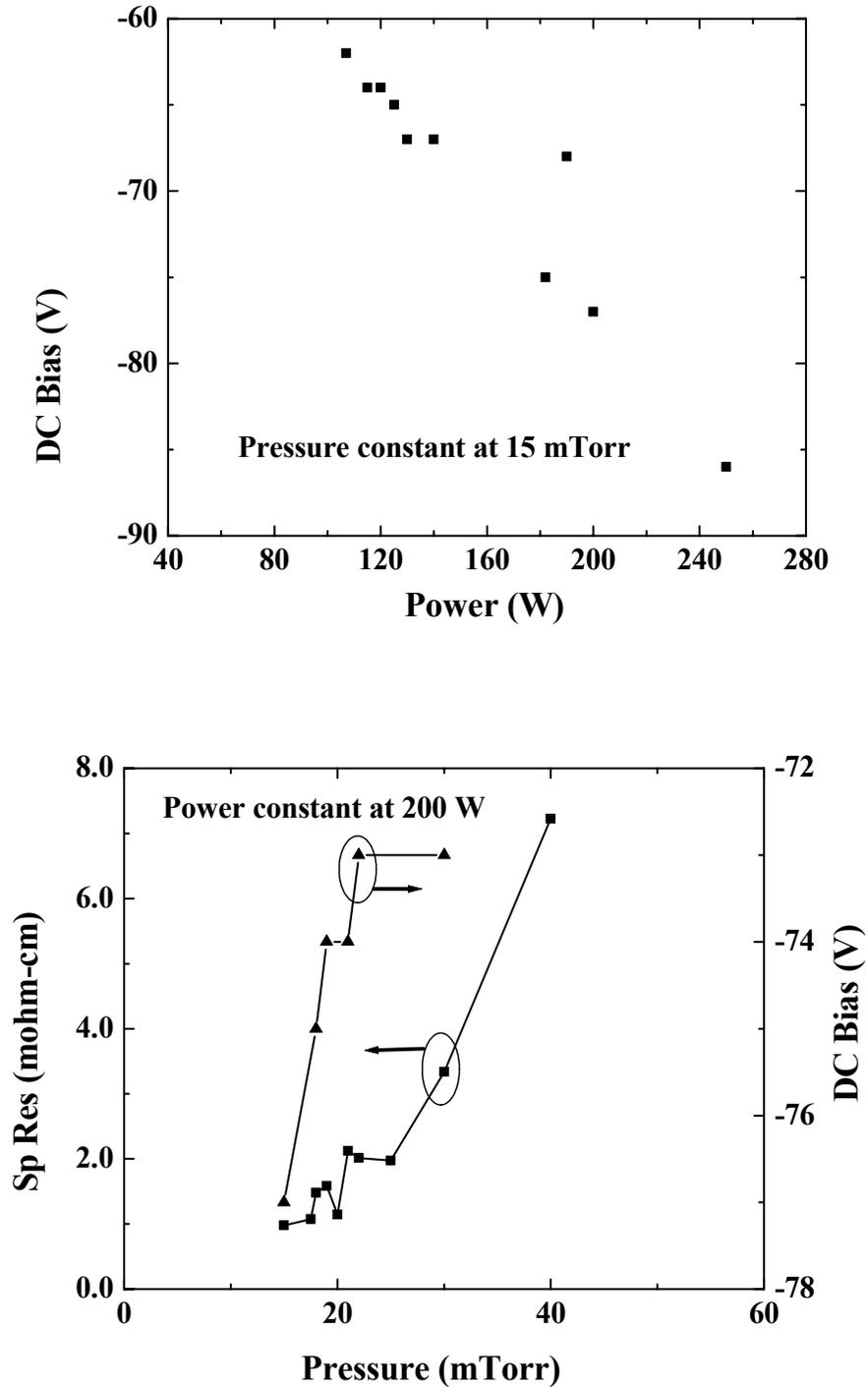


Figure 3-38. Dependence of a) Specific resistance of W contacts and b) DC self-bias on process pressure during deposition. The power was held constant at 200 W

Table 3-2. Barrier height and ideality factor of various contact schemes

Metal Scheme	n (ideality constant)	ϕ_{Bn} (eV)
Ni/Au	1.25243	0.79956
W/Pt/Au	1.3274	0.80186
W/Pt/Au 500 °C	1.32621	0.47325
W/Pt/Au 600 °C	1.14012	0.39961

Figure 3-39 (b) shows the reverse I-V characteristics from the diodes. In presence of image-force induced barrier lowering, the reverse current can be expressed as [198]

$$I_R = AA^{**}T^2 \exp\left[\frac{e}{kT}(\phi_b - \Delta\phi_b)\right], \quad (3-5)$$

where A is the area, A^{**} is the effective Richardson constant, $\Delta\phi_b$ is the image force barrier lowering given by $(eE_m/4\pi\epsilon)^{0.5}$, E_m the maximum electric field strength at the contact and ϵ is the GaN permittivity. The reverse current shown in Figure 3-39 is several orders of magnitude higher than expected from this relation and indicates other current transport mechanisms are present.

The high barrier height measured on the as-deposited W contacts may be due to the presence of an interfacial oxide layer since the theoretical value extracted from the relation $\phi_m - \chi_s$ (where ϕ_m is the metal work function and χ_s the electron affinity of GaN) is 0.4 eV and this is only reached after 600 °C annealing where the oxide is dissolved.

Summary

In conclusion, Sc_2O_3 thin films deposited by MBE were shown to provide high quality interfaces with AlGaIn/GaN HEMT structures, even after the ohmic contact anneal at 850 °C. Sc_2O_3 can act simultaneously as both the gate dielectric and as a surface passivation layer and is free of residual hydrogen, which may be an advantage in

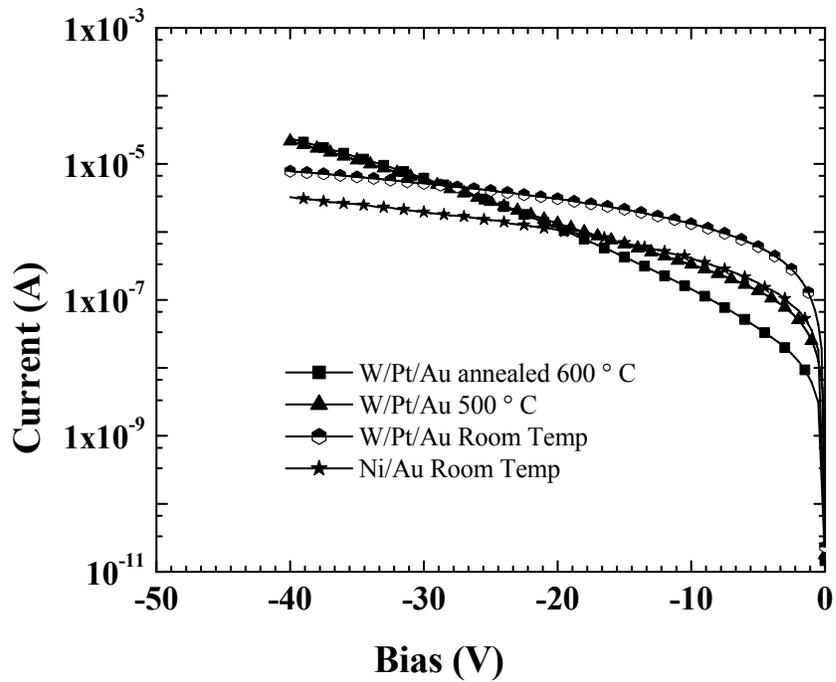
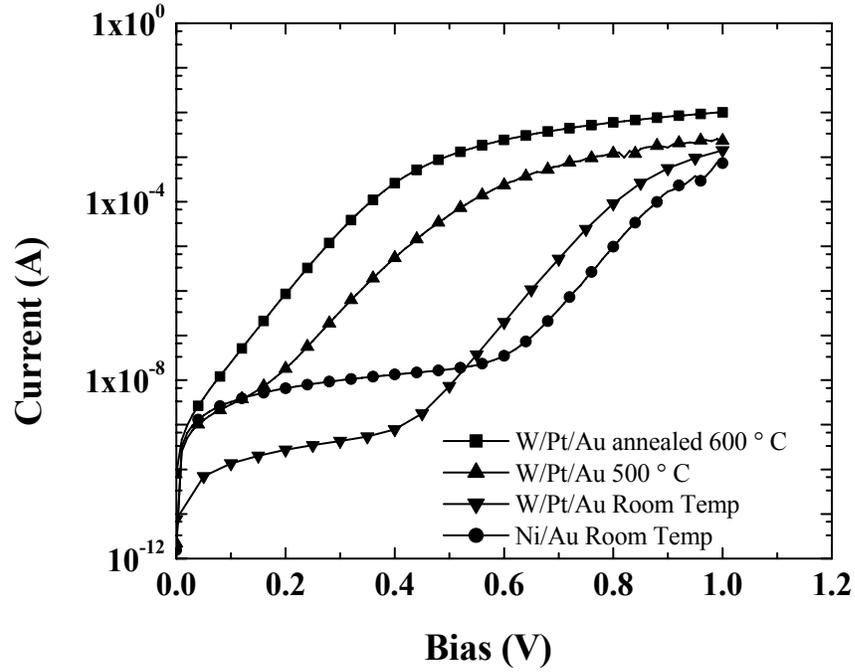


Figure 3-39. a) Forward and b) reverse I-V characteristics from the various contact schemes

terms of long term stability relative to dielectrics deposited using SiH_4 or other hydrogenated precursors. We demonstrated that Sc_2O_3 thin films deposited by plasma-assisted Molecular Beam Epitaxy can be used simultaneously as a gate oxide and as a surface passivation layer on an AlGaIn/GaN High Electron Mobility Transistors (HEMTs). The maximum drain source current, I_{DS} reached a value of over 0.8 A/mm and was $\sim 40\%$ higher on $\text{Sc}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ transistors relative to conventional HEMTs fabricated on the same wafer. The Metal – Oxide – Semiconductor HEMTs (MOS – HEMTs) threshold voltage was in good agreement with the theoretical value, indicating the Sc_2O_3 retains a low surface state density on the AlGaIn/GaN structures and effectively eliminates the collapse in drain current seen in unpassivated devices. The MOS-HEMTs can be modulated to +6 V of gate voltage.

In particular, Sc_2O_3 was shown to be a very promising candidate as a gate dielectric and surface passivant because it is more stable on GaN than is MgO. Sc_2O_3 has a bixbyite crystal structure, large bandgap (6.3 eV) and high dielectric constant. MgO and Sc_2O_3 thin films deposited by MBE showed very promising results as surface passivation layers on GaN based HEMTs. HEMTs with GaN-cap layer provided more effective mitigation of drain current collapse than AlGaIn-capped HEMT. Sc_2O_3 provided stable passivation characteristics over a period of at least 5 months, while the MgO was found less effectiveness under the same conditions. With respect to SiN_x passivation, no obvious advantage to the use of deuterated precursors for the deposition was found. Three different passivation layers (SiN_x , MgO and Sc_2O_3) were examined for their effectiveness in mitigating surface-state-induced current collapse in AlGaIn/GaN high electron mobility transistors (HEMTs). The plasma-enhanced chemical vapor deposited

SiN_x produced ~80-85% recovery of the drain-source current, independent of whether SiH_4/NH_3 or SiD_4/ND_3 plasma chemistries were employed. Both Sc_2O_3 and MgO produced essentially complete recovery of the current in GaN-cap HEMT structures and ~80-95% recovery in AlGaN-cap structures. Sc_2O_3 had superior long-term stability, with no change in HEMT behavior over 5 months aging.

The MOS-HEMTs showed experimental threshold voltages in good agreement with theoretical values, as expected from the low surface state densities of the $\text{Sc}_2\text{O}_3/\text{GaN}$ system. The DC and power characteristics of AlGaN/GaN MOSHEMTs with Sc_2O_3 gate dielectrics were compared with that of conventional metal-gate HEMTs fabricated on the same material. The MOSHEMT shows higher saturated drain-source current (~0.75 A/mm) and significantly better power-added efficiency (27%) relative to the HEMT (~0.6 A/mm and ~5%). Sc_2O_3 also provides effective surface passivation, with higher drain current, lower leakage currents and higher three-terminal breakdown voltage in passivated devices relative to unpassivated devices. The power added efficiency also increases (from ~5 to 12%) on the surface passivated HEMTs, showing that Sc_2O_3 is an attractive option for reducing gate and surface leakage in AlGaN/GaN heterostructure transistors.

The low temperature (100 °C) deposition of Sc_2O_3 or MgO layers was found to significantly increase the output power of AlGaN/GaN HEMTs. At 4 GHz, there was a better than 3 dB increase in output power of $0.5 \times 100 \mu\text{m}^2$ HEMTs for both types of oxide passivation layers. Both Sc_2O_3 and MgO produced larger output power increases at 4 GHz than conventional PECVD SiN_x passivation which typically showed ≤ 2 dB increase on the same types of devices. The HEMT gain also remained linear over a wider

input power range with the Sc_2O_3 or MgO passivation. These films appear promising for reducing the effects of surface states on the DC and rf performance of $\text{AlGaIn}/\text{GaIn}$ HEMTs. Sc_2O_3 and MgO are promising surface passivation materials for $\text{AlGaIn}/\text{GaIn}$ HEMTs. They produced significantly higher output power increases than the more conventional PECVD SiN_x passivation on the same devices and may be more suited to high temperature applications because of their larger bandgaps (6.3 eV for Sc_2O_3 , 8 eV for MgO compared to ~ 5 eV for SiN_x). It is still necessary to minimize the trap density in the HEMT buffer layers because the deposition of these oxides is effective only in reducing surface trapping effects that produce the frequency dependent current degradation.

$\text{AlGaIn}/\text{GaIn}$ ungated HEMTs showed dramatic changes in drain–source current upon exposure to polar liquids in the gate region. Bonding of polar liquid molecules appeared to alter the polarization-induced positive surface charge, leading to changes in the channel carrier density and hence the drain–source current. The results showed the potential of $\text{AlGaIn}/\text{GaIn}$ transistor structures for a variety of chemical, gas and biological sensing applications. An $\text{AlGaIn}/\text{GaIn}$ high electron mobility transistor structure was used for sensing different liquids present in the gate region. The forward current showed significant decreases upon exposure of the gate area to solvents (water, acetone) or acids (HCl). The pH sensitivity is due to changes in net surface charge that affects the relative depletion in the channel of the transistor. The results indicated that nitride-based heterostructures may have application in integrated chemical, gas and fluid monitoring sensors.

Sputter-deposited W Schottky contacts on n-GaN showed as-deposited barrier heights (ϕ_b) of 0.80 eV for optimized conditions. Subsequent annealing at 500-600 °C reduced the barrier height to ~0.4 eV, its theoretical value from the relation $\phi_b = \phi_m - \chi_s$ (where ϕ_m is the metal work function and χ_s the electron affinity of GaN). The lowest specific resistance for W was obtained for high power, low pressure (< 20 mTorr) deposition conditions where the incident ion energy and deposition rate were optimized to minimize damage to the GaN surface. At higher annealing temperatures the W reacted with the GaN to form β -phase W_2N .

CHAPTER 4
VERY LOW DARK CURRENT HIGH SPEED INFRA-RED PHOTODETECTORS
AND OPTO-ELECTRONIC MIXERS

Introduction

Long distance telecommunications applications require material system with 1.3 μm /1.55 μm capabilities, where the dispersion and attenuation of the traveling wave is minimized. Due to its low energy bandgap and high detection sensitivity at these wavelengths, InGaAs is very well suited for use in optoelectronic integrated circuits and in particular, in high speed photodetectors. An improved process technology for achievement of very low dark current in high speed 1.55 μm inter-digitated metal-semiconductor-metal (MSM) photo-detectors utilizing a multiple quantum well InGaAs/InAlAs layer structure and etch-back planarized-mesa process to reduce the dark current is considered.

There is strong interest in the development of high speed, low dark-current photodetectors in various parts of the electromagnetic spectrum. For example, GaN photodetectors are used for solar-blind UV detection [105-110]. Inter-digitated MSM photodetectors fabricated on GaAs have been used in a variety of applications, including high-speed sampling systems, chip-to-chip connections and high-speed communication systems [111-115]. InGaAs based optoelectronic devices on InP substrates are making their impact on telecommunication industry with improvements in fabrication technology [115-124]. As more research is accomplished on this material system, various alternatives emerge to solve manufacturing issues. InGaAs photodetectors based on

2 DEG structure [116] and InGaAs photodetectors on Si and GaAs substrates have been reported earlier [117]. Devices with small ($0.2\ \mu\text{m}$ feature size finger electrodes) have demonstrated a 3 dB bandwidth at 78 GHz ($1.55\ \mu\text{m}$ wavelength) [120]. The temporal response of InGaAs MSM photodetectors under high illumination conditions has also been reported and the shape of the rise and fall times analyzed [121].

Inter-digitated finger metal-semiconductor-metal photodetectors (MSMPDs) are widely used for high-speed optoelectronic (OE) applications and are also used as OE mixers to generate radio-frequency subcarriers in fiber-optic microwave links [125-126]. Recently, GaAs MSMPDs have been successfully utilized as OE mixers in an incoherent laser radar (LADAR) system where a backscattered intensity-modulated light signal and a bias voltage [local oscillator (LO) voltage] (0.1-1.0 GHz) are mixed to recover an intermediate frequency (IF) signal (100 Hz-1.0 MHz) [127-128].

InGaAs MSMPDs would allow LADAR operation at eye-safe wavelengths. Unfortunately, the Schottky barrier height on InGaAs is quite low ($\sim 0.1\text{-}0.2\ \text{eV}$) [3] leading to high dark current and, hence, low signal-to-noise ratio. To reduce dark current, various methods of “enhancing” the Schottky barrier are used. The most commonly used method employs a high-band-gap lattice-matched InP [4] or InAlAs [5-6] Schottky enhancement layer (SEL). Detectors using SELs yield low dark current, high responsivity, and high bandwidths.

The OE mixing effect in an InAlAs Schottky-enhanced InGaAs MSMPD will be analyzed. The frequency bandwidth of such a mixer would be compared to that of a photodetector. Mixing efficiency dependence on both the light modulation and IF frequencies would also be discussed along with reasons for the dependence. Band gap

discontinuity associated with the SEL would be utilized in a circuit model of the OE mixer to explain the experimental results.

The MBE grown InGaAs MSMPD consists of a 500 Å InAlAs SEL, a 250 Å In(Ga,Al)As graded layer, a 1.0 μm InGaAs absorption layer, and a 0.3 μm InAlAs buffer layer on a semi-insulating InP:Fe substrate. Ti/Au Schottky contacts were deposited by electron-beam evaporation with 3 μm finger widths and spacing. Contact pads and electrode tips are insulated from the InAlAs SEL to further reduce dark current [119].

Processing

Our metal-semiconductor-metal (MSM) structure consists of a 500 Å InAlAs/InGaAs multi-quantum well Schottky barrier enhancement layer, a 150 Å In(Ga,Al)As graded layer, a 1.0 μm InGaAs active layer, and a 0.3 μm InAlAs buffer layer grown on a semi-insulating InP:Fe substrate with a molecular-beam epitaxy (MBE) system. All devices were made using standard optical lithography and e-beam deposited Ti/Au metallization was used for Schottky and final metal contacts. Plasma enhanced chemical vapor deposited SiN_x and SiO₂ were employed for device passivation. CF₄/O₂ based plasma and H₂SO₄/H₂O₂/H₂O based wet-chemical etchant were used for dielectric etching and mesa definition.

Room temperature dark current measurements were performed using an HP4145B parameter analyzer. High speed measurements were conducted with a mode-locked Ti-sapphire laser-pumped optical parametric oscillator delivering 1.3-1.55 μm optical pulses at 76 MHz and power was tunable to 3-nJ. The pulses passed through a continuously variable inline attenuator for power control and a beam splitter for power

monitoring and the pulses were focused onto the device using a lens and a precision-adjustment stage. The high-speed signal was measured via two DC-to-40 GHz ground-signal-ground microwave probes attached through short transmission lines to a 40 GHz-digitizing oscilloscope.

Different Processing Sequences

Three different processing schemes were employed to achieve very low dark current, high speed and high responsive goal. In all of the processing schemes, the final metal contact pads were deposited on the top of a dielectric layer to reduce leakage current and capacitance resulting from the relatively large area of the final metal contact pads as compared to the actual device area. High leakage current means high dark current (high noise) and high capacitance means slower RC response in high frequency applications.

In the first MSM process scheme, Ti/Au (200 Å/1800 Å) based Schottky MSM fingers and finger-connections were deposited on top of the InGaAs/InAlAs MQW, followed by 1000 Å of Si₃N₄ and then 1850 Å of SiO₂. The thickness of dielectric films was determined through a simulation so as to have reflection losses of less than 5% in the wavelength of interest. Then a contact window was opened in the dielectric layer to contact the metal finger-connections as shown in Figure 4-1(a). The Ti/Au (200 Å/2500 Å) based final metal contact pads connected the MSM Schottky fingers through the dielectric window. In this process scheme, the dark current was generated from the MSM Schottky fingers as well as metal finger-connections. The second scheme, as shown in Figure 4-1(b), which has been demonstrate by Adesida et al. [117-118], employed a dielectric window. The metal finger-connections and finger-tips sit on the top of dielectric film. We opened the mesa window in the dielectric film (which was 2600 Å

of Si_3N_4) by dry etch and wet etch in succession. The final few 100 Å of dielectric was removed by wet etch to avoid any plasma damage.

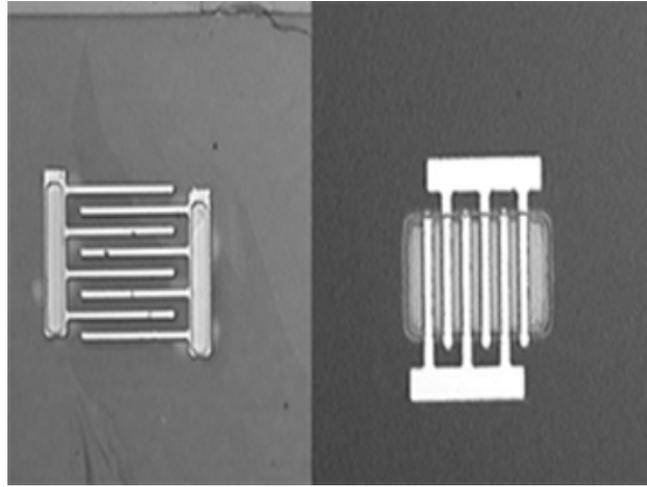


Figure 4-1. Photomicrographs of devices in which the a) contact window was opened after Schottky metal deposition and b) in which the mesa was opened in the dielectric before putting down Schottky metal

Dark current measurements were performed to determine the efficiency of each design in reducing noise. The measurements showed that the second processing scheme was more efficient in reducing the dark current. Dark current of less than 0.1 nA at a bias of 1V was obtained, as shown in the current-voltage (I-V) characteristics of Figure 4-2. By shape contrast, the dark current with the first processing scheme was on the order of 60 nA for a device of length 30 μm , finger width 1 μm and finger spacing 3 μm . In the second processing sequence, since the contact finger-tips were laying on top of the dielectric film, the dark current was greatly reduced. The electric field was also much more concentrated on the tip resulting in large leakage in the first case. This was further proven for measurements on a few devices in which their Schottky level was misaligned. The tips for these devices were on the semiconductor surface instead of the dielectric surface. These photodetectors displayed dark currents on the order of few 10's of

nano Amps. There was also an increase in the dark current with increase in device size as seen in Figure 4-2.

Figure 4-3 is a plot of the normalized temporal pulse response amplitude of these devices for three different biases. The device under test was a 50×50 MSM with $2.0 \mu\text{m}$ wide fingers with an inter-electrode spacing of $2.0 \mu\text{m}$. The optical power on the sample was 0.36 pJ/pulse and $\lambda = 1.50 \mu\text{m}$. Table 4-I gives the 10%-90% rise time, full width half maximum, and 10%-90% fall time for biases of 3.0 V , 6.0 V , and 9.0 V , respectively. Using the relation,

$$f_{3dB} \cdot \tau_{10\%-90\%} = 0.35, \quad (4-1)$$

where $\tau_{10\%-90\%}$ is the measured rise time, the estimated 3-dB cutoff frequency f_{3dB} for 6.0 V was estimated as (i.e., the 3 dB bandwidth) $\sim 22 \text{ GHz}$. At 12 V , we measured a rise time = 14.6 ps , FWHM = 40 ps , fall time = 129 ps and a 3 dB bandwidth of 24 GHz .

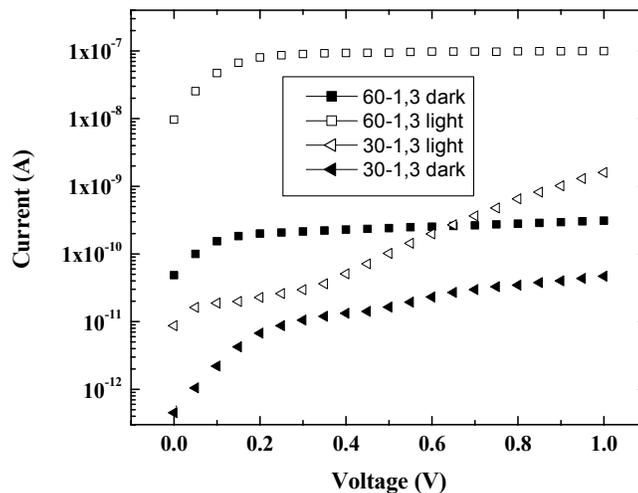


Figure 4-2. Measured I-V response of the device processed with the second type of fabrication sequence. The devices had lengths of $60 \mu\text{m}$ or $30 \mu\text{m}$ and finger widths of $1 \mu\text{m}$ and finger spacing of $3 \mu\text{m}$

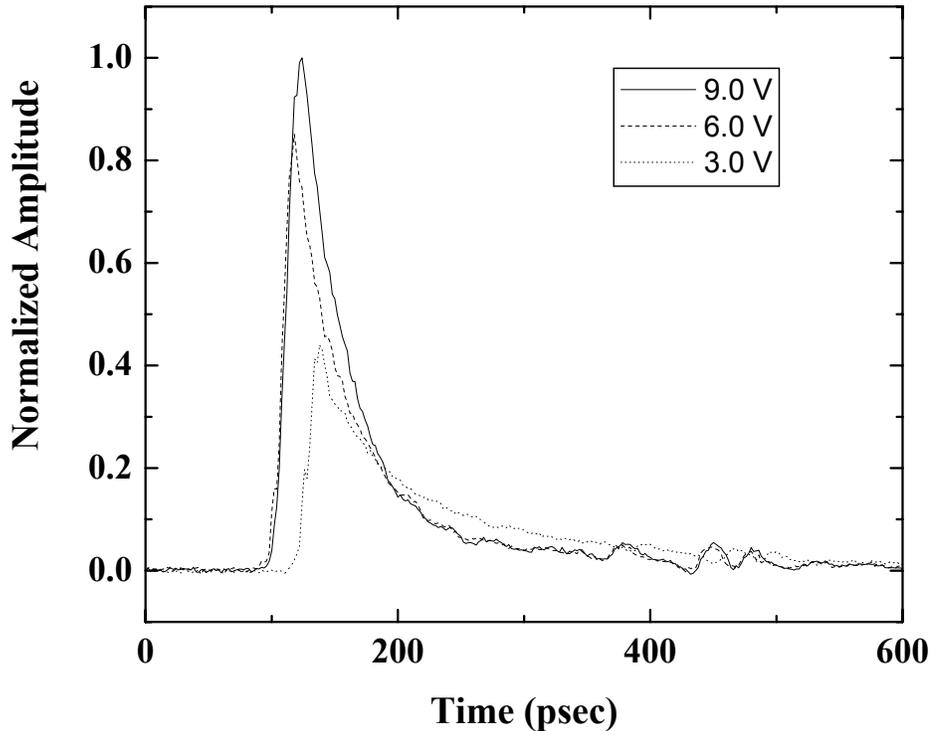


Figure 4-3. Temporal response for three different DC bias voltages for detectors processed with the second type of fabrication sequence

To further enhance the temporal response of the MSM detector without losing the advantage of low dark current, an etch back process was developed. Figure 4-4 shows the processing sequence to obtain a planarized structure before depositing the metal. The mesa was etched first, and then a dielectric equal in height to this mesa was deposited using PECVD. Planarization of the dielectric film was achieved with a polymer coating and a planarization coating etch-back to expose dielectric top. Then, the etch chemistry was switched to etch the dielectric using the planarization coating as a mask to expose the top surface of the semiconductor.

The planarization coating was subsequently removed with acetone at the completion of the process. Figure 4-5 illustrates a picture of a $30 \times 30 \mu\text{m}^2$ MSM etch-

back device with 1.0 μm wide fingers and an inter-electrode spacing of 3.0 μm . Figure 4-6 shows the dark current to be less than 1nA at 1 V and the device to be highly linear in response to the different levels of microscope light.

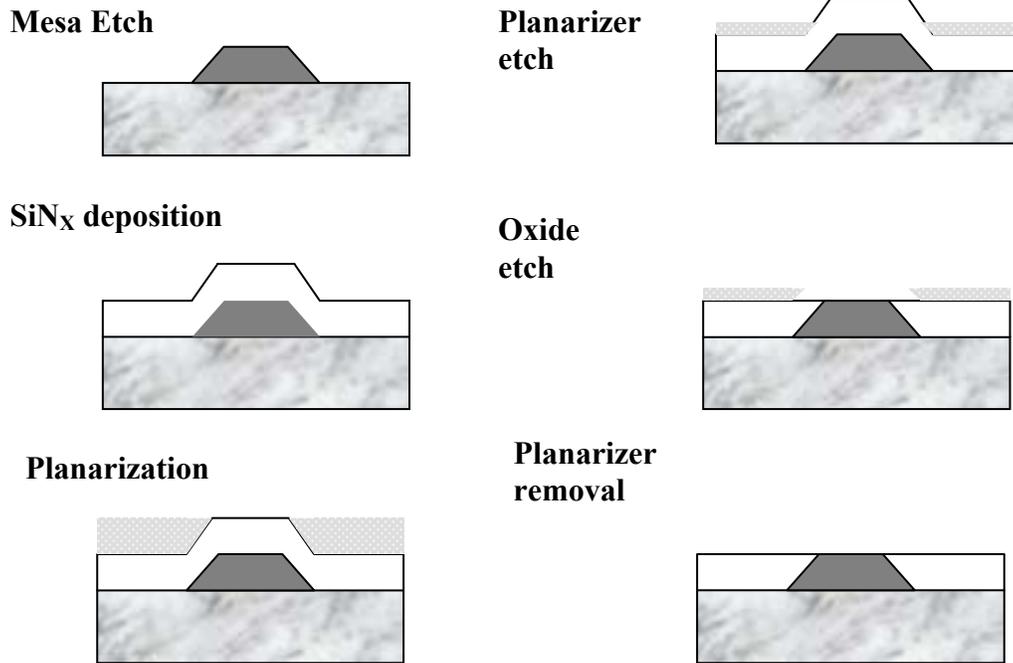


Figure 4-4. Processing sequence for etch back process

The dark current is slightly higher than for the second fabrication sequence, which may be resulting from the plasma etch damage during the etch back process. The damage can be reduced by switching the dry etch to wet chemical etching for the last few hundred angstroms of the dielectric film.

Table 4-1. Measured temporal response data for InGaAs MSM

Bias	10%-90% rise time	10%-90% fall time	FWHM
3.0 V	16.5 ps	242 ps	54 ps
6.0 V	16.1 ps	119 ps	40 ps
9.0 V	18.0 ps	97 ps	41 ps

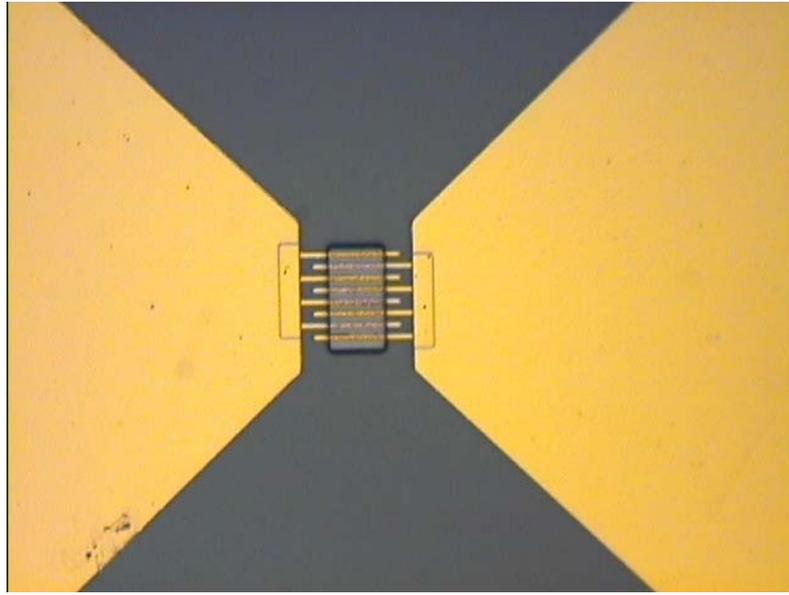


Figure 4-5. Top view of a $30 \times 30 \mu\text{m}^2$ MSM etch-back device with $1.0 \mu\text{m}$ wide fingers and an inter-electrode spacing of $3.0 \mu\text{m}$

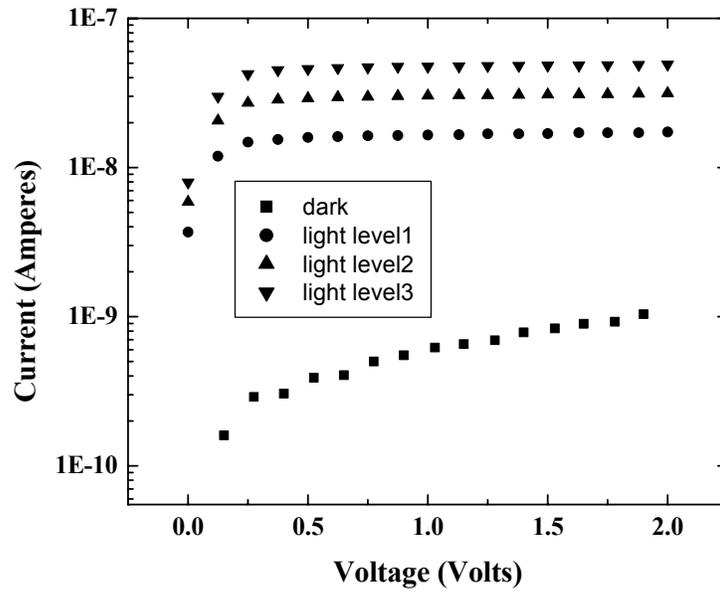


Figure 4-6. Current -Voltage characteristic of a $30 \times 30 \mu\text{m}^2$ MSM etch back device with $1.0 \mu\text{m}$ wide fingers with an inter-electrode spacing of $3.0 \mu\text{m}$

Indium-Gallium-Arsenide-Based Ultra-Fast Metal-Semiconductor-Metal Optical Switch

In this part we discuss preliminary results obtained for an indium-gallium-arsenide-based (InGaAs) inter-digitated-finger metal-semiconductor-metal (MSM) optoelectronic (OE) switch/detector.

The InGaAs MSM OE switch consists of InAlAs/InGaAs lattice-matched layers grown by molecular beam epitaxy (M.BE) on top of a semi-insulating InP:Fe substrate. The layer structure consists of a 3000 Å InAlAs buffer layer grown on top of the substrate, followed by a 1.0 μm InGaAs active layer, a 150 Å In(Ga,Al)As graded layer, and finally a 500 Å InAlAs Schottky barrier enhancement layer. The metal was deposited via e-beam evaporation and consists of 500 Å/4000 Å Ti/Au. The active area of the InGaAs MSM OE switch is $60 \times 60 \mu\text{m}^2$.

The experimental set-up utilized to test the MSM OE switch consists of a Ti:Sapphire laser-pumped optical parametric oscillator delivering 100-fs, 76-MHz, 3-nJ tunable, 1.3-1.55 μm optical pulses, a 40 GHz digital sampling oscilloscope (DSO) and a fully-adjustable probe station utilizing a 40 GHz ground-signal-ground microwave probe. A DC bias is applied to the InGaAs MSM OE switch via a short transmission line (with a 50 Ω termination). Laser light focused on the switch will change its conductivity and the resulting voltage output will appear, via another transmission line, on the 50-Ω 40 GHz DSO (triggered via the laser).

In Figures 4-7 and 4-8 we show two examples of the pulse response obtained for an incident optical pulse energy of 22.4 pJ. In Figure 4-7 the applied bias is 4 V while in figure 4-8 it is 5 V. The measured peak current increases with increase in applied bias yielding values of 16.6 mA and 22.2 mA for 4 V and 5 V, respectively. Parameters

relevant to the SSC-SD project are listed in Table 4-II. Also listed in Table 4-II are the desired pulse responses for the SSC-SD Optically Clocked Track and Hold Project provided by Bill Jacobs of SPAWAR. These two examples of the pulse response were chosen to show that the requirements of the detector for the SSC-SD project listed above do not differ very much from the parameters listed in Table 4-II. We find this to be quite encouraging. Note that the devices tested here do not employ an anti-reflection coating. The addition of an anti-reflection coating will reduce the required optical energy from 22.4 pJ to 15.7 pJ.

The full width at half maximum (FWHM) and fall time (90%-10%) as a function of both optical pulse energy and applied bias are plotted in Figures 4-9 and 4-10 respectively. Here we see that both the FWHM and the fall time increase with increase in optical pulse energy and decrease with increase in bias voltage. The increase in fall time with increase in optical pulse energy is attributed to a decrease in the hole-drift velocity due to screening of the dark electric field by optically generated carriers [121]. The increase in FWHM with increase in optical energy is attributed to a decrease in the electron-drift velocity [121].

In Figure 4-11, the peak current of the MSM OE switch is plotted as a function of both optical pulse energy and bias voltage. In figures 4-12 and 4-13 we plot the time it takes the OE switch to reach dark current (i.e., when the current is less than 3 mA) and the time at which the switch is at a current of 5 mA above dark current. Both of these parameters are important for the track-and-hold project. Finally, in Figure 4-14, we plot the rise time (10%-90%) of the pulse response as a function of DC bias voltage for

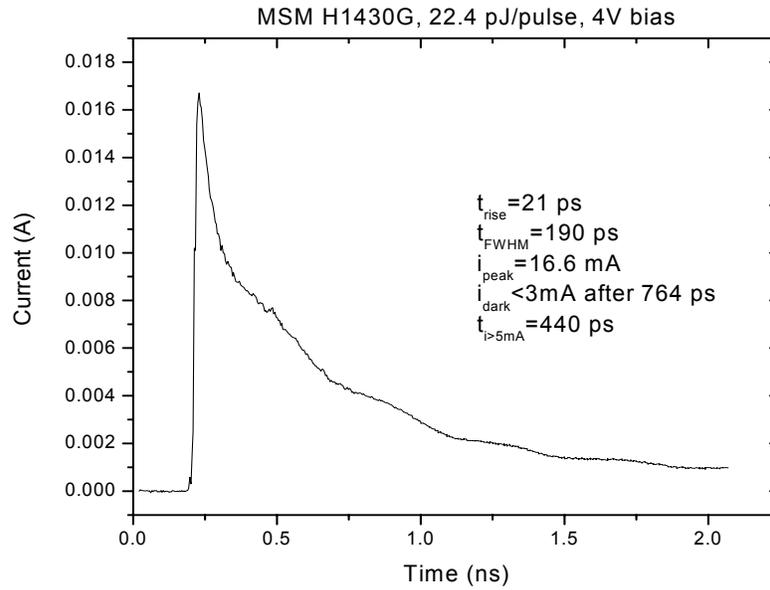


Figure 4-7. The output current of the optical switch for a pulse energy of 22.4 pJ and a bias of 4 V

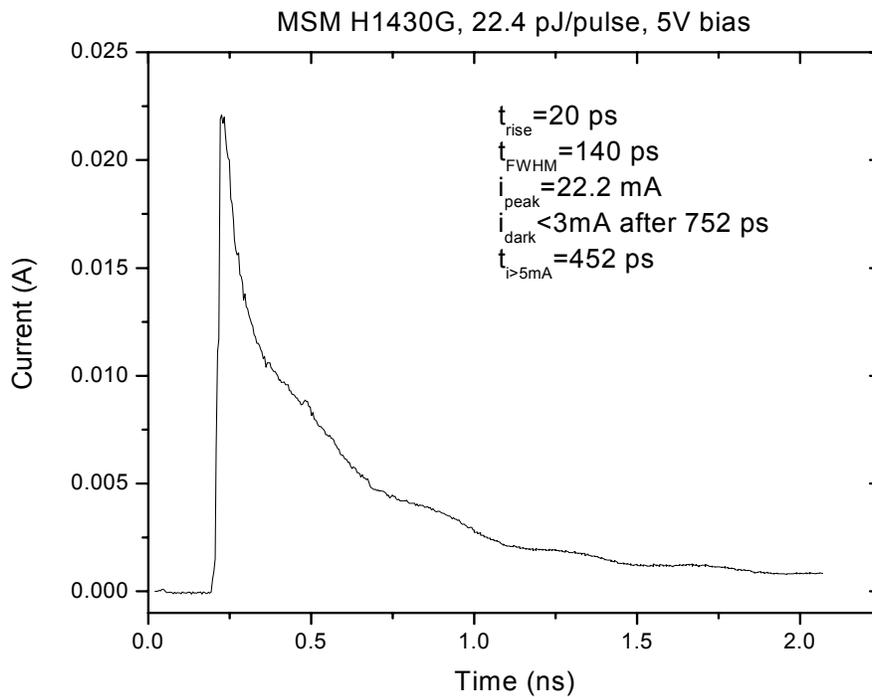


Figure 4-8. The output current of the optical switch for a pulse energy of 22.4 pJ and a bias of 5 V

Table 4-2. Relevant parameters for the SSC-SD track-and-hold project

	SSC-SD Requirements	Device under test:H1430G, 4-V bias	Device under test:H1430G, 5-V bias
Peak current (mA)	>20	16.6	22.2
FWHM (ps)	~150-250	190	140
Rise time (ps)	~20	21	20
Time idark<3 mA (ps)	~600	764	752
Time i>5 mA (ps)	~300-400	440	452
Capacitance (fF)	<80	70fF@0V*	70fF@0V*
Optical energy (pJ)	~17	22.4	22.4

* Measured on a similar device

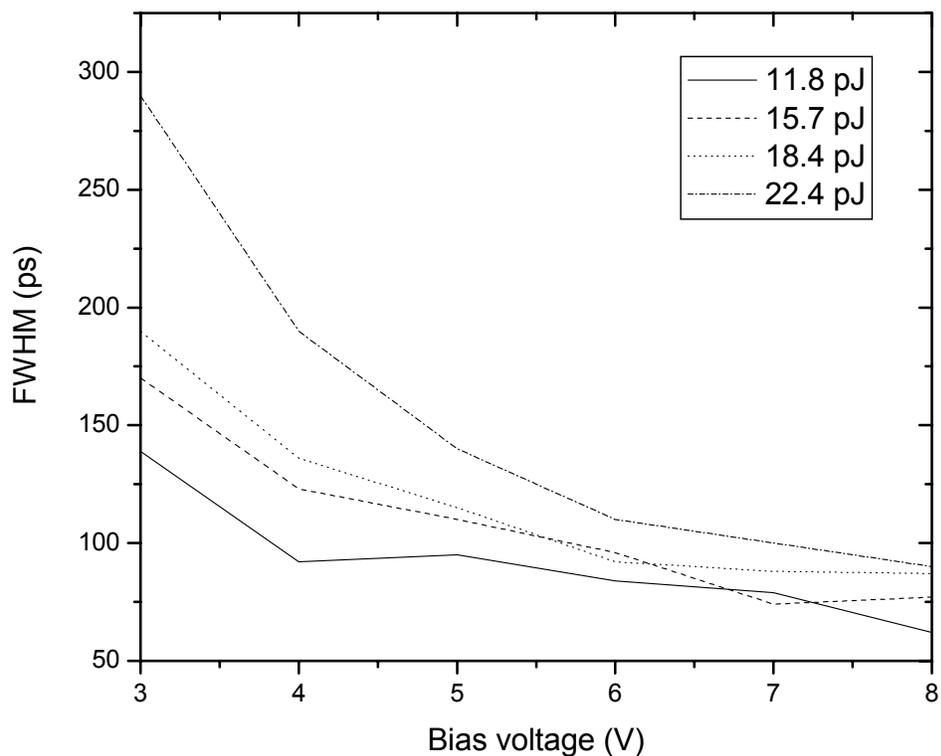


Figure 4-9. The FWHM of the optical switch as a function of DC bias voltage and optical power

various incident optical pulse energies. This rise time data is in the vicinity of the required rise time of the track-and-hold project.

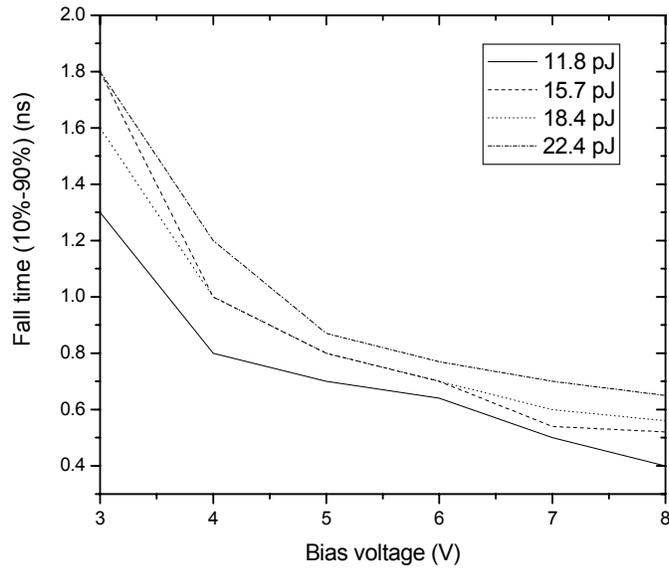


Figure 4-10. The fall-time of the optical switch as a function of DC bias voltage and optical power

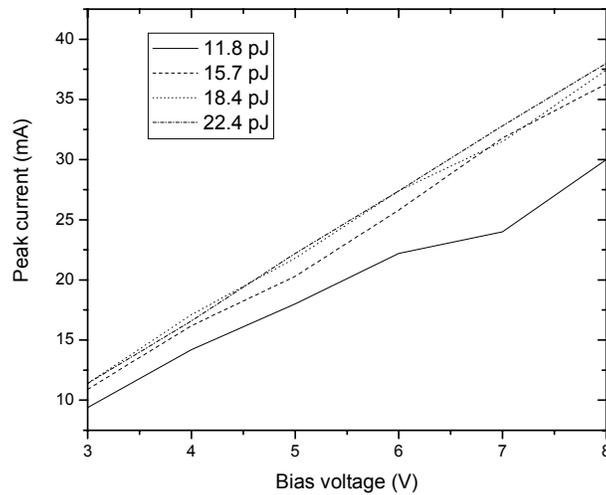


Figure 4-11. Peak current of the InGaAs OE switch as a function of optical pulse energy and applied DC bias

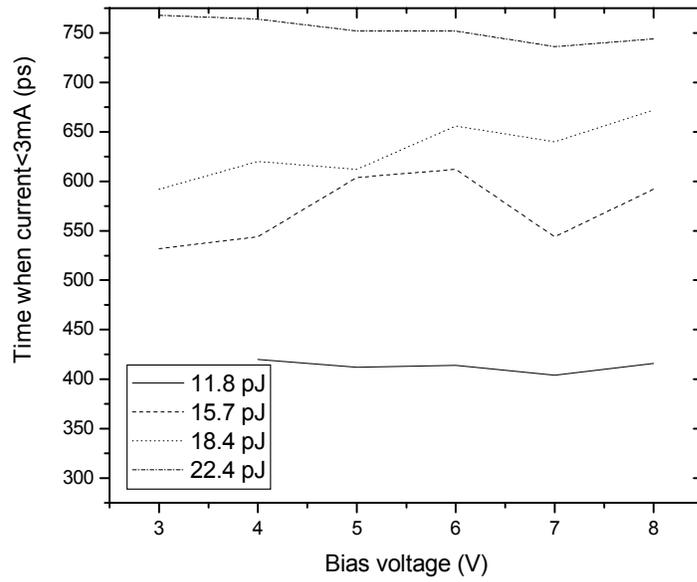


Figure 4-12. Time it takes the current to decrease below 3 mA as a function of DC bias voltage and optical pulse energy

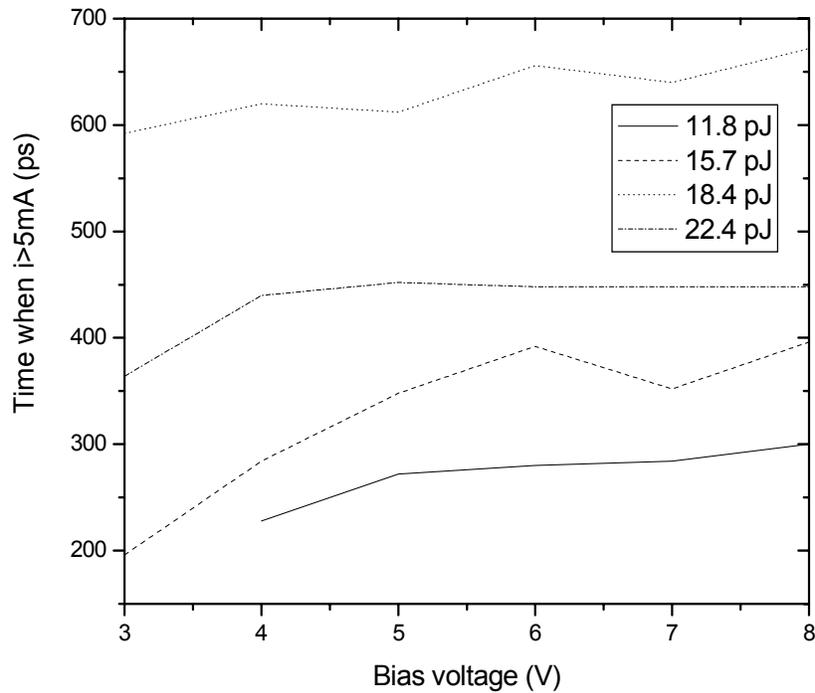


Figure 4-13. Time at which the current reaches 5 mA above dark current as a function of DC bias voltage and optical pulse energy

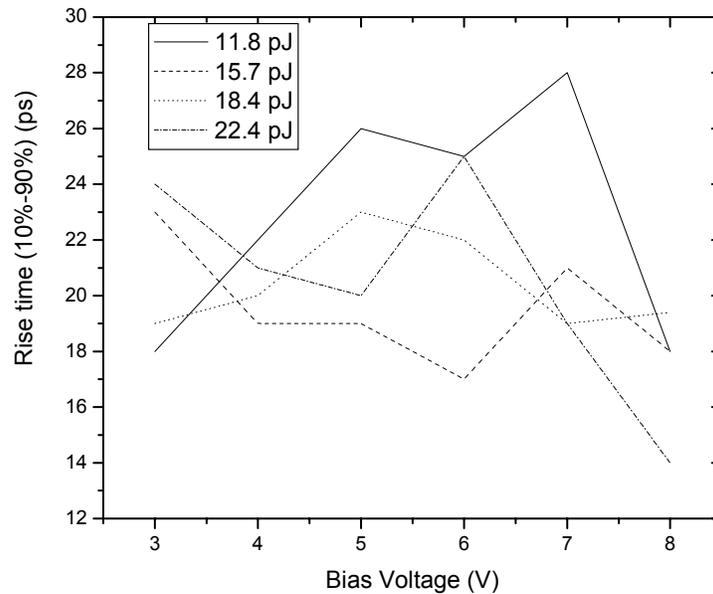


Figure 4-14. Rise time as a function of DC bias voltage and optical pulse energy

Analysis of the Mixing Effect in InAlAs/InGaAs Metal-Semiconductor-Metal Photodetectors

Optoelectronic Mixers

Mixing characteristics were measured with light from an amplitude-modulated 1.55 μm , 10 Gb/s, fiber-pigtailed laser. Optical power was adjusted via a continuously-variable, in-line, fiber-coupled attenuator. The LO bias was applied to one electrode, shunted with a 50 ohm termination, and the mixed signal was recovered from the other electrode, which was connected to a spectrum analyzer through a low-pass filter.

Photocurrent and Mixing Efficiency

In Fig. 4-15 we plot the IV characteristics of the MSMPD for optical powers of 7.0 μW and 0.722 mW. Both curves exhibit a region where dI/dV transitions from a low value to a high value: this is referred to as a “knee”. InGaAs MSMPDs without SELs do not have knee-like features. The knee voltage is defined as the bias voltage where the

photocurrent equals 5% of the value at the second region, where dI/dV is low. The inset of Fig. 1 shows the knee voltage as a function of the log of optical power.

We define the mixing efficiency (M_{eff}) as the ratio of the responsivity of the detector at the IF frequency to its DC responsivity at the DC bias voltage equal to the RMS value of the ac voltage. Fig. 4-16 (a) shows M_{eff} as a function of laser modulation frequency for optical powers of 4.0-170 μW . The modulation and LO frequencies were displaced by 10.0 KHz. M_{eff} is less than the theoretical value of 0.5 at low LO frequency and cuts off at about 0.1 GHz. Moreover, M_{eff} is optical power dependent: it increases with optical power and reaches the theoretical value at high optical powers. When the

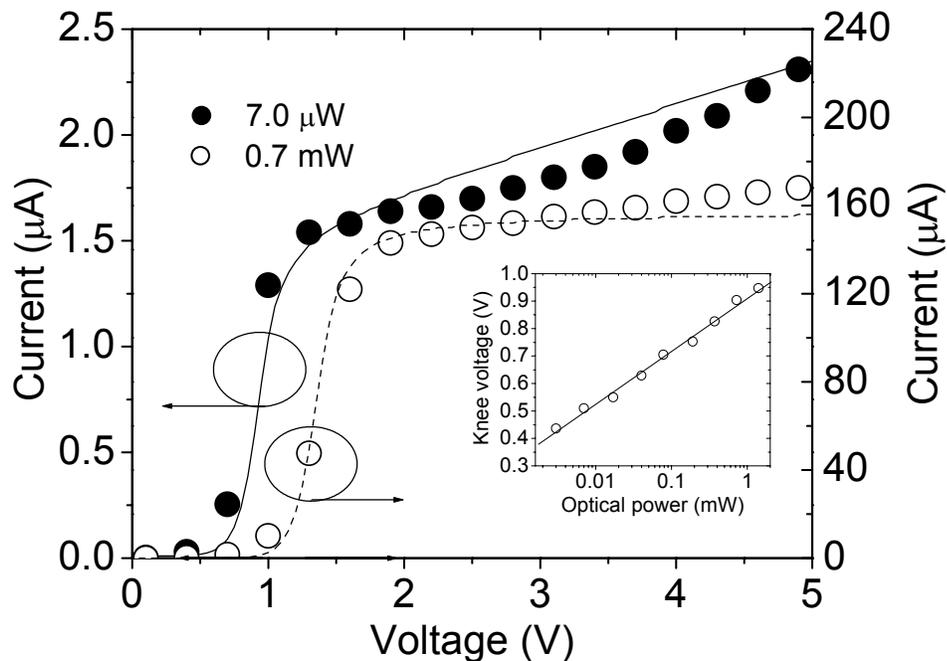


Figure 4-15. IV characteristics of InAlAs/InGaAs MSM for optical powers of 7.0 μW (solid circles) and 0.722 mW (open circles). Inset shows the knee voltage as a function of the log of optical power

same device is operated as a photodetector it has a flat frequency response with a 3.0 dB cut off at 3.0 GHz. In addition, the responsivity is independent of optical power except for powers above 4.0 mW where screening causes a slight decrease

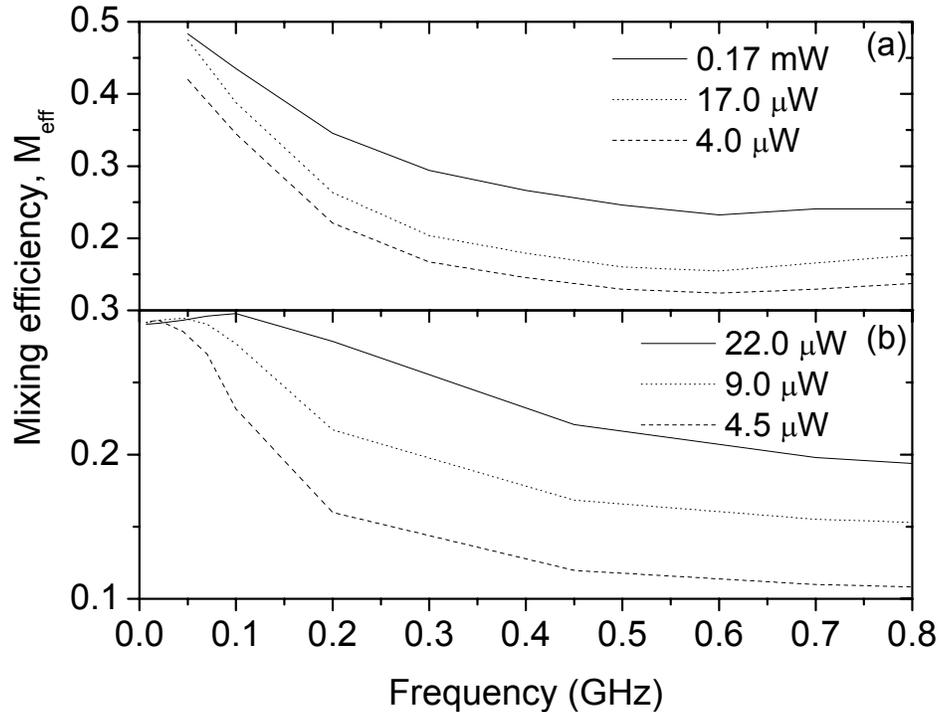


Figure 4-16. (a) Experimental and (b) simulated M_{eff} vs. laser modulation frequency as a function of optical power

Figure 4-17 (a) shows M_{eff} as a function of IF frequency for optical powers of 17.0-140 μW . Here, the modulation frequency was at 500 MHz, while the LO frequency was varied from 500-715 MHz, yielding IF frequencies from 0-215 MHz. M_{eff} is flat with IF frequency to 10-30 MHz beyond which an increase occurs. At low IF frequencies, M_{eff} decreases as optical power decreases, while at high IF frequencies it approaches its theoretical value. We have compared the sum frequency with the difference frequency signal and found that the sum signal is independent of optical power and is larger than the difference signal (M_{eff} of sum signal ≈ 0.5). We would expect that, since the difference

signal is at low frequency, an OE mixer would work better than or equal to a photodetector. Because this is true experimentally [129] and theoretically [130] for GaAs-based MSMPDs, but not for InAlAs/InGaAs-based MSMPDs indicates that low frequency signals are limited by some circuit component in the device.

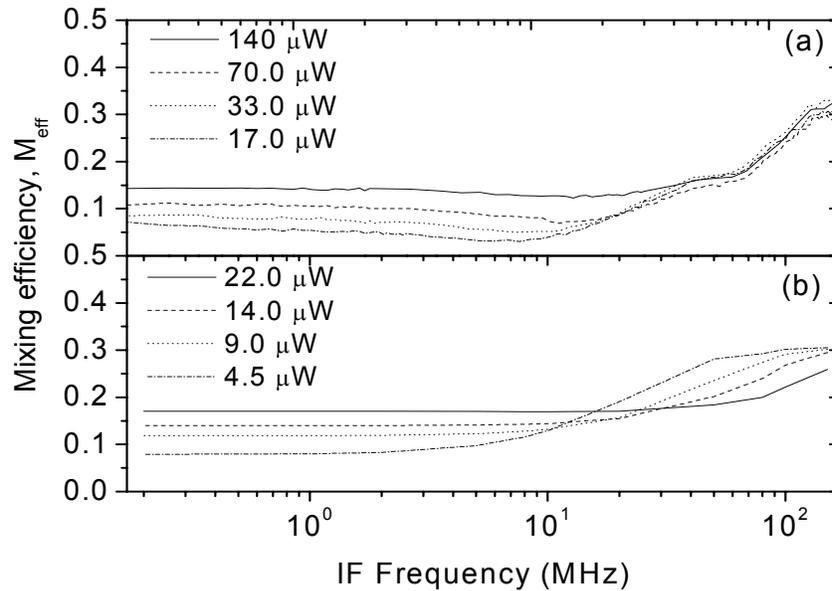


Figure 4-17. (a) Experimental and (b) simulated M_{eff} vs. IF frequency as a function of optical power

1-Dimensional Model of Mixer

The knee in the IV curve has been reported in the literature [4], [6], [131] and is usually attributed to the complete depletion of the InGaAs absorption layer. The relationship of optical power to knee voltage is usually attributed to interface trap states or space charges [6], [131]. The lack of a knee in the IV characteristics of InGaAs MSMPDs without SELs, however, may indicate that the knee is related to the SEL. Furthermore, the logarithmic relation between knee voltage and optical power (inset, Fig. 1) strongly suggests a thermionic emission and/or tunneling related process.

Using a 1-D drift-diffusion model to simulate InGaAs MSMs with SELs, we find a knee in the IV characteristics that is dependent on optical power. Fig.18A shows the 1-D band diagram (not to scale). 2-D electron and hole gases exist at the InGaAs/InAlAs interface near the anode and cathode, respectively. The density of the 2-D electron gas is much higher than the 2-D hole gas, indicating that the electron current is limited more than the hole current. Furthermore, we find that most of the bias voltage is dropped across the InAlAs layer near the anode.

To understand the mixing physics, we divide the device into three regions (see Fig 4-18 (a)). Regions A and C include the contact metal, the InAlAs SEL, and the InAlAs/InGaAs interface. The InGaAs absorption layer is included in region B. When the bias voltage is above flat band, the electric field in each layer is uniform, except for small band bending at the location of the 2-D gas. In region B, the generated photocurrent is given by

$$I_{ph} = \frac{g}{g+w} (1-R)(1-e^{-\alpha d}) \frac{\eta q}{h\nu} P \quad (4-2)$$

where g is the inter-digitated spacing, w is the finger width, R is the reflectivity, α is the absorption coefficient, d is the InGaAs thickness, η is the internal quantum efficiency, $h\nu$ is the photon energy, and P is the incident optical power. Photo-generated electrons move toward the anode, while holes move toward the cathode. Under low bias, the electron and hole currents are limited by the potential barriers at the heterointerface. Therefore, some of the photo-generated carriers will recombine before the electrons and holes are completely separated. Since the field in region B is uniform, we can calculate the drift time for electrons and write the current in this region as

$$I_B(V_B) = I_{ph} e^{-t/\tau} = I_{ph} e^{-d^2/2\mu V_B \tau} \quad (4-3)$$

where t is the average transient time for electrons, μ is the electron mobility, V_B is the voltage drop in region B and τ is the recombination lifetime. In regions A and C light is not absorbed, and the current is due to thermionic emission and/or tunneling. Under positive (negative) bias, the electron (hole) current will dominate. The hole current is limited by the valence band offset V_h while the electron current is limited by the Schottky barrier height V_{sh} and the conduction-band offset V_e . Since there are many electron states in the 500 Å SEL, the major barrier for electrons is the Schottky barrier.

Therefore we can write the current in region A as

$$I_A = \begin{cases} A_{el}^* T^2 e^{-eV_{sh}/kT} (e^{eV_A/n_{el}kT} - 1) & V_A > 0 \\ -A_{hole}^* T^2 e^{-eV_h/kT} (e^{-eV_A/n_{hole}kT} - 1) & V_A < 0 \end{cases} \quad (4-4)$$

where A_{el}^* and A_{hole}^* are the effective Richardson constants for electrons and holes, respectively, V_A is the voltage drop across region A, k is the Boltzmann constant, T is the device temperature, and n_{el} and n_{hole} are the ideality factors for electrons and holes, respectively. Similar equations can be given for the current in region C.

Fig. 4-18 (b) is a circuit model of the OE mixer. The diodes $D_{A_{el}}$ and $D_{A_{hole}}$ model, respectively, the electron and hole currents in region A. Region C is similarly modeled. Eq. (4-2) is represented by the current source in region B, and the dark current is modeled by a resistor R equal to dI/dV at large bias. The drop of the valence band barrier is only 1/3 of the total voltage across region A (or C) due to the 250 Å In(Ga,Al)As graded layer. Therefore, we let $n_{hole} = 3$. The internal quantum efficiency η and the ideality factor for electrons n_{el} are extracted from the IV curves as two free parameters. All other parameters

can be found in the literature. Using these values, with $\eta=100\%$ and $n_{el}=3.5$, the simulated IV curves are shown in Fig. 4-15, by solid and dashed lines, for optical powers of $7.0 \mu\text{W}$, and 0.7 mW , respectively.

We have also used parameters extracted from the DC IV curves to calculate M_{eff} . We add two capacitors ($C_A=C_C$) to the circuit for SELs and neglect the capacitance of region B. Due to the 2-D nature of the device, the values of $C_{A,C}$ are difficult to determine. The capacitance for the whole device, calculated using the conformal mapping technique, is 7.0 fF . We use 10.0 fF in our simulation. Figs. 2B and 3B show M_{eff} as a function of laser modulation and IF frequencies, respectively, for optical powers of $4.5\text{-}22.0 \mu\text{W}$. Considering that our model is 1-D, and that parasitic components are not included, the agreement with the experimental results is good. When the device is simulated as a photodetector (i.e., DC bias only), the cut-off frequency is much higher

Figure 4-18. a) 1-D band diagram of Schottky enhanced InGaAs-based MSM. b) Circuit model of the MSM OE mixer

and independent of optical power. The results can be explained as follows. When operated as a photodetector, the voltage drop across the SEL (V_A/V_B) is high, the differential resistance is low, and the detector responsivity is unaffected. When operated as an OE mixer, the high frequency LO bias on the SEL drops with frequency because of the shunt capacitance. For high frequencies, V_A/V_B is small and the differential resistance of the diodes is larger than in region B, therefore reducing the IF signal. However, increasingly higher IF signals are passed through the two capacitors, and M_{eff} increases to the limit of 0.5. For this same reason, the sum signal is always larger than the difference signal. In the low IF region, the only signal path is through the two diodes. As optical power increases, the differential resistance of the absorption region decreases, and V_A/V_B increases. As a result, M_{eff} increases with optical power.

M_{eff} can be improved with the following: decrease the capacitance of the InAlAs layer by reducing the inter-digitated finger width; reduce the ideality factor and enhance the tunneling process by reducing the ratio between the InAlAs layer and the graded layer; and reduce the band discontinuity by changing the SEL material.

Improving Performance of the OE Mixer

Schottky-enhanced InGaAs-based MSM-PDs do not operate well as OEMs. In particular, it was shown that the frequency bandwidth of such a mixer is much less than that of a corresponding photodetector. In addition, the mixing responsivity of the OEM was found to depend on the RF and LO signals and decreased non-linearly with decrease in optical power. The behavior of the InGaAs-based MSM-PD OEM was attributed to the large band-gap discontinuity associated with the SEL. One possible way to improve the mixing responsivity is to reduce the ideality factor and enhance tunneling in the MSM-

PD OEM. This may be achieved, for example, by reducing the ratio between the InAlAs SEL and the InGaAs active layer (or graded layer, if utilized).

Devices with two different SEL thickness were fabricated. We compare the mixing characteristics of a conventional InAlAs Schottky-enhanced InGaAs MSM-PD (SEL thickness of 500 Å) to that of an InAlAs Schottky-enhanced InGaAs MSM-PD OEM with a thin SEL (100 Å). For the thin SEL, the mixing characteristics are found to improve: The bandwidth of the optoelectronic mixer is similar to that of a corresponding photodetector and the mixing response de-creases only slightly with decrease in optical power. These results represent the first report of efficient optoelectronic mixing in InGaAs-based MSM-PDs.

In Figure 4-19, the responsivity of a 500-Å InAlAs Schottky-enhanced InGaAs MSM-PD (DC bias, RF light modulation) is compared to the responsivity of the same MSM-PD when operating as an OEM (LO bias, RF light modulation). Notice that the RF

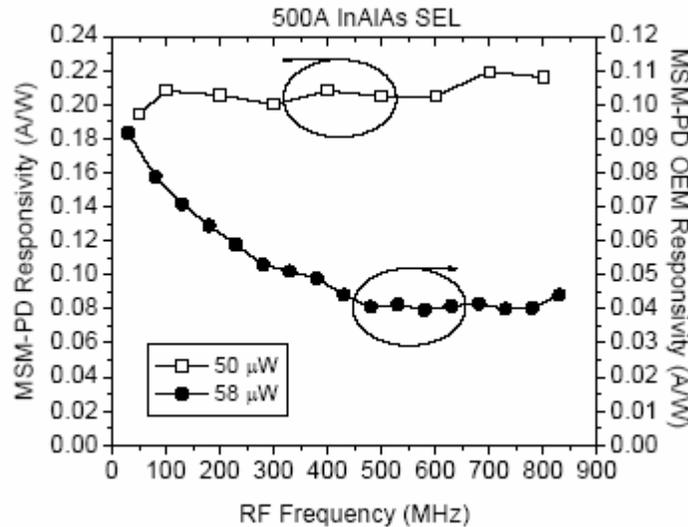


Figure 4-19. Responsivity of a MSM-PD (DC bias, RF light modulation) compared with the responsivity of a MSM-PD OEM (LO bias, RF modulation), as a function of RF frequency, for an InAlAs Schottky-enhanced device with a 500 Å thick SEL

bandwidth of the MSM-PD OEM is much less than the RF bandwidth of the MSM-PD.

To compare the behavior of MSM-PD OEMs with differing geometries and device structures, it is convenient to define a “mixing efficiency” (M_{eff}). We define M_{eff} as the ratio of the responsivity of the MSM-PD OEM at the IF (mixed signal) frequency to its ideal DC responsivity. Figure 4-20 compares M_{eff} , as a function of RF frequency, for 100 Å and 500 Å thick InAlAs Schottky-enhanced MSM-PD OEMs. There is a marked improvement in M_{eff} for the 100-Å MSM-PD OEM. In addition, the bandwidth of the 100 Å MSM-PD OEM is >1.0 GHz while the bandwidth of the 500 Å MSM-PD OEM is <200 MHz.

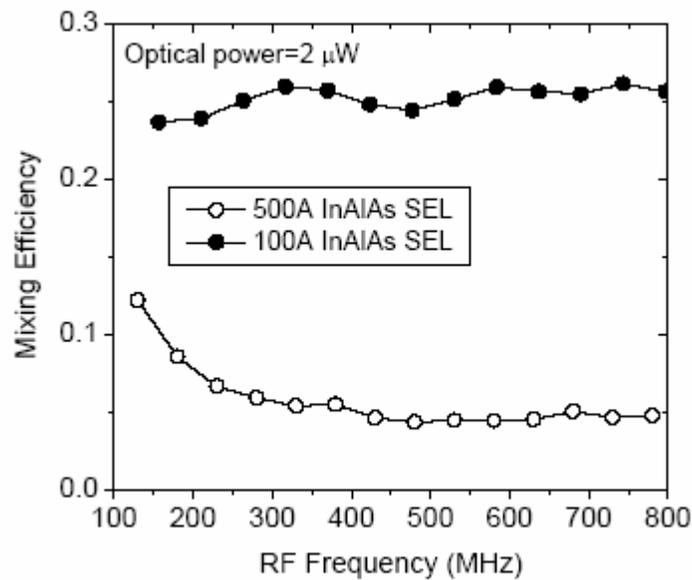


Figure 4-20. Mixing efficiency, as a function of RF frequency, of an InAlAs Schottky-enhanced MSM-PD OEM with a 100 Å SEL (solid circles) compared with the mixing efficiency of an InAlAs Schottky-enhanced MSM-PD OEM with a 500 Å SEL (open circles)

Figure 4-21 shows M_{eff} as a function of IF frequency for the 100 Å and 500 Å InAlAs Schottky-enhanced MSM-PD OEMs for two different optical powers. Here, the RF light modulation was set to 500 MHz while the LO was varied from 500-700 MHz.

This yields IF frequencies from 0 to 200 MHz. For the 500 Å SEL, M_{eff} is flat to 30 MHz, beyond which an increase occurs. At low IF frequencies, M_{eff} decreases as optical power decreases, while at high IF frequencies it approaches the calculated value of 0.5. At low IF frequencies we would expect the MSM-PD OEM to work better than or equal to a MSM-PD. This is true, experimentally and theoretically, for GaAs-based MSM-PD OEMs. The fact that this is not true for the 500 Å SEL In-GaAs MSM-PD OEM indicates that low-frequency signals are limited by some circuit component in the device. Decreasing the SEL thickness to 100 Å improves M_{eff} from 0.07 to 0.3. In addition, M_{eff} of the 100 Å MSM-PD OEM is flat for both low and high IF frequencies and does not vary with optical power.

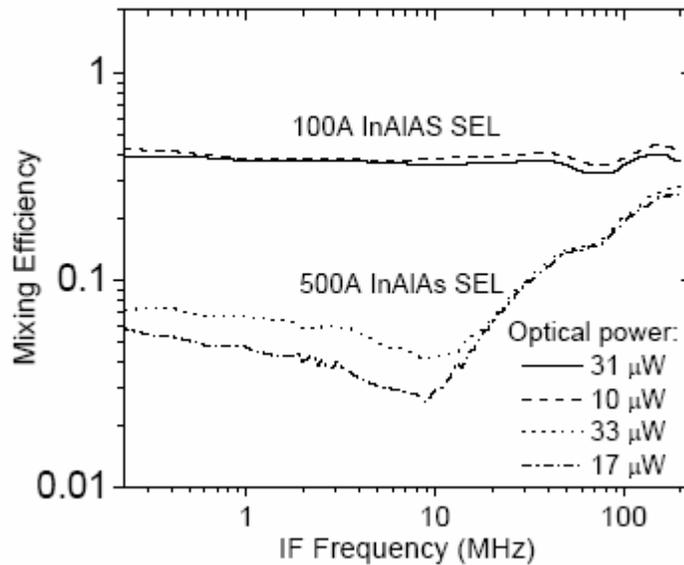


Figure 4-21. Mixing efficiency, as a function of IF frequency, of an InAlAs Schottky-enhanced MSM-PD OEM with a 100 Å SEL compared with the mixing efficiency of an InAlAs Schottky-enhanced MSM-PD OEM with a 500 Å SEL for two different optical powers

Figure 4-22 shows M_{eff} , as a function of optical power, for 100 Å and 500 Å InAlAs Schottky-enhanced MSM-PD OEMs. Here, the RF light modulation is set to

500 MHz and the LO bias frequency is set to 510 MHz (i.e., the IF frequency is at 10.0 kHz). M_{eff} for the 500 Å SEL is very low and decreases significantly (and non-linearly) with decrease in optical power. M_{eff} for the 100 Å SEL only slightly decreases with optical power.

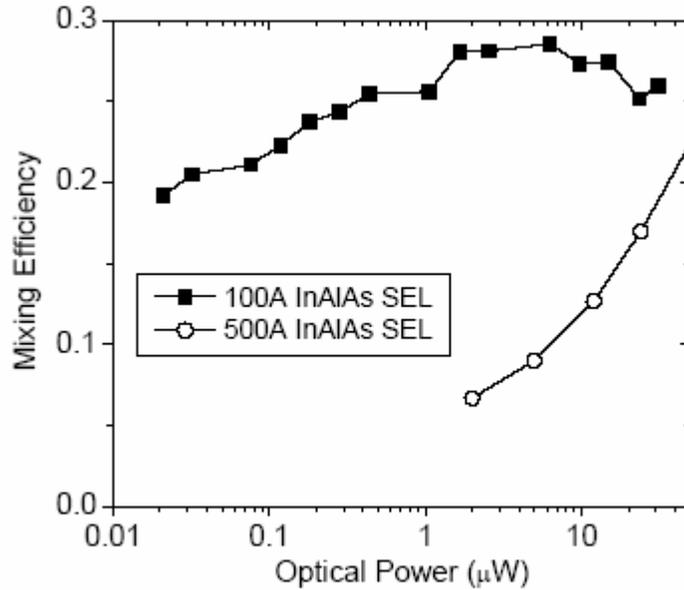


Figure 4-22. Mixing efficiency, as a function of optical power, of an InAlAs Schottky-enhanced MSM-PD OEM with a 100 Å SEL compared with the mixing efficiency of an InAlAs Schottky-enhanced MSM-PD OEM with a 500 Å SEL

To better understand the observed results it is advantageous to model the MSM-PD OEM via the circuit diagram shown in Figure 4-18(b) (Figure 4-18(a) is the band diagram of the MSM-PD OEM). We let diodes D_{Ae} and D_{Ah} model, respectively, the electron and hole currents in region A. Region C is similarly modeled by D_{Ce} and D_{Ch} . We place a current source in region B and model the dark current by a resistor R , equal to dV/dI at large bias. The two capacitors ($C_A=C_C$) in the circuit represent the SELs (the capacitance of region B is neglected).

When operated as a photodetector, there is a significant voltage drop across the SEL and, hence, the differential resistance of the forward-biased diode is low. For a MSM-PD, current is limited by the forward-biased diode [130]. Therefore, as shown in Figure 4-19, the responsivity of the MSM-PD is unaffected by the SEL, i.e., the current is not limited due to the fact that there is a SEL present. When operated as an OEM, however, there is now a LO bias on the SEL. The SEL acts like a capacitor and, hence, the LO bias is now frequency dependent. The capacitance effectively reduces the LO bias across the two diodes as the LO frequency increases. As a result, the differential resistance of the diodes increases thereby limiting the current. This is shown in Figure 20, where M_{eff} decreases with increase in LO (or RF) frequency for the thick SEL but not for the thin SEL. The behavior of M_{eff} for the thick SEL is especially low for low IF frequencies (see Figure 4-21) because the only signal path for the current is through the diodes. Increasingly higher IF signals pass through capacitors and, hence, M_{eff} increases with increase in IF frequency. As optical power increases, the differential resistance of the absorption region decreases and the differential resistance of the diodes decreases. As a result, M_{eff} increases with optical power (see Figure 4-22). As discussed earlier, the ideality factors of the diodes are proportional to the thickness of the SEL. MSM-PDs with thinner SELs have smaller ideality factors and, thus, a lower differential resistance than MSM-PDs with thick SELs. These factors led to the improvement in the mixing efficiency of the Schottky-enhanced MSM-PD OEM.

2 – Dimensional Simulation of Pulse Response, DC Light Response and Mixing Characteristics of Schottky Barrier Enhanced InGaAs MSM Photodetectors and OE Mixers

An understanding of device physics and accurate modeling of devices would help to develop better devices. With this motivation in mind finite volume modeling of MSM photodetectors and OE mixers was performed using CFD-ACE+ SEMI module. InGaAs MSM photodetectors with InAlAs Schottky Enhancement Layer (SEL) with very low dark current has already been demonstrated [119-120, 132-134]. First use of InGaAs MSM photodetectors as OE mixers utilizing InAlAs as Schottky Enhancement Layer (SEL) has already been demonstrated [135]. In this work Finite Volume based simulations were carried out for transient and DC response of the MSM photodetector and the results are compared with experimental ones. A close agreement between the two was observed.

Material Properties

Several devices with different SEL thickness and different dimensions were made. The simulations were performed for $60 \mu\text{m}^2$ devices with $3 \mu\text{m}$ finger width and $3 \mu\text{m}$ spacing. Using the existing MSM-photodetector tutorial as the starting point, modification in the template files and the python scripts were carried out to accomplish the goals of the project.

Since, the material system under consideration was different from one in CFDRC tutorial (GaAs), material properties in the database were checked first. The values for mobility for InGaAs and InAlAs were quite off since $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ values were derived from $\text{In}_{1-x}\text{Ga}_x\text{As}_y\text{P}_{1-y}$, and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ mobility values were derived from taking mole fraction average between mobility values of InAs and AlAs. It was found that such an

approximation for mobility was highly erroneous and it was replaced with more reasonable data [136].

For semiconductor alloys, *Matthiesen* rule can be used to determine the mobility of the alloy from that of constituent semiconductors.

$$\frac{1}{\mu^{AB}} = \frac{x}{\mu^A} + \frac{1-x}{\mu^B} + \frac{x(1-x)}{C_\mu} \quad (4-5)$$

where μ and x are mobility and mole fraction of corresponding species and C_μ is the bowing parameter. For n – type material, two – valley bowing parameter has to be used, whereas for p-type material one – valley bowing parameter could be used.

New mobility model for InAlAs was incorporated in the solver and used. For InGaAs a constant mobility model was used with electron mobility = 12000 cm²/V-s and hole mobility = 300 cm²/V-s. These values were obtained from the NSM webpage [137].

Constant recombination life times were used for both the materials. For InAlAs, $\tau_{\text{electron}} = 1 \times 10^{-9}$ s, $\tau_{\text{hole}} = 2 \times 10^{-8}$ s, and for InGaAs, $\tau_{\text{electron}} = 1 \times 10^{-9}$ s, $\tau_{\text{hole}} = 1 \times 10^{-9}$ s were used. All other properties were used from the CFD-ACE-SOLVER database.

Electromagnetic Simulation

Maxwell's equation can be reduced to the following equation

$$\frac{1}{\mu_0 \mu_r} \nabla^2 \vec{A} = \epsilon_0 \epsilon_r \frac{\partial^2 \vec{A}}{\partial t^2} + \epsilon_0 \epsilon_r \frac{\partial \nabla \phi}{\partial t} + \sigma \frac{\partial \vec{A}}{\partial t} + \sigma \nabla \phi - \sigma (\vec{u} \times \vec{B}) - \vec{J}_s \quad (4-7)$$

where \vec{A} is the vector magnetic potential, ϕ the electrostatic potential, \vec{B} the external magnetic field, \vec{u} the velocity of carriers, \vec{J}_s the current from any other source, μ_0 , μ_r are the permeability of free space and relative permeability of the semiconductor respectively, ϵ_0 , ϵ_r are the permittivity of free space and relative permittivity of the semiconductor respectively, σ the conductivity of semiconductor.

The equation is solved for vector magnetic potential, \vec{A} and electrostatic potential ϕ . Convective Current source is zero due to lack of any external Magnetic field in Z-direction. Light intensity I is given by the modulus of pointing vector, hence it can be seen that

$$I = |\vec{S}| \propto |\vec{A}|^2 \quad (4-8)$$

where \vec{S} is the pointing vector given by

$$\vec{S} = \frac{1}{\mu} \vec{E} \times \vec{B} \quad (4-9)$$

where \vec{E} is the electric field.

To define the boundary condition for the simulation, light intensity, I is used to calculate the magnitude of vector magnetic potential, \vec{A} at the surface, where it is varying in a sinusoidal manner. Inside the semiconductor, the power dissipation in each node can be found by taking the divergence of pointing vector. This term can be used to calculate the number of carriers generated in the semiconductor due to fundamental absorption process. Thus the semiconductor equations can be solved with the generation term G in the continuity equation calculated as above. The continuity equation is given by

$$\begin{aligned} q \frac{\partial n}{\partial t} - \nabla \cdot \vec{J}_n &= q(G - R) \\ q \frac{\partial p}{\partial t} + \nabla \cdot \vec{J}_p &= q(G - R) \end{aligned} \quad (4-10)$$

where \vec{J}_n and \vec{J}_p are current electron and hole current densities respectively, n and p the electron and hole densities respectively, q the electronic charge, G the generation rate of carriers and R the recombination rate of carriers.

Python Script Modification

CFDRC has developed python script [138] for data flow management and control of coupled electromagnetic optics/semiconductor physics simulation of MSM photodetector. The script has been modified to include an extra layer in the original MSM – photo detector simulation. The grid spacing was also changed to account for thin width of the incorporated layer. Template files for the optical, steady state and transient simulation were modified to include boundary and volume conditions for the included layer. To create new template file, the Python script was run to create a GEOM (GGD) file, using which template DTF files were created and boundary and volume conditions were manually assigned to these files.

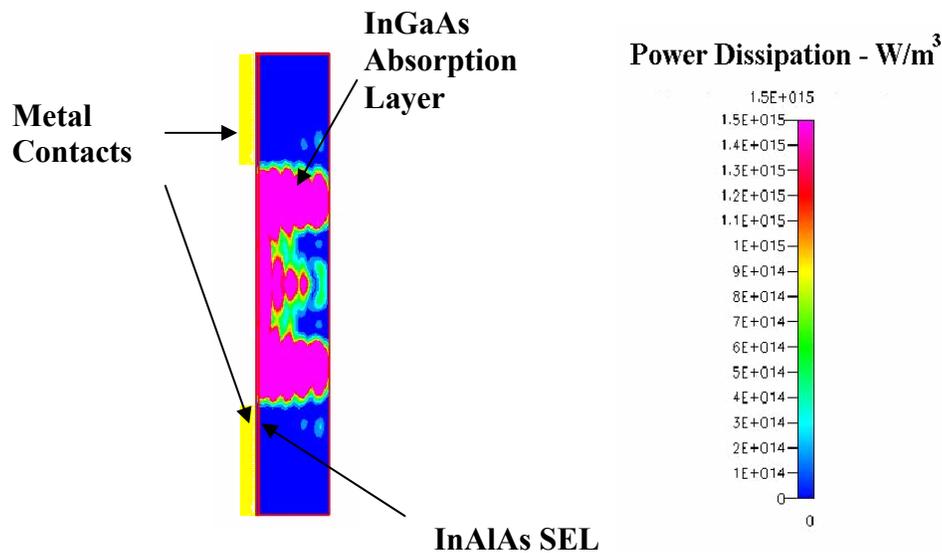


Figure 4-23. Power dissipation in the semiconductor at the end of CFD-ACE+ EMAG simulation

Pulsed Response

Modification of time period

Spatial distribution of the carrier photogeneration rate was calculated using CFD-ACE+ EMAG electromagnetic solver, and then it was used for transient CFD-ACE+

SEMI semiconductor simulations. Figure 4-23 shows the spatial distribution of optical power dissipation, which was fed into the CFD-ACE+ SEMI module. Figure 4-25 shows the electron and hole distribution just after the end of the light pulse and at two other time intervals from the removal of light pulse. It can be seen that electron and hole distributions follow the power dissipation profile very closely. After the light pulse was switched off the carriers were swept away by the bias and they were also terminated due to recombination.

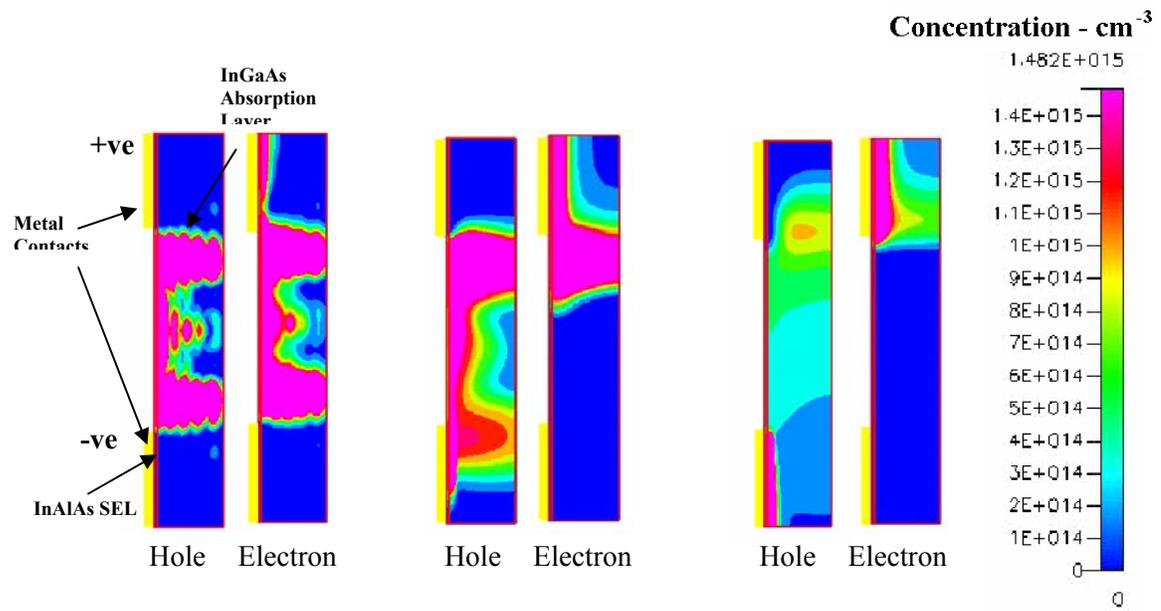


Figure 4-24. Electron and hole distributions at the end of the (a) 100 fs long light pulse (b) after 5 ps from removal of light pulse (c) after 215 ps from removal of light pulse

Original photo-detector simulation had the light pulse on for sufficient period of time (10 ps) and then it was switched off. This methodology could not be used for the transient simulation of the InGaAs MSM detector, due to short time period of the pulse (100 fs), which was incident on the detector. Instead, the transient simulations were divided into 3 different time period zones, depending on how fast the detector was switching. During the 100 fs time when the light was on the detector, a time period of 10

fs was used, during next 10^{-10} s, a time period of 10^{-12} s was used, and finally during last 9×10^{-10} s, a time period of 10^{-11} s, was used. This could be accomplished by using parametric input option in the time step and writing the time step as this function '1E-14*STEP(10-TSTP)+1E-12*(STEP(TSTP-11)*STEP(110-TSTP))+1E-11*STEP(TSTP-111)', with a total number of time steps=200. In actual simulation, the parametric input would not accept an expression this long so the simulation was divided into two parts. The first part included time step of 10^{-14} s and 10^{-12} s, and the second part included a time step of 10^{-11} s.

Light intensity calculation

The intensity of light incident on the photo detector was calculated using the area of the light incident and its power. The power of light incident was calculated as 22.4 pJ/100 fs. Since the beam was circular in radius the light intensity was $224 \text{ W}/(\pi \times r^2)$. 50% of the incident light was reflected back due to presence of optical components. Therefore the net intensity was $122 \text{ W}/(\pi \times (30 \mu\text{m})^2) = 3.96 \times 10^{10} \text{ W/m}^2$.

The reflection at the surface was $R = \left(\frac{n-1}{n+1} \right)^2$, using $n_{\text{InAlAs}} = 3.2$, $R=27.4\%$. Therefore, a very substantial portion of the light is lost due to reflection and the actual light absorbed on the surface of the detector is very little. By using anti-reflective (AR) coating this number can be drastically reduced, since then the reflection at the surface R is given by

$$R_{\min} = \left(\frac{n_0 n_2 - n_1^2}{n_0 n_2 + n_1^2} \right)^2 \quad (4-11)$$

where n_0 is the refractive index of the air, n_1 the refractive index of AR coating, and n_2

the refractive index of the semiconductor. Using this relation the reflection R is calculated as 5.7%, which is much less than the value without AR coating.

The pulse response simulation in Figure 4-25 shows a rise – time of 14 ps, and FWHM of 44 ps. The measured data gives rise time of 20 ps, and FWHM of 140 ps. The simulated detector is faster in its response compared to the measured device.

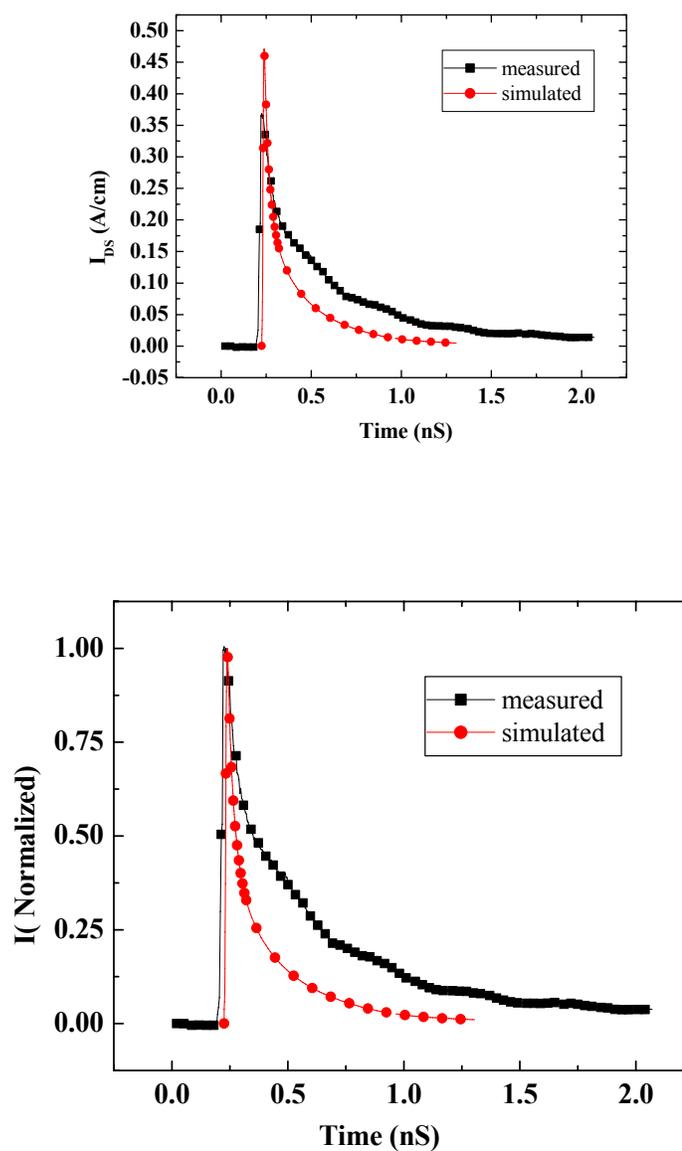


Figure 4-25. Pulsed response of MSM photo detector (a) absolute value (b) normalized

DC Response

To get the DC response of the detector, a small trick was employed since the steady state option used with photogeneration on would not converge! For example, the time step needed at the start of steady state simulation was very small in our case, since at this time the rate of change of current was very large. If the solver was not able to refine the time step such, it could result in difficulty in solver convergence. Also there is a contradiction in keeping photogeneration on for a finite period of time in steady state solver!

The simulation was setup for transient semiconductor simulation, with very long total time for photogeneration. It was seen that the current converged to a constant value after some time. When higher light intensity was simulated, time step had to be refined very much since the numbers of carriers were very large.

Figure 4-26 shows the DC response of the MSM – Photodetector when under illumination by 1.50 μm wavelength LASER. A good match between the simulated and measured I-V curves was observed. The I-V curves exhibit a region where dI/dV transitions from a low value to a high value: this is referred to as a “knee”. The “knee voltage” is defined as the bias at which the photocurrent equals 5% of the photocurrent at the second region where dI/dV is low.

As can be seen in Figure 4-27, the simulation predicts decrease in knee voltage with decrease in SEL thickness. This is what is expected, in fact, it is expected that the tunneling current will increase so much that the knee would vanish altogether. The presence of ‘knee’ is also considered responsible for poor mixing efficiency of 500 Å

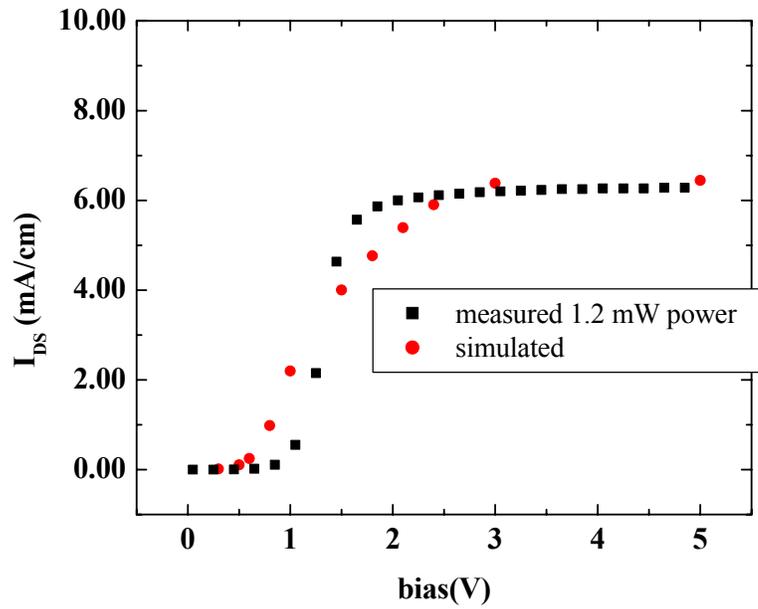
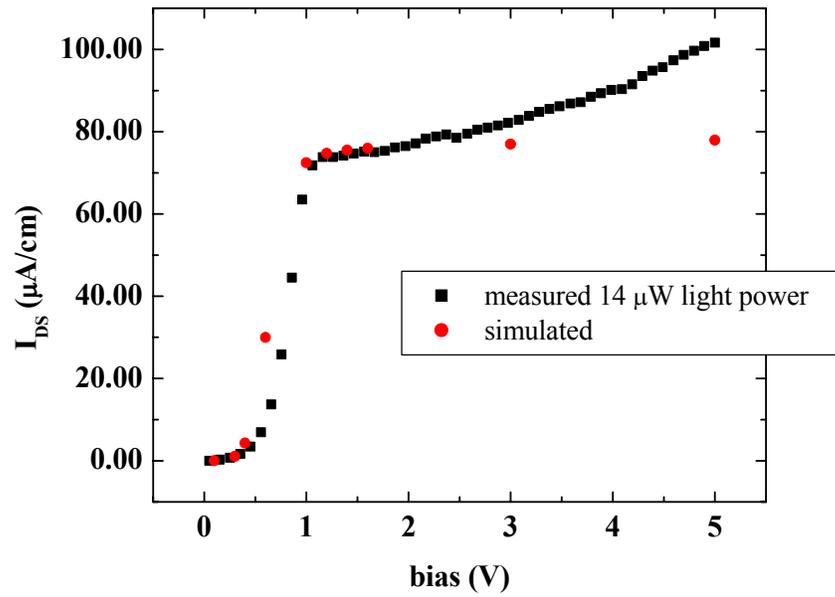


Figure 4-26. DC responsivity of 60 $\mu\text{m} \times 60 \mu\text{m}$ MSM photodetector with 3 μm finger width and 3 μm finger spacing for two different light intensities

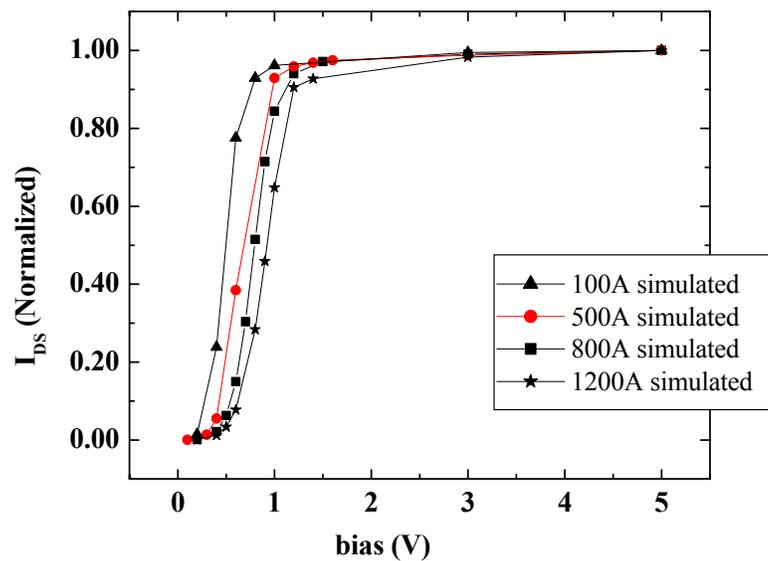


Figure 4-27. DC responsivity of $60\ \mu\text{m}\times 60\ \mu\text{m}$ MSM photodetector with $3\ \mu\text{m}$ finger width and $3\ \mu\text{m}$ finger spacing for different SEL thicknesses and $14\ \mu\text{W}$ light intensity

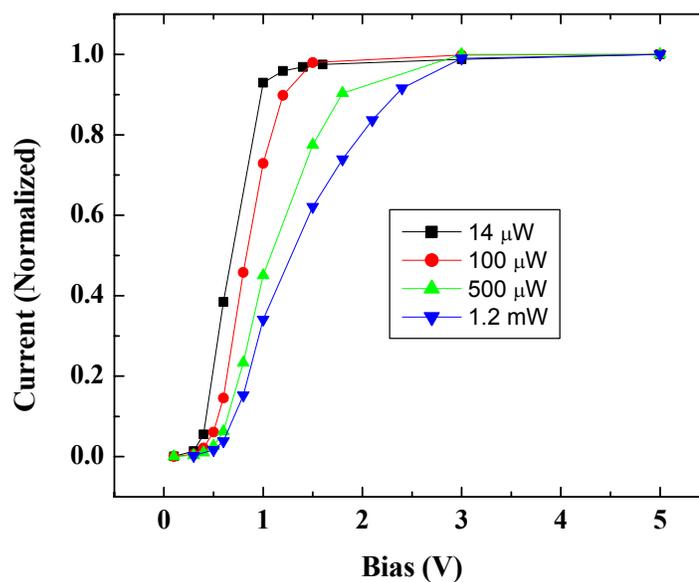


Figure 4-28. Simulated response of InAlAs/InGaAs OE mixer for different light intensities

SEL OE mixer. Figure 4-28 shows 2-Dimensional simulation of MSM Photodetector's response as a function of light intensity. The response for higher intensity light is slower compared to lower intensity light. The decrease in mobility caused by increased carrier generation is responsible for this "sluggish" behavior. Figure 4-29 shows simulated knee voltage as a function of light power and also as a function of Schottky Enhancement Layer thickness. Knee voltage increases both with increasing light intensity and with increasing Schottky Enhancement Layer thickness.

Mixing Characteristics

The mixing efficiency of the MSM-PD OE mixer is defined as the ratio of the responsivity of the detector at the IF frequency to its DC responsivity at the DC bias equal to the RMS value of the AC bias. To simulate mixing efficiency of the detector, the power dissipated is multiplied by function $(1 + \sin(2 \times \pi \times 500 \text{E} + 06 \times t))$ and a AC bias with frequency equal to Local Oscillator frequency is applied to the detector. The frequency of amplitude modulated light is 500 MHz, hence the intensity envelope of light is multiplied by the corresponding function. The result after frequency filtration should be a signal, which is sum of both sum frequency (up converted) and difference frequency (down converted) signals. Fourier transforms could be used to obtain the signal after passing through low pass filter.

Summary

We studied various MSM processing schemes for InGaAs based 1.55 μm MSM photodetectors. A state-of-the-art dark current of 46 pA at a bias of 1 V and 3 dB bandwidth of 24 GHz at a bias of 12 V was demonstrated. These devices were ideal for low noise and high frequency telecommunication applications. A planarization etch-back

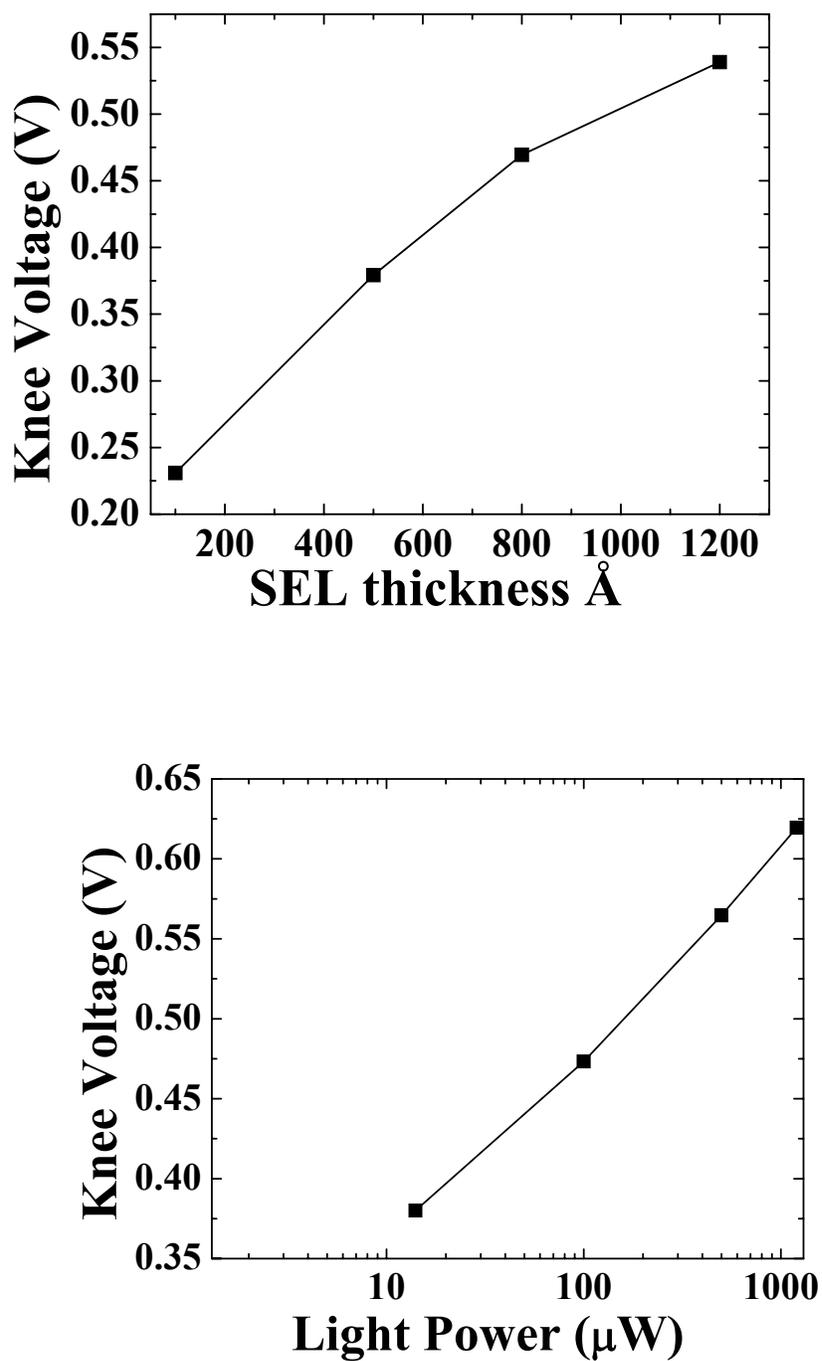


Figure 4-29. Knee Voltage as a function of a) InAlAs layer thickness for constant light intensity of $14 \mu\text{W}$ and b) as a function of power for constant InAlAs layer thickness of 500 \AA

process was also developed, which showed a low dark current and good photo-response.

The optoelectronic (OE) mixing effect in InAlAs Schottky-enhanced InGaAs-based metal-semiconductor-metal photodetectors (MSMPDs) was analyzed. The measured frequency bandwidth of such a mixer was less than that of a corresponding photodetector. The mixing efficiency was found to depend on the light modulation and mixed signal frequencies and it decreased non-linearly with optical power. This was not observed in GaAs-based and non-Schottky enhanced InGaAs MSMPDs. We presented a circuit model of the OE mixer to explain the experimental results.

M_{eff} decreased as LO frequency increased and increased as IF frequency increased. As optical power decreased, M_{eff} also decreased. The optoelectronic mixing characteristics of InAlAs, Schottky-enhanced, InGaAs-based metal-semiconductor-metal photodetectors for different SEL thickness was studied. M_{eff} of MSM-PD OEMs was dependent on the thickness of the InAlAs Schottky-enhancement layer. For thick SELs ($\approx 500 \text{ \AA}$), the bandwidth of a MSM-PD OEM was much less than that of a corresponding MSM-PD. In addition, $M_{500\text{eff}}$ varied as RF, LO, and IF frequencies were changed, and it decreased nonlinearly with decrease in optical power. Decreasing the thickness of the SEL to $\approx 100 \text{ \AA}$ improved the mixing characteristics of the MSM-PD OEM. The bandwidth of the OEM was similar to that of a corresponding photodetector and the mixing efficiency was found to decrease only slightly with decrease in optical power for 100 \AA SEL sample.

CHAPTER 5 THERMAL SIMULATION OF SEMICONDUCTOR DEVICES

Introduction

Tremendous progress has been achieved in the development of vertical-cavity surface-emitting lasers (VCSELs) for high-speed optical interconnects in high bit-rate data transmission systems [218-227]. We have earlier reported on 850 nm VCSELs [142-143]. Various designs involving better contacts and band gap engineered active regions have evolved over the years for VCSELs [7, 145-150]. Continuous wave operations of large signal performance above 10 Gbit/s data rates have been demonstrated for 850 nm, 980 nm and 1.3 μm VCSEL [161-163]. For local network applications, GaAs/AlGaAs based 850 nm VCSELs have already proved to be the laser of choice for short wavelength transmissions. However, the laser transmission distance becomes less than 1 km for 850 nm VCSEL operating at 10 Gb/s. The low-loss window of optical fiber for 1.3 and 1.55 μm provides an opportunity for VCSEL technology to extend the transmission distance in optical fiber out to more than 40 kilometers. This would be a major benefit for communications technology. The development of the long-wavelength VCSEL, however, has been slower than that of short-wavelength VCSELs (850/980 nm). The main reason is that there is no obvious pair of semiconductor materials with a large enough difference in indices of refraction compatible for optical quality epitaxial growth. Furthermore, the conventional InP/InGaAsP 1.55 μm distributed feedback laser (DFB) material system has a small conduction-band discontinuity. When it is operating at high power levels, thermal resistive and Auger nonradiative recombination generated heat lead

to excessive shifting of the fundamental mode to longer wavelengths, high threshold and thermal roll-over.

Good thermal dissipation for the device design is a prerequisite for high-speed performance. Flip chip bonded design has already been demonstrated to be advantageous for various electronic devices and lasers [2, 139-141]. A record low thermal resistance flip-chip bonding technique has been demonstrated with a 16×16 array of top $\text{TiO}_2/\text{SiO}_2$ mirror, implanted-apertures and lateral current injected 980 nm VCSELs. However there is no detailed study performed for this kind of flip-chip bonded VCSEL to confirm the temperature distribution in the active layer.

Different approaches were used for thermal analysis of the VCSELs. A finite difference simulation to quantitatively estimate the effect of flip-chip bonding on the thermal characteristics of a $\text{TiO}_2/\text{SiO}_2$ based top mirror, implanted-aperture and lateral current injected 850 nm VCSEL and a finite element based simulation was also used to simulate thermal characteristics of 1550 nm VCSEL. The simulation for 850 nm VCSEL employed three dimensional finite difference analysis to calculate the temperature, $T(r, \theta, z)$, and considered non-uniform heat source distribution. Carrier diffusion and distributed heat sources inside the active layer were also included.

For finite element analysis of flip-chip bonding on temperature distribution of 1550 nm intracavity-contacted VCSEL, commercially available software called FlexPDE was used. A novel design where flip-chip bonded tunnel junction VCSEL, having both top and bottom mirrors as dielectric, was investigated. LIV (Power Current Voltage) characteristics of 1550 nm VCSEL with similar electrical design, published by other researchers [7] combined with our electrical resistance model gave an estimate of heat

lost in active region. Distributed heat loss in various regions was estimated and used in a complete 3-dimensional model, which was solved using time dependent and steady state finite element analysis. Heat dissipation occurs through the final metal bonding pads to the heat sink. Effect of varying active region diameter and injection current was also estimated.

There is a strong interest in developing wide bandgap power devices for use in the electric power utility industry [164-166]. With the onset of deregulation in the industry, there will be increasing numbers of transactions on the power grid in the US, with different companies buying and selling power. The main applications are in the primary distribution system (100~2000 kW) and in subsidiary transmission systems (1~50 MW). A major problem in the current grid is momentary voltage sags, which affect motor drives, computers and digital controls. Therefore, a system for eliminating power sags and switching transients would dramatically improve power quality. For example it is estimated that a 2-second outage at a large computer center can cost US\$ 600,000 or more, and an outage of less than one cycle, or a voltage sag of 25% for two cycles, can cause a microprocessor to malfunction. In particular, computerized technologies have led to strong consumer demands for less expensive electricity, premium quality power and uninterruptible power.

The basic power electronics hierarchy would include the use of wide bandgap devices such as Gate Turn-Off Thyristors (GTOs), MOS-Controlled Thyristors (MCT) or Insulated Gate Bipolar Transistors (IGBTs) combined with appropriate packaging and thermal management techniques to make subsystems (such as switches, rectifiers or adjustable speed devices) which then comprise a system such as Flexible AC

Transmissions (FACTS). Common power electronics systems, which are inserted between the incoming power and the electrical load include uninterruptible power supplies, advanced motors, adjustable speed drives and motor controls, switching power supplies, solid-state circuit breakers and power conditioning equipment. Motors consume about 50% of the electricity in the US. Motor repairs cost ~US\$ 5 billion each year and could be dramatically reduced by high power electronic devices that permit smoother switching and control. Moreover, control electronics could dramatically improve motor efficiency. Other end uses include lighting, computers, heating and air-conditioning.

Some desirable attributes of the next generation wide bandgap power electronics include the ability to withstand currents in excess of 5 kA and voltages in excess of 50 kV, provide rapid switching, maintain good thermal stability while operating at temperatures above 250°C, have small size and be light-weight, and be able to function without bulky heat-dissipating systems. For these reasons, there is a strong development effort on wide bandgap power devices, predominantly SiC, with lesser efforts in GaN and diamond, which should have benefits that Si-based or electromechanical power electronics cannot attain. The higher standoff voltages should eliminate the need for series stacking of devices and the associated packaging difficulties. In addition these wide bandgap devices should have higher switching frequency in pulse-width-modulated rectifiers and inverters.

The absence of Si devices capable of application to 13.8 kV distribution lines (a common primary distribution mode) opens a major opportunity for wide bandgap electronics. However, cost will be an issue, with values of US\$ 200~2000 per kVA necessary to have an impact. It is virtually certain that SiC switches will become

commercially available within 3~5 years, and begin to be applied to the 13.8 kV lines. MOS Turn-Off-Thyristors involving a SiC GTO and SiC MOSFET are a promising approach [167]. An inverter module can be constructed from an MOS turn-off thyristor (MTO) and a SiC power diode.

Packaging and thermal management will be a key part of future power devices. For current Si IGBTs, there are two basic package types - the first is a standard attached die, wire bond package utilizing soft-solder and wire-bonds as contacts, while the second is the presspack, which employs dry-pressed contacts for both electrical and thermal paths [168, 34]. In the classical package the IGBTs and control diodes are soldered onto ceramic substrates, such as AlN, which provide electrical insulation, and this in turn is mounted to a heat sink (typically Cu). Thick Al wires (500 μm) are used for electrical connections, while silicone gel fills the package [168]. In the newer presspack style, the IGBT and diode are clamped between Cu electrodes, buffered by materials such as molybdenum or composites [34], whose purpose is to account for the thermal expansion coefficient differences between Si and Cu. The package is again filled with gel for electrical insulation and corrosion resistance.

The GaN materials system is attractive from the viewpoint of fabricating unipolar power devices because of its large bandgap and relatively high electron mobility [169-172]. An example is the use of Schottky diodes as high-voltage rectifiers in power switching applications [10, 169-181]. These diodes will have lower blocking voltages than p-i-n rectifiers, but have advantages in terms of switching speed and lower forward voltage drop. Edge termination techniques such as field rings or field plates, bevels or surface ion implantation are relatively well developed for Si and SiC and maximize the

high voltage blocking capability by avoiding sharp field distributions within the device. There is also a strong need to understand the temperature distributions in GaN rectifiers with and without flip-chip bonding and as a function of duty cycle and biasing conditions. Finite element analysis of thermal characteristics of pulsed mode bulk GaN rectifiers with flip-chip bond design was performed to establish the effect of flip chip bonding in power rectifiers.

Thermal Analysis of 850 nm VCSEL

Device Fabrication

The epitaxial layers were grown by metal organic chemical vapor deposition on n-doped GaAs substrates. The bottom semiconductor DBR mirror was grown epitaxially with the device structure and consists of 30 pairs of AlAs/AlGaAs quarter wavelength layers. A p-i-n structure was employed, with carbon as the p-type dopant and silicon as the n-type dopant. A TiO₂/SiO₂ top mirror deposited by electron beam evaporation was used as the lesser reflective mirror, for device top emission. The top mirror features were formed as the final step of device fabrication. The GaAs quantum wells were clad by lightly-doped AlGaAs for carrier confinement. The aperture was formed by O⁺ implantation into the graded p-layer a few hundred angstroms above the active region to reduce lateral current spreading. He⁺ implantation was used to reduce the capacitance under the contact pads.

Figure 5-1 shows schematics of the bottom mounted and flip-chip bonded VCSEL devices. The device fabrication steps are identical for these two VCSELs. The only difference is that conventional VCSEL is bottom mounted and the flip-chip bonded VCSEL uses Au-Sn based solder bumps to connect the VCSEL to the carrier through its contact pads.

Finite Difference Analysis

This modeling is based on the typical equation of energy for cylindrical coordinates (r-, θ - and z- axes),

$$\rho_d C_p \frac{\partial T}{\partial t} - k \left[\frac{1}{r} \frac{\partial}{\partial r} \left(r \frac{\partial T}{\partial r} \right) + \frac{1}{r^2} \frac{\partial^2 T}{\partial \theta^2} + \frac{\partial^2 T}{\partial z^2} \right] = \frac{J^2}{\sigma} \quad (5-1)$$

where t is time, ρ_d is density, C_p is heat capacity, J is current density [A/cm^2], k is thermal conductivity [$W/cm \cdot K$], and σ is conductivity of each layer. The term on the right side of equation (5-1) corresponds to heat generation quantity per unit volume [cal/cm^3]. The quantity of heat generation varies depending on specific regions and layers since current density and conductivity are functions of doping, composition and geometry of the device. The device dimension and temperature range considered in our case are very small, therefore, it is reasonable to assume the heat transfer through heat convection can be ignored. The heat transfer is dominated by heat conduction through the semiconductor, metal contacts and the air surrounding the device.

The main heat generation, (85%) in the device occurs due to Joule heating, the resistance of semiconductor layers. Joule heating is giving by

$$W(r, \theta, z) = \rho(r, \theta, z) j^2(r, \theta, z) \quad (5-2)$$

where j is the current density flowing in the device and ρ is the electrical resistivity of the materials for the VCSEL layers. We have generated a resistance model for our VCSELs, which included contact resistance, resistivities for each epi-layers in the device. Based on the resistances of each layer and the electrical current flow directions, vertical or lateral, the Joule heat generations were estimated for each unit cell in our model. [161] The other major heat source, (5%), is nonradiative recombination in the active region.

Nonradiative recombination is governed by Auger recombination and Shockley-Read-Hall recombination, this portion of the heat generation was determined from the measured LIV characteristics of the laser diode and estimated Joule heat generations. Two-dimensional temperature-distribution of VCSELs with and without flip-chip bonding are illustrated in Figure 5-2. The maximum temperature rise is 60 °C for the structure without flip-chip bonding and it is 42 °C for the flip-chip bonded VCSEL. The

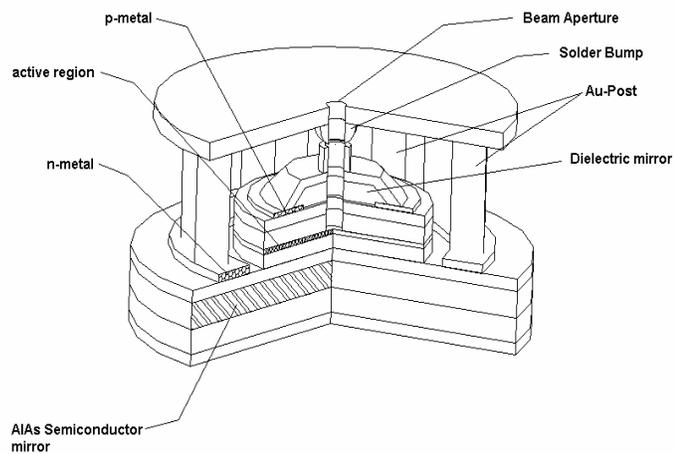
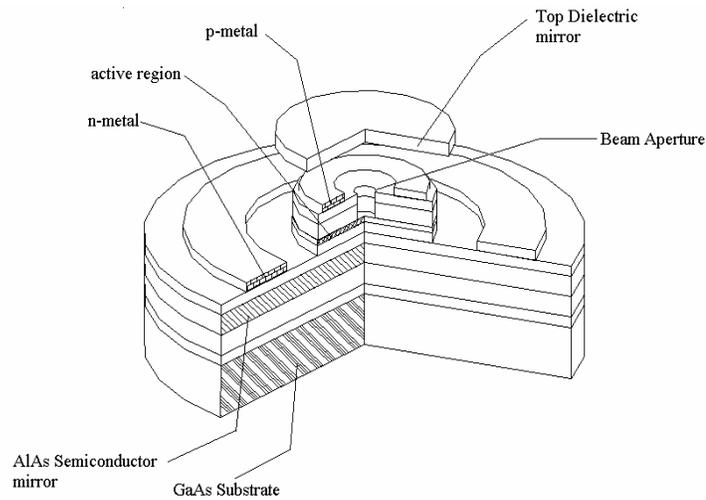


Figure 5-1. a) Bottom mounted and b) flip-chip bonded VCSEL devices

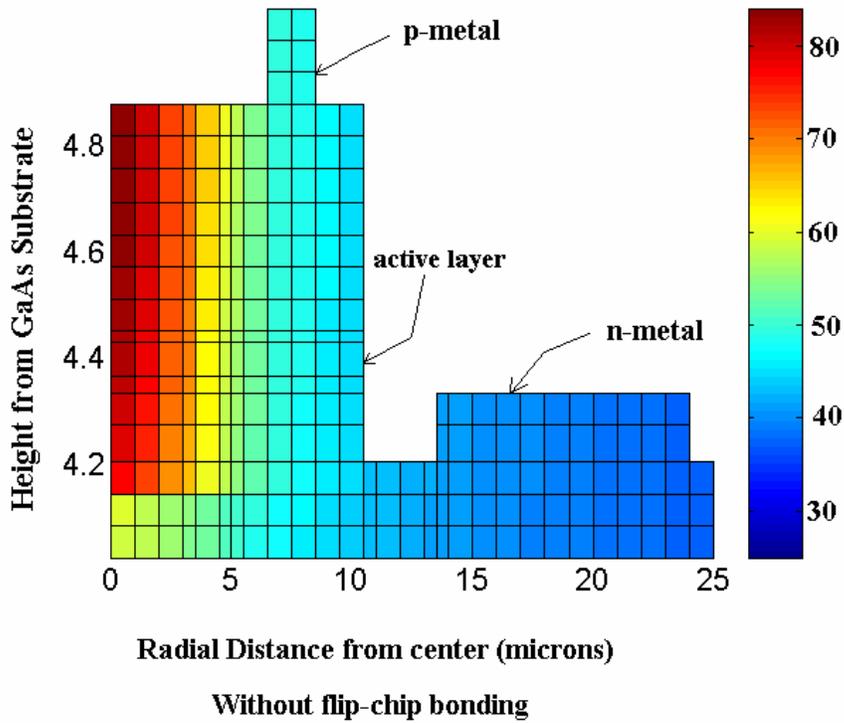
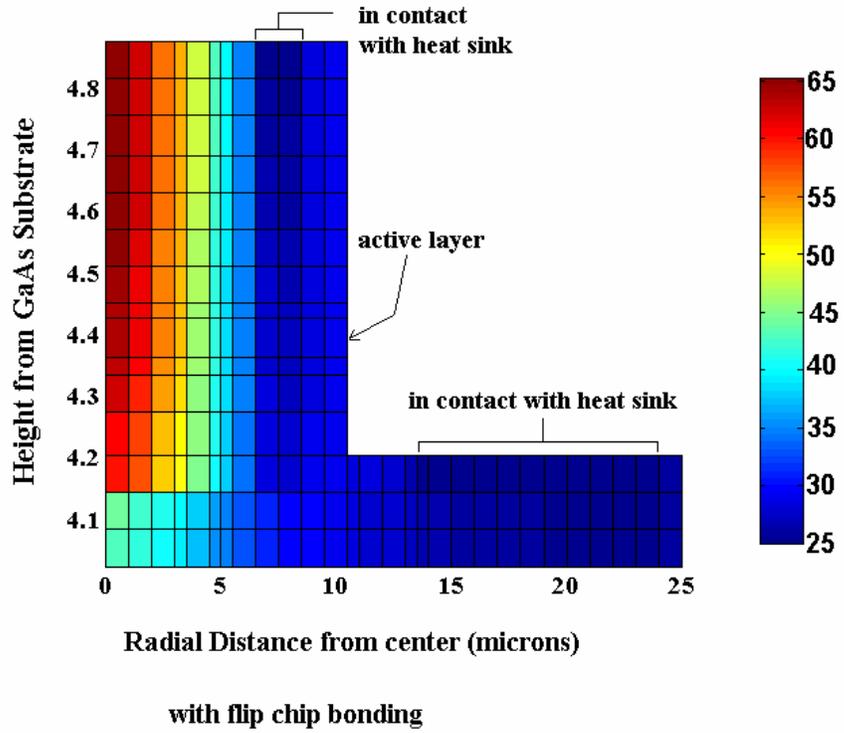


Figure 5-2. Two-dimensional temperature-distribution of VCSELs a) with and b) without flip-chip bonding

result is in excellent agreement with the measured temperature rise of $1.96\text{ }^{\circ}\text{C}/\text{mW}$ for 30 mW input power [143]. The flip-chip bonded structure differs from the other because the contact (n- and p-) acts as a heat sink. The maximum temperature occurred in the core of the cylindrical VCSEL near the top, because the center-top of VCSEL is covered by the dielectric mirror, which has a low thermal conductivity. Figure 5-3 illustrates the temperature in the active region at different levels of input current. The temperature difference between flip-chip bonded devices and bottom bonded devices increase from $15\text{ }^{\circ}\text{C}$ at low current injection level to $> 20\text{ }^{\circ}\text{C}$ at high current injection region. This clearly demonstrates the efficiency of heat dissipation of flip-chip bonded devices.

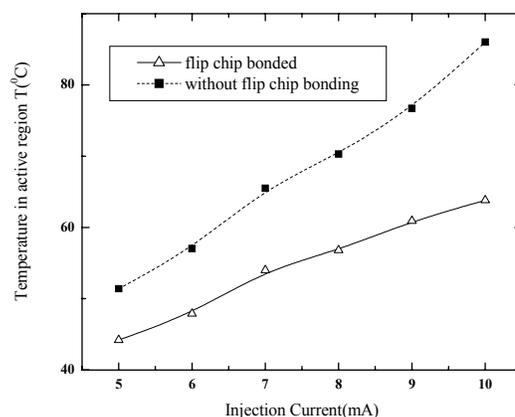


Figure 5-3. Temperature in the active region at different levels of input current

The thermal resistances of each epi-layer were estimated. Figure 5-4 only shows the device thermal resistance in the active region. The thermal resistance of the flip-chip bonded device shows almost half of that in the back-side bonded device. This is consistent with the temperature profiles of the devices that the heat dissipation is more efficient in the flip-chip bonded device. The thermal resistance R monotonically decreases as the active region diameter increases. In the model, we assume the constant

current for different diameters of the active layer. The larger diameter device has less current density, therefore, the thermal resistance is smaller. The effect of active layer thickness on thermal resistance was simulated and was found to be quite negligible.

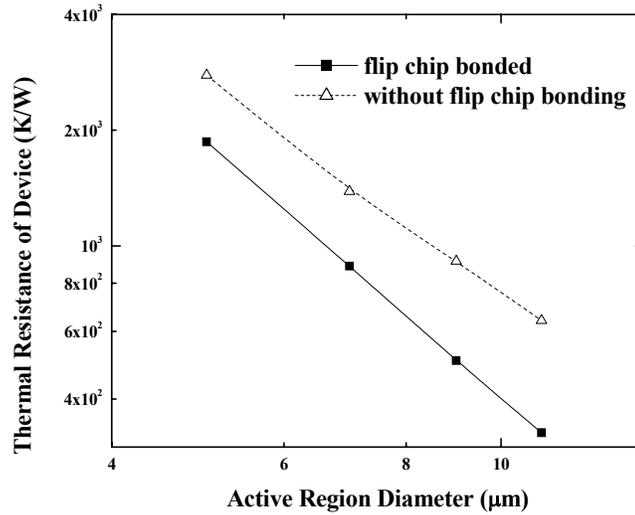


Figure 5-4. Simulated device thermal resistance in the active region

The above simulation results are based on a steady state solution, which describes only the thermal equilibrium reached. To investigate the temperature rising while the device is turning on, a dynamical modeling was investigated.

Figure 5-5 shows the temperature variation as a function of time in the active region. The simulation result shows the temperature rise due to internal heat generation is significant (maximum temperature is around 60 °C at $I = 10$ mA). The temperature profile reached steady state in the range of a few tenths of a milli-second, however, both small signal and large signal performance of our VCSELs are above 10 Gb/s. As mentioned earlier, the wavelength, peak power, threshold current and slope efficiency depend on the operation temperature of the VCSEL. This means that efficient heat

dissipation in the VCSEL is very critical to minimize the shifts in VCSEL optical characteristics.

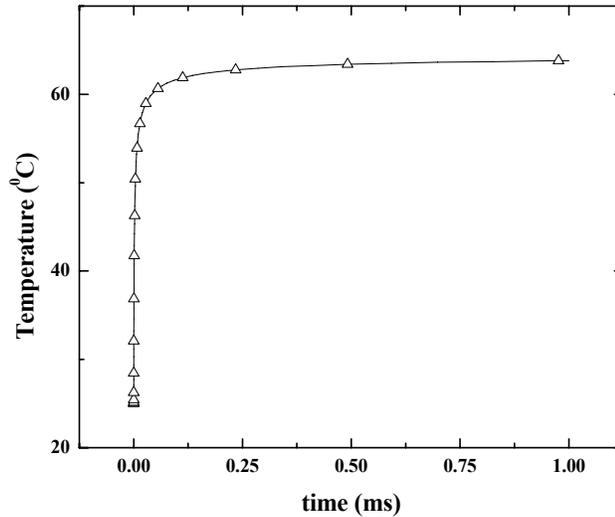


Figure 5-5 Temperature changes as a function of time in the active region

Thermal Analysis of 1550 nm VCSEL

Proposed 1550 nm Device

Figure 5-6 illustrates the proposed device structure. The device consists of top n-type InP cladding layer, a n⁺⁺ InP/p⁺⁺ InAlAs tunnel junction, InAlGaAs compressively strained MQW, followed by another n-type InP cladding layer and then by a InAlAs etch stop layer. Top dielectric mirror consists of 7 periods of SiO₂/TiO₂ DBR with reflectivity of 99.96%. The bottom mirror can be deposited after flip-chip bonding the device to the heat sink, and it consists of 5 periods of SiO₂/TiO₂ DBR with reflectivity of 99.59%. The use of dielectric DBRs simplifies the growth of VCSEL structure opening up the possibility of large-scale production. Fewer periods of dielectric mirror would achieve the desired reflectivity when compared to semiconductor mirrors, which have been used by other researchers [7, 144]. High electron mobility and high

thermal conductivity of InP leads to low electrical and thermal resistance in the VCSEL structure. Figure 5-7 shows the heat flow vector $-k(\text{grad}T)$ (on left) and constant temperature contours (on right) distribution across the cross-section of the VCSEL structure. Most of the heat flows into the heat sinks through the flip-chip bonded final metal bonding pads. Flip-chip bonding along with high electron mobility of InP also allows for the use of lower doping concentrations without compromising high current injection level in the device.

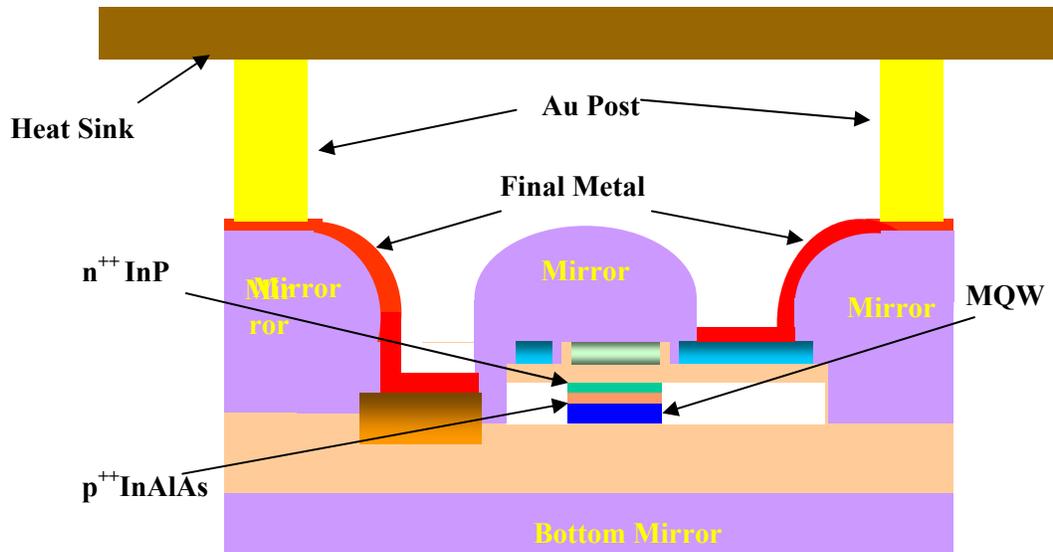


Figure 5-6. Cross-section of the flip-chip bonded VCSEL device

Further free-carrier absorption can be reduced by using low doping levels for InP layers.

Finite Element Analysis

The main heat generation, (70%) in the device occurs through Joule heating due to the resistance of semiconductor layers. Joule heating is given by Equation 5-2. A resistance model (as shown in Figure 5-8) was developed and the resistance for each epi-layer was estimated. Table 5-I enlists thickness, doping, mobility, resistivity, sheet resistance and calculated electrical resistance for each layer. A contact resistance of 25Ω

was assumed. Figure 5-9 shows the IV data which was used to estimate heating in active region. The curve published by other researchers [7] was used to get a conservative measure of the heating in active region. Their data was fit into equation (3),

$$I_F = I_{sat} \exp[q(V_F - R_T I_F) / m k_B T] \quad (5-3)$$

where I_F is forward current density, V_F is forward voltage drop to get an estimate of saturation current, I_{sat} and resistance, R_T .

Further data points were fit into equation (5-3) using same I_{sat} as theirs and R_T as the total resistance predicted by our resistance model, to obtain lower values of potential drop across the VCSEL as seen in Figure 5-9. This is intuitive since the resistance model would not account for any losses which might occur in the active region. 27% of the heat was generated by non-radiative recombination in the active region using their curve. Non-radiative recombination is governed by Auger recombination and Shockley-Read-Hall recombination. This portion of the heat generation was determined from the measured LIV characteristics of the laser diode and the estimated Joule heat generations. This modeling is based on the typical equation of energy for Cartesian coordinates (x-, y- and z- axes),

$$\rho_d C_p \frac{\partial T}{\partial t} - k \left[\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right] = \frac{J^2}{\sigma} \quad (5-4)$$

The term on the right side of equation (5-4) corresponds to heat generation quantity per unit volume [W/ μm^3]. The quantity of heat generation varies depending on specific regions and layers since current density and conductivity are functions of doping, composition and geometry of the device. The device dimension and temperature range considered in our case are very small, therefore, it is reasonable to assume the heat

transfer through heat convection can be ignored. Two-dimensional temperature-distribution of VCSELs with flip-chip bonding is illustrated in Figure 5-10. The maximum temperature rise is 15.9 °C for the flip-chip bonded VCSEL. The flip-chip bonded structure the top surfaces of final contact metal have been assumed to be at heat sink temperature. The maximum temperature occurred in the core of the active region in the VCSEL because the heat generation per unit volume is at its maximum in the active region layer. The excellent thermal characteristics of InP further help rapid heat dissipation to the heat sink.

Figure 5-11 shows the effect of various current injection levels and the active region radius on the maximum temperature rise in the flip-chip bonded VCSEL. The temperature rise is almost linear at higher current injection levels (8 to 10 mA) in flip-chip bonded device, indicating the enhanced efficiency of heat dissipation in a flip-chip bonded design. The maximum temperature rise decreases with increasing active region diameter, but the effect is not that significant in a flip-chip bonded VCSEL.

To investigate the temperature rise when device is turning on, a dynamical model was investigated. Figure 5-7 shows the transient characteristics of the device when the current is switched on from 0 to 10 mA. The time needed for the device to reach the steady-state temperature was in the range of tens of microseconds, which is orders of magnitude larger than the electrical or optical switch time.

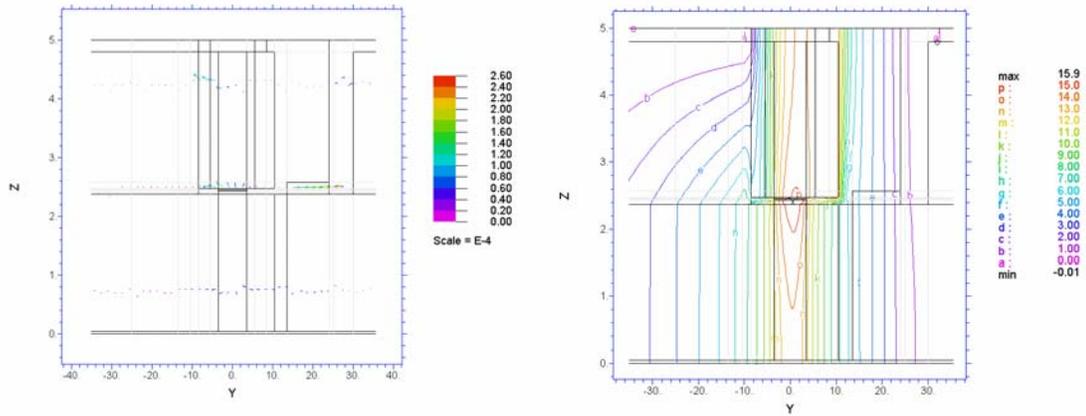


Figure 5-7. Across cross section of VCSEL a) Heat flow vector and b) constant temperature contour

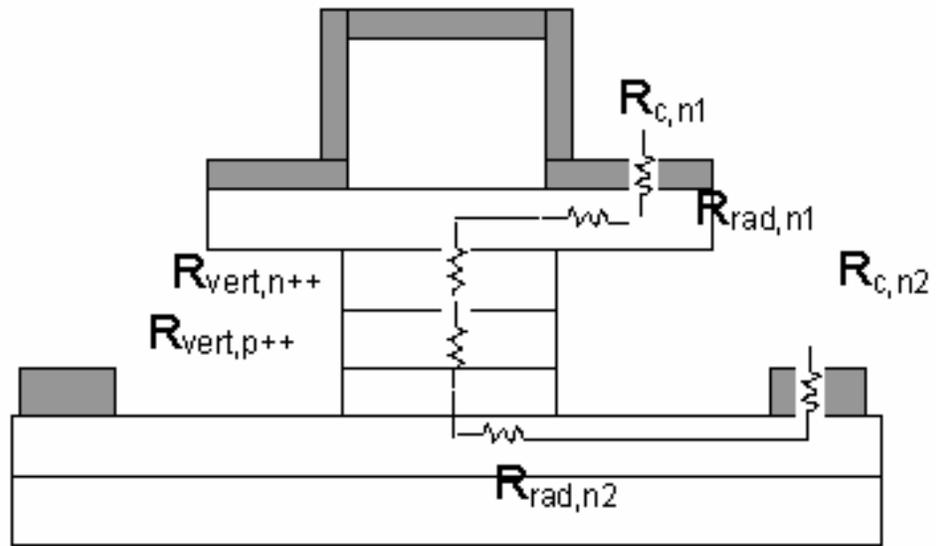


Figure 5-8. Schematic representation of tunnel junction VCSEL, showing individual resistance components

Table 5-1. Calculated resistances in VCSEL structure

Layer	Thickness	Doping	Est. Electron Mobility (cm ² /V-s)	Resistivity (Ω-cm)	ρ_s (Ω/sq.)	R (Ω)
In P top	2.33E-04	5.00E+17	1800	6.94E-03	29.90	3.34
n++ InP	2.00E-06	3.00E+18	800	2.6E-03	1300.00	1.35E-02
p++ InAlAs	2.00E-06	1.00E+19	32	1.95E-02	9770.00	1.02E-01
InP bottom	2.33E-04	5.00E+17	1800	6.94E-03	29.90	7.60

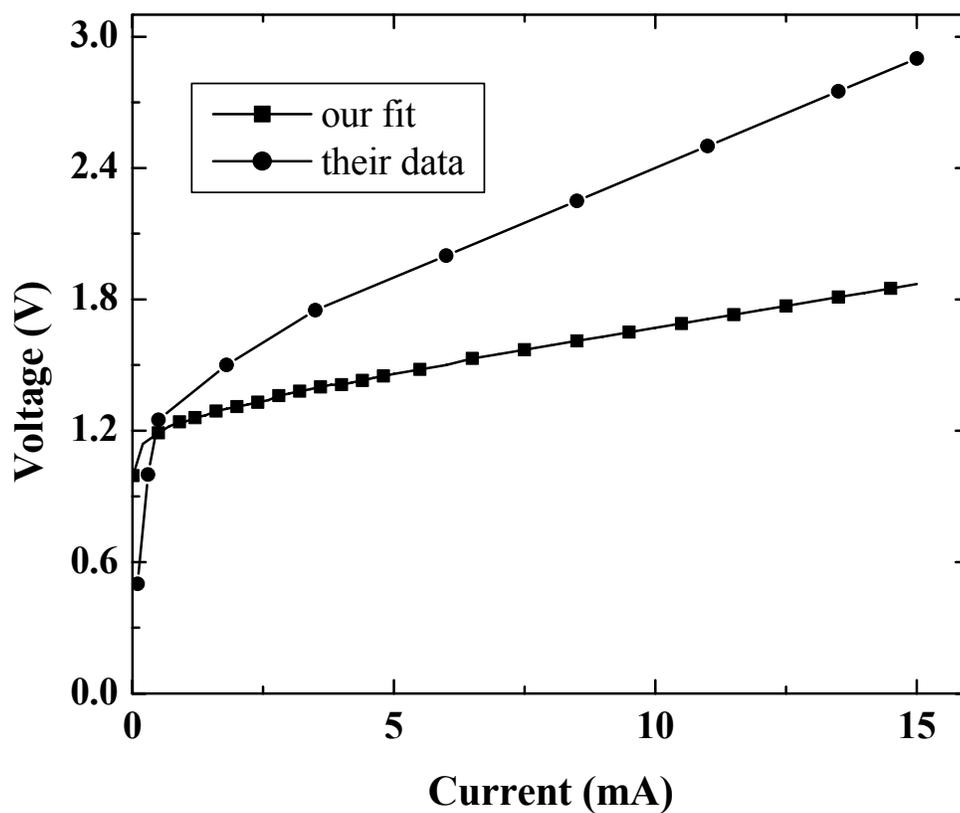


Figure 5-9. IV data measured by other group and fitted by our resistance model

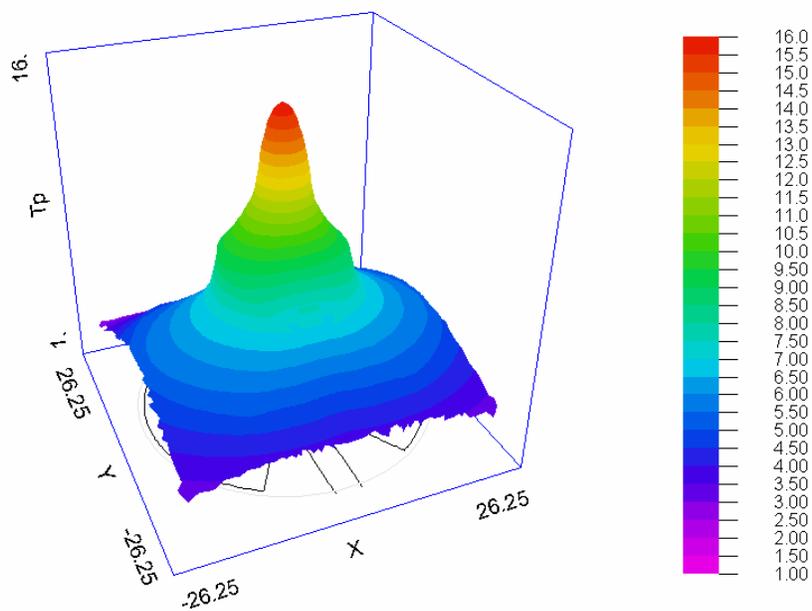


Figure 5-10. Surface plot of temperature distribution in active region

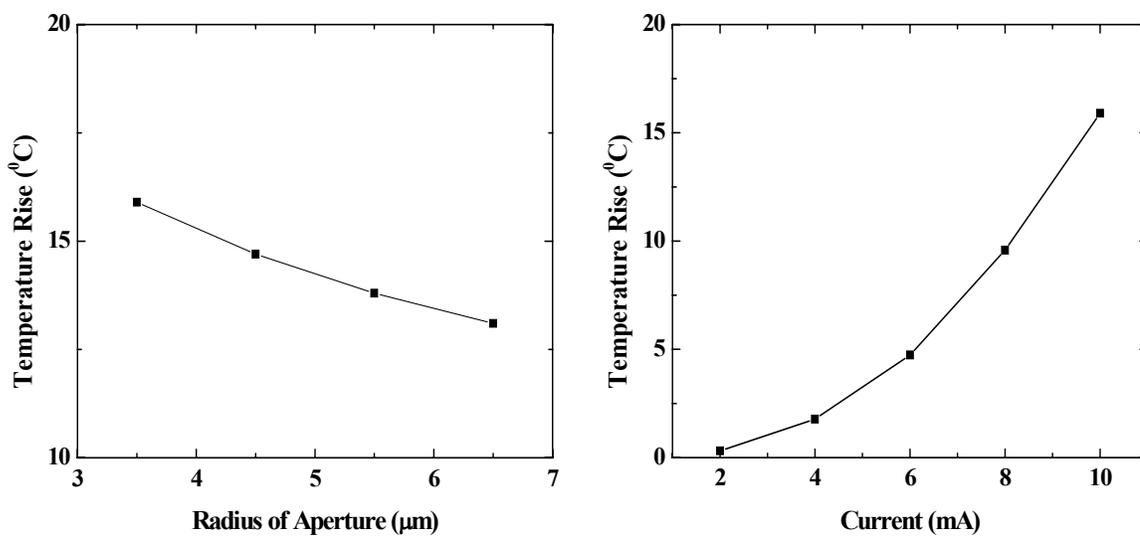


Figure 5-11. Active region a) temperature dependence Vs Injection Current and b) temperature dependence Vs aperture radius

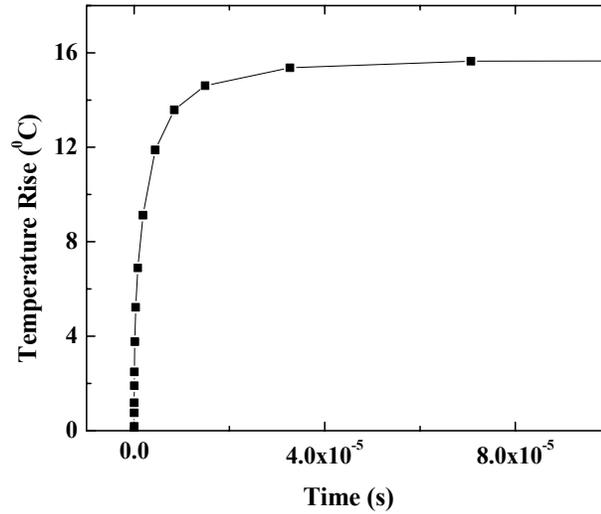


Figure 5-12. Temperature changes as a function of time in the active region

Thermal analysis of Bulk GaN Rectifiers

Theory

For a Schottky rectifier we can express the reverse breakdown voltage V_{br} , maximum electric field E_m , the on-state resistance R_{on} and the forward voltage drop V_F in the following equations:

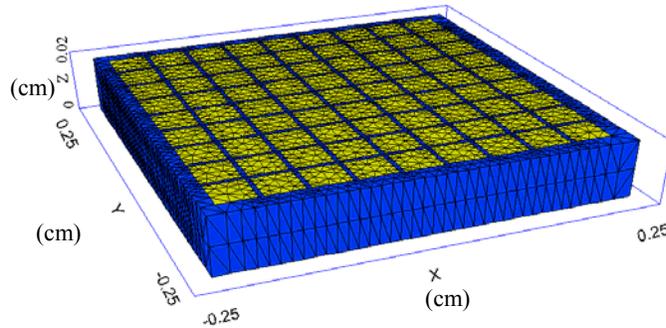
$$V_{br} = E_m W_{Br}/2 \quad (5-5)$$

$$E_m = \frac{2V_{br}}{\left(\frac{2\epsilon_s V_{br}}{qN_D}\right)^{1/2}} \quad (5-6)$$

$$R_{on} = \left(\frac{4V_{br}^2}{\epsilon_s \mu E_m^3}\right) + \rho W_s + R_C \quad (5-7)$$

where W_{Br} is the depletion region width at breakdown, ϵ_s the permittivity of GaN, q the electronic charge, N_D the doping level in the active region, μ the electron mobility, ρ the

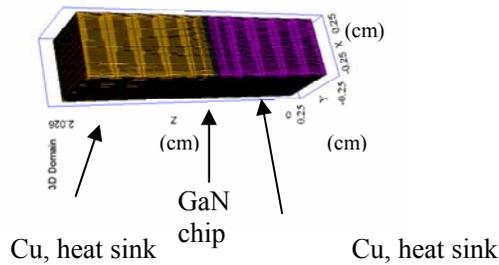
resistivity, W_s the thickness of GaN substrate, R_C the ohmic contact resistance, n the diode ideality factor, k the Boltzmann's constant, T the absolute temperature, J_F the forward current density and A^{**} is Richardson's constant for n-GaN.



Heat Equation

$$\rho C_p (\partial T / \partial \tau) - k \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right) = P_D$$

$$P_D = J_F V_F \frac{t_{on}}{T} + J_L V_R \frac{(T - t_{on})}{T}$$



Boundary Conditions

Temperature rise at top of top heat sink = 0°C
 Temperature rise at bottom of bottom heat sink = 0°C

Figure 5-13. Grid of a) the bulk rectifier device and b) flip-chip bonded rectifiers used for thermal simulation

The thermal simulation employs a 3-D finite element analysis to calculate the temperature distribution within flip-chip bonded and unbonded devices. Figure 5-13 (a) shows a schematic of the grid generated for the simulations, along with the structure after flip-chip bonding. The power dissipation P_D was obtained from the relation

$$P_D = J_F V_F \frac{t_{on}}{T} + J_L V_R \frac{(T - t_{on})}{T} \tag{5-8}$$

where t_{on}/T is the duty cycle. The main heat generation in the device occurs due to joule

heating due to resistance of the semiconductor layers. Joule heating is given by equation 5-2.

Finite Element Analysis

Two and three-dimensional temperature rises from room temperature with the flip-chip bonded structure are shown in Figure 5-14, with a typical increase in temperature of ~ 21 °C occurring in the center of the structure. These results assured a current density of 41.25 A/cm² and contact resistance of 5×10^{-5} Ω-cm².

The flip-chip bonding is effective in reducing the effective temperature rise. Figure 15 shows a schematic of device without flip-chip bonding. In this case, the simulations under the same conditions as for Figure 5-14 show a much larger temperature increase. Figure 5-16 shows the temperature distributions for the non flip-chip case, measured at the top of the structure. The maximum temperature rise is ~ 42 ° C above room temperature in this case. Fairly similar results were observed when the analysis was performed in the center or at the bottom of the chip. The fact that the flip-chip arrangement allows heat to escape from both sides through the heat sinks is consistent with the lower temperature rise relative to a device where effective heat conduction occurs only from one side.

Figure 5-17 shows the expected temperature rise as a function of duty cycle at a fixed current level of 41.25 A/cm² and fixed on-state resistance of 0.11 Ω-cm². As the on-time increases, the temperature of the flip-chip bonded device also increases in an almost linear fashion. However, even at a duty cycle of 0.9, the temperature rise above ambient is only ~ 40 ° C. One of the key determining factors in the final temperature rise is the value of the on-state resistance, as shown in Figure 5-18 (a). The on-resistance is the sum of the semiconductor resistance and contact resistance.

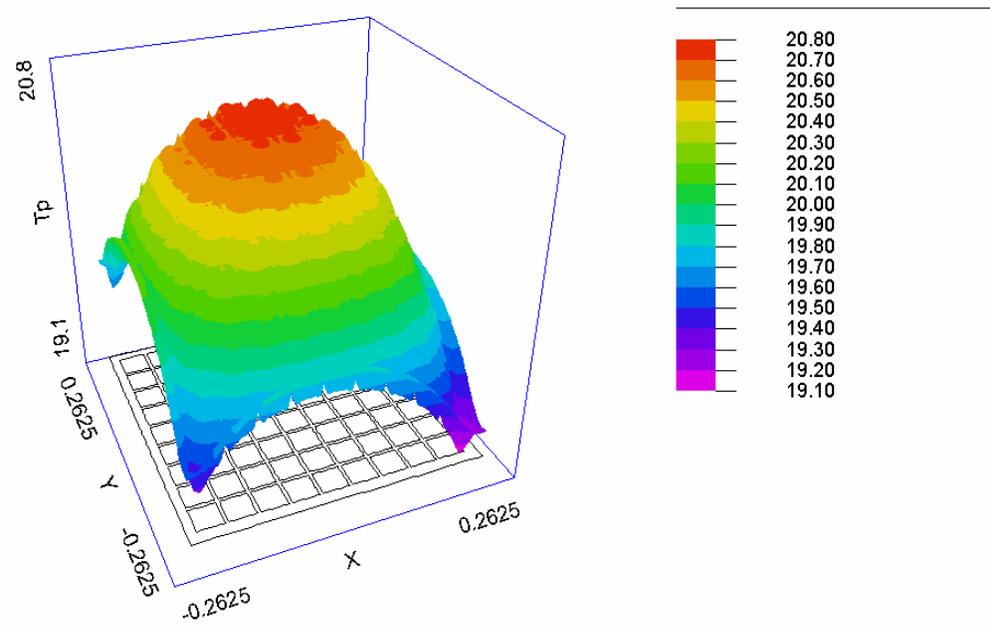
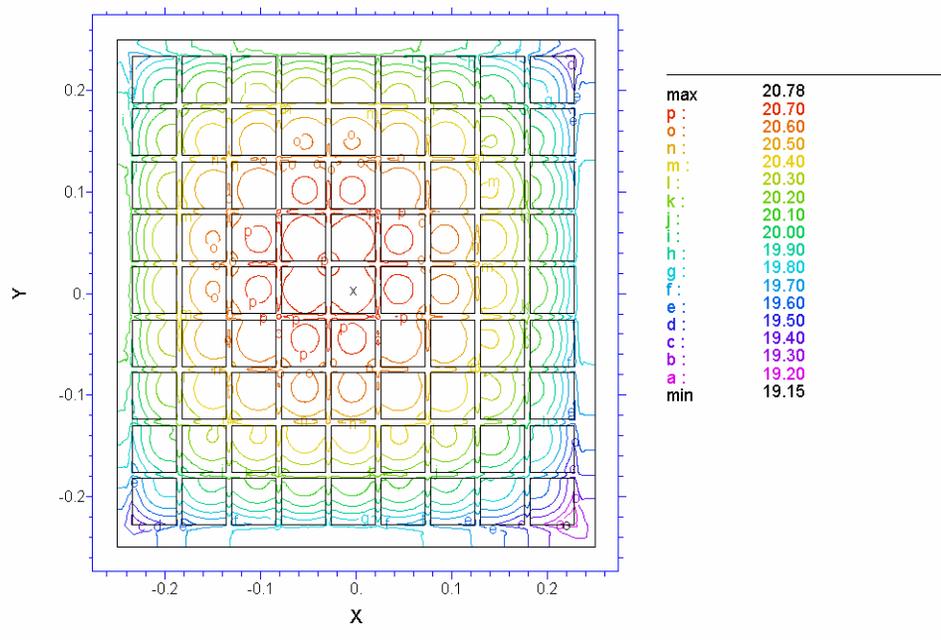


Figure 5-14. Distribution of temperatures at a) the top of flip-chip bonded rectifier and b) 3-D representation of temperature distribution

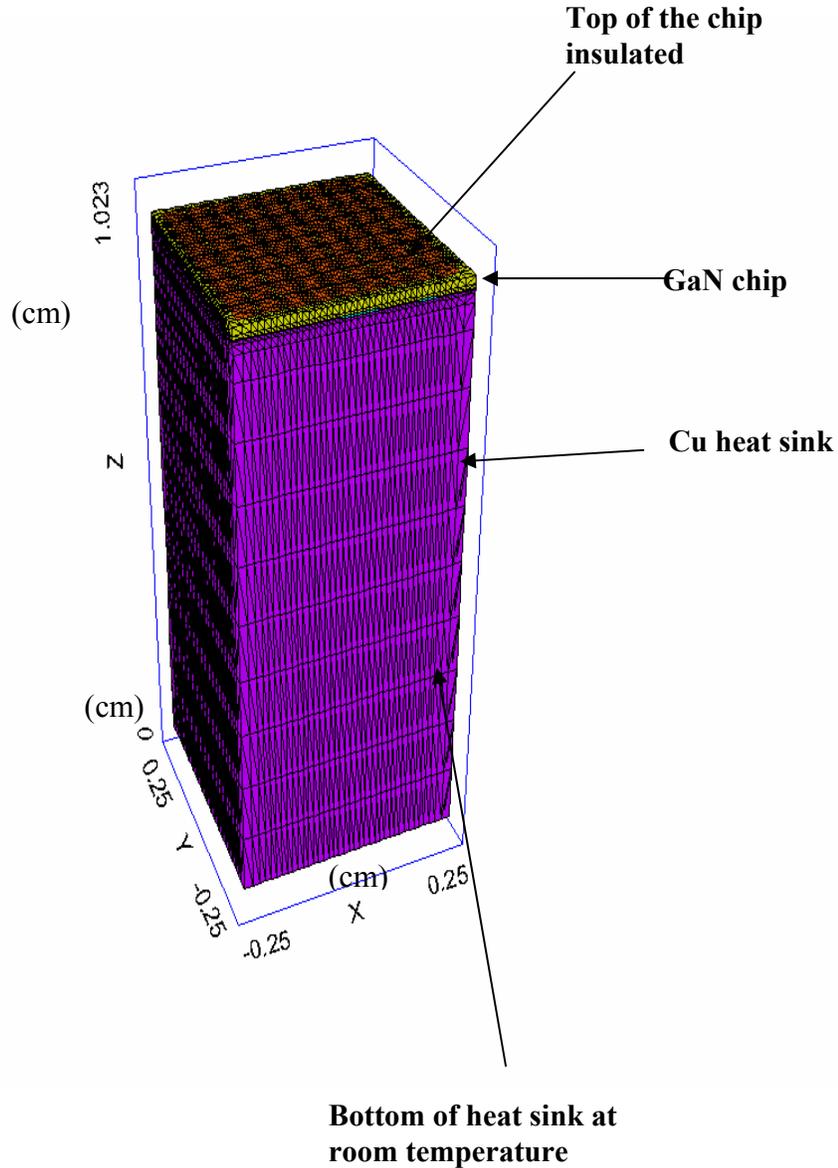


Figure 5-15. Grid structure used for thermal simulation of non flip-chip bonded rectifier

The latter is usually low if n-GaN is employed, with contact resistances of $\sim 10^{-6} \Omega\text{-cm}^2$ possible under optimum conditions. The temperature rise as a function of forward voltage for a fixed duty cycle of 0.5 and an on-state resistance of $0.11 \Omega\text{-cm}^2$ is shown in Figure 5-18 (b). The forward turn-on voltage of bulk GaN rectifiers is typically 3.5-4V, with a forward current density of $100 \text{ A}\text{-cm}^2$ at a voltage of $\sim 5\text{V}$.

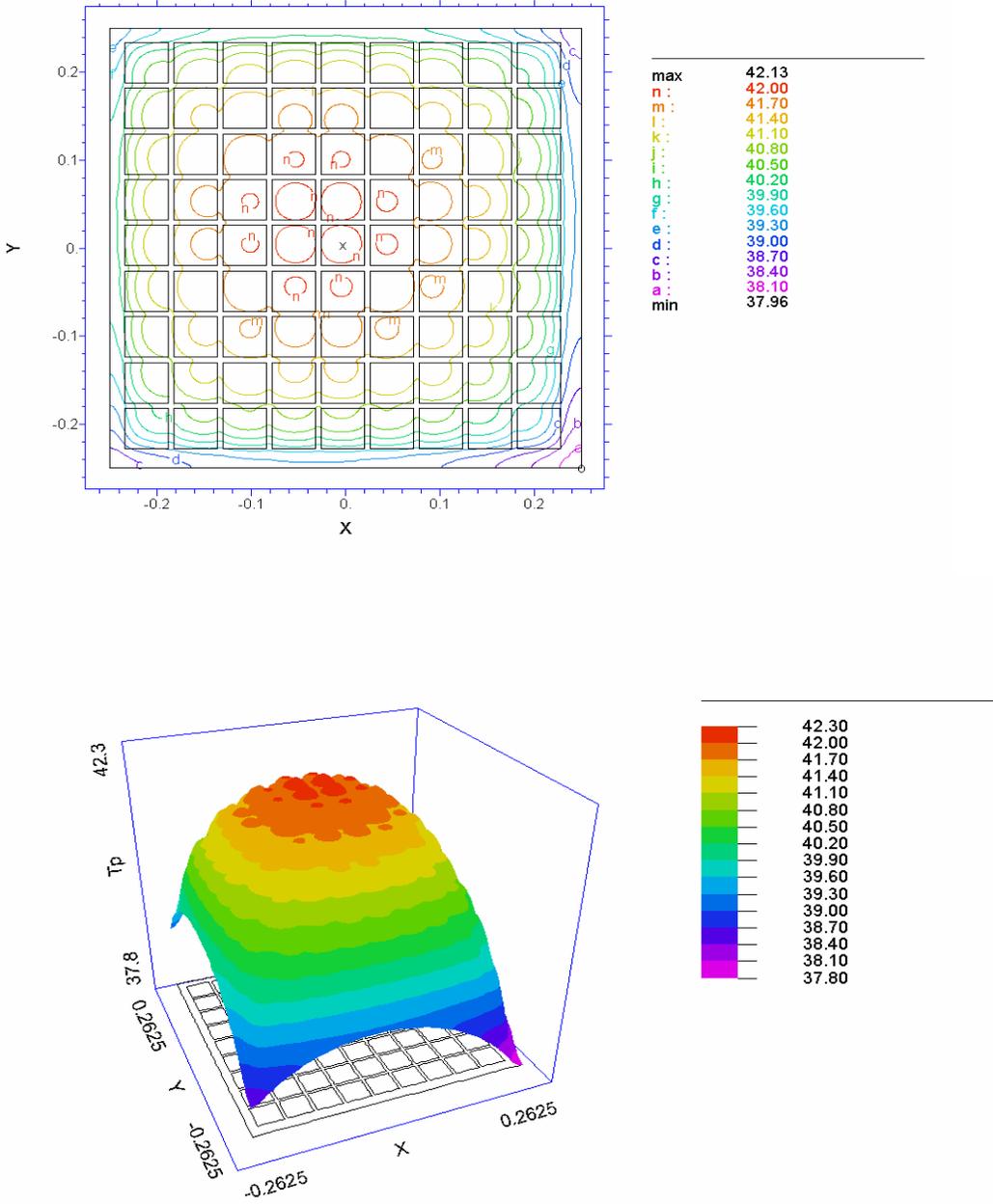


Figure 5-16. Distribution of temperatures a) at top of non flip-chip bonded rectifier and b) 3-D representation of temperature distribution

The effect of reverse breakdown voltage vs. temperature rise above ambient is shown in Figure 5-19 (a), for a fixed duty cycle of 0.5. Note that the reverse breakdown

voltage is not a significant factor in the temperature rise. The key factor in temperature rise is the forward current density, as shown in Figure 5-19 (b). The absolute temperature of the flip-chip bonded devices remains $< 100\text{ }^{\circ}\text{C}$ for current densities $< 50\text{ A/cm}^2$.

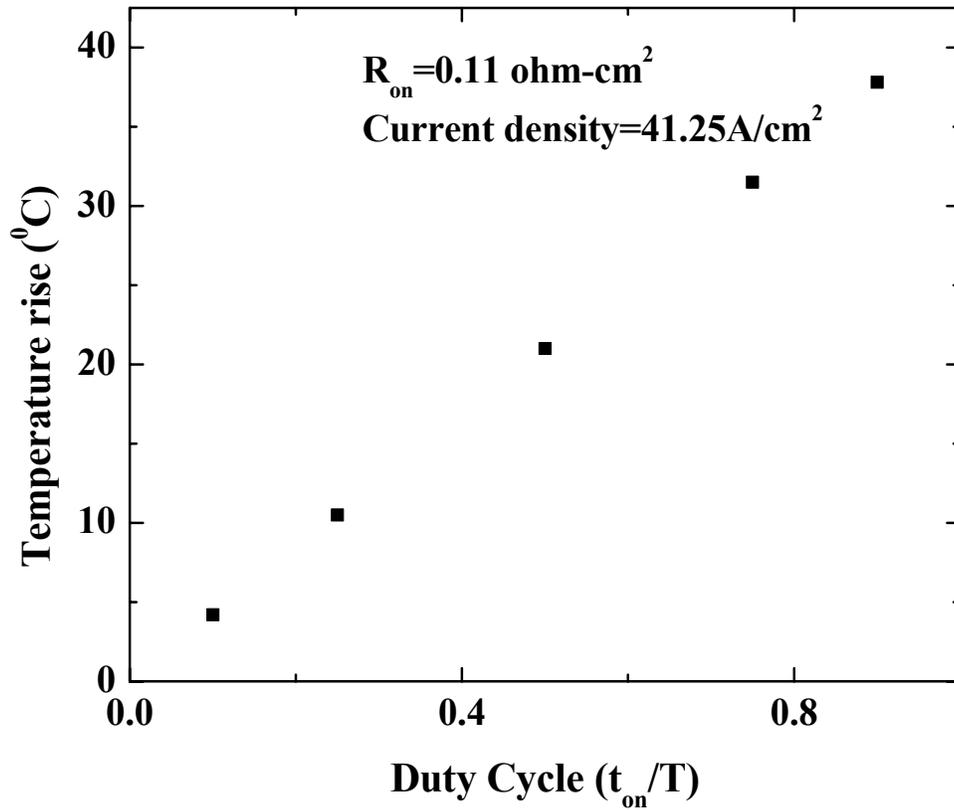


Figure 5-17. Temperature rise above ambient of flip-chip bonded rectifier as a function of duty cycle for a fixed current density of 41.25 A/cm^2 and on-state resistance of $0.11\text{ }\Omega\text{-cm}^2$

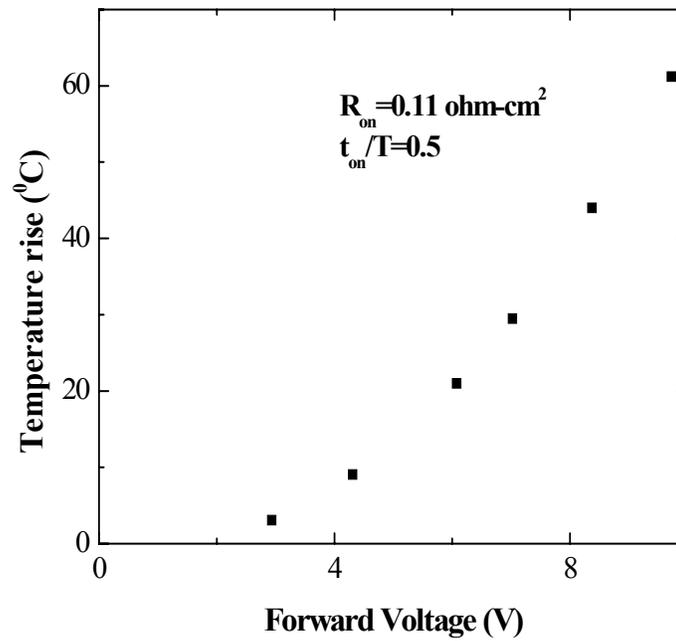
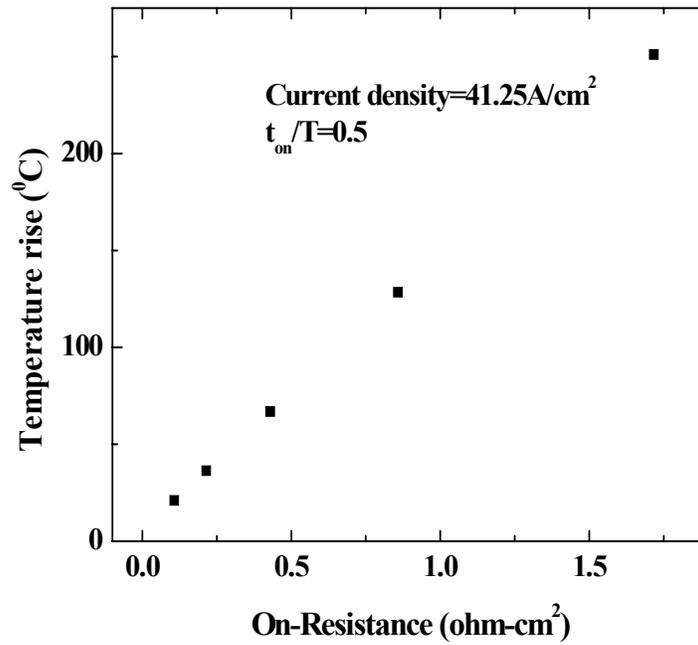


Figure 5-18. Temperature rise above ambient of flip-chip bonded rectifier as a function of a) on-state resistance for a duty cycle of 0.5 and current density of 41.25 A/cm² and b) forward bias at a fixed on-state resistance of 0.11 Ω -cm²

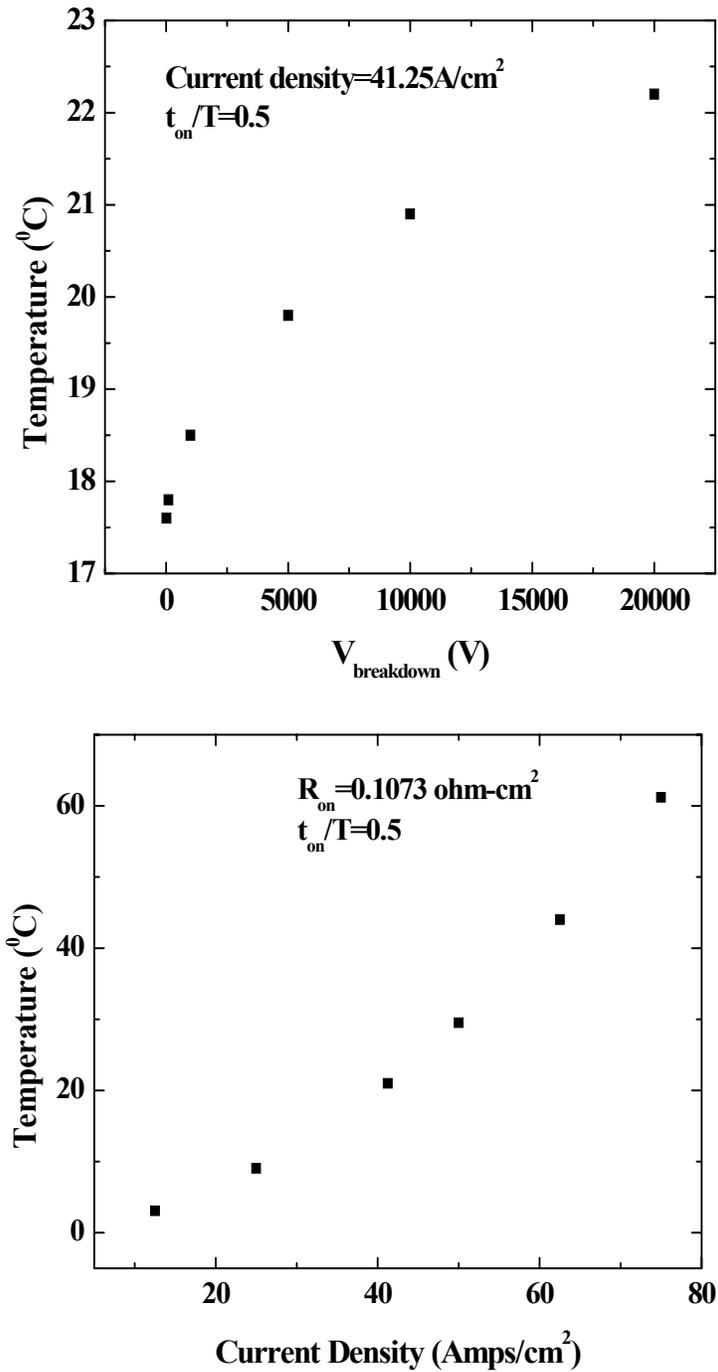


Figure 5-19. Temperature rise above ambient of flip-chip bonded rectifier as a function of a) breakdown voltage for a duty cycle of 0.5 and current density of 41.25 A/cm^2 and b) current density for a fixed on-state resistance of $0.11 \text{ } \Omega\text{-cm}^2$

Summary

Finite difference method was used to analyze the thermal characteristics of continuous wave (CW) 850 nm AlGaAs/GaAs Implant-apertured vertical-cavity surface-emitting lasers. A novel flip-chip design was used to enhance the heat dissipation. The temperature rise in the active can be maintained below 40 °C at 4 mW output power with 10 mA current bias. In the contrast, the temperature rise reaches above 60 °C without flip-chip bonding. The transient-temperature during turn-on of a VCSEL was also investigated. The time needed for the device to reach the steady-state temperature was in the range of a few tenths of a milli-second, which is orders of magnitude larger than the electrical or optical switch time. Flip-chip bonding will reduce the shift of the wavelength, peak power, threshold current and slope efficiency during VCSEL operations.

Flip-chip bonding allows for use of dielectric mirror along with improved heat dissipation in our proposed 1550 nm VCSEL design. Low operating temperatures in a VCSEL ensures less shift of the wavelength, higher peak power, lower threshold current and higher slope efficiency. Finite element analysis was used to analyze the thermal characteristics of continuous wave (CW) 1550 nm InAlGaAs active region double-intracavity-contacted flip-chip bonded vertical-cavity surface-emitting lasers with InP cladding layers. A novel flip-chip design was used to enhance the heat dissipation. The temperature rise in the active region can be maintained below 16 °C at 1 mW output power with 10 mA current bias. Dielectric DBRs on top and bottom are used in our design, with bottom DBR deposited after removing InP substrate. The time needed for the device to reach the steady-state temperature was in the range of a few tenths of a

milli-second, which is orders of magnitude larger than the electrical or optical switch time. Flip-chip bonding will reduce the shift of the wavelength, peak power, threshold current and slope efficiency during VCSEL operations.

A finite element simulation was needed to quantitatively estimate the effectiveness of flip-chip bonding in the temperature rise of bulk GaN Schottky rectifiers under various conditions of current density, duty cycle and on-state resistance. The temperature difference between flip-chip bonded devices and bottom bounded devices was ≥ 20 °C at modest current densities. The maximum temperature in the bulk cases occurred in the center of the GaN substrate thickness. Flip-chip bonding is suggested to improve the heat dissipation of high power, bulk GaN rectifiers.

CHAPTER 6 CONCLUSION

This study investigates GaN based power devices (diodes, HEMTs and MOSHEMTs, passivated HEMTs), GaN sensor devices, InGaAs based MSM Photodetectors and OE mixers, thermal and electrical simulation of GaN based power devices, thermal simulation of AlGaAs/GaAs and InGaAs based Vertical Cavity Surface Emitting Lasers (VCSELs), and electrical simulation of InGaAs OE mixers.

Sc₂O₃ thin films deposited on GaN and AlGaN by MBE provide high quality oxide/semiconductor interfaces for AlGaN/GaN HEMT structures. Sc₂O₃ was shown to act simultaneously as the gate dielectric and surface passivation layer. Sc₂O₃, which is free of hydrogen, may have an advantage in terms of long term stability as compared to the dielectrics deposited using SiH₄ or other hydrogen containing precursors. The maximum drain source current, I_{DS}, of the Sc₂O₃/AlGaN/GaN based MOSHEMT reached over 0.8 A/mm and was ~ 40% higher than that of conventional HEMTs fabricated on the same wafer. The threshold voltage of the MOSHEMTs was in good agreement with the theoretical value, indicating that Sc₂O₃ retains a low surface state density on the AlGaN/GaN structures, and effectively eliminates the collapse in drain current seen in unpassivated devices. The MOS-HEMTs could be modulated to +6 V of gate voltage. Sc₂O₃ has a bixbyite crystal structure, large bandgap (6.3 eV) and high dielectric constant, which make it favorable for use as gate dielectric.

MgO was also used for nitride HEMT passivation, and showed promising results. HEMTs with GaN-cap layer provided more effective mitigation of drain current collapse

than AlGaIn-capped HEMT, however MgO passivated HEMT showed some degradation after a month. On the contrary, Sc₂O₃ provided stable passivation characteristics over a period of at least 5 months. By comparing power characteristics of AlGaIn/GaN MOSHEMTs with Sc₂O₃ gate dielectrics to that of conventional metal-gate HEMTs fabricated on the same material, it was found that the MOSHEMT showed significantly higher power-added efficiency (27%) as compared to the HEMT (~5%). The power added efficiency also increased (from ~5 to 12%) for the surface passivated HEMTs, showing that Sc₂O₃ is an attractive option for reducing gate and surface leakage in AlGaIn/GaN heterostructure transistors.

An ungated AlGaIn/GaN high electron mobility transistor structure was used for sensing different liquids. The ungated HEMTs showed dramatic changes in drain–source current upon exposure to polar liquids in the gate region. Bonding of polar liquid molecules appeared to alter the polarization-induced positive surface charge, leading to changes in the channel carrier density and hence to the drain–source current. The forward current showed significant decreases upon exposure of the gate area to solvents (water, acetone) or acids (HCl). The results indicated that nitride-based heterostructures could be used for the applications in integrated chemical, gas and fluid monitoring sensors.

The effect of the deposition conditions on the electrical properties of W/Pt/Au Schottky contacts on n-GaN was investigated. The W/Pt/Au metal stack employed was particularly relevant for applications in gas sensing because Pt is used to catalytically decompose H₂ gas, while W provides a high-temperature stable contact for the GaN. Sputter-deposited W Schottky contacts on n-GaN showed as-deposited barrier heights (ϕ_b) of 0.80 eV for optimized conditions. After subsequent annealing at 500-600 ° C, the

barrier height was reduced to ~ 0.4 eV. At higher annealing temperatures W reacted with GaN to form β -phase W_2N , which results in a lower Schottky barrier height. The lowest specific resistance for sputtered W contacts was obtained for high power, low pressure (< 20 mTorr) deposition conditions (where the incident ion energy and deposition rate are optimum for minimum damage to the GaN surface).

InGaAs based $1.55 \mu\text{m}$ MSM photodetectors and opto-electronic mixers were fabricated with very low dark current ($< 1\text{nA}$) at room temperature. A 3dB bandwidth of 24 GHz was obtained for the high speed testing. A planarization etch-back process was also developed, which showed a low dark current and good photo-response. The optoelectronic (OE) mixing effect in InAlAs Schottky-enhanced InGaAs-based MSMPDs was analyzed, and the measured frequency bandwidth of the mixer was less than that of the corresponding photodetector. The mixing efficiency depended on the light modulation and mixed signal frequencies and decreased non-linearly with the input optical power. M_{eff} decreased as LO frequency was increased and it increased as IF frequency increased. As optical power decreased, M_{eff} also decreased. A circuit model of the OE mixer was proposed to predict the dc and ac results, which agreed with the experimental ones very well.

The optoelectronic mixing characteristics of InAlAs, Schottky-enhanced, InGaAs-based MSMPDs were also studied. M_{eff} of MSM-PD OEMs depends on the thickness of the InAlAs SEL. For thick SELs ($\approx 500\text{\AA}$), the bandwidth of a MSM-PD OEM was much less than that of the corresponding MSM-PD. Decreasing the thickness of the SEL to 100\AA improved the mixing characteristics of the MSM-PD OEM. The bandwidth of the OEM was similar to that of the corresponding photodetector and the mixing efficiency

was found to decrease only slightly with decreased optical power for 100 Å SEL OE mixer. CFDRC software was used to simulate MSM photodetector and OE mixer response under illumination with 1.50 μm LASER. The simulated results show the effect of light intensity and SEL thickness on photodetector response.

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BIOGRAPHICAL SKETCH

Rishabh Mehandru received his B.Tech degree in chemical engineering from Indian Institute of Technology. In year 2000, he became a graduate student at the University of Florida working in the area of compound semiconductors with Professor Fan Ren. He has contributed to 24 papers so far in this area. His main role has been in the development of Sc_2O_3 and MgO as surface passivation films and as gate dielectrics for power devices. He has also played a major part in developing state of the art opto-electronic mixers in collaboration with Army Research Lab.