FABRICATION AND CHARACTERIZATION OF MULTIPLE FLEXIBLE MAGNETIC WINDINGS

By

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A THESIS PRESENTED TO THE GRADUATE SCHOOL OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF SCIENCE

UNIVERSITY OF FLORIDA

2001
ACKNOWLEDGMENTS

I would like to thank my advisor, Dr. Khai D. T. Ngo for his interest and patience during the work for this thesis. His approach to problem solving and knowledge of practical issues made this work possible. He helped me to understand the process of engineering. I would also like to thank Dr. Alexander Domijan and Dr. Vladimir A. Rakov for all of their suggestions and for being on my advisory committee. I would also like to thank Dr. Charlie Korman, Dr. John A Mallick, Richard J Saia, and Sriram Ramakrishnan of General Electric Corporation for their funding in this research. Thanks are also due to Paiboon Nakmahachalasint, June Chen, and Mehul Shah for their help and camaraderie. I would like to place on record my appreciation and gratitude to the Bangladesh University of Engineering & Technology, Dhaka for the opportunity to study and learn in an environment that made it all fun. Finally, I thank my family for their love and support.
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Abstract of Thesis Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Master of Science

FABRICATION AND CHARACTERIZATION OF MULTIPLE FLEXIBLE MAGNETIC WINDINGS

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December 2001

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Major Department: Electrical and Computer Engineering

Flexible circuits are used for magnetic components to reduce size and weight and to increase power density. The flex foils are basically built using conductor and insulator materials. Among the conductor materials, probably the best solution is copper because it presents a good trade-off between electrical characteristics and cost. Because the insulator material needs good mechanical characteristics, it should be chosen carefully. When designing flex circuits, many factors must be considered, such as mechanical performance and electrical performance. The bend radius is the most important mechanical characteristic for this particular application.

This thesis presents the design, fabrication, and characterization of a five-winding transformer using a flex circuit. This design technique deals with the trade-off among core size, core loss, ease of manufacturing and folding; the minimum number of layers; and the winding assembly so that the terminations of the primary and secondary fall on both sides of the core. This method virtually eliminates
external soldering or conductive vias, thus reducing dc resistance and cost and increasing reliability. The designed transformer has twelve turns in the primary winding and twelve turns in the reset winding. The secondary windings have nine, five, and six turns. Before fabrication, the layout of the transformer was done in AutoCAD and the details of the layout were presented. A planar E core (E18/4/10) was used to design the transformer. The dc resistances of 91 mΩ, 1210 mΩ, 125 mΩ, 49 mΩ, and 108 mΩ were obtained for the primary, reset, nine-, five-, and six-turn windings, respectively. The transformer is modeled by using the Extended Cantilever Model (ECM) approach.
CHAPTER 1
INTRODUCTION

1.1. Background

Magnetic components are often fabricated using planar windings on printed circuit boards [1], flex circuits [2], and hybrid circuits [3] because of the trend toward miniaturization of electronic components. Compared to the conventional transformers/inductors, planar transformers/inductors have lower packaging profiles and higher power densities [4]. Planar windings using multilayer PCB (ML-PCB) have been reported in [5], but the number of turns of windings that can be placed in series is limited and is determined by the core type. This approach is not suitable for windings with a large number of turns and a high degree of interleaving.

The flex circuit is presented as a method to fabricate a winding assembly with a large number of conductive and insulating layers [6-12]. However, no detailed scheme is presented using 2D-folding for multiwinding magnetic components where several trade-offs exist including core size, core loss, ease of manufacturing and folding of flex circuits, and the minimum number of layers. This thesis deals with these issues. A five-winding transformer is laid out, fabricated, and modeled.

Two-dimensional (2D) folding is defined as the folding pattern in which the flex circuit is folded both along the x-axis and y-axis. A fabricated flex circuit for a five-winding transformer is shown in Figure 1-1. Figure 1-1 shows that to get the
required number of turns, the flex circuit should be folded both along the x-axis and y-axis; that is, the folding is two-dimensional (2D).

The advantages of 2D folding are as follows:

• It avoids long flex circuits that usually result if the turns are constrained to a 1D layout.

• It avoids a large number of separate flex circuits that need to be assembled. In fact, it might be possible to lay out all the windings on a single flex circuit.

• It minimizes the number of vias used. In fact, all the patterns shown in Figure 1-1 require no via. A via is used to connect the isolated copper pattern that will be in series.
In order to reduce the manufacturing cost, the number of layers should be kept at a minimum. One way to accomplish this is to put several windings on the same layer as shown in Figure 1-1. In addition, several half-turns (or fractional turns, in general) of the same winding can be put in the same layer.

Another way to reduce the number of layers in a winding stack is to increase the number of fractional turns on each layer. For instance, if a 5/6 turn is put on each layer, the 5/6 turn winding pattern shown in Figure 1-2 results. This pattern uses space more efficiently. That is, it covers most of the winding area on each side of the flex circuit with copper. Thus, for a given number of series turns, the number of 5/6-turn layers would be almost half of the number half-turn layers. Six folding edges are hexagonally distributed along the circumference of the winding stack. Copper build-up along the folding edges would be less than in the half-turn patterns, and planarization would be less of a problem.

1.1. Thesis Chapter Synopses

Different types of flex circuits are discussed in Chapter 2. Also discussed are some process rules and their advantages and limitations in keeping with the aim of this study. Layout and fabrication of a five-winding prototype transformer are detailed in Chapter 3. The folding sequence is also described.
A model of the transformer [13] and experimental results are presented in Chapter 4. The procedure to implement the ECM in a circuit simulator is also briefly described. Chapter 5 draws conclusions from the results and discusses insights obtained from this work. Finally, it proposes possible future directions that may be explored.
CHAPTER 2
FLEX MANUFACTURING

The flex circuits basically are built using conductor and insulator materials. Among the conductor materials, the use of copper probably is the best solution because it presents a good trade-off between electrical characteristics and cost. Because the insulator material needs good mechanical characteristics in order to allow folding with no cracking problems, its selection is more complicated. Usually kapton, which is chemically a polymide, is used as the insulator because of its good electrical, thermal, and mechanical properties.

2.1. Types of Flex Circuits

There are two types of flex circuits: single-sided flex and multi-sided flex. The single-sided flex circuit has one conductive layer on a flexible insulating layer and can be fabricated with or without coverlayers. Single-sided flex circuits are less expensive. The single-sided flex circuit is shown in Figure 2-1(b).

The multi-sided flex circuit has two or more conductive layers with a flexible insulating layer between two conductive layers and can be fabricated with or without coverlayers. Connections between conductive layers are provided by platted through-holes. Access holes or exposed pads without covers may be on either or both sides. The multilayer flex circuit is shown in Figure 2-1(a).
2.2. Some Process Rules

Building a flex-circuit generally involves employing the same steps from circuit to circuit. However, certain circuit design can add cost. Access holes and supplementary layers add cost. Usually the cost is comparable to the number of layers. The higher the number of layers, the higher the cost. For example, two double-sided circuits could potentially be less expensive than one four-layer multi-sided circuit. Circuits can also be folded in order to save space and layers.

2.2.1. Material Sizes in Flex circuits

Material sizes [14] used in flex circuits are listed in Table 2-1.

<table>
<thead>
<tr>
<th>Material</th>
<th>Sizes (milli inch)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insulator</td>
<td>0.5, 1, 2, 3, 5</td>
</tr>
<tr>
<td>Conductor</td>
<td>0.7, 1.4, 2.8, 4.2</td>
</tr>
<tr>
<td>Adhesive</td>
<td>0.5, 1, 3, 4</td>
</tr>
</tbody>
</table>

2.2.2. Design Rules

Some design rules [14] are given in Table 2-2.

<table>
<thead>
<tr>
<th>Function</th>
<th>Minimum Value (mili inch)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conductor width/spacing</td>
<td>5 for 1 ounce copper, 7 for 2 ounce copper</td>
</tr>
<tr>
<td>Trace to edge spacing</td>
<td>5</td>
</tr>
<tr>
<td>Inner radius for holes or slots</td>
<td>12.5</td>
</tr>
<tr>
<td>Conductor width</td>
<td>5 times greater than the thickness</td>
</tr>
</tbody>
</table>

Figure 2-1. Types of flex (a) double-sided; (b) single-sided
2.2.3. Improving Flexibility and Bend Radius

Single-sided circuits are probably the best choice for dynamic (flex-in-use) applications. Generally, multilayer circuits are better suited to static applications where the circuit is folded only during installation. The minimum allowable bend radius of a multi-sided flex is six times the overall thickness. Roughly, the circuit thickness is slightly smaller than the sum of the insulator, adhesive, and cover layers. Some possibilities to improve flexibility include:

• Circuits with two layers or more selectively plated to improve dynamic flexibility

• Keeping the number of bends to a minimum

• Conductors staggered to avoid an I-beam effect, and routed conductors perpendicular to a bend

• Pads or through-holes not be placed in bend areas

• Factory forming as a considered option. Most constructions can be factory formed depending on the geometry. Because circuits are flexible, formed circuits will relax in time. Form tolerances apply only to the part in the constrained position.

• Preferable not to place conductor, discontinuities in the cover or other stress concentrating features near any bend location.

• Unbonded layers in a relatively thick multilayer or rigid-flex circuit are an option in order to improve flexibility, but this may be more expensive.

2.2.4. Tear Stops

Polymide presents a high initial tear strength, but once a tear starts, it propagates easily. All inside corners must be radiused. The larger the inside radius, the greater the tear strength. If tearing is a concern, polymide-insulated circuits can be designed at the inner corners for corners of 120° or less. Internal or external
polymide or Teflon tear stops can be incorporated. Polymide or Teflon tear stops will add to circuit cost.

2.2.5. Circuit Pattern

For ease of manufacturing, flaring of lines into pads is necessary when the pad is unsupported by the coverlay. This is done to provide strain relief at the pad/line intersection to prevent broken conductors. For ease of manufacturing, sudden expansion or reduction in conductor width is not recommended. Acute angle copper pattern is also not recommended, as shown in Figure 2-2.

2.3. Flex Circuit Fabrication Process

Flex circuit fabrication process can be broken down into five separate production steps [15,16]. Each is described separately.

2.3.1. Computer Aided Design Translation

The flex circuit can be manufactured directly from CAD data (usually Gerber files). A PC based software translates Gerber data into a plot file. This plot file is
electronically sent to the Plotter/Etcher. In the Plotter/Etcher, a high precision ink jet print head images the circuit onto a flex circuit material.

2.3.2. Etching

After the circuit design has been imaged onto the flex material, the film is then forwarded using a positive drive motion control system into a cascading etch tank in front of the Plotter/Etcher. Once the film has been loaded into the etch tank, the Plotter/Etcher automatically starts a preset etch cycle. The flex circuit is sprayed with sodium persulfate. The sodium persulfate, etches away all of the exposed copper, leaving only the protected circuit design on the film. After the etch cycle is complete, the film is sprayed with a fresh water rinse. This rinse removes any active etchant still deposited on the circuit. The flex circuit is then forwarded out of the Plotter/Etcher.

2.3.3. Solder Masking

After the flex circuit has been removed from the Plotter/Etcher, a cover layer is used to protect the circuit from bridging or electrical gaps.

Figure 2-3. Small rectangle (in cm)
2.3.4. Alignment and Lamination

After solder masking, the layers are aligned with the alignment punch. Once aligned, the layers are then laminated in heat seal press.

2.3.5. Drilling

The laminated board is then placed in high performance driller for through hole drilling and final board routing.

\[\text{Figure 2-4. The large rectangle}\]

2.4. Definition of Terms

2.4.1. Small Rectangle:

A small rectangle contains only one hole as shown in Figure 2-3.
2.4.2. Large Rectangle:

A large rectangle contains three vertical rectangles as shown in Figure 2-4.
CHAPTER 3
LAYOUT DESCRIPTION AND FABRICATION OF THE FIVE-WINDING TRANSFORMER

Before the layout of the transformer, the core should be selected according to the requirements such as power, number of turns, power loss, duty ratio of the converter, operating frequency, power carried by different windings, voltage and current of different windings, and so forth. The specifications of the transformer are shown in Table 3-1. The primary and reset windings are referred to as windings \( W_1 \) and \( W_2 \), respectively, and the nine-, five-, and six-turn secondary windings are referred to as \( W_3, W_4, \) and \( W_5 \), respectively. Since the transformer fabricated is supposed to be used in a multiple output forward converter, the reset winding will be used to reset the converter. According to the specifications, core E18/4/10 [17], which is a planar E core, was selected by using Mathcad [18], and by using equations from [19]. The material of the core is 3F3 ferrite. The cross-sectional view of the core E18/4/10 is shown in Figure 3-1.

3.1. Description of Layout

The layout of the transformer was done by AutoCAD [20]. The layout of the primary and the reset winding was done in one flex and the layout of the secondary windings was done in another flex. The two flexes can be fabricated either in single-sided flex or in double-sided flex. For the rest of the thesis, the first flex will be
referred to as primary and reset windings and the second flex will be referred to as secondary windings.

![Diagram of flexes](image)

Figure 3-1. Planar core (E18/4/10). (a) Top view (b) Bottom view

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</tr>
<tr>
<td>W₁</td>
</tr>
<tr>
<td>W₂</td>
</tr>
<tr>
<td>W₃</td>
</tr>
<tr>
<td>W₄</td>
</tr>
<tr>
<td>W₅</td>
</tr>
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<td>Power loss</td>
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After trying in different methods, it was decided to use 24 small rectangles where a small rectangle is defined in Section 2.4.1. The holes and folding lines of the first and second flexes are shown in Figure 3-3. The hole dimensions of the flexes are determined by the size of the core. Figure 3-1 shows the dimensions of the middle leg of the core as 10 mm x 4 mm. Since it was determined that the Kapton and the copper, should not touch the core, a clearance of 0.15 mm was chosen between the Kapton and the core. If the copper touches the core, it might short the core. So the
hole dimensions were chosen as 10.3 mm x 4.3 mm. Figure 3-1 shows that the corners of the leg of the core are rounded. So the corners of the hole were also rounded. According to Section 2.2.2, the minimum round radius should be 12.5 mils. So a round radius of 31 mils was chosen. The zoom-in view of the hole with its dimensions is shown in Figure 3-5. To determine the dimensions of the small rectangles, the dimensions of the first rectangle should be determined first. The dimensions of the first rectangle are determined by the size of the core, too. Figure 3-1 shows that the maximum dimensions of a small rectangle can be 14 mm x 20 mm. To make sure there is a clearance of 0.15 mm between the Kapton and the core, the dimensions of the first small rectangle were chosen as 13.7 mm x 19.7 mm. Figure 3-3 shows that though there are 24 small rectangles, each of the three vertical small rectangles can be grouped as one large rectangle. So there are eight large rectangles in each of the flex, and the dimensions of the first large rectangle should be 13.7 mm x 3*19.7 mm, that is, the width and height are 13.7 mm and 3*19.7 mm. The first large rectangle is shown in Figure 3-6 with its dimensions. To align the holes after
the folding of the flex, the height of all large rectangles should be same. The width of the large rectangles can be different, but this should not affect the alignment of the holes. There are folding lines between all small rectangles.

The width of the large rectangles is made in a long-short pattern so that, upon folding, two consecutive folding edges do not fall on top of each other. By doing this, the jam-
ming of copper along the folding edges can be avoided. The width of each large rectangle is determined by the following equations:

\[
w_n = a, \quad n=1, 2, 6, 10 \tag{3.1}
\]

\[
w_n = a - b, \quad n=3, 5, 7 \tag{3.2}
\]

\[
w_n = a - 2b, \quad n=4, 8, 12 \tag{3.3}
\]

where \( w_n \) is the width of the \( n^{th} \) large rectangle, \( a \) is the width of the first large rectangle, and \( b \) is the length, which is shorter than the width of the first large rectangle. For the designed transformer, \( a \) and \( b \) are shown in Figure 3-4.

Figure 3-4. Width of the large rectangles

Figure 3-3 shows that the width of the large rectangles are determined by equations 3.1 to 3.3, and these equations can be applied for any number of large rectangles. For example, for \( n=3 \), the width of the 3rd large rectangle is 12.7 mm
(13.7 mm-1 mm) by using the Equation (3.2). In the design of the transformer, the value of ‘b’ was chosen to be 1 mm.

As previously discussed, there are two flex circuitries. The first flex circuit contains primary and reset windings, and the second flex circuit contains nine-, five-, and six-turn secondary windings. To understand the copper pattern of the windings clearly, each is described separately.

As shown in Figure 3-7, the primary winding starts at terminal P+ and ends at terminal P-. The serpentine copper pattern follows around 24 apertures to make twelve turns, according to the specifications as shown in Table 3-1. Figure 3-8 shows the layout of the reset winding which starts at terminal R+ and ends at terminal R-. The serpentine copper pattern follows around 24 apertures to make 12 turns, according to specification.

The nine-turn secondary winding starts at terminal 9+ and ends at terminal 9-, and the serpentine path follows 12 apertures to make nine turns as shown in

Figure 3-5. Hole dimensions in cm
Figure 3-9. The five-turn secondary winding starts at terminal 4+ and ends at terminal 4-, and the serpentine path follows 10 apertures to make five turns as shown in Figure 3-10. During the layout, an effort was made to increase the width of this five-turn winding because it carries more current. The six-turn secondary winding starts at terminal 6+ and ends at terminal 6-, and the serpentine path follows twelve apertures to make six turns as Figure 3-11.

The copper runs perpendicularly along the folding lines to make the folding easier and the copper is split along the folding lines in order to make the inter-layer
capacitance less and also to fold more easily. The copper pattern is extended outside at the beginning and end of the windings to form pads for the terminations. At the terminations, it is necessary to see the spacing between the copper.

Otherwise, one might short the copper. So at least 2 mm spacing was ensured. Figure 3-7 and Figure 3-8 were combined to form the first flex, as shown Figure 1-1(a) and Figure 3-9 -Figure 3-11 were combined to form the second flex, as shown in Figure 1-1(b). Since two or more windings were fabricated in one flex, a minimum copper spacing of 0.3 mm was chosen, as shown in Section 2.2.2 For all the windings, the copper thickness was 1.4 mils but the width of copper varies. Since the copper width of the reset winding can be smaller, a minimum copper width of 0.3 mm was chosen according to. An effort was made to use all areas of the rectangles for copper so that minimum winding copper loss occurs.

The layout was done in a way such that, after folding, the terminations of the primary and reset windings fell on one side of the transformer core, and the terminations of all the secondary windings fell on the other side of the transformer core. It was also
ensured that two terminations of any secondary winding were next to each other upon folding. By doing this, the length of the wire was reduced during testing of the transformer, and it also made the winding easier to short during the measurement. A primary benefit of this layout is that there are no vias or soldering.

As shown in Figure 3-12, the first flex has Kapton on both sides except where the terminations are. The secondary-winding flex has Kapton on one side except where the terminations are; the other side has exposed copper. It is obvious that the flexes are single-
sided and not double-sided. The single-sided flex was fabricated rather than double-sided because the double-sided flex is more costly. For all windings, the copper at the terminations is covered by solder so that the terminations do not oxidize. It is also seen in Figure 3-12 shows that the Kapton and adhesive thickness are both 0.5 mils. The Kapton and adhesive thickness of 1 mils could be used with less cost; however in order to fit two flexes into the window height of the core (4 mm total for two cores), the Kapton and adhesive thickness of 0.5 mils were chosen.
After folding, the total height of both the flexes were calculated from Figure 3-12 and was 3.536 mm \[ (1.4 \times 2 + 0.5 \times 6) \times 24 \times 10^{-3} \times 25.4 = 3.536 \text{mm} \].

### 3.2. Folding Sequence

The first and second flex of the transformer shown in Figure 1-1 should be folded along the folding lines according to the sequences. Otherwise, the primary and secondary winding flexes cannot be interleaved. The first and second flex of the transformer along with folding lines are shown in Figure 3-3. In Figure 3-3, the dotted lines are the folding lines, and they are numbered from 1 to 9 to maintain a folding order. For both the first and second flex, they are first z-folded along folding lines 1 and 2, as shown in Figure 3-13 and Figure 3-14, respectively.

Then they are z-folded along the folding lines 3, 4, 5, 6, 7, 8, and 9, respectively, as shown in Figure 3-15 and Figure 3-16. The two flexes are folded along folding lines 1...
and 2 first because if they are folded along folding lines 3, 4, 5, 6, 7, 8, and 9 first, it would be difficult to fold flex along the folding lines 1 and 2 because of the thick copper-stack. After folding along the folding lines, the two flexes are unfolded, and the second flex is placed on top of the first flex, to interleave the primary and secondary windings as shown in Figure 3-17. They are then folded again along folding lines 1 and 2 first. Then the folded first small rectangle is inserted in the E18/4/10 core, and then the two coupled windings are z-folded along the folding lines 3, 4, 5, 6, 7, 8, and 9, and then inserted into the core. This was done so that the apertures of the windings become aligned. The complete transformer is shown in Figure 3-18.
Figure 3-16. Second flex folded along Folding Lines 1 and 2 first and then Folding Lines 3, 4, 5, 6, 7, 8, and 9

Figure 3-17. First flex placed on top of the second flex, and Folded along folding Lines 1 and 2 first, then Folding Lines 3, 4, 5, 6, 7, 8, and 9
Figure 3-18. Complete transformer
CHAPTER 4
MODELING OF THE TRANSFORMER

Modeling of multiwinding magnetic components is difficult in view of the cross-coupling among the windings. Analytical expressions are invariably complex and difficult to obtain for such cases. Additionally, such an approach is limited to specific geometries and/or number of windings. Modeling a magnetic component from terminal port measurements is necessary in many cases for verifying or predicting converter dynamics. For applicability, the model has to be sufficiently broad-band to deal with the high frequency nonsinusoidal waveforms present in present-day converters.

The Extended Cantilever Model in [13], modified in [15], [21], and [22] is used to model the transformer. However, the measurement setup itself tends to have parasitic elements that can alter the observed frequency response of the Device Under Test (DUT). The four-point measurement system is preferred for its ability to reduce the effects of parasitic elements. Measurement of leakage impedances in the ECM requires sensing short-circuit currents. This is an extremely stringent condition. In fact, non-idealities in measurement of short-circuit currents can affect the very topology of the impedance being measured. It is important to understand the requirement of a “good short” with respect to the ECM.
4.1. Modeling

An equivalent circuit model is developed that is useful for the simulation of the converter into which the transformer is embedded. The procedure described in [21] is employed to measure the model parameters for the frequency of interest which is 300 KHz.

The model topology, an extended cantilever model (ECM) [13], is shown in Figure 4-1. In ECM, N(N+1)/2 independent parameters are required to model a transformer containing N winding. Each parameter of the ECM can be directly measured. The self-impedance $Z_{11}$ can be measured by open-circuiting $W_2$, $W_3$,..., and measuring the impedance of winding $W_1$. The self-impedance $Z_{11}$ is given by,

![Figure 4-1. Extended cantilever model for a five-winding transformer](image)

\[ \text{Figure 4-1. Extended cantilever model for a five-winding transformer} \]
To measure the effective turns ratios $n_2, n_3, \ldots$, a voltage is applied to winding $W_1$ with other windings open-circuited. The effective turns ratio $n_k$ is given by,

$$ n_k = \frac{v_k}{v_1}, \quad \text{for } k \neq 1, \ 2 \leq k \leq 5 $$

(4.2)

A negative value of $n_k$ indicates that the winding polarity marks should be reversed.

To measure the effective leakage impedance $Z_{jk}$, winding $W_j$ is driven with voltage source $v_j$, while all other windings are short-circuited. It is important that good low-impedance short-circuits be used. The current $i_k$ in winding $W_k$ is measured. The effective leakage impedance is $Z_{jk}$ is given by,

$$ Z_{jk} = \frac{v_j}{n_j n_k^* i_k}, \quad k \neq j; \ v_n = 0, \ n \neq j $$

(4.3)

4.1.1. Basic Measurement Methodology

The measurement of the ratio of the applied voltage to the output current/voltage is the first step in determining the desired transfer function. The actual transfer function is measured as a ratio of the applied and measured waveforms using an Impedance/Gain-Phase analyzer (Figure 4-2). A Hewlett-Packard 4194A Impedance/Gain-Phase analyzer was used to characterize the device under test (DUT). The quantities required for the model have dimensions of resistance (Ohms) for the self and leakage impedances or are dimensionless for the turns ratios. In other words, the applied stimulus is always a voltage, and the observed stimulus is a current for measuring the impedances or a voltage for the turns ratios. Measurement of the current is accomplished using current sense resistors in series with the winding.
being measured. This transforms the measurement of current to a measurement of voltage. For each leakage impedance, a current sense resistor is used to short the winding in order to sense the current in the “short-circuited” winding, as shown in Figure 4-3.

All other windings being excited have true shorts across their terminals. The effects of using current sense resistors in place of a “true short” is discussed in Section 4.2. The two voltages are then fed to the 4194A, and the ratio between the two voltages is scaled by the value of the current sense impedance to obtain the impedance being measured. For the self impedance, the current sense resistor is

Figure 4-2. Basic measurement setup
simply placed in series with the winding to obtain the current through it. These relations can be formally written as follows:

\[ Z_{ij} = \frac{v_{\text{app},i}}{v_{\text{Sense},i} \cdot n_i \cdot n_j} \cdot Z_{\text{Sense}} \]  \hspace{1cm} (4.4)

where \( \frac{v_{\text{Sense},j}}{v_{\text{app},i}} \) is the ratio measured by the 4194A.

The turns ratios are directly measured as the values recorded by the 4194A (Figure 4-4).
It should be noted that all these values are measured across a frequency range of 10 KHz to 1.01 MHz. Then these data were post-processed for 300 KHz.

The self-impedance of the primary winding, $Z_{11}$, is measured using the impedance analyzer, as this would avoid any parasitic effects by using the other measuring systems. Because $Z_{11}$ is large at high frequencies, parallel cable capacitances can cause problems if it is measured in a similar fashion to the leakage impedances.

Figure 4-4. Turn ratio measurement.

$$n_{jk} = \frac{v_{\text{Sense},k}}{v_{\text{app},j}} \tag{4.5}$$
4.1.2. Why Use the Four-point Measurement System?

In this section, the advantages of the four-point measurement system are illustrated using the case of self-impedance measurement. The oscillator of the 4194A typically sources out a sine wave of preset magnitude into the terminals of the DUT. During this measurement, the reference and the test inputs of the 4194A are set to a high impedance level of 1MΩ. The reference and test waveforms are fed back to

![Diagram showing reference waveform being sampled at the terminal where the source waveform is applied](image)

- Figure 4-5. Reference waveform being sampled at the terminal where the source waveform is applied

- the 4194A from the DUT. For the case shown in Figure 4-5, the reference waveform is fed back to the 4194A through a T-connector at the same point the source waveform is being applied to the DUT. In this case, the terminating impedance is 1 MΩ in parallel with a 28 pF Capacitance. Hence, the current in the cables connecting the reference and test potentials to the 4194A will be small. Again, the parasitic drops across the cable will be small. However, the drop across the exciting cable and its interconnects will be substantial as the cable carries the sourcing current, which could be large. In fact, the $Z_{par(s)}i_{src}$ voltage drop shown in Figure 4-5 is now being erroneously fed back as part of the reference voltage $v_{ref}$, instead of the actual voltage $v_p$. 
The four-point measurement system avoids this problem by using separate points for the sourcing and reference voltages (Figure 4-6). This ensures that the reference voltage does not include the parasitics caused by the interconnects as the current in this case is low. While series parasitic effects are avoided, parallel parasitic effects, such as the cable capacitance, can still affect the measurement.

4.1.3. The Measurement Board: Layout and Interconnections

The measurement board was fabricated on a double layer FR4 copper board using a T-Tech circuit board milling machine. Its dimensions are 4”x4”. The board layout is based on the four-point measurement system with an emphasis on keeping the reference and test points close to the actual windings and/or current sense resistors (Figure 4-7). The sourcing inputs are located farther from the test and reference points. Figure 4-8 details the actual layout of the bottom of the test board. All the BNC connections and transformer windings are soldered on the bottom of the board. The current sense impedances or shorts for various test configurations are soldered on the top of the board. The vias on the board connect the windings directly.
to the shorts or current sense impedances. The connections on the top of the board are shown in Figure 4-9.

The BNC terminations shown on the top of the board are connected to the 4194A through specially made short coaxial cables to reduce parasitics. Caddock 10 mΩ current sense resistors (Part No. MP916, [23]) with 5% precision were used for the measurement of leakage impedances. The inductance was estimated in the manufacturer’s data sheets at 7.5 nH. A 10 cm coaxial cable (17 pF capacitance) was used to sense the applied voltage, and a 13 cm coaxial cable (21 pF capacitance) was used to sense the voltage across the current sensor.
4.2. Effect of Nonzero Current Sense Impedances

There are three kinds of measurements to be performed. For the turns ratio measurements, no current sensors are needed. The measurement of the self-impedance $Z_{pp}(s)$ is performed on the impedance analyzer and does not need a current sensor. However, current sensors are needed for the measurement of leakage impedances, and Equation (4.3) requires short circuit conditions at the winding where the current is sensed.

Figure 4-10 shows the actual measurement setup referred to the primary node. If $Z_{sc}(s)$ is to be a good short, at all frequencies,

White= Cu  
Black= Isolation

![Diagram showing interconnects between BNC connectors and transformer ports.](image)

Figure 4-8. Layout diagram of the bottom of the test fixture showing interconnects between the BNC connectors and the various ports of the transformer.
Figure 4-9. Layout diagram of the top of the test fixture showing the BNC terminations.

Figure 4-10. Leakage impedance measurement referred to the primary node
\[ |Z_{sc}(s)| \ll |(Z_{1j}(s) \parallel Z_{2j}(s) \parallel \cdots \parallel Z_{ij}(s) \parallel \cdots \parallel Z_{Nj}(s))| \quad \text{where } Z_{sc}'(s) = \frac{Z_{sc}(s)}{|n_j(s)|^2} \tag{4.6} \]

At low frequencies, the right-hand side of the inequality will be extremely small, and it is difficult to use extremely small current sensors. Also, this is impractical at high frequencies because of the parasitic inductance of the current sense resistor. For instance, a 0.1 Ω surface mount precision resistor would realistically have a series inductance of about 5 nH. At 10 MHz, the imaginary part current sense impedance is approximately 30 mΩ. This would severely distort the measured phase and magnitude response. Hence, we have to change the measurement procedure suitably in order to avoid this problem.

The quantity being measured in Figure 4-10 is the leakage impedance \( Z_{ij}(s) \). The measured leakage impedance \( Z_{ij,mea}(s) \) is given by,

\[
Z_{lm,mea}(s) = \frac{v'_{app}(s)}{i_{sc,j} n_j^*(s)} \quad \text{where } v'_{app}(s) = \frac{v_{app}(s)}{n_l(s)} \tag{4.7}
\]

A relation between the measured and actual impedances can be derived easily by using the admittance equivalent of the measurement circuit in Figure 4-10. The Norton equivalent of the circuit is shown in Figure 4-11.

The short circuit current \( i_{sc}(s) \) is related to the input current \( i_{app}(s) \) by the following relation:

\[
i_{sc}(s) = \frac{Y'_{sc}(s)}{Y_{ij}(s) + Y'_{sc}(s) + \sum_{n=1, n \neq j}^N Y_{nj}(s)} i_{app}(s) \tag{4.8}
\]

where \( i_{app}(s) = Y_{lm}(s)v'_{app}(s) \).
The measured leakage impedance $Y_{lm,mea}(s)$ is given by

$$Y_{lm,mea}(s) = \frac{i_{sc}(s)}{v'_{app}(s)}$$  \hspace{1cm} (4.9)$$

Combining Equation (4.8) and Equation (4.9), we get

$$Y_{lm,mea}(s) = \frac{Y'_{sc}(s)Y_{ij}(s)}{Y_{ij}(s) + Y'_{sc}(s) + \sum_{n=1, n \neq j}^{N} Y_{nj}(s)}$$  \hspace{1cm} (4.10)$$

Simplifying the equation,

$$Y_{ij,mea}(s) \left( 1 + \frac{Y_{ij}(s)}{Y'_{sc}(s)} + \sum_{n=1, n \neq j}^{N} \frac{Y_{nj}(s)}{Y'_{sc}(s)} \right) = Y_{ij}(s)$$  \hspace{1cm} (4.11)$$

Equation (4.11) can be rewritten as

$$Y_{ij}(s) \left( 1 - \frac{Y_{ij,mea}(s)}{Y'_{sc}(s)} \right) \left( Y_{ij}(s) + Y_{2j}(s) + \ldots + Y_{Nj}(s) \right) \frac{Y_{ij,mea}(s)}{Y'_{sc}(s)} = Y_{ij,mea}(s)$$  \hspace{1cm} (4.12)$$

Figure 4-11. Norton equivalent of leakage impedance measurement circuit
Equation (4.12) represents a set of linear equations with one equation formed by each measurement of a leakage impedance. Hence, the number of unknowns (leakage impedances) is equal to the number of equations. The system is, therefore, uniquely determinable. By solving this set of linear equations, we can compensate for the non-ideality of the current-sense resistor. For an ideal short \((Y_{sc'}(s) \to \infty)\), Equation (4.12) reduces to the ideal case as defined in the ECM, i.e., \(Y_{ij}(s) = Y_{ij,\text{mea}}(s)\).

### 4.3. Experimental Results

The transformer constructed has five windings, including the reset one. The primary and reset windings are referred to as winding \(W_1, W_2\), respectively, and the nine-, five-, and six-turn secondary windings are referred to as \(W_3, W_4, W_5\), respectively. The transformer was designed for a 20W, 300 KHz forward converter. The length and width of the windings vary in different segments of the layout. So, the length and width at different segments are calculated from the layout, and then the dc resistances are calculated and summed up to get the total resistance. The dc resistances are calculated from the design Equation (4.13),

\[
R_{dc} = \rho \frac{1}{wt}
\]  

(4.13)

where \(R_{dc}\) is the dc resistance of the winding, \(\rho\) is the resistivity of copper, \(l\) is the length of the winding, \(w\) is the width of the winding, and \(t\) is the thickness of the winding.

<table>
<thead>
<tr>
<th>Windings</th>
<th>Thickness, (t) (cm)</th>
<th>Average width, (w) (cm)</th>
<th>Total length ((cm))</th>
<th>Measured ((m\Omega))</th>
<th>Calculated ((m\Omega))</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1</td>
<td>0.0036</td>
<td>0.278</td>
<td>55.488</td>
<td>91</td>
<td>97</td>
</tr>
<tr>
<td>W2</td>
<td>0.0036</td>
<td>0.020</td>
<td>55.488</td>
<td>1210</td>
<td>1230</td>
</tr>
<tr>
<td>W3</td>
<td>0.0036</td>
<td>0.182</td>
<td>41.616</td>
<td>125</td>
<td>111</td>
</tr>
<tr>
<td>W4</td>
<td>0.0036</td>
<td>0.244</td>
<td>23.120</td>
<td>49</td>
<td>46</td>
</tr>
<tr>
<td>W5</td>
<td>0.0036</td>
<td>0.135</td>
<td>27.744</td>
<td>108</td>
<td>100</td>
</tr>
</tbody>
</table>
After fabrication, the dc resistance was measured by a Keithley 2001 multimeter. The dc resistances are summarized in Table 4-1, indicating good agreement between the measured and calculated values.

To measure the ECM parameters, the transformer was implemented in a test fixture, as shown in Figure 4-12, which is the top of the test fixture. The bottom view of the test fixture is shown in Figure 4-13. The measurement board was fabricated on a double layer FR4 copper board using a T-Tech circuit board milling machine. Its dimensions are 4” x 4”. The board layout is based on the four-point measurement system with an emphasis on keeping the reference and test points close to the actual windings and/or current-sense resistors. The sourcing inputs are located farther from
the test and reference points. Measurements of the extended cantilever model parameters were made, as described in Section 4.1. Hewlett-Packard 4194A Impedance/Gain-Phase analyzer [24] was used to measure all the parameters. The turns ratios were measured using the Gain-Phase function of the HP 4194A. The magnetizing impedance $Z_{11}$ was measured using the Impedance function of the HP 4194A.

Table 4-2  Summary of the ECM parameters measurement at 300 KHz

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Measured Real</th>
<th>Measured Imaginary</th>
<th>Extracted Real</th>
<th>Extracted imaginary</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n_2$</td>
<td>1.010</td>
<td>0.0000</td>
<td>1.01</td>
<td>0.000</td>
</tr>
<tr>
<td>$n_3$</td>
<td>0.760</td>
<td>0.0000</td>
<td>0.76</td>
<td>0.000</td>
</tr>
<tr>
<td>$n_4$</td>
<td>0.420</td>
<td>0.0000</td>
<td>0.42</td>
<td>0.000</td>
</tr>
<tr>
<td>$n_5$</td>
<td>0.510</td>
<td>0.0000</td>
<td>0.51</td>
<td>0.000</td>
</tr>
<tr>
<td>$Z_{11}(\Omega)$</td>
<td>7.3570</td>
<td>651.35</td>
<td>7.36</td>
<td>651.3</td>
</tr>
<tr>
<td>$Z_{12}(\Omega)$</td>
<td>3.383</td>
<td>-1.0500</td>
<td>3.36</td>
<td>-1.060</td>
</tr>
<tr>
<td>$Z_{13}(\Omega)$</td>
<td>0.263</td>
<td>0.0970</td>
<td>0.27</td>
<td>0.100</td>
</tr>
<tr>
<td>$Z_{14}(\Omega)$</td>
<td>0.425</td>
<td>0.3530</td>
<td>0.41</td>
<td>0.360</td>
</tr>
<tr>
<td>$Z_{15}(\Omega)$</td>
<td>0.459</td>
<td>0.1710</td>
<td>0.44</td>
<td>0.175</td>
</tr>
<tr>
<td>$Z_{23}(\Omega)$</td>
<td>2.206</td>
<td>0.5200</td>
<td>2.21</td>
<td>0.510</td>
</tr>
<tr>
<td>$Z_{24}(\Omega)$</td>
<td>6.047</td>
<td>3.1710</td>
<td>6.05</td>
<td>3.170</td>
</tr>
<tr>
<td>$Z_{25}(\Omega)$</td>
<td>9.287</td>
<td>2.4810</td>
<td>9.28</td>
<td>2.475</td>
</tr>
<tr>
<td>$Z_{34}(\Omega)$</td>
<td>1.170</td>
<td>0.9940</td>
<td>1.17</td>
<td>0.992</td>
</tr>
<tr>
<td>$Z_{35}(\Omega)$</td>
<td>1.930</td>
<td>0.6800</td>
<td>1.92</td>
<td>0.680</td>
</tr>
<tr>
<td>$Z_{45}(\Omega)$</td>
<td>1.268</td>
<td>2.1800</td>
<td>1.27</td>
<td>2.170</td>
</tr>
</tbody>
</table>

To measure leakage impedance $Z_{jk}$, the current-sense resistor was used to short winding k in order to sense the current in the “short-circuited” winding k. The other windings j, except the excited winding k, had true shorts across their terminals. The ratio of the voltages across the windings k and j is then measured by the Gain-Phase analyzer. This was scaled by the current-sense admittance and the turns ratios $n_j$ and $n_k^*$ to compute $Z_{jk}$. All voltages were measured at the winding terminals to avoid interconnect and cable parasitics. It is necessary to mention that the value of the current sense resistor is 10 mΩ with 5%-precision and a package inductance of
7.5 nH (Caddock part number MP916 [23]. It is shown in [21] that the measured parameters with current sensor of 50mΩ+15nH, the extracted parameters do not vary much starting at 100 KHz. Since the operating frequency of the designed transformer is 300 KHz, 10mΩ+7.5nH was considered a sufficiently good “short.” The model parameters are summarized in Table 4-2.

To verify the measured ECM parameters, the transformer model was generated in PSPICE [25]. All the impedances were modeled as resistance in series with inductance except Z_{12} because it has a negative imaginary component. Since PSPICE cannot use negative inductance, L_{12} is implemented by using an inductance
An inductance block is generated using a Voltage-Current \( G(s) \) block (Glaplace, Figure 4-14).

The ideal transformer in Figure 4-14 was implemented by using a voltage controlled voltage source (VCVS) and a current controlled current source (CCCS) connected in an antiparallel sense. The voltage controlled voltage source transforms the primary voltage to the secondary, and the current controlled current source transforms the secondary current to the primary. Since the transformer terminals cannot be shorted to reproduce measurement results, as this would lead to topological and convergence errors, the transformer was shorted by using a 10n\( \Omega \) resistor when needed. The gain multiplier was set to the turns ratio. To verify the implemented ECM, 15 virtual experiments were performed on PSPICE. The schematic generated on PSPICE, along with the ECM parameters, is shown in Figure 4-15. All virtual experiments generate virtually the same data as the actual experiments, shown on Table 4-2.
A transient simulation was performed in PSPICE using the schematic as shown in Figure 4-15. A square wave of 300 KHz was applied at the input of the primary winding. All other windings were open-circuited except the six-turn secondary winding. A 0.5Ω load was connected across the six-turn winding. To make the open circuit, a 1e9Ω resistance was connected across the reset, nine-, and five-turn windings. The simulation waveforms of the voltages across all windings are shown in Figure 4-16 in which Vin, V3, V4, and V5 are the voltages across the primary, nine-, five-, and six-turn windings, respectively. As seen from the waveforms, the voltage rise time and overshoot at the primary winding are 7.35 ns and 110%, respectively. The rise time of the voltage at the six-turn winding is 37.6 ns, and there is no ripple. Since all other windings are open-circuited, the voltages basically follow the voltage at the primary winding. The overshoot is defined by the
The following equation:

\[ \text{Overshoot} = \frac{(y_1 - y_2)}{y_2} \times 100 \]  

(4.14)

where \( y_1 \) is the maximum value of a waveform and \( y_2 \) is the final value of a waveform.

Figure 4-16. PSPICE transformer winding voltage waveforms. (a) ECM model (dotted lines). (b) Ideal PSPICE model (solid lines)
The transformer was tested, as shown in Figure 4-12, to reproduce the simulated voltage waveforms. It was exactly the same setup as the simulation shown in Figure 4-15. The experimental waveforms are shown in Figure 4-17 in which ch1, ch2, ch3, and ch4 are the voltages across the primary, nine-, five-, and six-turn windings. The rise time and the ripple at voltage of the primary winding were 8 ns and 110%, respectively, which are consistent with the simulated values. The rise time of the voltage at the six-turn winding is 38 ns and there is no ripple. This value is also consistent with the simulated values.
CHAPTER 5
CONCLUSION

5.1. Summary

The practical design issues of multiple flexible magnetic windings for magnetic components and their fabrication techniques were studied. A flexible five-winding transformer was fabricated, and the dc resistances and the ECM parameters were measured. It is very important to use the correct values of the resistance and parasitic inductance values to measure ECM parameters, otherwise one might get unreliable values of ECM parameters. The key results are summarized as follows:

• The dc resistances of primary, reset, nine-, five-, and six-turn windings were 97 mΩ, 1230 mΩ, 111 mΩ, 46 mΩ, and 100 mΩ, respectively.

• The transformer was modeled by ECM parameters. Turn ratios of 1.01, 0.76, 0.42, and 0.51 was obtained for the reset, nine-, five-, and six-turn windings.

• To verify the measured ECM parameters, the transformer model was generated in PSPICE, and 15 virtual experiments were performed. All virtual experiments generate virtually the same data as the actual experiment.

5.2. Future Work

The following topics require further investigation to understand completely the proposed method of frequency domain modeling:

• A more efficient use of copper as compared to its utilization in the half-turn copper pattern.

• Evolving a topological or procedural procedure in model generation to take care of nonsymmetrical cases, that is, for the cases when the impedances are not bilateral in nature.

• Incorporating large signal core loss and hysteresis dependencies in the model.
• Effect of non-ideal grounds due to the test fixture parasitcs at high frequencies on the measured parameters.

• Obtaining a physical circuit representation or basis from the measured parameters.

• Validation of simulation results with actual hardware testing.
APPENDIX
MATLAB SCRIPT TO CALCULATE THE REAL AND IMAGINARY PARTS OF THE IMPEDANCES

% Load the measurement data
clear all;
V2=loadasc('N2.txt');
V3=loadasc('N3.txt');
V4=loadasc('N4.txt');
V5=loadasc('N5.txt');
V11=loadasc('Z11.txt');
V12=loadasc('Y12.txt');
V13=loadasc('Y13.txt');
V14=loadasc('Y14.txt');
V15=loadasc('Y15.txt');
V23=loadasc('Y23.txt');
V24=loadasc('Y24.txt');
V25=loadasc('Y25.txt');
V34=loadasc('Y34.txt');
V35=loadasc('Y35.txt');
V45=loadasc('Y45.txt');

% Defining frequency data
f=100e3:2.5e3:1.01e6;
f=f';

% Creating Vectors for Magnitude and Phase of the measured data
N2g=V2(37:401);
N2p=V2(438:802);
N3g=V3(37:401);
N3p=V3(438:802);
N4g=V4(37:401);
N4p=V4(438:802);
N5g=V5(37:401);
N5p=V5(438:802);
Z11g=V11(37:401);
Z11p=V11(438:802);
Y12g=V12(37:401);
Y12p=V12(438:802);
Y13g=V13(37:401);
Y13p=V13(438:802);
% Defining the current sense resistor
I=sqrt(-1);

% Defining the current sense resistor
Zsk=.01+f.*2*pi*7.5e-9*I;
Ysk=1./Zsk;

% Obtain magnitude and phase of magnetizing impedance
Z11g=(abs(Zsk))./Y11g;
Z11p=(180/pi)*angle(Zsk)-Y11p;

% Obtain magnitude and phase of leakage impedance
Z12g=1./(Y12g.*N2g.*abs(Ysk));
Z12p=-Y12p-N2p+180/pi*angle(Ysk);
Z13g=1./(Y13g.*N3g.*abs(Ysk));
Z13p=-Y13p-N3p+180/pi*angle(Ysk);
Z14g=1./(Y14g.*N4g.*abs(Ysk));
Z14p=-Y14p-N4p+180/pi*angle(Ysk);
Z15g=1./(Y15g.*N5g.*abs(Ysk));
Z15p=-Y15p-N5p+180/pi*angle(Ysk);
Z23g=1./(Y23g.*N2g.*N3g.*abs(Ysk));
Z23p=-Y23p-N2p-N3p+180/pi*angle(Ysk);
Z24g=1./(Y24g.*N2g.*N4g.*abs(Ysk));
Z24p=-Y24p-N2p-N4p+180/pi*angle(Ysk);
Z25g=1./(Y25g.*N2g.*N5g.*abs(Ysk));
Z25p=-Y25p-N2p-N5p+180/pi*angle(Ysk);
Z34g=1./(Y34g.*N3g.*N4g.*abs(Ysk));
Z34p=-Y34p-N3p-N4p+180/pi*angle(Ysk);
Z35g=1./(Y35g.*N3g.*N5g.*abs(Ysk));
Z35p=-Y35p-N3p-N5p+180/pi*angle(Ysk);
Z45g=1./(Y45g.*N4g.*N5g.*abs(Ysk));
Z45p=-Y45p-N4p-N5p+180/pi*angle(Ysk);
% Compute real and imaginary parts

N2 = N2g .* exp(I * N2p * pi / 180);
N3 = N3g .* exp(I * N3p * pi / 180);
N4 = N4g .* exp(I * N4p * pi / 180);
N5 = N5g .* exp(I * N5p * pi / 180);
Z11 = Z11g .* exp(I * Z11p * pi / 180);
Z12 = Z12g .* exp(I * Z12p * pi / 180);
Z13 = Z13g .* exp(I * Z13p * pi / 180);
Z14 = Z14g .* exp(I * Z14p * pi / 180);
Z15 = Z15g .* exp(I * Z15p * pi / 180);
Z23 = Z23g .* exp(I * Z23p * pi / 180);
Z24 = Z24g .* exp(I * Z24p * pi / 180);
Z25 = Z25g .* exp(I * Z25p * pi / 180);
Z34 = Z34g .* exp(I * Z34p * pi / 180);
Z35 = Z35g .* exp(I * Z35p * pi / 180);
Z45 = Z45g .* exp(I * Z45p * pi / 180);

R11 = real(Z11);
L11 = imag(Z11);
R12 = real(Z12);
L12 = imag(Z12);
R13 = real(Z13);
L13 = imag(Z13);
R14 = real(Z14);
L14 = imag(Z14);
R15 = real(Z15);
L15 = imag(Z15);
R23 = real(Z23);
L23 = imag(Z23);
R24 = real(Z24);
L24 = imag(Z24);
R25 = real(Z25);
L25 = imag(Z25);
R34 = real(Z34);
L34 = imag(Z34);
R35 = real(Z35);
L35 = imag(Z35);
R45 = real(Z45);
L45 = imag(Z45);

% Compute transfer function coefficients for Z12
[B12, A12] = invfreqs(Z12, f * 2 * pi, 3, 2);
hc12 = freqs(B12, A12, f * 2 * pi);

% Print real and imaginary parts of impedances at 300 KHz
k = 81;
f(k)
\[ \{R_{11}(k) \ L_{11}(k); R_{12}(k) \ L_{12}(k); \ldots; R_{15}(k) \ L_{15}(k); \ldots; R_{23}(k) \ L_{23}(k); R_{24}(k) \ L_{24}(k); \ldots; R_{34}(k) \ L_{34}(k); R_{35}(k) \ L_{35}(k); \ldots; R_{45}(k) \ L_{45}(k)\} \]
REFERENCES


BIOGRAPHICAL SKETCH

Mohammed S. Alam was born on August 30, 1973, in Rangpur, Bangladesh. He received a BS degree in Electrical and Electronics Engineering with an emphasis in Circuit Design from the Bangladesh University of Engineering & Technology, Dhaka (Bangladesh), in August 1997. Since January 1999, he has been pursuing an MS in Electrical and Computer Engineering at the University of Florida in the areas of Power Electronics and Circuit Design. He is also interested in RF IC Design. Other interests include photography and listening to music.