MODELING AND CHARACTERIZATION OF ADVANCED BIPOLAR TRANSISTORS AND INTERCONNECTS FOR CIRCUIT SIMULATION

BY

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LIST OF SYMBOLS

A_C	collector area
A_E	emitter area
A_{Eeff}	effective emitter area
a	emitter-base junction gradient
CC	Coupling coefficient for signal crosstalk
C_{JC}	collector-base junction capacitance
C_{JC0}	collector-base junction capacitance at V_{BE} = 0 V
C_{JE}	emitter-base junction capacitance
C_{JEX}	extrinsic emitter-base junction capacitance
C'_{JE}	derivative of emitter-base junction capacitance
C_{JE0}	emitter-base junction capacitance at V_{BE} = 0 V
C_{SCR}	space-charge region capacitance
C_{SiO2}	SiO_2 capacitance
C_e	even mode capacitance for coupled transmission lines
$C_e{}^a$	even mode capacitance for coupled transmission lines without dielectric interface
C_f	fringing capacitance
C_f'	modified fringing capacitance
C_{gt}	gate capacitance due to finite metal thickness
C_o	odd mode capacitance for coupled transmission lines
$C_o{}^a$	odd mode capacitance for coupled transmission lines without dielectric interface
C_p	plate capacitance

C_{sub}	substrate capacitance
C_2	forward low current nonideal base current coefficient
C_4	reverse low current nonideal base current coefficient
c	speed of light
c_n	Auger coefficient for electron in heavy doping effects
c_p	Auger coefficient for hole in heavy doping effects
E_{FN}	electron quasi-Fermi level
E_{FP}	hole quasi-Fermi level
E_i	intrinsic Fermi level
E_t	trap energy level
f	frequency
f_{BWM}	base width modulation factor
f_C	critical frequency in frequency-dependent permittivity
$f_{CR}(t)$	time-dependent emitter crowding factor
f_{CM}	base conductivity modulation factor
$f_{CROWDING}$	emitter crowding factor without the coupling effects
$f'_{CROWDING}$	emitter crowding factor with the coupling effects
f_c	parameter incorporating the second order effects in the emitter crowding mechanism
fD	critical frequency for frequency-dependent permittivity of coupled transmission lines
$f_{PUSHOUT}$	base pushout factor
f_T	bipolar transistor cut-off frequency
G_{n^+}	conductance of n^+ buried layer
h_1	height of the SiO_2 layer
h_2	height of the substrate
I_B	base current

I_{Bideal}	ideal base current with ohmic drops in the base and emitter regions
I_{Bj}	base current in the partitioned region j
I_C	collector current
I_C^{QNB}	collector current in the base quasi-neutral region
I_C^{QNR}	collector current in the collector quasi-neutral region
I_C^{SCR}	collector current in the collector space-charge region
I_E	emitter current
I_{Ej}	emitter current in the partitioned region j
I_L^{QNR}	lateral diffusion current in the collector quasi-neutral region
I_L^{SCR}	lateral diffusion current in the collector space-charge region
I_K	knee current
I_{KR}	reverse knee current
I_S	collector current at $V_{BE} = 0$ V
I_{SB}	pre-exponential base current
I_{SE}	emitter current at $V_{BE} = 0$ V
L_E	emitter length
J_C	collector current density
$J_E(x)$	position-dependent emitter current density
J_n	electron current density
J_0	onset of the collector current density for base pushout
k	Boltzmann's constant
L_E	emitter length
l	transmission line length
m_c	collector-base junction gradient coefficient
m_e	emitter-base junction gradient coefficient

N_A	acceptor doping density of p-type Si
$N_B(x)$	base doping density at depth x
N_{Beff}	effective base doping density
N_D	donor doping density of n-type Si
N_{EPI}	epitaxial layer doping density
n	nonideal base coefficient
n_c	nonideal collector-base emission coefficient
n_e	nonideal emitter-base emission coefficient
n_i	intrinsic carrier density
n_{ie}	effective intrinsic carrier density
n_0	electron concentration normalized by $N_B(0)$
Δn	excess electron density
P_E	emitter perimeter
p(x,y)	position dependent hole mobility
$\bar{p}$	average excess hole density
Q_{BC}	base-collector charge
Q_{BCX}	extrinsic base-collector junction charge
Q_{BCj}	base-collector charge in the partitioned region j
Q_{BE}	base-emitter charge
Q_{BEX}	base-emitter sidewall junction charge
Q_{BEj}	base-emitter charge in the partitioned region j
Q_{B0}	intrinsic base charge at V_{BE} = 0 V
Q_{QNR}	charge in the collector quasi-neutral region
Q_{SCR}	charge in the collector space-charge region
ΔQ_B	incremental intrinsic base charge due to base width modulation

δQ_B	incremental intrinsic base charge due to base conductivity modulation
q	electron charge
q_b	normalized base charge
R_B	base resistance
R_{BI}	intrinsic base resistance
R_{BIO}	intrinsic base resistance at $V_{BE} = 0$ V
R_{Bj}	base series resistance in the partitioned region j
R_{BX}	extrinsic base resistance
R_C	collector resistance
R_{CON}	base contact resistance
R_E	emitter resistance
R_{Ej}	emitter series resistance in the partitioned region j
R'_{EPI}	current-dependent epi-layer resistance
T	absolute temperature
t'	interconnect line thickness
t	time
t_1	height of the SiO_2 layer
t_2	height of the Si buried layer
t_3	height of the Si substrate
V_A	Early voltage
V_B	"late" voltage
V_{BC}	applied base-collector voltage
$V_{BC'}$	base-collector junction voltage
V_{BCI}	base-collector voltage at the moving boundary between the collector quasi-neutral region and the collector space-charge region
V_{BCj}	base-collector charge in the partitioned region j

V_{BCO}	base-collector voltage at the metallurgical base-collector region
V_{BE}	applied base-emitter voltage
V_{BEj}	base-emitter junction voltage in the partitioned region j
V_{BE}'	base-emitter junction voltage
V_{bi}	junction built-in voltage
V_{CB}	applied collector-base voltage
V_{CE}	applied collector-emitter voltage
V_D^{QNR}	lateral diffusion velocity in the collector quasi-neutral region
V_D^{SCR}	lateral diffusion velocity in the collector space-charge region
V_T	thermal voltage kT/q
V^*	effective junction built-in voltage
ΔV	ohmic drops in the emitter and base regions
v_p^e	even-mode phase velocity of propagated signal in coupled transmission lines
v_p^o	odd-mode phase velocity of propagated signal in coupled transmission lines
v_s	electron saturation velocity
W_E	emitter width
W_{QNR}	collector quasi-neutral region width
W_{SCR}	collector space-charge region width
W_{EPI}	epitaxial collector width
X_B	base width
X_{EPI}	epitaxial layer depth
X_{JB}	base junction depth
X_{JE}	emitter junction depth

ΔX_B	current induced incremental base width due to base pushout
w	interconnect width
w_e	effective interconnect width (TEM mode)
$w_{eff}(f)$	frequency-dependent effective interconnect width
Z	transmission line impedance
Z_0^e	even-mode characteristic impedance of coupled transmission line
Z_0^o	odd-mode characteristic impedance of coupled transmission line
$Z_0^e(f)$	frequency-dependent even-mode characteristic impedance of coupled transmission line
$Z_0^o(f)$	frequency-dependent odd-mode characteristic impedance of coupled transmission line
α	interconnect attenuation constant
α_c	interconnect conductor loss
α_c^e	conductor loss of coupled transmission lines in even mode
α_c^o	conductor loss of coupled transmission lines in odd mode
α_d	interconnect dielectric loss
α_d^e	dielectric loss of coupled transmission lines in even mode
α_d^o	dielectric loss of coupled transmission lines in odd mode
β	bipolar transistor current gain
β_F	maximum forward current gain
β_R	maximum reverse current gain
β_p	phase constant
γ	propagation constant
ϵ	permittivity of silicon
ϵ_{Si}	relative permittivity of silicon

ϵ_{SiO2}	relative permittivity of silicon dioxide
ϵ_r	relative permittivity
ϵ_{re}	effective relative permittivity
ϵ_{re}^{e}	effective permittivity of coupled transmission lines in even mode
ϵ_{re}^{o}	effective permittivity of coupled transmission lines in odd mode
ϵ_0	permittivity of free space
ϕ_c	collector-base junction potential
ϕ_e	emitter-base junction potential
τ	effective base doping gradient
τ_F	bipolar transistor forward transit time
τ_n	doping-dependent electron recombination lifetime
τ_{n0}	electron recombination lifetime at low doping
τ_p	doping-dependent hole recombination lifetime
τ_{p0}	hole recombination lifetime at low doping
τ_{QNR}	injection-level-dependent hole recombination lifetime in the collector quasi-neutral region
τ_R	bipolar transistor reverse transit time
μ_{n0}	electron mobility
$\mu_p(x,y)$	position-dependent hole mobility
μ_0	permeability of free space
ρ	resistivity of the conducting microstrip
ρ_b	intrinsic base sheet resistivity at V_{BE} = 0 V
σ_{METAL}	conductivity of metal line
σ_{Si}	conductivity of silicon
σ_{sub}	conductivity of substrate

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MODELING AND CHARACTERIZATION OF ADVANCED BIPOLAR
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Chairman: William R. Eisenstadt
Major Department: Electrical Engineering

This dissertation discusses the modeling of two-dimensional effects in advanced bipolar transistors (BJT's) and interconnects. The goal is to develop accurate and compact models for SPICE circuit simulation of advanced bipolar technologies. After reviewing base pushout mechanism in the bipolar transistor, the collector current spreading effects in quasi-saturation have been presented. A two-dimensional circuit model including collector spreading effects in the epitaxial collector is developed based on the physical insights gained from PISCES device simulations. Illustrative measurements and simulations demonstrate the bipolar circuit modeling accuracy.

Then a physics-based current-dependent base resistance model for circuit simulation is developed. Physical mechanisms such as base width modulation, base conductivity modulation, emitter crowding, and base pushout are accounted for in the comprehensive current-dependent base resistance model. Comparisons of the model predictions with measurements and device simulations show excellent agreement.

Two-dimensional circuit modeling is developed for the nonuniform current and charge distribution effects at the emitter-base sidewall and under the emitter during switch-on transients. The charge and current partitioning implemented in the bipolar transistor model treats the transient emitter crowding and current-dependent base resistance in a unified manner. Good agreement is obtained between model predictions and experimental results and transient device simulations.

In parallel to the work on fast BJT digital transients, the bipolar transistor high-frequency small-signal s-parameter prediction using a physical device simulator is developed. This is a novel result which includes the effects of the intrinsic bipolar response as well as the parasitics of interconnects, discontinuities, and bonding pads. This modeling technique can be used for sophisticated three-port or four-port network characterization and for predicting the high-frequency small-signal parameters other types of transistors.

The dissertation examines the improvement of IC interconnect models. Interconnect models including losses and dispersion are developed for advanced BJT IC doping profiles. In addition, signal crosstalk between adjacent interconnects is discussed. An ECL ring oscillator with interconnection line in mixed-mode circuit simulation

demonstrates the utility and necessity of accurate interconnect modeling.

In summary, the dissertation provides a comprehensive two-dimensional circuit and interconnect modeling for advanced bipolar IC techniques useful in computer-aided device and circuit design.

CHAPTER ONE
INTRODUCTION

The bipolar transistor (BJT) circuit model implemented in SPICE (the Gummel-Poon model) is derived based on one-dimensional device physics. Recently, the bipolar transistor has been scaled down to one micrometer emitter width. It exhibits the multidimensional current flow, especially when operated in high current transients rendering one-dimensional analysis inadequate. Thus, accurate device characterization and optimal integrated circuit (IC) fabrication process enhancement, through device and circuit simulations require better modeling of the advanced bipolar transistor. In addition, the interconnect delay in the submicrometer integrated circuits becomes increasing important during high speed transients. To precisely predict the BJT circuit performance, an accurate modeling of interconnect is essential. These facts motivate this study.

The general topology of this study is, first, to explore the importance of the multidimensional current flow by investigating the physical insight into the two-dimensional device simulations, and, second, to develop a representative two-dimensional circuit model for circuit simulation. The model developed describes the nonuniform current and charge distribution in the quasi-neutral base, the emitter-base sidewall, and the collector. The model shows good agreement when compared with measurements and device simulations.

Then, an interconnect model is developed based upon the first-order approximation and physical device simulation. The BJT circuit model and the IC interconnect model are integrated together for digital circuit simulation. The results of this study are directly applicable to advanced bipolar transistors and BiCMOS devices.

In Chapter Two, we developed a circuit model of the collector current spreading effects in quasi-saturation for advanced bipolar transistors. The discussion in this chapter reveals the importance of lateral current spreading in the epitaxial collector when base pushout occurs. The lateral diffusion currents ameliorates the quasi-saturation effects compared to one dimensional BJT model. Physical insight into the charge dynamics in the collector is shown by examining the current gain and hole concentration plots in PISCES simulations for 1-D-collector and 2-D-collector BJT's. Also, dc and transient circuit simulations at high currents are compared with measurements to demonstrate the model utility and accuracy.

Chapter Three presents a physics-based current-dependent base resistance model for all levels of injection. The model includes the 1-D and 2-D physical mechanisms of base width modulation, base conductivity modulation, emitter current crowding, and base pushout; it describes a current and voltage-dependent base resistance. Various measurement results and device simulation data are compared with the model predictions to demonstrate the model accuracy. For an emitter-coupled logic circuit, the BJT with a current-dependent R_B model results in a more realistic transient response compared with a BJT with constant base resistance model.

In Chapter Four, the author develops a partitioned circuit model taking into account the emitter crowding, sidewall current injection, and current-dependent base resistance in a unified manner. The model describes a nonuniform transient current and charge distribution under the emitter and at the emitter-base sidewall. This current and charge partitioning accurately represents the charge dynamics of the BJT during switch-on transient. The model predictions shows good agreement when compared with measurements and transient device simulations.

Chapter Five describes the s-parameter measurement prediction using a physical device simulator for advanced bipolar transistors. The prediction not only includes the intrinsic BJT small signal responses, but also accounts for the parasitic effects resulting from the interconnects, bends and pads. The intrinsic BJT small signal s-parameters are converted from y-parameters simulated in PISCES. The terminal responses are obtained by multiplying the cascaded T-matrix components representing the intrinsic BJT and extrinsic layout parasitic effects. Two interconnect cross-sections are compared to evaluate which is a superior test structure that introduces less signal attenuation and phase. In general, this technique can be used for three or four port network analysis and for the devices other than the BJT, such as GaAs heterojunction bipolar transistors in high frequency characterization.

In Chapter Six, the conventional interconnect model is improved. A new interconnect model which accounts for signal loss and dispersion is introduced for advanced IC cross-section profiles. An inverse Fourier transform is used for modeling transients. The prediction of

the interconnect model shows good agreement when compared with measurement. The model is implemented in SLICE/SPICE for mixed-mode circuit simulation. The utility of the interconnect model is demonstrated in a five-stage ECL ring oscillator transient simulation.

In Chapter Seven, the single interconnect model is extended to include crosstalk for coupled interconnect lines in close proximity. Signal crosstalk is important in digital switching. The model is developed from even mode and odd mode interconnect capacitance analysis. The picosecond transient measurement of photoconductive circuit element technique has been used to demonstrate the even mode and odd mode pulse splitting. An equivalent distributed, lumped circuit model for coupled interconnect lines is also developed. Circuit simulations employing the coupled transmission lines in digital switching have been used to demonstrate the signal crosstalk between interconnects. The discussion in this chapter supplements Chapter 6, thus providing a more complete interconnect modeling analysis.

Chapter Eight summarizes the contributions of this dissertation and presents recommendations for extension of this study.

CHAPTER TWO
TWO-DIMENSIONAL COLLECTOR CURRENT SPREADING EFFECTS IN QUASI-SATURATION

2.1 Introduction

Advanced self-aligned bipolar transistors based on a double polysilicon technology show multidimensional current flow in the collector, especially when operated at high currents. The multidimensional current flow effects are not included in existing bipolar circuit-simulator models such as the Gummel-Poon model in SPICE2 [1]. Recently, a novel 3-D BJT circuit model has been developed by using a 2-D device simulator [2]; however, the details of the collector spreading physical mechanism and the implementation in the equivalent circuit model have not been treated.

The quasi-saturation effects have been investigated by numerous authors for the past twenty years [3-8]. In general, two distinct models (one-dimensional and two-dimensional) have been developed. In the 1-D model, base push-out or quasi-saturation effect occurs when the current density is high enough that the intrinsic base-collector metallurgical junction becomes forward biased. Then carriers are injected into the epitaxial collector [3], [8].

In the two-dimensional model, there is a maximum current density, called space-charge-limited current flow, and any further increase in collector current results in a 2-D base spreading [4], [5]. Detailed explanations for the operating regions of each mechanism are shown in [6-8].

For the standard advanced BJT process, however, the heavily doped extrinsic base resulting from the double polysilicon technology makes base spreading negligible. In contrast, the base push-out due to high current in the collector is two-dimensional and results in lateral collector current spreading in the epitaxial collector [9], [10]. This collector current spreading, which is different from base spreading, has not previously been modeled.

Recently, Kull et al. [11] extended the Gummel-Poon model to include quasi-saturation, or base push-out in the BJT circuit model formulation. Kull's compact extension was modified by Jeong and Fossum [12] [13] to account for the possible existence of a current-induced space-charge region in the epitaxial collector. The modeling in [11] [12] is based a one-dimensional derivation and does not represent the two-dimensional currents in the collector. Thus, this modeling can overestimate quasi-saturation effects [9], [10].

In this chapter, the model in [12] is extended to take into account the multidimensional collector-current-spreading mechanism that occurs in quasi-saturation. The extension is facilitated by using the two-dimensional device simulator PISCES [14] to perform simulations of the advanced BJT's (Sec. 2.2). The PISCES simulations reveal the physical mechanism producing 2-D collector spreading. The mechanism was not reported in the previous BJT simulations [9], [15]. The modeling of collector transport in [12] [13] is modified to account for the lateral diffusion currents in the epitaxial collector region. The development of this modeling is described in Sec. 2.3. Comparisons of the model performance with measurements and device simulations are presented in

Sec. 2.4. Excellent agreement in dc and transient behavior is observed over a wide range of operating conditions.

2.2 Multidimensional Collector Current Spreading

An analysis of PISCES simulations of the advanced bipolar transistor was undertaken to identify the physical origin of the collector current spreading in the epitaxial collector. The BJT simulations with PISCES include heavy-doping effects (bandgap narrowing, Auger recombination), doping and field dependent carrier mobilities, and Shockley-Read-Hall (SRH) recombination. A generic advanced BJT cross-section was constructed by incorporating common features of many state-of-the-art transistors reported in the literature [16], [17].

The advanced bipolar transistor is illustrated in Fig. 2.1, where only half cross-section and doping profile need to be simulated due to the cross-section's symmetry. The emitter and base doping profiles and the emitter-base spacing were designed to avoid sidewall tunneling and perimeter punchthrough in the BJT [18]. Polysilicon contacts are simulated for the emitter and the base by using an effective surface recombination velocity of 3×10^4 cm/s [19]. The substrate contact is situated at the bottom of the buried collector. It is found that only a negligible perturbation on the lateral current flow in the lightly doped epitaxial collector results when a side-collector contact is used; this is discussed later in the paper.

A PISCES simulation predicted the multidimensional current flow in the collector and this is shown in Fig. 2.2. This diagram displays the

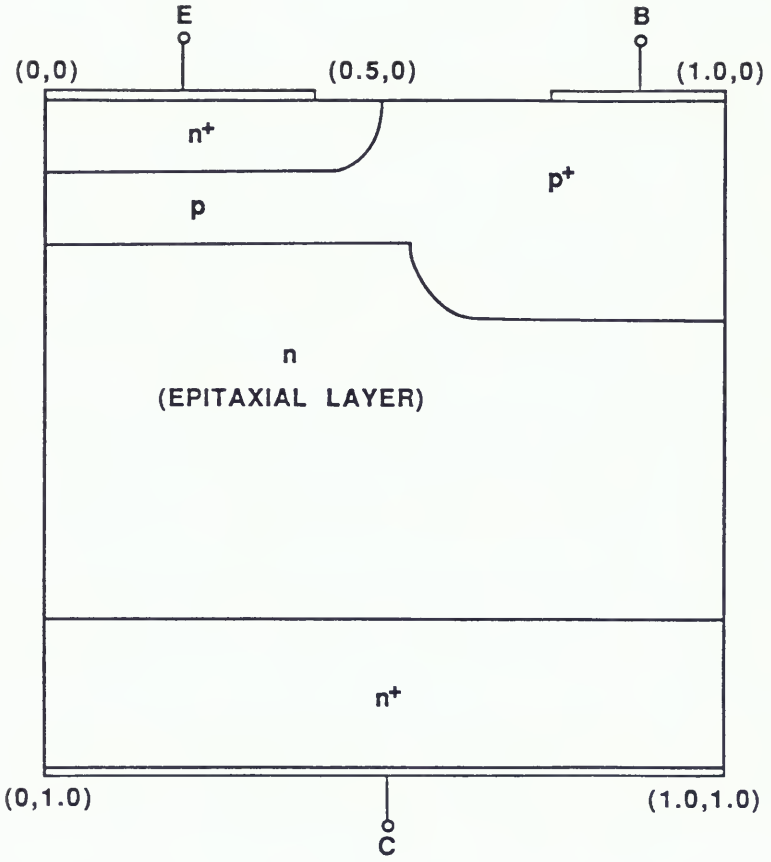

Figure 2.1.1 A right half cross-section of an advanced bipolar transistor used for multidimensional current studies. Dimensions of the cross-section are indicated in micrometer.

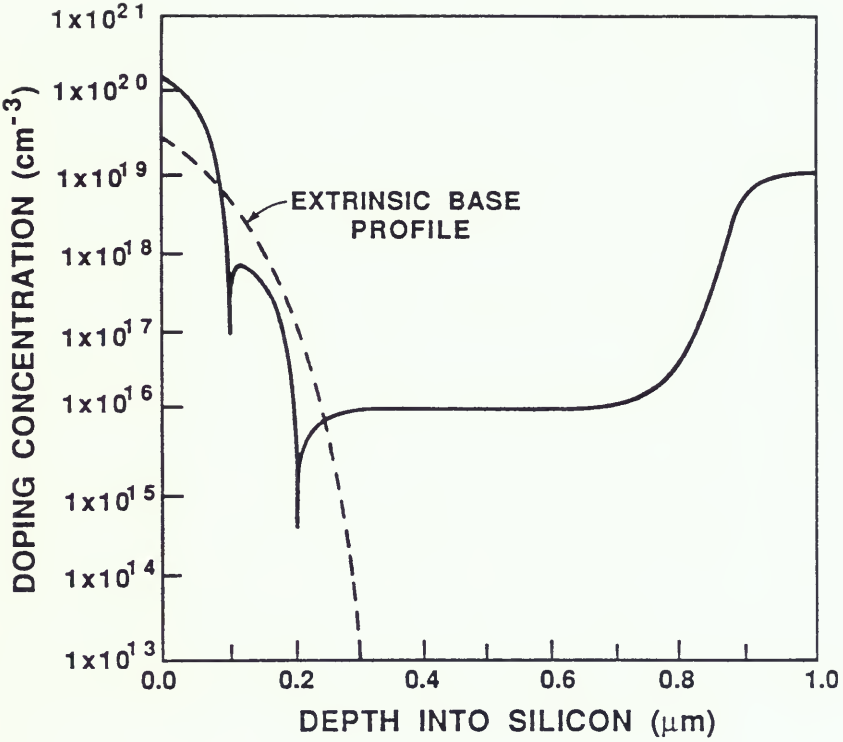

Figure 2.1.2 The doping profiles of the bipolar transistor shown in Figure 2.1.1. The solid line is the doping profile at the center of the emitter and the dashed line is the doping profile below the extrinsic base region.

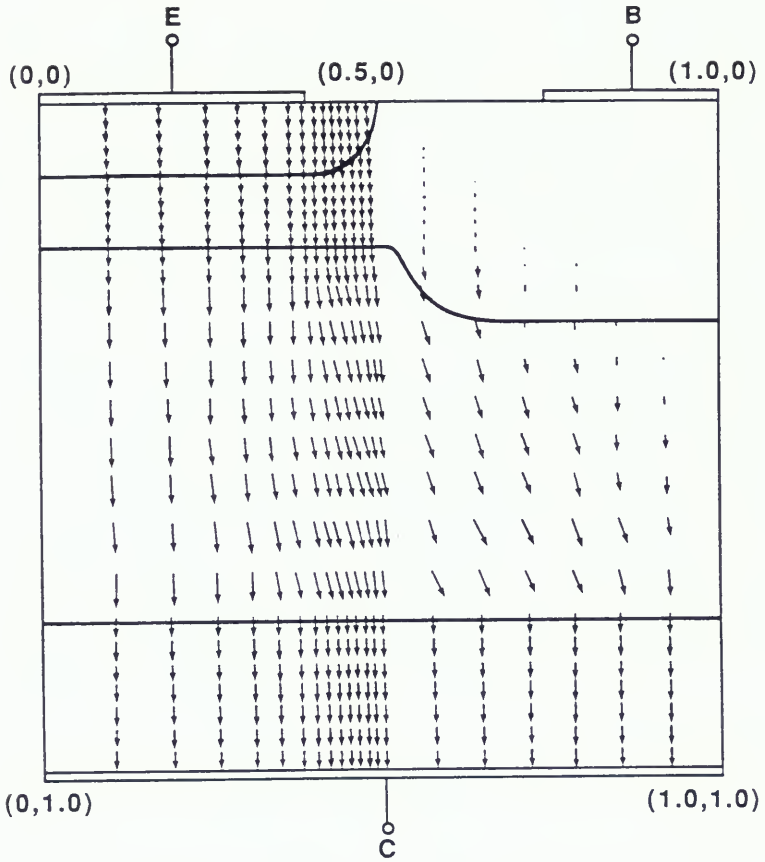

Figure 2.2 Plot of electron current vectors in the advanced BJT shown in Figure 2.1. In this PISCES simulation the collector contact is at the bottom of the buried collector at V_{CE} = 2.0 V and V_{BE} = 0.9 V.

PISCES simulation of the electron-current-density-vector plot, J_n, of the advanced BJT biased at applied collector-emitter voltage, V_{CE} = 2.0 V and applied base-emitter voltage, V_{BE} = 0.9 V ($I_C \simeq 0.5$ mA/μm). In the quasi-saturation region depicted in Fig. 2.2, excess carriers are injected into the epitaxial collector (base push-out). These excess electrons diffuse laterally in the epitaxial collector region under the extrinsic base due to the high carrier concentration gradient in the horizontal direction. Collector current spreading is indicated by the horizontal component of current-density vectors underneath the extrinsic base.

Note that Fig. 2.2 qualitatively shows where the multidimensional collector currents occur, but it does not lend itself to a quantitative estimation of the magnitude of these currents. The grid in Fig. 2.2 is nonuniform (for better simulation accuracy and convergence) and dense at emitter, base, and emitter-base junction because of the position-dependent doping density at these regions. The magnitudes of the current-density vectors at the grid points which are sparsely located are enhanced when compared to those of dense grid points.

The effect of electric field in the buried collector on the current distribution in the epitaxial collector can be seen by shifting the collector contact to the right-side of the BJT. Figure 2.3 shows a BJT simulation from PISCES of the current-density vectors for a right-side-collector contact, with V_{CE} = 2.0 V and V_{BE} = 0.9 V, the same bias as that of Fig. 2.2. Although there is a great difference in the current vectors in the buried collector (due to lateral ohmic drop), all the currents in the intrinsic BJT remain virtually the same. The

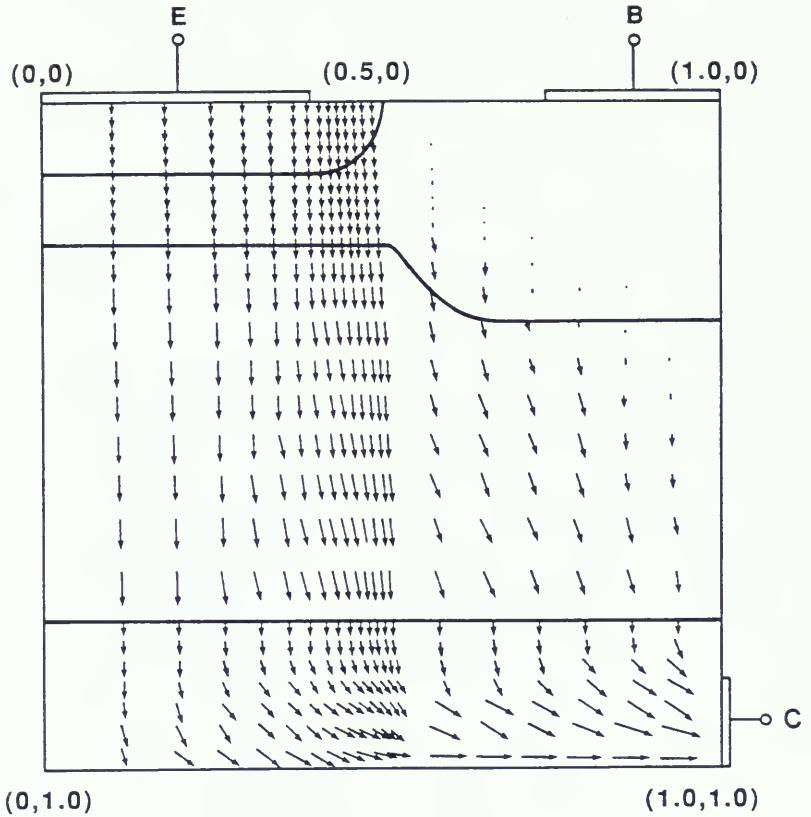

Figure 2.3 Plot of electron current vectors in the advanced BJT shown in Figure 2.1. In this PISCES simulation the collector contact is at the side of the buried collector at V_{CE} = 2.0 V and V_{BE} = 0.9 V.

magnitudes of the vertical and lateral current-density vectors in Fig. 2.2 and Fig. 2.3 are typically within 0.5% of each other. This indicates that the electric field from the right-side collector contact only controls the current flow in the buried-collector region, and that it does not significantly affect the lateral flow. Thus, there is no significant drift component in the collector spreading mechanism.

A 1-D-collector transistor was simulated in order to isolate the effects of collector spreading in the advanced BJT operation. This 1-D-collector BJT, shown in Fig. 2.4, has the same emitter and base regions as the 2-D BJT in Fig. 2.1; however, below the extrinsic base region of the 1-D-collector transistor, the epitaxial and buried-collector regions are replaced with SiO_2. This forces the collector current to flow solely in the vertical direction below the intrinsic base, hence the name 1-D-collector transistor.

Comparing the current gain, β and cut-off frequency, f_T of the 2-D BJT to those of the 1-D-collector BJT at high currents is one of the keys to understanding the role of collector current-spreading. The 2-D BJT exhibits a larger β (see Fig. 2.5) and f_T than the 1-D-collector BJT as both transistors are driven further into saturation [10].

Figure 2.6 indicates how quasi-saturation is ameliorated by lateral diffusion in the collector. This figure displays a hole concentration plot for a vertical slice along the center of the emitter of both the 2-D BJT and 1-D-collector BJT. This simulation is performed for BJT's with emitter width, W_E = 1 μm, V_{BE} = 0.9 V, and V_{CE} = 2.0 V. The base in the 1-D BJT displays significantly more base widening than the 2-D-collector BJT, which results in an enhanced 2-D-BJT β, and f_T

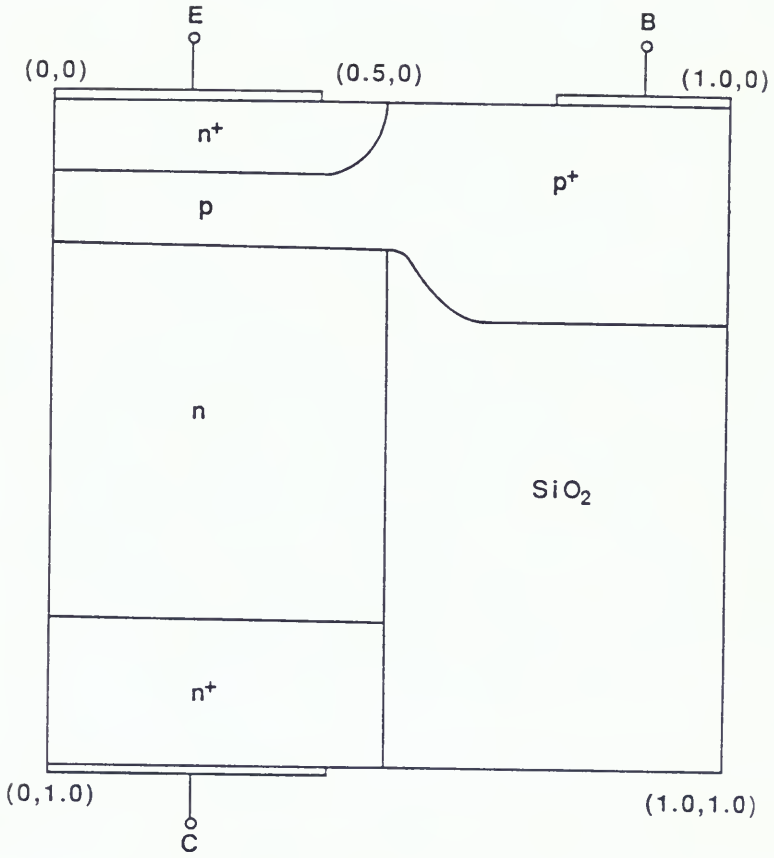

Figure 2.4 An advanced bipolar transistor cross-section designed with a 1-D-collector. This transistor is used to isolate the 2-D collector spreading effects.

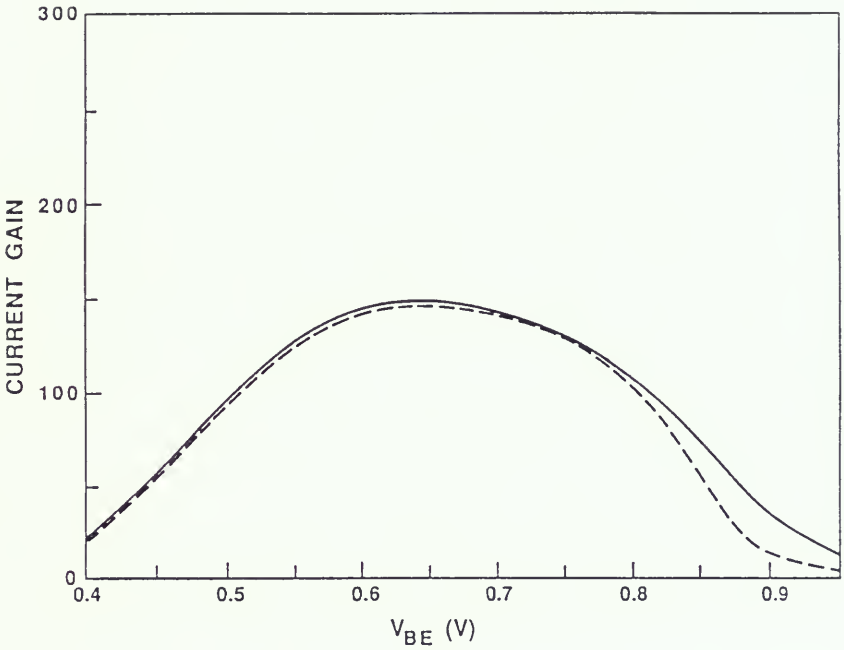

Figure 2.5 Plot of the current gain versus V_{BE}. The solid line represents the 2-D BJT and the dashed line represents the 1-D-collector BJT.

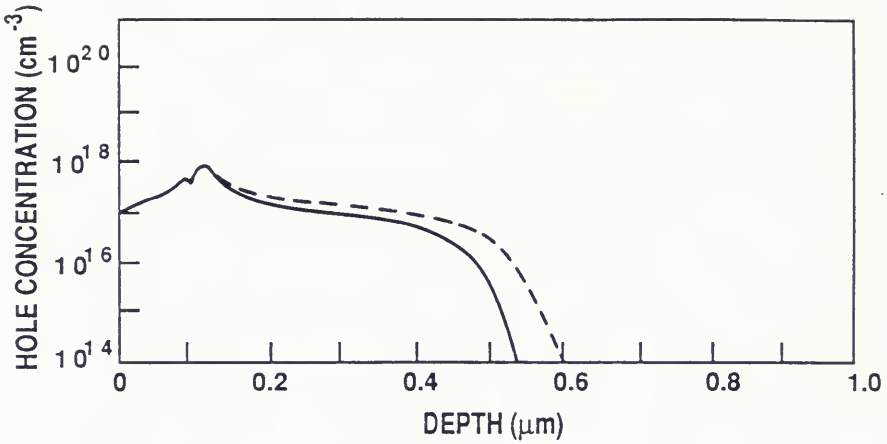

Figure 2.6 Plot of hole concentration from the center of the emitter to the collector at V_{CE} = 2.0 V and V_{BE} = 0.9 V. The solid line represents the 2-D BJT and the dashed line represents the 1-D-collector BJT.

at high currents. The reduced quasi-saturation effects in 2-D-BJT are due to the lateral diffusion current which results from the high carrier concentration gradient in the horizontal direction. Further simulation of current spreading at different emitter widths, with the same doping profiles and boundary conditions as in Fig. 2.2, indicates that the lateral diffusion current is not a function of W_E, but a function of normalized charge $Q(I_C,V_{CE},W_E)/W_E$ or the charge below the emitter periphery.

2.3 SPICE Modeling Including Collector Spreading Effects

A semi-empirical model was developed using PISCES simulation to suggest analytical approximations that would predict collector current spreading. This modeling of the collector spreading effect was incorporated into an existing charge-based 1-D BJT model [12] to yield a quasi-2-D model. The 1-D BJT model accounts for quasi-saturation (ohmic and non-ohmic) by describing the collector current in terms of the quasi-Fermi potentials at the boundaries of the epitaxial collector which, in conjunction with the base transport, characterizes $I_C(V_{BE},V_{BC})$. Since this charge-based 1-D model correctly accounts for the 1-D BJT physics [12] it can be modified to incorporate the multidimensional current effects in the advanced BJT.

In the formulation of the 2-D model, we estimate the lateral diffusion currents in the collector quasi-neutral region and the collector space-charge region (I_L^{QNR} and I_L^{SCR}) as a function of the normalized 1-D-collector quasi-neutral region charge and space-charge region charge (Q_{QNR}/A_E and Q_{SCR}/A_E, A_E is the emitter area). These

normalized excess charges are the sources of the lateral diffusion currents. Empirical lateral diffusion velocities (V_D^{QNR} and V_D^{SCR}) are estimated from the collector lateral current flow predicted by PISCES BJT simulation. These lateral diffusion velocities multiplied by the respective normalized charges and emitter perimeter, P_E form the lateral diffusion currents. The current and voltage dependence of the lateral diffusion currents are implicitly accounted for in the model by the collector charges $Q_{QNR}(I_C,V_{CE})$ and $Q_{SCR}(I_C,V_{CE})$. Figure 2.7 shows the base transport current, I_C^{QNB} in the quasi-neutral base, collector transport currents, I_C^{QNB} and I_L^{QNB} in the collector quasi-neutral region, and I_C^{SCR} and I_L^{SCR} in the collector space-charge region. In Fig. 2.7 a moving boundary between collector quasi-neutral region and collector space-charge region defines the collector quasi-neutral region width, W_{QNR} and the collector space-charge region width, W_{SCR} ($W_{SCR} = W_{EPI}-W_{QNR}$, and W_{EPI} is the epitaxial collector width).

The following equations incorporate the collector-spreading mechanism into the 1-D model and make it a 2-D model:

$$I_C^{QNB} = I_C^{QNR} + I_L^{QNR} \tag{2.1}$$

$$I_C^{QNR} = I_C^{SCR} + I_L^{SCR} \tag{2.2}$$

$$I_C^{QNB} = I_S/q_b\,[\exp(V_{BE}'/V_T) - \exp(V_{BCO}/V_T)] + C_2 I_S \exp[V_{BE}'/(n_e V_T)] \tag{2.3}$$

$$I_C^{QNR} = \frac{V_T}{R'_{EPI}}\left\{F(V_{BCO}) - F(V_{BCI}) - \ln\left[\frac{1+F(V_{BCO})}{1+F(V_{BCI})}\right] + \frac{V_{BCO}-V_{BCI}}{V_T}\right\} \tag{2.4}$$

$$I_C^{SCR} = q\,A_E\,(N_{EPI} + \Delta n)\,v_s \tag{2.5}$$

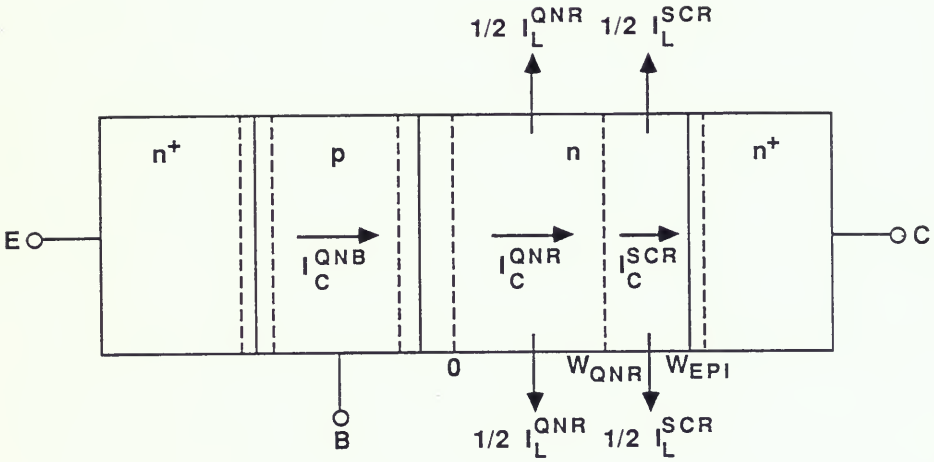

Figure 2.7 Regional BJT schematic used to show the transport currents associated with their regions and boundaries.

$$I_L^{QNR} = V_D^{QNR} (Q_{QNR}/A_E) P_E \tag{2.6}$$

$$I_L^{SCR} = V_D^{SCR} (Q_{SCR}/A_E) P_E \tag{2.7}$$

where $R'_{EPI} = Q_{QNR}/(\mu_{n0} N_{EPI} A_E)$, $F(V) = [1 + \alpha \exp(V/V_T)]^{1/2}$,

$V_{BC0} = [E_{FN}(0) - E_{FP}]/q$, $\alpha = 4n_i^2/N_{EPI}^2$,

$V_{BCI} = [E_{FN}(W_{QNR}) - E_{FP}]/q$, $V_T = kT/q$,

Q_{QNR}, Q_{SCR}, W_{QNR}, and Δn are defined in [12].

The notation used in the equations above is as follows: N_{EPI} is the epitaxial collector doping concentration, n_i is the intrinsic carrier concentration, v_s is the saturation velocity, μ_{n0} is the electron mobility, E_{FN} is the electron quasi-Fermi level, E_{FP} is the hole quasi-Fermi level, V_{BE}' is the base-emitter junction voltage, and I_S, q_b, C_2, and n_e retain their meanings given in the Gummel-Poon model [1].

Figure 2.8 displays the overall SPICE model topology of the 2-D model for collector spreading. Two new current sources which are highlighted in the figure have been added to the 1-D-BJT model [12] to account for the lateral diffusion currents in the epitaxial collector. Note that, since the 2-D model modifies the 1-D BJT quasi-static charge in the collector region, the transient currents dQ_{QNR}/dt and dQ_{SCR}/dt are effectively refined in terms of this new quasi-static charge distribution as Eqs. (2.1)-(2.7) are solved simultaneously. A 1-D BJT model can not represent this collector charge redistribution [12] and gives erroneous estimates of the BJT transient performance [10]. In contrast, the 2-D BJT circuit model correctly accounts for the charge

dynamics in the collector and the moving boundary between the quasi-neutral region and the space-charge region in the epitaxial collector.

In addition, collector conductivity modulation, which makes the collector resistance small, is accounted for in the modified R'_{EPI} that is a function of the varying quasi-neutral collector width, $W_{QNR}(I_C,V_{CE})$. A component of base recombination current, Q_{QNR}/τ_{QNR} due to a finite recombination lifetime, τ_{QNR} in the collector quasi-neutral region [20] is also included in the base current, I_B. The injection-level-dependent lifetime (τ_{QNR}) can be modeled as [21]:

$$\tau_{QNR} = \tau_{p0} + \tau_{n0} \frac{\bar{p}}{\bar{p} + N_{EPI}} \tag{2.8}$$

$$\bar{p} = \frac{Q_{QNR}}{q\, A_E\, W_{QNR}} \tag{2.9}$$

where τ_{n0} is the electron recombination lifetime, and τ_{p0} is the hole recombination lifetime in SRH recombination model.

2.4 Model Verification with Experiments and Device Simulations

The circuit model which includes collector current spreading was implemented in the user-defined controlled-sources (UDCS's) available in SLICE, the Harris Corporation enhanced version of SPICE. In the SPICE circuit analysis, UDCS's are user-defined subroutines that use the implicit nonlinear model equations to compute both charging current (dQ/dt) and transport (I) currents [22] (see Appendix B) in the model as depicted in Fig. 2.8. The underlying transport currents in Sec. 2.3

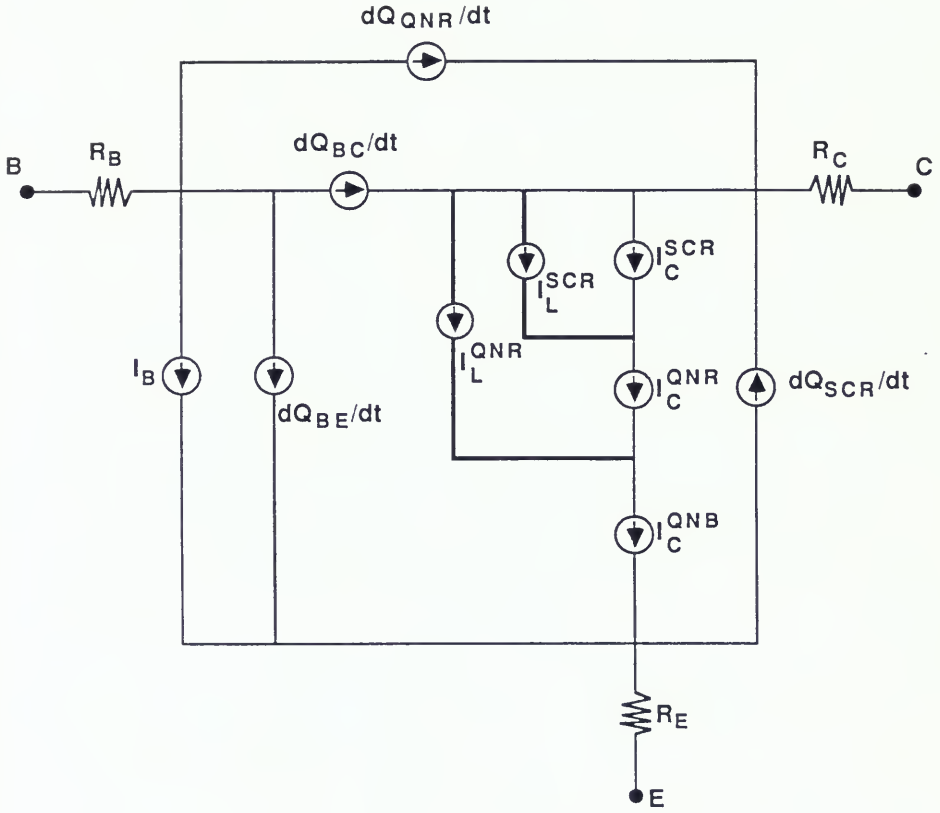

Figure 2.8 Network representation of the circuit model including collector current spreading effects. The bold lines are lateral diffusion currents in the collector.

are solved simultaneously to account for the correct charge dynamics in the collector. The time derivatives of the quasi-static stored charges thus properly represent the distributed charging currents. Also the inherent nonreciprocal transcapacitance of the BJT are simulated directly, without the use of equivalent-circuit capacitors [23].

Test devices representative of the advanced BJT were used to verify the model and to define a parameter-extraction scheme [24]. Some of the parameters can be defaulted directly from geometrical and process information such as A_E, P_E, N_{EPI}, and W_{EPI}. Empirical parameters of R_E, R_B, I_S, β_F, β_R, V_A, V_B, C_2, C_4, n_e, n_c, C_{JE0}, C_{JC0}, m_e, m_c, ϕ_e, ϕ_c, τ_F, τ_R are measured by standard methods [1]. Other parameters which related to device physics are known in [25] (n_i, μ_{n0}, v_s), by fitting measured and simulated I_B (τ_{n0}, τ_{p0}), by estimating PISCES results (V_D^{QNR}, V_D^{SCR}).

The physical parameters of the lateral diffusion velocities calculated from the collector lateral flow in PISCES 2-D simulation ($W_E \leq L_E$) are:

$$V_D^{QNR} \equiv \frac{A_E\ I_L^{QNR}}{P_E\ Q_{QNR}} \simeq \frac{W_E \int_0^{W_{QNR}} [J_n(x,y=0) + J_n(x,y=W_E)]\ dx}{2\int_0^{W_E}\int_0^{W_{QNR}} q[n(x,y) - N_{EPI}]\ dxdy} \tag{2.10}$$

$$V_D^{SCR} \equiv \frac{A_E\ I_L^{SCR}}{P_E\ Q_{SCR}} \simeq \frac{W_E \int_{W_{QNR}}^{W_{EPI}} [J_n(x,y=0) + J_n(x,y=W_E)]\ dx}{2\int_0^{W_E}\int_{W_{QNR}}^{W_{EPI}} q[n(x,y) - N_{EPI}]\ dxdy} \tag{2.11}$$

where n is the position-dependent electron carrier concentration, the x axis is in the vertical direction, the y axis is in the horizontal direction, y = 0 stands for the left-side emitter edge, and y = W_E stands for the right-side emitter edge.

The lateral diffusion velocities are in the range of 3×10^6 cm/s to 5×10^6 cm/s due to the error introduced in the double integration of discrete data. A fine tune-up of these parameters can be done by optimizing (or fitting) the measured and simulated results at high I_C, and low V_{CE}.

The simulation results of the collector current versus V_{CE} at different base currents from 1-D [12] and 2-D models are compared with measurements in Fig. 2.9. In this figure, the solid line represents measurements, the symbol x's represent 2-D model simulations, and the circles represent 1-D model simulations. It is clear that 1-D model overestimates quasi-saturation effects. This is seen in Fig. 2.9 at high I_C and low V_{CE}, where non-ohmic quasi-saturation dominates. The test device measured in Fig. 2.9 has the drawn dimension W_E = 2 μm, L_E = 4 μm and the approximate active emitter area $A_E \simeq 1.2 \times 3.2$ μm^2 due to its "boot-shaped" sidewall spacer technology [26]. In order to demonstrate the model's lateral scalability, a test device with active emitter area $A_E \simeq 0.7 \times 3.2$ μm^2 was measured and compared with model simulations in Fig. 2.10. Note that the lateral diffusion velocities (V_D^{QNR}, V_D^{SCR}) used in these simulations are the same as in the previous ones. The predictions of the present model show good agreement when compared with the experimental results on these two different emitter size BJT's. However, the 1-D model simulation results differ

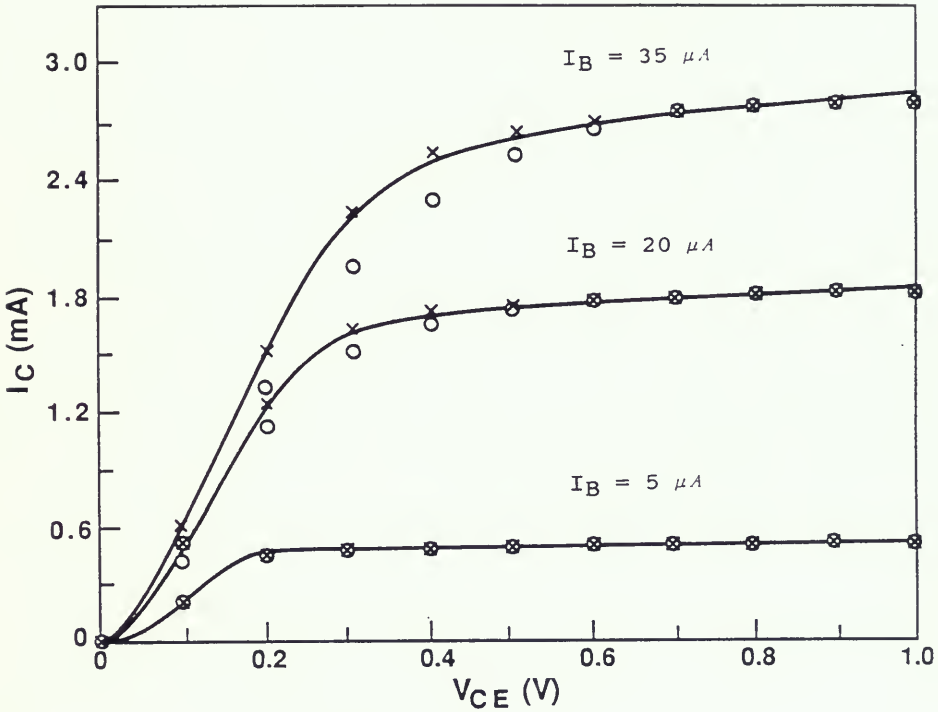

Figure 2.9 Plot of collector current I_C versus V_{CE} at different I_B with test device $A_E \approx 1.2 \times 3.2$ μm. The solid line represents measurements, "×" represents 2-D model simulations, and "O" represents 1-D model simulations.

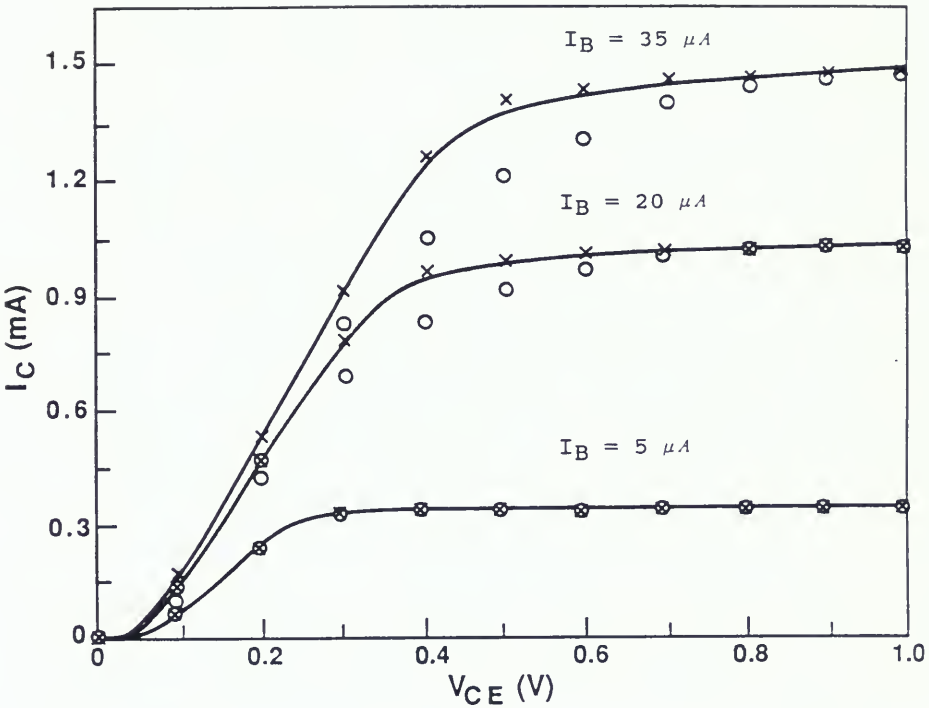

Figure 2.10 Plot of collector current I_C versus V_{CE} at different I_B with test device $A_E \approx 0.7 \times 3.2$ μm. The solid line represents measurements, "×" represents 2-D model simulations, and "O" represents 1-D model simulations.

significantly from measurements in quasi-saturation, especially with the small emitter size BJT.

The 2-D and 1-D models are used to simulate a BJT ($A_E \simeq 1.2 \times 3.2$ μm^2) inverter with 1.6 KΩ load resistor. The input pulse waveform consists of a 0.9 V, 50 ps ramp followed by a flat pulse of 950 ps duration and then a falling 0.9 V ramp of 50 ps. The circuit responses to the input pulse of the 2-D and 1-D BJT models are shown in Fig. 2.11. Both transistor models yield the same initial delay and falling waveform for the first 100 ps. After that the 2-D BJT model predicts a faster falling waveform that goes to a lower asymptote on the output pulse due to higher I_C, lower dQ_{QNR}/dt and dQ_{SCR}/dt. To verify model prediction in transient operation, transient device simulation is used for comparison. Transient measurement of a ring oscillator introduces an extra propagation delay from the interconnect between the first and last stages of the ring oscillator and the I/O pad capacitances which lead to the difficulty in measuring the actual transient switching responses [27]. The 2-D model simulations of an inverter show good agreement with PISCES numerical results (circles in Fig. 2.10) in transient operation which indicates that 2-D BJT model correctly accounts for the charge dynamics and the time derivatives of the quasi-static stored charges in the collector.

2.5 Conclusions

A circuit model for the advanced bipolar transistor including collector current spreading effects in quasi-saturation has been developed. The model is defined implicitly by a system of nonlinear

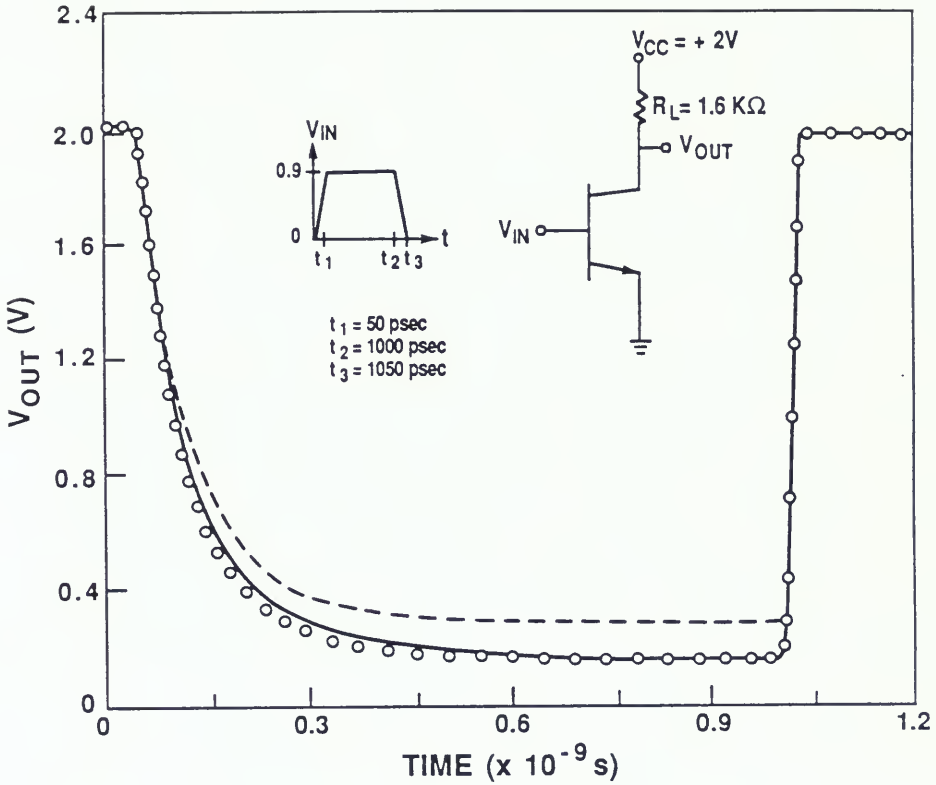

Figure 2.11 Plot of the simulated transient responses of a BJT inverter ($A_E \approx 1.2 \times 3.2$ μm) with load resistance 1.6 KΩ for 2-D model (solid line), 1-D model (dashed line), and PISCES simulation (circles).

equations describing base and collector transport. Two lateral diffusion current sources were added to the 1-D physical model to account for the multidimensional currents in the collector. The lateral diffusion currents due to a carrier concentration gradient between the collector area under the emitter and the collector area under the extrinsic base were investigated. It was found that the collector current spreading mechanism, which is entirely different from the base spreading mechanism, is independent of the drift component in the collector, and ameliorates quasi-saturation effects in terms of current gain and transient response. The collector spreading effect is significant when the BJT is operated at high I_C and low V_{CE}, with low epitaxial collector concentration, large epitaxial collector depth, or small emitter width. SPICE simulations employing the collector spreading model are in good agreement with the experimental results and device simulations. The present model correctly accounts for the charge dynamics in the collector and is scalable to small geometry BJT resulting lateral scaling.

CHAPTER THREE
PHYSICS-BASED CURRENT-DEPENDENT BASE RESISTANCE

3.1 Introduction

The base resistance R_B plays a significant role in the switching speed and frequency response of the bipolar transistors [28] [29]. In BJT circuit simulator models such as the Gummel-Poon model in SPICE, R_B is treated as constant with respect to applied bias [1], which in modern BJT's is inadequate because base resistance is current dependent.

The characterization and modeling of the BJT base resistance is a difficult task. For the past twenty years, various methods for deriving R_B have been reported [30-34] Recently, Ning and Tang [33] developed an elegant dc method for measuring the base and emitter resistances. However, the accuracy of this method depends on having the intrinsic base resistance R_{BI} linearly proportional to the forward current gain, β at high currents. This method may not be applicable to modern advanced bipolar transistors [35]. Neugroschel [34] presented an ac method for determining R_B at low currents. By varying the base-emitter voltages, the current-dependent base resistance was characterized at low currents. However, this ac technique can be sensitive to the picofarad parasitic capacitances associated with probed measurements on the integrated circuits and requires skilled experimental techniques.

In this chapter, we propose a physics-based base resistance model taking into account a wide range of injection levels. This model, which

is discussed in Secs. 3.2 and 3.3, includes the physical effects of base width modulation, base conductivity modulation, emitter crowding, and base pushout. Good agreement is obtained when the new R_B model is compared with BJT measurements and a 2-D device simulations (Sec. 3.4). In order to illustrate its usefulness, the R_B model is also implemented in the user-defined subroutines in SLICE. Then transient responses are simulated for an ECL circuit by performing circuit simulation with the current R_B model versus the constant R_B model (Sec. 3.5). Conclusions are given in Sec. 3.6.

3.2 Physical Mechanisms for Current Dependency

In this section, the various physical mechanisms (1-D and 2-D) that are involved in the R_B determination are treated separately and then a simple method of estimating their coupled effects is proposed.

The total base resistance of a bipolar transistor, R_B is composed of the following

$$R_B = R_{BI} + R_{BO} + R_{CON} \tag{3.1}$$

where R_{BI} is the intrinsic base resistance, R_{BO} is the extrinsic base resistance, and R_{CON} is the base contact resistance. The intrinsic base resistance occurs in the base region between the emitter and collector, the extrinsic base resistance occurs in the lateral extension of the base from its intrinsic region to the base contact, and the base contact resistance results from the ohmic contact between IC interconnect and the base. Generally, $R_{CON} < R_{BI}$ and $R_{CON} < R_{BO}$. Thus, R_{CON} will be neglected in this study. In addition, the R_{BO} of a BJT is

almost excitation independent [36]. Thus the only current dependent term in the right hand side of Eq. 1 is R_{BI}. Methods for characterizing ohmic base resistance behavior (R_{BO}) in the BJT are presented in the literature [33-36]. Therefore, the focus of this chapter will be on estimating R_{BI} from the physical mechanisms in the active base region.

3.2.1 Base Width Modulation

Figure 3.1 shows a simplified structure of n^+-p-n-n^+ bipolar transistor. Using conventional terminology, the base width, X_B is the vertical dimension between the emitter-base space-charge region (SCR) and the collector-base space-charge region. The emitter length, L_E is defined as the dimension pointing into the figure. The cross-sectional area of the base (perpendicular to the base current path) is determined by the product of the quasi-neutral base width, X_B and L_E.

Since R_{BI} is inversely proportional to the cross-sectional area of the base, the modulation of the emitter-base or the collector-base space-charge region will change the magnitude of R_{BI}. For example, assume that the emitter-base junction is forward-biased and there is a constant collector-base applied voltage, V_{CB}. Then X_B is modulated by the moving edge of the emitter-base space-charge region when V_{BE} changes. As V_{BE} increases, the emitter-base space-charge region contracts, and X_B expands. This reduces R_{BI} because the base cross-sectional area, $X_B \times L_E$ increases resulting in a larger base charge and a larger effective Gummel number.

The variation in quasi-neutral base charge can be modeled as $Q_{BO}/(Q_{BO}+\Delta Q_B)$ where Q_{BO} is the zero-biased intrinsic base charge

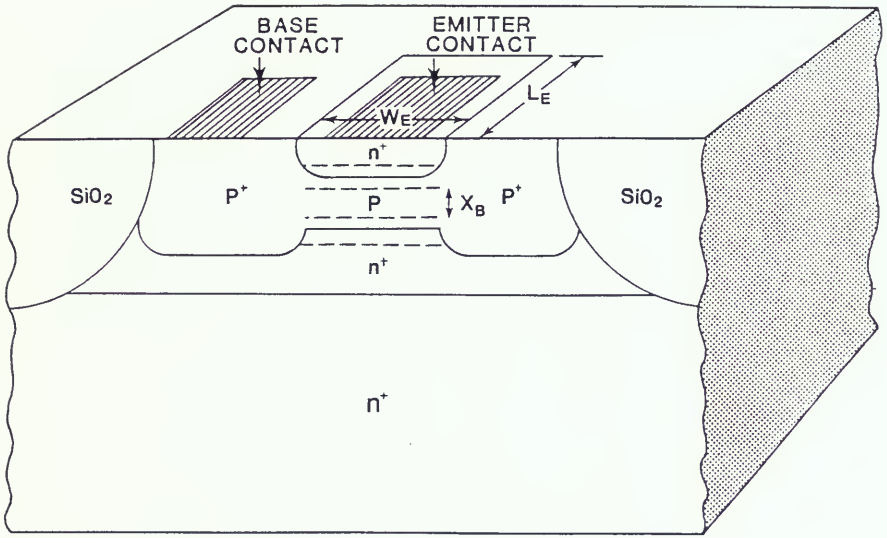

Figure 3.1 Schematic of an advanced bipolar transistor structure. The dashed lines represent the edges of the space-charge region.

($Q_{BO} = A_E\int N_B(x)\,dx$), and ΔQ_B is the incremental base charge resulting from base width modulation effect ($\Delta Q_B = A_E\int C_{JE}(V)\,dV$). A_E is the emitter area, and V_{BE}' is the base-emitter junction voltage ($V_{BE}' \simeq$ the quasi-Fermi level separation between the edges of the emitter-base space-charge region).

To find ΔQ_B, a recently reported comprehensive 1-D model for the emitter-base junction capacitance, C_{JE} is employed [37]:

$$C_{JE}(V_{BE}') = [q\epsilon^2 a/12(V^*-V_{BE}')]^{1/3} \quad \text{for } qN_B^3/(a^2\epsilon(V^*-V_{BE}')) > 0.1$$
$$= [q\epsilon N_B/2(V^*-V_{BE}')]^{1/2} \quad \text{for } qN_B^3/(a^2\epsilon(V^*-V_{BE}')) < 0.1$$
$$\text{for } V_{BE}' \le V_{bi} - 0.3 \qquad (3.2)$$

$$C_{JE}(V_{BE}') = (2q\epsilon n_i/V_T)^{1/2} \exp(V_{BE}'/4V_T)$$
$$\text{for } V_{bi} - 7V_T \le V_{BE}' < V_{bi} - 5V_T \qquad (3.3)$$

$$C_{JE}(V_{BE}') = (2q\epsilon n_i/V_T)^{1/2} \exp[-(V_{BE}'-2V_{bi}+10V_T)/4V_T]$$
$$\text{for } V_{BE}' \ge V_{bi} - 5V_T \qquad (3.4)$$

where q is the electron charge, n_i is the intrinsic carrier concentration, ϵ is the dielectric permittivity of silicon, "a" is the emitter-base junction impurity gradient, V_{bi} is the built-in junction voltage, N_{Beff} is the effective base doping density ($N_{Beff} = \int N(x)dx/X_B$, X_B is the base width), C'_{JE} is the derivative of the junction capacitance, V^* is the effective junction built-in voltage. For a linearly-graded junction $V^* = (2kT/3q)\ln(\epsilon kTa^2/8q^2n_i^3)$ [37].

The model defines parameters $V_1 = V_{bi} - 0.3$ and $V_2 = V_{bi} - 7V_T$. A polynomial fit calculates the capacitance using (3.2), (3.3) and the derivative of the capacitance (C'_{JE}) in the region between $V_{bi} - 0.3 <$

$V_{BE'} < V_{bi} - 7V_T$ [37].

$$C_{JE}(V_{BE'}) = C_{JE}(V_1)\,[1-2(V_{BE'}-V_1)/(V_1-V_2)]\,[(V_{BE'}-V_2)/(V_1-V_2)]^2 + C_{JE}(V_2)\,[1-2(V_{BE'}-V_2)/(V_2-V_1)]\,[(V_{BE'}-V_1)/(V_2-V_1)]^2 + C'_{JE}(V_1)\,(V_{BE'}-V_1)\,[(V_{BE'}-V_2)/(V_1-V_2)]^2 + C'_{JE}(V_2)\,(V_{BE'}-V_2)\,[(V_{BE'}-V_1)/(V_2-V_1)]^2 \quad \text{for } V_{bi} - 0.3 \equiv V_1 < V_{BE'} < V_{bi} - 7V_T \equiv V_2 \qquad (3.5)$$

Figure 3.2 shows a plot of a base-width modulation $Q_{BO}/(Q_{BO}+\Delta Q_B)$ versus $V_{BE'}$. We define a base-width modulation factor, $f_{BWM} = Q_{BO}/(Q_{BO}+\Delta Q_B)$ as the vertical axis of the plot in Fig. 3.3. In general, $V_{BE'} < V_{BE}$ because of ohmic drop in the quasi-neutral region [38]. The monotonic decrease of f_{BWM} at low $V_{BE'}$ is due to the contraction of the emitter-base SCR width shrinking. For $V_{BE'}$ above 0.8 V, the f_{BWM} slope is zero because the emitter-base SCR width can not contract further. The base width modulation due to the base-collector SCR edge variation in the base is neglected because modern BJT's have base doping density much higher than their epi-layer doping density, N_{epi}. This results in the SCR edge variation occurring in the epitaxial collector.

3.2.2 Base Conductivity Modulation

When a bipolar transistor (n-p-n) is in high current operation, the hole concentration (including the excess carrier concentration) in the base will exceed the acceptor (dopant) concentration to maintain charge neutrality. As a result, the base sheet resistance under the emitter decreases as the hole injection level increases. An excess base charge, δQ_B that results from this effect is given as [39]

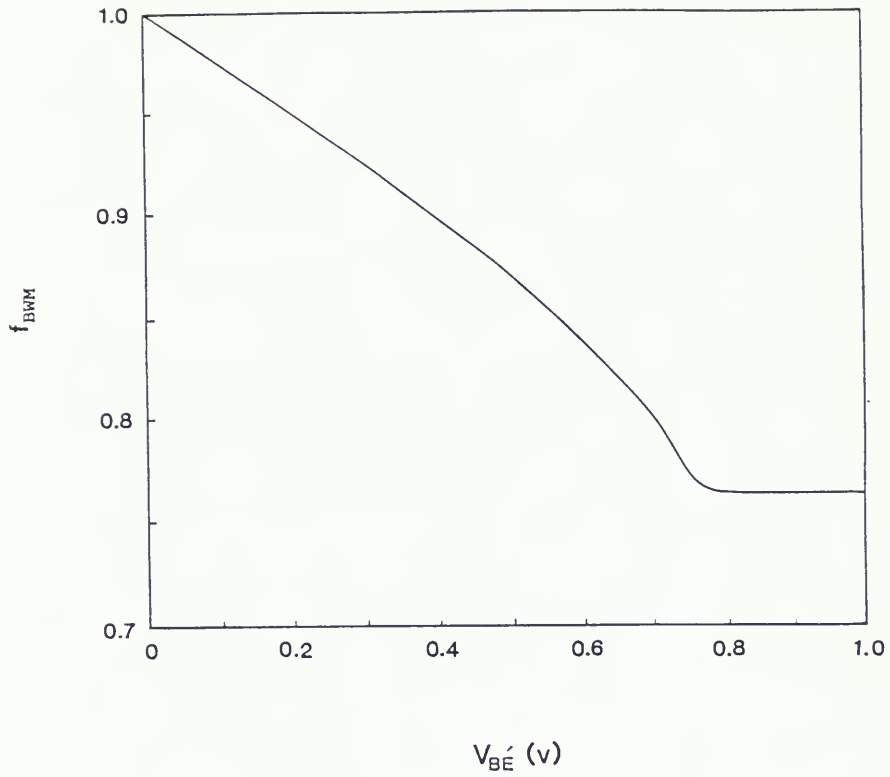

Figure 3.2 Plot of the base-width-modulation factor, f_{BWM} versus the base-emitter junction voltage, $V_{BE'}$.

$$\delta Q_B = Q_{B0} \frac{(2+A_1+n_0)A_2 n_0}{(2+A_1)A_2/A_3+n_0} \tag{3.6}$$

where $A_1=2[\exp(\tau)-1]/[\tau\exp(\tau)]$, $A_2=1/A_1$, $A_3=\exp[(\tau-1)\exp(\tau)+1]/[\exp(\tau)-1]^2$, τ is the effective base doping gradient ($\tau \equiv \ln[N(0)/N(X_B)]$), and n_0 is the electron concentration normalized by base doping N(0) at the base edge of the emitter-base space-charge region. Note that n_0 is determined by $n_0(1+n_0)=n_i^2/N^2(0)\exp(V_{BE}'/V_T)$.

The simulated result of base-conductivity modulation versus V_{BE}' is shown in Fig. 3.3. We define a base-conductivity-modulation factor, $f_{CM} \equiv Q_{B0}/(Q_{B0} + \delta Q_B)$ as the vertical axis of the plot in Fig. 3.3. The factor, f_{CM} stays constant at low voltages (low injection) and drops sharply for $V_{BE}' > 0.75$ V due to the presence of numerous excess carriers (high injection) in the quasi-neutral region.

3.2.3 Emitter Current Crowding

As the base current flows through the active base region, a potential drop in the horizontal direction causes a progressive lateral reduction of dc bias along the emitter-base junction. Consequently, the emitter current crowding occurs at the peripheral emitter edges. Figure 3.4 shows emitter current crowding across the active base region in a plot of the electron current density. This plot is drawn horizontally from the middle of the emitter ($x = 0$) to the left side emitter edge ($x = W_E/2$) using the two-dimensional device simulator PISCES [14]. In the PISCES simulations, the physical features of the transistor include a 2 μm emitter width ($W_E/2 = 1$ μm), a 0.1 μm emitter junction depth, X_{JE}, a 0.2 μm base junction depth, X_{JB}, and a 0.7 μm epi-layer depth, X_{EPI}.

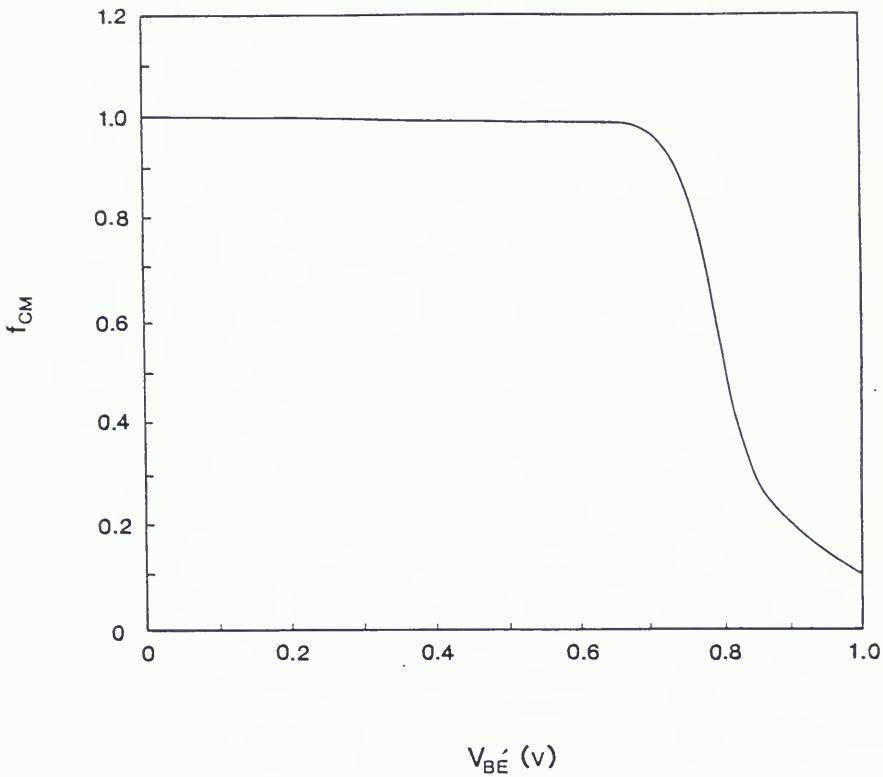

Figure 3.3 Plot of the base-conductivity-modulation factor, f_{CM} versus the base-emitter junction voltage, $V_{BE'}$.

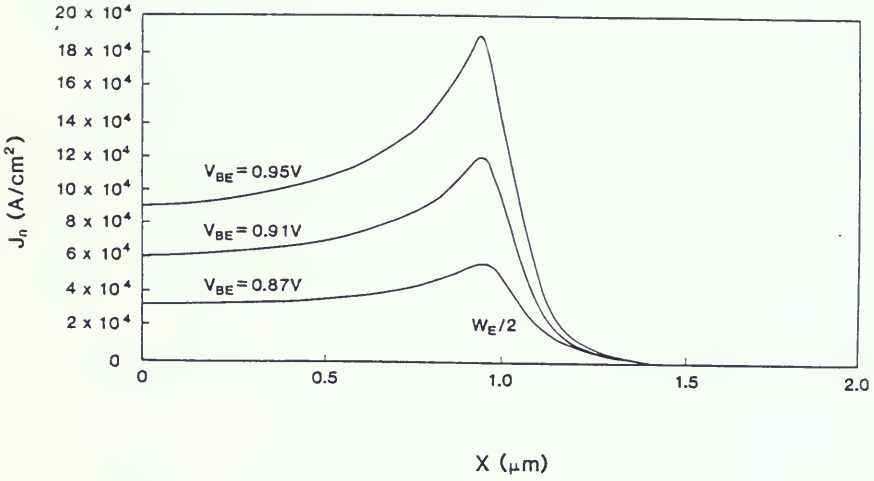

Figure 3.4 PISCES simulation of electron current density horizontally along the emitter-base junction. In this figure, x = 0 represents the center of the emitter; the increasing x is closer to the base contact.

The doping profiles are assumed Gaussian for the emitter, Gaussian for the base, and uniform for the epi-layer. The peak dopings are 2×10^{20} cm^{-3}, 8×10^{17} cm^{-3}, and 2×10^{16} cm^{-3} in the emitter, intrinsic base, and epi-layer, respectively. The non-uniform emitter current distribution (Fig. 3.4) makes the effective emitter width smaller [40-42]. Hence, emitter current crowding reduces the magnitude of R_{BI}.

In order to analytically represent the effects of emitter crowding, a variable named the emitter crowding factor, $f_{CROWDING}$ is employed. The emitter crowding factor is defined as the ratio of the emitter current with emitter crowding to the emitter current without emitter crowding [40], [41], [43]:

$$f_{CROWDING} \equiv I_E \text{ with emitter crowding} / I_E \text{ without emitter crowding}$$

$$= \frac{\int_0^{W_E} J_E(x)\, dx}{\int_0^{W_E} J_E(0)\, dx} \qquad (3.7)$$

where $J_E(0)$ is the emitter current density at the emitter edge.

In general, the integration of $J_E(x)$, the non-uniform emitter current caused by lateral ohmic drops, can not be solved analytically [40-42], [44]. Equation (3.7) is solved numerically by using Simpson's integration method applied to a circuit network.

The circuit network in Fig. 3.5 is used to model the current densities at various partitioned regions. The emitter-current density at the different emitter sections including the ohmic drops in the quasi-neutral base and emitter region are:

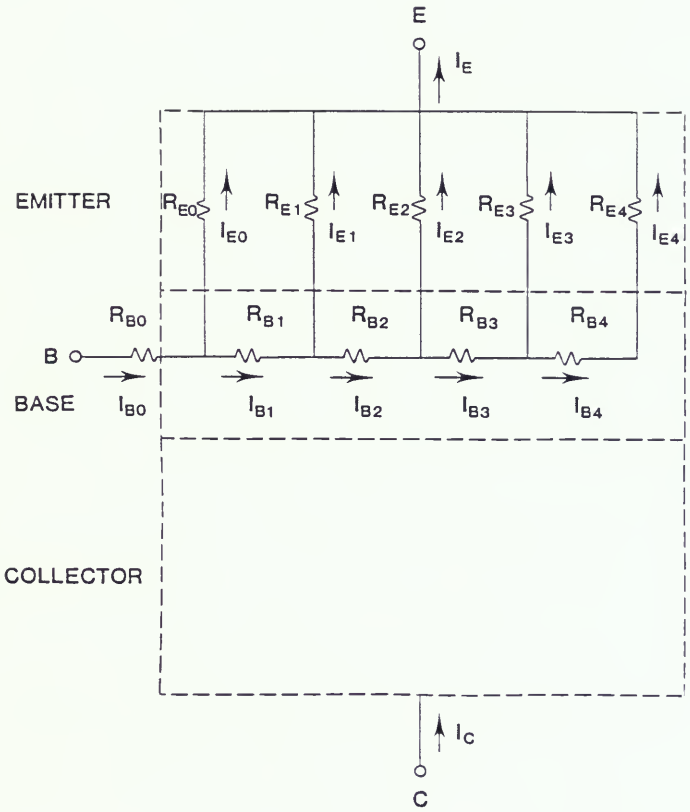

Figure 3.5 Equivalent circuit representing the ohmic drops in the quasi-neutral base and emitter regions.

$$I_{E0} = I_{SE}/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{E0}R_{E0})/V_T] \quad (3.8)$$

$$I_{E1} = I_{SE}/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{B1}R_{B1}-I_{E1}R_{E1})/V_T] \quad (3.9)$$

$$I_{E2} = I_{SE}/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{B1}R_{B1}-I_{B2}R_{B2}-I_{E2}R_{E2})/V_T] \quad (3.10)$$

$$I_{E3} = I_{SE}/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{B1}R_{B1}-I_{B2}R_{B2}-I_{B3}R_{B3}-I_{E3}R_{E3})/V_T] \quad (3.11)$$

$$I_{E4} = I_{SE}/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{B1}R_{B1}-I_{B2}R_{B2}-I_{B3}R_{B3}-I_{B4}R_{B4} -I_{E4}R_{E4})/VT] \quad (3.12)$$

where I_{SE} is the emitter current at $V_{BE} = V_{BE'} = 0$ V, R_{Bj}, R_{Ej} are the emitter, base series resistances in the partitioned region j. As a first order approximation, $R_{B0} = R_{BX}$, $R_{Bj}(j=1,2,3,4) = R_{BI}/4$, $R_{Ej}(j=0,1,2,3,4) = 5\ R_E$. The base currents ($I_{B0}$, I_{B1}, I_{B2}, I_{B3}, I_{B4}) can also be calculated by using (3.8)-(3.12) provided $I_{SE}/5$ is replaced by $I_{SE}/(5(\beta_F+1))$. β_F is the maximum forward current gain.

Using the Simpson's integration method, the total emitter current $I_E = (I_{E0}+4I_{E1}+2I_{E2}+4I_{E3}+I_{E4})/12$ is calculated for a single-base-contact BJT. The method also applies to a double-base-contact BJT in which the equations for I_{E3} and I_{E4} should be replaced by those of I_{E1} and I_{E0} due to a symmetry current crowding in the left and right halves of the BJT. Note that the accuracy can be improved if the structure in Fig. 3.5 is divided into more sections, but there is a trade-off in terms of the increased CPU time. The calculated $f_{CROWDING}$ versus V_{BE} is shown in Fig. 3.6. The solid line represents the emitter crowding factor without conductivity modulation. The dashed line represents the emitter crowding factor with conductivity modulation. This second order effect lessens the level of emitter current crowding and will be

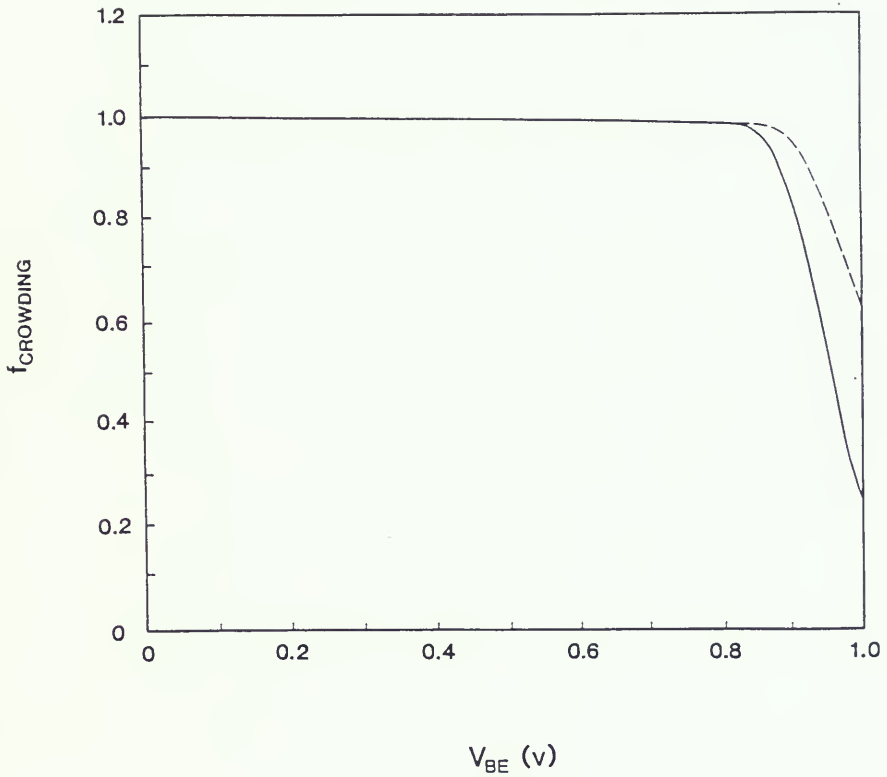

Figure 3.6 Plot of the emitter crowding factor, $f_{CROWDING}$ versus the base-emitter applied voltage, V_{BE} with R_{BI} = 480 Ω, R_E = 20 Ω, $I_{SE} = 10 \times 10^{-18}$ A, $I_{SB} = 6 \times 10^{-20}$ A for a single-base-contact BJT. The solid line represents the emitter crowding without base-conductivity modulation and the dashed line represents the emitter crowding with base conductivity modulation.

discussed later. The emitter current crowding becomes important when $V_{BE} \geq 0.85$ V. In general, emitter crowding is more pronounced at high currents (see Fig. 3.4) and for devices with large emitter width and high intrinsic base sheet resistance.

3.2.4 Base Pushout

For bipolar transistors operating at high currents, base pushout can occur [3]. Based on PISCES simulations, Fig. 3.7 shows hole concentrations of a n^+-p-n-n^+ BJT at the emitter-collector applied voltage, $V_{CE} = 2.0$ V and $V_{BE} = 0.87$ V, 0.91 V, and 0.95 V. Base pushout initiates when V_{BE} is greater than 0.87 V for the doping profile used in Sec. 3.2.

The current-induced incremental base width, δX_B is [25]

$$\delta X_B = W_{EPI} \left(1 - \frac{(J_0 - qv_sN_{EPI})^{1/2}}{(J_C - qv_sN_{EPI})^{1/2}}\right) \qquad \text{for } J_C > J_0 \tag{3.13}$$

where W_{EPI} is the epitaxial-collector width between the base-collector junction and collector high-low junction, v_s is the saturation velocity, J_C is the collector current density, and J_0 is the onset collector current density for base pushout ($J_0 = qv_s(N_{epi}+2V_{CB}/qW_{EPI}^2)$).

The variation of base resistance due to base-widening is shown in the plot in Fig. 3.8. We define a base-pushout factor, $f_{PUSHOUT}$ as the ratio of base width, X_B without base widening to base width with base widening ($X_B + \Delta X_B$). Thus,

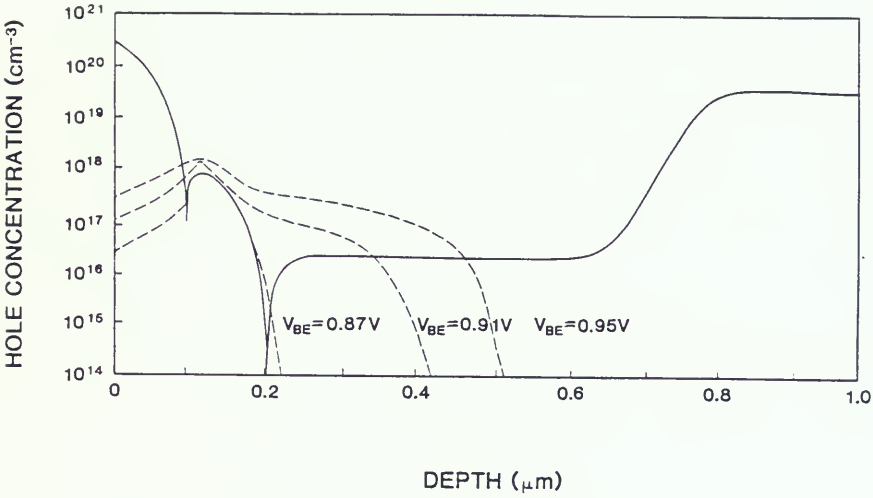

Figure 3.7 PISCES simulation of hole concentration plot along the vertical direction at V_{CE} = 2 V, V_{BE} = 0.87 V, 0.91 V, and 0.95 V (dashed lines). The solid line is the doping profile from emitter to collector. Depth zero stands for emitter surface.

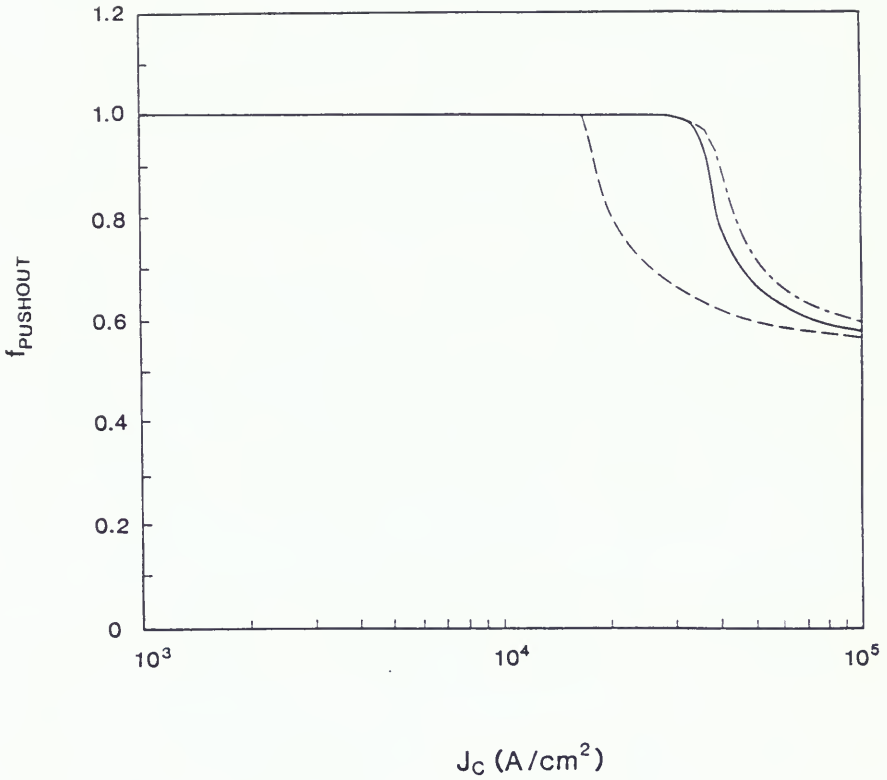

Figure 3.8 Plot of the base pushout factor, $f_{PUSHOUT}$ versus the collector current density, J_C (A/cm^2). The solid line represents the epi-layer doping density, $N_{epi} = 2 \times 10^{16}$ cm^{-3}, the epitaxial collector thickness, $W_{epi} = 0.5$ μm, and the collector-base applied voltage, $V_{CB} = 2.0$ V, the dashed line represents $N_{epi} = 0.8 \times 10^{16}$ cm^{-3}, $W_{epi} = 0.5$ μm, and $V_{CB} = 2.0$ V, and the dotted and dashed line represents $N_{epi} = 2 \times 10^{16}$ cm^{-3}, $W_{epi} = 0.5$ μm, and $V_{CB} = 3.0$ V.

$$f_{PUSHOUT} = 1 \qquad \text{for } J_C < J_0,$$

$$= \{1 + \frac{W_{EPI}}{X_B}\,[1 - \frac{(J_0 - qv_sN_{EPI})^{1/2}}{(J_C - qv_sN_{EPI})^{1/2}}]\}^{-1} \qquad \text{for } J_C > J_0. \qquad (3.14)$$

Figure 3.8 shows a plot of $f_{PUSHOUT}$ versus J_C. In Fig. 3.8, the solid line represents BJT pushout for a collector with $N_{EPI} = 2 \times 10^{16}$ cm^{-3}, $W_{EPI} = 0.5$ μm, and $V_{CB} = 2.0$ V, the dashed line represents BJT base pushout with $N_{EPI} = 0.8 \times 10^{16}$ cm^{-3}, $W_{EPI} = 0.5$ μm, and $V_{CB} = 2.0$ V, and the dotted and dashed line represents BJT base pushout with $N_{EPI} = 2 \times 10^{16}$ cm^{-3}, $W_{EPI} = 0.5$ μm, and $V_{CB} = 3.0$ V. The base widening is more significant when the epi-layer doping density is low, the width of the epitaxial collector is large, or the collector-base applied voltage is small. The base-widening increases dramatically for BJT operated at high current densities and results in a very low $f_{PUSHOUT}$.

3.2.4 The Coupling Effects

The emitter-crowding factor taking into account the conductivity modulation, base width modulation, and base pushout in the emitter crowding mechanism is discussed in this section. In general, the high conductivity from high injection reduces the emitter current crowding (see dotted line in Fig. 3.6). Also, the base width modulation and base pushout effects result in a smaller effective base resistance. These effects lessens the level of emitter current crowding.

To model a better emitter-crowding factor, $f'_{CROWDING}$ which accounts for the second order effects (base conductivity modulation, base width modulation, and base pushout) in the emitter crowding mechanism, a parameter f_c ($f_c \equiv f_{BWM} \times f_{CM} \times f_{PUSHOUT}$) is incorporated

into (3.8)-(3.12). The parameter fc modifies the base resistance in each partitioned region of the intrinsic base. Thus if base resistance is lower due to base conductivity modulation, base width modulation, or base pushout, the $I_B R_{BI}$ drop due to intrinsic base resistance is reduced in the current crowding calculation.

$$I_{E0} = I_{SE}/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{E0}R_{E0})/V_T] \tag{3.15}$$

$$I_{E1} = I_{SE}/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{B1}R_{B1}f_c-I_{E1}R_{E1})/V_T] \tag{3.16}$$

$$I_{E2} = I_{SE}/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{B1}R_{B1}f_c-I_{B2}R_{B2}f_c-I_{E2}R_{E2})/V_T] \tag{3.17}$$

$$I_{E3} = I_SE/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{B1}R_{B1}f_c-I_{B2}R_{B2}f_c-I_{B3}R_{B3}f_c -I_{E3}R_{E3})/V_T] \tag{3.18}$$

$$I_{E4} = I_{SE}/5 \exp[(V_{BE}-I_{B0}R_{B0}-I_{B1}R_{B1}f_c-I_{B2}R_{B2}f_c-I_{B3}R_{B3}f_c -I_{B4}R_{B4}f_c-I_{E4}R_{E4})/VT] \tag{3.19}$$

Using (3.7), (3.15)-(3.19) together with the Simpson's method, $f'_{CROWDING}$ can be calculated numerically.

3.3 The Nonlinear Base Resistance Model

The physical mechanisms for modeling the current-dependent base resistance have been discussed in Sec. 3.2. A simple method of estimating the combined effects of all the contributing factors in the base resistance is to multiply then together in a liner fashion. In fact, the multiplication of those physical factors produces a very acceptable first order model of the current-dependent base resistance that agrees with experiments. Thus,

$$R_{BI} = R_{BIO} \times f_{BWM} \times f_{CM} \times f'_{CROWDING} \times f_{PUSHOUT} \tag{3.20}$$

where R_{BIO} is the intrinsic base resistance at $V_{BE} = 0$ V. R_{BIO} equals $W_E\rho_b/12L_E$ for a rectangular emitter with base contact on two sides, and $W_E\rho_b/3L_E$ for a rectangular emitter with single base contact [45]. ρ_b is the intrinsic base sheet resistivity at $V_{BE} = 0$ V.

The solid line in Fig. 3.9 represents R_B ($R_B = R_{BI} + R_{BO}$) calculated from the present model, where R_{BO} can be obtained through measurements [33], [34], circuit simulation [36], or device simulations. The gradual reduction of R_B at low V_{BE} is caused by the emitter-base space-charge region shrinkage. The sharp decrease of R_B at high V_{BE} is due to base conductivity modulation, base pushout, and emitter current crowding effects.

3.4. Model Verification with Experiments

A method is developed in this section for obtaining R_B at high voltages. An ideal base current, I_{Bideal} without ohmic drops in the quasi-neutral base and emitter regions can be defined

$$I_{Bideal} = I_{SB} \exp(qV_{BE}/nkT) \tag{3.21}$$

where I_{SB} is the pre-exponential base current ($I_{SB} \equiv I_{SE}/(\beta_F+1)$), n is the nonideal base coefficient. $n \simeq 1$ for metal emitter contact, and $n \geq 1$ for a polysilicon contact BJT in the current technologies [35].

The actual base current from measurement is [1]

$$I_B = I_{SB} \exp[q(V_{BE}-\Delta V)/nkT] \tag{3.22}$$

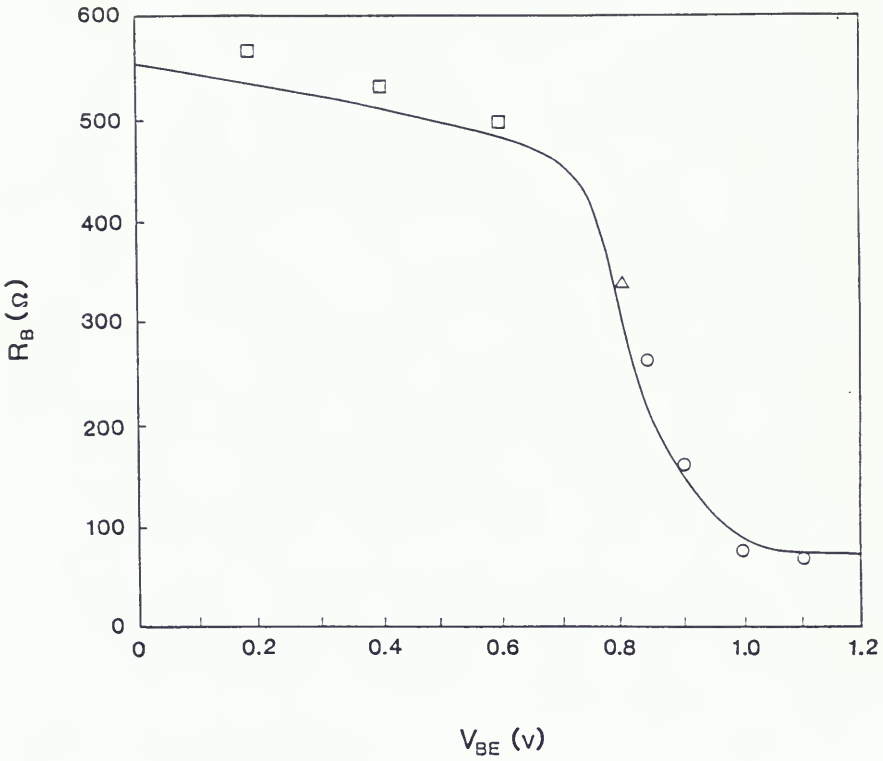

Figure 3.9 Plot of the base resistance, R_B versus the base-emitter applied voltage, V_{BE}. The solid line represents the simulation result from the present R_B model, squares represent PISCES simulation data, triangle represents Ning and Tang's method data, and circles represent DC measurement data at high currents.

From (3.21), (3.22) the ohmic drop ΔV ($\Delta V = I_E R_E + I_B R_B$) is

$$\Delta V = (nkT/q)[\ln(I_{Bideal}/I_B)] \tag{3.23}$$

$$\text{thus} \quad R_B(V_{BE}) = \frac{1}{I_B}\left\{\frac{nkT}{q}\ln\left(\frac{I_{Bideal}}{I_B}\right) - I_E R_E\right\} \tag{3.24}$$

Since I_B, I_{SB}, and I_E are known from measurement directly, n is extracted in the intermediate current level (prior to ohmic drop region) by (3.21), R_E can be extracted from open collector method [46] or ac method [34], and I_{Bideal} can be calculated from (3.21), the excitation-dependent base resistance R_B can be computed from (3.24). When emitter current crowding occurs, however, the emitter resistance R_E increases due to a smaller effective emitter area. Thus, emitter-crowding factor, $f'_{CROWDING}$ must be included in the R_E term in (3.24) to obtain a more accurate R_B:

$$R_B(V_{BE}) = \frac{1}{I_B}\left\{\frac{nkT}{q}\ln\left(\frac{I_{Bideal}}{I_B}\right) - \frac{I_E R_E}{f'_{CROWDING}}\right\} \tag{3.25}$$

The low current base resistance value, on the other hand, is extracted from device simulations because ΔV is negligible compared to V_{BE} in low current and difficult to measure. R_{BI} in low currents is computed as $W_E^2/mL_E\iint q\mu_p(x,y)p(x,y)dxdy$ where the position-dependent hole mobility $\mu_p(x,y)$ and hole concentration are known from PISCES simulations. Here, m = 3 for a rectangular emitter with one base contact, and m = 12 for a rectangular emitter with two base contacts.

Combining the above methods for R_B characterization and a dc method [33], the base resistance is obtained (Fig. 3.9). The results

from the present model are in good agreement with measurements. A small derivation is present at low V_{BE} and this is due to the fuzzy boundaries of the moving space-charge-region edges in the PISCES simulations.

3.5 Application

In order to demonstrate the utility of the current-dependent base resistance model, the present model was implemented in SLICE using user-defined subroutines [10]. Transient simulations from Gummel-Poon model with current-dependent base resistance for an ECL circuit are illustrated in Fig. 3.10. The ECL gate has the load resistances, R_{L1} = 270 Ω, R_{L2} = 290 Ω, and the current source resistance, R_I = 1.24 KΩ. The input pulse waveform has logic swing from -1.55 V to -0.75 V with 20 ps ramp followed by a flat pulse of 400 ps, and then a falling ramp of 20 ps from -0.75 to -1.55 V. Figure 3.10 indicates that the constant base resistance chosen at low injection (dashed line) overestimates the propagation delay of ECL logic and that the nonlinear base resistance model (solid line) yields a more realistic switching transient in which the base resistance changes drastically during the large-signal transition. These simulations indicate that the existing constant R_B model is inadequate for predicting the transient performance of advanced bipolar technologies and the current-dependent base resistance model is superior for BJT predicting transients.

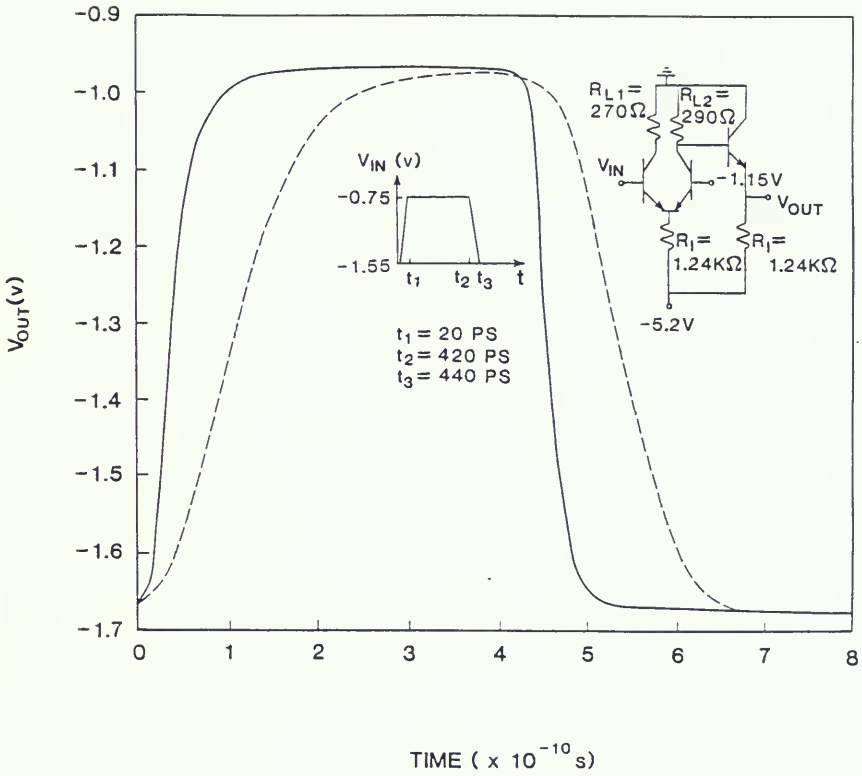

Figure 3.10 Transient responses from Gummel-Poon model with constant base resistance model (dashed line) and current-dependent base resistance model (solid line) for an emitter-coupled logic inverter with an emitter follower.

3.6 Summary and Discussion

A physics-based current-dependent base resistance model of bipolar junction transistors has been presented. The model is applicable for all injection levels and accounts for the effects of base width modulation, base conductivity modulation, base pushout, and emitter crowding. Interactions among these effects are also treated. The results obtained from the present model, from the two-dimensional device simulator PISCES, and from measurement data show excellent agreement.

We have implemented this physics-based base resistance model in SLICE/SPICE using user-defined subroutines. For an emitter-coupled logic circuit, the Gummel-Poon model with the present R_B model results in a more realistic transient response compared with that of the constant base resistance model. It is anticipated that the present model is useful for accurate bipolar integrated-circuit simulation in advanced IC technologies.

CHAPTER FOUR
CIRCUIT MODELING FOR TRANSIENT EMITTER CROWDING AND TWO-DIMENSIONAL CURRENT AND CHARGE DISTRIBUTION EFFECTS

4.1 Introduction

Today's advanced bipolar transistors, resulting from double polysilicon self-aligned technology, have been scaled down to submicrometer emitter widths and exhibit multidimensional current flow, especially when operated during high current transients. The one-dimensional BJT model [12] has been extended into a quasi-2-D model, useful for quasi-saturation, to account for the two-dimensional collector current spreading effects. In forward active mode the emitter current crowding will be significant if the base resistance is large and the collector current is high. In addition, this current crowding is enhanced during the BJT switch-on transient.

The emitter current crowding and sidewall injection effects have been investigated by numerous authors [40-45], [47-55]. Analytical solutions for emitter crowding were derived to formulate a distributed circuit model [42]. The assumption of a negligible emitter ohmic drop, $I_E R_E$ in [42] is not generally valid for the polysilicon bipolar transistors since $I_E R_E$ can be non-negligible compared to the base ohmic drop, $I_B R_B$. It is the author's experience that neither the distributed model [42] nor the two-lump empirical models [48] [49] are optimal for parameter extraction and circuit simulation in terms of CPU time. In addition, emitter-base sidewall injection and its junction charge

storage effects, usually neglected in the lumped circuit models, can be quite significant in small emitter-width VLSI BJT's.

In this chapter, an improved circuit model including nonuniform transient current and charge distribution effects is developed. The details of the model formulation are described in Section 4.2. In Section 4.3 the model is verified by measurements and transient device simulations. Conclusions are given in Section 4.4.

4.2. Model Development

A circuit model for the nonuniform current and charge distribution resulting from transient emitter crowding and emitter-base sidewall injection effects is discussed in this section.

4.2.1. Transient emitter crowding

As the base current flows through the active base region, a potential drop in the horizontal direction causes a progressive lateral reduction of dc bias along the emitter-base junction. Consequently, emitter current crowding occurs at the peripheral emitter edges. This nonuniform current distribution effect is enhanced in transient operation [55], in which the base resistance and junction capacitance contribute finite RC time constant (delay) in the base region. Thus the emitter edge of a BJT turns on earlier than the emitter center during a switch-on transient. Also, the charge (Q_{BE}) at the emitter edge is larger than at the center during switching.

In order to analytically represent the emitter crowding effect, a variable, emitter crowding factor f_{CR}, was defined as the ratio of the

emitter current with emitter crowding to the emitter current without emitter crowding (see Cahpter 3). In this Chapter, f_{CR} is treated as time-dependent for transient as well as steady state operation:

$$f_{CR}(t) = \frac{\int_0^{W_E} J_E[V(x,t)]dx}{\int_0^{W_E} J_E[V(0,t)]dx} \tag{4.1}$$

where J_E is the position and time-dependent emitter current density, x is the horizontal direction (x = 0 is the emitter edge), t is time, and V is the position and time-dependent junction voltage.

In general, $J_E(x,t)$, the nonuniform transient emitter current, can not be integrated analytically [41] [46]. Equation (4.1) is solved numerically using Simpson's integration method as

$$f_{CR} = \frac{\frac{W_E}{3n}\{J_E(0,t)+J_E(W_E,t)+4\sum_{j=1}^{n/2} J_E[(2j-1)W_E/n,t]+2\sum_{j=1}^{n/2-1} J_E(2jW_E/n,t)\}}{J_E(0,t)W_E} \tag{4.2}$$

A circuit network is used to model the current densities at various partitioned boundaries in a three-dimensional bipolar structure shown in Fig. 3.1. The concept of charge-based model was developed by Jeong and Fossum [12]. This work extends the development of Chapter 3 using this charge-based concept for regional BJT partitioning. The time-dependent lateral voltage drop, $I_{BI}(t)R_{BI}$ in the intrinsic base region is calculated using the partitioned intrinsic base series resistance, R_{Bj}, base current, $I_{BIj}(t)$, and charging currents,

$dQ_{BEj}(t)/dt$ and dQ_{BCj}/dt at the partioned region j.

The regional intrinsic base current $I_{BIj}(t)$ can be written as

$$I_{BIj} = \frac{I_S}{(n+1)\beta_F}\left[\exp\left(\frac{V_{BEj}(t)}{V_T}\right)-1\right] + \frac{C_2 I_S}{(n+1)}\left[\exp\left(\frac{V_{BEj}(t)}{V_T}\right)-1\right]$$
$$+ \frac{I_S}{(n+1)\beta R}\left[\exp\left(\frac{V_{BCj}(t)}{V_T}\right)-1\right] + \frac{C_4 I_S}{(n+1)}\left[\exp\left(\frac{V_{BCj}(t)}{V_T}\right)-1\right] \quad (4.3)$$

$$V_{BEj}(t) = V_{BE}(t) - I_B(t)R_{BX} - I_E(t)R_E - \sum_{k=1}^{j} I_{BI(k-1)}(t)R_{Bk} \quad (4.4)$$

$$V_{BCj}(t) = V_{BC}(t) - I_B(t)R_{BX} - I_C(t)R_C - \sum_{k=1}^{j} I_{BI(k-1)}(t)R_{Bk} \quad (4.5)$$

where R_{BX} is the extrinsic base resistance, R_{Bk} is the regional intrinsic base resistance ($R_{Bk} = 1/n\ R_{BI0} \times f_{BWM} \times f_{CM}$), V_T is the thermal voltage kT/q, and I_S, I_B, I_E, I_C, β_F, β_R, R_C, R_E, n_e, n_c, C_2, and C_4 retain their usual meanings in the Gummel-Poon model.

The regional base-emitter charging (transient) current is

$$\frac{dQ_{BEj}(t)}{dt} = \frac{1}{n+1}\frac{d}{dt}\left\{\tau_F I_S\left[\exp\left(\frac{V_{BEj}(t)}{V_T}\right)-1\right] + A_E\int C_{JE}[V_{BEj}(t)]dV\right\} \quad (4.6)$$

where C_{JE} is the voltage-dependent emitter-base junction capacitance, A_E is the emitter area, and τ_F is the forward transit time. Similarly, the regional base-collector charging current, $dQ_{BCj}(t)/dt$ can be found.

The junction capacitance model in SPICE2 is based on the depletion approximation. This simple model holds for C_{JC}, the collector-base junction capacitance, in which the collector-base

junction is reverse-biased when the BJT is at the forward active mode. When emitter crowding occurs, however, the junction voltage across the emitter-base space-charge region is usually high enough to invalidate the depletion approximation for finding the emitter-base junction capacitance. A recently developed junction capacitance model [37] which takes into account the free carrier charges in the space-charge region in high forward bias is therefore used in this circuit model to determine emitter-base charging currents. The biased-dependent C_{JE} model can be found in Section 3.2.1.

Through the regional voltage drops which define the position and time-dependent junction voltages, the nonuniform currents and charges under the emitter are determined. For example, the nonuniform quasi-static charges under the emitter are described by the position and time-dependent regional charge, $Q_j(x,t)$ which is a function of its junction voltage, $V_j(x,t)$.

Figure 4.1 shows a partitioned circuit model including the transient crowding effects using charge-based circuit modeling approach [12] [23]. In Fig. 4.1 the collector current under the emitter is the product of the current crowding factor f_{CR} and the collector current without emitter current crowding. The current crowding factor is equivalent to the effective emitter area ratio (A_{Eeff}/A_E) in [40] [41] [45]. Applying (4.1)-(4.2) to the partitioned model for n = 2 yields

$$I_C = f_{CR}\{I_S\exp[\frac{V_{BE}(t)-I_B(t)R_{BX}-I_E(t)R_E}{V_T}] + C_2I_S\exp[\frac{V_{BE}(t)-I_B(t)R_{BX}-I_E(t)R_E}{n_eV_T}]\} \quad (4.7)$$

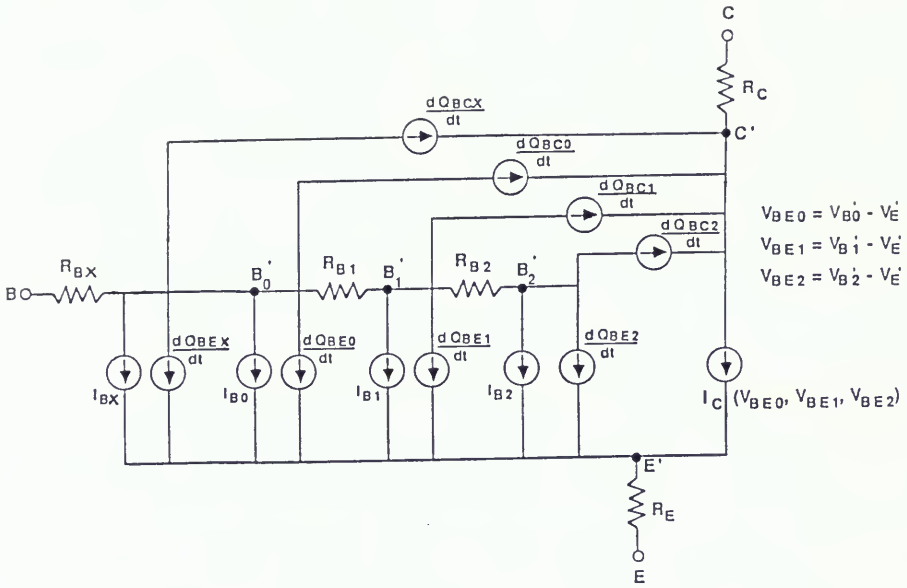

Figure 4.1 Network representation of the charge-based bipolar model including the nonuniform transient current and charge distribution effects.

$$f_{CR} = \frac{\exp[V_{BE0}(t)]+4\exp[V_{BE1}(t)]+\exp[V_{BE2}(t)]}{6\exp(V_{BE0}(t))} \tag{4.8}$$

where V_{BE0}, V_{BE1}, and V_{BE2} are the position and time-dependent base-emitter junction voltages at the emitter edges (V_{BE0}, V_{BE2}) and emitter center (V_{BE1}). Note that the present model takes into account both dc and transient emitter crowding and it can be easily reduced to a dc model by removing the transient current sources in Fig. 4.2. In addition, the equivalent distributed two-dimensional circuit model avoids the convergence, grid, and cost problems associated with transient numerical device simulations while still providing an accurate prediction of transient current crowding (see Fig. 4.7) with much less CPU time.

4.2.2. Sidewall Injection Current and Junction Charge Storage Effects

When the lateral dimensions of the emitter are in the same order of magnitude as the emitter width, the emitter-base sidewall plays a significant role in the performance of the bipolar transistor [52]. To accurately model the nonuniform current and charge distribution in the advanced BJT, the emitter-base sidewall injection current and its associated junction stored charge should be modeled. An analysis of a PISCES simulation of an advanced bipolar transistor is performed to identify multidimensional currents. In PISCES simulations, the BJT has a 1.2 μm emitter width, a 0.1 μm emitter junction depth, a 0.25 μm base junction depth, and a 0.7 μm epi-layer depth. The doping profiles are assumed Gaussian for the emitter, Gaussian for the base, and uniform for the epi-layer. The emitter dopant lateral straggles are assumed 75%

of the vertical straggles for the emitter sidewall lateral diffusion [18]. The peak dopings are 2×10^{20} cm^{-3}, 8×10^{17} cm^{-3}, and 2×10^{16} cm^{-3} in the emitter, intrinsic base, and epi-layer, respectively. The physical mechanisms used in PISCES simulations include Shockley-Read-Hall recombination, Auger recombination, bandgap narrowing, and doping and field-dependent mobility.

PISCES 2-D simulation readily shows the multidimensional current paths as illustrated in Fig. 4.2. The figure displays the electron-current-density and hole-current-density vector plots of the advanced BJT biased at V_{BE} = 0.85 V and V_{CE} = 3.0 V. The current vectors suggest that the sidewall injection contributes an important component of the base current. A quantitative measure of the sidewall current is given by integrating the electron current density and hole current density along the emitter-base junction sidewall. Simulation of the current gain versus emitter width also indicates the significance of the sidewall injection current and the emitter-width size effect on the current gain.

Figure 4.3 shows the β plots of three advanced BJT's with different emitter widths. The peak β of the BJT with the 1.5 μm emitter width is the highest followed by the peak β of the 1.0 μm emitter, and then the peak β of the 0.5 μm emitter. The PISCES 2-D-BJT simulations indicate the peak-current gains of the submicrometer advanced BJT's will be reduced significantly with scaling. Since the normalized collector currents (I_C/W_E) are approximately the same in these three structures, the primary reason for peak β reduction is the emitter-base sidewall injection current, which makes I_B not scalable. The β falloff

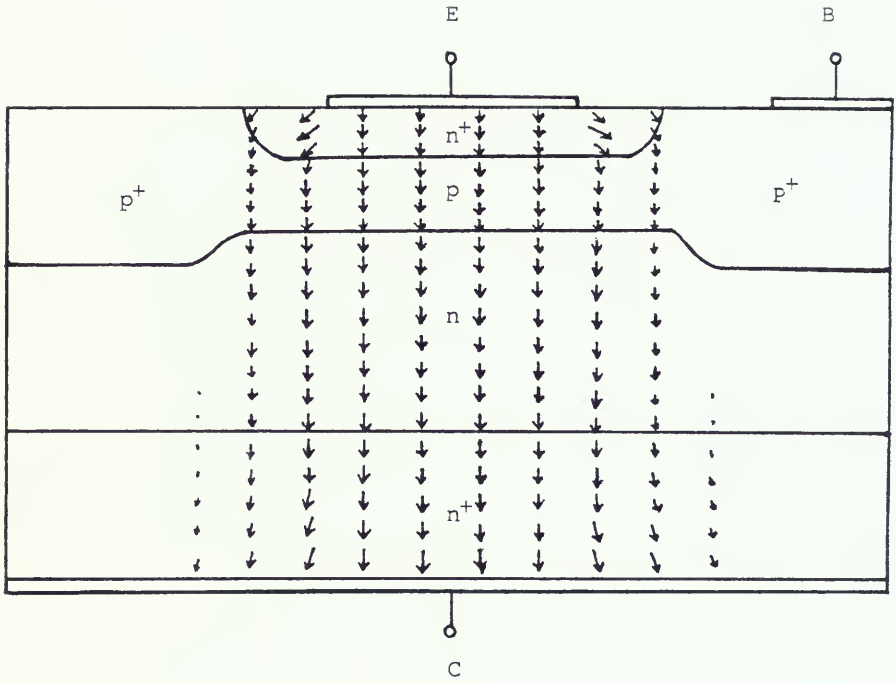

Figure 4.2.1 PISCES electron-current-density vector plot at V_{BE} = 0.85 V and V_{CE} = 3.0 V.

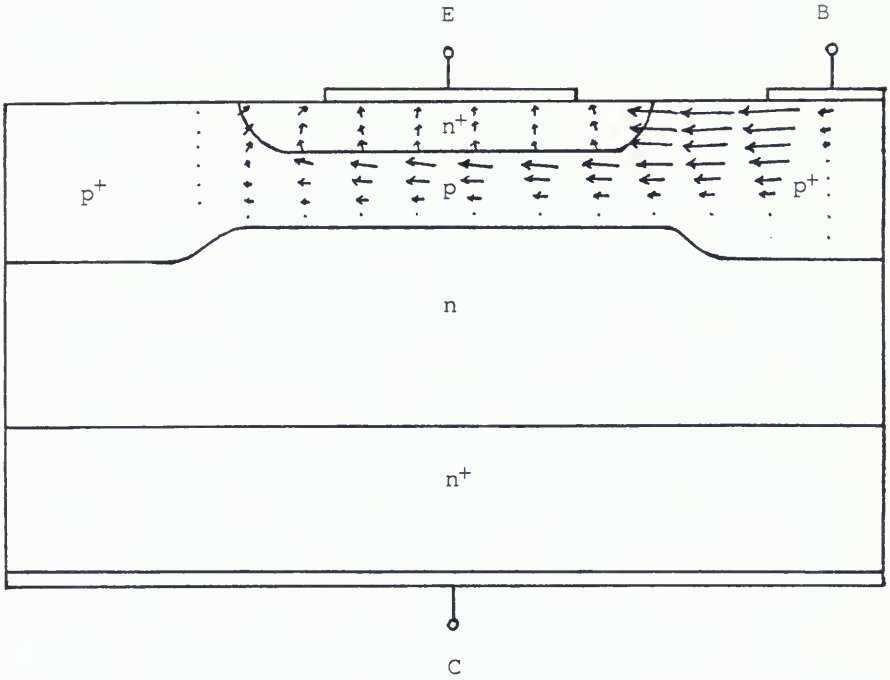

Figure 4.2.2 PISCES hole-current-density vector plot at V_{BE} = 0.85 V and V_{CE} = 3.0 V.

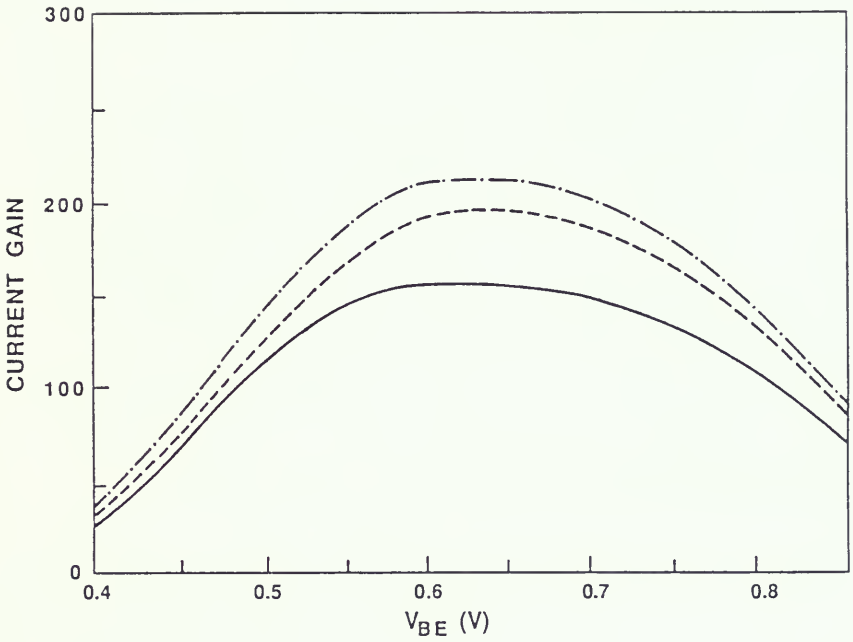

Figure 4.3 Plot of current gain versus V_{BE} at different emitter width, W_E. The solid line represents W_E = 0.5 μm, the dashed line represents W_E = 1.0 μm, and the dashed and dotted line represents W_E = 1.5 μm.

at the intermediate current level before high injection occurs is due to base-width modulation at the emitter-base junction; this effect is significant in narrow-base BJT's [56].

Based on device simulation and analytical approximation [52] [53], the emitter-base sidewall base current, I_{BX} is modeled using the ratio of the emitter perimeter to the emitter area:

$$I_{BX} = \frac{P_E X_{JE}}{A_E} \{\frac{I_S}{\beta_F} \exp[\frac{V_{BE}(t)-I_B(t)R_{BX}}{V_T}] + C_2 I_S \exp[\frac{V_{BE}(t)-I_B(t)R_{BX}}{V_T}]\} \tag{4.9}$$

where P_E is the emitter perimeter and X_{JE} is the emitter junction depth. Note that the lateral voltage drop under the emitter is defined as $I_{BI}R_{BI}$ in the emitter crowding mechanism. The use of voltage drop I_BR_{BI} in emitter crowding would overestimate the level of current crowding since the base current under the emitter (I_{BI}) can be quite different than the base terminal current (I_B) if the base sidewall current ($I_{BX} = I_B - I_{BI}$) is significant.

As a first-order approximation, the collector current flow out of the emitter-base sidewall can be neglected [52]. Thus the charge stored at the emitter-base junction sidewall, Q_{BEX} is determined by the sidewall junction capacitance, C_{JEX} so that $Q_{BEX} = P_E X_{JE} \int C_{JEX}(V)dV$. C_{JEX} is the same as Eqs. (3.2)-(3.5) providing different values for the junction gradient "a" and the effective junction built-in voltage V^*. Similarly, the extrinsic base-collector junction charge, Q_{BCX} associated with the collector-base junction outside the intrinsic emitter region is $(A_C - A_E) \int C_{JC}(V)dV$ because the collector current flows mainly in the intrinsic emitter region (see Fig. 4.3.1).

By combining the modeling methodologics in Secs. 4.2.1 and 4.2.2, the nonuniform transient currents and charges in an advanced BJT can be determined.

4.3. Model Verification with Experiments and Transient Device Simulations

The circuit model which includes the emitter crowding (dc and transient) and sidewall injection effects was implemented as user-defined-controlled-sources in SLICE. In SLICE/SPICE circuit analysis, UDCS's are user-defined subroutines (see Appendix B) that use the implicit nonlinear model equations to compute both charging current (dQ/dt) and transport current (I) in the model depicted in Fig. 4.1. The time derivatives of the quasi-static stored charges in the base thus properly represent the charge dynamics in the BJT. The lateral voltage drops ($V_{BE2}(t) < V_{BE1}(t) < V_{BE0}(t) < V_{BE}(t)$) are given as the system of model equations (I and dQ/dt) are solved simultaneously. Transient current crowding is then accounted for in the collector current by $f_{CR}(V_{BE0}(t), V_{BE1}(t), V_{BE2}(t))$.

Test devices representative of advanced BJT's were used to verify the model and to define a parameter-extraction scheme. The devices have drawn emitter width $W_E = 2\ \mu m$, emitter length $L_E = 8\ \mu m$ and the approximate active emitter area is $A_E = 1.2 \times 7.2\ \mu m^2$ due to sidewall spacer technology. The intrinsic and extrinsic base resistances are obtained by Ning and Tang's method [33]. The Gummel-Poon model parameters I_S, β_F, β_R, τ_F, τ_R, n_e, n_c, C_2, C_4, R_E, and R_C are extracted by the methods in [1]. Some of the physical parameters are determined from the process information (A_E, P_E, W_E, X_{JE}, and N_B) and from [25]

(n_i, V^*).

The BJT is measured from V_{BE} = 0.6 V to V_{BE} = 1.0 V with V_{CE} = 3 V to keep the transistor out of quasi-saturation. The simulated results from the present model and the Gummel-Poon model show excellent agreement with the experimental data at low currents; however, the simulated results from the Gummel-Poon model deviate significantly from measurements at high currents (see Fig. 4.4). The discrepancy would be exaggerated if Fig. 4.4 were shown on a linear scale.

Transient measurement of a ring oscillator introduces an extra propagation delay due to the interconnect between the first and last stages of the ring oscillator and the I/O pad capacitances which complicate measurement of the real inverter transient response [27]. Thus, to demonstrate the model utility in transient operation, the emitter crowding factor and pulse response of an inverter are simulated using the present model and compared with transient device simulation using PISCES. Figure 4.5 shows the emitter current density horizontally along the emitter-base junction at various times in the PISCES transient simulation. In Fig. 4.5 emitter crowding is very significant during the initial turn-on transient. The transient crowding factors obtained from PISCES and the present model are compared in Fig. 4.6. The model predictions show close agreement with PISCES transient simulations. This indicates that the lumped model in Fig. 4.1 correctly accounts for the nonuniform transient current and charge distribution effects. SLICE implementation employing the present model, which includes the transient crowding effects, is used to simulate a BJT inverter with 1.2 KΩ load resistor. The input pulse waveform consists

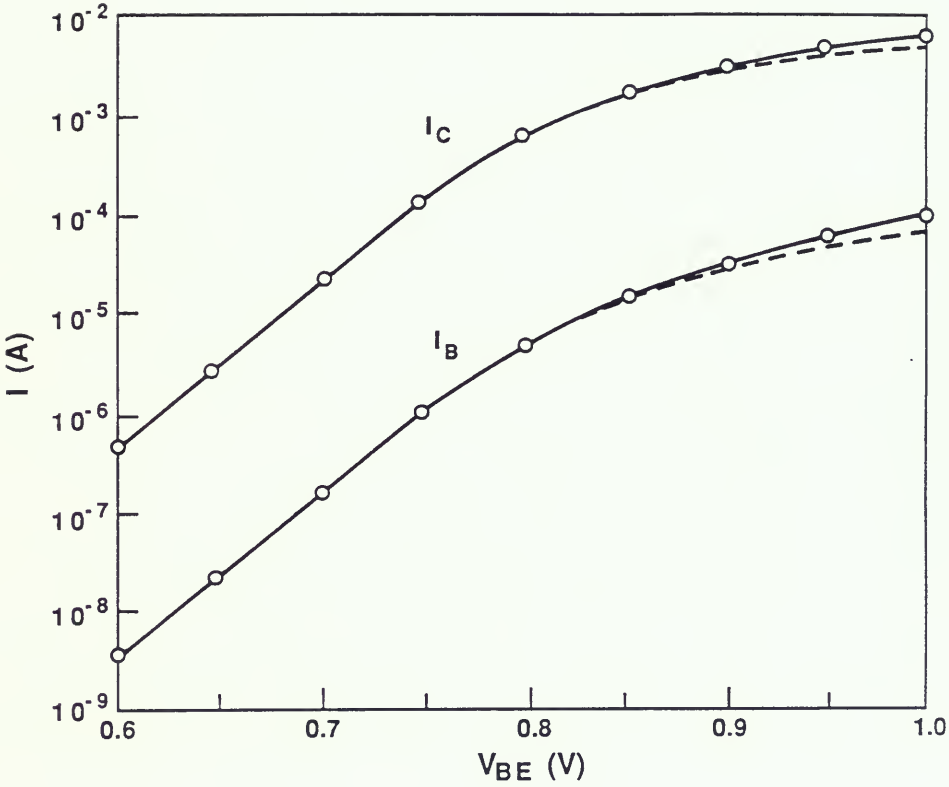

Figure 4.4 Log I versus base-emitter applied voltage, V_{BE}. The solid line represents the present model simulation, the dashed line represents the Gummel-Poon model simulation, and the circles represents the measurement.

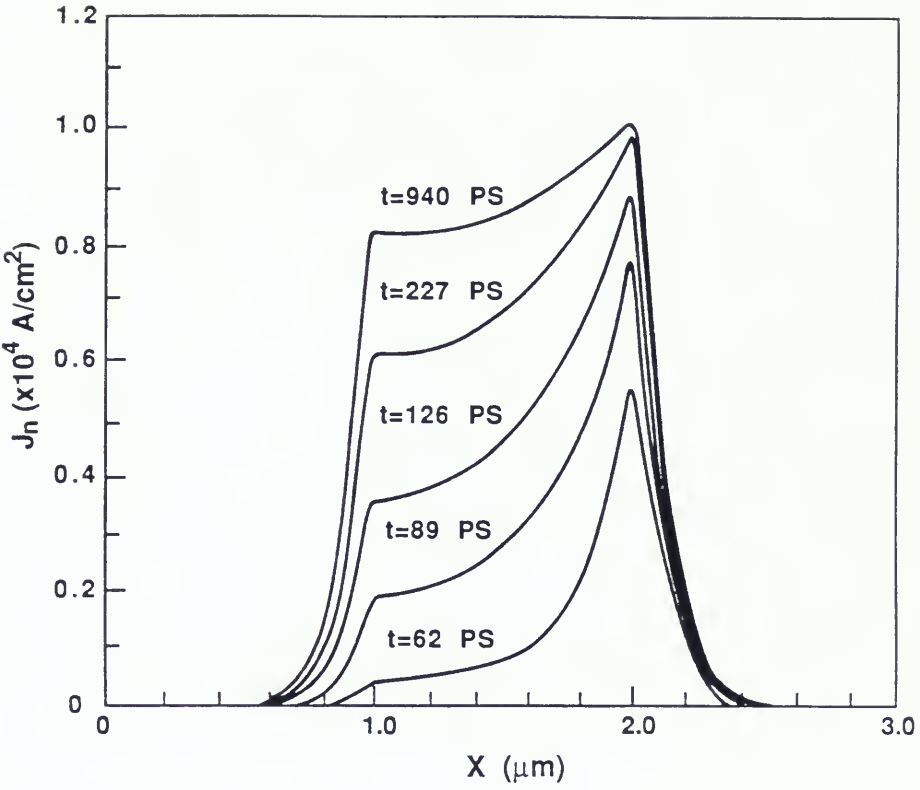

Figure 4.5 Electron current density distribution horizontally along the emitter-base junction at various times in PISCES transient simulation.

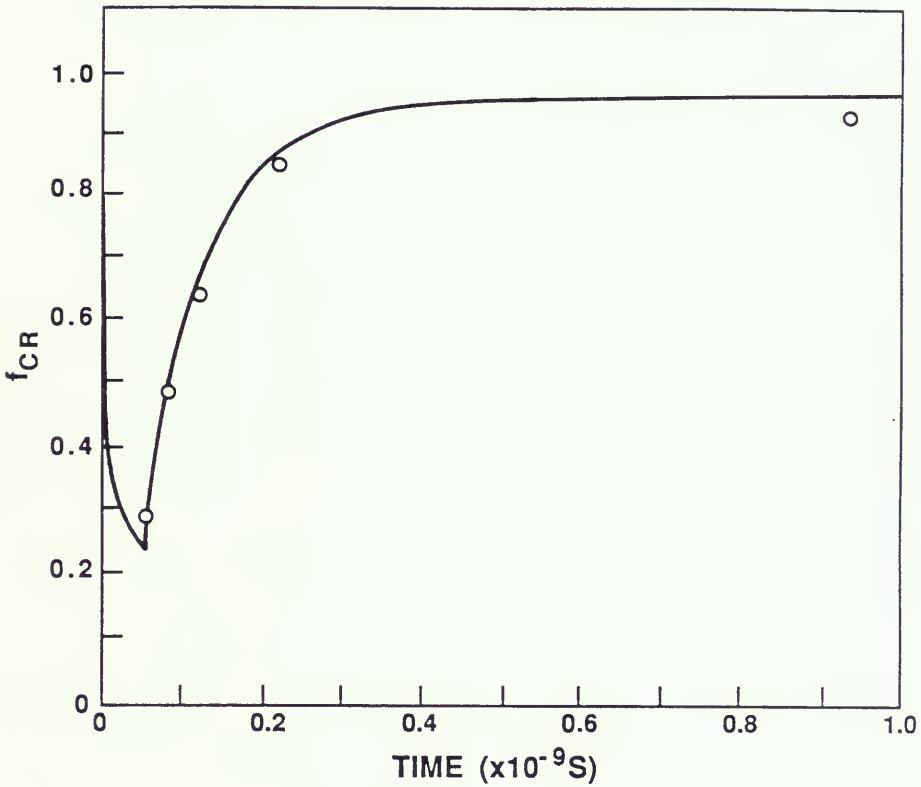

Figure 4.6 Plot of the emitter crowding factor versus time. The solid line represents SPICE simulation employing the present model, and the circles represent PISCES simulation.

of a 0.85 V, 50 ps ramp followed by a flat pulse of 1200 ps duration and then a falling 0.85 V ramp of 50 ps. Figure 4.7 shows the inverter transient responses from SPICE/SLICE (using the Gummel-Poon model and the present model) and PISCES. The predictions of the present model are in good agreement with PISCES results; however, the Gummel-Poon model shows a slower turn-on transient and a large propagation delay. The discrepancy between the Gummel-Poon and PISCES results is due to the nonuniform transient current and charge distribution in PISCES simulation which lowers the magnitude of the base impedance during switching. The use of a lumped base resistance measured at steady-state in the Gummel-Poon model predicts more delay than is actually observed.

4.4 Summary and Discussion

A new circuit model for the advanced bipolar transistor including nonuniform transient current and charge distribution effects has been developed. The model takes into account the transient emitter crowding mechanism, emitter-base sidewall injection, and extrinsic junction charge storage effects. The spatially partitioned model is developed based on physical insight gained from device simulations (dc and transient). Although the partitioning technique itself is straightforward, the present model represents the nonuniform current and charge distribution at the emitter-base sidewall and under the emitter in a unified manner. Furthermore, second order effects such as base-width modulation and base conductivity modulation, which decrease the intrinsic base resistance and emitter crowding are easily modeled in the equivalent circuit through a correction factor for the effective

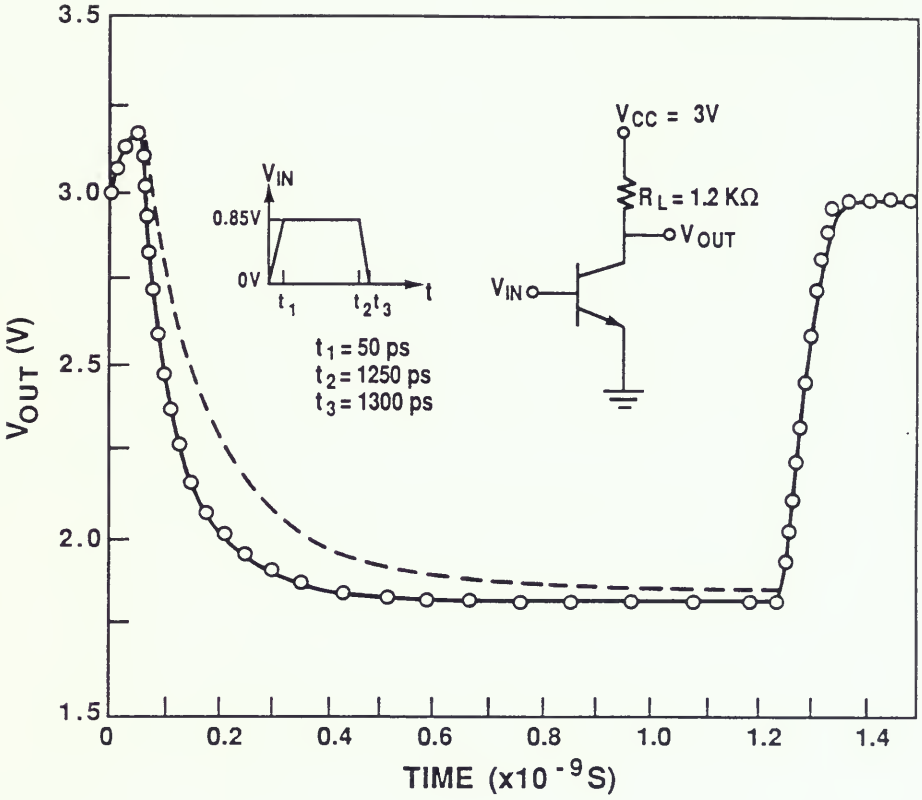

Figure 4.7 Simulated transient responses for a single-transistor inverter. The solid line represents the present model simulation, the dashed line represents the Gummel-Poon model simulation, and the circles represents PISCES transient simulation.

base charge. SLICE simulations employing the present model show excellent agreement with measurements and device simulations. Since the model correctly represents the charge dynamics of the BJT in transient operation, it is anticipated that the present model can be useful in advanced bipolar (or BiCMOS) modeling in technology computer-aided circuit design and process sensitivity diagnosis.

CHAPTER FIVE
S-PARAMETER MEASUREMENT PREDICTION USING A PHYSICAL DEVICE SIMULATOR

5.1 Introduction

Submicrometer emitter bipolar transistors produce small signal responses that are difficult to characterize with existing s-parameter equipment. State of the art probes, and proper calibration technique have proven essential in the measurement of s-parameters of single BJT test structure [57]. However, s-parameter measurements cannot predict the test-structure response of new BJT technologies in the "on paper" development stage.

A new method of predicting s-parameter test structure response from physical device simulator output has been developed. This predicted s-parameter response is particularly useful for examining the performance of conceptual designs of submicron BJT technologies. Submicrometer BJT's have significant dc, transient and small-signal multidimensional effects which include collector current spreading, emitter crowding, and emitter-base sidewall injection; these effects have been evaluated by a 2-D physical device simulator previously [58] [59] and are discussed in Chapters 2, 3, and 4. The new method of predicting s-parameter response provides a direct comparison between 2-D BJT simulations and measurement data from BJT test structures.

Important uses of this simulated s-parameter response also include verifying BJT test structure s-parameter measurements and

previous BJT characterizations. The derived BJT test structure response can be used to confirm the accuracy of existing test structures measurements, potentially reducing the total number of test structures, measurements, and cost necessary to characterize a BJT technology.

In order to get a complete characterization of a 3-port BJT, three sets of 2-port measurements must be taken. generally requiring 3 separate test structures. Since the 3-port measurement is time consuming and IC layout area intensive, often only a single 2-port BJT measurement is made. The s-parameter prediction technique can supplement an existing 2-port test structure measurement so that a complete 3-port BJT characterization is possible. The simulated s-parameter response also can be extended beyond s-parameter instrumentation frequency ranges.

This modeling technique is demonstrated using submicrometer BJT simulations from the PISCES 2-D physical device simulator [60]. Other small-signal device simulations or characterizations [61] could be substituted for the PISCES data. Simulated small-signal BJT y-parameter measurements are converted (via software) to s-parameters. S-parameter measurements are preferred for high-frequency characterizations and have been demonstrated on-chip at frequencies up to 50 GHz [62]. In addition, s-parameter best represent a distributed circuit with high frequency discontinuities [63], such as a BJT IC test structure measured at microwave frequencies. The BJT s-parameter response is incorporated into a BJT test structure model which includes the effects of IC interconnects, discontinuities and bond pads. The predicted s-parameter response for the BJT test structure is then calculated and

plots of the BJT test structure responses are presented. This modeling technique proves extremely useful for evaluating IC test structure characteristics.

This is the first time that the high frequency BJT test structure circuit modeling has been combined with a 2-D device simulation output in order to predict test structure s-parameter response. In addition, a novel two-layer metal-based BJT test structure with low attenuation is examined using this modeling. The modeling algorithms presented here may be applied in inverse fashion to extract accurate BJT small signal characteristics from s-parameter measurements or evaluate the accuracy of s-parameter calibration algorithms.

5.2 Bipolar Test Structure Modeling

In order to demonstrate the utility of the bipolar test structure modeling, an n-p-n BJT small-signal response was simulated using the PISCES program. The physical features of the BJT include a 1 μm emitter width (W_E = 0.5 μm), a 0.1 μm emitter-depth, a 0.2 μm base-depth, and a 0.8 μm epitaxial collector-depth shown in Fig. 2.1.1. The doping profiles are shown in Fig. 2.1.2. Small-signal parameters from 1-D, 2-D, or 3-D simulator may be used for input in this test structure modeling technique.

A 2-D simulation typically provides BJT y-parameter response up to the emitter contact, base contact, and collector contact. During y-parameter simulations the BJT is biased at V_{BE} = 0.8 V. and V_{CE} = 2.0 V and the frequency is varied from 10 MHz to 7 GHz. The y-parameters are normalized by the distributed circuit admittance (frequency dependent

interconnect admittance) and then converted to s-parameters. The y-parameter to s-parameter conversion equations are [64]:

$$s_{11} = \frac{(1-y_{11})(1+y_{22}) + y_{12}y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}y_{21}} \tag{5.1}$$

$$s_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22}) - y_{12}y_{21}} \tag{5.2}$$

$$s_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}y_{21}} \tag{5.3}$$

$$s_{22} = \frac{(1+y_{11})(1-y_{22}) + y_{12}y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}y_{21}} \tag{5.4}$$

In order to predict the s-parameter response of a specific BJT test structure layout, an equivalent high frequency circuit must be constructed. An example BJT test structure layout which is frequently used for s-parameter measurements is presented in Fig. 5.1. Here, the BJT is positioned between three bond pads that are connected to the transistor by IC interconnect. The bond pads are 100 μm by 100 μm and a bend is added to the IC interconnect between the base terminal and the base bond pad. The interconnect, the bond pads and the bend exhibit parasitic responses at microwave frequencies.

A flow chart which outlines the calculation of the BJT test structure response is shown in Fig. 5.2. The physical dimensions and doping profiles of the submicron BJT are entered into the device simulator program and dc and ac simulations are performed in order to predict y-parameters. These y-parameters are converted to s-parameters

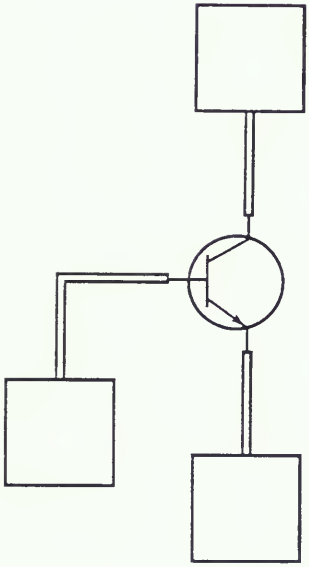

Figure 5.1 BJT test structure layout typically used for s-parameter measurement.

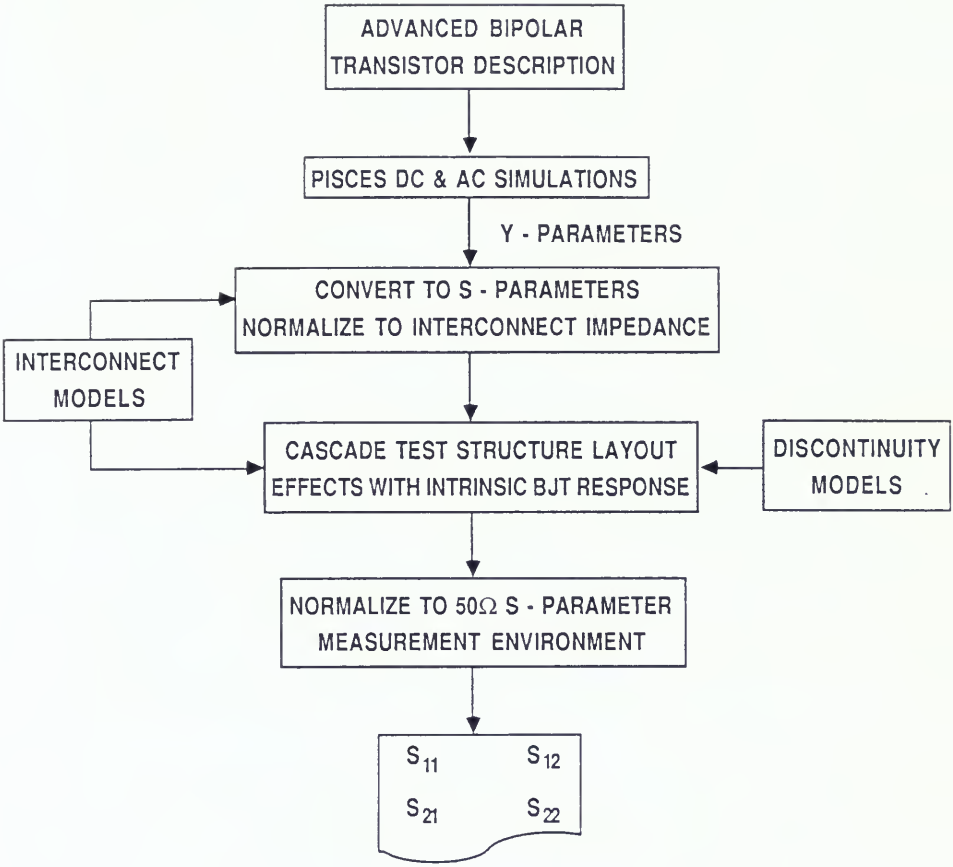

Figure 5.2 Flow chart outlining the calculation of the BJT test structure measurement.

after normalization by the on-chip interconnect admittance. Then the BJT s-parameters are cascaded with the s-parameter responses of the BJT layout elements (interconnect, bond pads and a bend in interconnect).

Figure 5.3 is a block diagram showing the order in which the matrix models of the interconnect, bend in interconnect and bond pads are cascaded. The BJT simulation (shown in the middle of the cascaded matrices) is multiplied by the surrounding component matrices. In order to do this, the s-parameter data in each component matrix are converted to readily cascaded high frequency T-parameters which are similar to low frequency ABCD parameters [63]. The cascaded T-parameter matrices are multiplied in order to model the BJT test structure response at the bond pads and the result is converted back to s-parameters.

The s-parameters at the bond pads, which are normalized by the on-chip interconnect admittance, are converted to a 50 Ω system impedance that is common to s-parameter instrumentation. This conversion employs the following equations [63]:

$$s_{11} = s_{22} = \frac{(Z^2 - Z_0^2)\ \sinh\gamma l}{2ZZ_0\cosh\gamma l + (Z^2+Z_0^2)\sinh\gamma l} \tag{5.5}$$

$$s_{21} = s_{21} = \frac{2ZZ_0}{2ZZ_0\cosh\gamma l + (Z^2+Z_0^2)\sinh\gamma l} \tag{5.6}$$

In these equations, Z is the transmission line impedance, Z_0 is the system impedance (50 Ω), γ is the propagation constant ($\gamma = \alpha + j\beta_p$), α is the attenuation constant, β_p is the phase constant, and l is the transmission line length.

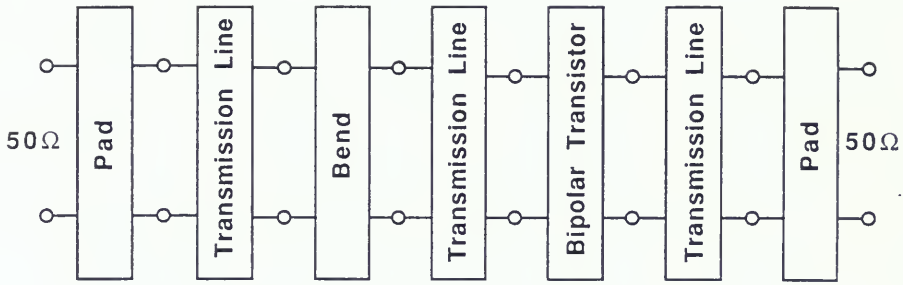

Figure 5.3 Cascade of the BJT test structure components and PISCES simulations for calculating s-parameter response.

Analytical circuit models from the microwave literature are used to represent the effects of IC interconnect and bends. The bond pads are treated as a section of wide lumped admittance since a probe or ball bond touches most of the bond pad area. The value of the bond pad admittance was estimated by calculating the lumped admittance of a short section of interconnect of the same dimensions as the bond pad. The microwave model for the bend in the interconnect was taken from the literature [63].

An IC interconnect cross-section with microstrip metal over SiO_2 over the Si substrate is used for the BJT test structure layout. Then a novel two-layer-metal IC interconnect is examined as a superior interconnect alternate. Fig. 5.4 displays a cross-section of a metal-SiO_2-Si microstrip interconnect cross-section. In Fig. 5.4 the width of the metal line is 20 μm, the thickness of the metal line is 1 μm, the thickness of the SiO_2 layer is 1 μm, the thickness of the Si substrate is 300 μm, and the resistivity of the Si substrate is 1 Ω-cm.

The transmission-line model for this interconnect system has a series impedance per unit length and a parallel admittance per unit length as shown in Fig. 5.5. The series impedance, Z is composed of R, the interconnect-line resistance plus L, the interconnect-line inductance. The parallel admittance of the transmission line includes the SiO_2 capacitance, C_1, in series with the parallel combination of the Si capacitance, C_2, and the Si conductance, G_2. The IC interconnect equations presented below are valid when the Si substrate layer is moderately to lightly doped [65] [66]:

$$L = \mu_0 F(h_1+h_2) \tag{5.7}$$

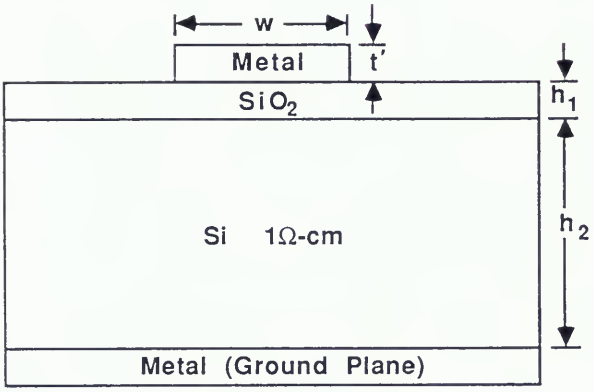

Figure 5.4 Cross-section of a metal-SiO_2-Si system, w = 20 μm, t' = 1 μm, h_1 = 1 μm, and h_2 = 300 μm.

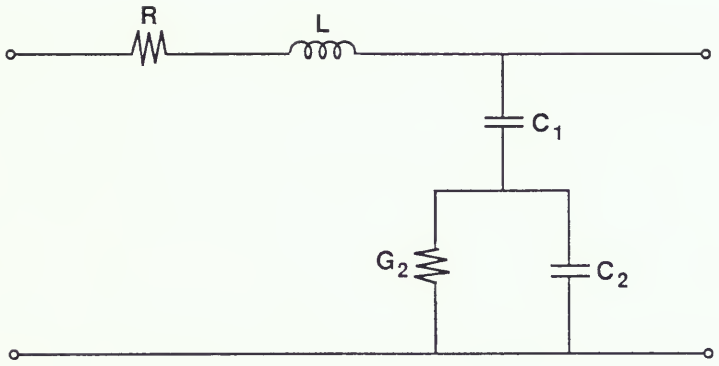

Figure 5.5 Transmission line circuit model for interconnect over metal-SiO_2-Si.

$$R = \frac{1}{\sigma_{METAL}\, w\, t'} \tag{5.8}$$

$$C_1 = \frac{\epsilon_0\, F_1(\epsilon_{SiO2},\, h_1)}{F(h_1)} \tag{5.9}$$

$$C_2 = \frac{\epsilon_0\, F_1(\epsilon_{Si},\, h_2)}{F(h_2)} \tag{5.10}$$

$$G_2 = \frac{\rho_{Si}\, [1+(1+10h_2/w)^{-1/2}]}{2\, F(h_2)} \tag{5.11}$$

$$F(h) = \frac{1}{2\pi} \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \quad \text{for} \quad h/w \geq 1 \tag{5.12}$$

$$= \frac{1}{w/h + 2.42 - 0.44h/w + (1-h/w)^6} \quad \text{for} \quad h/w < 1 \tag{5.13}$$

$$F_1(\epsilon,\, h) = \frac{\epsilon + 1}{2} + \frac{\epsilon - 1}{(1+10h/w)^{1/2}}. \tag{5.14}$$

In these expressions, ϵ_0 is the permittivity of free space, ϵ_{si} is the relative permittivity of Si, ϵ_{SiO2} is the relative permittivity of SiO_2, and μ_0 is the permeability of free space. The variable t', represents the interconnect thickness, w is the interconnect width, h_1 is the height of the SiO_2 layer, h_2 is the height of the Si substrate, σ_{Si} is the conductivity of the Si layer, and σ_{METAL} is the conductivity of the metal interconnect.

This interconnect model neglects the effect of skin-effect loss, α_c in the interconnect center conductor. The skin-effect loss may be

approximately modeled assuming that the phase constant, β_p is much greater than the attenuation of the transmission line. First the above equations are used to calculate $\alpha + j\beta_p = (ZY)^{1/2}$. The corrected propagation constant, γ is estimated from the following relationship, $\gamma = \alpha + \alpha_c + j\beta_p$ for low loss interconnect. The low loss condition implies that the addition of the skin-effect loss to the interconnect model has a negligible effect on the transmission line β_p. The equations governing the conductor skin-effect losses are [63] [67]:

$$\alpha_c = \frac{1.38\ C_1\ R_s\ [32-(w_e/h)2]}{h\ Z_0\ [32+(w_e/h)^2]} \qquad \text{for } \frac{w}{h} \le 1$$

$$= \frac{6.1\times10^{-5}\ C_1\ R_s\ Z_0\ \epsilon_{re}}{h}\left[\frac{w_e}{h} + \frac{0.667\ w_e/h}{w_e/h + 1.444}\right] \quad \text{for } \frac{w}{h} > 1 \qquad (5.15)$$

where $C_1 = 1 + \frac{w_e}{h}\left[1 + \frac{1}{\pi}\ln\frac{2C_2}{t}\right]$

$$R_s = (\pi f \mu_0 \rho)^{1/2}$$

$$C_2 = h \quad \text{for } \frac{w}{h} \ge \frac{1}{2\pi},$$

$$= 2\pi w \quad \text{for } \frac{w}{h} < \frac{1}{2\pi}.$$

In these expressions, ρ is the resistivity of the conducting microstrip and w_e is the effective conductor width which is a function of microstrip dimensions [63] [68] [69]:

$$\frac{w_e}{h} = \frac{w}{h} + \frac{\Delta w}{h} \tag{5.16}$$

where $\frac{\Delta w}{h} = \frac{1.25t'}{\pi h}\left[1 + \ln\frac{4\pi w}{t'}\right]$ for $\frac{w}{h} \leq \frac{1}{2\pi}$,

$= \frac{1.25t'}{\pi h}\left[1 + \ln\frac{2h}{t'}\right]$ for $\frac{w}{h} > \frac{1}{2\pi}$.

The novel double-layer metal interconnect cross-section we proposed for the BJT s-parameter test structure layout (see Fig. 5.1) is shown in Fig. 5.6. This interconnect has a 20 μm wide line in metal-2 separated from a metal-1 ground plane by 1 μm of insulating dielectric (SiO_2). This interconnect is integrated on the silicon substrate but the effects of the substrate are blocked by the metal-1 ground plane. This interconnect has a lower attenuation for the same physical geometry than the metal-SiO_2 interconnect since there are no substrate losses. The metal-insulator-metal transmission-line equations are reported in the literature [70]:

$$Z_0(f) = \frac{120\ \pi\ h}{w_{eff}(f)\ \epsilon_r(f)^{1/2}} \tag{5.17}$$

$$w_{eff}(f) = w_1 + \frac{w_{eff}(0) - w_1}{1 + f^2/f_T^2} \tag{5.18}$$

$$\epsilon_r(f) = \epsilon_r(0) - \frac{\epsilon_r(0) - \epsilon_{eff}}{1 + f^2/f_T^2} \tag{5.19}$$

Here, ϵ_{eff} is the effective permittivity of the insulator, $\epsilon_r(0)$ is the

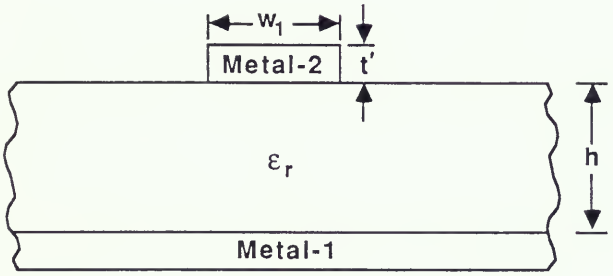

Figure 5.6 Cross-section of a metal-insulator-metal interconnect system, w_1 = 20 μm, t' = 1 μm, and ϵ_r = 4.

relative permittivity of the insulator at f = 0 (dc), ϵ_0 is the permittivity of free space, c is the speed of light, f is frequency, $w_{eff}(0)$ is the effective metal width at f = 0, h is the height of the dielectric, and w_1 is the width of the metal interconnect. The conductor losses are added to the model by using (5.14) and (5.15). The results of this modeling are shown in the next section.

5.3. Bipolar Test Structure S-parameter Response

The BJT test structure s-parameter response using the layout in Fig. 5.1 is predicted for BJT simulations. The BJT test structure response with microstrip interconnect (metal-SiO_2-Si substrate) and the double-layer metal interconnect (metal-SiO_2-metal) test structure response are both calculated. In order to investigate the relative contributions of the BJT test structure parasitic elements, simulations of: 1) the intrinsic BJT s-parameter response, 2) the s-parameter response of BJT transistor plus 200 μm of interconnect on each terminal, and 3) the response of the full BJT test structure are performed.

Figure 5.7 shows a pair of polar graphs of S_{11} and S_{21} simulated measurements for the BJT test structure with the metal-SiO_2-Si cross-section shown in Fig. 5.4. The curves labeled a and x display the BJT S_{11} and S_{21} response calculated from y-parameters. The curves labeled b, and c plot the S_{11} representation of 1) the BJT with 200 μm of interconnect on each terminal and 2) the BJT plus 200 μm of interconnect, bond pads, and an interconnect bend, respectively. the curves labeled y and z show the S_{21} response of the BJT test structure.

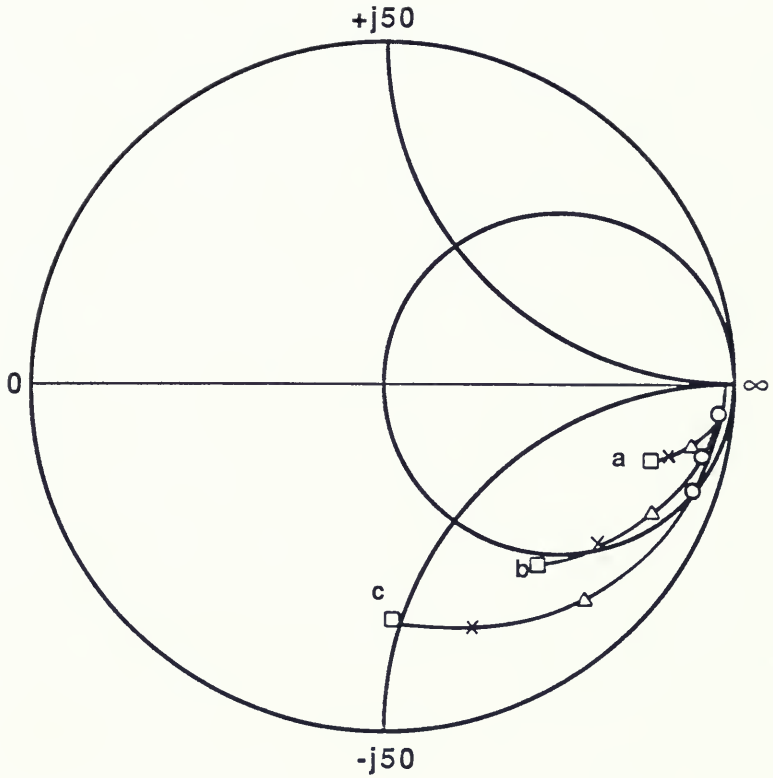

Figure 5.7.1 A polar graph of S_{11} for the metal-SiO_2-Si system shown in Fig. 5.4; curve a is a PISCES BJT simulation. Curves b and c show the BJT simulation plus the effects of 200 μm interconnect, and the BJT test structure layout (200 μm of interconnect bond pads and a bend), respectively.

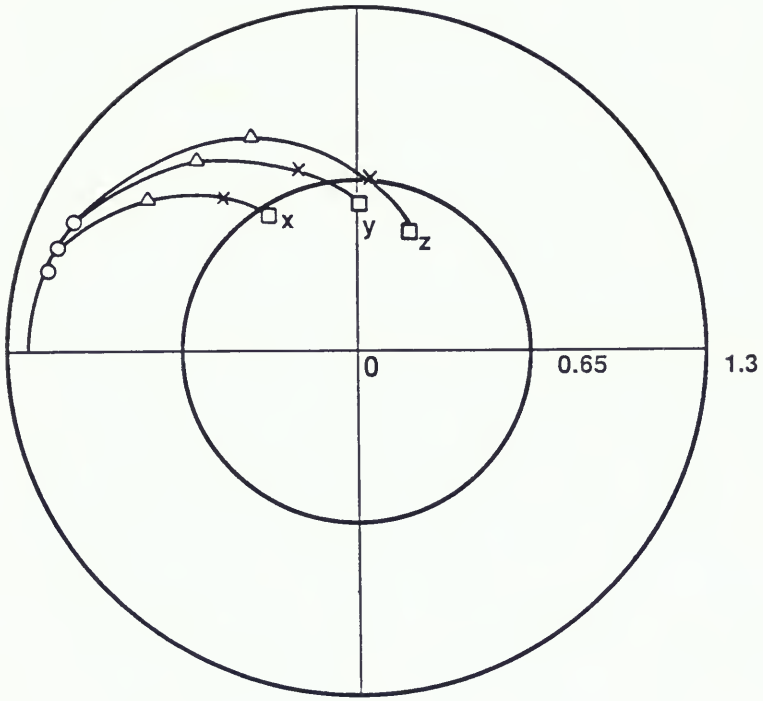

Figure 5.7.2 A polar graph of S_{21} for the metal-SiO_2-Si system shown in Figure 5.4. Curves x, y, and z correspond to curves a, b and c in Figure 5.7.1.

These s-parameter plots go from 10 MHz to 7 GHz and have markers at 1 GHz, 3 GHz, 5 GHz, and 7 GHz. The curves in Fig. 5.7 show that interconnect on the order of 200 μm significantly influences phase and gain of the s-parameter response simulation; bond pads and bend add additional parasitics effects to the s-parameter measurement.

Figure 5.8 displays the differences between the simulation of the BJT s-parameter response and the S_{21} magnitude (Fig. 5.8.1) and phase (Fig. 5.8.2) simulations of the BJT test structure. Figure 5.8.1 shows that the metal-SiO_2-Si BJT test structure has about 3 dB magnitude loss at 7 GHz and just 200 μm of interconnect will have 1 dB loss at 7 GHz. These losses will become large at frequencies above 10 GHz.

There are significant differences in phase between the BJT s-parameter response and the BJT test structure response at lower frequencies. A phase error of 10° is present for the BJT test structure at 1 GHz and just 200 μm of interconnect will add 10° phase error at 2 GHz. This phase error becomes larger than 58° for s-parameter measurements above 7 GHz for the BJT test structure.

Figure 5.9 displays a pair of polar graphs of S_{11} and S_{21} for the BJT test structure built on the novel metal-insulator-metal test structure. Again there are response differences between the BJT s-parameters of curve a, the BJT with 200 μm of interconnect (curve b), and the full BJT test structure (curve c). The s-parameter response curves for the metal-insulator-metal-based BJT test structure are closer on the polar graph than the response curves for the metal-SiO_2-Si interconnect-based BJT test structure (see Fig. 5.7). This indicates that the double-layer metal test structure has less parasitic effects.

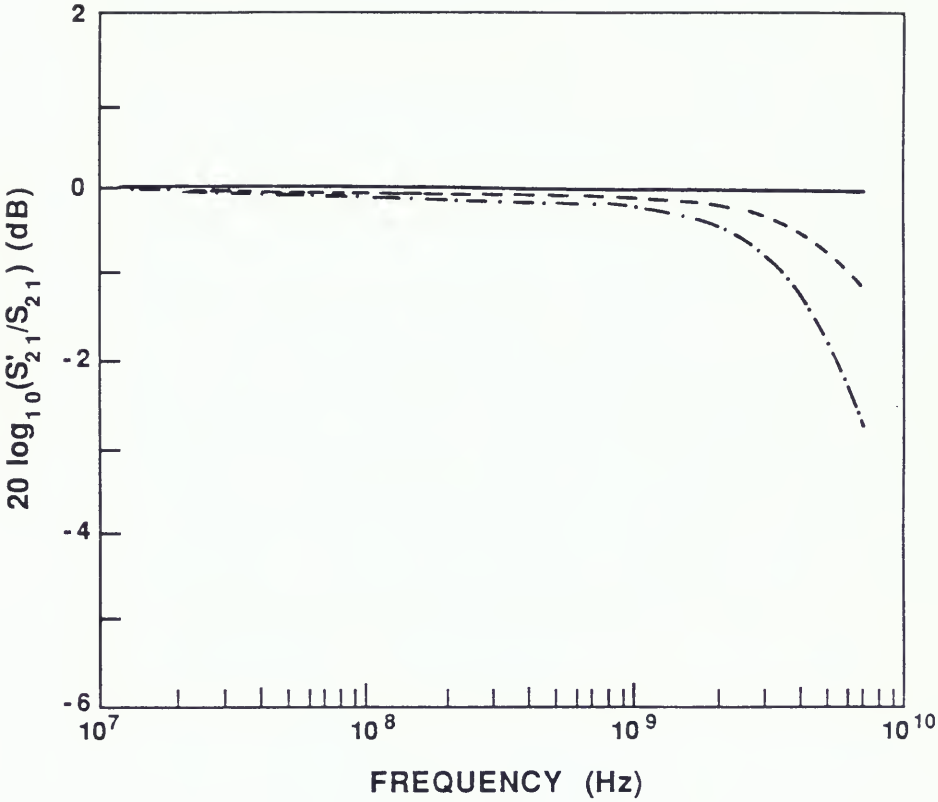

Figure 5.8.1 The relative magnitudes of the S_{21} responses shown in Figure 5.7.2. In this plot the solid line represents the PISCES BJT simulation, the dashed line represents the BJT plus 200 μm of interconnect, and the dashed and dotted line represents the BJT test structure response.

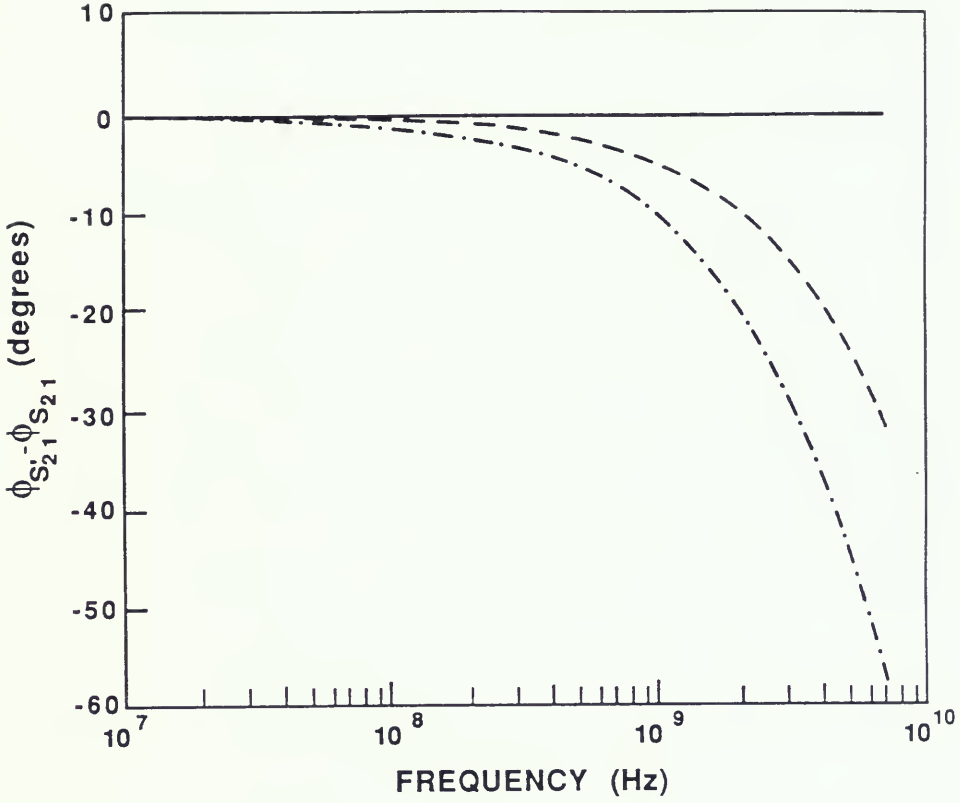

Figure 5.8.2 The difference in phase between the S_{21} shown in Figure 5.7.2. In this plot the solid line represents the PISCES BJT simulation, the dashed line represents the BJT plus 200 μm of interconnect, and the dashed and dotted line represents the BJT test structure response.

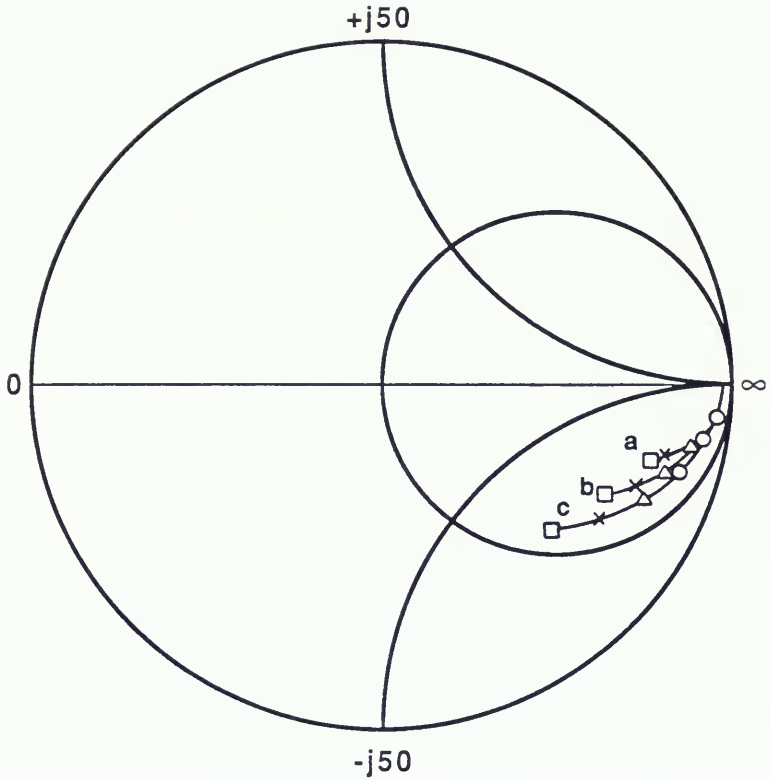

Figure 5.9.1 A polar graph of S_{11} for the metal-insulator-metal system shown in Figure 5.6; curve a is a PISCES BJT simulation. Curves b and c show the BJT simulation plus the effects of 200 μm interconnect, and the BJT test structure layout (200 μm of interconnect, bond pads and a bend), respectively.

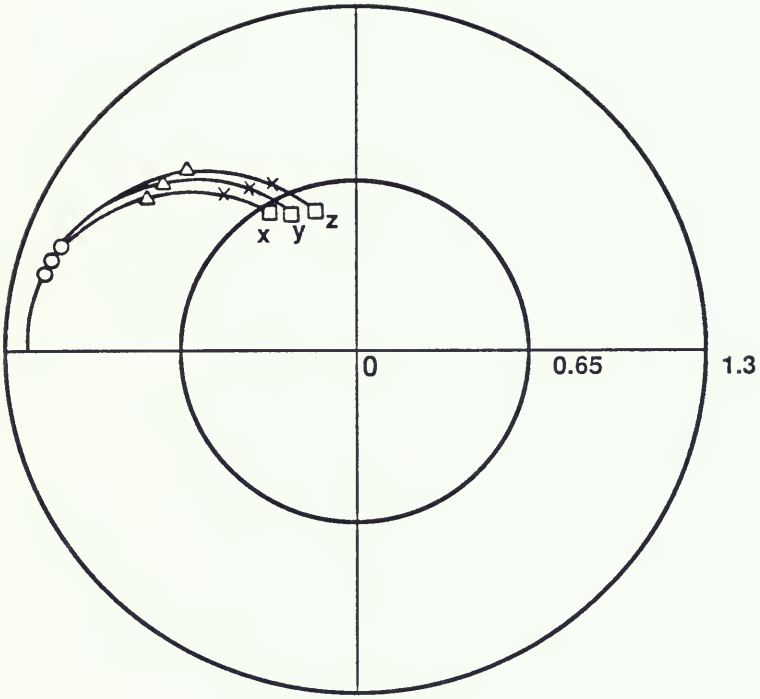

Figure 5.9.2 A polar graph of S_{21} for the metal-insulator metal system shown in Figure 5.6. Curves x, y and z correspond to curves a, b and c in Figure 5.9.1.

Figure 5.10 displays the differences in S_{21} magnitude (Fig. 5.10.1) and S_{21} phase (Fig. 5.10.2) between the BJT s-parameter response, the BJT test structure s-parameter response, and the s-parameter response of the BJT with 200 μm of metal-insulator-metal interconnect. Here, there is a 1.6 dB loss in S_{21} magnitude for the BJT test structure at 7 GHz, indicating a much improved measurement environment. This interconnect system also exhibits better phase agreement with the PISCES simulated s-parameter response than the metal-SiO_2-Si-based BJT test structure as shown by an 18° reduction in phase error at 7 GHz.

5.4 Conclusions

In general, the simulations produced by a 2-D device simulator do not incorporate test structure layout topology effects into account. We have demonstrated modeling techniques necessary to predict s-parameter response from 2-D simulations for a given BJT test structure layout. Thus, s-parameter simulations give insights into changes in BJT behavior with variations in doping profiles, and physical dimensions can be compared directly to measurements. This modeling technique also can be used to produce 3-port s-parameter characterizations and supplement existing 2-port device BJT s-parameter measurements. Moreover, the modeling can be applied to high frequency test structure modeling for transistor other than the BJT, such as GaAs heterojunction bipolar transistors.

The simulations presented in the paper [71] show that significant high frequency parasitics are present in a typical BJT test structure,

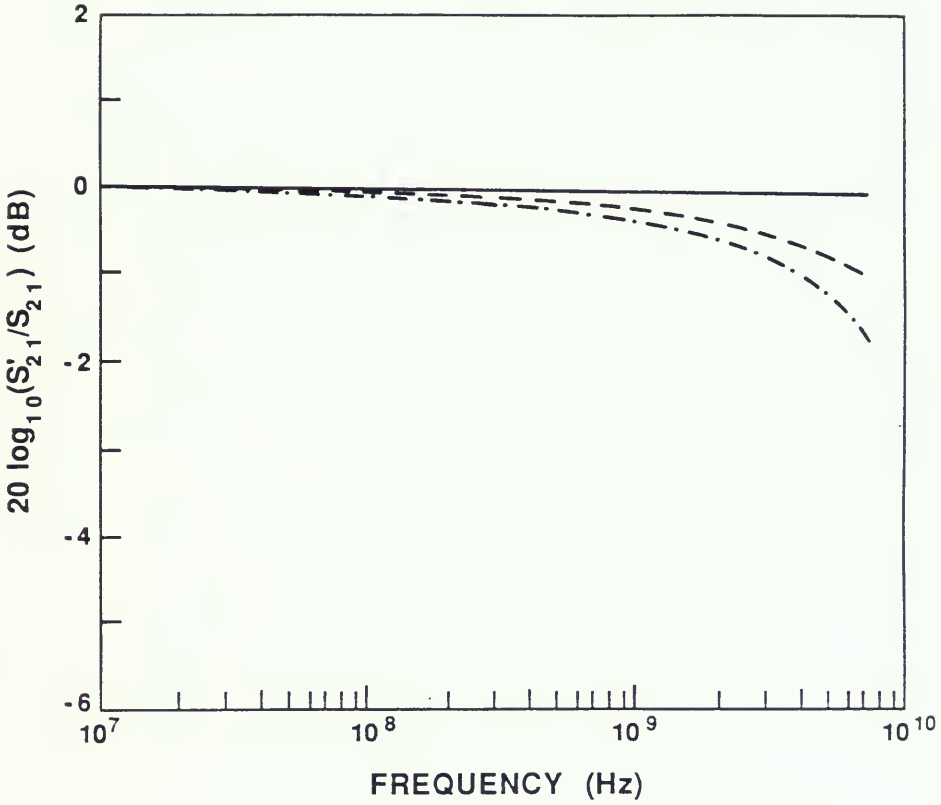

Figure 5.10.1 The relative magnitude of the S_{21} responses shown in Figure 5.9.2. In this plot the solid line represents the PISCES BJT simulation, the dashed line represents the BJT plus 200 μm of interconnect, and the dashed and dotted line represents the BJT test structure response.

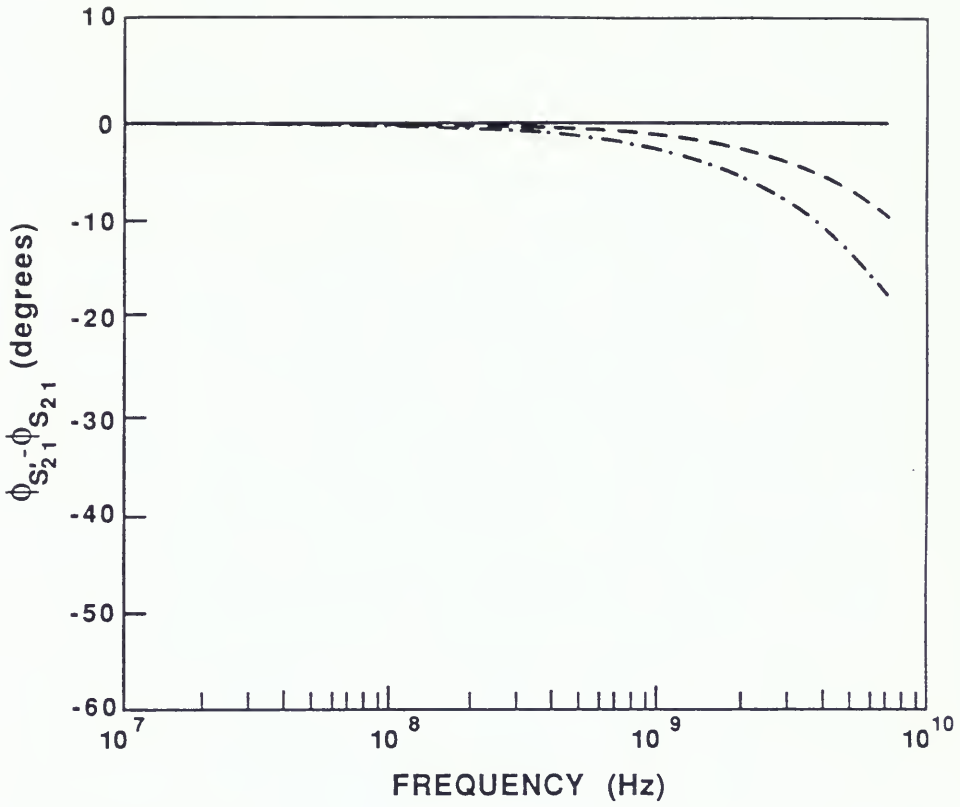

Figure 5.10.2 The difference in phase between the S_{21} shown in Figure 5.9.2. In this plot the solid line represents the PISCES BJT simulation, the dashed line represents the BJT plus 200 μm of interconnect, and the dashed and dotted line represents the BJT test structure response.

especially above 1 GHz. for example, the addition of 200 μm of interconnect on each terminal and bond pads will introduce a S_{21} magnitude error of 3.0 dB and S_{21} phase error of 58° at 7 GHz on a metal-SiO_2-Si interconnect system. The simulations also show that a metal-insulator-metal system with the same interconnect dimensions will be superior to the metal-SiO_2-Si system for BJT test structure layout across the frequency range of simulation.

CHAPTER SIX
INTEGRATED CIRCUITS INTERCONNECT MODEL FOR SPICE

6.1 Introduction

With the design of fast devices having switching times in the picosecond range, transmitting data at high speed rate has becomes very commonplace in digital integrated circuit systems. Signal delays and rise times are more and more limited by interconnection lengths rather than intrinsic device speed in submicrometer VLSI technology [72]. Accurate modeling and analysis of the interconnect structure is thus essential to the realization of the next generation of high performance IC's.

Careful modeling of IC interconnect and associated parasitics is required to push the performance of both digital and analog advanced bipolar circuits into the GHz frequency range. SPICE transmission line modeling (lossless and nondispersive) very poorly describes the behavior of signals on IC interconnect of advanced IC technologies (lossy and dispersive).

Existing interconnect circuit models for the silicon integrated circuit describe the transmission properties of a metal interconnect line on a dielectric substrate or on a SiO_2 layer of constant thickness over a substrate with constant doping. A model for this case is presented in Chapter 5. However, this existing interconnect circuit modeling neglects the effects of buried layers, epi-layers, and p-n junction space-charge capacitance that may occur in modern integrated

circuit technologies [73].

A method of modeling first-level metal interconnect signal transmission on silicon substrate with arbitrary doping profiles is presented in this chapter. Analytical modeling and the output of a 2-D device simulator are used to predict and verify the small-signal admittance per unit length of silicon IC interconnect. Then accurate analytical models of interconnect signal transmission are derived by combining the admittance information and existing modeling of interconnect series impedance per unit length. The model prediction in SPICE simulation is verified by experiments. An ECL ring oscillator transient analysis is used to study the practical utility of the interconnect circuit model. Finally, a conclusion section ends the chapter.

6.2 Interconnect Modeling Topology Development

An interconnect system tends to require complex modeling because the conductor material is not lossless and the lines can be coupled both capacitively and inductively. The finite conductivity of the conductor results in a variation of the current density distribution in the conductor. Skin effect loss (conductor loss) and dielectric loss as well as different signal phase velocities at high frequency make the interconnect resistance and capacitance frequency dependent. Thus, linear distributed interconnect models which are commonly used in CAD packages (such as SPICE and Touchstone) do not readily represent the interconnect dispersive and lossy characteristics. In this section, a nonlinear interconnect circuit modeling technique will be developed

that takes into account signal dispersion and signal loss.

First, a simplified interconnection line and its equivalent circuit model per unit length of the structure for frequency-dependency analysis are shown in Fig. 6.1. In Fig. 6.1.2, R represents the interconnection line series resistance, L is the interconnect line inductance resulting from the propagating electromagnetic field, G is the substrate shunt conductance, and C is the substrate capacitance. The circuit elements above are written in terms of the metal width w, thickness t', and substrate height h as follows [63] [66]:

$$R(f) = \left(\frac{\pi \mu_0 f}{\sigma_{METAL}\, w\, t'}\right)^{1/2} \tag{6.1}$$

$$L = \mu_0 F(w,h) \tag{6.2}$$

$$G = \frac{\sigma_{sub}\,[1+(1+10h/w)^{-1/2}]}{F(w,h)} \tag{6.3}$$

$$C(f) = \frac{\epsilon_0\, \epsilon_{eff}(f)}{F(w,h)} \tag{6.4}$$

$$F(w,h) = \frac{1}{2\pi} \ln\left[\frac{8h}{w} + \frac{w}{4h}\right], \qquad \text{for } h/w > 1$$

$$= \frac{1}{w/h + 2.42 - 0.44h/w + (1-h/w)^6}, \qquad \text{for } h/w < 1 \tag{6.5}$$

where σ_{sub} is the dielectric substrate conductivity.

The nonlinear characteristics of the circuit elements above is implicitly accounted for in the frequency-dependent permittivity,

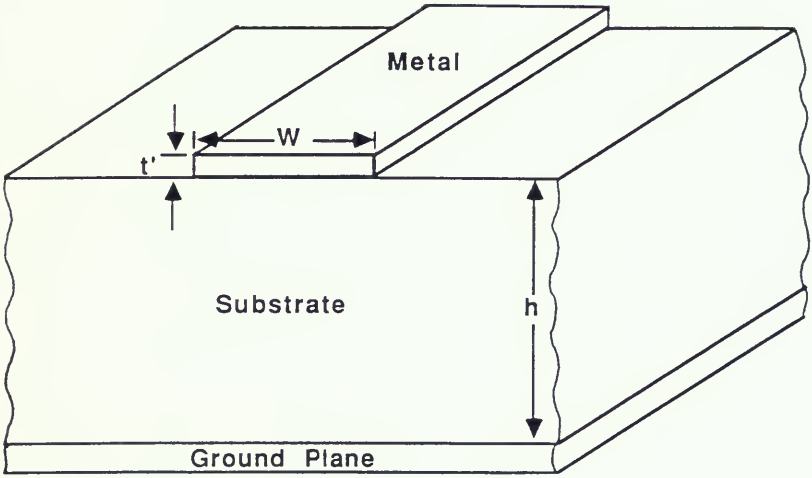

Figure 6.1.1 A metal-Si-metal interconnect line.

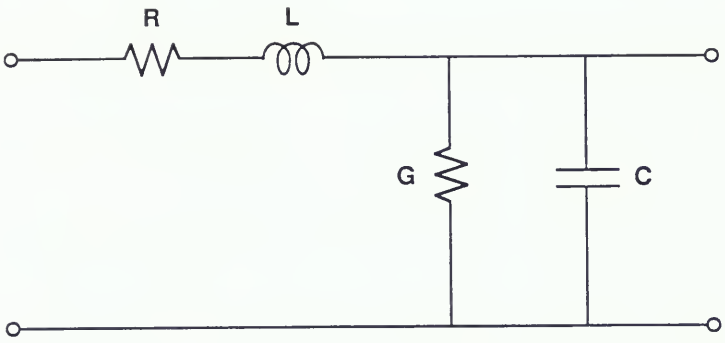

Figure 6.1.2 The equivalent circuit model per unit length of the interconnect shown in Figure 6.1.1.

$e_{eff}(f)$. The effective permittivity starts to increase to its maximum value ($\epsilon_{eff} \rightarrow \epsilon$) when the frequency is above the critical frequency, f_C [70].

$$\epsilon_{eff}(f) = \epsilon - \frac{\epsilon - \epsilon'}{1 + (f^2/f_C^2)} \tag{6.6}$$

$$\epsilon' = \frac{\epsilon+1}{2} + \frac{\epsilon-1}{2(1+10h/w)^{1/2}} \tag{6.7}$$

$$f_C = \frac{c^2 \epsilon_0 Z_0 \epsilon^{1/2}}{2 h \epsilon'^{1/2}} \tag{6.8}$$

$$Z_0 = \frac{120 \pi F(w,h)}{\epsilon'^{1/2}}. \tag{6.9}$$

Using Eqs. (6.1)-(6.9), the frequency-dependent propagation coefficient γ is given as

$$\gamma(f) = [Z(f) Y(f)]^{1/2} \tag{6.10}$$

where $Z(f) = R(f) + j\omega L(f)$, and $Y(f) = G(f) + j\omega C(f)$.

Time-domain simulations of pulse propagation can be performed using this interconnect model [74]. A Gaussian pulse is divided into frequency-domain components via the Fourier transform and these components are propagated along the IC interconnect using the wave equation. The frequency-domain components experience different wavespeeds and loss as they propagate. Applying the inverse Fourier transform to the input signal and the frequency-dependent propagation coefficient in Eq. (6.10), the pulse shape at any particular point on

the interconnect can be calculated [75-77]:

$$V(1,t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} V(0,x)\, e^{j\omega t}\, e^{-\gamma 1}\, dx \qquad (6.11)$$

where 1 is the interconnection length, ω is the radian frequency ($\omega = 2\pi f$), and t is time. A flow chart of this topology is shown in Fig. 6.2.

To demonstrate the necessity of the frequency-dependent components and the modeling utility, a Gaussian pulse propagating along an interconnect is simulated. In this simulation, 1 = 0.9 cm, t' = 0.0005 cm, w = 0.051 cm, h = 0.064 cm, ϵ = 10.2, $\sigma_{METAL} = 3.7 \times 10^5$, $\sigma_{sub} = 1 \times 10^{-2}$. The dashed line in Fig. 6.3 is the propagating pulse computed from the interconnect model without frequency-dependent permittivity ($\epsilon_{eff} = \epsilon'$) while the solid line is from the interconnect model with frequency-dependent $\epsilon_{eff}(f)$. In the semiconducting substrate, wave propagation is dispersive due to slow-wave propagation and mode transition [78]. Owing to this, propagation delay and rise time of high speed pulses are deteriorated in the semiconducting substrate. Therefore, the frequency-dependent permittivity used in nonlinear circuit elements formulation is necessary to represent signal dispersion. To verify the interconnect model, we compare the model simulations with the published data [76]. The circles in Fig. 6.3 [76] show excellent agreement with the model prediction (solid line); however, the frequency-independent circuit elements response has a large discrepancy (dashed line) with the dispersive signal. Therefore, the equivalent circuit modeling topology here is more accurate than the

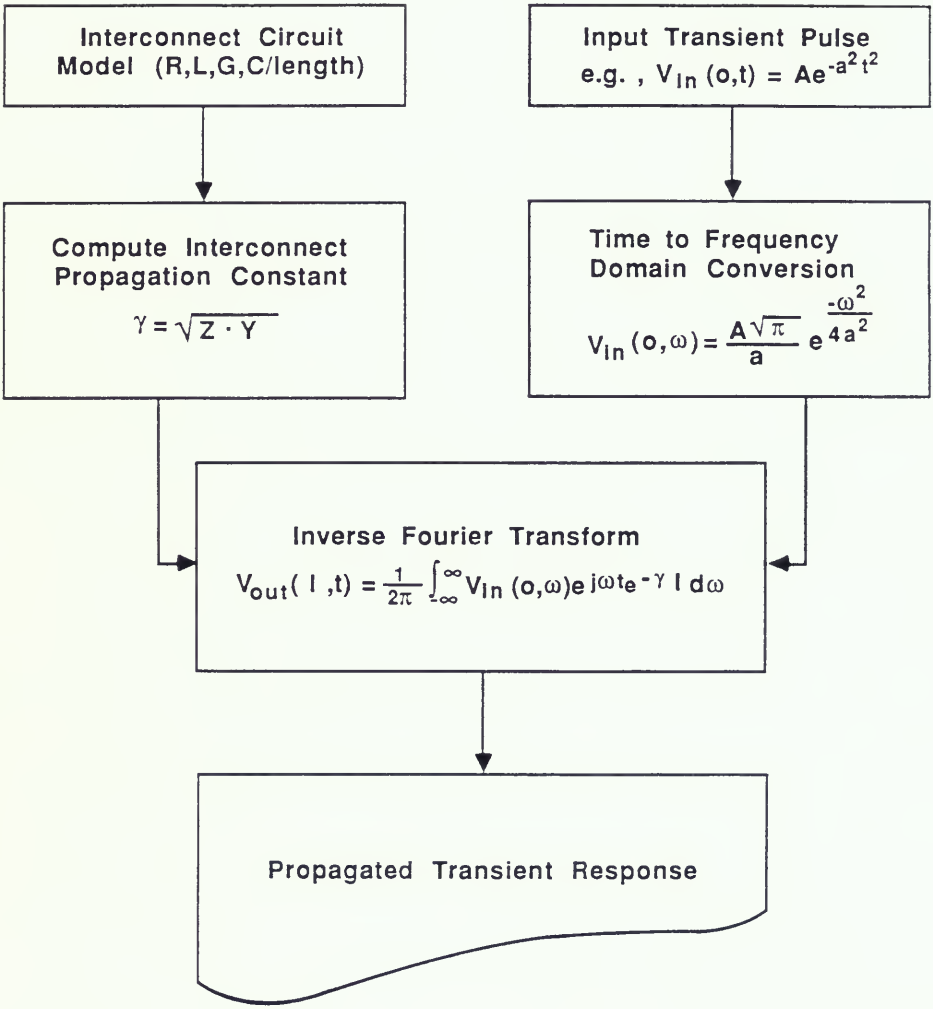

Figure 6.2 Calculation of pulse propagation using Fourier transforms and inverse Fourier transforms.

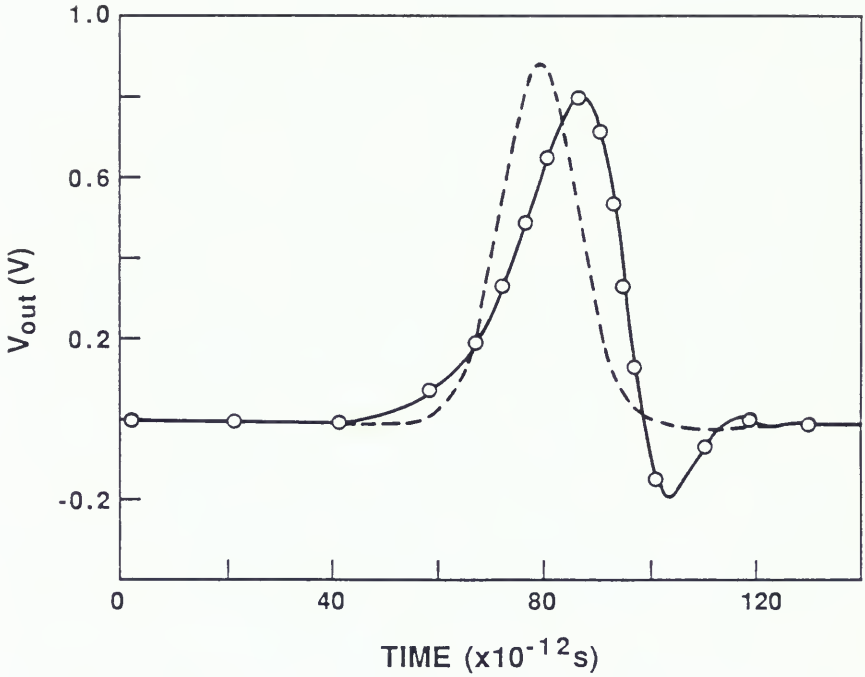

Figure 6.3 Plot of signal propagation on interconnect line. In this figure the solid line represents the model simulation with frequency-dependent circuit elements, the dashed line represents the model simulation with frequency-independent circuit elements, and the circles represent the published data in [76].

linear circuit elements model in [65] [66]. Note that even though the mathematical modeling technique in [76] is adequate for finding signal transmission for a single circuit element, equivalent circuit modeling is more suitable for SPICE circuit simulation.

6.3 Advanced IC Interconnect Cross-Section Analysis

The interconnect circuit model in Section 6.2 is extended for advanced IC technologies. First, the IC interconnect cross-section is partitioned into the relevant doping regions (oxide, epi-layer, buried-layer, substrate, etc.). Analytical expressions provide the conductance and capacitance of each region. Parallel admittance per unit length of the interconnect cross-section (Y) is modeled by stacking the circuit elements (G's and C's per unit length) into a series of admittances representing each of the doping regions. Space charge capacitances are placed between p region and n region. The 2-D device simulator is used to verified the validity of the overall analytical expressions for a particular IC interconnect cross-section.

Figure 6.4 shows a segment of the representative distributed circuit model (Fig. 6.4.2) for signal propagation on the interconnect integrated on an SiO_2 substrate over an n-type buried layer on a p-type substrate (Fig. 6.4.1). The parallel admittance elements of the interconnect circuit are the field oxide capacitance (C_{SiO2}), the buried layer conductance (G_{n+}), the buried layer capacitance (C_{n+}), the junction space-charge region capacitance (C_{SCR}), the substrate conductance (G_{sub}), and the substrate capacitance (C_{sub}). Extensions of existing analytical modeling are used to calculate the values of these

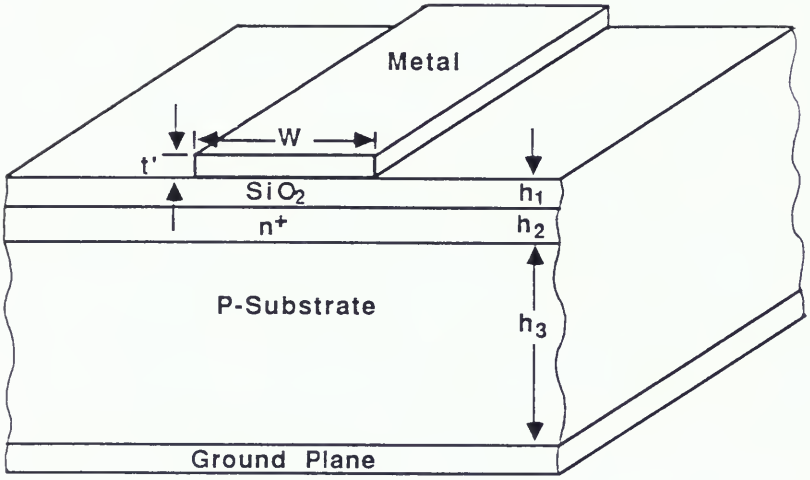

Figure 6.4.1 An interconnect line for advanced bipolar IC cross-section profile. The interconnect is integrated on an SiO_2 substrate over an n-type buried layer on a p-type substrate.

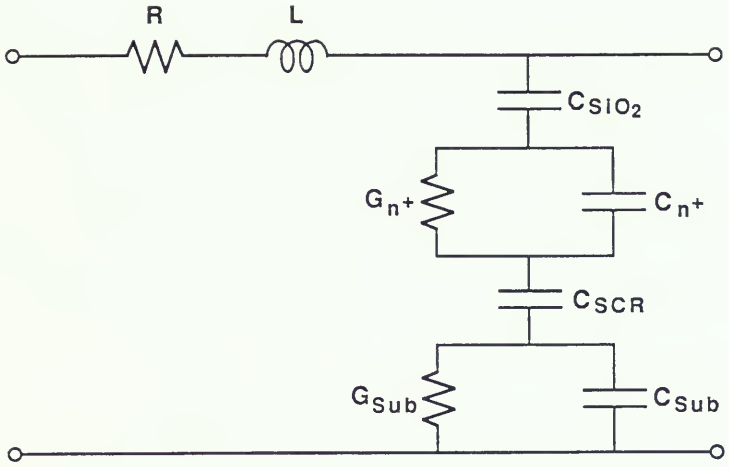

Figure 6.4.2 The equivalent circuit model per unit length of the interconnect shown in Figure 6.4.1.

parallel admittances as below:

$$C_{SiO2} = \frac{\epsilon_0 \, \epsilon_{eff}(f)}{F(w,t_1)} \tag{6.12}$$

$$G_{n^+} = \frac{\sigma_{n^+} \, [1+(1+10t_2/w)^{-1/2}]}{2F(w,t_2)} \tag{6.13}$$

$$C_{n^+} = \frac{\epsilon_0 \, \epsilon_{eff}(f)}{F(w,t_2)} \tag{6.14}$$

$$C_{SCR} = \frac{\epsilon_0 \, \epsilon_{eff}(f) \, w}{[2\epsilon_0 \epsilon_{eff}(f)(N_A+N_D)(V_{bi}-2V_T)/(qN_AN_D)]^{1/2}} \tag{6.15}$$

$$G_{sub} = \frac{\sigma_{sub} \, [1+(1+10t_3/w)^{-1/2}]}{2F(w,t_3)} \tag{6.16}$$

$$C_{sub} = \frac{\epsilon_0 \, \epsilon_{eff}(f)}{F(w,t_3)} \tag{6.17}$$

where N_A is the acceptor doping concentration for p-type Si substrate, N_D is the donor doping concentration for n^+-type Si layer, σ_{n^+} is the n^+ silicon conductivity. The variables t_1, t_2, and t_3 are the oxide height, the Si buried layer height, and the silicon substrate height, respectively.

Among the capacitances of C_{SiO2}, C_{n^+}, C_{SCR}, and C_{sub}, the substrate capacitance C_{sub} shows the strongest frequency-dependent behavior due to a large thickness and the small critical frequency f_C (see Eqs. (6.6) - (6.9)).

The series impedance elements (R and L) are determined by (6.1) and (6.2) providing h in (6.2) is replaced by $t_1 + t_2 + t_3$.

To verify the new cross-section modeling, the transient response of this IC interconnect cross-section admittance is simulated using PISCES-II. A pulse is applied to the cross-section with a 100 ps risetime ramp. The SPICE circuit simulation program simulated the interconnect circuit model transient response (parallel admittance elements only) to an identical pulse. These results are plotted in Fig. 6.5. The agreement between the PISCES cross-section transient simulation and SPICE interconnect circuit model transient simulation is excellent. This indicates that the circuit modeling of the interconnect parallel admittance is correct.

6.4 Interconnect Model Verification

The interconnect cross-section model in Sec. 6.3 plus the impedance model (R and L) in Sec. 6.2 give an advanced IC interconnect model. To verify the model accuracy, test structures representative of the interconnect lines are fabricated in Texas Instruments Inc. The interconnect dimensions and profiles where established from the fabrication process. Transient measurements were performed using the Tektronix 7854 sampling oscilloscope and 7S12 time domain reflectometry (TDR) sampler. TDR 7S12 generates fast transient pulse with amplitude 250 mV and rise time less than 35 ps. The fast switching-on transient enables characterization of signal dispersion. A measured transient response with signal delay, loss, and dispersion is displayed in Fig. 6.6.

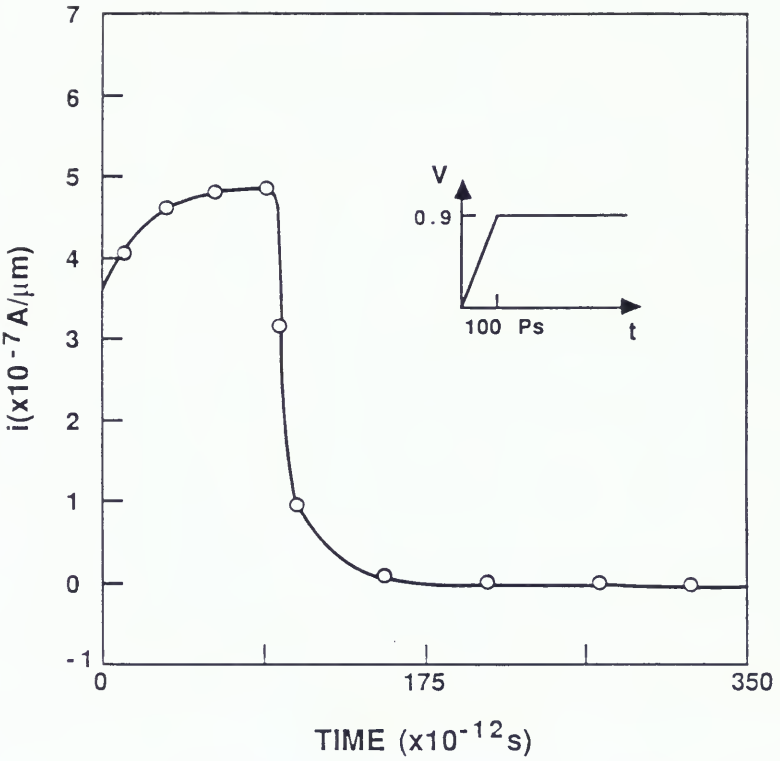

Figure 6.5 Comparison of interconnect model admittance simulation on SPICE (solid line) and admittance simulation of IC cross-section on PISCES (circles).

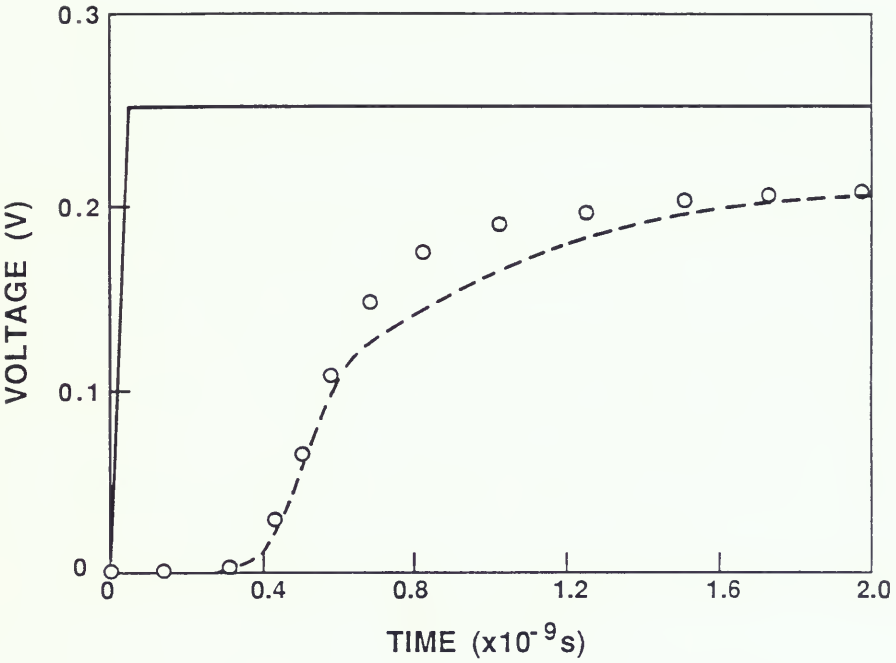

Figure 6.6 Step response of a 5 cm interconnect line. The solid line represents the step input, the dashed line represents the model simulation, and the circles represent measurement data.

To demonstrate interconnect model utility in SPICE circuit simulation, the interconnect circuit model is constructed as an n-sectional miniaturize network representing a distributed circuit. SPICE simulation employing the present nonlinear interconnect model is simulated by a input pulse with 35 ps ramp from 0 to 250 mV followed by a flat pulse. In the SPICE simulation, the equivalent circuit elements are determined to have a bandwidth defined by $f_{cutoff} \simeq 1/(2\pi\tau_{rise})$. Frequency variations in circuit elements can not be computed in transient simulation in SPICE [79]. However, by examining the characteristics of the frequency-dependent dielectric constant (see Fig. 6.7), the author determined that the capacitance's frequency-dependency behavior can be neglected if the signal frequency is below 30 Ghz. Therefore, for a 35 ps risetime ramp the frequency-independent circuit elements in SPICE simulation will be fairly accurate. Nevertheless, the use of $f \simeq 1/(2\pi\tau_{rise})$ for computing circuit elements is much better than the use of $f = \infty$. The simulated transient waveform is compared with the experimental result in Fig. 6.6. Good agreement is obtained between measurement and model prediction. This confirms the present interconnect circuit model utility and accuracy.

6.5 Mixed-Mode Circuit Simulation

The steady increases in chip complexity brought about by continuing improvements in lithographic resolution have created the economic incentive to implement subsystems containing both analog and digital functions on a single integrated circuit. In circuit design, mixed-mode circuits mean the combination of analog and digital circuits

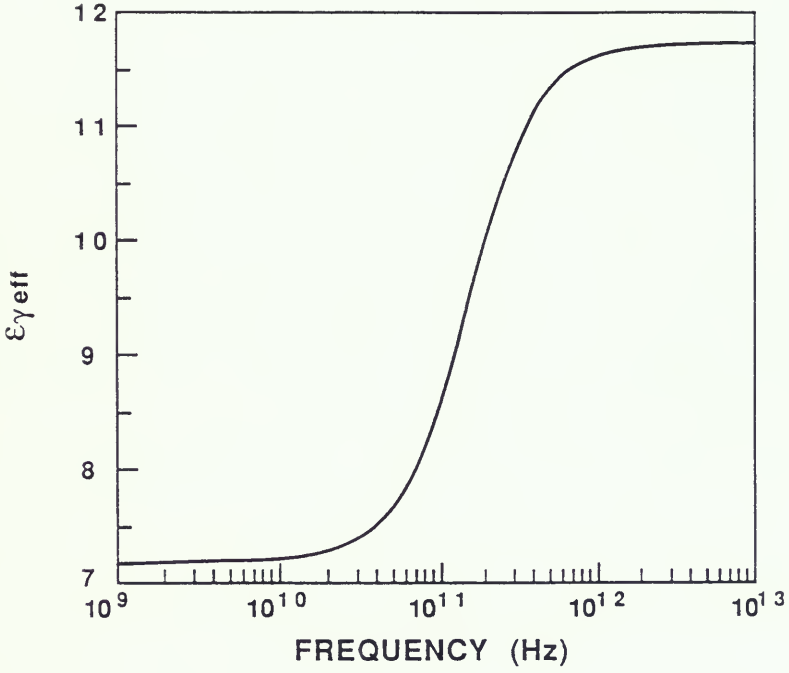

Figure 6.7 Plot of the permittivity versus frequency.

integrated in a single chip. In circuit simulation, however, mixed-mode simulation combines the level of device simulation and circuit simulation in circuit analysis, such as MEDUSA [80]. The "mixed-mode" circuit simulation described here includes bipolar transistors and interconnects. Since the bipolar circuit models in this work are derived from the physical insights of device simulations, the physical model contains a lot of information of device layout (emitter width, emitter length, emitter perimeter, etc.), device doping (base doping and epitaxial collector doping), and physical device parameters (lateral diffusion velocities) in circuit simulation. Therefore, the circuit simulator inputs have not only circuit parameters from measurements, but also physical parameters in device make up. In addition, the parasitics such as interconnects which are also process cross-section dependent are included in our circuit simulation. We then call it mixed-mode circuit simulation.

To demonstrate the interconnect model utility and necessity in mixed-mode circuit simulation, a ring oscillator with an interconnect feedback path between its last and first stages (see Fig. 6.8) is simulated in transient operation. The ring oscillator has a NOR gate as a stimulus input source and an inverter followed by four ECL inverters. The ECL circuits in Fig. 6.9 have R_{C1} = 500 Ω, R_{C2} = 500 Ω, R_e = 640 Ω, V_e = -4.0 V, V_{CS} = -2.5 V, and V_{REF} = -1.11 V. The input source used to trigger the NOR gate has a logic swing from -0.86 V to -1.36 V with 70 ps ramp and then stays at -1.36 V.

The transient simulation of the ring oscillator with 0.5 mm interconnect (the equivalent interconnect circuit is in Fig. 6.1) is

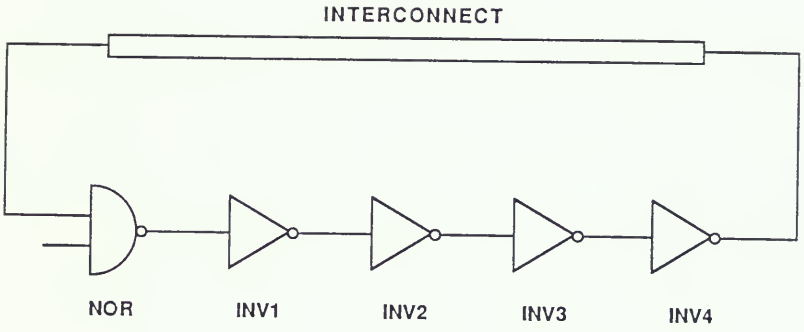

Figure 6.8 A five-stage ring oscillator with an interconnect feedback path between its last and first stages.

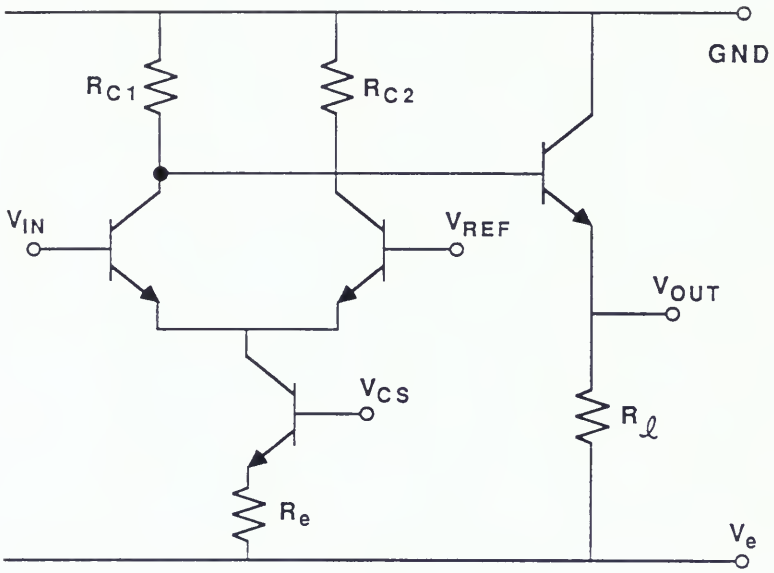

Figure 6.9 An ECL inverter circuit configuration.

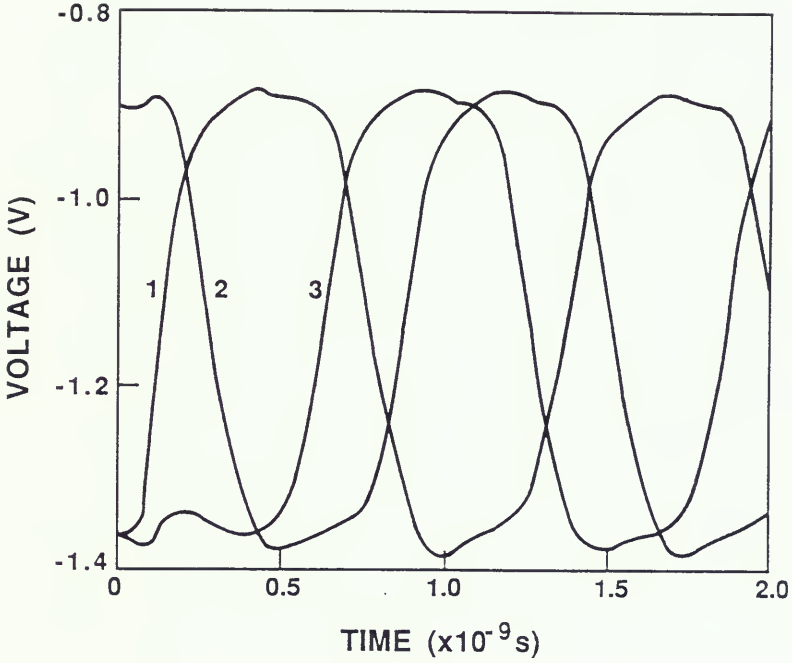

Figure 6.10 Transient response of a five-stage ring oscillator. In this figure, curve 1 is the output of INV 1, curve 2 is the output of INV 2, and curve 3 is the input of NOR gate.

shown in Fig. 6.10. In Fig. 6.10 curves 1, 2, and 3 represent the transient responses probed from the output of INV 1, INV 2, and the input of NOR, respectively. Curve 2 is the inverse of curve 1 providing a small finite time delay and curve 3 has the same polarity with curve 1 providing a larger finite delay due to delays in INV3, INV4, and interconnect. To demonstrate the model utility, the transient simulation of the same oscillator without interconnect has been performed in Fig. 6.11. In Fig. 6.11 curves 1, 2, and 3 correspond to curves with the same numbers as those in Fig. 6.10. In general, the transient response in Fig. 6.11 is faster in Fig. 6.10. For a better comparison, the inputs of the NOR gate, which are the output of the interconnect (solid line) and the output of the INV 4 without interconnect (dashed line), are plotted in Fig. 6.12. It is clear that the oscillator with interconnect has a wider delay time between 50% turn-on and 50% turn-off (≈700 ps) in logic ringing compared with the oscillator without interconnect (≈650 ps). The difference is due to the interconnect delay and the loading effects for INV 4. The interconnect contributes capacitance, resistance, and inductance effects which degrade the transient response of the ring oscillator. Thus, for a polysilicon interconnect, the difference in the delay time will be significantly enhanced due to a big polysilicon line resistance.

In order to further probe the origin of the difference, the input and output from the "input transistor" (V_{IN} connects BJT's base in Fig. 6.9) and the "level shifting transistor" (V_{OUT} connects BJT's emitter in Fig. 6.9) of INV 4 have been shown in Fig. 6.13. It is interesting to note in Fig. 6.13 that the delay of the ECL gate comes mainly from

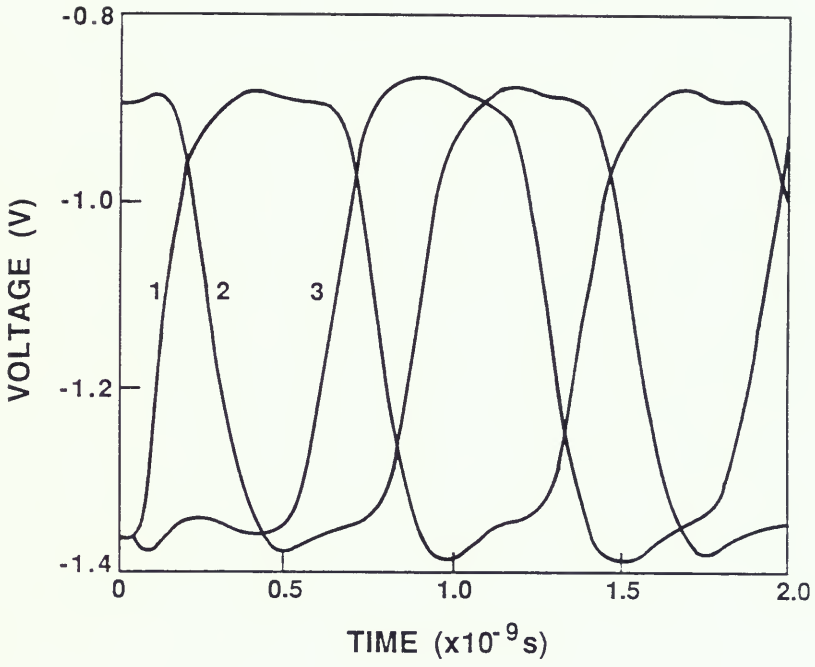

Figure 6.11 Transient response of a five-stage ring oscillator with an interconnect feed path between its first and last stages. In this figure, curve 1 is the output of INV 1, curve 2 is the output of INV 2, and curve 3 is the input of NOR gate.

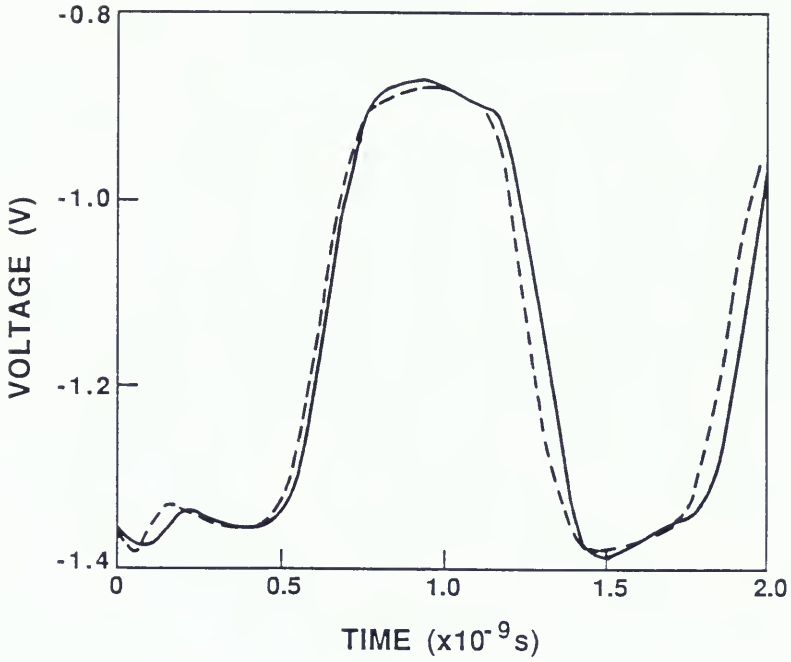

Figure 6.12 Comparison of ring oscillator transient responses at the input of NOR gate. The solid line represents the five-stage ring oscillator with a feed path interconnect and the dashed line represents the five-stage ring oscillator without an interconnect.

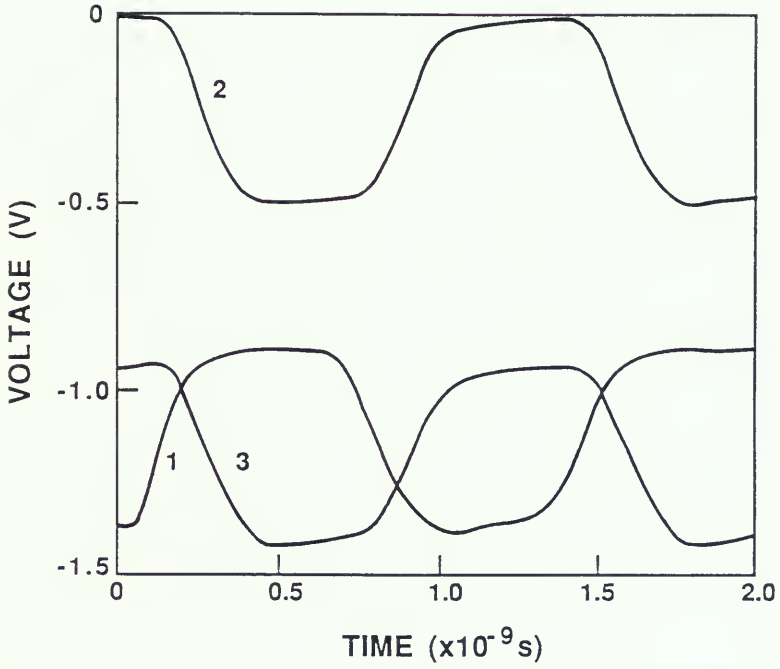

Figure 6.13 Internal transient response of INV 4. In this figure, curve 1 is the input pulse of INV 4, curve 2 is the output signal at the cllector side of the input transistor in INV 4, and the curve 3 is the output signal of the level shifting transistor in INV 4.

the input stage transistor (see curves 2 and 1 in Fig. 6.13). The level shifting transistor does not contributes much switching delay (see curves 3 and 2). The loading effects for the level shifting transistor in inverter 4 degrade the transient response (delay time between 50% turn-on and 50% turn-off in curve 3). Since this 50% turn-on and 50% turn-off delay divided by the number of gates in the ring oscillator is used for evaluating the gate propagation delay (τ_d) in measurement, τ_d will be underestimated if the effects of interconnect are not considered.

6.6 Summary and Discussion

A flexible technique for developing IC interconnect circuit models and verifying their properties through simulation is presented. The effects of dispersion and attenuation on pulse propagation on the IC interconnect of an advanced bipolar technology is demonstrated. The interconnect model is easily implemented on SPICE circuit simulation using an approximation of a distributed subcircuit. The agreement between model prediction and measurement is excellent. This interconnect modeling is of importance for mixed-mode circuit simulation environment of cascaded logic gates connected by long sections of interconnection. For VLSI signal crosstalk between adjacent lines may be significant to distort the circuit response, a subject of the next chapter.

CHAPTER SEVEN
MODELING FOR COUPLED INTERCONNECTION LINES

7.1. Introduction

As the speed of logic device increase, designers are confronted with limitations imposed by the packing and interconnect systems which could potentially degrade the electrical performance of the system [81]. Thus, in a high-speed digital integrated circuit, it is important to know the effects of signal coupling between different parallel interconnection lines.

Coupled transmission lines have received extensive amounts of modeling in the literature [82-92]. Based on the solution of the coupled transmission line equations, accurate models have been derived primarily for the coupled pairs of symmetric lines. These models provide an analysis of the pulse propagation characteristics of the interconnections in digital as well as microwave circuits.

In this chapter, a comprehensive study of coupled interconnect lines will be given. Even mode and odd mode capacitances which determine the phase delay and the coupling between two lines are discussed in Section 7.2. Signal losses, dispersion and crosstalk are presented in Section 7.3. In Section 7.4 the mode transition for a very fast signal propagation in picosecond photoconductor measurements is shown. An equivalent circuit model for coupled transmission lines in SPICE is demonstrated in Section 7.5. The model can be easily incorporated in the form of subcircuits making the coupled line 2n-port

a standard circuit element for computer-aided circuit design and analysis. The simulated results and discussions are presented in Section 7.6. Conclusions are given in Section 7.7.

7.2. Even Mode and Odd Mode Analysis for Two Parallel Lines

In order to properly analyze a periodic array of interconnect lines which have distributed characteristics, the interconnect system can be viewed as a coupled microstrip structure (Fig. 7.1). This structure consists of two adjacent lines which can support two different modes of propagation with different characteristic impedances and phase velocities.

If the lines are symmetric, the propagation can be divided into even and odd modes corresponding to an even and odd symmetry about a plane which can be replaced by a magnetic or electric wall for the purpose of analysis. In Figs. 7.2 and 7.3 the solid line arrows represent the electric field lines, and the dashed line arrows represent the magnetic field lines. From the distribution of the fields in different modes, the capacitances in even and odd modes can be determined. The even mode capacitance, C_e is simply the summation of the plate capacitance, C_p, the fringing capacitance, C_f, and a modified fringing capacitance, C_f' due to the influence of the magnetic wall [63] [93] [94]:

$$C_e = C_p + C_f + C_f' \tag{7.1}$$

$$C_p = \epsilon_0 \, \epsilon_{r2} \, \frac{w}{h} \tag{7.2}$$

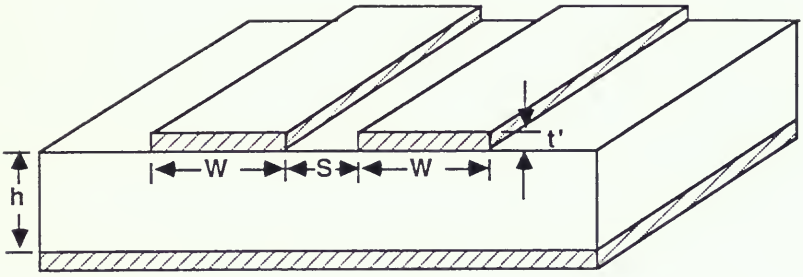

Figure 7.1 A coupled microstrip lines configuration. These interconnect lines have the same width and thickness.

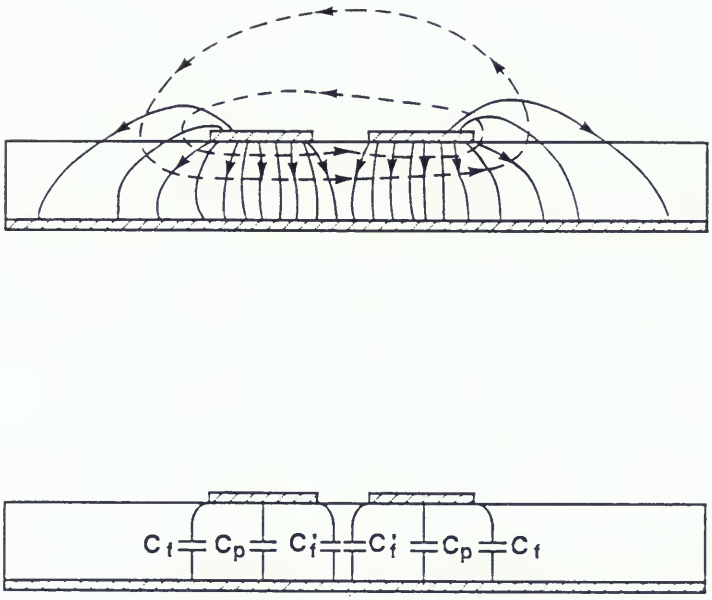

Figure 7.2 A coupled transmission lines cross-section and break-up of capacitances for even mode. The solid line arrows are electrical field lines and the dashed line arrows are magnetic field lines.

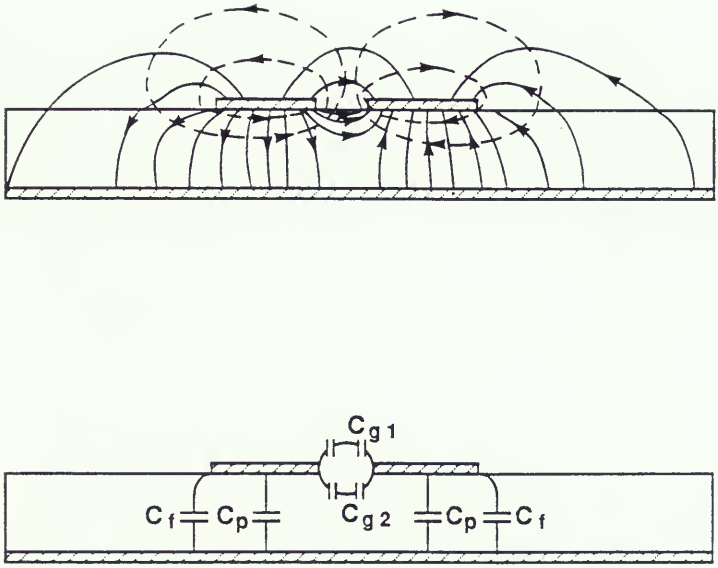

Figure 7.3 A coupled transmission lines cross-section and break-up of capacitances for odd mode. The solid line arrows are electrical field lines and the dashed line arrows are magnetic field lines.

$$C_f = \frac{(\epsilon_{re})^{1/2}}{2\ c\ Z_0} - \frac{C_p}{2} \tag{7.3}$$

$$C_f' = \frac{C_f}{1 + K_1(h/s)\tanh(10s/h)} \tag{7.4}$$

where the characteristic impedance Z_0, the effective dielectric constant ϵ_{re}, and a constant K_1 in Eqs. (7.3) and (7.4) are:

$$Z_0 = \frac{60}{(\epsilon_{re})^{1/2}} \ln\left(\frac{8h}{w_e} + 0.25\frac{w_e}{h}\right) \tag{7.5}$$

$$\epsilon_{re} = \frac{\epsilon_{r2} + 1}{2} + \frac{\epsilon_{r2} - 1}{2}\left(1 + 10\ \frac{h}{w}\right)^{-1/2} \tag{7.6}$$

$$K_1 = \exp[-0.1\ \exp(2.33 - 2.53\ \frac{w_e}{h})]. \tag{7.7}$$

Similarly, the odd mode capacitance, C_o can be written as

$$C_o = C_p + C_f + C_{g1} + C_{g2} + C_{gt}. \tag{7.8}$$

In Eq. (7.8) the capacitances C_{g1} and C_{g2} are given as follows [63] [94]:

$$C_{g1} = \frac{\epsilon_0\epsilon_{r1}}{\pi} \ln[2\ \frac{1+\sqrt{k'}}{1-\sqrt{k'}}] \qquad \text{for } 0 \le k \le 1/\sqrt{2} \tag{7.9}$$

$$= \frac{\pi\epsilon_0\epsilon_{r1}}{\ln(\frac{1+\sqrt{k}}{1-\sqrt{k}})} \qquad \text{for } 1/\sqrt{2} \le k \le 1 \tag{7.10}$$

$$C_{g2} = \frac{\epsilon_0 \epsilon_{r2}}{\pi} \ln\left[\coth\left(\frac{\pi s}{4h}\right) + 0.65 C_f + \left[\frac{0.02}{s/h}(\epsilon_{r2})^{1/2} + \left(1 - \frac{1}{\epsilon^2_{re}}\right)\right]\right] \tag{7.11}$$

where $k = \dfrac{s/h}{s/h+2w/h}$,

$$k' = (1-k^2)^{1/2},$$

and the gate capacitance, C_{gt} due to a finite metal thickness is

$$C_{gt} = \frac{2\epsilon_0 \epsilon_{r1} t}{s}. \tag{7.12}$$

Effective dielectric constants $\epsilon_{re}{}^e$ and $\epsilon_{re}{}^o$ for even mode and odd mode can be obtained by the equations below:

$$\epsilon_{re}{}^e = \frac{C_e}{C_e{}^a} \tag{7.13}$$

$$\epsilon_{re}{}^o = \frac{C_o}{C_o{}^a} \tag{7.14}$$

where $C_e{}^a$ and $C_o{}^a$ are even and odd mode capacitances when there is no dielectric interface between regions 1 and 2 ($\epsilon_{r1} = \epsilon_{r2} = \epsilon_0$).

The even mode and odd mode phase velocities, $v_p{}^e$ and $v_p{}^o$ and characteristic impedances describing the coupled transmission line behavior are (this assumes $\mu_r = 1$):

$$v_p{}^e = \frac{c}{(\epsilon_{re}{}^e)^{1/2}} \tag{7.15}$$

$$v_p^o = \frac{c}{(\epsilon_{re}^o)^{1/2}} \tag{7.16}$$

$$Z_0^e = \frac{1}{c\ (C_e C_e^a)^{1/2}} \tag{7.17}$$

$$Z_0^o = \frac{1}{c\ (C_o C_o^a)^{1/2}}. \tag{7.18}$$

where c is the speed light. The equations here will be used to investigate the signal crosstalk and mode transition in fast transient measurement in the next few sections.

7.3. Signal Dispersion, Loss and Coupling for Coupled Transmission Lines

For the development of high speed large scale integrated circuits, it is necessary to characterize: 1) signal distortion due to losses (in the conductor and the substrate); 2) impedance discontinuities (at the line termination); 3) coupling effects between adjacent lines; and 4) dispersion caused by changing of the effective dielectric constant with frequency.

The dispersive behavior of coupled microstrip lines describes frequency-dependent dielectric constants for different modes [63]:

$$\epsilon_{re}^e(f) = \epsilon_r - \frac{\epsilon_r - \epsilon_{re}^e}{1 + G\ (f/f_D)^2} \tag{7.19}$$

$$\epsilon_{re}^o(f) = \epsilon_r - \frac{\epsilon_r - \epsilon_{re}^o}{1 + G\ (f/f_D)^2} \tag{7.20}$$

where $G = 0.6 + 0.0045\ Z_0^e$ for even mode

$= 0.6 + 0.018\ Z_0^o$ for odd mode

$$f_D = \frac{Z_0^e}{4\mu_0 h} \quad \text{for even mode}$$

$$= \frac{Z_0^o}{4\mu_0 h} \quad \text{for odd mode.}$$

The above equations are better for CAD modeling than empirical fitting equations [95]. The dispersion concepts apply to the characteristics impedances yield [63]:

$$Z_0^e(f) = Z_0^e - \frac{Z_0^{es} - Z_0^e(0)}{1 + G\ (f/f_D)^{1.6}} \tag{7.21}$$

$$Z_0^o(f) = Z_0^o - \frac{Z0os - Z0o(0)}{1 + G\ (f/f_D)^{1.6}} \tag{7.22}$$

where $Z_0^e(0)$ and $Z_0^o(0)$ are the zero-frequency characteristic impedances given by Eqs. (7.17), (7.18), and

$$Z_0^{es} = \frac{30}{\sqrt{\epsilon_r}} \ln\left(2\,\frac{1+\sqrt{k_e'}}{1-\sqrt{k_e'}}\right) \quad \text{for } 0 \le k_e \le 1/\sqrt{2}$$

$$= \frac{30\pi^2}{\sqrt{\epsilon_r}} \left[\ln\left(2\,\frac{1+\sqrt{k_e}}{1-\sqrt{k_e}}\right)\right]^{-1} \quad \text{for } 1/\sqrt{2} \le k_e \le 1$$

$$Z_0^{os} = \frac{30}{\sqrt{\epsilon_r}} \ln\left(2\,\frac{1+\sqrt{k_o'}}{1-\sqrt{k_o'}}\right) \quad \text{for } 0 \le k_e \le 1/\sqrt{2}$$

$$= \frac{30\pi^2}{\sqrt{\epsilon_r}} \left[\ln\left(2\,\frac{1+\sqrt{k_o}}{1-\sqrt{k_o}}\right)\right]^{-1} \quad \text{for } 1/\sqrt{2} \le k_e \le 1$$

$$k_e = \tanh\left(\frac{\pi}{2}\frac{w}{2h}\right)\tanh\left(\frac{\pi}{2}\frac{w+s}{2h}\right), \qquad k_e' = (1-k_e^2)^{1/2}$$

$$k_o = \tanh\left(\frac{\pi}{2}\frac{w}{2h}\right)\tanh\left(\frac{\pi}{2}\frac{w+s}{2h}\right), \qquad k_o' = (1-k_o^2)^{1/2}.$$

Figures 7.4 and 7.5 show an example of frequency-dependent characteristics impedances and dielectric constants for even mode and odd mode, respectively where the coplanar line system is assumed symmetry. In Fig. 7.4 the even mode permittivity is larger than the odd mode permittivity due to a lower phase velocity. In high frequency ϵ_{re}^{e} and Z_0^e increase more rapidly than ϵ_{re}^{o} and Z_0^o because of the smaller f_D for even mode propagation.

The parameter normally representing the signal crosstalk between two interconnect lines is the coupling coefficient [63] [96] [97]. From the even mode and odd mode characteristic impedances, the coupling coefficient CC is defined as

$$CC = \frac{Z_0^e - Z_0^o}{Z_0^e + Z_0^o}. \tag{7.23}$$

To investigate the relationships of the coupling coefficient with the interconnect line width, substrate thickness, and interconnect lines spacing, CC versus w, s, and h are plotted in Figs. 7.6 and 7.7. When the substrate thickness is large, the interconnect cross coupling becomes smaller. Also, the narrower the interconnect spacing is, the larger is the signal coupling. This can limit VLSI packing density when high speed signal propagation is required. Applying the frequency-dependent characteristic impedances in Eqs. (7.21) and (7.22), the

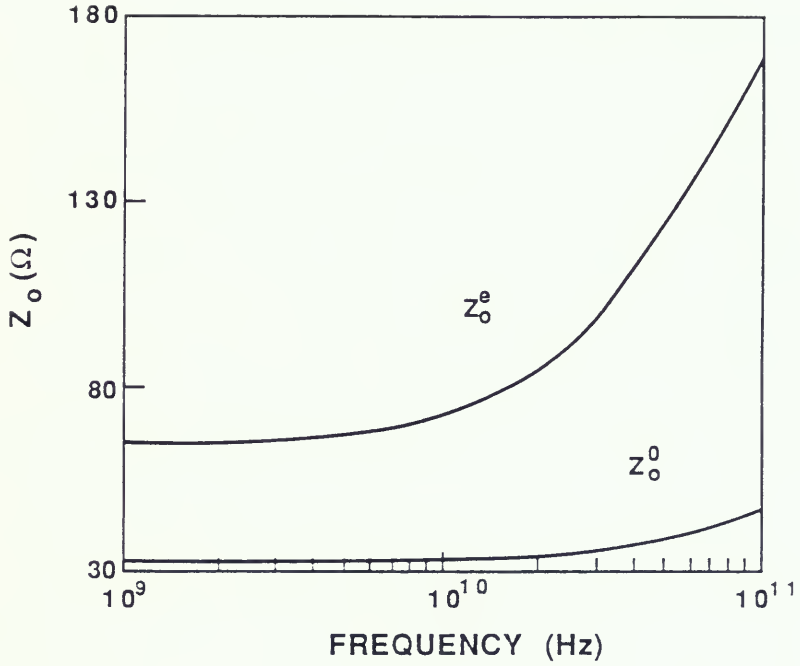

Figure 7.4 Plot of the frequency-dependent even-mode impedance, $Z_0{}^e$ and odd-mode impedance, $Z_0{}^o$.

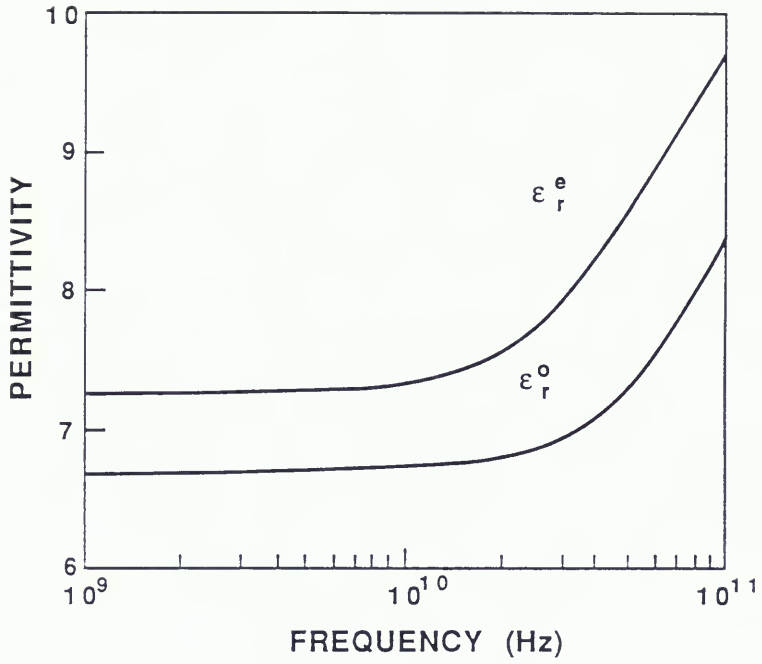

Figure 7.5 Plot of the frequency-dependent even-mode permittivity, ϵ_r^e and odd-mode permittivity, ϵ_r^o.

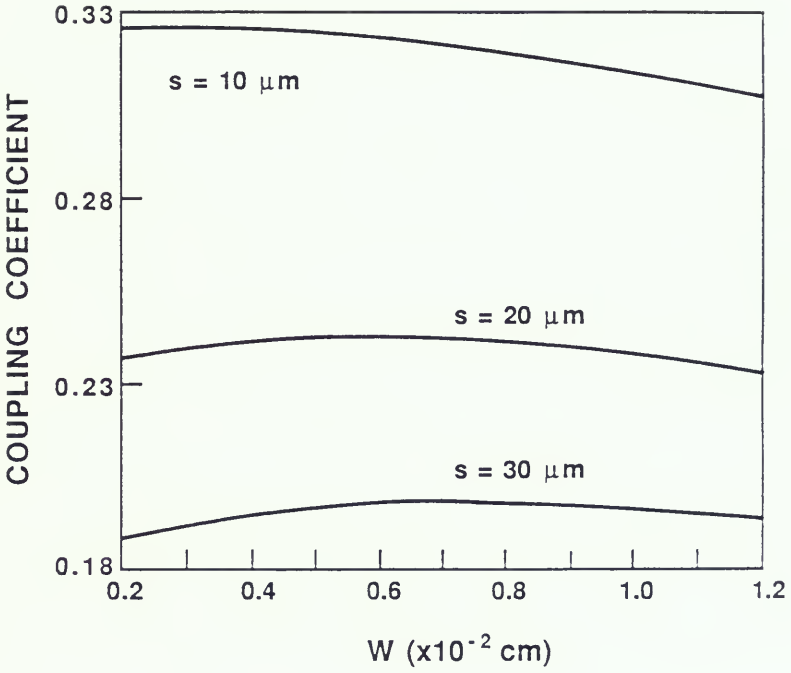

Figure 7.6 Plot of the coupling coefficient versus the interconnect line width, w at different coupled interconnect line spacing, s.

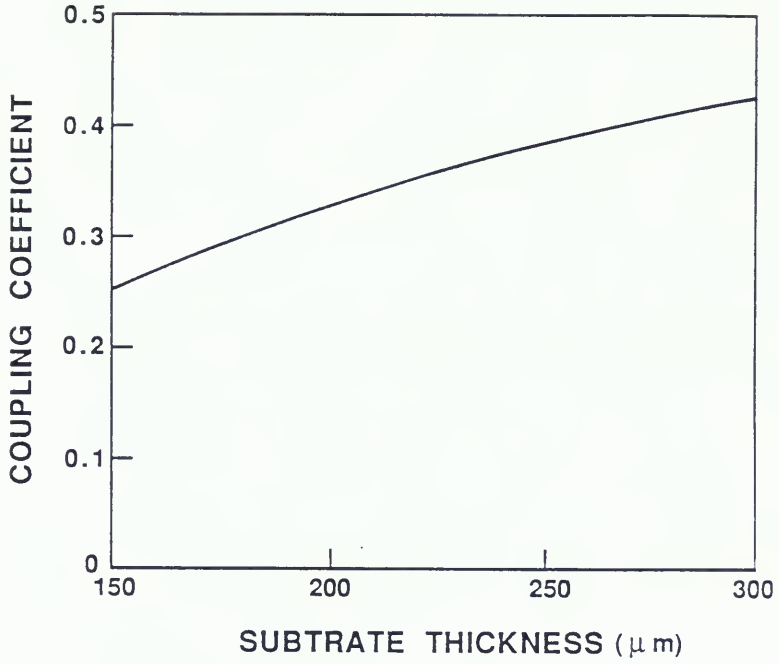

Figure 7.7 Plot of the coupling coefficient versus the substrate thickness.

coupling coefficient versus frequency is obtained in Fig. 7.8. Since Z_0^e increases more rapidly than Z_0^o at high frequencies, the coupling coefficient increases with frequency. This indicates that fast digital switching pulses have a higher cross coupling than steady-state signals.

Coupled microstrip lines have primarily two types of losses: conductor (ohmic) loss and dielectric loss. The conductor loss results from a finite conductivity in the interconnect line and the dielectric loss is from conductivity in the substrate. The attenuation due to conductor loss for even mode propagation and odd mode propagation are [63]:

$$\alpha_c^e = \frac{8.686\ R_s}{240\ \pi\ Z_0^e\ h\ c\ (C_e^a)^2} \left[\frac{ZC_e^a}{Z(w/h)}\left(1 + \delta\frac{w}{2h}\right) - \frac{ZC_e^a}{Z(s/h)}\left(1 - \delta\frac{s}{2h}\right) + \frac{ZC_e^a}{Z(t/h)}\left(1 + \delta\frac{t}{2h}\right)\right] \tag{7.24}$$

$$\alpha_c^o = \frac{8.686\ R_s}{240\ \pi\ Z_0^o\ h\ c\ (C_o^a)^2} \left[\frac{ZC_o^a}{Z(w/h)}\left(1 + \delta\frac{w}{2h}\right) - \frac{ZC_o^a}{Z(s/h)}\left(1 - \delta\frac{s}{2h}\right) + \frac{ZC_o^a}{Z(t/h)}\left(1 + \delta\frac{t}{2h}\right)\right] \tag{7.25}$$

and the attenuation due to dielectric loss are:

$$\alpha_d^e = 27.3\ \frac{\epsilon_r}{(\epsilon_{re}^e)^{1/2}}\ \frac{\epsilon_{re}^e}{\epsilon_r - 1}\ \frac{\tan\delta}{k_0} \tag{7.26}$$

$$\alpha_d^o = 27.3\ \frac{\epsilon_r}{(\epsilon_{re}^o)^{1/2}}\ \frac{\epsilon_{re}^o}{\epsilon_r - 1}\ \frac{\tan\delta}{k_0} \tag{7.27}$$

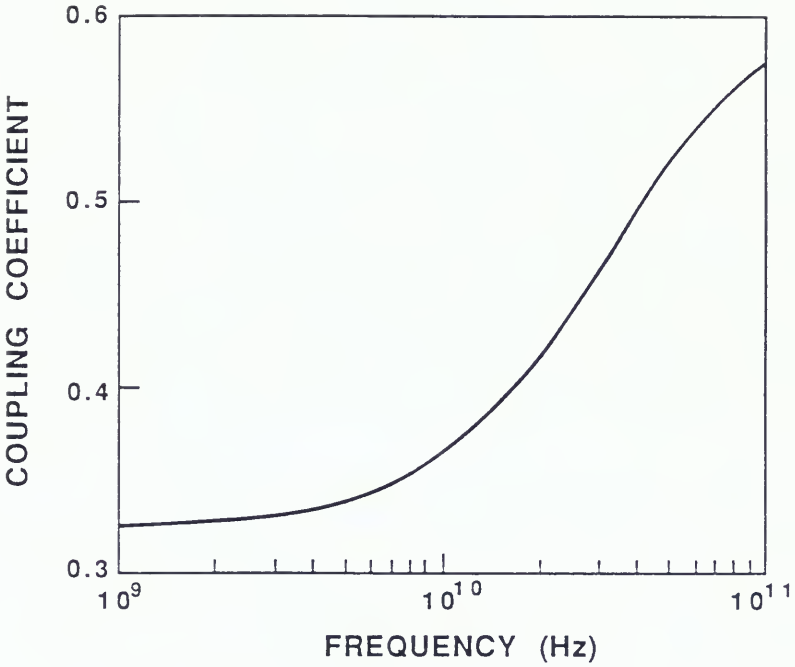

Figure 7.8 Plot of the coupling coefficient versus frequency.

where $\tan\delta$ is the loss tangent of the dielectric substrate, and k_0 is the free space wavelength.

7.4. Mode Transition in Photonic Picosecond Measurement

The signal propagation in even mode and odd mode can be investigated in picosecond time domain measurements by employing photoconductive circuit elements (PCE's). The test structures used in many of the PCE measurements are coupled transmission lines fabricated on a dielectric substrate. The PCE in this research is basically a thin film photoconductor on a silicon substrate [98]. Standard IC fabrication techniques followed by ion-beam irradiation are used to create the photoconductors with picosecond switching speeds [99]. The high recombination rates in the radiation-damaged PCE lead to a fast turnoff when the laser light ceases. This provides picosecond electrical switch.

In general, two PCE's are fabricated with the coupled transmission lines on the same substrate for on-chip fast transient characterization as shown in Fig. 7.9. The first (pulse) PCE is stimulated by a colliding-pulse model-locked (CPM) laser in order to cause rapid conduction. Laser interaction with the PCE gap in microstrip conducts for a short period of time. The second (sampler) PCE samples the charge from the output waveform of a device under test. This sample of charge is produced at a constant difference in time of switching between the pulser PCE and sampler PCE. By varying the difference in the CPM laser beam path length, the entire transient response can be reconstructed. Figure 7.10 shows a coupled transmission

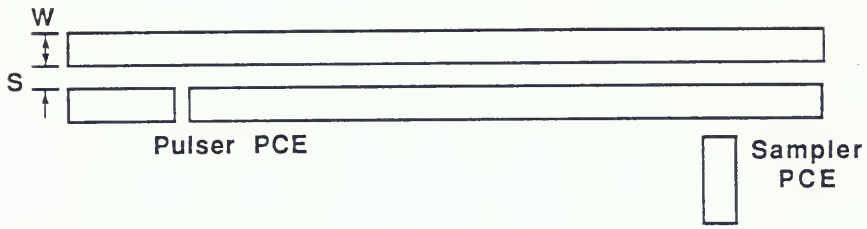

Figure 7.9 Coupled transmission lines layout used for PCE measurement. The left side photoconductor is a pulser PCE and the right side photoconductor is a sampler PCE.

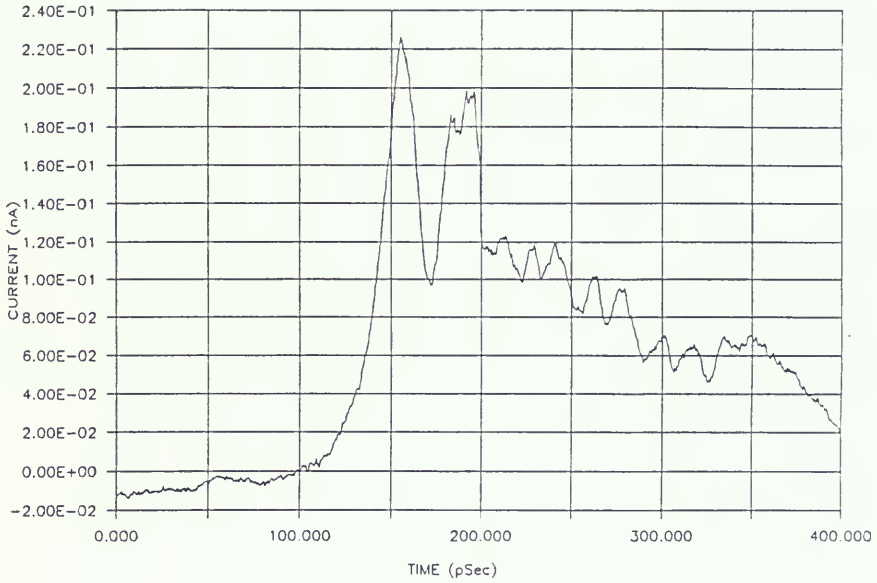

Figure 7.10 Measured picosecond signal propagation on the coupled transmission lines in Fig. 7.9. The PCE measurement was done at Los Alamas National Laboratory by J. Atwater.

line picosecond photoconductive measurement response [100]. In Fig. 7.10 the measured PCE response for coupled transmission lines shows two switching peaks due to even mode to odd mode transition. Applying the frequency-dependent permittivities to Eq. (6.11), the pulse responses for even mode and odd mode can be simulated. The odd mode propagation response for a Gaussian input is faster than that of the even mode due to a higher phase velocity. If the mode splitting occurs during the signal transmission, two-peak pulse response can be obtained, as shown in Fig. 7.11. This pulse splitting is consistent with the PCE measurement above. The details of physical reasoning for mode splitting deserve a further research.

7.5. Equivalent Circuit Model for SPICE

The equivalent circuit model for coupled transmission lines in SPICE simulation is developed in this section. The even mode and odd mode capacitances shown in Sec. 7.2 are used to determine the self capacitances (C_{11} and C_{22}), mutual capacitance (C_{12}), self inductance (L_{11} and L_{22}), and mutual inductance (L_{12}) in Fig. 7.12 as:

$$C_{11} = \frac{1}{2}(C_1^e + C_1^o) \tag{7.28}$$

$$C_{22} = \frac{1}{2}(C_2^e + C_2^o) \tag{7.29}$$

$$C_{12} = \frac{1}{2}(C_1^o - C_1^e) \tag{7.30}$$

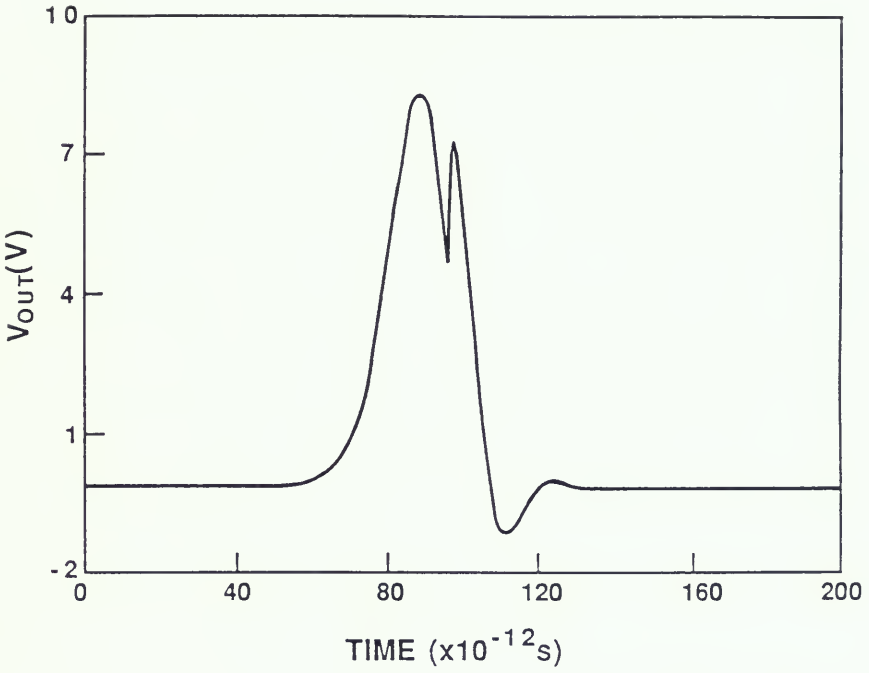

Figure 7.11 Simulated signal propagation on a coupled interconnect lines for even mode and odd mode splitting.

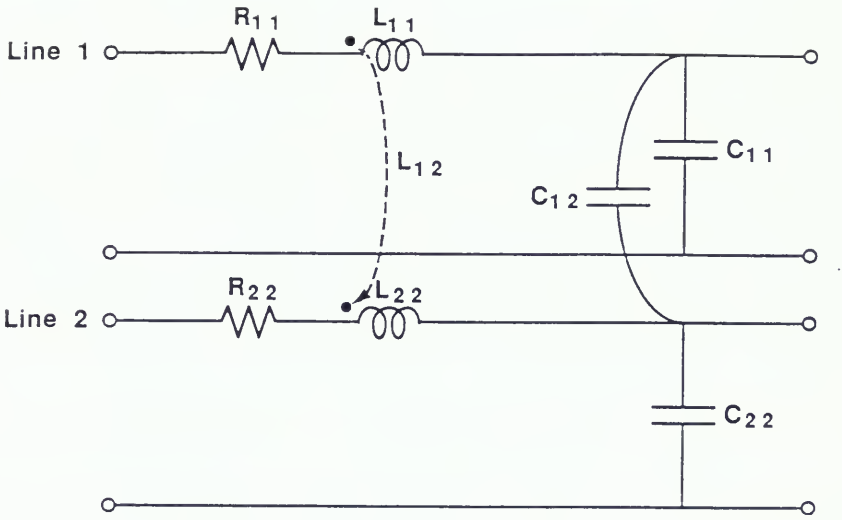

Figure 7.12 Equivalent circuit model per unit length for coupled transmission lines.

$$L_{11} = \frac{\mu_0 \epsilon_0}{2} \left(\frac{1}{C_1^{oa}} + \frac{1}{C_1^{ea}} \right) \tag{7.31}$$

$$L_{22} = \frac{\mu_0 \epsilon_0}{2} \left(\frac{1}{C_2^{oa}} + \frac{1}{C_2^{ea}} \right) \tag{7.32}$$

$$L_{12} = \frac{\mu_0 \epsilon_0}{2} \left(\frac{1}{C_1^{ea}} - \frac{1}{C_1^{oa}} \right) \tag{7.33}$$

where C_1^e is the even mode capacitance for interconnect 1, C_1^o is the odd mode capacitance for interconnect 2, C_2^e is the even mode capacitance for interconnect 2, C_2^o is the odd mode capacitance for interconnect 2.

The interconnect line resistances are given as:

$$R_{11} = \frac{1}{\sigma_{11} w_{11} t_{11}} \tag{7.34}$$

$$R_{22} = \frac{1}{\sigma_{22} w_{22} t_{22}} \tag{7.35}$$

where σ_{11} is metal 1 resistivity, w_{11} is the metal 1 width, t_{11} is the metal 1 thickness, σ_{22} is the metal 2 resistivity, w_{22} is the metal 2 width, and t_{22} is the metal 2 thickness. The interconnect circuit elements above can be used for SPICE/SLICE circuit simulation in a distributed circuit network. The use of frequency-dependent circuit elements is neglected here, but can be added to the simulation using the modeling topology developed in Chapter 6 (e.g., $\epsilon_{eff}(f)$). The voltages and currents on coupled transmission lines are described by

the differential equations below:

$$\frac{\partial V_1}{\partial x} = -R_{11}I_1 - L_{11}\frac{\partial I_1}{\partial t} - L_{12}\frac{\partial I_2}{\partial t} \tag{7.36}$$

$$\frac{\partial V_2}{\partial x} = -R_{22}I_2 - L_{22}\frac{\partial I_2}{\partial t} - L_{12}\frac{\partial I_1}{\partial t} \tag{7.37}$$

$$\frac{\partial I_1}{\partial x} = -C_{11}\frac{\partial V_1}{\partial t} + C12\frac{\partial X_1}{\partial t} \tag{7.38}$$

$$\frac{\partial I_2}{\partial x} = -C_{22}\frac{\partial V_2}{\partial t} + C_{12}\frac{\partial V_2}{\partial t}. \tag{7.39}$$

Those equations above can be solved in a straightforward fashion in the SPICE/SLICE circuit analysis presented in the next section.

7.5. SPICE Simulations and Discussions

The interconnect circuit model developed in Section 7.4 was implemented in SPICE/SLICE for transient response. Figure 7.13 shows three interconnect lines transient response in which curve 1 is from the end point of an active interconnect line and curves 2 and 3 are from the end point of inactive interconnect lines 2 and 3, respectively. It is interesting to note that during switching the inactive interconnect lines (curve 2 and curve 3) are activated by the active interconnect signal line, especially for the nearest neighbor line. The signal coupling results from the coupled electric field and magnetic field effects between interconnect lines. This is represented by the mutual capacitance and mutual inductance in the equivalent

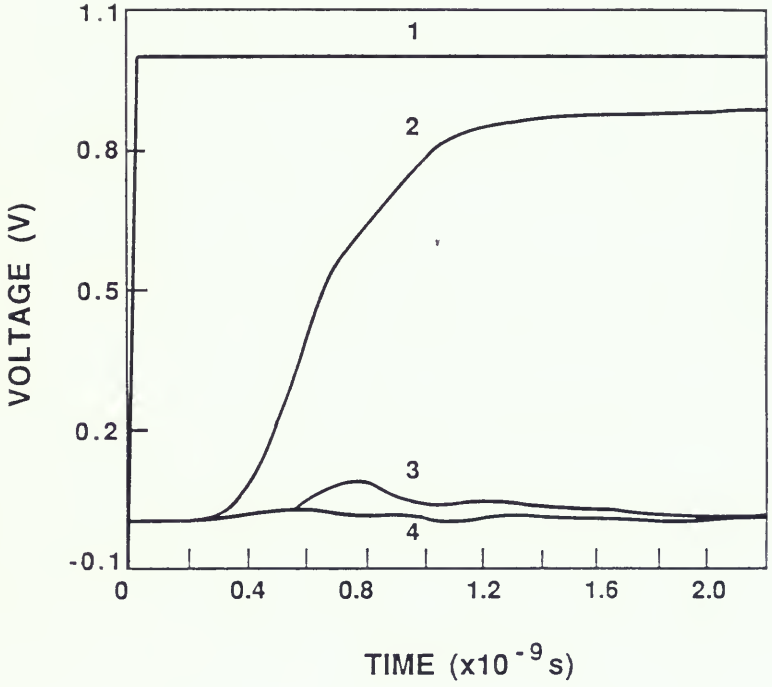

Figure 7.13 Step response of 5 cm coupled interconnect lines. In this plot, curve 1 is a step input, curve 2 is the step response on the active (signal) line, curve 3 and 4 are the signal crosstalk on the inactive lines with 50 Ω load resistances on each side.

circuit model.

Since the capacitance and inductance play an important role in signal transmission and crosstalk, C_{11}, C_{12}, L_{11}, and L_{12} versus w and s are presented in Figs. 7.14, 7.15, 7.16, and 7.17, respectively. In those figures C_{11} and C_{12} increase with w due to normal capacitance effects ($C \propto w$), but decrease with s. L_{11} and L_{12} decrease with w and s. The inverse proportionality of C_{12} and L_{12} with s (Figs. 7.15 and 7.17) happens because the signal crosstalk is reduced when the space between conductors increases.

By varying 2% value of the circuit elements individually in SPICE simulation, the circuit elements sensitivities are obtained. The most sensitivity component in the equivalent circuit is C_{12} which describes the significance of electric coupling. Further simulation of the coupled interconnect end resistance (see Fig. 7.18) indicates that when the neighbor interconnect is floating ($R_L \simeq \infty$), the signal crosstalk becomes larger due to an increase in mutual coupling.

In general, the signal crosstalk can be reduced by using adjacent shielding ground lines [97], a second ground plane over the interconnects [96], a larger substrate thickness, or a wide interconnect spacing.

7.6 Conclusions

The coupled interconnect lines for even mode and odd mode analyses have been studied. Signal loss, dispersion, and crosstalk are discussed. From the even mode and odd mode capacitances, the equivalent circuit model for coupled transmission lines in SPICE simulation is constructed. The space between interconnect lines, the substrate

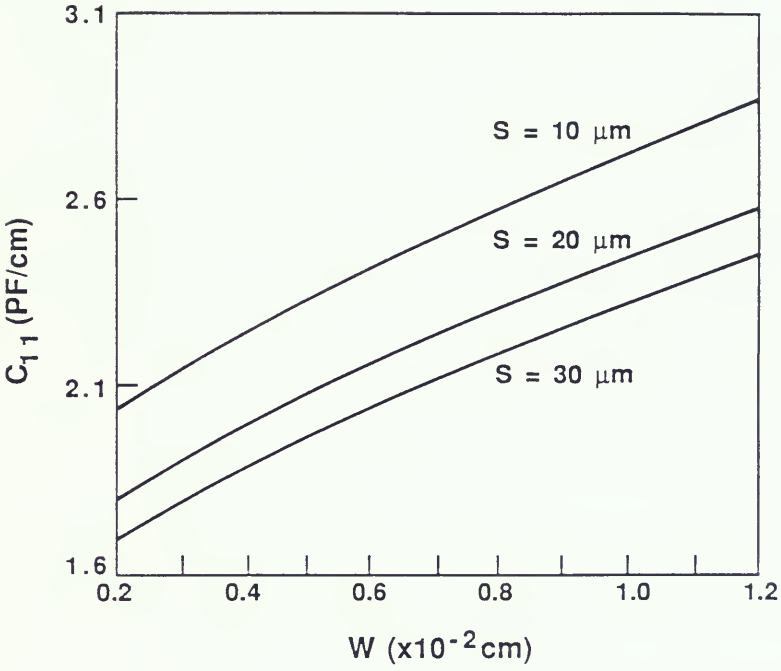

Figure 7.14 Plot of C_{11} versus the interconnect line width, w at different coupled interconnect line spacing, s.

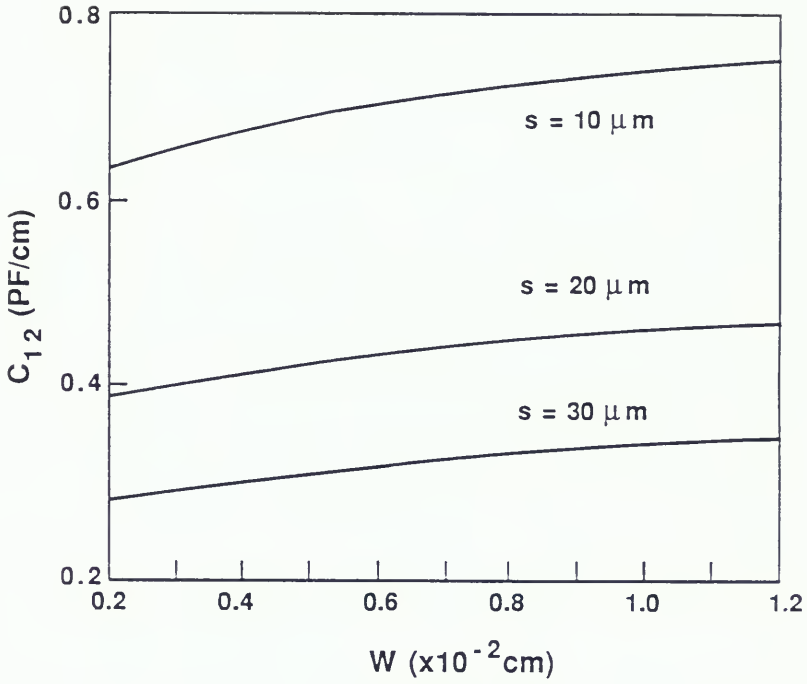

Figure 7.15 Plot of C_{12} versus the interconnect line width, w at different coupled interconnect line spacing, s.

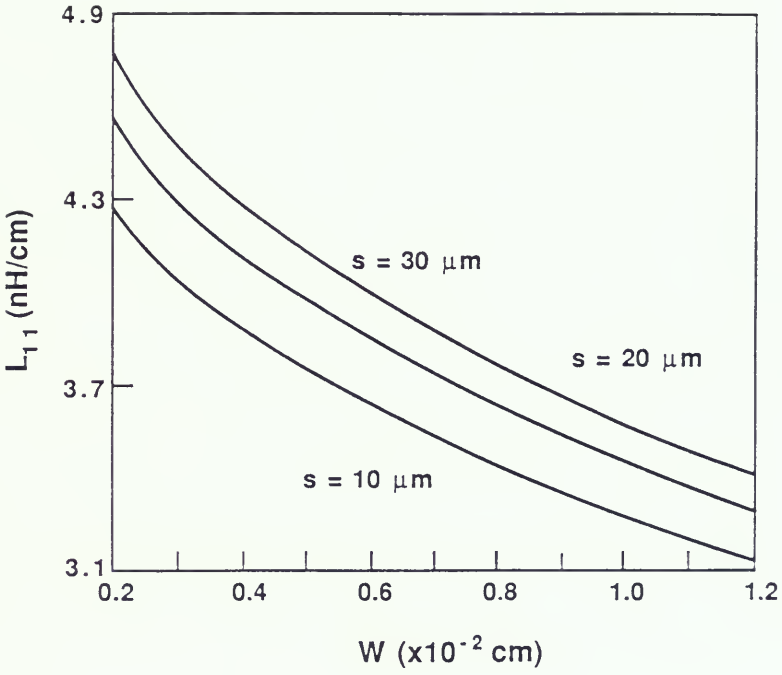

Figure 7.16 Plot of L_{11} versus the interconnect line width, w at different coupled interconnect line spacing, s.

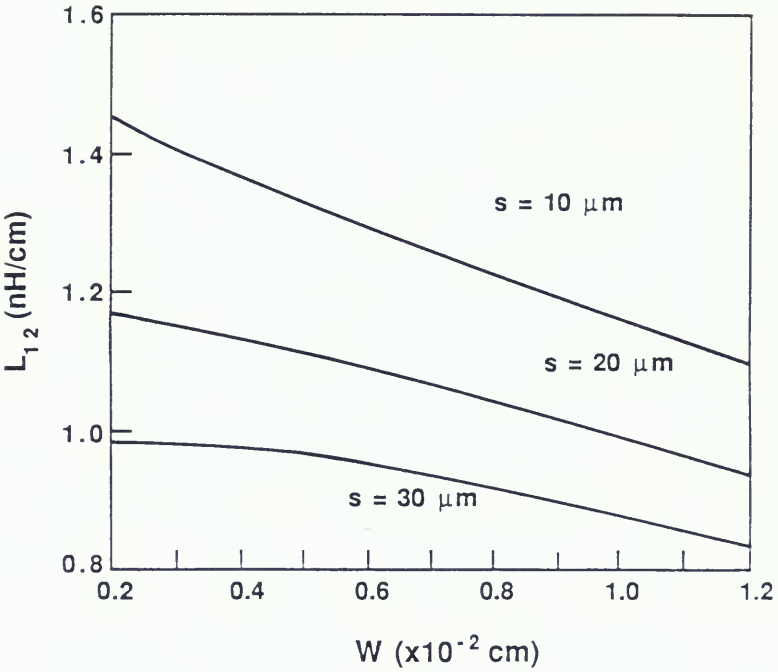

Figure 7.17 Plot of L_{12} versus the interconnect line width, w at different coupled line spacing, s.

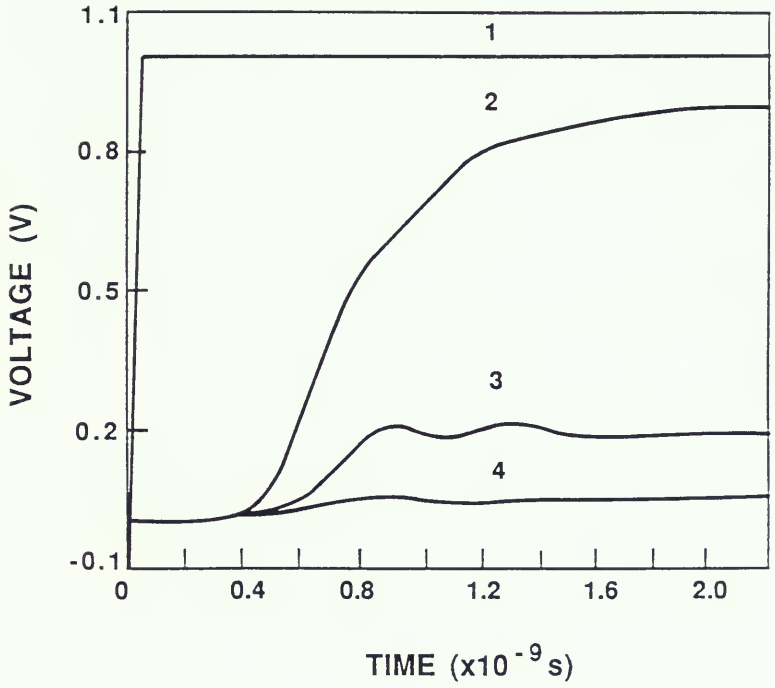

Figure 7.18 Step response of 5 cm coupled interconnect lines. In this plot, curve 1 is a step input, curve 2 is the step response on the active (signal) line, curve 3 and 4 are the signal crosstalk on the inactive lines without load resistances on each side (floating, $R_L = \infty$).

thickness, and the interconnect width are important for signal coupling. For a set of coupled lines, the induced signal on the inactivated lines depends on the coupling coefficients and the slew rate of the propagating signal. This coupling becomes stronger for very high frequency. In the equivalent circuit model, the mutual capacitance is the most significant component describing signal crosstalk. This capacitive cross coupling causes pickup of any signal carried on a nearby conductor track.

CHAPTER EIGHT
SUMMARY AND CONCLUSIONS

The modeling and characterization of bipolar transistors and interconnects for circuit simulation has been presented in earlier chapters. This work provides a comprehensive two-dimensional circuit and interconnect modeling for advanced bipolar IC techniques useful in computer-aided device and circuit design. Illustrative measurements and simulations demonstrate the modeling accuracy.

The major accomplishments of this study are: first, implemented the user-defined-controlled-sources techniques for new circuit model development. By using the voltage-controlled current sources, newly developed circuit model equations are inserted in UDCSs which are compiled with original SPICE circuit matrix programs for model implementation. Thus, physical mechanisms such as collector current spreading, emitter crowding, and sidewall injection can be included, second, explored the two-dimensional collector current spreading mechanism in quasi-saturation. The collector current spreading ameliorates base pushout to increase the BJT's current gain and cutoff frequency, third, developed a quasi-2-D circuit model for collector current spreading effects. The model refines the previous 1-D physical model for high current transients, fourth, developed a physics-based current-dependent base resistance model for all injection levels. The base resistance model accounts for the physical effects of base width modulation, base conductivity modulation, emitter current crowding, and

base pushout, fifth, developed a circuit model for transient emitter crowding, sidewall injection effects. The model represents the nonuniform current and charge distribution under the emitter and at the emitter-base sidewall and the current-dependent base resistance in a unified manner, sixth, predicted s-parameter measurement responses using a physical device simulator and newly developed software. The parasitics effects of the test structures are included in the modeling package, seventh, improved the single interconnect model for advanced IC cross-section profiles. The model includes the effects of conductor loss, dielectric loss, and dispersion, eighth, refined the coupled interconnect model for signal coupling and crosstalk. Finally, implemented the mixed-mode circuit simulation including the bipolar transistors and interconnects.

The author suggests the following research based on the methods and approaches of the present study: 1) explore the physics details about the transient collector spreading mechanism. One can start this by probing the transient device simulations in quasi-saturation; 2) investigate the three-dimensional behavior of collector spreading, emitter crowding, and sidewall injection by investigating the 3-D device simulation or strategical designed test structures for different emitter widths, emitter lengths, shapes of emitter area; 3) develop a comprehensive circuit model for the coupling effects of collector current spreading and emitter current crowding; 4) explore the time-dependent base resistance model in digital switching form the physical insight of transient device simulation ; 5) include more experimental studies for s-parameter terminal responses; 6) explore more

experimental evaluations for current spreading and transient crowding based on strategical test structures; 7) investigate the on-chip fast transient measurement of the advanced bipolar transistors by photoconductive circuit element techniques; 8) develop the multilevel interconnect model from 3-D capacitance solver for process diagnosis and circuit simulation; 9) include the frequency-dependent circuit elements in SPICE transient simulation for signal dispersion in very fast switching transient; 10) extend the mixed-mode circuit simulation for various regions of BJT operation in which the collector current spreading or emitter current crowding or both are significant.

APPENDIX A
TWO-DIMENSIONAL NUMERICAL SIMULATION WITH PISCES

A.1 Introduction

The two-dimensional bipolar transistor models, physics-based current-dependent base resistance, and s-parameter measurement prediction for advanced bipolar transistors in Chapters 2, 3, 4, and 5 are developed using the physical insights gained from PISCES based two-dimensional device simulations. Since the physical parameters internal to device simulators are critical to the accuracy of the device simulation, the physical modeling in PISCES is discussed in this Appendix. Also, some controversial parameters for heavy doping effects are addressed here in order to correctly interpret the simulation results.

A.2 Physical Mechanisms in PISCES - II

PISCES is a two-dimensional, two-carrier semiconductor device simulator which predicts transistor (e.g., BJT, NMOS, CMOS, SOI-MOSFET, power device, etc) electrical behavior under steady-state, transient, and small-signal excitations. In general, device simulators solve the partial differential Poisson equation ($\epsilon\nabla^2\psi = -q(p-n+N_D^+-N_A^-)-\rho_F$) and continuity equations ($\partial n/\partial t = 1/q\ \nabla J_n - U_n$, $\partial p/\partial t = -1/q\ \nabla J_p - U_p$) by finite element methods (PISCES) or finite difference methods (SEDAN, BAMBI).

In the continuity equations above, the recombination models supported in PISCES are the Shockley-Read-Hall (SRH) model and Auger recombination model:

$$U_{SRH} = \frac{pn - n_{ie}^2}{\tau_p[n+n_{ie}\exp(\frac{E_t-E_i}{kT})] + \tau_n[p+n_{ie}\exp(\frac{E_i-E_t}{kT})]} \quad (A.1)$$

$$U_{Auger} = c_n(pn^2-nn_{ie}^2) + c_p(np^2-pn_{ie}^2) \quad (A.2)$$

where E_i is the intrinsic Fermi energy, E_t is the trap energy level, n_{ie} is the effective intrinsic concentration including the bandgap narrowing effects [101]

$$n_{ie}(x,y) = n_i\exp\{\frac{9\times10^{-3}}{2kT/q}\{\ln\frac{N(x,y)}{10^{17}} + [(\ln\frac{N(x,y)}{10^{17}})^2 + \frac{1}{2}]^{1/2}\}\}, \quad (A.3)$$

τ_n and τ_p are the electron and hole lifetimes which are concentration dependent:

$$\tau_n(x,y) = \frac{\tau_{n0}}{1+N(x,y)/N_{SRH-n}} \quad (A.4)$$

$$\tau_p(x,y) = \frac{\tau_{p0}}{1+N(x,y)/N_{SRH-p}}, \quad (A.5)$$

and c_n and c_p are Auger coefficients for n^+ and p^+ materials.

The default parameters for N_{SRH-n}, N_{SRH-p}, c_n, and c_p in PISCES are 5×10^{16}, 5×10^{16}, 2.8×10^{-31}, and 9.9×10^{-32}, respectively. Note that the notation for c_n and c_p is different than the conventional

one which defines c_n for electron recombination in p^+-type silicon and c_p for hole recombination in n^+-type silicon. Due to the difficulty in characterization of heavy doping effects, the controversial physical parameter c_n is in the range of 1×10^{-31} to 3×10^{-31} [102] [103]. Different values for c_n are used in various device simulators (0.5×10^{-31} in [104], 1.0×10^{-31} [105], 1.5×10^{-31} [106], and 2.8×10^{-31} [107]).

Another controversial issue is the mobility model in PISCES. Due to a different scattering mechanism and Coulomb force on electrons (repulse force) and holes (attract force) in the heavily doped n^+ material, the majority carrier mobility and minority carrier mobility can be significantly different. Models for explaining the physical origin of the difference are presented in [108-110]. Even though the physical mechanisms are not clearly understood, the difference between the majority and the minority carrier mobilities is clearly established and it is enhanced in the highly doped region [111-113]. This difference is not accounted for at all in PISCES-II and deserves consideration in PISCES simulation interpretation.

A.3 Discussion

The self-aligned polysilicon-emitter transistor has become the predominant device structure for today's high-performance bipolar VLSI circuits due to its low base current or high β. This high current gain is usually traded for a low base resistance (high base doping) to increase f_T [114] [115]; however, the polysilicon and monosilicon interface is not readily controllable which results in a process-

dependent surface recombination at the polysilicon contact. The process variation and the uncertainties in the polysilicon heavy doping parameters make it difficult to match simulation results with measurements.

In order to get the representative simulation results, we model the polysilicon contact by an effective surface recombination velocity s_p in the range of 1×10^4 to 5×10^4 cm/s [19]. By adjusting s_p, c_n, mobilities, and carrier lifetimes to match dc measurements, reasonable simulation can be obtained. In addition, The uncertainties caused by the heavy doping effects and the polysilicon interface are critical in the emitter design, but are less significant for analysis of collector (collector spreading in Chapter 2), and analysis of the base (base resistance in Chapter 3, emitter crowding in Chapter 4). In fact, the author suggests that the circuit designers look at both the physical insight from device simulations and quantitative terminal responses from device measurements. The modeling implementation techniques for new circuit model development is presented in Appendix B.

APPENDIX B
BIPOLAR TRANSISTOR MODELING IMPLEMENTATION TECHNIQUES ON SLICE/SPICE

B.1 Introduction

The multidimensional current effects developed in chapters 2, 3, and 4 are not properly accounted for in the existing models built into the common circuit simulator SPICE. A flexible set of subroutines has therefore been developed which enable one to implement the novel bipolar transistor model into the SLICE, a Harris Corporation derivation of the SPICE program. The use of user-defined controlled sources for SOI MOSFET modeling was first investigated by S. Veeraraghavan et al. [23]. The methodology for implementing dc, transient, and small-signal models in the form of flexible subroutines for advanced bipolar transistor into SLICE is presented here.

B.2 User-Defined-Controlled-Sources

The flexible modeling subroutines, user-defined-controlled-sources (UDCS's), in the SLICE circuit simulator are typically used for new circuit model development. UDCS's include 1) voltage-controlled voltage sources, 2) voltage-controlled current sources, 3) current-controlled voltage sources, and 4) current-controlled current sources. The UDCS's nodes are automatically incorporated by the SLICE program [116] into a circuit simulation matrix during the computer simulation of a circuit. When using a UDCS form of the model equations, one can modify the transistor behavior and not be concerned with the matrix

operation, memory management, and data structures of the SPICE circuit simulator.

The formulation of UDCS subroutines requires 1) a device parametric description, 2) conservation of numerical overflow, 3) modeling the device current-voltage relations, and 4) evaluating the device charging currents. Figure B.1 is a flow chart outlining the steps necessary to write a UDCS subroutine. At the top of the UDCS subroutine, one must define the device model parameters and the model control nodes. Then the SPICE subroutine PNJLIM is called in order to prevent numerical overflow [117]. Next, the presentation of the device's currents as a function of node voltages is added to the subroutine. At this point the dc UDCS subroutine has been completed. Small-signal capability may be added to the UDCS subroutine by calculating the device's small-signal components in terms of dc bias and inserting the information in the UDCS subroutine.

Transient capability and charge-control modeling can also be added to the UDCS subroutine. First the SPICE COMMON block STATUS must be inserted into the subroutine and then device model parameters and transient model control nodes are defined. An initialization of the transient model values is performed at time equals zero. Numerical overflow must be prevented as in the dc UDCS subroutine. Finally, transient current and transient conductance representations are appended to the UDCS subroutine. Note, that the current-voltage relations and transient current derivations entered into the UDCS subroutine are based on the relevant analytical device model.

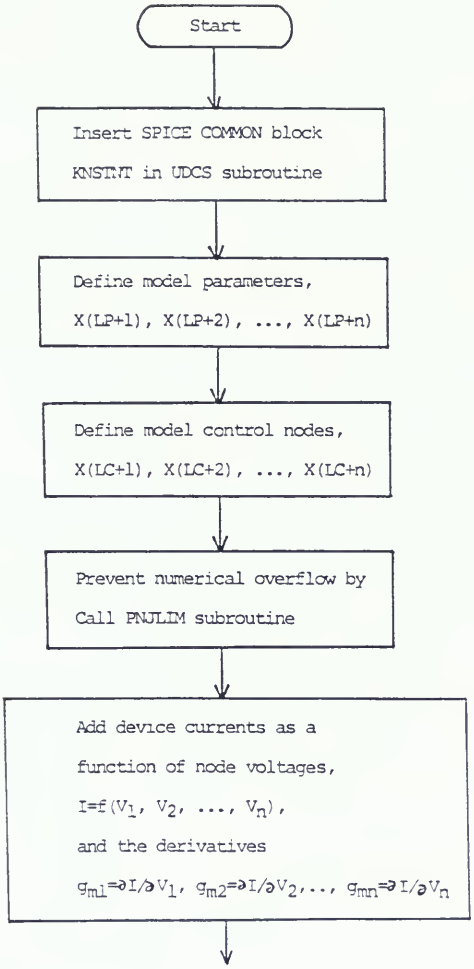

Figure B.1 Flow chart for UDCS subroutines implementation

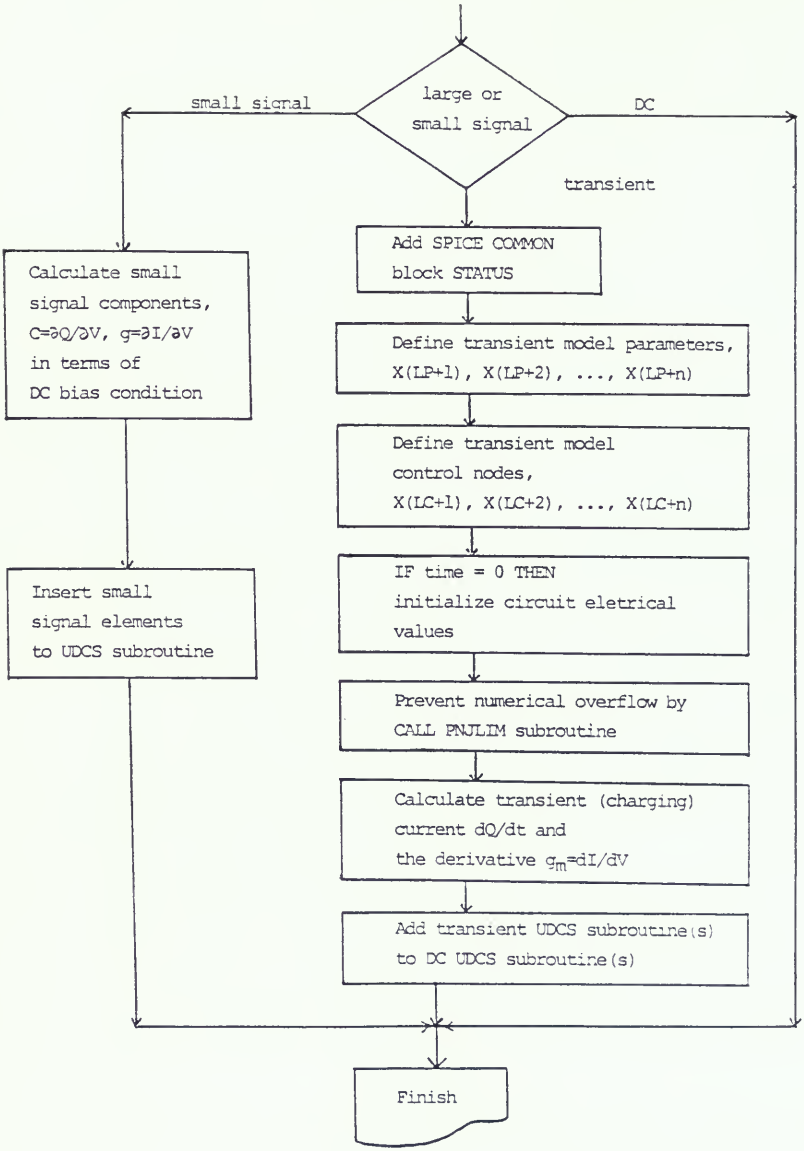

Figure B.1 continued

The transient current, dQ/dt, and transconductance, dI/dV, at different time points are calculated as follows:

$$\frac{dQ}{dt}[V_m(t)] = \frac{2Q[V_{m-1}(t)]}{dt}\left[\frac{2Q(t)}{dt} + \frac{dQ(t)}{dt}\right] \tag{B.1}$$

$$g_m = \frac{2}{dt}\frac{dQ}{dV}[V_{m-1}(t)] \tag{B.2}$$

where m and m-1 are the present and previous time points, respectively.

The numerical integration methods, such as 1) the implicit second-order trapezoidal rule or 2) the Gear-2 method, are available for the SPICE transient calculation. It is necessary to control the local truncation error using the time step, in order to obtain reasonable solution accuracy and stability in the transient simulation [118].

Since the bipolar transistor model has exponential voltage-controlled current source terms, it is possible to produce an unbounded solution point during the Newton-Raphson iterations. This numerical overflow problem should be avoided by setting the critical voltage as [118] [119]

$$V_{critical} = \frac{kT}{q}\ln\left(\frac{kT}{\sqrt{2}\,q\,I_S}\right). \tag{B.3}$$

Then, change the voltage increments during the Newton-Raphson iterations smoothly as [119]

$$\Delta V_i = \frac{kT}{q}\ln\left(1 + \frac{q\Delta V_i}{kT}\right). \tag{B.4}$$

The subroutine PNJLIM is SPICE is called in the UDCS subroutines to prevent the overflow problems. In addition, some of the built-in parameters in SLICE, such as the absolute tolerance, ϵ_a, the relative tolerance, ϵ_r, and the charge tolerance, ϵ_c, can be modified to avoid divergence. This is especially important when the circuit is ill-conditioned (i.e. the nodal capacitance is very small and the nodal inductance is large).

B.3 UDCS Implementation of the BJT model

The UDCS implementation of SPICE Gummel-Poon model is presented in this section in order to demonstrate flexible user-defined subroutines. The standard SPICE Gummel-poon implementation uses the following collector and base current equations [120]:

$$I_C = \frac{I_S}{q_b}\left[\exp\left(\frac{qV_{BE}'}{kT}\right) - \exp\left(\frac{qV_{BC}'}{kT}\right)\right] - \frac{I_S}{\beta_R}\left[\exp\left(\frac{qV_{BC}'}{kT}\right) - 1\right]$$

$$- \frac{I_S}{\beta_R}\left[\exp\left(\frac{qV_{BC}'}{kT}\right) - 1\right] - C_4 I_S \exp\left(\frac{qV_{BC}'}{n_c kT}\right) - 1] \qquad (B.5)$$

$$I_B = \frac{I_S}{\beta_F}\left[\exp\left(\frac{qV_{BE}'}{kT}\right) - 1\right] + \frac{I_S}{\beta_R}\left[\exp\left(\frac{qV_{BC}'}{kT}\right) - 1\right]$$

$$+ C_2 I_S\left[\exp\left(\frac{qV_{BE}'}{n_e kT}\right) - 1\right] + C_4 I_S\left[\exp\left(\frac{qV_{BC}'}{n_c kT}\right) - 1\right] \qquad (B.6)$$

where $q_b = \frac{q_1}{2} + \left[\left(\frac{q_1}{2}\right)^2 + q_2\right]^{1/2}$,

$$q_1 = 1 + \frac{V_{BC}'}{V_A} + \frac{V_{BE}'}{V_B},$$

$$q_2 = \frac{I_S}{I_K}\left[\exp\left(\frac{qV_{BE}'}{kT}\right) - 1\right] + \frac{I_S}{I_{KR}}\left[\exp\left(\frac{qV_{BC}'}{kT}\right) - 1\right].$$

Transient modeling of bipolar transistor behavior is essential for simulating high-speed bipolar switching circuits. Modern digital bipolar circuit models must be able to predict the behavior of ECL, and other logic family designs. During the bipolar transistor transient operation, it is necessary to consider the time-varying base-emitter and base-collector junction charging currents. The charge, Q_{BE}, associated with the base-emitter junction includes the neutralized charge (mobile carrier charge) and the unneutralized charge (deletion charge) which can be represented as:

$$Q_{BE} = I_S \tau_F \left[\exp\left(\frac{qV_{BE}'}{kT}\right) - 1\right] + C_{JE0} \int_0^{V_{BE}'} \left(1 - \frac{V}{\phi_e}\right)^{-me} dV. \qquad (B.7)$$

Similarly, the charge, Q_{BC}, associated with the base-collector junction is given as:

$$Q_{BC} = I_S \tau_R \left[\exp\left(\frac{qV_{BC}'}{kT}\right) - 1\right] + C_{JC0} \int_0^{V_{BC}'} \left(1 - \frac{V}{\phi_c}\right)^{-mc} dV. \qquad (B.8)$$

Adding the transient current component terms to (B.5) and (B.6) yields the following expressions:

$$I_C = \frac{I_S}{q_b}\left[\exp\left(\frac{qV_{BE}'}{kT}\right) - \exp\left(\frac{qV_{BC}'}{kT}\right)\right] - \frac{I_S}{\beta_R}\left[\exp\left(\frac{qV_{BC}'}{kT}\right) - 1\right]$$

$$- \frac{I_S}{\beta_R}\left[\exp\left(\frac{qV_{BC}'}{kT}\right) - 1\right] - C_4 I_S \exp\left(\frac{qV_{BC}'}{n_c kT}\right) - 1] - \frac{dQ_{BC}}{dt} \qquad (B.9)$$

$$I_B = \frac{I_S}{\beta_F}\left[\exp\left(\frac{qV_{BE}'}{kT}\right) - 1\right] + \frac{I_S}{\beta_R}\left[\exp\left(\frac{qV_{BC}'}{kT}\right) - 1\right]$$

$$+ C_2 I_S\left[\exp\left(\frac{qV_{BE}'}{kT}\right) - 1\right] + C_4 I_S\left[\exp\left(\frac{qV_{BC}'}{kT}\right) - 1\right] + \frac{dQ_{BC}}{dt} + \frac{dQ_{BE}}{dt} \qquad (B.10)$$

The charge control circuit model implemented in the UDCS subroutines is shown in Fig. B.2. Each voltage-controlled current source in Fig. B.2 is one UDCS subroutine in the SPICE subcircuit. The UDCS subroutines calculate the collector, base, emitter-base transient, and collector-base transient currents as (B.5)-(B.8), respectively. For the UDCS bipolar modeling, a controlled subroutine calls the transient UDCS subroutines in coordination with dc UDCS subroutines in response to a transient stimulus. The resistance R_C, R_E, and R_B are incorporated into the subcircuit file.

B.4 Conclusions

The Gummel-Poon bipolar transistor modeling using UDCS subroutines has been described. The UDCS approach is an efficient, flexible way to incorporate new device models into the SPICE/SLICE circuit simulator. The UDCS approach works independently of the matrix operations, the memory management, and the various numerical solution

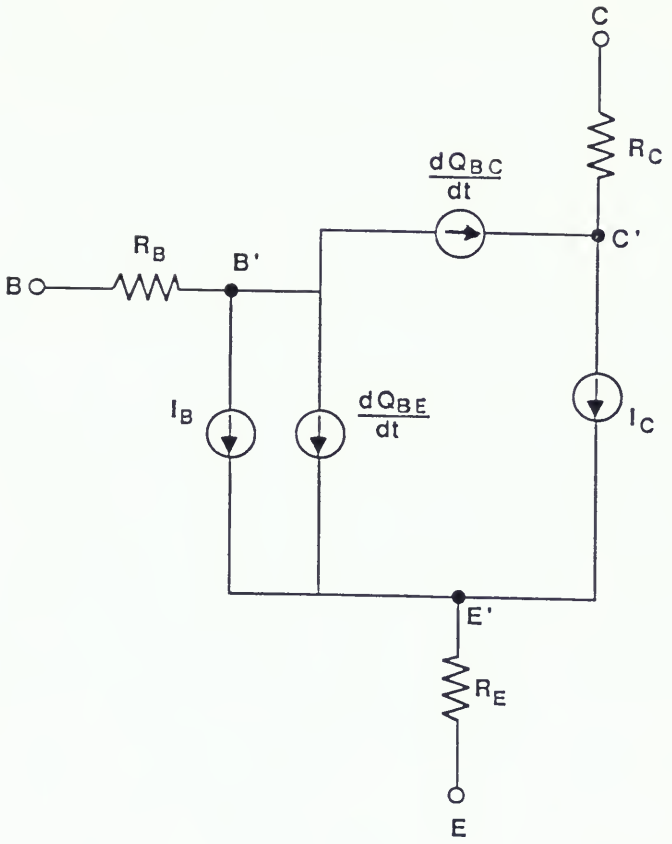

Figure B.2 Network representation of the Gummel-Poon model for UDCS implementation.

techniques implemented into the SPICE/SLICE program. The use of UDCS approach greatly reduces the time for inserting new model equations into the SPICE/SLICE program. In addition, the UDCS subroutine provides a method for simulating device behavior which can not be described in a closed-form analytic solution.

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I certify that I have read this study and that in my opinion it confirms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

William R. Eisenstadt, Chair
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I certify that I have read this study and that in my opinion it confirms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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December 1988

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