INVESTIGATION OF INTERFACE PROPERTIES AND HOT CARRIER DEGRADATION EFFECTS IN SILICON-ON-INSULATOR MATERIALS AND DEVICES

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This research effort mainly deals with the studies of interface properties and parasitic bipolar conduction on hot carrier degradation effects and the modeling of the GAA (Gate-All-Around) MOSFET's in thin-film silicon-on-insulator (SOI) materials and devices. It consists of three parts: In the first part, a contactless S-polarized reflectance optical technique for mapping and determining the top Si film and buried oxide layer thicknesses and an optical modulation technique for determining and mapping the interface recombination velocities and substrate carrier lifetimes in SIMOX (Separation by IMplantation of OXygen) SOI wafers have been developed for use as quality control and processing evaluation tools in the fabrication of ULSI circuits. In the second part, the extraction of degradation parameters in the defective region after hot carrier stress and the modeling of floating body effects in the partially depleted (PD) SOI devices are presented. In the third part, A modeling of GAA devices and the extraction of parameters are depicted.

Mapping of the top Si film and buried oxide thicknesses in a SIMOX wafer was performed by using a contactless S-polarized reflectance optical modulation (DBSPR) technique. The DBSPR method is based on the S-polarized reflectance measured at oblique incident angles in the SIMOX wafer. A theoretical model was developed to extract the top Si film and buried oxide layer thicknesses from the DBSPR technique. Mapping of the interface recombination velocities and substrate carrier lifetimes in a SIMOX wafer was performed by using a contactless optical modulation technique. The optical method is based on the modulation of transmission intensity of an infrared (IR) probe-beam by a visible pump-beam ($h\nu \geq E_g$) via free carrier absorption in the SIMOX wafer. A theoretical model was developed to determine the interface recombination velocities and substrate carrier lifetimes from the optical modulation technique. The evaluation of implantation-condition effects on the defect formation mechanisms in an annealed SIMOX wafer by using the DBSPR and the optical modulation techniques is also presented.

The extraction of degradation parameters in the defective region after hot carrier stress in the PD SOI MOSFET's is discussed. Moreover, the developed model and the experimental results reveal the aggravation of hot carrier effects on the parasitic bipolar transistor conduction in the PD SOI devices. Using the two-piece model, the degradation parameters in the defective region can be extracted. The modification of kink behavior, breakdown voltage, and parasitic bipolar action after the hot carrier stress is predicted by the developed models and observed in the experiment.

Modeling of the GAA devices was developed. The gate-all-around structure of the GAA devices provides the enhancement of drain current and transconductance. Due to the volume-inversion effect, the mobility is enhanced in the GAA devices. Using the measured drain current versus gate voltage characteristics, the modeling parameters can be obtained. Several current-voltage methods are employed to verify the extracted parameters.

CHAPTER 1
INTRODUCTION

In an MOS transistor, only the very top region of the silicon wafer is actually useful for electron transport. The inactive volume induces only undesirable, parasitic effects. SOI (silicon-on-insulator) structures emerged from the idea of isolating the active device overlay from the detrimental influence of silicon substrate. The top silicon film thickness of SOI can be adjusted to meet the requirements of the performance of any electronic devices.

The SOI technology is becoming increasingly important for many ULSI applications due to the many advantages of this technology such as being capable of operating at high temperature, high speed, high packing density, radiation hardness, and the lower fabrication cost of device isolation. In ULSI circuits the advantages of thin film SOI device structure over its bulk silicon counterparts include high carrier mobility, sharp subthreshold slope, ameliorated short-channel effects, reduced hot-carrier degradation, and increased drain current. In subquarter micron regime, the ultra-thin-film CMOS/SIMOX technology is very promising for future low voltage ULSIs [1]. Recently, the development of fully-depleted (FD) SOI devices fabricated on ultra-thin SOI films has drawn great interest in SIMOX and bonded SOI wafers for high-speed ULSI applications. This is mainly due to the reduction of parasitic capacitances, body charging effects, threshold voltage shifting, latch-up effects, short channel effect, and higher drive current ability. However, several device and material problems need to be overcome before mainstream IC applications of these SOI materials can be fully realized. These include (i) floating body effects; (ii) heat dissipation

through the buried oxide (BOX) layer; (iii) the effects of back interface on device reliability [2]; (iv) film thickness control in FD devices [3]; (v) the necessity of low defect density, low cost ultra-thin film substrate (e.g., top Si film $< 100\ nm$); (vi) buried oxide integrity, and (vii) heavy metal contamination. As the SOI technology enters the deep sub-micron CMOS regime, the supply voltage will be reduced below 2 V [4]. The inherent low breakdown voltage due to parasitic bipolar action in fully depleted(FD) devices, heat dissipation, and reliability problems will no longer be much of a problem for low voltage (< 2.5 V) applications. For a ultra-thin-film CMOS/SIMOX ULSIs, the high series resistance impairs the speed advantage. A selective deposited material on the source and drain region is necessary[5]. Salicidation on the source and drain may reduce drain/source parasitic resistance [6], but a gate-to-source/drain leakage due to bridge [7] was observed. In addition, impurities in the sources of silicidation metal (e.g. Ti, Co, W etc.) can thermally diffuse in the later annealing. The stacking fault on the Si/SiO_2 interface induced by oxygen implantation during formation of the SOI structure can be decorated by these heavy metals. Also, source/drain implantation and active region doping are other possible sources to introduce the contamination impurities. This intrinsic gettering becomes generation-recombination centers in the back channel, and the leaking current in the back channel may result an increased subthreshold swing and a deteriorated short channel effect.

Thinner BOX layers offer a better control of short channel effects, improvement of the quality of silicon overlayer, heat dissipation, and reduction of the wafer manufacturing costs. The advantageous reduction in parasitic capacitance offered by the SOI is somewhat diminished by thinning of the BOX. However, the PISCES simulations show that increased capacitances due to a thinner BOX layer are minor compared to bulk junction depletion capacitance [8]. Production of SIMOX wafers with thin BOX layers requires special processing techniques to achieve an integral insulating layer.

To optimize the integrity of the formed oxide layer needs further study.

This dissertation mainly deals with the study of interface properties and parasitic bipolar conduction on hot carrier degradation effects and the modeling of the GAA (Gate-All-Around) MOSFET's in thin-film silicon-on-insulator (SOI) materials and devices. There are three basic objectives: (1) To develop a contactless S-polarized reflectance optical technique for mapping and determining the top Si film and buried oxide layer thicknesses, and to develop an optical modulation technique for determining and mapping the interface recombination velocities and substrate carrier lifetimes in SIMOX SOI wafers for use as quality control and processing evaluation tools in the fabrication of ULSI circuits, (2) to extract the degradation parameters in the defective region after hot carrier stress and to investigate and modeling the floating body effects in the partially depleted (PD) SOI devices, (3) to analyze the current-voltage characteristics and to extract physical parameters for the GAA nMOS SOI devices.

Chapter 2 describes the theoretical and experimental aspects of the top Si film and buried oxide layer thickness measurements on SIMOX samples by using a dual-beam S-polarized reflectance (DBSPR) optical technique. A model for the DBSPR technique was developed. It is shown that the top Si film and the buried oxide layer thickness in SOI wafers can be determined by using a S-polarized He-Cd CW laser ($\lambda = 442$ nm) and a S-polarized He-Ne CW laser ($\lambda = 632.8$ nm) as the incident light source, respectively.

Chapter 3 presents a dual-beam optical modulation (DBOM) technique for determining the interface recombination velocities and substrate carrier lifetimes in thin-film SIMOX wafers. The DBOM method is successfully applied to determine the front interface (Si/SiO_2) recombination velocities and the back interface (SiO_2/Si substrate) recombination velocities and the substrate carrier lifetimes in SIMOX samples when a He-Cd CW laser ($\lambda = 442$ nm) and a He-Ne CW laser ($\lambda = 632.8$ nm) are used as the pump beam, respectively.

In Chapter 4, the investigation of implantation-condition effects on the defect formation mechanisms in the annealed SIMOX materials by using the DBSPR and DBOM techniques described in Chapter 2 and 3 is presented. Different implantation conditions such as implant energy, channeling, non-channeling, implant temperature, and implant beam current are used in the study. An etch-pit method is also employed to compare the defect density in the top silicon film with the measured interface recombination velocity. The correlation between the defect density and the recombination velocity can be used to optimize the conditions of SIMOX fabrication.

Chapter 5 presents the effects of parasitic bipolar-transistor conduction on the hot-carrier-degradation of SOI devices. An analytical model of parasitic BJT effects on the PD SOI nMOSFET is presented for correlating the hot-carrier-induced aging, and a modified lucky-electron model is developed for estimating the degradation of SOI nMOSFET characteristics. The discrepancy between floating- and unfloating-body connection in the hot-carrier-induced degradation is successfully explained by the present model. The device aging was monitored mainly by changes in threshold voltage, transconductance, and saturation current, and the corresponding degradation parameters of aged devices were extracted from the measured $I_{ds} - V_{g1}$ curves before and after stresses.

In Chapter 6, the modeling and parameter extraction of nMOS GAA transistors in linear region are presented. The non-ideal GAA MOSFET's was modeled as a parallel connection of one long-double-gate and two edge-gate transistors. Using Poisson equation which considers both the depletion charges and minority carriers, the current-voltage relationship and the expressions for the surface potential and surface electric fields were derived in the regions near and below threshold. Due to the volume inversion characteristics of the GAA devices, the surface potential at threshold is no longer pinned at the classical limit (i.e., $2\phi_F$, where ϕ_F is the Fermi

potential) of strong inversion. The models allow for the parameter extraction of low-field mobility μ_0, surface state density N_{ss}, series resistance R_s, and surface scattering parameter θ from the measured static current-voltage curves in the linear region of the GAA devices. Finally, key conclusions of this work are given in Chapter 7.

CHAPTER 2
A NEW CONTACTLESS S-POLARIZED REFLECTANCE TECHNIQUE FOR DETERMINING THE SILICON FILM AND BURIED OXIDE THICKNESS IN SILICON-ON-INSULATOR MATERIALS

2.1 Introduction

Silicon-On-Insulator (SOI) technology is becoming increasingly important for a wide variety of applications due to the many advantages of this technology such as simple isolation, capability of operating at higher temperature, higher packing density, radiation hardness, and reduction of parasitics. Nonuniformity in the thickness of top Si film and buried oxide of the SOI wafers can result in fluctuation of the threshold voltage in SOI MOSFETs. Moreover, both the Si film and buried oxide thicknesses are important parameters for modeling [9] and process control of the SOI materials and devices. The most commonly used methods for determining the SOI film thickness are reflection interference spectroscopy, ellipsometry, scanning electron microscopy (SEM), and transmission electron microscopy (TEM)techniques. Although other techniques such as threshold voltage method [10, 11] and high-frequency CV method [12] have also been applied to determine the Si film and buried oxide layer thicknesses in the processed SOI devices, these methods are performed on the finished SOI devices, and can not be considered as the nondestructive and contactless techniques for screening the film non-uniformities of the starting SOI wafers and for process monitoring. In this chapter, we report the development of a new contactless dual-beam S-polarized reflectance (DBSPR) technique for determining the film thickness on absorbing and nonabsorbing films formed on the same semiconductor substrate. The technique was applied to determine thicknesses of top Si film and buried oxide layer in SIMOX wafers. The DBSPR technique can be combined with

the dual beam optical modulation (DBOM) technique developed by us earlier [13, 14] as a nondestructive and contactless quality control tool for SOI technology.

2.2 Theory

In this section, we describe the DBSPR theory for determining the thicknesses of top Si film and buried oxide layer (BOX) in a SOI wafer using the S-polarized reflectance measurements. As shown in Fig. 2.1, an S-polarized laser beam is impinging at an angle of incidence θ_1 on the surface of a SIMOX wafer. The total reflection coefficient can be expressed as [15, 16]

$$r = \frac{r_0 + r_1 e^{-i\Delta_1} + r_2 e^{-i(\Delta_1+\Delta_2)} + r_0 r_1 r_2 e^{-i\Delta_2}}{1 + r_0 r_1 e^{-i\Delta_1} + r_0 r_2 e^{-i(\Delta_1+\Delta_2)} + r_1 r_2 e^{-i\Delta_2}} \tag{2.1}$$

where

$$\Delta_1 = \frac{4\pi}{\lambda} n_{si} t_f \cos\theta_2 \tag{2.2}$$

$$\Delta_2 = \frac{4\pi}{\lambda} n_{ox} t_{ox} \cos\theta_3 \tag{2.3}$$

where r_0, r_1 and r_2 are the Fresnel reflection coefficients at the air/Si film, Si film /buried oxide, and buried oxide/Si substrate interfaces, respectively; Δ_1 and Δ_2 are the phase changes that result from the double travel of light in the top Si film and buried oxide layer, respectively; λ is the wavelength of the incident light; t_f is the Si film thickness; t_{ox} is the buried oxide thickness; θ_2 and θ_3 are the refraction angles in the Si film and the buried oxide layer, respectively; n_{ox} is the refractive index of the buried oxide layer; n_{si} is the refractive index of Si film and $n_{si} = N_{si} - jk$, where N_{si} is the real part of the refractive index, and $k(= \frac{\alpha\lambda}{4\pi})$ is the imaginary part of the refractive index [17]; α is the optical absorption coefficient. The Fresnel reflection coefficients r_0, r_1 and r_2 are given by

$$r_0 = \frac{\cos\theta_1 - n_{si}\cos\theta_2}{\cos\theta_1 + n_{si}\cos\theta_2} \tag{2.4}$$

$$r_1 = \frac{n_{si}\cos\theta_2 - n_{ox}\cos\theta_3}{n_{si}\cos\theta_2 + n_{ox}\cos\theta_3} \tag{2.5}$$

$$r_2 = \frac{n_{ox}\cos\theta_3 - n_{si}\cos\theta_2}{n_{ox}\cos\theta_3 + n_{si}\cos\theta_2} \tag{2.6}$$

2.2.1 Measurement of Top Si Film Thickness

As shown in Fig. 2.1, to determine the thickness of top Si film in a SOI wafer, an S-polarized blue He-Cd CW laser ($\lambda = 442nm$) is used to obtain the S-polarized reflectance, and the total reflectance is measured by using a laser power meter. Equation (2.1) may be expressed as

$$r \approx \frac{r_0 + r_1 e^{-i\Delta_1}}{1 + r_0 r_1 e^{-i\Delta_1}} \tag{2.7}$$

Equation (2.7) is an approximation of Eq. (2.1) by neglecting the back reflectances (r') below the Si/buried oxide layer interface ($r \approx \frac{r_0 + r' e^{-i\Delta_1}}{1 + r_0 r' e^{-i\Delta_1}}$ with $r' \approx r_1$). Since the blue light is mainly absorbed in the top Si film ($\alpha \approx 3\text{x}10^4\ cm^{-1}$) [18], the approximation can be applied to both thick film and thin film for certain angles of incidence. For thin-film samples, Eq. (2.7) is valid over a wide range of incident angles (see Fig. 2.5). Under this approximation, the error on the measured top Si film thickness is less than 5%, as shown in Fig. 2.6(b). It is found that this technique is adequate for measuring the film thickness in semiconductor or SOI wafers with $t_f > 30nm$.

The total reflectance $R = r \cdot r^*$ (* denotes the complex conjugate) can be expressed as

$$R \approx \frac{R_0 + R_1 e^{-2b} + 2\sqrt{R_0 R_1} e^{-b}\cos(X + \delta_0 - \delta_1)}{1 + R_0 R_1 e^{-2b} + 2\sqrt{R_0 R_1} e^{-b}\cos(X - \delta_0 - \delta_1)} \tag{2.8}$$

where $X = \frac{4\pi t_f u}{\lambda}$ and $b = \frac{4\pi t_f v}{\lambda}$; u and v are given, respectively, by

$$2u^2 = N_{si}^2 - k^2 - \sin^2\theta_1 + \sqrt{(N_{si}^2 - k^2 - \sin^2\theta_1)^2 + 4N_{si}^2 k^2} \tag{2.9}$$

$$2v^2 = -N_{si}^2 + k^2 + \sin^2\theta_1 + \sqrt{(N_{si}^2 - k^2 - \sin^2\theta_1)^2 + 4N_{si}^2 k^2} \tag{2.10}$$

Note that u and v are the real and imaginary part of $n_{si}\cos\theta_2$, respectively, R_0 is the calculated reflectance at air/Si film interface; R_1 is the calculated reflectance

at Si film/buried oxide interface, and δ_0 and δ_1 are the calculated phase angles of Fresnel reflection coefficients at the interfaces of air/Si film and Si film/buried oxide, respectively.

The top Si film thickness of the SOI wafers can be determined from the DBSPR measurements using the expression given by

$$R_m - R = 0 \tag{2.11}$$

where R_m is the measured reflectance, and R is given by Eq. (2.8).

Since the blue light is mostly absorbed in the top Si film, the e^{-2b} terms in Eq. (2.8) are negligible. Thus, Eq. (2.11) can be written as

$$X + \xi + 2l\pi \pm \cos^{-1}\left(\frac{e^b(R_m - R_0)}{2\sqrt{R_0 R_1}\sqrt{A^2 + B^2}}\right) = 0, \qquad l = 0, 1, 2, 3, ... \tag{2.12}$$

where l denotes the different modes; A, B, and ξ are given by

$$A = \cos(\delta_0 - \delta_1) - R_m \cos(\delta_0 + \delta_1) \tag{2.13}$$

$$B = \sin(\delta_0 - \delta_1) + R_m \sin(\delta_0 + \delta_1) \tag{2.14}$$

$$\xi = \tan^{-1}(B/A) \tag{2.15}$$

In the DBSPR measurement system, only two parameters, namely, the film thickness t_f and the film real part refractive index N_{si}, are unknown. Thus, t_f and N_{si} can be determined from Eq. (2.12) by using the multiple angles of incidence in the measurements. In this case, Eq. (2.12) can be expressed in terms of the functions G and F as

$$G(t_f) = F(\lambda, N_{si}, \alpha, \theta_1, R_{m1}) = F(\lambda, N_{si}, \alpha, \theta_1', R_{m2}) = F(\lambda, N_{si}, \alpha, \theta_1'', R_{m3}) \tag{2.16}$$

where R_{m1}, R_{m2}, and R_{m3} are the measured reflectances at the angles of incidence θ_1, θ_1', and θ_1'', respectively. Therefore, t_f and N_{si} can be extracted from Eq. (2.16). Although different values of t_f and N_{si} are obtained from Eq. (2.16) due to the

different modes given in Eq. (2.12), only one unique solution of t_f and N_{si} will satisfy Eq. (2.16) under different incident angles, which is the sole solution of t_f and N_{si} for the SOI wafer.

As an example, the thickness of top Si film for a SIMOX wafer was measured by using this method. From Fig. 2.3(a) and (b), the reflectances R_{m1}=0.490, R_{m2}=0.485, and R_{m3}=0.640 were measured at angles of incidence θ_1=47°, θ_1'=18°, and θ_1''=57° on sample-1, respectively, and the arrows indicate the possible solutions of t_f and N_{si}. The two lines in each mode are the "+" and "−" solutions in Eq. (2.12). It is clearly shown that the value of (t_f, N_{si})=(200nm, 4.73) gives the closest cross point in both Fig. 2.3(a) and (b). Therefore, this set of (t_f, N_{si}) yields the correct values of t_f and N_{si} of the top Si film.

The multiple-angle of incidence method described above is tedious and time consuming; it is highly desirable to use a single-angle of incidence method along with numerical calculation of Eq. (2.11) to determine the Si film thickness across the entire SOI wafer. The multiple-angle step is only performed in the initial measurement to obtain the value of t_f, which is followed by the single-angle measurements over the entire wafer. This allows a quick determination of film thickness across the entire SIMOX wafer.

2.2.2 Measurement of Buried Oxide Layer Thickness

We next discuss the measurement of buried oxide thickness in SOI wafers by the DBSPR method. To determine the thickness of buried oxide layer in a SOI wafer, a red He-Ne CW laser ($\lambda = 632.8nm$) is employed to obtain the S-polarized reflectance data. Using the value of t_f obtained above, the buried oxide layer thickness t_{ox} is calculated from the following two equations

$$R_m - R_{total}(\theta_1, \lambda, t_f, t_{ox}, n_{ox}, n_{si}) = 0 \qquad (2.17)$$

and

$$R_{total}(\theta_1, \lambda, t_f, t_{ox}, n_{ox}, n_{si}) = \frac{C_1}{C_2} \tag{2.18}$$

where R_{total} is the total reflectance from the incidence of red laser beam, and

$$\begin{aligned} C_1 &= R_0\{1 + R_1^2 + 2R_1\cos(X_2 - \delta_1 - \delta_2)\} + 2R_1e^{-2b}(1 - \cos X_2) \\ &+ 2\sqrt{R_0R_1}e^{-b}\{\cos(\delta_0 - \delta_1 + X_1) + \cos(\delta_0 - \delta_1 + X_1 + X_2) \\ &+ R_1\cos(X_2 - X_1 - \delta_0 - \delta_2) + R_1\cos(X_1 + \delta_0 + \delta_1)\} \end{aligned} \tag{2.19}$$

$$\begin{aligned} C_2 &= 1 + R_1^2 + 2R_1\cos(X_2 - \delta_1 - \delta_2) + 2R_0R_1e^{-2b}(1 - \cos X_2) \\ &+ 2\sqrt{R_0R_1}e^{-b}\{\cos(X_1 - \delta_0 - \delta_1) + \cos(X_1 + X_2 - \delta_0 - \delta_2) \\ &+ R_1\cos(\delta_0 - \delta_2 - X_1 + X_2) + R_1\cos(\delta_0 - \delta_1 - X_1)\} \end{aligned} \tag{2.20}$$

where $X_1 = 4\pi t_f u/\lambda$ and $X_2 = 4\pi t_{ox}\sqrt{n_{ox}^2 - \sin^2\theta_1}/\lambda$; δ_2 is the phase angle of Fresnel reflection coefficient at the Si film/buried oxide interface. The value of t_{ox} can be determined by using the multiple-angle of incidence and Eq. (2.17).

As an example, the oxide layer thickness for a SIMOX wafer is determined using the above method. Figure 2.4 shows the measured values of R_m of 0.883, 0.896, and 0.925 at angles of incidence 32°, 41°, and 65° for sample-1, respectively. The cross point ($t_{ox} \simeq 360nm$) indicated by the arrow is the correct value of t_{ox}.

Similar to the Si film thickness measurements, the uniformity of buried oxide layer thickness in the SIMOX wafer can be determined from the measured reflectance at the angle of incidence θ_1 and the numerical solution of Eq. (2.17) using values of t_{ox} obtained from the multiple-angle reflectance measurements.

2.3 Experimental Details

Figure 2.2 shows the schematic diagram of the experimental setup for the dual-beam S-polarized reflectance technique. A 14 mW He-Cd CW laser ($\lambda = 442nm$) and

a 4 mW He-Ne CW laser ($\lambda = 632.8nm$) are used in the experiment. Both laser beams are focused to a beam size of about 2 mm diameter and polarized by the Dichroic linear polarizers (with extinction ratios of $< 1.6\text{x}10^{-4}$ for $\lambda = 442nm$ and $< 7.6\text{x}10^{-5}$ for $\lambda = 632.8nm$). The two laser beams are both reflected by half-silver coated mirrors and then focused at the same spot on the surface of the measured sample. The S-polarized reflectances are monitored by the laser power meter. Error in reflectance measurement due to the fluctuation of laser power can be reduced by monitoring the incident laser power intensity and reflected power intensity simultaneously. In the experiment, the blue laser beam ($\lambda = 442nm$) was used to determine the Si film thickness t_f and the red laser beam ($\lambda = 632.8nm$) was used to measure the buried oxide thickness t_{ox}. The multiple-angle reflectance measurement was first performed using blue laser beam, and the same procedure was then repeated using the red laser beam on the same spot of the wafer. Next, the single-angle reflectances of blue and red laser beams were measured by scanning the laser beam across the entire SIMOX wafer.

2.4 Results and Discussion

2.4.1 Measurement of Top Si Film Thickness

Si film thickness measurements were performed on both n- and p-type SIMOX wafers with different top Si film thicknesses. From Eqs. (2.12) and (2.16), we calculated the thickness t_f and the real part refractive index N_{si} of the top Si film using the measured values of R_m, θ_1, the average value of optical absorption coefficient [18] $\alpha \approx 3\text{x}10^4\ cm^{-1}$, film imaginary part refractive index [15] $k \approx 0.1055$, at $\lambda = 442nm$. The results for several SIMOX wafers are summarized in Table 2.1. For a thin-film sample, the approximation of Eq. (2.8) may produce a larger error in reflectance

data at certain angles of incidence, as shown in Fig. 2.5, but the error of film thickness is much smaller than the reflectance error, as shown in Fig. 2.6(b). From the single-angle reflectance measurements and the numerical solution of Eq. (2.11), the micro-uniformities of the top Si film thickness for different samples were obtained. The results are summarized in Table 2.3. In order to assess the accuracy of the values of t_f determined by the DBSPR technique, we compare our measured values with those determined by the conventional reflection interference spectroscopy measurements, as shown in Table 2.3. Reasonable agreement was obtained between these two methods.

Figure 2.8 shows the 3-D mapping of Si film thickness for sample-1. The average thickness is 198.8 nm and the standard deviation of thickness uniformity is about 1.5 nm. We scanned 300 points on each SIMOX wafer. Sample-2 and 3 are thick film SIMOX wafers; the uniformity of top Si film thickness for both samples is not as good as that of sample-1. Similar results on the Si film thickness uniformity across the entire SIMOX wafer were also obtained from the reflection interference spectroscopy measurements for sample-1, 2, and 3.

Figure 2.5 shows the reflectance calculated from Eqs. (2.8) and (2.1), and the measured reflectance at different angles of incidence for sample-1. The reflectance obtained from Eq. (2.8) is equal to the total reflectance at the angles of incidence of 18° and 46°. Within these equal-value angles of incidence, the measured Si film thickness has the smallest error. However, the equal-value angles of incidence are difficult to obtain if the Si film thickness is unknown. Figure 2.6(a) shows some optimal angles of incidence over a wide range of Si film thicknesses. Although a smaller error was obtained at angle 85°, a broadened beam spot on the surface of the measured samples is undesirable for the measurements. For samples with smaller film thickness, the largest error (peak-like shape) shown in Fig. 2.6(b) shifts to the smaller incident angles. Hence, the ideal angle of incidence is between 55° and 68°

over a wide range of film thicknesses.

Table 2.5 shows the statistical measurements of t_f for several SIMOX samples. Five measurements were repeated at each point. Values of the standard deviation of the measurement results indicate the excellent resolution and reproducibility of this method.

2.4.2 Measurement of Buried Oxide Thickness

Similar to the Si film thickness measurements, the buried oxide thickness can be determined from Eqs. (2.17) and (2.18) using the measured values of R_m, θ_1, t_f, the average value of absorption coefficient [18] $\alpha \approx 3.3\text{x}10^3\ cm^{-1}$, SiO_2 layer refractive index citesze $n_{ox} \approx 1.46$, Si film refractive index [15] $n_{si} \approx 3.85 - j0.015$, and $\lambda = 632.8nm$. The results for several SIMOX wafers are summarized in Table 2.2. Figure 2.6(c) shows the errors of buried oxide layer thickness as a function of incident angle by using the measured values of t_f in Eq. (2.17). The trend of errors is similar to that of film-thickness measurements. From the single-angle reflectance measurements and the numerical solution of Eq. (2.17), the micro-uniformities of buried oxide thickness for different samples were obtained. The measured buried oxide thicknesses for several SIMOX samples are listed in Table 2.4, which were found in reasonable agreement with those determined by the ellipsometry method. It is better to use larger incidence of angles, since the errors may be coupled to the measured values of t_f. Similar to t_f measurements, using larger incidence of angles may reduce the errors over a wide range of film thicknesses.

Figure 2.9 shows a 3-D mapping of the buried oxide thickness in sample-1. The average thickness is 389.1 nm and the standard deviation of thickness uniformity is 6.2 nm. We also scanned 300 points in each SIMOX wafer. Sample- 2 and 3 have the similar uniformity as sample-1. Moreover, the results of ellipsometry method also show the similar uniformity for sample- 1, 2, and 3.

Unlike Si film thickness measurement, the measurement of buried oxide thickness has no restrictions on the angles of incidence. The influence due to uncertainty of the measured reflectance in the substrate ($\Delta_2 = 2m\pi$, where $m = 0, 1, 2, 3, ...$) does not exist in this case since there are no cross points of total reflectance and the film-free reflectance at any angles of incidence, as shown in Fig. 2.7. Also, Table 2.6 shows the statistical measurements of t_{ox} for several SIMOX samples. Five measurements were repeated at each point. Similar to the results of t_f measurements, the excellent stability and reproducibility were obtained in the DBSPR method.

The discrepancy of the measured values of BOX thickness between the DBSPR and the ellipsometry methods (see Table 2.4) may be attributed to the presence of a transition layer (SiO_x) [16] between the BOX and the bulk Si substrate (see Fig. 2-10). The BOX thickness was confirmed by the SEM (e.g., t_{ox} of sample-1 measured by SEM varied between 340 nm and 360 nm as shown in Fig. 2-11) which indicated that the ellipsometry method is more accurate than the DBSPR method. The recalculated results revealed that the existence of the transition layer renders the measured BOX thickness much closer to the measurement results of ellipsometry method than that without consideration of the transition layer (e.g., the BOX thickness of sample 1 becomes 358.4 nm with a 12.5 nm transition layer presence). The total reflection coefficient (including the transition layer) may be rewritten as $r_{total} = D_1/D_2$ where D_1 and D_2 are given as follows

$$\begin{aligned} D_1 &= r_0 + r_1 e^{-i\Delta_1} + r_2 e^{-i(\Delta_1+\Delta_2)} + r_0 r_1 r_2 e^{-i\Delta_2} + r_0 r_1 r_3 e^{-i(\Delta_2+\Delta_3)} \\ &\quad + r_0 r_2 r_3 e^{-i\Delta_3} + r_1 r_2 r_3 e^{-i(\Delta_1+\Delta_3)} + r_3 e^{-i(\Delta_1+\Delta_2+\Delta_3)} \qquad (2.21) \\ D_2 &= 1 + r_0 r_1 e^{-i\Delta_1} + r_0 r_2 e^{-i(\Delta_1+\Delta_2)} + r_1 r_2 e^{-i\Delta_2} + r_1 r_3 e^{-i(\Delta_2+\Delta_3)} \\ &\quad + r_2 r_3 e^{-i\Delta_3} + r_0 r_3 e^{-i(\Delta_1+\Delta_2+\Delta_3)} + r_0 r_1 r_2 r_3 e^{-i(\Delta_1+\Delta_3)} \qquad (2.22) \end{aligned}$$

where r_2 and r_3 denote the Fresnel reflection coefficients at the BOX/transition layer and transition layer/Si substrate interfaces, respectively, and Δ_3 is the phase change

of incident light in the transition layer.

The thickness and refractive index of the transition layer can be determined by the ellipsometry measurements. The ellipsometry method [16] is to measure the phase change (Δ) and magnitude ratio (Ψ) of the polarized lights (S and P polarized). Using the measured Δ and Ψ to fit the theoretical curves of the three layer structure (i.e., Si overlayer, BOX , and transition layer), the BOX and transition layer thicknesses can be obtained. The DBSPR method can not distinguish the transition layer from the BOX. Inclusion of the transition layer reduces the sensitivity of thickness variation of top silicon film (see Figs. 2-12 and 13). From the previous report of Levy *et al.* [16], the transition layer thickness varied from 12.5 to 25 nm and the refractive index ranged from 2.4 to 3.1 for the transition layer/Si substrate interface and from 1.45 to 2.25 for the BOX/transition layer interface. The sensitivity of BOX thickness on the transition layer thickness and refractive index is shown in Figs. 2-14, 15, and 16, respectively.

2.5 Conclusion

In this work, a new contactless dual-beam S-polarized reflectance (DBSPR) technique for determining the top Si film and buried oxide thickness in the SOI wafers has been demonstrated. Basically, the limitation of the DBSPR method in the ultra-thin and thicker top Si film could be solved by using a dye laser (or multiple light source with different wavelengths) as light source. The longer wavelengths can be used in the thicker top silicon film structure. On the other hand, the shorter wavelengths can be used in the ultra-thin film structure. In principle, there is no limitations on the film thickness measurements of the two-layer structure. Except on very thin layer, the uniform optical property of the boundary between layers is not valid. In order to evaluate the DBSPR method, the advantages and disadvantages of the DBSPR, spectroscopic reflectance (SR), and spectroscopic ellipsometry (SE) methods

are compared, and the results are summarized as follows:

- Advantages:

  SE: nondestructive, quick, accurate, suitable for ultra-thin film and multiple layer structure.

  SR: nondestructive, suitable for thicker film measurements.

  DBSPR: quick, nondestructive, simultaneous determination of top Si film and BOX thicknesses, simple setup, and low cost.

- Disadvantages:

  SE: stable light source intensity control; linear detector response to avoid generation of harmonics; control of the stray light; very thin layer is questionable; thicker layer thickness measurements need multiple beams and angles of incidence.

  SR: thin film measurements need an extremely short wavelength as light source; need different incident light source scannings; detector noise.

  DBSPR: unable to be used in the samples with structure more than two layers; a very short wavelength light source is needed for measuring very thin layer.

Although the DBSPR method has some weaknesses in the film thickness measurements on SIMOX SOI wafers, it could be very suitable for use as a quality assessment tool in the bonded SOI wafer fabrication when the transition layer is absent.

Table 2.1 Measurements of Si film thickness and film real part refractive index by multiple angles of incidence for different SIMOX samples.

Sample	θ_1 (degree)	θ_1' (degree)	θ_1'' (degree)	R_{m1}	R_{m2}	R_{m3}	t_f (nm)	N_{si}
1	47	18	57	0.490	0.485	0.640	200	4.73
2	57	20	35	0.668	0.444	0.488	550	4.85
3	55	30	20	0.709	0.554	0.459	1660	4.84

Table 2.2 Measurements of buried oxide film thickness by multiple angles of incidence for different SIMOX samples.

Sample	θ_1 (degree)	θ_1' (degree)	θ_1'' (degree)	R_{m1}	R_{m2}	R_{m3}	t_{ox} (nm)
1	41	32	65	0.896	0.883	0.925	360
2	48	34	63	0.804	0.742	0.835	400
3	41	34	50	0.701	0.670	0.660	430

Table 2.3 Measured Si film thickness for different SIMOX samples.

Thickness (μm)	*Sample 1*		*Sample 2*		*Sample 3*	
Maximum	0.2048		0.5443		1.6484	
Minimum	0.1970		0.5246		1.5536	
Average	0.1988*	0.2004†	0.5389*	0.5300†	1.6162*	1.6500†
Standard Deviation	0.0015		0.0055		0.0436	

⋆ measured by S-polarized reflection method.
† measured by reflection interference spectroscopy.

Table 2.4 Measured buried oxide thickness for different SIMOX samples.

Thickness (μm)	*Sample 1*		*Sample 2*		*Sample 3*	
Maximum	0.3944		0.4032		0.4808	
Minimum	0.3629		0.3410		0.4065	
Average	0.3891*	0.3479†	0.3663*	0.3900†	0.4484*	0.3900†
Standard Deviation	0.0062		0.0127		0.0112	

⋆ measured by S-polarized reflection method.
† measured by spectroscopic ellipsometry.

Table 2.5 Statistical measurements of Si film thickness at different points of the SIMOX samples. The first point (pt. 1) is located at the center of the samples; the second and third points (pt. 2 and 3) are located, respectively, at the diagonal positions on the edge of the samples.

Thickness (μm)	*Sample 1*		*Sample MI3*		*Sample 2*	
	Average	Std.*	Average	Std.*	Average	Std.*
pt. 1	0.1970	0.0001	0.1848	0.0001	0.5421	0.0017
pt. 2	0.1971	0.0001	0.1867	0.0004	0.5440	0.0012
pt. 3	0.1971	0.0001	0.1857	0.0002	0.5411	0.0012

⋆ standard deviation.

Table 2.6 Statistical measurements of BOX layer thickness at different points of the SIMOX samples. The first point (pt. 1) is located at the center of the samples; the second and third points (pt. 2 and 3) are located, respectively, at the diagonal positions on the edge of the samples.

Thickness (μm)	*Sample 1*		*Sample MI3*		*Sample 2*	
	Average	Std.*	Average	Std.*	Average	Std.*
pt. 1	0.3689	0.0017	0.3538	0.0004	0.3610	0.0021
pt. 2	0.3742	0.0018	0.3416	0.0004	0.3849	0.0024
pt. 3	0.3634	0.0010	0.3498	0.0010	0.3931	0.0028

⋆ standard deviation.

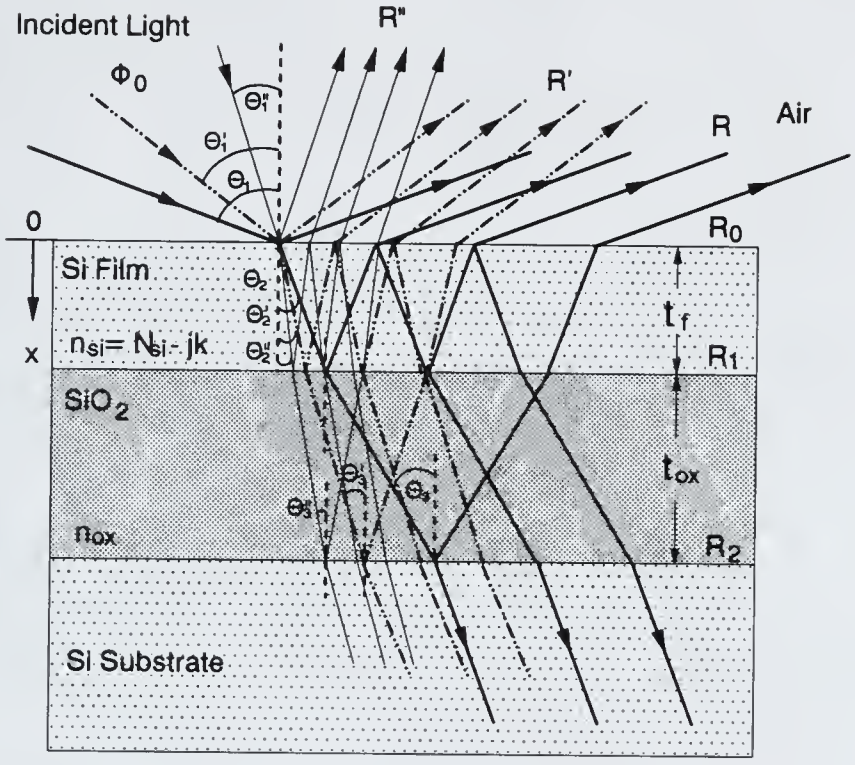

Figure 2.1: A schematic drawing of laser beams impinging on a SOI wafer under the angles of incidence at θ_1, $\theta_1^{'}$, and $\theta_1^{"}$ and the corresponding total reflectances R, $R^{'}$, and $R^{"}$; t_f is the Si film thickness; t_{ox} is the buried oxide thickness; n_{ox} and n_{si} are the refractive indices of SiO_2 layer and top Si film, respectively.

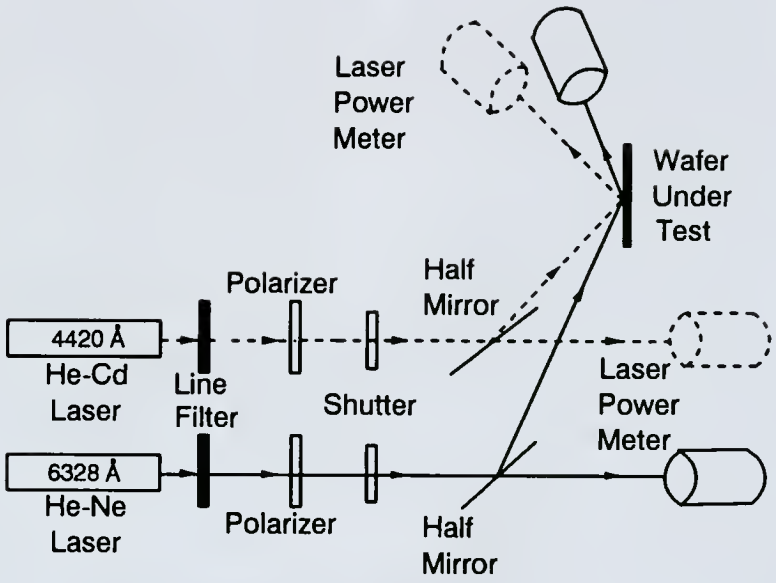

Figure 2.2: Schematic diagram for the dual-beam S-polarized reflectance measurement setup.

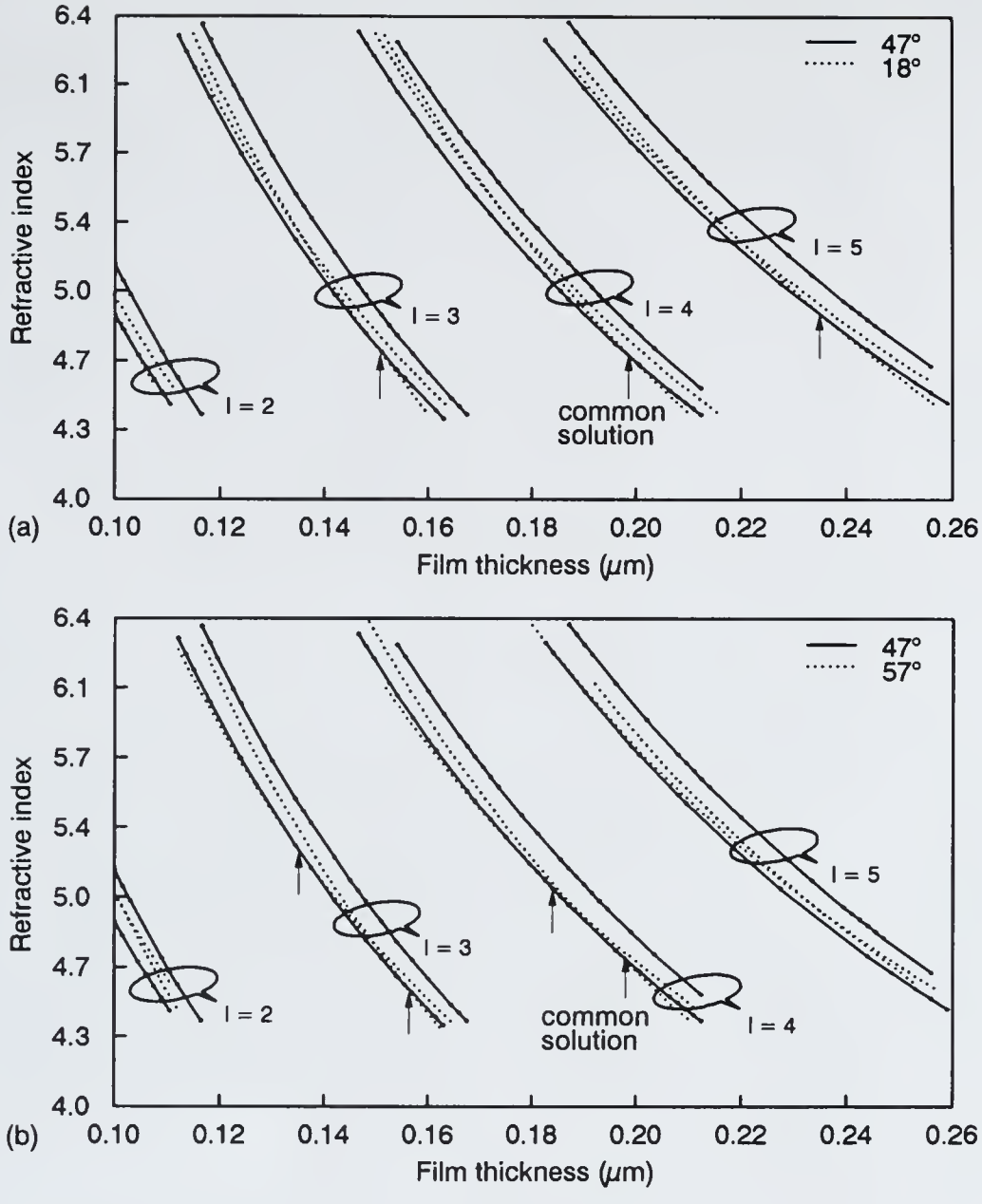

Figure 2.3: Thickness curves of the thin Si film for sample-1 under the angles of incidence (a) 47° and 18°, (b) 47° and 57°, with film real part refractive index varying from 4.3 to 6.4, l is the mode number given in Eq. (2.12).

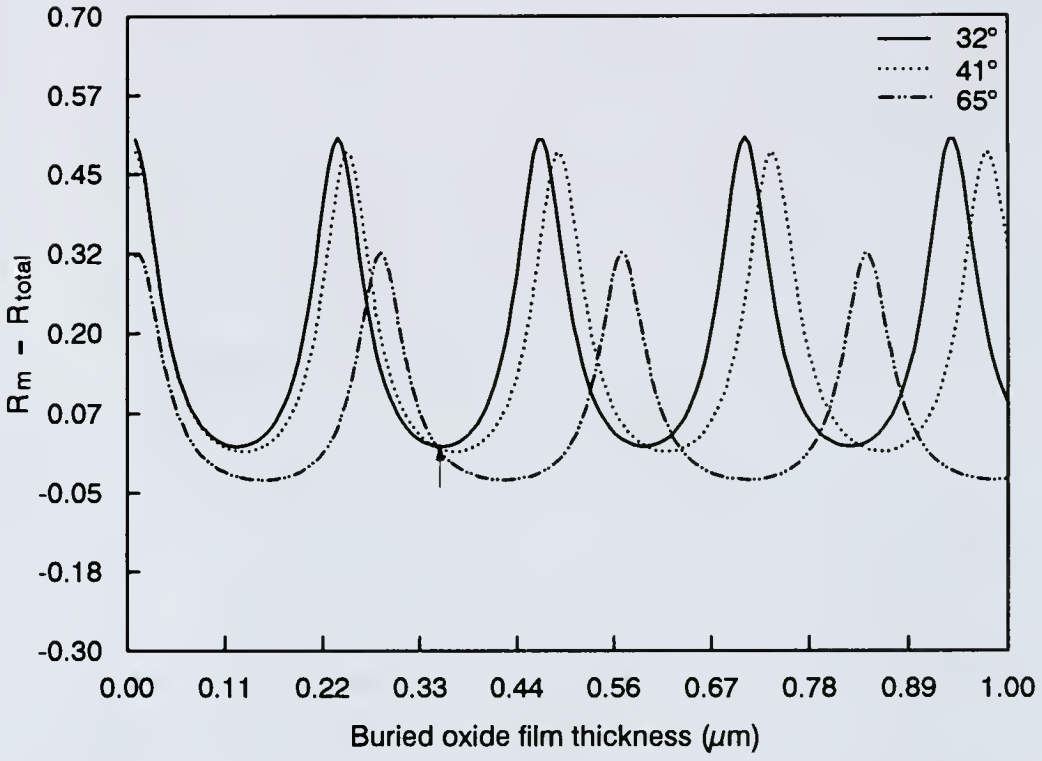

Figure 2.4: $R_m - R_{total}$ vs. buried oxide thickness t_{ox} for sample-1, which is plotted over a wide range of t_{ox} that fits Eq. (2.17) under the angles of incidence 32°, 41°, and 65°.

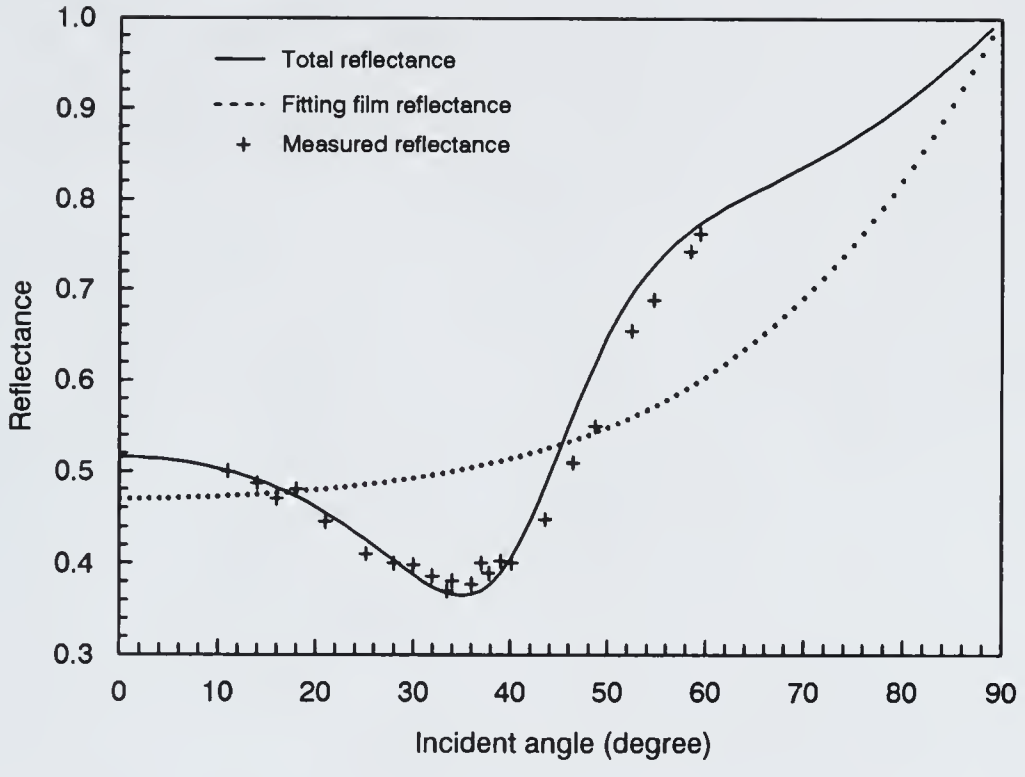

Figure 2.5: Plots of the reflectances vs. angles of incidence for sample-1; solid line is the total reflectance calculated from Eq. (2.1); dashed line is the reflectance obtained from Eq. (2.8).

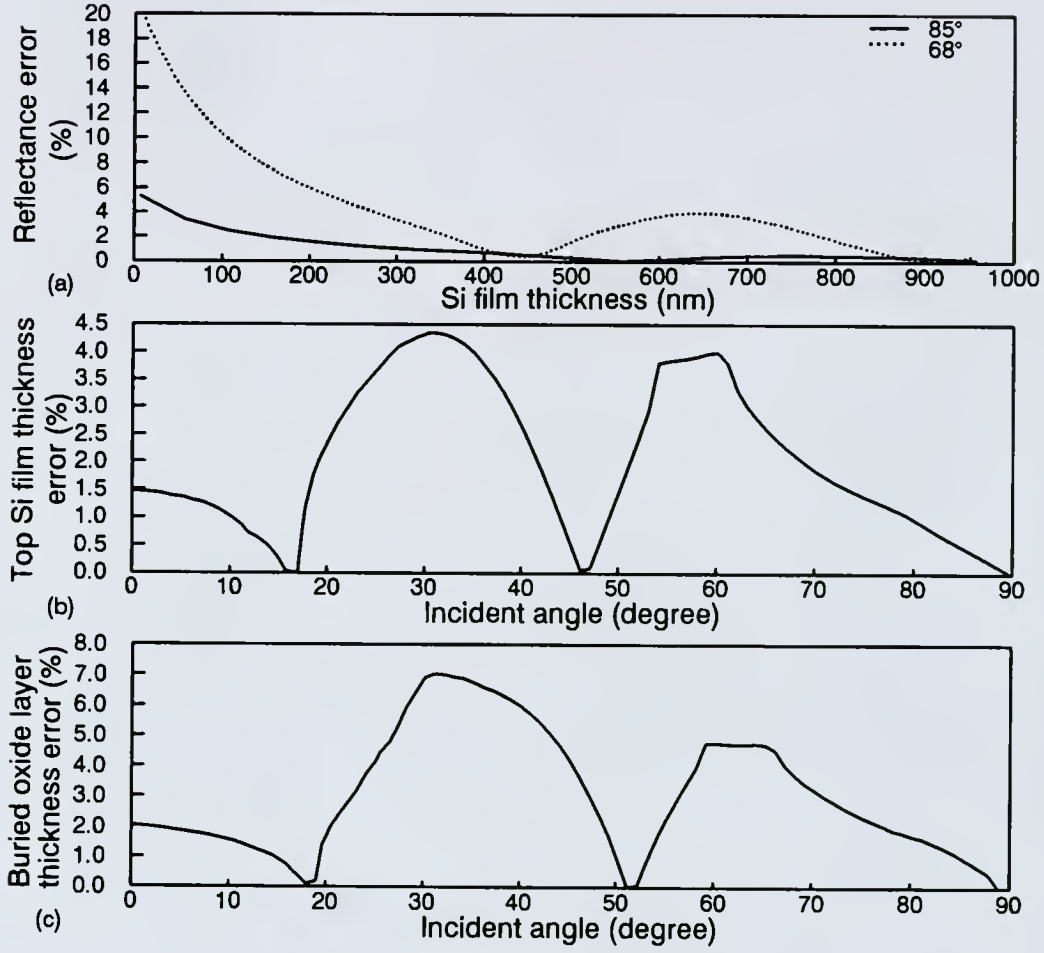

Figure 2.6: (a) Fitting errors of the reflectance obtained from Eq. (2.8) vs. Si film thickness t_f for sample-1. (b) The errors of film thickness vs. incident angle for sample-1. (c) The errors of buried oxide layer thickness vs. incident angle for sample-1.

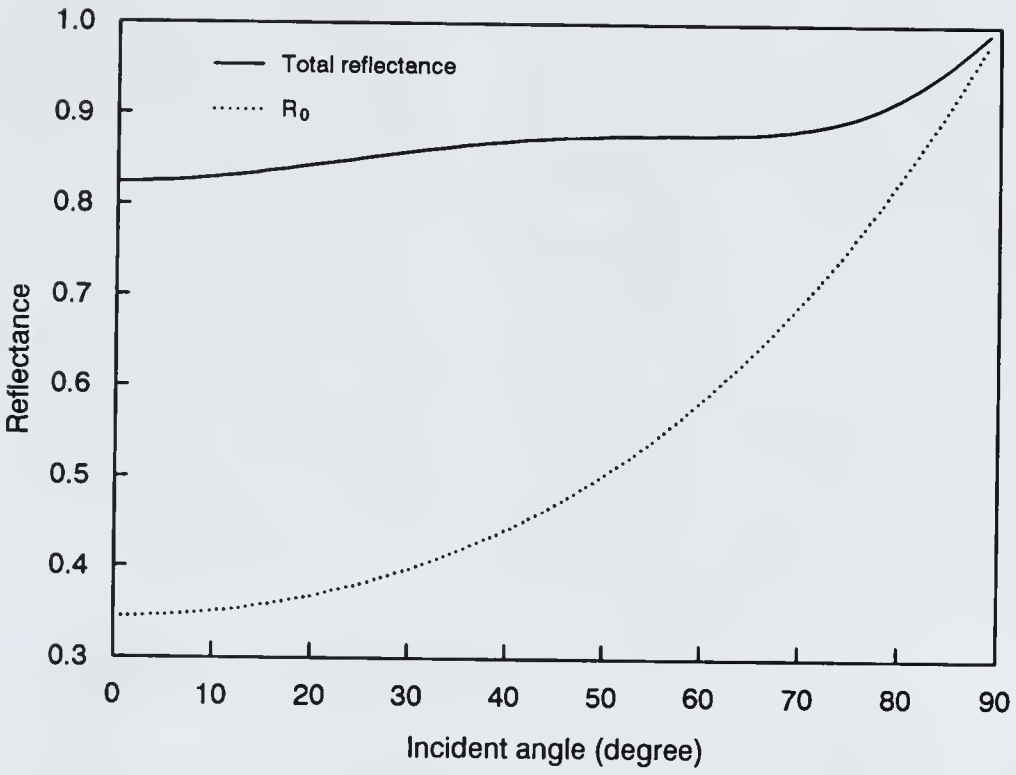

Figure 2.7: Dependence of the reflectances on the angle of incidence for sample-1; solid line is the total reflectance; dashed line is the reflectance calculated on the surface of film-free Si substrate.

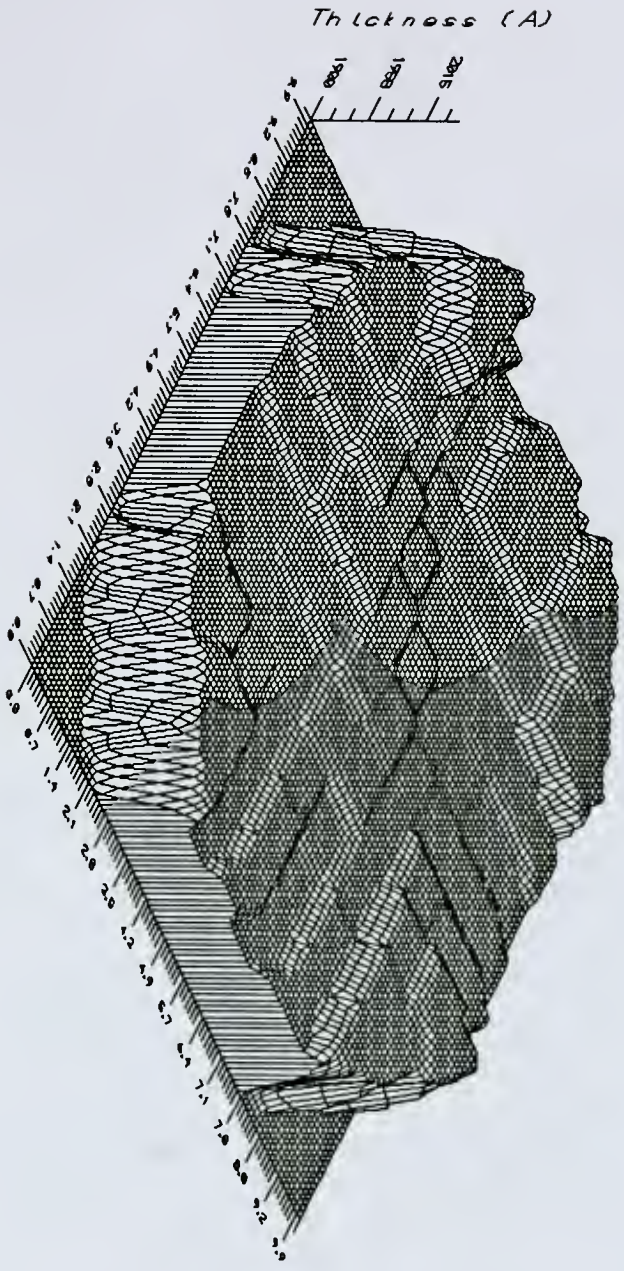

Figure 2.8: 3-D mapping of Si film thickness t_f on the surface of sample-1.

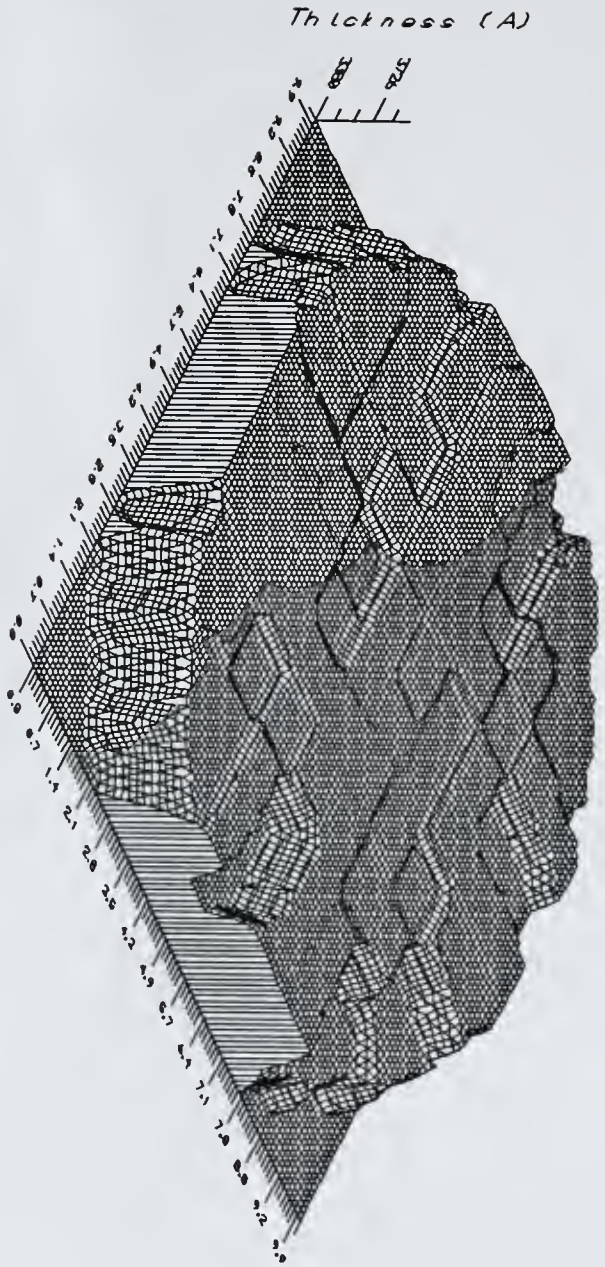

Figure 2.9: 3-D mapping of buried oxide thickness t_{ox} on the surface of sample-1.

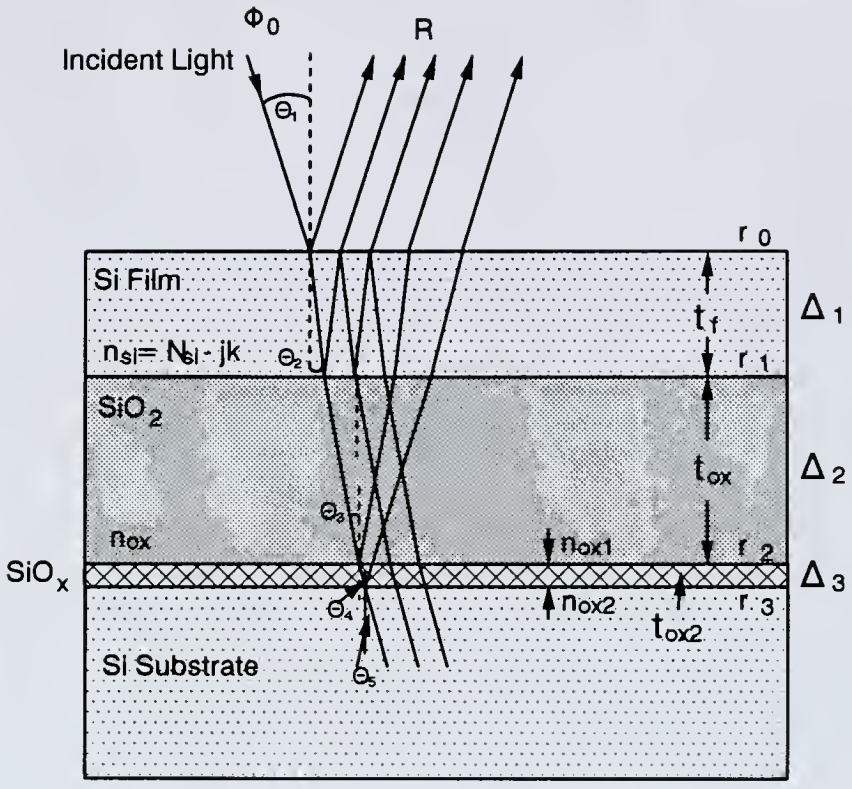

Figure 2.10: A schematic drawing of laser beams impinging on a SIMOX SOI structure with transition layer. Where t_{ox2}, n_{ox1}, n_{ox2}, and Δ_3 is the layer thickness, refractive indices, and incident light phase change of transition layer, respectively.

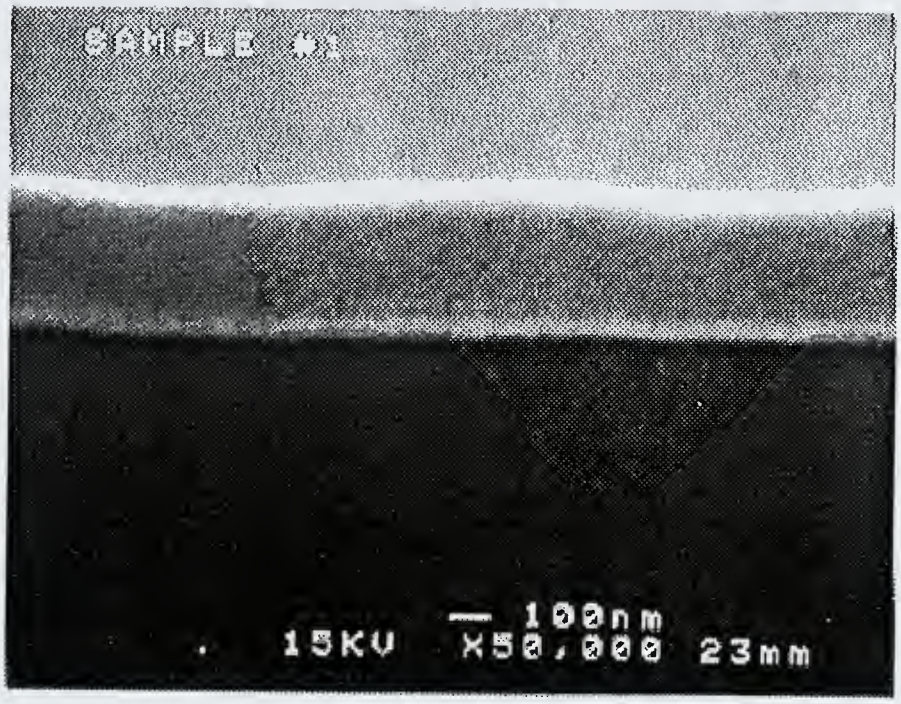

Figure 2.11: The SEM result for sample 1.

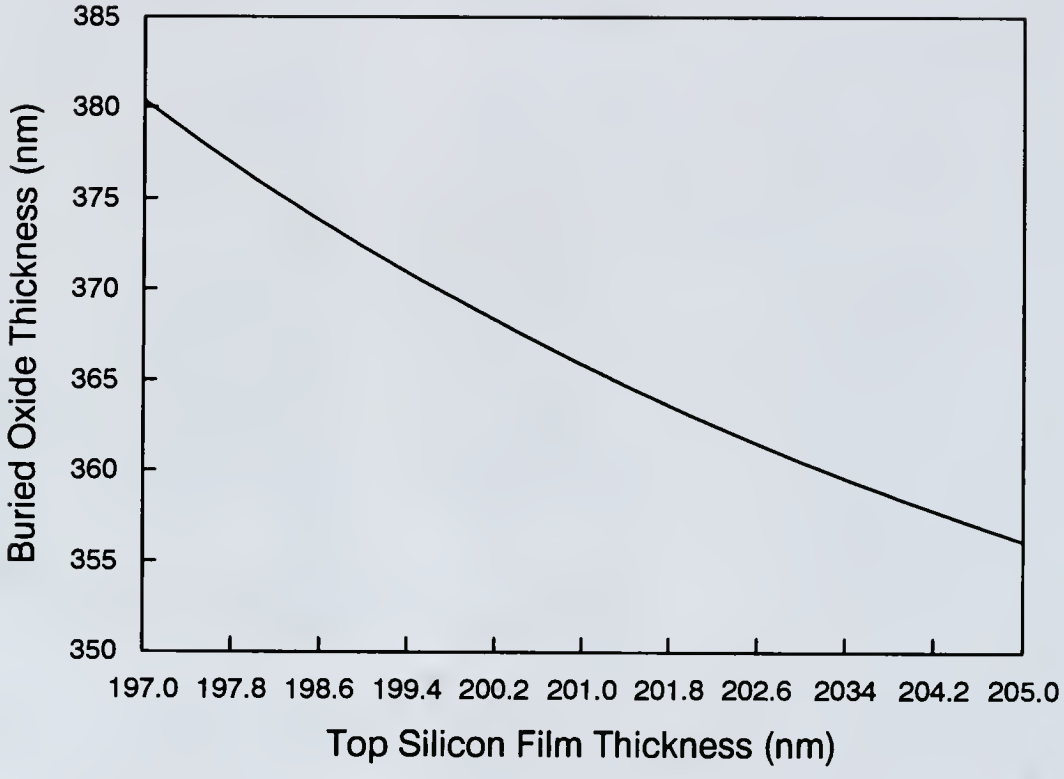

Figure 2.12: The sensitivity of t_{ox} to t_f without transition layer.

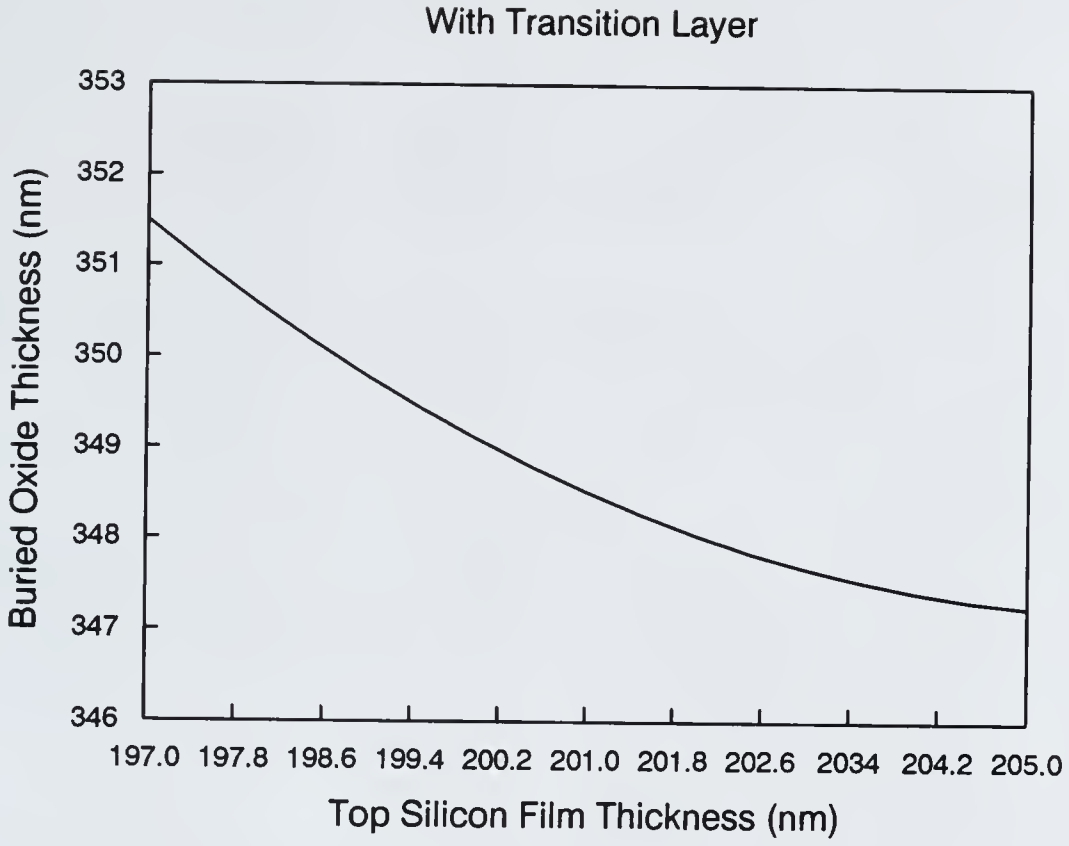

Figure 2.13: The sensitivity of t_{ox} to t_f with transition layer ($t_{ox2} = 12.5$ nm, $n_{ox2} = 2.4$, and $n_{ox1} = 2.25$).

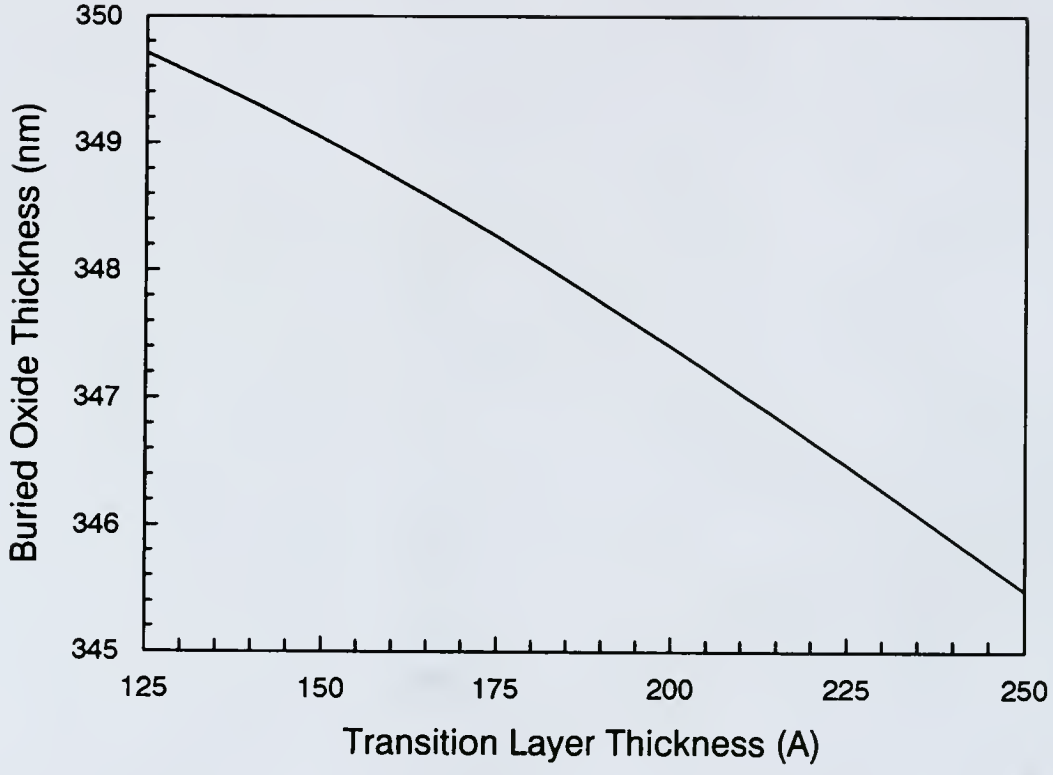

Figure 2.14: The sensitivity of t_{ox} to transition layer thickness ($n_{ox2} = 2.4$ and $n_{ox1} = 2.25$).

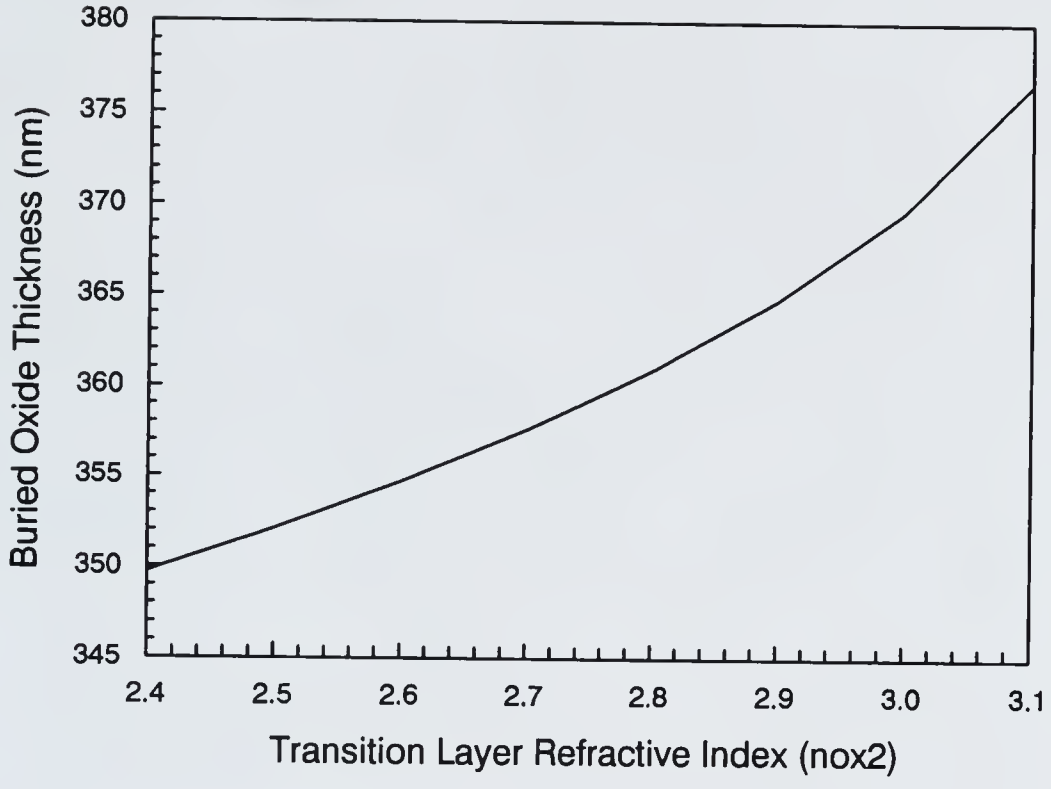

Figure 2.15: The sensitivity of t_{ox} to transition layer refractive index (n_{ox2}) ($t_{ox2} = 12.5$ nm and $n_{ox1} = 2.25$).

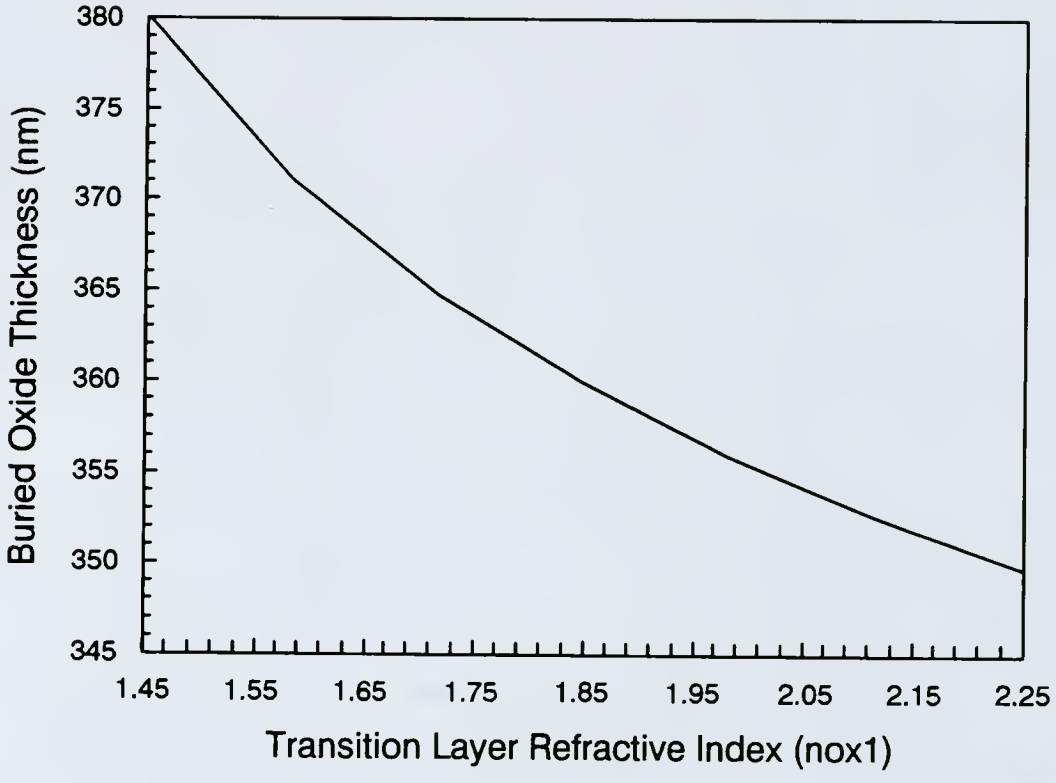

Figure 2.16: The sensitivity of t_{ox} to transition layer refractive index (n_{ox1}) ($t_{ox2} = 12.5$ nm and $n_{ox2} = 2.4$).

CHAPTER 3
DETERMINATION OF INTERFACE RECOMBINATION VELOCITIES AND CARRIER LIFETIMES IN SOI MATERIALS BY A CONTACTLESS OPTICAL MODULATION TECHNIQUE

3.1 Introduction

Recently, the development of fully-depleted (FD) SOI devices fabricated on ultra-thin SOI films has drawn great interest in SIMOX and bonded SOI wafers for high-speed ULSI applications. This is mainly due to the reduction of parasitic capacitances, body charging effects, threshold voltage, latch-up effects, soft error rate, and the lower fabrication costs of device isolation. However, several device and material problems need to be overcome before mainstream IC applications of these SOI materials can be fully realized. These include (i) floating body effects; (ii) heat dissipation through the buried oxide layer; (iii) the effects of back interface on device reliability [2]; (iv) film thickness control in FD devices [3], and (v) the necessity of low defect density, low cost ultra-thin film substrate (e.g., top Si film $< 100\ nm$). As the SOI technology enters the deep sub-micron CMOS regime, the supply voltage will be reduced below 2 V [4], the floating body effect, heat dissipation, and reliability problems become less significant. On the other hand, the fluctuation of SOI film thickness, which influences the threshold voltage, drive current, and latch-up voltage on the FD SOI devices, will have less important effect on the partially depleted (PD) devices with nonuniform channel doping and source/drain extension-halo instead [4]. One of the bottlenecks in the widespread use of the SOI technology is the availability of low defect density, low cost ultra-thin film SOI substrates. Although the optimization on ion-implantation and annealing conditions has significantly reduced the dislocation density and improved the interface property of SIMOX materials, it is highly

desirable to develop a contactless and nondestructive diagnostic technique for routine screening of the SOI wafers prior IC fabrication. Although several methods such as capacitance [19, 20], dynamic transconductance [21, 22], threshold-voltage [23], microwave lifetime measurement [24], surface photovoltage (SPV) [25], photoluminescence scanning (PL) [26], atomic force microscopy (AFM) [27], and transmission electron microscopy (TEM) [28] are available for characterization of SOI material quality, these techniques do not offer a direct means for determining the interface recombination velocities in SOI materials. In this chapter, we report a contactless dual-beam optical modulation (DBOM) technique [13, 14] for determining the substrate carrier lifetimes and interface recombination velocities in SIMOX wafers. Basically, This DBOM technique is to continue the previous works of Dr. Yang. The consideration of multiple reflection of the pump beam inside the top silicon film and the BOX layer was added into this technique. In addition, the refractive index of the pump beam inside the silicon film was corrected. Moreover, the multiple-pump-beam incidence at different oblique angles was developed for interface recombination velocity measurement. The DBOM technique can combine with the contactless dual-beam S-polarized reflectance (DBSPR) method [29] developed by us for quality control and defect study in SOI materials.

3.2 Theory for DBOM Technique

In this section, we describe the theory for determining the front-interface recombination velocity (S_2), back-interface recombination velocity (S_3), and the substrate carrier lifetime (τ_s) in a SIMOX wafer by using the DBOM technique. As shown in Fig. 3.1, a CW laser is impinging upon a p-type SOI substrate, the excess electron concentration Δn in the Si substrate can be obtained by solving the continuity

equation

$$D_n \frac{\partial^2 \Delta n}{\partial x^2} - \frac{\Delta n}{\tau} + G(x) = 0 \tag{3.1}$$

with boundary conditions given by

$$D_n \frac{\partial \Delta n}{\partial x}\bigg|_{x=0} = S_1 \Delta n(0) \tag{3.2}$$

$$-D_n \frac{\partial \Delta n}{\partial x}\bigg|_{x=t_f} = S_2 \Delta n(t_f) \tag{3.3}$$

$$D_n \frac{\partial \Delta n}{\partial x}\bigg|_{x=t_{ox}+t_f} = S_3 \Delta n(t_f + t_{ox}) \tag{3.4}$$

and the generation rate $G(x)$ can be expressed as

$$G(x) = \alpha\eta\phi_0 \cos\theta_2 (1 - R - T) e^{-\alpha x} \quad \text{in the top Si film} \tag{3.5}$$

$$G(x) = \alpha\eta\phi_0 \cos\theta_2 T e^{-\alpha(x+t_f)} \quad \text{in the Si substrate} \tag{3.6}$$

where α, η, ϕ_0, R, and T are the absorption coefficient, quantum efficiency, photon flux, total front surface reflectance, and back-interface transmittance at a given pump-beam wavelength, while, D_n, t_f, t_{ox}, τ, and S_1 are the diffusion coefficient, top Si film thickness, buried oxide (BOX) layer thickness, excess carrier lifetime, front-surface recombination velocity in the SOI wafer, respectively. Note that both R and T can be determined by using the DBSPR method [29].

The excess electron concentration in the top Si film (Δn_1) and the Si substrate (Δn_2) can be obtained by solving Eq. (3.1)

$$\Delta n_1(x) = \frac{\alpha\eta\phi_0(1 - R - T)\cos\theta_2}{D_n(\alpha^2 - \frac{1}{L_f^2})} \left(C_1 e^{\frac{x - t_f}{L_f}} + C_2 e^{-\frac{x - t_f}{L_f}} - e^{-\alpha x} \right) \tag{3.7}$$

$$\Delta n_2(x) = \frac{\alpha\eta\phi_0 T \cos\theta_2}{D_n(\alpha^2 - \frac{1}{L_S^2})} \left[\left(\frac{\alpha D_n + S_3}{\frac{D_n}{L_S} + S_3} \right) e^{-\frac{(x - (t_f + t_{ox}))}{L_s}} - e^{-\alpha(x - (t_f + t_{ox}))} \right] \tag{3.8}$$

where

$$C_1 = \frac{1}{2} \frac{(\alpha D_n + S_1)(\frac{D_n}{L_f} - S_2) - (\alpha D_n - S_2)(\frac{D_n}{L_f} + S_1) e^{-(t_f(\alpha - \frac{1}{L_f}))}}{\frac{D_n}{L_f}(S_1 + S_2)\cosh(\frac{t_f}{L_f}) + (S_1 S_2 + \frac{D_n^2}{L_f^2})\sinh(\frac{t_f}{L_f})} \tag{3.9}$$

$$C_2 = \frac{1}{2}\frac{(\alpha D_n + S_1)(\frac{D_n}{L_f} + S_2) - (\alpha D_n - S_2)(\frac{D_n}{L_f} - S_1)e^{-(t_f(\alpha+\frac{1}{L_f}))}}{\frac{D_n}{L_f}(S_1 + S_2)\cosh(\frac{t_f}{L_f}) + (S_1 S_2 + \frac{D_n^2}{L_f^2})\sinh(\frac{t_f}{L_f})} \tag{3.10}$$

where θ_2 is the refraction angle of the incident pump beam in the top Si film; $L_f = \sqrt{D_n \tau_f}$ and $L_s = \sqrt{D_n \tau_s}$ are the diffusion lengths of excess minority carriers, and τ_f and τ_s are the minority carrier lifetimes in the top Si film and the Si substrate, respectively.

When the pump beam is turned on, the excess carriers are generated in the top Si film (ΔN_1) and Si substrate (ΔN_2) which tend to modulate the IR transmitted intensity. Under low injection condition, the transmitted intensity of the probe beam, ΔN_1, and ΔN_2 can be expressed as [30]

$$\begin{aligned} I = \; & I_0 \exp\Big(\Delta N_1 \sigma_{fc} + \textstyle\int_0^{t_f} (\sigma_n n_0 + \sigma_p p_0) dx \\ & + \Delta N_2 \sigma_{fc} + \textstyle\int_{t_f + t_{ox}}^{d} (\sigma_n n_0 + \sigma_p p_0) dx\Big) \end{aligned} \tag{3.11}$$

where

$$\begin{aligned} \Delta N_1 \; = \; & \int_0^{t_f} \Delta n_1(x) dx = \frac{\alpha\eta(1 - R - T)\phi_0 \cos\theta_2}{D_n(\alpha^2 - \frac{1}{L_f^2})} \\ & \times \left[L_f C_1 (1 - e^{-\frac{t_f}{L_f}}) - L_f C_2 (1 - e^{\frac{t_f}{L_f}}) + \frac{1}{\alpha}(e^{-\alpha t_f} - 1)\right] \end{aligned} \tag{3.12}$$

and,

$$\begin{aligned} \Delta N_2 \; = \; & \int_{t_f + t_{ox}}^{d} \Delta n_2(x) dx \\ = \; & \frac{\alpha\eta\phi_0 T \cos\theta_2}{D_n(\alpha^2 - \frac{1}{L_S^2})} \left[L_s \left(\frac{\alpha D_n + S_3}{\frac{D_n}{L_S} + S_3}\right) - \frac{1}{\alpha}\right] \end{aligned} \tag{3.13}$$

where I_0, n_0, and p_0 are the transmitted intensity, electron concentration, and hole concentration in the absence of pump-beam excitation; d is the sample thickness; $\sigma_{fc} = \sigma_n + \sigma_p$ is the total optical absorption cross-section of electrons and holes with

$\sigma_n = 1 \times 10^{-18}\lambda^2\text{cm}^2$ and $\sigma_p = 2.7 \times 10^{-18}\lambda^2\text{cm}^2$ [31], respectively, and λ is the wavelength of the probe beam.

The fractional change in the probe-beam transmitted intensity $\Delta I/I$ (with $\Delta I = I - I_0$) can be expressed as

$$\begin{aligned}
\ln\left(\frac{\Delta I}{I}+1\right) &\simeq \frac{\Delta I}{I} = -\sigma_{fc}(\Delta N_1 + \Delta N_2) \\
&= -\sigma_{fc}\left\{\frac{\alpha\eta(1-R-T)\phi_0\cos\theta_2}{D_n(\alpha^2-\frac{1}{L_f^2})}\left(L_fC_1(1-e^{-\frac{t_f}{L_f}}) - L_fC_2(1-e^{\frac{t_f}{L_f}})\right.\right. \\
&+ \left.\left.\frac{1}{\alpha}(e^{-\alpha t_f}-1)\right) + \frac{\alpha\eta\phi_0 T\cos\theta_2}{D_n(\alpha^2-\frac{1}{L_S^2})}\left(L_s\frac{\alpha D_n + S_3}{\frac{D_n}{L_S}+S_3} - \frac{1}{\alpha}\right)\right\} \qquad (3.14)
\end{aligned}$$

Based on the facts that for ultra-thin Si film, with highly absorbed pump-beam ($\alpha > 4\times10^3 cm^{-1}$), low front surface recombination velocity ($S_1 \approx 10^2 cm/s$ [32]), low film carrier lifetime ($\tau_f \approx 1$ to 2 orders of magnitude smaller than bulk Si [33, 34]), and higher interface trap density in SIMOX [21, 22, 23] (about one order of magnitude higher than that of the thermally oxidized silicon [18]), the following assumptions prevail in the ultra-thin film SIMOX wafers: (i) $t_f/L_f \ll 1$, (ii) $\alpha L_f, \alpha L_s \gg 1$, (iii) $\alpha D_n \gg S_1$, (iv) $D_n^2 \gg S_1 S_2 L_f^2$, (v) $\alpha D_n \gg S_2$. Using these assumptions, Eq. (3.14) becomes

$$\begin{aligned}
\frac{\Delta I}{I} &= -\sigma_{fc}\eta\cos\theta_2\phi_0\left\{(1-R-T)\tau_f\left(\frac{\frac{t_f}{\tau_f}(1-e^{-\alpha t_f})}{(S_1+S_2)+\frac{t_f}{\tau_f}}\right)\right. \\
&+ \left. T\left(\frac{\tau_s}{\alpha}\right)\left(\frac{\alpha D_n + S_3}{D_n + S_3 L_S}\right)\right\} \qquad (3.15)
\end{aligned}$$

It should be noted that if the thickness of Si film is much smaller than the width of excess carrier distribution (e.g., $t_f \ll L_f$), the gradient of excess carrier concentration along the x direction (as shown in Fig. 3.1) due to the diffusion process is very smaller, then, Eq. (3.1) may no longer be suitable for describing the mechanism of excess carrier recombination. In Appendix A, we derived the excess carrier density

(ΔN_1) in the top Si film for ultra-thin film SOI wafer. The result is identical to the part of Si film shown in Eq. (3.15).

As shown in Fig. 3.1, to determine the front-interface recombination velocity S_2 in a SOI wafer, a He-Cd CW laser ($\lambda = 442\ nm$) is used as pump beam. Since the blue light is mainly absorbed in the Si film (see Fig. 3.3), and for an ultra-thin Si film with $S_1 + S_2 > t_f/\tau_f$ (see Fig. 3.4 and 3.5), the S_2 can be deduced by eliminating the second term in Eq. (3.15) under different incident angles θ_1 and θ_1'

$$\begin{aligned} S_1 + S_2 \approx & \left(\frac{\frac{\Delta I_1}{I_1}}{\sigma_{fc}\eta\phi_{01}\cos\theta_{21}T_1} - \frac{\frac{\Delta I_2}{I_2}}{\sigma_{fc}\eta\phi_{02}\cos\theta_{22}T_2} \right)^{-1} \\ & \times \left[t_f(1 - e^{-\alpha t_f}) \right] \left(\frac{1 - R_1 - T_1}{T_1} - \frac{1 - R_2 - T_2}{T_2} \right) \end{aligned} \tag{3.16}$$

where subscripts 1 and 2 are the measured parameters corresponding to incident angles θ_1 and θ_1', respectively. S_1 is in the order of $10^2\ cm/s$ for a well-passivated silicon surface [30, 32].

To determine the excess carrier lifetime τ_s in the SOI substrate, a He-Ne CW laser ($\lambda = 632.8\ nm$) is used as the pump beam to illuminate on the back surface of the SOI wafer. Since the reflectance R_r of a not well-passivated silicon surface can be determined by the known rms values of surface slopes m and surface roughness σ [35] and Si substrate of SOI wafer, the fractional change of the transmitted probe-beam intensity can be expressed as

$$\frac{\Delta I}{I} = \sigma_{fc}\eta\phi_0\cos\theta_2(1 - R_r)\left[\frac{\tau_s}{\alpha} \left(\frac{\alpha D_n + S_r}{D_n + S_r L_S} \right) \right] \tag{3.17}$$

and the substrate lifetime τ_s is obtained from Eq. (3.17) using the back surface recombination velocity of $S_r \approx 6 \times 10^4 cm/s$ [36]

$$\tau_s = \left(\frac{A + \sqrt{A^2 + 4\frac{\sqrt{D_n}}{S_r}A}}{2} \right)^2 \tag{3.18}$$

where

$$A = \left(\frac{\frac{\Delta I}{I}}{\sigma_{fc}\eta\phi_0 \cos\theta_2(1-R_r)} \right) \frac{S_r\alpha\sqrt{D_n}}{\alpha D_n + S_r} \tag{3.19}$$

Similar to the determination of S_2, the back-interface recombination velocity S_3 is obtained by measuring τ_s and using a He-Ne laser ($\lambda = 632.8\ nm$) as pump beam. Since the He-Ne laser is mainly absorbed in the Si substrate (see Fig. 3.3). The S_3 can be determined from Eq. (3.15) under different incident angles

$$S_3 = \frac{(K-\alpha)D_n}{1 - L_s K} \tag{3.20}$$

where

$$\begin{aligned} K &= \left(\frac{\frac{\Delta I_1}{I_1}}{\sigma_{fc}\eta\phi_{01}\cos\theta_{21}(1-R_1-T_1)} - \frac{\frac{\Delta I_2}{I_2}}{\sigma_{fc}\eta\phi_{02}\cos\theta_{22}(1-R_2-T_2)} \right) \\ &\times \frac{\alpha}{\tau_s}\left(\frac{T_1}{1-R_1-T_1)} - \frac{T_2}{1-R_2-T_2} \right)^{-1} \end{aligned} \tag{3.21}$$

where subscripts 1 and 2 are the measured parameters corresponding to incident angles θ_1 and θ_1', respectively. Note that the above analysis can be applied to n-type SOI wafers as well provided that the parameters for electrons are replaced by holes (i.e., D_n by D_p and τ_n by τ_p etc.).

3.3 Experimental Details

Figure 3.2 shows the schematic diagram of the DBOM experimental setup. A tungsten lamp, which is used as the probe beam, is passing through an IR filter (a low-doped Si wafer) with a cutoff wavelength of about 1.1 μm, and is focused to a beam size of about 4 mm diameter. A 14 mW He-Cd CW laser or a 4 mW He-Ne CW laser was used as the pump beam which is lined up with the probe beam in the experiment. Both laser beams are focused to a spot size of about 2 mm diameter and polarized by the Dichroic linear polarizers (with extinction ratios of $< 1.6\text{x}10^{-4}$ for $\lambda = 442\ nm$ and $< 7.6\text{x}10^{-5}$ for $\lambda = 632.8\ nm$). Both probe beam and pump beam are

chopped at 405 Hz for synchronous detection by a lock-in amplifier. The pump beam is reflected by half-silver coated mirrors and then focused into the same spot as the probe beam on the measured sample. In the experiment, the substrate carrier lifetime τ_s was measured by using an IR probe beam and a He-Ne laser pump beam impinging on the back surface of the SIMOX wafer. The rms values of the surface slope m and the surface roughness σ were measured by using Sloan Dektak II surface profiler to obtain the reflectance. The IR transmitted beam intensity I was first measured using the chopped probe beam and a lock-in amplifier. The change in the transmitted intensity ΔI was measured by using the chopped pump beam superimposed on the probe beam which was not chopped, and the resulting IR transmitted intensity was measured by using a lock-in amplifier.

To determine the back-interface recombination velocity S_3, the probe and pump beams were impinging on the front surface of the measured sample with the different oblique incident angles of the pump-beam excitation. The measurements of I and ΔI are the same as in the determination of τ_s. Values of R were measured by using a laser power meter. For different angles of pump-beam excitation, the measurements of I, ΔI, and R are carried out in a similar procedure.

The front interface recombination velocity S_2 was determined by using the He-Cd laser as pump beam and using the same procedures as described above. The S-polarized reflectances of pump beam were monitored by a laser power meter to determine the front surface reflectance R and the back-interface transmittance T of the SIMOX wafer.

3.4 Results and Discussion

3.4.1 Measurement of Front Interface Recombination Velocity

Front interface recombination velocity measurements were carried out in both n- and p-type SIMOX wafers with different top Si film thicknesses, annealing temperatures, and oxygen implant doses. From Eq. (3.16) and the values of R and T obtained by the DBSPR method [29], we calculated the front interface recombination velocity using the measured values of ΔI, I at the angles of incidence $\theta_1 = 23°$ and $\theta_1' = 63°$, the average value of optical absorption coefficient $\alpha \approx 3 \times 10^4\ cm^{-1}$ [18], $\sigma_{fc} \approx 9.5 \times 10^{-18}\ cm^2$ [31], $\eta \approx 0.5$ [18], $\phi_0 \approx 7.48 \times 10^{17}\ cm^{-2}s^{-1}$ at $\theta_1 = 23°$, and $\phi_0 \approx 4.62 \times 10^{17}\ cm^{-2}s^{-1}$ at $\theta_1' = 63°$. The results for several SIMOX wafers are summarized in Table 3.1. From the results, it is noted that the multiple implant sample has a larger defect density in the front interface than that of the single implant sample . This is consistent with previous work reported by Venables *et al.* [37].

For a thick-film ($t_f > 5000\mathring{A}$) SIMOX wafer with small film lifetime ($\tau_f < 0.3\mu s$), Eq. (3.16) may not give a good estimation of the front-interface recombination velocity, as shown in Fig. 3.4 and 3.5. Under such condition, a shorter wavelength pump beam (e.g., UV laser) can be employed to obtain the film lifetime (τ_f). The front-interface recombination velocity can be determined by substituting this measured τ_f into Eq. (3.15) and using the blue He-Cd laser as a pump beam and using different incident angles (e.g. θ_1 and θ_1') [13].

Figure 3.6 shows the mapping profile of the interface recombination velocities ($S_1 + S_2$) for sample-MI3. The average value is 325 cm/s. For a well passivated silicon surface [30, 32] S_1 is about 100 cm/s, while S_2 was found to be $225cm/s$. We scanned 300 points on each SIMOX wafer and divided the 4" SIMOX wafer into 60 squares in the DBOM measurements. Thus, the area of each square represents the average value of five measurements. From Fig. 3.6, it is shown that the uniformity of

front-interface recombination velocities in sample-MI3 is lower near the center region than the upper edge region of the wafer. Sample-MI1 and SI2 have the similar results as sample-MI3.

3.4.2 Measurement of Substrate Lifetimes

The substrate lifetimes were determined from Eqs. (3.17), (3.18), and (3.19) using the measured values of m, σ, ΔI, I, the average value of optical absorption coefficient $\alpha \approx 4.1 \times 10^3\ cm^{-1}$ [18], $\sigma_{fc} \approx 9.5 \times 10^{-18}\ cm^2$ [31], $\eta \approx 0.85$ [18], and $\phi_0 \approx 4.02 \times 10^{17}\ cm^{-2}s^{-1}$ at $\theta_1 = 23°$. Values of R_r in Eq. (3.17) were calculated using Eqs. (27) and (39) given in Davies' report [35] with the measured values of m and σ. The results of the calculated R_r are listed in Table 3.2. The measured substrate lifetimes for several SIMOX wafers are summarized in Table 3.1. Sample-SI has a lower τ_s than other SIMOX samples tested. This may be due to the heavy metal impurity introduced in this SIMOX wafer during the single oxygen implantation process. The heavy metal impurities are gettering in the Si substrate during the post implantation annealing [38, 39]. The gettering impurities degrade the substrate lifetime.

Figure 3.7 shows the mapping profile of the substrate lifetimes for sample-MI3. The average value is 10.8 μs. We also scanned 300 points on each SIMOX wafer. From Fig. 3.7, a uniform distribution of substrate lifetime was observed and the lifetimes are higher near the center region than the edge region of the wafer. Sample-MI1 and SI2 have similar uniformity profiles as sample-MI3.

3.4.3 Measurement of Back Interface Recombination Velocity

Similar to the front-interface recombination velocity measurements, the back-interface recombination velocity can be determined from Eqs. (3.20) and (3.21) using the measured values of τ_s, ΔI, I, the average value of optical absorption coefficient $\alpha \approx 4.1 \times 10^3\ cm^{-1}$ [18], $\sigma_{fc} \approx 9.5 \times 10^{-18}\ cm^2$ [31], $\eta \approx 0.85$ [18], $\phi_0 \approx 4.02 \times 10^{17}$

$cm^{-2}s^{-1}$ at $\theta_1 = 23°$, and $\phi_0 \approx 9.96 \times 10^{16}\ cm^{-2}s^{-1}$ at $\theta_1' = 63°$. Values of R and T in Eq. (3.21) were obtained from the DBSPR method [29]. The results for several SIMOX wafers are summarized in Table 3.1. It is noted that sample-SI1 has a higher back-interface recombination velocities than other SIMOX samples. This may be attributed to the post-implantation annealing induced by the copper diffusion from the Si surface into the buried oxide and Si substrate, with copper impurities precipitated in the back interface (e.g. intrinsic gettering) [38, 39] of the SIMOX wafer.

Figure 3.8 displays the mapping profile of the back interface recombination velocities for sample-MI3. The average value is 59.8 cm/s. We also scanned 300 points on each SIMOX wafer. From Fig. 3.8, the back-interface recombination velocities are lower near the central region than in the edge region of the wafer.

Finally, the statistical measurements of τ_s, S_3 ,and $S_1 + S_2$ were performed on the different points for several SIMOX samples (see from Table 3.3 through Table 3.5). Five measurements were repeated at each point. Values of the standard deviation of the measurement results indicate the excellent stability and reproducibility of the DBOM method. The determined τ_s, S_3, and S_1 maybe sensitive to temperature, back-side surface roughness, top Si film thickness, or BOX thickness. From the calculation results, τ_s is not much sensitive to temperature, backside roughness, and rough surface recombination velocity (see Figs. 3-9, 10, and 11). While, the back-interface recombination velocity is sensitive to temperature and BOX thickness (see Figs. 3-12, 13, and 14). For the front-interface recombination velocity, the measured values are more sensitive to t_f than to t_{ox} (see Figs. 3-15 and 16).

3.5 Conclusion

In this work, a contactless dual beam optical modulation (DBOM) technique for determining the front-and back-interface recombination velocities and the substrate

carrier lifetimes in SIMOX wafers has been demonstrated. For ultra-thin film, the limitations are (i) $\tau_f > 10^{-9}$ sec, (ii) $\tau_s > 10^{-11}$ sec, and (iii) interface recombination velocity smaller than 10^5 cm/sec. In general, τ_f varies from 0.1 to a few μs, and $\tau_s > \tau_f$ [33, 34]. The interface recombination is ranged from several tens to hundreds of cm/sec [21, 22, 23] ($s = \sigma v_{th} \pi k T D_{it}$ [75] where D_{it} is the density of interface states). The most commonly used methods to determine the carrier lifetimes are the photocoductivity and the SPV methods. While, the interface recombination velocity is usually determined by capacitance and conductance techniques [19]-[23]. The advantages and disadvantages for the photoconductivity decay, SPV (surface photovoltage), and DBOM techniques are described as follows:

- Advantages:

  Photoconductivity decay: traditional method; simple.

  SPV: nondestructive; sample preparation is simple; steady-state method; immune to slow trapping and detrapping.

  DBOM: contactless and nondestructive; simple for sample preparation; steady-state method; suitable for thin-film structure measurements.

- Disadvantages:

  Photoconductivity: thicker samples (at least several μm) to decouple surface and bulk recombination; contact necessary; and transient method.

  SPV: contact method; sample thickness needs much thicker than the diffusion length; SCR (space charge region) width must be smaller than the diffusion length; stray capacitance must be controlled for good signal-to-noise ratio.

  DBOM: sensitive to the variation of top silicon film thickness and the BOX thickness.

This method is especially useful for quality control and defect studies of the SOI wafer manufacturing. Using this technique, the interface properties and the quality

of SOI wafers can be evaluated versus processing and growth parameters. Thus, the contactless DBOM technique described in this work may be used to obtain optimal manufacturing process for the SOI materials.

Table 3.1 Substrate lifetimes, front-interface recombination velocities, and back-interface recombination velocities measured by DBOM method for several SIMOX samples.

Sample	t_f (Å)	t_{ox} (Å)	Dose (cm^{-2})	Anneal (°C, h)	Resistivity (type, Ω-cm)	τ_s (μs)	$S_1 + S_2$ ($cm \cdot s^{-1}$)	S_3 ($cm \cdot s^{-1}$)
MI1†	2004	3479	1.8E18	1310, 5	p,10-20	23.26	174.40	44.70
SI2	5300	3900	1.8E18	1285, 6	n, 6	7.39	242.63	95.99
MI3†	1870	3744	1.8E18	1285, 6	p 10-20	10.79	324.87	59.79

† multiple implant wafer with doses of 0.5, 0.5,0.8 $\times 10^{18}$ cm^{-2}.

Table 3.2 Measured reflectance R_r of the back surface for different SIMOX samples.

Sample	m	$\frac{\sigma}{\lambda^*}$	$R_r^\dagger$
MI1	0.0456	0.3557	0.2371
SI2	0.0460	0.3311	0.2371
MI3	0.0495	0.3454	0.2371

$* \lambda = 6328 \mathring{A}$ is the wavelength of the incident pump beam.

† $R_r = R_0 \times R_{rel}$ where R_0 is the reflectance of a well passivated Si surface, and R_{rel} is the relative reflectance [35] obtained from the measured m and σ.

Table 3.3 Statistical measurements of substrate lifetimes at different points of the SIMOX samples. The first point (pt. 1) is located at the center of the samples; the second and third points (pt. 2 and 3) are located, respectively, at the diagonal positions on the edge of the samples.

τ_s (μs)	*Sample 1*		*Sample MI3*		*Sample 2*	
	Average	Std.*	Average	Std.*	Average	Std.*
pt. 1	33.98	0.11	11.84	0.017	9.97	0.018
pt. 2	32.91	0.19	12.40	0.045	5.73	0.018
pt. 3	21.47	0.27	11.74	0.051	5.83	0.012

⋆ standard deviation.

Table 3.4 Statistical measurements of back-interface recombination velocities at different points of the SIMOX samples. The first point (pt. 1) is located at the center of the samples; the second and third points (pt. 2 and 3) are located, respectively, at the diagonal positions on the edge of the samples.

S_3 (cm/s)	*Sample 1*		*Sample MI3*		*Sample 2*	
	Average	Std.*	Average	Std.*	Average	Std.*
pt. 1	58.62	1.11	52.86	1.01	96.85	3.56
pt. 2	48.45	1.52	57.75	1.04	106.50	3.79
pt. 3	48.51	1.24	46.87	1.50	115.05	4.05

⋆ standard deviation.

Table 3.5 Statistical measurements of front-interface recombination velocities at different points of the SIMOX samples. The first point (pt. 1) is located at the center of the samples; the second and third points (pt. 2 and 3) are located, respectively, at the diagonal positions on the edge of the samples.

$S_1 + S_2$ (cm/s)	*Sample 1*		*Sample MI3*		*Sample 2*	
	Average	Std.*	Average	Std.*	Average	Std.*
pt. 1	154.84	3.55	278.94	7.14	222.50	7.85
pt. 2	176.02	3.53	318.51	8.21	251.50	8.71
pt. 3	197.22	5.64	322.44	8.14	247.82	6.73

⋆ standard deviation.

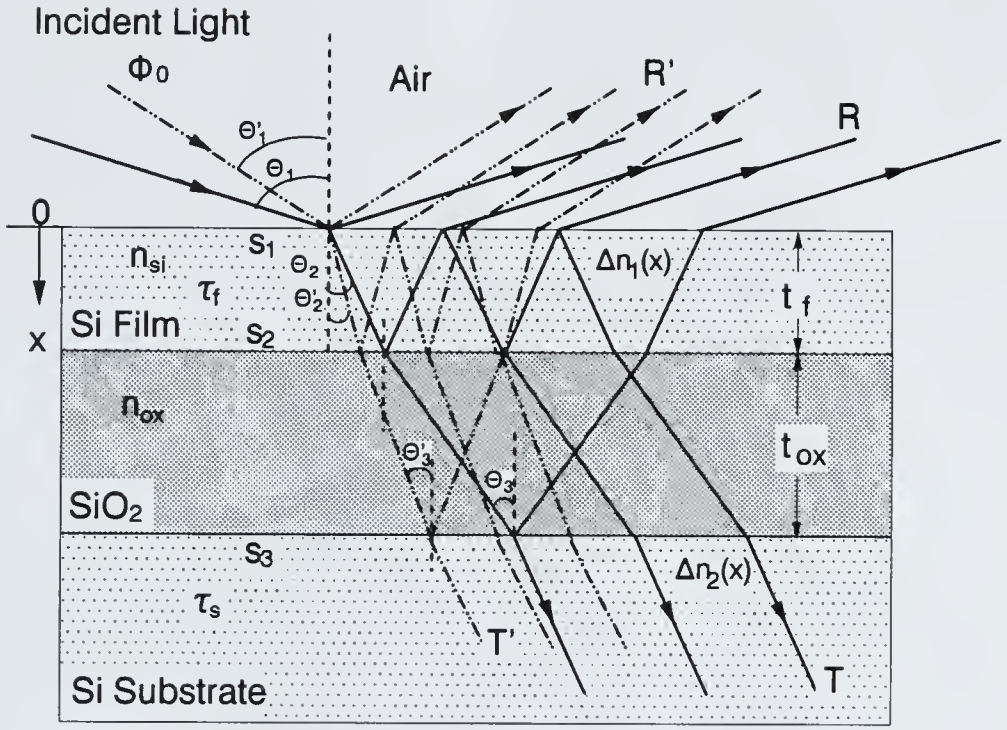

Figure 3.1: A schematic diagram of pump beams impinging on a SOI wafer under different angles of incidence at θ_1 and θ_1' and the corresponding total reflectances R and R', transmittances T and T'; t_f is the Si film thickness; t_{ox} is the buried oxide thickness; n_{ox} and n_{si} are the refractive indices of SiO_2 layer and top Si film, respectively; S_1, S_2, τ_f, and $\Delta n_1(x)$ are the recombination velocities, minority carrier lifetime, and minority excess carrier concentration in the top Si film, respectively; S_3, τ_s, and $\Delta n_2(x)$ are the recombination velocities, minority carrier lifetime, and minority excess carrier concentration in the Si substrate, respectively.

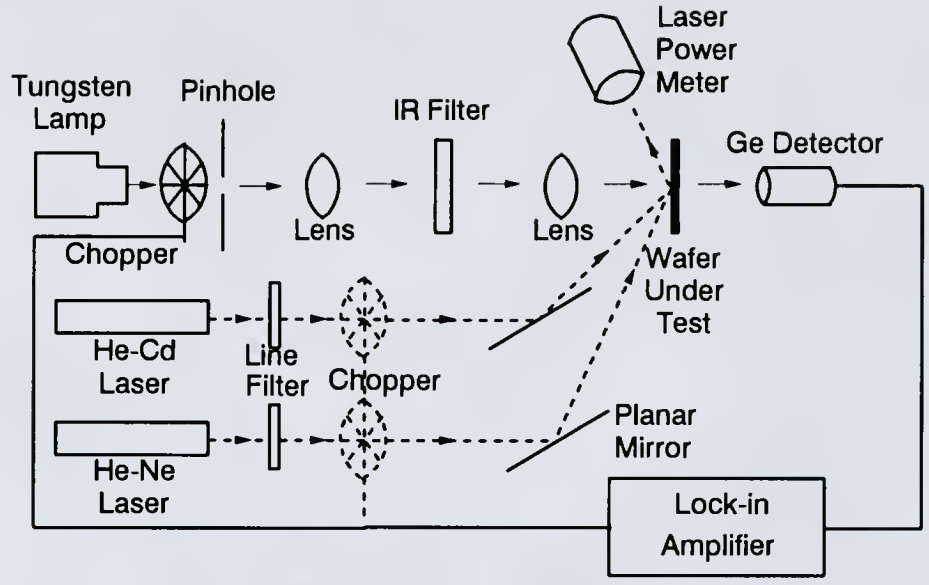

Figure 3.2: Schematic diagram for the contactless dual-beam optical modulation (DBOM) experimental setup.

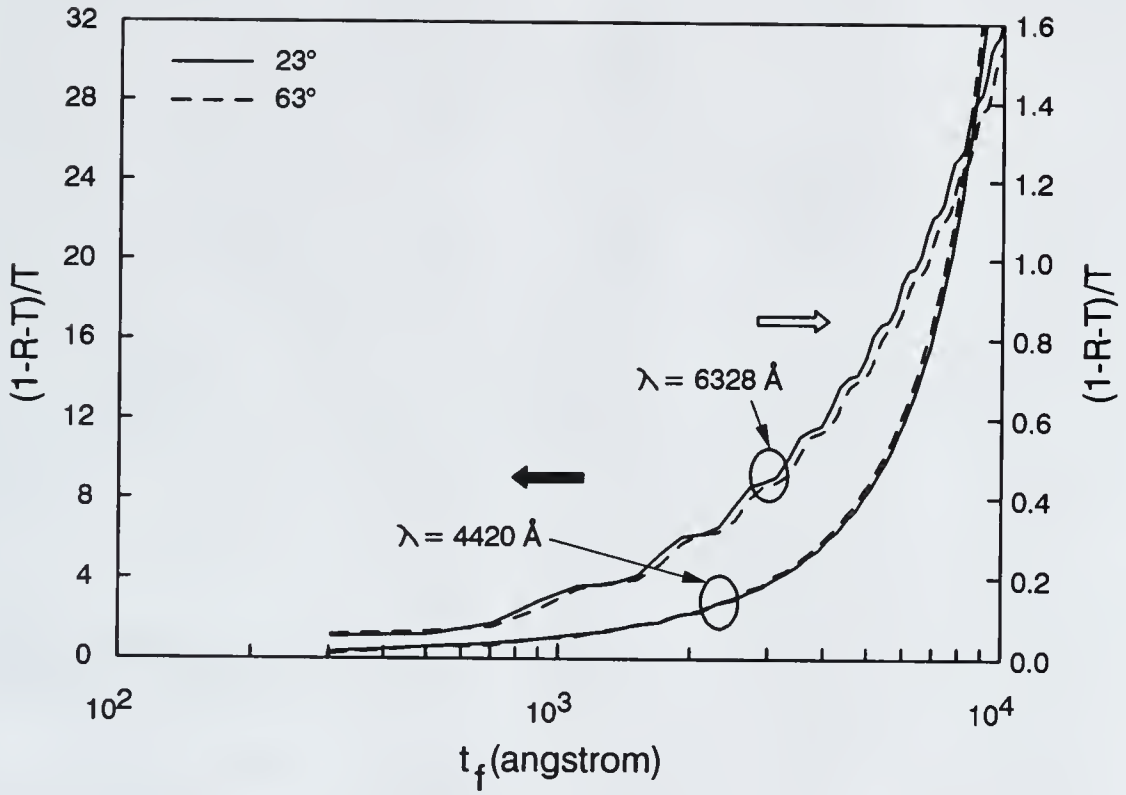

Figure 3.3: Ratio of the absorption of pump beam in top Si film to Si substrate vs. top Si film thickness under different incident angles.

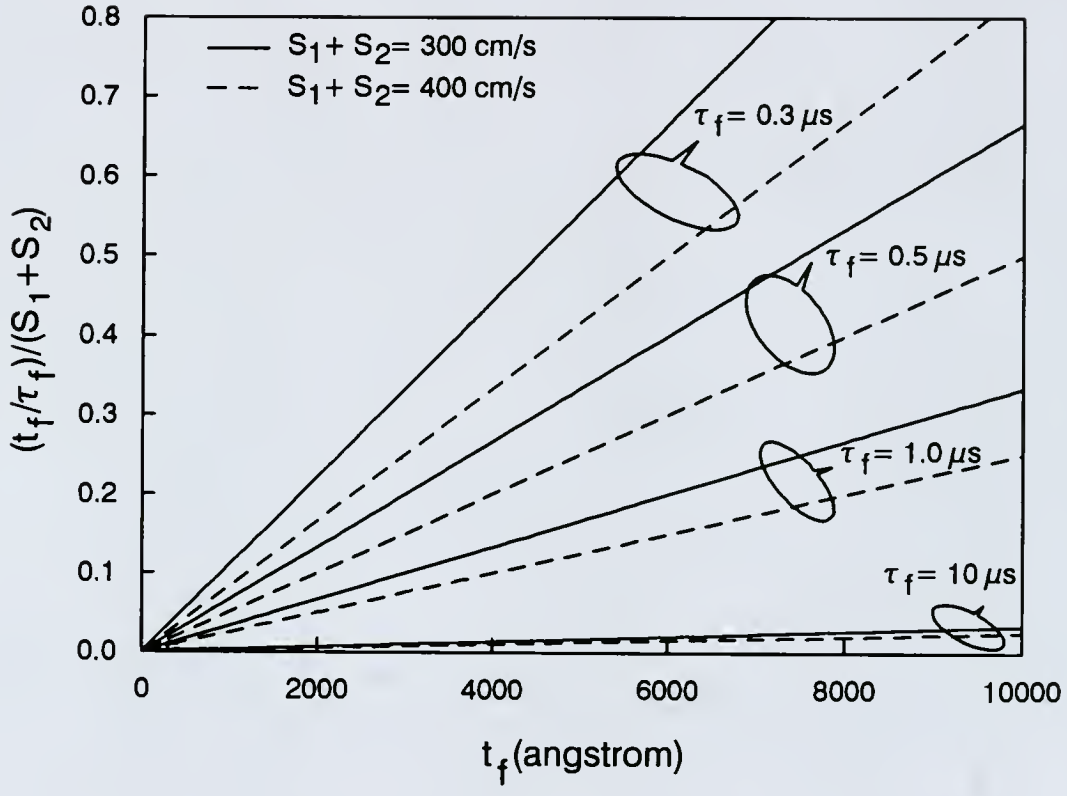

Figure 3.4: Ratio of $(t_f/\tau_f)/(S_1 + S_2)$ in Eq. (3.15) for different top Si film thicknesses and film lifetimes with $S_1 + S_2 = 300$ and 400 cm/s.

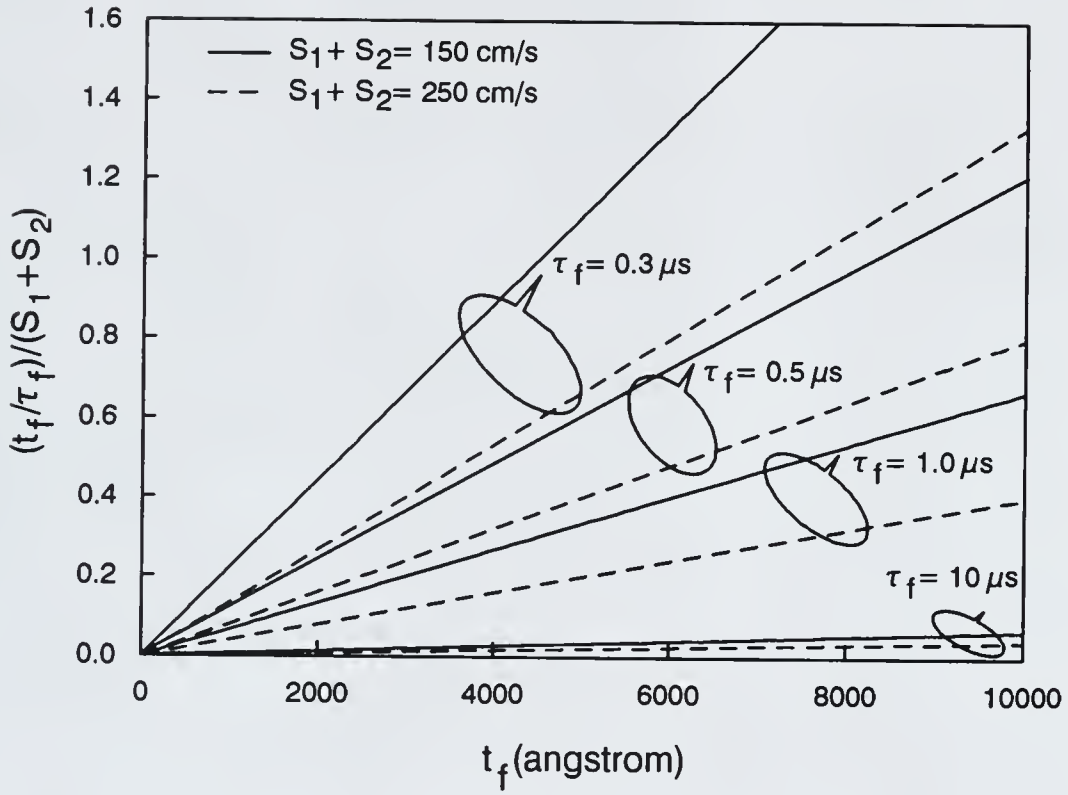

Figure 3.5: Ratio of $(t_f/\tau_f)/(S_1 + S_2)$ in Eq. (3.15) for different top Si film thicknesses and film lifetimes with $S_1 + S_2 = 150$ and 250 cm/s.

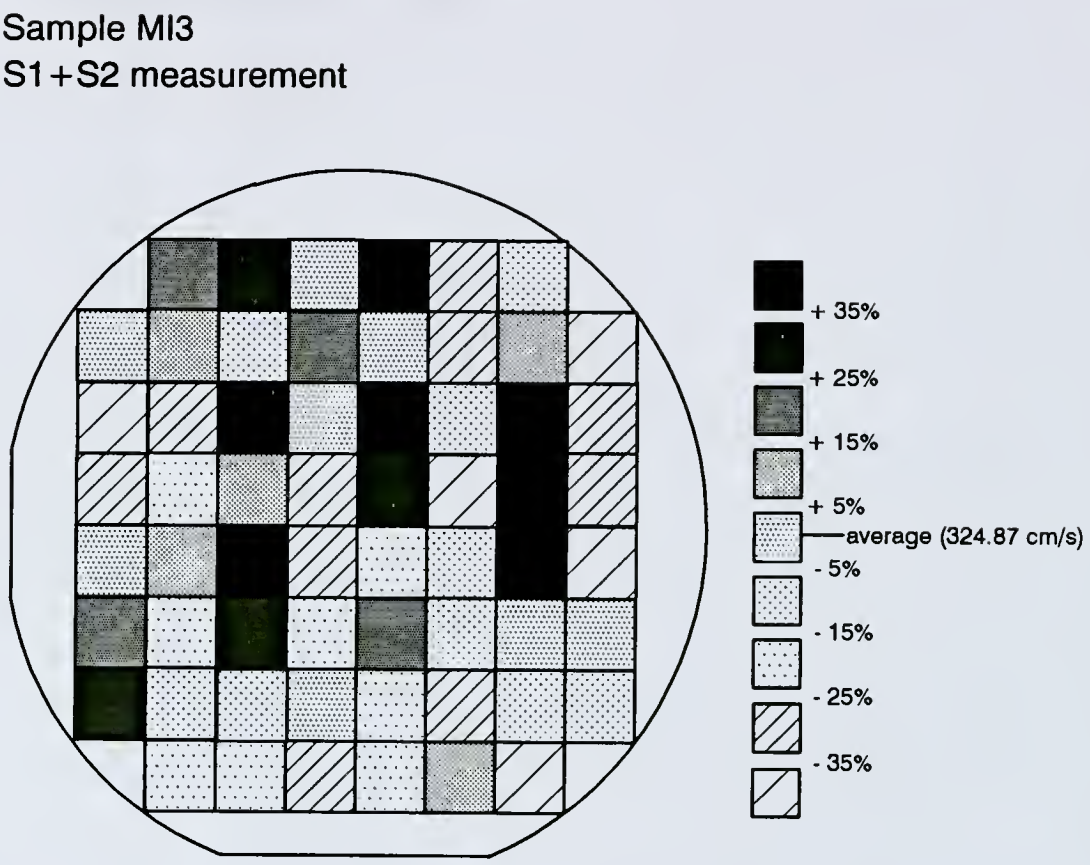

Figure 3.6: Mapping of the front interface recombination velocities $S_1 + S_2$ for sample-MI3.

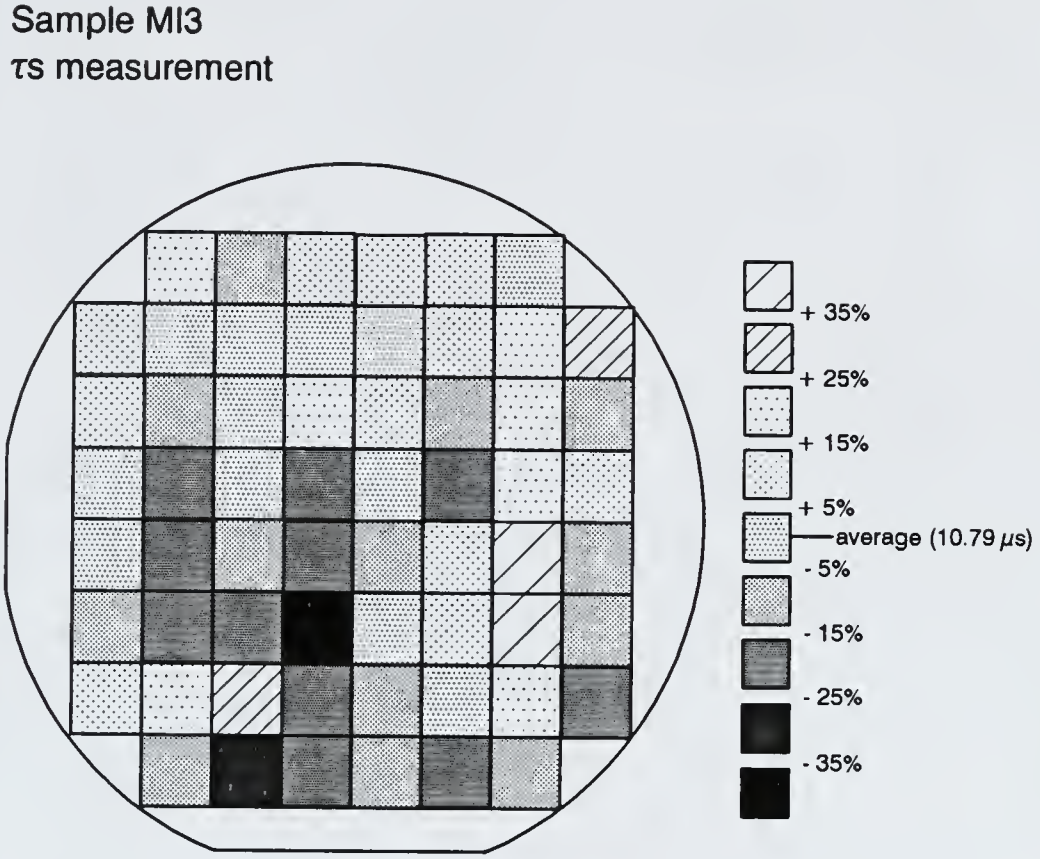

Figure 3.7: Mapping of the substrate lifetimes τ_s for sample-MI3.

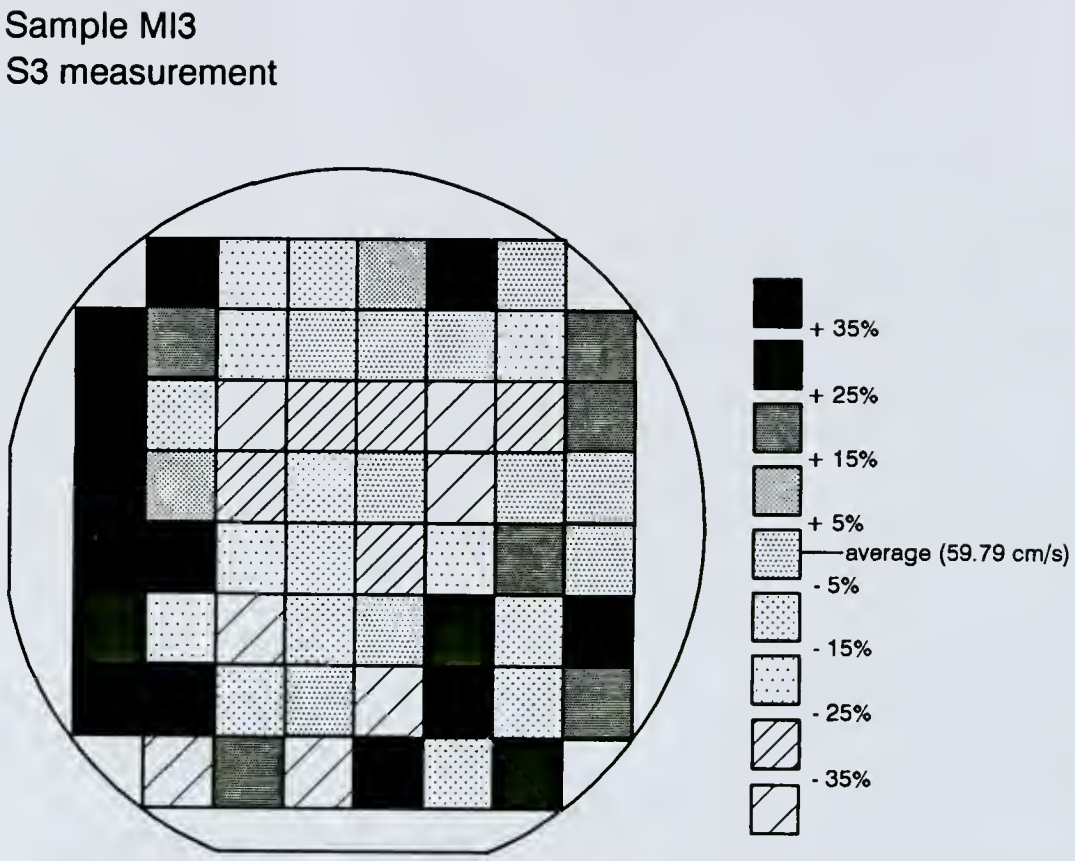

Figure 3.8: Mapping of the back interface recombination velocities S_3 for sample-MI3.

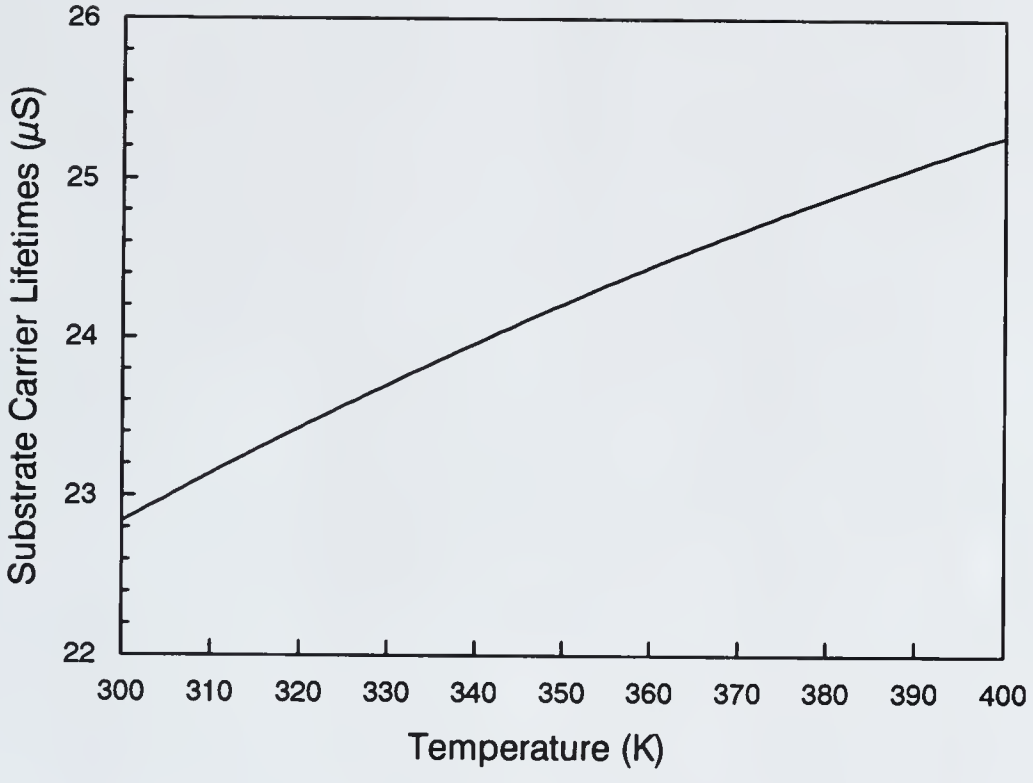

Figure 3.9: The sensitivity of substrate carrier lifetimes to temperature.

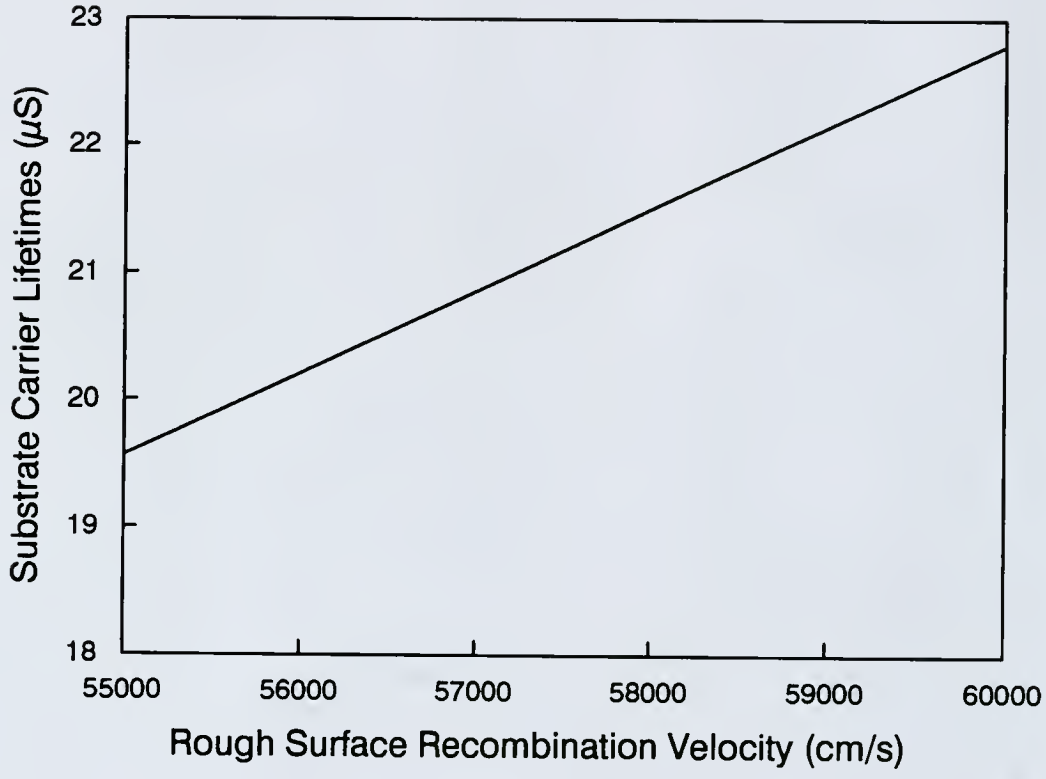

Figure 3.10: The sensitivity of substrate carrier lifetimes to S_r of the rough back side of measured wafer.

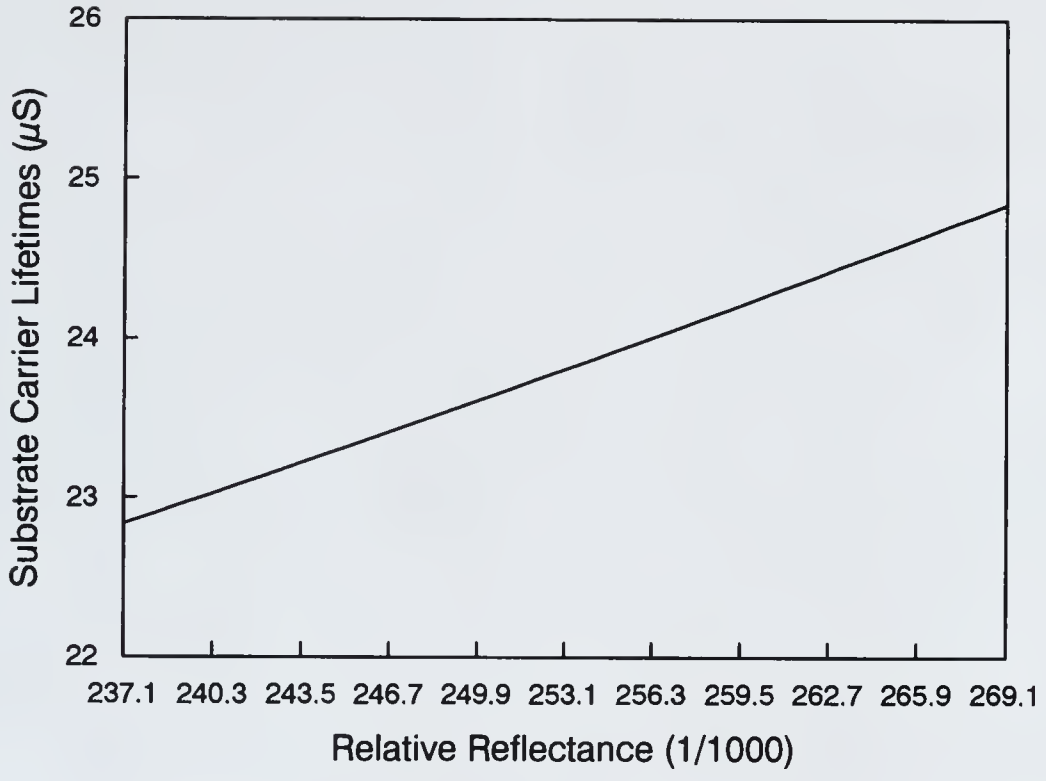

Figure 3.11: The sensitivity of substrate carrier lifetimes to relative reflectance of the rough back side of measured wafer.

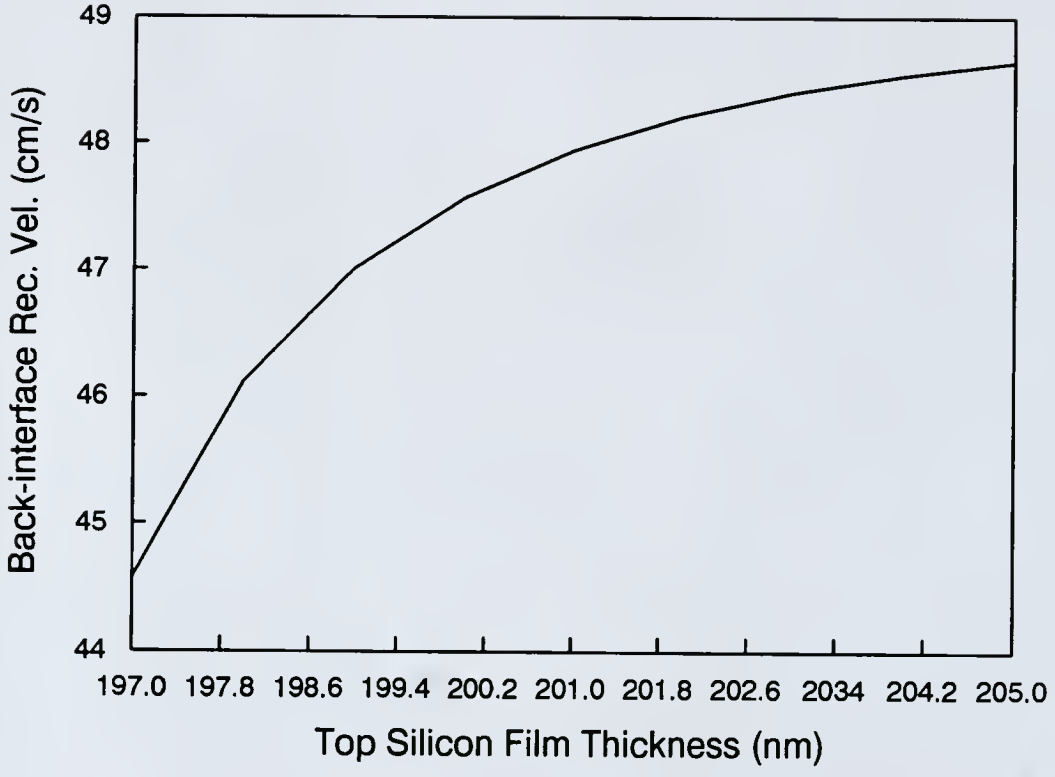

Figure 3.12: The sensitivity of back-interface recombination velocity to t_f.

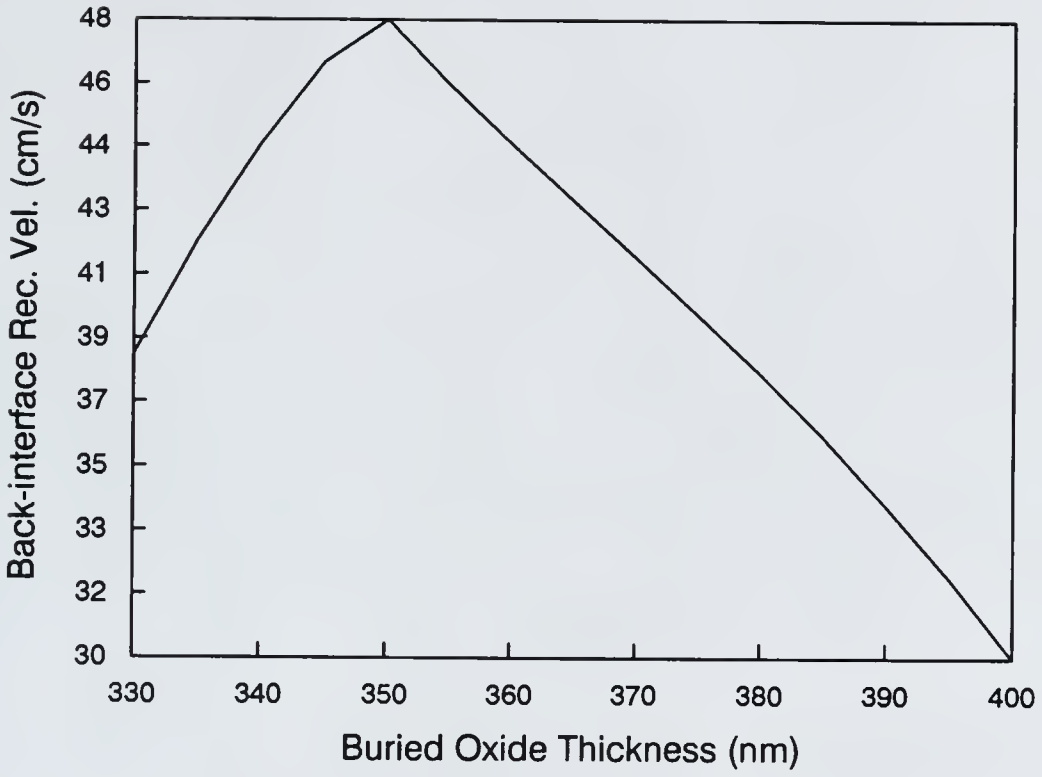

Figure 3.13: The sensitivity of back-interface recombination velocity to t_{ox}.

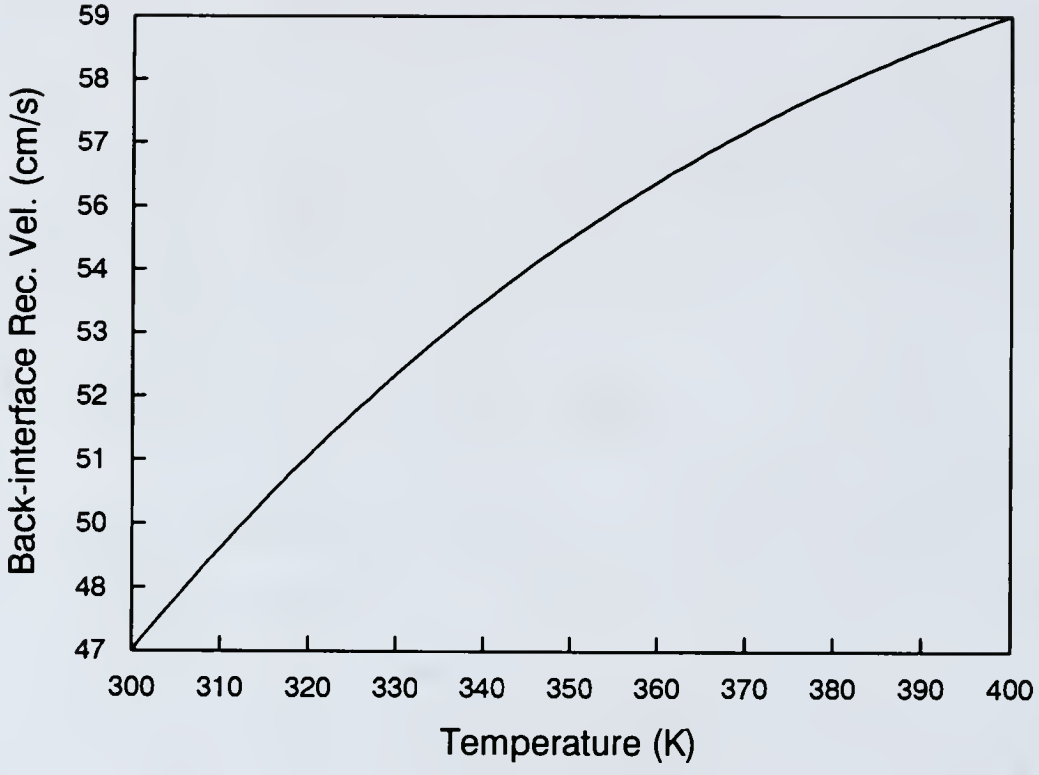

Figure 3.14: The sensitivity of back-interface recombination velocity to temperature.

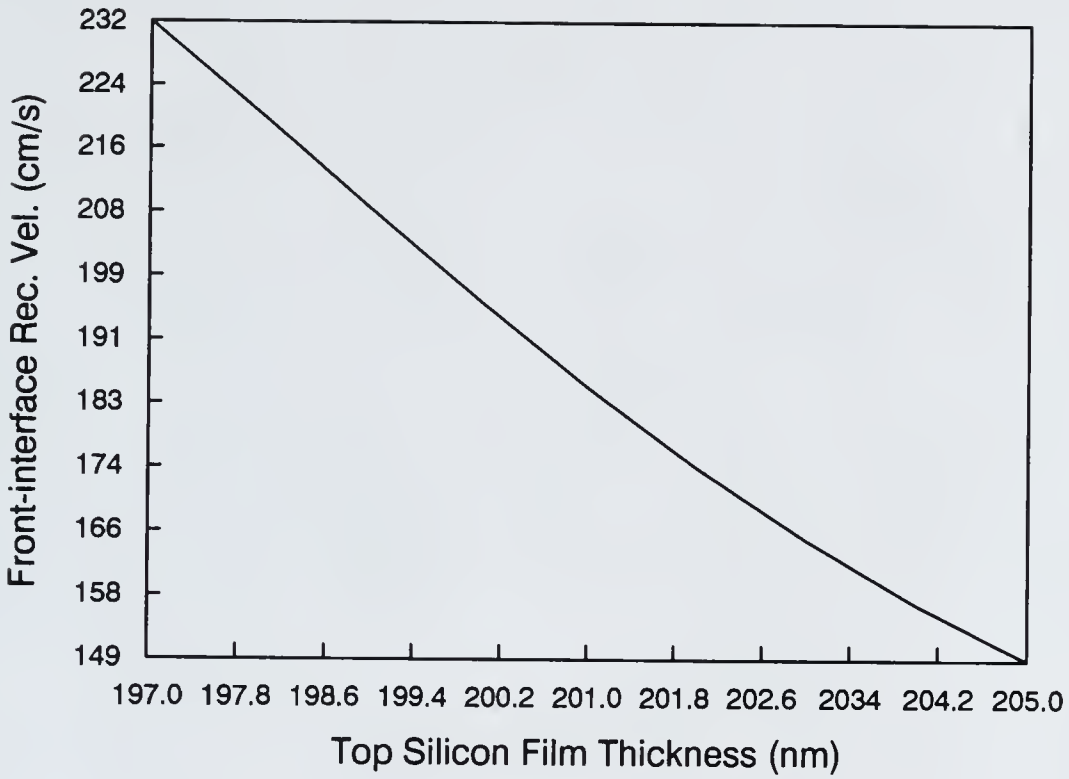

Figure 3.15: The sensitivity of front-interface recombination velocity to t_f.

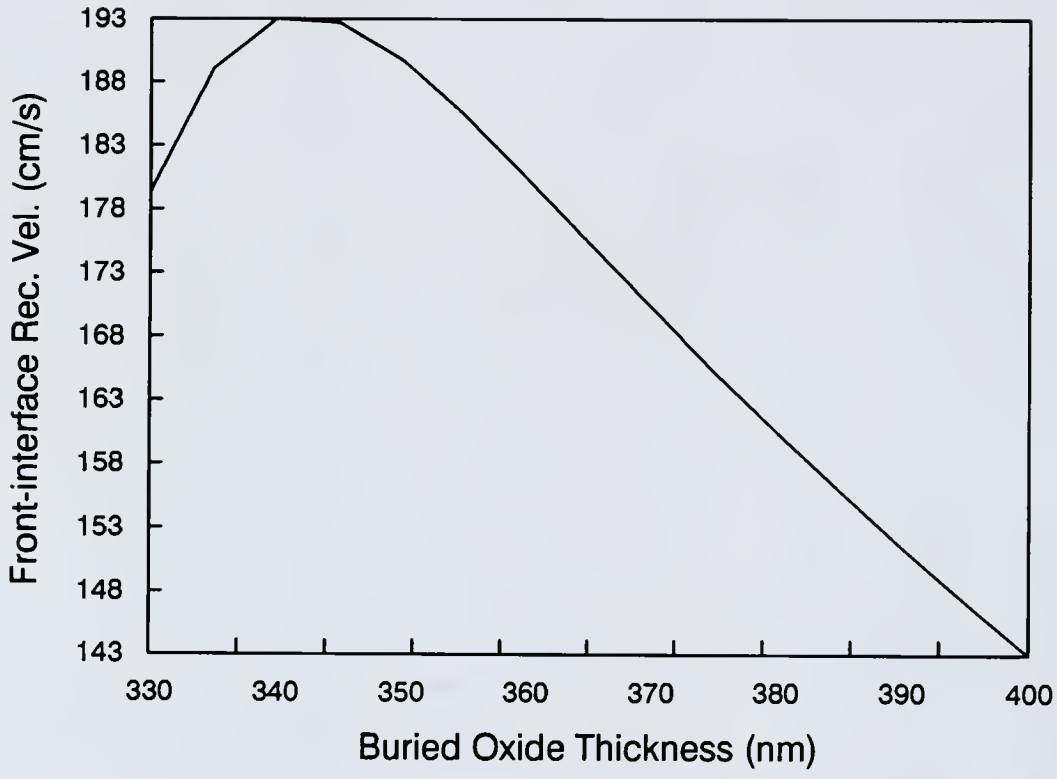

Figure 3.16: The sensitivity of back-interface recombination velocity to t_{ox}.

CHAPTER 4
CORRELATION OF IMPLANTATION DEFECTS WITH DETERMINED INTERFACE RECOMBINATION VELOCITIES AND CARRIER LIFETIMES IN ANNEALED SIMOX SOI MATERIALS BY USING A CONTACTLESS OPTICAL MODULATION TECHNIQUE

4.1 Introduction

The development of low-power and high-speed ULSI circuits fabricated on ultra-thin film SOI wafers has recently drawn great interest. Key to the success of low-power and high-speed applications will be the availability, cost, and performance advantage of quality SOI material meeting the requirements of low-power and high-speed ULSI circuits. SIMOX (Separation by IMplantation of OXygen) is a promising candidate for low-power, high-speed, and high density ULSI circuit applications [6]. A quality Si-overlayer is crucial for such applications. Although the multiple low dose implantation and annealing sequences have been applied to reduce the threading dislocations in the Si-overlayer, the drawbacks of multiple low-dose implantation include time consumption, expense, and yield reduction, as well as a possibility for increased metal contamination. The use of single-dose implant SIMOX is economically feasible and has proven satisfactory for large demonstration circuit fabrication [42]. In order to make the SOI technology widespread use in mainstream IC applications, the reduction of defect density in the Si-overlayer of single-dose implant SIMOX wafers is inevitable.

There are two possible sources of defect formation in the top silicon film: (i) evolution of defects from the as-implanted state and (ii) creation of point defects during high temperature annealing (HTA). That is, defects are created at the uppermost part of the Si-overlayer due to silicon interstitial (Si_I) migration at the surface [43, 44], and defects are formed near the front-interface due to the strain gradients generated

in densification of the buried oxide (BOX). The growth defects at the uppermost part of the Si-overlayer are mainly small dislocation loops which evolve to threading dislocations and segments [44]. The formation of pairs of threading dislocation attributes to small loops pinned at the Si/BOX interface. The defects growing near Si/BOX interface during HTA is due to the reconstruction of silicon when the SiO_2 precipitates dissolve [44, 45]. Stacking faults may form under certain conditions. These defects degrade the device performance. In addition, the interaction of Si_I with BOX during HTA is of great interest, because point defects play a key role in interface defect kinetics [46]. Although several dislocation studies [47]-[51] were performed under different implantation conditions, a general discussion on defect formation mechanisms and their relation to carrier lifetimes in high-dose implant SIMOX is of interest. In this work, we determine the interface recombination velocities and substrate carrier lifetimes of annealed SIMOX wafers under different implantation conditions by using the DBOM technique. The correlation between the formation of defects and the interface recombination velocities and substrate carrier lifetimes under different implantation conditions can be obtained for improving the wafer quality of the single-dose implant SIMOX materials.

4.2 Experimental Details

Four sets of SIMOX samples were prepared for this study by oxygen implantation into silicon wafers using an Ibis 1000 implanter. The wafers were annealed at 1310 °C for 5 hours in a 95.5% Ar ambient. The first and second sets of samples were used for implant energy, channeling and non-channeling studies. Six n-type samples were prepared for these two sets, and the implant energies were ranging from 155 to 185 keV with an implant temperature of 580 °C. The top Si film thickness varied from 124.4 to 196.3 nm for different channeling wafers and 201.1 to 248.8 nm for non-channeling wafers. The BOX thickness varied from 353 to 354.4 nm for channeling

wafers and 360.1 to 369.5 nm for non-channeling wafers. The third and the fourth sets of samples were used for implant temperature and beam current studies. There are three p-type samples in each set with the implant dose of 1.70×10^{18} cm^{-2} and the implant energy of 175 keV. The implant temperature ranged from 540 to 640 °C for the three different lots, with the top Si film and BOX thickness ranging from 197.1 to 178.5 nm and 387.8 to 392.7 nm, respectively, for samples of the third set. The implant beam current ranged from 45 to 65 mA for the three beam current lots, with the top Si film and BOX thickness ranging from 183.4 to 179 nm and 377.3 to 383.8 nm for samples of the fourth set.

In this experiment, the DBOM technique [40, 41] was employed for determining the interface recombination velocities and substrate carrier lifetimes. The measurements of interface recombination velocities were carried out with the incidence of pump beam at $\theta_1 = 23°$ and $\theta_1' = 63°$. For the measurements of substrate-excess-carrier lifetimes, the pump beam was incident at $\theta_1 = 23°$. First, the substrate carrier lifetime τ_s was measured by using an IR probe beam and a He-Ne laser pump beam impinging on the back surface of a SIMOX wafer. The rms values of the surface slope m and the surface roughness σ were measured by using Sloan Dektak II surface profiler to obtain the reflectance. The IR transmitted beam intensity, I, was measured using the chopped probe beam and a lock-in amplifier. The change in the transmitted intensity ΔI was measured by using the chopped pump beam superimposed on the probe beam which was not chopped. The resulting IR transmitted intensity was measured by using a lock-in amplifier.

To determine the back-interface recombination velocity, S_3, the probe and pump beams impinged on the front surface of the sample with different oblique incident angles of the pump-beam excitation. The measurement procedures for I and ΔI were the same as in the determination of τ_s. Values of R were measured by using a laser power meter. For different angles of pump-beam excitation, the measurements

of I, ΔI, and R were carried out in a similar procedure.

Finally, the front interface recombination velocity, S_2, was determined by using the He-Cd laser as the pump beam and using the same procedures described above. The S-polarized reflectances of the pump beam were monitored by a laser power meter to determine the front surface reflectance, R, and the back-interface transmittance, T, of the SIMOX wafer.

4.3 Results and Discussion

Before discussing the implantation effects and results, the etch-pit method and the formation of dislocations in SIMOX wafer are described briefly as follows.

The etching rate of a chemical solution depends distinctly on the crystallographic orientation. The etching rate is significantly affected by local stress caused by defects. In regions near dislocations, chemical etching proceeds more rapidly compared with perfect regions. As a result, etch pits that often have crystallographic symmetry are formed on the sample surface. Etch pit is commonly observed with an optical microscope, which gives rise to the differential interference contrast due to the etched features on the sample surface.

Three types of simple dislocation in the diamond lattice are (i) screw dislocation (A dislocation that has its axis perpendicular to its Burgers vector is called a pure edge dislocation), (ii) 60° dislocation (A 60° dislocation that has its axis 60° to its Burgers vector is called a 60° dislocation), (iii) pure edge dislocation (A dislocation that has its axis parallel to its Burgers vector is called a screw dislocations).
If the dislocation lies entirely within the crystal, the dislocation line forms a closed loop, which is referred as a dislocation loop. Most of the dislocation line is of mixed type, partly edge and partly screw. The dislocation may move inside the crystal by slip (e.g., applying shearing forces in the opposite direction to the top and bottom of the crystal will result in prismatic dislocation loops) and or climb (since the edge of

an extra half-plane consists of a row of atoms having incomplete lattice boding, atom can easily be added or removed from these sites. A climb force can be produced as an elastic stress applied to the extra plane of a dislocation $F/L = -\sigma b$ where b is the Burgers vector and σ is the stress).

The dislocation formation mechanism in SIMOX structure is not fully understood. The dislocations may be divided into as-implanted and HTA (high-temperature-annealing) induced. Here the as-implanted effects are discussed first.

The dislocation formed in implantation maybe come from (i) ion implantation and (ii) silicon oxidation into silicon dioxide. In ion implantation, the implant collision cascades produce the silicon interstitial (Si$\rightarrow$ Si_I+V). And, in the internal oxidation (2.25 Si+2 $O_i \rightarrow$ 1.25 Si_I+SiO_2), the Si_I is also produced after the oxidation. The Si_I will either form dislocations or migrate toward the surface and incorporated there. During implantation the formed oxide precipitates block Si_I diffusion to the surface. Hence, the internal oxidation is the main source for emission of Si_I and creation of stress.

After HTA, threading dislocations are formed by (i) evolution of defects in the as-implanted state and (ii) creation of defects during annealing. The as-implanted defects near the Si overlayer surface will agglomerate the Si_I (from internal oxidation) and evolve it into threading dislocations. The internal oxidation will densify the BOX and will emit the Si_I. Moreover, if the annealing temperature is inhomogeneous, the stress may be induced and then the dislocations generated.

The measurements of interface recombination velocities and substrate-excess-carrier lifetimes were carried out for four sets of samples used in this study. The results for different implantation conditions are shown in Figs. 4-1 through 4-8.

4.3.1 Implant Energy, Channeling, and Non-channeling Conditions

In Figure 4.1, the relationship between the defect density, the front-interface recombination velocity, and the implantation conditions for the six wafers is shown. The results indicate that a higher implant energy yields lower defect density and lower recombination velocity in the Si-overlayer area. As the energy of implant decreases, the quality of Si-overlayer degrades as measured by defect density and recombination velocity.

Figure 4.2 presents the front interface recombination velocity versus implant energy in the channeling (0°) and non-channeling (10°) implanted samples. Based on the low recombination velocity values, the results reveal that higher energy (185 keV) and channeling implants lead to a better interface quality. The non-channeling implant produces more damage to the interface than that of the channeling implants.

In the low energy implant, the implant range, R, was more shallow than that of higher energy implant. Defects are created at the uppermost part of Si-overlayer due to the Si_I migration to the surface [43, 44]. The semiloop dislocations introduced during implantation annealed out the surface during HTA. Meanwhile, some semiloop dislocations extended downwards to the front interface and formed pairs of threading dislocations [44]. Most of the existing defects, created by implantation and located near the front interface, become dominant if the Si-overlayer is thinned [44]. During HTA, the SiO_2 precipitates at this zone are dissolved as

$$SiO_2 + 1.2Si_I \rightarrow 2.2Si + O_2 \tag{4.1}$$

The Si_I is provided by the formation of BOX at the front interface according to

$$2.2Si + O_2 \rightarrow SiO_2 + 1.2Si_I \tag{4.2}$$

The dissolution of the SiO_2 precipitates and the absorption of Si_I is needed to balance each other. If the outdiffusion of oxygen occurs, the extra defects will be introduced [52]. The reconstruction of silicon in this zone is a three-dimensional coalescence process which introduces dislocations in order to accommodate the translational and rotational displacements. For a thinner Si-overlayer, the Si_I can easily migrate to the surface. Hence, the dislocation loop is easily formed. In the channeled samples, the implanted oxygen atoms travel down channels for the initial part of the implant process, and are slowed down mainly by electronic stopping. A deeper oxygen atom penetration results in less damage and a lower probability of oxide precipitation in the Si-overlayer.

Figure 4.3 shows the back-interface recombination velocity versus the implant energy in the channeling and non-channeling implanted samples. Contrary to the front interface, the back interface indicates that a better interface quality is attributed to the lower energy (155 keV) and non-channeled implant. In Figure 4.4, the substrate carrier lifetimes versus implant energy for the channeled and non-channeled samples are presented. Similar to the results of the back-interface recombination velocity measurements, a better silicon substrate quality was obtained from lower energy (155 keV) and non-channeled implant. The results are consistent with Fig. 4.3 in that the channeled implants produce more damage to the substrate than that of non-channeled implants. A deeper oxygen atom penetration results in more damage to the silicon substrate and Si island in BOX near back interface [47]. The higher energy and channeled implants generate damage in the deeper region of the implanted samples. Hence, a poor interface and silicon substrate quality is presented at the backside of BOX.

4.3.2 Implant Temperature Conditions

Figure 4.5 shows the relationship between the defect density, the front-interface recombination velocity, and the implantation temperature for the three SIMOX wafers. The results show that higher implant temperature yields a low defect density and lower recombination velocity in the Si-overlayer region. As the implant temperature decreases below 590 °C, the quality of Si-overlayer degrades as measured by defect density and recombination velocity. The results also show that defect density and recombination velocity decrease sharply when the implant temperature is higher than 590 °C.

The amount of oxygen present in the Si-overlayer is strongly dependent on the implantation temperature [53]. The concentration of oxygen interstitials in the silicon can be estimated as [54]

$$[O_I] = 1.53 \times e^{-1.03eV/kT} \qquad \text{cm}^{-3} \tag{4.3}$$

where kT is the thermal energy. A higher dissolution rate of oxygen in the Si-overlayer may result in a reduction of semiloop defects and producing of thermal donors during the HTA treatment. A reduction of semiloop dislocations after HTA in higher temperature (550-700 °C) implant has been observed by P. Roitman *et al.* [45]. From the earlier works of Tuppen *et al.* [55] and Davis *et al.* [53], amorphous silicon can be formed near both sides of the BOX at a lower implantation temperature ($<$ 500 °C). These regions may become polycrystalline zones after the HTA treatment. Our results reveal that implant temperatures at 590 °C or greater may result in a good active silicon layer.

Figure 4.6 illustrates the back-interface recombination velocity and substrate carrier lifetimes versus the implant temperature. Similar to the studies in the front interface, higher implant temperatures produce a better back interface quality. The results of the substrate-excess-carrier lifetime measurements exhibit a different trend from

the measured results of back-interface recombination velocity. The measurements reveal that the lower implant temperature (540 °C) yields a better silicon substrate quality. The lower lifetime in the Si substrate is suggested to result from heavy metal gettering [39]. Heavy metal is introduced during implantation and diffuses into the Si substrate during HTA process. The BOX does not prevent the diffusion of heavy metals [56] into the silicon substrate. Due to a better back-interface quality under higher temperature implants, less gettering of extrinsic heavy metals at the interface is expected. Hence, more heavy metals are presented inside the silicon substrate.

4.3.3 Implant Beam Current Conditions

In Figure 4.7, a plot showing the relationship between the defect density, the front-interface recombination velocity, and the implantation beam current for the three SIMOX lots is presented. The results show that the lower implant beam current yields lower defect density and lower recombination velocity in the Si-overlayer region. As the beam current of implant increases, the quality of the Si-overlayer degrades as measured by defect density and recombination velocity. The high beam current implant produces more damage to the interface than that of the lower beam current implants. In the high beam current implants, more damage is expected to form near the surface of the implant samples [57]. A large quantity of half loop dislocations is created in the Si-overlayer for the higher beam current implants which form threading dislocations during the HTA [45].

Figure 4.8 illustrates the back-interface recombination velocity and the substrate carrier lifetimes versus the implant beam current. Contrary to the studies in front interface, a higher beam current produces a better back interface quality. The substrate-excess-carrier lifetime measurements show a different result from that of the back-interface recombination velocity. The measurements reveal that the lower beam current yields a better substrate quality. The poor back interface quality found

in lower beam current implants maybe attributed to the oxygen deficiency and a greater number of Si islands generated in the BOX near the back interface will result. The quality of the silicon substrate is influenced by the heavy metal gettering and the quality of back interface.

Finally, the defects and the relationship to the measured recombination parameters will be discussed here. The formation defects in the Si overlayer of SIMOX wafers maybe attributed to the crystal strain around dislocation cores, the dangling bonds of different dislocation types, and the known trapping which occurs with metallic point defects (see Fig. 4-9). Under low injection, the lifetime and surface recombination velocity are expressed as $1/\sigma v_{th} N_t$ and $\sigma v_{th} N_{it}$, respectively, where N_t and N_{it} are the defect density in the bulk and at the interface, respectively. The dangling bond or electron trapping is consistent with the faster recombination results. That is, the dangling bond acts as the trapping center. In the history of defect examination in SIMOX material, there are several kinds of defects which have been identified. The most common type of top Si film defects is the threading dislocation (see Fig. 4-10) [45]. These typically result through the initial half loop formation which grows in diameter to eventually intersect the Si surface and the BOX interface, resulting in the characteristic threading dislocation pair formation (see Fig. 4-11) (extending from surface to BOX interface) [45]. Threading dislocations, even up to 10^9 cm^{-2} density, have not been shown to adversely affect device performance [58]. Although the crystal strain extends for several hundred nm around the dislocation core, there has been no published correlation between device failure and dislocation density. However, if there are any metals present, chances are the dislocations will getter the metals to the dislocation sites. Then, the device performance will be hindered, as metals are known to trap and kill lifetimes [75]. Another type of dislocation that has recently been discovered, under certain implant and anneal conditions, are pyramidal stacking faults (not the standard tetrahedral stacking faults found in the bulk silicon!) (see

Fig. 4-12). These very small stacking faults will form at the BOX interface if and when the BOX is slightly under-implanted [59]. With a slightly increased oxygen dose, the pyramidal stacking faults will be absorbed by the growing BOX thickness. Thus, this emphasizes their extremely small size and extremely proximity to the BOX interface. Dislocation types have been classified through standard Secco chemical etching and SEM (threading dislocation pairs resulting from loop expansion) (see Fig. 4-11), and TEM has shown the pyramidal stacking faults when the material is underdose with oxygen (see Fig. 4-10). The TEM may result in a misleading of defect counts as the defect density below 1×10^7 cm^{-2} [60]. There are other types of dislocations, but these have been eliminated in the most recent SIMOX material [61]. Each type of dislocations behaves differently with respect to etch pit density. For the threading dislocations, the etch pit pairs are visible at about 1000 from the interface and all the way to the interface as the etch continues. For the stacking faults near the BOX interface, the etch pits appear as a singular pits and only at the last 250 to 150 from the BOX interface [61]. The density of the threading dislocations is a function of dose (the thicker the BOX, the greater the dislocation density). The pyramidal stacking fault density is rather constant provided that they appear at all.

4.4 Conclusion

In this work, a study of defects in SIMOX wafers under different implantation conditions has been carried out by using the DBOM technique. Using this technique, the quality of SIMOX wafers can be evaluated versus processing and growth parameters. The measurement results reveal that higher energy, channeling, higher temperature, and lower beam current implants may result in a lower front-interface recombination velocity and a lower Si-overlayer defect density. A better Si-overlayer quality is obtained with those conditions. As described, the half loop dislocations and interstitial point defects near the front interface play a decisive role in the dislocation

formation in the Si-overlayer during HTA process. A minimization of the dislocation loops formed in the Si-overlayer during implantation is the key factor to improve the quality of the single-dose implant SIMOX wafers. From the results of back-interface recombination velocity and substrate lifetime measurements, a better back interface and silicon substrate quality is obtained under lower energy and non-channeling implants. Although higher implant temperature and higher beam current implants may result in a lower back-interface recombination velocity, the substrate carrier lifetime measurements show the contrary tendency. A higher substrate carrier lifetime is obtained under lower temperature and lower beam implants. This discrepancy may attribute to the heavy metal gettering at the silicon substrate and the backside of BOX after HTA treatment.

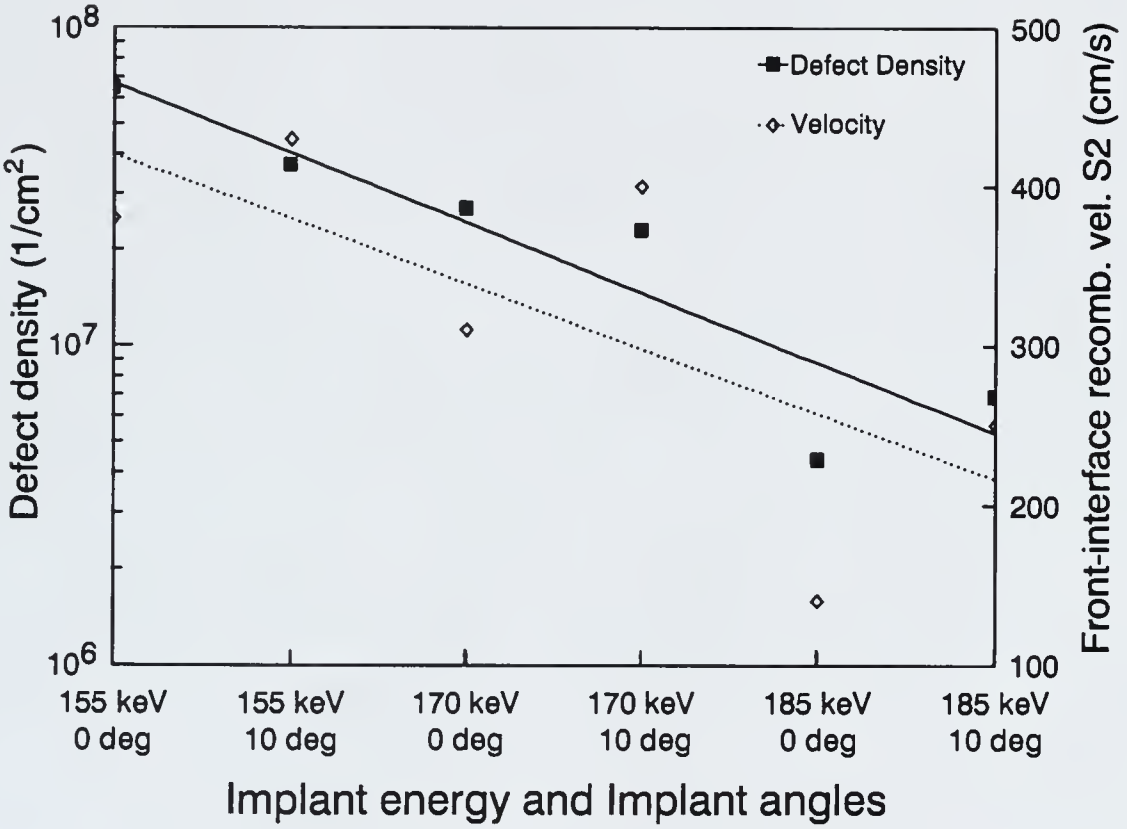

Figure 4.1: Measured defect densities and frontinterface recombination velocities for the different energies and angle implants.

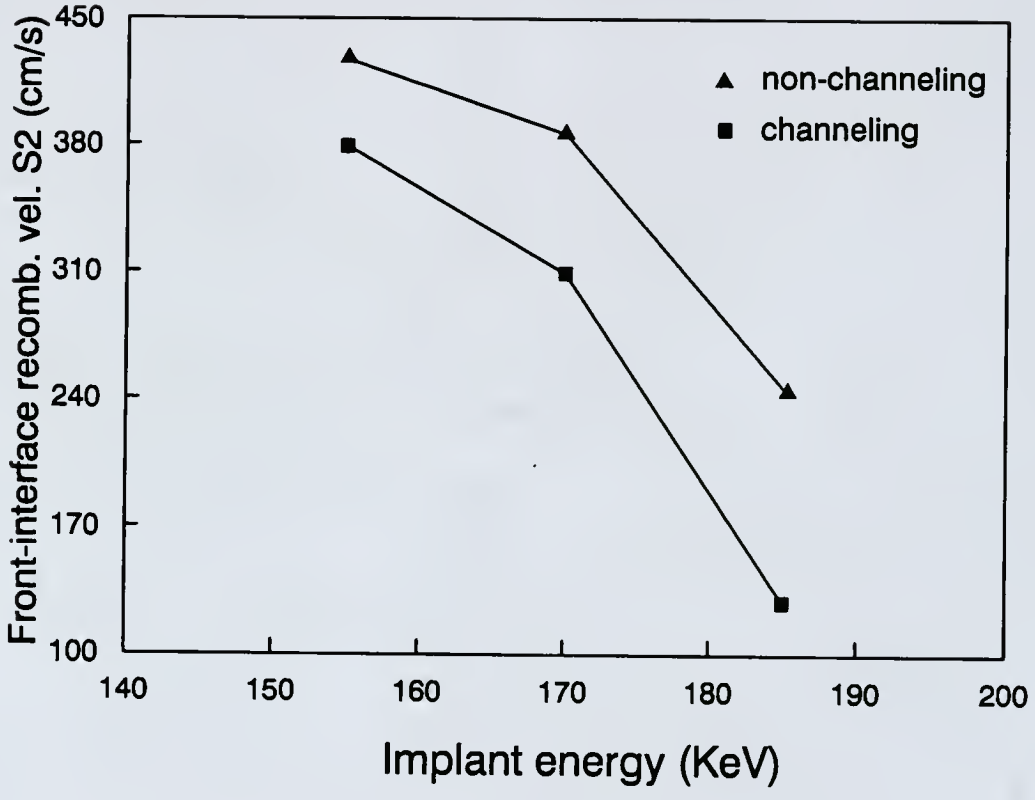

Figure 4.2: Measured front-interface recombination velocities for the channeling and non-channeling implants versus the implant energy.

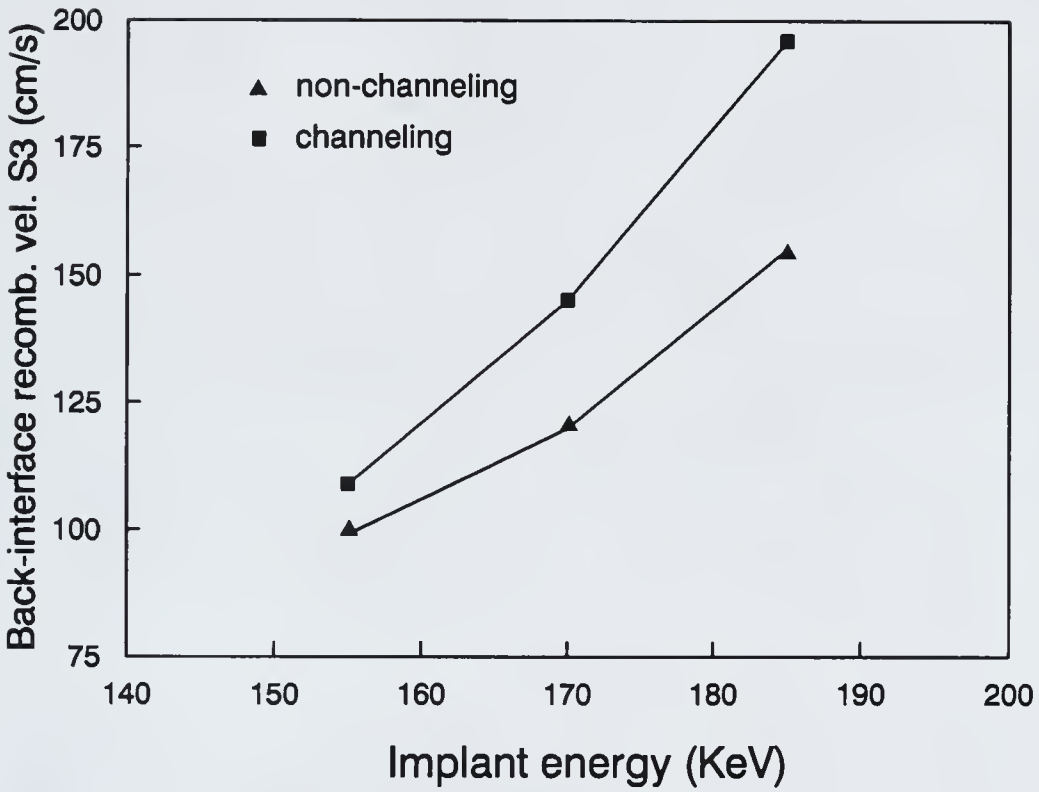

Figure 4.3: Measured back-interface recombination velocities for the channeling and non-channeling implants versus the implant energy.

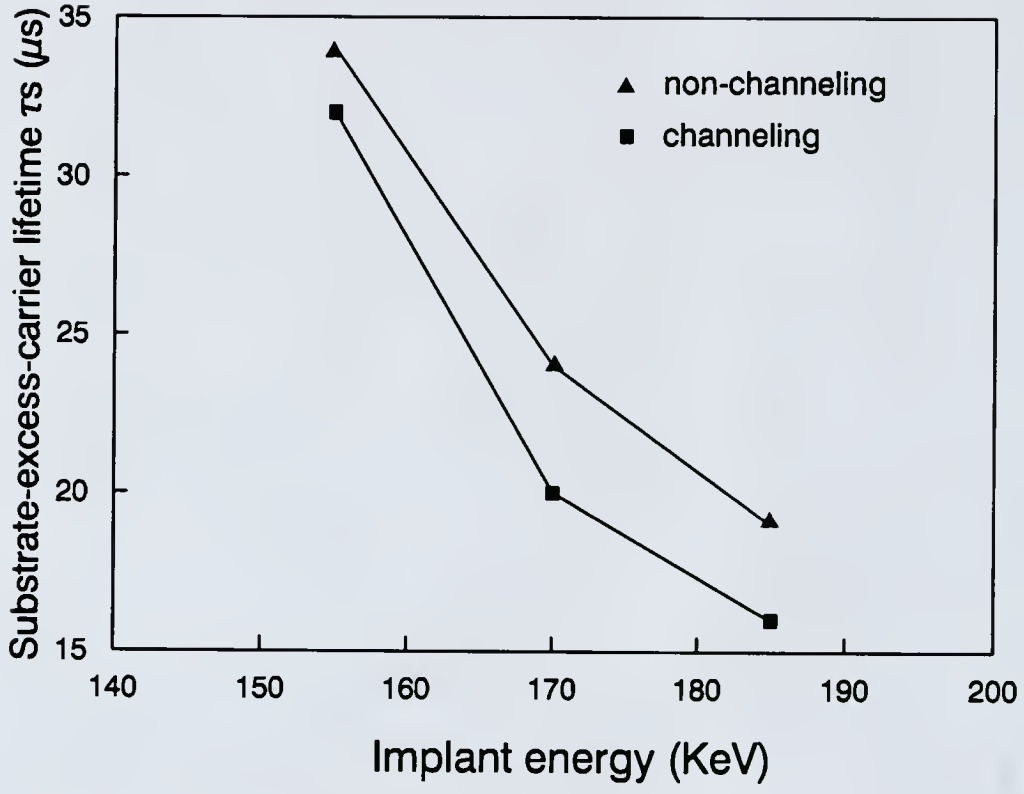

Figure 4.4: Measured substrate-excess-carrier lifetimes for the channeling and non-channeling implants versus the implant energy.

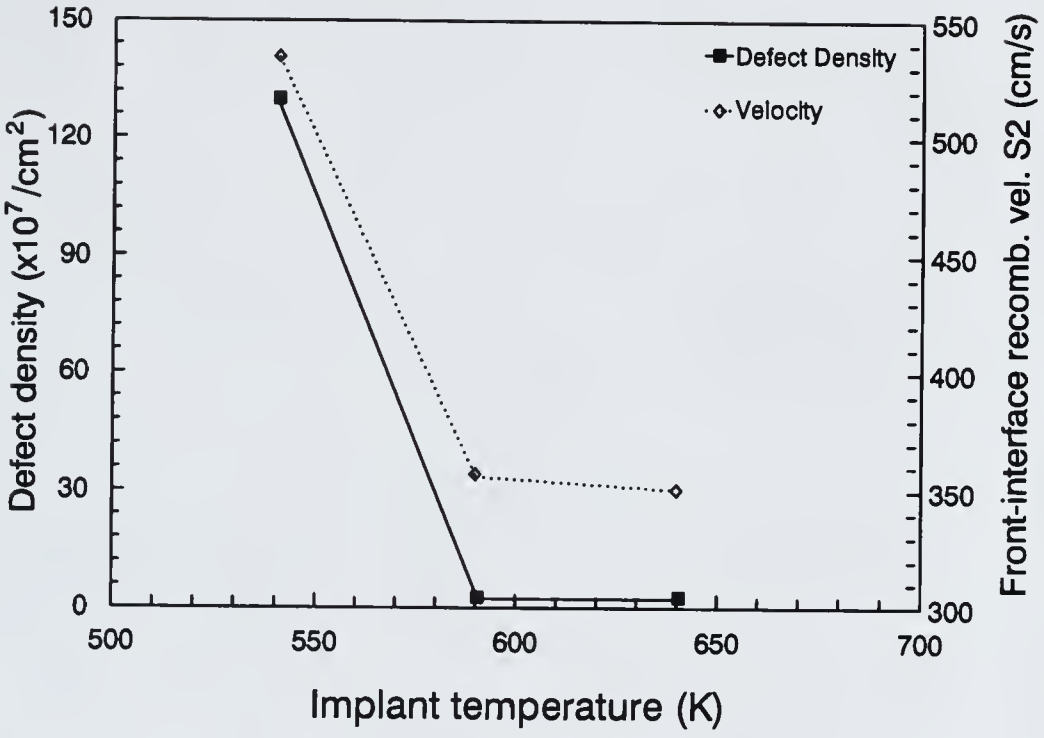

Figure 4.5: Measured defect densities and front-interface recombination velocities for the different temperature implants.

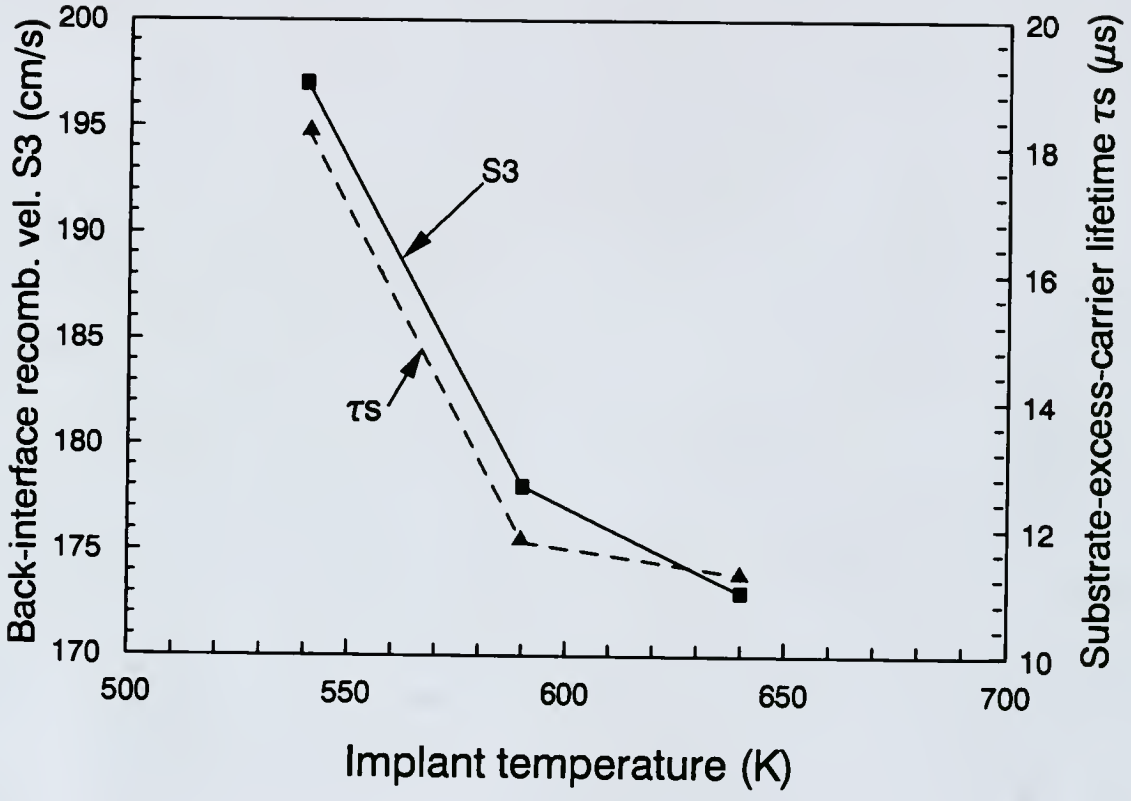

Figure 4.6: Measured substrate-excess-carrier lifetimes and back-interface recombination velocities for the different temperature implants.

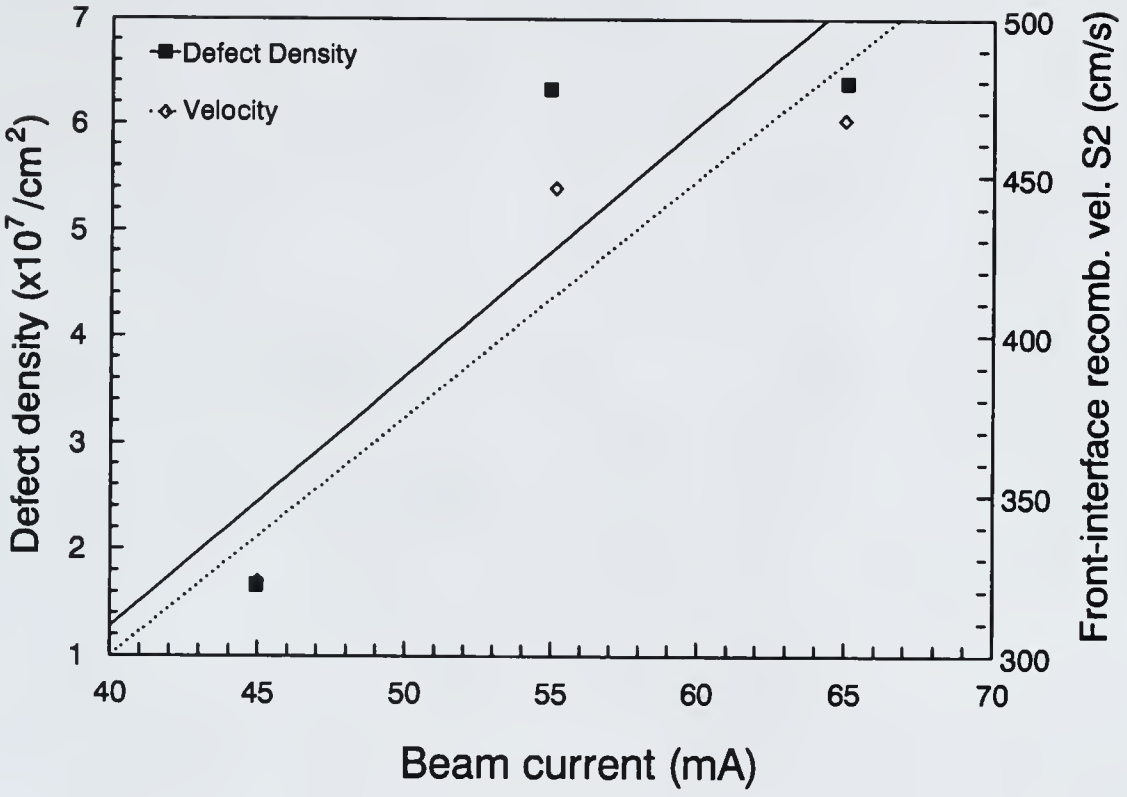

Figure 4.7: Measured defect densities and front-interface recombination velocities for the different beam current implants.

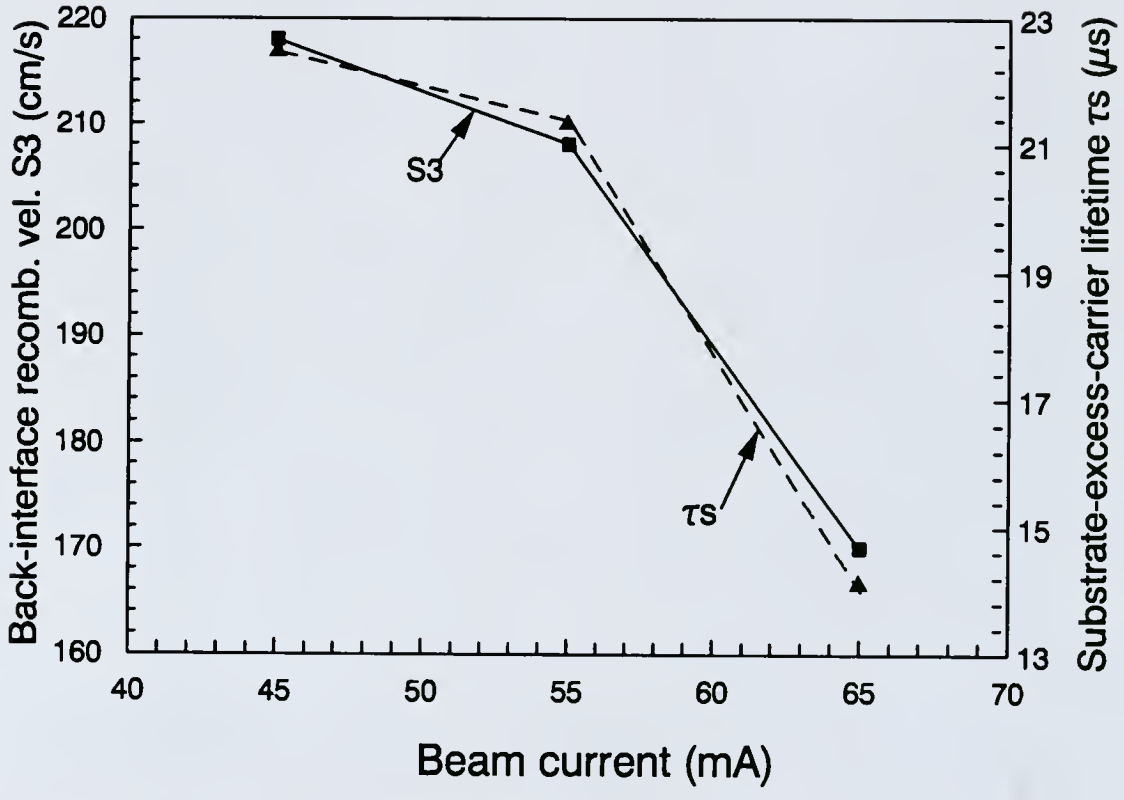

Figure 4.8: Measured substrate-excess-carrier lifetimes and back-interface recombination velocities for the different beam current implants.

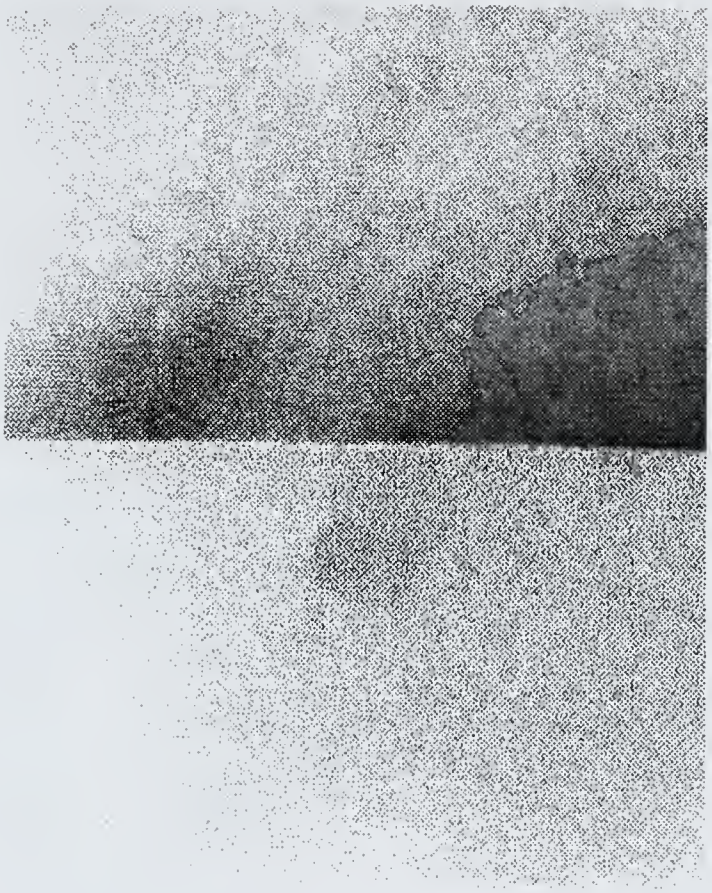

Figure 4.9: The High Resolution TEM for distinguishing the metallic gettering in the dislocation site.

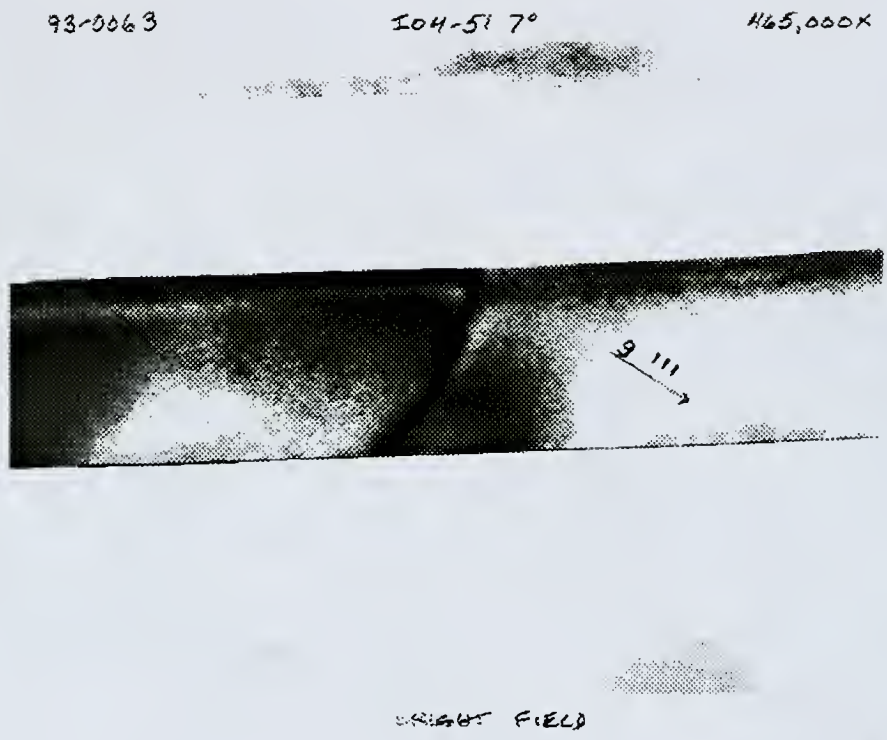

Figure 4.10: The TEM shown threading dislocation through the top silicon film.

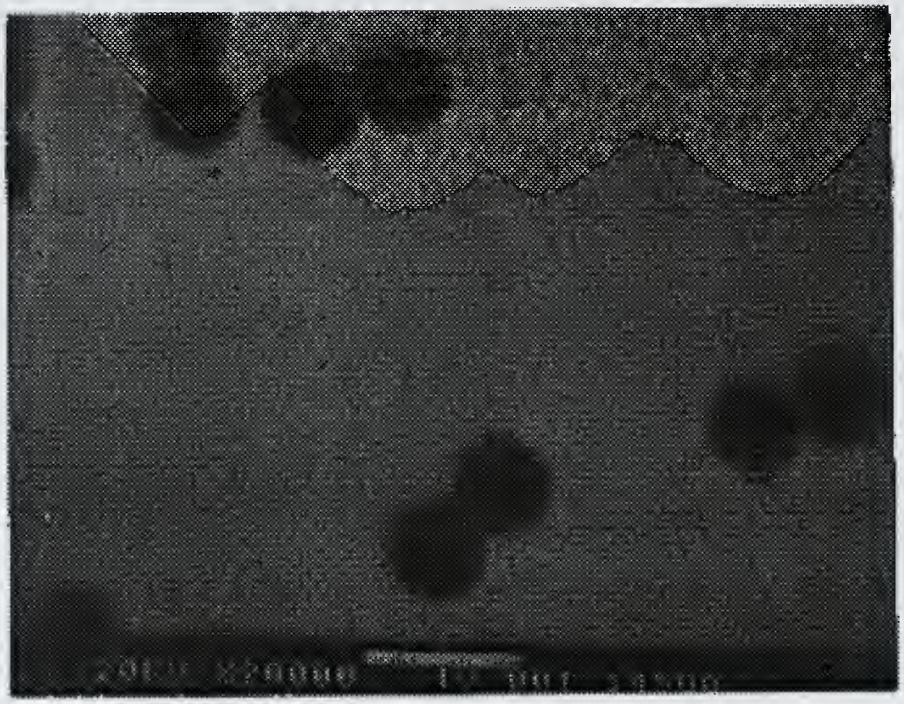

Figure 4.11: The SEM shown threading dislocation pairs after etch-pit etching.

Figure 4.12: The TEM shown threading dislocation and pyramidal stacking fault in the top silicon film.

CHAPTER 5
THE EFFECTS OF PARASITIC BIPOLAR-TRANSISTOR CONDUCTION ON THE HOT-CARRIER-DEGRADATION OF SOI MOSFETS

5.1 Introduction

The hot-carrier-induced degradation is one of the major challenges for shrinking further the size of bulk Si or SOI components into deep submicrometer dimensions. The degradation of nMOSFET resulted in circuit failure maybe attributed to the high electric field near drain/body junction. In SOI transistors, fully depleted (FD) device exhibits less aging effects than that of PD devices [2, 62]. This was due to the smaller maximum channel-electric field and vertical oxide field for the FD devices [62]. The hot-carrier damage in subthreshold region due to the floating-body effects has been investigated for PD devices [63]. Although no clear evidence has been shown that the aging of SOI MOSFETs is more severe than that of the bulk Si counterparts, the degradation mechanisms are more complex. These include (i) not only the front gate oxide but also the buried oxide and related interface may be damaged [2, 64, 65]; (ii) interface coupling allows the front channel to sense the presence of defects at the opposite interface [2]; (iii) the field maps are different, and (iv) floating body effects may come into play. The purpose of this work is to investigate the latter aspect by revealing the main consequences of stresses conducted in floating- and unfloating-body modes. In next section, an analytical model of parasitic BJT effects in PD SOI nMOSFET is presented for correlating the hot-carrier-induced aging, and a modified lucky-electron model is developed for estimating the degradation of SOI nMOSFET characteristics. A comparison of the degradation between floating and unfloating-body modes are presented. The defective parameters are extracted by

using the measurements of $I_{ds} - V_{g1}$ characteristics before and after stresses. Finally, the aggravation of aging in floating-body mode is obtained, and some possible solutions in processing and device structure to alleviate the aging effects in the PD SOI nMOSFET's is discussed.

5.2 Theory

5.2.1 Parasitic BJT Effects

In this section, the parasitic BJT effects in the PD SOI NMOSFET will be discussed. The models of parasitic-current components, body potential for body floating and unfloating, and front-gate threshold voltage are depicted.

Figure 5.1 shows the various current components in a partially depleted (PD) floating body (FB) SOI nMOSFET with lateral parasitic BJT conduction. The source, body, and drain behaves as emitter, base, and collector, respectively in the parasitic BJT. In the saturation region, the substrate-hole current (I_{sub}) is generated by the impact ionization of channel (I_{ch}), collector (I_C), and generation current (I_g) near the drain-body junction. the hole current generated by the channel current is given as (see Appendix B)

$$I_{chm} = (M_{ch} - 1)I_{ch} \tag{5.1}$$

with

$$M_{ch} - 1 = \frac{\alpha_0 \mathcal{C}}{\beta_i} \exp\left(\frac{-\beta_i l}{C}\right) + \int_0^{Lnn} \alpha_0 e^{-\beta_i/\mathcal{E}_{y2}} dy \tag{5.2}$$

$$\mathcal{C} = V_{ds} - V_{dsat} - V_{Ldd} \tag{5.3}$$

where M_{ch} is the impact-ionization multiplication factor of MOSFET part, $\alpha_0 = 1.4 \times 10^6$ cm^{-1}, $\beta_i = 2.4 \times 10^6$V/cm [66]; V_{ds} is the drain voltage; V_{Ldd} is the voltage drop in the LDD region, l is the characteristic length of the MOSFET; L_{nn}, N_d and

$\mathcal{E}_{y2}$ are the width, doping concentration, and the electric field of LDD, respectively; L_{sat} is the width of velocity saturation region; η is a fitting factor accounted for the nonuniform lateral electric field distribution induced by the drain voltage, and V_{dsat} is the drain saturation voltage which is described in Appendix B. The hole current attributed to the parasitic BJT collector current I_C (see Appendix C) is given by

$$I_{cm} = (M_b - 1)I_{C1} + (M_{ch} - 1)I_{C2} \tag{5.4}$$

$$M_b - 1 = 1.18(V_{ds} - V_{be})e^{\frac{-\beta_i}{\mathcal{E}'_m}} \tag{5.5}$$

$$\mathcal{E}'_m = \frac{1}{\eta}\sqrt{\frac{2qN_A(V_{ds} - V_{be})}{\epsilon_{Si}}} \tag{5.6}$$

where M_b is the impact-ionization multiplication factor of the parasitic BJT part [67]; V_{be} is the body-source junction potential, and N_A is the body doping concentration. The hole current generated by the generation current in body-drain depletion region is given by

$$I_g = M_b I_{g1} \tag{5.7}$$

where I_{g1} is the generation current originated from the quasi-neutral body/drain junction [32] and can be written as

$$I_{g1} = \frac{qn_i W_{cb} W(t_{Si} - X_d)}{2\tau_g} \tag{5.8}$$

$$\tag{5.9}$$

where n_i is the intrinsic carrier concentration; W is the channel width; X_d is the body depletion depth; W_{cb} is the depletion width in body-drain junction; ϕ_t is the thermal voltage, and τ_g is the carrier generation lifetime and can be expressed as a function of the low concentration lifetime τ_0 and the body doping concentration N_A [68]

$$\tau_g = \frac{\tau_0}{1 + N_A/1 \times 10^{15}} \tag{5.10}$$

The total substrate-hole current is

$$I_{sub} = I_{chm} + I_{cm} + I_g \tag{5.11}$$

From Fig. 5.2, the total drain current is given by

$$I_{ds} = M_{ch}(I_{ch} + I_{C2}) + M_b I_{C1} + I_g \tag{5.12}$$

In the floating body, the substrate-hole current is equal to the base current of parasitic BJT (see Fig. 5.2). The body potential V_{be} is obtained by solving eqns. (5.11) and (B1)-(B3) and given as

$$V_{be} = 2\phi_t \ln\left(\frac{-k_3 + \sqrt{k_3^2 + 4I_{sub}\,(k_1(1-\alpha_T) + k_2 + k_5)}}{2\,(k_1(1-\alpha_T) + k_2 + k_5)}\right) \tag{5.13}$$

where k_1, k_2, k_3, and k_5 are given in Appendix C; α_T is the transport factor of the parasitic BJT.

In Figure 5.2, when the body is unfloating, a part of the body current I_{bb} flows through the body resistance R_b to the ground. In order to include the distributed nature of the body resistance, the R_b is extracted by experimental measurements [69]. In the subthreshold region, the base current of the parasitic BJT is approximately equal to $I_{bb} = V_{be}/R_b$ [69]. Above saturation region, a part of base current is drained into the ground and the body potential can be expressed as

$$V_{be} = 2\phi_t \ln\left(\frac{-k_3 + \sqrt{k_3^2 + 4(I_{sub} - I_{bb})(k_1(1-\alpha_T) + k_2 + k_5)}}{2\,(k_1(1-\alpha_T) + k_2 + k_5)}\right) \tag{5.14}$$

As described in Appendix B, the initial front-gate threshold voltage V_{t0} is given by

$$V_{t0} = V_{FB1} + 2\psi_F(1 + \frac{C_b + C_{it1}}{C_{ox1}}) - \frac{Q_{beff}}{2C_{ox1}} - \frac{C_b}{C_{ox1}}V_{be} \tag{5.15}$$

where C_{it1} is the interface state density in the front interface and $\psi_F = \phi_t \ln\frac{N_A}{n_i}$ is the Fermi potential. The increase in body potential influences the front-gate threshold voltage V_{t1} as

$$V_{t1} = V_{t0} + \gamma(\sqrt{2\psi_F - V_{be}} - \sqrt{2\psi_F}) \tag{5.16}$$

for $V_{be} < 2\psi_F$ and

$$V_{t1} = V_{t0} + K(V_{be} - 2\psi_F) \tag{5.17}$$

for $V_{be} > 2\psi_F$, where $\gamma = \sqrt{2\epsilon_{Si}qN_A}(1-\xi)/2C_{ox1}$ is the body effect coefficient. ξ (see eqn.(B11)) is the charge sharing for the short channel effect; K is a linear fitting factor determined experimentally [69] and is equal to -1.67 for this study.

5.2.2 Hot Electron Injection

In this section, the hot-carrier injection mechanism leading to oxide damage in SOI nMOSFET will be discussed. The underlying physical factors of charge trapping and interface trap generation will also be briefly reviewed.

In order for hot electrons to inject into gate oxide, hot electrons have to gain sufficient kinetic energy from the high electric field near drain junction to surmount the potential barrier of gate oxide and to redirect the momentum towards the gate-oxide interface [70]. Based on quasi-elastic scattering probabilities of electrons, a gate-injection current is approximately given by [70]

$$\begin{aligned} I_{ei} &= \frac{1}{2}(I_{ch}+I_{C2})\frac{t_{ox1}}{\lambda_r}(\frac{\lambda\mathcal{E}_m}{\psi_b})^2 P(\mathcal{E}_{ox1})e^{\frac{-\psi_b}{\mathcal{E}_m\lambda}} \\ &+ \frac{1}{2}(I_{C1}+I_g)\frac{t_{ox1}}{\lambda_r}(\frac{\lambda\mathcal{E}'_m}{\psi_b})^2 P(\mathcal{E}_{ox1})e^{\frac{-\psi_b}{\mathcal{E}'_m\lambda}} \end{aligned} \tag{5.18}$$

where,

$$\begin{aligned} \psi_b &= 3.2 - 2.59\times10^{-4}\mathcal{E}_{ox1}^{0.5} - 4\times10^{-5}\mathcal{E}_{ox1}^{2/3} \quad \text{V} \qquad \text{for } \mathcal{E}_{ox1} \geq 0 \\ &= 3.2 - (V_{ds} - V_{g1} - V_{be}) \quad \text{V} \qquad \text{for } \mathcal{E}_{ox1} < 0 \end{aligned} \tag{5.19}$$

$$\mathcal{E}_{ox1} = \frac{V_{g1} - V_{ds} - \psi_{ms} - \psi_{s1}}{t_{ox1}} \tag{5.20}$$

Here $P(\mathcal{E}_{ox1})$ is the probability that a hot electron travels to the gate oxide interface without suffering any collision after undergoing a re-directing collision at varying depths below the interface [70], ψ_{ms} and ψ_{s1} are the work function difference and surface potential in the front channel, respectively, $\lambda_r(=61.6nm)$ [70] is the mean free path of hot electron to have momentum re-direction, and $\lambda(=9.2nm)$ is the mean free path of the hot electron [71].

Interface states generation in nMOS devices was explained by the breaking of silicon-hydrogen bonds by hot carriers injection and the diffusion of hydrogen atoms inside oxide to form more silicon dangling bonds and hydrogen molecules [72, 73]. The bond-breaking electron current density can be written as $I_{BB} = (1/W)I_{sub}^{m}/I_{ds}^{m-1}$, where $m(=3)$ [73] is the ratio of critical energy for interface-state generation to impact ionization. The generation of interface states is strongly dependent on the injected density of bond-breaking carrier, silicon-hydrogen-bonds density at the interface, and the diffusion of hydrogen atoms inside the oxide. Water-related traps such as high-temperature wet oxidation, silicon-nitride passivation, and the implantation of dopants in source/drain and active regions, etc., are possible trap centers for acceptor interface defects.

The trapping of negative oxide fixed charges can be derived by first-order chemical approximation [74], and the expression is given by

$$\begin{aligned} N_{ox1}(t) &= N_{ox1}(0)\left(1 - e^{\frac{\int_0^t I_{ei}dt}{\sigma v_{th}/q v_d}}\right) \\ &= N_{ox1}(0)(1 - e^{Q/Q_i}) \end{aligned} \tag{5.21}$$

where $N_{ox1}(0)$ is the maximum number of traps in which charges can be accommodated; σ is the capture cross-section of the traps, v_{th} and v_d are the thermal velocity and drift velocity of injected carriers, respectively. In order to correlate measured quantity, eqn.(5.21) can be rewritten as

$$\Delta V_{FB1} = \Delta V_{FB1}(0)(1 - e^{Q/Q_i}) \tag{5.22}$$

where $\Delta V_{FB1}(0)$ is the flat-band-voltage shift for $N_{ox1}(0)$. The water-related SiOH bonds are the plausible trap centers which can easily to capture electrons to become negatively charged centers.

5.2.3 Extraction of Degradation Parameters

In this section, the extraction of degradation parameters (e.g. threshold voltage shift (ΔV_{t1}), length of defective region (ΔL), interface-state increment (ΔN_{it1}), and oxide-fixed charge (ΔN_{ox1})) in the defective region will be described.

The drain current in a front-channel SOI MOSFET operated in strong inversion and linear region can be approximately expressed as

$$I_{ds} = \frac{C_{ox1} W V_{ds} \mu_1}{L[1 + (\theta_0 + R_{sd}\mu_1 C_{ox1} W/L)(V_{g1} - V_{t1})]}(V_{g1} - V_{t1}) \tag{5.23}$$

where $\theta_0 (\approx 0.1 V^{-1})$ is the mobility degradation factor [75], R_{sd} is the series resistance, and μ_1 is the low electric-field mobility [76]. The transconductance of the defective MOS devices after stress is given by two-piece model [77]

$$g_{ma} = \frac{G_d^2}{(G_{nd} + G_d)^2} g_m^{nd} + \frac{G_{nd}^2}{(G_{nd} + G_d)^2} g_m^d \tag{5.24}$$

where d and nd denote the transconductance (g_m) and the channel conductance (G) in the defective and nondefective region, respectively. The degradation parameters ΔV_{t1}, ΔL, ΔN_{it1}, and ΔN_{ox1} can be obtained from the measured $I_d - V_{g1}$ curves in the strong and weak inversion regions before and after stresses [78]. The corresponding shift of the front-gate threshold voltage after stress can be expressed as

$$\Delta V_{t1} = (\Delta N_{it1} \psi_{s1} + N_{ox1}) q / C_{ox1} \tag{5.25}$$

5.3 Results and Discussion

Test devices were n-channel, enhancement-mode, partially depleted MOSFETs fabricated on the standard SIMOX substrates. The gate lengths were from 1.0 to 1.6 μm, the film thickness was 150 nm, the gate oxide thicknesses were ranging from 15 to 20 nm, and the doping level was above 2×10^{17} cm^{-3}. The transistors had LDD and 5-terminal configurations which allow the body to be either floating (open),

unfloating or independently biased. The front channel was stressed for (V_{g_1}, V_{ds}) bias corresponding to a maximum value of the substrate current (i.e. for the most aggressive conditions of degradation). The device aging was essentially monitored through changes in the transconductance, threshold voltage, and saturation current. When the drain voltage is low enough for the bipolar transistor to be inactive, only a very small amount of defects is generated at the front interface. The absence of any back interface damage in the n-channel devices confirms the previous investigations [2, 64].

The parameters used in the simulations (Figs. 5.3 through 5.6) are $W/L = 10$ μm /1.4 μm, L_{nn}=0.1 μm, $t_{Si} = 150$ nm, $t_{ox1} = 15$ nm, $R_b = 30\text{k}\Omega$, W_E=2μm, $\mu_0 = 550$ cm^2/V-sec, $\eta = 1.2$, τ_g=50 ns, and τ_r=10 ns. Figure 5.3 shows the simulation results of the body potential and the front-gate threshold voltage for the floating- and unfloating-body modes. The floating-body mode reflects higher body potential increase which leads to a larger reduction of the front-gate threshold voltage than that of the unfloating mode. The reduction of front-gate threshold voltage results in a positive feedback between the current components and the quasi-Fermi potential separation inside the body of SOI devices. Although the negative feedback is also taking place in the impact ionization factor due to body potential increase, eventually, the parasitic bipolar effects is more palpable in the floating-body mode. For $V_{ds} \simeq$ 7.5 V, the degradation is substantially accelerated by the increased lateral field. More importantly, the bipolar action becomes possible, giving rise to additional damage. The substrate hole current of bipolar part overwhelms that of the MOS part when parasitic BJT activates (see Fig. 5.4). The larger the parasitic bipolar current, the higher the injection carriers inject into the gate oxide, which results in more damages for the floating-body mode than that of the unfloating-body mode (see Figs. 5.5 and 5.7).

Figure 5.6 presents the peak shape of the generated hole current versus front-gate

bias. At higher gate bias the maximum channel-electric field decreases, and hence the hole generation rate also reduced. Figure 5.7 shows a general trend: a more dramatic degradation was always observed after stress conducted with the body floating than after the equivalent stress (i.e. constant drain current) with the body unfloating. The generation of negative charges at the front interface and their preferential location within the drain spacer are clearly demonstrated by the transconductance curves of Fig. 5.7 and by the comparison of $I_{ds}(V_{ds})$ plots in the forward (S–D) and reverse (D–S) modes (shown in Fig. 5.8). It has been shown that accumulation of the back channel during stress will reinforce the floating body and bipolar action, and hence reduces the whole degradation rate (shown in Fig. 5.9). The extracted degradation parameters are listed in Table 5.1. Floating-body mode displays a more severe aging effects than that of the unfloating-body mode.

The bipolar transistor is also responsible for electron injection into the buried oxide [65]. Post-stress monitoring of the back channel shows that the current is lower in the reverse-mode than in the direct-mode (shown in Fig. 5.10). The inhomogeneous back interface defects are *effective*, not *virtual* as they subsist even if the front interface defects are masked, by accumulating the top interface during the test (shown in Fig. 5.10). We have pointed out that different features were observed when the measurements were made under the body floating or unfloating condition.

A number of unusual post-stress measurements were made and will be discussed in more detail: modification of the breakdown voltage and kink behavior, influence of V_{ds} scanning from 0 to 7.5 V and vice-versa on $I_{ds}(V_{ds})$ plots (see Fig. 5.11), etc. It is noted that, after front-channel stress, the efficiency of the back-gate controlled bipolar transistor is reduced in the reverse-mode of operation. This is explained by the influence of newly created recombination centers on the bipolar gain. Figure 5.12 shows a possible hot-hole injection into the buried oxide (BOX) during the stress of front transistor at the accumulation of back channel. For the BOX of SIMOX, the

non-stoichiometric SiO_2 structure assists the injected carriers to be trapped inside BOX. The subthreshold slope of the back transistor exhibits a nearly parallel shift from the original slope. The injected carriers perform thermionic emission as well as tunneling into BOX [79]. Figure 5.13 represents the power relationship between the threshold voltage shift and the stress time ($\Delta V_{t1} = t^n$), where n is 0.335 and 0.352 for the floating- and the unfloating-body mode, respectively.

Finally, studies of the stress of the floating-body devices varying with the front-gate bias and the channel length were made. The results of the extracted degradation parameters are list in Table 5.2 and 5.3, respectively. The trend of front-gate bias is consistent with the prediction of Fig. 5.6. For channel-variation stress, the discrepancy of degradation parameters is small. Such situation is most likely attributed to the fact that shorter channel length has larger current injection which may suppress the parasitic bipolar gain as the high level injection occurs. We have also modified SPICE to include the series association of the two channel regions (short defective and long non-defective zones) [80]. This allows the successful simulation of the typical properties of the degraded MOSFET: the transconductance overshoot and asymmetry of the S–D and D–S characteristics.

5.4 Conclusion

From previous experimental and simulation results, an n-channel PD SOI MOSFET with floating-body connection encounters more severe aging effects than that of the unfloating-body mode. Although floating-body PD SOI structure has several advantages over the bulk CMOS (e.g., low-V_{ds} current enhancement in low voltage application [81], reduction of parasitic capacitance, simple isolation, capability of operating at higher temperature, radiation hardness, etc.), the solutions in processing and structure are necessary for the PD SOI devices to enter the mainstream IC technology. The possible solutions to reduce parasitic bipolar effects are (i) increasing

the back channel doping to suppress current gain; (ii) decreasing the emitter (source) Gummel number in the source junction; (iii) increasing the source to drain area ratio, and (iv) using a body contact. Using the body contact will trade off the packing density. Thus, a structure modification is employed to reduce the maximum electric field near the drain junction: (i) increasing the doping in the n^- region of the LDD; (ii) sloped-junction LDD [82], and (iii) halo structure with low-high active-region doping [4]. Besides the solutions mentioned above, the reduction of hydrogen and moisture contents during processing is another good approach.

Table 5.1 Results of the degradation parameter extraction for the PD SOI NMOSFET's after various periods of stress at $V_{ds} = 7.5$ V, $V_{g1} = 3$ V, and $V_{g2} = 0$ V. Here FB and GB are for the floating- and unfloating-body stress, respectively.

Time (sec)	W/L	FB/GB	ΔV_{t1} (mV)	ΔL (μm)	ΔN_{it1} (10^{10}eV^{-1}cm^{-2})	ΔN_{ox1} (10^{9}cm^{-2})
10^2	10/1	FB	12	0.02	1.20	1.39
10^3	10/1	FB	36	0.07	3.82	2.76
10^4	10/1	FB	55	0.16	5.98	3.35
5×10^4	10/1	FB	107	0.30	10.31	16.92
10^2	10/1	GB	8	0.017	0.85	0.12
10^3	10/1	GB	25	0.06	2.64	2.04
10^4	10/1	GB	38	0.10	4.04	2.86

Table 5.2 Results of the degradation parameter extraction for the PD SOI NMOSFET's with various channel lengths after stress at $V_{ds} = 7.5$ V, $V_{g1} = 3$ V, $V_{g2} = 0$ V, time $= 10^3$ sec and floating-body.

W/L	ΔV_{t1} (mV)	ΔL (μm)	ΔN_{it1} (10^{10}eV^{-1}cm^{-2})	ΔN_{ox1} (10^{9}cm^{-2})
10/1.0	36	0.07	3.82	2.76
10/1.2	34	0.07	3.81	1.02
10/1.4	32	0.06	3.62	8.63
10/1.6	31	0.06	3.53	2.52

Table 5.3 Results of the degradation parameter extraction for the PD SOI NMOSFET's after various front-gate voltage stresses at V_{ds} = 7.5 V, V_{g2} = 0 V, time = 10^3 sec and floating-body.

V_{g1} (V)	W/L	ΔV_{t1} (mV)	ΔL (μm)	ΔN_{it1} (10^{10}eV^{-1}cm^{-2})	ΔN_{ox1} (10^{9}cm^{-2})
2	10/1.6	23	0.04	2.48	1.83
3	10/1.6	31	0.06	3.53	2.50
4	10/1.6	22	0.03	2.13	3.60
5	10/1.6	13	0.01	0.57	8.02

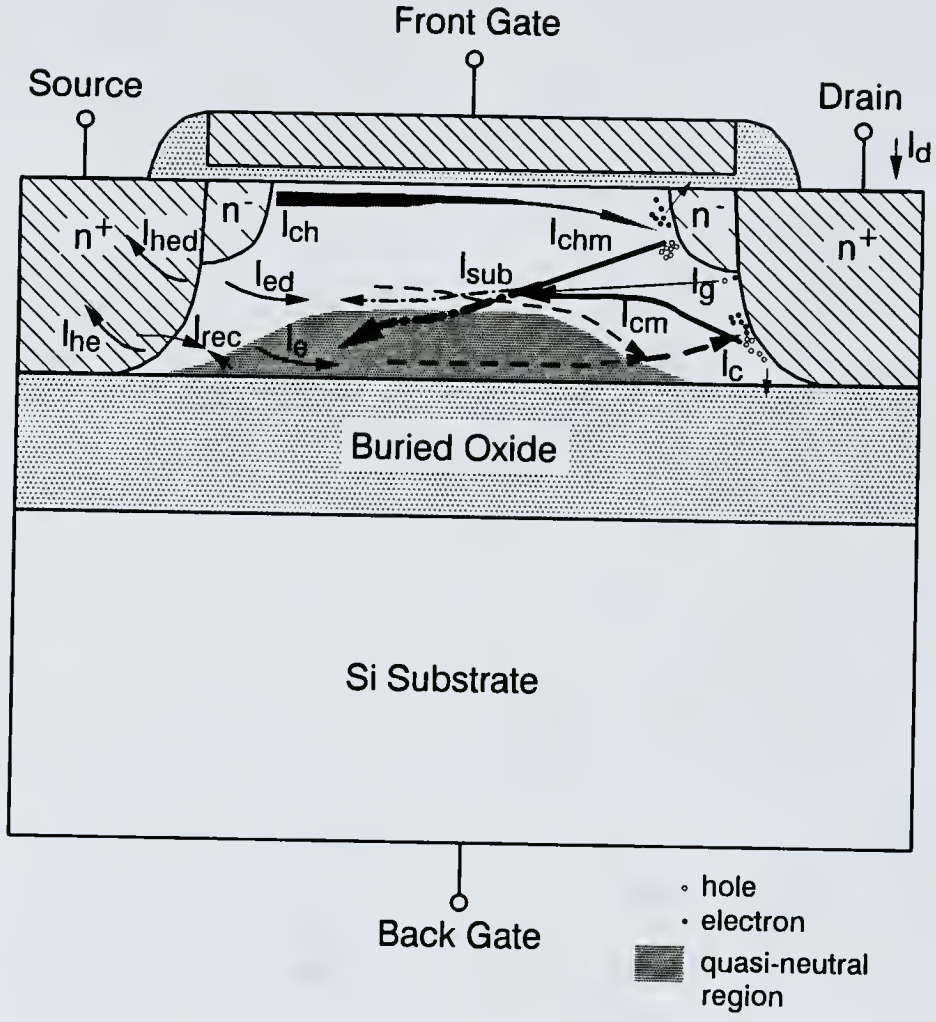

Figure 5.1: Schematic diagrams showing current flow in the SOI nMOSFET's operated in the saturation regime.

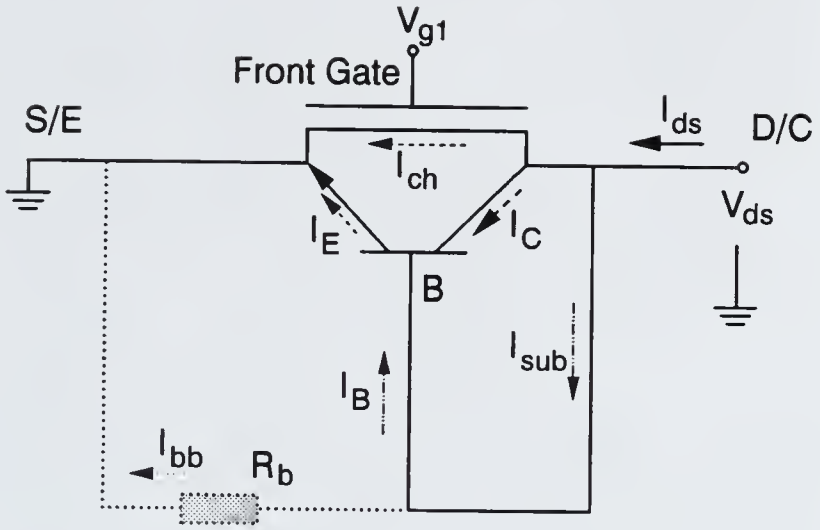

Figure 5.2: The current components in a body-floating and a body-contacted (dashed line) SOI nMOSFET's operating in the weak avalanche regime.

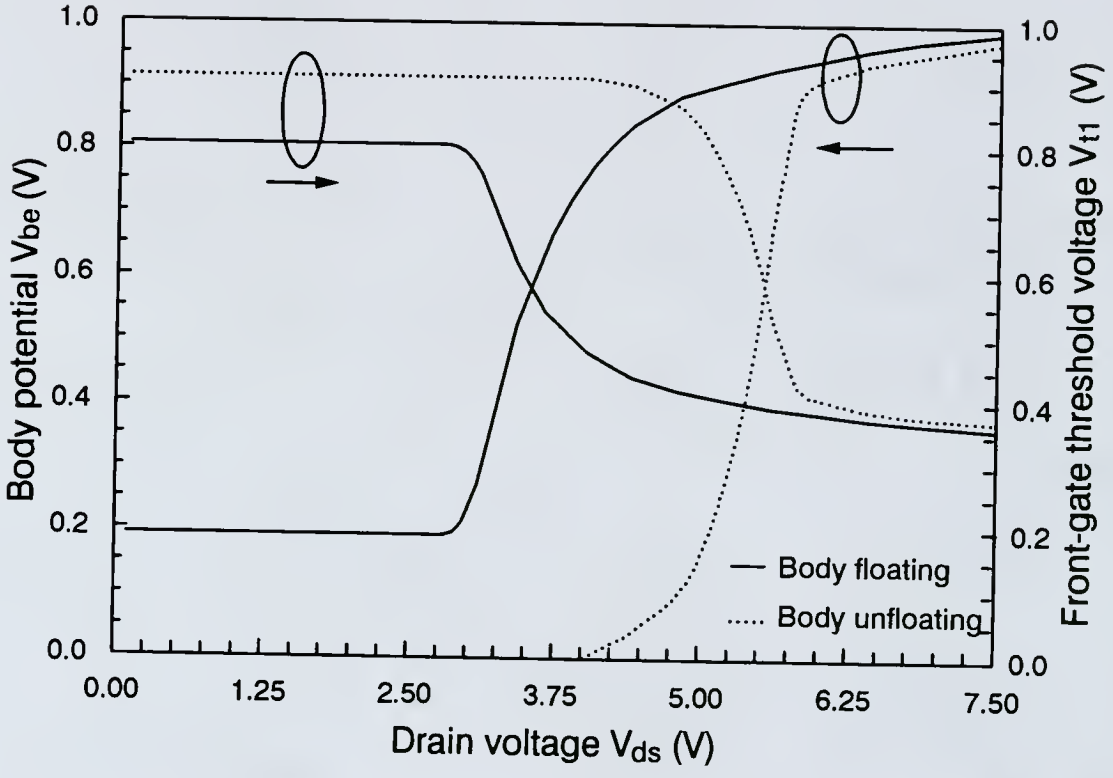

Figure 5.3: Simulated quasi-Fermi-level separation in the body-source junction and front-gate threshold voltage versus drain-source bias for the floating- and unfloating-body PD SOI nMOSFET.

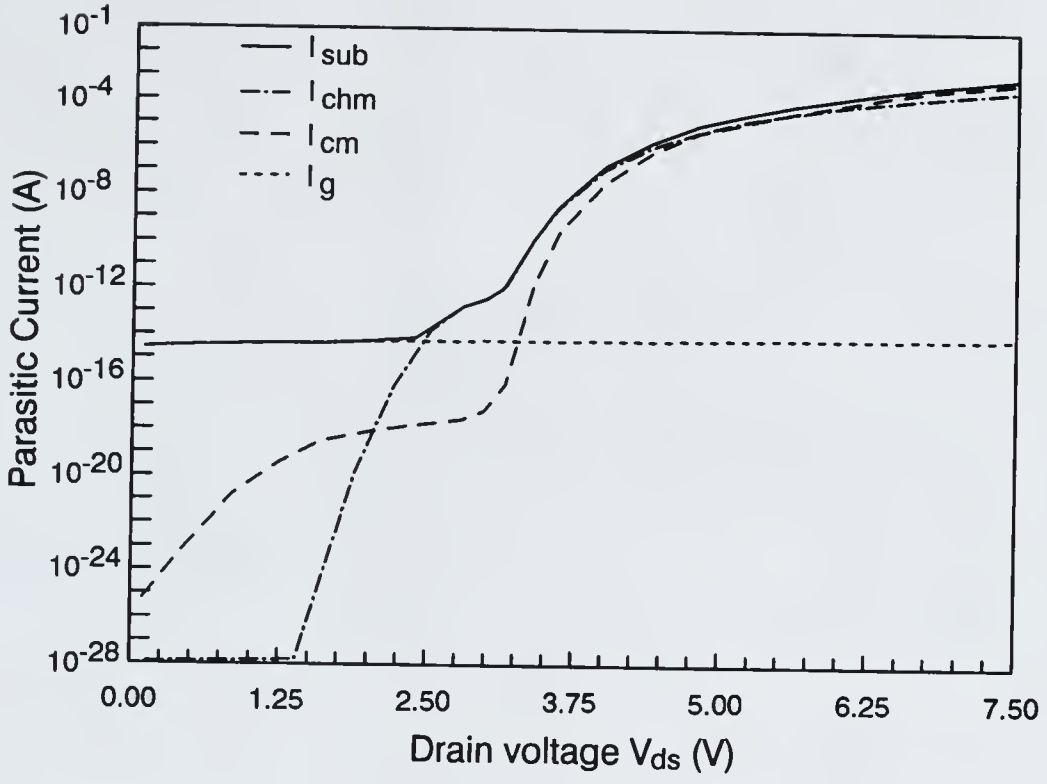

Figure 5.4: The parasitic hole-current components of the floating-body SOI nMOSFET extracted from the simulation in Fig. 5.3.

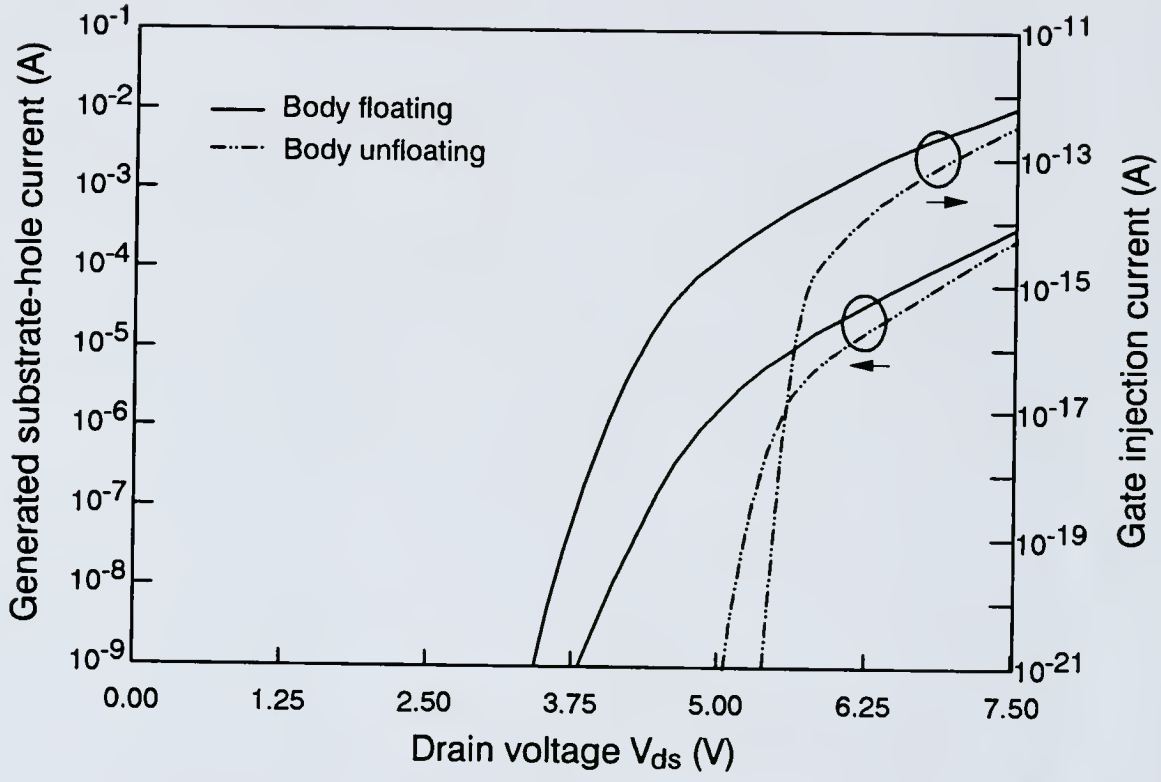

Figure 5.5: The substrate hole current and the gate-inject electron current obtained from simulations in Fig. 5.3.

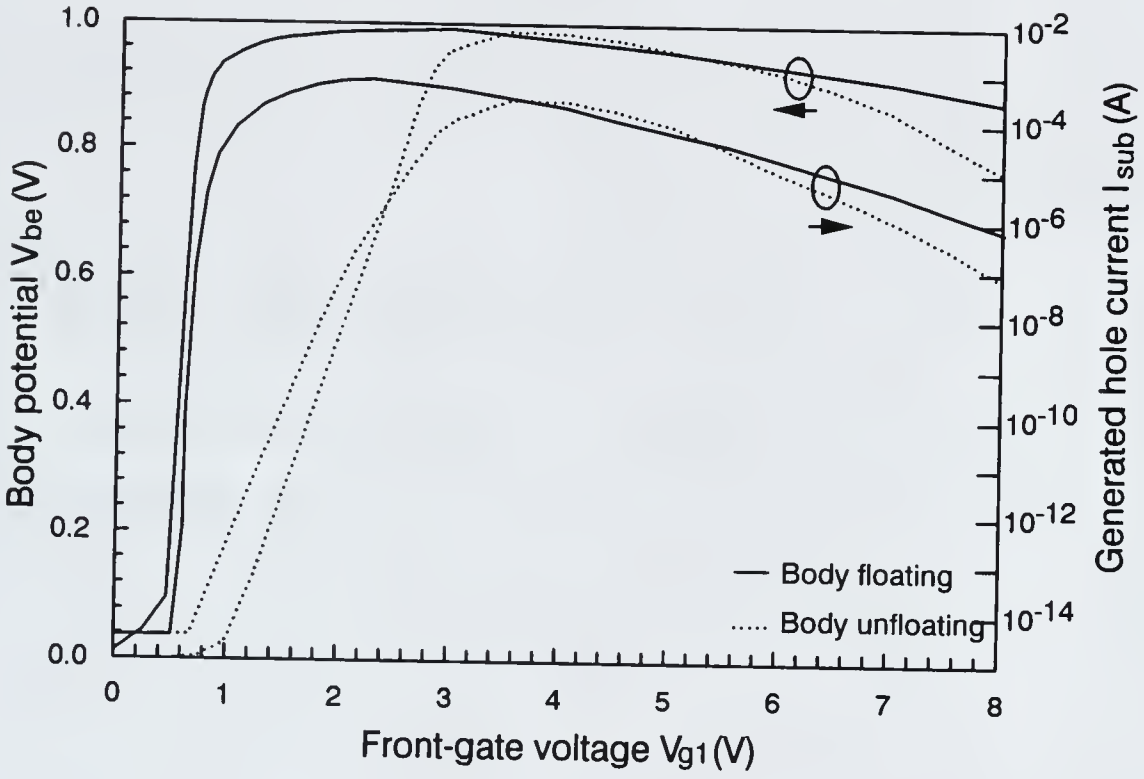

Figure 5.6: Simulated quasi-Fermi-level separation in the body-source junction and generated hole current versus front-gate bias for the floating- and unfloating-body PD SOI nMOSFET at $V_{ds} = 7.5V$.

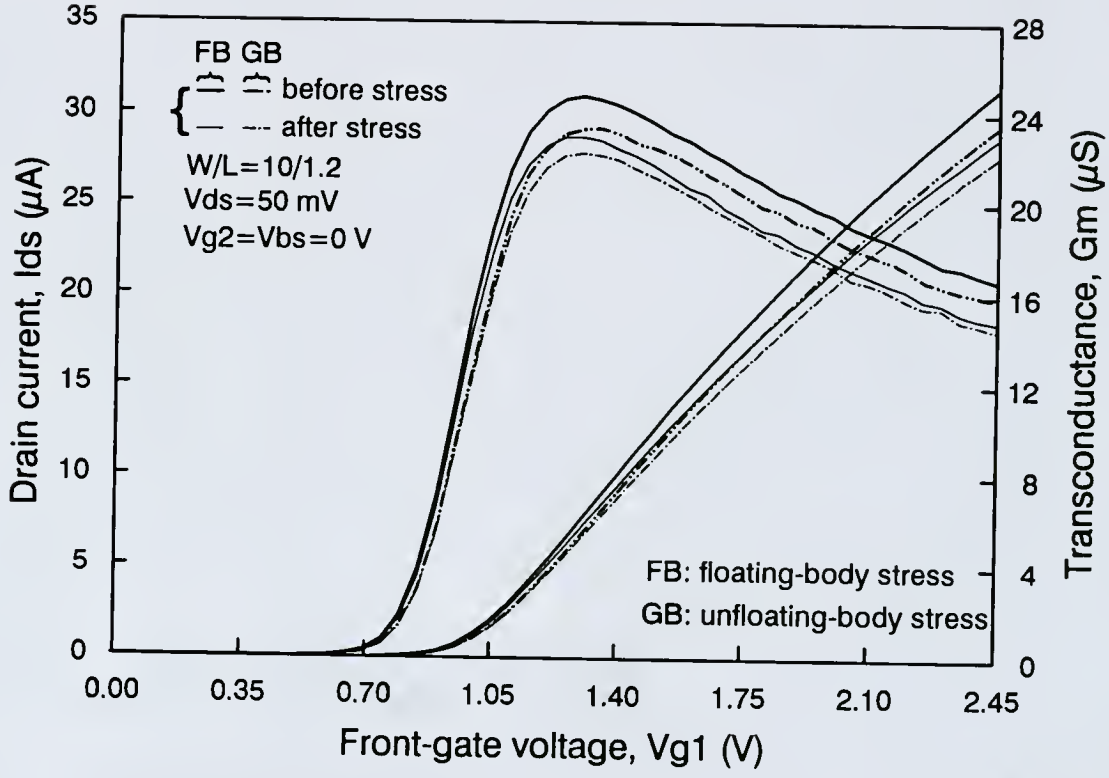

Figure 5.7: Measured $I_{ds} - V_{g1}$ and $g_m - V_{g1}$ characteristics of the PD SOI nMOSFET after stress at body floating and unfloating (stress: $V_{ds} = 7.5V$, $V_{g1} = 3V$, $V_{g2} = 0V$, and time = 10^3 sec).

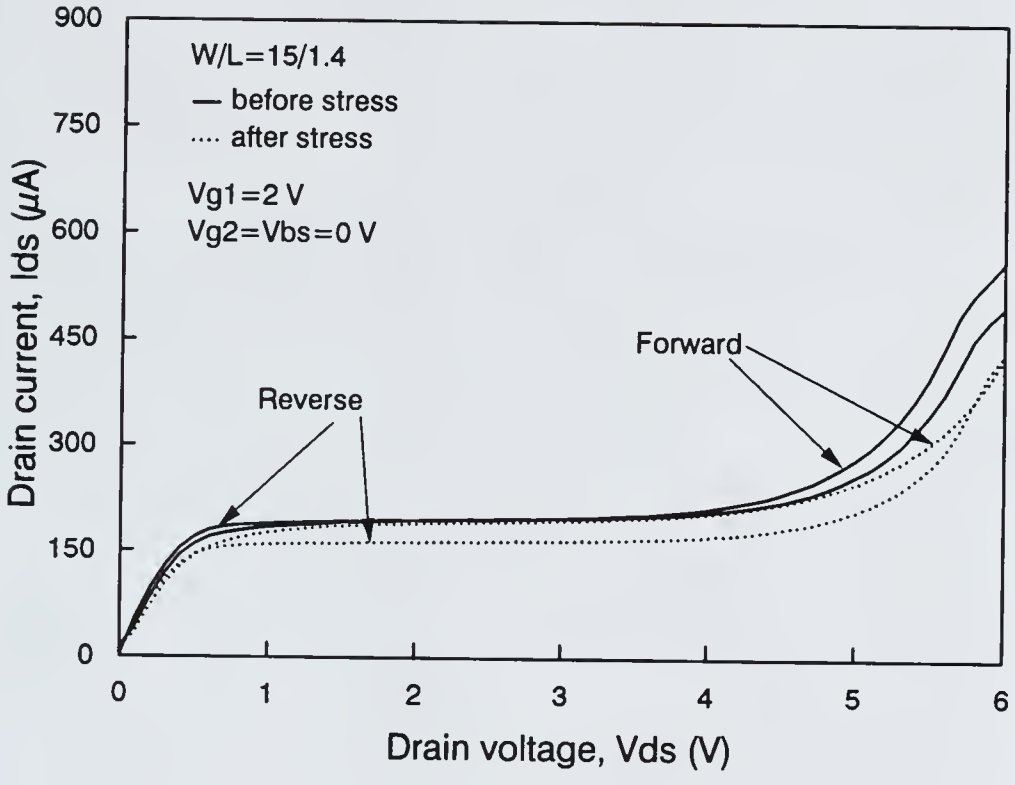

Figure 5.8: Measured $I_{ds} - V_{ds}$ characteristics of the PD SOI nMOSFET after stress at $V_{ds} = 8.5V$, $V_{g1} = 3V$, $V_{g2} = 0V$, time $= 10^4$ sec, and body floating.

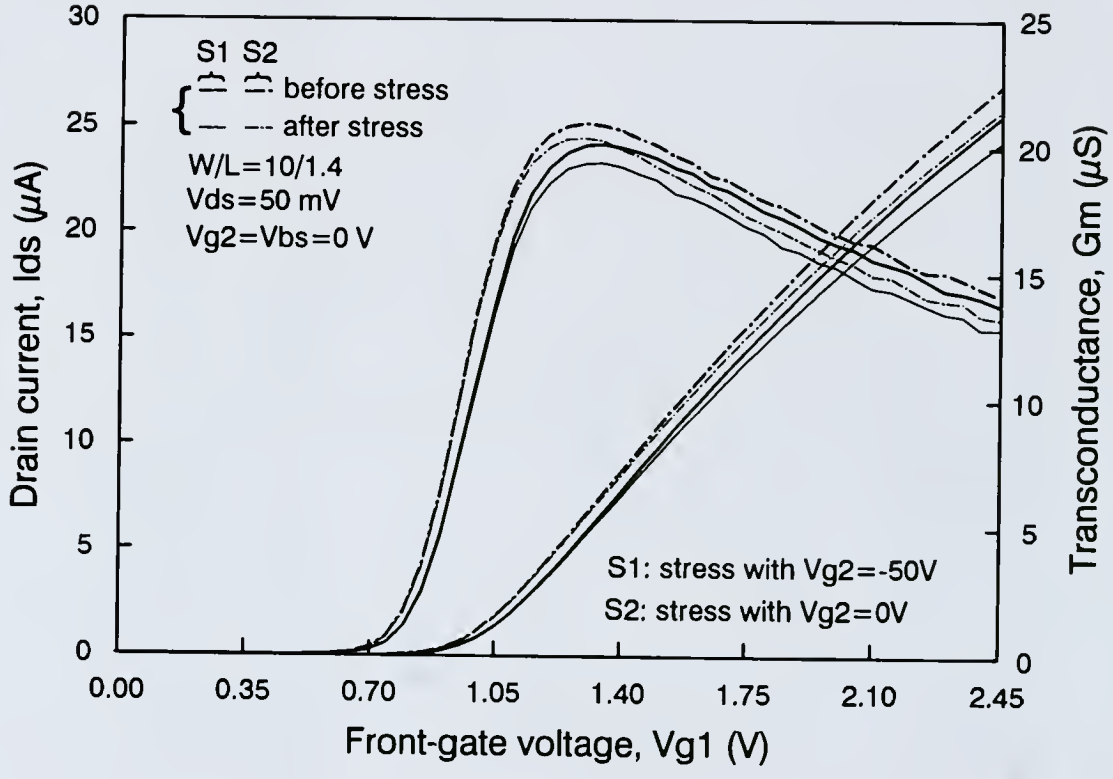

Figure 5.9: Measured $I_{ds} - V_{g1}$ and $g_m - V_{g1}$ characteristics of the PD SOI nMOSFET after stress at back interface accumulated ($V_{g2} = -50V$) and depleted ($V_{g2} = 0V$) (stress: $V_{ds} = 7.5V$, $V_{g1} = 3V$, and time = 10^3 sec).

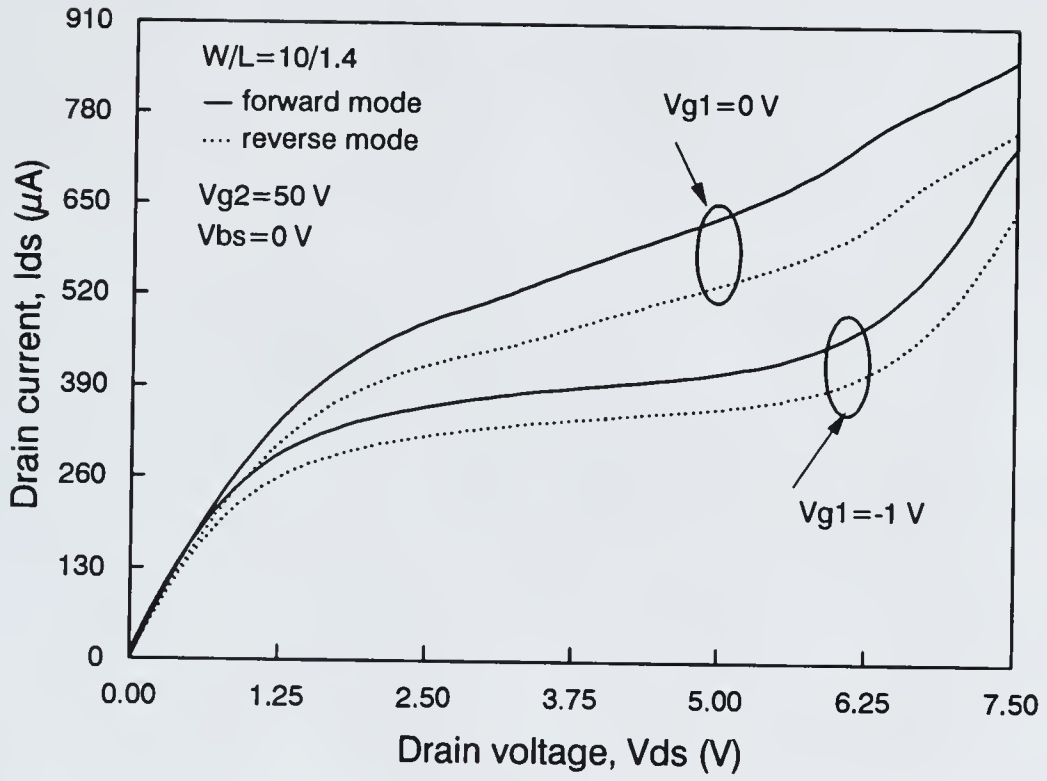

Figure 5.10: Measured $I_{ds} - V_{ds}$ characteristics of the PD SOI nMOSFET in depleted ($V_{g1} = 0V$) and accumulated ($V_{g1} = -1V$) front interface after stress at $V_{ds} = 7.5V$, $V_{g1} = 3V$, $V_{g2} = -50V$, time = 10^3 sec, and body floating.

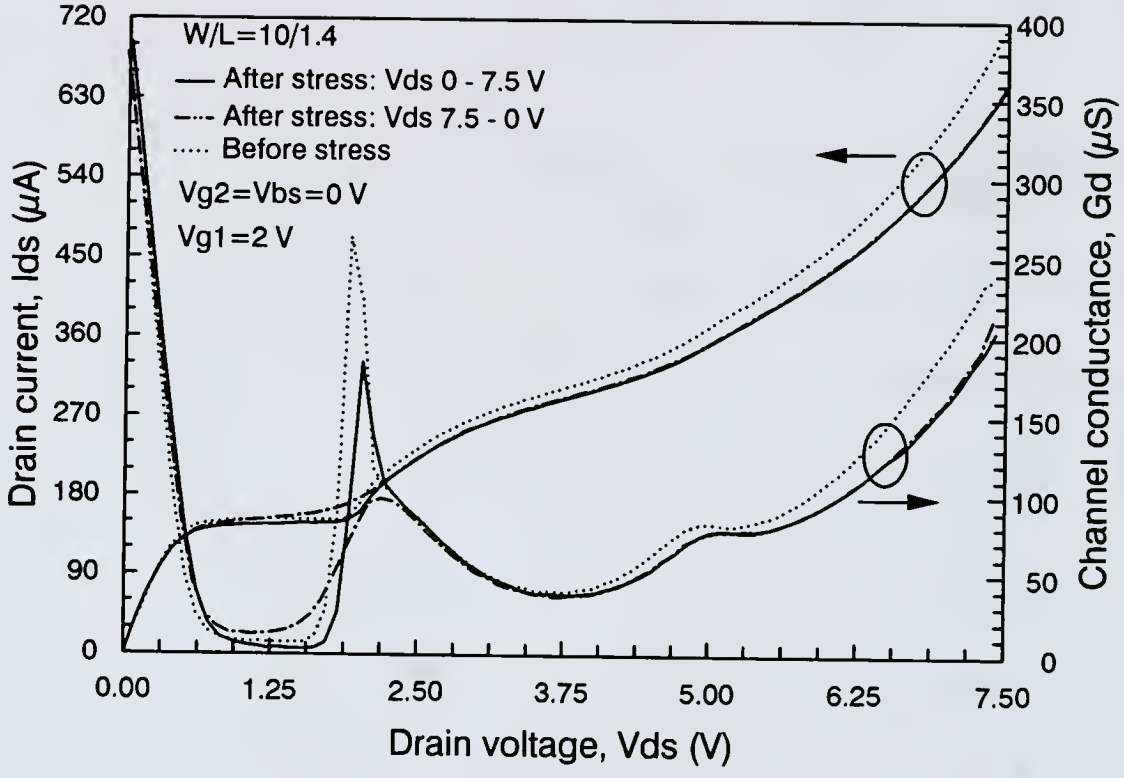

Figure 5.11: The $I_{ds} - V_{ds}$ characteristics of the PD SOI nMOSFET measured under forward ($0 \rightarrow 7.5V$) and backward ($7.5 \rightarrow 0V$) V_{ds} scanning after the same floating-body stress shown in Fig. 5.7.

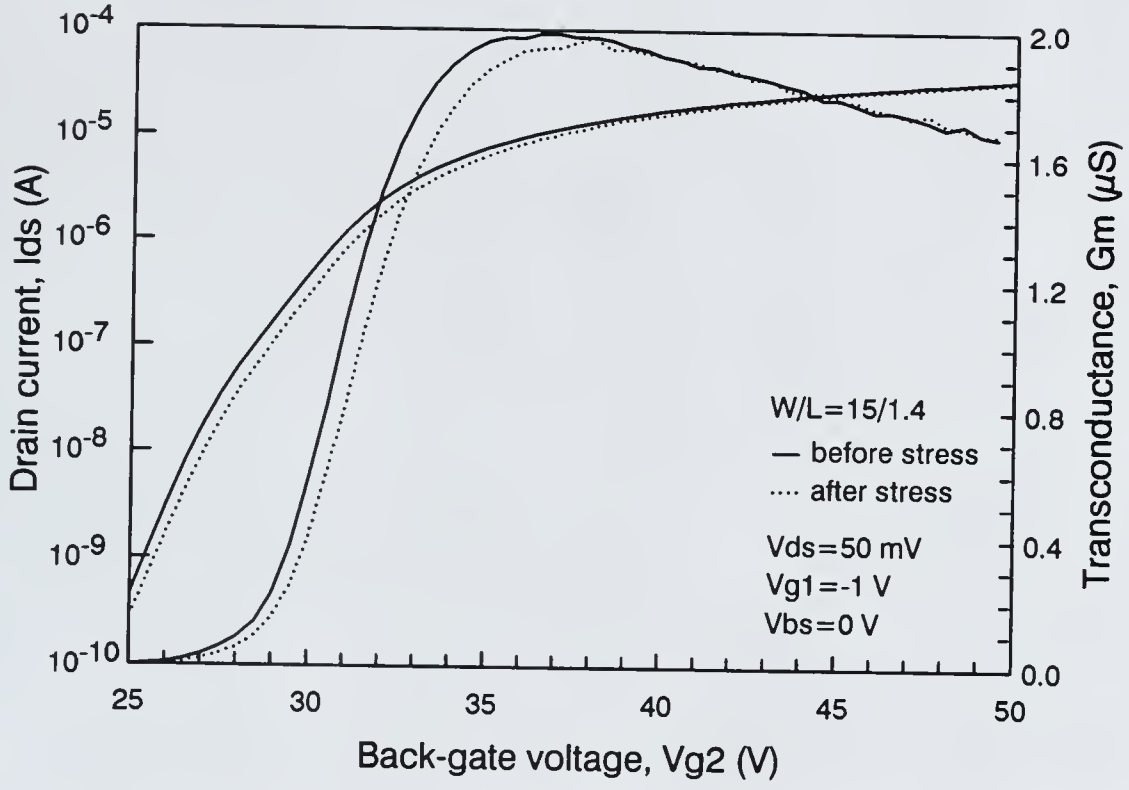

Figure 5.12: Measured back-channel subthreshold and transconductance characteristics of the PD SOI nMOSFET after stress at $V_{ds} = 8.5V$, $V_{g1} = 3V$, $V_{g2} = -50V$, time $= 2 \times 10^3$ sec, and body floating.

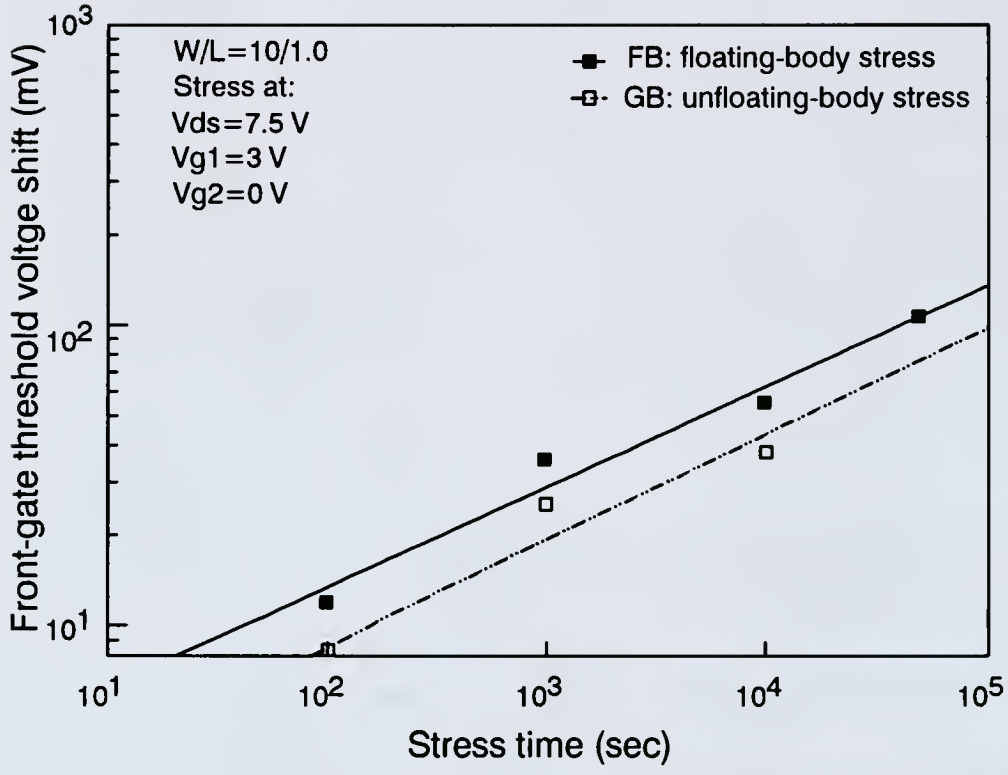

Figure 5.13: Extracted front-gate threshold voltage shift after various periods of stress at the same stress conditions shown in Fig. 5.7.

CHAPTER 6
MODELING AND PARAMETER EXTRACTION OF GATE-ALL-AROUND NMOS/SOI TRANSISTORS IN LINEAR REGION

6.1 Introduction

Ultra-thin fully depleted (FD) silicon-on-insulator (SOI) with gate electrode on both the front and backside of the silicon film exhibits some advantages over the standard thick film SOI counterpart, such as sharper subthreshold slope, higher transconductance [87], reduction of short-channel effects [88], elimination of undesirable transient and hysteresis effects [89], and good low frequency noise characteristics [90]. The presence of a thin gate oxide (see Fig. 6.1) in the backside of silicon film of the gate-all-around (GAA) device is suitable for applications in radiation-hardness circuits [91]. In addition, the good low frequency noise characteristic is particularly desirable for analog circuit applications. The fabrication process of GAA devices is almost identical to that of the standard MOSFET's with only one extra mask step required [87].

Due to the geometric asymmetry, the non-ideal GAA transistor can be considered as a combination of one long-double-gate and two edge-gate transistors connected in parallel (see Figs. 6.1 and 6.2). The edge-gate transistors are responsible for the early conduction and the presence of a hump in the subthreshold region [92]. Models for the constant potential [93] and moderate inversion [94] have been derived for the double-gate transistor structure in the regions below and near threshold by neglecting the effect of interface defects. Although previous work by Balestra *et al.* [95] claimed that the effect of interface defects is negligible, our experimental results revealed that this effect is indeed important over the entire subthreshold region (see Fig. 6.4). An

underestimation of the subthreshold slope occurs when the effect of interface defects is neglected. In the strong inversion region, the amount of induced inversion charges is much larger near the surface than at the center of silicon film [87]. Thus, the mobility degraded by the surface-roughness scattering [87, 76] reduces the advantage of volume inversion. In this paper, models for the GAA SOI MOSFET operating in subthreshold and moderate inversion regions are derived by taking into account the effect of interface defects, while in strong inversion region model is developed by considering the effects of parasitic resistance and surface scattering. Using our models, the decoupling of surface scattering parameters from other device parameters such as parasitic series resistance can be obtained by measuring the $(I_d - V_{gs})$ characteristics in the strong inversion region. To verify our models, the extracted parameters were employed in our models, and the simulated results were compared with the measured $(I_d - V_{gs})$ characteristics.

6.2 Theory

The GAA device may be considered as three MOS transistors with one long-double-gate transistor and two edge-gate transistors (two edges of the silicon bridge as shown in Figs. 6.1 and 6.2) connected in parallel. The long-double-gate transistor will be discussed first, followed by the edge-gate transistors.

According to volume inversion characteristics of the double-gate structure in an SOI MOSFET's [93, 95], the charge sheet model is inadequate to depict the characteristics of the GAA device. Since both the depletion charges and minority carriers are presented in the silicon film, the Poisson equation can be expressed as

$$\frac{d^2\phi(x,y)}{dx^2} = q/\epsilon_{Si}\left(N_A + \frac{n_i^2}{N_A}e^{[\phi(x,y)-V(y)]/\phi_t}\right) \tag{6.1}$$

where $\phi(x,y)$ is the potential in the silicon film referenced to the Fermi level in the neutral region of the equivalent bulk MOS transistor with a doping density of N_A;

$V(y)$ is the channel potential which is assumed to be independent of x; ϕ_t=kT/q is the thermal voltage; ϵ_{Si} is the permittivity of silicon; k is the Boltzmann constant; T is the temperature, and n_i is the intrinsic carrier concentration.

Due to the symmetry property of a GAA-device, the electric field is equal to zero at the center of silicon film along the x-direction (see Fig. 6.1). Solving eqn. (6.1), the conduction charge is given by

$$\begin{aligned} Q_n(y) &= 2\int_0^{t_{Si}/2}\left(\epsilon_{Si}\frac{d^2\phi(x,y)}{dx^2} - qN_A\right)dx \\ &= 2\epsilon_{Si}\mathcal{E}_s(y) - qN_A t_{Si} \end{aligned} \tag{6.2}$$

where t_{Si} is the silicon film thickness; $qN_A t_{Si}$ is the depletion charge, and $\mathcal{E}_s(y)$ is the surface electric field, which can be obtained by solving eqn. (6.1). The result yields

$$\mathcal{E}_s(y) = \sqrt{2qN_A/\epsilon_{Si}\left((\phi_s - \phi_c) + \phi_t\frac{n_i^2}{N_A^2}\left(e^{(\phi_s - V(y))/\phi_t} - e^{(\phi_c - V(y))/\phi_t}\right)\right)} \tag{6.3}$$

where ϕ_s is the surface potential, and ϕ_c is the potential at the center of silicon film. Thus, the drain current can be expressed in terms of the long-double-gate transistor width W, effective mobility μ_{eff}, conduction charges, and the gradient of the channel potential along the drain-source direction (y direction)

$$I_{d1} = W\mu_{eff}Q_n(y)\frac{dV(y)}{dy} \tag{6.4}$$

By applying Gauss' law to the Si/SiO_2 interface, the gate voltage V_{gs} can be expressed in terms of ϕ_s, N_{ss}, C_{ox}, and the channel potential $V(y)$ as

$$V_{gs} = V_{FB} + \phi_s(y) + \frac{qN_{ss}(\phi_s(y) - V(y))}{C_{ox}} + \frac{\epsilon_{Si}\mathcal{E}_s(y)}{C_{ox}} \tag{6.5}$$

where V_{FB} is the flat-band voltage; N_{ss} is the surface state density per unit area, and C_{ox} is the oxide capacitance per unit area.

6.2.1 Weak Inversion

From eqn. (6.1), it is noted that $(\phi_s - \phi_c)$ can be approximated by $Q_b/8C_{Si}$ [93]; where $Q_b = qN_A t_{Si}$ is the depletion charge in the fully depleted silicon film, and

$C_{Si} = \epsilon_{Si}/t_{Si}$ is the capacitance associated with the silicon film. Using the relationship of surface potential (ϕ_s), film-center potential (ϕ_c) and Tylor's series expansion of ϕ_s at $1.5\phi_F$ ($\phi_F = \phi_t \ln(N_A/n_i)$) [96], eqn. (6.3) becomes

$$\mathcal{E}_s^*(y) = \sqrt{2qN_A/\epsilon_{Si}\left(Q_b/8C_{Si} + \phi_t \frac{n_i^2}{N_A^2} e^{(1.5\phi_F - V(y))/\phi_t}\left(1 - e^{-Q_b/8C_{Si}\phi_t}\right)\right)} \tag{6.6}$$

and

$$\mathcal{E}_s(y) = \mathcal{E}_s^*(y) + (\phi_s - 1.5\phi_F)\,(C_n^*/2\epsilon_{Si}) \tag{6.7}$$

where C_n^* is defined as $\frac{dQ_n(y)}{d\phi_s}|_{\phi_s = 1.5\phi_F}$.

Using eqns. (6.5), (6.6), and (6.7) and $C_{ox} \gg C_{ss}$ ($C_{ss} = qN_{ss}$), ϕ_s can be expressed as

$$\phi_s \simeq (V_{gs} - V_{gs}^*)/n^* + 1.5\phi_F \tag{6.8}$$

where $V_{gs}^* = V_{FB} + 1.5\phi_F + 1.5\phi_F C_{ss}/C_{ox} + \epsilon_{Si}\mathcal{E}_s^*(y)/C_{ox}$ and $n^* = (C_{ox} + C_n^*/2 + C_{ss})/C_{ox}$.

In the weak inversion region, the $(\phi_s - \phi_c)$ term is dominated in eqn. (6.3) [93, 95]. Thus, eqn. (6.2) can be reduced to

$$Q_n(y) = 4C_{Si}\phi_t e^{(\phi_s - 2\phi_F - V(y))/\phi_t}\left(1 - e^{-Q_b/(8C_{Si}\phi_t)}\right) \tag{6.9}$$

Now, assuming a constant mobility (i.e., $\mu_{eff} = \mu_0$, μ_0 is the low field mobility), which is valid in the weak inversion region, from eqns. (6.8) and (6.9), the drain current in the linear regime can be expressed by

$$\begin{aligned} I_{d1} &= \frac{W}{L}\mu_0 \int_0^{V_{ds}} Q_n(y)dV(y) \\ &= \frac{W}{L}\mu_0 4C_{Si}\phi_t V_{ds} e^{((V_{gs} - V_g^*)/n_1) - 0.5\phi_F)/\phi_t}\left(1 - e^{-Q_b/(8C_{Si}\phi_t)}\right) \end{aligned} \tag{6.10}$$

where L is the channel length; V_{ds} is the drain to source bias; $V_g^* = V_{FB} + 1.5\phi_F + 1.5\phi_F C_{ss}/C_{ox} + Q_b/2C_{ox}$, and $n_1 \simeq (C_{ox} + C_{ss})/C_{ox}$ (in the weak inversion $C_{ox} \gg C_n^*$).

Due to charge sharing, part of the charges under the edge gate is controlled by the long-double gate [97](see Fig. 6.2). A fraction of the depletion charges controlled by the edge-gate transistor is

$$F = 1 - \frac{x_d}{W_e} = 1 - \frac{x_d}{t_{Si}} \tag{6.11}$$

where $x_d = t_{Si}/2$ and $F = 1/2$ for the fully depleted silicon film . In the ultra-thin film SOI structure ($W \gg W_e$), the ratio of the depletion charge controlled by the edge-gate transistor and the long-double-gate transistor is equal to $t_{Si}/2W$.

Assuming that the edge-gate transistors have identical doping concentration, oxide charge, and interface charge as the long-double-gate transistor, the drain current of the edge-gate transistors in the linear regime can be expressed as

$$I_{d2} = \frac{W_e}{L}\mu_0 4 C_{Si}\phi_t V_{ds} e^{((V_{gs}-V_{ge}^*)/n_1)-0.5\phi_F)/\phi_t}\left(1 - e^{-Q_b'/(8C_{Si}\phi_t)}\right) \tag{6.12}$$

Here W_e is the width of the edge-gate transistors; V_{ge}^* is the V_g^* with Q_b replaced by Q_b' $(= Q_b t_{Si}/2W)$. Thus, the total drain current is equal to the sum of the drain currents of the edge-gate and long-double-gate transistors.

The interface state density can be extracted from the slope (S_ℓ) of $\log_{10}(I_d)$ versus V_{gs}

$$N_{ss} = \frac{C_{ox}}{q}\left\{[(\ln 10)S_\ell \phi_t]^{-1} - 1\right\} \tag{6.13}$$

And the channel conductance g_d is given by

$$g_d = \mu_0 4 C_{Si}\phi_t e^{V_{gs}/(n_1\phi_t)} e^{-0.5\phi_F/\phi_t}(kk1 + kk2) \tag{6.14}$$

where

$$kk1 = \frac{W}{L}\left(1 - e^{-Q_b/(8C_{Si}\phi_t)}\right) e^{-V_g^*/(n_1\phi_t)}$$

$$kk2 = \frac{W_e}{L}\left(1 - e^{-Q_b'/(8C_{Si}\phi_t)}\right) e^{-V_{ge}^*/(n_1\phi_t)}$$

6.2.2 Strong Inversion

Similar to the derivation in weak inversion, the long-double-gate transistor will be discussed first, followed by the edge-gate transistors. Due to the volume inversion mechanism of GAA devices [87, 93, 95], the conventional definition of threshold at surface band bending of $2\phi_F$ is inadequate. Therefore, the transconductance change (TC) method [98] is employed to determine the threshold voltage. As shown in Appendix D, the surface potential at threshold is given by

$$\begin{aligned}\phi_s^* &= 2\phi_F + V(y) + \phi_t \ln\left(\frac{C_{ox}/(4C_{Si})\left(C_{ox}\phi_t/Q_b + \sqrt{C_{ox}^2\phi_t^2/Q_b^2+1}\right)}{1-e^{-Q_b/(8C_{Si}\phi_t)}}\right)\\ &= 2\phi_F + V(y) + \Delta\phi \end{aligned} \tag{6.15}$$

Solving eqns. (6.2), (6.5), and (6.15), yields the conduction charge $Q_n(y)$ and the threshold voltage V_T

$$Q_n(y) = 2C_{ox}\left(V_{gs} - V_T - V(y)\right) \tag{6.16}$$

and

$$V_T = 2\phi_F + \Delta\phi + V_{FB} + (2\phi_F + \Delta\phi)\frac{C_{ss}}{C_{ox}} + \frac{Q_b}{2C_{ox}}\sqrt{1+\eta} \tag{6.17}$$

where

$$\eta = \frac{2\phi_t C_{ox}}{Q_b}\left[C_{ox}\phi_t/Q_b + \sqrt{1+\left(C_{ox}\phi_t/Q_b\right)^2}\right] \tag{6.18}$$

In the double-gate structure, the $\sqrt{1+\eta}$ term in eqn. (6.17) is a correction factor of the depletion charges at the threshold for the silicon film of the fully-depleted GAA devices.

The edge-gate transistor has the similar conduction charge ($Q_{ne}(y)$) and the threshold voltage (V_{Te}) as the long-double-gate transistor except that Q_b is replaced by $Q_b' = Q_b t_{Si}/2W$ in eqns. (6.15), (6.16), (6.17), and (6.18).

In the strong inversion region, the amount of induced inversion charges is much larger near the surface than at the center of silicon film [87]. Thus, the mobility

is no longer constant along the channel, and an effective mobility degraded by the surface-roughness scattering [87, 76] can be expressed as [76]-[101]

$$\begin{aligned} \mu_{eff} &= \mu_0/(1+\mu_0/\mu_{sr}) \\ &= \mu_0/(1+[\theta_1(Q_n+\alpha Q_b)]) \end{aligned} \tag{6.19}$$

where θ_1 is equal to $1/4\epsilon_{Si}\mathcal{E}_c$; μ_0 is the low field mobility [76]; μ_{sr} is the mobility due to surface-roughness scattering [99, 100]; $\mathcal{E}_c$ is the critical field often used in describing the degradation of mobility with gate voltage [76], and α is a constant equal to 2 in n-type devices at room temperature [102].

For small drain bias, using eqns. (6.4) and (6.19) and the conduction charges $Q_n(y)$ and $Q_{ne}(y)$ derived above , the total drain current is given by

$$I_d \approx 2\beta_0\frac{(V_{gs}-V_T)V_{ds}}{1+\theta(V_{gs}-V_T^*)} + 2\beta_0'\frac{(V_{gs}-V_{Te})V_{ds}}{1+\theta(V_{gs}-V_{Te}^*)} \tag{6.20}$$

where

$$\begin{aligned} \theta &= \theta_1(2C_{ox}) \\ \beta_0 &= C_{ox}\mu_0 W/L \\ V_T^* &= V_T - \alpha Q_b/(2C_{ox}) \\ \beta_0' &= C_{ox}\mu_0 W_e/L \\ V_{Te}^* &= V_{Te} - \alpha Q_b'/(2C_{ox}) \end{aligned}$$

Now, including the series resistance at the source and drain (assuming $R_s = R_d$) and the domination of long-double-gate transistor in eqn. (6.20), the drain current can be expressed approximately by

$$I_d \simeq 2C_{ox}W\mu_{eff}(V_{gs}-V_T)V_{ds}/L \tag{6.21}$$

$$\simeq \frac{2\beta_0(V_{gs}-V_T)V_{ds}}{1+(\theta+4\beta_0 R_s)(V_{gs}-V_T)+\theta(V_T-V_T^*)} \tag{6.22}$$

The gate transconductance, defined by $g_m = dI_d/dV_{gs} = g_{ml} + g_{me} \approx g_{ml}$, is given by

$$g_m \simeq \frac{2\beta_0 V_{ds}\left[1+\theta(V_T - V_T^*)\right]}{\left[1+(\theta+4\beta_0 R_s)(V_{gs}-V_T)+\theta(V_T-V_T^*)\right]^2} \tag{6.23}$$

where g_{ml} and g_{me} are the transconductance of the long-gate and edge-gate transistor, respectively.

The low-field mobility μ_0 can be obtained by extrapolating the measured μ_{eff} versus $(V_{gs} - V_T)$ (eqn. (6.21)) curve at $V_{gs} = V_T$. Rearranging eqn. (6.22) and combining the measured value of μ_0 yields

$$\frac{(V_{gs}-V_T)V_{ds}}{I_d} = S_1(V_{gs}-V_T) + Int_1 \tag{6.24}$$

where

$$S_1 = \frac{\theta + 4\beta_0 R_s}{2\beta_0} \quad \text{and} \quad Int_1 = \frac{1}{2\beta_0} + \frac{\theta}{2\beta_0}(V_T - V_T^*)$$

The series resistance R_s and the mobility degradation factor θ can be extracted from the measured values of S_1 and Int_1 in eqn.(6.24).

6.2.3 Moderate Inversion

The depletion approximation model developed in the weak inversion region is not adequate for describing the current behavior near the threshold in GAA devices. The increase of electron density is not limited to the region near Si/SiO_2 interface, it prevails over the entire silicon film and piles up mainly near the interface as the gate voltage is increased [91]. Both diffusion and drift currents contribute significantly to the value of drain current. Using the first order approximation [94], the potential in eqn. (6.1) can be approximated by the surface potential, and eqn. (6.1) becomes

$$\frac{d^2\phi(x,y)}{dx^2} = \frac{q}{\epsilon_{Si}}\left(N_A + n_s e^{[-\mathcal{E}_s(y)(t_{Si}/2-x)]/\phi_t}\right) \tag{6.25}$$

where n_s is the surface electron concentration which is equal to $n_i^2/N_A \exp((\phi_s(y) - V(y))/\phi_t)$. Solving eqn. (6.25) with the proper boundary conditions (e.g., $\mathcal{E} = 0$ at

the center of Si film, the potential and electric field in the surface, etc.) and Gauss' law (eqn. (6.5)), the potential can be expressed by

$$\begin{aligned}\phi(x,y) &= \frac{qN_A}{2\epsilon_{Si}}(t_{Si}/2-x)^2 + C_1(t_{Si}/2-x) \\ &+ q/\epsilon_{Si}\phi_t^2 n_s/\mathcal{E}_s^2(y)e^{-\mathcal{E}_s(y)(t_{Si}/2-x)/\phi_t} + C_2 \end{aligned} \tag{6.26}$$

where

$$\begin{aligned} C_1 &= \frac{q\phi_t n_s}{\epsilon_{Si}\mathcal{E}_s(y)}e^{-\mathcal{E}_s(y)t_{Si}/(2\phi_t)} - Q_b/(2\epsilon_{Si}) \\ C_2 &= \frac{1}{n_1}\{V_{gs} - V_{FB} + q\phi_t n_s/(\epsilon_{Si}\mathcal{E}_s(y)) \\ &\times \left(\epsilon_{Si}/C_{ox}\left(e^{-\mathcal{E}_s(y)t_{Si}/(2\phi_t)}-1\right) - \phi_t n_1/\mathcal{E}_s(y)\right) - Q_b/(2C_{ox}) + C_{ss}V(y)/C_{ox}\} \end{aligned}$$

and

$$\mathcal{E}_s(y) = -q\phi_t n_s/(\epsilon_{Si}\mathcal{E}_s(y))\left(e^{-\mathcal{E}_s(y)t_{Si}/(2\phi_t)}-1\right) + Q_b/(2\epsilon_{Si}) \tag{6.27}$$

$$\phi_s(y) = q\phi_i^2 n_s/(\epsilon_{Si}\mathcal{E}_s^2(y)) + C_2 \tag{6.28}$$

From eqns. (6.2) and (6.4) and at low drain voltage (the channel potential is linear along the channel), the drain current is obtained by using eqn. (6.5) and numerically solving $\mathcal{E}_s$ in eqn. (6.27), and the result yields

$$I_d = \frac{W}{L}\mu_{eff}\left(2\epsilon_{Si}\mathcal{E}_s - Q_b\right)V_{ds} \tag{6.29}$$

The transconductance g_m can be obtained by solving eqns. (6.5), (6.27), and (6.29), which reads

$$g_m = 2\frac{W}{L}C_{ox}\mu_{eff}V_{ds}\frac{\frac{qn_s}{C_{ox}\mathcal{E}_s n_1}Y}{1-\frac{qn_s}{2C_{Si}\mathcal{E}_s}e^{-\mathcal{E}_s t_{Si}/(2\phi_t)} + \frac{q\phi_t n_s}{\epsilon_{Si}\mathcal{E}_s^2} + \frac{qn_s}{C_{ox}\mathcal{E}_s n_1}} \tag{6.30}$$

where

$$Y = 1 - e^{-\mathcal{E}_s t_{Si}/2\phi_t}$$

A similar expression of g_m for the edge-gate transistor may be obtained by replacing Q_b and W with Q_b' and t_{Si}, respectively in eqns.(6.27) and (6.30).

6.3 Results and Discussion

The GAA devices were fabricated on the standard SIMOX substrates, as described in [87]. The final silicon film thickness t_{Si} is $100nm$ for all the GAA devices studied in this work. The gate oxide was formed at $850°C$ in wet O_2 and annealed at 800°C in N_2, from which a final oxide thickness of $30nm$ was obtained. A channel doping density of $N_A = 1 \times 10^{17} cm^{-3}$ was obtained by using a boron dopant with implant energy of $25KeV$ and a dose of $2 \times 10^{12} cm^{-2}$. The static current-voltage measurements were performed on these GAA devices using an HP 4145B parameter analyzer.

6.3.1 Weak Inversion

The interface state density is determined from the slope of measured drain current operated in the subthreshold region, as shown in Fig. 6.3. The interface state density determined from Fig. 6.3 for different geometric GAA devices are summarized in Table 6.1. Due to volume-inversion effect, the mobility is higher than that of the surface-channel devices. This results in the overshoot of the transconductance by more than two times of the standard SOI devices (see Fig. 6.8). Figure 6.4 shows the subthreshold drain current for different geometric GAA devices. It is obvious that the effect of interface defects can not be neglected in these devices. The subthreshold swing ($\approx 66mV/dec$ at $300K$) is larger than those observed in references [92, 95]. This larger subthreshold swing may be attributed to the early edge conduction and the larger interface state density in the non-ideal GAA devices. To prevent the early edge conduction, a threshold adjustment implant may be used around the edge area of the GAA devices. The interface defects attribute to the micro-roughness at the interfaces of air/Si and Si/buried oxide layer and stacking fault tetrahedra (SFT) in silicon overlayer of SOI wafers. During oxidation, the micro-roughness will lead to oxide defects [103] and the SFT will induce oxidation-induced stacking fault (OISF) [104].

The OISF is a vacancy-type defect, and hence Si dangling and Si-O stretch bonds are easy to form at the Si/SiO_2 interfaces. The stack thermal oxidation [103] and the high temperature oxidation [105] can be employed to ameliorate such oxide-defect problems. A comparison between the simulated and the measured values is shown in region I of Fig. 6.7. Good agreement was obtained between the simulated and the measured values.

6.3.2 Strong Inversion

In region III of Fig. 6.7, both the edge-gate and the long-double-gate transistors are under strong inversion. Since the center of silicon film is still inverted even at higher gate voltages, the conventional method for determining the threshold is no longer valid. Instead of using the definition of band bending of $2\phi_F$, the surface potential at threshold was derived in Appendix D by using the threshold voltage determined at maximum transconductance change [98]. The extraction of the threshold voltage is shown in Fig. 6.5. In order to confirm the measured value of V_T, a different $I_{ds} - V_{gs}$ extraction method for determining V_T by the extrapolation of $Y(V_{gs}) = \sqrt{I_{ds}^2/g_m}$ to V_{gs} [106] was employed. The measured results are summarized in Table 6.1. Good agreement was obtained between our method and that of reference [106]. At higher gate voltages, most of the minority carriers are piled up near the Si/SiO_2 interface [87, 91]. As a result, the surface scattering of minority carriers by the surface roughness and interface defects is increased. The surface scattering degrades both the mobility and the transconductance. This degradation renders the reduction of transconductance. In our model, the parasitic series resistance and the scattering factor are considered. Figure 6.6 shows the extraction of surface scattering factor θ and series resistance R_s. Using the low field mobility determined by extrapolating the measured μ_{eff} versus $V_{gs} - V_T$ curve at $V_{gs} = V_T$, both θ and R_s can be easily decoupled. In order to confirm the measured values of μ_0, θ, and R_s, a

conventional method [107] for the determination of R_S by varying channel length was employed to compare our method. Using the measured value of R_s in eqn.(6.24), μ_0 and θ can be obtained. The extracted values of μ_0, R_s, and θ for two different $I_{ds}-V_{gs}$ extraction methods are listed in Table 6.1. Good agreement between the measured results was obtained. In Fig. 6.7, the experimental and simulated results at higher gate voltages were found in good agreement. The discrepancy at the saturation of surface potential ($\approx 2\phi_F + 5\phi_t$ [94]) is due to the discontinuity of the strong and moderate inversion models.

6.3.3 Moderate Inversion

In region II of Fig. 6.7, the edge-gate transistors are in strong inversion. For the long-double-gate transistor, neither weak nor strong inversion model is suitable for describing the exponential characteristics of the measured drain current. Using the developed moderate inversion model in the linear region and the extracted values of μ_0 and N_{ss}, good agreement between the simulated and measured results was obtained.

6.4 Conclusion

Analytical models for the subthreshold, moderate inversion, and strong inversion regions have been developed for the GAA nMOS/SOI devices. For the non-ideal GAA devices, the edge effects are considered. These models are valid over a wide range of gate-voltage operation region. In our models, the minority carriers and depletion charges are taken into account. Both the surface potential and surface electric field are expressed explicitly including the effects of interface defects in the weak and moderate inversion regions. In the strong inversion region, the effects of mobility degradation and parasitic series resistance are considered. Due to volume-inversion effect, the drain current and transconductance are enhanced. Using our models,

parameters extraction is achieved by using simple dc current-voltage measurements. The extracted parameters may be used in the evaluation of processing effects and the performance of GAA devices.

Table 6.1 Results of parameter extraction for different geometry-types of GAA SOI MOSFET's using the current-voltage technique. All the GAA devices were fabricated with $N_A = 1 \times 10^{17} cm^{-3}$, oxide thickness of $30nm$, and silicon film thickness of $100nm$.

Device	W/L	μ_0 (cm^2/V-sec)	V_T (V)	V_{Te} (V)	N_{ss} ($eV^{-1}cm^{-2}$)	R_s (Ω)	θ (V^{-1})
A	4/5	723/714†	1.23/1.19‡	-0.123	7.89×10^{10}	454/487†	0.211/0.201†
B	4/3	669/677†	1.11/1.09‡	-0.027	3.51×10^{11}	148/126†	0.140/0.159†
C	3/3	673/678†	1.02/1.03‡	0.00	7.62×10^{11}	228/210†	0.125/0.133†

† measuring R_s [107] first and then using this extracted R_s in eqn.(6.24) to obtain μ_0 and θ.

‡ measured by the extrapolation of $\sqrt{I_{ds}^2/g_m}$ to V_{gs} [106].

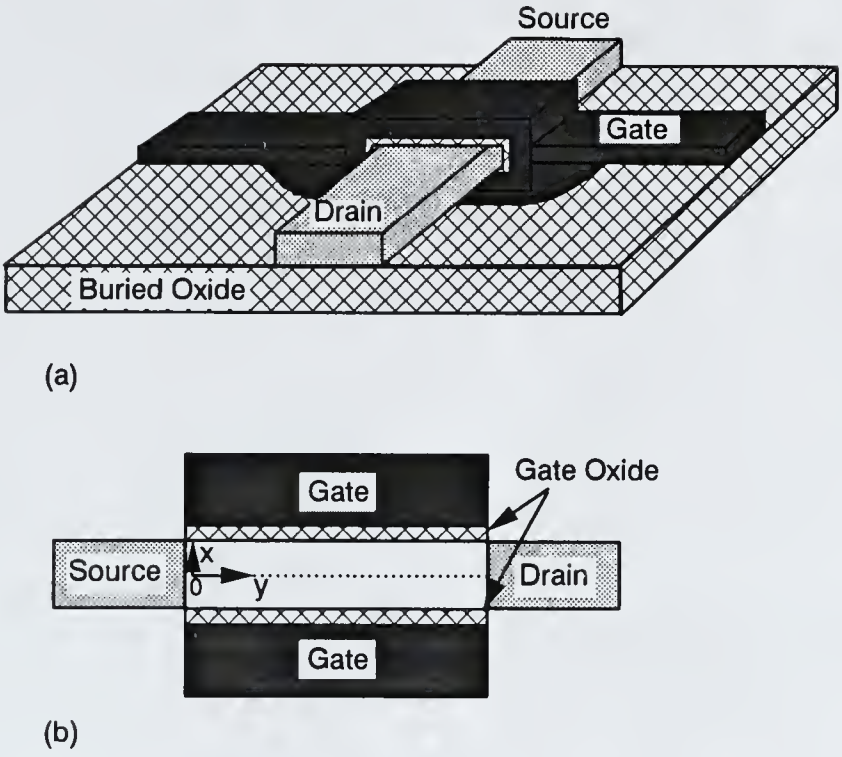

Figure 6.1: (a) The three-dimensional schematic representation and (b) the cross-sectional view of a GAA SOI MOSFET.

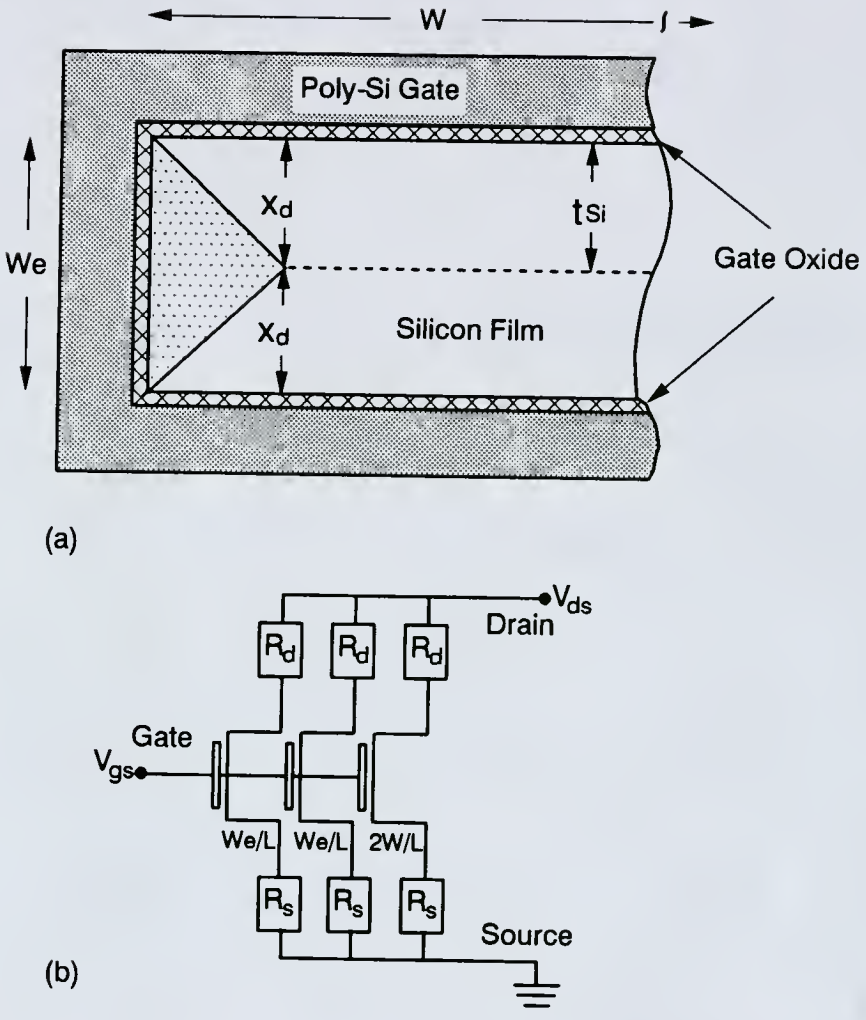

Figure 6.2: (a) Schematic cross-sectional view of the edge of a GAA SOI MOSFET showing the sidewall, front-side, and back-side depletion regions. (b) The parallel connection of long-gate and edge-gate transistors with parasitic resistance R_d and R_s of a GAA SOI MOSFET; W and W_e are the gate widths of long-gate and edge-gate transistor, respectively, and L is the channel length.

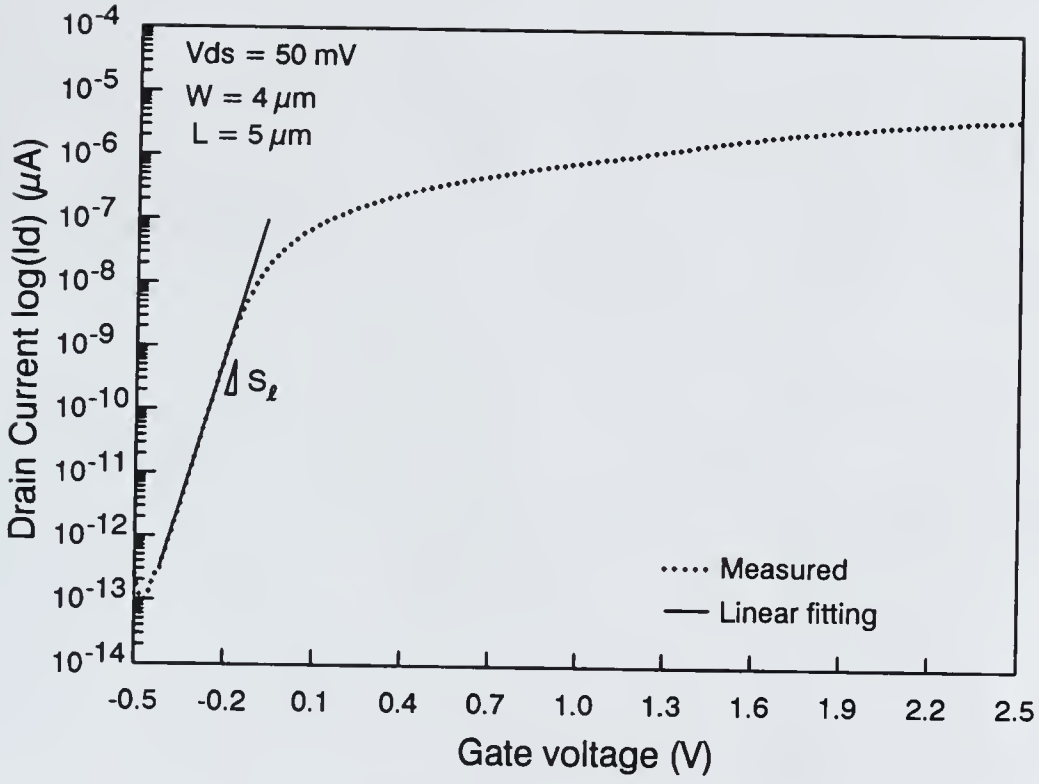

Figure 6.3: The extraction of interface-state density N_{ss} (eqn. 6.13) by fitting the slope of a measured subthreshold drain current.

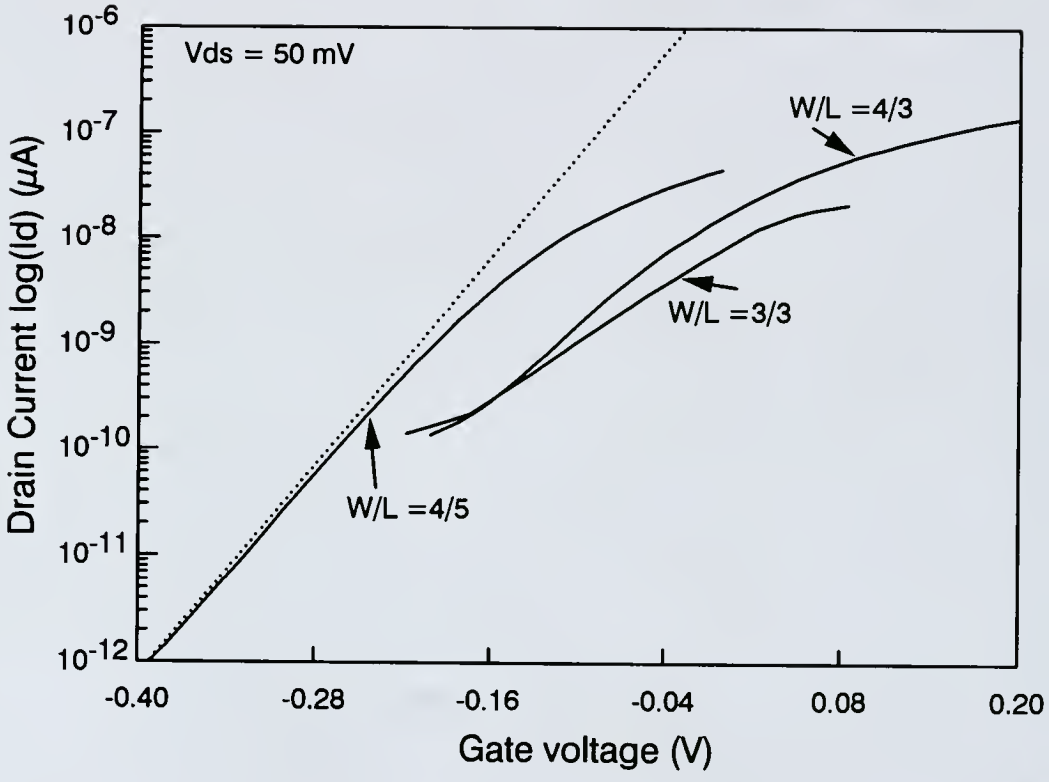

Figure 6.4: The measured subthreshold drain current of different GAA transistors. The dot line represents the slope obtained in the absence of interface defects.

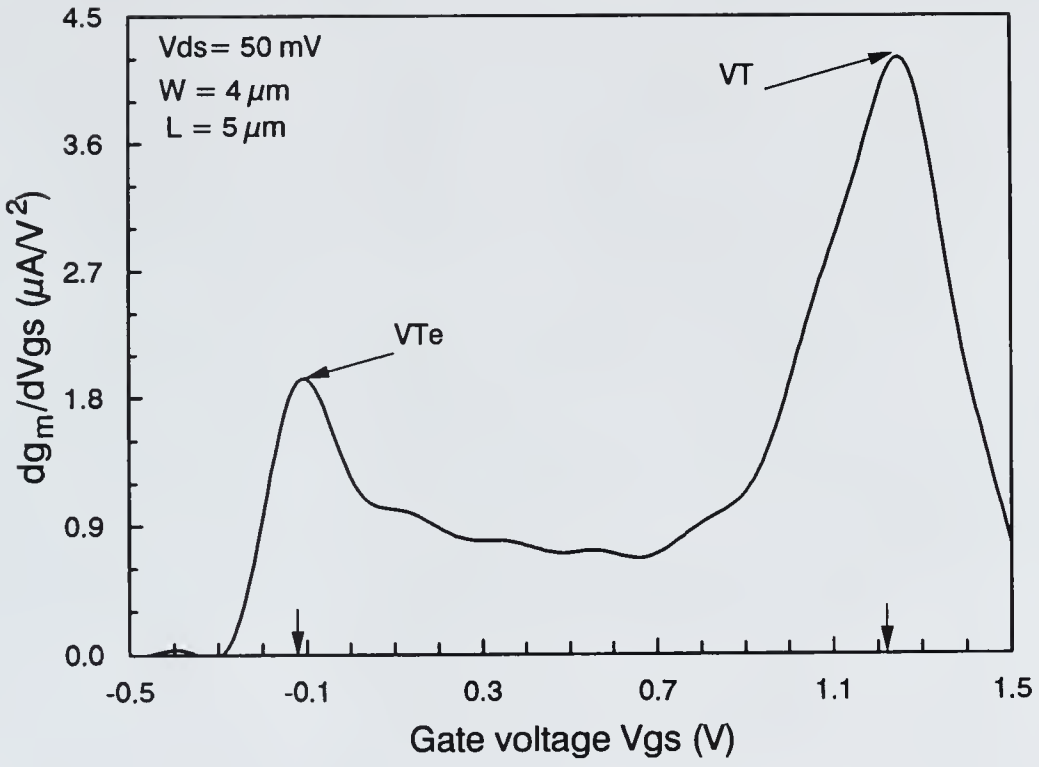

Figure 6.5: The extraction of the values of threshold voltage in a GAA MOSFET by using the maximum transconductance change (TC) method [98]. The arrows indicate the values of threshold voltage.

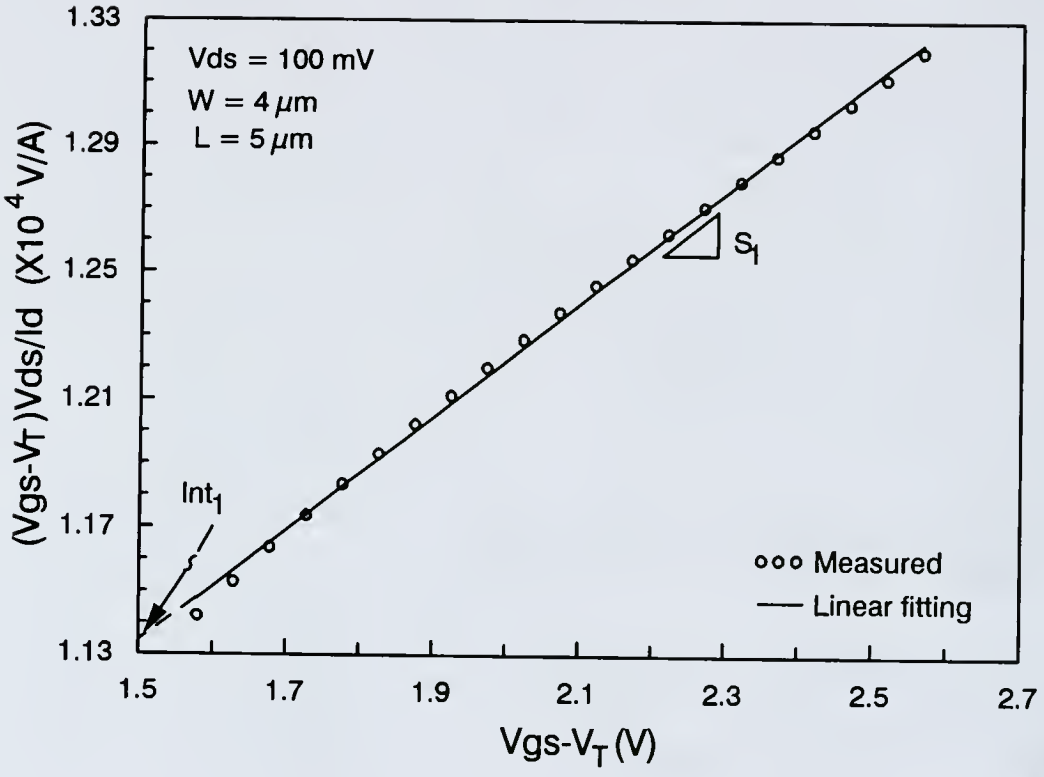

Figure 6.6: The extraction of parasitic series resistance R_s and surface scattering factor θ (eqn. (6.24)) in the strong inversion region of a GAA SOI MOSFET.

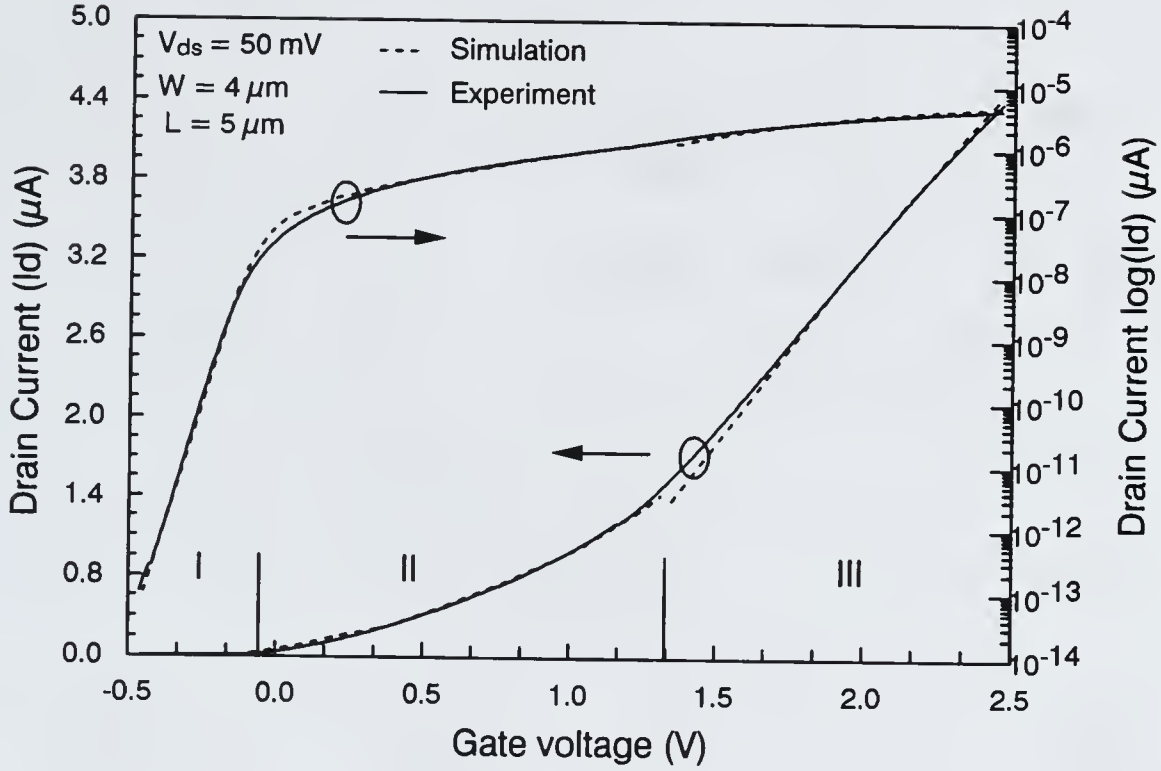

Figure 6.7: A comparison of the measured drain current and the simulation results using the extracted values of N_{ss}, μ_0, R_s, and θ.

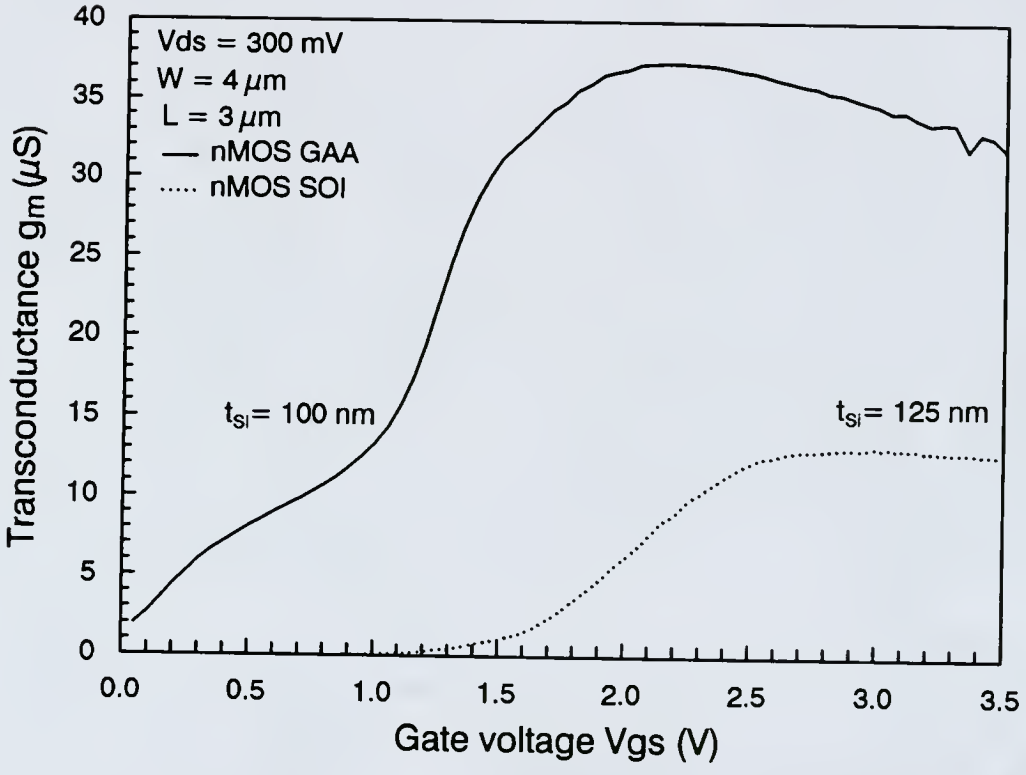

Figure 6.8: The measured transconductance of a GAA and a conventional SOI MOSFET with the same fabrication processes.

CHAPTER 7
SUMMARY AND CONCLUSIONS

In this dissertaion, a new contactless dual-beam S-polarized reflectance (DBSPR) technique has been developed for measuring the top Si film and buried oxide thickness in a SIMOX wafer. Top Si film and buried oxide thicknesses of the SIMOX wafers ranging from 0.2 to 1.6 μm and 0.36 to 0.44 μm, respectively, were determined using the DBSPR technique. The t_f measurement results of DBSPR show an excellent agreement with the values determined by the conventional reflection interference spectroscopy method. Due to the presence of a transition layer between the BOX and the bulk Si substrate, an error ($\sim 10\%$) will be resulted from the measurements of t_{ox} in the SIMOX wafers. For the DBSPR technique, the inaccuracy was resulted from the measurements of t_{ox} in the SIMOX wafers, but for the bonded SOI wafers which do not contain the transition layer the DBSPR technique can be employed. The main contributions of Chapter 2 are (i) to develop a new nondestructive dual-beam S-polarized reflectance optical measurement method for determining t_f and t_{ox} in SOI materials, (ii) to determine t_f and t_{ox} simultaneously by using the measured reflectance data and numerical calculations, and (iii) the extracted t_f and t_{ox} employed to determine the reflectance (R) and transmittance (T) which as described in Chapter 3.

The main contributions of Chapter 3 are (i) to develop an nondestructive dual-beam optical modulation (DBOM) technique for determining the interface recombination velocities and substrate carrier lifetimes in SOI materials, (ii) the consideration of the multiple reflections inside the top silicon film and the BOX, (iii) to decouple the recombination effects in the top silicon film and the Si substrate by using

dual-pump-beam (different wavelengths) and dual-angle incidence, and (iv) using the back-side and front-side illuminations to decouple the back-interface recombination velocities and substrate carrier lifetime. Mappings of the front- and back-interface recombination velocities and the substrate carrier lifetimes for several SIMOX wafers with different Si film thicknesses and oxygen implantation processes have been carried out. This method is especially useful for quality control and defect studies of the SOI wafer manufacturing. Using this technique, the interface properties and the quality of SOI wafers can be evaluated versus processing and growth parameters.

The main contributions of Chapter 4 are (i) using the optical methods described in Chapter 2 and 3, the implant effects (e.g., implant energy, temperature, beam current, channeling, and non-channeling) on the defect density of high temperature annealed single-dose-implant SIMOX wafers can be obtained and (ii) a strong correlation between the results of the optical measurements and the etch-pit method was obtained. This correlation reveals that the threading dislocation is the main defect in the top silicon film [45]. The measurement results indicate that the higher energy, channeling, higher temperature, and lower beam current implants have a better front-interface quality. Contrary to the front interface, the back interface shows that the lower energy, non-channeling, and higher beam current implants have a better interface quality. Channeling and lower temperature implants produce more damage on the back interface than that of non-channeling and higher temperature implants. Similar to the back-interface recombination velocity measurements, the substrate carrier lifetime measurements reveal that the lower energy, non-channeling, lower temperature, and lower beam current implants have a better substrate quality. An etch-pit method was used to correlate the relationship between the Si-overlayer defect density and the front-interface recombination velocity. The results indicate a closed relationship between the interface quality (front-interface recombination velocity) and the Si-overlayer defect density.

The main contributions of Chapter 5 are (i) the parasitic BJT effects and experimental results show that the FB PD SOI encounters more serious aging effects than that of the GB mode, (ii) during the stress test on the front interface, the aging may be induced at the back interface, (iii) after the parasitic BJT action, the bulk impact-ionization will dominate the impact-ionization effect near the drain/body junction, and (iv) a new model for the parasitic current components in the neutral and depleted bases of the parasitic BJTs was derived. When the hot carrier degradation takes place inside the PD SOI devices, the parasitic bipolar action was found to aggravate the aging effects. The degradation of device characteristics is negligible prior the parasitic BJT action. During the stress at accumulation of the back interface, the floating body effects are reinforced, and the aging in the front-channel transistor is accelerated. The kink voltage, parasitic bipolar action, and breakdown voltage were altered after stress. Hot-carrier-induced interface defects and fixed charges are responsible for modification of these device characteristics. From previous experimental and simulation results, an n-channel PD SOI MOSFET with floating-body connection encounters more severe aging effects than that of the unfloating-body mode. Although floating-body PD SOI structure has several advantages over the bulk CMOS, the solutions in processing and structure are necessary for the PD SOI devices to enter the mainstream IC technology. The possible solutions to reduce parasitic bipolar effects are: (i) increasing the back channel doping to suppress current gain; (ii) decreasing the emitter (source) impurity doping; (iii) using a body contact. Using the body contact will trade off the packing density. Thus, a structure modification may be employed to reduce the maximum electric field near the drain junction: (i) increasing the doping in the n^- region of the LDD; (ii) sloped-junction LDD, and (iii) halo structure with low-high active-region doping [4]. Besides the solutions mentioned above, the reduction of hydrogen and moisture contents during processing is another good approach.

The main contributions of Chapter 6 are (i) to develop analytical models for the weak, moderate, and strong inversion for the GAA nMOS/SOI devices. Both the depletion charge and minority carrier are included in the Poisson equation for the case of below threshold conditions. In addition, the influence of interface states was also taken into consideration (Eq. 6.5). A new derivation of the $I_d - V_{gs}$ characteristics for the weak inversion case was carried out (Eqs. 6.6 to 6.10), (ii) the new analytical model for the strong inversion included the parasitic resistance and the mobility degradation factor (Eqs. 6.20-6.22). The derivation of threshold condition in Appendix D is also new. Based on this model, the low field mobility, the mobility degradation factor, and the parasitic resistance can be extracted from the measured $I_{ds} - V_{gs}$ characteristic curves (Eqs. 6.21-6.24), and (iii) to include the edge-gate conduction in the derivation (Eqs. 6.11-6.14 and 6.20). Based on this model, the hump observed in the subthreshold region (see Fig. 6.8) may be explained. Due to the low noise, higher mobility, enclosure structure, the GAA device is suitable for use in the analog and radiation hardness circuit applications. These models are valid over a wide range of gate-voltage operation region. In the models, the minority carriers and depletion charges are taken into account. Both the surface potential and surface electric field are expressed explicitly including the effects of interface defects in the weak and moderate inversion regions. In the strong inversion region, the effects of mobility degradation and parasitic series resistance are considered. Due to volume-inversion effect, the drain current and transconductance are enhanced. Using the models, parameters extraction is achieved by using simple dc current-voltage measurements. The extracted parameters may be used in the evaluation of processing effects and the performance of GAA devices.

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APPENDIX A
DERIVATION OF EXCESS CARRIER CONCENTRATION IN UNLTRA-THIN TOP SILICON FILM

For the ultra-thin Si film SOI wafer, the photogenerated excess carrier concentration gradient is usually very small along the direction of incident beam. As a result, the diffusion process is negligible while the volume and surface recombination processes will dominate the excess carrier decay in the top Si film. Thus, Eq. (3.1) becomes

$$G(x) - \frac{\Delta n}{\tau} = 0 \tag{A.1}$$

where

$$\begin{aligned} \frac{1}{\tau} &= \frac{1}{\tau_f} + \frac{1}{t_f/S_1} + \frac{1}{t_f/S_2} \\ &= \frac{(S_1 + S_2) + \frac{t_f}{\tau_f}}{t_f} \end{aligned} \tag{A.2}$$

The total excess carrier concentration in the Si film can be obtained by solving Eqs. (3.5), (A.1), and (A.2)

$$\begin{aligned} \Delta N_1 &= \int_0^{t_f} \Delta n_1(x)dx = \eta(1-R-T)\phi_0 \cos\theta_2 \tau \left(1 - e^{-\alpha t_f}\right) \\ &= \eta(1-R-T)\phi_0 \cos\theta_2 \left(\frac{t_f(1-e^{-\alpha t_f})}{(S_1+S_2)+\frac{t_f}{\tau_f}}\right) \end{aligned} \tag{A.3}$$

APPENDIX B
DERIVATION OF IMPACT-IONIZATION MULTIPLICATION FACTOR AND CHANNEL CURRENT IN MOSFET PART

In the saturation region, the impact ionization generated by channel current in the pinch-off region of SOI MOSFET with LDD (lightly doped drain) structure can be expressed as follow [79,80]

$$M_{ch} - 1 = \int_{\mathcal{E}_{sat}}^{\mathcal{E}_m} \alpha_1(\mathcal{E}) \frac{dy}{d\mathcal{E}} d\mathcal{E} + \int_{\mathcal{E}_m}^{\mathcal{E}_d} \alpha_2(\mathcal{E}) \frac{dy}{d\mathcal{E}} d\mathcal{E} \tag{B.1}$$

$$\alpha_1(\mathcal{E}) = \alpha_0 e^{\frac{-\beta_i}{\mathcal{E}_{y1}}} \tag{B.2}$$

$$\alpha_2(\mathcal{E}) = \alpha_0 e^{\frac{-\beta_i}{\mathcal{E}_{y2}}} \tag{B.3}$$

where $\mathcal{E}_{sat}$, $\mathcal{E}_m$, and $\mathcal{E}_d$ are the channel electric field at the start point of pinch-off region ($y = -L_{sat}$), the body-LDD junction ($y = 0$), and LDD-drain junction ($y = L_{nn}$), respectively. α_0 and β_i are the ionization coefficients with the value of 1.4×10^6 cm^{-1} and 2.6×10^6 V/cm, respectively [62]. For small L_{nn}, the channel electric field $\mathcal{E}_{y1}$ and $\mathcal{E}_{y2}$ can be expressed as

$$\begin{aligned} \mathcal{E}_{y1} &= \mathcal{E}_{sat} \cosh\left(\frac{y + L_{sat}}{l}\right) \\ &= \sqrt{\left(\frac{V(y) - V_{dsat}}{l}\right)^2 + \mathcal{E}_{sat}^2} \end{aligned} \tag{B.4}$$

$$\mathcal{E}_{y2} = \mathcal{E}_{sat} \cosh\left(\frac{y + L_{sat}}{l}\right) - \frac{q\eta N_d l}{\epsilon_{Si}} \sinh(y/l) \tag{B.5}$$

$$L_{sat} = l \sinh^{-1}\left\{\frac{1}{\mathcal{E}_{sat} l}\left[V_{ds} - V_{dsat} + \frac{q\eta N_d l^2}{\epsilon_{Si}}\left(\cosh\frac{L_{nn}}{l} - 1\right)\right]\right\} - L_{nn} \tag{B.6}$$

where $V(y)$ and V_{dsat} denote the channel potential in the pinch-off region and at the point of starting pinch-off, respectively, $l = \sqrt{\frac{\epsilon_{Si} t_{ox1} x_j}{\eta \epsilon_{ox}}}$ are the characteristic length of

the SOI MOSFET, ϵ_{Si} and ϵ_{ox} is the dielectric permittivity of silicon and gate oxide, respectively, t_{ox1} is front-gate oxide thickness, x_j is the LDD junction depth, N_d is the doping concentration in LDD, and η is a fitting factor accounted for the nonuniform lateral electric field distribution induced by the drain voltage. Generally, $\mathcal{E}_m \gg \mathcal{E}_{sat}$ and the first term on the right hand side of eqn. (B.1) can be expressed as [81]

$$\frac{\alpha_0 \mathcal{C}}{\beta_i} \exp\left(\frac{-\beta_i l}{\mathcal{C}}\right)$$

where,

$$\begin{aligned} \mathcal{C} &= V_{ds} - V_{dsat} - V_{Ldd} \\ &= V_{ds} - V_{dsat} - \mathcal{E}_{sat} l \left[\sinh \frac{L_{nn} + L_{sat}}{l} - \sinh \frac{L_{sat}}{l}\right] \\ &+ \frac{q\eta N_d l^2}{\epsilon_{Si}} (\cosh \frac{L_{nn}}{l} - 1) \end{aligned} \tag{B.7}$$

Next, the channel current including the short channel effects (e.g., charge sharing, drain-induced-barrier-lowing, and drain-induced-current-enhanced, *etc.*) is given as follow [77]

$$I_{ch} = W v_{sat} Q_{L_{sat}} \tag{B.8}$$

$$\begin{aligned} Q_{L_{sat}} &= -C_{ox1}\left(V_{g1} - V_{FB1} - \frac{C_{ox1} + C_b + C_{it1}}{C_{ox1}}\psi_{s1}\right. \\ &+ \left.\frac{Q_{beff}}{2C_{ox1}} + \frac{C_b}{C_{ox1}} V_{be} - \Delta Q_c / C_{ox1}\right) \end{aligned} \tag{B.9}$$

$$\Delta Q_c = (C_{ox1} + C_b) V_{dsat} - \frac{\epsilon_{Si} X_d \zeta}{2} \tag{B.10}$$

where V_{g1}, V_{FB1}, ψ_{s1}, C_{it1}, and C_{ox1} are the front gate voltage, flat-band voltage, surface potential, interface state and gate-oxide capacitance, respectively, v_{sat} is saturation velocity, C_b is the depleted-body capacitance, X_d is the maximum depletion depth controlled by the front-gate voltage, V_{be} is the body potential, $\zeta = 2V_{ds}/L^2$ is

an empirical constant [82], V_{dsat} is the saturation voltage and listed in Reference [77], and Q_{beff} is the effective depleted-body charge attributed to charge sharing from the drain/source and can be expressed as

$$\begin{aligned} Q_{beff} &= -qN_A X_d \left(1 - \frac{x_j(V_{bi} - V_{be})N_d}{LX_d E_b(N_A + N_d)}\right) \\ &= -qN_A X_d(1 - \xi) \end{aligned} \tag{B.11}$$

$$E_b = \sqrt{\frac{q(V_{bi} - V_{be})N_A N_d}{2\epsilon_{Si}(N_A + N_d)}} \tag{B.12}$$

V_{bi} is the build-in potential at the body-drain/source junction.

APPENDIX C
DERIVATION OF CURRENT COMPONENTS FOR PARASITIC BJT

In Fig. 5.1, the collector current of the parasitic BJT can be considered as the combination of two currents from the depleted body and non-depleted body. The emitter current of the parasitic BJT is given as

$$\begin{aligned} I_{E1} &= I_e + I_{he} + I_{rec} \\ &= k_1 e^{V_{be}/\phi_t} + k_2 e^{V_{be}/\phi_t} + k_3 e^{V_{be}/2\phi_t} \\ &= \frac{qD_n n_i^2}{N_A W_B} W(t_{Si} - X_d) e^{V_{be}/\phi_t} + \frac{qD_p n_i^2}{N_D W_E} W(t_{Si} - X_d) e^{V_{be}/\phi_t} \\ &+ \frac{qn_i W_{eb}}{2\tau_r} W(t_{Si} - X_d) e^{V_{be}/2\phi_t} \end{aligned} \tag{C.1}$$

for the quasi-neutral body and

$$\begin{aligned} I_{E2} &= I_{ed} + I_{hed} \\ &= k_4 e^{V_{be}/\phi_t} + k_5 \\ &= \frac{qD_n' n_i^2}{N_A W_B'} W X_d e^{V_{be}/\phi_t} + k_2 X_d/(t_{Si} - X_d) e^{V_{be}/\phi_t} \end{aligned} \tag{C.2}$$

for the depleted body, where D_n and D_n' are the electron diffusion coefficients in the quasi-neutral and depleted body, respectively, D_p, N_D, and W_E are the hole diffusion coefficient ,doping concentration, and width of the source region, respectively, t_{Si} is the silicon film thickness, τ_r is the carrier recombination lifetime, $W_B = L - (W_{eb} + W_{cb})$ is the width of quasi-neutral base, $W_B' = L - 2L_{nn}$ is the width of the depleted base, W_{be} and W_{cb} are the depleted width in the body-source and body-drain junction, respectively. The total emitter current I_E is equal to the summation of I_{E1} and I_{E2}.

The collector current can be obtained by using the transport factor $\alpha_T^{-1} = cosh(\frac{W_B}{L_n})$ and the electron current transports through the body [32], and is given as

$$\begin{aligned} I_C &= \alpha_T I_e + I_{ed} \\ &= I_{C1} + I_{C2} \\ &= (\alpha_T k_1 + k_4) e^{V_{be}/\phi_t} \end{aligned} \tag{C.3}$$

where L_n is the electron diffusion length in the quasi-neutral body.

APPENDIX D
DERIVATION OF SURFACE POTENTIAL AT THRESHOLD

Using the transconductance change (TC) method and eqns. (6.2), (6.5), and (6.6), the surface potential at threshold may be obtained by solving $\frac{d^3 I_d}{dV_{gs}^3} = \frac{d^3 \phi_s}{dV_{gs}^3} = 0$ and the results yield

$$\begin{aligned}
\frac{d\phi_s}{dV_{gs}} &= \left(1 + 2C_{Si}/C_{ox}\frac{X}{Y}\right)^{-1} \\
\frac{d^2\phi_s}{dV_{gs}^2} &= \left(\frac{-2C_{Si}X}{\phi_t C_{ox} Y}\left(1 - \frac{4C_{Si}\phi_t X}{Y^2 Q_b}\right)\right)\left(1 + 2C_{Si}/C_{ox}\frac{X}{Y}\right)^{-3} \\
\frac{d^3\phi_s}{dV_{gs}^3} &= \frac{2C_{Si}X/(\phi_t^2 C_{ox}Y)}{\left(1 + 2C_{Si}/C_{ox}\frac{X}{Y}\right)^4} \\
&\times \left(\frac{\left(1 - \frac{4C_{Si}\phi_t X}{Y^2 Q_b}\right)^2 \frac{6C_{Si}X}{C_{ox}Y}}{\left(1 + 2C_{Si}/C_{ox}\frac{X}{Y}\right)} - \left[1 - 3\frac{4C_{Si}\phi_t X}{Q_b Y^2} + 3\left(\frac{4C_{Si}\phi_t X}{Q_b Y^2}\right)^2\right]\right) \qquad \text{(D.1)}
\end{aligned}$$

where $X = e^{(\phi_s - 2\phi_F - V(y))/\phi_t}(1 - e^{-Q_b/(8C_{Si}\phi_t)})$ and $Y = \sqrt{1 + X(8C_{Si}\phi_t)/Q_b}$.

Now solving $\frac{d^3\phi_s}{dV_{gs}^3} = 0$ in eqn. (D.1) for $N_A > 1.1 \times 10^{13} cm^{-3}$ and $t_{Si} > 10nm$ $(X, Y > 0)$, the surface potential at threshold is given by

$$\phi_s^* = 2\phi_F + V(y) + \phi_t \ln\left(\frac{C_{ox}/(4C_{Si})\left(C_{ox}\phi_t/Q_b + \sqrt{C_{ox}^2\phi_t^2/Q_b^2 + 1}\right)}{1 - e^{-Q_b/(8C_{Si}\phi_t)}}\right) \qquad \text{(D.2)}$$

BIOGRAPHICAL SKETCH

Yun-Shan Chang was born in Keelung, Taiwan, R.O.C., on May 23, 1962. He received the B.S. degree from the Department of Physics of National Central University in June, 1985. From August 1985 to June 1987 he served in the Taiwan Army. After fulfilling his military service, he worked as a research assistant in the Plasma Lab at the National Central University until July, 1989. His research topics were deposit amorphous carbon film on glass and RF plasma metal sputtering.

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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