

Resistive switching in strained Ag/SrTiO₃/In RRAM devices

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Abstract

Resistive random-access memory (RRAM) devices are a type of memristor based on resistance switching that boast nanosecond switching speeds, low operating power, high retention times, and long lifetimes. Coupled with their nonvolatility and scalability, RRAM technology has the potential to replace conventional flash memory and dynamic random-access memory. In this study, Ag/SrTiO₃/In RRAM device resistive switching is explained via Schottky barrier modulation, either through the diffusion of oxygen vacancies or oxygen ion conduction. With the potential of improving device performance, the effects of strain on the device were assessed and tested. We report a memory window enlarged by one of order of magnitude as well as lower power consumption with the potential for other improvements that have yet to be tested. Overall, the preliminary performance results of the strained Schottky-based device show promise for further device optimization and novel physical phenomena through strain engineering.

Background

Resistive random-access memory (RRAM or ReRAM) devices are a type of memristor based on resistance switching. These devices have variable resistance states depending on their history of electrical stimulus and can “remember” their most recent resistance after electric power supply is removed. Boasting fast state switching (on the order of ns), low operating voltage (approximately 1 V), and long retention times, RRAM has great potential to replace conventional flash memory and dynamic random-access memory storage¹. One of the most important advantages of RRAM devices is their scalability. As electronics are designed smaller, conventional flash memory technology has already struggled to scale accordingly. RRAM devices could be the next step in nonvolatile, high density working and main memory storage². Furthermore, applying strain to these devices and introducing phase transitions in their constituent materials has the potential to favorably alter their electronic properties, thus improving performance.

1.1 RRAM Devices

A simple RRAM device consists of an insulator or semiconductor sandwiched by two metal electrodes. With a bias applied across it, the device can switch between resistive states either in the bulk of the insulator (bulk-switching) or at the metal-insulator junction (interface switching).

The two logic states for data storage are represented by either a low or high resistive state (LRS or HRS). Multiple resistive states can also be exploited for higher density memory storage. A typical bulk-switching RRAM device with a metal-insulator-metal structure (Figure 1a) begins in the insulating HRS. Resistive switching is accessed via a ‘forming’ process during which the insulator undergoes soft dielectric breakdown and temporarily becomes conducting (resistance decreases by at least one order of magnitude). Unlike hard dielectric breakdown, soft dielectric breakdown is reversible. Such reversibility in conductivity is the basis of the switching mechanism in bulk-switching RRAM devices. Switching from HRS into LRS occurs at a ‘setting’ voltage (V_{SET}), and the transition from LRS back to HRS is achieved by applying a ‘reset’ voltage (V_{RESET}). Typically, V_{SET} is larger than V_{RESET} and their polarities depend on the material. For interface-switching RRAM devices however, resistive switching occurs at the interface of the metal and semiconductor/insulator junction and is driven by other mechanisms (discussed in Section 1.3). Our interface-switching devices are best described by Figure 1b.

1.2 Materials

Resistance switching behavior has been observed in a variety of materials—including binary oxides, ternary oxides (perovskites), and chalcogenides—with each type exhibiting different switching mechanisms. Binary oxides have been the most extensively studied among the resistance switching materials because of their easy fabrication and reliability (both crucial factors for RRAM development in industry)². Furthermore, materials for RRAM devices must be chosen so that conducting and insulating phases of the material do not chemically interact with each other, especially at the high temperatures induced by Joule heating³. In this study, device materials were chosen with the desired switching mechanism in mind. For bulk switching, insulators with controlled dopant/defect concentrations and metals with low work functions (that form ohmic contacts with the insulator) are desirable. For devices in this study undergoing interface switching, metals with relatively higher work functions, such as gold and silver, are used as front electrodes. At the interface between the gold or silver and the semiconducting dielectric, a Schottky barrier is formed and the switching mechanism occurs at the interface via modulation of the barrier. The indium back electrode forms an ohmic contact with the dielectric and does not play a role in the switching mechanism. Figure 2 shows the band structure of an interface-switching device as a Schottky barrier. An interfacial layer made up of mid-gap interface states, derived from the

semiconductor's bulk states, is included in the band structure. With a higher areal density of trap states than in a bulk layer, the Fermi energy is pinned and forms a thin potential barrier at the interface. In the case of our devices however, this thin interfacial layer plays a negligible role in the switching and is thus, not considered further in the discussion.

SrTiO₃, an insulator with a high dielectric constant, has a high charge-storing capacity, good insulating properties, and chemical stability at elevated temperatures⁴. Resistive switching properties can be achieved by doping SrTiO₃ with Nb (substituting Ti atoms) or intentionally introducing oxygen vacancies⁵. Additionally, its excellent optical transparency in the visible region is useful for optoelectronic applications⁶. Our devices use oxygen vacancy-doped SrTiO₃. During their formation, oxygen vacancies generate free electrons released into the conduction band and can therefore be considered donor impurities. Empty oxygen vacancies can be modeled as positive charge carriers, while electron-filled oxygen vacancies can be modeled as trap states. The oxygen vacancies' role in resistive switching is described in Section 1.3.

1.3 Switching mechanisms

RRAM devices can exhibit either unipolar or bipolar switching depending on the switching mechanism and material. In the case of a unipolar device, the switching mechanism is independent of the applied voltage bias polarity, and V_{SET} and V_{RESET} will have the same polarity. Conversely, a bipolar device's V_{SET} and V_{RESET} must have opposite polarities. Figure 3 shows the hysteresis in the I-V curve of a unipolar and bipolar RRAM devices with each one's LRS, HRS, V_{SET} , and V_{RESET} labeled.

Generally, insulator-based RRAM devices express unipolar switching through soft dielectric breakdown. Conductive filaments are formed through the bulk of the material to the bottom electrode and the switching occurs in a small gap between the bulk's conductive filaments and the electrode⁷.

Filament formation is not required for bipolar switching, which occurs at the metal-oxide interface. The polarity dependent operation can be explained through either the movement of oxygen vacancies (positive charge carriers) or oxygen ion conduction. Conduction through the material is a consequence of either electric field or thermal effects via electron transport processes

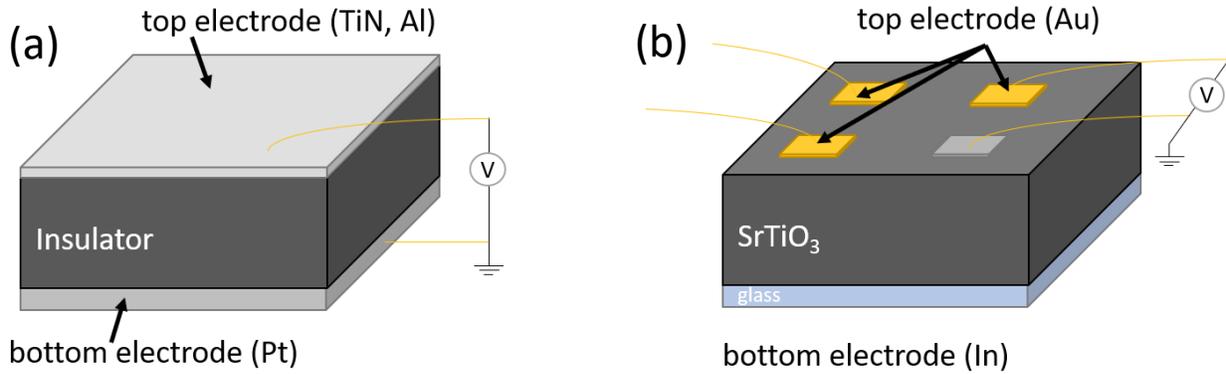


Figure 1. Schematics of RRAM (a) bulk-switching device and (b) three interface-switching devices.

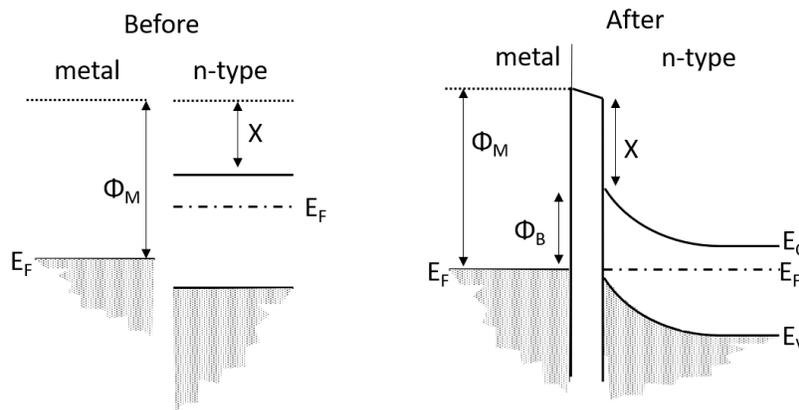


Figure 2. Band structure of metal/n-type semiconductor junction before and after contact. Φ_M is the work function of the metal, X is the semiconductor's electron affinity, and Φ_B is the Schottky barrier height. The interfacial layer in series with the Schottky barrier is present in our device but is so thin that it negligibly affects the device's switching and is not considered further.

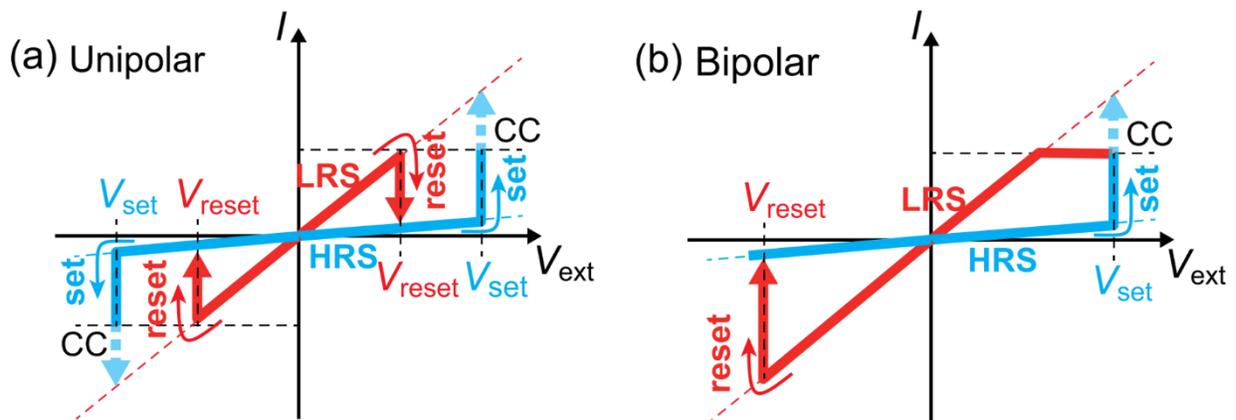


Figure 3. Schematic I-V curves showing (a) unipolar and (b) bipolar switching methods⁷.

that often coexist within the device. Distinguishing the prevalent transport process is challenging, but generally, bipolar devices are dominated by electric field effects (polarity dependent) whereas unipolar devices are dominated by thermal effects (polarity independent). Figure 4 summarizes the possible electron transport mechanisms of an RRAM device. The oxygen vacancies are treated as mid-gap trap states that result in trap-assisted conduction. Thermal effects, which can be exacerbated by high current densities ($> 10^6 \text{ A} \cdot \text{cm}^{-2}$), are summarized as (1) electron injection over the Schottky barrier into the conduction band (Schottky emission) and (2) electron excitation from trap states into the conduction band (Poole-Frenkel emission). The thermal fluctuations of trapped electrons—also collectively known as Poole-Frenkel emission—become evident in the I-V curves as a $I \sim V \exp((\alpha\sqrt{V} - \Phi_B)/kT)$ dependence⁷ where Φ_B is the Schottky barrier height and α is a constant.

Electric field effects manifest through electron tunneling processes: (3) Fowler-Nordheim tunneling (field emission) from the electrode to conduction band, (4) direct tunneling between electrodes if the material is thin enough, tunneling (5) from electrode to trap state, (6) from trap state to trap state, (7) from trap state to conduction band, or (8) from trap state to electrode³. The trap-assisted tunneling processes manifest in the I-V curve as a $\ln(I/V^2) \sim 1/V$ ⁷. The prevalence of either thermal or electric field effects depends on the type of device (bulk or interface switching) and the level of doping. Fitting of the I-V curves can help elucidate the dominating conduction behavior.

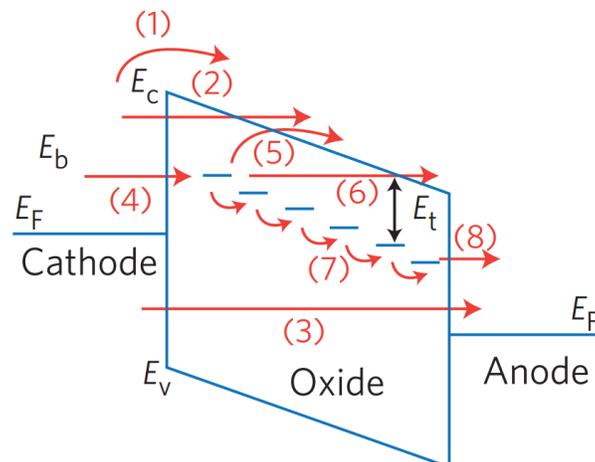


Figure 4. Electron transport mechanisms in an interface-switching RRAM device³ labeled as: (1) Schottky emission; (2) Fowler-Nordheim emission; (3) direct tunneling; (5) Poole-Frenkel emission; (4), (6), (7), and (8) trap-assisted tunneling

Driving forces that affect carrier motion include species concentration gradients and temperature gradients. The electric field, Soret, and Fick forces affect the migration rate of oxygen vacancies that drive the switching as the vacancies “hop” between the crystal’s period potentials. With an applied electric field, the vacancies and ions migrate parallel and antiparallel to the field. The Soret and Fick forces work in conjunction with the force of the applied electric field. The Soret force is a consequence of Joule heating that occurs around the conducting channel. A local rise in temperature forms a temperature gradient, perpendicular to the conducting channels, that pushes oxygen vacancies toward the hotter conducting channel⁷. Additionally, higher temperatures around the channel increase “hopping” rate, aiding the migration of oxygen vacancies and lead to oxygen vacancy-rich regions during switching. Opposing the Soret force is the Fick force, which restores the original distribution of oxygen vacancies and removes the oxygen vacancy concentration gradient generated by the Soret force. Because the conducting paths are formed parallel to the applied electric field, both the Soret and Fick forces act perpendicularly to the electric field and are thus, polarity independent. These forces are most relevant for conductive filament-based devices. The conduction paths and short conductive filaments formed in interface-switching device have even more localized heating that most probably negligibly affects the switching mechanism.

Wide-bandgap perovskites, such as SrTiO_3 , can accept large amounts of dopants. Doping pure SrTiO_3 with oxygen vacancies dramatically affects the material’s resistance. The higher the concentration of oxygen vacancies, the higher the conductivity. In the bulk of thicker materials (thickness greater than a few nm), oxygen vacancies can form conducting filamentary paths between sandwiching electrodes and lead to the material’s soft dielectric breakdown.

In devices where switching occurs at the metal-semiconductor interface and not in the bulk, the Schottky-barrier’s height and width can be changed as the oxygen vacancies diffuse and redistribute within the material under an applied bias. In vacancy doped SrTiO_3 , the height of the barrier remains approximately constant and can be approximated as the difference in Fermi energy and electron affinity. The switching mechanism we consider in our devices results from the accumulation of oxygen vacancies at the interface. Consider the metal-semiconductor interface as analogous to a p-n junction: the electrode is the n-type material and the SrTiO_3 also is an n-type material but with much fewer carriers and can be modeled as a p-type material. The intrinsic electric field formed in the depletion region in a p-n junction at equilibrium is analogous to the

Schottky potential barrier at the metal-semiconductor interface. A p-n junction at forward bias will decrease the electric field strength within the depletion region. Similarly, applying a negative bias to the top electrode of the RRAM device will cause the positive oxygen vacancies to migrate to the electrode, and at equilibrium the Schottky barrier width will decrease. Thus, the device switches from HRS to LRS. Tunneling effects increase and begin to dominate in this scenario because the potential barrier becomes much thinner and Schottky emission becomes much less likely. Under forward bias the oxygen vacancies migrate away from the top electrode and widen the Schottky barrier, switching the device from LRS to HRS. In this scenario, tunneling effects become negligible while Schottky emission and other thermionic emission effects dominate.

Some models suggest that the switching mechanism is due to the formation of new oxygen vacancies rather than the rearrangement of the existing ones introduced during annealing. This mechanism of ionic conduction is analogous to the electron trapping/detrapping models suggested by many studies⁷. When applying a positive bias to the top electrode, oxygen vacancies will diffuse away as in the previous case. Oxygen ions within the SrTiO₃ lattice, however, will redistribute and migrate towards the electrode, eventually diffusing out of the material and leaving an accumulation of newly formed oxygen vacancies at the interface. In this case, the buildup of oxygen vacancies at the interface decreases the width of the barrier, increases trap-assisted tunneling, and switches the device from HRS to LRS under forward bias. Under negative bias, the oxygen vacancies are “re-filled” by diffusing oxygen ions, therefore eliminating the trap states that assist conduction. The Schottky barrier width increases, Schottky emission becomes the dominating form of current, and the device switches from LRS to HRS. The two competing models of oxygen vacancy migration coexist within our devices, but the latter mechanism seems to dominate. As can be inferred from the two conflicting switching mechanism models, the exact role of oxygen vacancies in the resistive switching is still under investigation and varies with material.

1.4 Parameters and Dependencies

RRAM features are described by several parameters: window size, operating voltage, switching speed, retention, and lifetime. Window size is the ratio between the HRS and LRS resistance and is determined at low voltage biases where the I-V curve can be approximated as linear (-0.1 V – 0.1V). A ratio of 10 to 15 is considered large enough for a device to be qualified as RRAM. The minimum voltage at which this ratio is achieved is the operating voltage which

also determines the device's power consumption. One challenge in RRAM industry is the variability in the HRS and LRS between cycles. Only considering RRAM devices with window sizes of at least 10 is generally enough to avoid having either the HRS or LRS resistance within the other's variations. Increasing the window size further creates opportunities for denser memory storage with more than two logic states given the window size between each state is large enough to distinguish the states each cycle. Window size can be increased by increasing either the applied bias or the compliance current, so long as the device does not breakdown.

In this study we define switching speed is the shortest amount of time required for the RRAM device to switch between resistive states with a window of at least 20. Methods used to determine device switching speeds are outlined in Section 2.2. Because the switching speed depends on the temperature-dependent carrier transport, switching speed is temperature dependent and the relationship varies with material and dominant switching mechanism⁷.

Retention time is defined as the time required for the device to lose its RRAM features or "forget" its last resistive state. For nonvolatile memory devices such as RRAM, retention time should be on the order of months to years⁸. Typically, to keep our devices in LRS, they must be reset and set anew at least every 15 minutes. Determining the optimal trade-off between switching speed and retention time is a common challenge in the RRAM industry. As one parameter increases, the other necessarily decreases as both are governed by the same processes⁷.

As our devices approach their lifetime of approximately 10^4 switching cycles, they breakdown and lose RRAM features. Some bulk-switching anion-based RRAM devices however, have been shown to have endurances up to 10^6 cycles¹. The lifetime of the interface-switching devices has potential for improvement once the device materials are prepared with more precision and control to effectively study the source of the degradation.

1.5 Strain Effects

Applying strain to RRAM devices has the potential to improve device performance and reveal novel device physics. Studies of oxygen vacancy-doped SrTiO₃ under strain have shown that both tensile and compressive strain have the same effect on the material suggesting a common mechanism between the two types of strain. For SrTiO₃ thin films—or at the thin Au/SrTiO₃ interface in our case—tensile and compressive strain both decrease the vacancy formation enthalpy and potentially increase the diffusion coefficient of the vacancies along particular directions in the

perovskite's structure⁹. If the diffusion rate of oxygen vacancies within the material increases with strain, the process will still be relatively slow thus decreasing the switching speed. Other studies also show enhanced electron mobility in strained SrTiO₃ resulting from a reduced bandgap¹⁰. Thin film SrTiO₃'s dielectric constant has been modeled to show a rapid increase in dielectric constant under tensile strain up to $\epsilon = 0.010\%$ at 300 K. At higher strains (greater than $\epsilon = 0.012\%$ at 300 K), the dielectric constant is found to rapidly decrease, restoring its original value¹¹. Increased interfacial ferroelectric polarization of the material may be the mechanism behind the increasing dielectric constant. At temperatures approaching 0 K, SrTiO₃ behaves as a ferroelectric, and at temperatures above its Curie temperature (T_C) it behaves as a paraelectric. SrTiO₃'s ferroelectric properties become more apparent at higher strain because of reduced quantum fluctuations¹¹. Furthermore, applying strain has been shown to increase T_C (up to 300 K for 1% compressive or tensile strain)¹¹. This increased spontaneous and maintained polarization may be why the dielectric constant increases.

Although the reduction of the quantum fluctuations may contribute to the changing dielectric constant, the formation of extra dipoles at the interface may be the more likely mechanism. Under strain, the extension or contraction of bond lengths or the crystal lattice constant may create dipole moments, especially at the interface of the device. These interface dipoles may increase SrTiO₃'s ability to shield an applied electric field and thus, increase its dielectric constant.

Treating the interface volume where switching occurs as a thin film, a similar dielectric dependency on strain is expected to prevail in our devices' switching mechanism. Thus, with a larger dielectric constant, the material will screen the applied electric field more effectively and V_{SET} and V_{RESET} both increase as a larger applied electric field will be required to switch the device. In the band diagram, the Schottky barrier will drop off more slowly, widening the potential barrier. We hypothesize that the strain effects will manifest themselves in the I-V plots as downward shifts (lower current for a given voltage) in the LRS and HRS curves.

Experimental Methods

2.1 Sample preparation

Oxygen vacancies are introduced into the SrTiO₃ through annealing in vacuum around 1000°C for approximately 1 hour. The top gold electrodes are evaporated onto annealed SrTiO₃ and wired using silver paint and gold wires. Given a perfect crystal (without surface and internal defects and strains) with uniform oxygen vacancy doping, the RRAM features (LRS and HRS resistance) should not vary with electrode area. However, the SrTiO₃ crystal has nonuniform distribution of oxygen vacancies, intrinsic defects and strain from growth, and additional surface defects introduced during annealing. Annealing the material in medium vacuum (10⁻⁷ Torr) to introduce oxygen vacancies roughens the surfaces as the oxygen diffuses out⁴. Because of the additional mid-gap states that annealing introduces in addition to the trap states from other defects, the switching properties being studied may not be dominated by oxygen vacancy migration and the corresponding electric transport. Additionally, oxygen vacancies tend to accumulate along grain boundaries and dislocations in the material, creating pathways for faster migration. Relatively large accumulations of oxygen vacancies within a device's volume increases (1) the conductivity of the material too much and (2) the likelihood of large conductive filaments will form. Both are undesirable effects in interface-switching devices. Thus, the electrodes' contact areas must be minimized to limit the unwanted side effects of defects. Furthermore, smaller contact areas tend to produce more stable devices. Our devices had areas of approximately 0.5 to 1 mm². Ideally the device has a HRS resistance of 1 to 10 MΩ when measured using an ohmmeter.

2.2 Characterization

After identifying devices with resistance values within 1 to 10 MΩ, the device's I-V curves are measured using a Keithley 2400's two-wire ohm sensing method. RRAM features revealed in the I-V plots (V_{SET} , V_{RESET} , window size, HRS/LRS resistance) are compared before and after applying strain.

Switching speed of the device is determined by pulsing the device with single square waves until it switches from one resistive state into the other (with a window size of at least 20). The square wave is generated by a HP3312 function generator and is offset so that it delivers a entirely negative or positive pulse. Pulse times are equal to half of the square wave's period. To investigate

the switching speed from HRS to LRS, the experiment begins with a short pulse time (10 ns) and a small pulse amplitude (2 V). After each pulse, the resistance of the device is determined by acquiring a portion of its I-V in the linear regime (-0.05 to 0.05 V) and is compared to the original resistance. Pulse times are increased at this voltage bias until the resistance changes at least by a factor of 20. Data of the window size collected for pulse lengths close to the target pulse length may be linearly fit or extrapolated to determine the exact switching time at each bias. Switching from LRS to HRS requires the same process with a negative pulse. To more accurately determine the window size, the device must be set or reset (depending on which switch is being investigated) between pulses.

Hall measurements can be performed to determine carrier type and concentrations. Furthermore, a Physical Properties Measurement System (PPMS) can be used to find temperature dependency of RRAM features. Device I-V characterization with strain is typically destructive and performed last. Strain is applied to devices using a smooth, micrometer screw-tip. Devices are loaded into a custom strain stage, contacts facing away from the tip. Figure 5 shows the stage schematic with a loaded sample. Our preliminary experiments have only studied the effects of tensile strain. Studying compressive strain only requires flipping the device, contacts facing up.

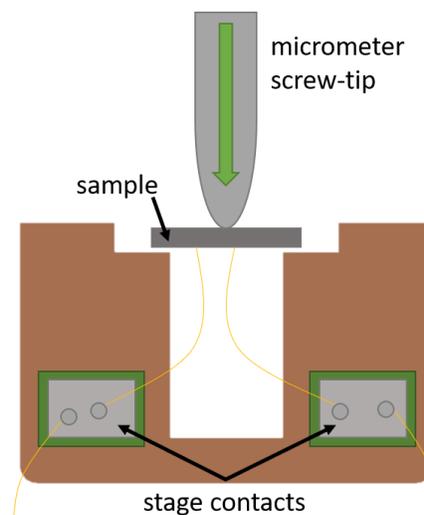


Figure 5. Schematic of strain device and sample.

Preliminary Results and Future Work

Before preparing Au/SrTiO₃/In devices, the strain device and characterization methods were tested with simpler Ag/SrTiO₃/In devices that do not require an additional step of evaporation. This device's I-V characteristic before and after strain are shown in Figure 6. Strain on the sample is approximated as $\epsilon \approx xt/L_0^2$ where x is the small displacement of the strain tip into the sample, and t and L₀ are the thickness and length of the sample respectively¹². The drop in current through the strained device is apparent, which may confirm the hypothesis of an increased dielectric constant. We calculated the strain on our devices as roughly $\epsilon = 0.05\%$, which is much greater than the critical strain ($\epsilon = 0.012\%$)¹¹ thus eliminating the idea of reduced quantum fluctuations as the root cause of an increasing dielectric constant. Additional data from several devices is required to confirm that this phenomenon of lowered current under strain is not anomalous. HRS resistance changed from 1.1 M Ω in the unstrained device to 550.0 M Ω in the strained device and LRS resistance changed from 91.0 k Ω to 694.7 k Ω . These resistance states reveal a dramatically enlarged window of approximately 790 in the strained sample compared to the window of 12 in the unstrained sample. The strained device's decreased current corresponds to a lower operational power. The power consumption can further be lowered by switching at lower biases without significantly compromising the device's large window size.

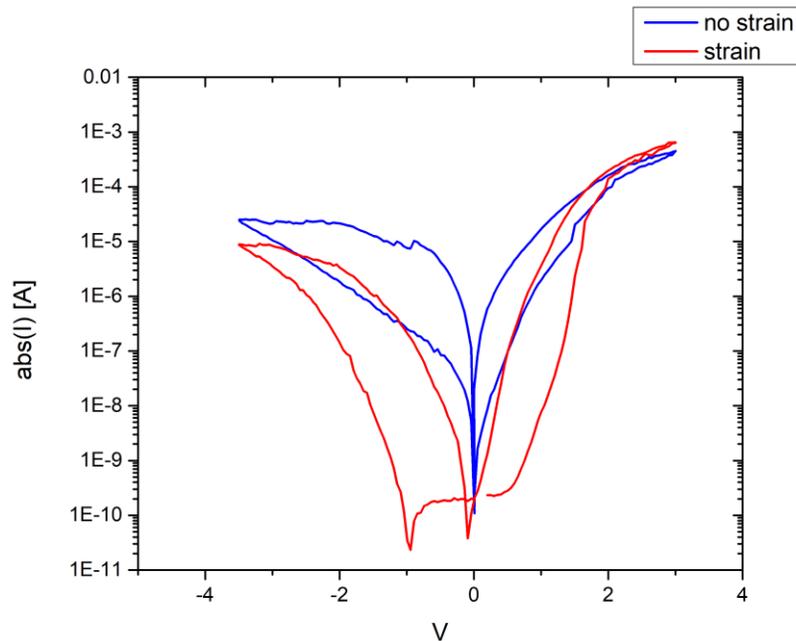


Figure 6. Ag/SrTiO₃/In device I-V curves with strain ($\epsilon = 0.05\%$) and without strain.

The origin of the leftward shift in the strained sample's I-V plot is unknown and still under investigation. The shift might have arisen from systematic instrumentation error or from intrinsic material properties. In the latter case, interface dipoles (originating from surface states) effectively screen the applied electric field over a range of biases. Thus, within this range the current through the device does not increase, shifting the I-V plot.

The theoretical value of the Schottky barrier height, Φ_B , is the energy difference between the metal's work function (silver alloy paint) and the semiconductor's (SrTiO₃) electron affinity. For this device: $\Phi_B = 5.00 \text{ eV} - 3.90 \text{ eV} = 1.10 \text{ eV}$. Using data from the I-V curves, we calculated the device's effective Schottky barrier height, Φ_B' , before and after strain. The actual value of the barrier height (determined by the Schottky emission current) cannot easily be determined experimentally because the various current contributions are difficult to distinguish. In general, $I_{total} = I_{SBE} + I_{TE} + I_{FE}$, where I_{SB} , I_T , and I_{FE} are the current contributions from Schottky emission, other thermionic emission (Poole-Frenkel), and field emission (Fowler-Nordheim and direct tunneling) respectively. Ideally, the Schottky barrier height will not vary with applied bias and will have an ideality factor (η) of 1. Experimentally, however, metal/semiconductor interface states, tunneling effects, and thermionic emission all increase the ideality factor. At forward bias, Schottky emission is the dominant source of current and thus, calculations of the effective Schottky barrier height are closer to the true value of Φ_B .

At low biases, the (thermionic emission dominated) current can be approximated using the Richardson-Dushman equation as $I \approx I_0 e^{eV/\eta kT}$ where e is the elementary charge, V is the applied bias, η is the Schottky barrier ideality factor, k is the Boltzmann constant, T is the temperature, and $I_0 = AR * T^2 e^{-e\Phi_B'/kT}$ where A is the contact area, R^* is the Richardson constant¹³. Rearranging the equation gives

$$\ln I = \ln(AR * T^2) - \frac{e\Phi_B'}{kT} + \frac{eV}{\eta kT}$$

which is used to calculate η and Φ_B' from the linear regime in the I-V plots.

Using an approximate contact area of 1 mm^2 , the unstrained device current ideality factor is calculated to be 4.8 in HRS and 7.1 in LRS. The strained device's current ideality factor is 3.9 in HRS and 4.6 in LRS. In LRS and HRS the unstrained device's Φ_B' was 0.83 eV and 0.71 eV respectively. Φ_B' for the strained device is 1.02 eV and 0.85 eV in HRS and LRS respectively. As

expected, the ideality factor drops for a device in LRS, when Schottky emission current competes with more field emission and thermionic emission.

Degradation in the devices is noticeable between measurements hours to days apart. One source of degradation is the diffusion of oxygen back into the SrTiO₃. Samples are kept in the ambient with ample opportunity to refill their intentionally introduced oxygen vacancies. Although the ambient oxygen will not fill all the vacancies, enough will be filled (especially close to the surface) to transition SrTiO₃ into a more insulating state.

One possible source of error may result from using several years old, previously annealed SrTiO₃. Although the samples have likely returned to their intrinsic state by refilling the originally introduced oxygen vacancies, they may have more defects and impurities from previous experiments. Past the preliminary experiments, freshly grown and control-annealed SrTiO₃ will be used. Another source of error may arise during the strain testing. The straining tip is metal and may itself be responsible for changing devices' electrical properties while it contacts the SrTiO₃ samples. Similarly, the strain stage is made of copper and any contact the device may have with it could affect the electronic measurements. To avoid any electrical effects from the tip and stage, paint or tape will be used to cover the metal areas to prevent them from directly contacting the sample.

After the sample preparation techniques are improved and the characterization during strain is improved to be nondestructive, the effects of strain on Au/SrTiO₃/In devices will be tested and compared with the strain effects on Ag/SrTiO₃/In devices. Furthermore, device performance will be investigated under tensile strain to confirm that both types of stress prove advantageous. Changes in switching speed in devices under strain will also be investigated. Performing switching speed experiments at various temperatures can reveal the prevailing switching mechanism. Additional efforts will be made to better control the annealing process. Annealing in partial oxygen pressure may help improve the surface smoothness, and thus improve device contacts and performance. Future experiments may investigate temperature effects on devices under strain in hopes of further elucidating the devices' complex dependence on these parameters. Further on the horizon, RRAM devices with 2D semiconducting vdW materials (such as transition metal dichalcogenides (TMDs) and brominated multilayer graphene) as electrodes may be studied under strain. These materials have yet to be thoroughly investigated—especially in the context of RRAM devices—and may reveal fascinating physical phenomenon. Overall, the preliminary results show

great promise in strained RRAM devices. More controlled studies of strain effects are possible through heteroepitaxial growth of SrTiO₃, introducing strain (compressive or tensile) through lattice mismatch. Strain engineering will be a critical component of maximizing future RRAM device performance.

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