ANALYSIS, MODELING, AND CONTROL OF FLOATING-BODY EFFECTS IN NANOMETER-GATE-LENGTH PARTIALLY DEPLETED SILICON-ON-INSULATOR CMOS DEVICES AND CIRCUITS

By

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KEY TO ABBREVIATIONS

BOX	back oxide
BTS	body-tied-to-source
CMOS	complementary metal-oxide-semiconductor
DIBL	drain-induced barrier lowering
FB	floating body
FD	fully depleted
GIDL	gate-induced drain leakage
IC	integrated circuit
MOSFET	metal-oxide-semiconductor field-effect transistor
NFD	non-fully depleted (partially depleted)
SOI	silicon-on-insulator
UFSOI	University of Florida silicon-on-insulator

Abstract of Dissertation Presented to the Graduate School of the
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This dissertation focuses on the analysis, modeling, and control of floating-body (FB) effects in scaled (nanometer-gate-length regime) silicon-on-insulator (SOI) complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs). Refinements to the University of Florida SOI (UFSOI) partially depleted (PD) (or non-fully depleted, NFD) SOI MOSFET model are developed and applied to gain insight into the behavior of SOI MOSFETs in integrated circuits.

The scalability of PD/SOI CMOS is assessed while giving a physically insightful analysis of the FB effect on off-state current (I_{off}), which tends to be high compared to that of bulk-Si technologies. The analysis shows that the FB effect on I_{off} can be naturally ameliorated by typical high operating temperatures (T) and increased junction recombination currents. Physical insight into such control of FB effects is provided.

An efficient new methodology to properly analyze hysteresis is developed utilizing the four fundamental delays of an FB PD/SOI CMOS inverter, which are defined. The hysteretic-delay analysis reveals the possibility of non-monotonic delays caused by a newly recognized dynamic-loading effect. Hysteresis trends are shown to increase or decrease when the device structure is modified; an asymmetric design concept is thereby conceived. Moreover, hysteresis is shown to worsen as the technology is scaled.

A new unified UFSOI modeling capability is implemented to enable performance of bulk-Si CMOS to be assessed as a counterpart technology to PD/SOI CMOS. This models allows a bulk-Si counterpart structure to be simulated with exactly the same device design assumptions as the PD/SOI technology. With this capability, the performance benefits for contemporary and scaled FB PD/SOI versus bulk-Si technologies are assessed. Insights underlying the benefits are given; the advantages are shown to diminish for scaled inverter circuits, while stacked gate logic circuits are shown to restore the performance advantage for the FB PD/SOI technologies.

The behavior of FB PD/SOI is investigated at low operating temperatures (T), revealing an anomalous drain current near and below the I_{off} condition. This anomalous current is shown to be caused by the parasitic lateral BJT and is corroborated by I-V and IDDQ measurements. The gate dependence of the BJT model in UFSOI is revised to improve its physical accounting of the behavior near and below the I_{off} condition. The impacts of two T-scaling scenarios are assessed, revealing a significant performance gain as T is decreased to -50°C to -100°C.

CHAPTER 1
INTRODUCTION

Silicon-on-insulator (SOI) MOSFETs have generated enormous interest due to the promise of improved isolation and integration density, reduced parasitic capacitances, and improved radiation-hardened features as compared to their bulk-Si counterparts. Along with providing superior power/performance, SOI CMOS is progressing towards becoming the ULSI technology of choice for low-power, high-performance electronic system applications.

Although both fully depleted (FD) and partially depleted (PD) SOI device structures are being developed in the semiconductor industry, PD/SOI CMOS has emerged as the leading candidate to become the mainstream device technology. This is due to the improved scalability and better threshold control (manufacturability) of PD/SOI leading to greater flexibility in optimizing the device design over FD/SOI. However, the floating body (FB) of the PD/SOI device, due to its isolated neutral body region, can lead to device and circuit instabilities causing unwanted glitches or failures in circuits, especially in dynamic logic and memory circuits. With SOI-material concerns rapidly diminishing, the problematic FB effects in PD/SOI technologies are the most significant design issue preventing its ubiquitous use in product designs.

The FB effects of PD/SOI are manifested in both the static (e.g., kink effect, single transistor latch, premature drain-source breakdown) and dynamic (e.g., transient threshold voltages, capacitive coupling to the body, drain current overshoot, hysteretic memory effects, transient parasitic bipolar leakage effects) operations of the device. To deal with the implied design issues, the unique behavior

of these FB effects must be fully understood (via physical mechanisms) and implemented into mature device models so that product designers can reliably evaluate their circuits for possible instabilities. The aim of this work is to assess the scalability of the PD/SOI device structure at both room temperature and moderately low temperature, while evaluating the FB effects and amenable approaches to control them. Extending and refining deficiencies of the UFSOI PD (or non-fully-depleted (NFD)) device model [Suh95], [Kri96], [Cha97b], [Wor99], [Fos99] are pursued when necessary to enhance its predictive capability. To truly capture the complex FB dynamics in PD/SOI technologies it is essential that the analyses use a physical (based on device structure and profile information) charged-based compact device model, such as the UFSOI model shown in Fig. 1.1. Empirical (especially capacitance-based) models are vulnerable to numerical instability, charge-nonconservation, and integrity issues, and hence are unreliable for accurately predicting the behavior of the FB PD/SOI technologies as described in this work.

The scalability and viability of PD/SOI CMOS are addressed in Chapter 2 while giving a physically insightful analysis of the FB effect on I_{off}, which tends to be high compared to that of bulk-Si technologies and significantly impacts the nominal design point and performance of a given SOI technology. The analysis indicates that the FB effect on I_{off} can be naturally ameliorated by typical high operating temperatures (T) and increased junction recombination currents. The temperature dependence of the induced body-source bias, $V_{BS}(T)$, is developed to gain insight into possible ways to control FB effects; it is shown to have a significant negative temperature coefficient. The impacts of using increased T and I_R as controlling techniques for the FB effect are evaluated in RO inverter circuits and

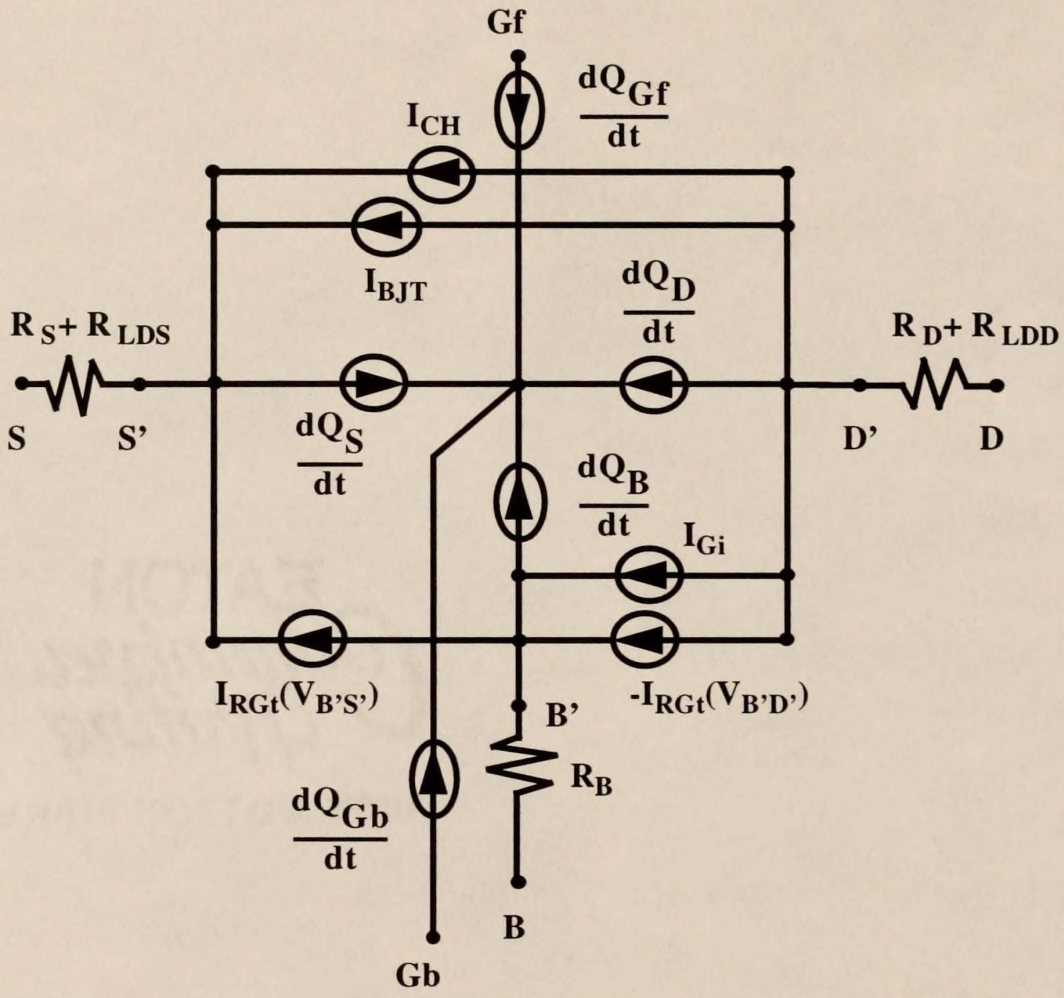


Figure 1.1 The network representation of the UFSOI physical charged-based compact device model.

device characteristics, the results of which contradict a negative assessment recently put forth in the literature [Cha97].

An efficient new methodology to properly analyze history-dependent propagation delay (hysteresis) [Suh94] is developed, including its true worst case, utilizing the four fundamental delays of a FB PD/SOI CMOS inverter that are defined in Chapter 3. This methodology enables a fundamental understanding of the complex FB dynamics that govern the hysteretic delays and provides the flexibility of analyzing variations in duty cycle and slew rate in any particular circuit. The analysis reveals the possibility of non-monotonic delays caused by a newly recognized dynamic-loading effect. Hysteresis trends are shown to increase or decrease by adjusting the device structure or by using a proposed asymmetric design concept. Moreover, hysteresis is shown to worsen as the technology is scaled, and the impacts of dynamic (i.e., changing gate load of an inverter chain) and heavy (e.g., long metal lines) loading effects are investigated. Additional analyses are included to provide insight into a discrepancy in the literature between simulations and measurements of the hysteretic delay.

A new unified modeling capability is implemented in UFSOI to enable performance assessments of bulk-Si CMOS in a stand-alone technology or as a counterpart technology to PD/SOI CMOS. This model allows a bulk-Si counterpart structure to be simulated with exactly the same device design assumptions as the PD/SOI technology, eliminating any ambiguities in device design and structure. With this capability, the performance benefits for contemporary and scaled FB PD/SOI versus bulk-Si technologies are assessed in Chapter 4. Insights underlying these

benefits are given; the advantages FB PD/SOI are shown to diminish for scaled inverter circuits, while stacked gate logic circuits are shown to restore the performance advantage for the FB PD/SOI technologies.

As the CMOS scaling trend begins to slow due to fundamental factors such as oxide tunneling, excessive off-state current, and voltage nonscaling [Tau97], [SIA99], one option to improve performance is to reduce the ambient operating temperature (T) of the semiconductor chip. In Chapter 5, the behavior of FB PD/SOI is investigated at low operating temperatures, revealing an anomalous drain current near and below the I_{off} condition. This anomalous drain current is shown to be caused by the parasitic lateral BJT and is corroborated by I-V and IDDQ measurements. The gate dependence of the BJT model in UFSOI, which predicted the anomaly, is revised to improve its physical accounting of the behavior near and below the I_{off} condition. As T decreases, I_{off} is shown to switch from being controlled by the MOSFET channel current to being controlled by the parasitic BJT current, which increases with decreasing T, giving rise to a non-monotonic trend for I_{off} and suggesting a possible limit to the low-T operating range. The impacts on threshold voltage and propagation delay for two T-scaling scenarios (*same-device* and *same-I_{off}*) are assessed revealing a significant performance gain as T is decreased to -50°C to -100°C, a practical range of operating T.

Chapter 6 summarizes the significant contributions of this work, and then concludes with recommendations to preserve the predictive capabilities of the UFSOI compact models as device technologies are scaled to dimensions (~10nm) near the end of the SIA roadmap [SIA99].

The Appendix describes an alternative device structure to suppress the FB effects in PD SOI CMOS, which naturally increases the recombination current of the

junctions. The modified device structure intentionally employs a gap between the source/drain regions and the buried oxide (e.g., as in [Hor96]). The gap provides additional junction area for recombination current at the source to prevent the build-up of excess charge in the neutral region of the body. A preliminary analysis of this device structure via Medici is included, showing the potential benefits of using such a design.

CHAPTER 2
ANALYSIS AND CONTROL OF OFF-STATE CURRENT IN SCALED PD/SOI WITH FLOATING BODIES

2.1 Introduction

A recent study [Cha97] of the scalability of partially depleted (PD) SOI CMOS technology led to the conclusion that it was no better than bulk-Si CMOS for sub-0.25μm logic applications, irrespective of its inherent advantages. The investigators argued that the PD/SOI nMOSFET would need a higher threshold voltage (V_t) to limit off-state current (I_{off}) because of the V_t reduction resulting from the drain (V_{DS})-induced floating-body (FB) effect, in addition to the barrier lowering (DIBL). Results obtained from circuits made by using the same process flow for SOI and bulk-Si wafers, except for a modification to give higher V_t for the SOI nMOSFETs, were presented to project inferior SOI speed performance for L_{eff} < 0.15μm, as well as undermined SOI (dynamic) power performance. Of course, the performance losses were due to the higher V_t.

In this chapter a physically insightful analysis of the FB effect on I_{off} is given, based on the scaled PD/SOI CMOS technology described in [Cha97], which contradicts the negative assessment of the scalability of SOI digital ICs. Operation at high chip temperatures (T=55-85°C) that are typical for high-performance circuits is shown to naturally ameliorate the FB effect, and previously proven techniques for controlling FB effects are shown to be effective in limiting I_{off} as well. Further, it is

shown that the amelioration at high T is significantly enhanced when the mentioned techniques are employed. The performance (I_{on}, τ_{RO}) impact of elevated temperature and increased I_R operation is shown to be minimal, and the analysis indicates that PD/SOI can achieve at least a 15% relative speed advantage over its body-tied PD/SOI (or bulk-Si) counterpart.

2.2 Analysis of the Floating-Body Effect on Off-State Current

The measured subthreshold I_{DS}-V_{GS} data plotted in Fig. 2.1 were given in [Cha97] for a floating-body PD/SOI nMOSFET with L_{eff} = 0.145μm and V_t = 0.61V (at low V_{DS}). These data and device structural information (4.5nm gate oxide, etc.) also given in [Cha97] were used to calibrate the non-fully depleted (or PD) model in UFSOI/SPICE [Fos97]. The UFSOI model is physical and process-based, and hence amenable to reliable calibration based on the device structure and minimal I-V data. Unlike typical empirical compact models, it has only a few parameters that need to be tuned to measured data, and hence it can be predictive, as exemplified in [Suh94]. The process-based calibration procedure used here is similar to that described in [Chi98]. The UFSOI model-predicted I_{DS}-V_{GS} characteristics, as shown superimposed in Fig. 2.1, match the data quite well and the results give good insight about the device and the technology. For example, the FB effect, reflected by the large V_{DS}-induced shift in $I_{DS}(V_{GS})$, is influenced significantly by GIDL [Che87]; with the GIDL current in the UFSOI model turned off, the predicted shift, shown in the figure, is much smaller at currents where impact ionization is not predominant in charging the floating body.

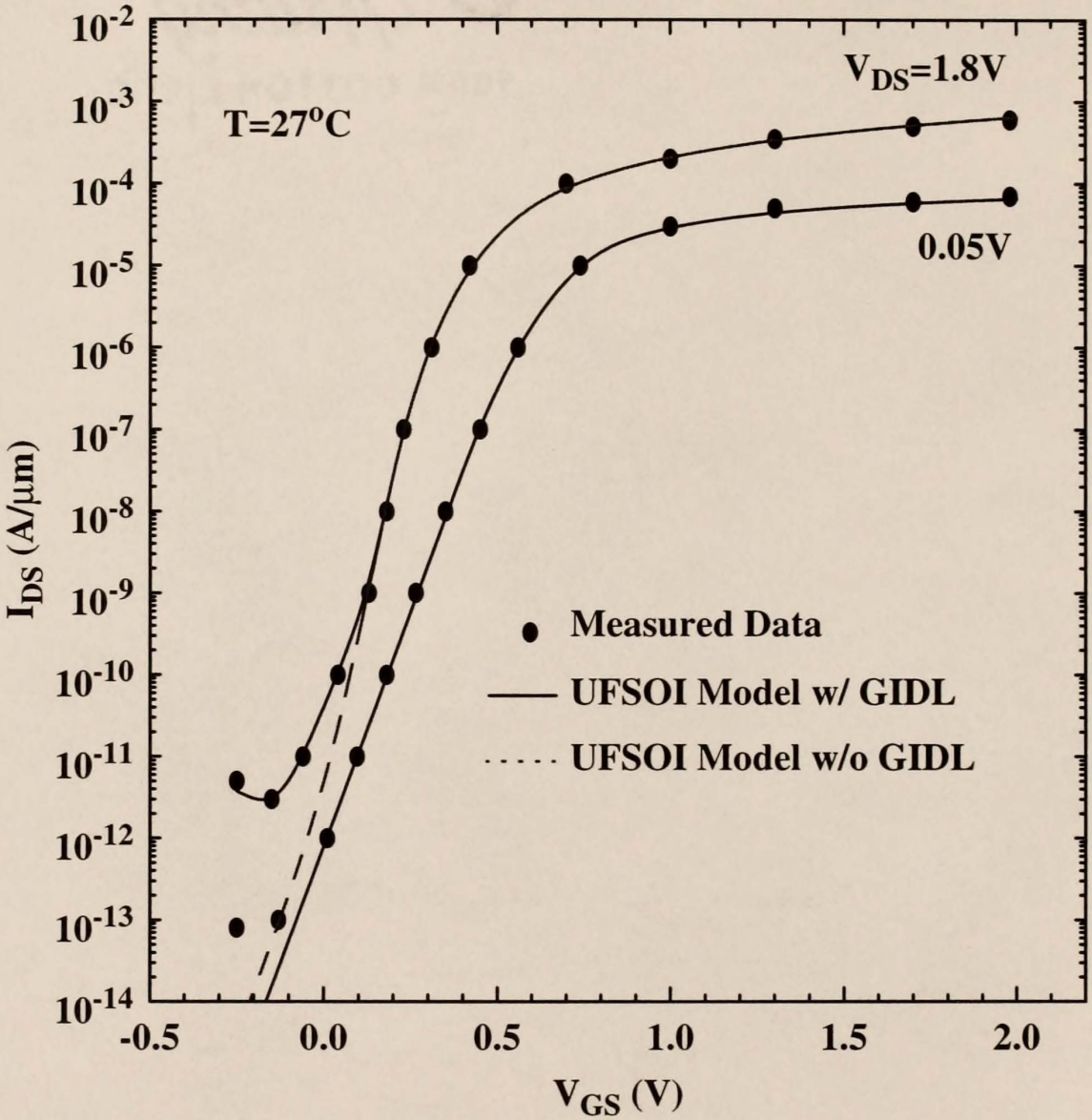


Figure 2.1 Model calibration for 145nm technology.
Measured subthreshold current-voltage characteristics of a PD/SOI nMOSFET (L_{eff}=145nm, t_{ox}=4.5nm, V_t=0.61V) [Cha97], and UFSOI-predicted characteristics with and without GIDL.

The high V_t was chosen in [Cha97] to limit I_{off} to about 1nA/μm (at T = 27°C) at V_{DD} = 1.8V for the minimum L_{eff} of 0.11μm in the 0.15μm PD/SOI CMOS technology described. In fact, the nominal V_t = 0.4V design (with lower channel doping) would yield an excessive I_{off} (drain current at V_{GS} = 0 with V_{DS} = 1.8V) for the L_{eff} = 0.11μm device as shown by the UFSOI-predicted characteristics in Fig. 2.2. By comparing the characteristics with those of the same device with its body tied to the source (BTS), also shown in Fig. 2.2, it can be seen that the large drain-induced shift of $I_{DS}(V_{GS})$ is due predominantly to the FB effect; at $I_{DS} = I_{off}$, the FB effect adds 219mV (ΔV^{FB} as labeled in Fig. 2.2) to that due to the DIBL effect. The latter, only about 80mV as reflected by the BTS device, is comparable to that of a 0.1μm bulk-Si device.

The FB effect increases I_{off} by more than two orders of magnitude in Fig. 2.2, and does indeed portend the need for higher V_t. (Note that the increase in V_t (143mV) needed to make $I_{off} = I_{off(BTS)}$, which is tantamount to $\Delta V^{FB} = 0$, is substantially smaller than ΔV^{FB}.) However, as the ambient, or chip temperature is raised, the FB effect becomes less severe as predicted by additional UFSOI/SPICE simulations. The temperature dependence of the UFSOI model [Wor98] is physical too, being defined directly by well known dependences of the pertinent physics-based model parameters without any new parameters. The inset in Fig. 2.2 gives UFSOI-predicted ΔV^{FB} versus T, and the corresponding relative increase in I_{off} due to the FB effect. For T=85°C, ΔV^{FB} is reduced to only about 100mV and the increase in I_{off} is reduced to less than one order of magnitude. Measured subthreshold current-voltage characteristics [Kri98b] of a L_{eff}=100nm nMOSFET as a function of T, shown in

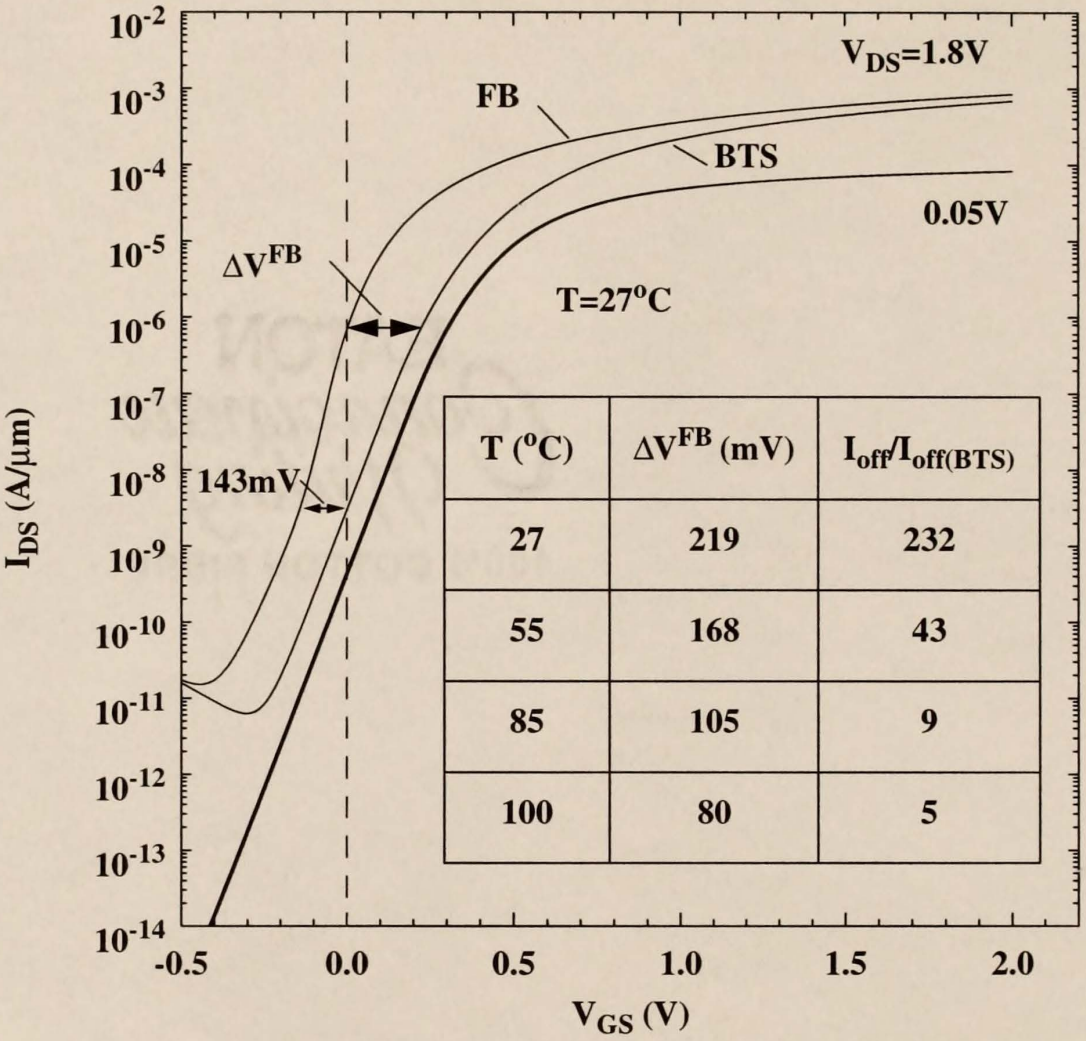


Figure 2.2 Predicted I_{DS}-V_{GS} for minimum L with nominal threshold. UFSOI-predicted subthreshold current-voltage characteristics of the L_{eff} = 0.11μm nMOSFET in the V_t = 0.4V (for L_{eff}= 0.145μm) design. The table inset gives the predicted ΔV^{FB} (as labeled) and I_{off} /$I_{off(BTS)}$ ratio for increasing temperature.

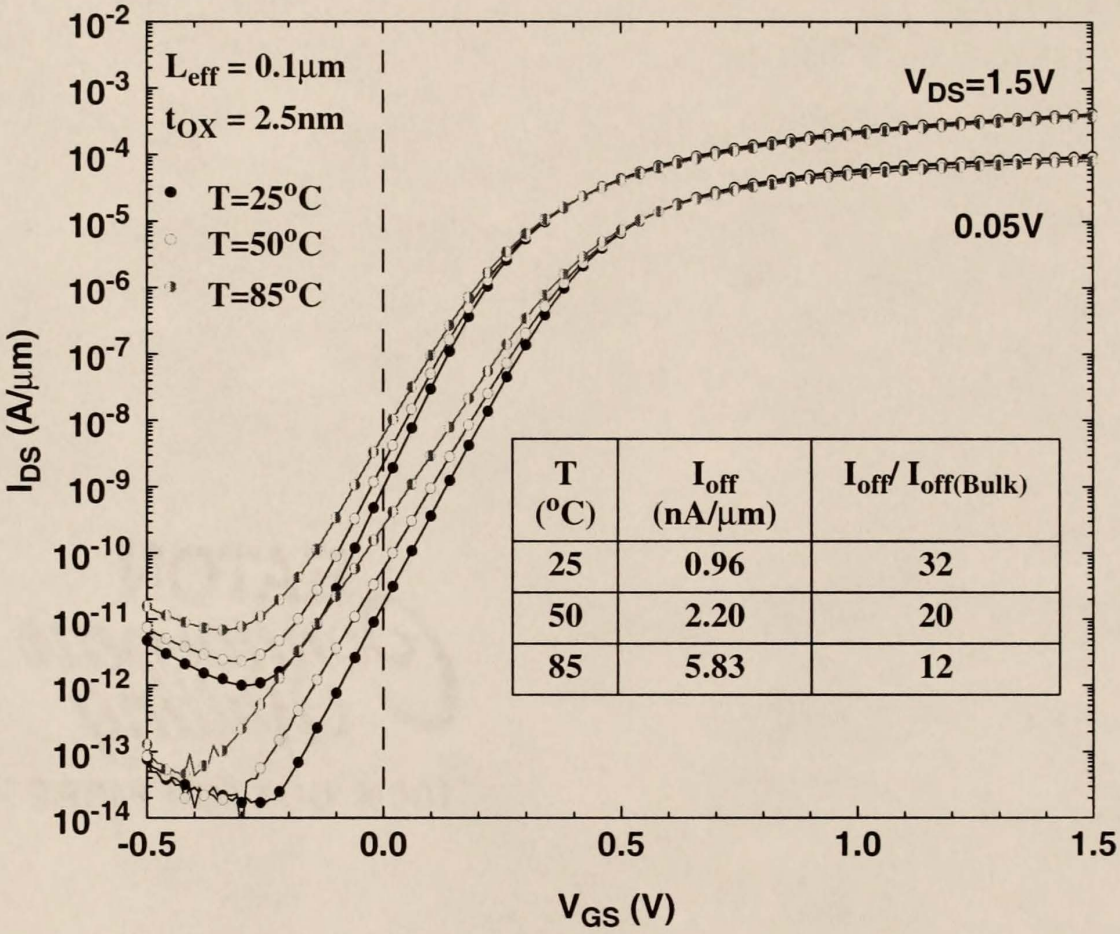
Fig. 2.3, corroborate the negative temperature-coefficient trend of the $I_{off}/I_{off(Bulk\text{-}Si)}$ ratio as predicted by the UFSOI models. These results imply the viability of scaled PD/SOI CMOS in high-performance applications where 55-85°C operation is typical. Explanation of this improvement at high T follows from a physics-based interpretation of the simulation results in Fig. 2.2.

2.3 Temperature Dependence of the Body Voltage at Off State

The FB effect underlying the increase in I_{off} is a reduction in V_t caused by a forward bias V_{BS} (i.e., a separation of the electron and hole quasi-Fermi potentials) developed on the body-source junction at high V_{DS}. Holes generated near the drain are injected into the floating body, and henceforth raise V_{BS} in support of carrier recombination to balance the generation in the DC steady state. The simulations of Fig. 2.2 (as well as measurements of typical scaled, low-V_t PD/SOI MOSFETs) show that the predominant generation mechanism in the subthreshold region is weak impact ionization driven by the channel current. Thermal generation (I_{Gt}) and tunneling current (I_{tun}) are negligible; GIDL, as depicted in Fig. 2.1, could be important for higher V_t. Thus, the generation current at the off condition is

$$I_G = I_{Gt} + I_{tun} + I_{GIDL} + (M-1)I_{off} \cong (M-1)I_{off} \qquad (2.1)$$

where (M-1) << 1 is the multiplication factor for impact ionization, which is characterized by a non-local model [Kri96] in UFSOI. (Note that lowering V_{DS}, or scaling V_{DD}, would reduce the FB effect since (M-1) would decrease sharply.) The



T (°C)	I_{off} (nA/μm)	I_{off}/ $I_{off(Bulk)}$
25	0.96	32
50	2.20	20
85	5.83	12

Figure 2.3 Measured I_{DS}-V_{GS} for 100nm technology as a function of T. Measured subthreshold current-voltage characteristics [Kri98b] of an L_{eff}=0.1μm nMOSFET that corroborate the UFSOI model predictions. The table inset gives the measured I_{off} and I_{off} /$I_{off(Bulk-Si)}$ ratio for increasing temperature that corroborates the decreasing $I_{off}/I_{off(bulk-Si)}$- ratio trend of the UFSOI model predictions in Fig. 2.2.

off-state *channel* current in the FB device can be expressed in terms of that in the BTS device [Suh95]:

$$I_{off} = I_{off(BTS)} \exp\left[\frac{qV_{BS}}{\left(\frac{1+\alpha}{\alpha}\right)kT}\right] \tag{2.2}$$

where $\alpha = C_b/C_o$ (= 0.42 for the technology in [Cha97]) is the ratio of the depletion and oxide capacitances of the MOS structure.

The DC value of V_{BS}, which governs I_{off}, is thus defined by

$$I_G = I_R \cong I_{RO} \exp\left(\frac{qV_{BS}}{mkT}\right) \tag{2.3}$$

where the recombination current I_R (for $V_{BS} > 0$) is represented by the general forward-bias diode equation [Sze81] with $1 \leq m \leq 2$ (= 1.3 for the technology in [Cha97]). For increasing T, both I_G and I_R in (2.3) increase, but at different rates depending on the device design. Insight on optimal design as well as on the predicted temperature dependences of I_{off} and ΔV^{FB} in Fig. 2.2 is obtained by combining (2.3) with (2.1) and (2.2). Using the basic weak-inversion current relation $I_{off(BTS)} \propto n_i^2 \exp(q\psi_s/kT)$ [Suh95], where ψ_s ($\cong -\Phi_{MS}/(1+\alpha) \cong 0.75V$) is the surface potential when $V_{GS} = 0$, we get

$$V_{BS}(T) \cong \frac{m(1+\alpha)}{1+\alpha-m\alpha}\left[\psi_s + \frac{kT}{q}\ln\left(C\mu\left(\frac{kT}{q}\right)^2 (M-1)\frac{n_i^{\,2}(T)}{I_{RO}(T)}\right)\right] \tag{2.4}$$

where C is assumed constant ($=qW/(L_{eff}N_BE_{xf})$). The coefficient in (2.4) is positive and has only weak dependence on T. The predominant T dependence of V_{BS} is defined by the ln term, the argument of which dictates whether V_{BS} will decrease or increase with T. Since (M-1) has relatively weak T dependence [Wor98], [Kri96] and $I_{RO} \propto n_i^{(3-m)}/\tau_r$ is representative [Wor98], [Sze81], we can write:

$$V_{BS}(T, m, I_{RO}) \cong \frac{m(1+\alpha)}{1+\alpha-m\alpha}[F(T, m, I_{RO})]$$

with

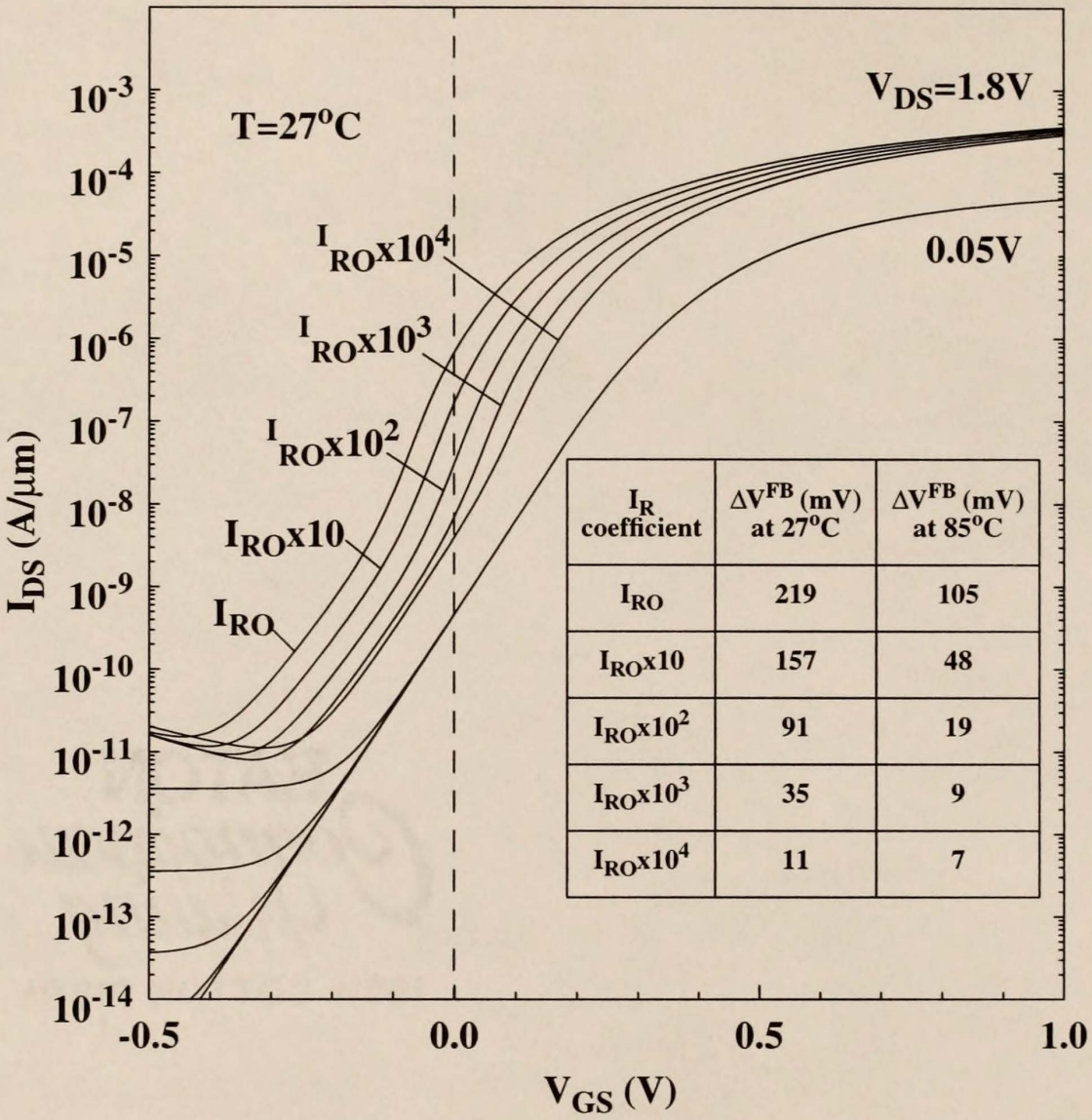
$$F(T, m, I_{RO}) = \left[\psi_s(T) + \frac{kT}{q}\ln\left(C\mu\left(\frac{kT}{q}\right)^2(M-1)\frac{n_i^{m-1}(T)n_i^{3-m}(T_{ref})\tau_r}{I_{RO}(T_{ref})\tau_r(T_{ref})}\right)\right] \quad (2.5)$$

where τ_r is the carrier recombination lifetime and T_{ref} is a reference temperature. Note that the ln argument varies as $\sim\tau_r n_i^{(m-1)}$. Hence for m low (~1), the $n_i(T)$ dependence is negated and the ln argument tends to be less that unity, giving $V_{BS}(T)$ a negative temperature coefficient. This is the case for the technology in [Cha97] as implied by the simulations of Fig. 2.2; at $I_{DS} = I_{off}$, $V_{BS} = 0.47V$ at 27°C and it drops to 0.12V at 100°C. However for m high (~2), the $n_i(T)$ dependence undermines the negative temperature coefficient of $V_{BS}(T)$ and possibly makes it positive. Note though that decreasing the lifetime τ_r, or increasing I_{RO}, makes the ln argument smaller, and hence tends to give a negative temperature coefficient as well as lowering V_{BS} at a specific T.

2.4 Controlling Floating-Body Effects at the Off-State Condition

This insight afforded in Sec. 2.4 suggests how the FB effect on I_{off} can be controlled by design. Killing carrier lifetime via defects created by ion implantation of inert ions has been shown to effectively enhance recombination current in SOI MOSFETs. Implantation of Ar in the source/drain junction regions [Ohn98], or implantation of Ge in the channel region [Wei93] and/or in the source/drain regions [Yos97], which are simple processes that are not incompatible with scaled CMOS technology, can increase I_{RO} by orders of magnitude. Implantation-induced defects result in bandgap traps, which lower τ_r. The generation lifetime is lowered too, but, as indicated in (2.1), the increase in I_{Gt} is inconsequential. (Junction tunneling, e.g., that resulting from halo regions [Che97], can supplement I_R at the source, but can also augment I_G at the drain. Its benefit, if any, would depend on the nature of the forward- and reverse-bias tunneling current components.)

UFSOI-predicted subthreshold characteristics of the device of Fig. 2.2 at 27°C for increasing I_{RO} (and I_{Gt} accordingly), via lowering τ_r (and τ_g), are shown in Fig. 2.4; the inset tabulates the decreasing ΔV^{FB}. For I_{RO} increased by a factor of 100 over its calibrated value (Fig. 2.2), ΔV^{FB} is reduced to only 91mV; for another order of magnitude or so of lifetime killing, the FB effect on I_{off} is virtually eliminated. The increasing I_{Gt}, evident in the low-V_{DS} characteristics in Fig. 2.4 at negative V_{GS}, is innocuous. Furthermore, as indicated by (2.4) and (2.5), the benefit of operation at higher T is substantively enhanced by the lifetime killing. Predicted ΔV^{FB} at 85°C is included in the inset of Fig. 2.4. At 85°C, with I_{RO} increased by a factor of 100, ΔV^{FB}



I_R coefficient	ΔV^{FB} (mV) at 27°C	ΔV^{FB} (mV) at 85°C
I_{RO}	219	105
$I_{RO}x10$	157	48
$I_{RO}x10^2$	91	19
$I_{RO}x10^3$	35	9
$I_{RO}x10^4$	11	7

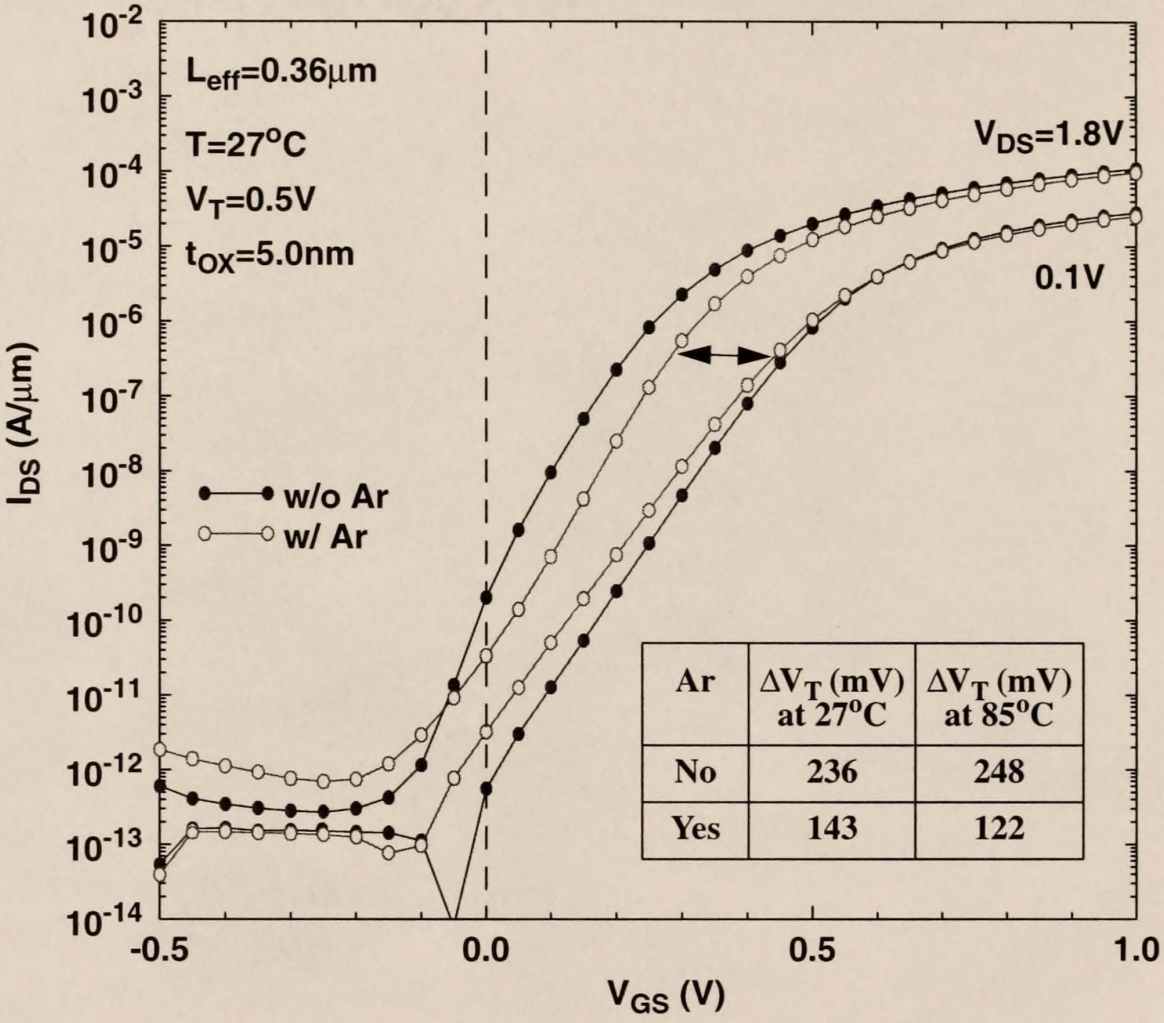
Figure 2.4 Predicted I_{DS}-V_{GS} as a function of recombination current. UFSOI-predicted subthreshold current-voltage characteristics for increasing thermal recombination (and generation) current in the nMOSFET of Fig. 2.2. The table inset gives the corresponding ΔV^{FB} at two temperatures.

(= 19mV) is smaller than the thermal voltage (kT/q = 31mV) and I_{off} (= $1.5I_{off(BTS)}$) is nearly equal to that of the BTS device. (Note that even though the lifetime killing typically increases m and I_{RO}, the latter increase is predominant in (2.4), ensuring a negative temperature coefficient for $V_{BS}(T)$, as will be illustrated in Fig. 2.6.) Recently published data from [Cha98], which employed a high-energy Ar implantation into the source/drain regions of the MOSFET to intentionally induce recombination centers in the silicon, corroborate this prediction and our simulation results, as shown in Fig. 2.5. These data demonstrate a decreasing ΔV_t trend at 27°C and a shift in the temperature coefficient of ΔV_t from positive to negative when Ar (lifetime killing) is employed.

The predicted sensitivity of $V_{BS}(T)$ to m and I_{RO} is shown in Fig. 2.6(a). For low m (~1), $V_{BS}(T)$ has a strong negative coefficient, which is reflected by the simulations of Fig. 2.2, where m=1.3 for the technology in [Cha97]. However, the negative coefficient of $V_{BS}(T)$ is undermined as m is increased, leading to a temperature insensitive $V_{BS}(T)$. However, as shown in Fig. 2.6(b) for high m (=2), increasing I_{RO} tends to restore and enhance the negative coefficient of $V_{BS}(T)$.

2.5 Effects on Performance

The corresponding predicted variations of on-state current (I_{on}) for the devices of Fig. 2.2 are depicted in Fig. 2.7. For the FB device at 27°C, I_{on} is only reduced by 5% when I_{RO} is increased by 100X, as indicated in the table inset. When T increases to 85°C, I_{on} decreases substantially more for the FB device than the BTS device; however, the additional loss in drive current is not manifested into a slower



Ar	ΔV_T (mV) at 27°C	ΔV_T (mV) at 85°C
No	236	248
Yes	143	122

Figure 2.5 Measured I_{DS}-V_{GS} with and without Ar I/I.

Measured [Cha98] subthreshold current-voltage characteristics of the L_{eff}=0.36μm nMOSFET. The table inset gives the measured ΔV_t at two temperatures (27°C and 85°C). The decreasing ΔV_t trend at 27oC and the shift in the temperature coefficient of ΔV_t when Ar (lifetime killing) is employed corroborates the UFSOI model predictions of Fig. 2.4.

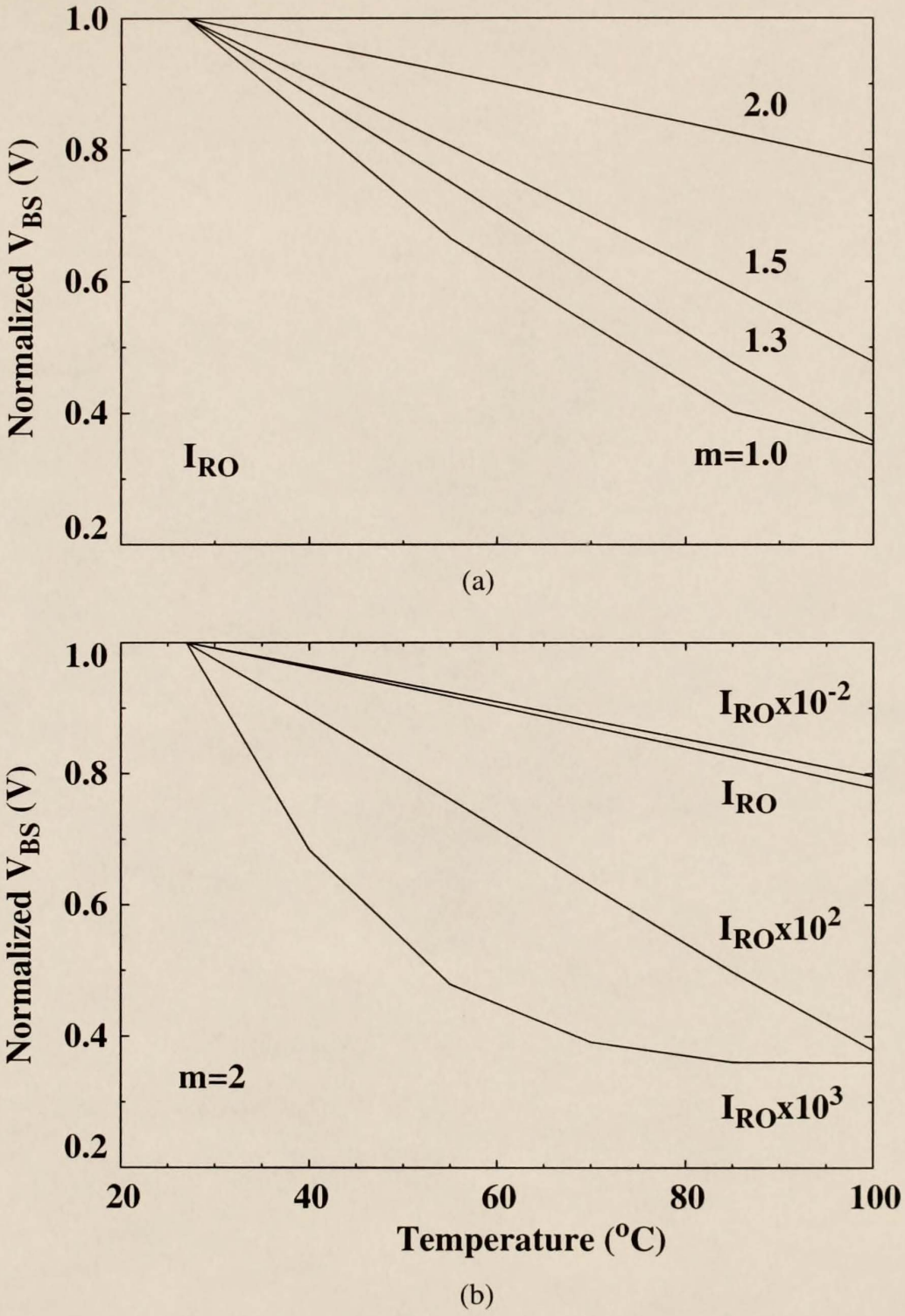
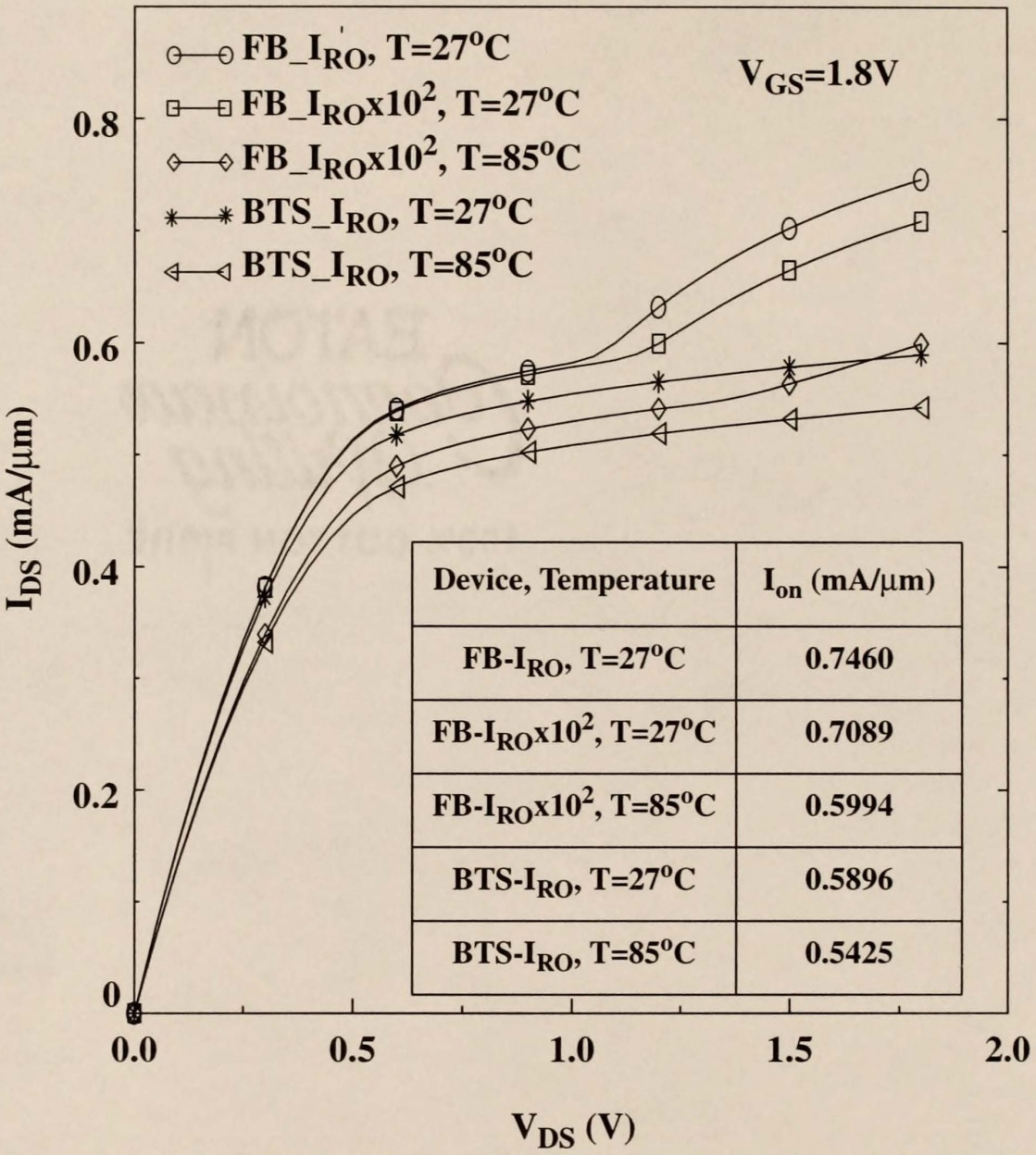


Figure 2.6 Floating-body voltage versus T with m and I_R varying.
Predicted sensitivity of the body-source voltage (V_{BS}) to temperature for variations in (a) ideality factor (m) and (b) recombination current (I_{RO})/ lifetime.



Device, Temperature	I_{on} (mA/μm)
FB-I_{RO}, T=27°C	0.7460
FB-I_{RO}x10², T=27°C	0.7089
FB-I_{RO}x10², T=85°C	0.5994
BTS-I_{RO}, T=27°C	0.5896
BTS-I_{RO}, T=85°C	0.5425

Figure 2.7 Predicted I_{DS}-V_{DS} for T and I_R variations.
UFSOI-predicted output current-voltage characteristics for nominal and 100X thermal recombination currents in the nMOSFET of Fig. 2.2 at 27°C and 85°C. The table inset gives the corresponding I_{on} (V_{DS}=V_{GS}=1.8V).

performance. In fact, the FB circuit performance at 85°C (see Fig. 2.8) is faster than that of the BTS circuit at 27°C, which is a consequence of the dynamic threshold in the FB device. These results undermine the utility of I_{on} as a figure-of-merit for FB/SOI technologies. The circuit performances are reflected by the UFSOI/SPICE-simulated gate propagation delay (τ_D), plotted in Fig. 2.8 as a function of supply voltage, of a CMOS inverter ring oscillator with the FB and BTS devices of Fig. 2.7. For T=27°C and V_{DD}=1.8V, τ_D for the FB circuit is only increased by 4% when I_{RO} is increased by 100X, and by <2% at V_{DD}=1.0V. Then, raising T to 85°C increases τ_D of the FB circuit by only 15%, compared to 12% for the BTS circuit. At 85°C and V_{DD}=1.8V, the BTS circuit is 17% slower than the FB circuit with the 100X I_{RO}, and is 27% slower at V_{DD}=1.0V. These results indicate that the FB device reflected in Fig. 2.2, with a 100X increase in I_{RO} and operating at 85C, will have an equivalent I_{off} and at least a 15% advantage in circuit speed relative to its BTS, or bulk-Si counterpart.

2.6 Conclusions

UFSOI/SPICE simulations, calibrated to the scaled PD/SOI CMOS technology in [Cha97], have been used to gain physical insight concerning the FB effect on I_{off}, and to note the efficacy of proven lifetime-killing processes, in conjunction with normal high chip temperature operation, in suppressing the FB effect. The insight explains why the effect can be naturally ameliorated by operation at high temperatures that are typical for high-performance circuits. The results contradict the negative outlook for SOI digital circuits put forth in [Cha97], and

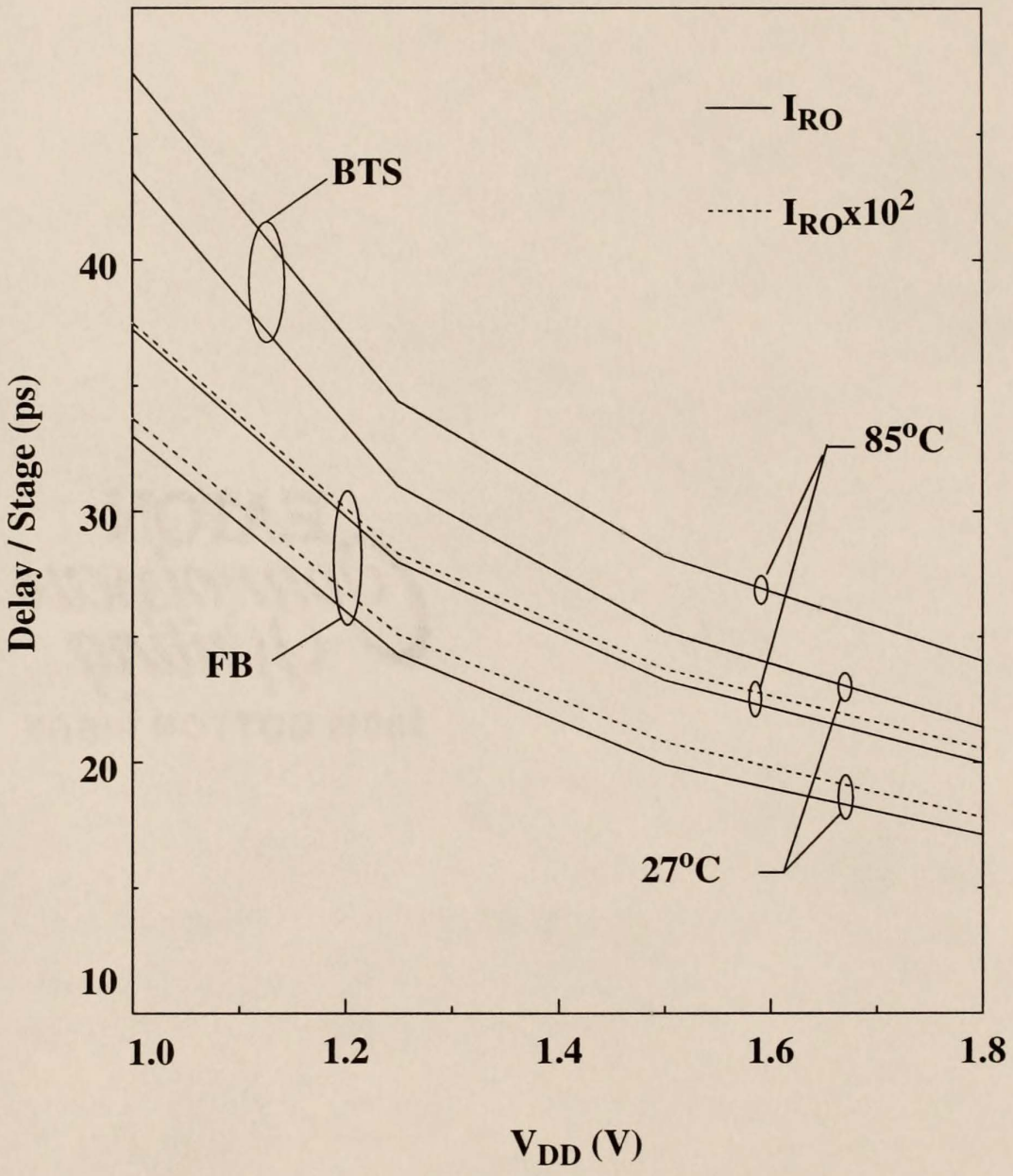


Figure 2.8 Predicted RO delay vs. VDD with T and I_R variations
Simulated gate-propagation delay of a nine-stage CMOS inverter ring oscillator comprising the FB and BTS devices in Fig. 2.5 versus supply voltage; $L_{eff\ n,p}$= 0.145µm, W_P/W_N=32/16, C_{LOAD}=10fF.

imply that PD/SOI CMOS technology can be optimally designed to be scalable with low V_t such that its inherent advantages can be exploited in low-power as well as high-performance digital IC applications. The advantages include not only negligible source/drain junction capacitance, which as noted in [Cha97] tends to be undermined in predominantly interconnect-loaded circuits, but others such as the elimination of the normal body effect ($V_{BS} < 0$ in nMOSFETs), which is significant in interconnect- as well as gate-loaded circuits having stacked devices or pass transistors. UFSOI/SPICE circuit simulations based on the model calibration done herein reveal that on-state currents are not significantly reduced when I_{off} is controlled as discussed, and that FB SOI/CMOS IC performance (speed versus power) can indeed be superior to that of bulk-Si CMOS when the devices are properly designed.

CHAPTER 3
ANALYSIS AND CONTROL OF HYSTERESIS IN PD/SOI CMOS

3.1 Introduction

As ULSI SOI CMOS technologies mature and become more pervasive in industry, controlling floating-body (FB) effects in partially depleted (PD) SOI MOSFETs, such as increased off-state current as studied in Chapter 2, is essential for defining a nominal design center for a technology. Perhaps the most worrisome FB effect is hysteresis [Suh94], e.g., history-dependent propagation delay, which is due to the relatively slow carrier recombination/generation processes, indicated in the device structure in Fig. 3.1, superimposed on the fast body charge dynamics driven by the intrinsic capacitive coupling. In this chapter, we define a new methodology to characterize and analyze hysteresis in PD/SOI CMOS inverter-based circuits, including its true worst case, and we provide new insight into the underlying physics. We use this methodology to explore novel device/circuit designs for controlling hysteresis. We show that scaling will tend to worsen the hysteretic effects, necessitating the implementation of specific hysteresis-controlling techniques at both the device and circuit levels.

The hysteretic delay trends described above are evaluated in a microprocessor latch-based pipelined circuit to assess timing fail mechanisms and amenable techniques to control them. By employing a newly described *asymmetric*

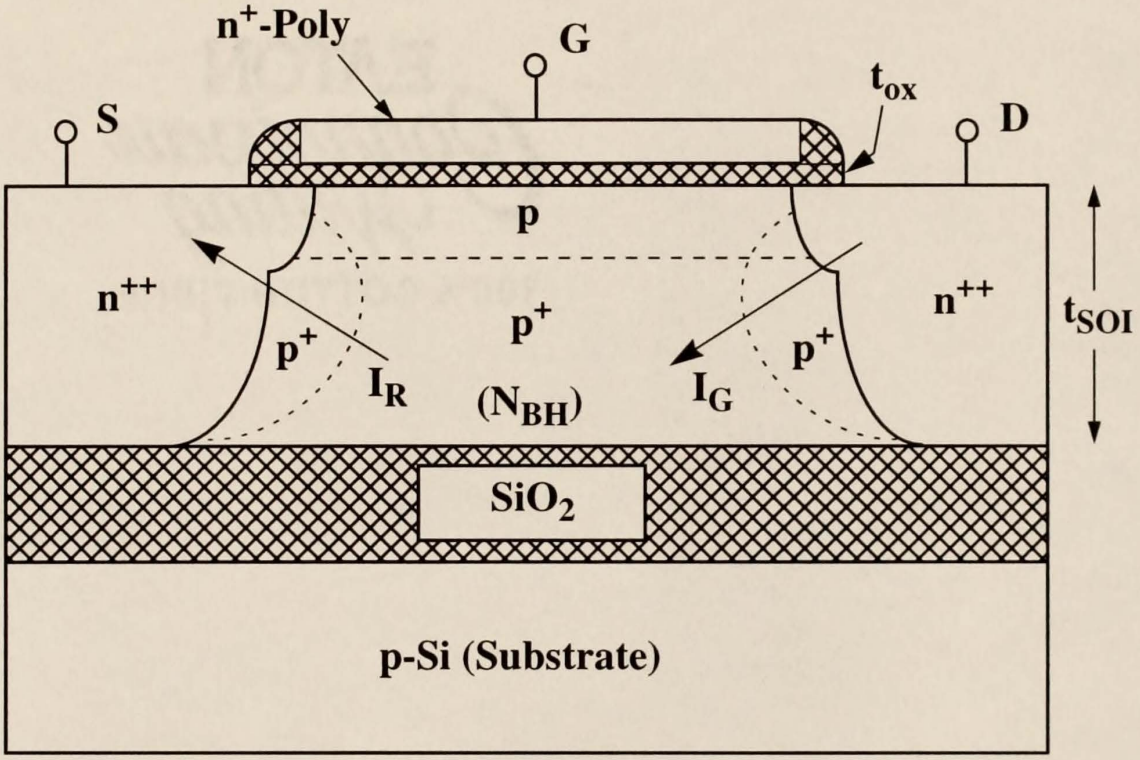


Figure 3.1 Schematic depicting I_R and I_G charging.
Schematic cross-section of the floating-body PD/SOI nMOSFET indicating the recombination/generation-defined body charging.

SOI CMOS design concept, the hysteresis associated with a given fundamental delay is shown to be adjusted sufficiently to eliminate the fail mechanism and allow normal operation of the circuit.

3.2 Fundamental Delays and Methodology

A new methodology is developed to characterize the hysteretic propagation delay versus time from DC to dynamic steady state. The simulation-based method utilizes the *four fundamental delays* obtained from a single-stage CMOS inverter, a basic building block for higher-order digital circuits, thus providing the flexibility of analyzing variations in duty cycle and slew rate in any particular circuit. The four delays, illustrated in Fig. 3.2, are obtained from two separate initial conditions for the input voltage: 1) DC low-to-high (LH) transition, and 2) DC high-to-low (HL) transition. The corresponding initial output voltages define the nMOSFET and pMOSFET initial body charges, which affect the delays. When V_{DS} is high for a long time, the body is charged, implying fast delays, whereas V_{DS}=0V implies no body charge and slow delays. The pull-down-fast (a.k.a. as "first-switch") ($\tau_{pd\text{-}f}$) and pull-up-slow (a.k.a. as "second-switch") ($\tau_{pu\text{-}s}$) delays are obtained from the first and second transitions of the LH input condition, respectively; and the pull-up-fast ($\tau_{pu\text{-}f}$) and pull-down-slow ($\tau_{pd\text{-}s}$) delays are obtained from the first and second transitions of the HL input condition, respectively. Application-specific averages of these four fundamental delays define pertinent circuit delays; for example, as illustrated in Fig. 3.2, the "fast" open-chain average delay ($\tau_{OC\text{-}f} = (\tau_{pd\text{-}f} + \tau_{pu\text{-}f})/2$), the "slow" open-chain average delay ($\tau_{OC\text{-}s} = (\tau_{pd\text{-}s} + \tau_{pu\text{-}s})/2$), and the

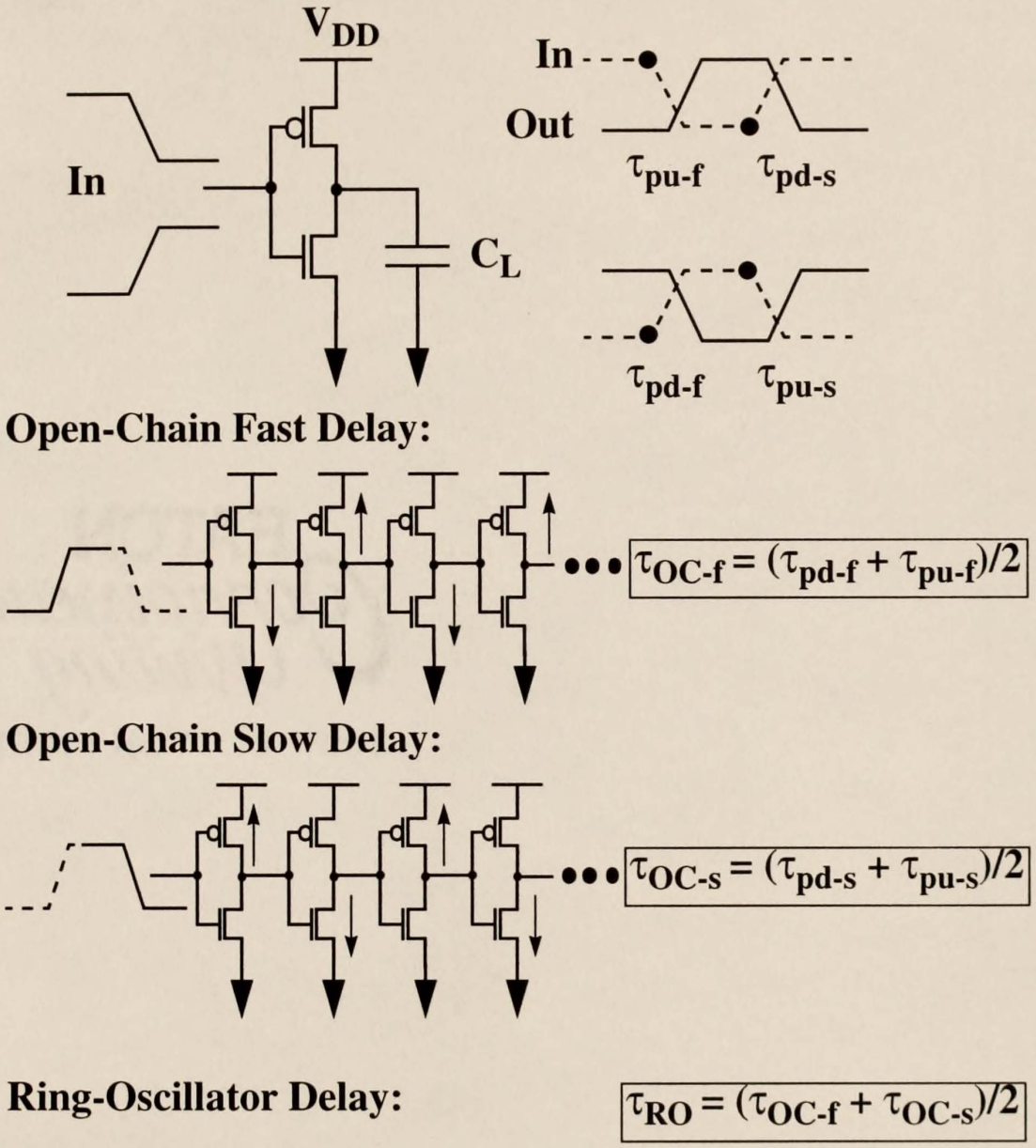


Figure 3.2 Definitions of fundamental and average delays.
Schematic representation of the four fundamental and average delays of floating-body PD/SOI CMOS inverter-based circuits. The arrows depict the active devices as the waveform propagates down the chain for the first ($\tau_{OC\text{-}f}$) and second ($\tau_{OC\text{-}s}$) transition of the input waveform.

(pre-biased) ring-oscillator average delay ($\tau_{RO} = (\tau_{OC\text{-}f} + \tau_{OC\text{-}s})/2$), which are the delays obtained by common measurements.

Possible hysteresis associated with the four fundamental delays and the three noted average delays, simulated with our physical charge-based device model (UFSOI/Spice3 [Fos99]) for repetitive input pulsing, is indicated in Fig. 3.3(a) for the L_{eff}=145nm technology (t_{ox}=4.5nm, t_{SOI} =150nm, V_t=0.4V @ I_{DS}=100nA*W/L) in Chapter 2. The corresponding body-to-source voltages for the nMOS (V_{BSn}) and pMOS (V_{BSp}) devices are shown in Fig. 3.3(b). The body voltages were recorded at time-points just prior to the input rise and fall transitions, as indicated by the dots superimposed on the input waveforms in Fig. 3.2. (Note that $V_{BS}(t)$ is virtually periodic over one period of the input waveform as defined by the capacitance coupling, but with the average value slowly changing in accord with the net recombination/generation [Kri98].) The predicted average delays all decrease in time by 4-7%, with $\tau_{OC\text{-}s}$ showing the largest variation. The four fundamental delays show significantly larger, *non-monotonic* variations, with a worst case of 9% for $\tau_{pd\text{-}s}$ occurring prior to the dynamic steady state.

The dynamic threshold voltage ($V_t(t)$) and the hysteretic propagation delay in PD/SOI circuits are governed by the transient body voltages in both the nMOS and pMOS devices, dependent on the input pulse waveform as well as the electrical properties of the device (e.g., recombination, generation, and capacitive coupling). The initial DC values of the body voltages are defined by the condition of equal recombination and generation currents (I_R=I_G in Fig. 3.1) in the devices. The

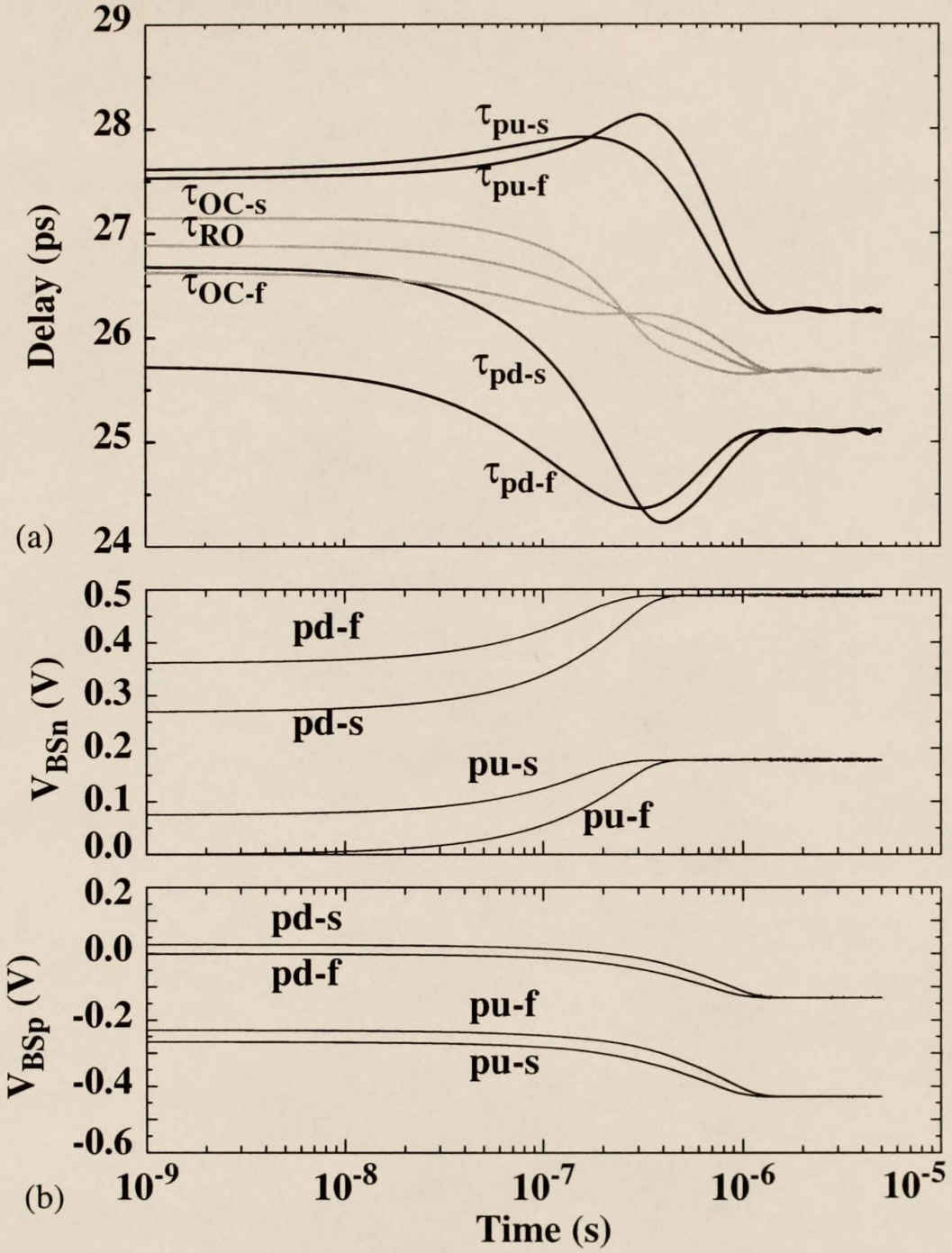


Figure 3.3 Hysteretic delay and body voltage results of an CMOS inverter. Simulated floating-body PD/SOI CMOS inverter-based delays showing non-monotonic hysteresis: a) delay versus time, and b) corresponding nMOSFET and pMOSFET $V_{BS}(t)$ prior to each input transition. (L_{eff}=145nm, V_t=0.4V, T=27°C, V_{DD}=1.8V, $\tau_{rise}=\tau_{fall}$=100ps, W_p/W_n=32/16, C_L=85fF, Per=1ns, 50% duty cycle)

dynamic steady-state body voltages are defined by the condition of equal integrated I_R and I_G over one period:

$$\int_{Per} I_G(t)dt = \int_{Per} I_R(t)dt \quad . \tag{3.1}$$

The dynamic steady-state condition (3.1), which typically takes several microseconds to obtain, implies different (corresponding) body voltages than the DC condition, and hence reflects hysteresis; but the intermediate transient body voltages show the complete (and worst-case) hysteresis as evident in Fig. 3.3.

3.3 Dynamic Loading Effect

The non-monotonic hysteretic behavior is manifested by the asymmetry of the FB charging currents in both devices of the CMOS inverter, due mainly to the difference of the impact-ionization coefficients for electrons and holes. A newly recognized *dynamic-loading* effect is revealed when the pMOSFET body continues to charge ("strengthen" as $|V_{BSp}(t)|$ increases) subsequent to a dynamic steady-state condition for the nMOSFET as evident in Fig.3.3(b). It is clear from Fig. 3.3 that, because of the dynamic loading, the common practice of setting the body voltage to high and low values to estimate the range of hysteresis will not capture the true worst-case delay variation in a given technology.

The *dynamic-loading* effect is a manifestation of the dynamic V_t of the load device on the switching delay of the inverter. For example, in the pull-down transient, when the nMOSFET current is discharging the output node, it also has to support the pMOSFET channel current along with the capacitive charging current of

the drain (dQ_D/dt). As the pMOSFET's $V_t(t)$ is lowered during the pull-down transient (via gate-body coupling) and previous switching cycles (via body charging), its channel current becomes larger, which lengthens the pull-down delay by effectively reducing the nMOSFET drive current that is discharging the node capacitance. This newly recognized effect can be important for heavy as well as light loads.

3.4 Dynamic-Gate and Heavy-Loading Effects

To assess if the proposed hysteresis characterization methodology is generally applicable, two additional loading conditions were evaluated. The first utilizes a second inverter stage as a representative dynamic load, as shown in Fig 3.4(a) with the hysteretic propagation delay results shown in Fig. 3.4(b). Although all of the delays are shortened compared to the results of Fig. 3.3 with a static gate capacitance load, the non-monotonic hysteretic behavior is still present and has nearly the same delay variation, thus demonstrating the utility of the characterization methodology.

The second condition is a large load, (e.g., long metal line), as exemplified in Fig. 3.5(a). The delay results of Fig. 3.5(b) show monotonically decreasing delays, which demonstrates how the charge dynamics of a large load at the output node can inhibit the dynamic-loading effect of the load transistor of the CMOS inverter. In this case, The nodal equation during a pull-down transient is given by

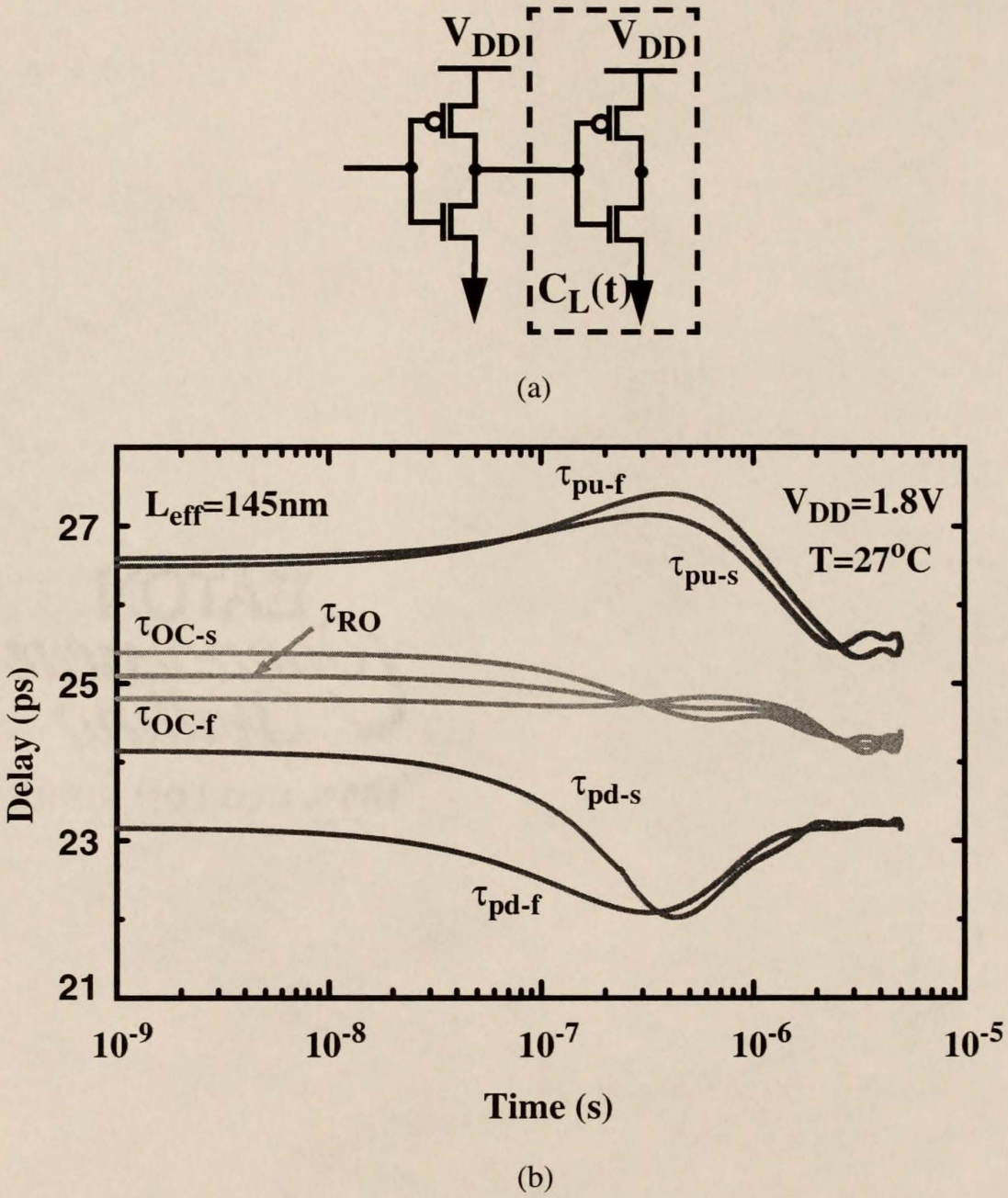
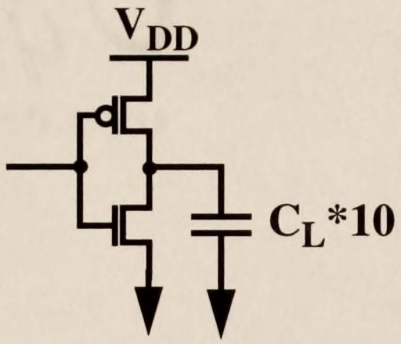
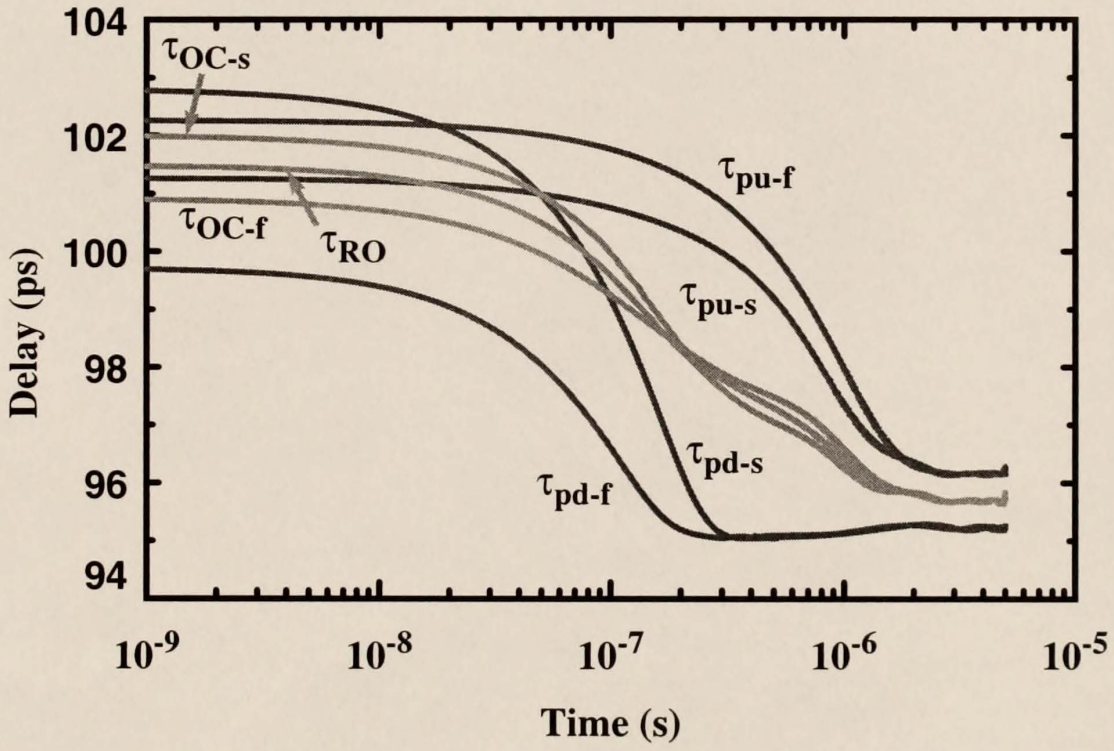


Figure 3.4 Dynamic loading effect on hysteretic delays.
Hysteretic delays for dynamic output node load (replaced static load of Fig. 3.3 with actual gate load of subsequent inverter stage). (L_{eff}=145nm, V_t=0.4V, T=27°C, I_R*100, V_{DD}=1.8V, $\tau_{rise}=\tau_{fall}$=100ps, W_p/W_n=32/16, Per=1ns, 50% duty cycle)



(a)



(b)

Figure 3.5 Heavy loading effect on hysteretic delays.
Hysteretic delays for large output node load (replaced static load of Fig. 3.3 with a large load (e.g., long metal line). (L_{eff}=145nm, V_t=0.4V, T=27°C, I_R*100, V_{DD}=1.8V, $\tau_{rise}=\tau_{fall}$=100ps, W_p/W_n=32/16, Per=1ns, 50% duty cycle)

$$I_n(t) = \frac{dQ_{Dn}}{dt} + \left(I_p(t) + \frac{dQ_{Dp}}{dt}\right) + C_L \frac{dV_{out}}{dt} \qquad (3.2)$$

where $I_n(t)$ is the drive current of the nMOSFET. Since the capacitive load is very large, the transient voltage across the load decreases slowly making the output node voltage ($V_{out}(t)$) maintain its pre-switch value for a longer time prior to its decrease. This constrains the build-up of V_{DS} across the load device during the tranient and thus suppresses the influence of the increased load current (e.g., for the pMOSFET: $I_p(t)+dQ_{Dp}/dt$) due to the *dynamic-loading* effect, sufficiently such that the non-monotonic behavior of Figs. 3.2 and 3.3 is not present.

3.5 Integrity of the Dynamic Steady-State Results

At the dynamic steady-state (DSS) condition of (3.1) for a CMOS inverter, the pull-up ($\tau_{pu\text{-}f}$, $\tau_{pu\text{-}s}$) and pull-down ($\tau_{pd\text{-}f}$, $\tau_{pd\text{-}s}$) fundamental delays must be equal (to within a given tolerance), as in Figs. 3.3-3.5. If the delays do not merge at the DSS condition, the predicted results may be unreliable, due to numerical instabilities such as truncation error or charge non-conservation [Kun95]. Empirical (especially capacitance-based) compact models are more vulnerable to these instabilities, and the inherent complex dynamics of PD/SOI technologies necessitate the use a physical charge-based model such as the UFSOI compact device model [Fos99].

3.6 Does Controlled Off-State Current Imply Hysteresis Control?

When the I_{off}-controlling techniques of Chapter 2, i.e., increasing the recombination (and thermal generation) rate by 100x and temperature from 25°C to

85°C, are checked for hysteresis control, the non-monotonic behavior is eliminated, but $\tau_{OC\text{-}s}$, $\tau_{pd\text{-}s}$, and $\tau_{pu\text{-}s}$ all show, in Fig. 3.6, worsened hysteresis. These delays, along with τ_{RO}, show a shift from decreasing delays to increasing delays, due to the discharging or *dynamic weakening of the active device*. The hysteresis of the "fast" delays ($\tau_{OC\text{-}f}$, $\tau_{pd\text{-}f}$, $\tau_{pu\text{-}f}$) remains about the same. All of the delays are longer because of the higher temperature (reduced mobility), but the initial "fast" delays have been lengthened the most because of the suppression of V_{BS} in both devices at the DC condition (t=0) due to the higher recombination rates. In time, the "fast" delays shorten due mainly to the discharging of the load device. This *dynamic weakening of the load device* is due to the net recombination that occurs each cycle, in contrast to the net generation (via impact ionization) each cycle reflected by Fig. 3.3. For $\tau_{pu\text{-}f}$, V_{BS} of the nMOSFET load becomes increasingly negative in time. For $\tau_{pd\text{-}f}$, V_{BS} of the pMOSFET load becomes increasingly positive in time. These results suggest that an "intermediate" design point could be achieved which is *void of hysteresis* for τ_{RO} and the "slow" delays.

3.7 Correlation to Measurements

Recent measured data [Ass96], [Hou98], though limited to only the average delays, show dynamic steady-state delays that increase, relative to the initial delay, as the input pulse period decreases (increasing frequency). Contrarily, simulations [Gau95], [Wei98] of such hysteresis typically predict that the steady-state delays decrease as indicated in Fig. 3.3. This discrepancy in hysteretic trends can be explained via measurement uncertainties (voltage supply collapse, self-

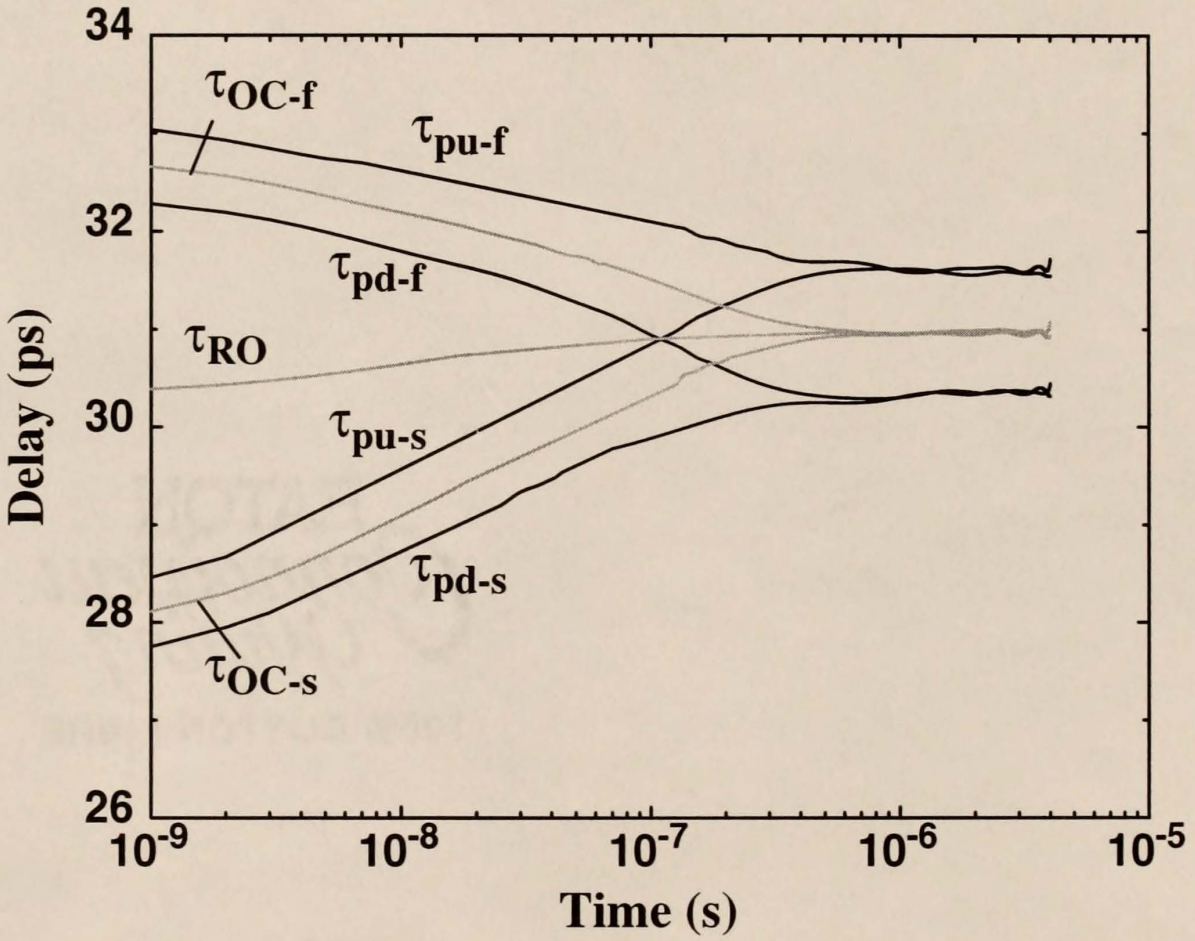


Figure 3.6 Increased T and I_R effects on hysteretic delays.

Hysteretic delays for higher recombination rates and elevated temperature, relative to those in Fig. 3.3. (L_{eff}=145nm, V_t=0.4V, T=85C, I_R*100, V_{DD}=1.8V, $\tau_{rise}=\tau_{fall}$=100ps, W_p/W_n=32/16, C_L=85fF, Per=1ns, 50% duty cycle)

heating) and device technology differences, as suggested and Fig. 3.6 and by Fig. 3.7. The FB dynamics which underlie the hysteresis in circuits can be influenced by the ratio of the gate-to-body capacitance (C_{GB}) to the drain-to-body capacitance (C_{DB}) [Pel97], [Kri98] and by the unbalanced body charging rates of the nMOS and pMOS devices, as exemplified in Fig. 3.7 where predicted $\tau_{OC\text{-}f}$ for thinner t_{SOI} is contrasted to that for t_{SOI}=150nm as in Fig. 3.3. The results show that early in time the smaller C_{DB} ($\propto t_{SOI}$) enables more gate-to-body capacitive coupling, enhancing the current-overshoot effect, which significantly shortens $\tau_{OC\text{-}f}$. Later in time the *dynamic strengthening of the load device* lengthens $\tau_{OC\text{-}f}$. These results demonstrate that the hysteretic delay can be made to either increase or decrease in time by altering the SOI film thickness (changing C_{DB}), and by changing C_{GB} (e.g., varying L) too.

3.8 Scaling

As the voltage supply is scaled from 1.8V to 1.2V, the worst-case hysteretic delay variation increases significantly from 9 to 17%, as shown in Fig. 3.8. When the device technology (t_{ox}, t_{SOI}, etc.) is also scaled to L_{eff}=70nm at 1.2V in accord with the SIA ITRS [SIA99], as detailed in Chapter 4, a delay hysteresis of 12% is predicted, as shown in Fig. 3.9. The increased C_{GB}/C_{DB} ratio of the scaled technology helps to suppress the hysteresis somewhat. These results suggest that as PD/SOI technologies are scaled, hysteresis will tend to worsen, mainly because ΔV_t (the dynamic threshold due to hysteresis) cannot be scaled while V_{DD} is reduced, and hence will become more significant in the delay equation: $\tau = 1/[(V_{DD}/2) - |V_T|]^2$. Also, a slower slew rate (rise/fall time) enhances the associated hysteresis, due to

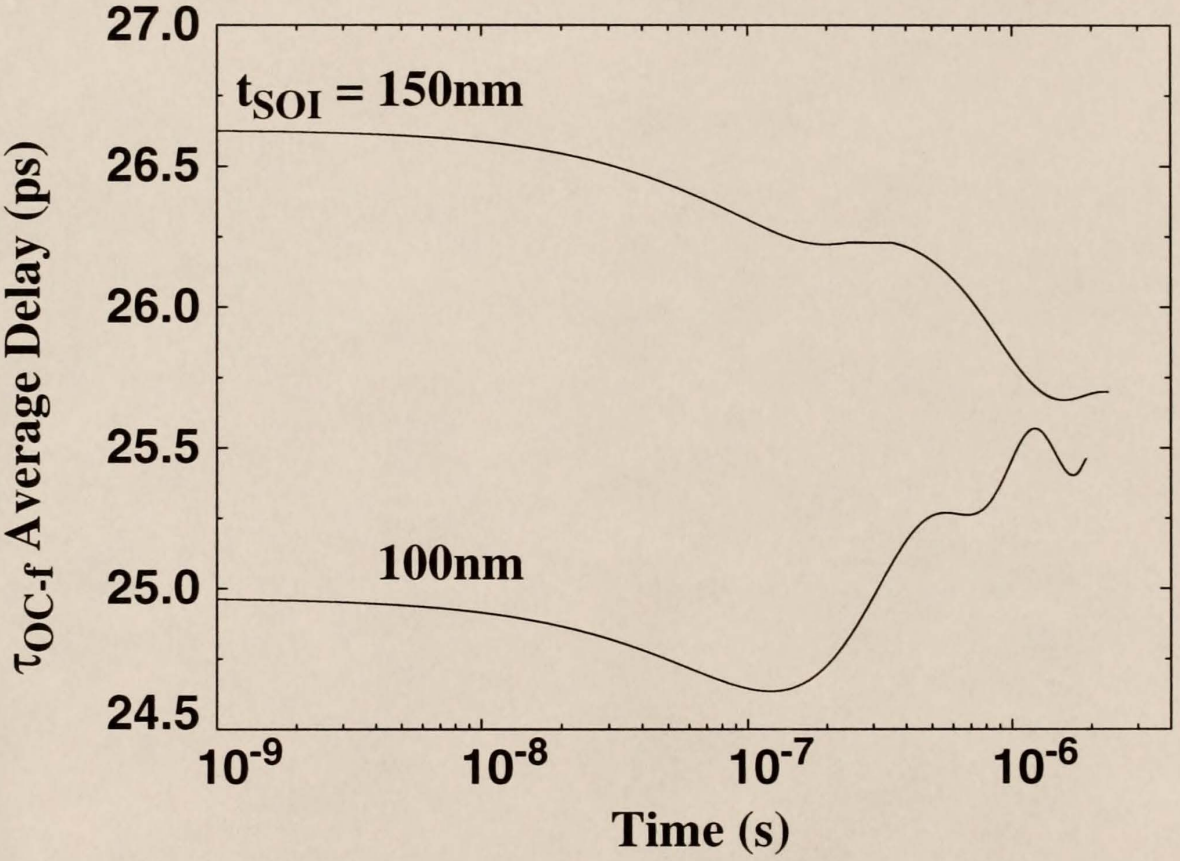


Figure 3.7 Sensitivity of film thickness on hysteretic delay.
Modified fast open-chain delay for a thinner SOI film thickness, relative to that in Fig. 3.3. (L_{eff}=145nm, V_t=0.4V, T=27C, V_{DD}=1.8V, τ_{rise}=τ_{fall}=100ps, W_p/W_n=32/16, C_L=85fF, Per=1ns, 50% duty cycle)

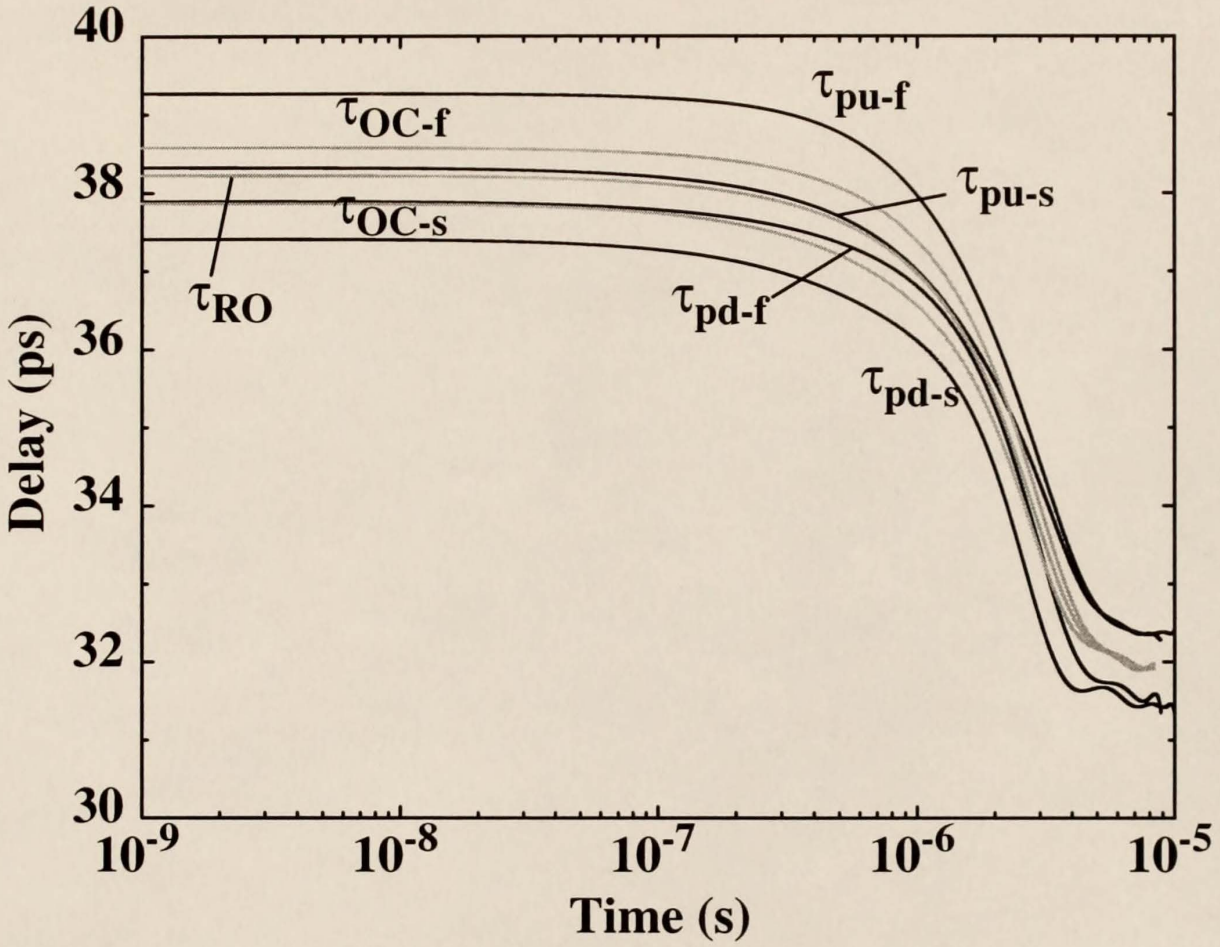


Figure 3.8 Effect of lower V_{DD} on hysteretic delays.

Hysteretic delays for reduced supply voltage, relative to those in Fig. 3.3. (L_{eff}=145nm, V_t=0.4V, T=27°C, V_{DD}=1.2V, $\tau_{rise}=\tau_{fall}$=100ps, W_p/W_n=32/16, C_L=85fF, Per=1ns, 50% duty cycle)

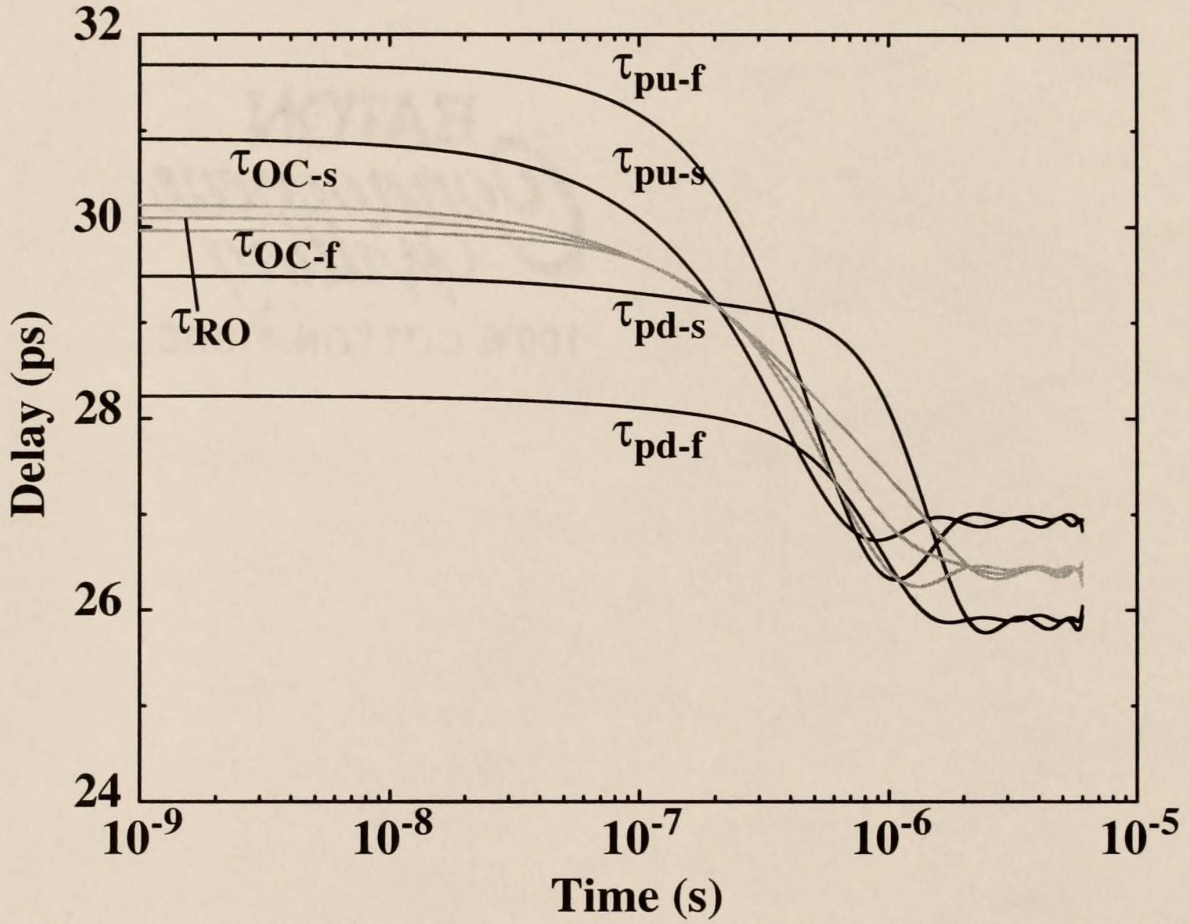


Figure 3.9 Scaled technology effects on the hysteretic delays.
Hysteretic delays for scaled technology, relative to those in Fig. 3.3. (L_{eff}=70nm, t_{ox}=2.5nm, t_{SOI}=100nm, V_t=0.4V, T=27°C, V_{DD}=1.2V, $\tau_{rise}=\tau_{fall}$=100ps, W_p/W_n=32/16, C_L=85fF, Per=1ns, 50% duty cycle)

increased impact-ionization charging of the body during the lenghtened transition period when both nMOS and pMOS devices conduct current [Pel99a].

3.9 Control of Hysteresis: Asymmetric SOI CMOS

Results of applying hysteresis-controlling techniques to the technology of Fig. 3.3 are shown in Fig. 3.10. By thinning t_{SOI} from 150nm to 100nm (case "A") as demonstrated in Fig. 3.7, in both nMOS and pMOS device structures, the hysteresis of the average delay $\tau_{OC\text{-}f}$ is made to increase in time, suggesting that a *null-hysteresis* design can be achieved for $\tau_{OC\text{-}f}$. Because the adjustments in t_{SOI} are typically limited (PD neutral region design, S/D resistance, and thickness control), to suppress the hysteresis associated with $\tau_{OC\text{-}f}$, we propose an *asymmetric SOI CMOS design* concept that adjusts key device/structure parameters of the pMOSFET while maintaining the original nMOSFET design (or vice versa). This allows a decoupling of the device structures so that the nMOSFET can be designed to fully exploit the benefits of SOI, while the pMOSFET can be utilized to control hysteresis. This is demonstrated by cases "B" and "C" in Fig. 3.10. By additionally increasing the junction recombination current (100x) of the pMOSFET, a virtual *null-hysteresis* for $\tau_{OC\text{-}f}$ is achieved, as shown by case "B." By additionally increasing the halo and/or retrograde (N_{BH}) doping density (5x) of the pMOSFET, which decreases the C_{GB}/C_{DB} ratio and reduces the current overshoot caused by the gate-body coupling, the $\tau_{OC\text{-}f}$ delay is now shown to decrease in time, as shown by case "C." These asymmetric device adjustments demonstrate that the $\tau_{OC\text{-}f}$ delay can be designed to either increase, decrease, or remain the same in time. However, the $\tau_{OC\text{-}s}$ delays for

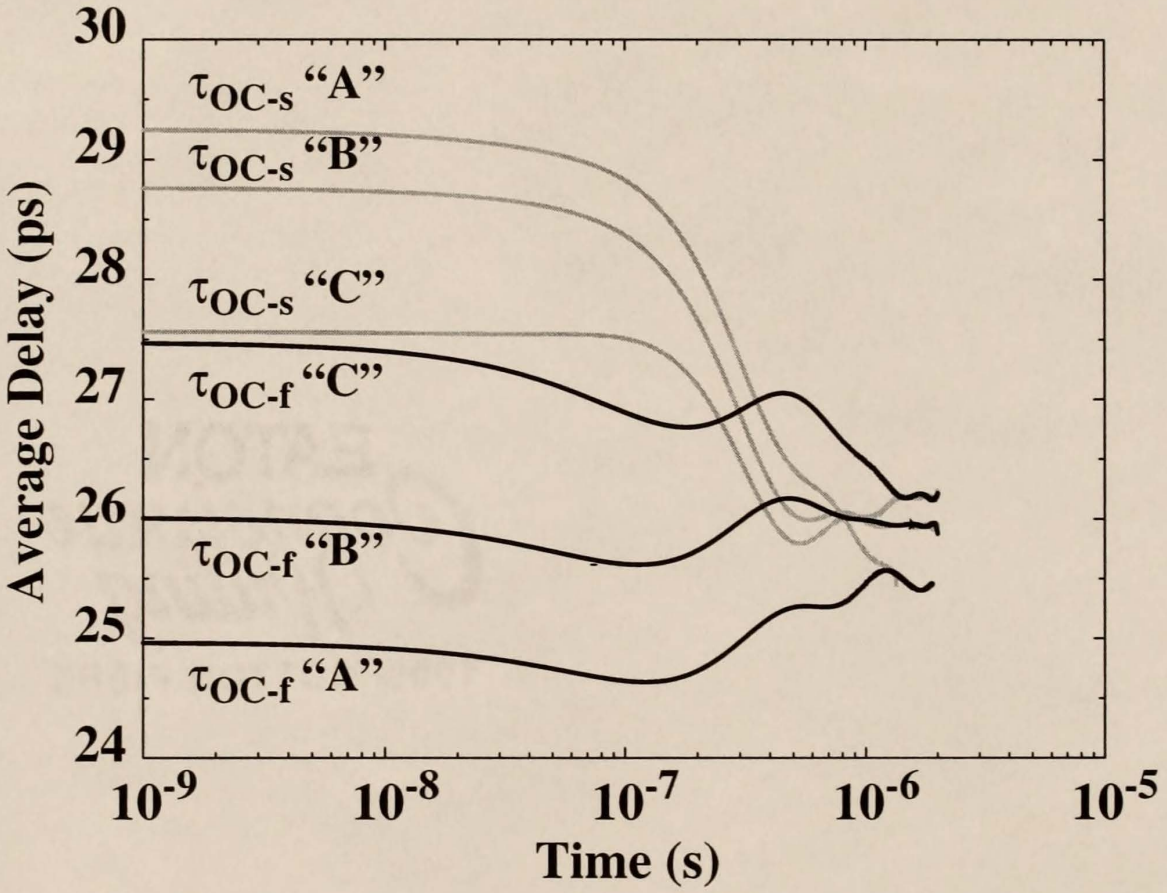
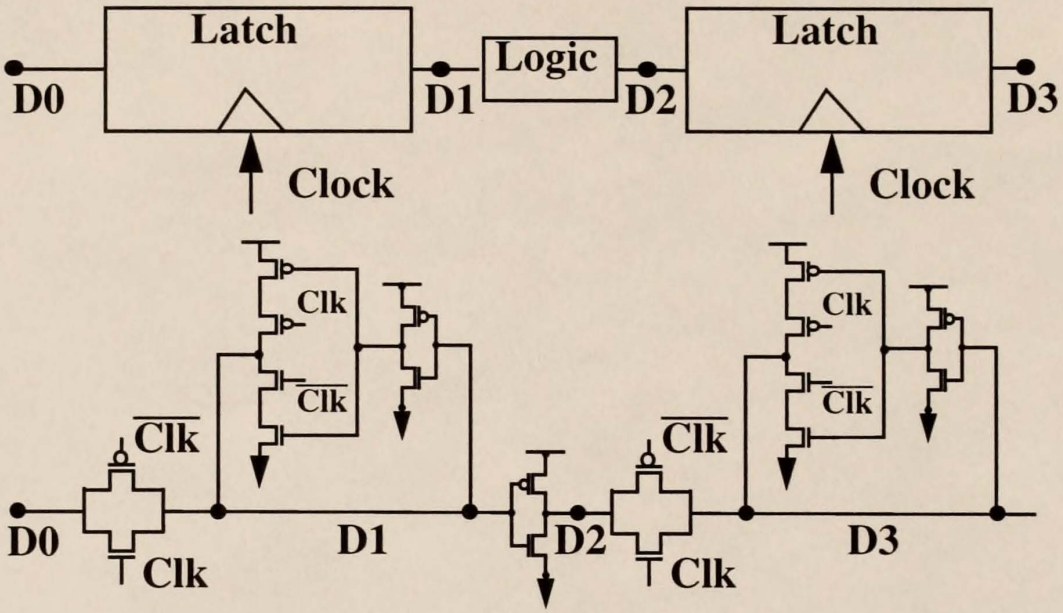


Figure 3.10 Techniques to control hysteresis.
Controlled hysteretic delays, relative to those in Fig. 3.3; SOI film thickness ("A", "B", and "C"), recombination rates ("B" and "C"), and halo doping density ("C") have been modified. (L_{eff}=145nm, t_{ox}=4.5nm, t_{SOI}=100nm, V_t=0.4V, T=27°C, V_{DD}=1.8V, $\tau_{rise}=\tau_{fall}$=100ps, W_p/W_n=32/16, C_L=85fF, Per=1ns, 50% duty cycle)

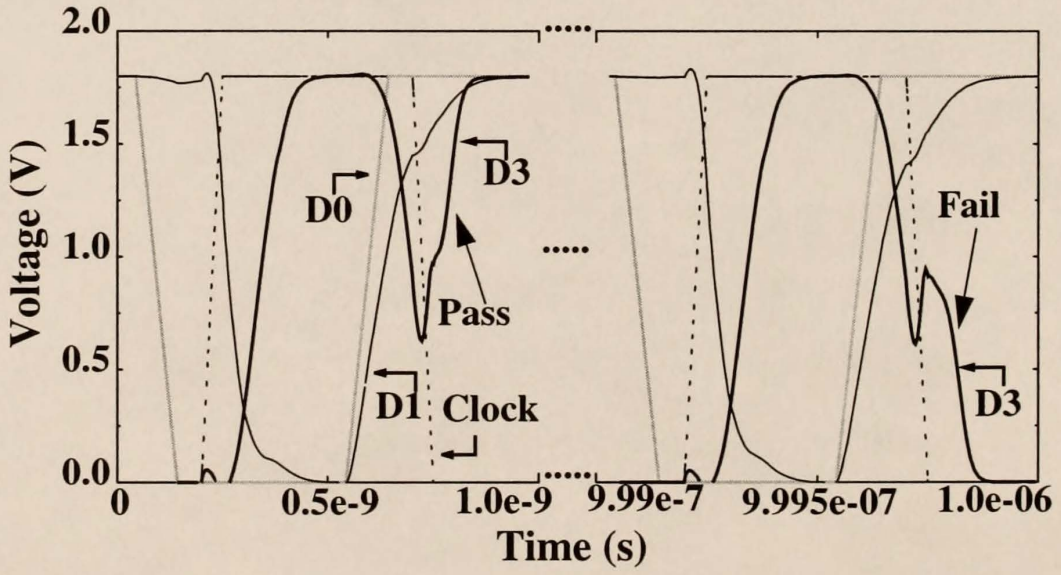
cases "A" and "B" show a marked increase in hysteresis, which may be problematic in some circuit designs. By utilizing case "C," a closer balance of hysteresis is achieved for the $\tau_{OC\text{-}f}$ and $\tau_{OC\text{-}s}$ delays. The hysteresis for both delays of case "C" is less than 5%.

3.10 Circuit Application

The problematic nature of hysteresis is exemplified via simulation of a microprocessor circuit in Fig. 3.11 which depicts an early-mode (or race) feedthrough timing fail mechanism. The circuit is a latch-based pipelined clocked system, which has input and output latches (captures the data at each stage at the end of each clock cycle) separated by a logic block. When data D0 of Fig. 3.11(a) goes to a high ("1") level, with the clock at a high level, the data will propagate through the first latch (which includes a complementary pass gate) and subsequently through the logic gates within one clock cycle. A timing issue arises if the setup time, minimized for chip-performance reasons, is too short and allows the data from the first cycle to propagate through to the second latch within one clock cycle. If the delay of the first latch and logic gates decreases in time (hysteresis), it will compromise the setup timing design and lead to a feedthrough fail, as shown in the UFSOI/SPICE simulation results of Fig. 3.11(b). During the first cycle (with no hysteresis), the inverted signal of data D1 (D2) does not propagate through to the second latch, as indicated by the high logic level of D3 at time equal to ~1ns, and thus passes the timing condition. However, subsequent to many cycles at time equal to ~1μs, data D3 is shown to change (flip) its logic state to a low level, since the



(a)



(b)

Figure 3.11 FB PD/SOI CMOS microprocessor simulation.
(a) Latch-based pipelined clocked system. (b) Dependent on the hysteresis, the second (invalid-data) transition of the data signal D0 could be propagated (fail) or not (pass) through the second latch before the clock closes; an early-mode (or race) feedthrough fail is predicted. (L_{eff}=145nm, T=27°C, V_{DD}=1.8V; Logic: W_p/W_n= 4/2.4; Pass Gate: W_p/W_n= 0.4/0.4)

second latch did not close before the next data signal approached. This timing failure is due to the delay speedup from the associated hysteresis of the prior latch and logic block.

To eliminate this fail mechanism, the setup time should include the worst-case hysteresis expected, or a technology adjustment could be employed utilizing the insight gained from the proposed *fundamental delay-based methodology* and the *asymmetric SOI CMOS design* concept. The pertinent hysteretic delay for the given application is $\tau_{pd\text{-}s}$ of Fig. 3.3, which decreases by 7% at 1μs because of nMOSFET charging.

By employing an increased I_R for only the nMOSFET, simulations of Fig. 3.12 show that the hysteresis is effectively suppressed and the noted feedthrough fail is eliminated without significant loss of performance. Alternatively, a decreased I_R for the pMOSFET would control this hysteresis effect as well. Fig. 3.12 exemplifies the effects of increasing I_R only in the nMOSFET and decreasing I_R only in the pMOSFET on the $\tau_{pd\text{-}s}$ of Fig. 3.3. The results show a successful suppression of $\Delta\tau(\tau_{nom} - \tau_{min})$ by either asymmetrical design technique. The weakened nMOSFET (increased I_{Rn} by 10x) design reduced the worst-case $\Delta\tau$ from 9% for the nominal design to 5%. If I_{Rn} is increased by 100x, $\Delta\tau$ decreased further to only 2%. Alternatively, if the pMOSFET is strengthened by reducing I_{Rp}, the worst-case $\Delta\tau$ is also reduced to only 5%. Thus, both of these asymmetric design techniques will suppress the hysteresis of the $\tau_{pd\text{-}s}$ delay and restore the pass condition for the microprocessor latch circuit application. Other asymmetric designs, e.g., those suggested by Fig. 3.10, could also be considered in this application. If the transition

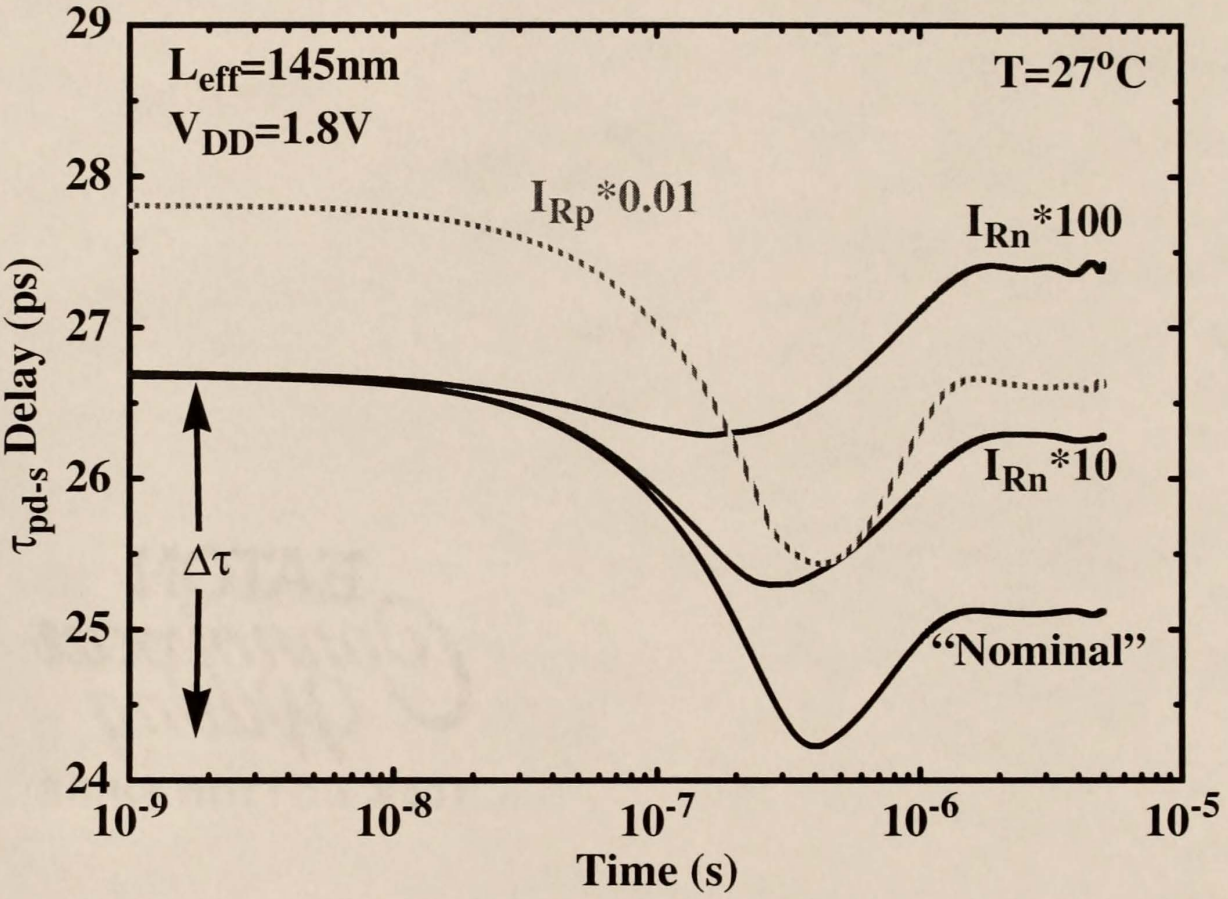


Figure 3.12 Suppressing hysteresis to prevent microprocessor fails. Modified floating-body PD/SOI CMOS fundamental τ_{pd-s} delay for increased nMOSFET recombination currents (I_{Rn}) and decreased pMOSFET I_{Rp} current, relative to the nominal τ_{pd-s} of Fig. 3.3 depicting the suppression of $\Delta\tau$ by employing the *asymmetric SOI CMOS design concept*. (L_{eff}=145nm, V_t=0.4V, T=27°C, V_{DD}=1.8V, τ_{rise}=τ_{fall}=100ps, W_p/W_n=32/16, C_L=85fF, Per=1ns, 50% duty cycle)

of data D0 is flipped, the pertinent hysteretic delay would be $\tau_{pu\text{-}s}$, and its associated feedthrough fail could also be resolved by these asymmetric designs.

3.11 Summary

The fundamental delays of a PD/SOI CMOS inverter have been defined along with a new methodology to properly analyze hysteresis. Our analysis revealed the possibility of a non-monotonic hysteretic delay caused by a dynamic loading effect that is due to the imbalance of the impact-ionization rates of the electrons and holes in the nMOS and pMOS devices. Hysteresis can be suppressed via the same controlling techniques for I_{off}, but not generally. An increasing or decreasing hysteretic delay was demonstrated by physically adjusting the C_{GB}/C_{DB} ratio (resolving an open discrepancy between simulations and measurements). Hysteresis will tend to worsen as the technology is scaled, due mainly to the non-scaling of V_t. However, a new asymmetric SOI CMOS design concept was proposed to generally suppress and control hysteresis per specific applications within a given technology, while retaining the benefits of SOI.

CHAPTER 4
PERFORMANCE ADVANTAGE OF PD/SOI WITH FLOATING BODIES

4.1 Introduction

The floating-body (FB) partially depleted (PD) silicon-on-insulator (SOI) CMOS technology potentially offers superior performance/power relative to its bulk-Si counterpart. The PD/SOI advantage is due in part to FB effects [Kri98], which, however, can lead to device and circuit instabilities, especially in dynamic logic and memory circuits as described in Chapter 3. These problematic FB effects are manifested in both the static (e.g., kink effect, single-transistor latch, premature drain-source breakdown) [Col97], [Cri95] and dynamic (e.g., transient threshold voltages, capacitive coupling, drain current overshoot/undershoot, hysteretic memory effects, transient parasitic bipolar leakage effects) [Suh94], [Gau95], [Pel96], [Pel97], [Gau97], [Wei98] operation of the devices and circuits. (Fully depleted SOI CMOS devices tend to suppress the FB effects, but their scalability is limited by pragmatic, finite Si-film and buried-oxide thicknesses [Yeh95].)

Recent demonstrations of SOI microprocessors [Buc20]] reveal that the detrimental FB effects of a PD/SOI technology can be suppressed enough via device and circuit modifications [Can99], [All99] to achieve a viable ULSI high-performance processor technology. However, it has recently been suggested that the 10-30% improvement in performance over the bulk-Si counterpart will diminish as

the technologies are scaled to 150nm (effective channel length) [Cha97] and below [Mis20].

The aim of this chapter, based on physical device/circuit simulations, is to quantify the performance benefits of the FB PD/SOI CMOS technology over its bulk-Si counterpart using a newly developed unified UFSOI model capability, provide insight into the physical mechanisms underlying the benefits, and to assess these benefits as the technology is scaled, noting the need for device/circuit design optimization to control and exploit the FB effects. The study begins with simulations of a static CMOS-inverter ring oscillator from the contemporary 145nm (effective channel length), 1.8V FB PD/SOI technology of Chapter 2, the speed of which is predicted to be more than 25% faster than that of its bulk-Si counterpart. This advantage is shown to be due mainly to the dynamic capacitive coupling of the floating body to the gate and drain, which often has been ignored (relative to the kink effect) in previous explanations of the SOI advantage. However, in accord with the suggestion in [Cha97], this coupling is shown to diminish as the technology is scaled ($L_{eff} \rightarrow 70$nm, $V_{DD} \rightarrow 1.2$V), mainly because of the reduced power-supply voltage. Additional simulations reveal though that this potential loss of the SOI advantage can be mitigated via design optimization (increased recombination current) as well as operation at typically elevated ambient temperatures. Moreover, the suppression of the body-bias effects in stacked-transistor (e.g., NAND) circuits is shown, in accord with [All99], to provide a significant advantage for SOI technologies over equivalent bulk-Si technologies, even as the technology is scaled, providing an additional 5-25% performance benefit.

4.2 Unified Model for PD/SOI and Bulk-Si MOSFETs

In order to properly evaluate and benchmark both FB SOI and bulk-Si technologies at the same technology node, the UFSOI model formalism for PD/SOI [Fos99] was extended creating a new unified capability (UFSOI/PD-B) to enable a bulk-Si counterpart structure to be simulated with exactly the same device design assumptions as the PD/SOI technology. This new unified capability allows direct performance comparisons of the two technologies without ambiguities in device design and structure, and enables reliable benchmarking of scaled technologies projected in the SIA International Technology Roadmap for Semiconductors (ITRS) [SIA99]. This unique feature is facilitated in UFSOI by its process-based physical model formalism, e.g., a MOS theory-based source/drain-substrate capacitance that simplifies to source/drain-body depletion capacitance when the buried oxide is theoretically thinned to ~0 and the back-gate/substrate and body terminals are merged.

The new bulk-Si feature is activated by changing a UFSOI/PD-B model flag (**NFDMOD**=2) and updating the substrate doping density (**NSUB**) to reflect an equivalent well doping. To obtain the correct junction recombination current for the bulk-Si counterpart technology, which must include the areal as well as the sidewall components, the following adjustment to the model parameter **JRO** [Fos99] can be made:

$$\mathbf{JRO_{bulk-Si}} = \mathbf{JRO_{SOI}}\left(1 + \frac{A_j}{t_{SOI} \times W}\right) \tag{4.1}$$

where A_j is the source/drain areal junction area, t_{SOI} is the SOI film thickness, and W is the width of the MOSFET.

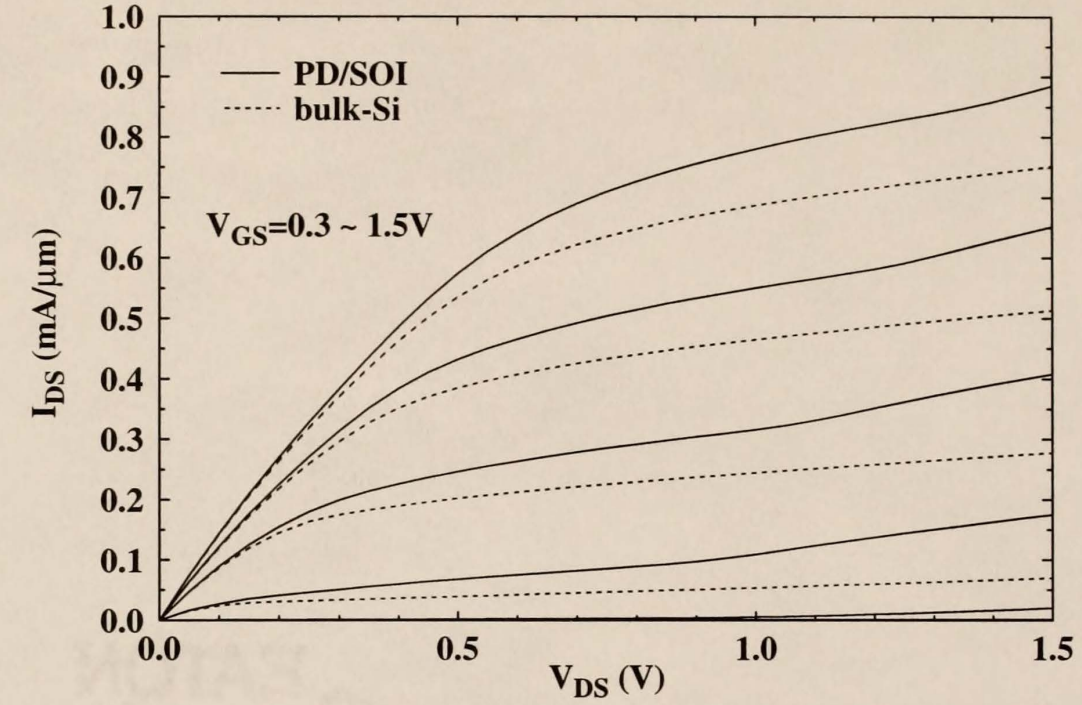
The results of this new unified model capability are exemplified in Fig. 4.1 where the predicted I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of an L_{eff}=70nm FB PD/SOI nMOSFET and its bulk-Si counterpart (with NFDMOD=2, NSUB=N_{WELL}) are shown. The discernible FB effects, e.g., the strong-inversion and subthreshold kink effects, the enhanced I_{on}, the increased I_{off}, the lower V_t(sat), and the degraded drain/output conductance are all evident.

In UFSOI/PD-B, the source/drain-substrate capacitance is characterized by modeling the MOS substrate depletion charge under the source/drain region [Yeh95]. In essence, the capacitance (per source/drain area) is a series combination of the buried oxide capacitance (C_{BOX}) and the depletion-layer capacitance of the substrate (C_{sub}):

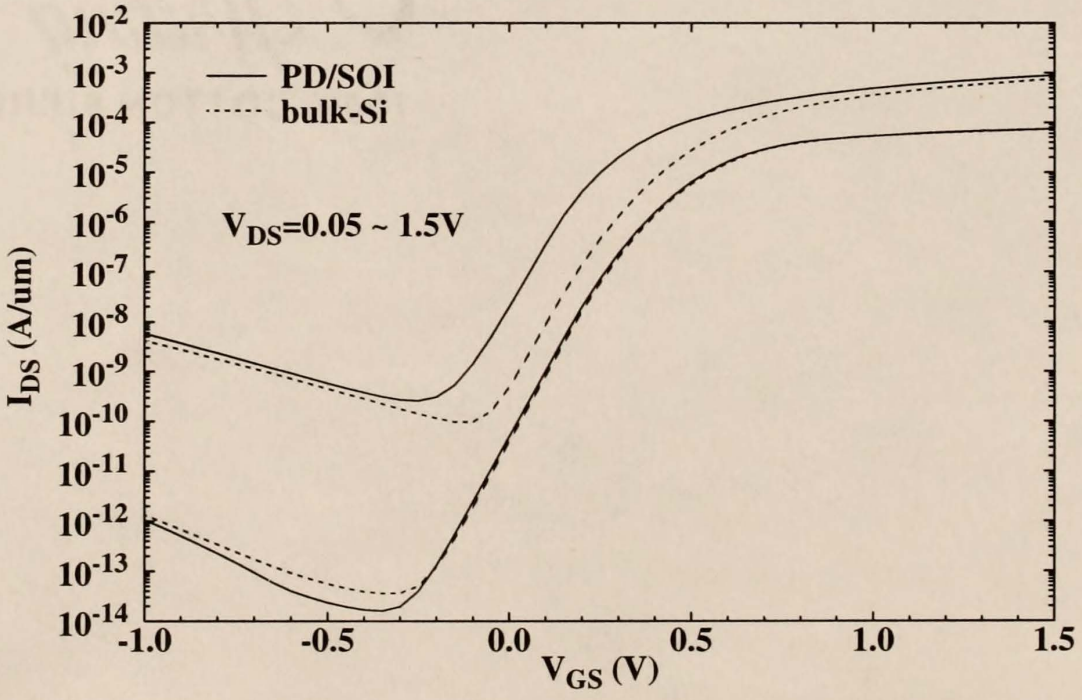
$$\frac{1}{C_{S/D}} = \frac{1}{C_{sub}} + \frac{1}{C_{BOX}} \tag{4.2}$$

where $C_{BOX}=\varepsilon_{ox}/t_{BOX}$ and $C_{sub}=\varepsilon_s/W_{depl}$. The depletion width ($W_{depl}$) in the substrate is a function of the surface potential ($\psi_{s\text{-}sub}$) below the BOX, under the source/drain regions, and is modeled by the depletion approximation dependent on the source/drain-to-substrate voltage ($V_{S/D\text{-}sub}$). For $t_{BOX} \rightarrow \sim 0$, $C_{BOX} >> C_{sub}$, and

$$\frac{1}{C_{S/D}} \rightarrow \frac{1}{C_{sub}} \approx \frac{1}{C_{j-areal}} \tag{4.3}$$



(a)



(b)

Figure 4.1 PD/SOI and bulk-Si I_{DS}-V_{DS}, I_{DS}-V_{GS} predicted by UFSOI/PD-B. The predicted I-V characteristics for a L_{eff}=70nm nMOSFET at 27°C exemplifying the utility of the new unified UFSOI/PD-B model.

where Cj-areal is the areal component of the source/drain junction capacitance (per source/drain area), now modeled physically when the substrate doping density is set to the well doping density.

4.3 Performance Benefits of Contemporary SOI

4.3.1 Modeling and DC Characteristics

Device and circuit simulations are done using the unified process-based UFSOI/PD-B MOSFET model. Because the model parameters relate directly to device structure and physics, the simulation results are representative and predictive of important trends. UFSOI-predicted subthreshold I_{DS}-V_{GS} device characteristics, at room temperature (T=27°C), of the minimum-L_{eff} (110nm) condition for the contemporary V_{DD}=1.8V, L_{eff}=145nm PD/SOI technology of Chapters 2 and 3 are shown in Fig. 4.2. The gate oxide thickness (t_{ox}) is 4.5nm; $V_{t(linear)}$=0.4V@ I_{DS}=100nA*W/L; the buried oxide thickness (t_{BOX}) is 400nm; and the Si-film thickness (t_{SOI}) is 150nm. The bulk-Si counterpart technology, also portrayed in Fig. 4.2, is defined by identical processing as the SOI technology with its well doping at $10^{17}cm^{-3}$. Superimposed in Fig. 4.2 too are the body-tied-to-source (BTS) results for the FB PD/SOI devices, which indicate the minimum off-state (V_{GS}=0V) leakage current (I_{off}) that can be achieved if there is no enhancement of I_{DS} due to the DC floating-body (subthreshold-kink) effect. Also in Fig. 4.2 are the characteristics of the FB PD/SOI devices with threshold voltages (V_t) increased via channel-doping adjustments to achieve an I_{off} equal to that of the BTS/SOI and bulk-Si devices [Cha97]. The V_{tn} for the nMOSFET and V_{tp} for the pMOSFET were increased by

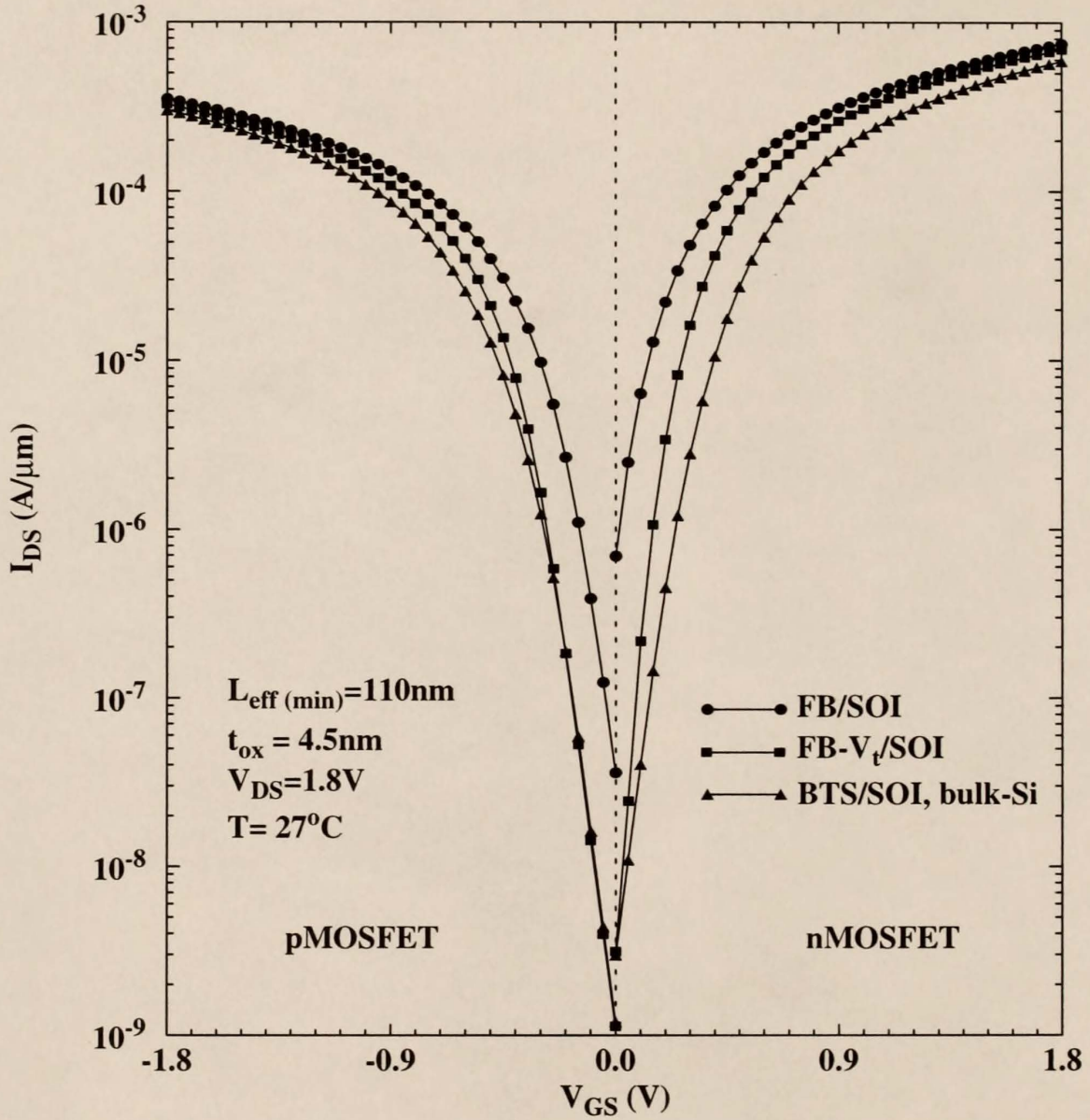


Figure 4.2 Predicted I_{DS}-V_{GS} for SOI and bulk-Si 145nm technologies. UFSOI-predicted subthreshold current-voltage characteristics of the minimum devices (L_{eff}=110nm) for 145nm L_{eff} SOI nMOSFET and pMOSFET technologies including: FB/SOI, FB-V_t/SOI, BTS/SOI(bulk-si equivalent DC characteristics); t_{ox}=4.5nm, t_{soi}=150nm, $V_{t(linear)}$=0.4V@I_{DS}=100nA*W/L, T=27°C.

143mV and 141mV, respectively. The drive currents (I_{on}) at V_{DD} = 1.8V (without self-heating) for the nMOSFETs/pMOSFETs are 0.74/0.35 mA/μm for FB-SOI, 0.69/0.325 mA/μm for FB-V_t/SOI, and 0.59/0.3 mA/μm for BTS-SOI/bulk-Si. Table 4.1 summarizes I_{off} and I_{on} for the minimum-L_{eff} devices of each technology.

Table 4.1 Comparison of I_{on} and I_{off} for the nominal L_{eff}=145nm MOSFET devices at the minimum L_{eff} condition

L_{eff}=110nm (min) V_{DD}=1.8V, T=27°C	FB/SOI		FB-V_t/SOI		BTS/SOI		bulk-Si	
	nMOS	pMOS	nMOS	pMOS	nMOS	pMOS	nMOS	pMOS
I_{on} (mA/μm)	0.74	0.35	0.69	0.325	0.59	0.3	0.59	0.3
I_{off} (nA/μm)	690	36	3	1	3	1	3	1

4.3.2 Performance Comparison

With reference to the hysteretic delay-analysis methodology described in Chapter 3, the predicted ring-oscillator (fanout=1) propagation delay (τ_{RO}) at T=27°C for the four technologies described above are shown, varying in time, in Fig. 4.2. The device layouts assume a 6λ-based ground rule for the source/drain contact lengths, with λ equal to L_{gate}/2.0 (L_{gate}=195nm). UFSOI simulations predict the performance benefit to the dynamic steady-state τ_{RO} (τ^{ss}_{RO}) to be 29% for the FB/SOI technology over bulk-Si counterpart. However, the FB/SOI technology has an excessive I_{off}, as indicated in Table 4.1, and requires I_{off}-controlling techniques as suggested in Chapter 2 and [Fos98], [Ohn98], [Wei93], [Yos97], [Che97], [Hor96], [Che96] to maintain reasonable chip power and SRAM functionality. Alternatively, increasing V_t of the FB/SOI technology (which yields FB-V_t/SOI) to get I_{off} equal to

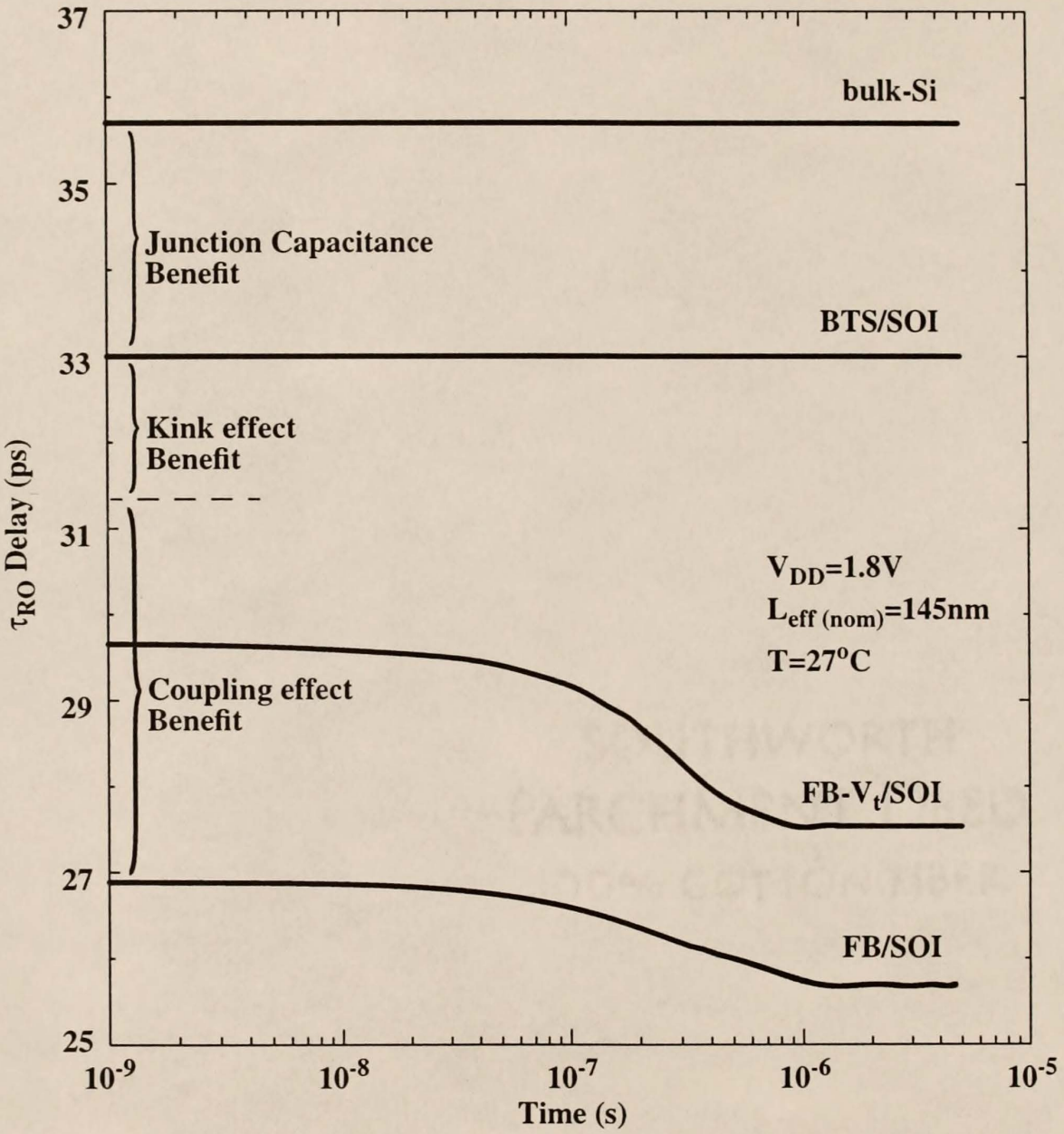


Figure 4.3 Predicted delay for SOI and bulk-Si 145nm technologies.
UFSOI-predicted τ_{RO} propagation delay for the 145nm L_{eff} technologies (L_{gate}=195nm, t_{ox}=4.5nm, $V_{t(linear)}$=0.4V@I_{DS}=100nA*W/L, T=27°C, V_{DD}= 1.8V, τ_{rise}/τ_{fall}=100ps, Wp/Wn=32/16, $L_{S/D}$=6λ G/R.)

that of bulk-Si still yields a 23% τ^{ss}_{RO} performance benefit over the bulk-Si technology. The predicted τ^{ss}_{RO} delays and accompanying history-dependent propagation-delay (hysteresis) results are summarized for the above technologies in Table 4.2.

Table 4.2 Predicted steady-state delay and hysteresis results for the four L_{eff}=145nm technologies.

L_{eff}=145nm (nom) V_{DD}=1.8V, T=27°C	FB/SOI	FB-V_t/SOI	BTS/SOI	bulk-Si
τ^{ss}_{RO} (ps)	25.5	27.5	33	35.7
SOI Benefit over bulk-Si	28.6%	23%	7.6%	--%
τ_{RO} Hysteresis ($\Delta\tau_{RO}/\tau^{i}_{RO}$)	4.5%	7.1%	--%	--%

4.3.3 Hysteresis Effect

Hysteresis is reflected by the relative change of a specific delay as a function of time from its initial delay (τ^{i}_{D}) to its steady-state delay (τ^{ss}_{D}), computed by $(\tau^{i}_{D}-\tau^{ss}_{D})/\tau^{i}_{D}$. The hysteresis of τ_{RO} for the FB-V_t/SOI technology increases to 7.1% from 4.5% for the nominal FB/SOI technology as noted in Table 4.2 and as can be seen in Fig. 4.3. This increase reflects the wider variation of body voltage over time, ΔV_{BS} {initial V_{BS} (V^{i}_{BS}) relative to the steady-state V_{BS} (V^{ss}_{BS})}.

To gain additional insight regarding the impact of the increased V_t of the FB-V_t/SOI technology, Fig. 4.4 shows the $V_{BS}(t)$ during the first switching cycle for the nMOSFET and pMOSFET devices of an inverter circuit. Figs. 4.4(a) and (b) reveal the $V_{BS}(t)$ behavior for the low-to-high (LH) input signal case, while Figs. 4.4(c) and (d) depict the $V_{BS}(t)$ behavior for the high-to-low (HL) input signal case.

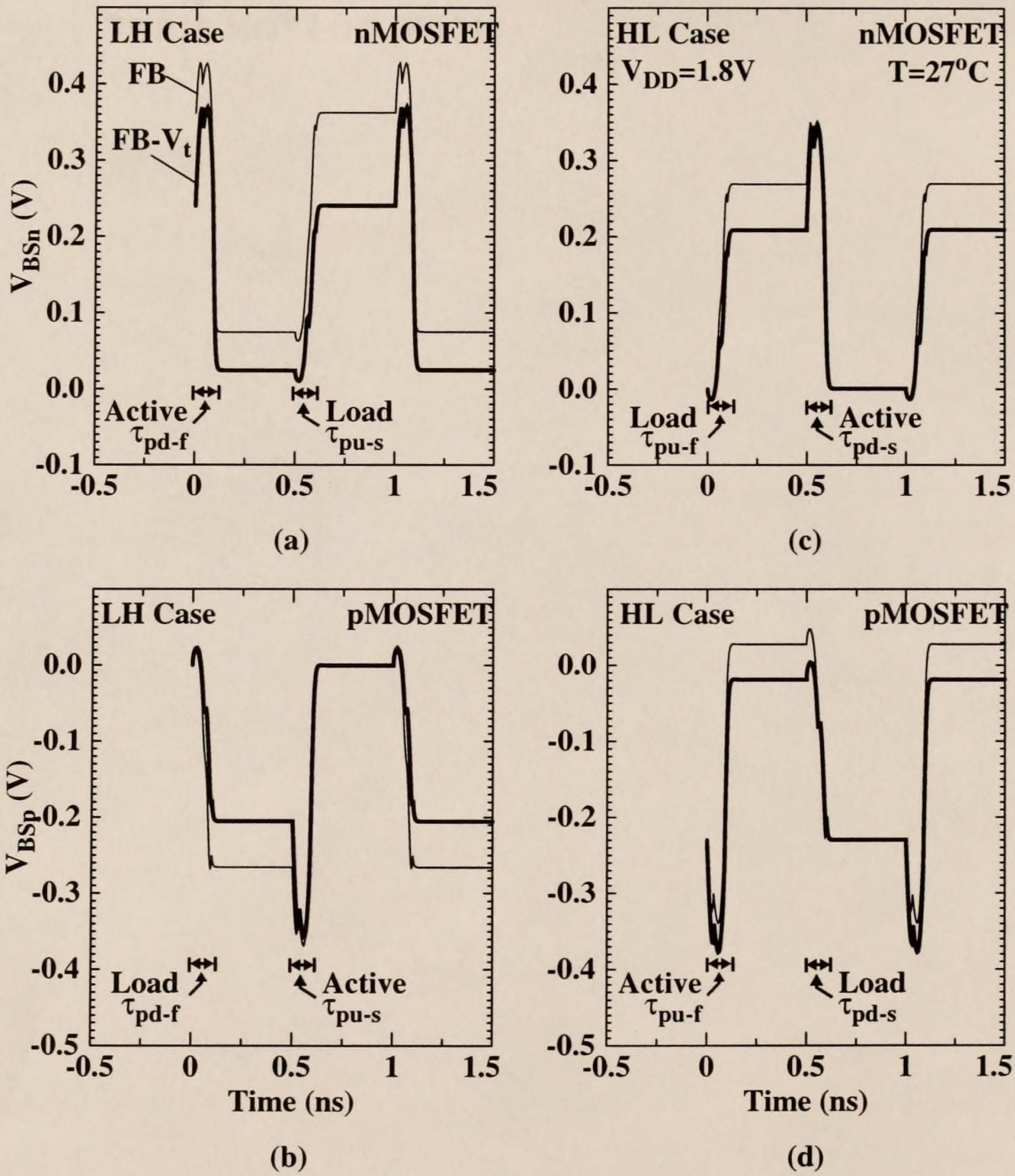


Figure 4.4 V_{BS} vs. time for nominal and increased V_t FB/SOI technologies. UFSOI-predicted $V_{BS}(t)$ for the nominal FB/SOI and FB-V_t/SOI 145nm L_{eff} technologies. L_{gate}=195nm, t_{ox}=4.5nm, $V_{t(linear)}$=0.4V@ I_{DS}=100nA*W/L, T=27°C, V_{DD}=1.8V, τ_{rise}/τ_{fall}=100ps, Wp/Wn=32/16, $L_{S/D}$ =6λ G/R.

Also, superimposed on Fig. 4.4 are the corresponding fundamental delays and an indication of what mode (active or load) the device is operating in during each input switching event.

As shown in Fig. 4.4(a), increasing V_t (FB-V_t/SOI) results in V^i_{BS} dropping from 0.36V to 0.24V, while the V^{ss}_{BS} remains about the same. The decrease in V^i_{BS} is due to the reduced impact-ionization current (I_{Gi}), driven by the channel current, in the off-state condition where $I_R(V_{BS}) = I_{Gi}$, as described in Chapter 2. The V^{ss}_{BS}, defined by the dynamic steady-state condition in (3.1), remains unchanged since the (dynamic) I_{on} for both technologies is nearly the same.

4.4 Performance Insights

4.4.1 Delay Benefit from Junction Capacitance

With reference to Fig. 4.3 and Table 4.2, if the bodies of the FB/SOI devices are tied to the sources (BTS/SOI), yielding I_{off} equal to that of the bulk-Si devices, the τ^{ss}_{RO} performance benefit is reduced to 7.6%. This result reflects the benefit of the reduced SOI source/drain junction capacitance afforded by the thick t_{BOX}. The rest of the previously noted τ_{RO} performance benefit is due to the FB effects described as follows.

4.4.2 Delay Benefit from the Kink Effect

To distinguish the FB delay benefit of the (subthreshold) kink effect (i.e., a V_t lowering due to impact-ionization charging of the body) versus that of the capacitive-coupling effects, the two input conditions defined in Chapter 3 were simulated with the body voltages (V_{BS}) of their devices fixed to the initial DC levels.

For the low-to-high (LH) input condition, the pull-down "fast" or "first-switch" (τ_{pd-f}) and pull-up "slow" or "second-swicth" (τ_{pu-s}) fundamental inverter delays of Fig. 3.2 are derived with the body voltages of the devices tied to their initial DC values (V_{BSn}=0.36V and V_{BSp}=0V) defined by the input-low simulation. Similarly, for the high-to-low (HL) input condition, the pull-up "fast" or "first-switch" (τ_{pu-f}) and pull-down "slow" or "second-swicth" (τ_{pd-s}) fundamental inverter delays are obtained with the body voltages of the devices tied to their initial DC values (V_{BSn}=0V and V_{BSp}= -0.23V) defined by the input-high simulation. Then, the initial τ_{RO} (τ^i_{RO}) without the capacitive-coupling effect can be computed from these fundamental delays: $\tau^i_{RO} = (\tau^i_{pd-f} + \tau^i_{pu-s} + \tau^i_{pu-f} + \tau^i_{pd-s})/4$. The results, as depicted in Fig. 4.3, indicate that the FB/SOI performance benefit from the kink effect is only 5.0% of the total 25% τ^i_{RO} benefit.

This result contradicts the I_{on} improvement (20%) from the DC kink effect for the nMOSFET and is due to the relatively long time ($<Q_B/I_{Gi}>$ ~1 μs) required to fully charge the body via impact ionization as compared to the fast $V_{GS}(t)$ input switching signal [Jen96], [Wei95]. For fast input rise times, the total generation current ($I_G = I_{Gi}+I_{Gt}+I_{Gtun}$) first supports the transient body-charging current (dQ_B/dt) prior to it significantly influencing I_R (or $V_{BS}(t)$), which can be expressed as

$$I_R = I_G - \frac{dQ_B}{dt} \tag{1}$$

where

$$I_R \propto \exp\left(\frac{qV_{BS}}{nkT}\right) \tag{2}$$

and

$$\frac{dQ_B}{dt} = C_{BS}\frac{d}{dt}(V_{BS}) + C_{BD}\frac{d}{dt}(V_{BD}) + C_{BGf}\frac{d}{dt}(V_{BGf}) + C_{BGb}\frac{d}{dt}(V_{BGb}) \cdot \qquad (3)$$

Thus, for fast slew rates, the full performance benefit of the DC kink-effect enhancement of I_{on} is not realized. For slow slew rates, I_G can more directly affect I_R since dQ_B/dt is small, and the benefit can be realized. Changes to the slew rate will thus significantly affect the propagation delay and their hysteretic behavior [Pel99a]; an increase in the slew rate will increase both the propagation delay and the accompanying hysteresis. Note that if $V_{BS}(t=0)=0V$, the device will not acquire any significant performance benefit from the kink effect until I_G becomes significantly greater than dQ_B/dt during subsequent switching events.

4.4.3 Delay Benefit from the Capacitive-Coupling Effect

The remaining 12% of the τ^i_{RO} performance improvement as indicated in Fig. 4.3 can be attributed to the capacitive-coupling effects, which strongly influence $V_{BS}(t)$ and the dynamic V_t in two ways. The first is the classical *current-overshoot effect* [Lim84], which improves the fast delays ($\tau_{pd\text{-}f}$, $\tau_{pu\text{-}f}$) by increasing $|V_{BS}(t)|$ (lowering the dynamic V_t) via *gate-to-body coupling* during the first and subsequent odd transitions of the input signal. The second is the *dynamic loading effect* as described in Chapter 3, which improves the slow delays ($\tau_{pd\text{-}s}$, $\tau_{pu\text{-}s}$) by decreasing $|V_{BS}(t)|$ (raising the dynamic V_t) of the load device via *drain-to-body coupling* during the second and subsequent even transitions of the input signal. As shown in Fig. 4.4(a), the capacitive coupling of the drain to body, subsequent to the pull-down of the output voltage, pulls V_{BSn} lower prior to the pull-up transition of the output voltage. This beneficial coupling weakens the drive current of the nMOSFET and

thus provides a smaller load for the active pMOSFET when it pulls up the output voltage. At the same time, as shown in Fig. 4.4(b), the gate-to-body capacitive coupling induces a V_{BSp} overshoot in the pMOSFET that helps strengthen its drive current prior to the output pull-up transition, also enhancing this performance benefit.

4.4.4 Body-Voltage Dynamics and Increased Threshold Voltage

The τ_{RO} delay, defined by the fundamental delays ($\tau_{pd\text{-}f}$, $\tau_{pu\text{-}s}$, $\tau_{pu\text{-}f}$, $\tau_{pd\text{-}s}$) as discussed in Chapter 3, strongly depends on the behavior of the V_{BS} as a function of time, shown in Fig. 4.4. The initial V_{BSn} for this fundamental delay is established at the DC condition of equal recombination and generation currents (I_R=I_G) and subsequently pulled higher by the gate-to-body coupling (overshoot) prior to the formation of the inversion region ($V_{GS} < V_{tn}$). When $V_{GS} > V_{tn}$, the inversion layer forms and inhibits the gate-to-body coupling; V_{BSn} then follows the drain (output) voltage lower via the drain-to-body capacitive coupling. Concurrently, the V_{BSp} of the pMOSFET load is first coupled higher from the gate-to-drain Miller capacitance, since the inversion layer screens the direct gate-to-body coupling, and then follows the drain voltage lower (increasingly negative) until $|V_{GS}| < |V_{tp}|$. The dynamic-capacitive coupling mechanisms described above all contribute positively to improve the fundamental delays, which translates into an improved τ_{RO} speed performance for the FB/SOI technology.

If we now consider the $\tau_{pu\text{-}s}$ delay for the second switching transition of the LH case when V_{GS} returns to its low voltage level, the V_{BSp} of the active pMOSFET is first coupled to increasing negative voltages via the gate-to-body

coupling (overshoot), since $|V_{GS}| < |V_{tp}|$ and the inversion layer is not formed. Then, when $|V_{GS}| > |V_{tp}|$ the inversion layer forms and V_{BSp} follows the drain higher (decreasing negative voltages) via the drain-to-body coupling, which "weakens" the pMOSFET for the next input transition when it becomes the load device for the pull-down condition. Concurrently, for the $\tau_{pu\text{-}s}$ delay, the V_{BSn} of the nMOSFET is first coupled lower via the gate-to-drain Miller capacitance and the drain-to-body coupling, since the channel inversion layer is present, and then follows the drain to a higher voltage level, until $V_{GS} < V_{tn}$. The $V_{BS}(t)$ behavior of the $\tau_{pu\text{-}f}$ and $\tau_{pd\text{-}s}$ delays can be similarly described for the HL input transitions, as depicted in Figs. 4.4(c) and 4.4(d).

As described previously, the $V_{BS}(t)$ results for the increased-V_t FB/SOI (FB-V_t/SOI) technology are shown in Fig. 4.4 superimposed on the nominal FB/SOI results. The initial V_{BSn} is lower, due to the reduction in the channel current at the I_{off} condition, which lowers I_{Gi} and thus V^i_{BSn} is reduced (0.36V to 0.24V). The overshoot condition is enhanced since the gate-to-body coupling can affect the body voltage for a longer duration given the higher V_t. The drain-to-body coupling remains the same, except that the coupling of the V_{BS} for the load device terminates earlier than the nominal technology, since V_{GS} reaches V_t sooner during the input transitions and removes the inversion layer. The reduction of V_{BS} and the reduced drive current from the higher V_t combine to degrade the τ_{RO} performance of the FB-V_t/SOI technology, as reflected in Fig. 4.3.

4.5 Scaling SOI: Diminishing Returns?

4.5.1 Scaled SOI CMOS Devices

Via UFSOI simulation, the SOI CMOS technology is scaled to L_{eff}=70nm consistent with the ITRS [SIA99] technology requirements for the 100nm MPU gate length node, with the idea of reducing the device dimensions (to reduce the cost per function) and the power supply (to minimize power increase and high field effects) while still maintaining the current drive (per unit width) of the prior technology for improved performance. The L_{eff}=145nm, 1.8V nMOSFET technology was scaled to the L_{eff}=70nm, 1.2V technology by first thinning the t_{ox} (**TOXF**) from 4.5nm to 2.1nm to control short channel effects; the channel doping concentration (**NBL**) was then adjusted to maintain a $V_{t\text{-}lin}$ (at I_{DS}=100nA*W/L) of 0.4V in order to control I_{off}; and the depth (**TB**) of the retrograded channel was reduced sufficiently less than the MOSFET's maximum depletion width to maintain the model's validity, but keeping in mind the trade-off with the subthreshold slope (which degrades as **TB** is reduced). The BOX thickness was also reduced to 200nm (consistent with lower cost wafer trends) and the mobility and source/drain resistances were adjusted to achieve an appropriate I_{on} level that was consistent with recently published PD/SOI technologies [Mis00], [Leo99] at 1.5V. The pMOSFET was scaled in a similar way as the nMOSFET, with the hole mobility reduced by ~0.5x (relative to the electron mobility) and the source/drain resistance doubled, while maintaining its $I_{on\text{-}p}$ at ~0.5x of the nMOSFET's $I_{on\text{-}n}$.

The room-temperature subthreshold I_{DS}-V_{GS} FB device characteristics for the minimum-L_{eff} (50nm) condition in the scaled technology are shown in Fig. 4.5; V_{DD}=1.2V, $V_{t(linear)}$=0.4V @ I_{DS}=100nA*W/L, t_{ox}=2.1nm, t_{BOX}=200nm, t_{SOI}=100nm. Analogous to Fig. 4.2, the predicted bulk-Si (well doping at $10^{17}cm^{-3}$), BTS-SOI, and FB-V_t/SOI (ΔV_{tn}=118mV, ΔV_{tp}=102mV) characteristics are also shown in Fig. 4.5. The drive currents at V_{DD}=1.2V (without self-heating) for the minimum channel length (L_{eff}=50nm) nMOSFETs/pMOSFETs of each technology are 0.79/0.40 mA/μm for FB-SOI, 0.71/0.37 mA/μm for FB-V_t/SOI, and 0.65/0.33 mA/μm for BTS-SOI/bulk-Si. Table 4.3 summarizes I_{on} and I_{off} for the minimum-L_{eff} nMOSFET and pMOSFET for each scaled technology.

Table 4.3 Comparison of I_{on} and I_{off} of the nominal L_{eff}=70nm devices at the minimum L_{eff} condition for the scaled MOSFET technologies

L_{eff}=50nm (min) 1.2V, 27°C	FB/SOI		FB-V_t/SOI		BTS/SOI, bulk-Si	
	nMOS	pMOS	nMOS	pMOS	nMOS	pMOS
I_{on} (mA/μm)	0.79	0.40	0.71	0.37	0.65	0.33
I_{off} (nA/μm)	118	157	4	9	4	9

4.5.2 Performance Comparison

The predicted τ^{ss}_{RO} performance benefit for the scaled FB/SOI technology over the scaled bulk-Si counterpart is reduced slightly to 28%, as shown in Fig. 4.6. The device layouts again assume a 6λ based ground rule for the source/drain contact lengths, with λ equal to L_{gate}/2.0 (L_{gate}=100nm). However, when V_t is increased (FB-V_t/SOI) to achieve an equivalent I_{off} as in the bulk-Si technology, the

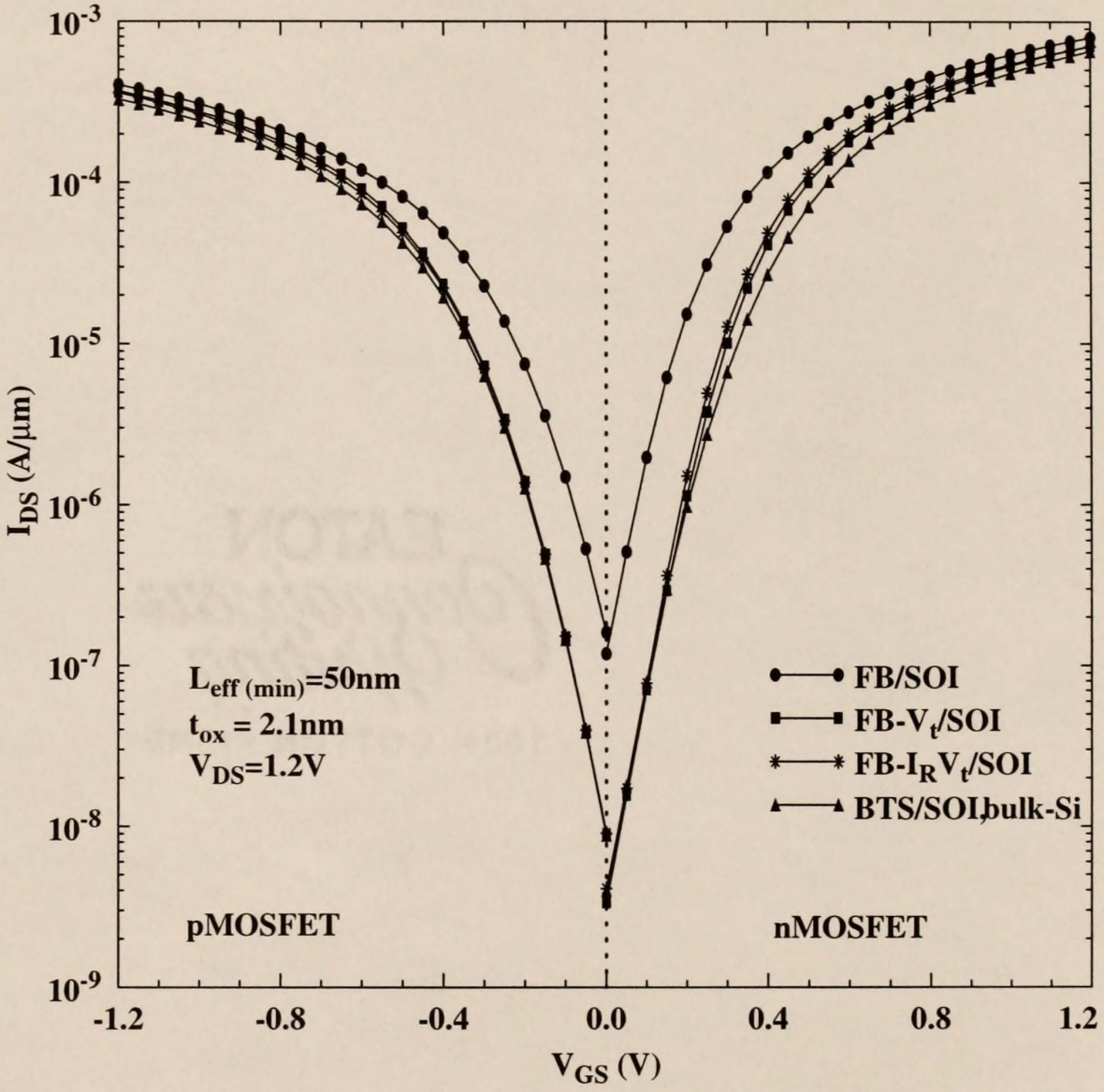


Figure 4.5 Predicted I_{DS}-V_{GS} for SOI and bulk-Si 70nm technologies. UFSOI-predicted subthreshold current-voltage characteristics of the minimum devices (L_{eff}=50nm) for 70nm L_{eff} SOI nMOSFET and pMOSFET technologies including: FB/SOI, FB-V_t/SOI, FB-$I_R V_t$/SOI, BTS/SOI(bulk-si equivalent DC characteristics); t_{ox}=2.1nm, t_{soi}=100nm, $V_{t(linear)}$=0.4V@I_{DS} =100nA*W/L, T=27°C.

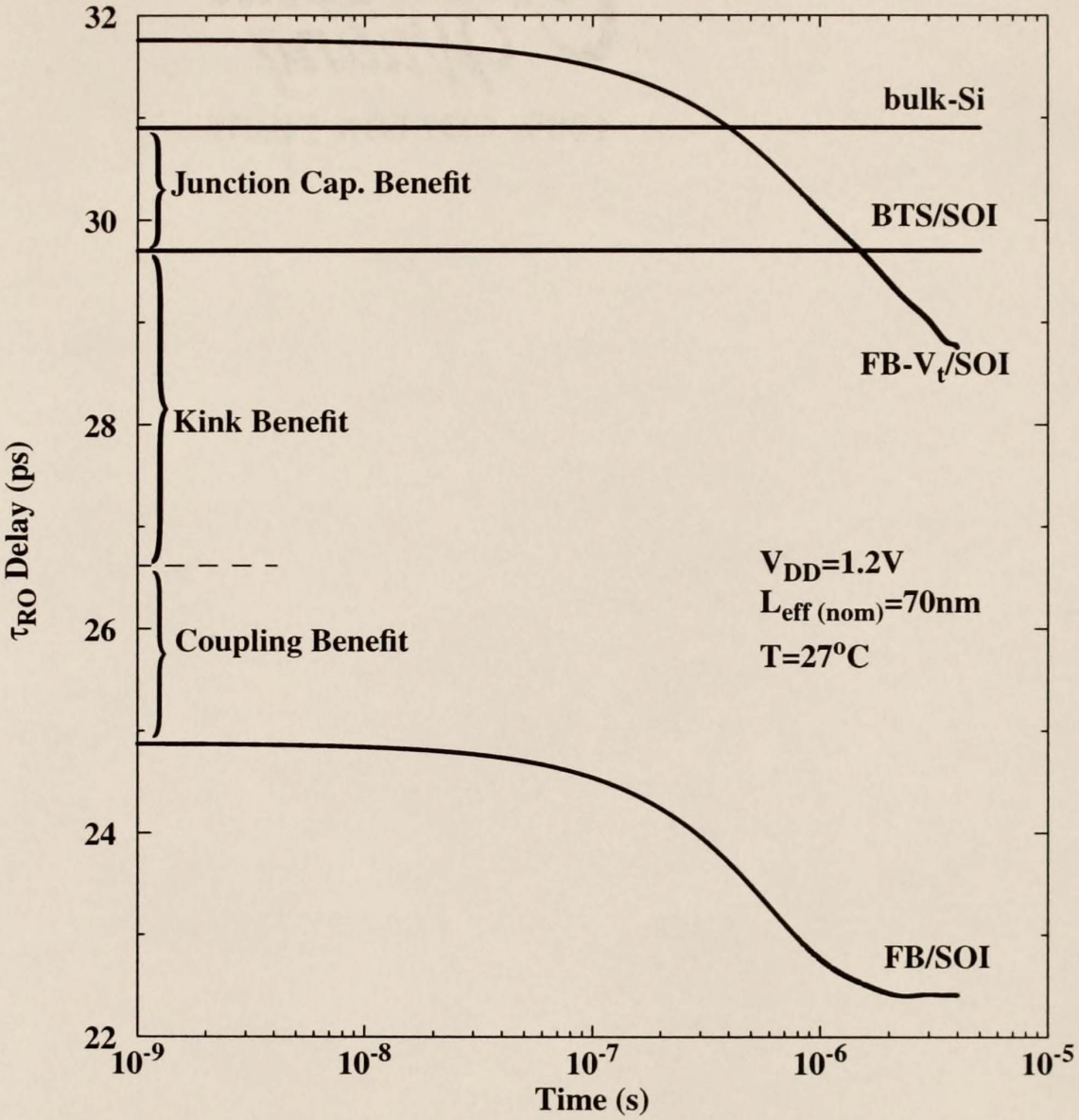


Figure 4.6 Predicted delay for SOI and bulk-Si 70nm technologies. UFSOI-predicted τ_{RO} propagation delay for the 70nm L_{eff} technologies. L_{gate}=100nm, t_{ox}=2.1nm, $V_{t(linear)}$=0.4V@I_{DS}=100nA*W/L, T=27°C, V_{DD}= 1.2V, τ_{rise}/τ_{fall}=100ps, Wp/Wn=32/16, $L_{S/D}$=6λ G/R.

performance benefit of the FB-V_t/SOI technology is significantly reduced to only 6.5%, as summarized in Table 4.4 for the four scaled technologies. The hysteresis is also predicted to worsen (to 10% from 4.5%) as the technology is scaled, due mainly to the reduction in the power supply as described in Chapter 3 and [Pel99a].

Table 4.4 Predicted steady-state delay and hysteresis results for the five scaled L_{eff}=70nm technologies.

L_{eff}=70nm (nom) V_{DD}=1.2V, T=27°C	FB/SOI	FB-V_t/SOI	BTS/SOI	bulk-Si
τ^{ss}_{RO} (ps)	22.4	28.9	29.7	30.9
SOI Benefit over bulk-Si	27.5%	6.5%	3.9%	--%
τ_{RO} Hysteresis($\Delta\tau_{RO}/\tau^{i}_{RO}$)	10%	10.6%	--%	--%

4.5.3 Loss of SOI Advantage

As the technology is scaled, the performance benefit, as quantified in Fig. 4.6, is predicted to diminish, especially for the I_{off} controlled (FB-V_t/SOI) technology. This is due in part to a lesser gain from the decreased junction capacitance since the layout ground rules of the source/drain regions are correspondingly reduced. Moreover, as the areal component of junction capacitance is reduced, the perimeter component (adjacent to the body region) is increasing due to the higher doping concentrations in the body and halo implants. This indicates that the difference between the bulk-Si and the SOI junction capacitances will shrink, and portends a diminishing performance benefit from the reduction of the junction capacitance in scaled SOI technologies.

Furthermore, the delay contribution of the capacitive-coupling effect is reduced to only 5.0% compared to 12% for the contemporary L_{eff} =145nm technology. The beneficial *dynamic loading effect* is the predominate component reduced; this is a result of the reduced output voltage swing, due to the lower supply voltage, V_{DD}, as can be inferred from the discussions of Fig. 4.4. (These results, in conjunction with those in Fig. 4.3, clearly show that the main capacitive-coupling effect is due to the body-drain junction capacitance.) Consequently, the kink-effect contribution increased to 10% for the scaled FB/SOI technology compared to 5% for the contemporary technology. This is not a beneficial trade-off since the DC kink effect typically controls I_{off} and is usually suppressed.

4.5.4 Temperature Effects

At elevated ambient temperatures (T=85°C), the performance benefit of the τ^{ss}_{RO} delay for the scaled FB/SOI technology is predicted to reduce from 28% to 20% relative to the bulk-Si counterpart technology, as shown in Fig. 4.7. This is due to the natural amelioration of the FB effect by the increased $I_R(T)$ at elevated temperatures discussed in Chapter 2, which while diminishing the τ_{RO} performance benefit some, helps to suppress the excessive I_{off} and hysteresis of the FB/SOI technology, making it more palatable.

For the scaled FB-V_t/SOI technology at T=85°C, with a controlled I_{off}, the performance benefit increased from 6.5% to 9.9% over an equivalent bulk-Si technology, with its associated hysteresis reduced by half of the room-temperature value. This improvement is due to a smaller V_t shift (ΔV_{tn}=62mV, ΔV_{tp}=46mV

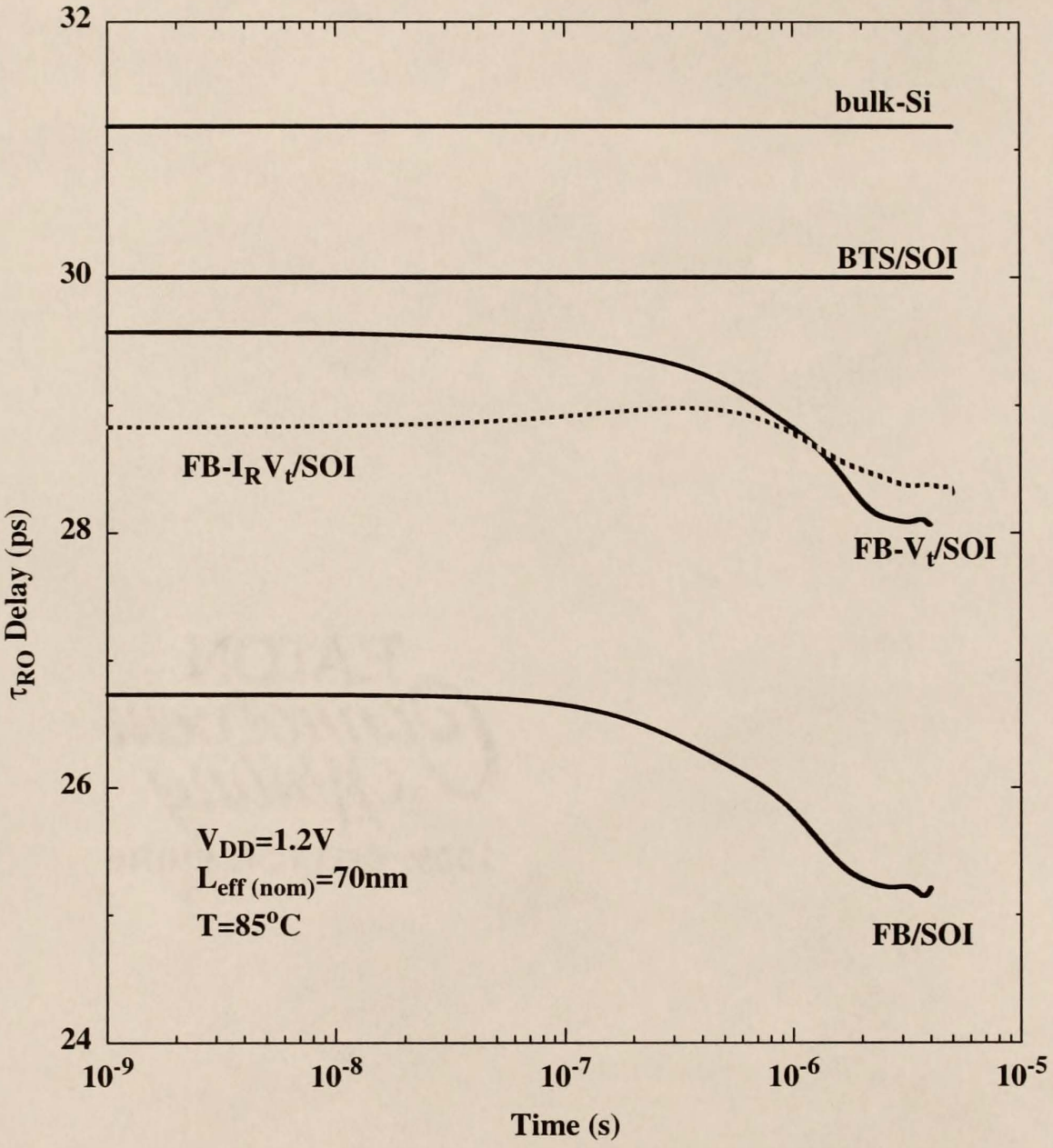


Figure 4.7 Predicted delay for SOI and bulk-Si 70nm technologies at T=85°C. UFSOI-predicted τ_{RO} propagation delay for the scaled L_{eff}=70nm technologies with the optimized FB-I_R/SOI superimposed at elevated ambient temperatures. L_{gate}=100nm, t_{ox}=2.1nm, $V_{t(linear)}$=0.4V@I_{DS}=100nA*W/L, T=85°C, V_{DD}= 1.2V, τ_{rise}/τ_{fall}=100ps, Wp/Wn=32/16, $L_{S/D}$=6λ G/R.

compared to ΔV_{tn}=118mV, ΔV_{tp}=102mV at T=27°C) that is needed to achieve a controlled I_{off} at elevated temperatures.

If I_R is intentionally increased further by 10x (beyond the increase from the temperature effect), yielding FB-$I_R V_t$/SOI (ΔV_{tn}=36mV, ΔV_{tp}=24mV), the performance benefit is maintained at 9.3% while its associated hysteresis is reduced to a negligible value (only 1.7%), as depicted in Fig. 4.7. The performance results for the all technologies discussed above at elevated ambient temperatures are summarized in Table 4.5.

Table 4.5 Predicted steady-state delay and hysteresis results for the five scaled L_{eff}=70nm technologies at elevated ambient temperatures.

L_{eff}=70nm (nom) V_{DD}=1.2V, T=85°C	FB/SOI	FB-V_t/SOI	FB-$I_R V_t$/SOI	BTS/SOI	bulk-Si
τ^{ss}_{RO} (ps)	25.1	28.1	28.3	30.0	31.2
SOI Benefit over bulk-Si	19.6%	9.9%	9.3%	3.9%	--%
τ_{RO} Hysteresis ($\Delta\tau_{RO}/\tau^{i}_{RO}$)	6.3%	4.8%	1.7%	--%	--%

4.6 Increased SOI Advantage: Stacked Logic Gates

The CMOS inverter, which has been studied so far, provides the basic building block for higher level static logic circuits, e.g., two-input or two-way NAND (2WNAND), as shown in Fig. 4.8. The stacked (or series-connected nMOSFETs) nature of 2WNANDs gives rise to an added benefit in SOI technologies by eliminating the detrimental body-bias (reverse V_{BS}) effects associated with the top nMOSFET (N2) in bulk-Si technologies. The performance benefit of the scaled 1.2V, L_{eff}=70nm FB SOI CMOS technology with I_{off} controlled (FB-V_t/SOI) is

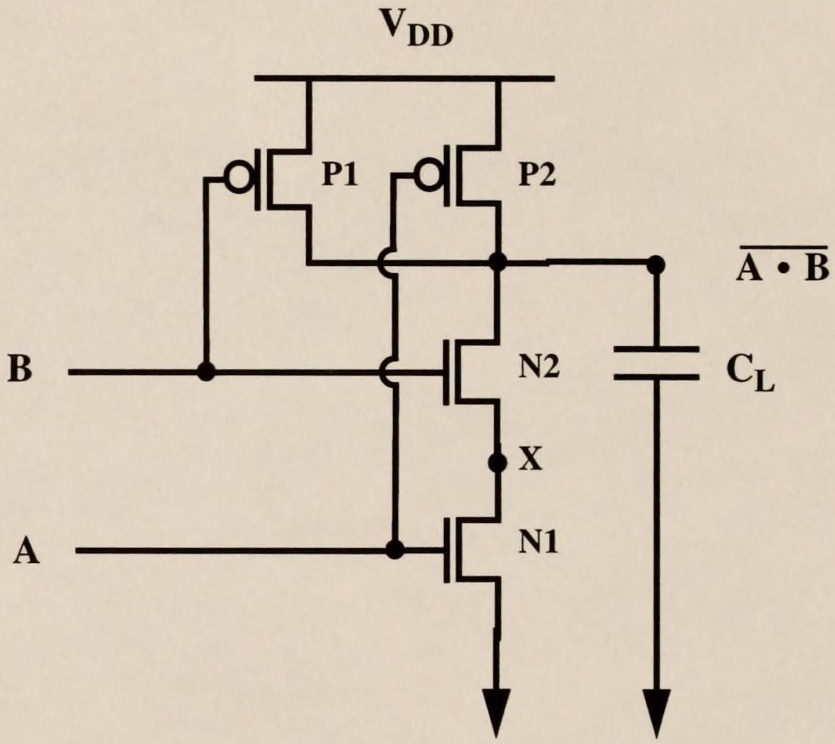


Figure 4.8 Schematic of a two-input NAND circuit.
The transistors are labeled P1,P2, N1, and N2; The connecting node of N1 and N2 is labeled as X. The capacitive load is labeled as C_L.

investigated, using UFSOI/SPICE, for the three possible switching configurations of a 2WNAND logic circuit with $W_n=W_p$ (device width ratio is equal to 1): top, bottom, and simultaneously switching, where the designation refers to the active switching device of the nMOSFET stack.

4.6.1 Top-Switching Case

The τ_{RO} (as obtained from the hysteretic inverter delay methodology described in Chapter 3 for the 2WNAND circuit) results for the top-switching case of the 2WNAND circuit (the top nMOSFET (N2) in the stack continuously switches its logic level while the bottom nMOSFET (N1) maintains a high or "on" level, as depicted in Table 4.6) are shown in Fig. 4.9. An 11% τ^{ss}_{RO} performance benefit for the FB-V_t/SOI technology over its bulk-Si counterpart is predicted as shown in Fig. 4.9(a); an associated hysteresis of 11% is also predicted. The τ^{i}_{RO} results indicates

Table 4.6 2WNAND top-switching configuration truth table of Fig. 4.8.

Input: A	Input: B	Output: $\overline{AB}$
1	0	1
1	1	0

that there is no performance benefit during the initial switching cycles of the 2WNAND circuit. This is mainly due to the increased threshold voltage of the FB-V_t/SOI technology compared to the bulk-si counterpart, suggesting that an alternative technology or operation at an elevated ambient T should be used if this part of the delay is vital. The increased performance benefit of the 2WNAND as compared to the 6.5% inverter benefit is mainly due to the elimination of the reverse body-bias effect. The floating-body effect also contributes to this performance gain

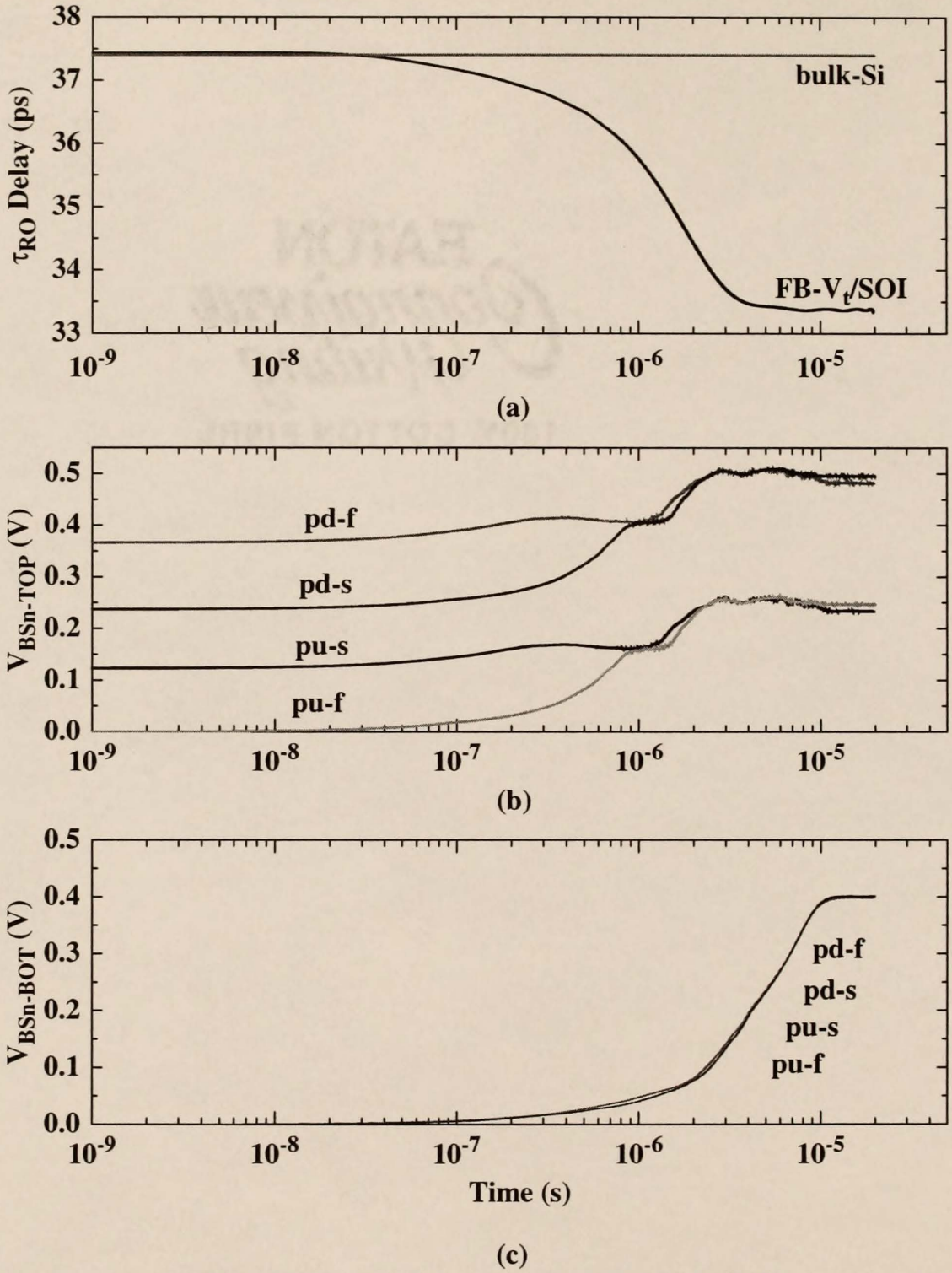


Figure 4.9 Predicted 2WNAND delay for SOI and bulk-Si 70nm technologies. UFSOI-predicted top-switching 2WNAND τ_{RO} propagation delay analysis for the scaled L_{eff}=70nm I_{off} controlled (FB-V_t/SOI) technology with its bulk-Si counterpart superimposed. a) delay versus time, b) corresponding FB-V_t/SOI top nMOSFET $V_{BS}(t)$ prior to each input transition for each fundamental delay, and c) corresponding FB-V_t/SOI bottom nMOSFET $V_{BS}(t)$. L_{gate}=100nm, t_{ox}=2.1nm, $V_{t(linear)}$=0.4V @ I_{DS}=100nA*W/L, T=27°C, V_{DD}=1.2V, τ_{rise}/ τ_{fall}=100ps, Wp/Wn=32/32, $L_{S/D}$=6λ G/R.

but to a lesser extent (mainly through the dynamic-loading effect identified in Chapter 3), since the charging effects of the floating body are nearly the same. Although node X (the node connecting the two stacked nMOSFETs (N1 and N2) in Fig. 4.8) still rises to support the discharge current as in the bulk-Si technology, its affect on the threshold voltage is overwhelmed by the increased body potential of FB SOI technology. For each of the fundamental delays described in Chapter 3, the body-to-source voltages as a function of time for N1 and N2 of the stack are shown in Figs. 4.9(b) and (c), respectively, which were recorded at time-points just prior to the input rise and fall transitions. The charging of the floating body in N2 is in accord with the charging dynamics of the inverter. However, N1charges much more slowly since it is constantly on and hence only charges its body during the output pull-down transients when node X increases slightly to support the discharge current (or channel current) that drives impact ionization near the drain.

4.6.2 Bottom-Switching Case

For the bottom-switching case of the 2WNAND circuit (the bottom nMOSFET in the stack continuously switches its logic level while the top nMOSFET maintains a high or "on" level, as depicted in Table 4.7), the predicted τ^{ss}_{RO} performance benefit of the FB-V_t/SOI technology over its bulk-Si counterpart is 6.9%, as summarized later in Table 4.9, with an associated hysteresis of 5.0%. The

Table 4.7 2WNAND bot-switching configuration truth table of Fig. 4.8.

Input: A	Input: B	Output: $\overline{AB}$
1	1	0
0	1	1

delay-versus-time results are shown in Fig. 4.10(a) superimposed on the top-switching case results, indicating degraded delay. The reduction in the performance benefit, compared to the bulk-Si counterpart and the top-switching case, is due in part to a reduced FB effect in N2 since node X is much higher than in the top-switching case during the switching transients, as shown in Fig. 4.10(b), and to a lower drain voltage ($V_{DS\text{-}Bot}$) for N1; the output voltage is divided across both nMOSFETs, contingent upon their operating region, in the stack, which lowers the drive current. This causes the body voltage of N2 to drop (or the body discharge) in time, also weakening its drive current. As a result, the dynamic-loading effect described in Chapter 3 is much more significant under this switching configuration, which counters the τ^{ss}_{RO} speedup and reduces the performance gain and its affiliated hysteresis.

4.6.3 Simultaneously Switching Case

For the simultaneously switching case of the 2WNAND circuit (the top and bottom nMOSFETs in the stack continuously switch their logic levels at the same time, as depicted in Table 4.8), the predicted τ^{ss}_{RO} performance benefit of the FB-V_t/SOI technology over its bulk-Si counterpart is 3.2% with an associated hysteresis

Table 4.8 2WNAND simultaneously switching configuration truth table of Fig. 4.8.

Input: A	Input: B	Output: $\overline{AB}$
1	1	0
0	0	1

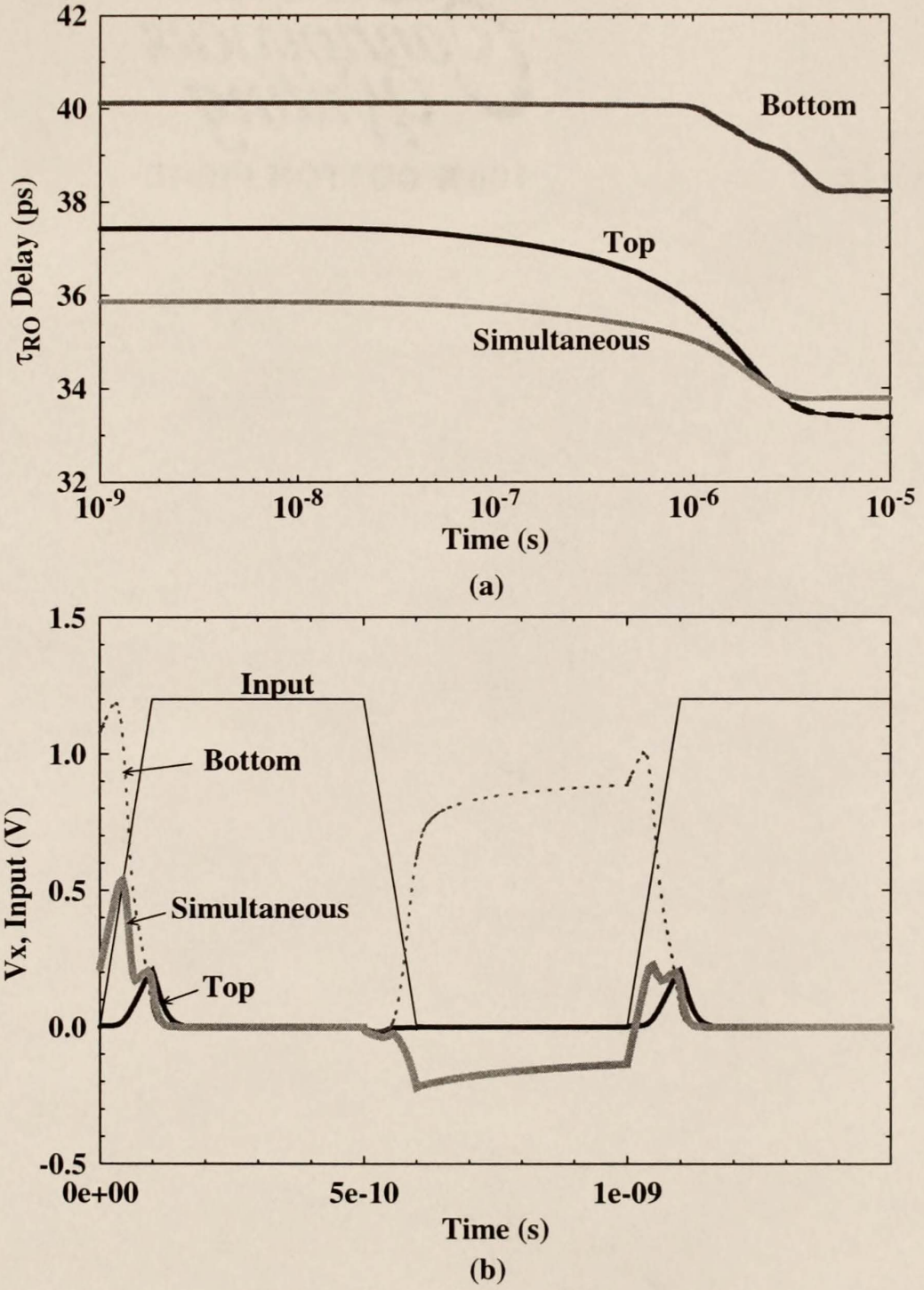


Figure 4.10 Predicted 2WNAND delay for various switching configurations. UFSOI-predicted 2WNAND τ_{RO} propagation delay analysis with W_p/W_n=1 in the scaled L_{eff}=70nm I_{off} controlled (FB-V_t/SOI) technology. a) delay versus time for the top, bottom, and simultaneously switching configurations, b) V_x node (the node connecting the two stacked nMOSFETs) versus time during the first input cycle for the three switching configurations. L_{gate}=100nm, t_{ox}=2.1nm, $V_{t(linear)}$=0.4V@I_{DS}= 100nA*W/L, T=27°C, V_{DD}=1.2V, τ_{rise}/τ_{fall}=100ps, Wp/Wn=32/32, $L_{S/D}$=6λ G/R.

of 5.9%. The τ_{RO} results, as shown superimposed on Fig. 4.10(a), indicate a significant speedup in the τ^{i}_{RO} delay (compared to the top- and bottom-switching configurations) which is due to: i) the doubling of the pull-up drive current since both pMOSFETs are switched on, ii) the moderately charged bodies of the nMOSFETs, which reduce the body-bias effects as in the other switching cases, and iii) the gate coupling of node X to a negative voltage (see Fig. 4.10(b)) during the high-to-low input transitions, which helps to eliminate the transient drain current in the nMOSFETs (which act as the load during this transition) while the pMOSFETs pull the output node high. However, as with the bottom-switching case, the lack of significant charging in the nMOSFETs relative to the pMOSFETs enhances the dynamic-loading effect and contributes to a reduced τ^{ss}_{RO} speedup and hysteresis. Table 4.9 summarizes the 2WNAND circuit results for all three switching cases.

Table 4.9 Predicted propagation delay and hysteresis results for the three switching configurations of a 2WNAND circuit.

2WNAND, W_p/W_n=1 L_{eff}=70nm (nom), V_{DD}=1.2V, T=27°C	bulk-Si τ_{RO} (ps)	FB-V_t/SOI τ^{i}_{RO} (ps)	FB-V_t/SOI τ^{ss}_{RO} (ps)	SOI Benefit $(\tau_{RO\text{-}bulk} - \tau^{ss}_{RO})/\tau_{RO\text{-}bulk}$	SOI Hysteresis $(\Delta\tau_{RO}/\tau^{i}_{RO})$
Top	37.4	37.4	33.3	11%	11%
Bottom	40.9	40.1	38.1	6.9%	5.0%
Simultaneously	34.8	35.8	33.7	3.2%	5.9%

4.6.4 Device Width Ratio and Temperature Sensitivity

When the device width ratio (W_p/W_n) is altered from 1 ($W_n=W_p$) to 2 ($W_n=W_p/2$) or 0.5 ($W_n=2W_p$), the 2WNAND performance benefit of the FB-V_t/SOI technology over its bulk-Si counterpart remains about the same (~11%) for all three

cases in the top-switching configuration. The absolute delays (initial and dynamic steady-state) were the shortest for the W_n=W_p case. Even though the performance benefit results are nearly the same, the shift in the ratio affects the voltage level of node X, which influences the dynamic-loading effect and hence the level and time that each device in the circuit achieves its dynamic steady state. Although there are noise-margin implications associated with changing the device width ratio, the nearly constant performance benefit suggests that the circuit layout density may be improved by using smaller device width ratio, i.e., (W_p = W_n/2).

When the ambient temperature is increased to 85°C, increasing I_R, the predicted τ^{ss}_{RO} delay for the top-switching case of the 2WNAND circuit with W_n=W_p is 33.7ps, which is nearly the same as the T=27°C case (33.3ps), and the performance benefit over its bulk-Si counterpart is also the same at 11%. However, the τ^{i}_{RO} delay at T=85°C improves by 6.7% to 34.9ps, reducing the hysteresis to only 3.4%. If I_R is intentionally increased further (by 10x) along with T=85°C, the predicted τ^{ss}_{RO} delay improves to 32.7ps and the τ^{i}_{RO} delay improves to 34.1ps, while improving the performance benefit over its bulk-Si counterpart to 14%.

4.7 Discussion: Optimization and Future Opportunities

To further enhance the SOI performance benefit of the CMOS inverter circuit over its bulk-Si counterpart, additional and more aggressive approaches are considered based on the insight provided in the analyses of the previous sections.

4.7.1 Optimization: Recombination Current and Device Structure

If I_R is moderately increased (100x) in conjunction with an increased V_t (V_{tn} and V_{tp} shifted by 60 and 50mV, respectively) at T=27°C, yielding FB-I_R100V_t/SOI with an equivalent I_{off} as its bulk-Si counterpart, the CMOS inverter τ^{ss}_{RO} performance benefit for the scaled technology improves to 9.7%, with its accompanying hysteresis decreasing from 10.6% to 6.4%. Further, to enhance the capacitive-coupling effect (single-cycle dynamic loading), which is undermined by the V_{DD} reduction, t_{SOI} can be adjusted (100nm to 200nm) to increase C_{DB}. The τ_{FAST} ($\tau_{pd\text{-}f}$, $\tau_{pu\text{-}f}$) delays lenghtened or degraded from the reduction of the overshoot effect due to the stronger drain coupling while the τ_{SLOW} ($\tau_{pd\text{-}s}$, $\tau_{pu\text{-}s}$) delays improved from the enhancement of the dynamic-loading effect. Thus, the delay results show that there is a trade-off between the τ_{FAST} and τ_{SLOW} delays, which leads to nearly an unchanged $\tau^{i}_{RO}/\tau^{ss}_{RO}$ delay and hysteresis.

Alternatively, the *asymmetric SOI CMOS design concept* described in Chapter 3 can be employed via modifying the halo or retrograde doping asymmetrically in either CMOS device to uniquely adjust the dynamic-loading effect. For example, when the halo/retrograde doping is increased in only the pMOSFET, the τ_{FAST} delays increase while the τ_{SLOW} delays decrease, as in the case for increased t_{SOI} in Chapter 3, while hysteresis tends to be negligible. This also suggests an added degree of freedom in the device design, which allows a decoupling of the device structures so that the technology can be designed to fully exploit the performance benefits of SOI, while simultaneously controlling hysteresis.

4.7.2 Present Benefits

In today's 200nm gate length (L_{eff}=145nm), 1.8V PD/SOI technology, the expected τ^{ss}_{RO} performance benefit from the propagation delay of a basic static CMOS ring-oscillator inverter or a 2WNAND circuit, with controlled I_{off}, as predicted in this study and measured in the literature [Buc20], is about 15-25%. The main performance contribution is the dynamic-loading effect of the capacitive coupling, which significantly enhances the τ_{SLOW} or second-transition delays of the τ_{RO} delay for the CMOS circuit. The kink and junction capacitance effects contribute to the overall performance benefit, but to a lesser extent.

4.7.3 Near-Term Future

As the PD/SOI device technology is scaled to 100nm gate lengths (L_{eff}=70nm) and a V_{DD}=1.2V voltage supply, to improve density and performance and contain switching power, the performance benefit of a static PD/SOI CMOS inverter, with controlled I_{off}, over the bulk-Si technology is predicted to diminish to about 6% at T=27°C. The reduced power supply of the scaled technology significantly undermines the dynamic-loading effect, letting the kink effect dominate the performance benefit. However, the fast signal transitions of high-performance CMOS gates do not allow the circuits to fully benefit from the kink-effect enhancement of I_{on}.

At higher operating temperatures (55-85°C), which are typical for high-performance circuits, the FB effects are naturally suppressed from the increased $I_R(T)$. This relinquishes the amount of FB controlling technique needed for a well controlled I_{off}, and thus enables the SOI technology to recover some of its

performance advantage over an equivalent bulk-Si technology while significantly reducing hysteresis as well.

Further, the suppression of the body-bias effects in stacked-transistor circuits (e.g., NAND, Domino, or CPL) also provides a significant advantage for SOI technologies over equivalent bulk-Si technologies, even as the technology is scaled, providing an additional 5-25% [Buc20] performance benefit beyond the intrinsic CMOS inverter benefit. Additionally, the advantage of an attenuated short-channel effect (SCE) in PD/SOI technologies [Cro95] will likely enable the device to be scaled beyond that of conventional bulk-Si technologies, thus providing continued performance and density benefits.

4.7.4 Future

In light of the diminishing performance benefits for conventional scaled PD/SOI CMOS, variations of the SOI device structure should be considered to continue its performance advantage over an equivalent bulk-Si technology, especially when scaled below L_{eff}=50nm and V_{DD}=1.0V. These alternative device designs include: body-contacted schemes, (such as, body-tied-to-gate (BTG) SOI), ultra-thin-film (UTF) fully depleted (FD) SOI, and double-gate (DG) SOI. Another possible approach to enhance the SOI performance advantage is to lower the ambient operating temperature of the chip [Tau97], which may allow the exploitation of the FB effects as the temperature is decreased. Operating PD/SOI MOSFETs at low ambient temperatures will be investigated in Chapter 5.

4.8 Conclusions

The performance benefit of FB PD/SOI technologies over equivalent bulk-Si technologies have been evaluated, suggesting a 23% CMOS inverter-based τ^{ss}_{RO} advantage with I_{off} controlled (FB-V_t/SOI) for a L_{eff}=145nm, 1.8V technology. The dynamic-loading effect was shown to predominate the performance advantage of the 1.8V PD/SOI technology. As PD/SOI CMOS technologies are scaled to 70nm effective channel lengths and a 1.2V power supply, the performance benefit over the bulk-Si counterpart technology was projected to diminish, mainly due to the lower power supply reducing the dynamic-loading effect, providing only a 6.5% τ^{ss}_{RO} performance advantage. The kink effect was shown to dominate the performance advantage for this scaled technology, which is not as effective as the capacitive-coupling effect since the input signal transition rates are too fast for the device to fully realize the enhanced DC drive current levels.

However, operation at elevated ambient temperatures is shown to increase the SOI τ^{ss}_{RO} performance advantage to 9.9%. Moreover, by the utilizing unique optimization techniques (e.g., increased I_R) for the scaled PD/SOI device structure, mitigation of the diminishing performance benefit is shown to be possible, increasing the SOI performance advantage to near 10% with a suppressed hysteresis effect. Furthermore, by employing the *asymmetric SOI CMOS design concept,* the fundamental delays and their associated hysteresis can be improved per specific applications within a given technology. In addition, by exploiting stacked-transistor logic circuits an additional 5-25% performance benefit can be expected. For the three switching configurations of the 2WNAND inverter investigated, the top-switching

case offers the greatest performance benefit over its bulk-Si counterpart, with the simultaneously switching case providing the least benefit. However, the simultaneously switching case provides the shortest τ^{i}_{RO} with the smallest associated hysteresis.

Alternative or more aggressive optimization approaches can increase the performance benefit of PD/SOI technologies, but not generally since there are trade-offs for a given fundamental delay. Exploring aggressive techniques to increase I_R, implementing the *asymmetric SOI CMOS design concept*, and exploiting the capacitive-coupling (or single-cycle dynamic-loading) effect will provide design flexibility while optimizing the delay performance for a given application.

CHAPTER 5
PD/SOI MOSFETS AT LOW TEMPERATURE

5.1 Introduction

One option to counter the slowing CMOS scaling trend [SIA99] is to reduce the ambient temperature (T) of the semiconductor chip. At low operating T, increased carrier mobility, subthreshold slope, and threshold voltage (V_t) have been demonstrated for bulk-Si MOSFETs [Sun87], as exemplified in Fig. 5.1, thus lowering off-state current, enhancing drive current, allowing lower-V_t design, and providing significant improvement in the speed-power performance of the technology, especially for the *same-off-current* T-scaling scenario [Tau97]. In this chapter, the behavior of floating-body (FB) partially depleted (PD) SOI CMOS is evaluated at low T down to -100°C, which reflects a practical range of operating temperature subject to the cost of the required cooling system. The results show that the negative T-coefficient of the FB voltage $V_{BS}(T)$, described in Chapter 2, can lead to activation of the parasitic bipolar transistor (BJT), inducing an anomalous subthreshold current characteristic as T is reduced. They further reveal an increasing off-state current (I_{off}), below a critical T, which implies a possible limit to the low-T operating range of FB PD/SOI CMOS. However, device design optimization is shown to ameliorate this low-T bipolar effect, enabling a lower-T operating range and a significantly enhanced circuit performance. The results also reveal that, as T is

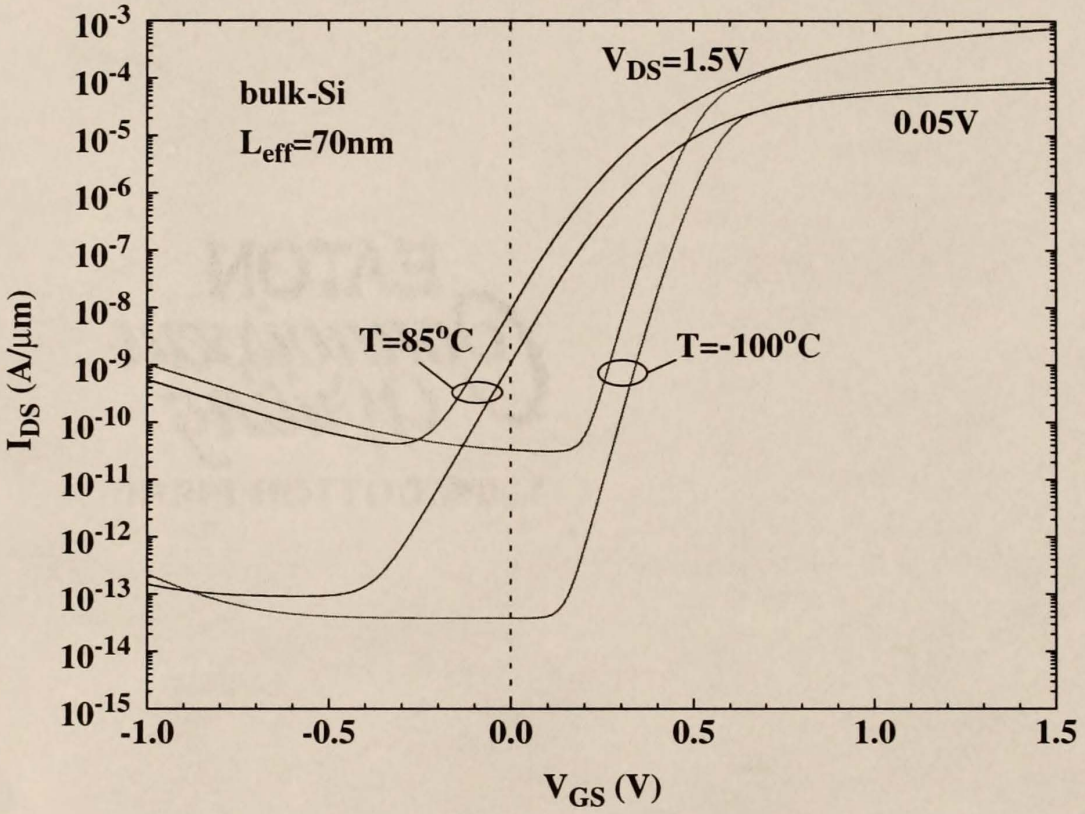


Figure 5.1 Predicted I_{DS}-V_{GS} for bulk-Si as a function of T

UFSOI-predicted saturated subthreshold I_{DS}-V_{GS} as a function of T, exemplifying increased carrier mobility, subthreshold slope, and threshold voltage at low temperatures, for a bulk-Si technology. (L_{gate}=100nm, L_{eff}=70nm, t_{ox}=2.1nm, $V_{t(lin)}$= 0.4V @ I_{DS}=100nA*W/L @ T=27°C)

decreased, the $V_{DS}=V_{DD}$ threshold voltage ($V_{t(sat)}$) for PD/SOI *same-device* T-scaling increases at a lower rate than for bulk-Si due to the increasing $V_{BS}(T)$, described in Chapter 2, thus enhancing the SOI performance advantage for this T-scaling option. In general, with a controlled parasitic BJT, low-T PD/SOI CMOS can provide relief from the I_{on}/I_{off} paradigm at typical operating T, allowing exploitation of the beneficial FB effects without excessive I_{off}.

5.2 Anomalous Drain Current at Low T: New BJT Effect

The UFSOI [Fos99] model-predicted I_{DS}-V_{GS} subthreshold characteristics for an FB PD/SOI nMOSFET (L_{eff}=70nm, t_{ox}=2.1nm, t_{SOI}=100nm, t_{BOX}=200nm, $V_{t(lin)}$=0.4V @ I_{DS}=100nA*W/L @ T=27°C) at V_{DS} = 1.5V are shown in Fig. 5.2 for T varying from 85°C to -100°C. As T is decreased below 0°C, the FB $V_{BS}(T)$ increases such that a significant parasitic lateral npn BJT current {$I_{BJT}(T) \propto \exp(qV_{BS}(T)/nkT)$} is induced. The predicted channel (I_{MOS}) and parasitic BJT (I_{BJT}) current components constituting I_{DS} at T = -100°C are superimposed in Fig. 5.2; they reveal that I_{off} shifts from being I_{MOS}-controlled to I_{BJT}-controlled at low T. Carrier-injection mechanisms (impact ionization, GIDL, and tunneling, the latter two of which become more prevalent as T is decreased) drive the parasitic BJT and hence can control I_{off}. Experimental evidence of such an anomalous I_{DS} at low T, corroborating the predicted increasing $V_{BS}(T)$ (kink effect) and the BJT effect evident in Fig.5.2, is given by in the measured I_{DS}-V_{GS} subthreshold characteristics in Fig.5.3 for an FB PD/SOI nMOSFET (L_{gate}=100nm). The characteristics also depict the expected improvement in subthreshold slope and mobility for decreasing

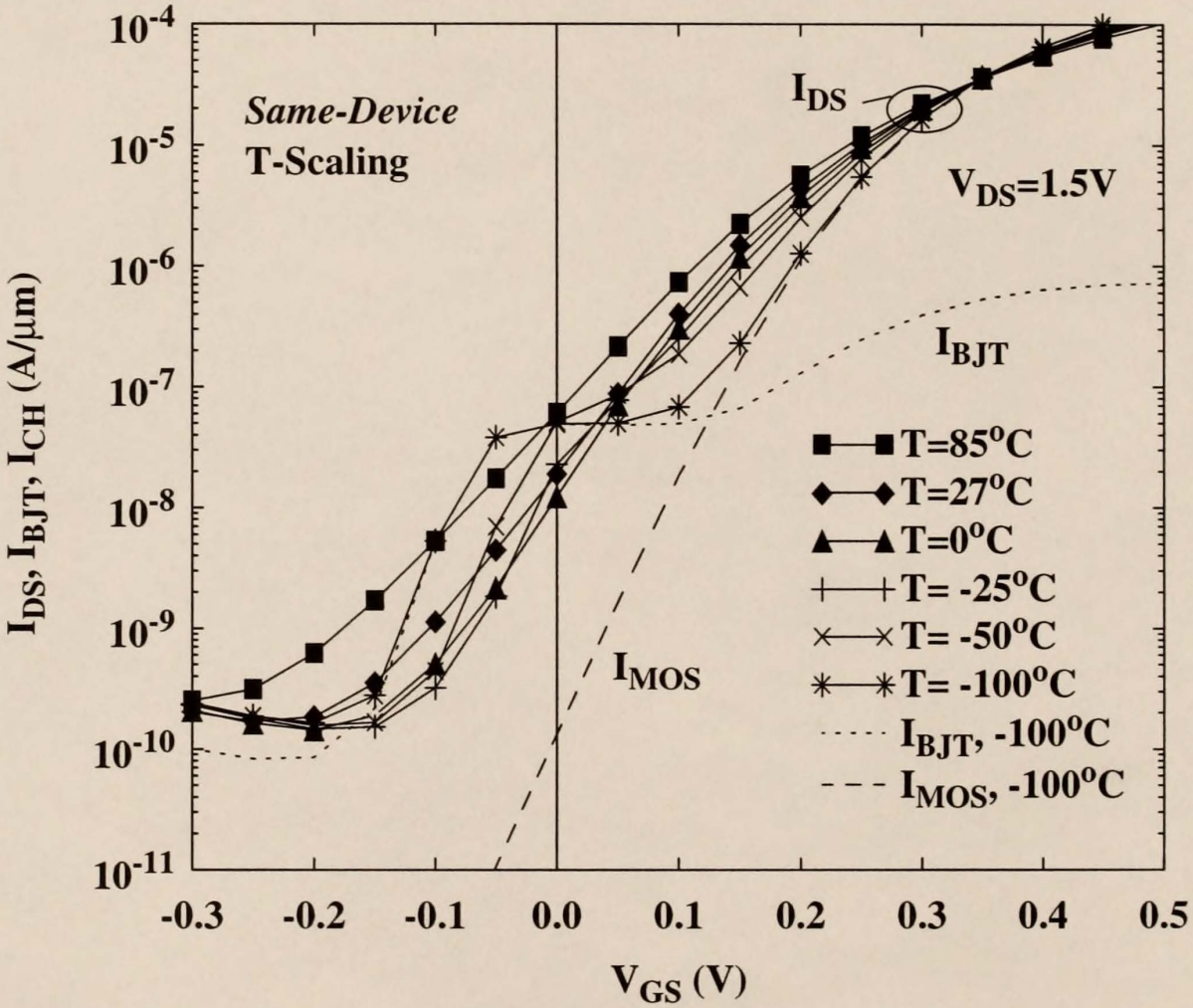


Figure 5.2 Predicted I_{DS}-V_{GS} for PD/SOI as a function of T.
UFSOI-predicted saturated subthreshold I_{DS}-V_{GS} as a function of T, revealing significant parasitic bipolar action at low temperatures. I_{off} shifts from I_{MOS}-controlled to I_{BJT}-controlled at low temperatures. (L_{gate}=100nm, L_{eff}=70nm, t_{ox}=2.1nm, $V_{t(lin)}$= 0.4V @ I_{DS}=100nA*W/L @ T=27°C)

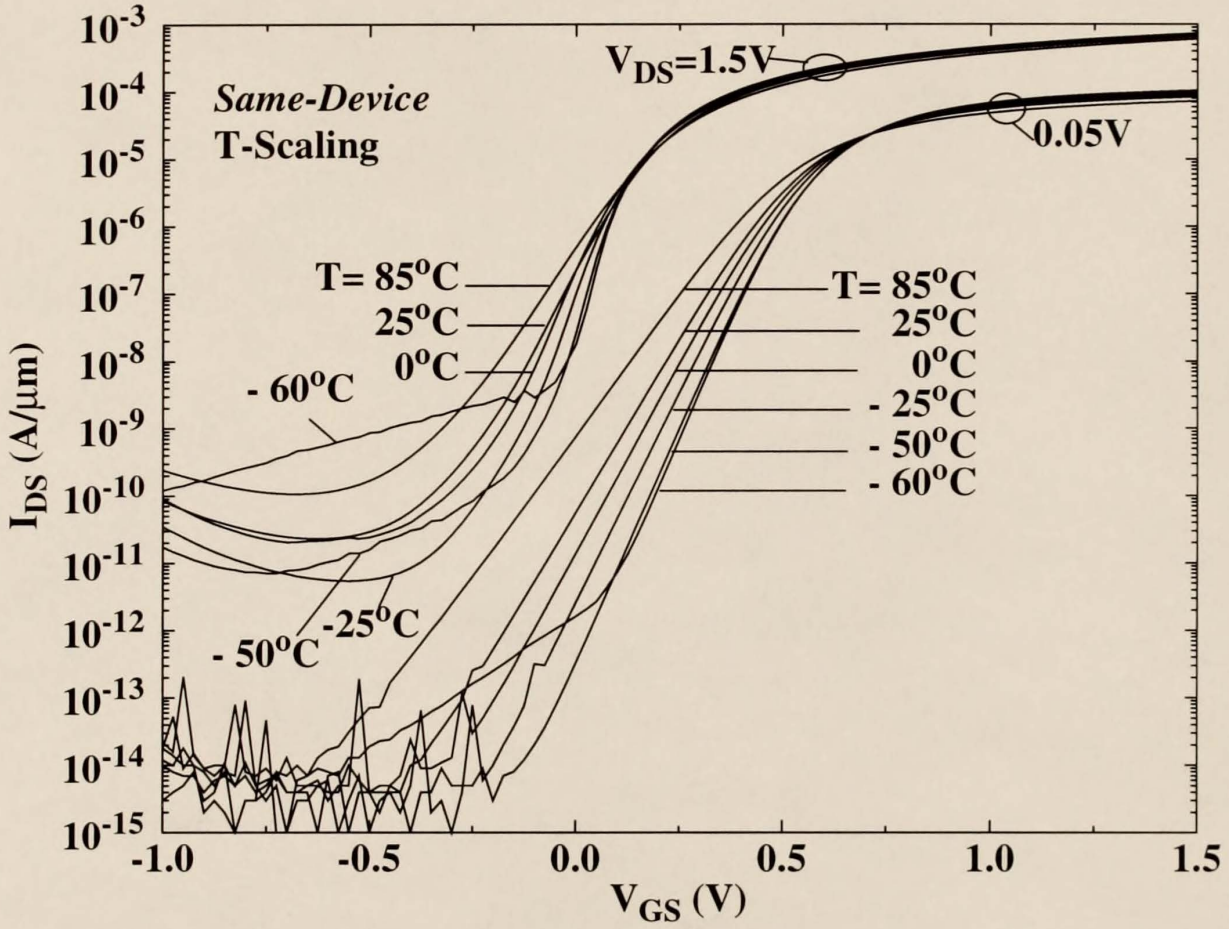


Figure 5.3 Measured I_{DS}-V_{GS} for L_{gate}=100nm PD/SOI as a function of T. Measured subthreshold I_{DS}-V_{GS} [Pel00] as a function of T for a PD/SOI nMOSFET revealing an anomalous increasing I_{DS} component below -25°C and an increasing FB kink effect for decreasing T, corroborating the negative-T coefficient of V_{BS}(T) predicted in [4].

T. Further evidence that the anomalous I_{DS} near and below I_{off} is enhanced BJT transport current from the parasitic lateral npn device is shown in the measured I_{DS}-V_{GS} subthreshold characteristics of Fig. 5.4 for an FB PD/SOI nMOSFET with an increased gate length (L_{gate}=250nm). The increased L_{gate} implies an increased base width for the lateral npn device which lowers its carrier-transport current and thus reduces the magnitude of anomalous I_{DS} current near and below I_{off} as can be seen in the -60°C and -50°C T curves of Fig. 5.4 when compared to the same T curves of Fig. 5.3.

5.3 Revised Gate Control of the BJT Model

With the parasitic BJT transport identified as the anomalous current controlling I_{off} at low T, modeling the dependence of I_{BJT} on V_{GS}, as expressed by [Kri96]

$$I_{BJT}(V_{GS}, x) = \frac{qA_s D n_i^2 \exp\left(\frac{V_{BS}}{V_T}\right)}{\int_0^{L_{BJT}} p(V_{GS}, x, y)dy} \tag{5.1}$$

where A_s is the source sidewall area, D is the diffusion coefficient, V_T is the thermal voltage, and L_{BJT} is the effective base width of the BJT. The integral of the majority hole density in the denominator of (5.1) (which for low injection is the Gummel number), is essential for accurately describing the BJT behavior at low T near and below the I_{off} condition. In Fig. 5.5 as V_{GS} is decreased through 0V, the PD/SOI nMOSFET changes from a strongly inverted condition to a weak-inversion/depleted

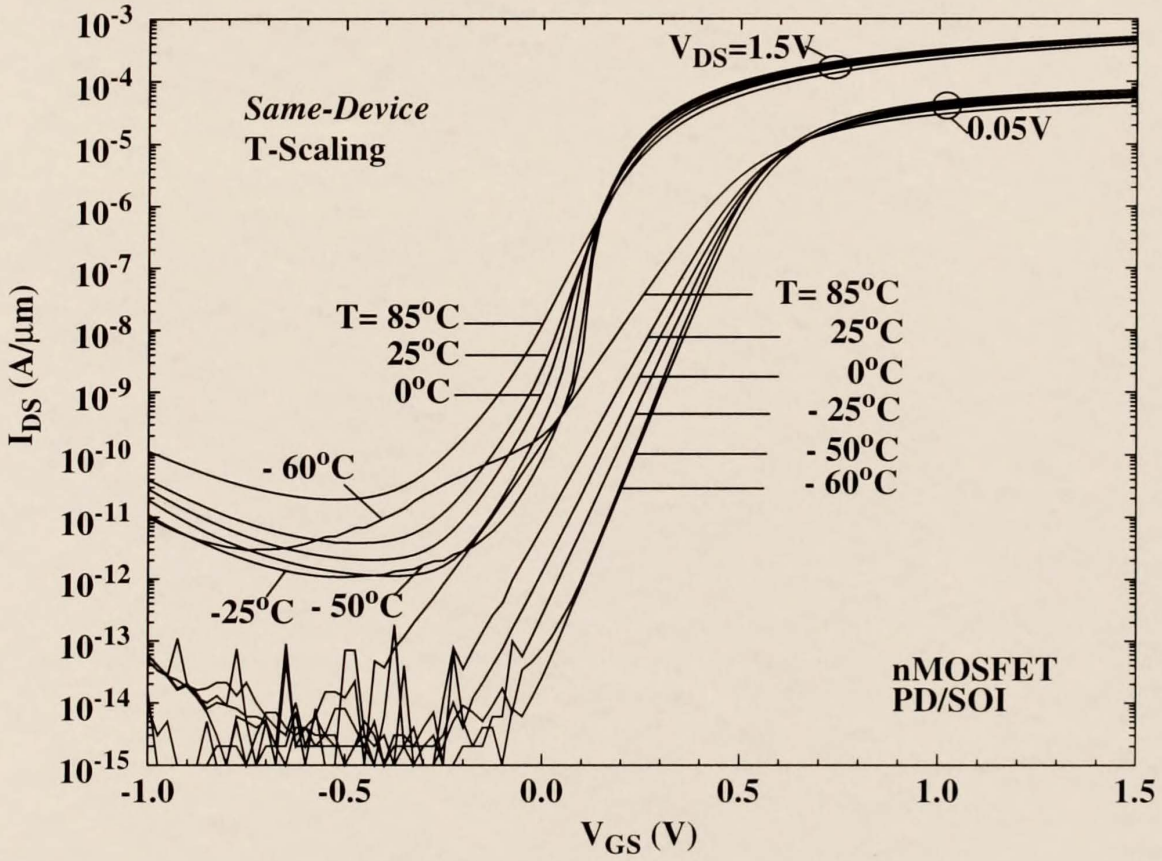


Figure 5.4 Measured I_{DS}-V_{GS} for L_{gate}=250nm PD/SOI as a function of T. Measured subthreshold I_{DS}-V_{GS} [Pel00] as a function of T for a PD/SOI nMOSFET with an increase channel length revealing a reduced anomalous I_{DS} component below -25°C, further corroborating the assertion that the anomalous current is from the parasitic lateral npn device.

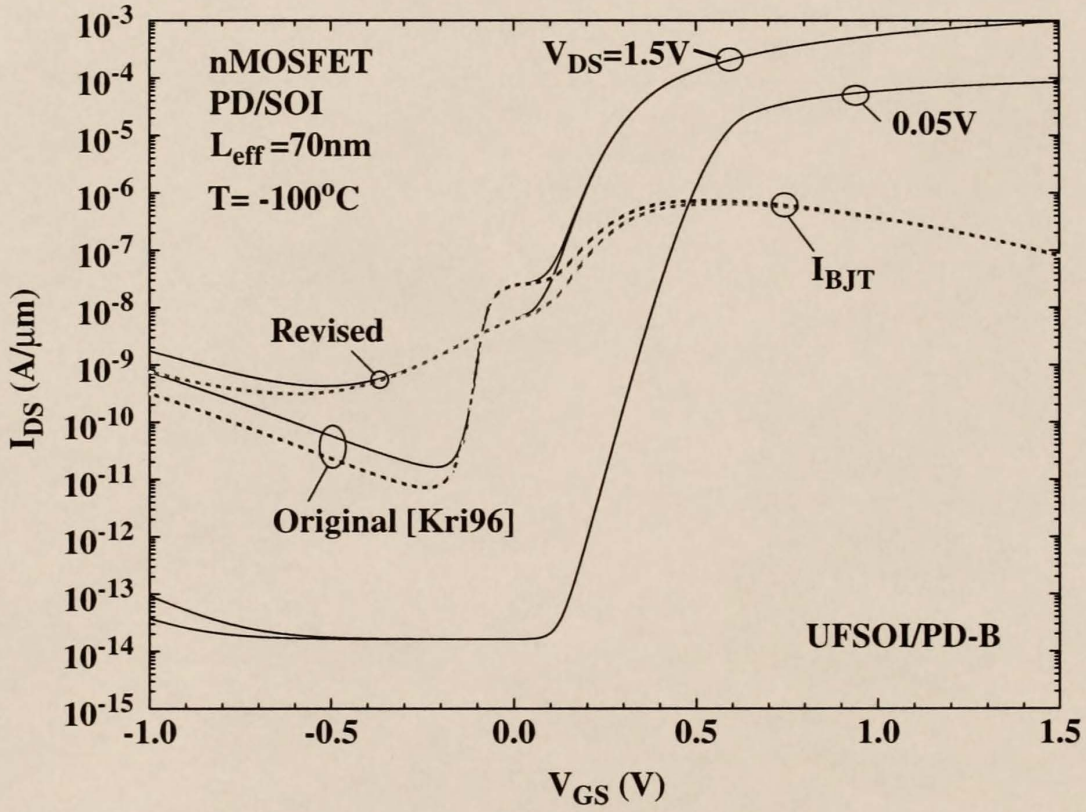


Figure 5.5 Revised BJT($\psi_{sf}(V_{GS})$) model.

condition, which lowers the inversion charge density while increasing the majority-carrier density in the channel region, in accord with the decreasing surface potential. The gate-controlled hole density, which is depth-dependent as defined by [Kri96]

$$p(V_{GS}, x) \cong N_{BL} \exp\left(-\frac{(\psi(V_{GS}, x) - V_{BS})}{V_T}\right) \quad , \tag{5.2}$$

controls the integral in (5.1) and hence determines the magnitude and behavior of I_{BJT}.

The potential variation $\psi(V_{GS},x)$ (where $\psi(V_{GS},x)$-V_{BS} is the effective band bending at the source) in (5.2) is approximated by a linear function of surface potential (ψ_{sf}), which varies from V_{BS} in accumulation to ψ_{sfS} in strong inversion. In [Kri96], the model formalism of the parasitic BJT utilizes the ψ_{sf} at the source of the MOSFET at each bias point, but does not iterate/update the solution based on the influence of the BJT's transport mechanisms. This approximation was retained due to numerical and run-time implications of the parasitic device. To ensure a smooth transition across the moderate-inversion boundaries and to improve the physical relationship between the gate voltage and the surface potential, the $\psi_{sf}(V_{GS})$ dependence is refined to be

$$\psi_{sf} = \frac{\psi_{sfS}}{1 + \exp\left[\frac{-(V_{GS} - V_{ref})}{\Delta V}\right]} + \frac{V_{BS}}{1 + \exp\left[\frac{(V_{GS} - V_{ref})}{\Delta V}\right]} \tag{5.3}$$

where V_{ref} is the reference voltage of the smoothing function given by $(V_{FB}+\overline{V}_{BS}+V_{TS})/2$, $\overline{V}_{BS}$ is an average value of V_{BS}, as in [Kri96], and ΔV defines

the slope of the transition of ψ_{sf}, which is given by $[V_{TW}-(V_{FB}+\overline{V}_{BS})]$. Fig. 5.6 shows the revised ψ_{sf} smoothing function in contrast to the original equation (5.15) of [Kri96]. Thus, through the gate-controlled majority carrier density modeling, the parasitic BJT is physically coupled to the MOS-controlled charge in the UFSOI models.

5.3.1 BJT Current Insight at Low T

To gain further insight into the behavior of the drain current at low T, an analytical expression is derived which includes the generation currents driving the parasitic BJT current. At the DC condition, the drain current is given by

$$I_{DS} = I_{MOS} + I_{BJT} \tag{5.4}$$

where $I_{BJT}=\beta I_R=\beta I_G$, since $I_R=I_G$ for DC conditions in the FB device. The generation currents (I_G) include impact ionization ($I_{Gi}=(M-1)I_{DS}$), GIDL (I_{GIDL}), gate (I_{gate}) and junction tunneling (I_{tun}), and thermal (I_{Gt}):

$$I_{DS} = I_{MOS} + \beta[(M-1)I_{DS} + I_{GIDL} + I_{gate} + I_{tun} + I_{Gt}] \tag{5.5}$$

which when simplified gives

$$I_{DS} = \frac{I_{MOS} + \beta[I_{GIDL} + I_{gate} + I_{tun} + I_{Gt}]}{1 - \beta(M-1)} \tag{5.6}$$

with $\beta=I_{BJT}/I_R$. (Note that β is not modeled explicitly in UFSOI/PD-B.) At low T, near and below I_{off}, the elevated $V_{BS}(T)$ increases the BJT current such that the drain current (5.5) becomes

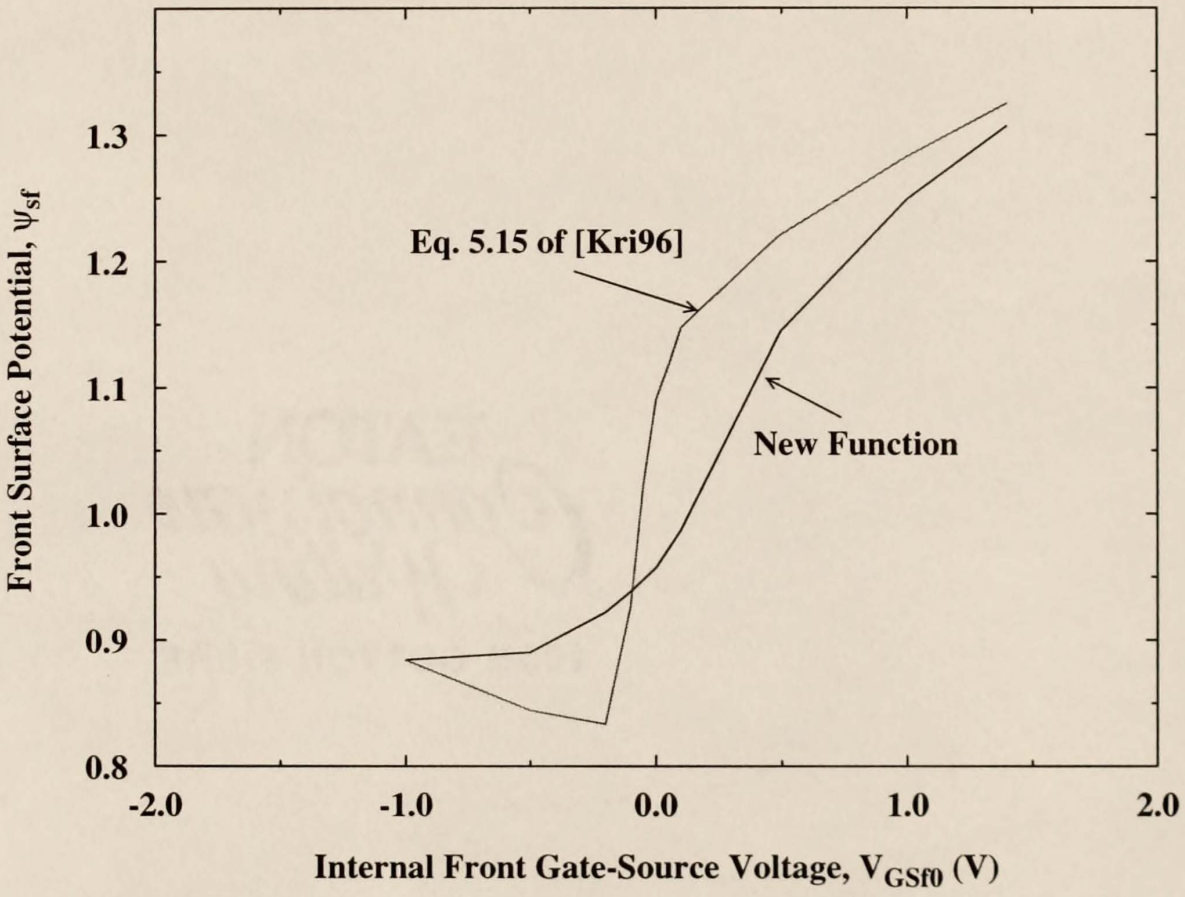


Figure 5.6 Revised ψ_{sf} Smoothing Function, T=-100C, Leff=70nm.

$$I_{DS} = I_{MOS} + I_{BJT} \approx I_{BJT} \tag{5.7}$$

with the I_{GIDL} term in (5.6) being the predominant driver of the BJT.

5.3.2 Revised Subthreshold Characteristics as a Function of T

Using the revised BJT($\psi_{sf}(V_{GS})$) model, the upgraded UFSOI-predicted subthreshold I_{DS}-V_{GS} characteristics versus T are shown in Fig. 5.7. The new model predictions are in better agreement with the measured results of Fig. 5.3, reflecting the anomalous I_{DS} trends more consistently at and below the I_{off} condition.

5.4 Impact of Low-T BJT Effect on Off-State Current and IDDQ

Figure 5.8 shows the predicted I_{off} as a function of T for the PD/SOI nMOSFET characterized in Fig. 5.7. The results reveal a decreasing-I_{off} trend from 85°C through -25°C, and then an increasing-I_{off} trend below 0°C until I_{off} virtually saturates (due to BJT high injection and β rolloff) near -50°C; the minimum I_{off} occurs near -25°C. The constituent I_{MOS} and I_{BJT} components of $I_{off}(T)$ are superimposed in Fig. 5.8; they exhibit a crossover point near where I_{off} is minimum. IDDQ (V_{DD} supply current Quiescent) chip-level test results, which measure the DC leakage current of the CMOS logic gates, are shown in Fig. 5.9 as a function of T. The IDDQ data were taken from a test chip fabricated in a 1.8V, PD/SOI technology (L_{eff}=120nm, t_{ox}=3.5nm) [All99] and a counterpart bulk-Si technology, with V_{DD}=1.7V. The chip consists of various storage macros (SRAMs), CRAs, RLFs, noise experiments, and other custom-design structures, all powered on when the

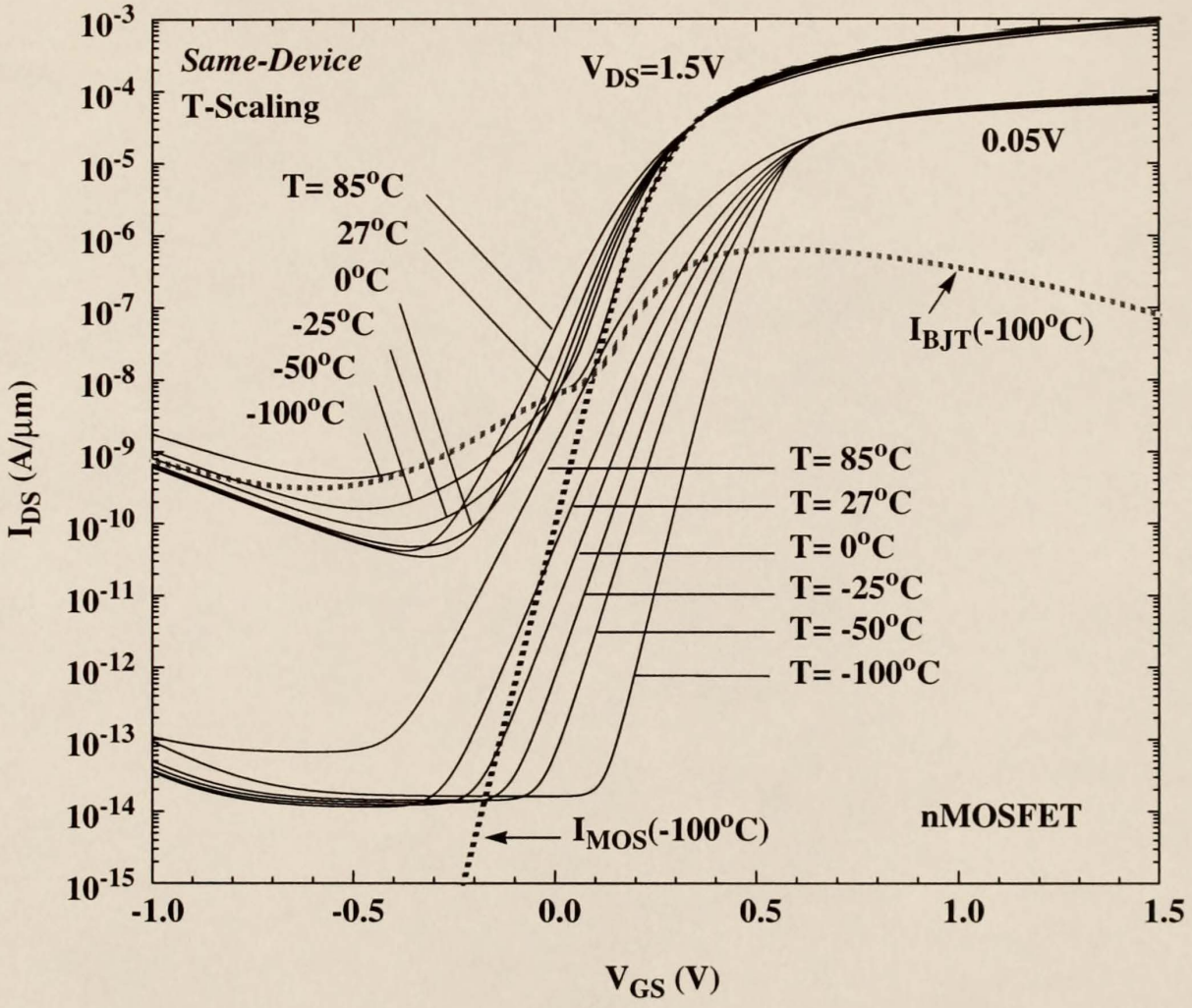


Figure 5.7 Revised I_{DS}-V_{GS} for PD/SOI as a function of T with new BJT model. Revised UFSOI subthreshold I_{DS}-V_{GS} as a function of T, depicting better agreement with the measured results of Fig. 5.3. (L_{gate}=100nm, L_{eff}=70nm, t_{ox}=2.1nm, $V_{t(lin)}$= 0.4V @ I_{DS}=100nA*W/L @ T=27°C)

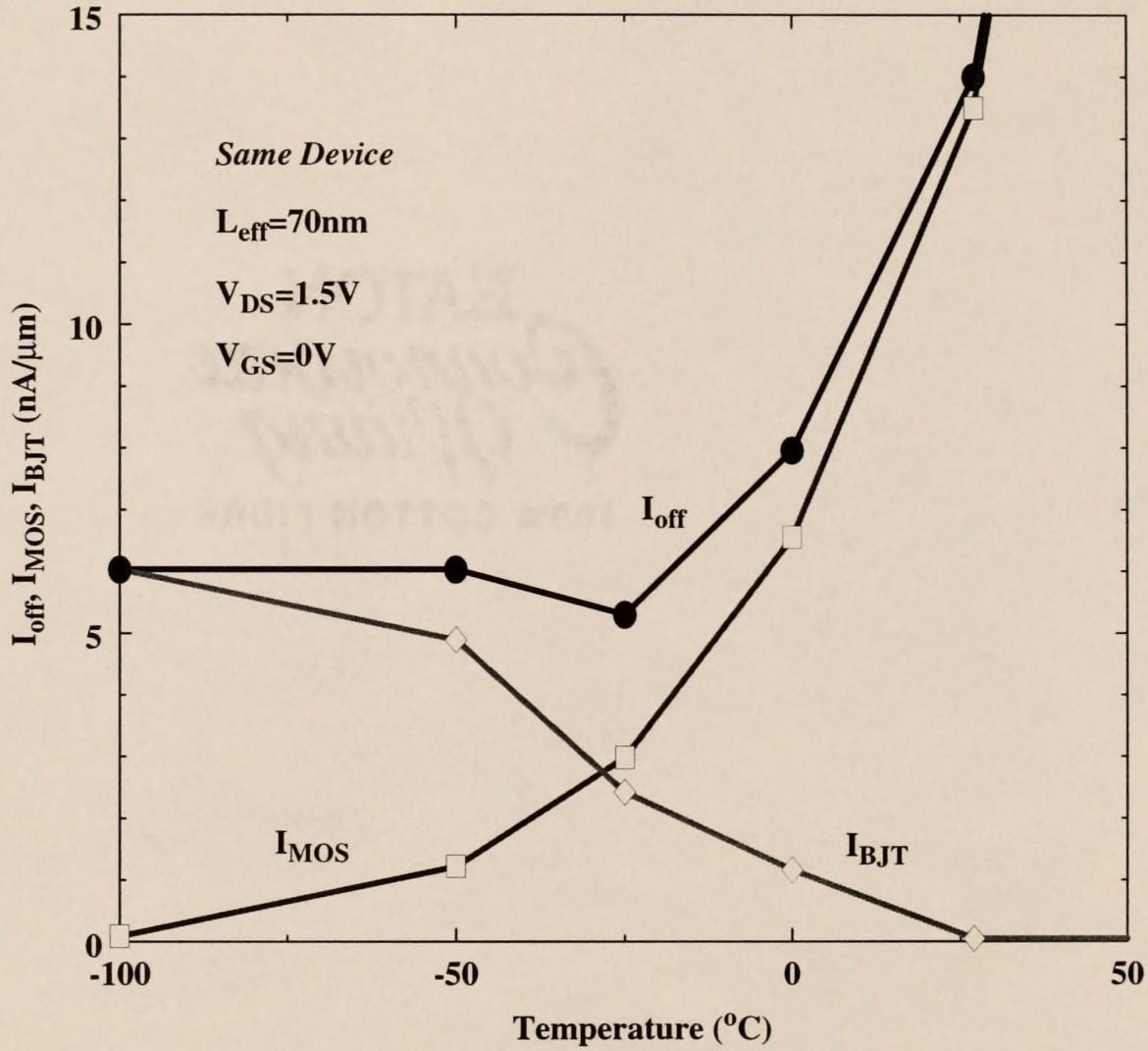


Figure 5.8 Predicted I_{off} as a function of T.

UFSOI-predicted I_{off} as a function of T for the PD/SOI nMOSFET in Fig. 5.7, with the I_{MOS} and I_{BJT} current components at each I_{off}(T) condition superimposed.

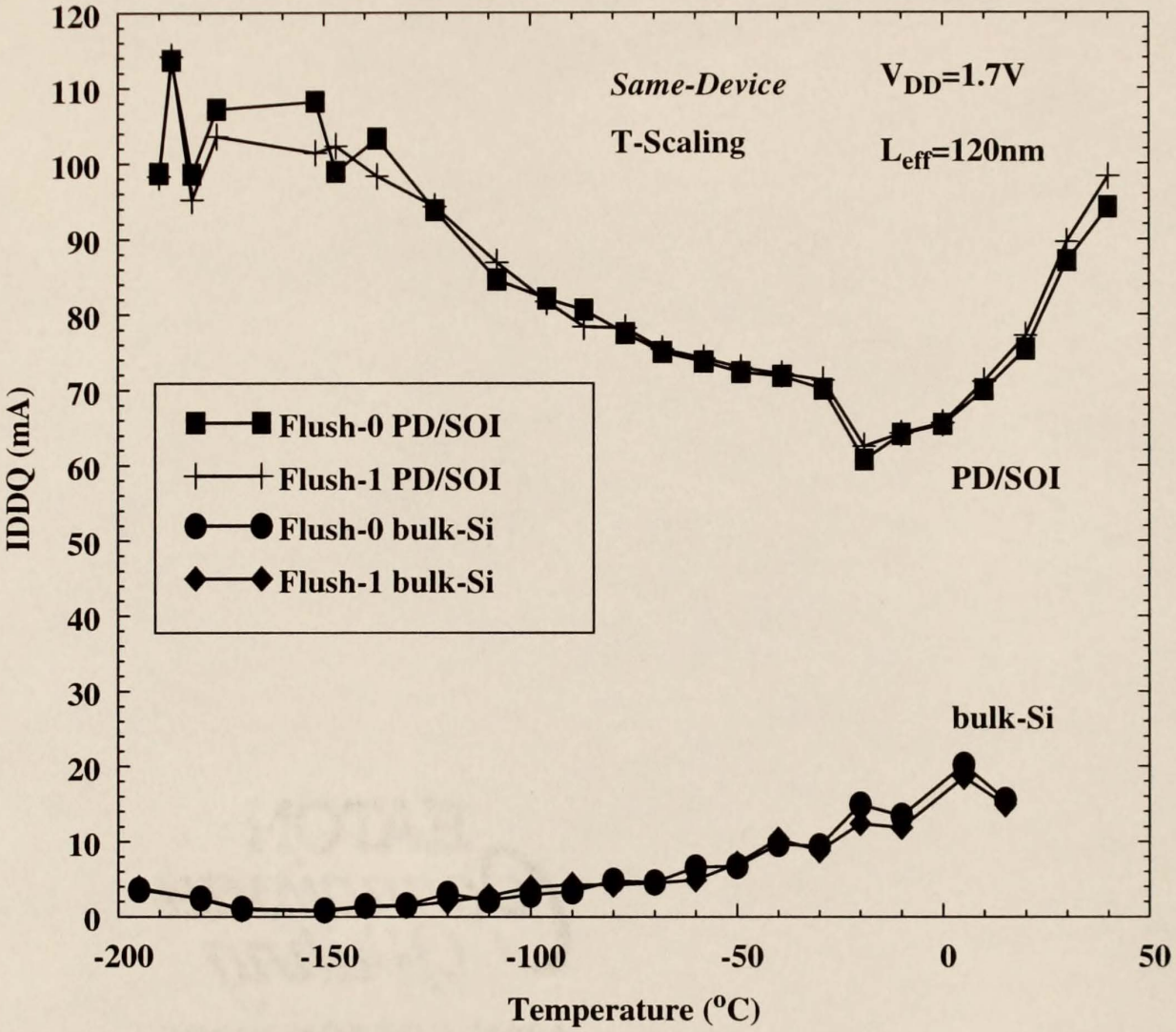


Figure 5.9 Measured IDDQ versus T.

Measured IDDQ versus T for a test chip fabricated in the PD/SOI technology of [All99] and a counterpart bulk-Si technology. The two curves show the IDDQ when all latches are flushed to '0' (FL0) and flushed to '1' (FL1).

IDDQ measurement was taken. The SOI IDDQ results support the predicted results of Fig. 5.8, showing an increasing leakage trend below -20°C.

5.5 *Same-Off-Current* T-Scaling Scenario

5.5.1 Threshold and Performance Impact

The predicted $V_{DS}=V_{DD}$ threshold voltages, $V_{t(sat)}$ (V_{DS}=1.5V), as a function of T for the PD/SOI nMOSFET in Fig. 5.2 and a counterpart bulk-Si device are shown in Fig. 5.10. The *same-I_{off}* T-scaling scenario is achieved by physically lowering $V_{t(sat)}$ via channel-doping adjustment (I_{off} is controlled at the bulk-Si 85°C level). The *same-I_{off}* scaling results for the nominal PD/SOI device show a modest decrease in $V_{t(sat)}$ between 85°C and -25°C, and then an increasing trend below T= -25°C due to the low-T BJT effect. This trend significantly undermines the low-T performance benefit, in contrast to the trend of the bulk-Si counterpart for which $V_{t(sat)}$ monotonically decreases with T. When BJT-suppression techniques are employed (yielding PD-BJTfix/SOI), e.g., increased source (base) recombination current by a bandgap reduction at the source via a deep Ge implantation [Nis97], or by an enhanced surface-recombination via an optimized silicidation to the metallurgical junction [Fos93], the decreasing $V_{t(sat)}$ trend is restored, as shown in Fig. 5.10. However, even with the BJT suppressed, $V_{t(sat)}$ is shown to decrease at a reduced rate when T is decreased, as compared to the bulk-Si counterpart, which also undermines its low-T performance benefit. This is due to the remnant $V_{BS}(T)$ effects that are not completely suppressed by the employed BJT-suppression techniques. Additional FBE suppression techniques such as those suggested in Chapter 2 could

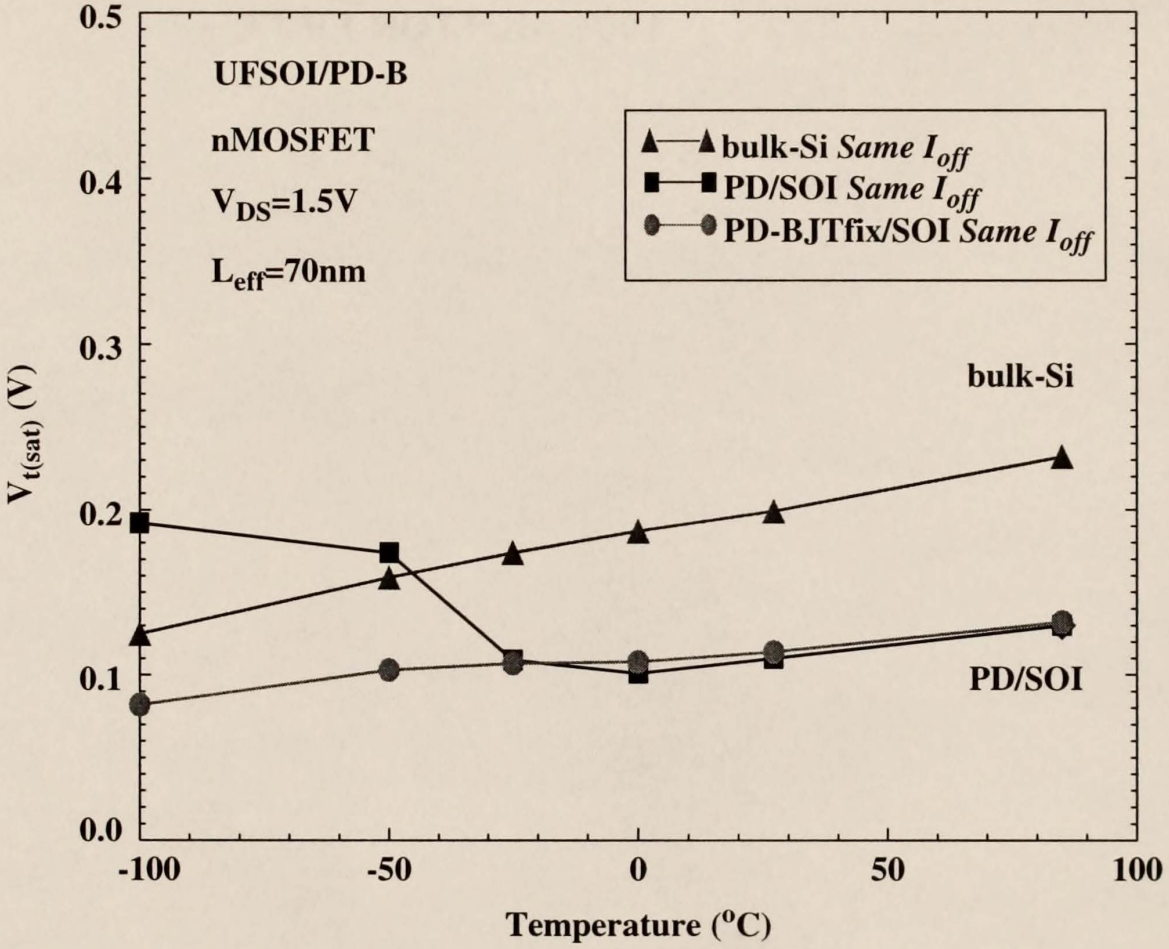


Figure 5.10 Predicted saturated threshold voltage versus T for *same-I_{off}*.
UFSOI-predicted saturated threshold voltage versus T for the PD/SOI nMOSFET in Fig. 5.2 and a counterpart bulk-Si MOSFET for the *same-I_{off}* T-scaling scenarios. The PD/SOI device with its BJT suppressed (PD-BJTfix/SOI) [Nis97], [Fos93] is superimposed for the *same-I_{off}* scenario. (L_{eff}=70nm, t_{ox}=2.1nm, $V_{t(lin)}$=0.4V@ I_{DS}=100nA* W/L@T=27^{o}C)

also be employed to further reduce the adverse $V_{BS}(T)$ effects for this scaling scenario.

The implied impact on CMOS performance is provided by UFSOI ring-oscillator (RO) simulations. The predicted dynamic steady-state RO-delays (τ_{RO}) of a static CMOS inverter for the *same-I_{off}* (I_{off} controlled at the bulk-Si 85°C level) T-scaling scenario of the PD-BJTfix/SOI and counterpart bulk-Si technologies of Fig. 5.10 are shown in Fig. 5.11(a). Note that with the BJT fix, the SOI performance monotonically improves with decreasing T, like that of the bulk-Si technology. The corresponding τ_{RO} performance factor for each technology relative to 85°C is shown in Fig. 5.11(b).

5.6 *Same-Device* T-Scaling Scenario

5.6.1 Threshold Voltage and Performance Impact

The predicted $V_{t(sat)}$'s (V_{DS}=1.5V) as a function of T for the PD/SOI nMOSFET in Fig. 5.2 and a counterpart bulk-Si device are shown for *same-device* T-scaling scenario in Fig. 5.12. The *same-device* T-scaling scenario assumes that there are no changes in the device technology as T changes. The predicted PD/SOI $V_{t(lin)}$ for the *same-device* T-scaling has a negative T coefficient similar to that of the bulk-Si counterpart. However, $V_{t(sat)}$ increases significantly less (-0.4mV/°C compared to -1.07mV/°C for the bulk-Si counterpart) due to $V_{BS}(T)$ increasing as T decreases, and hence implies an enhanced performance benefit at low T. The predicted dynamic steady-state RO-delays (τ_{RO}) of a CMOS inverter for the *same-device* T-scaling scenario of the PD/SOI and counterpart bulk-Si technologies in Fig. 5.12 are shown

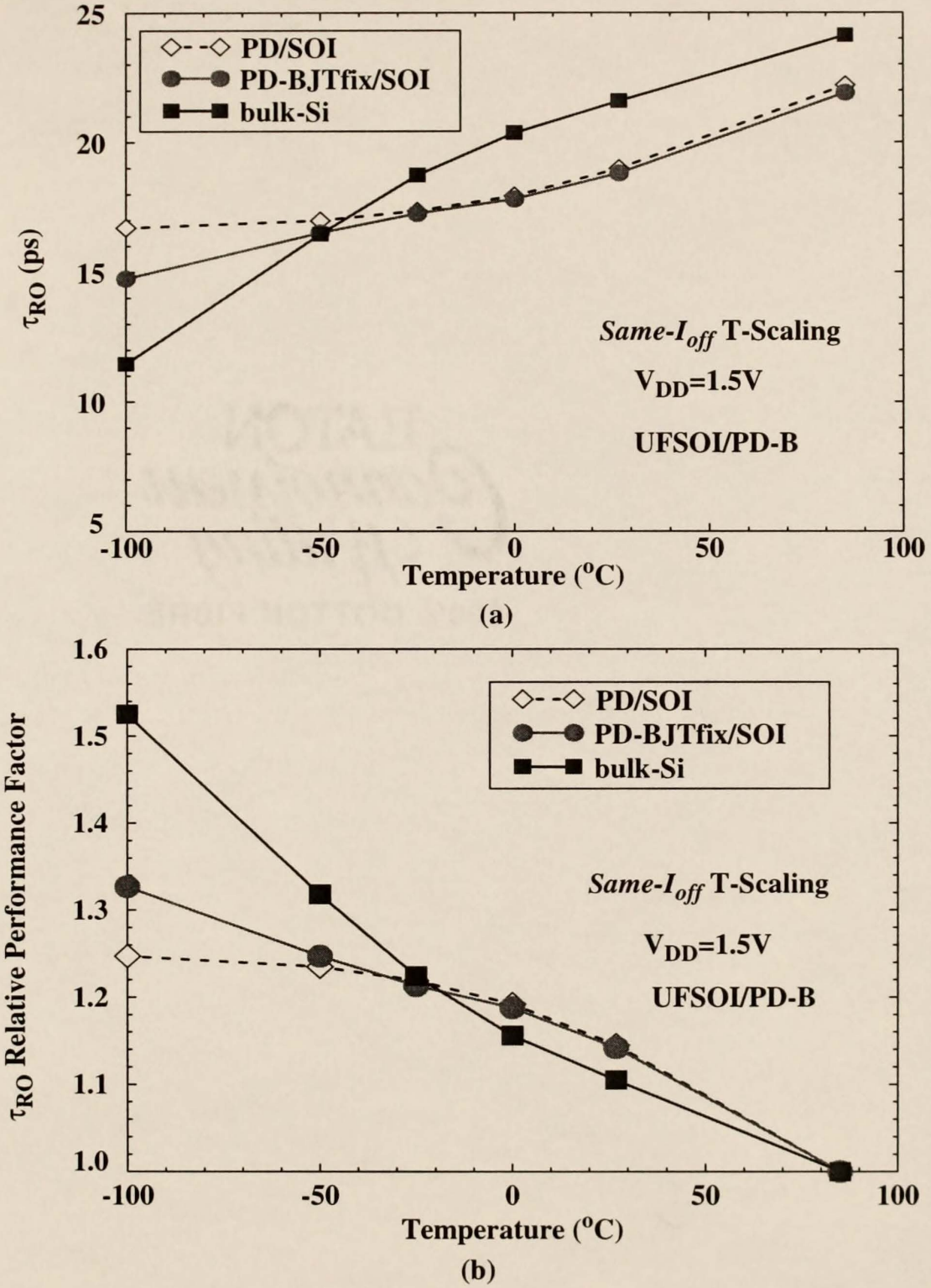


Figure 5.11 RO delays for *same-I_{off}* T-scaling vs. T

Dynamic steady-state CMOS-inverter RO delays (a) for the PD/SOI (w/ and w/o BJT fix) and counterpart bulk-Si technologies for the *same-I_{off}* (bulk-Si 85°C level) T-scaling scenario. (b) The relative (to 85°C) performance for each technology. (L_{eff}=70nm, $V_{t(lin)}$=0.4V @I_{DS}=100nA*W/L @T=27°C, τ_{rise}=τ_{fall} =100ps, W_p/W_n=32/16, C_L=85fF, Per.=1ns, 50% duty cycle)

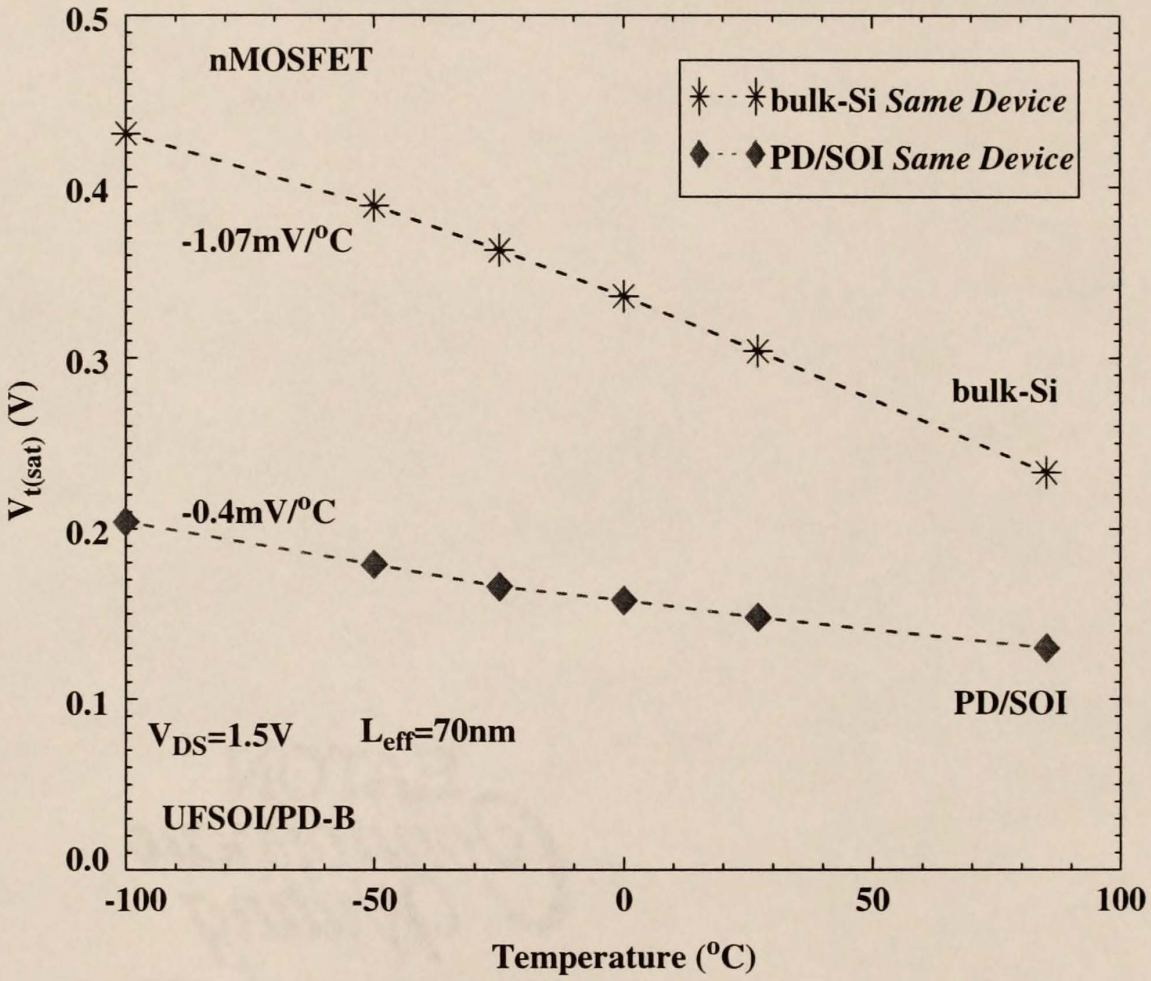


Figure 5.12 Predicted saturated threshold voltage versus T for *same-device*. UFSOI-predicted saturated threshold voltage versus T for the PD/SOI nMOSFET in Fig. 5.2 and a counterpart bulk-Si MOSFET for the *same-device* T-scaling scenarios. (L_{eff}=70nm, t_{ox}=2.1nm, $V_{t(lin)}$=0.4V@ I_{DS}=100nA* W/L@T=27°C)

in Fig. 5.13. The corresponding τ_{RO} performance factor for each technology relative to 85°C is shown in Fig. 5.13(b).

5.7 SOI Benefit at Low T

Both low-T scaling scenarios described in the previous sections provide a significant increase in performance for PD/SOI technologies as the T is reduced. Moreover, the scaling constraint of I_{off} is mitigated allowing an additional degree of freedom to design the device technology in future generations. Dependent on the magnitude of the low-T BJT effect (and FBEs) present in a given device technology, the *same-I_{off}* T-scaling scenario provides the most performance benefit at the expense of increased processing cost and complexity, due to the threshold adjustments that are made for each T-design point. In addition, there may be a technological limit to adjusting (via channel doping) the V_t lower without impacting other key device design features, such as short-channel effects (SCE) and sub-threshold slope (S). On the other hand, the *same-device* T-scaling scenario offers a considerable performance benefit with essentially no additional cost (no changes in the device technology as T is decreased) while exploiting the enhanced FB effects at low T where I_{off} is not an issue.

In general, the performance advantage of PD/SOI over its bulk-Si counterpart is enhanced when the *same-device* T scaling is employed, enabling the exploitation of the FB benefit without the I_{off} problem associated with conventional high-T operation, as noted above. Determining the design point for V_t depends on the criterion for I_{off} in the technology at a given T. However, if the same technology is

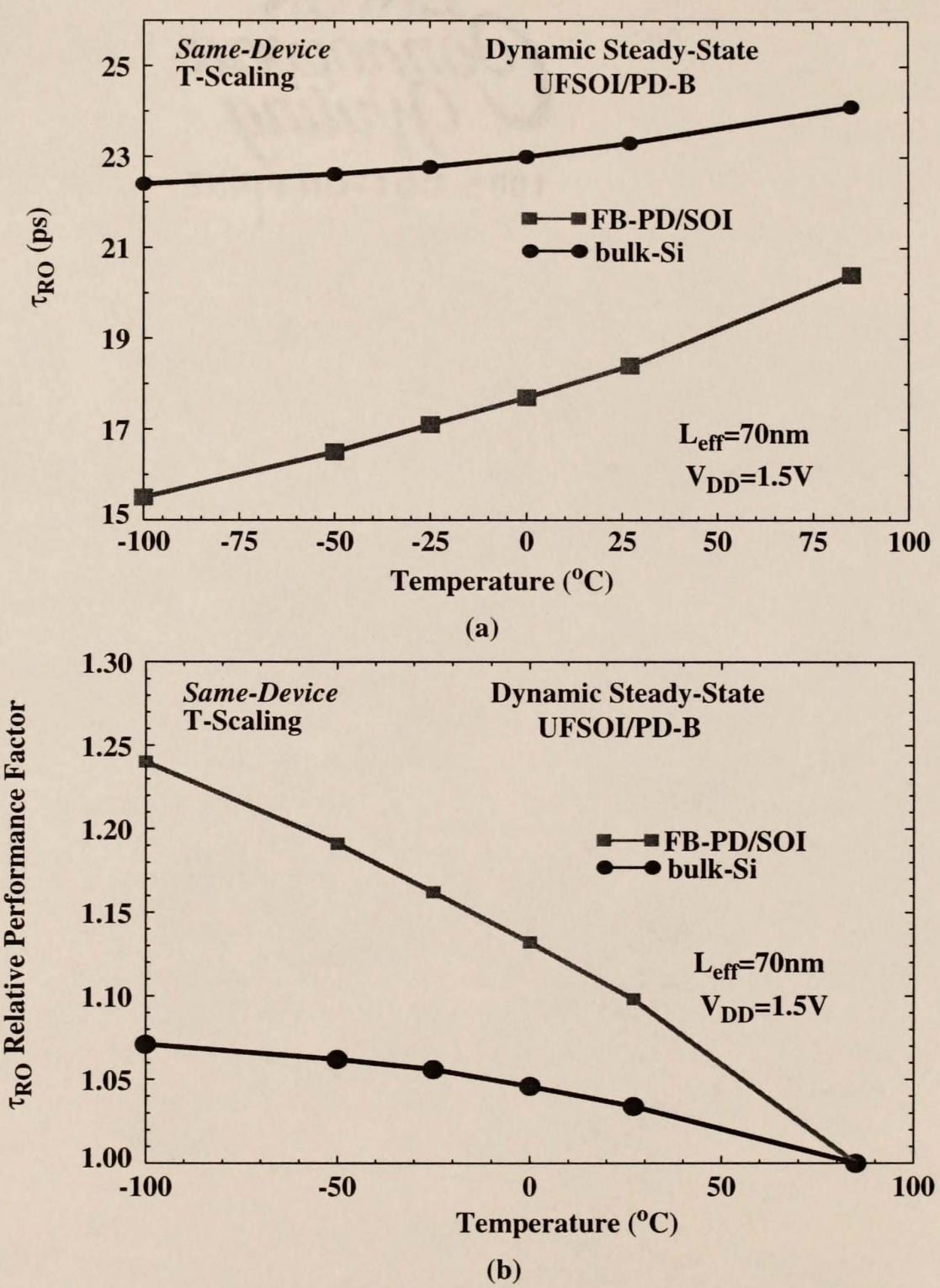


Figure 5.13 RO delays for *same-device* T-scaling vs. T
Dynamic steady-state CMOS-inverter RO delays (a) for the PD/SOI and counterpart bulk-Si technologies for the *same-device* T-scaling scenario. (b) The relative (to 85°C) performance for each technology. (L_{eff}=70nm, $V_{t(lin)}$=0.4V @I_{DS}=100nA*W/L @T=27°C, $\tau_{rise}=\tau_{fall}$ =100ps, W_p/W_n=32/16, C_L=85fF, Per.=1ns, 50% duty cycle)

used at multiple T's, the choice of V_t is more challenging. Since I_{off} increases with increasing T, V_t should be set at the highest operating T level. I_{off} will naturally decrease as T is decreased at the lower operating T level. Alternately, a compromise of the V_t level may be utilized, where V_t is set to achieve an average value of I_{off} at a midrange value of the two operating T's. This will improve the overall delay at both T's, while impacting the static power moderately at the higher operating T.

An added benefit of the *same-device* T-scaling scenario is that if the rate of $V_{BS}(T)$ is increased with decreasing T, the negative T coefficient of $V_{t(sat)}(T)$ will decrease further, possibly becoming positive. This would dramatically improve the performance benefit PD/SOI over its bulk-Si counterpart since $V_{t(sat)}$ could become invariant or even decrease with decreasing T. To achieve this enhanced performance benefit, the source/drain junction characteristics can be adjusted, as suggested in Chapter 2. For example, by improving the ideality (n) towards 1.0 while decreasing the recombination lifetime (increasing I_{RO}), the negative T coefficient of $V_{BS}(T)$ can be significantly increased.

5.8 Conclusions

The behavior of FB PD/SOI CMOS was investigated at low T for two different T-scaling scenarios. A newly recognized low-T off-state BJT effect, which is manifested as an anomalous drain current near and below I_{off} as T decreases, was found to underlie an anomalous I_{DS} current at low V_{GS} that has a significant impact on I_{off} and propagation delays, i.e, τ_{RO}. Measured data for two channel lengths support the predicted behavior at low T including the anomalous I_{DS} current.

Predicted $I_{off}(T)$ as a function of T reveals an increasing trend below a critical T(~ -25°C) and is corroborated with IDDQ chip measurements. The performance benefit of the *same-Ioff* T-scaling scenario is undermined by the negative T coefficient of $V_{BS}(T)$ and the low-T BJT effect; whereas the *same-device* T-scaling scenario affords an improved performance benefit as T decreases, with the possibility of an increased benefit by optimizing the negative coefficient of $V_{BS}(T)$.

CHAPTER 6
SUMMARY AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Summary

The research submitted in this dissertation pertains to the development of physical compact models for PD/SOI and bulk-Si technologies and the analysis and control of unique FB SOI effects that cause instabilities in both device and circuit applications under DC and transient conditions. The utility of the new modeling features was demonstrated while analyzing the FB effects in scaled device and circuit simulations that provided insight in the underlying mechanisms and possible ways to control their detrimental effects without significantly affecting their beneficial effects.

The scalability and viability of PD/SOI CMOS was assessed in Chapter 2 while giving a physically insightful analysis of the FB effect on I_{off}, which tends to be high compared to that of bulk-Si technologies and significantly impacts the nominal design point and performance of a given SOI technology. The analysis indicated that the FB effect on I_{off} can be naturally ameliorated by typical high operating temperatures (T) and increased junction recombination currents. An expression for the temperature dependence of $V_{BS}(T)$ was developed which provides insight into ways to control FB effects and was shown to have a significant negative temperature coefficient that is strongly dependent on the junction characteristics, i.e., ideality and the recombination current coefficient. The impact of using increased

T and I_R as controlling techniques for the FB effect were evaluated in RO inverter circuits and device characteristics which contradicted a negative assessment put forth in the literature by other researchers.

An efficient new characterization methodology to properly analyze hysteresis was developed in Chapter 3, utilizing four fundamental delays of a FB PD/SOI CMOS inverter that were defined. This methodology enables a fundamental understanding of the complex FB dynamics that govern the hysteretic delays and provides the flexibility of analyzing variations in duty cycle and slew rate in any particular inverter circuit. The hysteretic delay analysis revealed the possibility of non-monotonic delays caused by a new dynamic-loading effect that was discovered and described in this Chapter. Hysteresis trends were shown to increase or decrease by adjusting the device structure or by using a proposed *asymmetric design concept.* Moreover, hysteresis was shown to worsen as the technology is scaled. The impacts of dynamic (changing gate load of an inverter chain) and heavy (i.e., long metal lines) loading were investigated, indicating that the methodology is generally applicable. Additional analyses helped to provide insight into a discrepancy in the literature between simulations and measurements showing increasing and/or decreasing hysteretic delays can be designed into a given technology by appropriate device structure adjustments, which suggests the possibility of exploiting the beneficial FB effects or generally controlling hysteresis in specific applications.

In Chapter 4, a new unified (UFSOI/PD-B) modeling capability was implemented to enable performance assessments of bulk-Si CMOS in a stand-alone technology or as a counterpart technology to PD/SOI CMOS. This allows a bulk-Si

counterpart structure to be simulated with exactly the same device design assumptions as the PD/SOI technology, eliminating any ambiguities in device design and structure. With this capability, the performance benefits for contemporary and scaled PD/SOI and bulk-Si technologies were assessed. Insights underlying the benefits of a FB were given and the advantages were shown to diminish for inverter circuits while stacked gate logic circuits were shown to restore the performance advantage the FB PD/SOI technologies. Moreover, at elevated temperatures (T=85^{o}C) the performance benefit over its bulk-Si counterpart improves significantly due to the smaller V_t shift needed to achieve a controlled I_{off} technology, thus mitigating the diminishing performance benefit of scaled technologies. Also, by employing additional optimization techniques (such as, increased I_R or the asymmetric SOI CMOS design concept), further mitigation is possible.

The behavior of FB PD/SOI was investigated at low operating temperatures in Chapter 5, revealing an anomalous drain current near and below the I_{off} condition. This anomalous drain current was shown to be caused by the parasitic lateral BJT device and was corroborated by I-V and IDDQ measurements. The gate dependence of the BJT model was revised to improve its physical accounting of the behavior near and below the I_{off} condition. As T decreases, I_{off} was shown to switch from being controlled by the MOSFET channel current to being controlled by the parasitic BJT current that increases with decreasing T, giving rise to a non-monotonic trend for I_{off} and suggesting a possible limit to the low-T operating range. The impact of threshold voltage and propagation delay (τ_{RO}) for two T-scaling scenarios (*same-device* and *same-I_{off}*) were assessed revealing a significant

performance gain as T is decreased from 85°C to -100°C, a practical range of operating T subject to the cost of the cooling system. The *same-device* T-scaling is the most cost effective scenario, since no process changes are needed as T is decreased while taking advantage of the negative T coefficient of $V_{BS}(T)$; whereas the *same-I_{off}* T-scaling is undermined by $V_{BS}(T)$ and is costly due to the process adjustments needed. Hence, low-T PD/SOI CMOS can provide relief from the I_{on}/I_{off} paradigm at typical operating T, allowing exploitation of the beneficial FB effects without excessive I_{off}.

6.2 Recommendations for Future Work

To preserve the predictive capabilities of the UFSOI models as device technologies are scaled to dimensions (~10nm) near the end of the SIA roadmap, new features/effects should be developed for the models.

For reliable nanometer gate length device characteristics, the models should address gate oxide tunneling since oxide thicknesses below 2nm can experience tunneling currents that are comparable with off-state currents of the technology.

To suppress short-channel effects (SCE), nonuniform doping profiles (halo) near the source/drain junctions are typically used. However, in extremely scaled technologies halo doping concentrations are becoming excessively high (>1e18/cm3). These high doping concentrations gives rise to junction tunneling currents that can be significant as we approach the ned of the roadmap. Although there is an existing reverse bias tunneling accounting in the UFSOI model, there is

no accounting for forward bias tunneling, which can influence the level of V_{BS} and general operation of the MOSFET.

The present GIDL current model should be refined to include the affects of V_{BD}, which may be decreased or enhance depending on the dynamics of the MOSFET. Recent low-T measurements support this hypothesis which indicates that as T decreases, $V_{BS}(T)$ is increased and leads to a debiasing or lowering of V_{BD} (reduced reversed biased). The lower V_{BD} widens the energy bandgap of the drain junction in the GIDL region and thus reduces the level of current generated.

The new unified UFSOI model feature should be extensively exercised as a stand-alone bulk-Si technology and verified with an extensive set of hardware measurements. This valuable feature was mainly used to obtain a bulk-Si counterpart technology to the existing PD/SOI technologies used in this dissertation and not used to assess the scalability and performance issues associated with scaled bulk-Si issues.

Using the hysteresis methodology presented in Chapter 3 to obtain dynamic steady-state delays, the performance advantage analysis of Chapter 4 should be extended to assess the merits of FB PD/SOI in pass-gate circuit, which have been shown to exhibit much higher hysteretic delays than in CMOS inverter circuits.

With the merits of low-T operation described in Chapter 5, an extensive calibration to measured hardware is warranted to assess and verify the revised BJT modeling and the temperature coefficients of the UFSOI model. Also extending the performance impact of low-T operation in stacked- and pass-gate circuits would help to provide a broader assessment of the true merits of operating at low ambient temperatures.

APPENDIX
CONTROL OF FLOATING-BODY EFFECTS BY SOURCE/DRAIN JUNCTION ENGINEERING

Discussion

Another possible technique to suppress the FB effects in PD/SOI devices is to increase the recombination current of the junctions by physically adjusting the structure to increase the junction area. The increased junction area can be achieved by utilizing a proposed PD-t_{gap}/SOI device structure that intentionally separates the source/drain junctions from the buried oxide, as illustrated in Fig. A.1. The separation thickness (t_{gap}) is nominally designed to equal the zero bias depletion width of the source/drain junctions, so that there is no impact (i.e., no increase in the depletion capacitance of the junctions) on the transient performance of the device. t_{gap} will need to be adjusted to accommodate tolerances in the process, doping concentration conditions, and inactive silicon layers near the buried oxide surface.

Medici Analysis

The preliminary Medici [Tec97] results of the source-body junction current flow for a conventional device (with the source/drain junctions abutted to the buried oxide) and that of the proposed PD-t_{gap}/SOI device (with t_{gap}=50nm) structure are shown in Figs. A.2 and A.3, respectfully. The Medici simulations assume default material (τ_n=τ_p=1e-7s), insulator, and contact values. The silicon film thickness (t_{SOI}) is assumed to be 200nm. Fig. A.3 depicts the current flow lines for the PD-t_{gap}/SOI device structure, which assumes that its source/drain junctions

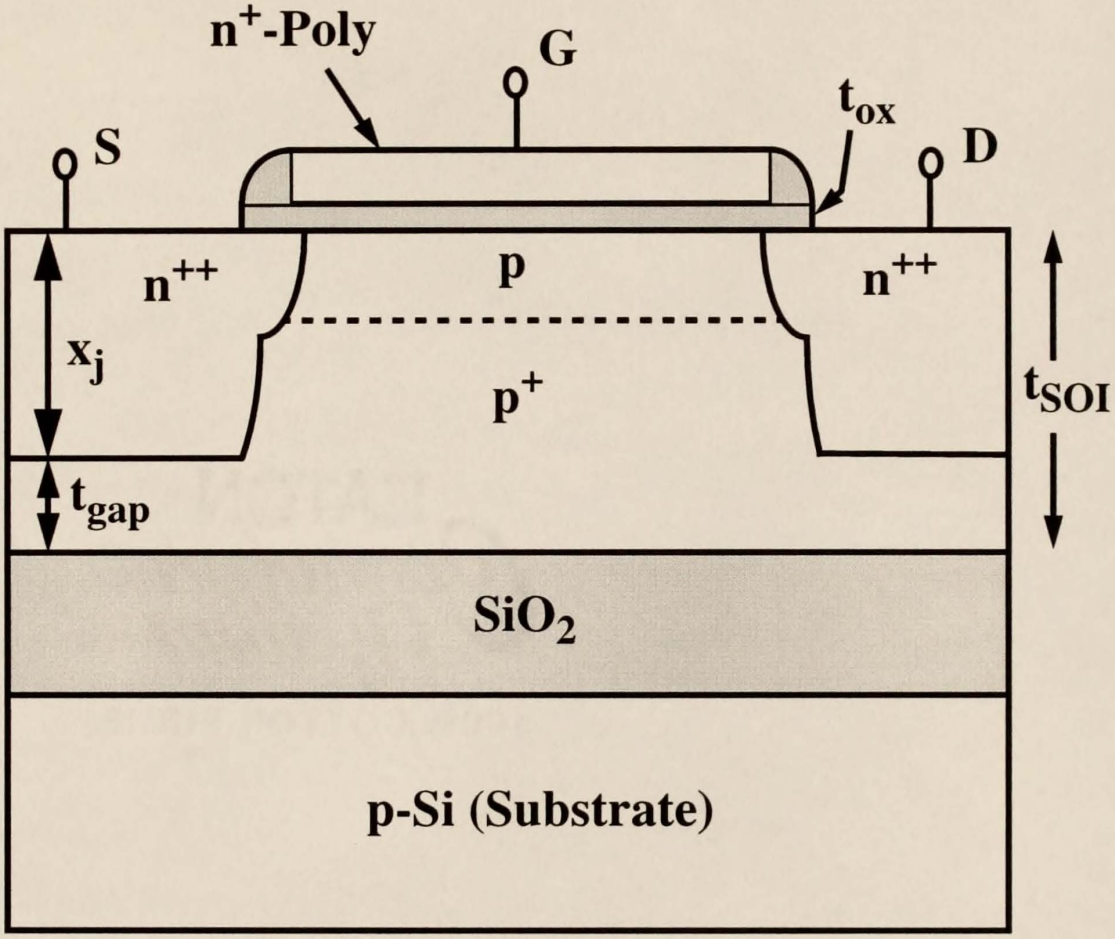


Figure A.1 Schematic cross-section of the PD-t_{gap}/SOI nMOSFET.

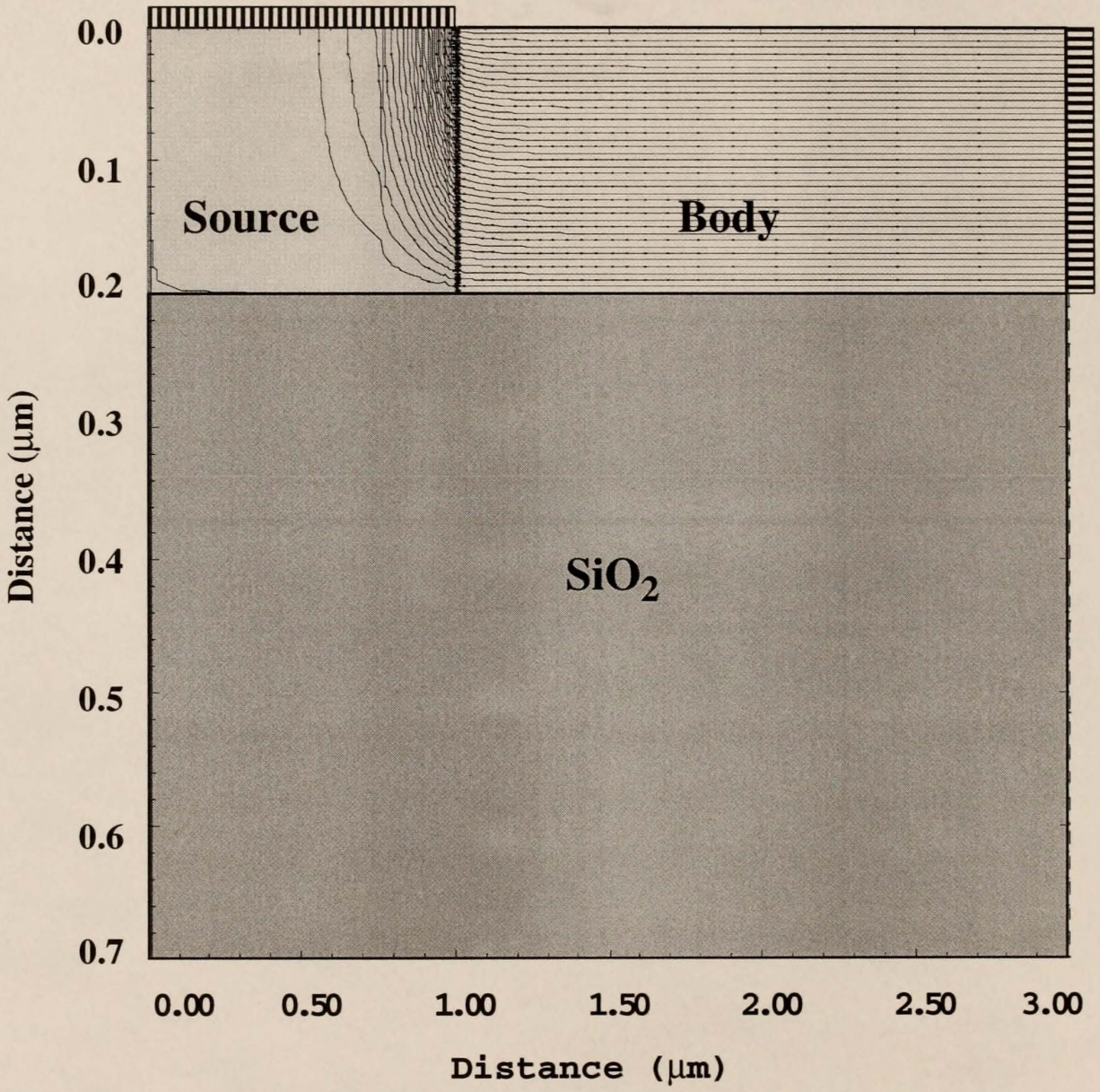


Figure A.2 Medici current flow of an abutted source junction to the buried oxide.
(t_{SOI}=200nm, x_j=200nm)

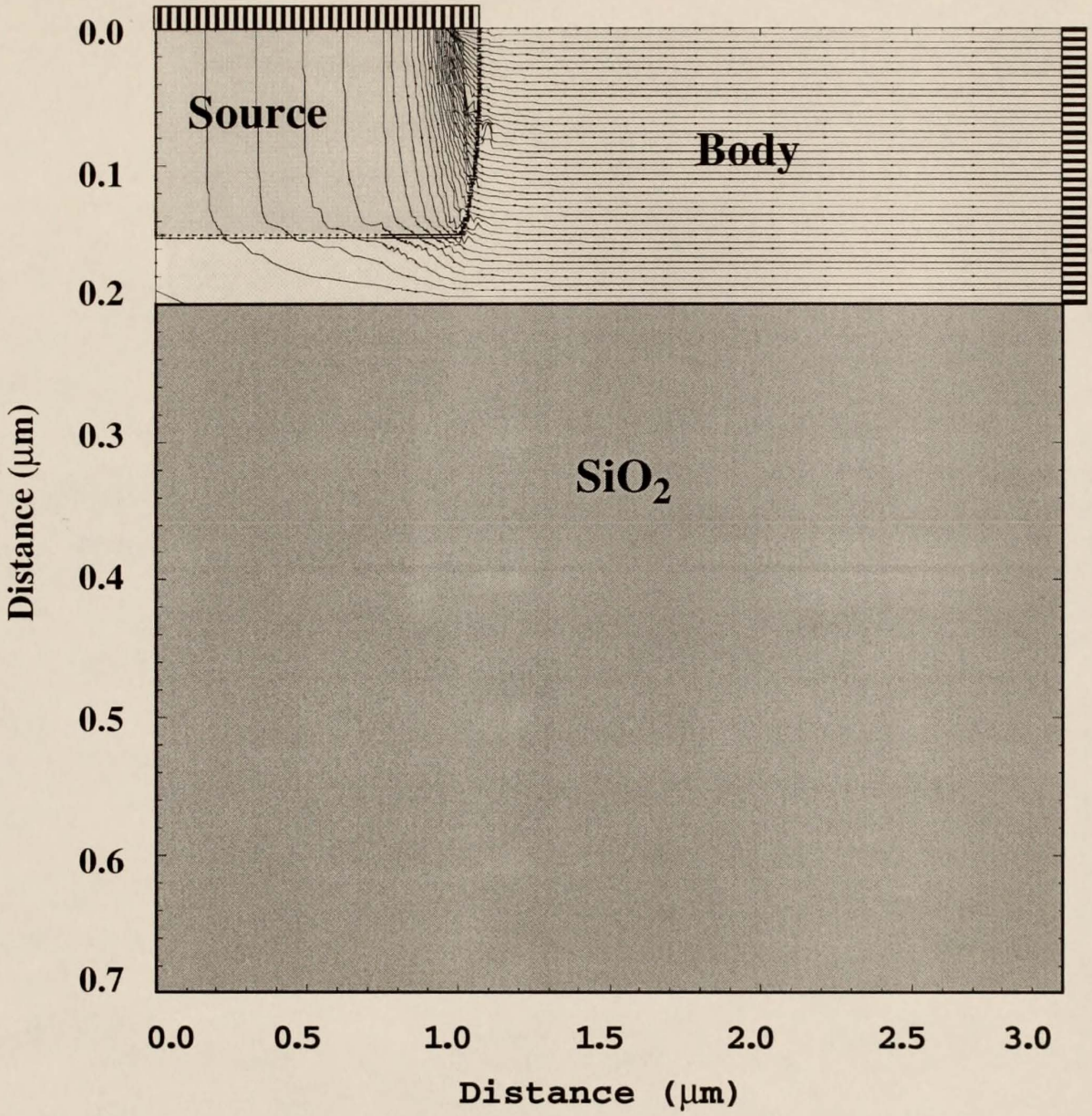


Figure A.3 Medici current flow of the PD-t_{gap}/SOI device structure 50nm gap between the source junction and the buried oxide. (t_{SOI}=200nm, x_j=150nm)

extend vertically to 150nm, intentionally forming a gap between the junctions and the buried oxide. The separation of the junction from the buried oxide allows the bottom portion of the junction to become active, providing additional recombination current flow and thus a more efficient junction to remove the excess majority carriers in the floating body. The efficiency of the exposed junction area will depend on the conductivity of the gap region which will experience current crowding and should be considered in the refinement of the compact modeling for this option. In addition, the gap exposes the oxide-silicon interface below the junctions which also provides an extra recombination current component in the form of a high surface recombination velocity [Col97], [Cri95]. Moreover, the extra area under the junctions can also contribute to an additional recombination current component contingent on the lifetime in that region and a beneficial diffusion capacitance, due to the large volume of stored charge while under a forward bias condition, that tends to suppress transient FB effects and soft-error upsets. And, if the exposed silicon near the top surface of the BOX is heavily damaged, either by the BOX formation processes or by the subsequent device technology processes, the carrier lifetime can be extremely low, further enhancing the recombination and suppressing the FB effects.

The predicted I-V curves for both device structures are shown in Fig. A.4. The results clearly indicated that the PD-t_{gap}/SOI device structure (x_j=150nm, t_{gap}=50nm) provides increased recombination current as compared to the abutted device structure (x_j=200nm). This would imply that the PD-t_{gap}/SOI structure would support a higher recombination current flow at a lower V_{BS} forward bias (lower FB voltage) which is beneficial in suppressing the FB effects in PD/SOI technologies.

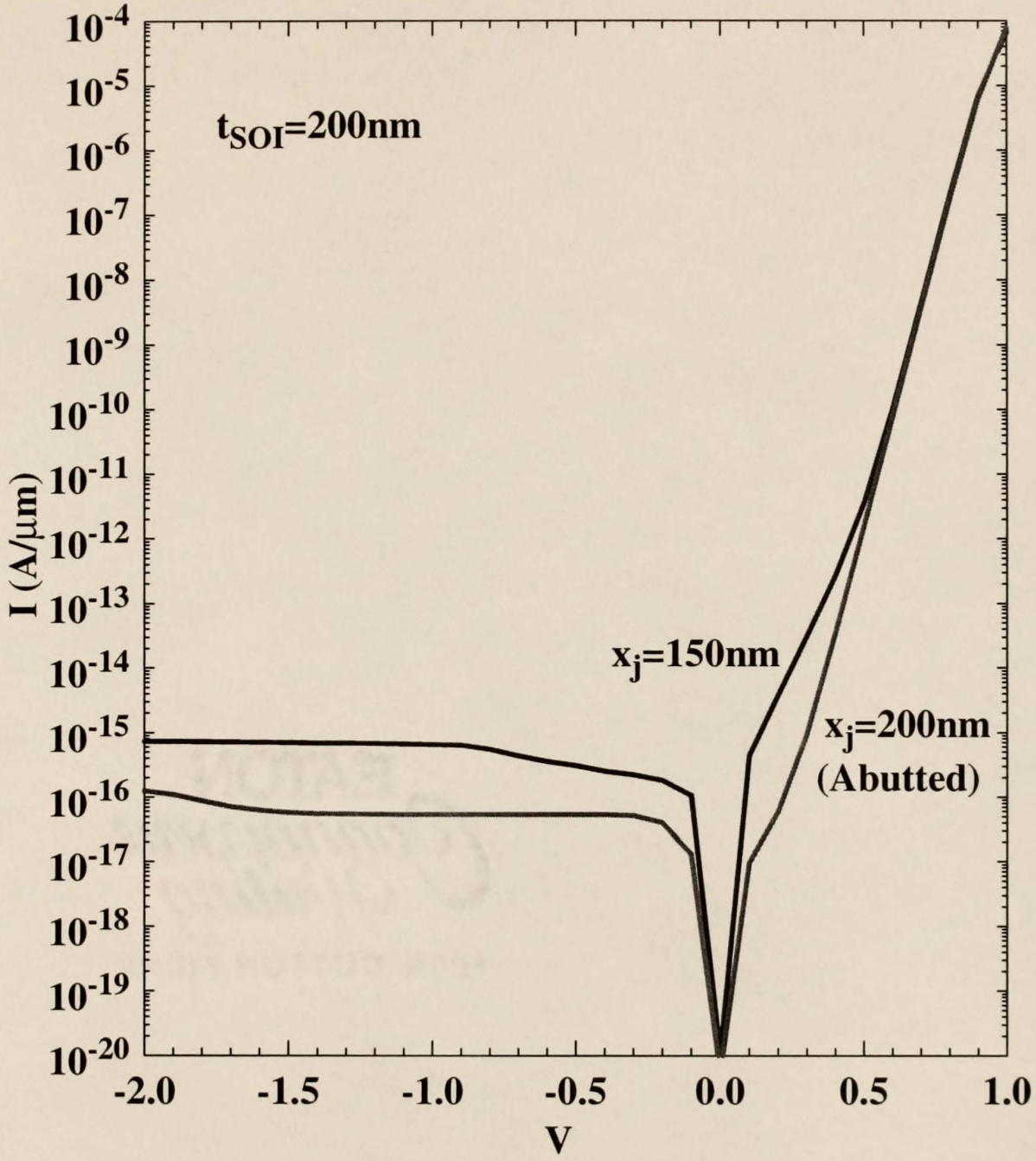


Figure A.4 Medici current-voltage for abutted and x_j defined source junction. PD-t_{gap}/SOI structure assumes an intentional gap between the junction and the buried oxide. (t_{SOI}=200nm, x_j=200nm (abutted) and x_j=150nm (50nm gap))

REFERENCES

[All99] D. Allen, A. Aipperspach, D. Cox, N. Phan, S. Storino, "A 0.2um 1.8V SOI 550Mhz 64b PowerPC Microprocessor with Copper Interconnects," *ISSCC Dig. of Technical Papers,* p. 438, Feb. 1999.

[Ass96] F. Assaderaghi, G.G. Shahidi, M. Hargrove, K. Hathorn, H. Hovel, S. Kulkarni, W. Rausch, D. Sadana, D. Schepis, R. Schulz,D. Yee, J. Sun, R. Dennard, B. Davari, " History dependence of non-fully depleted (NFD) digital SOI circuits," *Proc. Symp. VLSI Technology*, p. 122, June 1996.

[Buc20] T. Buchholtz, A. Aipperspach, D. Cox, N. Phan, S. Storino, J. Storm, R. Williams, "A 660Mhz 64b SOI Processor with Cu Interconnects," *IEEE ISSCC Dig. of Technical Papers*, p. 88, Feb. 2000.

[Can99] M. Canada, C. Akrout, D. Cawthron, J. Corr, S. Geissler, R. Houle, P. Kartschoke, D. Kramer, P. McCormick, N. Rohrer, G. Salem, L. Warriner, "A 580MHz RISC Microprocesser in SOI," *ISSCC Dig. of Technical Papers*, p. 430, Feb. 1999.

[Cha97a] R. Chau, R. Arghavani, M. Alvani, D. Douglas, J. Greason, R. Green, S. Tyagi, J. Xu, P. Packan, S. Yu, C. Liang, "Scalability of Partially Depleted SOI Technology for Sub-0.25um Logic Applications," *IEEE IEDM Tech. Dig.*, p. 591, Dec. 1997.

[Cha97b] D. Chang, "Pragmatic and Reliable Device/Circuit Simulation for Design in Advanced Silicon-Based Technologies," Ph.D. Dissertation, University of Florida, Gainesville, 1997.

[Che87] J. Chen, T. Y. Chan, P. K. Ko, and C. Hu, "Subbreakdown Drain Leakage Current in MOSFET," *IEEE Electron Device Lett.*, vol. EDL-8, p. 515, Nov. 1987.

[Che96] W. Chen, Y. Taur, D. Sadana, K.A. Jenkins, J. Sun, S. Cohen, "Suppression of the SOI floating-body effects by linked-body device structure," *Symp. on VLSI Technology Dig. of Technical Papers*, p. 92, June 1996.

[Che97] V. M. C. Chen and J. C. S. Woo, "Tunneling Source-Body Contact for Partially-Depleted SOI MOSFET," vol. 44, p. 1143, July 1997.

[Chi98] M.-H. Chiang and J. G. Fossum, "UFSOI Model Parameter Evaluation: Process-Based Calibration," University of Florida SOI Group Report, http://www.soi.tec.ufl.edu/, November 1998.

[Col97] J. P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, 2nd Ed. Boston: Kluwer Academic Publishers, p. 139, 1997.

[Cri95] S. Cristoloveanu and S. Li, Electrical Characterization of SOI Matrials and Devices, Boston: Kluwer Academic Publishers, pp. 214-227, 1995.

[Cro95] S. Crowder, P. Rousseau, J. Snyder, J. Scott, P. Griffin, J. Plummer, "The effect of source/drain processing on the reverse short channel effect of deep sub-micron bulk and SOI NMOSFETs," *IEEE IEDM Tech. Dig.*, p. 427, Dec. 1995.

[Fos93] J.G. Fossum, P.-C. Yeh, and J.-Y. Choi, "Computer-aided performance assessment of fully depleted SOI CMOS VLSI circuits," *IEEE Trans. Electron Devices*, vol. ED-40, p. 598, Mar. 1993

[Fos97] J. G. Fossum, *SOISPICE-4 (Ver. 4.41) User's Guide,* University of Florida, Gainesville, Jan. 1997.

[Fos98] J.G. Fossum, M. M. Pelella, and S. Krishnan, "Scalable PD/SOI CMOS with Floating Bodies," *IEEE Electron Device Lett.*, vol. 19, p. 414, Nov. 1998.

[Fos99] J.G. Fossum, "UFSOI-5.0 User's Guide," University of Florida, Gainesville (http://www.soi.tec.ufl.edu/), Dec. 1999

[Gau95] J. Gautier, K. A. Jenkins, and J.Y.C. Sun, "Body Charge Related Transient Effects In Floating Body SOI MOSFET's," *IEEE IEDM Tech. Dig.*, p. 623, Dec. 1995.

[Gau97] J. Gautier, M.M. Pelella, and J.G. Fossum, "SOI Floating-Body,Device and Circuit Issues" (Invited Paper), *IEEE IEDM Tech. Dig.*, pp. 407, Dec. 1997.

[Hor96] M. Horiuchi and M. Tamura, "BESS: A Source Structure that Fully Suppresses the Floating-Body Effects in SOI CMOSFETs," *Tech. Digest IEEE Internat. Electron Devices Meeting,* p. 121, Dec. 1996.

[Hou98] T. Houston and S. Unnikrishnan, Proc. *IEEE Internat. SOI Conf.*, p. 121, Oct. 1998.

[Jen96] K.A. Jenkins, J.Y.-C. Sun, J. Gautier, "History Dependence of Output Characteristics of Silicon-on-Insulator (SOI) MOSFETs," *IEEE Electron Device Lett.*, vol. 17, p. 7, Jan. 1996.

[Kri96a] S. Krishnan and J. G. Fossum, "Compact Non-Local Modeling of Impact Ionization in SOI MOSFETs for Optimal CMOS Device/ Circuit Design," Solid-State Electronics , vol. 39, p. 661, May 1996.

[Kri96b] S. Krishnan, "Analysis and Modeling of Nonlocal and Dynamic Floating-Body Effects for Application in Scaled SOI CMOS Technology," Ph.D. Dissertation, University of Florida, Gainesville, 1996.

[Kri98a] S. Krishnan and J. G. Fossum, "Grasping SOI Floating-Body Effects" (Invited Paper), *IEEE Circuits and Devices Magazine*, vol. 14, No. 4, pp. 32-37, July 1998.

[Kri98b] S. Krishnan, Unpublished data on I-V measurements as a function of temperature.

[Kun96] K. S. Kundert, The Designer's Guide to SPICE & SPECTRE, 2nd Ed. Boston: Kluwer, 1996, p. 166.

[Leo99] E. Leobandung, E. Barth, M. Sherony, S.-H. Lo, R. Schutz, W. Chu, M. Khare, D. Sadana, D. Schepis, R. Boiam, J. Sleight, F. White, F. Assaderaghi, D. Moy, G. Biery, R. Goldblatt, T.-C. Chen, B. Davari, G. Shahidi, "High Performance 0.18mm SOI CMOS Technology," *IEEE IEDM Tech. Dig.*, p. 679, Dec. 1999.

[Lim84] H.K. Lim and J.G. Fossum, "Transient Drain Current and Propagation Delay in SOI CMOS," *IEEE Trans. on Electron Devices*, vol. ED-31, p. 1251, Sept. 1984.

[Mis00] K. Mistry, T. Ghani, M. Armstrong, S. Tyagi, P. Packan, S. Thompson, S. Yu, M. Bohr, "Scalability Revisited: 100nm PD-SOI Transistors and Implications for 50nm Devices," *Symp. on VLSI Technology Dig. of Technical Papers*, p. 204, June 2000.

[Nis97] A. Nishiyama, O. Arisumi, and M. Yoshimi, IEEE Trans. Electron Devices, vol. ED-44, p. 2187, Dec. 1997.

[Ohn98] T. Ohno, M. Takahashi, Y. Kado, and T. Tsuchiya, "Suppression of Parasitic Bipolar Action in Ultra-Thin-Film Fully-Depleted CMOS/ SIMOX Devices by Ar-Ion Implantation into Source/Drain Regions," *IEEE Trans. Electron Devices*, vol. 45, pp. 1071-1076, May 1998.

[Pel96] M.M. Pelella, J.G. Fossum, D. Suh, S. Krishnan, K.A. Jenkins,and M.J. Hargrove, "Low-Voltage Transient Bipolar Effect Induced by Dynamic Floating-Body Charging in Scaled PD/SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 17, p. 196, May 1996.

[Pel97] M.M. Pelella and R. Flaker, "Dynamic Effects in SOI Devices and Circuits" (Invited Paper), *Electrochemical Society Proc. Volume 97-23 (8th International Symposium on SOI Technology and Devices)*, p. 215, Aug. 1997.

[Pel99a] M. M. Pelella, C.-T. Chuang, Christophe Tretz, Brian W. Curran, and Mike G. Rosenfield, "Hysteresis in Floating-Body PD/SOI Circuits," *International Symposium on VLSI Technology, Systems, and Applications*, pp278-281, June 1999.

[Pel00] M.M. Pelella, Unpublished data on I-V measurements as a function of temperature.

[SIA99] Semiconductor Industry Association, The International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures, 1999.

[Suh94] D. Suh and J. G. Fossum, "Dynamic Floating-Body Instabilities in Partially Depleted SOI CMOS Circuits," *Tech. Digest IEEE Internat. Electron Devices Meeting*, p. 661, Dec. 1994.

[Suh95a] D. Suh and J. G. Fossum, "A Physical Charge-Based Model for Non-Fully Depleted SOI MOSFET's and Its Use in Assessing Floating-Body Effects in SOI CMOS Circuits," *IEEE Trans. Electron Devices*, vol. 42, p. 728, Apr. 1995.

[Suh95b] D. Suh, "Modeling of Non-Fully Depleted Silicon-on-Insulator MOSFETs, and Applications to High-Performance/Low Power ULSI Design," Ph.D. Dissertation, University of Florida, Gainesville, 1995.

[Sun87] J.Y.-C. Sun, Y. Taur, R. Dennard, and S. Klepner, *IEEE Trans. Electron Devices*, vol. ED-34, p. 19, Jan. 1987.

[Sze81] S. M. Sze, Physics of Semiconductor Devices, 2nd Ed., New York: John Wiley & Sons, 1981, p. 92

[Tau97] Y. Taur and E. Nowak, "CMOS Devices Below 0.1um: How High Will Performance Go?" *Tech. Digest IEEE Internat. Electron Devices Meeting*, p. 215, Dec. 1999.

[Tau98] Y. Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices, Cambridge University Press*, New York, 1998, p. 128.

[Tec97] Technology Modeling Associates, Inc., "TMA MEDICI Two-Dimensional Device Simulation Program," Palo Alto, CA, 1997.

[Wei93] H. F. Wei, N. M. Kalkhoran, F. Namavar, and J. E. Chung, "Improvement of Breakdown Voltage and Off-State Leakage in Ge-Implanted SOI n-MOSFETs," *IEEE IEDM Tech. Dig.*, p. 739, Dec. 1993.

[Wei95] A. Wei, M.J. Sherony, and D.A. Antoniadis, "Transient Behavior of the Kink Effect in Partially-Depleted SOI MOSFET's," *IEEE Electron Device Lett.*, vol. 16, p. 494, Nov. 1995.

[Wei98] A. Wei, M. Sherony, and D. Antoniadis, "Effect of Floating-Body Charge on SOI MOSFET Design," *IEEE Trans. Electron Devices*, vol. 45, p. 430, Feb. 1998.

[Wor98] G. O. Workman, J. G. Fossum, S. Krishnan, and M. M. Pelella, Jr., "Physical Modeling of Temperature Dependences of SOI CMOS Devices and Circuits Including Self-Heating", *IEEE Trans. Electron Devices*, vol. 45, p. 125, Jan. 1998.

[Wor99] G. O. Workman, "Physical Modeling and Analysis of Deep-Submicron Silicon-on-Insulator CMOS Devices and Circuits," Ph.D. Dissertation, University of Florida, Gainesville, 1999.

[Yeh95] P.-C. Yeh and J. G. Fossum, "Physical Subthreshold MOSFET Modeling Applied to Viable Design of Deep-Submicrometer Fully

Depleted SOI Low-Voltage CMOS Technology," *IEEE Trans. on Electron Devices*, vol. 42, p. 1605, Sept. 1995.

[Yos95] M. Yoshimi, A. Nishiyama, M. Terauchi, O. Arisumi, A. Murakoshi, Y. Ushiku, S. Takeno, and K. Suzuki, "Bandgap Engineering Technology for Suppressing the Substrate-Floating-Effect in 0.15mm SOI-MOSFETs," *Proc. IEEE Internat. SOI Conference*, pp. 80-81, October 1995.

[Yos97] M. Yoshimi, M. Terauchi, A. Nishiyama, O. Arisumi, A. Murakoshi, K. Matsuzawa, N. Shigyo, S. Takeno, M. Tomita, K. Suzuki, Y. Ushiku, and H. Tango," *IEEE Trans. Electron Devices*, vol. 44, p. 423, March 1997.

BIOGRAPHICAL SKETCH

Mario Michael Albert Pelella received the B.S. degree in electrical engineering from Clarkson College of Technology, Potsdam, NY, in 1983 and the M.S. degree in electrical engineering from Clarkson University, Potsdam, NY, in 1985. He is currently pursuing the Ph.D. degree in electrical and computer engineering at the University of Florida, Gainesville.

He joined IBM Microelectronics (General Technology) Division in 1985 where he worked on the device design and modeling of advanced high-speed bipolar transistor technologies. He was recently engaged in the device design and modeling of advanced Silicon-on-Insulator (SOI) CMOS technologies for IBM's, DARPA's and NCCOSC's Low Power Electronics programs. In 1996 he joined the Silicon Technology Innovation and Modeling group at the IBM T.J. Watson Research Center, Yorktown Heigths, NY, where he work on improvements to TCAD modeling tools and the analysis of floating-body effects in scaled PD/SOI technologies. His research and development interests include the device design, modeling and performance analysis of advanced Si Bipolar, SiGe HBT's, BiCMOS, Bulk-Si MOS, SOI CMOS technologies and Electrostatic Discharge (ESD) protection devices. He has received seven U.S. (2 pending) and 15 worldwide patents and is an author or coauthor of over 30 refereed publications.

Mr. Pelella was chairman of the IEEE Electron Device Society, Mid-Hudson Valley Chapter, 1995-1997, participated in the 1995-1996 and 1996-1997 National Technology Roadmap Committee for Semiconductor Compact Modeling, and served on the technical program committee of the IEEE International SOI Conference, 1996-1998. He was the recipient of the Semiconductor Research Corporation (SRC) outstanding industrial mentor award in 1996. He received a 1983-1984 TI Fellowship award and a 1998-1999 IBM Cooperative Fellowship award to pursue his academic research.

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